**←—Bit Number**

| 7(MSB) | 6 | 5 | 4 | 3 | 2 | 1 | 0(LSB) |
| --- | --- | --- | --- | --- | --- | --- | --- |

The value of ‘i’ in below assertions can be 0,1,2,3. Used ‘i’ to indicate the assertion is valid for 4 channels of DMA.

**Assertion Based Verification for DMA internal registers**

* If DACK[i] and HLDA signals are asserted,the current address register of the channel ‘i’ should Increment if bit number 5 of mode register is 0, it should decrement if bit number 5 of mode register is 1.

Assertion Failed:Current address register is not Incremented and Decremented during DMA transfer.

* If DACK[i], HLDA signals are asserted and the value in the word count register of the channel ‘i’ goes from 0 to FFFFH ,the terminal count should be generated and the bit number ‘i‘ of the status register should be set to 1.

The Current word count is not Decrementing and Could not check if Status register is updated when word count goes from 0 to FFFFH

* When reset or master clear instruction is asserted , the command register and status register should be 0.

Assertion Passed.

* If controller disable(bit number 2 of Command Register) is 1, the control signals HRQ,HLDA,DACK[i] should not be asserted.

Assertion Passed

* If DACK[i] is asserted and if its write transfer(bit number 3 and 2 of mode register is 0,1 respectively) , MEMW and IOR signals should be asserted in the next cycle.

Assertion Passed

* If DACK[i] is asserted and if its read transfer(bit number 3 and 2 of mode register is 1,0 respectively) , MEMR and IOW signals should be asserted in the next cycle.

Assertion Passed

* If DACK[i] is asserted ,word count is greater than 0 and 8 lower address bits(A7-A0) for channel ‘i’ is FFH , the ADSTB signal should be asserted.

Assertion Passed

* If DACK[i] is asserted, the current word count register for channel ‘i’ should be decremented in each clock cycle until the value in the word count register goes from 0 to FFFFH.

Assertion Failed: The current word count register is not decrementing.

* If DACK[i] is asserted and the value in the word count register of the channel ‘i’ goes from 0 to FFFFH ,the control signals HRQ,DACK and HLDA should be deasserted in the next cycle.

Assertion Passed