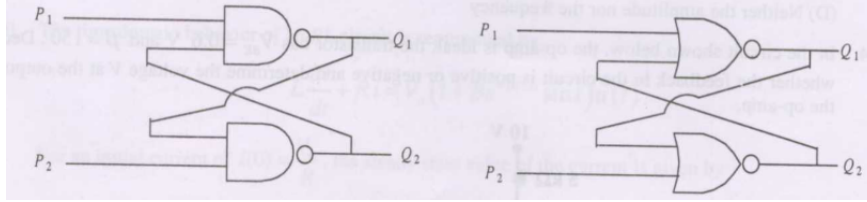


Q.38 Refer to the NAND and NOR latches shown in the figure below.



The inputs (P_1, P_2) for both the latches are first made (0, 1), and then, after a few seconds, made (1, 1). The corresponding stable outputs (Q_1, Q_2) are:

Options:

- (A) NAND: first (0, 1) then (0, 1); NOR: first (1, 0) then (0, 0)
- (B) NAND: first (1, 0) then (1, 0); NOR: first (1, 0) then (1, 0)
- (C) NAND: first (1, 0) then (1, 0); NOR: first (1, 0) then (0, 0)
- (D) NAND: first (1, 0) then (1, 1); NOR: first (0, 1) then (0, 1)

Answer and Explanation

Answer: (C)

NAND Latch:

- With inputs (0, 1): the latch stabilizes to $(Q_1, Q_2) = (1, 0)$
- With inputs (1, 1): it remains at (1, 0)

NOR Latch:

- With inputs (0, 1): the latch stabilizes to $(Q_1, Q_2) = (1, 0)$
- With inputs (1, 1): it transitions to (0, 0)

Final outputs:

- NAND Latch: $(1, 0) \rightarrow (1, 0)$
- NOR Latch: $(1, 0) \rightarrow (0, 0)$