Machine Learning Assisted Optimization of Hybrid Full Adder Based 4-bit Digital Comparator

***Abstract*-The full adder, a crucial component of the ALU and essentially a fundamental functional unit of the DSP and microprocessors, is used in this study to design the comparator. Low power circuits are now a primary concern in contemporary VLSI design. The power consumption comparisons of several 4 Bit Magnitude comparator designs are presented in this paper. The simplest arithmetic procedure for figuring out whether one number is bigger than, equal to, or less than another is comparison. The suggested approach makes use of a four-bit magnitude comparator that is full adder-based and built utilising full adders that are designed using various ways. A full adder with two XNOR gates and one multiplexer, a conventional full adder, a full adder based on a 2×1 multiplexer, a full adder based on a NAND gate, and an XOR-XNOR with multiplexer-based full adder are some of these techniques. In terms of power consumption, delay, and transistor count, the suggested Digital Magnitude Comparator with machine learning algorithm outperforms the current 4 Bit Magnitude comparator design. By using Cadence Tool's 45nm technology simulation, the comparison between several designs is computed. The most power-delay efficient design for low-power digital comparators is the XNOR-MUX.**

Keywords— Low Power VLSI Design, 4-Bit Magnitude Comparator, Full Adder Based Comparator, Digital Comparator

I. INTRODUCTION

Full adders (FAs) are fundamental arithmetic units extensively employed in digital signal processors (DSPs), image and video processing systems, and application-specific integrated circuits (ASICs), where efficient computation of convolution and filtering operations is essential [1], [2]. With the continued scaling of transistors and the proliferation of portable electronic devices, the design of low-power and high-performance arithmetic circuits has become increasingly critical [3], [4]. Studies report that up to one-third of the total power consumption in high-performance microprocessors is due to arithmetic units, underscoring the importance of optimized FA design [5].Traditional full adders implemented using complementary CMOS logic provide full output swing and high noise immunity but suffer from high input capacitance and large transistor count (typically 28 transistors), which limit their speed and area efficiency [6], [7]. To address these limitations, hybrid full adder architectures have been proposed, decomposing the design into distinct modules—primarily XOR-XNOR generation, SUM, and CARRY units—thereby allowing localized optimization and reduction of internal power-dissipating nodes [8], [9], [10]. The performance of hybrid FAs is largely determined by the efficiency of the XOR-XNOR block. Several XOR-XNOR designs have been introduced to balance speed, power, and area, with recent efforts focusing on six-transistor structures that utilize complementary feedback mechanisms to restore logic levels for identical inputs (00 or 11) [11], [12], [13]. Although compact, these designs exhibit increased delay due to a two-step logic transition. To overcome this, enhancements using additional pMOS and nMOS transistors at the output nodes have been proposed, achieving full swing outputs and improved driving capability with minimal parasitic effects introduced by the cross-coupled structure [14], [15].

To address this, improved structures incorporating additional pMOS and nMOS transistors at the XOR and XNOR outputs have been developed, providing enhanced drive strength and ensuring full-swing outputs with minimal propagation delay [16], [17]. The inclusion of cross-coupled transistor pairs contributes to signal restoration but also introduces parasitic capacitances that must be carefully managed to avoid performance degradation in high-frequency applications [18]. Furthermore, comparative studies across different logic styles indicate that hybrid designs consistently outperform traditional CMOS implementations in terms of power-delay product (PDP), making them ideal for integration in power-constrained VLSI systems such as biomedical devices, edge AI processors, and mobile SoCs [19]. These advancements in low-power FA design not only enhance the energy efficiency and speed of arithmetic blocks but also contribute significantly to the scalability and reliability of modern digital systems. In conclusion, In this work, a low-power and high-performance full adder design based on an optimized NAND Gate based circuit has been presented. The proposed design achieves full output swing, reduced delay, and improved driving capability with a minimal transistor count. These features make it suitable for energy-efficient VLSI applications, especially in portable and high-speed systems.

This work is organized in different sections. Introduction explains an efficient full adder-based magnitude comparator in Section I. Section II the Literature Review follows, summarizing existing and reduction methods and their limitations. The Project methodology and internal blocks explained and presented in section III. The Simulation and Analysis section presents the simulation setup, parameters measured, and analysis of results are presented in Section IV. Section V concludes with a Conclusion and Future Work section summarizing findings and suggesting areas for further research.

II. RELATED WORK

DSCH-3.1 is used to create the schematics and simulate their behaviour. Verilog-based netlist files are used to generate the layout of simulated circuits, which are then simulated in Microwind 3.1 to examine the comparators' performance for the two design styles at 45 nm and 32 nm CMOS technology [20]. These various digital circuit ideas are used in the design and implementation of a 4-bit comparator based on the addition principle of 2's complement. Majority Gate Logic (MGL), Mirror Adder Logic (MAL), Complementary Pass Transistor Logic (CPL), Transmission Gate Logic (TGL), and Gate Diffusion Input Logic (GDI) were used in the design and implementation in order to examine how well they performed under various demanding temperature, power

supply, and other situations. Using the Cadence Spectre Simulator and a 1.8 V power source, the circuits are implemented in the UMC 180 nm process [21]. This paper proposes a hybrid design technique to create a two-bit Magnitude Comparator (MC). Three distinct logic techniques make up the hybrid design: (a) conventional static CMOS logic (C-CMOS logic), (b) transmission gate logic (TGL), and (c) pass transistor logic (PTL). Additionally, the design's low power consumption makes it ideal for portable devices that need low power usage [22]. DSCH 3.1 and Microwind 3.1 on 120nm have been used to construct and simulate the suggested 4-bit GDI comparator. According to the results, the suggested 4-bit comparator design's area using 120nm technology is 1320.3μm2. The suggested 4-bit GDI comparator uses 13.739μW of power at BSIM-4 when the input supply voltage is set to 1.2V. When compared to the PTL 4-bit comparator, the suggested GDI 4-bit comparator has demonstrated improvements of 6.3% in area and 69.42% in power at 1.2V [23]. The suggested design has been compared against the current two-bit binary magnitude comparator architecture in order to assess design viability. The simulation results showed that the suggested design had a much lower average power consumption of 9.865 μ W, a delay of 0.193 ns, and a power delay product of 1.904 fJ compared to the two-bit magnitude comparator designs that were currently in use [24]. Compared to a standard CMOS magnitude comparator, the proposed GDI technique-based magnitude comparator has the advantage of consuming less power in relation to various design parameters; also, it covers less on-chip area because fewer transistors are needed in the circuit design. Tanner EDA Tool version 12.6 is used to design and simulate both circuits at 45 nm manufacturing technology [25]. In the reviewed literature, machine learning (ML)-based optimization techniques have not been explored for comparator design. All existing approaches rely on traditional logic design methods, analytical optimization, or manual logic selection. The absence of ML-based optimization in existing comparator design studies limits the potential for automated, scalable, and intelligent design decisions, especially in advanced nodes and complex systems. Integrating ML techniques can enhance design efficiency, reduce time-to-market, and result in better performance under real-world constraints.

III. Propsed Work: Digital Magnitude Comparator Using Machine Learning Algorithm

Designing a 4-bit magnitude comparator using a full adder-based approach involves implementing and evaluating five different logic styles to determine the most efficient design. This block diagram shows in fig.1 is Digital Magnitude Comparator using machine learning algorithm, a smart automated loop where ML selects comparator design parameters, simulates them, and improves the design with each iteration. It reduces manual tuning and helps achieve high-performance, low-power comparator circuits faster. The comparator, which identifies whether one 4-bit number is greater than, equal to, or less than another, is constructed using full adders designed with different techniques shown in fig.2.. These methods include a full adder using two XNOR gates and one multiplexer, a traditional full adder, a 2×1 multiplexer-based full adder, a NAND gate-based full adder, and a XOR-XNOR with multiplexer-based full adder.

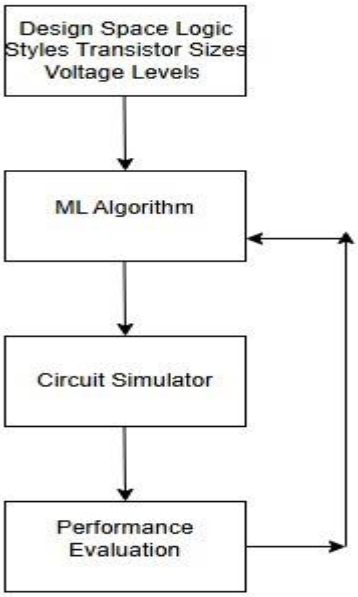

Fig. 1. Digital Magnitude Comparator using machine learning algorithm

The objective is to use intelligent sampling and feedback to automate and optimise critical design decisions including logic style, transistor sizing, and supply voltage in order to include Machine Learning (Bayesian Optimisation) into the design of a complete adder-based digital comparator. Using a cadence tool, the Bayesian Optimisation methodology simulates the power, delay, and area of a few configurations that are randomly selected. The Power-Delay Product (PDP) is estimated from design parameters using a Gaussian Process model. Performance measures are calculated by simulating a certain complete adder-based comparator architecture. New data is added to the surrogate model, and this cycle is repeated until convergence or a predetermined number of iterations. The simulation of these designs is performed using the 45nm CMOS technology node in the Cadence Virtuoso tool, where key performance metrics such as power consumption, transistor count, and propagation delay are analyzed. Among the five designs, the NAND gate-based full adder proves to be the most efficient, offering the lowest power consumption of 106 μW, a moderate transistor count of 196, and a low propagation delay of 35 ps. These results highlight the superiority of the NAND gate-based approach in achieving a balance between power efficiency, circuit complexity, and speed. This study underscores the importance of transistor-level optimization in modern VLSI design, demonstrating that the NAND gate-based full adder is a viable solution for energy-efficient applications.

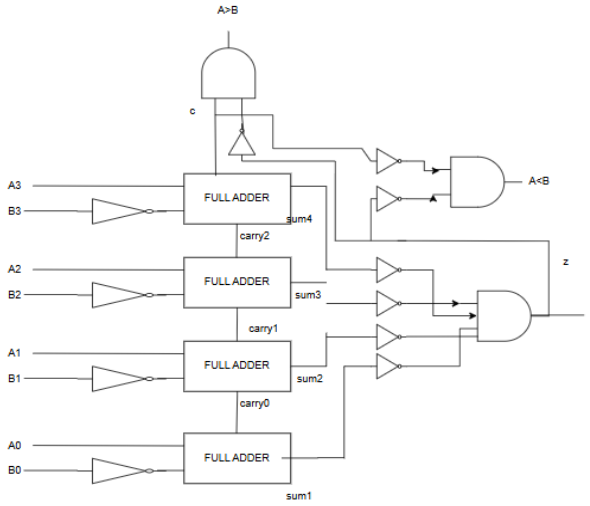

Fig. 2. 4 Bit Digital Magnitude Comparator

This circuit is a 4-bit magnitude comparator designed using full adders, inverters, and basic logic gates shown in fig.2. It compares two 4-bit binary numbers, A and B, by performing a subtraction operation using the 2's complement method. Each bit of B is inverted and then added to the corresponding bit of A using four full adder blocks. A logic high (1) is provided as the initial carry-in to the least significant full adder to complete the 2's complement addition. The outputs from the adders are then used to determine the relationship between A and B. If the final carry-out is high, and the result is non-zero, the circuit identifies A > B. If all sum outputs are zero, the circuit detects A = B. The A < B condition is derived by using logic that negates both A > B and A = B. This design efficiently utilizes arithmetic logic to perform comparison operations, making it compact, reusable, and suitable for integration in digital processors and VLSI systems.

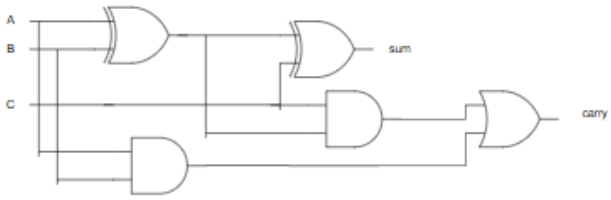

Fig. 3. Traditional Full adder

Full Adder circuit built using basic logic gates like XOR, AND, and OR shown in fig.3. A full adder is a fundamental digital circuit used in arithmetic operations to add three input bits (A, B, and Cin) and produce a sum and carry output

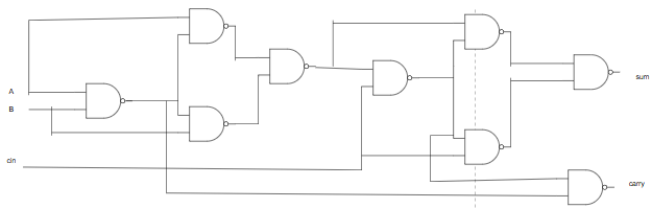

Fig. 4. Full adder using Universal Gates

Full Adder circuit built using only NAND gates , which are universal logic gates shown in fig.4. It takes three inputs (A, B, and Cin) and produces two outputs: Sum (S) and Carry-out (Cout). Using only NAND gates makes the design simple, cost-effective, and easy to implement in digital integrated circuits.

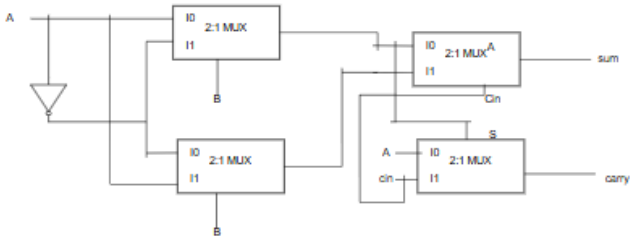

Fig. 5. Full adder using Multiplexer

Fig.5 represents a full adder implemented using only 2:1 multiplexers (MUX) and one NOT gate. It performs binary addition of three inputs: A, B, and Cin (carry-in), and generates two outputs: Sum and Cout (carry-out).

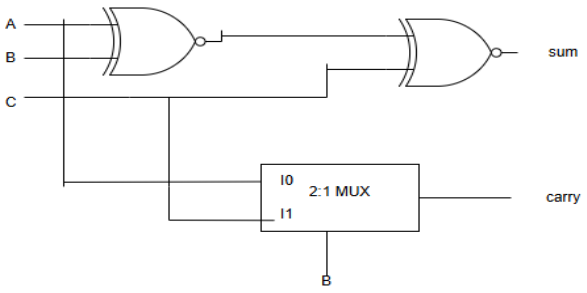

Fig. 6. Full Adder Using 2 Xnor 1 multiplexer

Hybrid full adder circuit that combines XOR gates and a 2:1 multiplexer shown in fig.6 to generate the sum and carry outputs efficiently. The sum is produced using two cascaded XOR gates, implementing the logic Sum = A ⊕ B ⊕ Cin. The intermediate XOR output is also used as the select line for the multiplexer, which determines the carry-out. The multiplexer inputs are derived from A·B and Cin, effectively implementing the carry logic Cout = A·B + (A ⊕ B)·Cin.

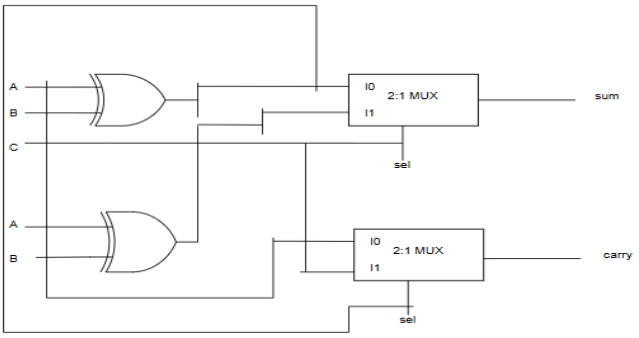

Fig. 7. Full adder using Xor and 2 multiplexer

A compact full-adder circuit designed using two XORgates and two 2:1 multiplexers shown in fig.7. The circuit efficiently

utilizes the output of the XOR gates as select lines for the multiplexers, reducing the need for multiple logic gates

IV. SIMULATION RESULTS

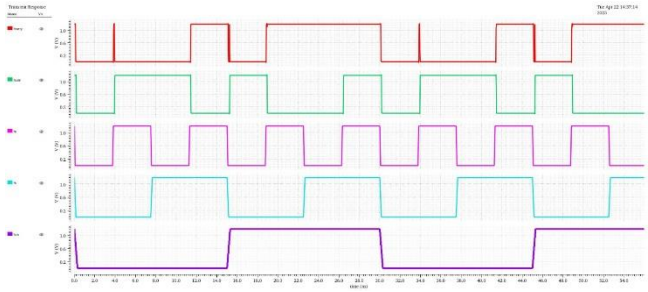

Fig.8. Full Adder Waveform

Fig.8 illustrates the operation of a full adder circuit by displaying the timing relationships between its inputs and outputs. In the image, the top three traces represent the input signals—typically labeled as A, B, and Carry-in (Cin)—which cycle through all possible binary combinations. The lower traces correspond to the outputs: Sum and Carry-out (Cout). As the input signals change, the Sum and Cout outputs respond according to the full adder's logic equations: the Sum output is high when an odd number of inputs are high, while the Carry-out is high when at least two of the inputs are high. The diagram demonstrates that for each unique combination of inputs, the outputs transition as expected, verifying the correct functionality of the full adder circuit across all input states.

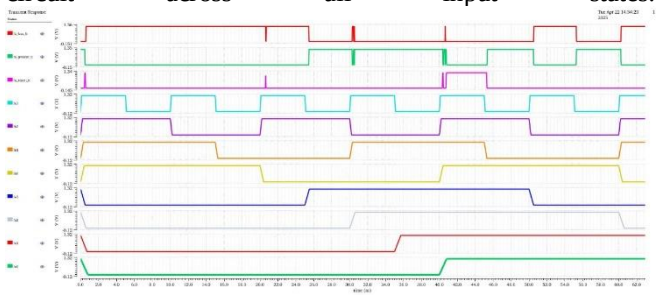

Fig.9. 4 Bit Digital Comparator Waveform

Fig.9 represent the 4-bit comparator, based on the various labeled signals. Each horizontal trace represents the voltage level of a specific signal over time, with the x-axis indicating time in nanoseconds. The signals labeled as A0, A1, A2,A3, B0, B1, and B2, B3 likely correspond to the individual bits of two 4-bit binary numbers (A and B). The other traces, such as "A>B" "A<B," and "A=B" appear to represent output conditions or intermediate results, such as which input is greater or the result of a comparison or addition. As the input bits change state at different times, the output signals respond accordingly, demonstrating the circuit's correct operation..

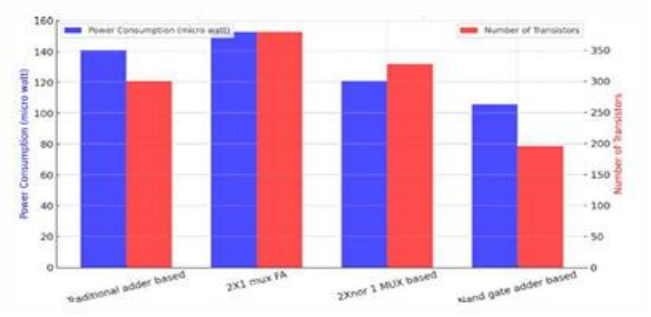

Fig.10. Performance Comparison of Full Adder-Based Comparators: Power Consumption vs. Transistor Count

The chart fig.10.compares four adder designs based on power consumption and transistor count. The 2x1 MUX full adder uses the most power and transistors, while the NAND gate adder is the most efficient, with the lowest power consumption and fewest transistors. Traditional and 2Xnor 1 MUX based adders fall in between. Overall, NAND gate adders offer better performance for low-power, compact designs.

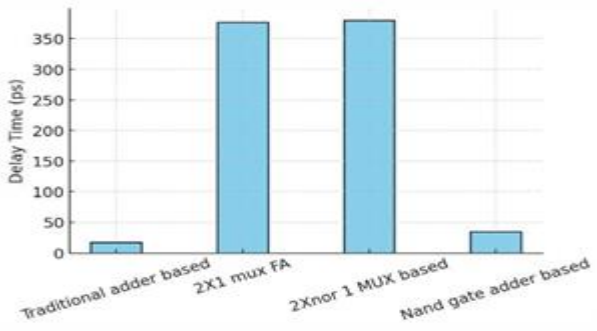

Fig 11. Delay Comparison of Full Adder Based Comparators

Delay comparison of full adder-based comparator is shown in fig.11 observed that traditional adder based comparator delay is less compared to the other designs in proposed work These simulation results compare five distinct complete adder architectures with random variations in supply voltage and transistor width. Figure 12 displays the Power-Delay Product (PDP) variance for each complete adder method over several random settings (transistor width and VDD Better and more reliable performance is indicated by the smaller box and lower median of the XNOR-MUX Full Adder. Higher medians and a wider spread are displayed by the 2×1 MUX-Based and Traditional Full Adders, suggesting greater variation and higher average PDP. XOR-XNOR-MUX performs reasonably well despite having a little bit more fluctuation. The NAND-Based design exhibits a moderate level of performance and stability.

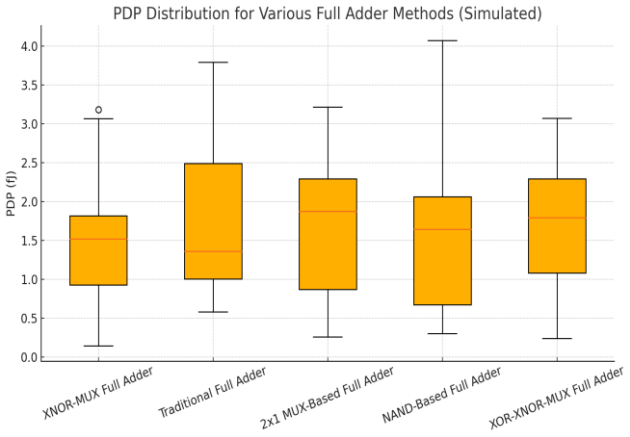

Fig 12. Power delay product (PDP) distribution for various full adder methods

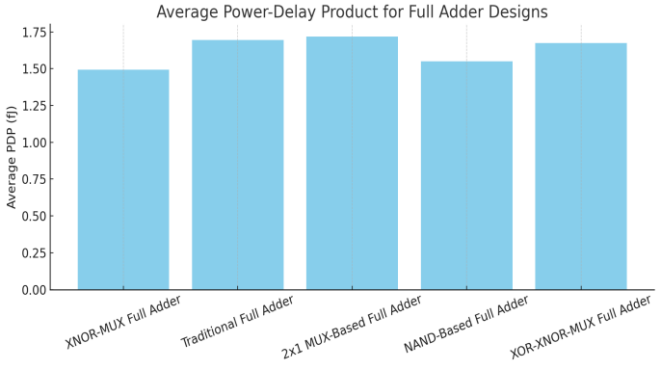

Fig 13. Average Power delay product (PDP) distribution for various full adder methods

compares the average PDP for each full adder design in fig. 13 across all evaluated configurations. The simulation's most energy-efficient option is the XNOR-MUX Full Adder (~1.49 fJ). Under the identical test settings, the 2×1 MUX-Based Full Adder (~1.72 fJ) is less optimum. PDPs for the others (Traditional, NAND, XOR-XNOR-MUX) range from about 1.55 to 1.69 fJ. The most power-delay efficient design for low-power digital comparators is the XNOR-MUX. When designing a full adder-based comparator circuit, use these insights to help choose the logic type, particularly for energy-sensitive applications.

TABLE I. COMPARISON BETWEEN PROPOSED AND EXISTING WORKS

S. No	Proposed design Type	Technology(nm)	Power Consumption (nW)	Supply voltage (V)	Delay Time(ps)
1	Traditional Full adder	45	141	0.8	17.6
2	Full adder using 2X1 multiplexer	45	153	0.8	377
3	FA_2xnor,1 Mux	45	121	0.8	380
4	FA_NandGate	45	106	0.8	35
	Existing works				
5	[24]	90	9865	1	193
6	[23]	120	13739	1.2	-
7	[22]	90	7792	-	192

Table 1 shows that proposed designs at 45 nm are significantly more power-efficient than existing designs at 90 nm and 120 nm. NAND gate-based full adders offer the best trade-off between acceptable latency and minimum power consumption. Fastest (lowest delay) in a traditional full adder. The suggested designs using machine algorithms are perfect for contemporary, low-power VLSI systems because the current designs are antiquated and use a lot more power.

V. CONCLUSION

The Proposed work, a 4-bit magnitude comparator has been effectively designed and evaluated using multiple full adder logic styles to identify the most efficient architecture in terms of power, area, and speed. The study showcases the critical role that optimized full adder circuits play in the performance of arithmetic operations within modern VLSI systems. Through extensive simulations using the Cadence Virtuoso tool on a 45nm technology node, five different full adder- based comparator architectures were implemented and analyzed. Among these, the NAND gate-based full adder emerged as the most optimal solution, demonstrating the lowest power consumption of 106 µW, a moderate transistor count of 196, and a minimal propagation delay of 35 ps. These results confirm that the NAND-based approach provides a well-balanced trade-off among key design metrics, making it highly suitable for energy-efficient and high-performance digital systems. The XNOR-MUX design is the most power-delay efficient for use in low-power digital comparators. Use these insights to guide logic style selection during full adder-based comparator circuit design, especially for energy-critical applications. Overall, the work successfully validates that targeted transistor-level optimizations can significantly enhance the operational efficiency of core arithmetic blocks like comparators in VLSI design.

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