ages & Libraries

Design

Verilog

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Enable TL-Verilog

Enable Easier UVM

Enable VUnit

Tools & Simulators

Examples

```
1  ////////////////////////////////////////////////////
2
3  `include "uvm_macros.svh"
4  import uvm_pkg::*;
5
6
7  class comp1 extends uvm_component;
8    `uvm_component_utils(comp1)
9
10   int data1 = 0;
11
12   function new(input string path = "comp1", uvm_component parent = null);
13     super.new(path,parent);
14   endfunction
15
16   virtual function void build_phase(uvm_phase phase);
17   super.build_phase(phase);
18     if(!uvm_config_db#(int)::get(null,"uvm_test_top","data",data1))
19       `uvm_error("comp1","Unable to access Interface");
20   endfunction
21
22    virtual task run_phase(uvm_phase phase);
23      phase.raise_objection(this);
24      `uvm_info("comp1", $sformatf("Data rcvd comp1 : %0d
                                                    VM_NONE);
25      phase.drop_objection(this);
26    endtask
```

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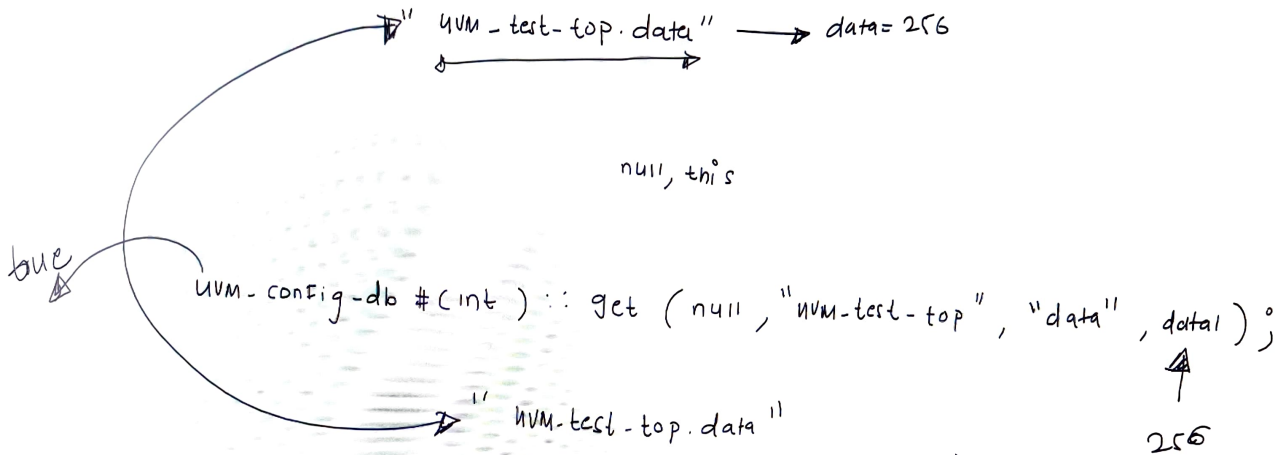
" uvm_test_top.data" → data=256
null, this
bue
uvm_config_db #(int)::get(null, "uvm_test_top", "data", data1);
" uvm_test_top.data "
256