Sathvik Swaminathan

sathvikswaminathan@gmail.com | | linkedIn/sathvik-swaminathan-50b424178 | github/sathvikswaminathan

EDUCATION

B.E. Electronics and Communication Engineering; M.Sc. Physics Hyderabad, India | Aug. 2019 – July 2024
Birla Institute of Technology and Science, Pilani

TECHNICAL BACKGROUND

Interests: Computer Architecture/Systems for Performance and Security, Systems for Machine Learning, Memory Optimization
Relevant Courses: Computer Architecture, Operating Systems, Computer Networks, Microprocessors, Digital Design, Computer Programming, Device Physics, Microelectronic Circuits, Digital VLSI Design
Languages: C, C++, RISC-V assembly, x86 assembly, Verilog, Python
Tools: Git, Synopsys (VCS, DVE), Xilinx Vivado, QEMU, perf, Intel Vtune, PyTorch

PUBLICATIONS

- TierTrain: Proactive Memory Tiering for CPU-based DNN Training
  Proceedings of the ACM SIGPLAN International Symposium on Memory Management (ISMM), 2025.
  Sathvik Swaminathan, Sandeep Kumar, Aravinda Prasad, Sreenivas Subramoney (Intel Labs)

PATENTS

- Context-aware Memory Tiering for Optimizing Xeon-based AI DNN Training

EXPERIENCE

INTEL LABS | Research Scientist — Bangalore | July 2024 – Present

- Performed workload analysis, characterized memory access patterns and profiled DNN Training workloads on Intel Xeon CPUs.
- Designed software to manage memory across in a tiered memory (DRAM, Optane / CXL) architecture for DNN training workloads.
- Outperformed SOTA memory tiering techniques by 35–84%.
- Patent granted and paper published at ISMM '25
- Profiled LLM Inference workloads on Intel Xeon CPUs and identified bottlenecks.
- Designed an algorithm to manage KV cache and Weights across memory tiers to maximize system memory bandwidth.
- To be submitted to ASPLOS '26.

INTEL LABS | Architecture Research Intern — Bangalore | Aug 2023 – June 2024

- Interned at the Processor Architecture Research Lab.
- Conducted a comprehensive performance analysis of Graph Neural Network (GNN) workloads across multiple frameworks using various tools such as *perf*, Intel Vtune, etc.
- Analyzed the impact of data migration of various tensors across different tiers (fast and slow memory) in NUMA systems.

NVIDIA | ASIC Design Intern — Bangalore | May 2023 – July 2023

- Interned in the SoC Verification team.
- Worked on modifying a verification framework to allow for easier integration during SoC/cluster verification.

INTEL LABS | Architecture Research Intern — Bangalore | Feb 2023 – April 2023

- Interned in the Processor Architecture Research Lab.

- Hacked into the Ligra framework and analysed the impact of relocation of data on performance in a heterogeneous memory system.

KU LEUVEN | Informal Research Assistant (RA) Remote | July 2022 – Jan 2023

- Performed a literature review on Capability-based systems with a specific focus on the CHERI architecture.
- Contributed to QEMU to extend the CHERI-RISCV ISA in order to support a secure calling convention.

IIT BOMBAY | Informal Research Assistant (RA) Remote | June 2022 – January 2023

- Worked on designing a covert channel by exploiting the relative order of thread execution.

ABCR LABS | Digital Design Engineer Intern Remote | Feb 2022 – July 2022

- Developed a Python script to automate the functional verification of the Shakti E-Class Processor.
- Designed and simulated the architecture of a SPI programmer in System Verilog.

BITS PILANI | Research Assistant (RA) Hyderabad | Aug 2021 – Dec 2021

- Verified the functionality of a Network on Chip with 2 RISC-V cores.
- Extended the current prototype to support transmission of multiple packets between RISC-V cores.

PERSONAL PROJECTS

THRESHOLDLESS COVERT CHANNEL Computer Architecture, Operating Systems, C
Implemented and tested a cache-based covert channel which doesn't require threshold calibration to distinguish between a cache-hit and cache-miss.

RISC-V PROCESSORS Digital Electronics, Computer Architecture, Verilog
Designed a single cycle and 5 stage pipelined processor based on the RV32I Base Integer Instruction Set. Resolved Data and Control Hazards using forwarding and bubbles.

VIRTUAL MEMORY SIMULATOR Computer Architecture, Operating Systems, C
Developed a virtual memory simulator in C which uses the clock sweep algorithm for page replacement and TLB eviction. It provides statistics such as number of TLB hits, pagefaults, and average memory access time for a given program.

SHELL Operating Systems, C
Developed a shell program in C which supports 6 built-in commands, reaps jobs after termination, and can run jobs in the background or foreground.

16 BIT COMPUTER Digital Electronics, Computer Architecture, Python
Designed a 16 bit computer in a HDL based on the Harvard Architecture. Developed an Assembler for the same in Python

UART Digital Design, Verilog
Designed a UART Core equipped with FIFO buffers at the TX and RX ends in Verilog.

EXTRACURRICULARS

NSM-CAWS 2021 Winter School
The goal of NSM-Computer Architecture Winter School (NSM-CAWS 2021) is to provide an introduction to basic and advanced topics in Computer Architecture to undergraduate students who have undergone basic training in computer organization.