Sathwika Bavikadi

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Experience

Tenure Track Assistant Professor **From August 2024**
at Rochester Institute of Technology, *Rochester, New York, USA*

- Teaching Graduate Level and Undergraduate Level Courses in Electrical and Computer Engineering Department
- Research in the areas of Computer architecture, Security, Machine Learning, Artificial Intelligence

Graduate Research Assistant
at George Mason University, *Fairfax,Virginia, USA*

- Developed ML algorithms like CNN, DNN, and Transformer models to implement on hardware accelerators
- Worked on model optimization of CNNs for tiny memory platforms like non-von Neumann computing architectures and achieved 98% accuracy
- For AlexNet inference at a nearly 13× faster rate and 125× more efficiency compared to state-of-the-art GPU
- Worked on developing a new computing system to enable ML acceleration.
- Published 16 papers (5 journals, 11 conferences) and a Patent.

Graduate Teaching Assistant
at George Mason University, *Fairfax,Virginia, USA*

- Instructor for courses like Digital System Design with VHDL, FPGA Design with VHDL, Computer Architecture
- Instructor for Learning from data, Big data Technologies helped in designing the Machine Learning based assignment

Visiting Research Assistant **May 2021 to August 2021**
at University of Southern California- Information Sciences Institute *Arlington, Virginia, USA*

- Working on implementing ML on Side-channel analysis (SCA)
- Generating of power traces using FPGAs like Artix, Virtex board using chipwhisperer platform for SCA

PD Baseband Developer **August 2017 to February 2020**
at Ericsson *Lund, Sweden*

- Mainly working on the L1 Physical layer and in Uplink section
- Implementation of 5G baseband architecture, functionality and features. 5G feature systemization and participate in pre-studies as needed

Summer Internship **June 2016 to August 2016**
at Defence Electronics Research Laboratory (DLRL) *Hyderabad, India*

Engineering Trainee **June 2015 to July 2015**
at Advance Training Institute Electronics & Process Instrumentation (ATI-EPI) *Hyderabad, India*

Education

Doctor of Philosophy (Ph.D.) in Electrical and Computer Engineering **January 2020 - July 2024**
George Mason University, Fairfax, Virginia, USA

Thesis: Machine Learning for Hardware Accelerator Design

Master of Science in Electrical Engineering Signal Processing **January 2016 - January 2018**
Blekinge Institute of Technology, Karlskrona, Sweden

Thesis: Estimation and Correction of the Distortion in Forensic Image due to Rotation in the Photo Camera

Bachelor of Technology in Electronics and Communications Engineering **September 2012 - January 2018**
Jawaharlal Nehru Technological University, Kukatpally, Hyderabad, India

Thesis: Face Recognition using PCA Algorithm

Technical Skills

Programming Languages: 80x86 Assembler, C/C++, Python, VHDL, Verilog, CUDA
Scientific softwares: MATLAB, Simulink, Scilab, Lab-VIEW
ML libraries and frameworks: TensorFlow, Keras, PyTorch, Caffe, OpenCV, scikit-learn, numpy, pandas
Software and IDE Tools: Visual Studio, PyCharm, Spyder, Jupyter Notebook, Eclipse, Visual DSP++, Xilinx
Office softwares: Microsoft Office, Libre Office, LaTeX, DocBook
Operating system: iOs, Linux, Windows, Unix

Projects

• GPU Accelerated Beam-forming, • IoT-based indoor human-presence detection using PIR sensor using Raspberry Pi, • Chirpbased acoustic radar, • Image enhancement and restoration using signal processing techniques, • Secured transmission of Image using run-length encoding, • Fetal heartbeat recognition, • Line controlled robot using Arduino.

Selected Publications

Patents:

1. Heterogeneous multi-functional reconfigurable processing-in memory architecture. Pending: 2024-2-14
2. Look-up table containing processor-in-memory cluster for data-intensive applications. https://patents.google.com/patent/US20220326958A1/en. US Patent No.: US11775312B2, Published: 2023-10-03

Journal Articles:

1. **Sathwika Bavikadi**, Purab Ranjan Sutradhar, Mark Indovina, Amlan Ganguly, and Sai Manoj Pudukotai Dinakarrao. Reapprox-pim: Reconfigurable approximate look-up-table (lut)-based processing-in- memory (pim) deep learning accelerator. In *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2023 (IF= 2.9)*
2. Purab Ranjan Sutradhar, **Bavikadi, Sathwika**, Sai Manoj Pudukotai Dinakarrao, Mark A. Indovina, and Amlan Ganguly. 3dl-pim: A look-up table oriented programmable processing in memory architecture based on the 3-d stacked memory for data-intensive applications. *IEEE Transactions on Emerging Topics in Computing ((IF = 5.08)*, pages 1–13, 2023
3. **Bavikadi, Sathwika**, Abhijitt Dhavlle, Amlan Ganguly, Anand Haridass, Hagar Hendy, Cory Merkel, Vijay Janapa Reddi, Purab Ranjan Sutradhar, Arun Joseph, and Sai Manoj Pudukotai Dinakarrao. A survey on machine learning accelerators and evolutionary hardware platforms. *IEEE Design & Test (IF = 2.223)*, 39(3):91–116, 2022
4. P. R. Sutradhar, **S. Bavikadi**, M. Connolly, S. K. Prajapati, M. A. Indovina, S. M. Pudukotaidinakarrao, and A. Ganguly. Look-up-table based processing-in-memory architecture with programmable precision-scaling for deep learning applications. *IEEE Transactions on Parallel and Distributed Systems (IF= 4.3)*, 2021
5. P. R. Sutradhar, M. Connolly, **S. Bavikadi**, S. M. Pudukotai Dinakarrao, M. A. Indovina, and A. Ganguly. pPIM: A programmable processor-in-memory architecture with precision-scaling for deep learning. *IEEE Computer Architecture Letters (IF= 2.33)*, 2020

Conference Papers:

1. **Sathwika Bavikadi**, Sanket Shukla, and Sai Manoj Pudukotai Dinakarrao. Energy harvesting, iot, processing in memory, neural networks, low-power. In *Proceedings of the Great Lakes Symposium on VLSI 2024*. Association for Computing Machinery, 2024
2. **Sathwika Bavikadi**, Purab Ranjan Sutradhar, Mark Indovina, Amlan Ganguly, and Sai Manoj Pudukotai Dinakarrao. Reconfigurable processing-in-memory architecture for data-intensive applications. In *IEEE International Conference on VLSI Design (VLSID), 2024*
3. **Sathwika Bavikadi,** Sreenitha Kasurapu and Sai Manoj Pudukotai Dinakarrao. Processing-in-memory architecture with precision-scaling for malware detection. In *IEEE International Conference on VLSI Design (VLSID), 2024*
4. Purab Ranjan Sutradhar, **Bavikadi, Sathwika**, Mark Indovina, Sai Manoj Pudukotai Dinakarrao, and Amlan Ganguly. Flutpim: A look-up table-based processing in memory architecture with floating-point computation support for deep learning applications. In *Proceedings of the Great Lakes Symposium on VLSI 2023*, GLSVLSI '23, page 207–211, New York, NY, USA, 2023. Association for Computing Machinery
5. **Bavikadi, Sathwika**, Purab Ranjan Sutradhar, Amlan Ganguly, and Sai Manoj Pudukotai Dinakarrao. Heterogeneous multi-functional look-up-table-based processing-in-memory architecture for deep learning acceleration. In *2023 24th International Symposium on Quality Electronic Design (ISQED)*, pages 1–8, 2023
6. Raghul Saravanan, **Bavikadi, Sathwika**, Shubham Rai, Akash Kumar, and Sai Manoj Pudukotai Dinakarrao. Reconfigurable fet approximate computing-based accelerator for deep learning applications. In *2023 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 1–5, 2023
7. Katherine Mercado, **Bavikadi, Sathwika**, and Sai Manoj PD. Coarse-grained high-speed reconfigurable array-based approximate accelerator for deep learning applications. In *2023 57th Annual Conference on Information Sciences and Systems (CISS)*, pages 1–6. IEEE, 2023
8. Shiyi Liu, **Bavikadi, Sathwika**, Tanmoy Sen, Haiying Shen, Purab Ranjan Sutradhar, Amlan Ganguly, Sai Manoj Pudukotai Dinakarrao, and Brian L Smith. Accelerating adversarial attack using process-in-memory architecture. In *2022 18th International Conference on Mobility, Sensing and Networking (MSN)*, pages 325–330. IEEE Computer Society, 2022
9. **Bavikadi, Sathwika**, Purab Ranjan Sutradhar, Mark A. Indovina, Amlan Ganguly, and Sai Manoj Pudukotai Dinakarrao. Polar: Performance-aware on-device learning capable programmable processing-in-memory architecture for low-power ml applications. pages 889–898, 2022
10. **Bavikadi, Sathwika**, Purab Ranjan Sutradhar, Amlan Ganguly, and Sai Manoj Pudukotai Dinakarrao. upim: Performance-aware online learning capable processing-in-memory. In *2021 IEEE 3rd International Conference on Artificial Intelligence Circuits and Systems (AICAS)*
11. **Bavikadi, Sathwika**, Purab Ranjan Sutradhar, Khaled N. Khasawneh, Amlan Ganguly, and Sai Manoj Pudukotai Dinakarrao. A review of in-memory computing architectures for machine learning applications. GLSVLSI '20

Professional Activites

Books Writing Assistance: Machine Learning for Computer Scientists and Data Analysts from an Applied Perspective.

Contributed/Invited talks:
- Selected to present my PhD work at the 2024 ECEDHA Annual Conference, Tuscan, Arizona (March 2024).
- Giving an ECE seminar on my PHD work at George Mason University, Virginia (Feb 2024).
- Invited guest lecture at Indian Institute of Technology, Hyderabad,India (IITH) (Jan 2024).
- Presented my research work in the Sustainable Research Pathways (SRP) Workshop by Sustainable Horizon Institute (Feb 2023).
- Presented my PhD work at the International Conference on Neuromorphic Systems (ICONS) Doctoral Consortium (July 2021).

Awards and Recognition:
- Selected as Design Automation Conference (DAC) Young Fellowship Program (2024).
- Selected as an NSF iREDEFINE Fellow by the Electrical and Computer Engineering Department Heads Association (ECEDHA) (2024).
- Received Provost Doctoral Fellowship from George Mason University (2024).
- Selected for Design Automation and Test in Europe (DATE) Young Fellow Program (2023).
- Received Student Travel Grant for ISQED conference (2023).
- Selected for Design Automation Conference (DAC) Young Fellowship Program (2021,2022).
- Achieved 50% Scholarship during masters program (2016).
- Ranked 17 out of thousands in IIMDP JNTU Kakinada Entrance Examination (2012).

Leadership Experiences:
- President of a Yoga Club at George Mason University (2020-2024)
- At Ericsson was the Scrum master for the team I worked with, as well as a lead driver for Ericsdotter (women's network in Ericsson) (2018-2019)
- Led a Student Innovative cell at BTH (2017)
- I was Team Leader for a team of 4 members for my Bachelor thesis (2016).
- Volunteered for a non-profit organization called Swecha (2015).

Main Reviewer :
- IEEE International Symposium on Circuits and Systems (ISCAS) (2024)
- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (2023, 2024)
- IEEE Transactions on Circuits and Systems I (TCAS-I) (2023, 2024)
- IEEE Transactions on Circuits and Systems II (TCAS-II) (2023, 2024)
- Elsevier Integration,The VLSI Journal (2023)
- International Conference on Sustainable Computing (SUSCOM) (2023)
- IEEE International Conference on Computer Design (ICCD) (2022)