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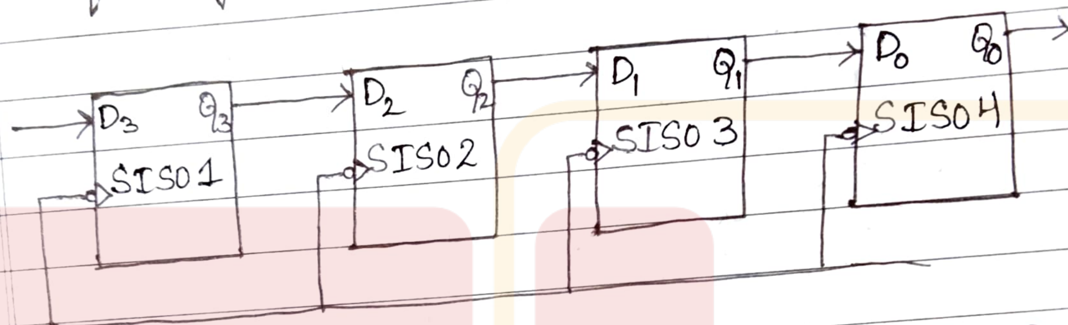
Module - 5

Register → Collection of all flip flops

Application

* Shift register
* Storage register

1 Shift register / SISO

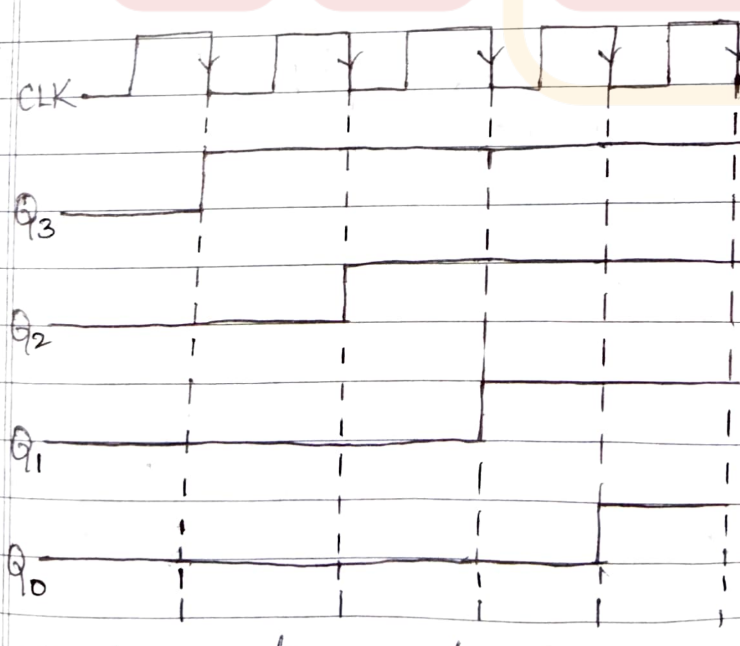


1111

Sin	Q_3	Q_2	Q_1	Q_0
Initially	0	0	0	0
↓	1	0	0	0
↓	1	1	0	0
↓	1	1	1	0
↓	1	1	1	1

Sout	Q_3	Q_2	Q_1	Q_0
↓	1	1	1	1
↓	0	1	1	1
↓	0	0	1	1
↓	0	0	0	1
↓	0	0	0	0

Sin



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~~Write time diagram for Sout~~

* Registers
* Flip flop stores 1-bit memory cell at a time
* Register is defined as group of flip flops or collection of flip flops together & it stores n-bit flip flops
* It increases the storage capacity
* The n-bit register consist of n no. of flip flops & is capable of storing n-Bit word

* Classification of Registers.
Dependency on i/p & o/p

Imp 1 Serial-in-serial-out (SISO)
2 Serial-in-parallel-out (SIPO)
Imp 3 Parallel-in-serial-out (PISO)
4 Parallel-in-parallel-out (PIPO)

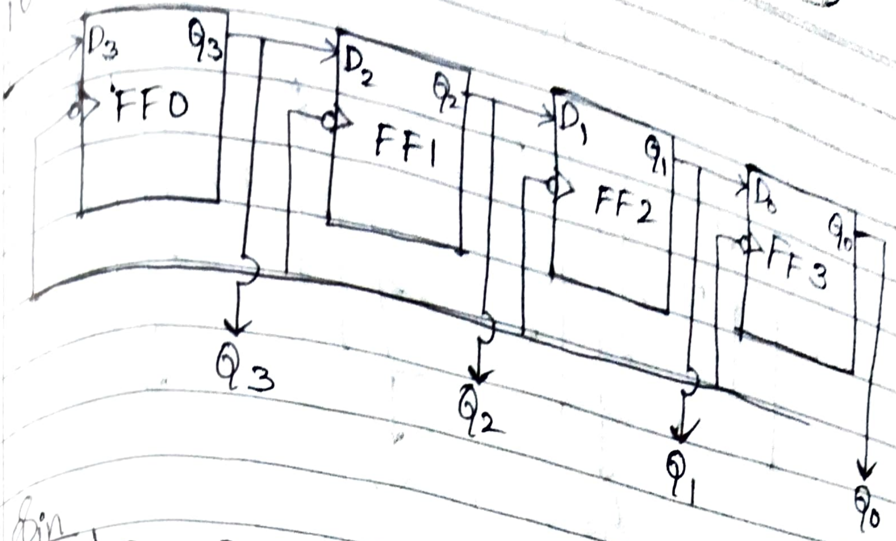
* Application of Registers

1 Shift register
In shift register, the i/p will be shifted 1 after the other & the o/p is also same as the i/p

2 Storage register
In storage register, whatever the i/p is given that will stored in the current flip flop & immediately it will produces a result

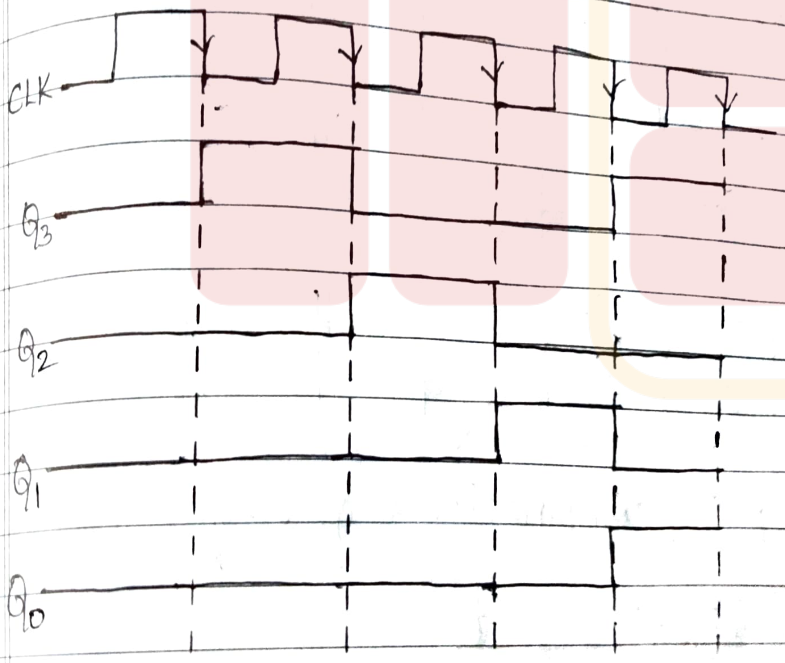
SIPO

1001



Sin

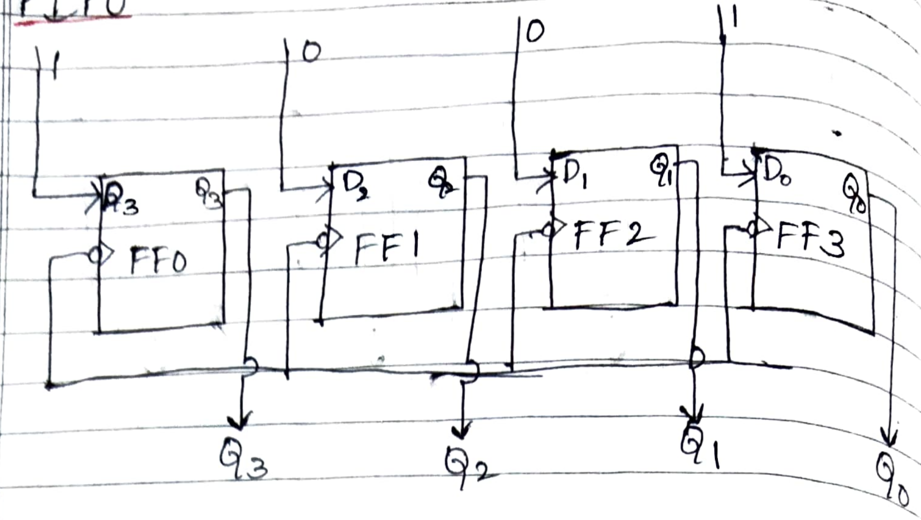
CLK	Q_3	Q_2	Q_1	Q_0
Initially ↓	0	0	0	0
↓	1	0	0	0
↓	0	1	0	0
↓	0	0	1	0
↓	1	0	0	1



Pout

CLK	Q_3	Q_2	Q_1	Q_0
	1	0	0	1
	1	0	0	1

3 PIPO

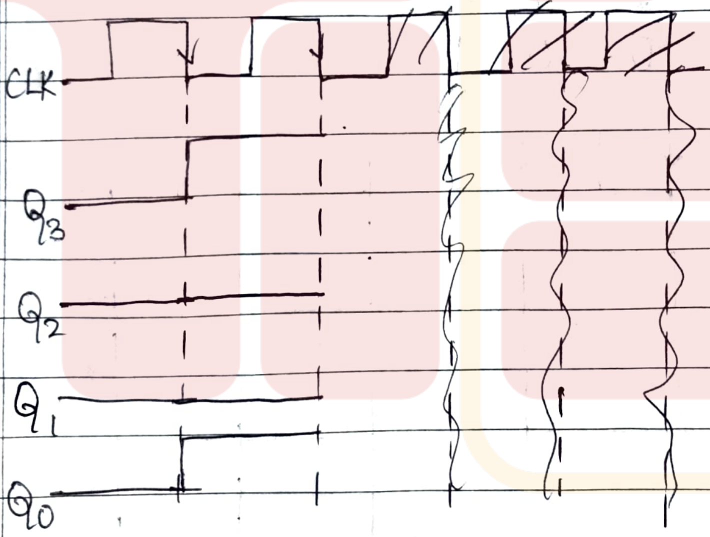


Pin

CLK	Q_3	Q_2	Q_1	Q_0
↓	0	0	0	0
↓	1	0	0	1

Pout

CLK	Q_3	Q_2	Q_1	Q_0
↑	1	0	0	



V Imp* Pakka

Explain combinational & sequential ckt

Combinational ckt

1 The o/p of the combinational ckt depen[ds] entirely on the present i/p
2 It exhibits a faster speed
3 It is comparatively easy to design

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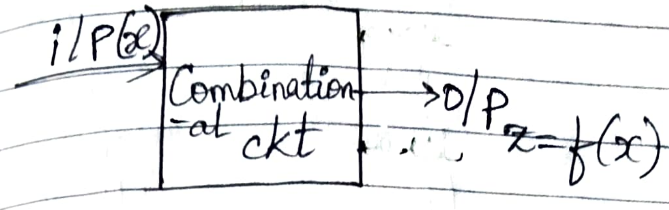
4 No feedback is present b/w the i/p & o/p
5 The combinational ckt depends on time
6 Logic gates form the building blocks of the ckt
It can use both boolean & arithmetic operation
Ex:- Multiplexer, decoder, encoder, D-multiplexer



Sequential ckt

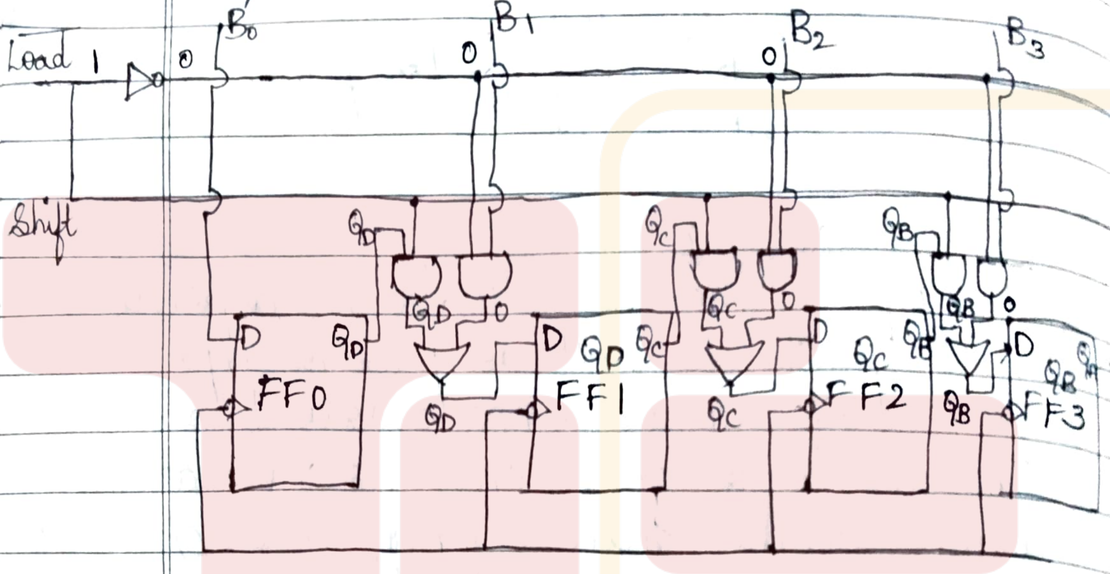
1 The o/p of the sequential ckt depends on both past as well as present i/p
2 It works as a comparatively slower speed
3 The design of these ckts is comparatively much tougher than combinational ckt
4 Feedback exists b/w the i/p & o/p
5 The ckt is time dependent
6 Flipflop constitute the building block of ckt
Ex:- Counters, flipflops, registers

4 PISO
PISO register stores data, shifts it on a clock by clock basis & delay it by the no. of stages times the clock period. In addition that PISO register means we can load the data into all stages before any shifting ever begins
* This is a way to convert data from a parallel format to a serial format. By parallel format the data bites are present

4-bit → 4FF
5-bit → 5FF

simultaneously by on individual wires

* In serial format the data bits are stored sequentially on a single wire
* A stage consist of a type D FF for storage, & "AND-OR" selector to determine whether the data will load in parallel or shift load data to the right



Sout

Sout	Q_3	Q_2	Q_1	Q_0
↓	1	1	1	1
↓	0	1	1	1
↓	0	0	1	1
↓	0	0	0	1
↓	0	0	0	0

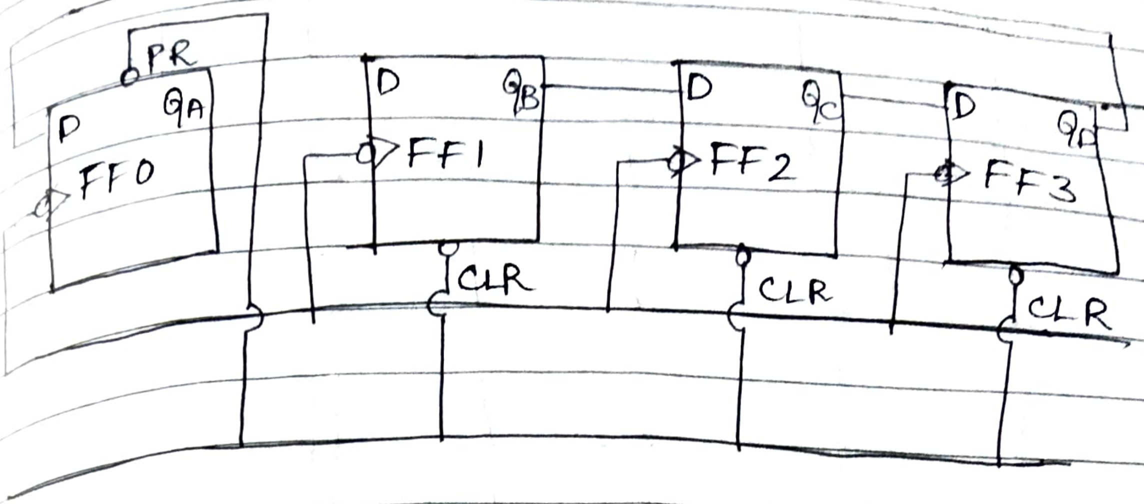
Q_3	Q_2	Q_1	Q_0
1	1	0	1
0	1	1	0
0	0	1	1
0	0	0	1
0	0	0	0

Write timing diagram

* **Applications**

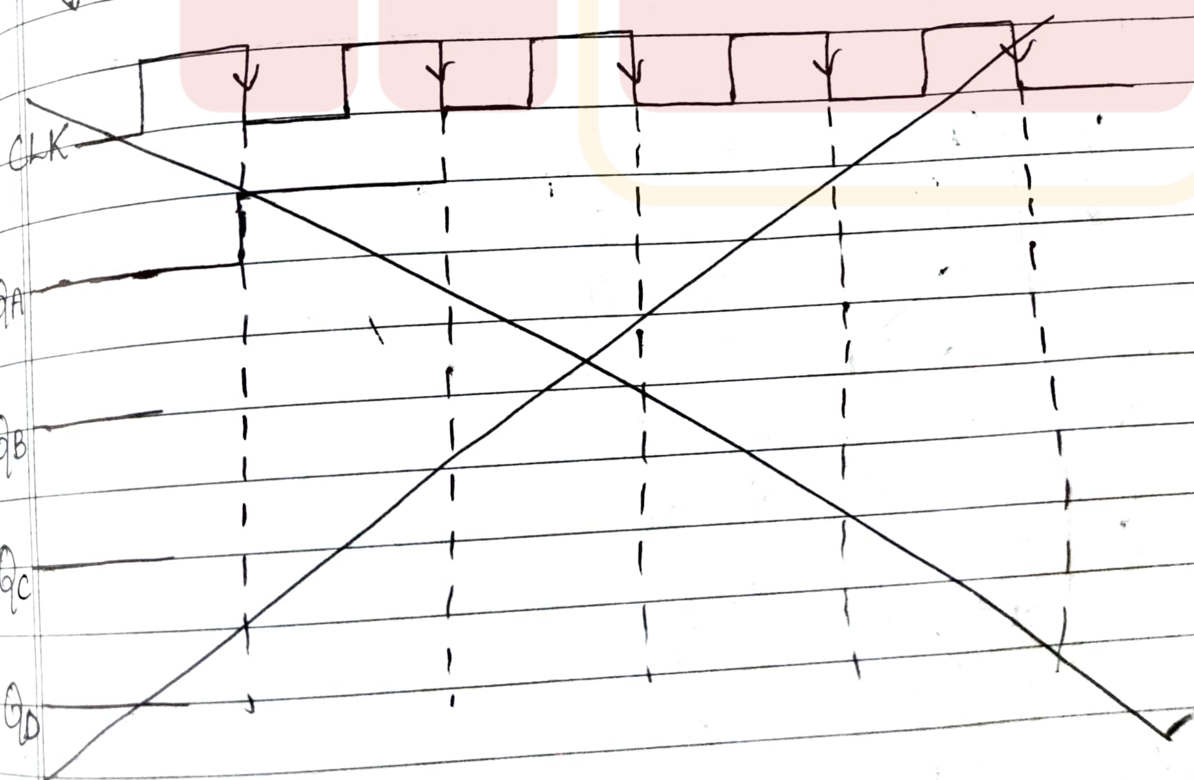
* 8M 1 Ring Counter - o/p of the last register will be connected to the 1st register

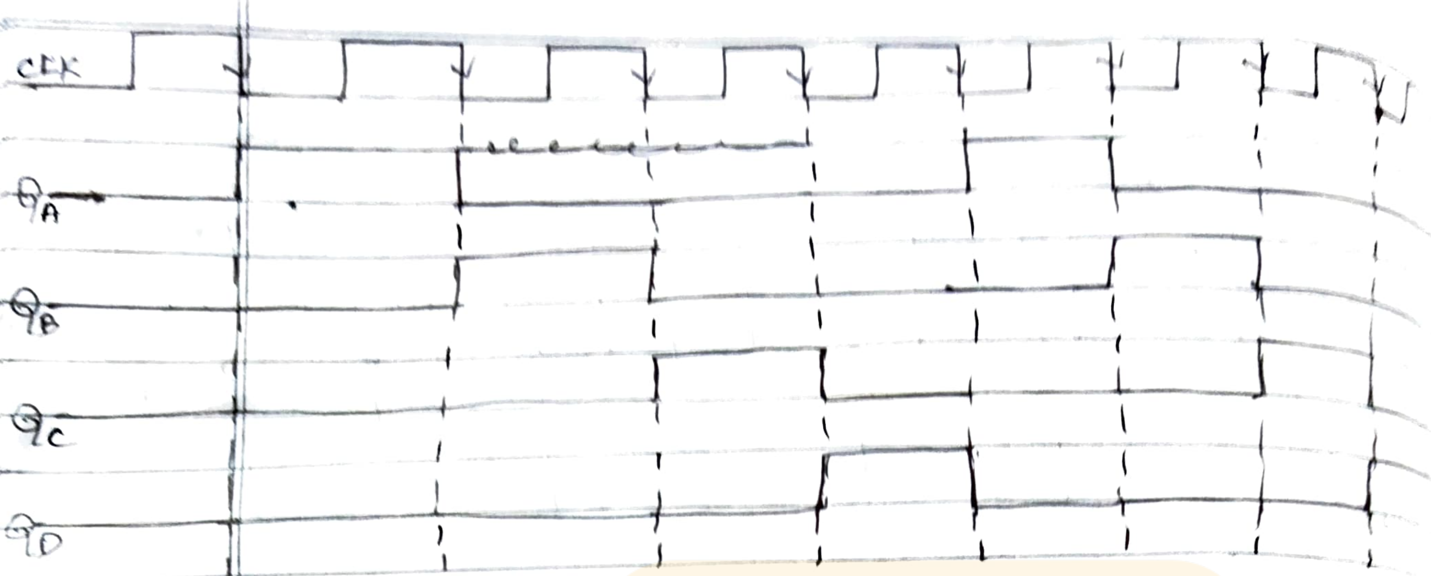
PR = 1 (preset)
CLR = 0 (clear)



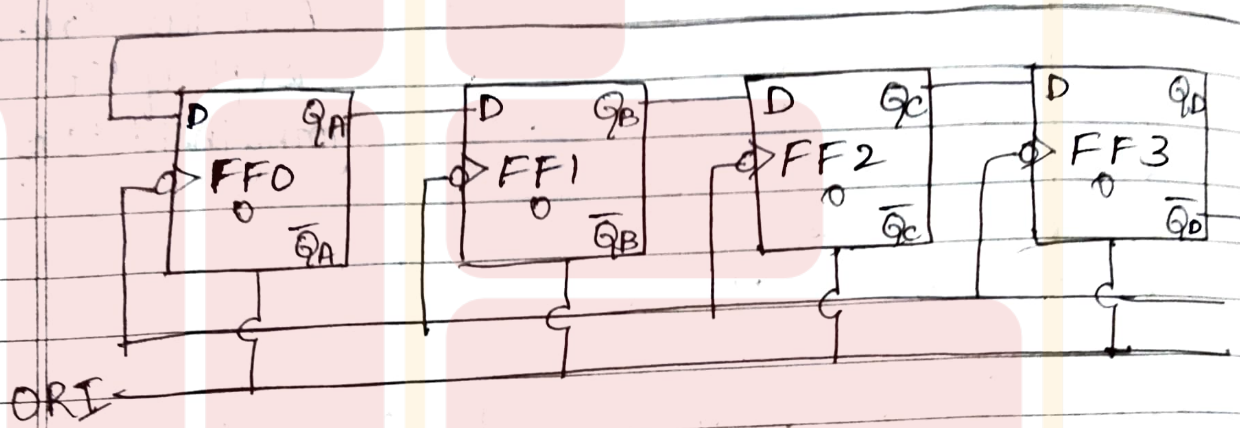
OR

CLK	Q_A	Q_B	Q_C	Q_D
	1	0	0	0
↓	0	1	0	0
↓	0	0	1	0
↓	0	0	0	1
↓	1	0	0	0
↓	0	1	0	0
↓	0	0	1	0
↓	0	0	0	1



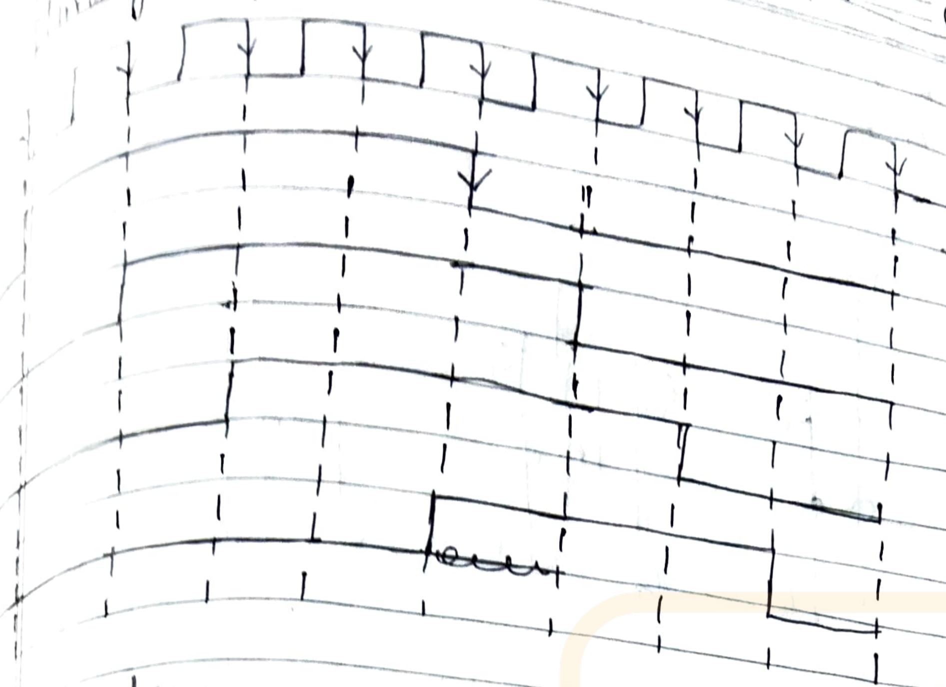


2 Johnson's Counter/Switch Tail/Twist Pair



CLK	QA	QB	QC	QD
↓	0	0	0	0
↓	1	0	0	0
↓	1	1	0	0
↓	1	1	1	0
↓	1	1	1	1
↓	1	1	1	1
↓	0	1	1	1
↓	0	0	1	1
↓	0	0	0	1
↓	0	0	0	0

Timing diagram



* Counters
Counter is defined as a counts a no. in seconds. It should be mainly depends on clk. There are 2 types of counters
a Asynchronous counter
b Synchronous counter

a Asynchronous/ Ripple up counter
It is a counter, the o/p of the 1st FF is connected to the i/p of the clock of the next FF & so on
There are 3 types of asynchronous counter
1 Up counter (a) low → high
2 Down counter (a) high → low
3 Up & down counter

1 Up counter
3 types
• 2 bit

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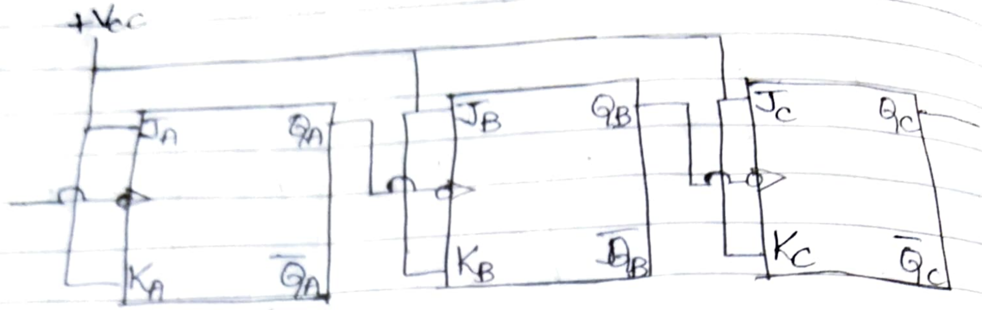
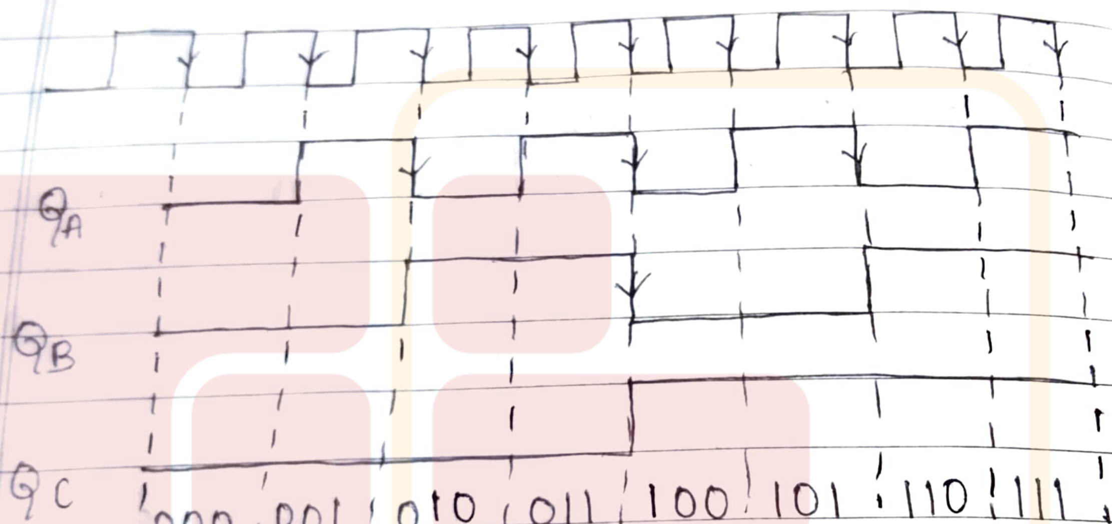
- 3 bit
- 4 bit

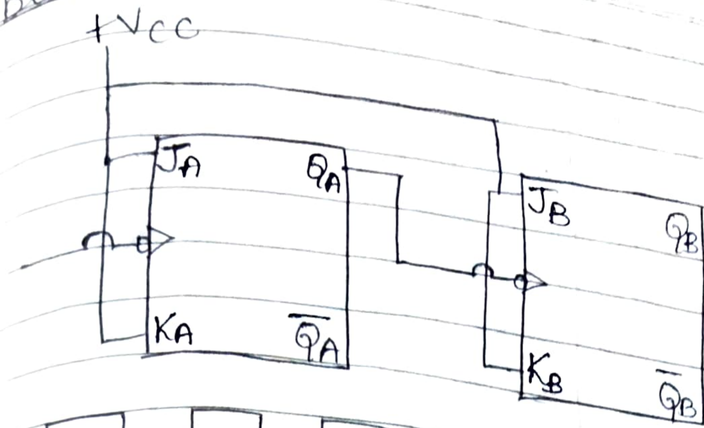
- 3 bit counter

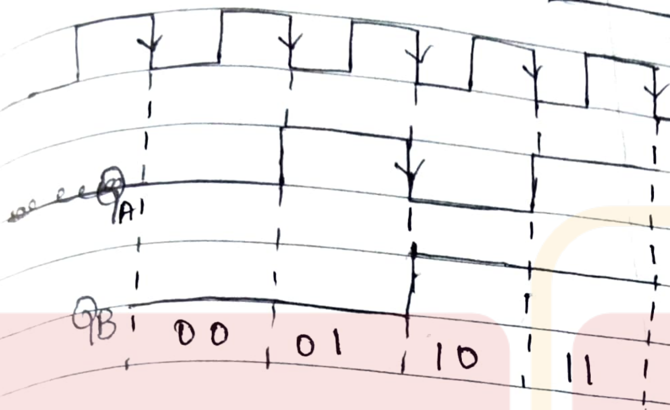




Q_C	Q_B	Q_A
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

2 bit counter





Q_B	Q_A
0	0
0	1
1	0
1	1

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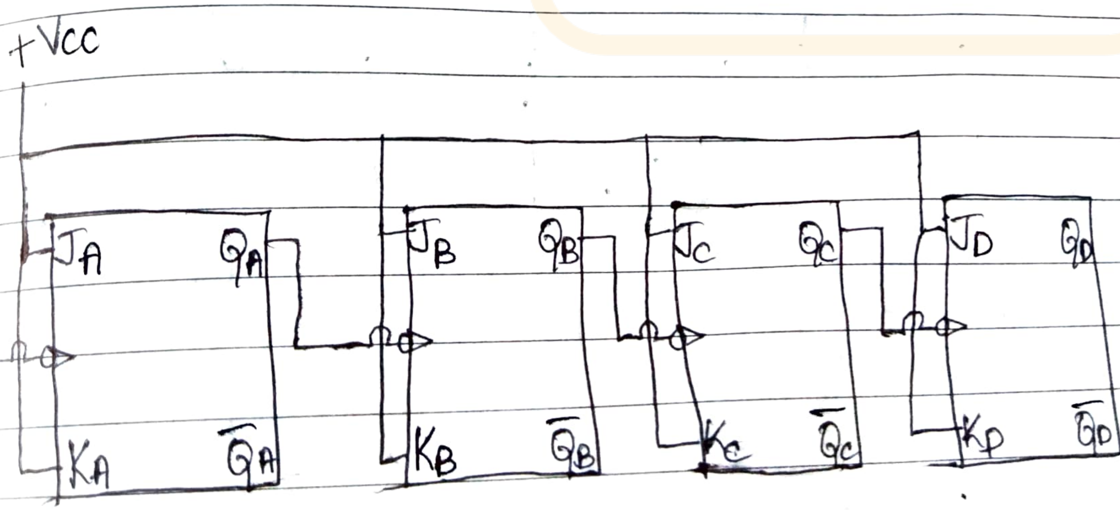
4 bit counter



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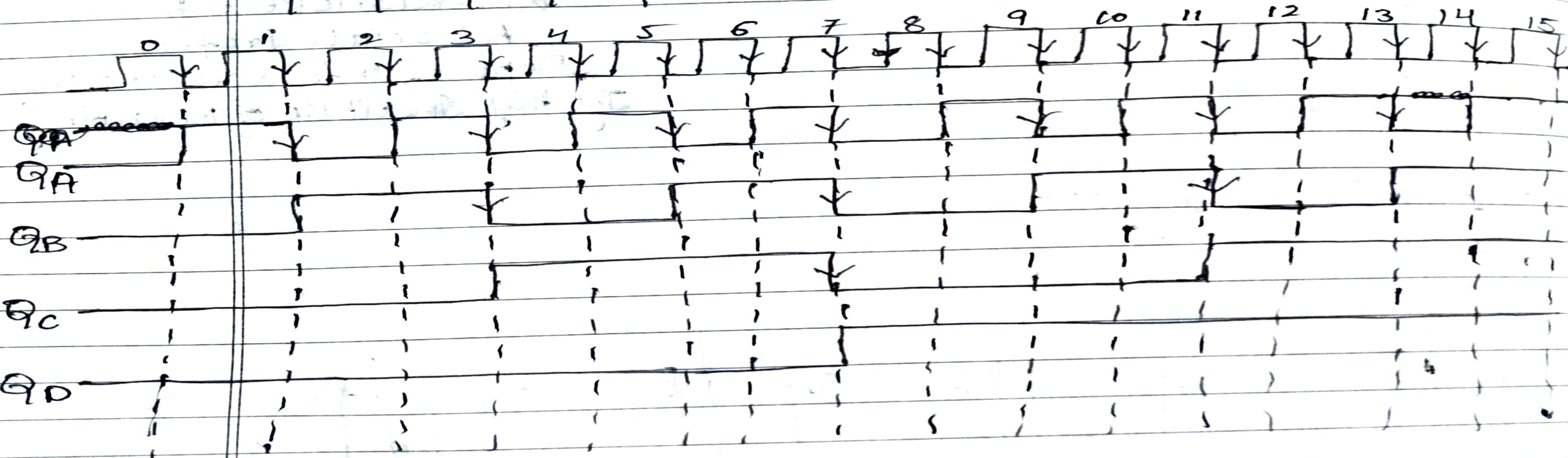
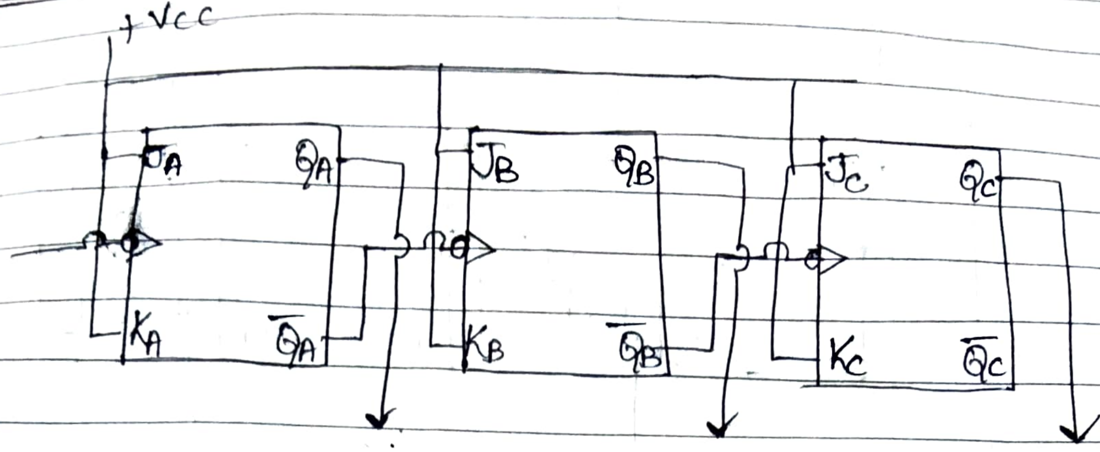
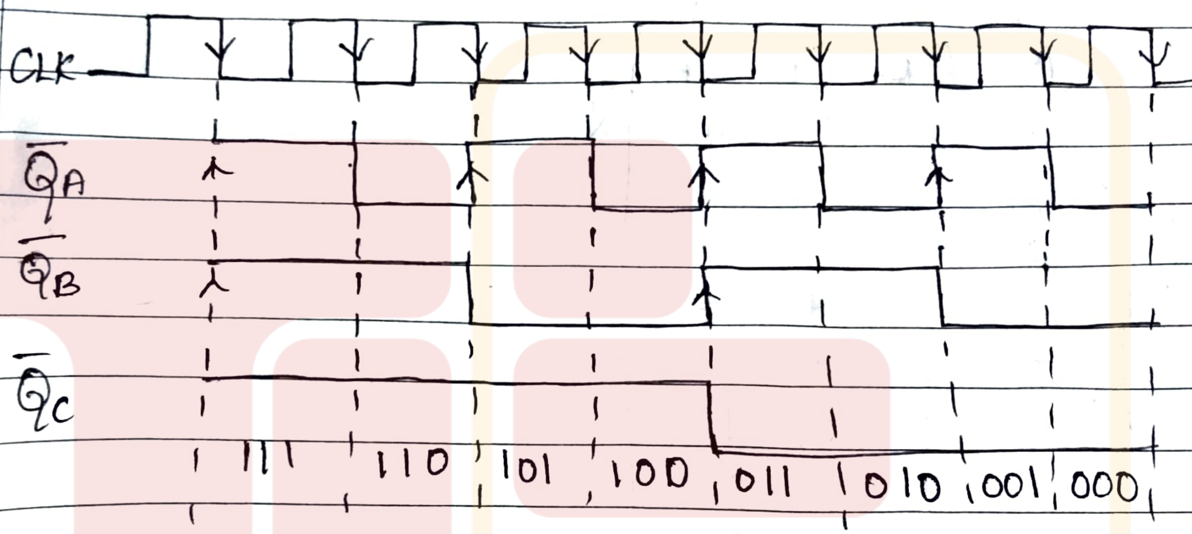
8 QD	4 QC	2 QB	1 QA
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1



2. Down counter

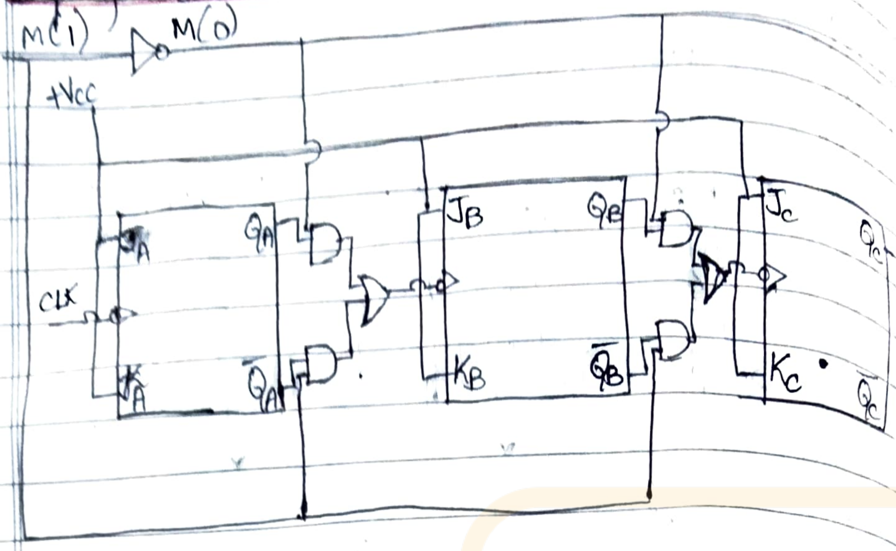
• 3 bit





Q_C	Q_B	Q_A
1	1	1
1	1	0
1	0	1
1	0	0
0	1	1
0	1	0
0	0	1
0	0	0

3 Up & down counter



8 M	4 QC	2 QB	1 QA
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

fall up

Down rise

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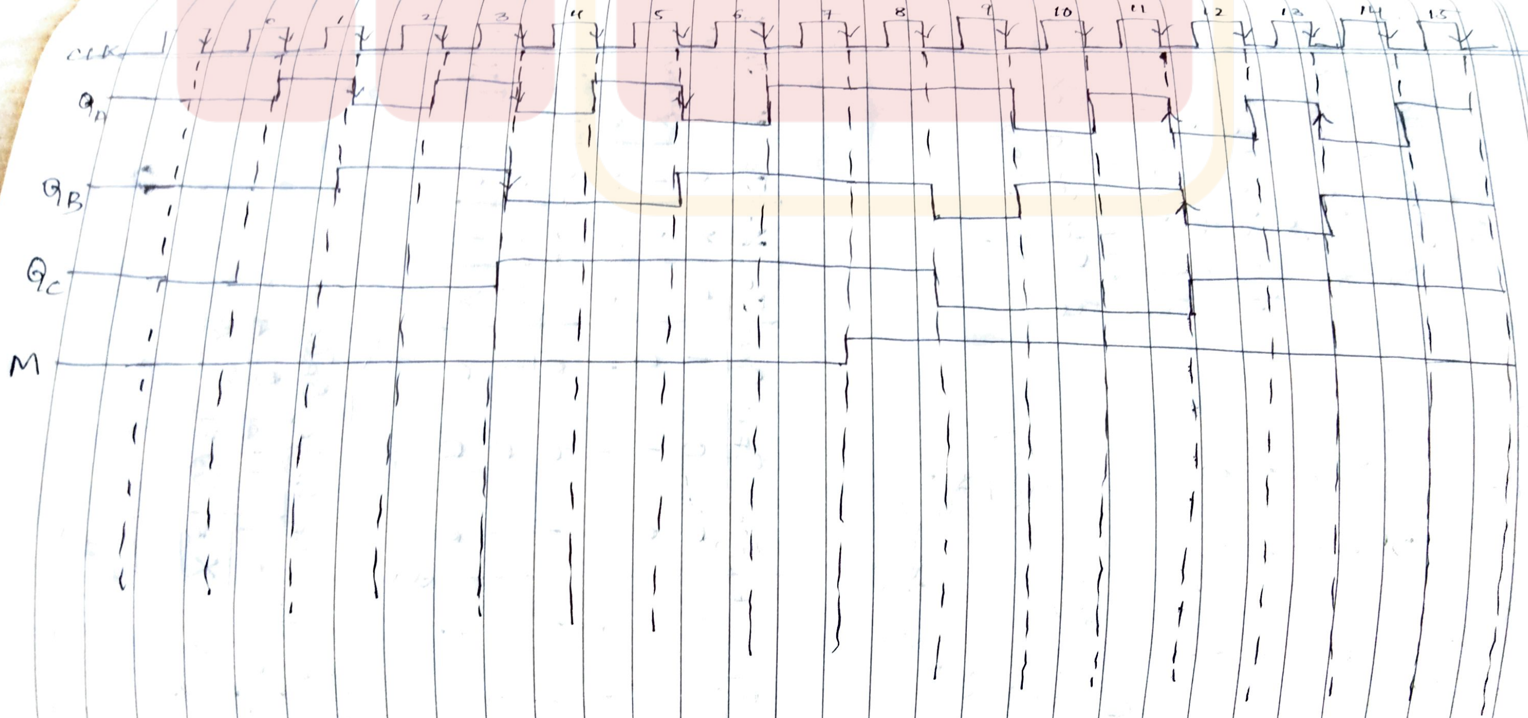


CLK
Q_A
Q_B
Q_C
M
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15

Imp * **Synchronous up Mod 6 (JK)**

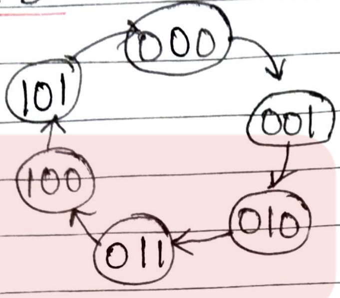
Steps

1) Identification of FF
2) Write the ET for given FF
3) Write the STD for given FF
4) Write the TT for present & next state
5) Write the boolean expression using K-map method
6) Design a ckt for synchronous ckt

I **ET (JK)**

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

II **STD**



III

Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	0	0	0	X	1	0	X	X	1

IV

$Q_C \backslash Q_BQ_A$	$\overline{Q_B}\,\overline{Q_A}$	$\overline{Q_B}Q_A$	Q_BQ_A	$Q_B\overline{Q_A}$
$\overline{Q_C}$	0 (0)	0 (1)	1 (3)	0 (2)
Q_C	X (4)	X (5)	X (7)	X (6)

$$\boxed{J_C = Q_BQ_A}$$

$Q_C \backslash Q_BQ_A$	$\overline{Q_B}\,\overline{Q_A}$	$\overline{Q_B}Q_A$	Q_BQ_A	$Q_B\overline{Q_A}$
$\overline{Q_C}$	X 0	X 1	X 3	X 2
Q_C	0 4	1 5	X 7	X 6

$\boxed{K_C = Q_A}$

$Q_C \backslash Q_BQ_A$	$\overline{Q_B}\,\overline{Q_A}$	$\overline{Q_B}Q_A$	Q_BQ_A	$Q_B\overline{Q_A}$
$\overline{Q_C}$	0 0	1 1	X 3	X 2
Q_C	0 4	0 5	X 7	X 6

~~$J_B = \overline{Q_B}Q_A$~~ $\boxed{J_B = \overline{Q_C}Q_A}$

	$\overline{Q_B}\,\overline{Q_A}$	$\overline{Q_B}Q_A$	Q_BQ_A	$Q_B\overline{Q_A}$
$\overline{Q_C}$	X 0	X 1	1 3	0 2
Q_C	X 4	X 5	X 7	X 6

$\boxed{K_B = Q_A}$

	$\overline{Q_B}\,\overline{Q_A}$	$\overline{Q_B}Q_A$	Q_BQ_A	$Q_B\overline{Q_A}$
$\overline{Q_C}$	1 0	X 1	1 3	X 2
Q_C	1 4	X 5	X 7	X 6

$\boxed{J_A = 1}$

	$\overline{Q_B}\,\overline{Q_A}$	$\overline{Q_B}Q_A$	Q_BQ_A	$Q_B\overline{Q_A}$
$\overline{Q_C}$	X 0	1 1	X 3	1 2
Q_C	X 4	1 5	X 7	X 6

$\boxed{K_A = 1}$

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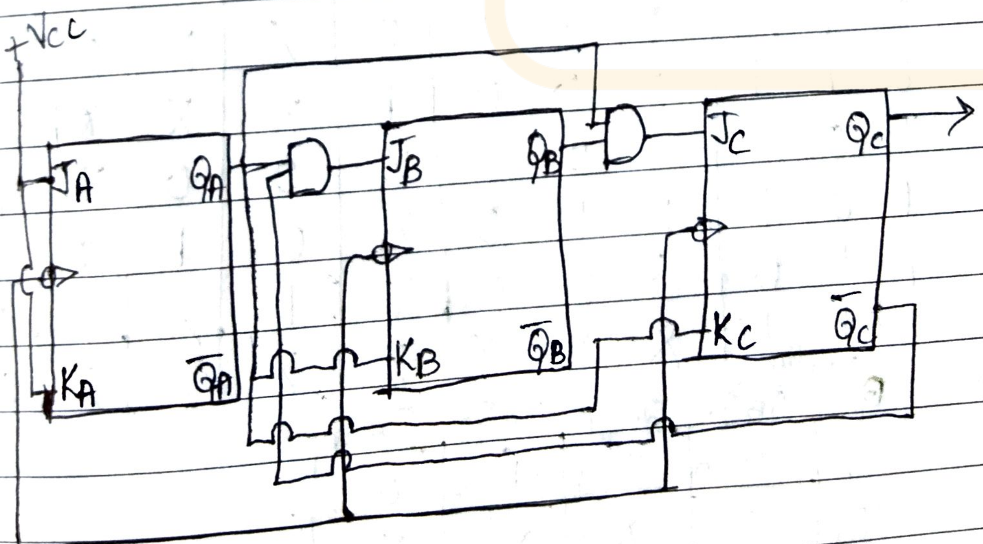
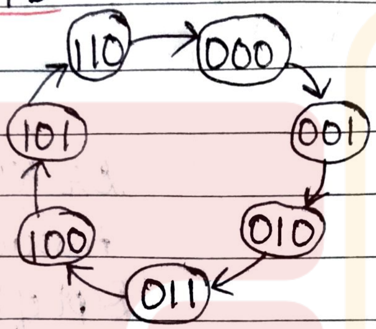


* Mod 7 (JK) (Up counter)

I. ET (JK)

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

II. STD



III.

Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	X	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	0	0	0	X	1	X	1	0	X
1	1	1	X	X	X	X	X	X	X	X	X

IV.

$Q_C \backslash Q_BQ_A$	$\overline{Q_B}\,\overline{Q_A}$	$\overline{Q_B}Q_A$	Q_BQ_A	$Q_B\overline{Q_A}$
$\overline{Q_C}$	0 (0)	0 (1)	1 (3)	0 (2)
Q_C	X (4)	X (5)	X (7)	X (6)

$$\boxed{J_C = Q_B Q_A}$$

	$\bar{Q}_B\bar{Q}_A$	$\bar{Q}_BQ_A$	Q_BQ_A	$Q_B\bar{Q}_A$
$\bar{Q}_C$	X 0	X 1	X 3	X 2
Q_C	0 4	0 5	X 7	1 6

$\boxed{K_C = Q_B}$

	$\bar{Q}_B\bar{Q}_A$	$\bar{Q}_BQ_A$	Q_BQ_A	$Q_B\bar{Q}_A$
$\bar{Q}_C$	0 0	1 1	X 3	X 2
Q_C	0 4	1 5	X 7	X 6

$\boxed{J_B = Q_A}$

	$\bar{Q}_B\bar{Q}_A$	$\bar{Q}_BQ_A$	Q_BQ_A	$Q_B\bar{Q}_A$
$\bar{Q}_C$	X 0	X 1	X 3	X 2
Q_C	1 4	0 5	X 7	1 6

~~$K_B = \bar{Q}_A$~~

	$\bar{Q}_B\bar{Q}_A$	$\bar{Q}_BQ_A$	Q_BQ_A	$Q_B\bar{Q}_A$
$\bar{Q}_C$	X 0	X 1	1 3	0 2
Q_C	X 4	X 5	X 7	1 6

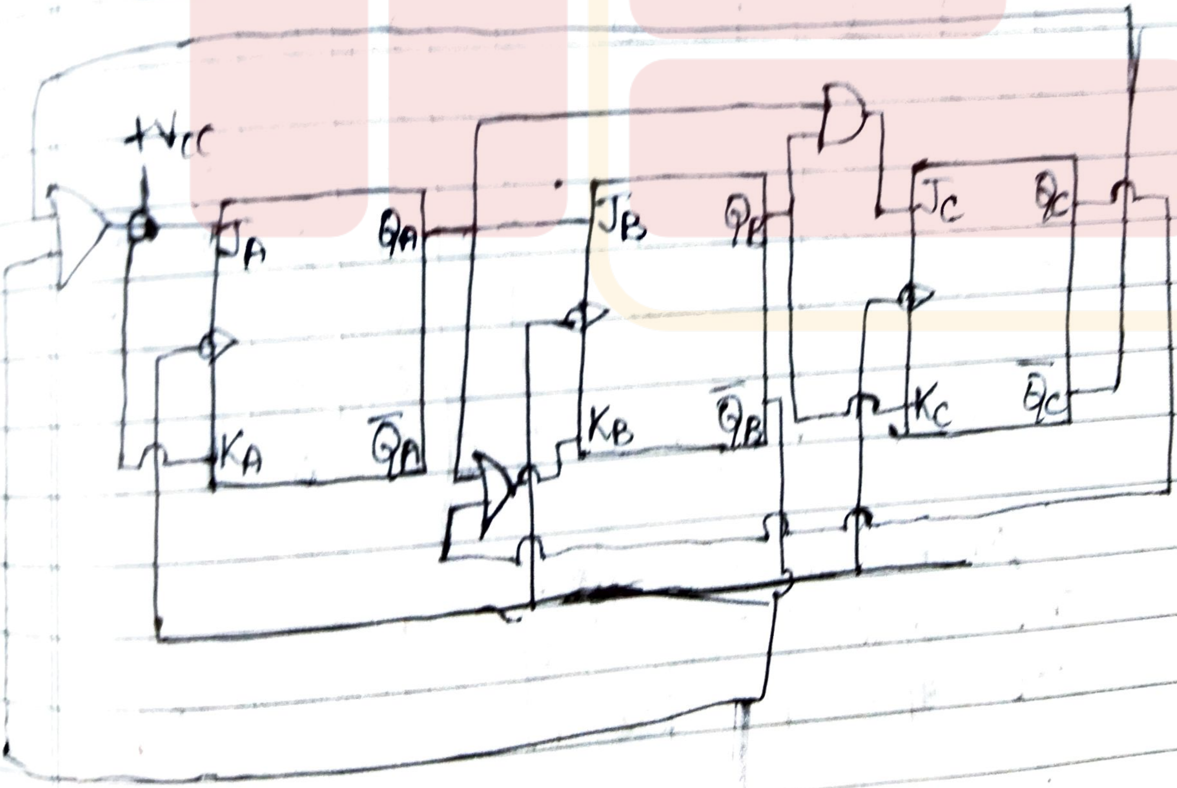
$\boxed{K_B = Q_A + \bar{Q}_C}$

	$\bar{Q}_B\bar{Q}_A$	$\bar{Q}_BQ_A$	Q_BQ_A	$Q_B\bar{Q}_A$
$\bar{Q}_C$	1 0	X 1	X 3	0 2
Q_C	1 4	X 5	X 7	0 6

$\boxed{J_A = \bar{Q}_B + \bar{Q}_C}$

	$\bar{Q}_B\bar{Q}_A$	$\bar{Q}_BQ_A$	Q_BQ_A	$Q_B\bar{Q}_A$
$\bar{Q}_C$	X 0	1 1	1 3	X 2
Q_C	X 4	1 5	X 7	X 6

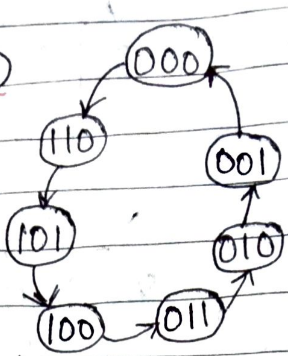
~~$K_A = Q_A$~~ $\boxed{K_A = 1}$



* Down counter

Mod (7)

STD



ET Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	J_C	K_C	J_B	K_B	J_A	K
1	1	0	1	0	1	X	0	X	1	1	X
1	0	1	1	0	0	X	0	X	1	X	1
1	0	0	0	1	1	X	1	X	0	1	X
0	1	1	0	1	0	0	X	1	X	X	1
0	1	0	0	0	1	0	X	0	X	1	X
0	0	1	0	0	0	0	X	0	X	X	1
0	0	0	1	1	0	1	X	1	X	0	X

	$\bar{Q}_B\bar{Q}_A$	$\bar{Q}_B Q_A$	$Q_B Q_A$	$Q_B\bar{Q}_A$
$\bar{Q}_C$	X 0	X 1	0 3	X 2
Q_C	0 4	0 5	X 7	1 6

$$\boxed{J_C = Q_B\bar{Q}_A}$$

	$\bar{Q}_B\bar{Q}_A$	$\bar{Q}_B Q_A$	$Q_B Q_A$	$Q_B\bar{Q}_A$
$\bar{Q}_C$	0 0	0 1	X 3	1 2
Q_C	X 4	X 5	X 7	X 6

$$\boxed{K_C = Q_B}$$

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	$\bar{Q}_B\bar{Q}_A$	$\bar{Q}_BQ_A$	Q_BQ_A	$Q_B\bar{Q}_A$
$\bar{Q}_C$	X 0	X 1	1 3	X 2
Q_C	0 4	0 5	X 7	1 6

$\boxed{J_B = Q_B}$

	$\bar{Q}_B\bar{Q}_A$	$\bar{Q}_BQ_A$	Q_BQ_A	$Q_B\bar{Q}_A$
$\bar{Q}_C$	1 0	1 1	X 3	0 2
Q_C	X 4	X 5	X 7	X 6

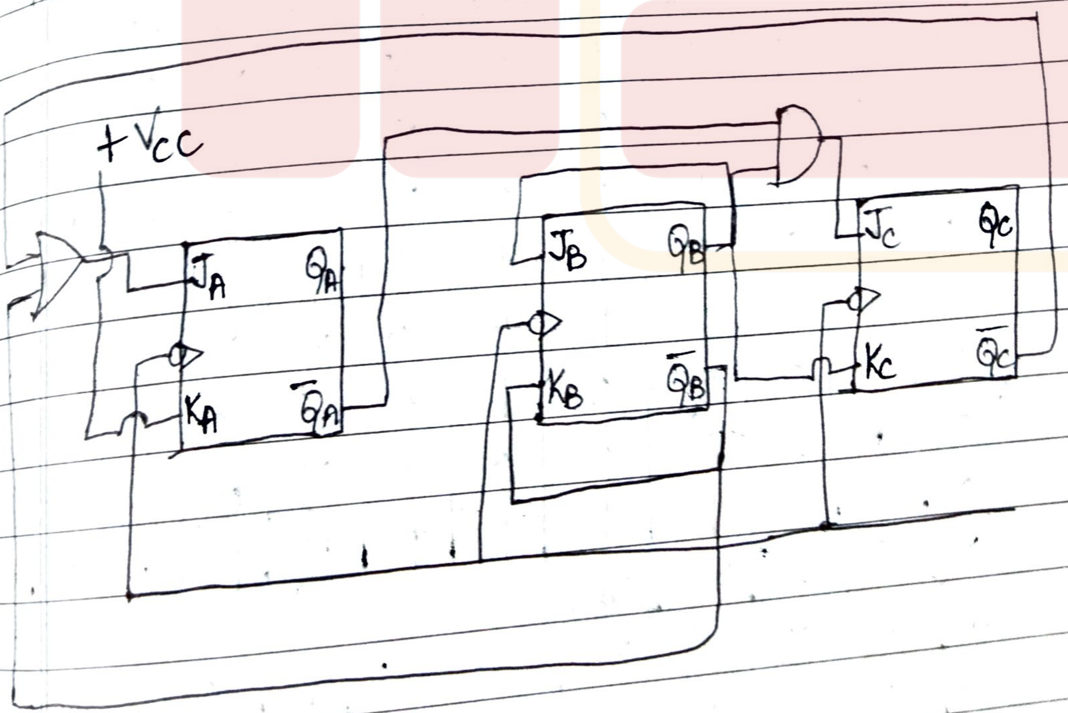
$\boxed{K_B = \bar{Q}_B}$

	$\bar{Q}_B\bar{Q}_A$	$\bar{Q}_BQ_A$	Q_BQ_A	$Q_B\bar{Q}_A$
$\bar{Q}_C$	1 0	X 1	X 3	1 2
Q_C	1 4	X 5	X 7	0 6

$\boxed{J_A = \bar{Q}_B + \bar{Q}_C}$

	$\bar{Q}_B\bar{Q}_A$	$\bar{Q}_BQ_A$	Q_BQ_A	$Q_B\bar{Q}_A$
$\bar{Q}_C$	X 0	1 1	1 3	X 2
Q_C	X 4	1 5	X 7	X 6

$\boxed{K_A = 1}$

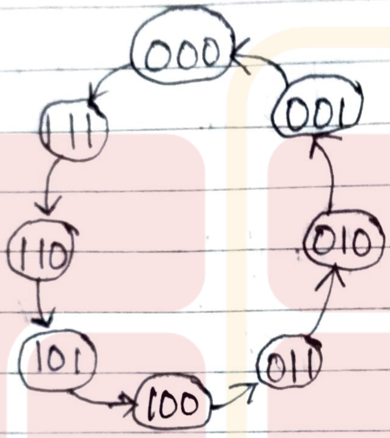


MOD 8 (Down Counter)

J.K E.T

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

STD



Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	J_C	K_C	J_B	K_B	J_A	K_A
1	1	1	1	1	0	X	0	X	0	X	1
1	1	0	1	0	1	X	0	X	1	1	X
1	0	1	1	0	0	X	0	0	X	X	1
1	0	0	0	1	1	X	1	1	X	1	X
0	1	1	0	1	0	0	X	X	0	X	1
0	1	0	0	0	1	0	X	X	1	1	X
0	0	1	0	0	0	0	X	0	X	X	1
0	0	0	1	1	1	1	X	1	X	1	X

	$\bar{Q}_B\bar{Q}_A$	$\bar{Q}_B Q_A$	$Q_B Q_A$	$Q_B\bar{Q}_A$
$\bar{Q}_C$	X	X	X	X
Q_C	0	0	1	0

$\boxed{J_C = Q_B Q_A}$

	$\bar{Q}_B\bar{Q}_A$	$\bar{Q}_B Q_A$	$Q_B Q_A$	$Q_B\bar{Q}_A$
$\bar{Q}_C$	0	0	1	0
Q_C	X	X	X	X

$\boxed{K_C = Q_B Q_A}$

$Q_C \backslash Q_BQ_A$			
X	X	1	0
X	X	1	0

$\boxed{J_B = Q_A}$

$Q_C \backslash Q_BQ_A$			
0	1	X	X
0	1	X	X

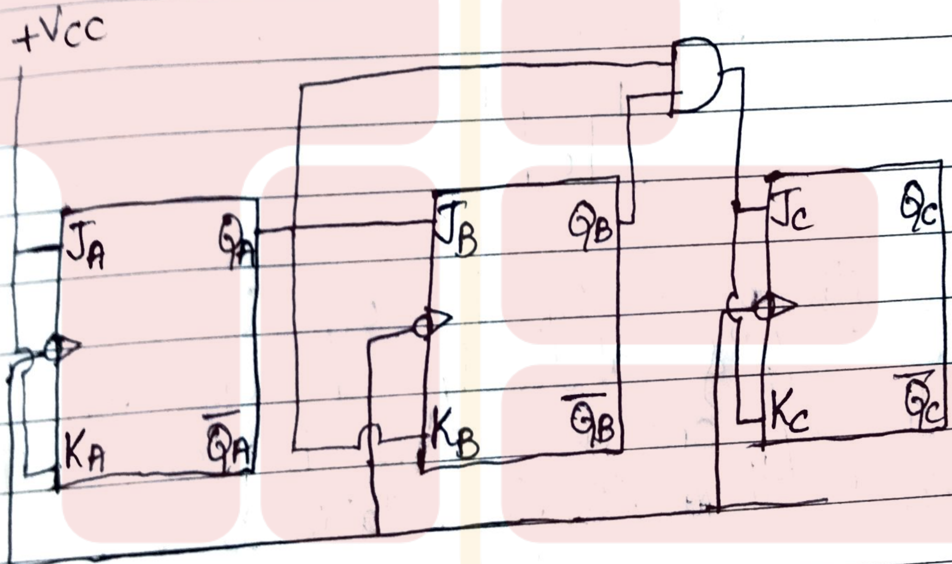
$\boxed{K_B = Q_A}$

$Q_C \backslash Q_BQ_A$			
X	1	1	X
X	1	1	X

$\boxed{J_A = 1}$

$Q_C \backslash Q_BQ_A$			
1	X	X	1
1	X	X	1

$\boxed{K_A = 1}$



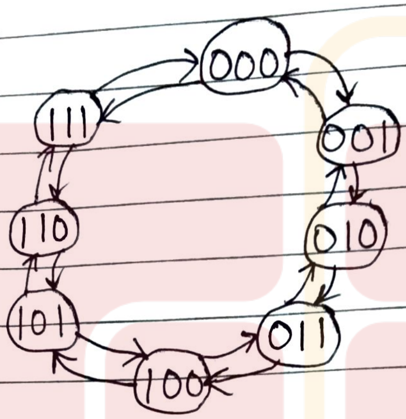
* Up & down counter

MOD 8

ET

Qn	Qn+1	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

STD



M	Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	0	0	1	0	X	0	X	1	X
0	0	0	1	0	1	0	0	X	1	X	X	1
0	0	1	0	0	1	1	0	X	X	0	1	X
0	0	1	1	1	0	0	1	X	X	1	X	1
0	1	0	0	1	0	1	X	0	0	X	1	X
0	1	0	1	1	1	0	X	0	1	X	X	1
0	1	1	0	1	1	1	X	0	X	0	1	X
0	1	1	1	0	0	0	X	1	X	1	X	1
1	0	0	0	1	1	1	1	X	1	X	1	X
1	0	0	1	0	0	0	0	X	0	X	X	1
1	0	1	0	0	0	1	0	X	X	1	1	X
1	0	1	1	0	1	0	0	X	X	0	X	1
1	1	0	0	0	1	1	X	1	1	X	1	X
1	1	0	1	1	0	0	X	0	0	X	X	1
1	1	1	0	1	0	1	X	0	X	1	1	X
1	1	1	1	1	1	0	X	0	X	0	X	1

Q_BQ_A / MQ_C	$\bar Q_B\bar Q_A$	$\bar Q_BQ_A$	Q_BQ_A	$Q_B\bar Q_A$
$\bar M\bar Q_C$	0	0	1	0
$\bar M Q_C$	X	X	X	X
$M Q_C$	X	X	X	X
$M\bar Q_C$	1	0	0	0

$$\boxed{J_C = \bar M Q_B Q_A + M \bar Q_B \bar Q_A}$$

X	X	X	X
0	0	1	0
1	0	0	0
X	X	X	X

$$\boxed{K_C = \bar M Q_B Q_A + M \bar Q_B \bar Q_A}$$

0	1	X	X
0	1	X	X
1	0	X	X
1	0	X	X

$$\boxed{J_B = \bar M Q_A + M \bar Q_A}$$

X	X	1	0
X	X	1	0
X	X	0	1
X	X	0	1

$$\boxed{K_B = \bar M Q_A + M \bar Q_A}$$

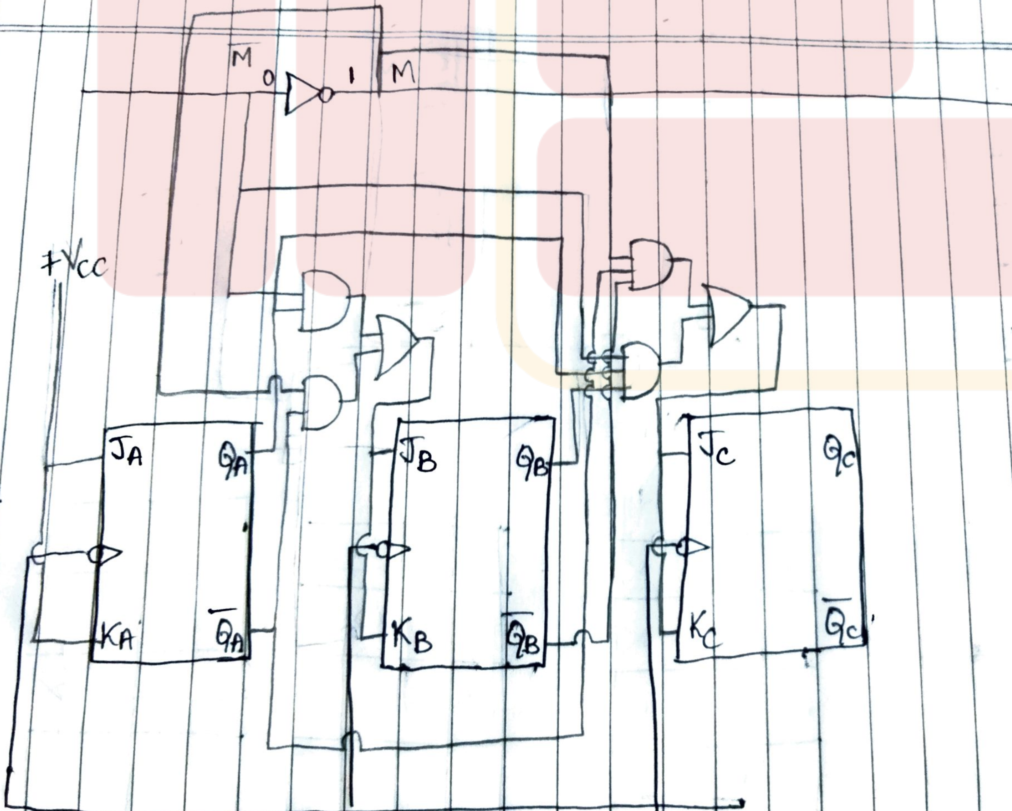
1	X	X	1
1	X	X	1
1	X	X	1
1	X	X	1

$$\boxed{J_A = 1}$$

X	1	1	X
X	1	1	X
X	1	1	X
X	1	1	X

$$\boxed{K_A = 1}$$

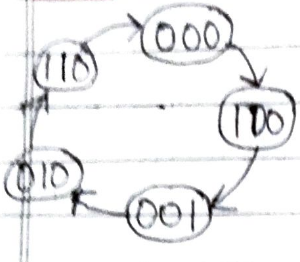
Up & down counter



IMP
Imp × PS Counter (Pre-stable counter)

1 Design a synchronous counter for the sequence
$0 \to 4 \to 1 \to 2 \to 6 \to 0 \to 4$

STD



ET (JK)

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	1	0	0	1	X	0	X	0	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	1	1	0	1	X	X	0	0	X
0	1	1	X	X	X	X	X	X	X	X	X
1	0	0	0	0	1	X	1	0	X	1	X
1	0	1	X	X	X	X	X	X	X	X	X
1	1	0	0	0	0	X	1	X	1	0	X
1	1	1	X	X	X	X	X	X	X	X	X

	$\bar{Q}_B\bar{Q}_A$	$\bar{Q}_B Q_A$	$Q_B Q_A$	$Q_B \bar{Q}_A$
$\bar{Q}_C$	1	0	X	1
Q_C	X	X	X	X

$\boxed{J_C = \bar{Q}_A}$

$Q_C \backslash Q_B Q_A$				
	X	X	X	X
	1	X	X	1

$\boxed{K_C = 1}$

	0	1	X	X
	0	X	X	X

$\boxed{J_B = Q_A}$

	X	X	X	0
	X	X	X	1

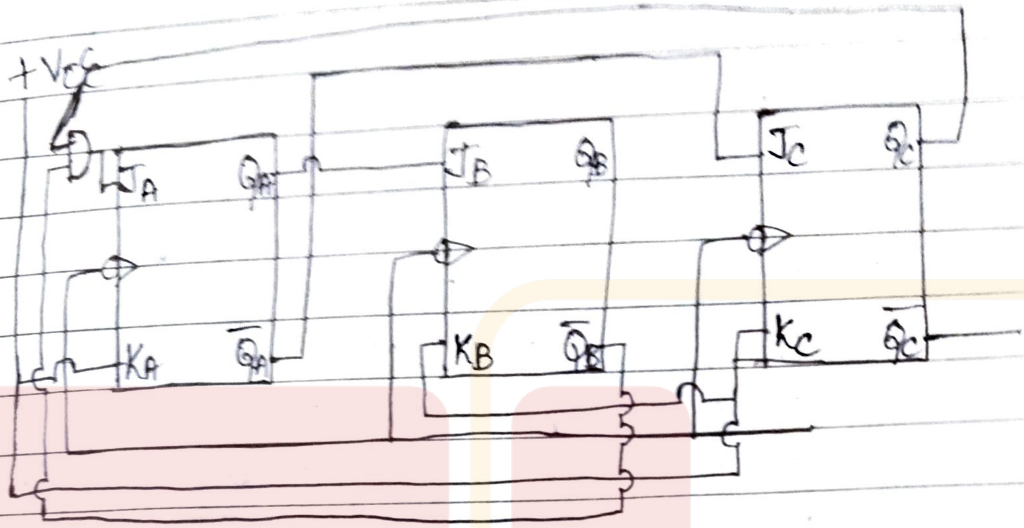
$\cancel{K_B = Q_C}$ $\boxed{K_B = Q_C}$

0	X	X	0
1	X	X	0

X	1	X	X
X	X	X	X

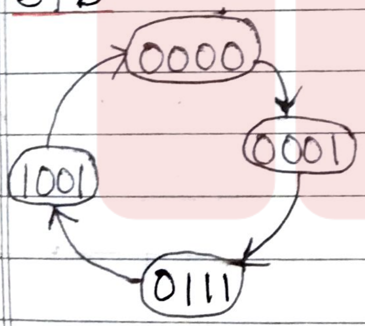
$J_A = Q_C \bar{Q}_B$

$K_A = 1$



2. $0 \rightarrow 1 \rightarrow 7 \rightarrow 9 \rightarrow 0 \rightarrow 1$

STD



ET (SR)

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

8 Q_D	4 Q_C	2 Q_B	1 Q_A	D+1	C+1	B+1	A+1	S_D	R_D	S_C	R_C	S_B	R_B	S_A	R_A
0	0	0	0	0	0	0	1	0	X	0	X	0	X	1	0
0	0	0	1	0	1	1	1	0	X	1	0	1	0	X	0
0	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X
0	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X
0	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X
0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X
0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X
0	1	1	1	1	0	0	1	1	0	0	1	0	1	X	0
1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X
1	0	0	1	0	0	0	0	0	0	0	X	0	X	0	1
1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X
1	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X
1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X
1	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X
1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X
1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X

Q_DQ_C \ Q_BQ_A	$\bar{Q}_B\bar{Q}_A$	$\bar{Q}_BQ_A$	Q_BQ_A	$Q_B\bar{Q}_A$
$\bar{Q}_D\bar{Q}_C$	0	0	X	X
$\bar{Q}_DQ_C$	X	X	1	X
Q_DQ_C	X	X	X	X
$Q_D\bar{Q}_C$	X	0	X	X

$\boxed{S_D = Q_C}$

X	X	X	X
X	X	0	X
X	X	X	X
X	1	X	X

$\boxed{R_D = Q_D}$

0	1	X	X
X	X	0	X
X	X	X	X
X	0	X	X

$\boxed{S_C = \bar{Q}_D\bar{Q}_C Q_A}$

X	0	X	X
X	X	1	X
X	X	X	X
X	X	X	X

$\boxed{R_C = Q_C}$

0	1	X	X
X	X	0	X
X	X	X	X
X	0	X	X

X	0	X	X
X	X	1	X
X	X	X	X
X	X	X	X

$S_B = Q_A$

$\boxed{S_B = Q_D Q_C Q_A}$

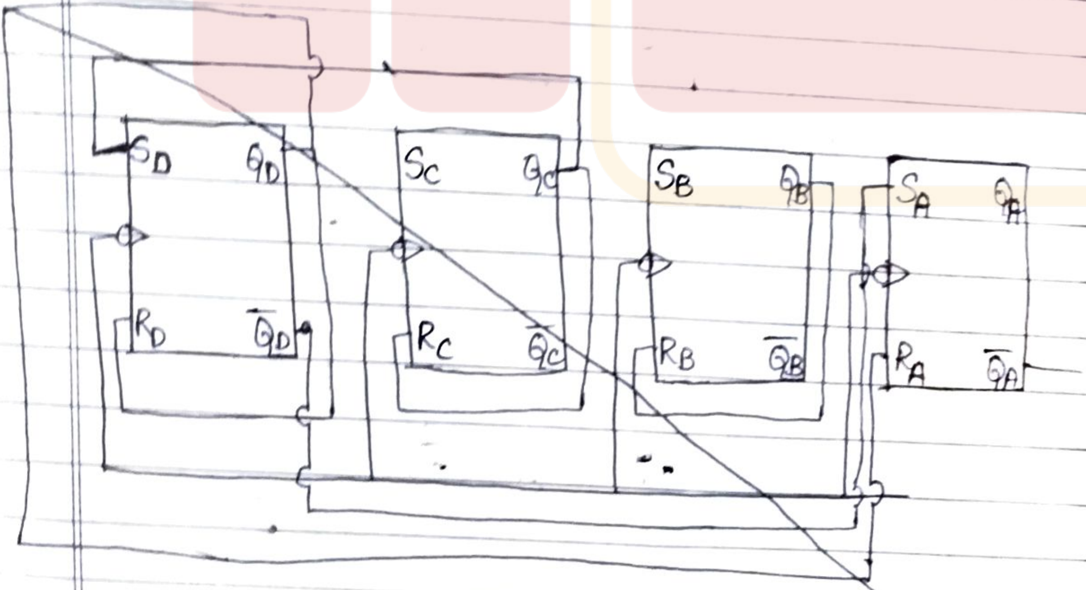
$\boxed{R_B = Q_B}$

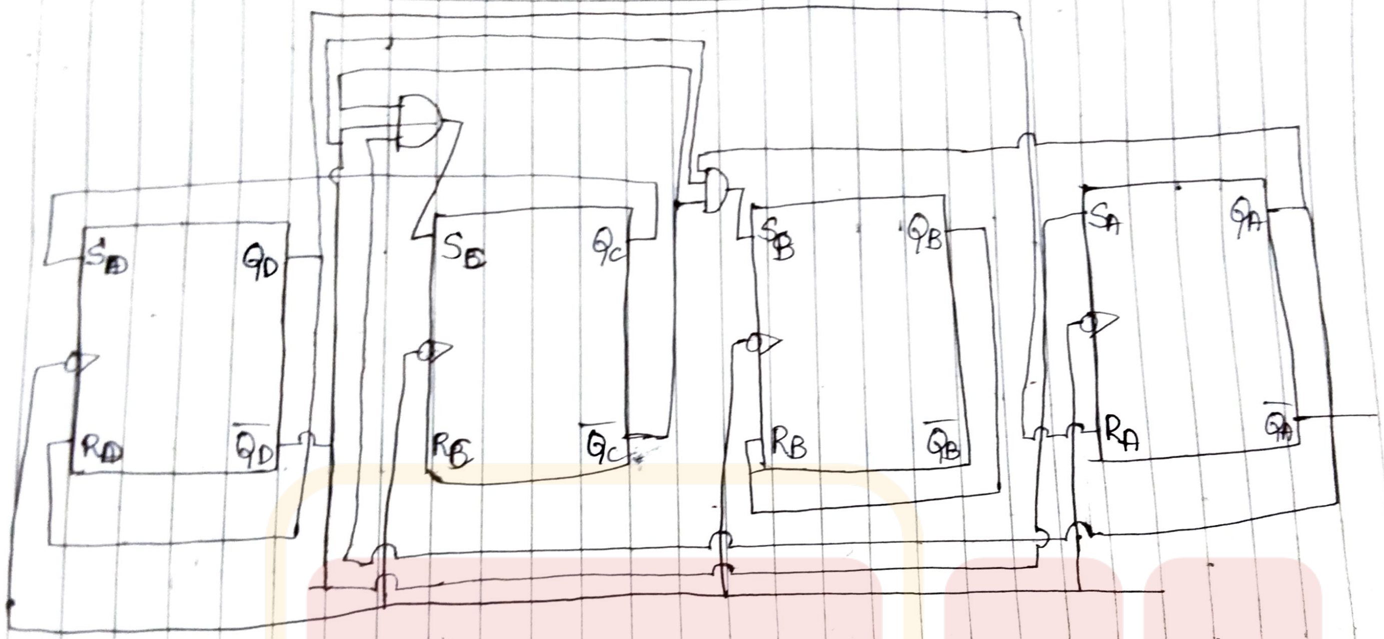
1	X	X	X
X	X	X	X
X	X	X	X
X	0	X	X

0	0	X	X
X	X	0	X
X	X	X	X
X	1	X	X

$\boxed{S_A = \bar{Q}_D}$

$\boxed{R_A = Q_D}$



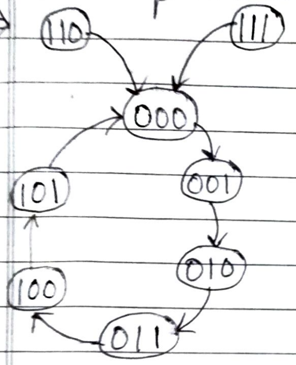


SD
QD
RD
QD
SC
QC
RC
QC
SB
QB
RB
QB
SA
QA
RA
QA

correcting

* Synthesized (Self control counter/lockout condition)

1 Consider a design of MOD 6 counter i.e, it has to be count from 000 to 101, but by chance if 110 & 111 conditions are counted by counter. It won't have any values & we logoff the counter i.e, go for any of the loop in that condition

⇒ 

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	0	0	0	X	1	0	X	X	1
1	1	0	0	0	0	X	1	X	1	0	X
1	1	1	0	0	0	X	1	X	1	X	1

	$\bar{Q}_B\bar{Q}_A$	$\bar{Q}_B Q_A$	$Q_B Q_A$	$Q_B\bar{Q}_A$
$\bar{Q}_C$	0	0	1	0
Q_C	X	X	X	X

$J_C = Q_B Q_A$

	X	X	X	X
	0	1	1	1

$K_C = Q_A + Q_B$

0	1	X	X
0	0	X	X

$J_B = \overline{Q}_C Q_A$

X	X	1	0
X	X	1	1

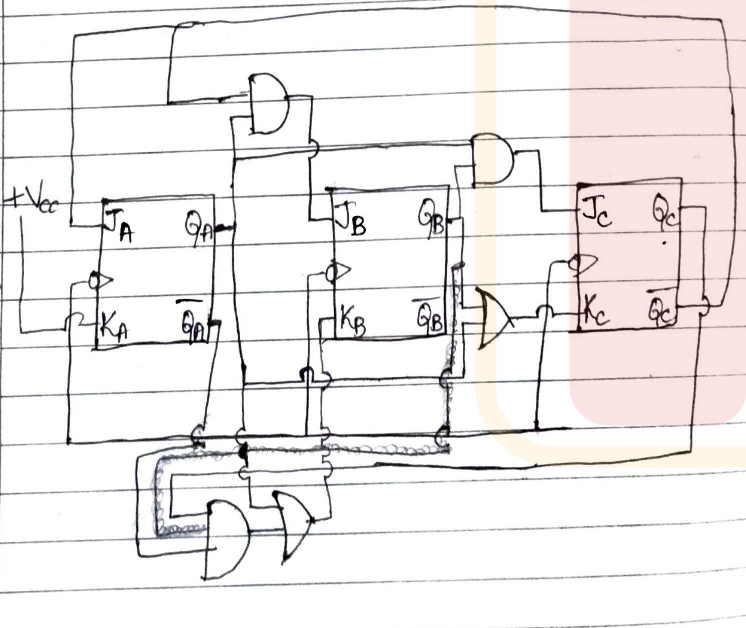
$K_B = Q_A + Q_C \overline{Q}_A$

1	X	X	1
1	X	X	0

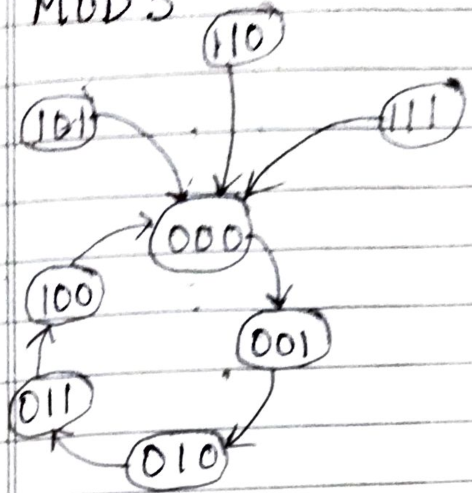
$J_A = \overline{Q}_C$

X	1	X	1
X	1	1	X

$K_A = 1$



2 MOD 5



Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	0	0	0	X	1	0	X	0	X
1	0	1	0	0	0	X	1	0	X	X	1
1	1	0	0	0	0	X	1	X	1	0	X
1	1	1	0	0	0	X	1	X	1	X	1

	$\overline{Q_B}\,\overline{Q_A}$	$\overline{Q_B}Q_A$	Q_BQ_A	$Q_B\overline{Q_A}$
$\overline{Q_C}$	0	0	1	0
Q_C	X	X	X	X

$\boxed{J_C = Q_B Q_A}$

	X	X	X	X
	1	1	1	1

$\boxed{K_C = 1}$

	0	1	X	X
	0	0	X	X

$\boxed{J_B = \overline{Q_C} Q_A}$

	X	X	1	0
	X	X	1	1

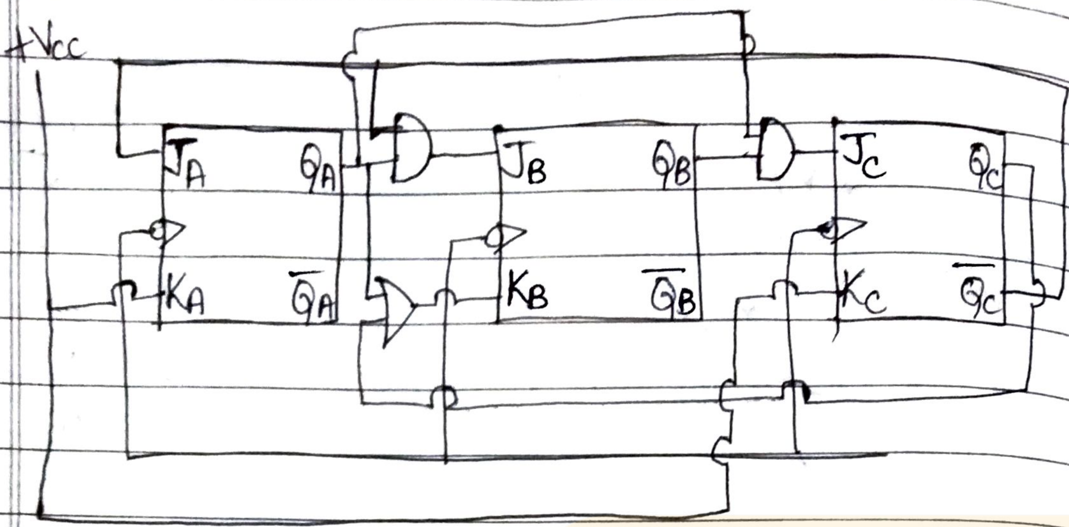
$\boxed{K_B = Q_C + Q_A}$

	1	X	X	1
	0	X	X	0

$\boxed{J_A = \overline{Q_C}}$

	X	1	1	X
	X	1	1	X

$\boxed{K_A = 1}$



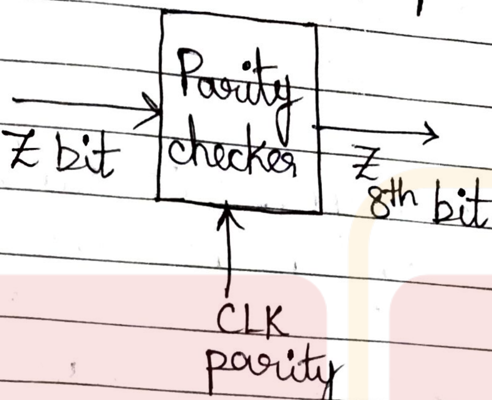
* Difference b/w sequential & combinational logic ckt

Sequential logic ckt	Combinational logic ckt
* It is a logic ckt whose o/p not only depends on present i/p but also depends on previous o/p	* It is a logic ckt whose o/p depend only on present i/p
* It is less speed	* It is more speed
* They are time dependent	* They are time independent
* They have the capability to store data	* They do not have capability to store data
* They have memory	* They donot have memory

* A sequential parity checker & generator

A module which accepts binary bit with a clock & generates 1 bit parity as an o/p is said to be a parity generator Ex:- 7 bit i/p is given to parity generator module to obtain 8 bit as parity bit

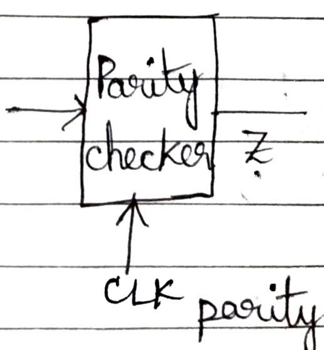
Ex:



0 0 0 0 0 0 0 1
1 0 1 0 0 0 1 0
1 1 1 1 1 1 1 0
1 1 0 0 1 1 0 1
1 1 1 1 0 0 1 0

By the generated no. of bit (8 bit) is given to parity checker to check whether the no. of bits sent from the sender is corrupted or not

parity 0 → False
Ex:- 1 0 1 0 0 0 1 1   1 → True

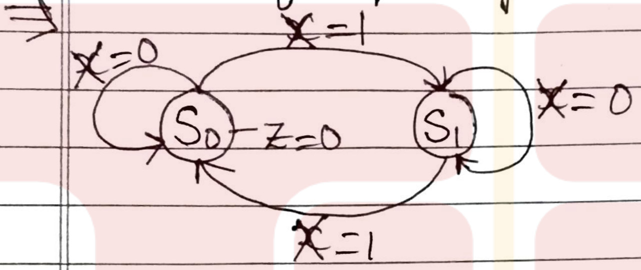


Z = 0

1010001   Z = 1

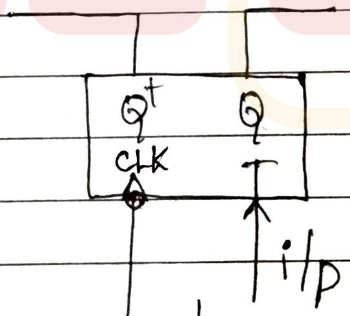
* We use T Flipflop to construct PC module where x acts as i/p when $x=1$ it toggles when $x=0$ it is a memory
* We are considering only 2 states for i/p 0 & 1. If $Q=0$ then it is in state S_0 & when $Q=1$ then it is in state S_1 where Q is a present state Q^+ is a next state
$T=1$ if Q & Q^+ differ
$T=0$ if Q & Q^+ common.

1 Design a state graph, state table & a state module for parity checker using T flipflop



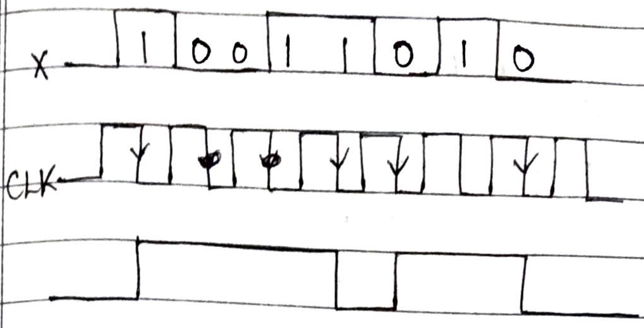
State	X=0	X=1
S_0	S_0	S_1
S_1	S_1	S_0

State	X=0	X=1	Present o/p	Q	Q^+ X=0	Q^+ X=1	T FF X=0	T FF X=1
S_0	S_0	S_1	0	0	0	1	0	1
S_1	S_1	S_0	1	1	1	0	0	1



i/p	S_1	S_0	o/p n Q_n		o/p n+1 Q_{n+1}	
	0	0	0	1	0	0
	0	1	0	1	1	1
	1	0	0	1	1	1
	1	1	0	1	0	0

$X = 10011010$



Before FF start the transition for PC it resets to start state So reset to zero

State table & Graph

To construct ST & SG we use 2 method of construction

1 Moore transition
2 Mealy transition

The following methods can be used to construct transition ~~state~~ table

The FF i/p eq^n & o/p eq^n are as shown below

$DA = X \oplus B'$

$DB = X + A$

$Z = A \oplus B$

The next state eq^n for FF i.e

$A^+ = X \oplus B'$

$B^+ = X + A$

		A^+		B^+		
A	B	X= 0	1	X= 0	1	Z
0	0	1	0	0	1	0
0	1	0	1	0	1	1
1	0	0	1	1	1	0
1	1	1	0	1	1	1

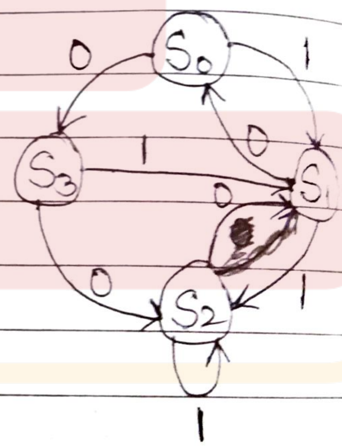
State Table

	A	B	A^+B^+ X=0	A^+B^+ X=1
S_0	0	0	1 0	0 1
S_1	0	1	0 0	1 1
S_2	1	0	0 1	1 1
S_3	1	1	1 1	0 1

$A^+ B'$

A B	X=0	X=1
S_0	S_3	S_1
S_1	S_0	S_2
S_2	S_1	S_2
S_3	S_2	S_1

AB	X=0	X=1	Z
S_0	S_3	S_1	0
S_1	S_0	S_2	1
S_2	S_1	S_2	0
S_3	S_2	S_1	1



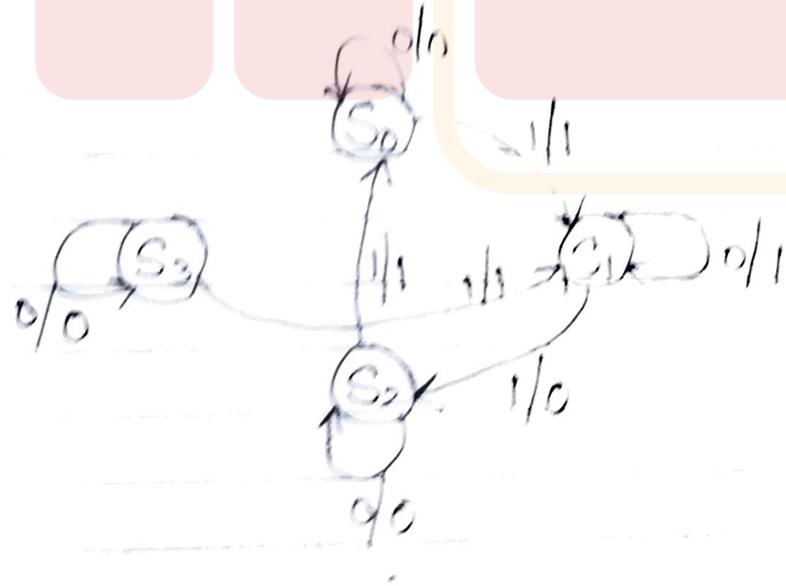
Mealy model using the below formulae

$A^+ = XBA' + X'A$
$B^+ = XB' + X'B + A'B$
$Z = X'A'B + XB' + XA$

		A'		B'			
A	B	X = 0	X = 1	X = 0	X = 1	Z	
S_0 0	0	0	0	0	1	0	1
S_1 0	1	0	1	1	1	1	0
S_2 1	0	1	0	1	0	0	1
S_3 1	1	1	0	0	1	0	1

$Z = X'A'B + XB' + XA$
$= 010 + 11 + 10$
$= 0 + 1 + 1 + 0$
$= 1$

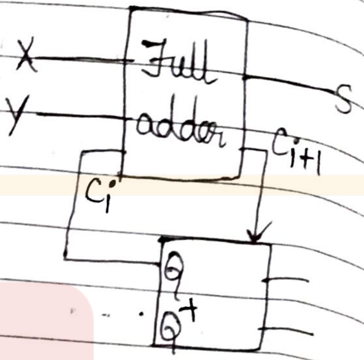
A B	X = 0	X = 1	
S_0	S_0	S_1	0 1
S_1	S_1	S_2	1 0
S_2	S_2	S_0	0 1
S_3	S_3	S_1	0 1

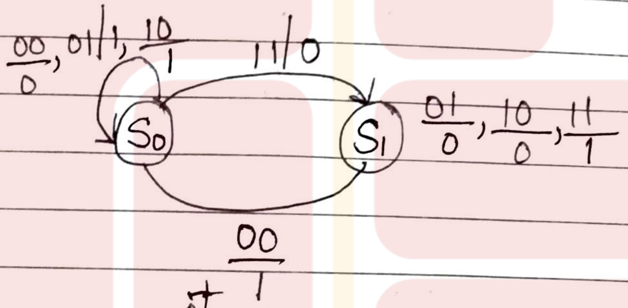


* Serial Adder

Construct SA using Mealy machine by constructing module using D FF

x	y	Ci	Ci+1	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



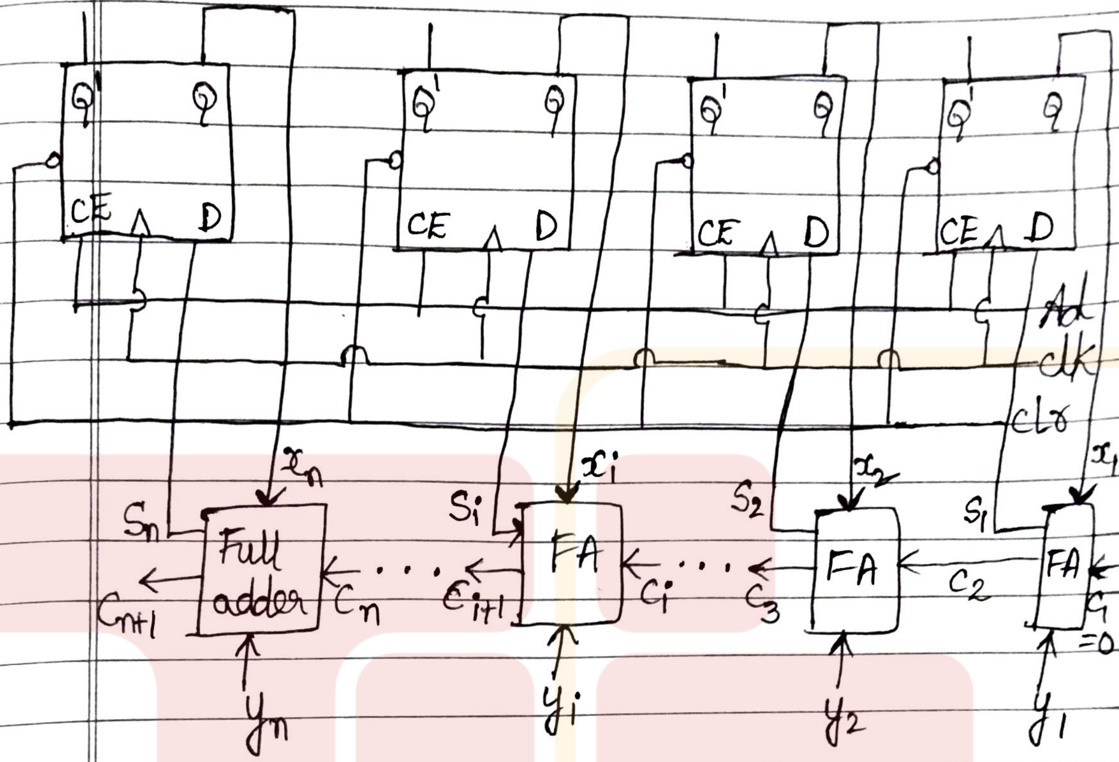


A^+

	AB	00	01	10	11
S_0	00	00	00	00	00
S_1	01	00	01	10	01
S_2	10	11	10		
S_3	11				

	Next state				Present o/p			
Present	00	01	10	11	00	01	10	11
S_0	S_3	S_2	S_1	S_0	00	10	11	01
S_1	S_0	S_1	S_2	S_1	10	10	11	11
S_2	S_3	S_0	S_1	S_1	00	10	11	01
S_3	S_2	S_2	S_1	S_0	00	00	01	01

V. Imp ✗ Parallel Adder Accumulator



With MUX