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SATHYANARAYANAN RAMESH BABU

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EDUCATION

Masters in Electrical and Computer Engineering **GPA: 3.38** (Jan 2014 – May 2016)
University of North Carolina at Charlotte, NC, USA

Bachelor in Electrical and Electronics Engineering **GPA: 3.00** (Sep 2009 - Jul 2013)
Sri Venkateswara College of Engineering-(Affiliated to Anna University), Chennai, India

TECHNICAL SKILLS

Programming/Scripting	C, C++, Python, CUDA C, Assembly Language Programming.
Compiler Directives/APIs	POSIX threads (pthreads), OpenMP, MPI, Standard Template Library.
Profiling Tools/Simulators	Intel V TUNE amplifier, GPROF, Valgrind,kcachegrind,QEMU.
Computer Architectures	Intel-CISC architecture. ARM-RISC architecture
Operating System concepts	Socket Programming, Client-Server Architecture, IPC, Concurrent programming and Synchronization, Real time scheduling, Virtual memory.
Courses	Computer Architecture, Fault Tolerant Systems, Reconfigurable Computing, Real Time Operating System, Control Systems, Performance Evaluation, Parallel Computing, Embedded Systems, Advanced Operating Systems

EXPERIENCE

Technical Intern(R&D) **SYNOPSYS Inc** (June-Sep – 2015)
Mountain View- California

Integrated the Synopsys-memory-module(MEM) with a mixed signal Fastspice simulator (Customsim-XA) and analyzed the performance of the simulator with and without MEM across various test cases using profiling tools.

GRADUATION PROJECT

Asynchronous Multi-threaded Implementation(using Pthreads) of Push Relabel Network Flow Algorithm and its Performance Analysis on Intel Xeon Architecture (May 2014 –present)

PROJECTS

Advanced Embedded Operating systems – XV6(Fall 2015-present)

Implemented 4 basic parts of the JOS kernel: Virtual memory, User process abstraction, interrupts and file systems.

- **Implementation of memory management infrastructure:** Implemented a physical page allocator that allocates and manages physical pages. Configured page directory and page table infrastructure for kernel and user processes to provide the user with an address space abstraction.
- **Interrupt and exception handling:** Configured the Interrupt Descriptor table, and wrote handlers for interrupt and exception handling. Also does protected control transfer from user to kernel mode for execution of system calls.
- **Simultaneous Multi processing**: Wrote Kernel level APIs to provide and manage 'process' abstraction to the user. Also supports inter-process communication between concurrent user processes. Simultaneous Multi-Processing for parallel execution of user processes and also pre-emptive multi-tasking using timer interrupts.
- **File Systems**: Implemented a basic Exo-kernel File System infrastructure.

Parallel Computing/Programming (Fall 2014)

- Developed and implemented parallel solutions using openMP, MPI and CUDA C for various mathematical problems (Ex. Monti Carlo π) and other contemporary Algorithms.

Performance analysis using Intel VTune Amplifier

- Performance optimization techniques using spatial and temporal locality was employed to various algorithms. Simple techniques to improve cache hit ratio were included and analysis was done using profiling tool, Intel VTune Amplifier.

Modelling and performance evaluation of computer systems (Fall 2015-present)

- A queuing theory driven approach for optimizing various computing resources was studied. Implementation of analytical models of different computer systems using Simulink's SimEvents library in MATLAB.
- Developed Linear Regression models and performed analysis based on confidence intervals of various real life data.

Multilevel Cache Simulator (Spring 2014)

- The simulator accepts Cache size, Victim cache size, Block replacement policy and associativity as input and builds a model of a functioning cache simulator to compute hits and misses for a given tracefile (valgrind).