**Intel Interview Questions - Freshers Stuff**  
  
1. Have you studied buses? What types?  
  
2. Have you studied pipelining? List the 5 stages of a 5 stage pipeline. Assuming 1 clock per stage, what is the latency of an instruction in a 5 stage machine? What is the throughput of this machine ?  
  
3. How many bit combinations are there in a byte?  
  
4. For a single computer processor computer system, what is the purpose of a processor cache and describe its operation?  
  
5. Explain the operation considering a two processor computer system with a cache for each processor.  
  
6. What are the main issues associated with multiprocessor caches and how might you solve them?  
  
7. Explain the difference between write through and write back cache.  
  
**8. Are you familiar with the term MESI?** Definite question they asked me also  
  
9. Are you familiar with the term snooping?  
  
10. Describe a finite state machine that will detect three consecutive coin tosses (of one coin) that results in heads.  
  
11. In what cases do you need to double clock a signal before presenting it to a synchronous state machine?  
  
12. You have a driver that drives a long signal & connects to an input device. At the input device there is either overshoot, undershoot or signal threshold violations, what can be done to correct this problem?  
  
13. What are the total number of lines written by you in C/C++? What is the most complicated/valuable program written in C/C++?  
  
14. What compiler was used?  
  
15. What is the difference between = and == in C?  
  
16. Are you familiar with VHDL and/or Verilog?  
  
17. What types of CMOS memories have you designed? What were their size? Speed?  
  
18. What work have you done on full chip Clock and Power distribution? What process technology and budgets were used?  
  
19. What types of I/O have you designed? What were their size? Speed? Configuration? Voltage requirements?  
  
20. Process technology? What package was used and how did you model the package/system? What parasitic effects were considered?  
21. What types of high speed CMOS circuits have you designed?  
  
22. What transistor level design tools are you proficient with? What types of designs were they used on?  
  
23. What products have you designed which have entered high volume production?  
  
24. What was your role in the silicon evaluation/product ramp? What tools did you use?  
  
25. If not into production, how far did you follow the design and why did not you see it into production?

**Hardware Architecture Interview Questions**  
  
   1. Are you familiar with the term MESI?  
  
   2. Are you familiar with the term snooping?  
  
   3. Describe a finite state machine that will detect three consecutive coin tosses (of one coin) that results in heads.  
  
   4. In what cases do you need to double clock a signal before presenting it to a synchronous state machine?  
  
   5. You have a driver that drives a long signal & connects to an input device. At the input device there is either overshoot, undershoot or signal threshold violations, what can be done to correct this problem?  
  
   6. For a single computer processor computer system, what is the purpose of a processor cache and describe its operation?  
  
   7. Explain the operation considering a two processor computer system with a cache for each processor.  
  
   8. What are the main issues associated with multiprocessor caches and how might you solve it?  
  
   9. Explain the difference between write through and write back cache.  
  
  10. What are the total number of lines written in C/C++? What is the most complicated/valuable program written in C/C++?  
  11. What compiler was used?  
  
  12. Have you studied busses? What types?  
  
  13. Have you studied pipelining? List the 5 stages of a 5 stage pipeline. Assuming 1 clock per stage, what is the latency of an instruction in a 5 stage machine? What is the throughput of this machine ?  
  
  14. How many bit combinations are there in a byte?  
  
  15. What is the difference between = and == in C?  
  
  16. Are you familiar with VHDL and/or Verilog?  
  
Read more: <http://discuss.itacumens.com/index.php/topic,19541.msg23116.html#msg23116#ixzz1FiHJTnTM>  
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**Hardware Design Interview Questions and Answers**  
  
   1. Give two ways of converting a two input NAND gate to an inverter  
  
   2. Given a circuit, draw its exact timing response. (I was given a Pseudo Random Signal Generator; you can expect any sequential ckt)  
  
   3. What are set up time & hold time constraints? What do they signify? Which one is critical for estimating maximum clock frequency of a circuit?  
  
   4. Give a circuit to divide frequency of clock cycle by two  
  
   5. Design a divide-by-3 sequential circuit with 50% duty circle. (Hint: Double the Clock)  
  
   6. Suppose you have a combinational circuit between two registers driven by a clock. What will you do if the delay of the combinational circuit is greater than your clock signal? (You can’t resize the combinational circuit transistors)  
  
   7. The answer to the above question is breaking the combinational circuit and pipelining it. What will be affected if you do this?  
  
   8. What are the different Adder circuits you studied?  
  
   9. Give the truth table for a Half Adder. Give a gate level implementation of the same.  
  
  10. Draw a Transmission Gate-based D-Latch.  
  
  11. Design a Transmission Gate based XOR. Now, how do you convert it to XNOR? (Without inverting the output)  
  
  12. How do you detect if two 8-bit signals are same?  
  
  13. How do you detect a sequence of "1101" arriving serially from a signal line?  
  
  14. Design any FSM in VHDL or Verilog.  
  
  15. Explain RC circuit.s charging and discharging.  
  
  16. Explain the working of a binary counter.  
  
  17. Describe how you would reverse a singly linked list.  
  
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**Frequent Intel interview questions**  
  
   1. Insights of an inverter. Explain the working?  
  
   2. Insights of a 2 input NOR gate. Explain the working?  
  
   3. Insights of a 2 input NAND gate. Explain the working?  
  
   4. Implement F= not (AB+CD) using CMOS gates?  
  
   5. Insights of a pass gate. Explain the working?  
  
   6. Why do we need both PMOS and NMOS transistors to implement a pass gate?  
  
   7. What does the above code synthesize to?  
  
   8. Cross section of a PMOS transistor?  
  
   9. Cross section of an NMOS transistor?  
  
  10. What is a D-latch? Write the VHDL Code for it?  
  
  11. Differences between D-Latch and D flip-flop?  
  
  12. Implement D flip-flop with a couple of latches? Write a VHDL Code for a D flip-flop?  
  
  13. What is latchup? Explain the methods used to prevent it?  
  
  14. What is charge sharing?  
  
  15. While using logic design, explain the various steps that r followed to obtain the desirable design in a well defined manner?  
  
  16. Why is OOPS called OOPS? (C++)  
  
  17. What is a linked list? Explain the 2 fields in a linked list?  
  
  18. Implement a 2 I/P and gate using Tran gates?  
  
  19. Insights of a 4bit adder/Sub Circuit?  
  
  20. For f = AB+CD if B is S-a-1, what r the test vectors needed to detect the fault?  
  
  21. Explain various adders and diff between them?  
  
  22. Explain the working of 4-bit Up/down Counter?  
  
  23. A circuit has 1 input X and 2 outputs A and B. If X = HIGH for 4 clock ticks, A = 1. If X = LOW for 4 clock ticks, B = 1. Draw a state diagram for this Spec?  
  
  24. Advantages and disadvantages of Mealy and Moore?  
  
  25. Id vs. Vds Characteristics of NMOS and PMOS transistors?  
  
  26. Explain the operation of a 6T-SRAM cell?  
  
  27. Differences between DRAM and SRAM?  
  
  28. Implement a function with both ratioed and domino logic and merits and demerits of each logic?  
  
  29. Given a circuit and asked to tell the output voltages of that circuit?  
  
  30. How can you construct both PMOS and NMOS on a single substrate?  
  
  31. What happens when the gate oxide is very thin?  
  
  32. What is setup time and hold time?  
  
  33. Write a pseudo code for sorting the numbers in an array?  
  
  34. What is pipelining and how can we increase throughput using pipelining?  
  
  35. Explain about stuck at fault models, scan design, BIST and IDDQ testing?  
  
  36. What is SPICE?  
  
  37. Differences between IRSIM and SPICE?  
  
  38. Differences between netlist of HSPICE and Spectre?  
  
  39. What is FPGA?  
  
  40. Draw the Cross Section of an Inverter? Clearly show all the connections between M1 and poly, M1 and diffusion layers etc?  
  
  41. Draw the Layout of an Inverter?  
  
  42. If the current thru the poly is 20nA and the contact can take a max current of 10nA how would u overcome the problem?  
  
  43. Implement F = AB+C using CMOS gates?  
  
  44. Working of a 2-stage OPAMP?  
  
  45. 6-T XOR gate?  
  
  46. Differences between blocking and Non-blocking statements in Verilog?  
  
  47. Differences between Signals and Variables in VHDL? If the same code is written using Signals and Variables what does it synthesize to?  
  
  48. Differences between functions and Procedures in VHDL?  
  
  49. What is component binding?  
  
  50. What is polymorphism? (C++)  
  
  51. What is hot electron effect?  
  
  52. Define threshold voltage?  
  
  53. Factors affecting Power Consumption on a chip?  
  
  54. Explain Clock Skew?  
  
  55. Why do we use a Clock tree?  
  
  56. Explain the various Capacitances associated with a transistor and which one of them is the most prominent?  
  
  57. Explain the Various steps in Synthesis?  
  
  58. Explain ASIC Design Flow?  
  
  59. Explain Custom Design Flow?  
  
  60. Why is Extraction performed?  
  
  61. What is LVS, DRC?  
  
  62. Who provides the DRC rules?  
  
  63. What is validation?  
  
  64. What is Cross Talk?  
  
  65. Different ways of implementing a comparator?  
  
  66. What r the phenomenon which come into play when the devices are scaled to the sub-micron lengths?  
  
  67. What is clock feed through?  
  
  68. Implement an Inverter using a single transistor?  
  
  69. What is Fowler-Nordheim Tunneling?  
  
  70. Insights of a Tri-state inverter?  
  
  71. If an/ap = 0.5, an/ap = 1, an/ap = 3, for 3 inverters draw the transfer characteristics?  
  
  72. Differences between Array and Booth Multipliers?  
  
  73. Explain the concept of a Clock Divider Circuit? Write a VHDL code for the same?  
  
  74. Which gate is normally preferred while implementing circuits using CMOS logic, NAND or NOR? Why?  
  
  75. Insights of a Tri-State Inverter?  
  
  76. Basic Stuff related to Perl?  
  
  77. Have you studied buses? What types?  
  
  78. Have you studied pipelining? List the 5 stages of a 5 stage pipeline. Assuming 1 clock per stage, what is the latency of an instruction in a 5 stage machine? What is the throughput of this machine ?  
  
  79. How many bit combinations are there in a byte?  
  
  80. For a single computer processor computer system, what is the purpose of a processor cache and describe its operation?  
  
  81. Explain the operation considering a two processor computer system with a cache for each processor.  
  
  82. What are the main issues associated with multiprocessor caches and how might you solve them?  
  
  83. Explain the difference between write through and write back cache.  
  
  84. Are you familiar with the term MESI?  
  
  85. Are you familiar with the term snooping?  
  
  86. Describe a finite state machine that will detect three consecutive coin tosses (of one coin) that results in heads.  
  
  87. In what cases do you need to double clock a signal before presenting it to a synchronous state machine?  
  
  88. You have a driver that drives a long signal & connects to an input device. At the input device there is either overshoot, undershoot or signal threshold violations, what can be done to correct this problem?  
  
  89. What are the total number of lines written by you in C/C++? What is the most complicated/valuable program written in C/C++?  
  
  90. What compiler was used?  
  
  91. What is the difference between = and == in C?  
  
  92. Are you familiar with VHDL and/or Verilog?  
  
  93. What types of CMOS memories have you designed? What were their size? Speed?  
  
  94. What work have you done on full chip Clock and Power distribution? What process technology and budgets were used?  
  
  95. What types of I/O have you designed? What were their size? Speed? Configuration? Voltage requirements?  
  
  96. Process technology? What package was used and how did you model the package/system? What parasitic effects were considered?  
  
  97. What types of high speed CMOS circuits have you designed?  
  
  98. What transistor level design tools are you proficient with? What types of designs were they used on?  
  
  99. What products have you designed which have entered high volume production?  
  
 100. What was your role in the silicon evaluation/product ramp? What tools did you use?  
  
 101. If not into production, how far did you follow the design and why did not you see it into production?  
  
Read more: <http://discuss.itacumens.com/index.php/topic,6713.msg6941.html#msg6941#ixzz1FiGQDfTm>

**VLSI and hardware engineering interview questions**  
  
   1.  Explain why & how a MOSFET works  
  
   2. Draw Vds-Ids curve for a MOSFET.  
  
Now, show how this curve changes (a) with increasing Vgs (b) with increasing transistor width (c) considering Channel Length Modulation  
  
   3. Explain the various MOSFET Capacitances & their significance  
  
   4. Draw a CMOS Inverter. Explain its transfer characteristics  
  
   5. Explain sizing of the inverter  
  
   6. How do you size NMOS and PMOS transistors to increase the threshold voltage?  
  
   7. What is Noise Margin? Explain the procedure to determine Noise Margin  
  
   8. Give the expression for CMOS switching power dissipation  
  
   9. What is Body Effect?  
  
  10. Describe the various effects of scaling  
  
  11. Give the expression for calculating Delay in CMOS circuit  
  
  12. What happens to delay if you increase load capacitance?  
  
  13. What happens to delay if we include a resistance at the output of a CMOS circuit?  
  
  14. What are the limitations in increasing the power supply to reduce delay?  
  
  15. How does Resistance of the metal lines vary with increasing thickness and increasing length?  
  
  16. You have three adjacent parallel metal lines. Two out of phase signals pass through the outer two metal lines. Draw the waveforms in the center metal line due to interference. Now, draw the signals if the signals in outer metal lines are in phase with each other  
  
  17. What happens if we increase the number of contacts or via from one metal layer to the next?  
  
  18. Draw a transistor level two input NAND gate. Explain its sizing (a) considering Vth (b) for equal rise and fall times  
  
  19. Let A & B be two inputs of the NAND gate. Say signal A arrives at the NAND gate later than signal B. To optimize delay, of the two series NMOS inputs A & B, which one would you place near the output?  
  
  20. Draw the stick diagram of a NOR gate. Optimize it  
  
  21. For CMOS logic, give the various techniques you know to minimize power consumption  
  
  22. What is Charge Sharing? Explain the Charge Sharing problem while sampling data from a Bus  
  
  23. Why do we gradually increase the size of inverters in buffer design? Why not give the output of a circuit to one large inverter?  
  
  24. In the design of a large inverter, why do we prefer to connect small transistors in parallel (thus increasing effective width) rather than lay out one transistor with large width?  
  
  25. Given a layout, draw its transistor level circuit. (I was given a 3 input AND gate and a 2 input Multiplexer. You can expect any simple 2 or 3 input gates)  
  
  26. Give the logic expression for an AOI gate. Draw its transistor level equivalent. Draw its stick diagram  
  
  27. Why don’t we use just one NMOS or PMOS transistor as a transmission gate?  
  
  28. For a NMOS transistor acting as a pass transistor, say the gate is connected to VDD, give the output for a square pulse input going from 0 to VDD  
  
  29. Draw a 6-T SRAM Cell and explain the Read and Write operations  
  
  30. Draw the Differential Sense Amplifier and explain its working. Any idea how to size this circuit? (Consider Channel Length Modulation)  
  
  31. What happens if we use an Inverter instead of the Differential Sense Amplifier?  
  
  32. Draw the SRAM Write Circuitry  
  
  33. Approximately, what were the sizes of your transistors in the SRAM cell? How did you arrive at those sizes?  
  
  34. How does the size of PMOS Pull Up transistors (for bit & bit- lines) affect SRAM’s performance?  
  
  35. What’s the critical path in a SRAM?  
  
  36. Draw the timing diagram for a SRAM Read. What happens if we delay the enabling of Clock signal?  
  
  37. Give a big picture of the entire SRAM Layout showing your placements of SRAM Cells, Row Decoders, Column Decoders, Read Circuit, Write Circuit and Buffers  
  
  38. In a SRAM layout, which metal layers would you prefer for Word Lines and Bit Lines? Why?  
  
  39. How can you model a SRAM at RTL Level?  
  
  40. What’s the difference between Testing & Verification?  
  
  41. For an AND-OR implementation of a two input Mux, how do you test for Stuck-At-0 and Stuck-At-1 faults at the internal nodes?  
 (You can expect a circuit with some redundant logic)  
  
  42. What is Latch Up? Explain Latch Up with cross section of a CMOS Inverter. How do you avoid Latch Up?  
  
Read more: <http://discuss.itacumens.com/index.php/topic,6681.msg6907.html#msg6907#ixzz1FiI30PKf>

**Hardware Based Interview Questions and Answers**  
  
   1. What is a Microprocessor? - Microprocessor is a program-controlled device, which fetches the instructions from memory, decodes and executes the instructions. Most Micro Processor are single- chip devices.  
  
   2. Give examples for 8 / 16 / 32 bit Microprocessor? - 8-bit Processor - 8085 / Z80 / 6800; 16-bit Processor - 8086 / 68000 / Z8000; 32-bit Processor - 80386 / 80486.  
  
   3. Why 8085 processor is called an 8 bit processor? - Because 8085 processor has 8 bit ALU (Arithmetic Logic Review). Similarly 8086 processor has 16 bit ALU.  
  
   4. What is 1st / 2nd / 3rd / 4th generation processor? - The processor made of PMOS / NMOS / HMOS / HCMOS technology is called 1st / 2nd / 3rd / 4th generation processor, and it is made up of 4 / 8 / 16 / 32 bits.  
  
   5. Define HCMOS? - High-density n- type Complimentary Metal Oxide Silicon field effect transistor.  
  
   6. What does microprocessor speed depend on? - The processing speed depends on DATA BUS WIDTH.  
  
   7. Is the address bus unidirectional? - The address bus is unidirectional because the address information is always given by the Micro Processor to address a memory location of an input / output devices.  
  
   8. Is the data bus is Bi-directional? - The data bus is Bi-directional because the same bus is used for transfer of data between Micro Processor and memory or input / output devices in both the direction.  
  
   9. What is the disadvantage of microprocessor? - It has limitations on the size of data. Most Microprocessor does not support floating-point operations.  
  
  10. What is the difference between microprocessor and microcontroller? - In Microprocessor more op-codes, few bit handling instructions. But in Microcontroller: fewer op-codes, more bit handling Instructions, and also it is defined as a device that includes micro processor, memory, & input / output signal lines on a single chip.  
  
  11. What is meant by LATCH? - Latch is a D- type flip-flop used as a temporary storage device controlled by a timing signal, which can store 0 or 1. The primary function of a Latch is data storage. It is used in output devices such as LED, to hold the data for display.  
  
  12. Why does microprocessor contain ROM chips? - Microprocessor contain ROM chip because it contain instructions to execute data.  
  
  13. What is the difference between primary & secondary storage device? - In primary storage device the storage capacity is limited. It has a volatile memory. In secondary storage device the storage capacity is larger. It is a nonvolatile memory. Primary devices are: RAM / ROM. Secondary devices are: Floppy disc / Hard disk.  
  
  14. Difference between static and dynamic RAM? - Static RAM: No refreshing, 6 to 8 MOS transistors are required to form one memory cell, Information stored as voltage level in a flip flop. Dynamic RAM: Refreshed periodically, 3 to 4 transistors are required to form one memory cell, Information is stored as a charge in the gate to substrate capacitance.  
  
  15. What is interrupt? - Interrupt is a signal send by external device to the processor so as to request the processor to perform a particular work.  
  
  16. What is cache memory? - Cache memory is a small high-speed memory. It is used for temporary storage of data & information between the main memory and the CPU (center processing unit). The cache memory is only in RAM.  
  
  17. What is called .Scratch pad of computer.? - Cache Memory is scratch pad of computer.  
  
  18. Which transistor is used in each cell of EPROM? - Floating .gate Avalanche Injection MOS (FAMOS) transistor is used in each cell of EPROM.  
  
  19. Differentiate between RAM and ROM? - RAM: Read / Write memory, High Speed, Volatile Memory. ROM: Read only memory, Low Speed, Non Voliate Memory.  
  
  20. What is a compiler? - Compiler is used to translate the high-level language program into machine code at a time. It doesn.t   
require special instruction to store in a memory, it stores automatically. The Execution time is less compared to Interpreter.  
  
  21. Which processor structure is pipelined? - All x86 processors have pipelined structure.  
  
  22. What is flag? - Flag is a flip-flop used to store the information about the status of a processor and the status of the instruction executed most recently  
  
  23. What is stack? - Stack is a portion of RAM used for saving the content of Program Counter and general purpose registers.  
  
  24. Can ROM be used as stack? - ROM cannot be used as stack because it is not possible to write to ROM.  
  
  25. What is NV-RAM? - Nonvolatile Read Write Memory, also called Flash memory. It is also know as shadow RAM  
  
Read more: <http://discuss.itacumens.com/index.php/topic,48023.msg64519.html#msg64519#ixzz1FiH6NqlE>