DADDA MULTIPLIER DELAY ANALYSIS

Each layer will give maximum of one full adder delay and the last layer gives the delay of the brent kung adder. It can be seen from the dot diagram of the multiplier. So the total delay is given by

Total delay=6(full adder delay)+1(brent kung adder)+routing delay.

Cell:in->out	fanout	0000		Logical Name (Net Name)
IBUF:I->O	23	0.715		mltpd 4 IBUF (mltpd 4 IBUF)
LUT2: I1->0	2	0.479	1.040	partial_products[0].p5/cl (part_prod<4><0>)
LUT4: I0->0	2			fll5/Mxor sum xo<0>1 (sixth 1<4>)
LUT4: I0->0	2	0.479	1.040	last_stage[4].fl20/Mxor_sum_xo<0>1 (seventh_1<4>)
LUT3: I0->0	2	0.479	0.915	b1/Mxor sum<5> Result SW0 (N392)
LUT3:I1->0	2	0.479	1.040	b1/carry2[1].g8/out1 (b1/carry<6>)
LUT3:10->0	3	0.479	0.941	bl/Mxor sum<7> Result SWO (N394)
LUT3: I1->0	2	0.479	0.804	bl/fourth order[0].g4/outl (bl/carry<8>)
LUT3:12->0	1	0.479	0.740	b1/carry2[2].g8/out1 SW0 (N424)
LUT3: I2->0	3	0.479	0.830	b1/carry2[2].g8/outl (b1/carry3[1].g9/out20)
LUT3:12->0	1	0.479	0.740	b1/carry3[1].g9/out50 SW0 (N428)
LUT3:12->0	5		0.953	
LUT4:I1->0	1	0.479	0.976	bl/fifth order[0].g5/out29 (bl/fifth order[0].g5/out29
LUT4: I0->0	5	0.479	0.842	bl/fifth order[0].g5/out57 (bl/carry<16>)
LUT4:12->0	1	0.479	0.740	b1/carry3[2].g9/out30 (b1/carry3[2].g9/out30)
LUT4: I2->0	5	0.479	0.953	b1/carry3[2].g9/out77 (b1/carry<20>)
LUT4: I1->0	1	0.479	0.976	b1/g12/out29 (b1/g12/out29)
LUT4: I0->0	2	0.479	1.040	b1/g12/out57 (b1/carry<24>)
LUT3:10->0	2	0.479	0.915	b1/Mxor sum<25> Result SWO (N408)
LUT3: I1->0	2	0.479	1.040	b1/carry2[6].g8/out1 (b1/carry<26>)
LUT3: I0->0	2	0.479	0.915	b1/Mxor sum<27> Result SW0 (N410)
LUT3:I1->0	2	0.479	1.040	b1/carry3[3].g9/out1 (b1/carry<28>)
LUT3:10->0	2	0.479	0.915	b1/Mxor sum<29> Result SWO (N412)
LUT3: I1->0	2	0.479	1.040	b1/carry2[7].g8/out1 (b1/carry<30>)
LUT4:10->0	1	0.479	0.681	b1/Mxor_sum<30> Result1 (product 30 OBUF)
OBUF: I->O		4.909		product_30_OBUF (product<30>)

40.896ns (17.120ns logic, 23.776ns route) (41.9% logic, 58.1% route)