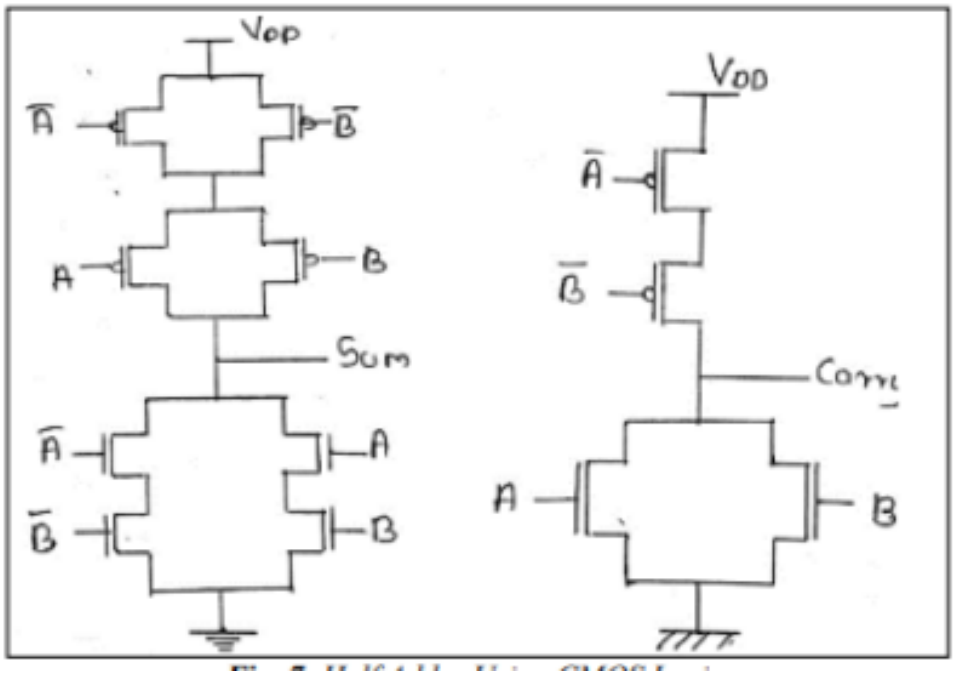
IMPLEMENTATION OF HALF ADDER USING 28nm FOR CMOS TECHNOLOGY

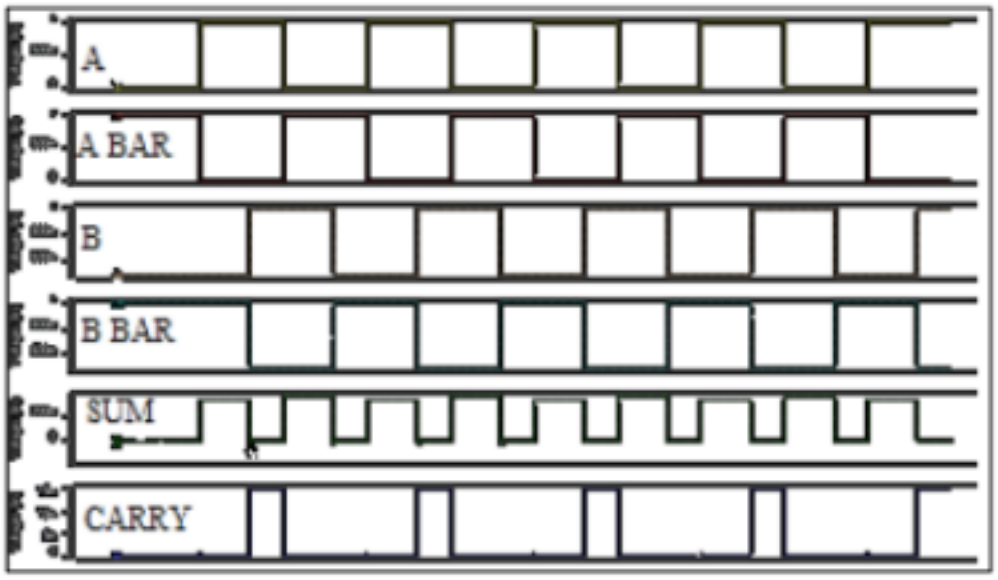
Abstract:

A half adder is a digital logic circuit that performs addition of two single bit binary numbers. Generally, in various types of processors, adders are used to perform arithmetic and logical operations . In this paper, working of half adder is analysed by designing it by using CMOS logic Technology. Simulation of the circuits is carried out using Synopsys tool at 28nm technologies at 1V power supply.

Reference Circuit Diagram



Reference Waveforms



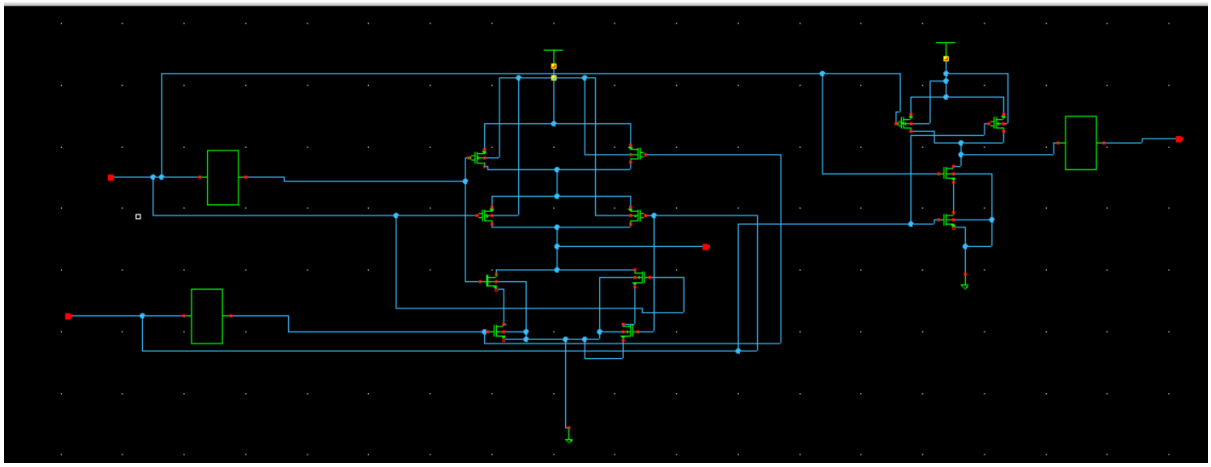
Truth table:

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

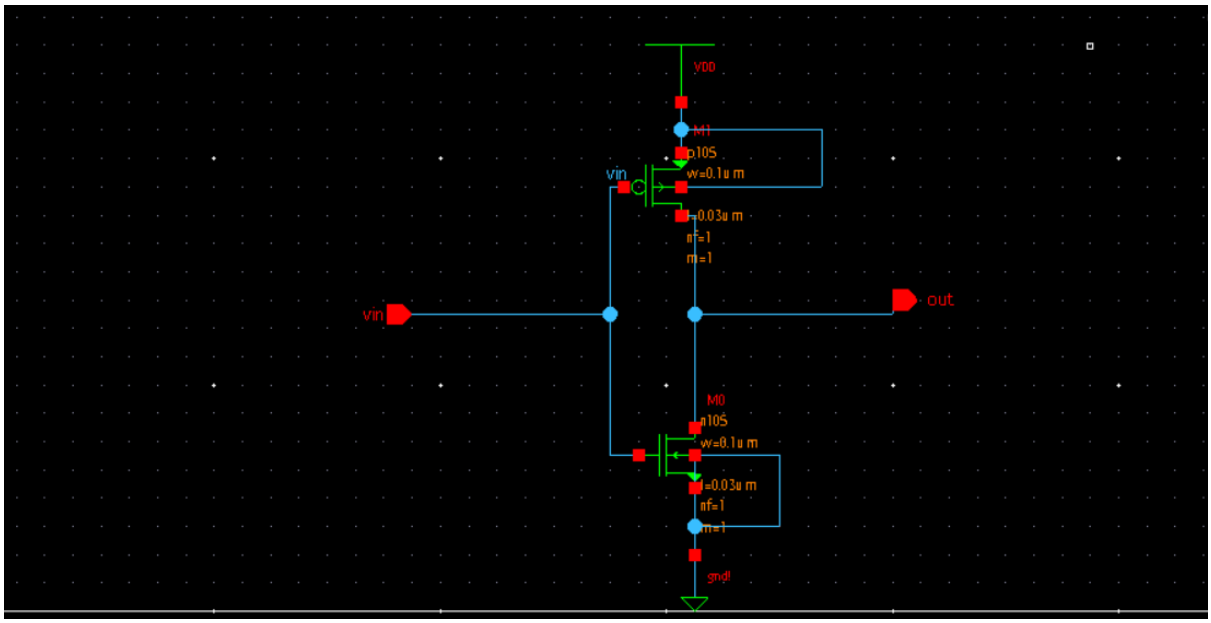
Circuit Details

Half adder [3] is a digital combinational circuit that executes addition of two single bit binary numbers and generates two outputs i.e., a sum bit (S) and carry bit (C). If A and B are taken as primary input bits, then sum bit (S) is obtained by X-ORing of input bits A and B and the carry bit (C) is obtained by ANDing of input bits A and B [4]. Complementary Metal Oxide Semiconductor (CMOS) logic deploys symmetric number of both types of MOSFETs, i.e., pMOS and nMOS. This leads to better performance of any logic circuit since nMOS is strong '0' device and pMOS is strong '1'device. Thus, CMOS provides complete '1' and complete '0' logics at the output without any distortion. Half Adder using CMOS modeled using 12 transistors as shown in below.

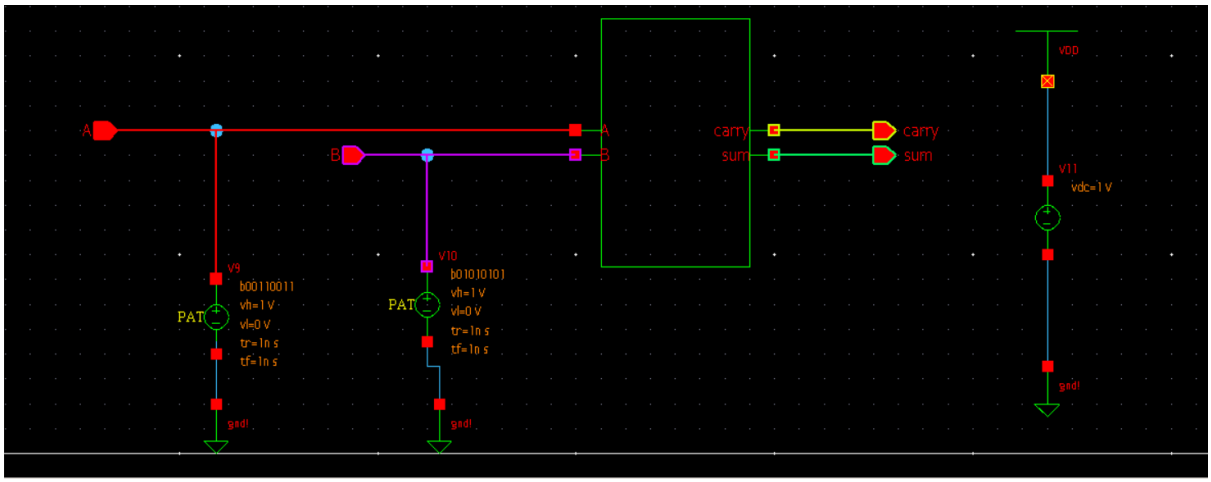
Schematic Diagram



Internal structure of inverter



Symbol Diagram



Parameter set of voltage source for input A

Property Editor (9)

Current Inst A

Parameters

Prompt	Value
DC Voltage	0 V
Voltage High	1 V
Voltage Low	0 V
Delay Time	10n s
Rise Time	1n s
Fall Time	1n s
Sample Time	30n
Data	b00110011
Repeat	10s s
Repeat Bit	
AC Magnitude	
AC Phase	
# HB Tones	0
DC Resistance	
AC Resistance	
HB Resistance	

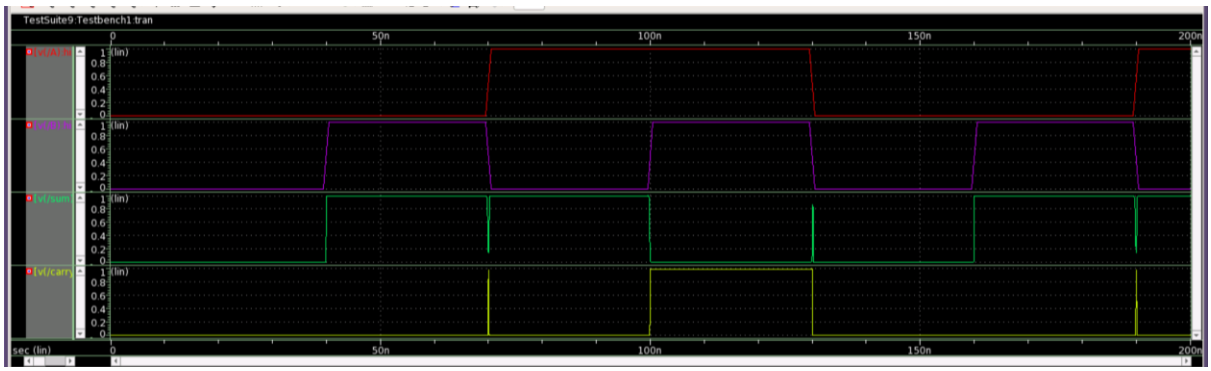
Parameter set of voltage source for input B

Current Inst B

Parameters

Prompt	Value
DC Voltage	0 V
Voltage High	1 V
Voltage Low	0 V
Delay Time	10n s
Rise Time	1n s
Fall Time	1n s
Sample Time	30n
Data	b01010101
Repeat	10s s
Repeat Bit	
AC Magnitude	
AC Phase	
# HB Tones	0
DC Resistance	
AC Resistance	
HB Resistance	

Output Waveforms



Netlist

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*  Generated for: PrimeSim
*  Design library name: cp_lib1
*  Design cell name: halfadder_tb
*  Design view name: schematic
.lib '/PDK/SAED_PDK32nm/hspice/saed32nm.lib' TT


*Custom Compiler Version S-2021.09
*Fri Feb 25 04:34:41 2022


.global vdd gnd!
********************************************************************************
* Library         : cp_lib1
* Cell            : cp_inv
* View            : schematic
* View Search List : hspice hspiceD schematic spice veriloga
* View Stop List   : hspice hspiceD
********************************************************************************
.subckt cp_inv out vin
xm0 out vin gnd! gnd! n105 w=0.1u l=0.03u nf=1 m=1
xm1 out vin vdd vdd p105 w=0.1u l=0.03u nf=1 m=1
.ends cp_inv


********************************************************************************
* Library         : cp_lib1
* Cell            : hafadder1
* View            : schematic
* View Search List : hspice hspiceD schematic spice veriloga
* View Stop List   : hspice hspiceD
********************************************************************************
.subckt hafadder1 a b carry sum
```

```
xi25 carry net106 cp_inv
xi22 net103 a cp_inv
xi23 net85 b cp_inv
xm24 net106 b vdd vdd p105 w=0.1u l=0.03u nf=1 m=1
xm6 net106 a vdd vdd p105 w=0.1u l=0.03u nf=1 m=1
xm5 sum b net89 vdd p105 w=0.1u l=0.03u nf=1 m=1
xm4 sum a net89 vdd p105 w=0.1u l=0.03u nf=1 m=1
xm3 net89 net85 vdd vdd p105 w=0.1u l=0.03u nf=1 m=1
xm2 net89 net103 vdd vdd p105 w=0.1u l=0.03u nf=1 m=1
xm20 net115 b gnd! gnd! n105 w=0.1u l=0.03u nf=1 m=1
xm21 net106 a net115 gnd! n105 w=0.1u l=0.03u nf=1 m=1
xm11 net41 b gnd! gnd! n105 w=0.1u l=0.03u nf=1 m=1
xm10 sum a net41 gnd! n105 w=0.1u l=0.03u nf=1 m=1
xm9 net33 net85 gnd! gnd! n105 w=0.1u l=0.03u nf=1 m=1
xm8 sum net103 net33 gnd! n105 w=0.1u l=0.03u nf=1 m=1
.ends hafadder1

********************************************************************************
* Library        : cp_lib1
* Cell           : halfadder_tb
* View           : schematic
* View Search List : hspice hspiceD schematic spice veriloga
* View Stop List   : hspice hspiceD
********************************************************************************
xi8 a b carry sum hafadder1
v9 a gnd! dc=0 pat ( 1 0 10n 1n 1n 30n b00110011 r='10s' )
v10 b gnd! dc=0 pat ( 1 0 10n 1n 1n 30n b01010101 r='10s' )
v11 vdd gnd! dc=1
```

```
.tran '10n' '200n' name=tran


.option primesim_remove_probe_prefix = 0
.probe v(*) i(*) level=1
.probe tran v(a) v(b) v(carry) v(sum)

.temp 25




.option primesim_output=wdf



.option parhier = LOCAL









.end
```

Acknowledgement

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2. Chinmay panda, IIT Hyderabad
3. Sameer Durgoji, NIT Karnataka
4. Synopsys Team/Company
5. https://www.iith.ac.in/events/2022/02/15/Cloud-Based-Analog-IC-Design-Hackathon/

Conclusion

In this paper, comparison of half adder implemented using CMOS logic Technology has been reviewed on the basis of power consumption and transistor count. The circuits are simulated using Synopsys HSPICE tool at 28 nm technologies at 1V power supply. It is concluded that circuit designed by PTL is area efficient as it deploys minimum number of transistors as compared to CMOS design styles.

References

[1] Y Syamala, K Srilakshmi, and N Somasekhar Varma. design of low power cmos logic circuits using gate diffusion input (gdi) technique. In ternational Journal of VLSI design & Communication Systems (VLSICS) Vol, 4, 2013.

[2] Arun Pratap Singh Rathod , Brijesh Kumar, SC Yadav, and Poornima Mittal. Low power vlsi design using pass transistor logic. National Technical Expo, pages 2455–1872, 2014.

[3] Ishika Sharma and Rajesh Mehra. Delay analysis of half subtractor using cmos and pass transistor logic. International Journal of Computer Application, 141:12–16, 2016.

[4] Ravi Kumar Anand, Kartar Singh, Pankaj Verma, and Ashish Thakur. De sign of area and power efficient half adder using transmission gate. inter national Journal of Research in Engineering and Technology, 4(04):122– 125, 2015