StrongArm Latch based Analog Comparator

Satish Kumar L
Electrical and Electronics Engineering
National Institute of Technology , Tiruchirappalli

***Abstract*—In this paper , a high speed clocked analog comparator with the strongArm latch as comparator core followed by a RS latch is designed using 28nm CMOS technology and its performance parameters such as input offset, speed, power consumption, input and kickback noise are evaluated.**

***Index Terms*—StrongArm Latch, RS Latch, clocked comparator, offset, speed, kickback noise**

I. Introduction

A differential Comparator is an integral part of analog to digital converters where it is used to perform quantisation and sampling. A standard opamp as a comparator is not preferred for these applications as it reduces the maximum sampling frequency that could be attained. In this design, a strongArm latch is used as the comparator core and is chosen as the core for this circuit because it consumes zero static power, produces full swing rail to rail outputs, requires single clock phase and provides higher sampling bandwidth. The strongArm latch stage is followed by a RS latch which is used to hold the output data during precharge phase of the strongArm latch.

II. WORKING OF REFERENCE CIRCUIT

The latch consists of 5 NMOS and 5 PMOS transistors. Transistor M1 and M2 form the input differential pair, transistor M3-M6 form the cross coupled inverters, S1-S4 are the charging transistors and M7 is the tail current transistor. Operation of the latch consists of three phases, Reset, Amplification, and Regeneration.

During the reset phase, input clock is low which turns of the tail current transistor M7 and the input differential pair is disconnected. Nodes P,Q,X,Y charge to Vdd through the charging transistors which are on when clock is low.The entire circuit draws no current during reset phase.

The amplification phase begins as soon as clock goes from low to high turning off the charging transistors and turning on M7 thereby activating M1,M2 which draws current proportional to the differential input provided at gate terminals of M1 and M2 which discharges the nodes P and Q.

The regeneration phase begins when nodes P and Q discharge to Vdd-Vthn , turning M3 and M4 on. Nodes X and Y then begins discharging from Vdd. Since they form a cross coupled inverter with positive feedback, eventually one node regenerates back to Vdd and the other node falls to zero, depending on the polarity of input differential votalge.

During every reset phase, which lasts half a clock period both output Vx and Vy is Vdd which is an invalid state. For correct interpretation , a RS latch follows the strongArm latch whose inputs are buffered using inverters.

III. Reference Circuit Schematic

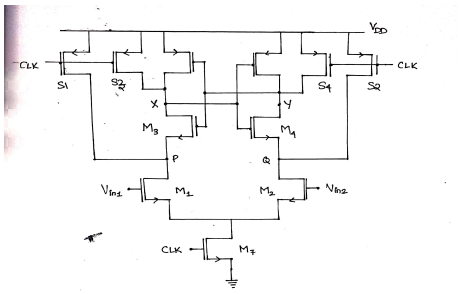

Fig. 1. Stage-1: SuperArm Latch

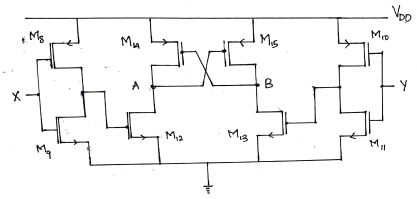

Fig. 2. Stage-2: RS Latch

IV. Expected Output Waveforms

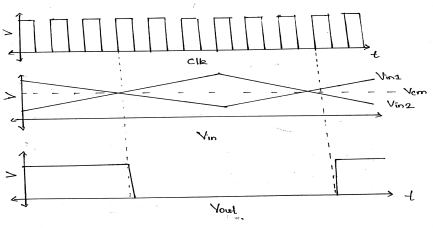

Fig. 3. Waveforms

References

[1] B. Razavi, "The StrongARM Latch [a circuit for all seasons]," IEEE Solid State Circuits Mag., vol. 7, no. 2, pp. 12–17, Spring 2015. doi: 10.1109/MSSC.2015.2418155.

[2] B. Razavi, "The Design of a Comparator [The Analog Mind]," in IEEE Solid-State Circuits Magazine, vol. 12, no. 4, pp. 8-14, Fall 2020, doi: 10.1109/MSSC.2020.3021865.

[3] A. Almansouri, A. Alturki, A. Alshehri, T. Al-Attar and H. Fariborzi, "Improved StrongARM latch comparator: Design, analysis and performance evaluation," 2017 13th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME), 2017, pp. 89-92, doi: 10.1109/PRIME.2017.7974114.

[4] R vinoth, S Ramasamy, "Design and Implementation of High Speed Latched Comparator using gm/Id Sizing Method