1. VLSI

1.1 Introduction to VLSI :

Very large-scale Integration (VLSI) is the process of creating an integrated circuit (IC) by combining millions of MOS transistors onto a single chip. VLSI began in the 1970s when MOS integrated circuit chips were widely adopted, enabling complex semiconductor and telecommunication technologies to be developed. The microprocessor and memory chips are VLSI devices. Before the introduction of VLSI technology, most ICs had a limited set of functions they could perform. An electronic circuit might consist of a CPU, ROM, RAM and glue logic. VLSI lets IC designers add all of these into one chip. General Microelectronics introduced the first commercial MOS integrated circuit in 1964. In the early 1970s, MOS integrated circuit technology allowed the integration of more than 10,000 transistors in a single chip. This paved the way for VLSI in the 1970s and 1980s, with tens of thousands of MOS transistors on a single chip (later hundreds of thousands, then millions, and now billions).

The first semiconductor chips held two transistors each. Subsequent advances added more transistors, and as a consequence, more individual functions or systems were integrated over time. The first integrated circuits held only a few devices, perhaps as many as ten diodes, transistors, resistors and capacitors, making it possible to fabricate one or more logic gates on a single device. Now known retrospectively as small-scale integration (SSI), improvements in technique led to devices with

hundreds of logic gates, known as medium-scale integration (MSI). Further improvements led to large-scale integration (LSI), i.e. systems with at least a thousand logic gates. Current technology has moved far past this mark and today's microprocessors have many millions of gates and billions of individual transistors.

At one time, there was an effort to name and calibrate various levels of large-scale integration above VLSI. Terms like ultra-large scale integration (ULSI) were used. But the huge number of gates and transistors available on common devices has rendered such fine distinction moot. Terms suggesting greater than VLSI levels of integration are no longer in widespread use.

In 2008, billion-transistor processors became commercially available. This became more commonplace as semiconductor fabrication advanced from the then-current generation of 65nm processors. Current designs, unlike the earliest devices, use extensive design automation and automated logic synthesis to lay out the transistors, enabling higher levels of complexity in the resulting logic functionality. Certain high- performance logic blocks like the SRAM (static random-access memory) cell, are still designed by hand to ensure the highest efficiency.

1.2 VLSI Design Flow :

The design process, at various levels, is usually evolutionary in nature. It starts with a given set of requirements. Initial design is developed and tested against the requirements. When requirements are not met, the design has to be

improved. If such improvement is either not possible or too costly, then the revision of requirements and its impact analysis must be considered. The Y-chart (first introduced by D. Gajski) shown in Fig. 1.4 illustrates a design flow for most logic chips, using design activities on three different axes (domains) which resemble the letter Y.

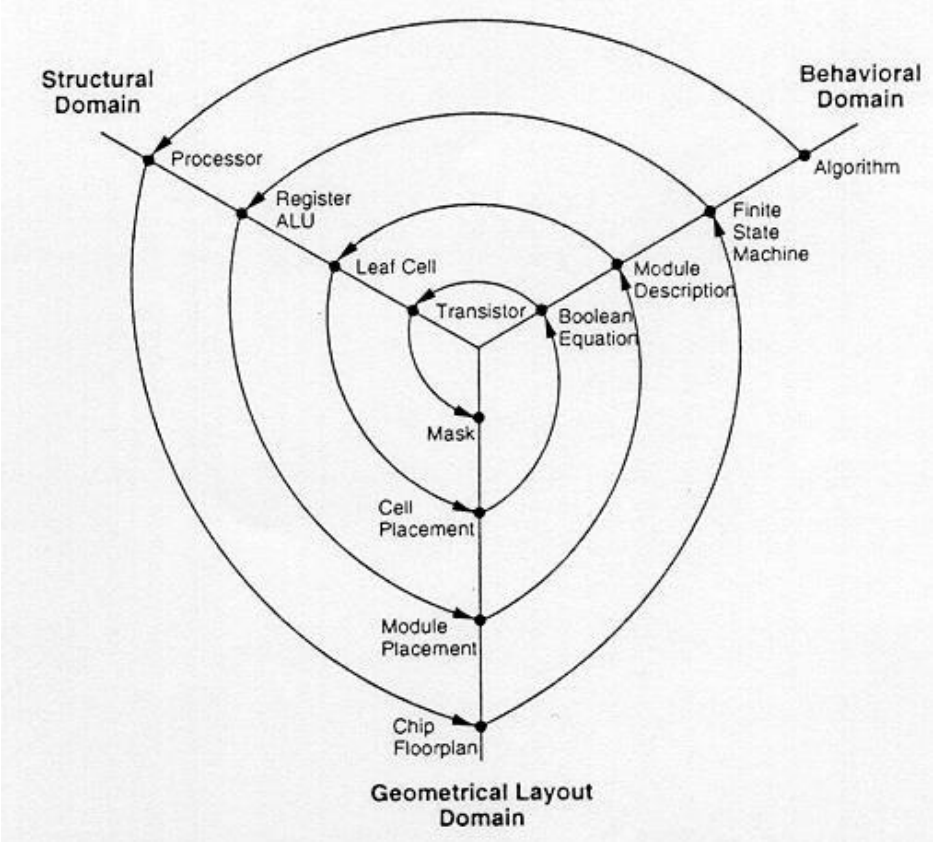


Fig:1.1 : Typical VLSI design flow in three domains (Y-chart representation).

The Y-chart consists of three major domains, namely:

- Behavioral domain,
- Structural domain,
- Geometrical layout domain.

The design flow starts from the algorithm that describes the behavior of the target chip. The corresponding architecture of the processor is first defined. It is mapped onto the chip surface by floor planning. The next design evolution in the

behavioral domain defines finite state machines (FSMs) which are structurally implemented with functional modules such as registers and arithmetic logic units (ALUs). These modules are then geometrically placed onto the chip surface using CAD tools for automatic module placement followed by routing, with a goal of minimizing the interconnects area and signal delays. The third evolution starts with a behavioral module description. Individual modules are then implemented with leaf cells. At this stage the chip is described in terms of logic gates (leaf cells), which can be placed and interconnected by using a cell placement & routing program. The last evolution involves a detailed Boolean description of leaf cells followed by a transistor level implementation of leaf cells and mask generation. In standard-cell based design, leaf cells are already pre-designed and stored in a library for logic design use.

Figure 1.2 provides a more simplified view of the VLSI design flow, taking into account the various representations, or abstractions of design - behavioral, logic, circuit and mask layout. Note that the verification of design plays a very important role in every step during this process. The failure to properly verify a design in its early phases typically causes significant and expensive re-design at a later stage, which ultimately increases the time-to-market. Although the design process has been described in linear fashion for simplicity, in reality there are many iterations back and forth, especially between any two neighboring steps, and occasionally even remotely separated pairs.

Although top-down design flow provides an excellent design process control, in reality, there is no truly unidirectional top-down design flow. Both top-down and bottom-up approaches have to be combined. For instance, if a chip designer defined architecture without close estimation of the corresponding chip area, then it is very likely that the resulting chip layout exceeds the area limit of the available technology. In such a case, in order to fit the architecture into the allowable chip area, some functions may have to be removed and the design process must be repeated.

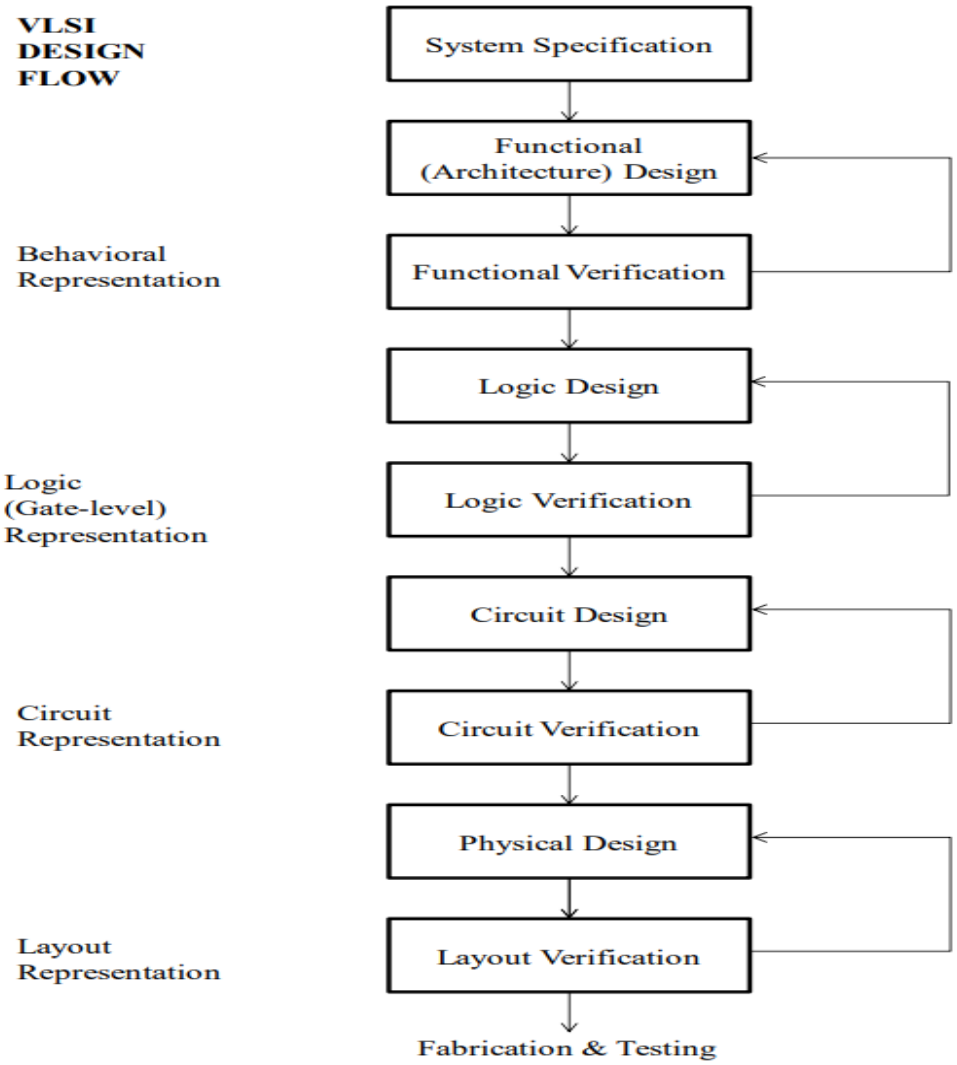


Fig 1.2 : A more simplified of VLSI design flow

1.3 History of Scale Integration :

The electronics industry has achieved a phenomenal growth over the last two decades, mainly due to the rapid advances in integration technologies, large-scale systems design - in short, due to the advent of VLSI. The number of applications of integrated circuits in high- performance computing, telecommunications, and consumer electronics has been rising steadily, and at a very fast pace. Typically, the required computational power (or, in other words, the intelligence) of these applications is the driving force for the fast development of this field. Figure 1.3 gives an overview of the prominent trends in information technologies over the next few decades. The current leading-edge technologies (such as low bit-rate video and cellular communications) already provide the end-users a certain amount of processing power and portability. This trend is expected to continue, with very important implications on VLSI and systems design. One of the most important characteristics of information services is their increasing need for very high processing power and bandwidth (in order to handle real-time video, for example).

The other important characteristic is that the information services tend to become more and more personalized (as opposed to collective services such as broadcasting), which means that the devices must be more intelligent to answer individual demands, and at the same time they must be portable to allow more flexibility/mobility.

The level of integration as measured by the number of logic gates in a monolithic chip has been steadily rising for almost

three decades, mainly due to the rapid progress in processing technology and interconnects technology. Table 1.1 shows the evolution of logic complexity in integrated circuits over the last three decades, and marks the milestones of each era. Here, the numbers for circuit complexity should be interpreted only as representative examples to show the order-of-magnitude. A logic block can contain anywhere from 10 to 100 transistors, depending on the function. State-of-the-art examples of ULSI chips, such as the DEC Alpha or the INTEL Pentium contain 3 to 6 million transistors.

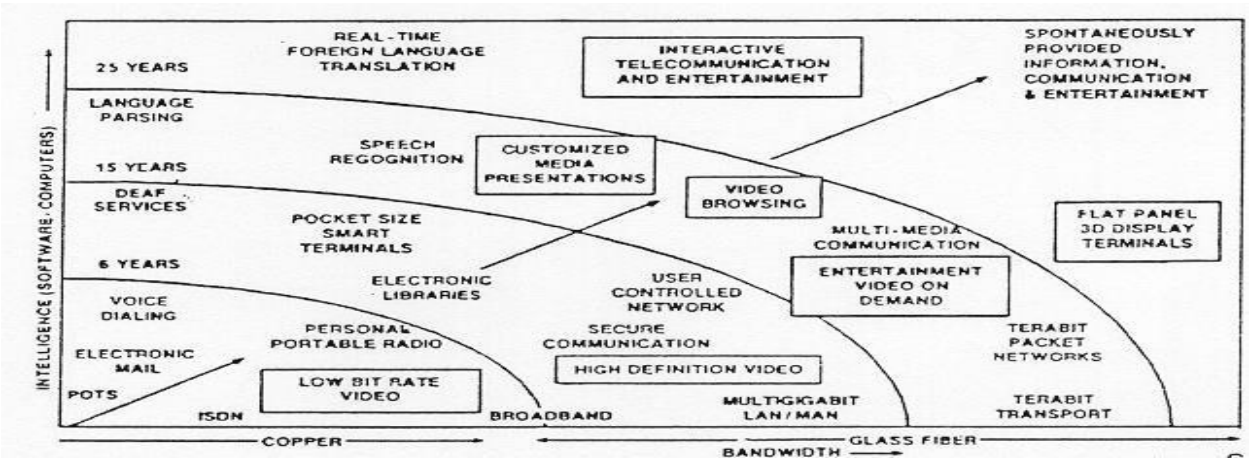


Fig 1.3: Prominent trends in information service technologies.

ERA (number of logic blocks per chip)	**Date**	**Complexity**
Single Transistor	1959	Less than 1
Unit logic (one gate)	1960	1
Multi-function	1962	2 – 4
Complex function	1964	5 – 20
Medium Scale integration	1967	20 – 200 (MSI)
Large Scale Integration	1972	200 – 2000 (LSI)
Very Large Scale Integration	1978	2000 – 20000 (VLSI)

Table 1.1: Evolution of logic complexity in integrated circuits.

The most important message here is that the logic complexity per chip has been (and still is) increasing exponentially. The monolithic integration of a large number of functions on a single chip usually provides:

- Less area/volume and therefore, compactness
- Less power consumption
- Less testing requirements at system level
- Higher reliability, mainly due to improve on-chip interconnects
- Higher speed, due to significantly reduced interconnection length
- Significant cost savings

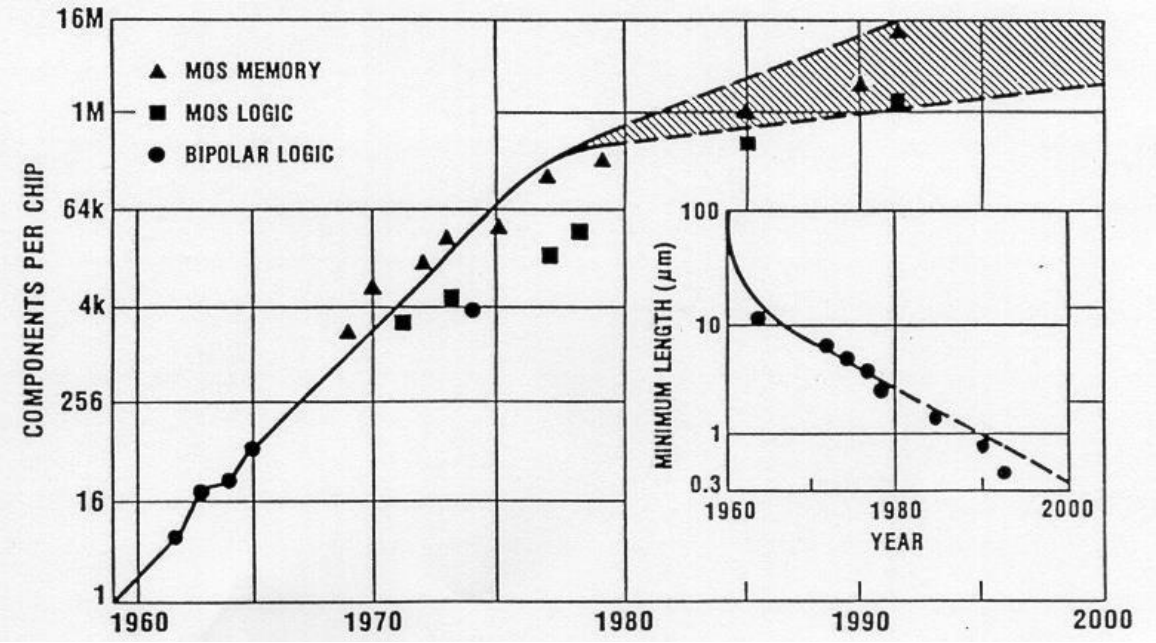


Figure-1.4: Evolution of integration density and minimum feature size, as seen in the early 1980s.

Therefore, the current trend of integration will also continue in the foreseeable future. Advances in device manufacturing technology, and especially the steady reduction of minimum feature size (minimum length of a transistor or an interconnect realizable on chip) support this trend. Figure 1.4 shows the history and forecast of chip complexity - and minimum feature size - over time, as seen in the early 1980s.

At that time, a minimum feature size of 0.3 microns was expected around the year 2000. The actual development of the technology, however, has far exceeded these expectations. A minimum size of 0.25 microns was readily achievable by the year 1995. As a direct result of this, the integration density has also exceeded previous expectations - the first 64 M-bit DRAM, and the INTEL Pentium microprocessor chip containing more than 3 million transistors were already available by 1994, pushing the envelope of integration density.

When comparing the integration density of integrated circuits, a clear distinction must be made between the memory chips and logic chips. Figure 1.5 shows the level of integration over time for memory and logic chips, starting in 1970. It can be observed that in terms of transistor count, logic chips contain significantly fewer transistors in any given year mainly due to large consumption of chip area for complex interconnects. Memory circuits are highly regular and thus more cells can be integrated with much less area for interconnects.

Generally speaking, logic chips such as microprocessor chips and digital signal processing (DSP) chips contain not only large arrays of memory (SRAM) cells, but also many different functional units. As a result, their design complexity is considered much higher than that of memory chips, although advanced memory chips contain some sophisticated logic functions. The design complexity of logic chips increases almost exponentially with the number

of transistors to be integrated. This is translated into the increase in the design cycle time, which is the time period from the start of the chip development until the mask-tape delivery time. However, in order to make the best use of the current technology, the chip development time has to be short enough to allow the maturing of chip manufacturing and timely delivery to customers. As a result, the level of actual logic integration tends to fall short of the integration level achievable with the current processing technology. Sophisticated computer- aided design (CAD) tools and methodologies are developed and applied in order to manage the rapidly increasing design complexity.

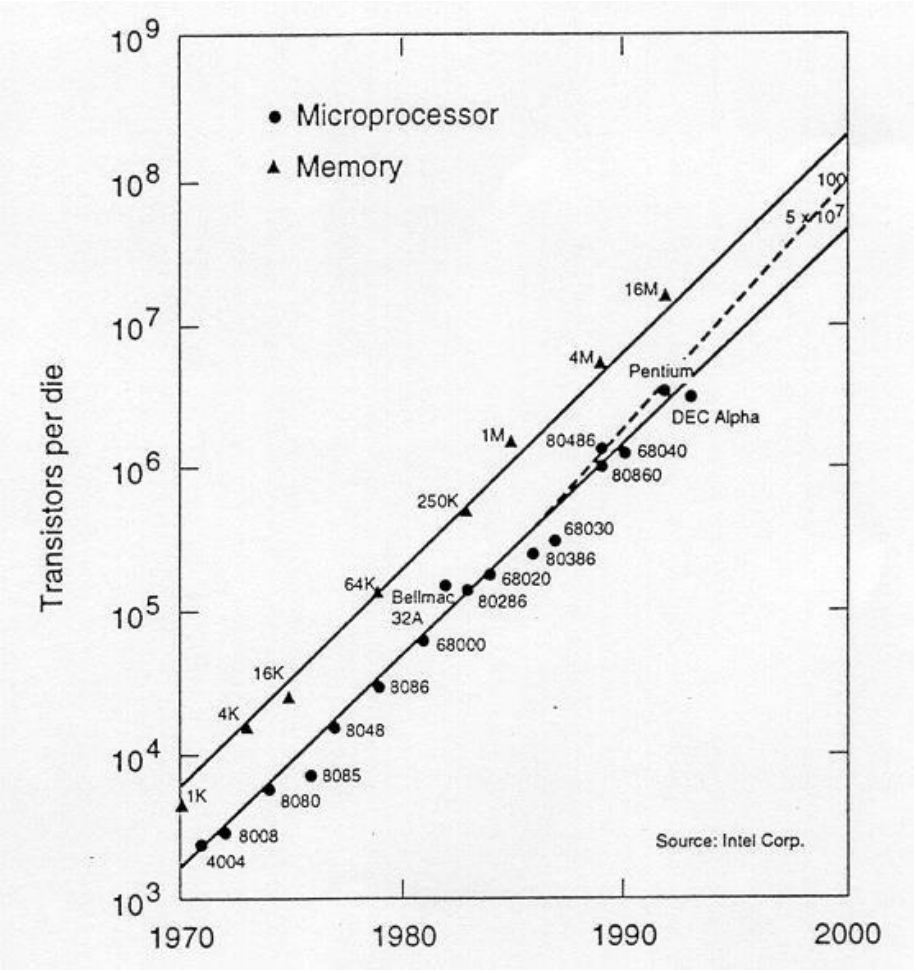


Figure-1.5: Level of integration over time, for memory chips and logic chips.

1.4 ADVANTAGES OF ICS OVER DISCRETE COMPONENTS:

- Extremely small size – Thousands times smaller than discrete circuits. It is because of fabrication of various circuit elements in a single chip of semiconductor material.
- Very small weight owing to miniaturized circuit.
- Very low cost because of simultaneous production of hundreds of similar circuits on a small semiconductor wafer. Owing to mass production of an IC costs as much as an individual transistor.
- More reliable because of elimination of soldered joints and need for fewer interconnections.
- Lower power consumption because of their smaller size.
- Easy replacement as it is more economical to replace them than to repair them.
- Increased operating speed because of absence of parasitic capacitance effect.
- Close matching of components and temperature coefficients because of bulk production in batches.
- Improved functional performance as more complex circuits can be fabricated for achieving better characteristics.
- Greater ability of operating at extreme temperatures.
- Suitable for small signal operation because of no chance of stray electrical pickup as various components of an INC are located very close to each other on a silicon wafer.

1.5 Advantages of VLSI :

The following are the primary advantages of VLSI technology:

- Reduced size for circuits
- Increased cost-effectiveness for devices
- Improved performance in terms of the operating speed of circuits
- Requires less power than discrete components
- Higher device reliability
- Requires less space and promotes miniaturization

1.6 Applications of VLSI :

- Defense
- Aerospace
- Wireless & Wire line Communication
- Consumer Electronics
- MEMS & Bio Electronics
- Medical Electronics
- Electronic Design Optimization

2. Literature Survey

[1]R. H. Dennard, F. H. Gaensslen, H.-N. Yu, V. L. Rideout, E. Bassous, and A. R. LeBlanc, "Design of ion-implanted MOSFET's with very smaller physical dimensions," IEEE J. Solid-State Circuits, vol. SSC-9, no. 5, pp. 256–268, Oct. 1974.

This paper considers the design, fabrication, and characterization of very small MOSFET switching devices suitable for digital integrated circuits using dimensions of the order of 1 p. Scaling relationships are presented which show how a conventional MOSFET can be reduced in size. An improved small device structure is presented that uses ion implantation to provide shallow source and drain regions and a nonuniform substrate doping profile. One-dimensional models are used to predict the substrate doping profile and the corresponding threshold voltage versus source voltage characteristic. A two-dimensional current transport model is used to predict the relative degree of short-channel effects for different device parameter combinations. Polysilicon-gate MOSFET'S with channel lengths as short as 0.5 ~ were fabricated, and the device characteristics measured and compared with predicted values.

The performance improvement expected from using these very small devices in highly miniaturized integrated circuits is projected. New high resolution lithographic techniques for forming semiconductor integrated circuit patterns offer a decrease in linewidth of five to ten times over the optical contact masking approach which is

commonly used in the semiconductor industry today. This paper concerns the design, fabrication, and characterization of very small MOSFET switching devices suitable for digital integrated circuits using dimensions of the order of 1 p. It is known that reducing the source to-drain spacing (i.e., the channel length) of an FET leads to undesirable changes in the device characteristics. These changes become significant when the depletion regions surrounding the source and drain extend over a large portion of the region in the silicon substrate under the gate electrode. For switching applications, the most undesirable "short-channel" effect is a reduction in the gate threshold voltage at which the device turns on, which is aggravated by high drain voltages. All of the equations that describe the MOSFET device characteristics will be scaled.

[2] A. J. García-Loureiro, K. Kalna, and A. Asenov, "Intrinsic fluctuations induced by a high-K gate dielectric in sub-100 nm Si MOSFETs," AIP Conf. Proc., vol. 780, no. 1, pp. 239–242, 2005.

In this work, an efficient 3D parallel simulator to study a Si metal-oxide semiconductor field effect transistor (MOSFET) with a high-κ gate stack. The simulator is employed to study the impact of the intrinsic parameter fluctuations within a high-κ dielectric on the threshold voltage and drive current. The large regions of crystal high-κ dielectrics with a lower dielectric constant than the amorphous high-κ lower the drive current by more than 100% and shifts threshold

voltage by 2 V. The same effect on the drive current and threshold voltage is observed when high-κ fluctuations follow a Gaussian distribution with a correlation length of 3 n. A major problem limiting the scaling of the conventional Si metal-oxide-semiconductor field effect transistors (MOSFETs) beyond the 45 nm technology node is the requirement of an extremely thin gate SiO2 layer which introduces intolerable gate tunnelling . The solution lies in the replacement of SiO2 or oxynitride by a high-κ dielectric material which provides the same equivalent oxide thickness (EOT) for a much larger physical thickness due to a higher dielectric constant but reduces the gate tunnel. The replacement of SiO2 by a high-κ dielectric material calls also for a replacement of the heavily doped polysilicon gate with a metal gate.

Most of the high-κ dielectrics exhibit a thermal instability which leads to the local crystallization of the initially amorphous high-κ layer. The fabrication of the metal gate can be carried out at a lower temperature thus preserving the amorphous state of the high-κ dielectric material as much as possible. Intrinsic fluctuations introduced by the discrete charge and interface roughness create problems when scaling MOSFETs to sub-100 nm dimensions. The introduction of the high-κ dielectric materials into the gate stacks brings also new sources of intrinsic fluctuations as: (i) islands of crystal materials with a different dielectric constant, (ii) trapped and fixed charges occurring at the boundaries of the islands, (iii) an interface roughness between the interfacial layer with a thickness of 1-

2 nm and the high-κ dielectric, and (iv) interface roughness between the high-κ dielectric and the metal gate. Constant Our 3D parallel device simulator originally developed for a modelling of heterostructure semiconductor devices was adapted to simulate MOSFET structures while preserving its capabilities to deal with a complex layer geometry.

[3] Bayerl, Albin; Lanza, Mario; Porti, Marc; Nafria, Montserrat; Aymerich, Xavier; Campabadal, F.; Benstetter, Günther (2011).” Nanoscale and Device Level Gate Conduction Variability of High-k Dielectrics-Based Metal-Oxide-Semiconductor Structures”. IEEE Transactions on Device and MaterialsReliability,11(3),495 501.doi:10.1109/tdmr.2011.2161087

Ultra-Scaled technologies suffer from variability and reliability issues, which are intrinsically related to device scaling. Electrical characteristics of highly scaled MOSFETs may exhibit significant device-to-device variability, which is ultimately associated with the discrete nature of matter and charge. Several variability sources, such as random dopant distribution, line edge roughness, gate oxide roughness and granularity of the poly-Si gate (either during deposition or fabrication), etc. In particular, as modeling, these might lead to variations in threshold voltage .The homogeneity of the morphological and electrical properties of the high-k gate stack may also be expected to affect the variability of the electrical properties of scaled devices. However, few reports

have addressed this topic since standard electrical characterization techniques can only provide information that is averaged over the entire device gate area of fully processed metal-oxide-semiconductor (MOS) capacitors or transistors . This confirms the need for advanced characterization methods with high lateral resolution.

This granularity has been attributed to the polycrystalline microstructure of the high-k layer after the high temperature treatment, as other works have observed, whereas thermal treatment at the lowest temperature (350 °C) maintained samples in their amorphous phase. In the polycrystalline structure (annealed at 800 °C), grains correspond to individual (or a cluster of) randomly oriented nanocrystals separated by grain boundaries (GBs). Although the local thickness (t_{ox}) of the gate dielectric depends not only on the scanned top surface (gate/dielectric) but also on the dielectric/bulk interface (information not available in this experiment), it is reasonable to assume similar characteristics of both interfaces. Therefore, the larger topographical inhomogeneity observed in the higher temperature annealed samples suggests larger local thickness (t_{ox}) fluctuations within the polycrystalline structures. A statistical analysis of the grains shows that their average size is ~130 and ~230 nm^2 in the case of 3.6 and 5.3 nm thick gate dielectric, respectively, suggesting that the grain size, which is compatible depends on the high k layer thickness.

[4] Iglesias, V.; Lanza, M.; Zhang, K.; Bayerl, A.; Porti, M.; Nafría, M.; Aymerich, X.; Benstetter, G.; Shen, Z. Y.; Bersuker, G. (2011).” Degradation of polycrystalline HfO2-based gate dielectrics under nanoscale electrical stress”. Applied Physics Letters, 99(10), 103510–. doi:10.1063/1.3637633

In this work, The intrinsic process variability and aging mechanisms can strongly affect the performance and reliability of MOS devices. The polycrystallization of high-k-based gate dielectrics, which can occur even during relatively low temperature device fabrication steps (e.g., atomic layer deposition, forming gas anneal), as one of the device-to-device variability sources. Conductive atomic force microscope (CAFM) experiments, which may address nanoscale topographical and electrical properties of dielectric stacks, reveal significantly higher leakage currents through the grain boundaries (GBs) than through nanocrystal (NC) grains. Theoretical models suggest that the current through the GBs could be related to a large concentration of oxygen vacancies at the GBs, which might effectively act as conductive paths through the dielectric film. However, the relative role of the vacancies vs. topological factors (e.g., the dielectric thickness at the GB region) as well as the evolution of GB electrical properties under electrical stress remains unexplored. In this work, a CAFM technique has been applied to investigate conduction characteristics of the GBs in polycrystalline HfO2 gate dielectrics. Kelvin probe force

microscope (KPFM) measurements were used to assess the charge state of defects in these structures.

The dielectric stack under investigation consists of a 5 nm Atomic layer deposited (ALD) HfO_2 film (annealed at 1000C to induce polycrystallization and a 1 nm SiO_2 interfacial layer grown on a Si substrate. Gate stack properties were investigated using CAFM (air conditions and contact mode). Current and topography maps were measured by applying voltage between the tip and the substrate, and current-voltage (I-V) data were collected in a ramped voltage mode at different oxide locations (GBs and grains). Some I-V characteristics were also measured with a modified CAFM approach to provide a larger current dynamic range . KPFM (air conditions) was employed to obtain topography and the probe tip-sample contact potential difference (CPD) map, which is proportional to the amount of charge trapped in the dielectric at the probe tip position.

3. MOSFET

3.1 Introduction to MOSFET

The MOSFET (Metal Oxide Semiconductor Field Effect Transistor) transistor is a semiconductor device which is widely used for switching and amplifying electronic signals in the electronic devices. The MOSFET is a core of integrated circuit and it can be designed and fabricated in a single chip because of these very small sizes. The MOSFET is a four terminal device with source(S), gate (G), drain (D) and body (B) terminals. The body of the MOSFET is frequently connected to the source terminal so making it a three terminal device like field effect transistor. The MOSFET is very far the most common transistor and can be used in both analog and digital circuits. The MOSFET works by electronically varying the width of a channel along which charge carriers flow (electrons or holes). The charge carriers enter the channel at source and exit via the drain. The width of the channel is controlled by the voltage on an electrode is called gate which is located between source and drain. It is insulated from the channel near an extremely thin layer of metal oxide. The MOS capacity present in the device is the main part. A metal–oxide–semiconductor field-effect transistor (MOSFET, MOS-FET, or MOS FET) is a field-effect transistor (FET with an insulated gate) where the voltage determines the conductivity of the device. It is used for switching or amplifying signals. The ability to change conductivity with the amount of applied voltage can be used for amplifying or switching electronic signals. MOSFETs are now even more common than BJTs (bipolar junction

transistors) in digital and analog circuits. The silicon dioxide forms the gate of the MOSFET. It is used to provide isolation by prevent the direct flow of charges on gate to the conducting channel.

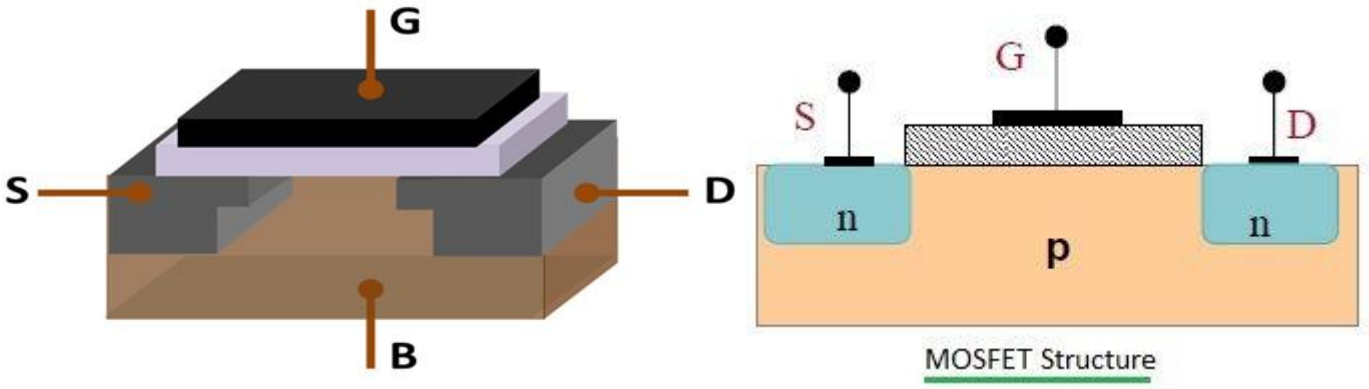


Figure 1.6 : MOSFET Structure

3.2 Why MOSFET ?

MOSFETs are particularly useful in amplifiers due to their input impedance being nearly infinite which allows the amplifier to capture almost all the incoming signal. The main advantage is that it requires almost no input current to control the load current, when compared with bipolar transistors. The various types of MOSFET are given below:

Depletion Type:

The transistor requires the Gate-Source voltage (VGS) to switch the device "OFF". The depletion-mode MOSFET is equivalent to a "Normally Closed" switch. When there is no voltage on the gate, the channel shows its maximum conductance. As the voltage on the gate is either positive or negative, the channel conductivity decreases.

Enhancement Type:

The transistor requires a Gate-Source voltage(VGS) to switch the device "ON". The enhancement-mode MOSFET is equivalent to a "Normally Open" switch. When there is no voltage on the gate the device does not conduct. More is the voltage on the gate, the better the device can conduct.

3.3 MOSFET device structure & Operation ;

The aim of the MOSTFET is to be able to control the voltage and current flow between the source and drain. It works almost as a switch. The working of MOSFET depends upon the MOS capacitor. The MOS capacitor is the main part of MOSFET. The semiconductor surface at the below oxide layer which is located between source and drain terminal. It can be inverted from p- type to n-type by applying a positive or negative gate voltages respectively. When we apply the positive gate voltage the holes present under the oxide layer with a repulsive force and holes are pushed downward with the substrate. The deflection region populated by the bound negative charges which are associated with the acceptor atoms. The electrons reach channel is formed. The positive voltage also attracts electrons from the n+ source and drain regions into the channel. Now, if a voltage is applied between the drain and source, the current flows freely between the source and drain and the gate voltage controls the electrons in the channel. Instead of positive voltage if we apply negative voltage , a hole channel will be formed under the oxide layer.

It is a four-terminal device with source (S), drain (D) and gate Terminal (G) and body (B) terminals. The body is frequently connected to the source terminal, reducing the terminals to three. It works by varying the width of a channel along which charge carriers flow (electrons or holes). The charge carriers enter the channel at source and exit via the drain. The width of the channel is controlled by the voltage on an electrode is called gate which is located between source and drain. It is insulated from the channel near an extremely thin layer of metal oxide. A metal-insulator-semiconductor field-effect transistor or MISFET is a term almost synonymous with MOSFET. Another synonym is IGFET for the insulated-gate field-effect transistor.

Operation :

The working of a MOSFET depends upon the MOS capacitor. The MOS capacitor is the main part of MOSFET. The semiconductor surface at the below oxide layer is located between the source and drain terminals. It can be inverted from p-type to n-type by applying positive or negative gate voltages.

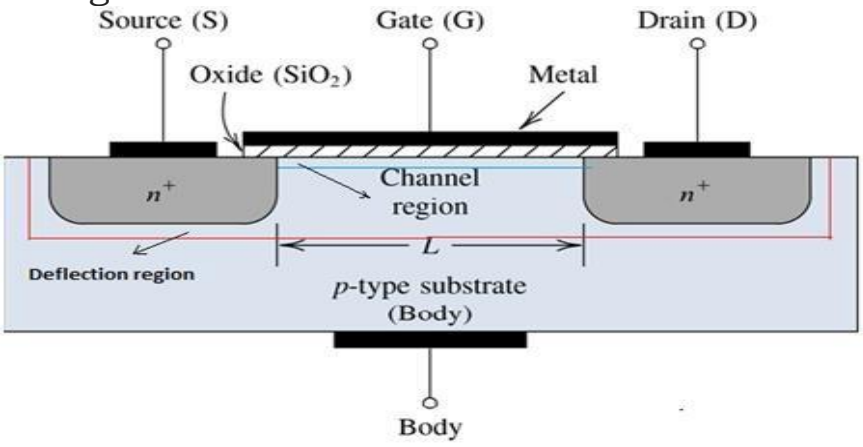


Fig 1.7 : MOSFET Operation

When we apply positive gate voltage the holes present under the oxide layer with a repulsive force and holes are pushed downward with the substrate. The depletion region is populated by the bound negative charges which are associated with the acceptor atoms. The electrons reach the channel is formed. The positive voltage also attracts electrons from the n+ source and drain regions into the channel. Now, if a voltage is applied between the drain and source, the current flows freely between the source and drain and the gate voltage controls the electrons in the channel. If we apply negative voltage.

P – Channel MOSFET :

The P- Channel MOSFET has a P- Channel region between source and drain. It is a four terminal device such as gate, drain, source, body. The drain and source are heavily doped p+ region and the body or substrate is n-type. The flow of current is positively charged holes. When we apply the negative gate voltage, the electrons present under the oxide layer with are pushed downward into the substrate with a repulsive force.

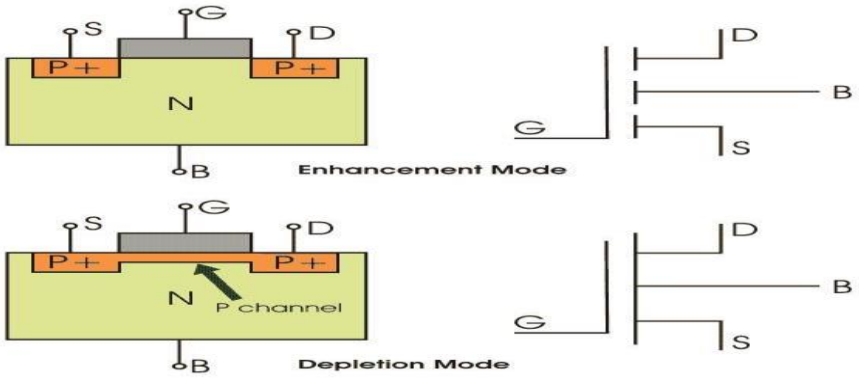


Fig 1.8 : P - MOSFET Operation

The deflection region populated by the bound positive charges which are associated with the donor atoms. The negative gate voltage also attracts holes from p+ source and drain region into the channel region.

The drain and source are heavily doped p+ region and the substrate is in n-type. The current flows due to the flow of positively charged holes also known as p-channel MOSFET. When we apply negative gate voltage, the electrons present beneath the oxide layer experience repulsive force and they are pushed downward into the substrate, the depletion region is populated by the bound positive charges which are associated with the donor atoms. The negative gate voltage also attracts holes from the P+ source and drain region into the channel region.

N-Channel MOSFET :

The N-Channel MOSFET has a N- channel region between source and drain It is a four terminal device such as gate, drain , source , body. This type of MOSFET the drain and source are heavily doped n+ region and the substrate or body is P- type. The current flows due to the negatively charged electrons. When we apply the positive gate voltage the holes present under the oxide layer pushed downward into the substrate with a repulsive force. The deflection region is populated by the bound negative charges which are associated with the acceptor atoms. The electrons reach channel is formed. The positive voltage also attracts electrons from the n+ source and drain regions into the channel. Now, if a voltage is applied between the drain and source the

current flows freely between the source and drain and the gate voltage controls the electrons in the channel. Instead of positive voltage if we apply negative voltage a hole channel will be formed under the oxide layer.

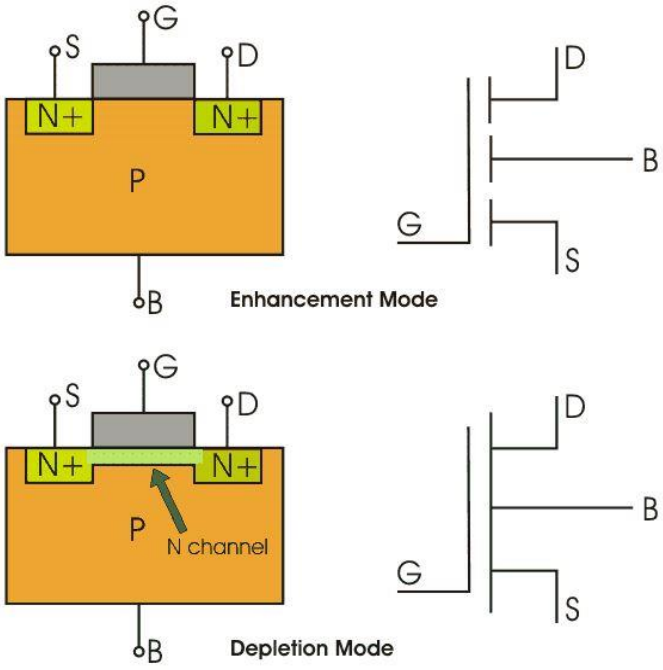


Fig 1.9 : N - MOSFET Operation

The drain and source are heavily doped N+ region and the substrate is p-type. The current flows due to the flow of negatively charged electrons, also known as n-channel MOSFET. When we apply the positive gate voltage the holes present beneath the oxide layer experience repulsive force and the holes are pushed downwards into the bound negative charges which are associated with the acceptor atoms. The positive gate voltage also attracts electrons from the N+ source and drain region into the channel thus an electron reach channel is formed.

3.4 Important MOSFET Parameters :

Maximum Drain-Source Voltage, V_{DS} :

V_{DS} is the maximum instantaneous operating voltage.

Continuous Drain Current, I_D :

I_D is the maximum current the MOSFET can carry sometimes specified at a particular junction temperature.

Maximum Pulsed Drain Current, I_{DM} :

I_{DM} is greater than I_D and specified for a particular pulse width and duty cycle.

Maximum Gate-Source Voltage, V_{GS} :

V_{GS} is the maximum voltage that can be applied between gate and source without damaging the gate insulation. Gate Threshold Voltage, V_T , {V_{TH} , $V_{GS(th)}$ } :

V_T is the minimum gate voltage at which the transistor will turn ON.

3.5 Noise Margin

Noise margin is the amount of noise that a CMOS circuit could withstand without compromising the operation of circuit. Noise margin does makes sure that any signal which is logic '1' with finite noise added to it, is still recognized as logic '1' and not logic '0'.

In digital integrated circuits, to minimize the noise it is necessary to keep "0" and "1" intervals broader. Hence noise margin is the measure of the sensitivity of a gate to noise and expressed by, NML (noise margin Low) and NMH (noise margin High).

NML and NMH are defined as,

NML = VIL – VOL and NMH = VOH – VIH

In order to define the terms VIL, VOL, VOH and VIH again consider the VTC of Inverter as shown in Figure below. The VOH is the maximum output voltage at which the output is "logic high". The VOL is the minimum output voltage at which the output is "logic low". The regions of acceptable high and low voltages are defined by VIH and VIL respectively. VIH and VIL represents the points where the gain dVoutdVin of VTC is equals to – 1 as shown in above Figure. The region between VIH and VIL is called as the undefined region or transition width.

Figure below shows the NMH and NML levels of two cascaded inverters. The noise margin shows the levels of noise when the gates are connected together. For the digital integrated circuits the noise margin is larger than '0' and ideally it is high.

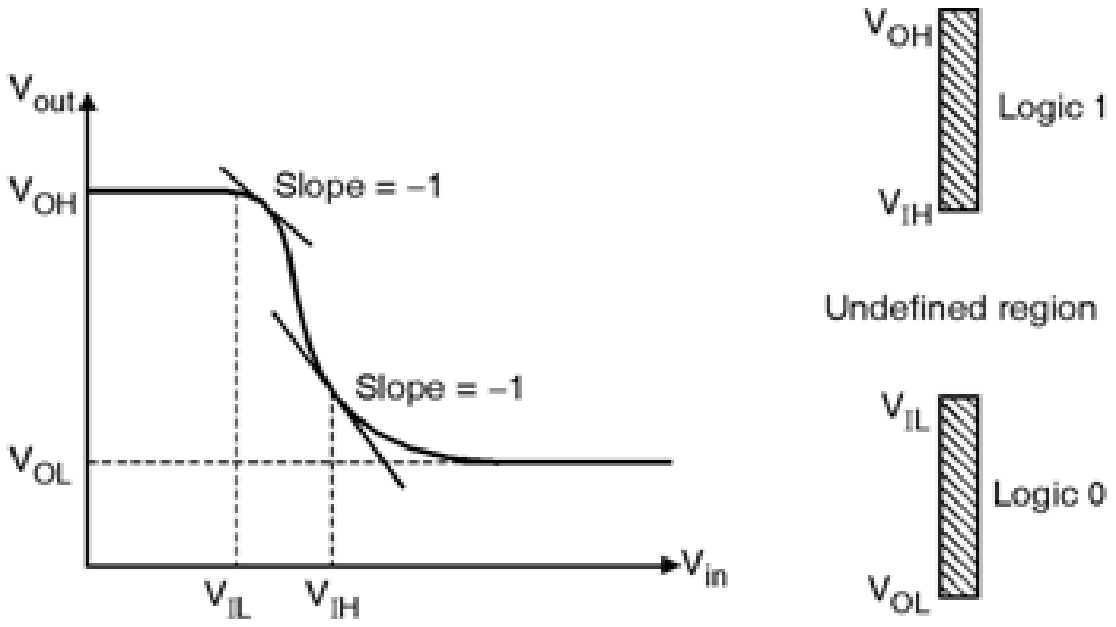


Fig 2.0 : Slope of Noise margin

4. Dielectric & Moore's Law

4.1 Dielectric

In electromagnetism, a dielectric (or dielectric material or dielectric medium) is an electrical insulator that can be polarized by an applied electric field. When a dielectric material is placed in an electric field, electric charges do not flow through the material as they do in an electrical conductor, because they have no loosely bound, or free, electrons that may drift through the material, but instead they shift, only slightly, from their average equilibrium positions, causing dielectric polarization. Because of dielectric polarization, positive charges are displaced in the direction of the field and negative charges shift in the direction opposite to the field (for example, if the field is moving parallel to the positive x axis, the negative charges will shift in the negative x direction). This creates an internal electric field that reduces the overall field within the dielectric itself. If a dielectric is composed of weakly bonded molecules, those molecules not only become polarized, but also reorient so that their symmetry axes align to the field.

The study of dielectric properties concerns storage and dissipation of electric and magnetic energy in materials. Dielectrics are important for explaining various phenomena in electronics, optics, solid-state physics and cell biophysics. Although the term *insulator* implies low electrical conduction, dielectric typically means materials with a high polarizability. The latter is expressed by a number called the relative permittivity. The term insulator is generally used to

indicate electrical obstruction while the term dielectric is used to indicate the energy storing capacity of the material (by means of polarization). A common example of a dielectric is the electrically insulating material between the metallic plates of a capacitor. The polarization of the dielectric by the applied electric field increases the capacitor's surface charge for the given electric field strength.

The term *dielectric* was coined by William Whewell (from *dia* + *electric*) in response to a request from Michael Faraday. A *perfect dielectric* is a material with zero electrical conductivity (perfect conductor infinite electrical conductivity), thus exhibiting only a displacement current; therefor it stores and returns electrical energy as if it were an ideal capacitor.

4.2 Electric susceptibility

The electric susceptibility of a dielectric material is a measure of how easily it polarizes in response to an electric field. This, in turn, determines the electric permittivity of the material and thus influences many other phenomena in that medium, from the capacitance of capacitors to the speed of light.

It is defined as the constant of proportionality (which may be a tensor) relating an electric field **E** to the induced dielectric polarization density **P** such that

$$\mathbf{P} = \varepsilon_0 \chi_e \mathbf{E},$$

where ε_0 is the **electric permittivity of free space**

The susceptibility of a medium is related to its relative permittivity ε_r by $\chi_e = \varepsilon_r - 1.$

The electric displacement $\mathbf{D}$ is related to the polarization density $\mathbf{P}$ by $\mathbf{D} = \varepsilon_0 \mathbf{E} + \mathbf{P} = \varepsilon_0 (1 + \chi_e) \mathbf{E} = \varepsilon_0 \varepsilon_r \mathbf{E}.$

4.3 Dispersion and causality

In general, a material cannot polarize instantaneously in response to an applied field. The more general formulation as a function of time is

$$\mathbf{P}(t) = \varepsilon_0 \int_{-\infty}^{t} \chi_e (t - t') \mathbf{E}(t') \, dt'.$$

That is, the polarisation is a convolution of the electric field at previous times with time-dependent susceptibility given by $x_e(\Delta t)$. The upper limit of this integral can be extended to infinity as well if one defines $x_e(\Delta t) = 0$ for $\Delta t < 0$. An instantaneous response corresponds to Dirac delta function susceptibility $x_e(\Delta t) = x_e \delta(\Delta t)$.

It is more convenient in a linear system to take the Fourier transform and write this relationship as a function of frequency. Due to the convolution theorem, the integral becomes a simple product,

$$\mathbf{P}(\omega) = \varepsilon_0 \chi_e (\omega) \mathbf{E}(\omega).$$

The susceptibility (or equivalently the permittivity) is frequency dependent. The change of susceptibility with respect to frequency characterizes the dispersion properties of the material.

4.4 Basic atomic model :

In the classical approach to the dielectric, the material is made up of atoms. Each atom consists of a cloud of negative charge (electrons) bound to and surrounding a positive point charge at its centre. In the presence of an electric field, the charge cloud is distorted, as shown in the top right of the figure. This can be reduced to a simple dipole using the superposition principal. A dipole is characterised by its dipole moment, a vector quantity shown in the figure as the blue arrow labelled *M*. It is the relationship between the electric field and the dipole moment that gives rise to the behaviour of the dielectric. (Note that the dipole moment points in the same direction as the electric field in the figure. This isn't always the case, and is a major simplification, but is true for many materials.)

When the electric field is removed the atom returns to its original state. The time required to do so is the so-called relaxation time; an exponential decay.

The relationship between the electric field **E** and the dipole moment **M** gives rise to the behavior of the dielectric, which, for a given material, can be characterized by the function **F** defined by the equation: **M = F(E)**

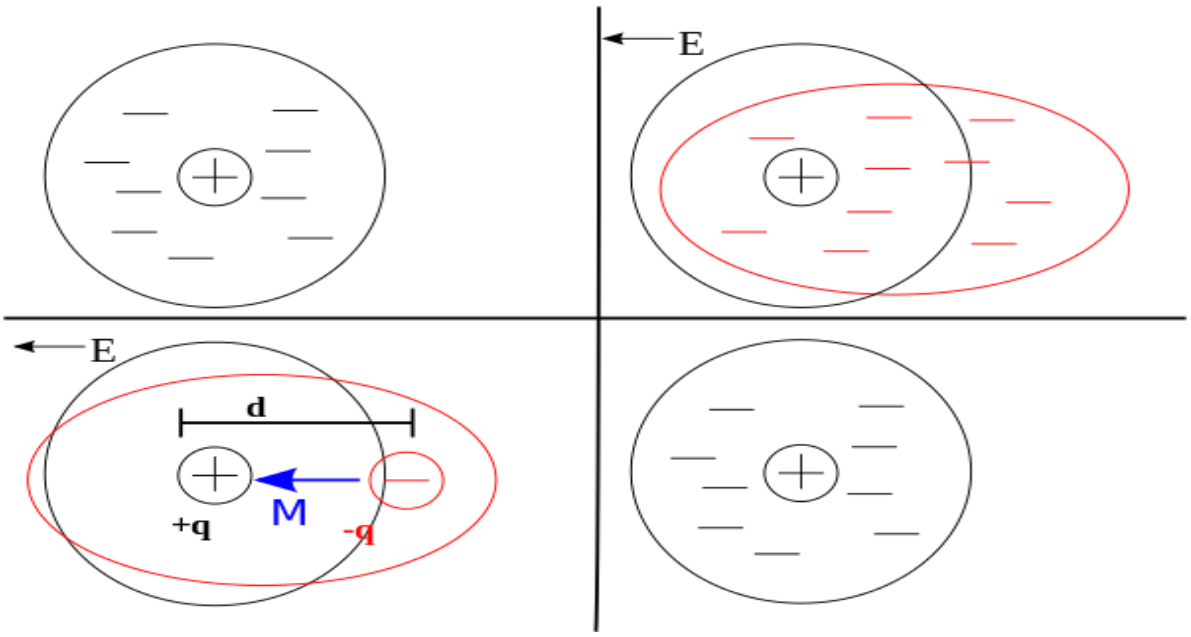


Fig 2.1: Basic Atomic Model

4.5 Dipolar polarization :

Dipolar polarisation is a polarisation that is either inherent to polar molecules (orientation polarisation), or can be induced in any molecule in which the asymmetric distortion of the nuclei is possible (distortion polarisation). Orientation polarisation results from a permanent dipole, e.g., that arising from the 104.45° angle between the asymmetric bonds between oxygen and hydrogen atoms in the water molecule, which retains polarisation in the absence of an external electric field. The assembly of these dipoles forms a macroscopic polarisation.

When an external electric field is applied, the distance between charges within each permanent dipole, which is related to chemical bonding, remains constant in orientation polarisation; however, the direction of polarisation itself rotates. This rotation occurs on a timescale

that depends on the torque and surrounding local viscosity of the molecules. Because the rotation is not instantaneous, dipolar polarisations lose the response to electric fields at the highest frequencies. A molecule rotates about 1 radian per picosecond in a fluid, thus this loss occurs at about 10^{11} Hz (in the microwave region). The delay of the response to the change of the electric field causes friction and heat.

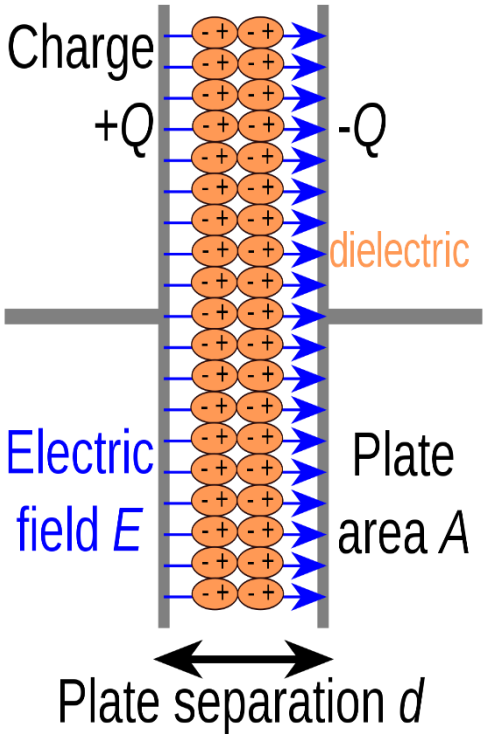


Fig 2.2 : Electric plates

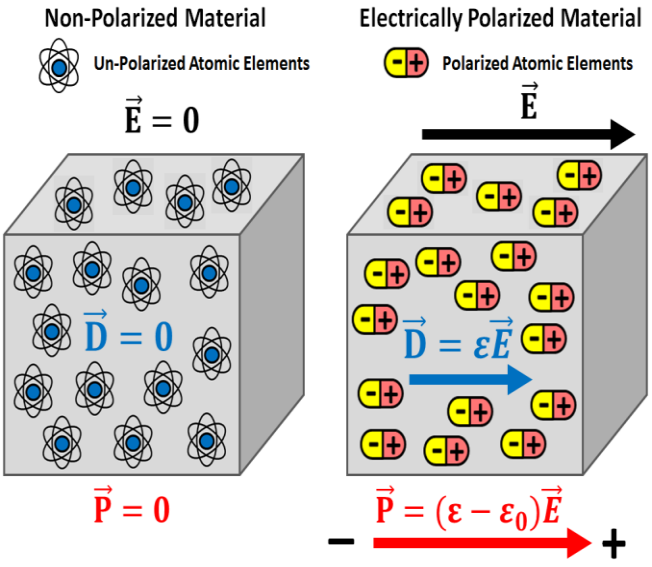


Fig 2.3 : Polarized Materials

When an external electric field is applied at infrared frequencies or less, the molecules are bent and stretched by the field and the molecular dipole moment changes. The molecular vibration frequency is roughly the inverse of the time it takes for the molecules to bend, and this distortion polarisation disappears above the infrared.

4.6 Moore's Law :

Moore's law is the observation that over the history of computing hardware, the number of transistors on integrated circuits doubles approximately every two years. The period often quoted as "18 months" is due to Intel executive David House, who predicted that period for a doubling in chip performance (being a combination of the effect of more transistors and their being faster). The law is named after Intel co-founder Gordon E. Moore, who described the trend in his 1965 paper. The paper noted that the number of components in integrated circuits had doubled every year from the invention of the integrated circuit in 1958 until 1965 and predicted that the trend would continue "for at least ten years". His prediction has proven to be uncannily accurate, in part because the law is now used in the semiconductor industry to guide long-term planning and to set targets for research and development.

The capabilities of many digital electronic devices are strongly linked to Moore's law: processing speed, memory capacity, sensors and even the number and size of pixels in digital cameras. All of these are improving at (roughly) exponential rates as well (see Other formulations and similar laws). This exponential improvement has dramatically enhanced the impact of digital electronics in nearly every segment of the world economy. Moore's law describes a driving force of technological and social change in the late 20th and early 21st centuries.

This trend has continued for more than half a century. Sources in 2005 expected it to continue until at least 2015 or 2020. However, the 2010 update to the International Technology Roadmap for Semiconductors has growth slowing at the end of 2013, after which time transistor counts and densities are to double only every three years.

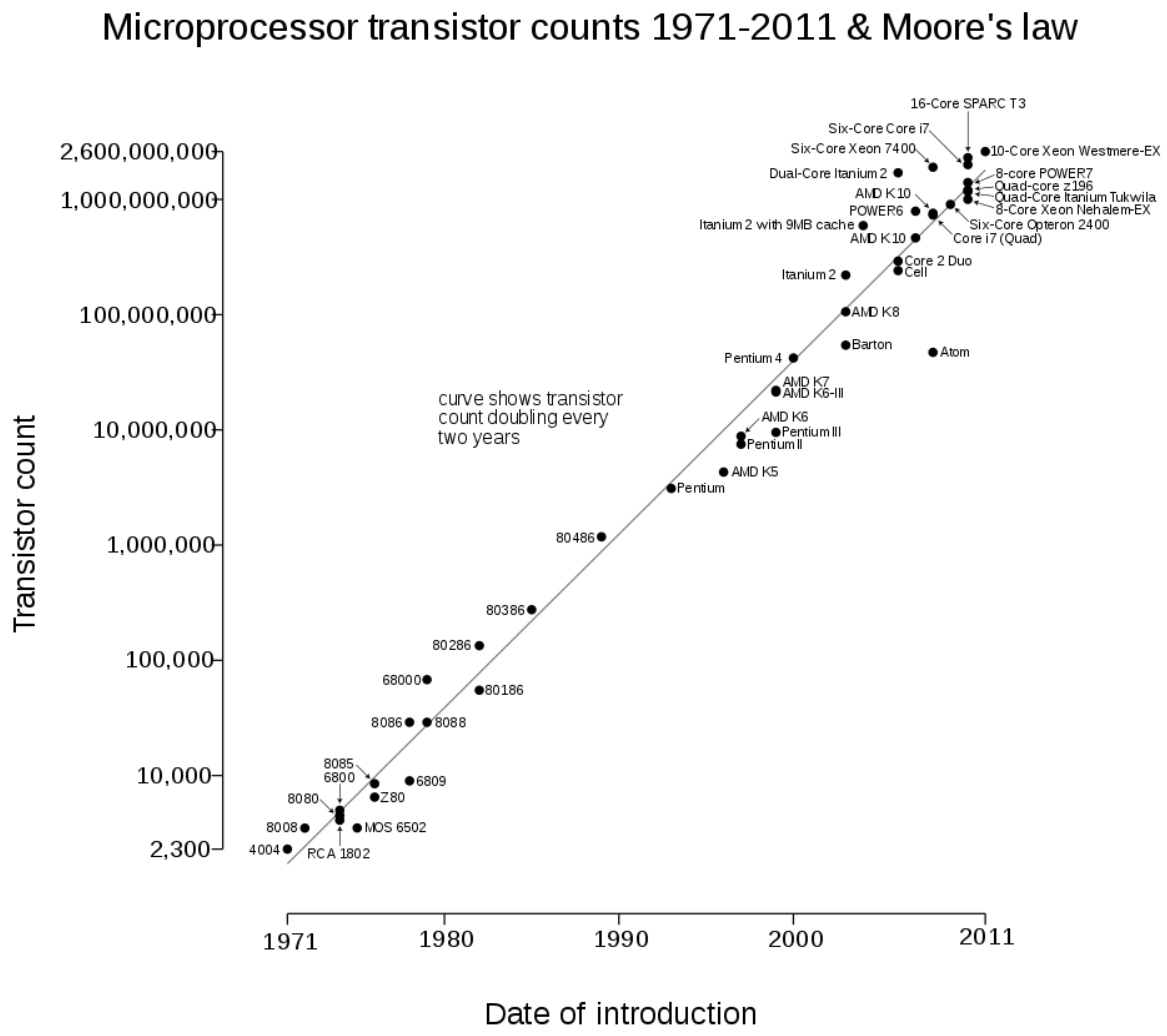


Fig 3.4 : Transistor counts

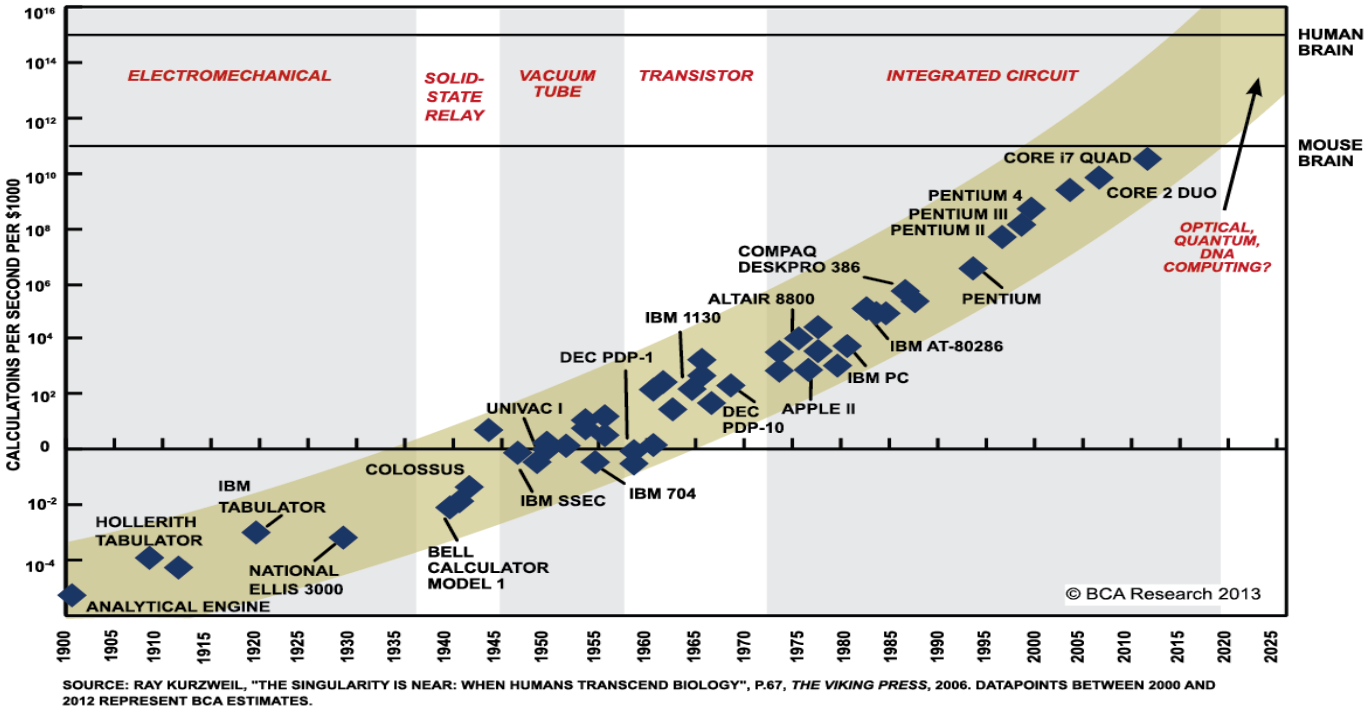
Moore's law is the observation that the number of transistors in a dense integrated circuit (IC) doubles about every two years. Moore's law is an observation and projection

of a historical trend. Rather than a law of physics, it is an empirical relationship linked to gains from experience in production. The observation is named after Gordon Moore, the co-founder of Fairchild Semiconductor and Intel(and former CEO of the latter), who in 1965 posited a doubling every year in the number of components per integrated circuit, and projected this rate of growth would continue for at least another decade. In 1975, looking forward to the next decade, he revised the forecast to doubling every two years, a compound annual growth rate (CAGR) of 41%. While Moore did not use empirical evidence in forecasting that the historical trend would continue, his prediction held since 1975 and has since become known as a "law". Moore's prediction has been used in the semiconductor industry to guide long-term planning and to set targets for research and development, thus functioning to some extent as a self-fulfilling prophecy.

Advancements in digital electronics, such as the reduction in quality-adjusted microprocessor prices, the increase in memory capacity , the improvement of sensors, and even the number and size of pixels in digital cameras, are strongly linked to Moore's law. These step changes in digital electronics have been a driving force of technological and social change, productivity, and economic growth.

Industry experts have not reached a consensus on exactly when Moore's law will cease to apply. Microprocessor architects report that semiconductor advancement has slowed industry-wide since around 2010, below the pace

predicted by Moore's law. Between 2019 and 2021, the highest commercially available chip transistor count increased from 39.54 trillion to 57 trillion or 44% – less than half of the doubling predicted by Moore's Law. Similarly, since the mid-2010s, the increase in the performance of the top supercomputers has been slowing down substantially.



SOURCE: RAY KURZWEIL, "THE SINGULARITY IS NEAR: WHEN HUMANS TRANSCEND BIOLOGY", P.67, *THE VIKING PRESS*, 2006. DATAPOINTS BETWEEN 2000 AND 2012 REPRESENT BCA ESTIMATES.

Fig 2.5 : Calculations of IC's

4.7 History of Moore's Law :

In 1959, Douglas Engelbart discussed the projected downscaling of integrated circuit (IC) size in the article "Microelectronics, and the Art of Similitude". Engelbart presented his ideas at the 1960 International Solid-State Circuits Conference, where Moore was present in the audience. That same year, Mohamed Atalla and Dawon Kahng invented the MOSFET (metal-oxide-semiconductor

field–effect transistor), also known as the MOS transistor, at Bell Labs The MOSFET was the first truly compact transistor that could be miniaturized and mass–produced for a wide range of uses, with its high scalability and low power consumption resulting in a higher transistor density and making it possible to build high–density IC chips. In the early 1960s, Gordon E. Moore recognized that the ideal electrical and scaling characteristics of MOSFET devices would lead to rapidly increasing integration levels and unparalleled growth in electronic applications.

In 1965, Gordon Moore, who at the time was working as the director of research and development at Fairchild Semiconductor, was asked to contribute to the thirty–fifth anniversary issue of *Electronics* magazine with a prediction on the future of the semiconductor components industry over the next ten years. His response was a brief article entitled "Cramming more components onto integrated circuits". Within his editorial, he speculated that by 1975 it would be possible to contain as many as 65,000 components on a single quarter–square–inch semiconductor.

The complexity for minimum component costs has increased at a rate of roughly a factor of two per year. Certainly over the short term this rate can be expected to continue, if not to increase. Over the longer term, the rate of increase is a bit more uncertain, although there is no reason to believe it will not remain nearly constant for at least 10 years. Moore posited a log–linear relationship between device complexity (higher circuit density at reduced cost)

and time. In a 2015 interview, Moore noted of the 1965 article: "...I just did a wild extrapolation saying it's going to continue to double every year for the next 10 years." One historian of the law cites Stigler's law of eponymy, to introduce the fact that the regular doubling of components was known to many working in the field.

In 1974, Robert H. Dennard at IBM recognized the rapid MOSFET scaling technology and formulated what became known as Dennard scaling, which describes that as MOS transistors get smaller, their power density stays constant such that the power use remains in proportion with area. MOSFET scaling and miniaturization have been the key driving forces behind Moore's law. Evidence from the semiconductor industry shows that this inverse relationship between power density and areal density broke down in the mid−2000s.

At the 1975 IEEE International Electron Devices Meeting, Moore revised his forecast rate, predicting semiconductor complexity would continue to double annually until about 1980, after which it would decrease to a rate of doubling approximately every two years. He outlined several contributing factors for this exponential behavior:

- The advent of metal−oxide−semiconductor (MOS) technology
- The exponential rate of increase in die sizes, coupled with a decrease in defective densities, with the result that semiconductor manufacturers could work with larger areas without losing reduction yields

- Finer minimum dimensions
- What Moore called "circuit and device cleverness"

Shortly after 1975, Caltech professor Carver Mead popularized the term "Moore's law". Moore's law eventually came to be widely accepted as a goal for the semiconductor.

Semiconductor device fabrication

- 10 µm – 1971
- 6 µm – 1974
- 3 µm – 1977
- 1.5 µm – 1981
- 1 µm – 1984
- 800 nm – 1987
- 600 nm – 1990
- 350 nm – 1993
- 250 nm – 1996
- 180 nm – 1999
- 130 nm – 2001
- 90 nm – 2003
- 65 nm – 2005
- 45 nm – 2007
- 32 nm – 2009
- 22 nm – 2012
- 14 nm – 2014
- 10 nm – 2016
- 7 nm – 2018
- 5 nm – 2020

Future

- 3 nm ~ 2022
- 2 nm ~ 2024
- 1.8 nm ~ 2025

5. Software Tools

5.1 Introduction to Tool

General Editing Operations		
Edit Properties		Edit properties (e.g. coordinates of polygon of the current drawing item. vertices).
Make a Clone		Make a copy of the selected drawing items.
Mirror Horizontally		Flip the current drawing item in the horizontal direction.
Mirror Vertically		Flip the current drawing item in the vertical direction.
Move points		Enter the corner point editing mode. User can select a vertex in the highlighted polygon and move the vertex.

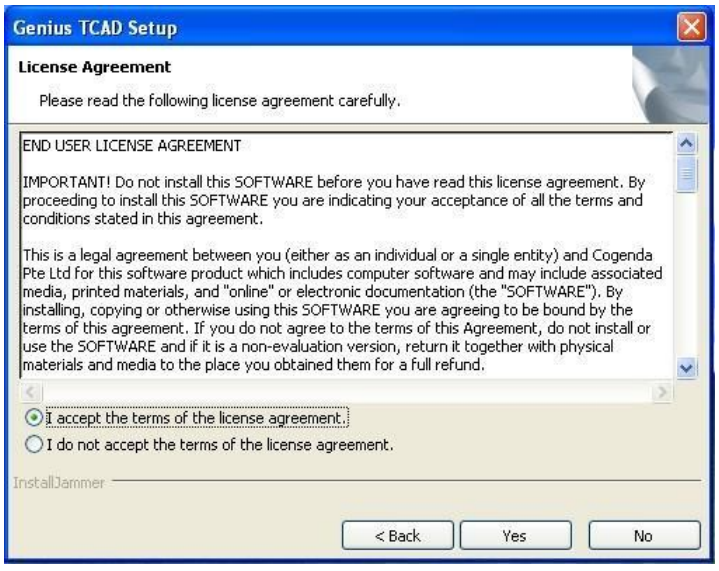
Menu	Icon	Description
Snap		
Auto Snap		Enter the automatic snapping mode. Mouse coordinates are snapped to a nearby grid point or a vertex in existing drawing.
Grid Snap		Enter the grid snapping mode. Mouse coordinates are snapped to a nearby grid point.
Line Snap		Enter the line snapping mode. Mouse coordinates are snapped to a point on a nearby line segment.
Horizontal Line Snap		Enter the horizontal line snapping mode. Mouse coordinates are snapped to a point on a nearby line,
Vertical Line Snap		Enter the horizontal line snapping mode. Mouse coordinates are snapped to a point on a nearby line, the line segment currently being drawn is kept vertical.
No Snap		Enter the free-hand drawing mode. No snapping of coordinates is applied.

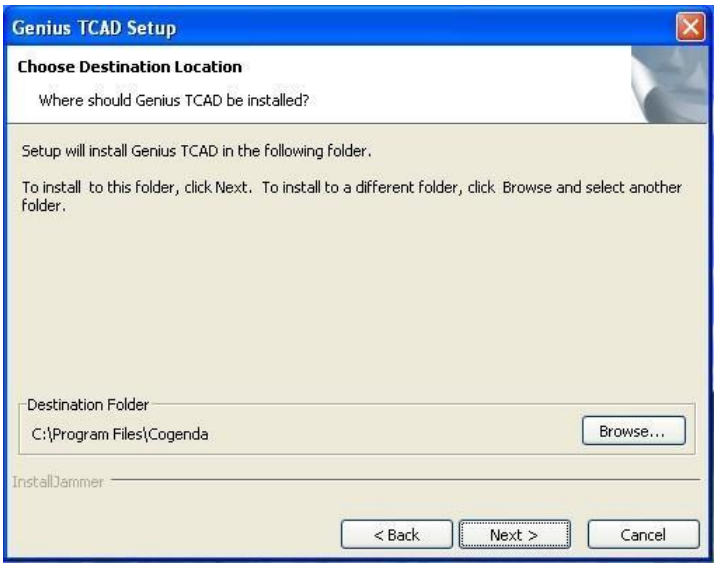
5.2 Installing on Windows

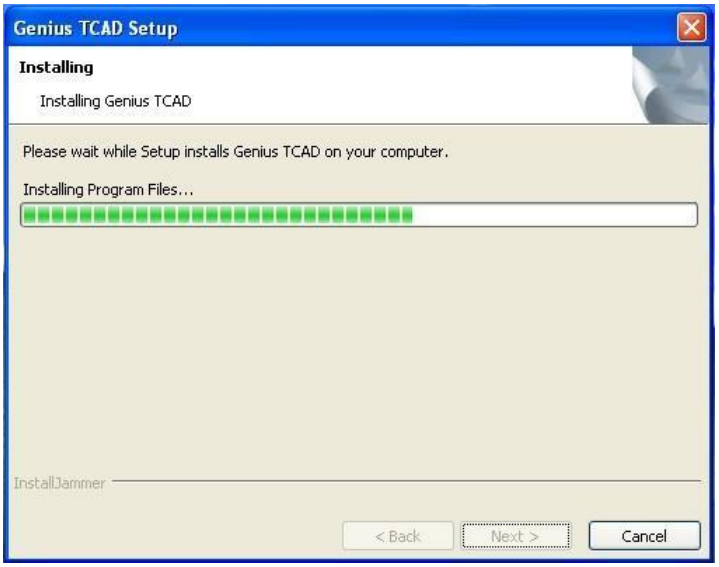
- The installation package comes as ab executable file.
- Double clicking on it will start the installation wizard.

- We recommend install Para view, a versatile visualization software package, to examine the output file generated by Genius. The installer of Para view is included, and the user can choose to install it. After installation, we can test the installation with the bundled examples. Please click

Start ▷ All Programs ▷ Cogenda Genius TCAD ▷ VisualTCAD

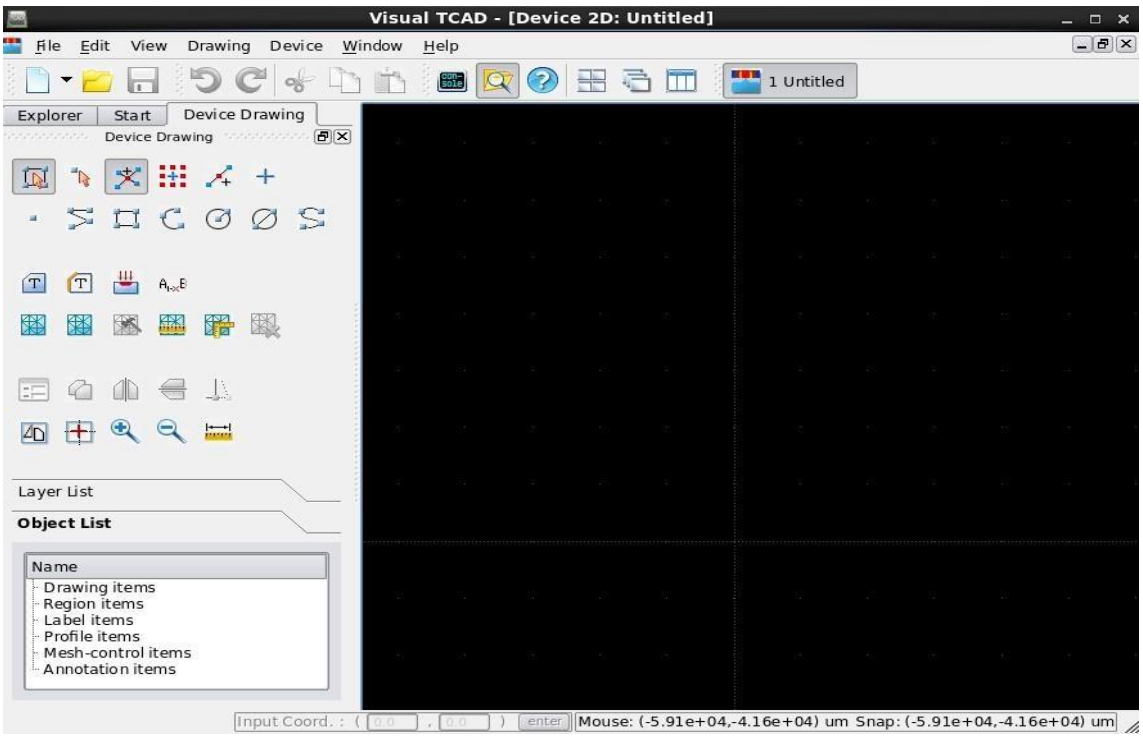


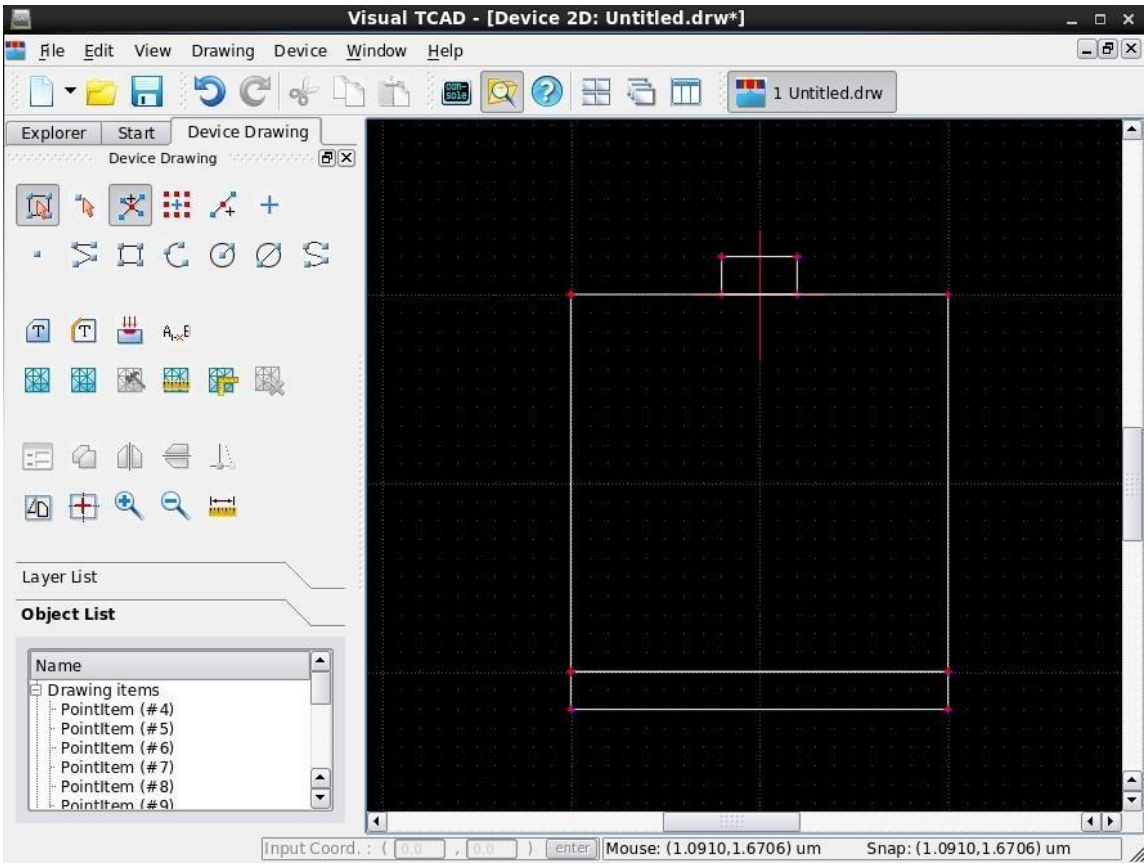




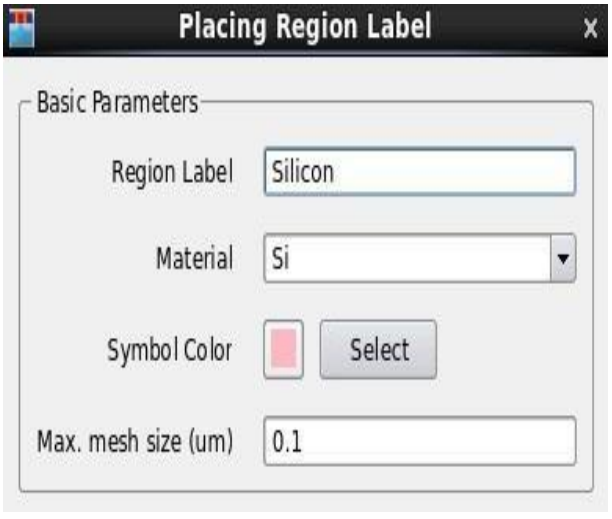
5.3 Steps to draw a device in TCAD software

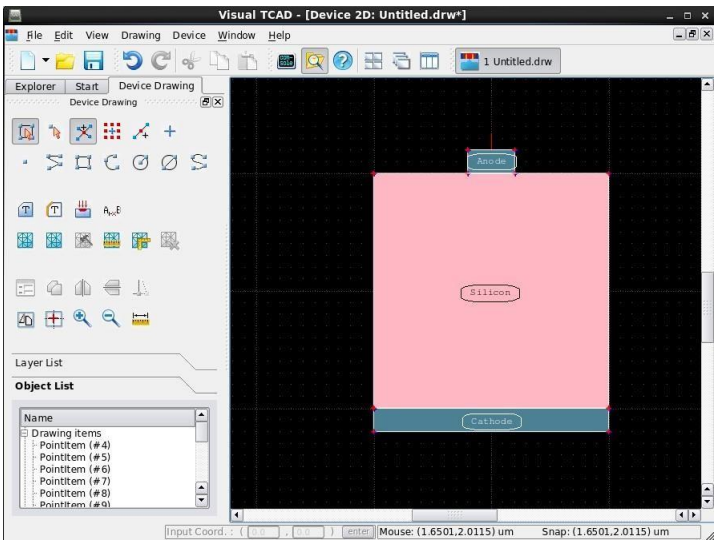
- Click on the TCAD simulation software and open it and it appears as shown in below figure.


Visual TCAD - [Device 2D: Untitled]
File Edit View Drawing Device Window Help
1 Untitled
Explorer Start Device Drawing
Device Drawing
Layer List
Object List
Name
Drawing items
Region items
Label items
Profile items
Mesh-control items
Annotation items
Input Coord. : (0.0 , 0.0) enter
Mouse: (-5.91e+04,-4.16e+04) um Snap: (-5.91e+04,-4.16e+04) um

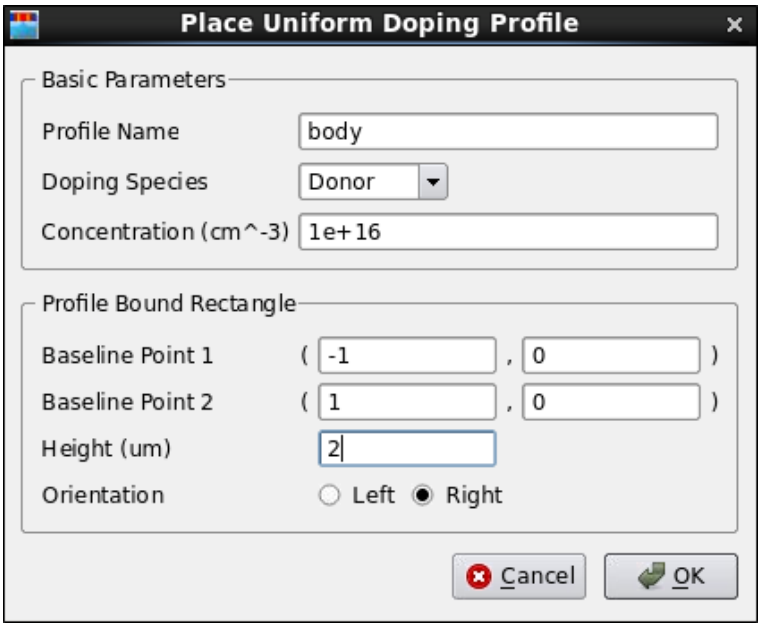

Visual TCAD - [Device 2D: Untitled.drw*]
File Edit View Drawing Device Window Help
1 Untitled.drw
Explorer Start Device Drawing
Device Drawing
Layer List
Object List
Name
Drawing items
PointItem (#4)
PointItem (#5)
PointItem (#6)
PointItem (#7)
PointItem (#8)
PointItem (#9)
Input Coord. : (0.0 , 0.0) enter
Mouse: (1.0910,1.6706) um
Snap: (1.0910,1.6706) um

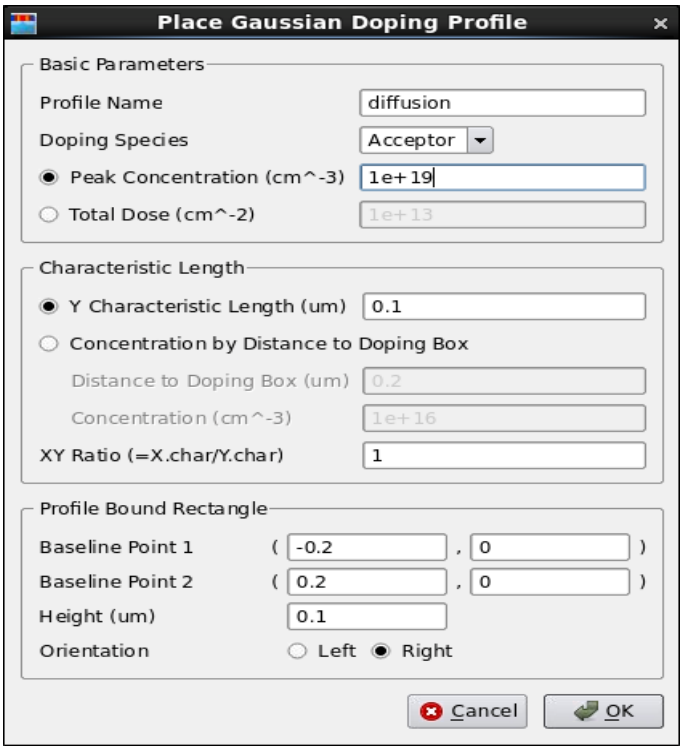
- We start by drawing a box representing the body of the silicon diode. Choose from drawing tools **Add Rectangle.** We define the first corner of the rectangle by clicking at the coordinates (-1,0). one may notice that in the Add Rectangle tool, the mouse cursor is snapped to the background grip. Click again at (1,-2) to define the other corner, and complete the rectangle. This closed rectangle region is slightly shaded. We then proceed to define the anode and cathode by drawing the two the rectangles (-0.2,0.2)(0.2,0) and (-1,-2)-(1,-2.2), respectively. The outline of the device structure is shown in figure.
- **Assigning Material** Every enclosed region in the drawing must be labelled and assigned a material **Regions.** To label Region such a region, one chooses the **Add Region Label** and click within one of the regions.

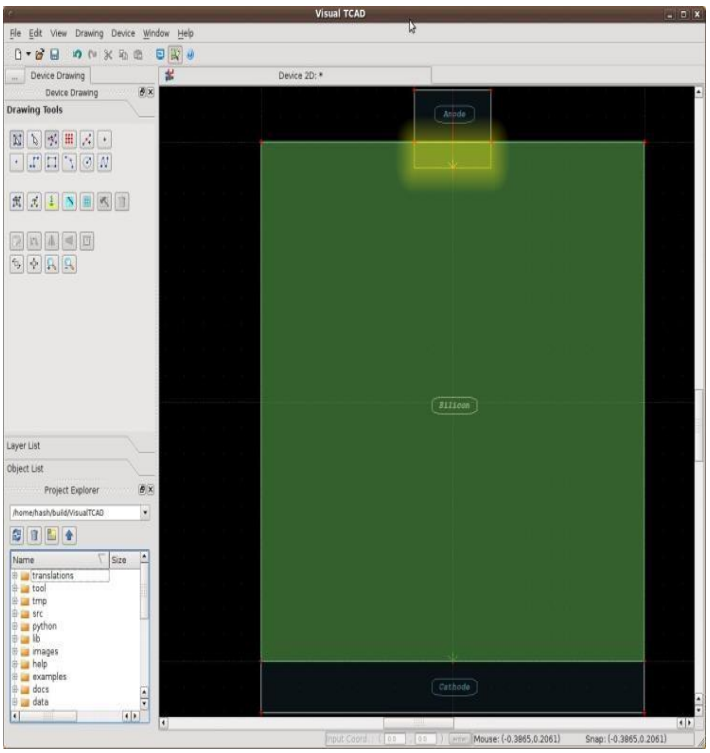




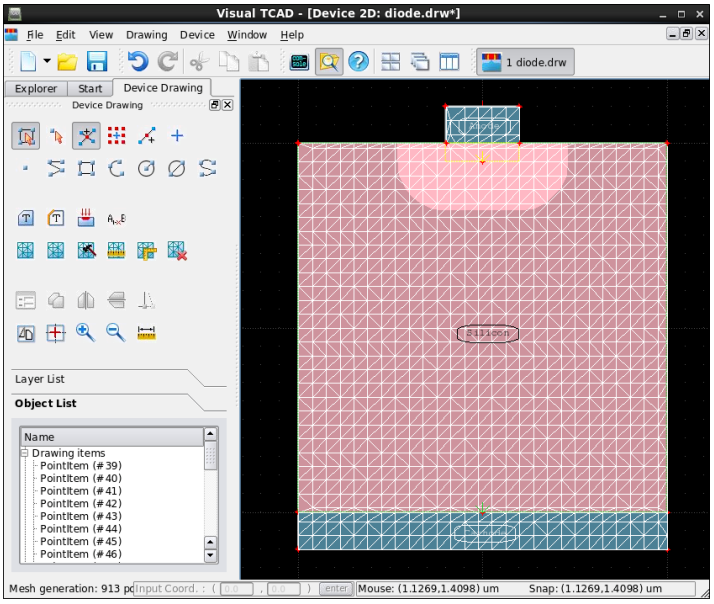
- Now doping is essential for semiconductor devices to function. To place a doping profile to the device, one chooses the **Add Doping Profile Tool.** A doping box consists of a baseline and a height, and the available doping functions include uniform, gaussian and Erf. Give the doping profile with respective concentration.

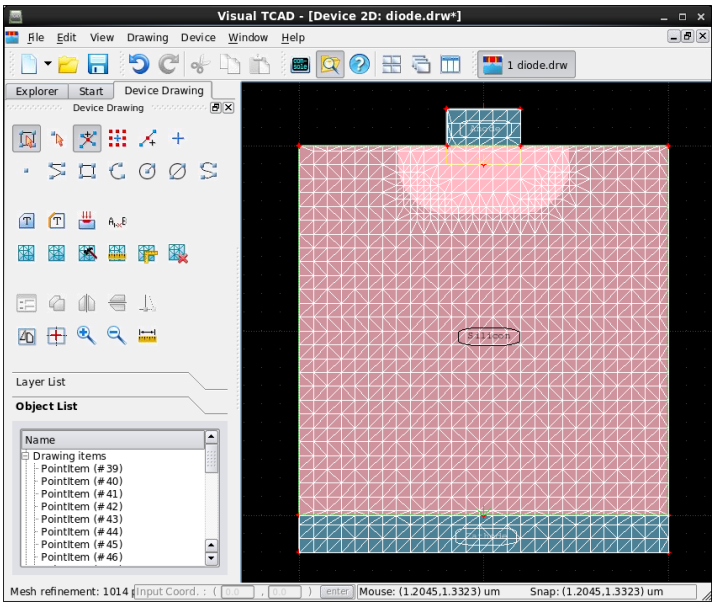




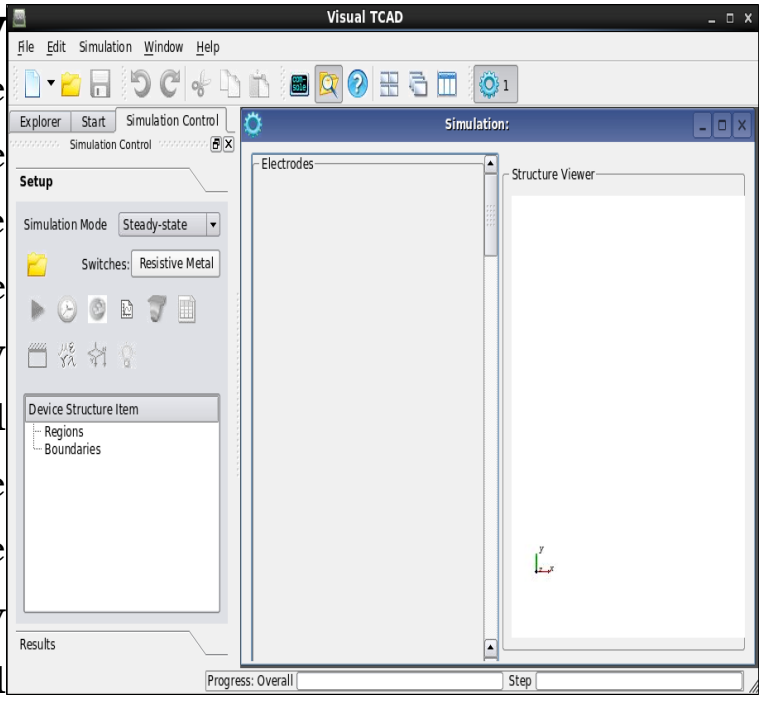


- **Meshing** the numerical device simulation always relies on a mesh grid that grid that divides the devices into many small elements. Click on the **Do Mesh** tool and accepts the default parameters in the mesh parameter dialog.

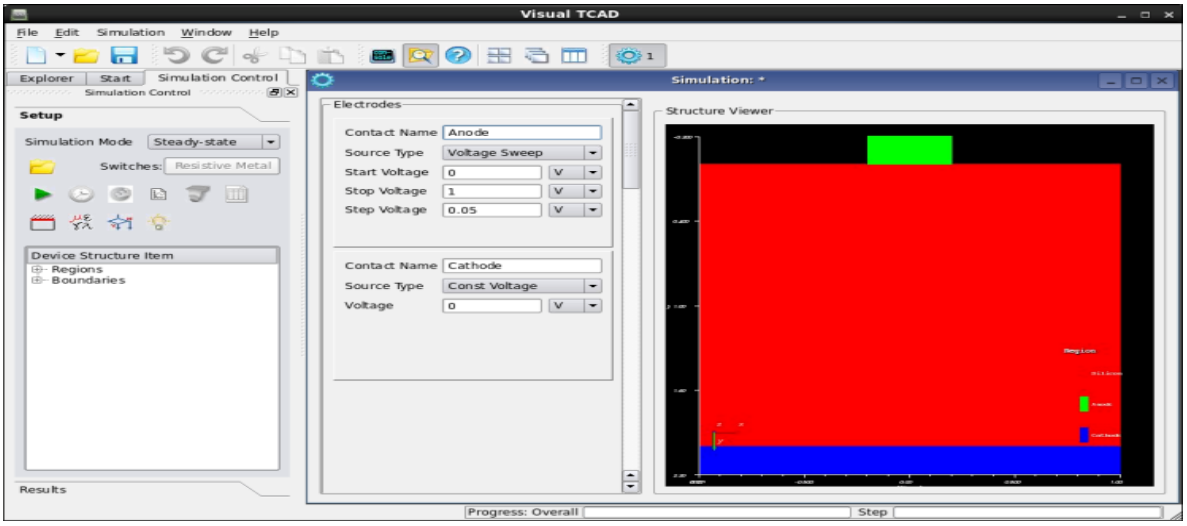




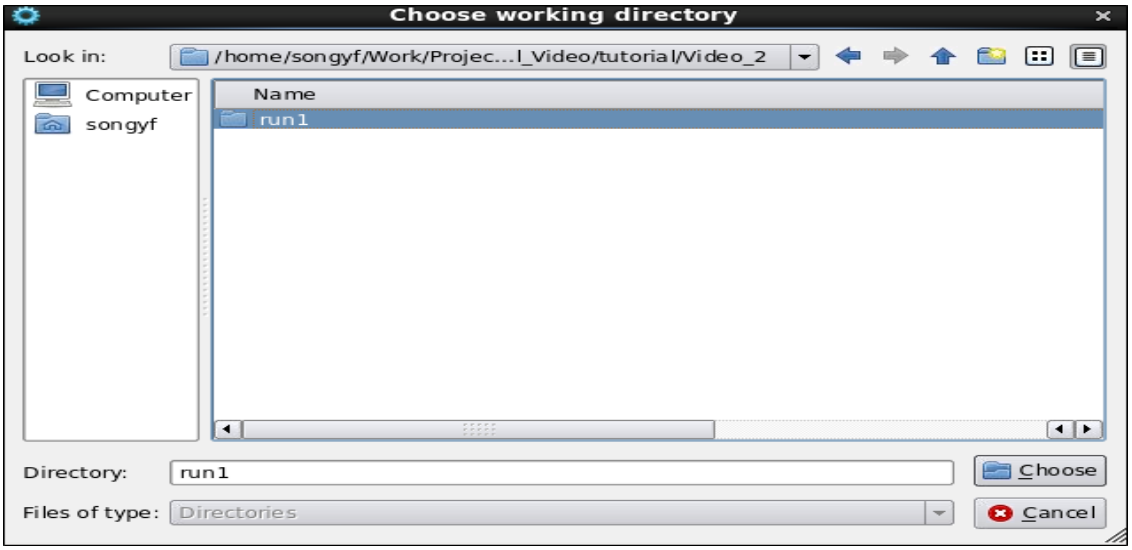
- **Saving the device** we save the device with **Save,** and key in the file name **.draw** additionally, we choose in the menu Device save mesh to file to export the mesh grid to **.tif.** We start by creating a new simulation control window by clicking in the menu file New Device Simulation. The empty simulation control window is appears as shown in below figure.



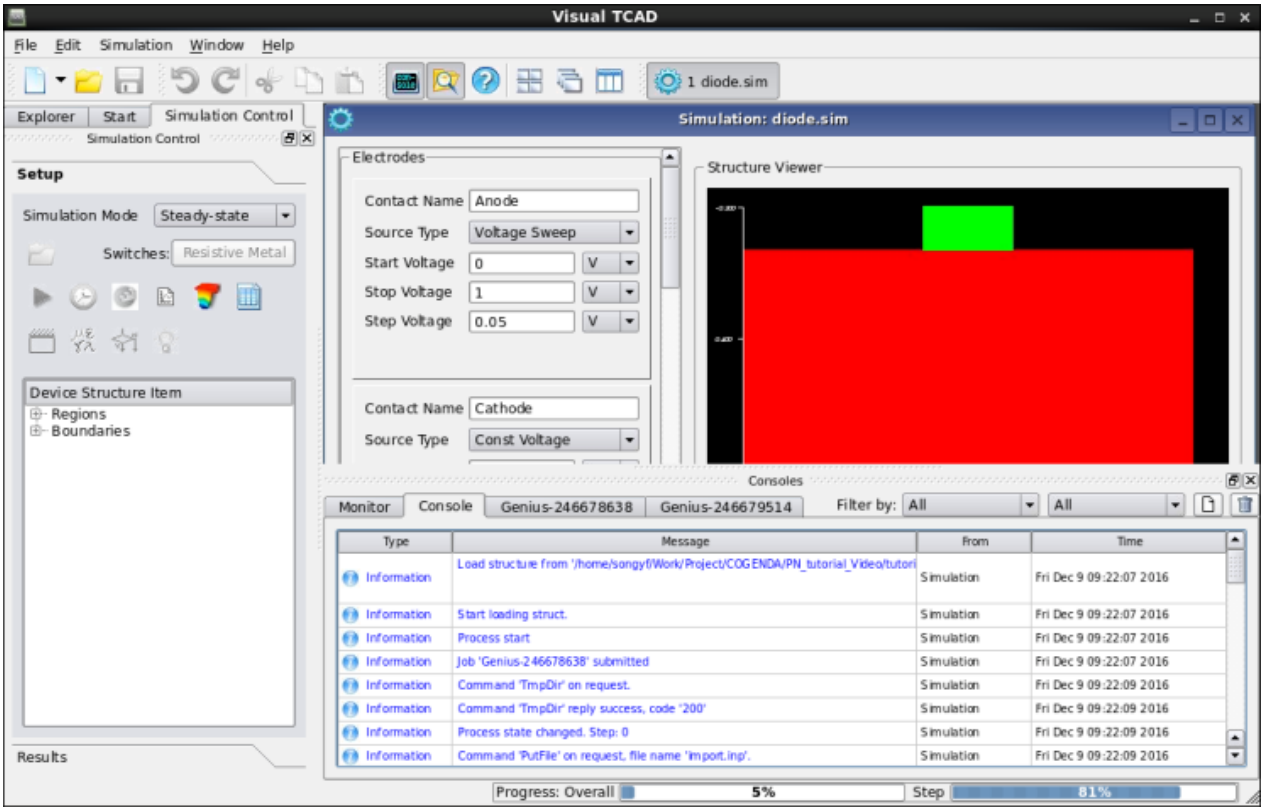
- **Loading Device Structure** we first load the device structure by clicking **Load** button. We select the .tif file, we just created. It takes a few seconds for Visual TCAD and Genius to analyse the tif file. When it finishes, the device structure is visualized.



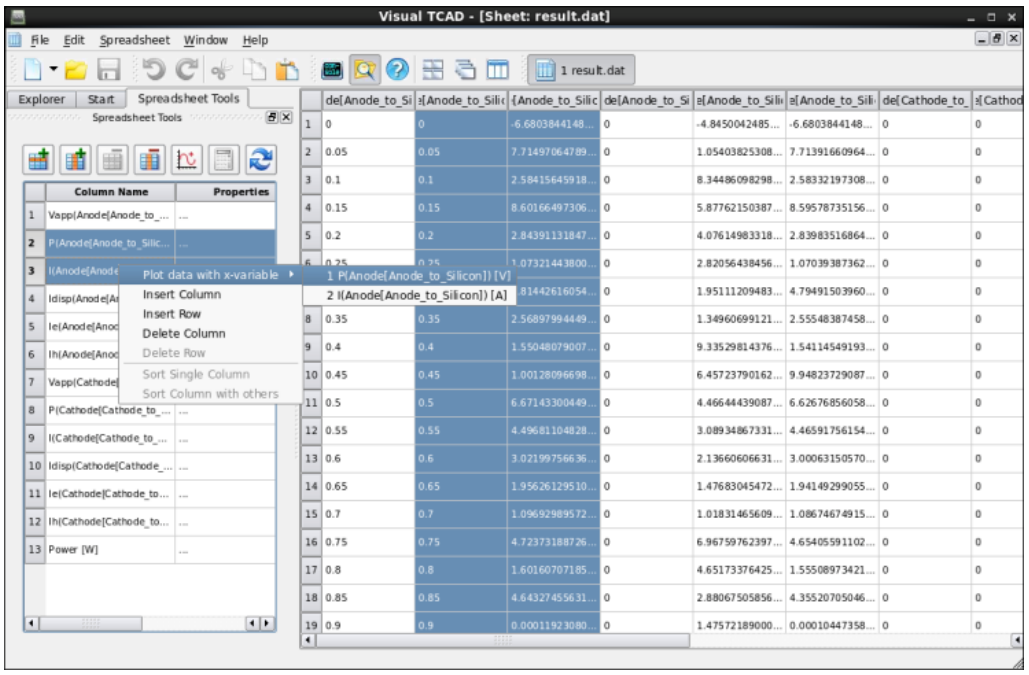
- **Starting Simulation,** we save the simulation setup to the file **.sim** To start the simulation job, click the job **Run** and choose a working directory in the dialog. We create a new directory called **run** and all the simulation results will be kept in this directory.



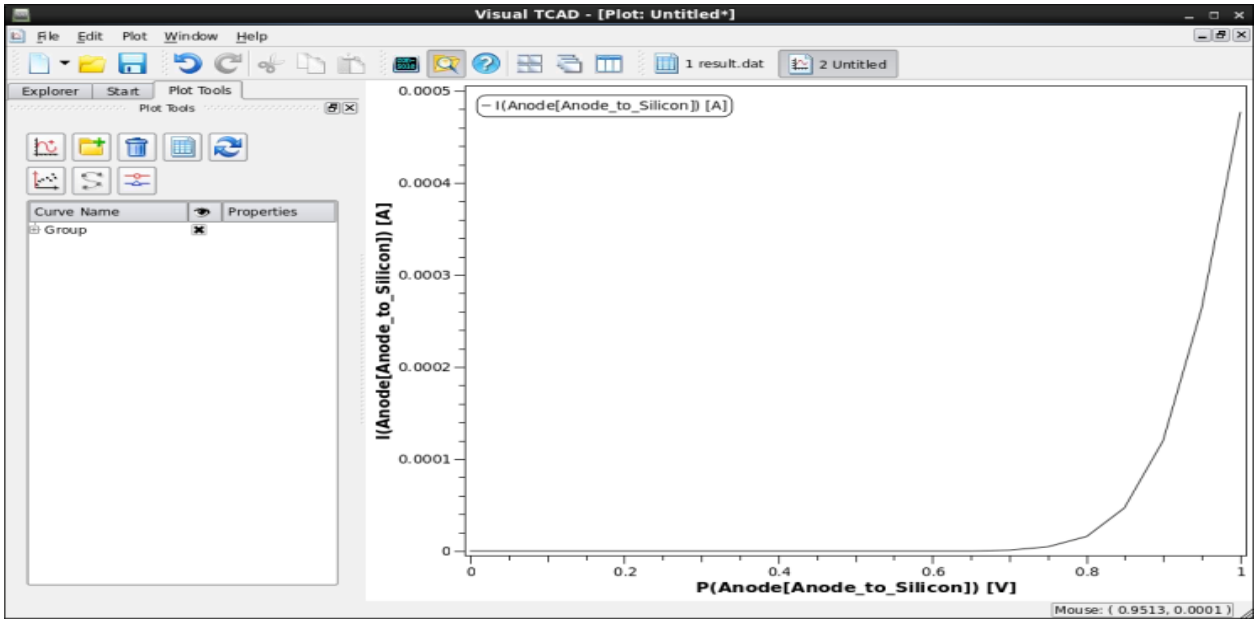
- **Monitoring Progress** as the simulation proceeds, the progress is updated in the status bar, at the right bottom corner of the window as shown in the below figure. For advanced users, the running log message is available in the process monitor, which is activated by clicking **console** in the toolbar.

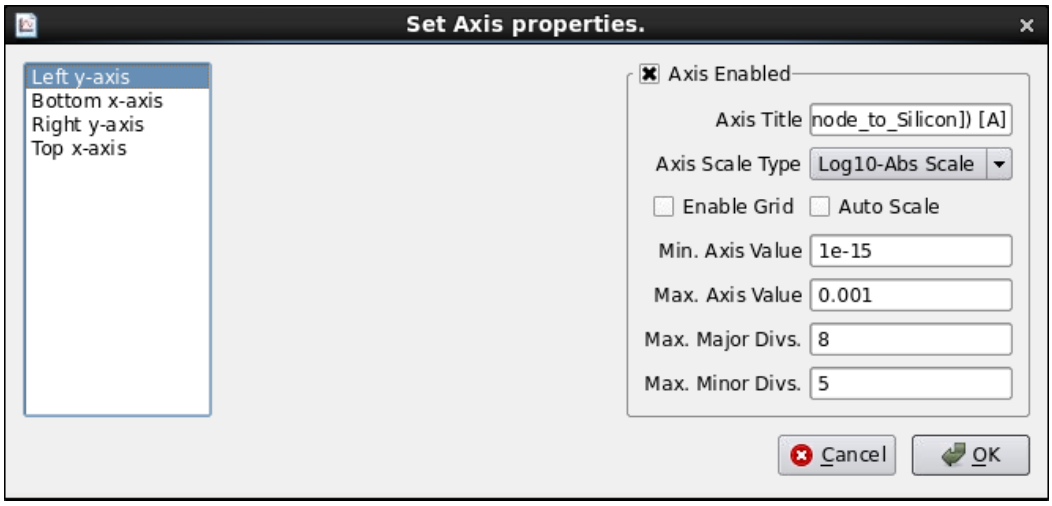


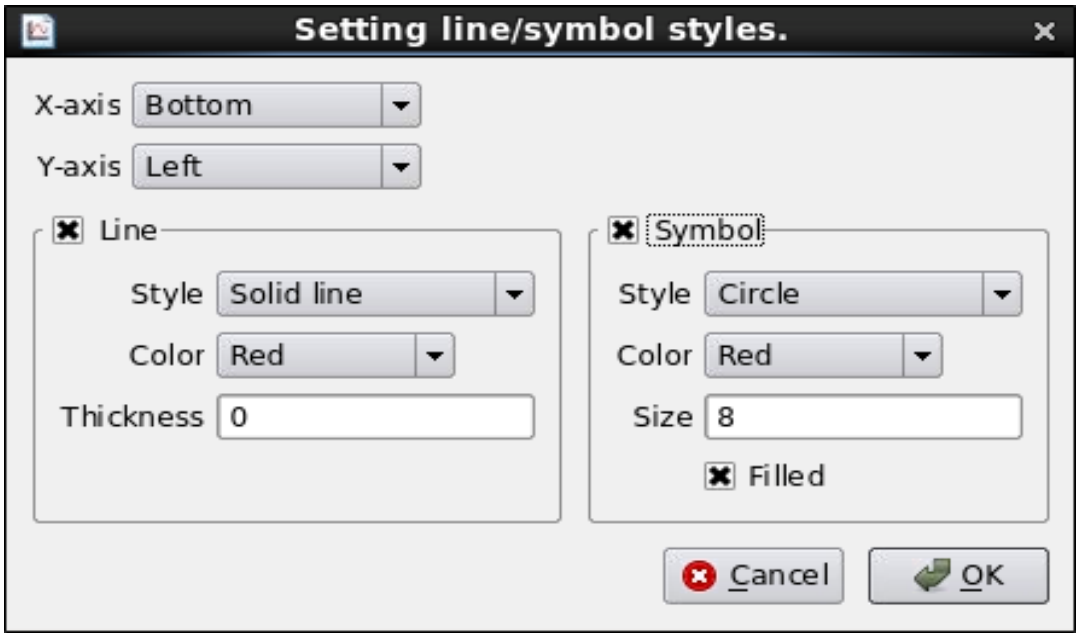
- **Examining the I-V Characteristics,** After the simulation completes, we wish to plot the I-V characteristics of the respective device. We can click the Show IV data button to open the spread sheet containing the terminal information of the solutions. The spread sheet is shown in the below figure.

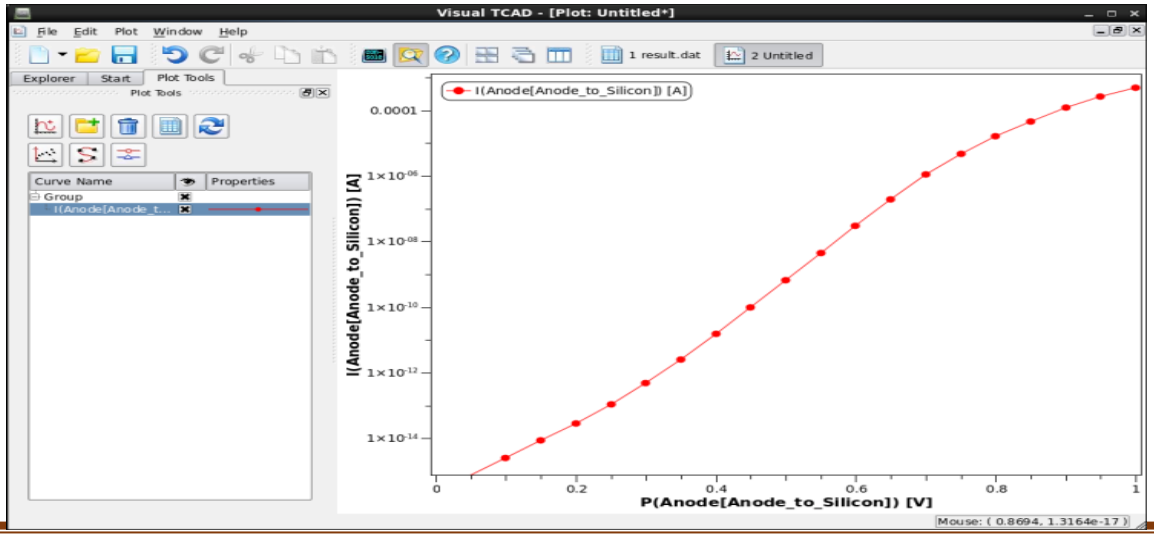


- **Plotting the I-V curve,** when we want to plot the data, one can select multiple columns by clicking on the column header and holding the Control key. When the two columns are selected, right click to activate the context menu, and choose to plot the data as shown in below figure.

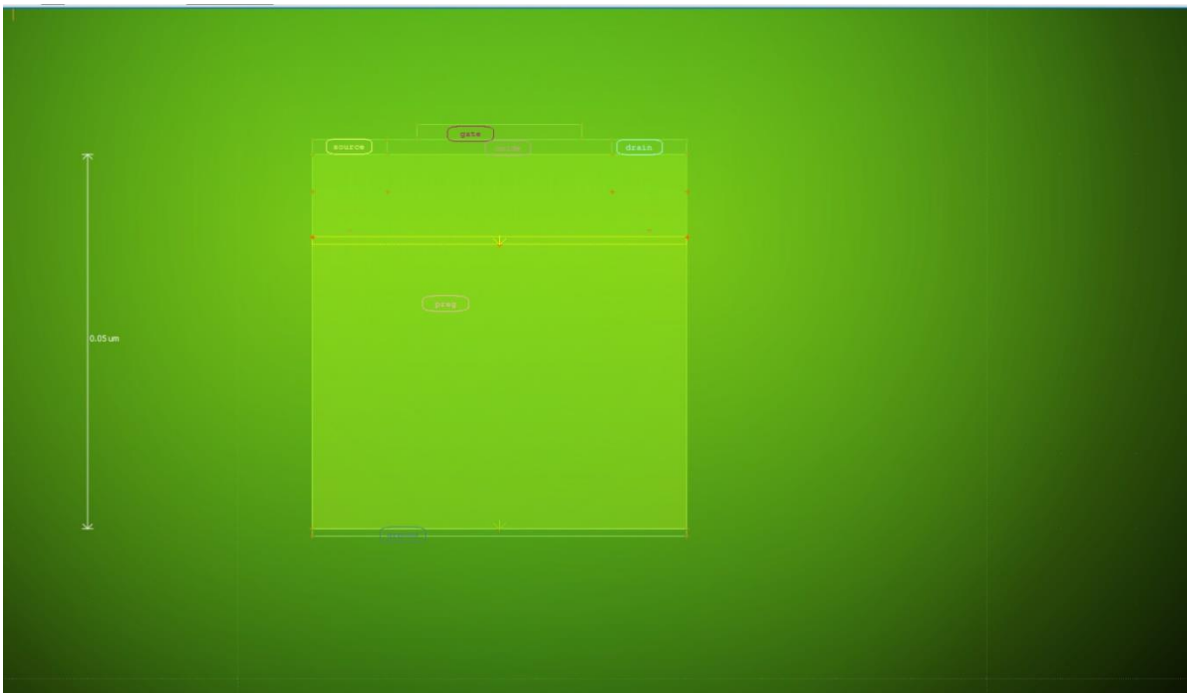



Set Axis properties.
Left y-axis
Bottom x-axis
Right y-axis
Top x-axis
Axis Enabled
Axis Title
node_to_Silicon]) [A]
Axis Scale Type
Log10-Abs Scale
Enable Grid
Auto Scale
Min. Axis Value
1e-15
Max. Axis Value
0.001
Max. Major Divs.
8
Max. Minor Divs.
5
Cancel
OK

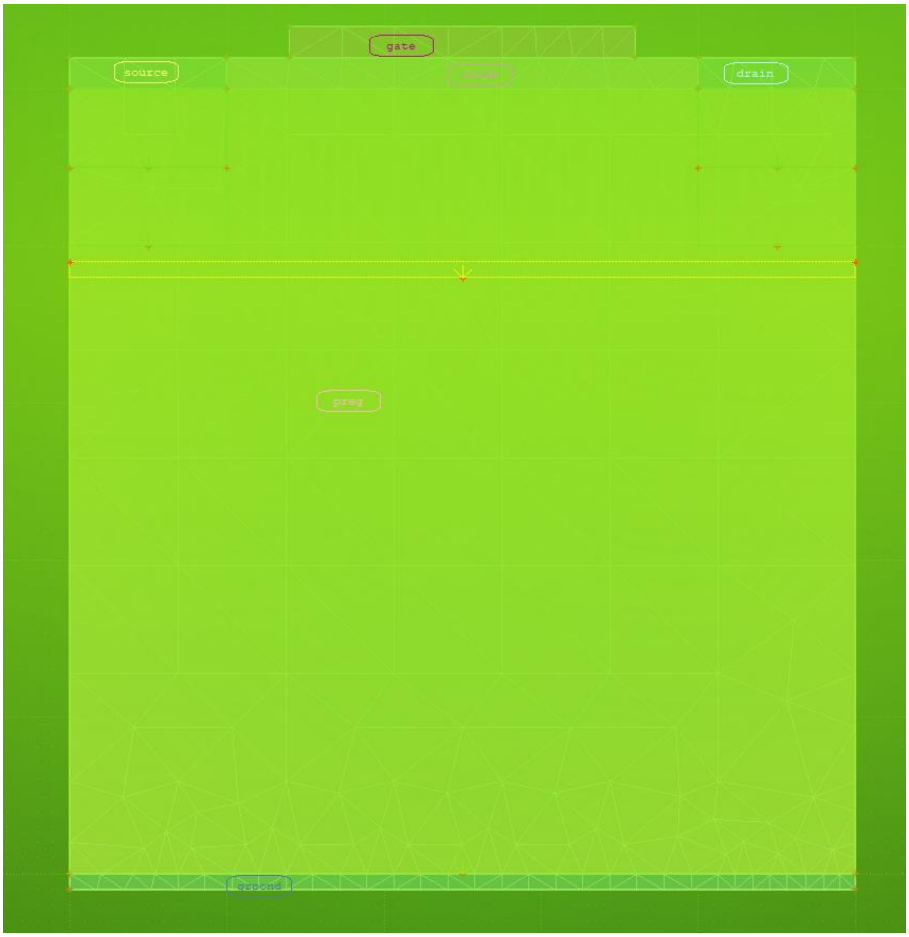

Setting line/symbol styles.
X-axis
Bottom
Y-axis
Left
Line
Style
Solid line
Color
Red
Thickness
0
Symbol
Style
Circle
Color
Red
Size
8
Filled
Cancel
OK


Visual TCAD - [Plot: Untitled*]
File Edit Plot Window Help
Explorer Start Plot Tools
Curve Name
Properties
I(Anode[Anode_to_Silicon]) [A]
P(Anode[Anode_to_Silicon]) [V]

PROPOSED DESIGN OF MOSFET IN THIS WORK



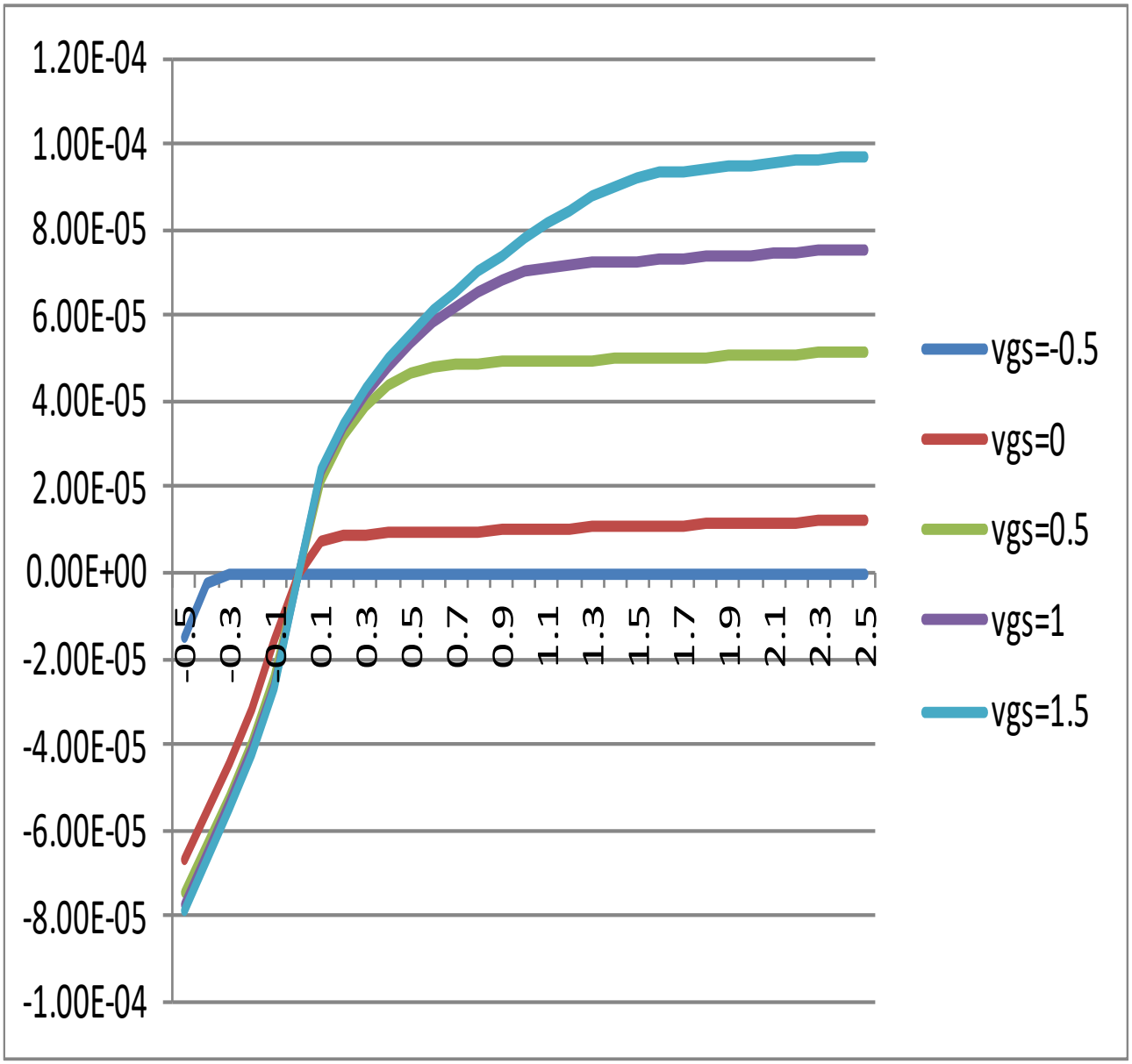
Mess Diagram:



6. Output & Waveforms

6.1 Outputs :

- **VI Characteristics of MOSFET (SiO2 as oxide layer)**

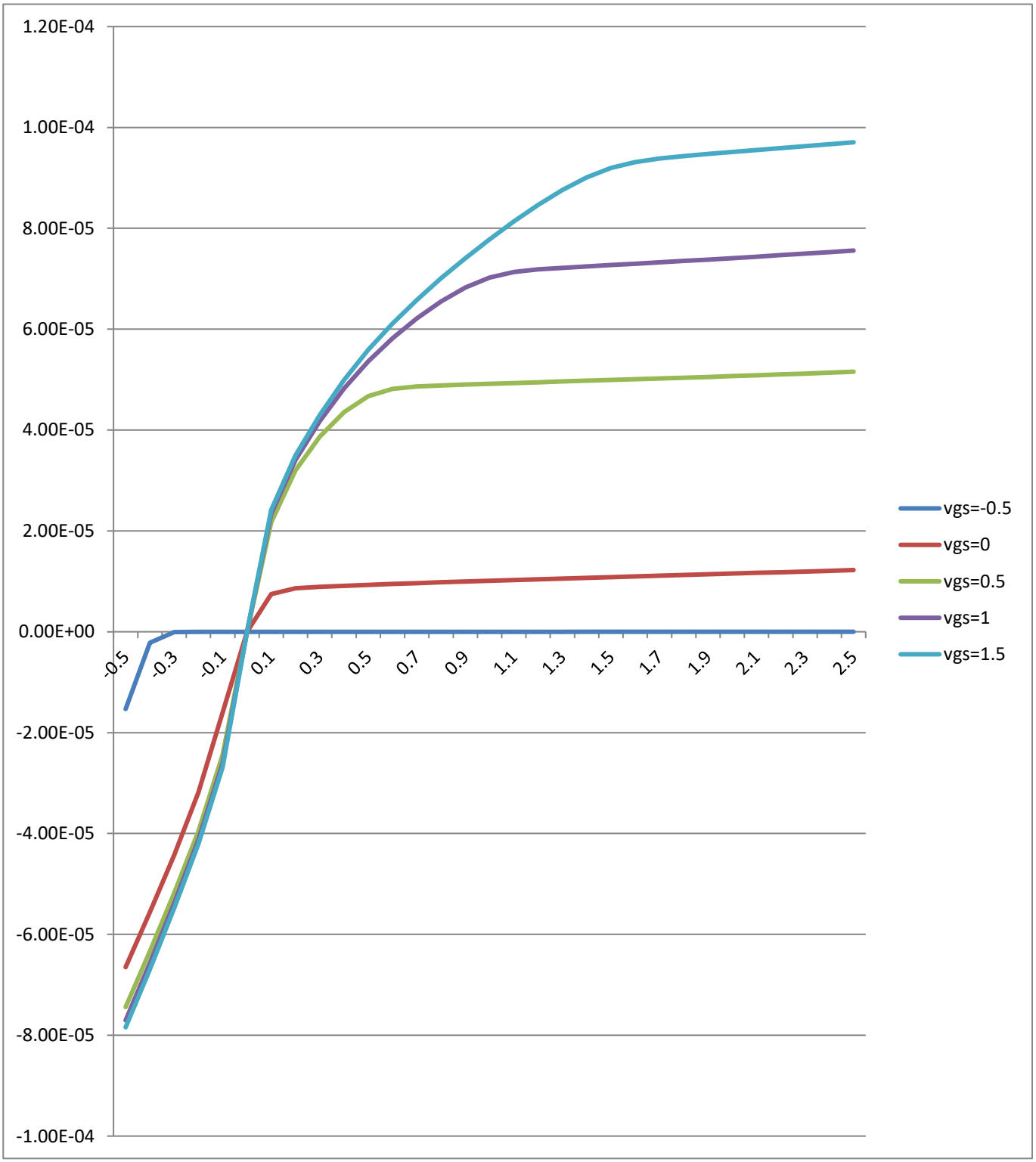


- **Values of current drain(Id) & gate to source voltage(SiO2) :**

id	vgs=-0.5	Vgs=0	Vgs=0.5	Vgs=1	Vgs=1.5
-0.5	-1.53E-05	-6.65E-05	-7.44E-05	-7.70E-05	-7.84E-05
-0.4	-2.20E-06	-5.56E-05	-6.34E-05	-6.57E-05	-6.69E-05
-0.3	-7.45E-08	-4.43E-05	-5.18E-05	-5.38E-05	-5.48E-05
-0.2	-1.71E-09	-3.19E-05	-3.96E-05	-4.13E-05	-4.21E-05
-0.1	-3.70E-11	-1.61E-05	-2.45E-05	-2.61E-05	-2.69E-05
-2.78E-17	-9.75E-19	-3.99E-19	4.05E-17	8.60E-18	2.91E-18
0.1	8.53E-13	7.45E-06	2.17E-05	2.34E-05	2.42E-05
0.2	9.11E-13	8.62E-06	3.20E-05	3.41E-05	3.49E-05
0.3	9.51E-13	8.91E-06	3.87E-05	4.17E-05	4.29E-05
0.4	9.91E-13	9.12E-06	4.36E-05	4.82E-05	4.99E-05
0.5	1.03E-12	9.31E-06	4.67E-05	5.36E-05	5.59E-05
0.6	1.07E-12	9.48E-06	4.82E-05	5.82E-05	6.11E-05
0.7	1.12E-12	9.64E-06	4.86E-05	6.21E-05	6.58E-05
0.8	1.17E-12	9.80E-06	4.88E-05	6.55E-05	7.01E-05
0.9	1.21E-12	9.95E-06	4.90E-05	6.83E-05	7.41E-05
1	1.26E-12	1.01E-05	4.92E-05	7.03E-05	7.78E-05
1.1	1.31E-12	1.03E-05	4.93E-05	7.14E-05	8.14E-05
1.2	1.36E-12	1.04E-05	4.95E-05	7.18E-05	8.46E-05
1.3	1.41E-12	1.05E-05	4.96E-05	7.22E-05	8.76E-05
1.4	1.47E-12	1.07E-05	4.98E-05	7.24E-05	9.01E-05
1.5	1.53E-12	1.08E-05	4.99E-05	7.27E-05	9.20E-05
1.6	1.59E-12	1.10E-05	5.01E-05	7.30E-05	9.31E-05
1.7	1.65E-12	1.11E-05	5.02E-05	7.32E-05	9.38E-05
1.8	1.72E-12	1.12E-05	5.04E-05	7.35E-05	9.43E-05
1.9	1.79E-12	1.14E-05	5.05E-05	7.38E-05	9.47E-05
2	1.86E-12	1.15E-05	5.07E-05	7.41E-05	9.51E-05
2.1	1.94E-12	1.17E-05	5.09E-05	7.44E-05	9.55E-05
2.2	2.02E-12	1.18E-05	5.10E-05	7.47E-05	9.59E-05
2.3	2.11E-12	1.20E-05	5.12E-05	7.50E-05	9.63E-05
2.4	2.20E-12	1.21E-05	5.14E-05	7.53E-05	9.67E-05

2.5	2.29E-12	1.22E-05	5.16E-05	7.56E-05	9.71E-05

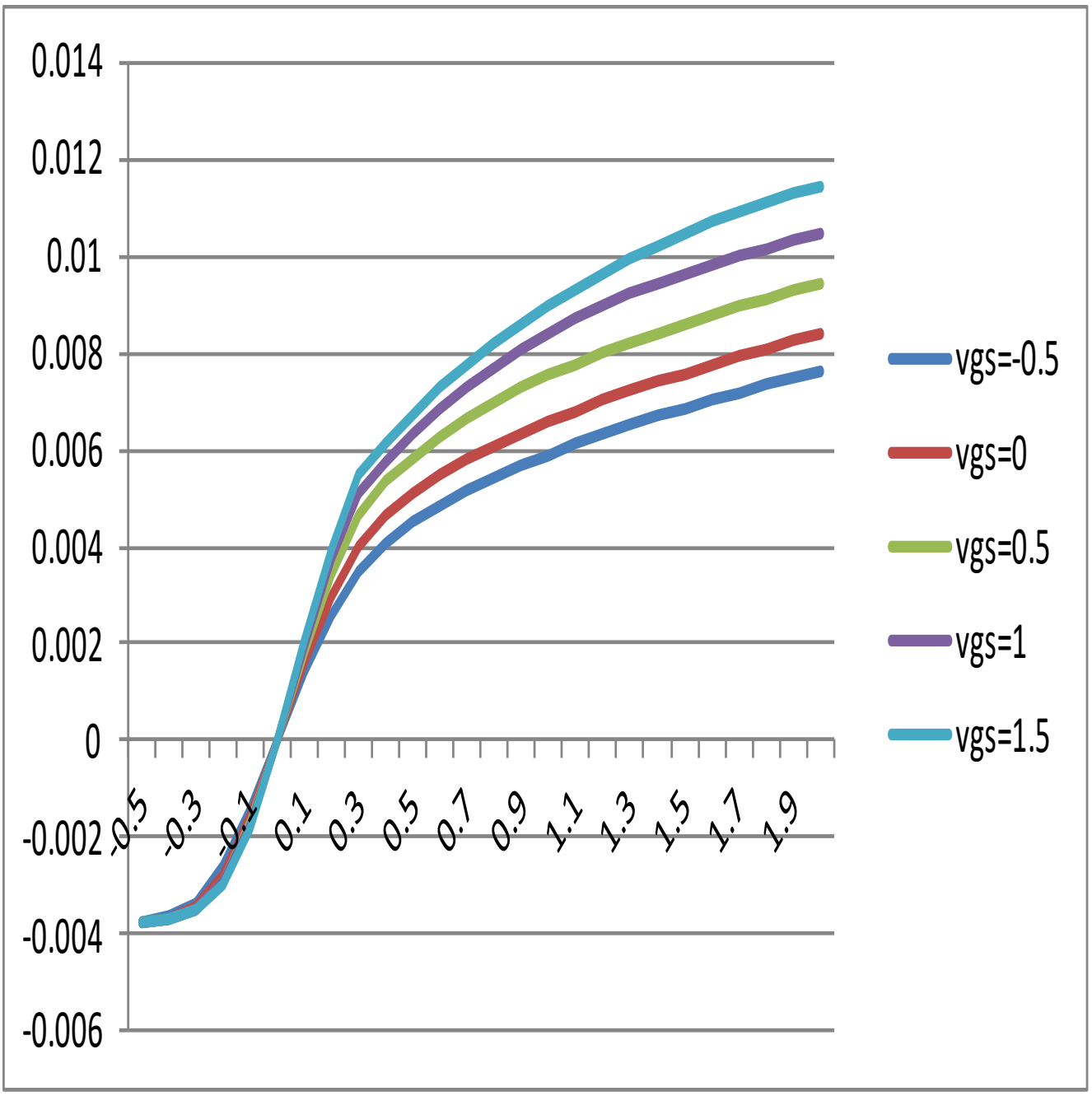
- **VI Characteristics of MOSFET (HfO2 as oxide layer)**



- **Values of current drain(Id) & gate to source voltage(HfO2) :**

ID	vgs=-0.5	Vgs=0	Vgs=0.5	Vgs = 1	Vgs = 1.5
-0.5	-1.53E-05	-6.65E-05	-7.44E-05	-7.70E-05	-7.84E-05
-0.4	-2.20E-06	-5.56E-05	-6.34E-05	-6.57E-05	-6.69E-05
-0.3	-7.45E-08	-4.43E-05	-5.18E-05	-5.38E-05	-5.48E-05
-0.2	-1.71E-09	-3.19E-05	-3.96E-05	-4.13E-05	-4.21E-05
-0.1	-3.70E-11	-1.61E-05	-2.45E-05	-2.61E-05	-2.69E-05
-2.78E-17	-9.75E-19	-3.99E-19	4.05E-17	8.60E-18	2.91E-18
0.1	8.53E-13	7.45E-06	2.17E-05	2.34E-05	2.42E-05
0.2	9.11E-13	8.62E-06	3.20E-05	3.41E-05	3.49E-05
0.3	9.51E-13	8.91E-06	3.87E-05	4.17E-05	4.29E-05
0.4	9.91E-13	9.12E-06	4.36E-05	4.82E-05	4.99E-05
0.5	1.03E-12	9.31E-06	4.67E-05	5.36E-05	5.59E-05
0.6	1.07E-12	9.48E-06	4.82E-05	5.82E-05	6.11E-05
0.7	1.12E-12	9.64E-06	4.86E-05	6.21E-05	6.58E-05
0.8	1.17E-12	9.80E-06	4.88E-05	6.55E-05	7.01E-05
0.9	1.21E-12	9.95E-06	4.90E-05	6.83E-05	7.41E-05
1	1.26E-12	1.01E-05	4.92E-05	7.03E-05	7.78E-05
1.1	1.31E-12	1.03E-05	4.93E-05	7.14E-05	8.14E-05
1.2	1.36E-12	1.04E-05	4.95E-05	7.18E-05	8.46E-05
1.3	1.41E-12	1.05E-05	4.96E-05	7.22E-05	8.76E-05
1.4	1.47E-12	1.07E-05	4.98E-05	7.24E-05	9.01E-05
1.5	1.53E-12	1.08E-05	4.99E-05	7.27E-05	9.20E-05
1.6	1.59E-12	1.10E-05	5.01E-05	7.30E-05	9.31E-05
1.7	1.65E-12	1.11E-05	5.02E-05	7.32E-05	9.38E-05
1.8	1.72E-12	1.12E-05	5.04E-05	7.35E-05	9.43E-05
1.9	1.79E-12	1.14E-05	5.05E-05	7.38E-05	9.47E-05
2	1.86E-12	1.15E-05	5.07E-05	7.41E-05	9.51E-05
2.1	1.94E-12	1.17E-05	5.09E-05	7.44E-05	9.55E-05
2.2	2.02E-12	1.18E-05	5.10E-05	7.47E-05	9.59E-05
2.3	2.11E-12	1.20E-05	5.12E-05	7.50E-05	9.63E-05
2.4	2.20E-12	1.21E-05	5.14E-05	7.53E-05	9.67E-05
2.5	2.29E-12	1.22E-05	5.16E-05	7.56E-05	9.71E-05

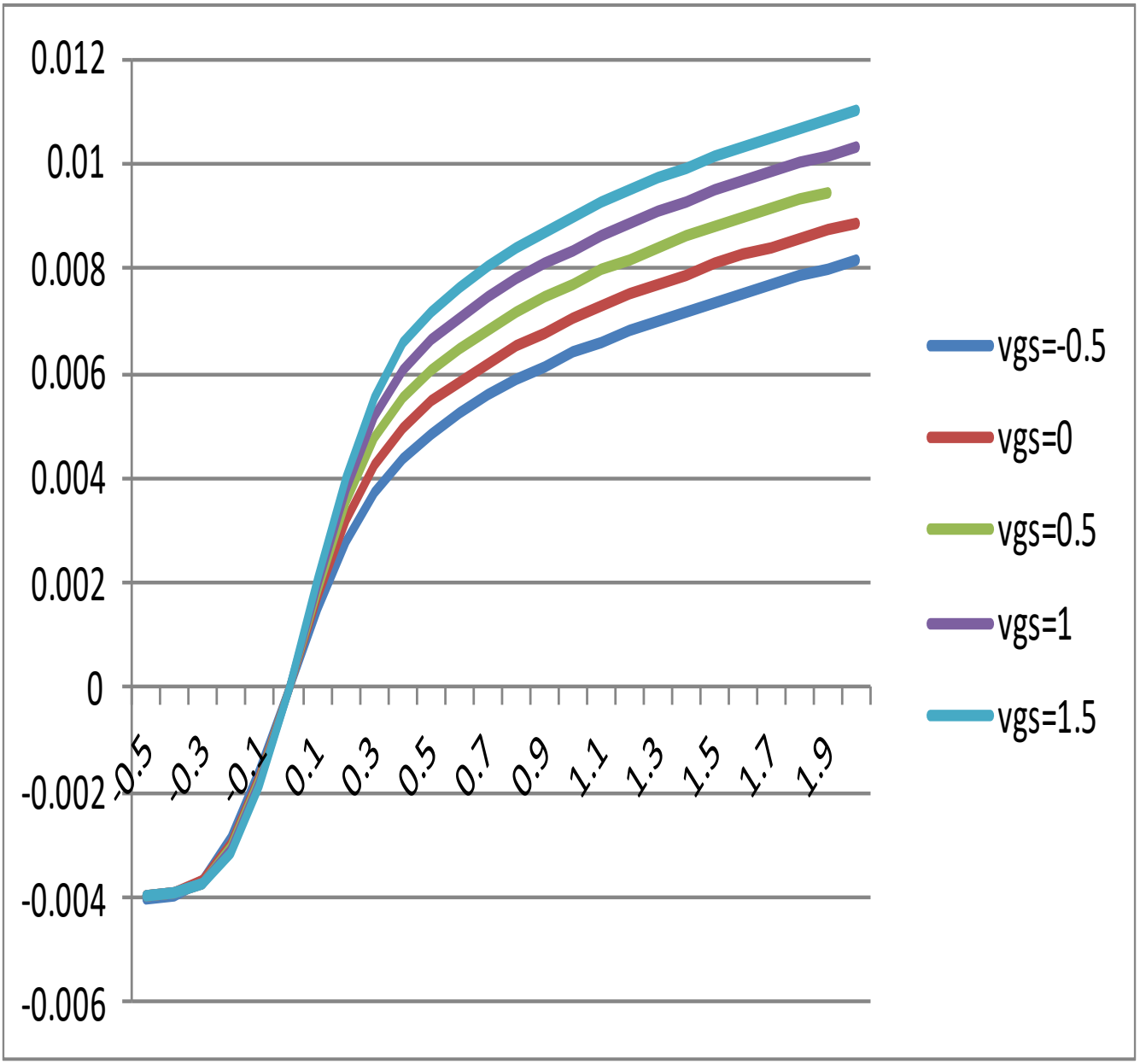
- **VI Characteristics of MOSFET (epoxy as oxide layer)**



- **Values of current drain(Id) & gate to source voltage(epoxy) :**

I(d)	Vgs= -0.5	Vgs = 0	Vgs = 0.5	Vgs = 1	Vgs = 1.5
-0.5	-0.00376	-0.00377	-0.00377	-0.00377	-0.00377
-0.4	-0.00366	-0.00369	-0.0037	-0.00371	-0.00371
-0.3	-0.00335	-0.00345	-0.0035	-0.00352	-0.00354
-0.2	-0.0026	-0.00279	-0.00289	-0.00295	-0.00299
-0.1	-0.00142	-0.00158	-0.0017	-0.00177	-0.00181
-2.78E-17	5.67E-20	-3.74E-17	-1.97E-17	6.04E-17	2.01E-16
0.1	0.001404	0.001602	0.001809	0.001945	0.002046
0.2	0.002601	0.002957	0.003411	0.00372	0.003957
0.3	0.003503	0.003983	0.004647	0.005118	0.005492
0.4	0.00409	0.004677	0.005333	0.005773	0.006118
0.5	0.004516	0.005098	0.00584	0.006353	0.006742
0.6	0.004864	0.005469	0.006281	0.006866	0.007297
0.7	0.005163	0.00579	0.006657	0.007315	0.007785
0.8	0.005429	0.006076	0.006984	0.007716	0.008222
0.9	0.005672	0.006335	0.007274	0.008078	0.00862
1	0.005898	0.006575	0.007536	0.008407	0.008987
1.1	0.00611	0.006799	0.007778	0.008704	0.009329
1.2	0.006312	0.00701	0.008002	0.008973	0.00965
1.3	0.006505	0.007211	0.008213	0.009214	0.00995
1.4	0.00669	0.007402	0.008412	0.009433	0.010231
1.5	0.006867	0.007585	0.008602	0.009634	0.01049
1.6	0.007037	0.00776	0.008783	0.009822	0.010728
1.7	0.007201	0.007928	0.008955	0.009999	0.010944
1.8	0.007359	0.008088	0.00912	0.010167	0.011137
1.9	0.00751	0.008243	0.009278	0.010327	0.01131
2	0.007657	0.008391	0.00943	0.01048	0.011468

- **VI Characteristics of MOSFET (SiO2 of oxide layer with thickness of 0.002um)**



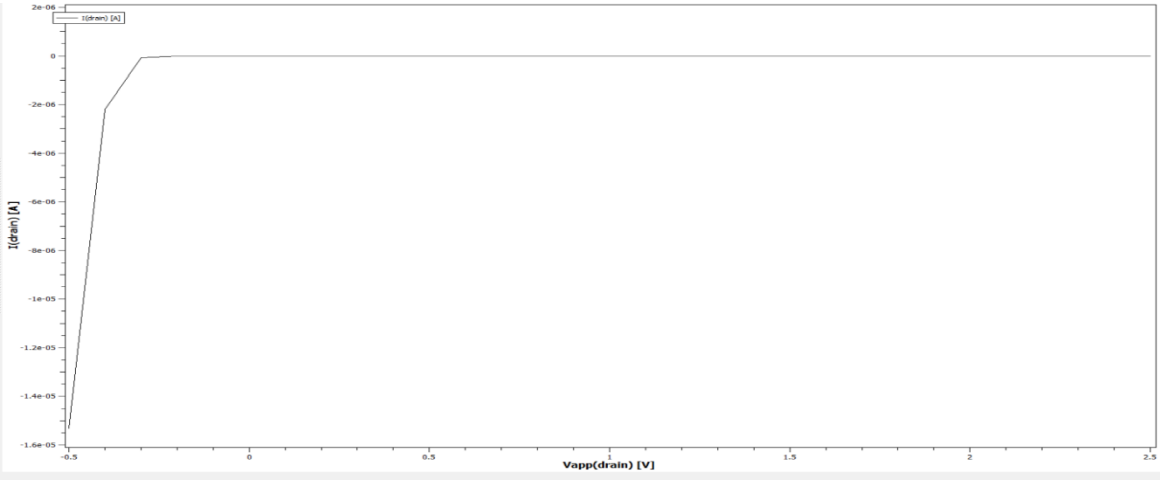
- **Values of current drain(Id) & gate to source voltage(SiO2 of oxide layer with thickness of 0.002um):**

I(d)	Vgs = -0.5	Vgs = 0	Vgs = 0.5	Vgs = 1	Vgs = 1.5
-0.5	-0.00402	-0.00398	-0.00397	-0.00396	-0.00395
-0.4	-0.00394	-0.00392	-0.00391	-0.0039	-0.00389
-0.3	-0.00365	-0.00369	-0.00371	-0.00371	-0.00372
-0.2	-0.00286	-0.00299	-0.00306	-0.0031	-0.00313
-0.1	-0.00156	-0.00169	-0.00177	-0.00182	-0.00186
-2.78E-17	1.50E-16	2.09E-16	6.95E-17	1.71E-15	6.87E-15
0.1	0.001533	0.001732	0.001887	0.002	0.002088
0.2	0.002823	0.003205	0.00354	0.003802	0.004006
0.3	0.003756	0.004273	0.004765	0.00519	0.005539
0.4	0.004387	0.004957	0.005531	0.006072	0.006568
0.5	0.00486	0.005447	0.00605	0.006629	0.007176
0.6	0.00525	0.00585	0.006473	0.007075	0.00765
0.7	0.005584	0.006197	0.006836	0.007455	0.008051
0.8	0.005877	0.006504	0.007157	0.007788	0.008397
0.9	0.006141	0.006781	0.007445	0.008086	0.008705
1	0.006382	0.007034	0.007709	0.008358	0.008983
1.1	0.006605	0.007268	0.007954	0.008609	0.00924
1.2	0.006814	0.007487	0.008182	0.008844	0.009479
1.3	0.007009	0.007693	0.008396	0.009064	0.009703
1.4	0.007194	0.007887	0.008598	0.009273	0.009915
1.5	0.007369	0.008071	0.008789	0.00947	0.010115
1.6	0.007536	0.008246	0.00897	0.009657	0.010306
1.7	0.007694	0.008413	0.009142	0.009834	0.010488
1.8	0.007846	0.008571	0.009306	0.010004	0.010661
1.9	0.007992	0.008723	0.009462	0.010165	0.010826
2	0.008132	0.008869	0.009611	0.010319	0.010984

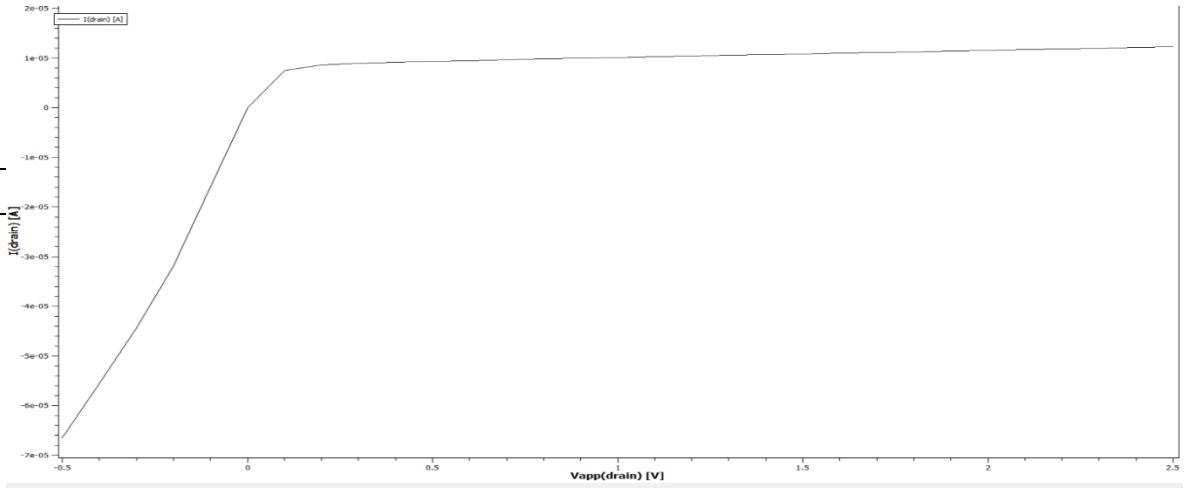
6.2 Obtained Waveforms:

- **SiO2 as oxide layer :**

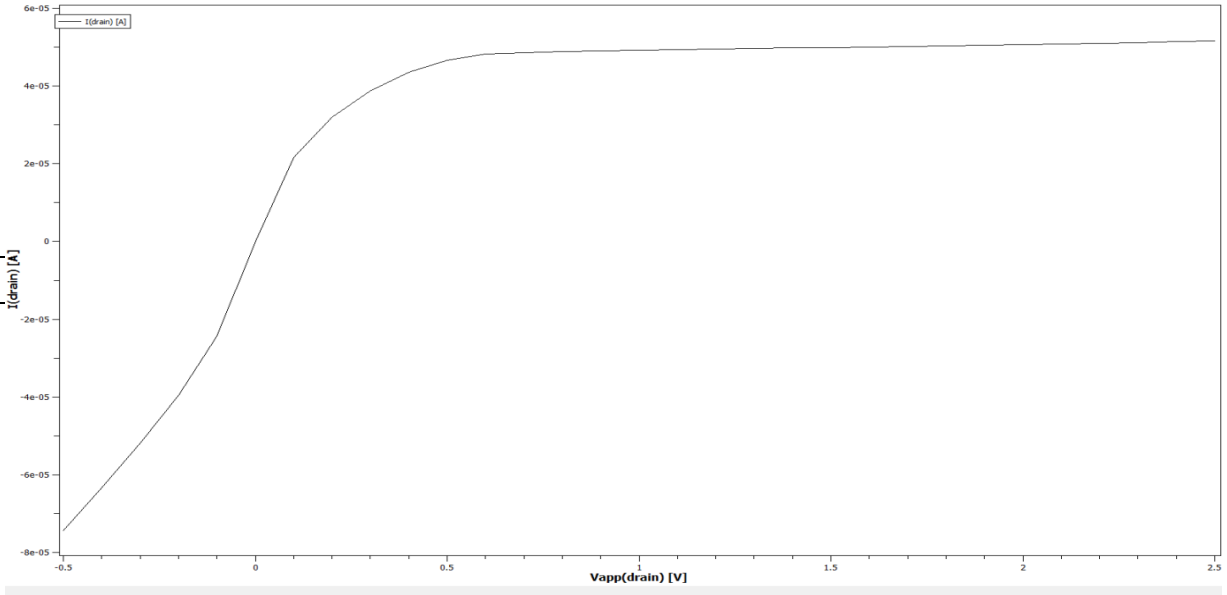
SiO2 Vgs = -0.5V

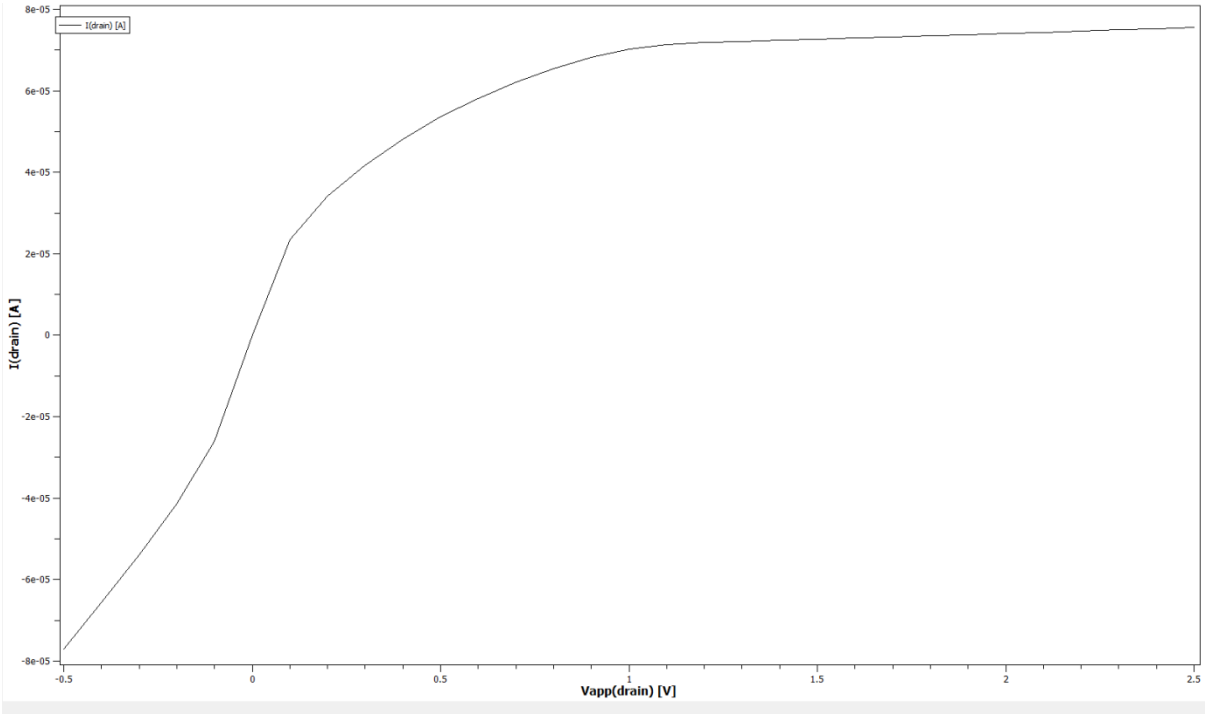


SiO2 Vgs = 0V

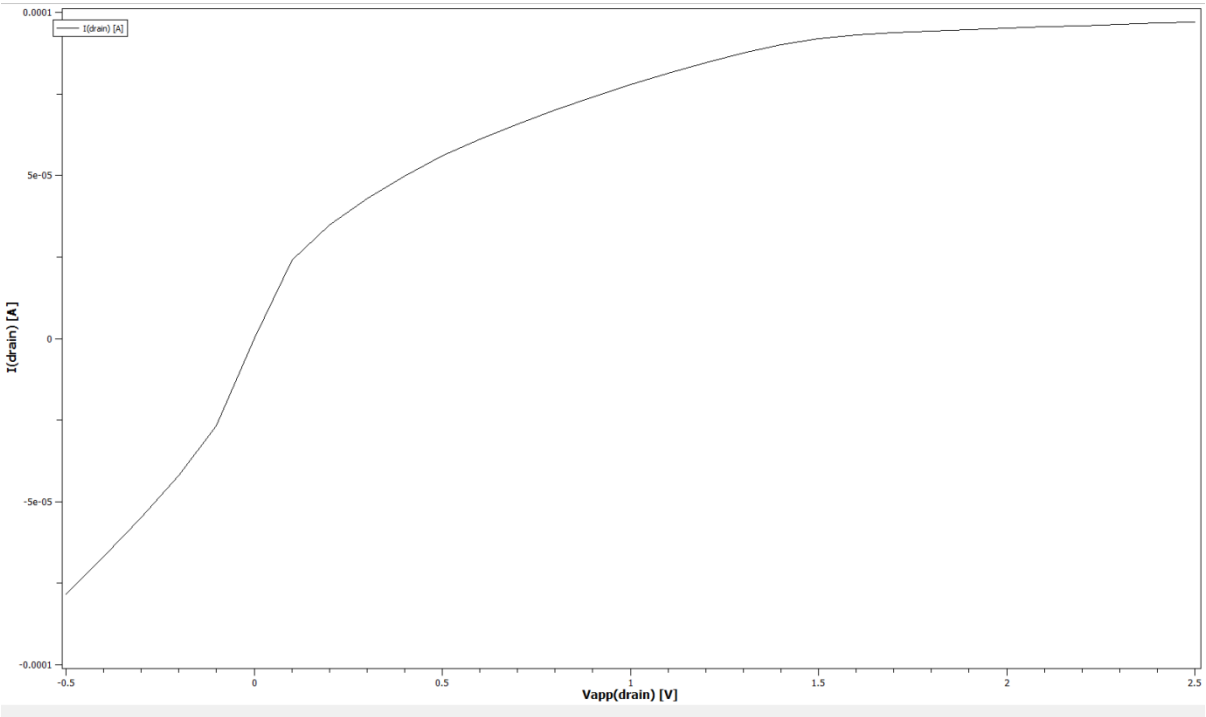


SiO2 Vgs = 0.5V





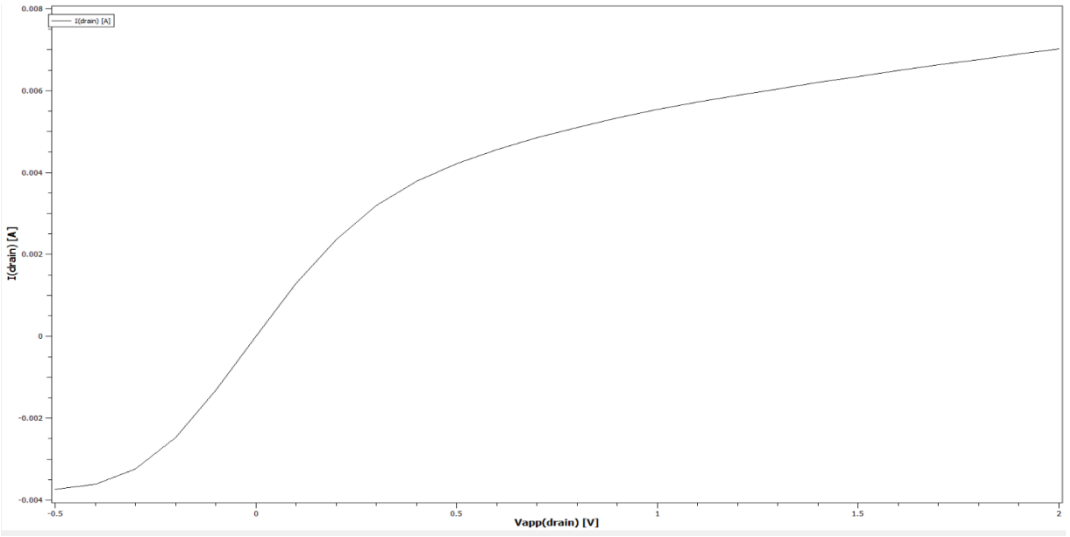
SiO2 Vgs = 1 V



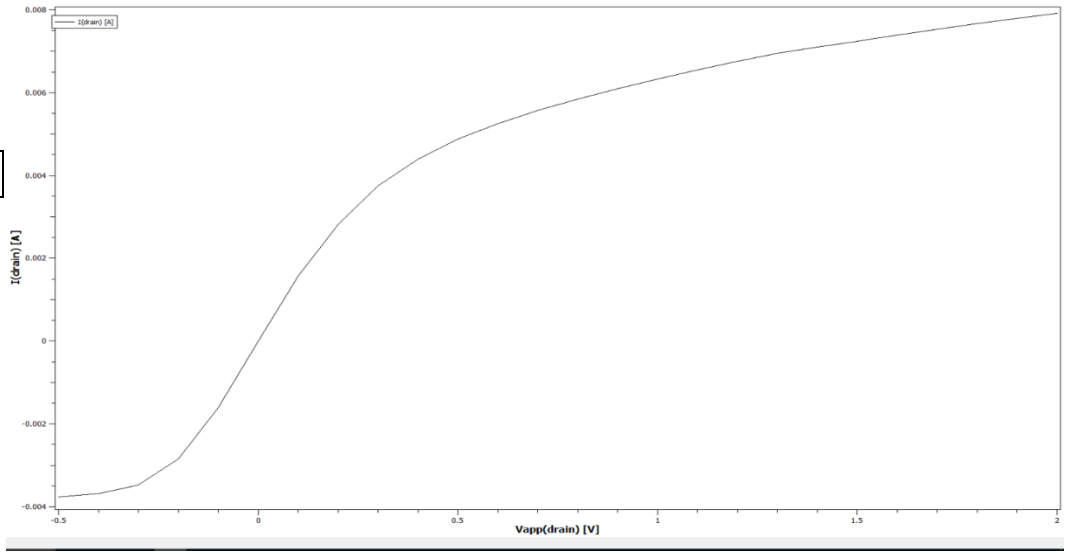
SiO2 Vgs = 1.5V

- **HfO2 as oxide layer :**

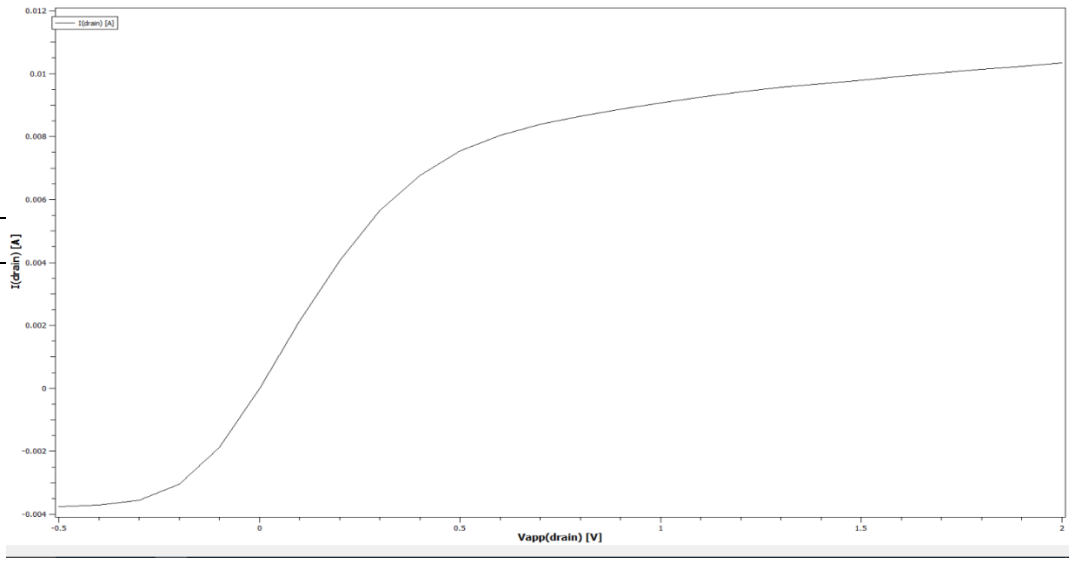
HfO2 Vgs = -0.5 V

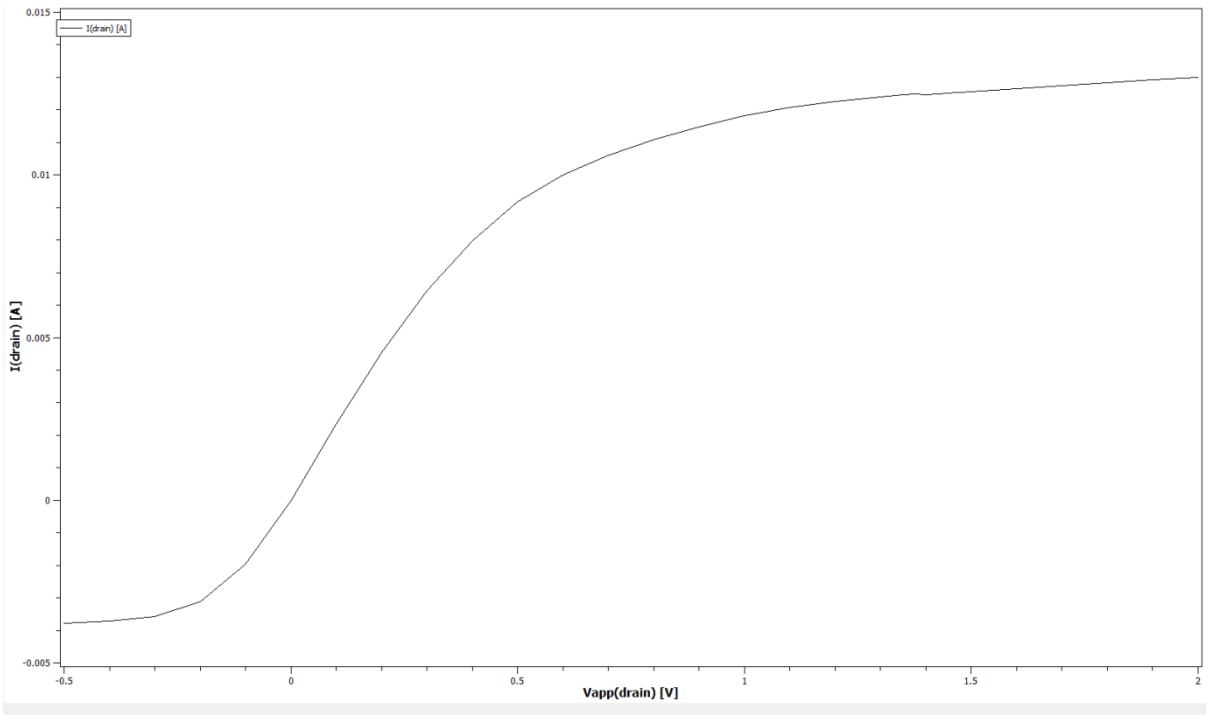


HfO2 Vgs = 0 V

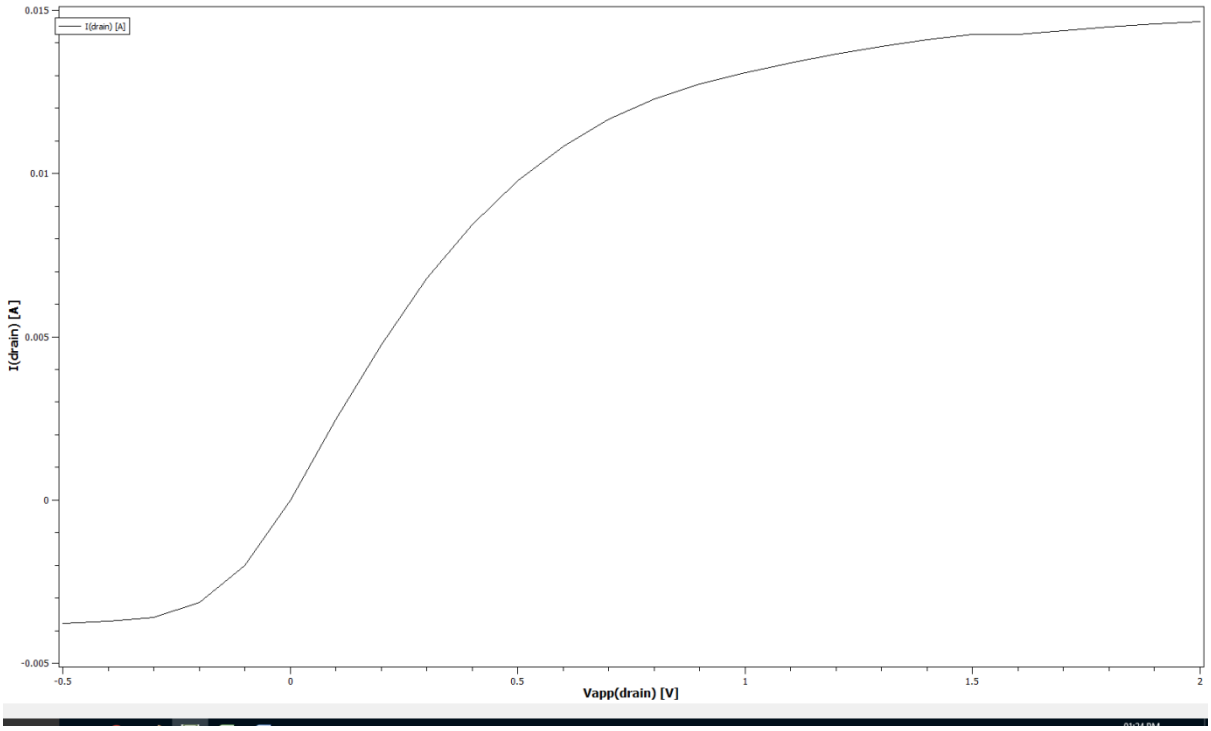


HfO2 Vgs = 0.5 V





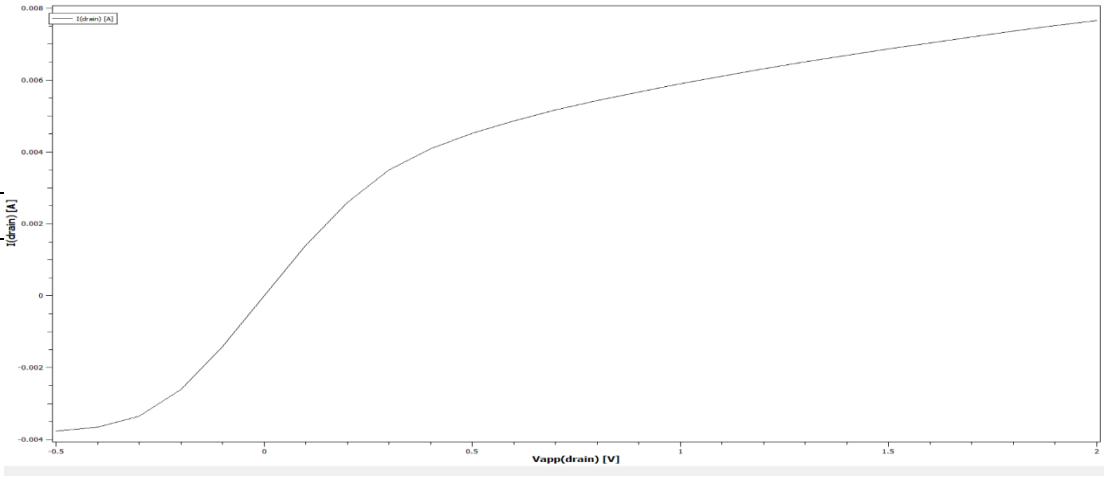
HfO2 Vgs = 1 V



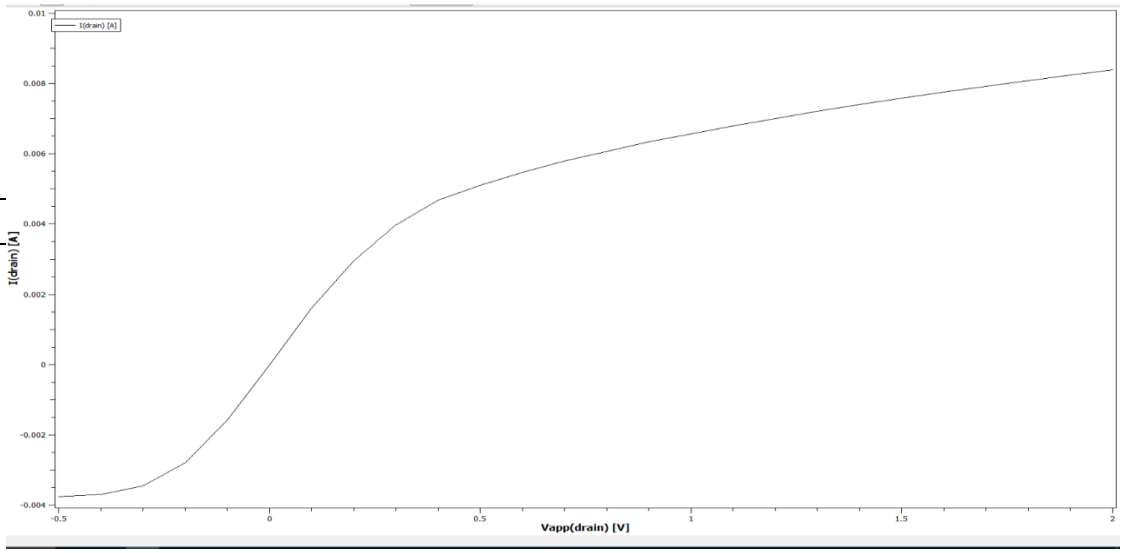
HfO2 Vgs = 1.5 V

- **Epoxy as oxide layer :**

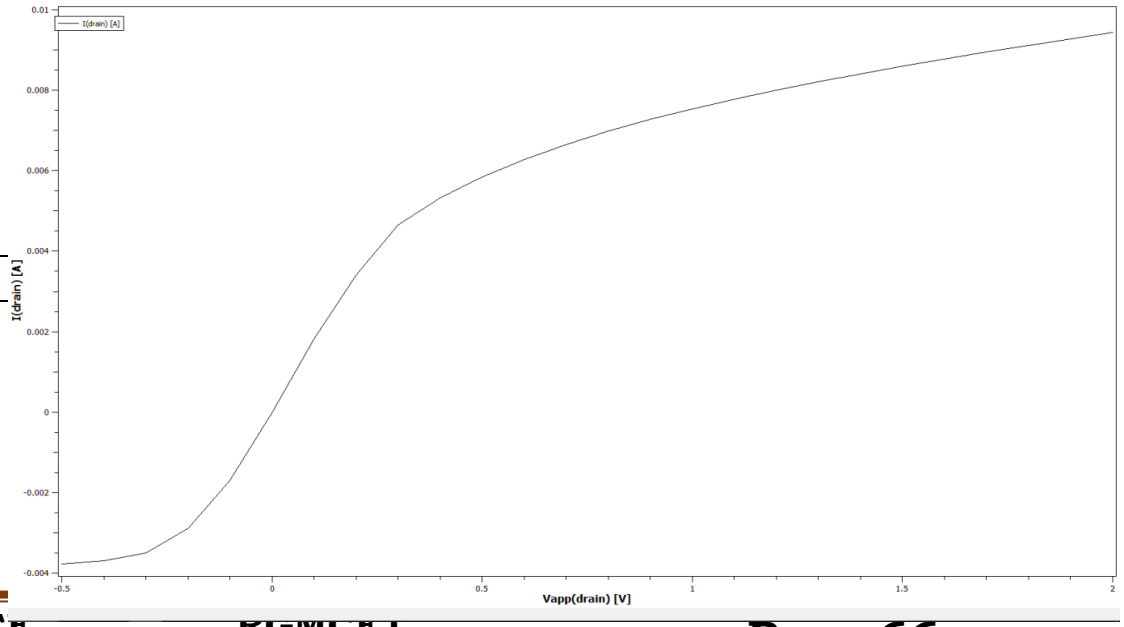
Epoxy Vgs = -0.5 V

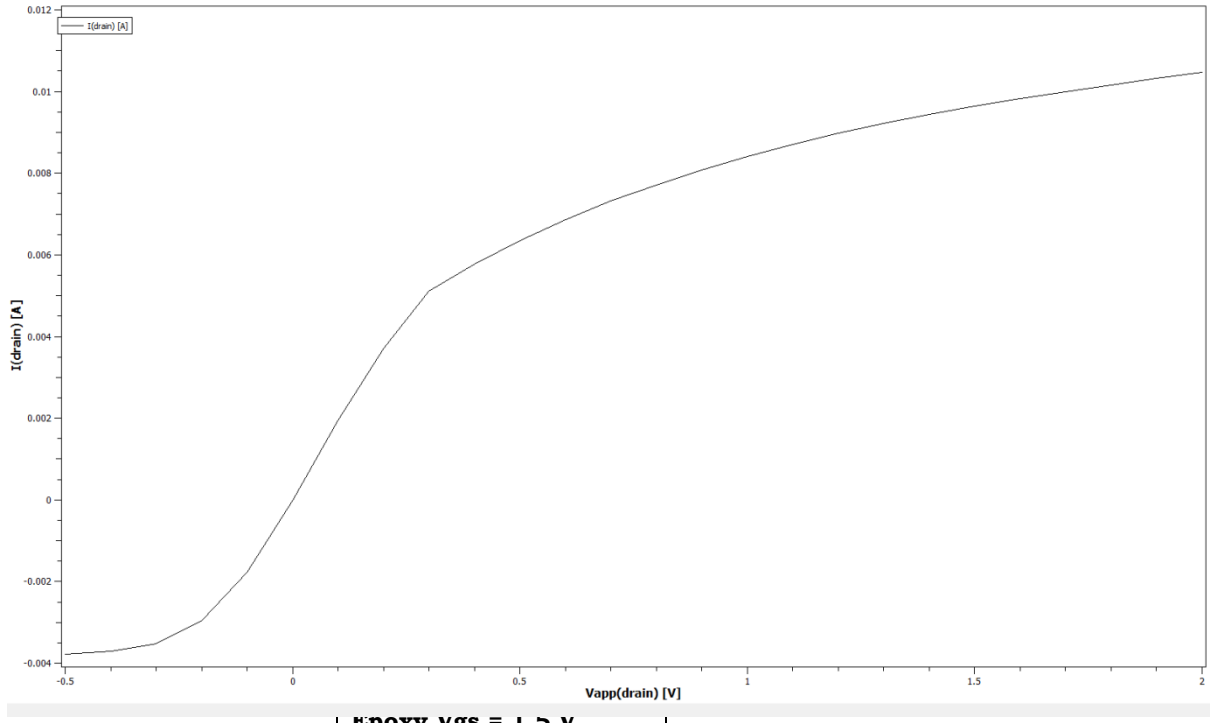


Epoxy Vgs = 0 V

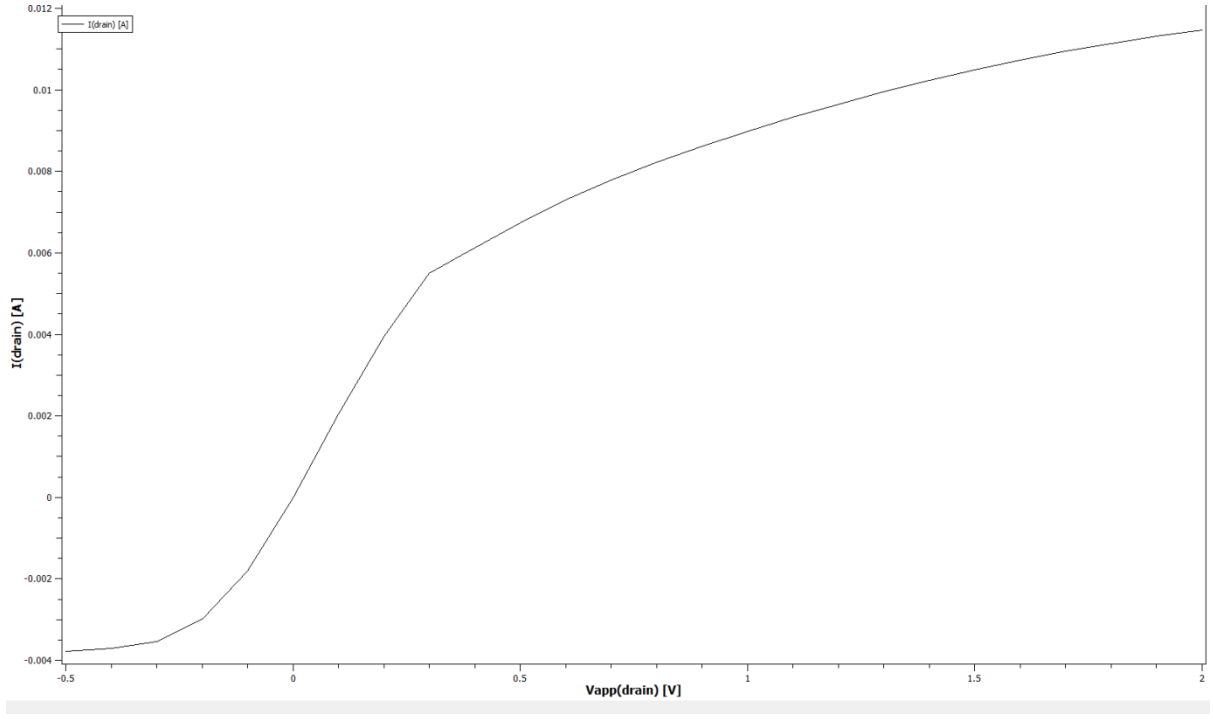


Epoxy Vgs = 0.5 V





Epoxy Vgs = 1.5 V



Epoxy Vgs = 1.5 V

6.3 Comparison between layers

- **Ion current of MOSFET for various VGS values obtained from IV characteristics**

Dielectric material	Vgs = -0.5	Vgs = 0	Vgs = 0.5	Vgs = 1	Vgs = 1.5
SiO2	0A	e-05A	5e-05A	7e-05A	0.0001A
HfO2	0.006A	0.007A	0.01A	0.013A	0.015A
Epoxy	0.007A	0.0075A	0.009A	0.011A	0.012A

- **Ion current for various thickness of Oxide layer in MOSFET**

Thickness of Oxide layer(SiO2)	Vgs = -0.5	Vgs = 0	Vgs = 0.5	Vgs = 1	Vgs = 1.5
0.001um	0A	e-0.5A	5e-0.5A	7e-0.5A	0.001A
0.002um	0.007A	0.008A	0.009A	0.01A	0.011A

- **I off current of MOSFET for various VGS values obtained from IV characteristics**

Dielectric material	Vgs = -0.5	Vgs = 0	Vgs = 0.5	Vgs = 1	Vgs = 1.5
SiO2	0.1e-06A	0.2e-05A	0.4e-05A	0.8e-05A	e-05A
HfO2	0.0005A	-0.0005A	-0.0005A	-0.001A	-0.001A
Epoxy	-0.0002A	-0.0005A	-0.0005A	-0.0006A	-0.0006A

6.4 Subthreshold Conduction :

Theoretical equation to find Id: Ion . e^(Vgs-Von).(q/nkT)

Von=V_T +KT/q

Where,

Ion= ON current,

Vgs=Gate to Source Voltage,

q/nkT=(1/0.0259)

K=Boltzman Constant,(1.38064852 X 10^-23 m^2kgs^-2k^-1)

q=Charge,(1.6 X 10^-19 c)

For sio2 Vgs=1.5 subthreshold conduction is,

Ion of sio2 for Vgs=1.5 is 0.0001A

Ion . e^(Vgs-Von).(q/nkT)

=0.0001X e^((1.5-1.4+0.0259)/0.0259)

Id=0.046A

Similarly for Hfo2 Vgs=1.5 subthreshold Conduction is,

Ion of hfo2 for Vgs=1.5 is 0.015A

Id=Ion . e^(Vgs-Von).(q/nkT)

=0.015 X e^((1.5-1.5+0.0259)/0.0259)

Id=5.518 X 10^-3

From the above calculation it is clear that subthreshold conduction is reduced for high k dielectrics since, sio2 is having 3.9 dielectric constant whereas Hfo2 have 25 so the leakage current also decreased.

7. Future Scope

High K dielectrics are used in semiconductor manufacturing processes where they are usually used to replace a silicon dioxide gate dielectric or another dielectric layer of device in order to reduce the leakage current in metal oxide layer. In this work, a simulation methodology is proposed to evaluate the nano scale variability source related to the poly crystallization of high K dielectric (i.e., Oxide thickness, tox and charge density, ρox fluctuations in small range) on the MOSFET. Meanwhile, the practical demonstration of nanoscale variability source related to high – K dielectric (i.e., charge density) was not studied in this work. According to moore's law at some point the high temperature of transistors eventually would make it impossible to create smaller transistors. From the above results it is observed by replacing high-k dielectric in fabrication , we can decrease leakage current so that rate of transistors can be increase in chip with low heat dissipation.

8. Conclusion

In this work, we proposed a simulation methodology using Cogenda visual TCAD software to verified that impact of nano scale variability of source related High -k dielectrics i.e., thickness of the MOSFET. By calculating I ON and I OFF from. IV characteristics of MOSFET. As per results for various High - K dielectrics materials of MOSFET such as SiO2, HfO2 and epoxy we justified the difference among them from {6.9.3, 6.9.4, 6.9.5} which helps to understand better about the leakage current of oxide layer in MOSFET. Finally regarding to the outputs we obtained we can say leakage current of oxide layer is reduced by replacing MOSFET oxide layer with high k dielectric and drain current is amplified with respect to the nano scale Variability of source related to the high k dielectric i.e. , tox(thickness).

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