A Multi-Mode Control Based Asymmetrical Dual-Active-Bridge Series-Resonant DC-DC Converter (DABSRC)

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Keywords

≪Bi-directional converters≫, ≪Dual-Active-Bridge (DAB) DC-DC converter≫, ≪Resonant converter≫, ≪Switching and conduction losses≫, ≪High power density systems≫.

Abstract

A multi-mode control for asymmetrical dual-active-bridge series-resonant DC-DC converter (DABSRC) based on half-bridge and full-bridge switching configurations is proposed. The proposed control is configured to eliminate burst-mode operation while supporting an efficient wide-voltage range voltage variation handling and bidirectional power-flow capabilities. Under heavy and medium load conditions, the proposed control method regulates converter's output by varying the switching frequency. When switching frequency exceeds its predetermined maximum value under light load conditions, a second control mode is employed (instead of opting for burst mode) where the switching frequency is fixed to maximum value and converter output is regulated by varying both the phase shift and duty cycle. The effectiveness of the proposed method is validated by experimental results with the peak efficiency of 98.95 % and power density of approximately 218 $\mathrm{W/in^3}$ or 13.3 kW/L (including output filter and auxiliary-power circuit).

Introduction

A control method for a bidirectional dual-active-bridge series-resonant DC-DC converter (DABSRC) involving variable input and output DC voltage sources is proposed. A typical application of such a control method could be in DABSRC based DC-DC power converter stage of an AC-DC rectifier system used in power telecom equipment and DC-AC inverter system for photovoltaic (PV) applications. Generally, for an efficient and reliable performance, the DC-DC converter stage should be able to operate efficiently under wide-range voltage variations without burst-mode operation. Over the past several years, various topological and control solutions for the DC-DC conversion stage and its control were proposed to strive for aforementioned traits. These solutions are summarized below:

- An internal phase-shift or duty-cycle variation based control methods were proposed in [1] and [2]. Both of these control methods are applicable for two inductors and one capacitor (*LLC*) based DC-DC converter topology. However, this converter topology lacks the wide-range voltages variation handling capability along with inability of enabling bi-directional power flow.
- Reference [3] proposed a control method for half-bridge and full-bridge type switching networks based dual-active-bridge (DAB) converter. The proposed method is unable to handle wide-range voltage variations efficiently, and it lacks the burst mode elimination which could lead to high-voltage stress when required power is more than the rated power.
- A conventional *LC*-type DABSRC operating with single-phase-shift (SPS) modulation was proposed in [4]. With SPS modulation, power is modulated with one degree of freedom using the external phase shift between the primary and secondary bridge voltages but this method can result in

substantial conduction and switching loss, particularly under light-load and non-unity voltage-gain conditions. An efficient control method to overcome drawbacks associated with [4] was proposed in [5] for symmetrical full-bridge type DABSRC. This method utilized two degrees of freedom i.e., using SPS modulations and frequency variations. However, both aforementioned control methods suffer from back-flow power and burst-mode is required for light-load conditions.

- The authors of [6] proposed an efficient four-degrees-of-freedom control method for symmetrical full-bridge type DABSRC. However, similar to [1]-[5], burst mode is required to achieve low power levels. Furthermore, the burst mode requirement may move up to near to the medium power levels, when the value inductor and capacitor is chosen to handle the power more than rated power (overload condition).

To overcome the associated drawbacks of prior literature, a new control method is proposed to handle the wide-range voltage variations efficiently and eliminate the burst mode to allow high power density (by opting for smaller value the inductor). The proposed control method is based on two modes: mode 1 utilizes phase-shift modulation and frequency variation typically at medium-to-high power levels, while mode 2 is employed to regulate the low power levels by making use of both duty cycle and phase shift with frequency being fixed at its maximum value. A detailed analysis, derivation, control structure and its validation are illustrated in next sections of the paper.

Analysis of the Proposed Control Method

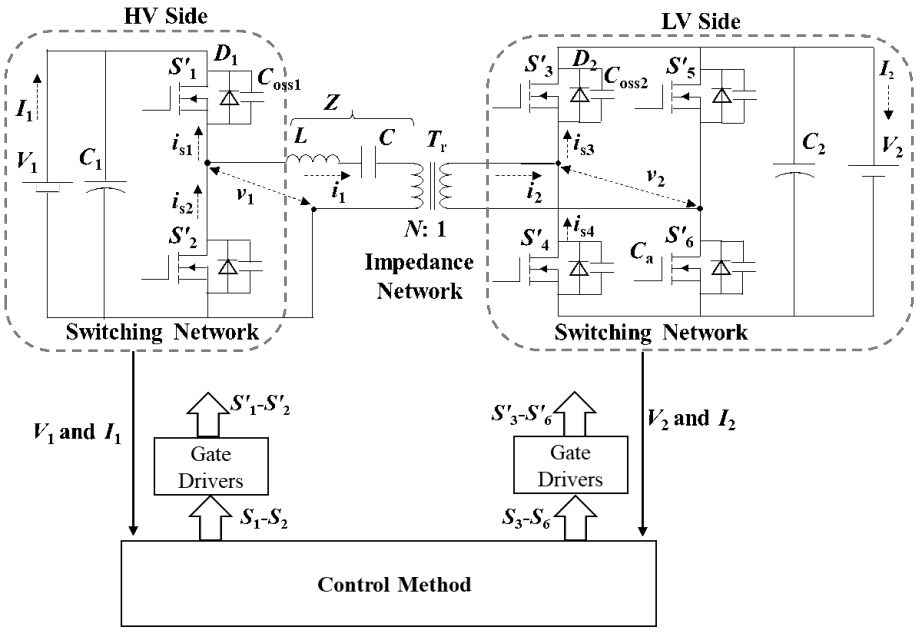
A circuit diagram of asymmetrical half-bridge and full-bridge based DABSRC and typical operating waveforms of the proposed control method are shown in Fig 1a-c. The choice of half-bridge (i.e., two switches $S_1' - S_2'$) switching network for high-voltage (HV) side and full-bridge switching network forming low-voltage (LV) side (i.e., four switches $S_3' - S_6'$) allow lower number of semiconductor switches (and hence the high-power density) compared to the most of the prior literature solutions. For the mode 1, the voltages v_1 and v_2 generates the near-sinusoidal currents i_1 and i_2 by exciting the series-resonant impedance Z. This property of currents i_1 and i_2 being near sinusoidal leads to lower current stress and reduced high-order harmonics, and hence lower conduction and core losses in transformer and inductor. The use of aforementioned switching-network configurations under mode 1 operate with near 50% ON and OFF time i.e., D=0.5 for the all semiconductor switches $S_1' - S_6'$ create a v_1 with the levels of 0 and $+V_1$ and v_2 with the levels of $-V_2$ and $+V_2$. As for the mode 2, the switching network at the HV operates with D <0.5 and the currents i_1 and i_2 opt to be piece-wise linear. Due the presence of capacitor C in series with inductor L and transformer T_r, (i.e., the choice of series-resonant impedance Z) gives inherent DC-bias removal generated by HV-side switching network. Both Mode 1 and Mode 2 operations are further explained below:

- **Mode 1:** By considering the power flow from HV→LV and fundamental component analysis, the average power and current at LV side can be calculated using the HV or LV bridge voltage (i.e., $v_1(t)$ or $v_1(t)$) and tank current $i_1(t)$ or $i_2(t)$; both approaches lead to the same expressions given by (1) and (2) [4].

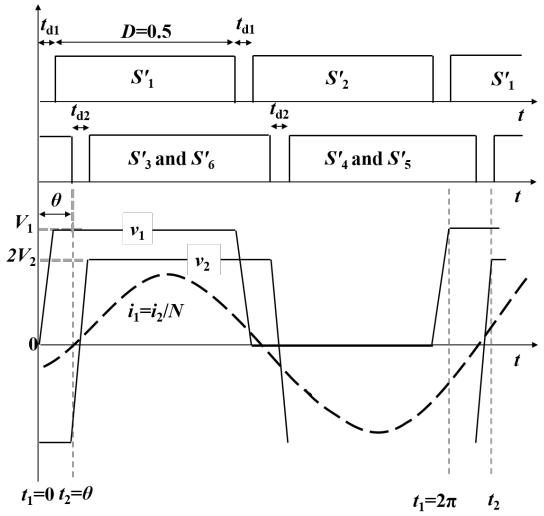
$$\begin{aligned} P_{o,2} &= \frac{1}{2\pi}\int_0^{2\pi} v_1(t) i_1(t) dt \\ &= \frac{4NV_1V_2\sin\theta}{\pi^2 Z} = \frac{2MV_1^2\sin\theta}{\pi^2 Z} \end{aligned} \tag{1}$$

$$I_2 = \frac{4NV_1\sin\theta}{\pi^2 Z} \tag{2}$$

where N is transformer T_r turn ratio and $-\pi/2 \leq \theta \leq +\pi/2$ is the phase shift between v_1 and v_2 determining the direction and the magnitude of the power/current flow between HV and LV sides. The positive value of $+\theta$ depicts the power/current from HV→LV side while negative value of $-\theta$ leads to the power/current flow from LV→HV side. Furthermore, voltage gain M (across



(a)



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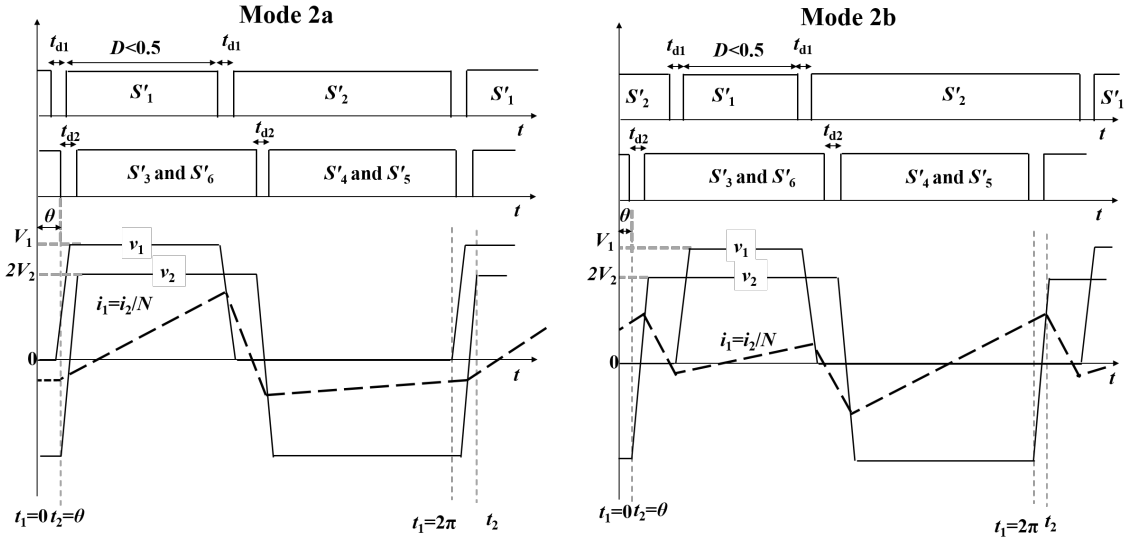


(c)

Fig. 1: (a) Circuit diagram of the half-bridge and full-bridge switching networks based DABSRC, (b) key operating waveforms under mode 1, and (c) key operating waveforms under mode 2 for the power flow from HV→LV side.

impedance Z) and impedance Z are given by (3) and (4) with f_s as switching frequency,

$$M = \frac{NV_2}{0.5V_1}, \tag{3}$$

$$Z = 2\pi f_s L - \frac{1}{2\pi f_s C}. \tag{4}$$

The conduction loss in DABSRC is mainly dependent on rms values of $i_1 = i_2/N$ which is given by (5),

$$I_{1,\text{rms}} = \frac{\pi I_2}{4N\sin\theta} \times \sqrt{2M^2 - 4M\cos\theta + 2}. \tag{5}$$

In order to find the minimum rms current $I_{1,\text{rms,min}}$ through Z for the given value of I_2, the first derivative of $I_{1,\text{rms}}/I_2$ with respect to phase shift θ should be kept zero and solve it for the required values of phase shift θ. The final result is presented as (6)[6],

$$\frac{\partial}{\partial\theta}\left(\frac{I_{1,\text{rms}}}{I_2}\right) = 0 \Rightarrow \theta = \begin{cases} \cos^{-1}(M) & \text{for} \quad M \leq 1 \\ \cos^{-1}(1/M) & \text{for} \quad M > 1 \end{cases} \tag{6}$$

Substituting (6) into (5) leads to the relationship of $I_{1,\text{rms,min}}$ and I_2 which is given by (7),

$$I_{1,\text{rms,min}} = \frac{I_{2,\text{rms,min}}}{N} = \begin{cases} \frac{\pi\times\sqrt{2}}{4N} I_2 & \text{for} \quad M \leq 1 \\ \frac{\pi M\times\sqrt{2}}{4N} I_2 & \text{for} \quad M > 1 \end{cases} \tag{7}$$

From (7), it can be seen that for the $M > 1$, the current increases proportionally to an increase in M. Hence, by choosing the value of N using (3) to keep $M \leq 1$ would be an appropriate design decision. Furthermore, by substituting (6) into (2), I_2 can be rewritten as (8),

$$I_2 = \begin{cases} \frac{4NV_1\sqrt{1-M^2}}{\pi^2 Z} & \text{for} \quad M \leq 1 \\ \frac{4NV_1\sqrt{1-\frac{1}{M^2}}}{\pi^2 Z} & \text{for} \quad M > 1 \end{cases} \tag{8}$$

At M =1, from (6) phase shift θ=0 and from (8) output current I_2=0. To avoid such situation, there is a need to limit the values of M around 1 i.e., $M < 1$. Equation (6) is plotted in Fig 2 for $M < 1$ along with the maximum limit of M i.e., M_{max}, and therefore, the minimum phase-shift θ_{min} at M_{max} can be given as (9):

$$\theta_{\text{min}} = \cos^{-1}(M). \tag{9}$$

Equations (6) and (9) can be written together as (10) and plotted in Fig 2.

$$\theta = \cos^{-1}(M) \quad \text{for} \quad M \leq M_{\text{max1}} \tag{10}$$

The zero-voltage-switching (ZVS) operation at the HV-side switches $S_1' - S_2'$ depends on the minimum value of phase shift θ_{min} (or inductor current i_1 within dead time t_{d1}) which consequently depends on the choice of M_{max} given by (11),

$$M_{\text{max}} = \frac{\sqrt{(\pi I_{2,\text{min,zvs}} t_{\text{d1}})^2 - (4NQ_{1,\text{max}})^2}}{\pi I_{2,\text{min,zvs}} t_{\text{d1}}} \tag{11}$$

where $I_{2,\text{min,zvs}}$ is the minimum output current at LV side above which ZVS at HV is guaranteed

and below this value the ZVS at HV side is not possible, t_{d1} is the dead time between $S'_1 - S'_2$, and $Q_{1,\max}$ = max of ($V_1 C_{oss1}$) is the maximum charge stored on S'_1 with C_{oss1} as the parasitic output capacitance of the HV-side switches. The ZVS operation for the LV-side switches $S'_3 - S'_6$ is always guaranteed following (10) under mode 1 [5].

From (8), it can be seen that to change the I_2, Z (or f_s from (4)) can be varied because θ is already bounded by M i.e., variations in input and output voltages. Hence, the minimum required impedance $Z_{\min}$ to deliver given maximum $I_{2,\max}$ can be calculated for $M_{\max}$ and $V_{1,\min}$ and the result can be given by (12),

$$Z_{\min} = \frac{4NV_{1,\min}\sqrt{1-M_{\max}^2}}{\pi^2 I_{2,\max}} = 2\pi f_{s,\min} L - \frac{1}{2\pi f_{s,\min} C}, \tag{12}$$

where $V_{1,\min}$, $f_{s,\min}$ are the given minimum input voltage and frequency. Furthermore, the given resonance frequency $f_r < f_s$ (to behave inductive) of the impedance Z can be given by (13),

$$f_r = \frac{1}{2\pi\sqrt{LC}}. \tag{13}$$

Equations (12) and (13) can be solved simultaneously to determine the values of L and C to form the impedance Z.

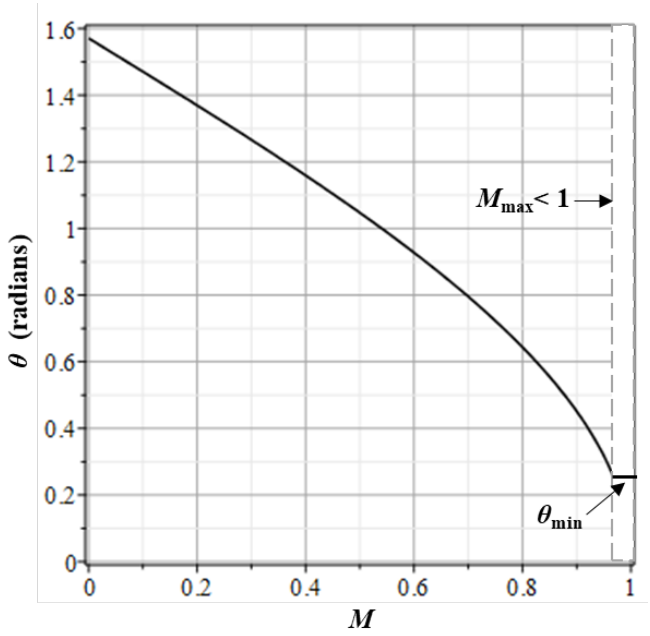


Fig. 2: Variation of voltage gain M vs. phase shift θ to achieve minimum rms current and ZVS operation at HV and LV sides.

- **Mode 2:** From (2) and (4), it can be seen that at $f_{s,\min}$, the I_2 is of maximum value and at the $f_{s,\max}$ (user defined based on hardware specifications) the I_2 would be of minimum value. In order to achieve the value of I_2 further lower than what $f_{s,\max}$ can provide, it is a normal practice to opt for burst mode where all of the switching devices are periodically turned ON and OFF. However, when the M (i.e., input and output voltages) is varied under the wide-range, converter is pushed to deliver power more than its rated power and inductor is required to be reduced for increased power density, the start of burst mode is shifted from lower-to-medium values of I_2. Under this specific operation where burst mode starts at higher values of I_2, the reliability of the switching devices decrease and could lead to converter's failure. Hence, it is desired to eliminate the burst mode, and from mode 1 it is proposed to go to mode 2 (instead of starting burst-mode) after reaching $f_{s,\max}$. Mode 2 is initiated when $f_s = f_{s,\max}$, and instead of varying f_s to reduce I_2, duty-cycle at HV-side

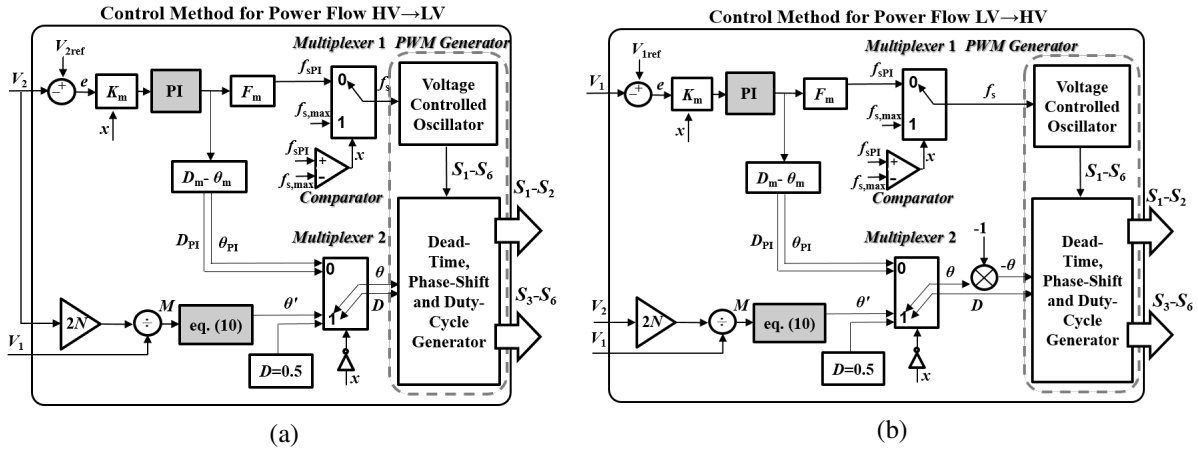
is reduced from 0.5 i.e., D <0.5 and the remaining value of θ is reduced to modulate I_2 by stop following (10). By varying both D and θ, the currents waveforms i_1 and i_2 become piece-wise linear leading to two sub-modes i.e., mode 2a and mode 2b depicted in Fig 1c. For the power flow of HV→LV side i.e., +θ, mode 2a appear when the rising edge of the v_1 is leading the rising edge of v_2, while mode 2b starts when rising edge of v_2 is leading the v_1 (c.f., Fig 1c). As for the power flow of LV→HV side i.e., –θ, rising edge of v_2 leads v_1 for the mode 2a, vice versa. In this mode 2, minimum rms current operation cannot be maintained due to not following (10). As for ZVS operation, it remains same for HV-side switches (as in mode 1) with $M \leq M_{\max}$. For the LV-side switches, under the mode 2a, the two switches undergo hard-switching while for mode 2b, all switches at LV undergo ZVS operation. This aforementioned mode 2 of varying D and θ generally occurs at the medium-to-lower (depending on M) values of the I_2, and hence it doesn't have a big impact on the converter's overall performance.

- **Overall Control Structure:** Fig 3a-b, represents an overall control implementation of aforementioned modes of operations. It can be seen from Figure 3a, that for the power flow from HV→LV, a desired reference voltage $V_{2\text{ref}}$ is compared with sensed voltage V_2, and the resulting error e is fed to the proportional-integral (PI) controller. Two multiplexers and a comparator are used to choose between two modes of operations. The output value of PI is passed to frequency (F_{m}) and duty-cycle and phase-shift (D_{m}-θ_{m}) modulators. For the mode 1 (i.e., when x=0 is given by the comparator), the value of PI is converted into frequency by F_{m} i.e., f_{s}= $f_{\text{s,PI}}$ to control and achieve the desired value of voltage V_2, while phase shift θ′= θ from (10), and D=0.5 is used to maintain minimum rms current and ZVS operations. When f_{s} hits the maximum allowed limit with f_{s}= $f_{\text{s,max}}$ i.e., mode 2, PI value is converted into duty-cycle and phase-shift by D_{m}-θ_{m} modulator, which is then used to control θ =θ_{PI} and D=D_{PI} (i.e., when x=1 is given by the comparator) to deliver the remaining power flow with frequency limited to f_{s}= $f_{\text{s,max}}$. Furthermore, the PI gain K_{m} is changed based on the x i.e., based on mode of operation. The value of the K_{m} is dependent the converter's model and behavior in response to the variations in f_{s}, θ and D. Control parameters f_{s}, θ and D are fed to the PWM generator which comprises of a voltage-controlled oscillator, dead-time, phase-shift and duty-cycle generator. For the case, where power flows from LV→HV (c.f., Fig 3b), $V_{1\text{ref}}$ is compared to the sensed value of V_1 to generate the error e. The rest of the control method behave similarly as in the case of HV→LV power flow, except that the output θ of the multiplexer 2 is multiplied with -1 to generate a negative phase shift -θ (i.e., LV side voltage v_2 is leading the HV side v_1). Fig 3 is shown to explain the control at block levels and the aforementioned control method can be implemented using both analog and digital (using microcontroller unit (MCU)) approaches.

Experimental Results

In order to validate the proposed control method, a hardware prototype with specifications given in Table I is built to imitate bidirectional DC-DC converter with maximum power flow of 3 kW (4 kW in overload conditions) for voltage sources of V_1 (380-430 V) and V_2 (42-58 V). The waveforms for a case of power from $V_2 \rightarrow V_1$ i.e., LV→HV are depicted in Fig 4a-c. The optimal combinations of the control parameters are used according to Fig 3a-b with objectives of power transfer with high efficiency, burst-mode elimination and high-power density.

Furthermore, the measured efficiency curves of the converter's operation for the power flow of HV→LV under various voltage variations are depicted in Fig 5a with a peak efficiency of 98.95% (including output filter and auxiliary power supply). Relatively, lower efficiency values were observed for maximum input voltage $V_{1,\max} = 430\text{V}$ and minimum output voltage $V_{2,\min} = 42\text{V}$, representing the case of $M = 0.68$. This can be explained by observing Fig 2 showing higher values of θ for lower M, which consequently leads to higher switching (due to high current turn-off at HV-side MOSFETs) and conduction losses (due to circulating current at HV-side). Fig 5b represents the comparison of measured efficiency values for the power flow from both HV→LV and LV→HV. The difference in efficiencies at light load is due to the different values of D and θ provided by PI in mode 2 operation.

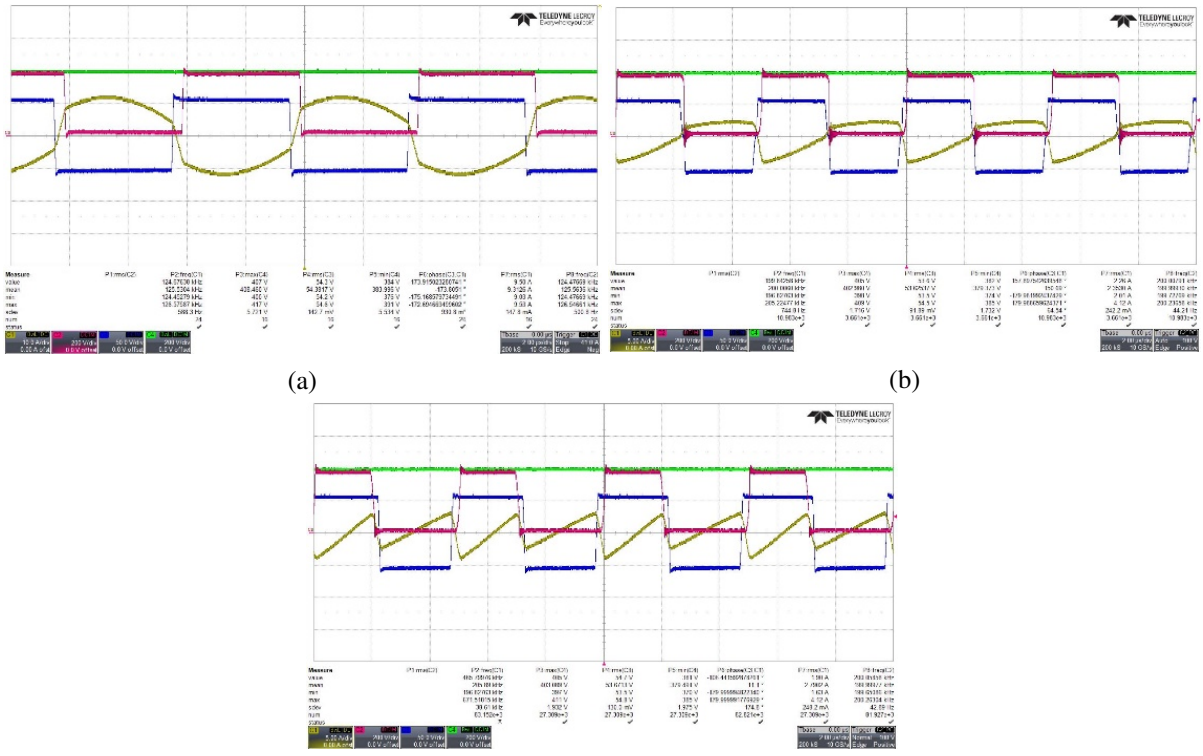


(a) (b)

Fig. 3: Proposed control methods, (a) for the power flow from HV→LV, and (b) for the power flow from LV→HV.

Table I: Specifications of the Converter Prototype

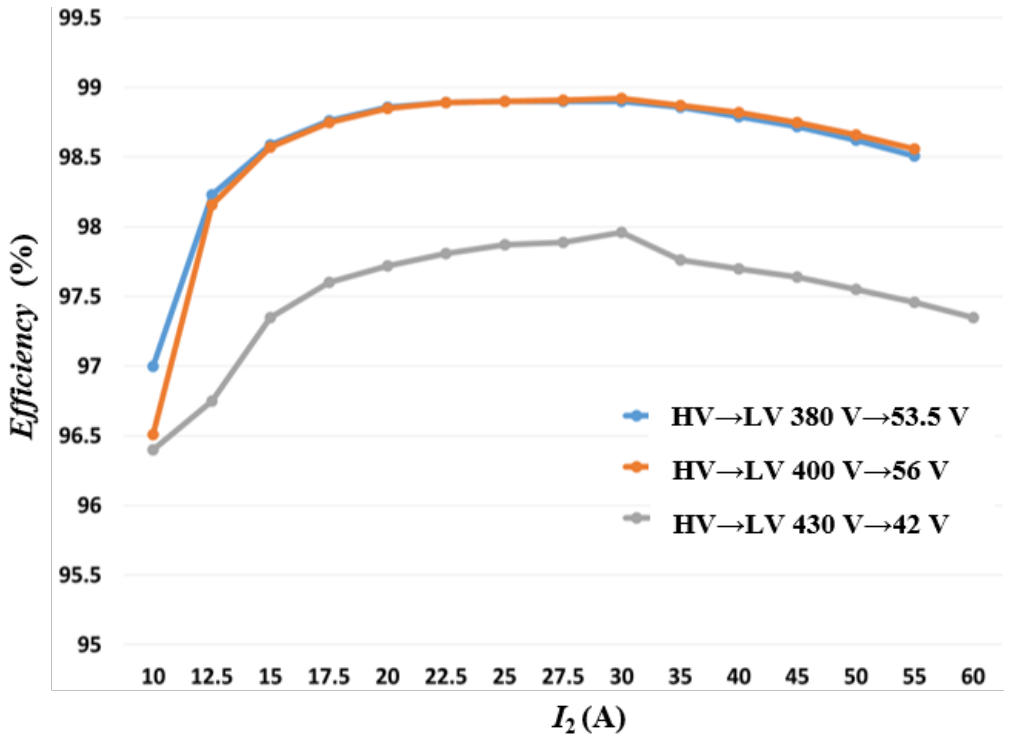
Input Voltage Range V_i	380-430 V
Output Voltage Range V_o	42-58 V
Variation in Switching Frequency f_s	100-220 kHz
Maximum Rated Output Power P_o	3 kW
Primary Side MOSFETs	GaN
Secondary Side MOSFETs	Si
Control Implementation	Digital using STM32G4 MCU



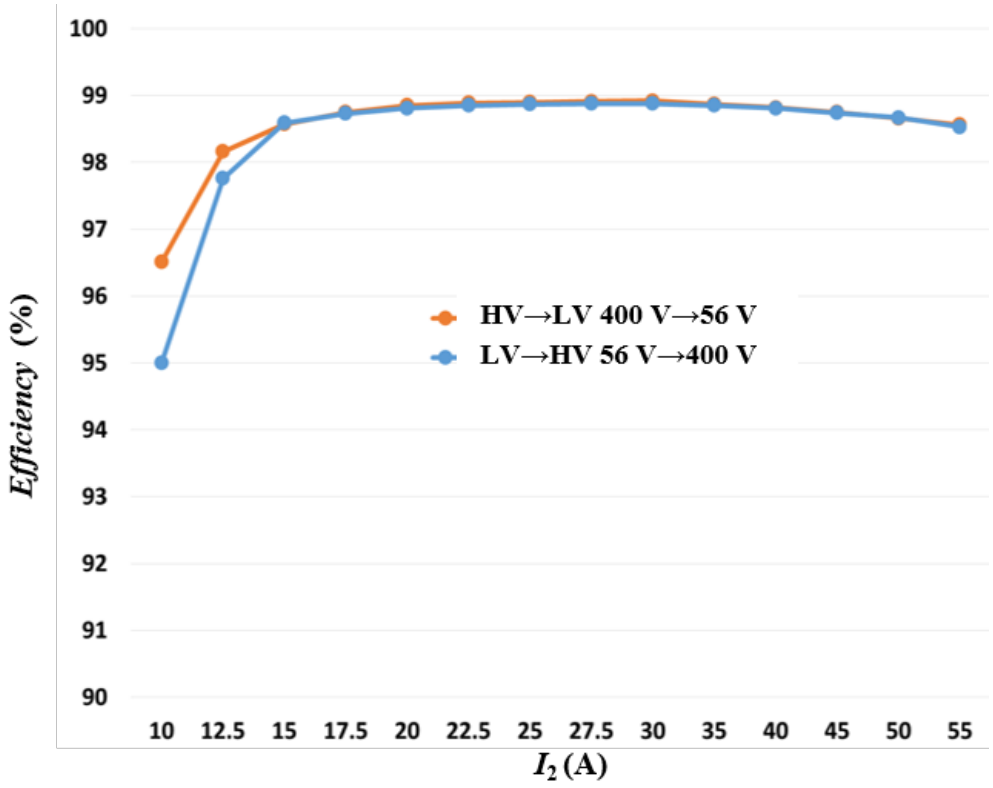
(a) (b)

(c)

Fig. 4: Power transfer from LV→HV with V_1 = 380 V and V_2 = 54 V, with green V_1, pink v_1, blue v_2 and yellow i_1 (a) mode 1 with frequency variation, (b) mode 2a, and (c) mode 2b with phase-shift θ and duty-cycle D variations when frequency hits the maximum allowed limit of $f_{s,max}$.



(a)



(b)

Fig. 5: Measured efficiency, (a) for various input and output voltage levels with power flow from HV→LV, (b) comparing both power flows i.e., HV→LV and LV→HV at typical operating point.

Conclusion

A control method is proposed for an asymmetrical half-bridge (HV-side) and full-bridge (LV-side) switching networks based DABSRC to address the drawbacks of the past literature. The proposed method opts for two modes of operation. The first mode uses the frequency variation to control the power flow while soft-switching and minimum rms current operations are achieved by varying phase shift. The second mode starts when the pre-assigned maximum value of frequency is achieved and the converter utilizes the HV-side's duty cycle and phase shift (between HV and LV sides) to control the power. The aforementioned modes of operations allows burst-mode elimination along with efficient wide-range voltage handling and high-power density capabilities.

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