

# Neutral-Point Voltage Regulation of Three-Level Neutral-Point Clamped Converter for LVDC Power Distribution Application

Mina Kim<sup>1</sup>, Hwa-Pyeong Park<sup>2</sup>, Seung-Yeol Oh<sup>1</sup>, Daeseak Cha<sup>1</sup>,  
Byoung-Sun Ko<sup>1</sup>, and Jung-Sik Choi<sup>1</sup>

<sup>1</sup> Intelligent LVDC Demonstration Group, Korea Electronics Technology Institute, South Korea

<sup>2</sup> School of Electronics Engineering, Kumoh National Institute of Technology, South Korea

**Abstract--** A three-level neutral clamp (NPC) converter is a promising candidate for constructing a low-voltage DC (LVDC) power distribution system with a bipolar DC bus structure since it can provide a unipolar high-voltage DC output and bipolar low-voltage DC outputs. However, it has a severe neutral-point (NP) voltage imbalance with the load deviation between the bipolar low-voltage DC outputs. This paper proposes a neutral-point (NP) voltage regulation method for the three-level NPC converter in the LVDC power distribution system application. The proposed method injects DC and AC signals into the PWM reference to mitigate both AC and DC components of the NP voltage error. Therefore, the three-level NPC converter can improve the power quality of the low voltage DC outputs under the load unbalance condition. The proposed method has been verified using a 400-kW three-phase three-level NPC converter prototype.

**Index Terms—**LVDC Power Distribution System, Multi-Output Converter, Neutral-Point Voltage Balancing, Three Level Neutral-Point Clamped Converter.

## I. INTRODUCTION

Fig. 1 shows a LVDC power distribution system with a bipolar DC-bus voltage structure [1]-[3]. The bipolar DC-bus configuration can improve the overall power distribution efficiency since it can reduce the input-to-output-voltage conversion ratio. Besides, as it can continuously deliver the power to the load under fault conditions, the LVDC power distribution system can achieve high reliability. Fig. 2 shows a three-phase three-level neutral-point clamped (NPC) converter that can interface the bipolar LVDC power distribution system with the conventional AC grid. It can mitigate the total harmonic distortion (THD) of the AC current and reduce the voltage stress applied to the power switches [4]-[5]. Besides, as described in Fig. 2, the three-level NPC converter can provide a unipolar DC output ( $V_{PN}$ ) and bipolar DC outputs ( $V_P$ ,  $V_N$ ). However, the three-level NPC converter suffers from a neutral-point (NP) voltage deviation, which becomes severe when the load is imbalanced at each bipolar DC output. Therefore, since the load power of the bipolar DC outputs cannot be perfectly balanced in the bipolar LVDC power distribution system, the three-level NPC converter requires an output voltage control algorithm to balance the NP voltage and

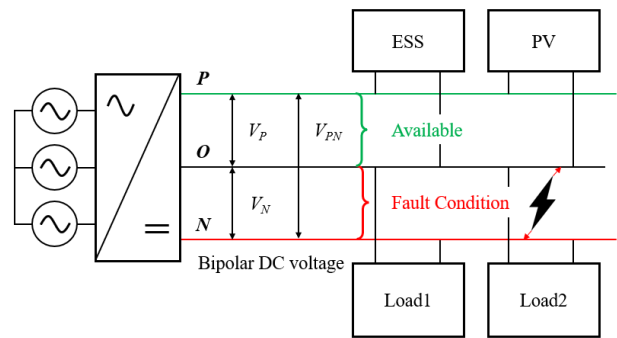


Fig. 1. LVDC power distribution system with bipolar DC-bus structure.

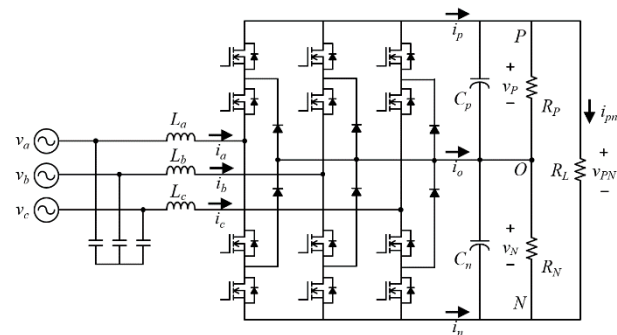


Fig. 2. Three-phase three-level NPC converter for LVDC power distribution applications.

bipolar DC outputs.

Previously, there are many NP voltage regulation algorithms for three-level NPC converters. In [6]-[7], NP voltage regulation methods using a discontinuous PWM (DPWM) modulation have been introduced. It can suppress the bipolar DC output voltage imbalance, however, the DPWM modulation induces high audible noise from the converter, which degrades the usability of the converters. In [8]-[9], NP voltage regulation methods using a space vector PWM (SVPWM) have been introduced. They select the current operating vector by sensing the current state and values of the converter, therefore, their reliability according to the sensing accuracy and noise becomes lower. In [10]-[11], power stage model-based NP voltage controllers have been introduced. However, the performance of the power stage model-based approach is strongly dependent on the

tolerance of the hardware. In [12]-[13], NP voltage regulation methods using an offset injection strategy have been introduced. It can suppress the NP voltage imbalance by prospering injecting the offset signal to the PWM reference. However, the offset calculation is divided into many different equations according to the operating conditions and requires high computation resources. Besides, the previous NP voltage balancing methods cannot consider the NP voltage imbalance due to the load deviation between the bipolar outputs.

This paper proposes a neutral-point (NP) voltage regulation method of the three-level NPC converter for the bipolar LVDC power distribution system application. The proposed NP voltage regulation method injects AC and DC signals into the PWM reference using separate computation algorithms to compensate for the AC and DC NP voltage deviation, respectively. Therefore, the three-level NPC converter can not only operate with imbalanced load power at each bipolar output but also can further suppress the current THD at the AC side and improve the power quality of the bipolar output voltage. The NP voltage stabilization performance of the proposed NP voltage regulation algorithm has been verified using a 400-kW three-level NPC converter prototype. The NP voltage deviation has been suppressed by 41.22% using the proposed algorithm.

## II. THEORETICAL ANALYSIS OF NP VOLTAGE DEVIATION

To obtain the numerical expression of the bipolar DC output voltage, the positive and negative phase currents ( $i_p$ ,  $i_n$ ) and the load current can be derived as follows:

$$i_p = \frac{1}{2} [|D_a| i_a + |D_b| i_b + |D_c| i_c] + I_{Rp} \quad (1)$$

$$i_n = -\frac{1}{2} [|D_a| i_a + |D_b| i_b + |D_c| i_c] + I_{Rn} \quad (2)$$

where  $D_a$ ,  $D_b$ , and  $D_c$  are the three-phase PWM references,  $I_a$ ,  $I_b$ , and  $I_c$  are the three-phase AC current, and  $I_{Rp}$  and  $I_{Rn}$  are the bipolar output current, respectively. Using (1)-(2), the current flows into the bipolar output capacitors ( $i_{cp}$ ,  $i_{cn}$ ) can be obtained as follows:

$$i_{Cx} = (i_x - I_{Rx}) \left| \frac{R_x}{Z_{Cx} + R_x} \right| \quad (3)$$

where  $x$  denotes the pole (positive pole:  $p$ , negative pole:  $n$ ),  $Z_{Cx}$  is the impedance of the bipolar output capacitors. Finally, the bipolar DC output voltage ( $v_p$ ,  $v_n$ ) can be obtained as follows:

$$v_p = \frac{1}{C_p} \int i_{cp} dt + V_p, \quad v_n = \frac{1}{C_n} \int i_{cn} dt + V_n \quad (4)$$

$$V_p = V_{PN} \frac{R_L || R_P}{R_L || R_P + R_L || R_N}, \quad V_n = V_{PN} \frac{R_L || R_N}{R_L || R_P + R_L || R_N} \quad (5)$$

Fig. 3 shows the bipolar DC output voltage according to the different operating conditions of the three-level NPC converter. The bipolar DC output voltage difference consists of AC and DC harmonics. The AC harmonic has a constant frequency as  $3f_{grid}$ , and the amplitude and phase vary according to the power factor. Besides, The DC harmonic is proportional to the load deviation between the bipolar DC outputs. Specifically, the imbalanced load power at the bipolar DC outputs can frequently happen in the LVDC power distribution system, which induces the NP voltage imbalance and degrades the output voltage

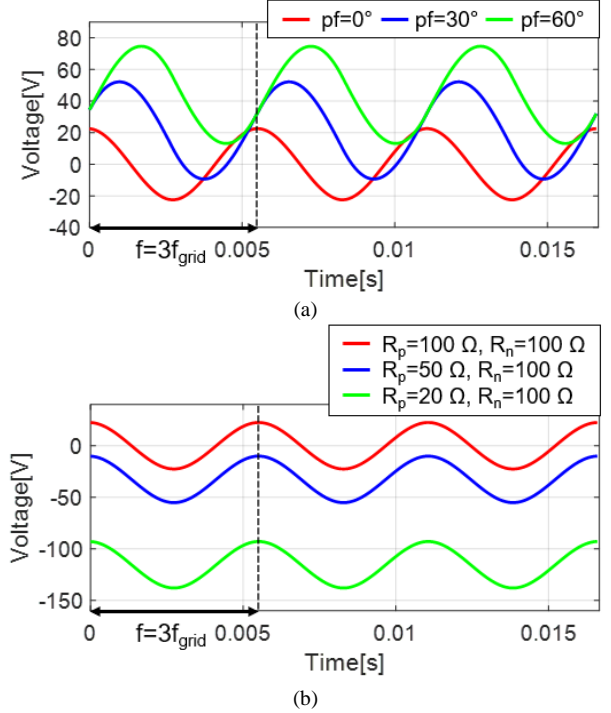


Fig. 3. Bipolar DC output voltage according to the different operating conditions: (a) Different power factor condition, (b) Load deviation condition.

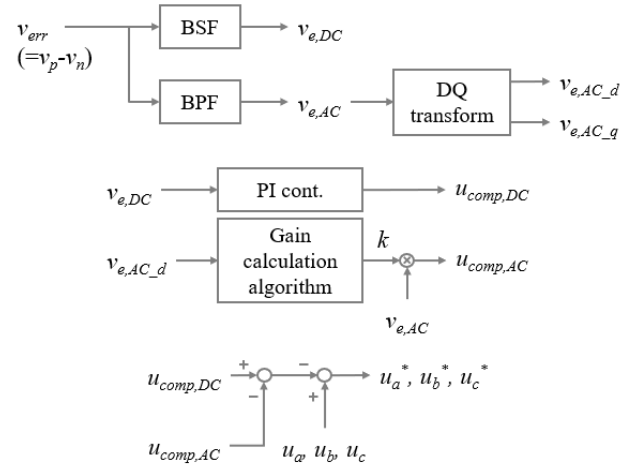


Fig. 4. Proposed NP voltage regulation method.

quality of the converter. Consequently, the NP voltage regulation method, which can suppress both AC and DC harmonics, is demanded for the three-level NPC converter for the LVDC power distribution system applications.

## III. NP VOLTAGE REGULATION STRATEGY

Fig. 4 shows the proposed NP voltage regulation method to suppress both AC and DC NP imbalance. The proposed method divides the NP voltage imbalance as AC and DC harmonics by introducing a band stop filter (BSF) and a band pass filter (BPF) with band frequency as  $3f_{grid}$ . Besides, an additional DQ transform for the AC harmonic is introduced to obtain the amplitude of the AC harmonic. The AC harmonic control using the amplitude value can improve the controllability of the AC harmonic. Besides, it can also suppress the AC harmonic with different phases

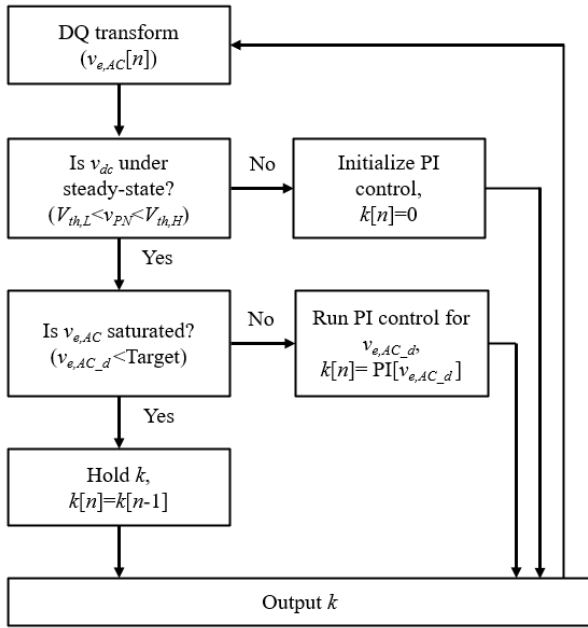


Fig. 5. Gain calculation algorithm for AC harmonic reduction.

due to various power factor conditions of the converter, as shown in Fig. 2. The DC harmonic controlled by the PI controller is added to the PWM reference to mitigate the DC harmonic to zero. On the other hand, the AC harmonic multiplied by the proper gain ( $k$ ) is added to the PWM reference to suppress the AC harmonic to zero.

Fig. 5 shows the gain calculation algorithm for the AC harmonic reduction. It distinguishes the steady state by the unipolar output voltage and the threshold values. Under the steady state, the gain calculation algorithm runs the PI control to minimize the amplitude of the AC harmonic. As the amplitude of the AC harmonic becomes lower than the target value, the gain calculation algorithm holds the previous value to avoid an unstable condition [12].

#### IV. EXPERIMENTAL RESULTS

In this section, a 400-kW three-level NPC converter has been tested to verify the NP voltage regulation capability of the proposed method. Fig. 6 shows the experimental results of the three-level NPC converter. It is noticed that the load power of the bipolar output is the same for these experimental results. However, due to the different hardware tolerance, such as output capacitors, PCB layout, and PWM latency, the 400-kW three-level NPC converter cannot operate without the DC harmonic regulation method. Therefore, the NP voltage imbalance using the DC harmonic regulation and the proposed method has been compared. Using the DC harmonic regulation, the NP voltage imbalance ( $v_p-v_n$ ) is 12.59 V. On the other hand, using the proposed method that suppresses both AC and DC harmonic, the NP voltage imbalance is 7.4 V. Therefore, the proposed method can successfully operate the three-level NPC converter with reasonable hardware tolerance and suppress the NP voltage imbalance to 41.22% without any additional circuit components and sensors.

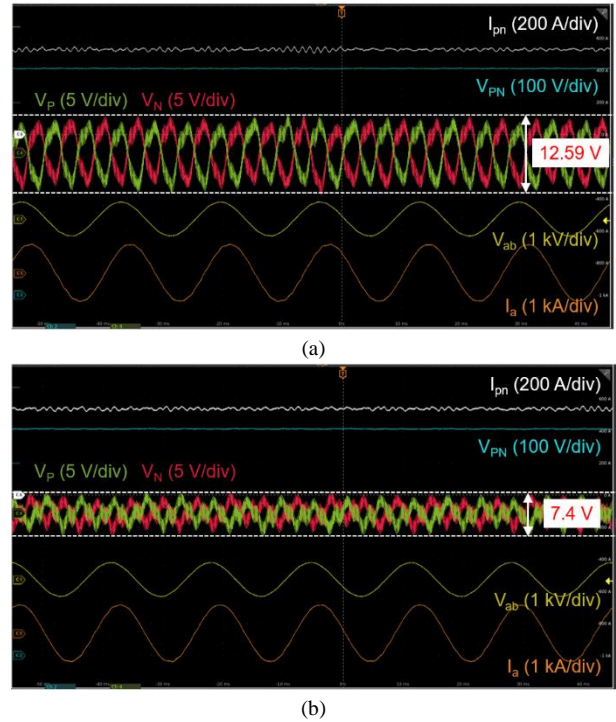


Fig. 6. Experimental results of three-level NPC converter: (a) Using DC harmonic reduction, (b) Using proposed method.

#### V. CONCLUSIONS

This paper has proposed the NP voltage regulation method to suppress the NP voltage imbalance of the three-level NPC converter under load deviation conditions for LVDC power distribution system applications. Using the proposed method, the three-level NPC converter can suppress the NP voltage imbalance to 41.22% under the balanced load between the bipolar outputs.

#### ACKNOWLEDGMENT

This work was supported by the Korea Institute of Energy Technology Evaluation and Planning (KETEP) and the Ministry of Trade, Industry & Energy (MOTIE) of the Republic of Korea (No. 20193810100010).

#### REFERENCES

- [1] T. Jung, G. Gwon, C. Kim, J. Han, Y. Oh and C. Noh, "Voltage Regulation Method for Voltage Drop Compensation and Unbalance Reduction in Bipolar Low-Voltage DC Distribution System," in *IEEE Transactions on Power Delivery*, vol. 33, no. 1, pp. 141-149, Feb. 2018, doi: 10.1109/TPWRD.2017.2694836.
- [2] K. Kim and H. Cha, "Dual-Active-Half-Bridge Converter With Output Voltage Balancing Scheme for Bipolar DC Distribution System," in *IEEE Transactions on Industrial Electronics*, vol. 69, no. 7, pp. 6850-6858, July 2022, doi: 10.1109/TIE.2021.3099233.
- [3] H. Kakigano, Y. Miura and T. Ise, "Low-Voltage Bipolar-Type DC Microgrid for Super High Quality Distribution," in *IEEE Transactions on Power Electronics*, vol. 25, no. 12, pp. 3066-3075, Dec. 2010, doi: 10.1109/TPEL.2010.2077682.
- [4] Dongsheng Zhou and D. G. Rouaud, "Experimental comparisons of space vector neutral point balancing strategies for three-level topology," in *IEEE Transactions on Power Electronics*, vol. 16, no. 6, pp. 872-879, Nov. 2001, doi: 10.1109/63.974387.
- [5] W. -. Oh, S. -. Han, S. -. Choi and G. -. Moon, "Three Phase Three-Level PWM Switched Voltage Source Inverter With Zero Neutral

- Point Potential," in *IEEE Transactions on Power Electronics*, vol. 21, no. 5, pp. 1320-1327, Sept. 2006, doi: 10.1109/TPEL.2006.880300.
- [6] I. M. Alsofyani and K. -B. Lee, "Simple Capacitor Voltage Balancing for Three-Level NPC Inverter Using Discontinuous PWM Method With Hysteresis Neutral-Point Error Band," in *IEEE Transactions on Power Electronics*, vol. 36, no. 11, pp. 12490-12503, Nov. 2021, doi: 10.1109/TPEL.2021.3074957.
  - [7] S. Mukherjee, S. K. Giri and S. Banerjee, "A Flexible Discontinuous Modulation Scheme With Hybrid Capacitor Voltage Balancing Strategy for Three-Level NPC Traction Inverter," in *IEEE Transactions on Industrial Electronics*, vol. 66, no. 5, pp. 3333-3343, May 2019, doi: 10.1109/TIE.2018.2851967.
  - [8] C. -Q. Xiang, C. Shu, D. Han, B. -K. Mao, X. Wu and T. -J. Yu, "Improved Virtual Space Vector Modulation for Three-Level Neutral-Point-Clamped Converter With Feedback of Neutral-Point Voltage," in *IEEE Transactions on Power Electronics*, vol. 33, no. 6, pp. 5452-5464, June 2018, doi: 10.1109/TPEL.2017.2737030.
  - [9] X. Xing, X. Li, F. Gao, C. Qin and C. Zhang, "Improved Space Vector Modulation Technique for Neutral-Point Voltage Oscillation and Common-Mode Voltage Reduction in Three-Level Inverter," in *IEEE Transactions on Power Electronics*, vol. 34, no. 9, pp. 8697-8714, Sept. 2019, doi: 10.1109/TPEL.2018.2886378.
  - [10] Y. Yang et al., "Improved Model Predictive Current Control for Three-Phase Three-Level Converters With Neutral-Point Voltage Ripple and Common Mode Voltage Reduction," in *IEEE Transactions on Energy Conversion*, vol. 36, no. 4, pp. 3053-3062, Dec. 2021, doi: 10.1109/TEC.2021.3073256.
  - [11] R. Maheshwari, S. Munk-Nielsen and S. Busquets-Monge, "Design of Neutral-Point Voltage Controller of a Three-Level NPC Inverter With Small DC-Link Capacitors," in *IEEE Transactions on Industrial Electronics*, vol. 60, no. 5, pp. 1861-1871, May 2013, doi: 10.1109/TIE.2012.2202352.
  - [12] J. Lyu, W. Hu, F. Wu, K. Yao and J. Wu, "Variable Modulation Offset SPWM Control to Balance the Neutral-Point Voltage for Three-Level Inverters," in *IEEE Transactions on Power Electronics*, vol. 30, no. 12, pp. 7181-7192, Dec. 2015, doi: 10.1109/TPEL.2015.2392106.
  - [13] J. -S. Lee and K. -B. Lee, "Time-Offset Injection Method for Neutral-Point AC Ripple Voltage Reduction in a Three-Level Inverter," in *IEEE Transactions on Power Electronics*, vol. 31, no. 3, pp. 1931-1941, March 2016, doi: 10.1109/TPEL.2015.2439689.