High reliable transformer-less deadtime less Inverter for Grid-connected Applications

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***Abstract*-- This paper presents a transformer-less inverter topology that brings out the high-performance for grid connected inverters. The main advantages of this inverter eliminate the dead-time requirement, and allows both top and bottom switch from being on at same time, and thus shorting the DC bus supply to ground. This avoids the freewheeling diodes connected across the switches for loads other than purely resistive. Low output voltage distortion and low fundamental and common voltages losses result in high efficiency and high output power density. The input dc source and the output ac voltage share the same ground in proposed inverter, which effectively eliminates the leakage current caused by the DC source (PV panel, battery bank etc.). Analysis and simulation results are presented to demonstrate the effectiveness of the proposed inverter. Compared to the prior literature mentioned in this paper, 75–86% reduction of semiconductor components is achieved with proposed inverter topology.**

***Index Terms*-- Inverter, grid, deadtime, voltage distortion.**

I. INTRODUCTION

The photovoltaic systems (PV), wind turbine systems, and energy storage system like battery bank output voltage are usually DC power, but it should be converted to AC power before being discharged into the grid or used by various loads. Therefore, grid-connected inverters play a key role in converting DC voltage and current to AC power and deliver them to grid. In fact, the inverter is an interface between grid and DC source to transfer the high-quality power. Since the grid waveforms are AC and sinusoidal, the inverter output should be sinusoidal as possible [1-5].

The transformer-less inverters have many advantages as a grid-connected inverter, such as high-efficiency, small size, light weight, low cost [6-22]. The unipolar sinusoidal pulse width modulation (SPWM) full-bridge inverter has received extensive attentions to its good differential-mode characteristics such as higher dc voltage utilization, smaller current ripple in the filter inductor and higher processing efficiency [23-24]. However, the common-mode voltage at switching frequency is brought in so that this kind of inverter cannot be directly equipped to the transformer-less grid-connected application [25-26].

To make efficient use of the unipolar SPWM full-bridge in transformer-less grid-connected inverter, many in-depth research, where new freewheeling paths are constructed to separate the PV array from the grid in the freewheeling period [27-35]. Based on the common-mode equivalent model of the full-bridge inverter derived in [27-28], it is necessary that the potential of the freewheeling path is clamped to half input voltage in the freewheeling period instead of disconnecting the PV array from the grid simply. And depending on this way, the high-frequency common-mode voltage can be completely avoided in the unipolar SPWM full-bridge inverter. The topologies in [27-35] are complying with the above conclusion, but they have different clamping ability. In [27] (as in Fig.1(b)), if the freewheeling path potential rises, it can be clamped; but, if the freewheeling path potential falls, it cannot be clamped. In [28-31], a diode clamping branch to the input voltage side (as in Fig.1(c)), and the potential can be freely clamped in the freewheeling period. In [34], Fig.1(d), when the freewheeling path potential falls, it can be clamped; however, when the freewheeling path potential rises, it cannot be clamped effectively during dead time between the switches *S1* and *S2*. Apparently, the leakage current suppression performance in these three kinds of topologies is different due to the clamping ability. The

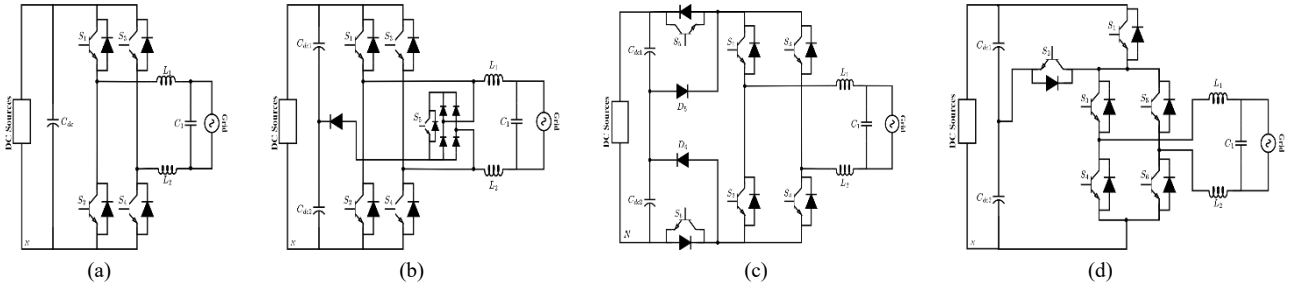


Fig. 1 Basic full-bridge topology and improved full-bridge topologies in prior research papers,
(a). Basic full-bridge topology, (b). Topology in paper [27], (c). Topology1 in paper [28-31], (d), Topology2 in paper [34]

prior topology in [34] as in Fig.1(d) has best performance about leakage current suppression in existing topologies of single-phase full-bridge transformer-less grid-connected inverter.

However, leakage current suppression and mismatch in turn-on and turn-off delays of switching devices, a dead time should be considered in the control of above inverter topologies to avoid the shoot through in dc link caused by the simultaneous conduction on both switches in an inverter leg. Also, for load other than purely resistive, load current will not be in phase with the load voltage, therefore freewheeling diode should be connected anti-parallel with switches to prevent the development of high voltage across the switch. The freewheeling diode increase the cost of the inverter system and, dead-time can cause some problems such as output waveform distortion, fundamental voltage loss, and common-mode voltage loss, especially with high switching frequency and large dead-time.

In this paper a new transformer-less inverter topology without dead-time, and freewheeling diodes have been presented to overcome the above issues.

II. Proposed Inverter Topology

Figure2 shows the schematic of proposed transformer-less inverter topology. This inverter composed of two semiconductor switches (S_1,S_2), two inductors (L_1, L_2) and two capacitors (C_1, C_2). Both switches (S_1,S_2) operate complementary manner and output the positive and negative voltages with continuous voltage gain. Therefore, using SPWM modulation method this topology can be used as an inverter and output voltage range is same as the full-bridge inverter.

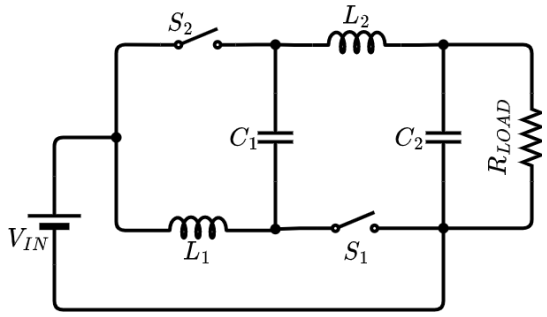


Fig. 2 Schematic of proposed inverter

A. Circuit operations and operating principles

Figure 3 shows the voltage gain against the switch *S1* duty cycle of proposed inverter. The switch S_1 and S_2 is conducted in a complementary manner. The orange portion of the curve in Fig.3 confirm that, by operating the switch S1 with duty cycle (D_{S1}) changing from 0 to 2/3, the proposed inverter is able to output the voltage range from $-V_{in}$ to $+V_{in}$ similar to the conventional full bridge inverter.

When the duty cycle of S_1 changes from (0~0.5), the inverter can output the positive voltage. And when the duty cycle of S_1 changes from (0.5~2/3), the inverter can output the negative voltage. When the duty cycle is equal to 0.5 the inverter is able to output zero voltage.

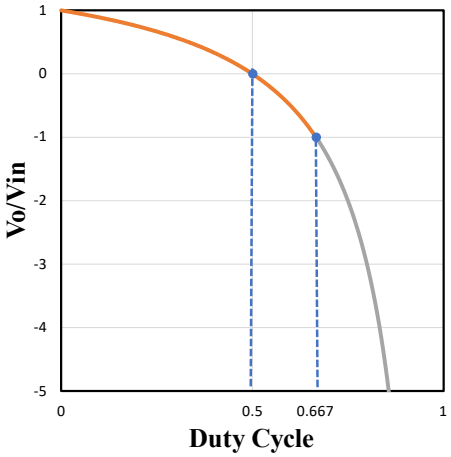
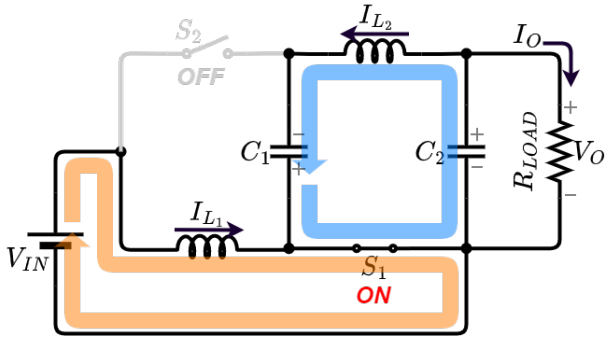
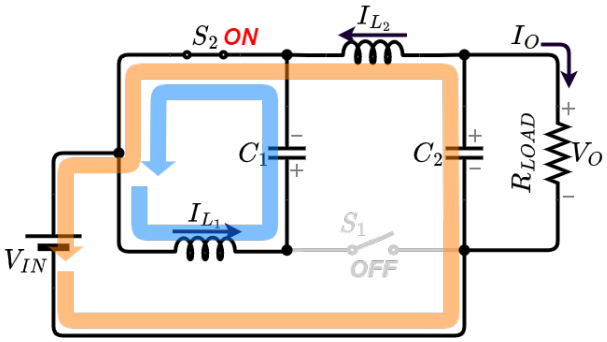


Fig. 3 Duty cycle and voltage gain of the proposed inverter

Fig. 4 shows the equivalent circuit of operating states in a switching cycle using proposed inverter. Fig. 4(a) shows the Mode-I when switch S_1 is conducted and S_2 is OFF. During this period, the capacitor C_1 and the input voltage source charge the two inductors (L_1, L_2), and the inductor current is increased. Fig. 4(b) shows the Mode II when switch S_2 is conducted. During this period, the two inductors become the source and the inductor current is decreased.



(a). Mode-I Switch S_1:ON, S_2:OFF



(b). Mode-II Switch S_1:OFF, S_2:ON

Fig. 4 Operation mode of the proposal inverter in a switching cycle

According to the inductor voltage second balance and the capacitor charge balance equations, voltage gain (V_o/V_{in}), capacitor voltage V_{C1}, inductor current (I_{L1}), inductor current (I_{L2}) can be derived as in (1),(2),(3),(4) respectively.

$$\frac{V_O}{V_{IN}} = \frac{1 - 2D_{S_1}}{1 - D_{S_1}} \tag{1}$$

$$V_{C_1} = \frac{D_{S_1}}{1 - D_{S_1}} V_{IN} \tag{2}$$

$$I_{L_1} = \frac{D_{S_1}}{1 - D_{S_1}} I_O \tag{3}$$

$$I_{L_2} = -I_O \tag{4}$$

The output voltage of the proposed inverter can be defined as (5). And the modulation index can be defined as (6), the duty cycle D_{S1} of the switch *S1* as in (7) can be determine using (5),(6) and (1).

$$V_O = Vsin(\omega t) \tag{5}$$

$$M = \frac{V}{V_{IN}} \tag{6}$$

$$D_{S_1} = \frac{1 - Msin(\omega t)}{2 - Msin(\omega t)} \tag{7}$$

$D_{S2}=1- D_{S1}$ is the duty cycle of *S2* is derived as (8).

$$D_{S_2} = \frac{1}{2 - Msin(\omega t)} \tag{8}$$

Since relationship of the conventional full bridge inverter output and input voltage is linear in terms of switch duty cycle, the sinusoidal output voltage can be achieved using a sinusoidal signal as a reference to the duty cycle variation. However, the output voltage and the input voltage of the proposed inverter are not a linear relationship with the switch duty cycle. In order to achieve the sinusoidal output voltage of proposed inverter, a nonlinearly changed duty cycle is determined as in (7).
This duty cycle reference in (7) and (8) are used to generate the gate-source signal of switches S_1 and S_2 respectively. Switches S_1, S_2 ,voltage stress and current stress can be derived as (9) and (10). Assume $C_1 = C_2$, $L_1 = L_2$. where T_s is switching period.

$$V_{S_1} = V_{S_2} = V_{IN} + V_{C_1} = \frac{1}{1 - D_{S_1}} V_{IN} \tag{9}$$

$$I_{S_1} = I_{S_2} = I_{L_1} + I_{L_2} = -\frac{1}{1 - D_{S_1}} I_O \tag{10}$$

The capacitors C_1 ,C_2, peak voltage ripple can be derived as (11). And the inductors L_1, L_2 , peak current ripple can be derived as (12). Capacitors C_1 ,C_2, and Inductors L_1, L_2 , can be selected using peak ripple values derived in (11),(12).

$$\Delta V_{C_1} = \Delta V_{C_2} \frac{I_{L_1} T_S \left(1 - D_{S_1}\right)}{C_1} \tag{11}$$

$$\Delta I_{L_2} = \Delta I_{L_2} = \frac{V_{IN} T_S D_{S1}}{L_1} \tag{12}$$

B. Deadtime effect on grid-connected inverter and deadtime-less operation of proposed inverter

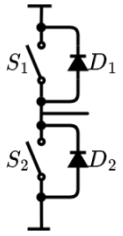
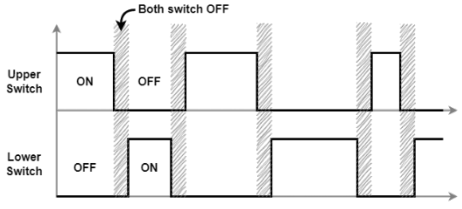


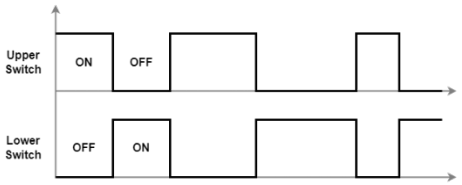
Fig. 5 Inverter bridge (phase-leg)

Power electronic inverters are devices that are used to interface renewables, such as photovoltaic panels or wind turbines, with the electrical power system. The inverter should control its output current to follow a sinusoidal reference to avoid distorting the voltage waveform of the power system.

However, in traditional inverter bridge (as in Fig.5) shoot-through must be prevented to ensure effective operation. This is because it introduces additional losses and can cause thermal runaway. It may lead to failure of the switching device and the entire inverter. When both devices conduct simultaneously, the current limited mainly by the parasitic inductance of the DC link. To prevent the generating of a bridge shoot-through current, add dead time as in Fig.6(a) into the control scheme. This additional time make sure, one of the two switch is always turned OFF first, and the other one will be turned on after the dead time has elapsed. Thus, preventing the bridge shoot-through caused by the asymmetrical turn-on and turn-off times of the devices.



(a). Conventional inverter with dead-time

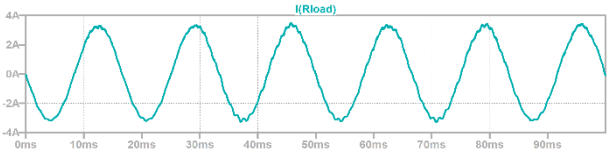


(b). Proposed inverter without dead-time

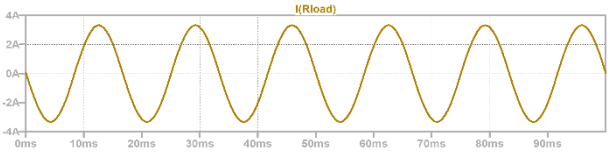
Fig.6 Single phase-leg switch control signal for upper and lower switch

In general, applying dead time in the control signals which causes unwanted harmonics, distorts the output voltage and the output current leading to lower power quality.
For an induction motor, selecting an unnecessarily long dead time can lead to system instability and catastrophic consequences.
The exact value of harmonics is difficult to predict due to nonlinear nature of the deadtime. Also, deadtime varies with gate resistor value, gate driver collector current on switching time. Thus, the process of choosing a dead time is indispensable, and should be performed with caution.

Proposed inverter drive the both switches as in Fig.6(b) without deadtime leads to improve the power quality of grid-connected inverter. Compared to the conventional inverter, Fig.7 shows the effect of dead-time to grid current quality. Fig.7(a) shows simulated output current when single-phase conventional inverter operated with dead-time and Fig.7(b) shows simulated output current in a proposed inverter when dead time is ignored.



(a). With dead-time



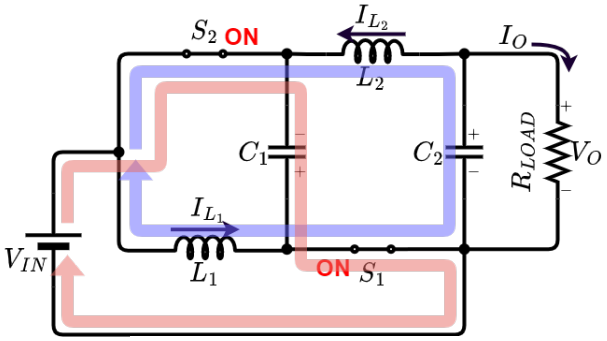
(b). Without dead-time

Fig.7 Effect of dead-time to grid current quality

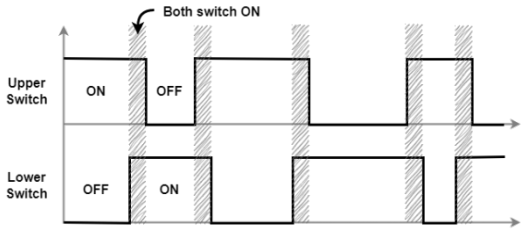
C. Elimination of free-wheeling diode of proposed inverter

During the dead-time, in a conventional inverter bridge (as in Fig,5) either diode D1 or D2 conduct, depending on the instantaneous direction of the output current. The conduction of these anti-parallel diodes causes distortion in the output terminal voltage of the inverter and introduces harmonic current.

However, in proposed inverter shoot-through switching state allows both top and bottom switches from being on at same time as in Fig.8. This avoids the freewheeling diodes connected across the switches for loads other than purely resistive.



(a). Simultaneous ON of both switches



(b). Shoot-through switching waveform

Fig.8 Shoot-through state of proposed inverter

D. Leakage current mitigation with common ground

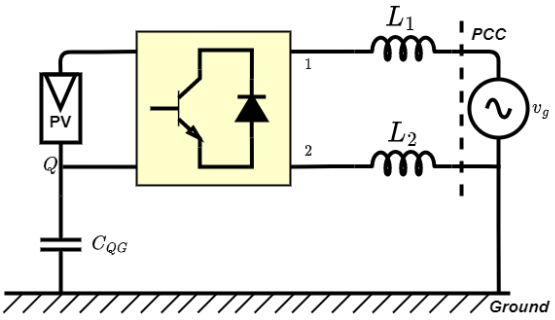
In photovoltaic systems, parasitic capacitance is often formed between PV panels and the ground. Because of the switching nature of PV converters, a high-frequency voltage is usually generated over these parasitic capacitances and results a common mode current known as leakage current. This current can badly reach a high value if a resonance circuit is excited through the PV's parasitic capacitance and the converter's inductive components. Transformers are usually used for leakage current mitigation. However, this decreases the efficiency and increases the cost, size, and weight of the PV systems. Number of strategies have been introduced to mitigate the leakage current in transformer-less converters. Among these strategies, using common-ground converters is considered the most effective solution as it offers a solid connection between the negative terminal of PV modules and the neutral of the grid side. In addition, the grounding of a PN system can minimize the effects of lighting and other usages[35].

The mechanism of leakage current generation can be explained by using the single-phase PV system as shown in Fig.10. Where v_{1Q} v_{2Q} are the voltages of the inverter terminals to the reference point Q. Two voltage components, differential mode(DM) and common-mode (CM) can er identified in terms of v_{1Q} and v_{2Q} as in (13) and current of the inverter terminals, i_1 i_2, can be expressed as in (14). According to (13) and (14) simple model (as in Fig.9(c)) for the total common-mode voltage ($v_{cm\text{-}total}$) can be determined as in (15).

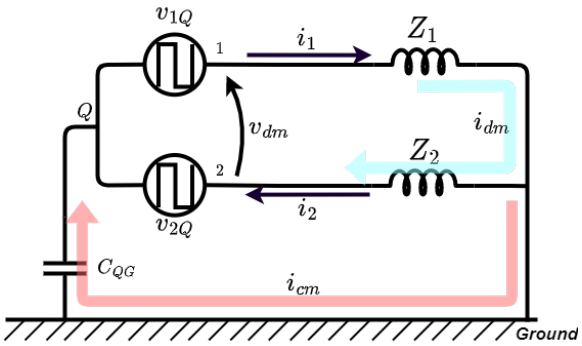
$$v_{dm} = v_{1Q} - v_{2Q} \;\; and \;\; v_{cm} = \frac{v_{1Q} + v_{2Q}}{2} \qquad (13)$$

$$i_1 = i_{dm} + \frac{i_{cm}}{2} \quad and \quad i_2 = \frac{i_{dm} - i_{cm}}{2} \tag{14}$$

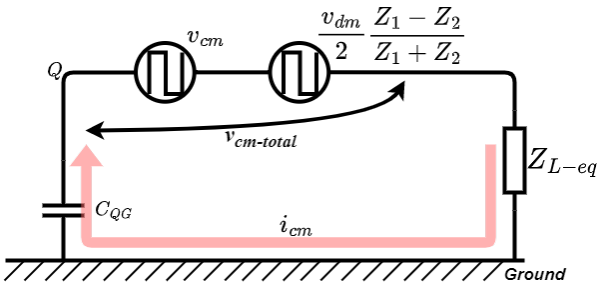
$$v_{cm-total} = v_{cm} + \frac{v_{dm}}{2}\left(\frac{Z_1 - Z_2}{Z_1 + Z_2}\right) \tag{15}$$



(a). General Circuit



(b). Common-mode equivalent circuit



(c). Simplified circuit for total common mode voltage

Fig.9 Single-phase grid-connected PV inverter

According to the above analysis, there are mainly three directions that can be adopted to eliminate or minimize leakage current in single-phase PV inverters [36].

1. Equal line impedances (Z1 and Z2). This requires two filter inductors with independent iron cores, which results in increased size and cost.
2. Achieving constant value for CM components, there are two methods in prior research, modulation-based method and converter-based method. Both methods need extra cost due to high-switching losses, high harmonic contents and the implementation problem with switch parasitic capacitances.
3. By passing the parasitic capacitance of PV system using common-ground converters. This represents the most effective solution as it offers complete mitigation of leakage current.

Proposed converter introduced in this paper is common-grounded inverter and suitable to eliminate leakage current in single -phase PV inverters. This uses the few numbers of components and only two semiconductor switches use in simple circuit operation.

E. Inverter Control

Control structure has been implemented for the single-phase inverter is shown in Fig.10. Both switches (*S1,S2*) operate complementary manner and output the positive and negative voltages with continuous voltage gain. Therefore, using SPWM modulation method this topology can be used as an inverter and output voltage range is same as the full-bridge inverter. In conventional full-bridge inverter sinusoidal reference as in (16) is used to achieve inverter sinusoidal output.

$$V_{ref\_conv} = Vsin(\omega t) \tag{16}$$

However, in the proposed inverter input and output voltages ae not a linear relationship with duty cycle. Therefore, modified reference as in (17) is used to achieve the sinusoidal output of proposed inverter.

$$V_{ref\_modified} = \frac{1}{2 - Msin(\omega t)} \tag{17}$$

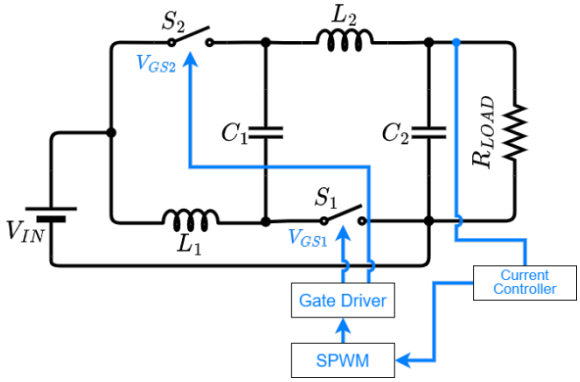


Fig.10 Proposed inverter control structure

F. Specifications and Parameters

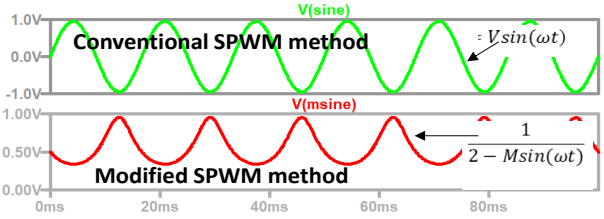
Table 1 shows the specifications and parameters used in the computer simulation.

TABLE 1 SPECIFICATIONS AND PARAETERS

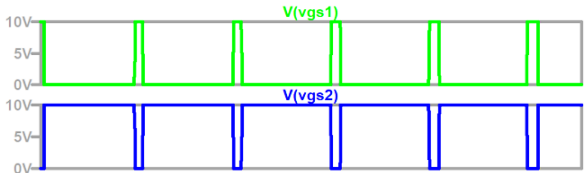
Description	Symol	Value
Input voltage	*Vin*	162V
Output power	*Po*	250W
Switching frequency	*fs*	10kHz
Modulation index	*M*	.95
Modulating wave frequency	*fm*	60Hz
Load	*RLOAD*	49Ω
Capacitors	*C1,C2*	270µF
Inductors	*L1,L2*	100µH

III. Simulation Verification

Computer simulation is conducted to verify the operation of proposed inverter using LTspice simulator. Fig.11(a) shows the conventional and modified reference signal for SPWM modulation. Gate-driver signals (V_{GS1},V_{GS2}) for the switch S_1 and S_2 generated using the modified reference signal as shown in Fig.11(b).



(a). Reference signal for SPWM modulation

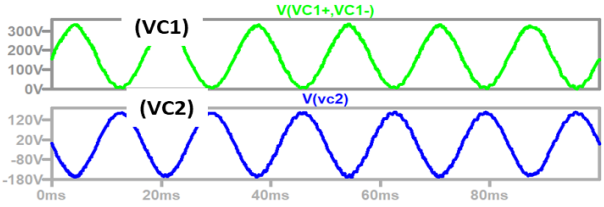


(b). Gate driver signal for switch S1 and S2

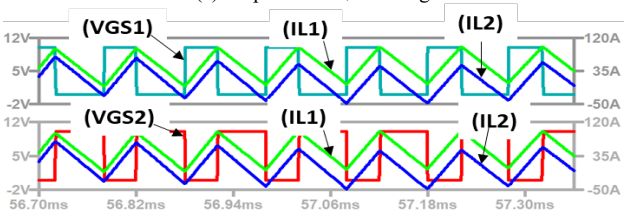
Fig.11 Gate driver and reference signals

Fig.12(a) shows the gate-source voltages (V_{GS1},V_{GS2}), drain-source voltages (V_{DS1}), (V_{DS2}), inverter output voltage (V_o) and output current (I_o). Fig.12(b) shows the zoomed waveforms of the Fig.12(a). Both waveforms of inverter output voltage and current are pure sinewave and no any waveform distortion appeared. Peak output current is 3.6A, peak output voltage is 130V and the peak output power is 468W. The RMS output power is 281W.

Fig.13 shows the voltages (V_{C1},V_{C2}) across the capacitors C_1,C_2 and, current waveforms (I_{L1},I_{L2}) through the inductors L_1,L_2. Above all simulation results confirmed that the proposed inverter topology provides the sinewave output with reduced components and without output voltage distortion.

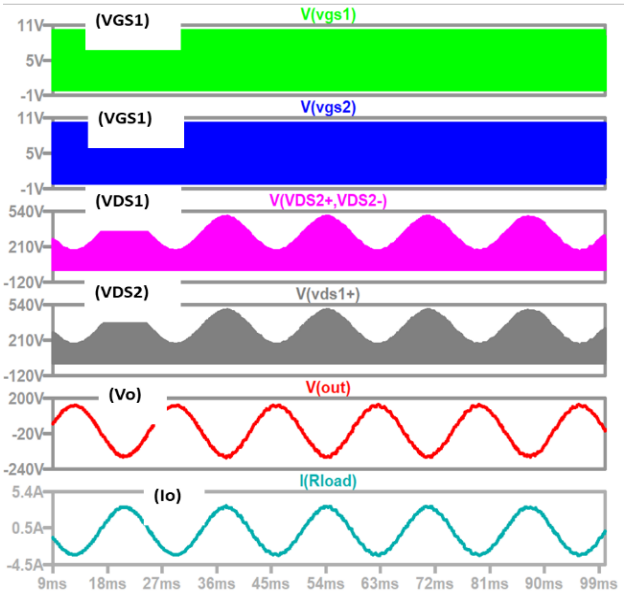


(a). Capacitors C_1,C_2 voltages

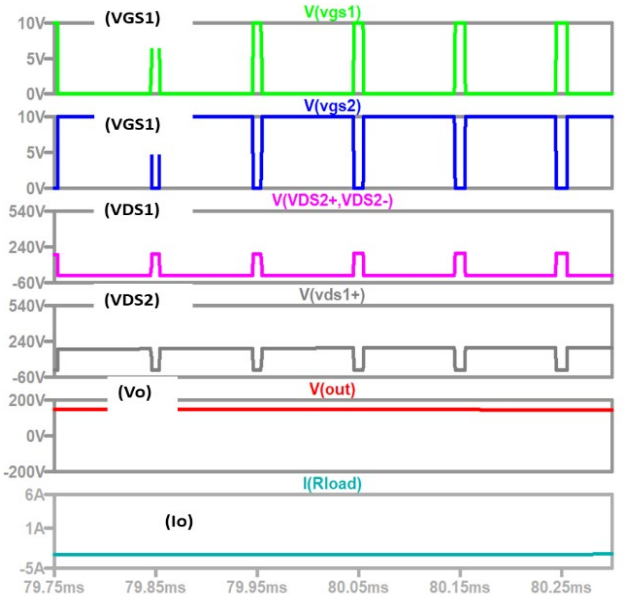


(b). Inductors L_1,L_2 currents

Fig.13 Waveforms for voltages (V_{C1},V_{C2}) across the capacitors C_1,C_2 and, current waveforms (I_{L1},I_{L2}) through the inductors L_1,L_2



(a). V_{GS1},V_{GS2},V_{DS1},V_{DS2},V_o,I_o



(b). Zoom waveforms of V_{GS1},V_{GS2},V_{DS1},V_{DS2},V_o,I_o

Fig.12 Simulation waveforms of proposed inverter using LTspice

IV. Conclusions

This paper proposed a single-phase transformer-less, deadtime-less reduced component inverter topology. This topology can be used to grid-tie inverter application especially suitable for photovoltaic (PV) panel because it is naturally eliminating the leakage current caused by the PV panel since the input DC source and output AC source share the same ground. Compared to the conventional single-phase full-bridge topologies, proposed inverter can utilize only two switching devices to achieve the same output voltage as the conventional full-bridge inverter. This inverter eliminates the dead-time requirement and allows both top and bottom switches from being on at same time. This avoids the freewheeling diodes connected

across the switches for loads other than purely resistive. Analytical results are presented, and validity of proposed inverter topology verified by using the LTspice simulation and more results will be provided with final paper. Compared to the prior literature mentioned in this paper, 75–86% reduction of semiconductor components is achieved with proposed inverter topology.

REFERENCES

[1] Xue Y, Chang L, Kjaer SB, Bordonau J, Shimizu T. Topologies of single-phase inverters for small distributed power generators: an overview. IEEE Trans Power Electron 2004,vol.19 no.5, pp1305–14.

[2] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," IEEE Trans. Ind. Appl., vol. 41, no. 5, pp. 1292–1306, Sep./Oct. 2005.

[3] A. Sangwongwanich, Y. Yang, and F. Blaabjerg, "A sensorless power reserve control strategy for two-stage grid-connected PV systems," IEEE Trans. Power Electron., vol. 32, no. 11, pp. 8559–8569, Nov. 2017.

[4] Z. Zhao, M. Xu, Q. Chen, J.-S. Lai, and Y. Cho, "Derivation, analysis, and implementation of a boost–buck converter-based high-efficiency PV inverter," IEEE Trans. Power Electron., vol. 27, no. 3, pp. 1304–1313, Mar. 2012.

[5] Z. Zhao, J.-S. Lai, and Y. Cho, "Dual-mode double-carrier-based sinusoidal pulse width modulation inverter with adaptive smooth transition control between modes," IEEE Trans. Ind. Electron., vol. 60, no. 5, pp. 2094–2103, May 2013.

[6] Z. Yang, P. C. Sen, "A novel switch-mode DC-to-AC inverter with nonlinear robust control," IEEE Trans. Industrial Electronics, vol. 45, pp. 602-608, 1998.

[7] R. O. Caceres, I. Barbi, "A boost DC-AC converter: analysis, design, and experimentation," IEEE Trans. Power Electronics, vol. 14, pp. 134-141, 1999.

[8] Z. Yang, P. C. Sen, "Bidirectional DC-to-AC inverter with improved performance," IEEE Trans. Aerospace and Electronic Systems, vol. 35, pp. 533- 542, 1999.

[9] N. Vazquez, J. Almazan, J. Alvarez, C. Aguilar, and J. Arau, "Analysis and experimental study of the buck, boost and buck-boost inverters," in Power Electronics Specialists Conference, 1999. PESC 99. 30th Annual IEEE, 1999, pp. 801-806 vol.2.

[10] N. Kasa, T. Iida, H. Iwamoto, "An inverter using buck-boost type chopper circuits for popular small-scale photovoltaic power system," Proceeding of IEEE 25th Annual Conference of Industrial Electronics Society, 1999. IECON '99, pp. 185-190 vol.1.

[11] S. Funabiki, T. Tanaka, and T. Nishi, "A new buck-boost-operation-based sinusoidal inverter circuit," IEEE Power Electronics Specialists Conference, 2002., pp. 1624-1629.

[12] F.-S. Kang, C. U. Kim, S.-J. Park, and H.-W. Park, "Interface circuit for photovoltaic system based on buck-boost current-source PWM inverter," IEEE Industrial Electronics Society 28th Annual Conference, 2002, vol.4, pp. 3257-3261.

[13] K. Chomsuwan, P. Prisuwanna, V. Monyakul, "Photovoltaic grid-connected inverter using two-switch buck-boost converter," 29th IEEE Photovoltaic Specialists Conference, 2002, pp. 1527- 1530.

[14] C.-M. Wang, "A novel single-stage full-bridge buck-boost inverter," IEEE Trans. Power Electronics, vol. 19, pp. 150-159, 2004.

[15] W. Yu, L. Jih-Sheng, H. Qian, C. Hutchens, J. Zhang, G. Lisi, A. Djabbari, G. Smith, and T. Hegarty, "High-efficiency inverter with H6-type configuration for photovoltaic non-isolated ac module applications," 25th IEEE Applied Power Electronics Conference and Exposition (APEC), 2010, pp. 1056-1061.

[16] V.-G. Gerardo, M.-R. P. Raymundo, and S.-Z. J. Miguel, "High efficiency single-phase transformer-less inverter for photovoltaic applications," Ingeniería, Investigación y Tecnología, vol. 16, no. 2, pp. 173–184, Apr./Jun. 2015.

[17] Y. R. Kafle, G. E. Town, X. Guochun, and S. Gautam, "Performance comparison of single-phase transformerless PV inverter systems," in Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC), Tampa, FL, USA, Mar. 2017, pp. 3589–3593.

[18] E. Afshari, G. R. Moradi, A. Ramyar, R. Rahimi, B. Farhangi, and S. Farhangi, "Reactive power generation for single-phase transformerless Vehicle-to-Grid inverters: A review and new solutions," in Proc. IEEE Trans. Electrific. Conf. Expo (ITEC), Chicago, IL, USA, Jul. 2017, pp. 69–76.

[19] S. V. Araujo, P. Zacharias, and R. Mallwitz, "Highly efficient singlephase transformerless inverters for grid-connected photovoltaic systems," IEEE Trans. Ind. Electron., vol. 57, no. 9, pp. 3118–3128, Sep. 2010.

[20] Z. Ozkan and A. M. Hava, "Classification of grid connected transformerless PV inverters with a focus on the leakage current characteristics and extension of topology families," J. Power Electron., vol. 15, no. 1, pp. 256–267, Jan. 2015.

[21] M. Islam, S. Mekhilef, and M. Hasan, "Single phase transformerless inverter topologies for grid-tied photovoltaic system: A review," Renew. Sustain. Energy Rev., vol. 45, pp. 69–86, May 2015.

[22] B. Liu, M. Su, J. Yang, D. Song, D. He, and S. Song, "Combined reactive power injection modulation and grid current distortion improvement approach for H6 transformer-less photovoltaic inverter," IEEE Trans. Energy Convers., vol. 32, no. 4, pp. 1456–1467, Dec. 2017.

[23] N. Mohon, T. M. Undeland and W. P. Robbins, Power Electronics: Converters Applications and Design, 2nd ed. New York, NY, USA: Wiley, 1995

[24] D. G. Holmes and T. A. Lipo, Pulse Width Modulation for Power Converters: Principles and Practice. Hoboken, NJ, USA: Wiley, 2003.

[25] Gu, Y.J., Li, W.H., Zhao, Y., Yang, B., Li, C.S., He, X.N.: 'Transformerless inverter with virtual DC bus concept for cost-effective grid-connected PV power systems', IEEE Trans. Power Electron., 2013, 28, (2), pp. 793–805.

[26] Xiao, H.F., Xie, S.J.: 'Transformerless split-inductor neutral point clamped three-level PV grid-connected inverter', IEEE Trans. Power Electron., 2012, 27, (4), pp. 1799–1808.

[27] Xiao, H.F., Xie, S.J.: 'Leakage current analytical model and application in single-phase transformerless photovoltaic grid-connected inverter', IEEE Trans. Electromagnetic. Compat.ibility, 2010, 52, (4), pp. 902–913.

[28] M. T. Azary, M. Sabahi, E. Babaei, and F. A. A. Meinagh, "Modified single-phase single-stage grid-tied flying inductor inverter with MPPT and suppressed leakage current," IEEE Trans. Ind. Electron., vol. 65, no. 1, pp. 221–231, Jan. 2018.

[29] T. Kerekes, R. Teodorescu, P. Rodriguez, G. Vazquez, and E. Aldabas, "A new high-efficiency single-phase transformerless PV inverter topology," IEEE Trans. Ind. Electron., vol. 58, no. 1, pp. 184–191, Jan. 2011.

[30] M. Xu, L. Zhang, Y. Xing, and L. Feng, "A novel H6-type transformerless inverter for grid-connected photovoltaic application," Proc. IEEE Ind. Electron. Appl., pp. 58–63, Jul. 2012.

[31] B. Ji, J. Wang, and J. Zhao, "High-efficiency single-phase transformerless PV H6 inverter with hybrid modulation method," IEEE Trans. Ind. Electron., vol. 60, no. 5, pp. 2104–2115, May 2013.

[32] B. Yang, W. Li, Y. Gu, W. Cui, and X. He, "Improved transformerless inverter with common-mode leakage current elimination for a photovoltaic grid-connected power system," IEEE Trans. Power Electron., vol. 27, no. 2, pp. 752–762, Feb. 2012.

[33] W. Yu, J.-S. Lai, H. Quian, and C. Hutchens, "High-efficiency MOSFET inverter with H6-type configuration for photovoltaic noniolated AC-module applications," IEEE Trans. Power Electron., vol. 26, no. 4, pp. 1253–1260, Apr. 2011.

[34] M. Victor, F. Greizer, S. Bremicker, and U. Hubler, "Method of converting ¨ a direct current voltage from a source of direct current voltage, more specifically from a photovoltaic source of direct current voltage, into an alternating current voltage," U.S. Patent 7 411 802, Aug. 12, 2008.

[35] Y. Tang, W. Yao, P. C. Loh, and F. Blaabjerg, "Highly reliable transformerless photovoltaic inverters with leakage current and pulsating power elimination," IEEE Trans. Ind. Electron., vol. 63, no. 2, pp. 1016–1026, Feb. 2016.

[36] Gaafar, M.A, Orabi, M.,Ahmed Ibrahm,etc.,"Common-ground photovoltaic inverters for leakage current mitigation:comparative review". Int. J. Applied Sciences.11-11226, pp1-27. 2021.