Modeling method for conducted noise flowing in power lines of DC/DC converter

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Keywords

«EMC», «Noises», «Modeling», «Simulation», «DC/DC converter»

Abstract

This paper presents the modeling method of the conducted noise flowing in the input and output side power lines of DC/DC converter. The noise evaluation of DC-DC converters for automotive is based on the leakage current flowing in the power lines. The equivalent circuit of the conducted noise is derived by measuring and frequency analysis the leakage current flowing in the power lines. The noise evaluation simulation is performed by using the equivalent circuit. The usefulness of this proposed method for noise evaluation simulation has been confirmed by comparing the noise reduction effect of EMI filters in simulation and experiment.

Introduction

Recently, due to global environmental issues, carbon neutrality is desired. One approach to this problem is the development and widespread use of HEV (hybrid electric vehicle) and EV (electric vehicle) that can reduce CO_2 emissions. In such vehicles, motor drive and battery charging are performed by power electronics devices, and the demand for power electronics devices is increasing. Nowadays, the power electronics devices are improved power density by downsizing. [1] In order to reduce the size of passive components of power electronics devices such as inductors and capacitors, the switching frequency of power semiconductors (MOSFET, IGBT, etc.) in the power electronics devices has been increased. However, since higher switching frequencies of power semiconductors lead to shorter voltage and current turn-on and turn-off times in the power semiconductors, electromagnetic interference (EMI) is increased. The conducted noise generated by switching may cause malfunctions in peripheral devices, and EMI countermeasure is an important technical issue.[2]-[4]

Current EMI countermeasures use a method of optimizing noise filters in experiments, which is time-consuming and expensive. In order to achieve efficient EMI countermeasures, the conducted noise must be evaluated and countermeasures using simulation. [5]-[11] Conventionally, by modeling the leakage currents flowing to the LISN (Line Impedance Stabilization Network) [12]-[17] or measuring the impedance of the noise path [18]-[20], the noise evaluation simulation by disturbance voltage has been performed. The noise evaluation method based on the disturbance voltage can only evaluate the noise

in one direction where the LISN is inserted. The DC-DC converters for EV and HEV need to be evaluated for noise in both input and output directions to convert power between two batteries in both directions. Evaluating the noise flowing in the power lines on the input and output sides make it possible evaluate the noise in bidirectional. Therefore, the noise modeling method that enables bidirectional noise simulation is needed.

This paper presents the modeling method of conducted noise flowing in the power lines of DC-DC converter. The noise modeling is performed by deriving equivalent circuits from measurements and analysis leakage current. The noise evaluation simulation is performed using equivalent circuit. Furthermore, comparing experimental and simulation result with Y-capacitor as EMI filter show the usefulness of this modeling method.

Evaluation Method of Conducted Noise

Fig. 1 shows the noise evaluation experimental system with DC-DC converter. In this circuit, the voltage of the regulated power supply is stepped down by the DC-DC converter and flows to the load. This DC/DC converter is used to convert the voltage between batteries in HEV and EV. The voltage is converted by switching MOSFETs. This DC-DC converter has four phases MOSFETs, and each switching frequency is 200 kHz. The LISN is inserted between the stabilized power supply and DC-DC converter on the input side to suppress external noise. The LISN, surface layer and GNDlow terminal of the DC-DC converter are connected to the copper plate in the experimental system. The leakage current occurred by the MOSFETs switching flows to the copper plate (i_l). The leakage current on the copper plate flows to the input side power lines through the LISN (i_{Vhigh} and $i_{GNDhigh}$) or to the output side through the LOAD (i_{Vlow} and i_{GNDlow}). These four currents flowing on the input and output sides are measured with current probe. To evaluate the noise on the input and output side of the DC/DC converter, performing FFT analysis on the four measured leakage currents. The parameters of noise evaluation experiment are indicated in TABLE 1.

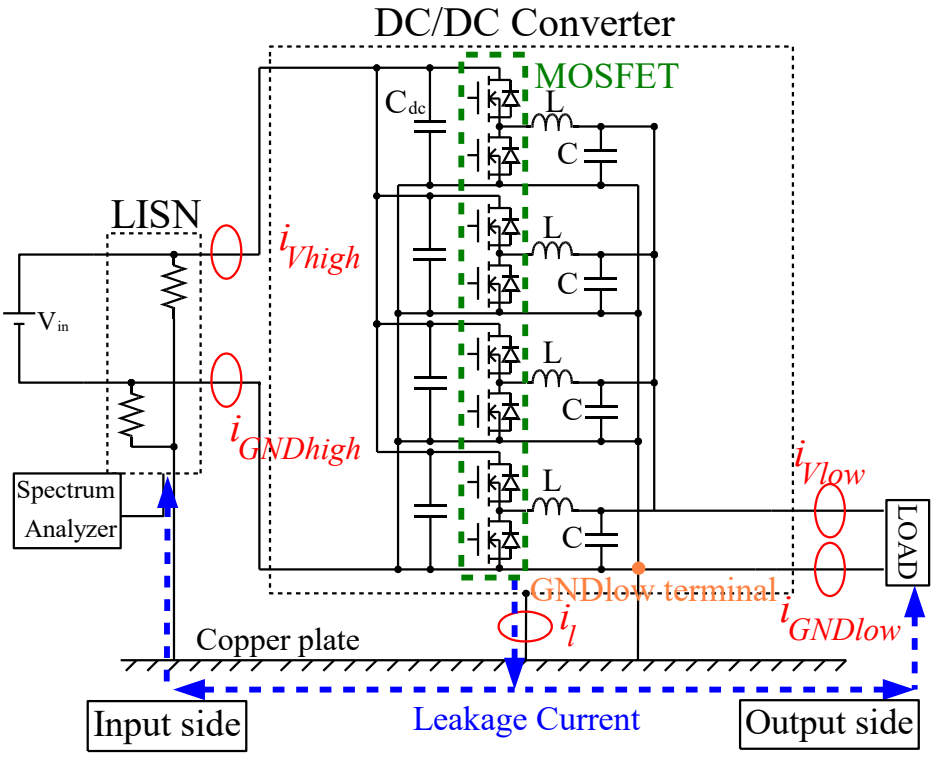

Fig. 1: Experimental system

Table I: Experimental condition

Input voltage V_{in}	35.0 V
Input current I_{in}	2.06 A
Output voltage V_{out}	12.0 V
Output current I_{out}	6.00 A
Output power P_{out}	72.0 W
LOAD R	2.00 Ω
Switching frequency f_{sw}	200 kHz

Experimental result

Fig. 2 shows the experimental FFT analysis result of the leakage current flowing to the copper plate from the surface layer of DC-DC converter (i_l). This leakage current consists of frequencies of 23.5, 28.3, 30.1 and 38.0 MHz. Fig. 3 shows the experimental result of the leakage current flowing in the input and output side power lines of DC/DC converter (i_{Vhigh}, $i_{GNDhigh}$, i_{Vlow} and i_{GNDlow}). The leakage currents in the power lines on the input and output sides are damped and vibrating. Fig. 4, Fig. 5, Fig. 6 and Fig. 7 shows the experimental FFT analysis result of the four leakage currents (i_{Vhigh}, $i_{GNDhigh}$, i_{Vlow} and i_{GNDlow}) in the input and output side power lines. The leakage currents in the power lines on the input and output sides consist of frequencies from 20 to 40 MHz and need to be reduced for EMI. Comparing Fig. 2, Fig. 4, Fig. 5, Fig. 6 and Fig. 7, the frequencies that constitute the leakage currents flowing into each of the power lines match the frequencies that constitute the leakage currents flowing from the substrate surface layer of the DC-DC converter to the copper plate. The conducted noise generated by MOSFET switching flows from the surface layer of the DC-DC converter board to the copper plate and then to the power lines on the input and output sides. In order to focus on the conducted noise leaking from the substrate surface layer of the DC-DC converter, in this paper 20 to 40 MHz bandpass filter is applied to the measured result of the leakage currents in the input and output sides power lines.

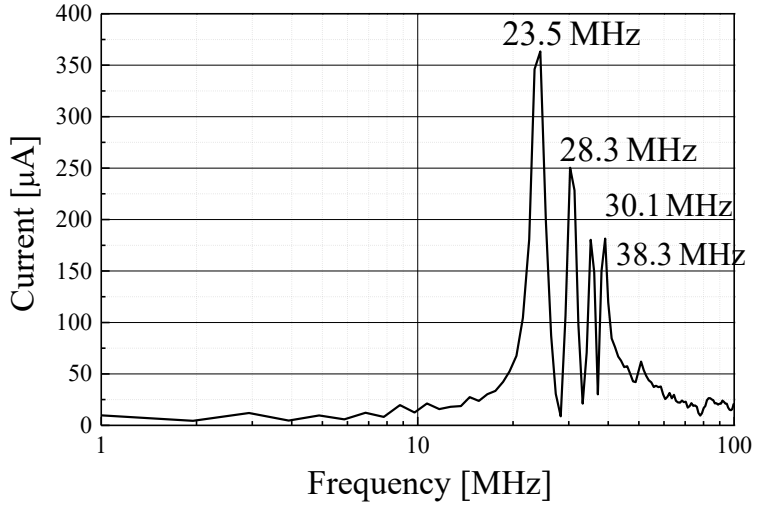

Fig. 2: Experimental FFT analysis result of the leakage current flowing to copper plate (i_l)

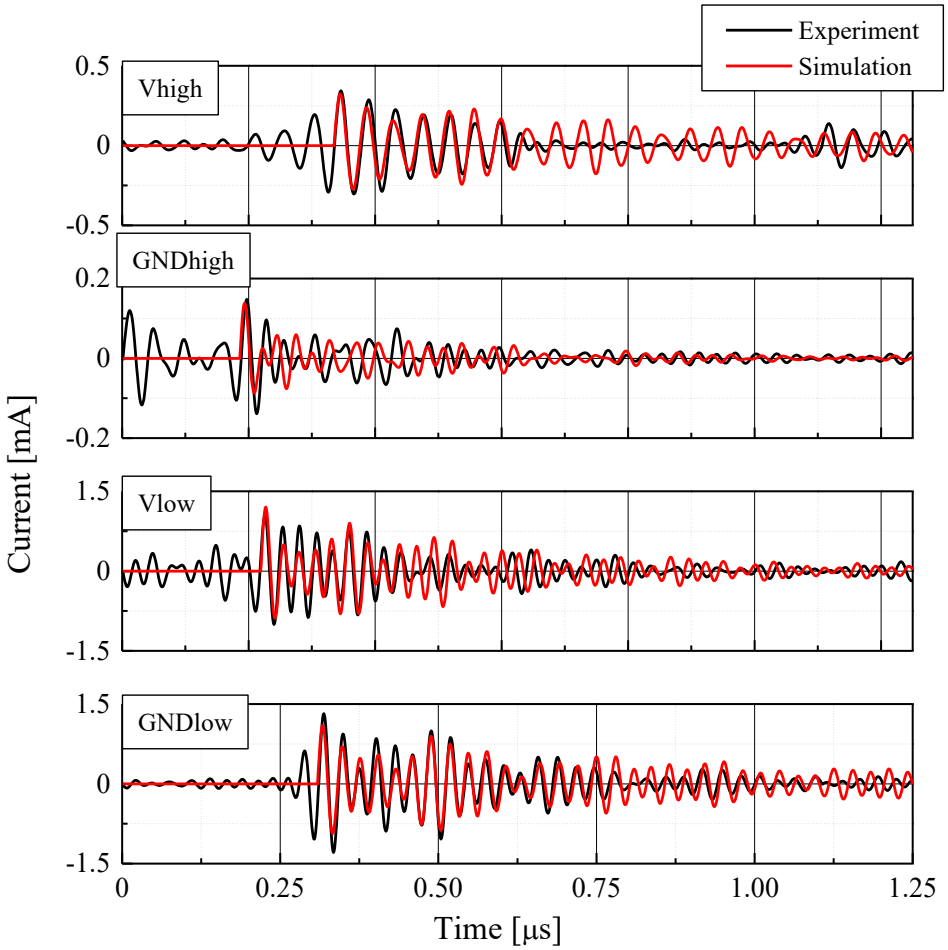

Fig.3: Experimental and simulation result of the leakage current flowing to the power lines

Simulation

The conducted noise flowing in the power lines on the input and output sides of DC-DC converters must be counteracted, and the noise modeling method is proposed to enable noise evaluation in simulation for efficient noise countermeasures. The leakage currents are modeled with a simple equivalent circuit from the measurement results.

Modeling Method

To simulate the conducted noise in the power lines, the leakage current equivalent circuit is derived by using experimental result of the four leakage currents. From Fig. 3, the waveform of i_{Vhigh}, i_{Vhigh}, i_{Vlow} and i_{GNDlow} are damped vibration. Therefore, the leakage current equivalent circuit of the four leakage currents is approximated by simple RLC series circuits. The equation of the damped vibration current after applying the step voltage E_c to the RLC series circuit is shown by the following equation.

$$i(t) \cong \frac{E_c}{Z_0} e^{-\zeta \omega_n t} \sin \omega_n t \tag{1}$$

$$Z_0 = \frac{E_c}{i_{peak}}, \qquad \zeta = \frac{R}{2Z_0}, \qquad \omega_n = 2\pi f \tag{2}$$

In the eq. (1) and (2), the parameter Z_0 is the characteristic impedance, the parameter ω_n is the eigen frequency, the parameter i_{peak} is the maximum value of the leakage current and the parameter ζ is the

attenuation coefficient. If the step voltage E_c is known, the eigen frequency and characteristic impedance can be derived from the peak current as in equation (2). The eigen frequency ω_n and the characteristic impedance Z_0 are obtained from the following equations for L and C of the resonant circuit.

$$\omega_n = \frac{1}{\sqrt{LC}}, \quad Z_0 = \sqrt{\frac{L}{C}} \tag{3}$$

In the eq. (3), the parameter L and C are inductance and capacitance of RLC series circuit. The parameters L and C are decided by the following equation.

$$L = \frac{Z_0}{\omega_n}, \quad C = \frac{1}{\omega_n Z_0} \tag{4}$$

The parameter R of RLC series circuit is determined by the state of the attenuation. Therefore, the leakage current equivalent circuit is completed when the parameters of RLC are determined with accuracy.

In this paper, the parameters of the equivalent circuit of the leakage current in Fig. 3 are determined by this modeling method. The step voltage E_c is 35 V, the maximum leakage current amplitude i_{peak} is referenced from Fig. 3, the resonance frequency is extracted from the results of each leakage current FFT analysis Fig. 4 - Fig. 7. Since the leakage current is generated by the sum of leakage currents of several frequencies, the high frequency equivalent circuit of the leakage current is composed of three or four parallel RLC circuits. The parameters of the equivalent circuit are calculated by using eq. (2) and eq. (4). The parameters are shown in TABLE II.

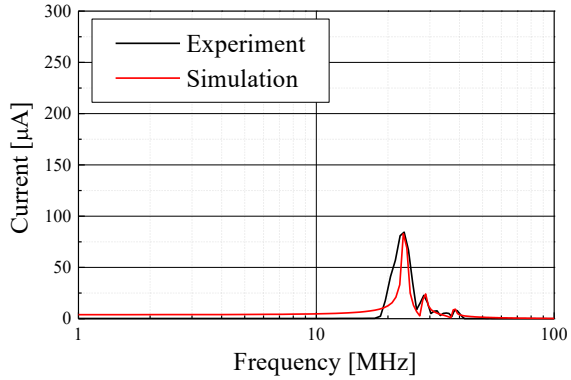

Fig. 4: Experimental and simulation FFT analysis result of i_{Vhigh}

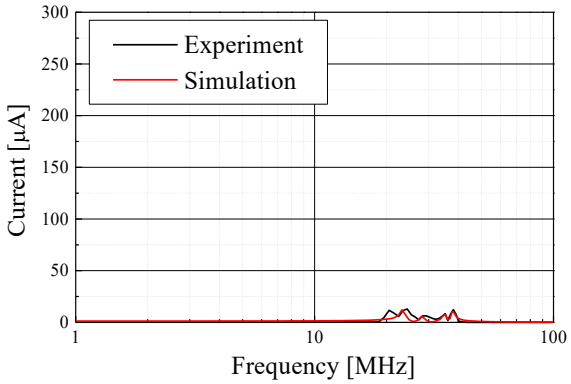

Fig. 5: Experimental and simulation FFT analysis result of $i_{GNDhigh}$

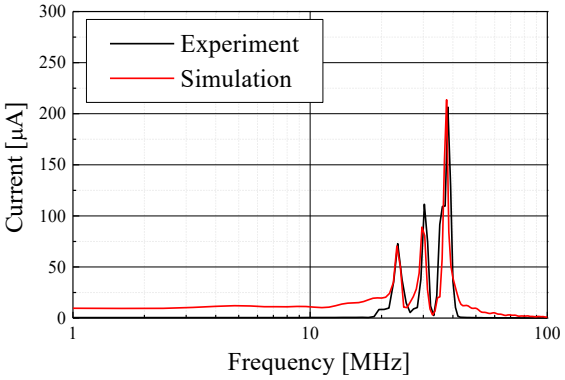

Fig. 6: Experimental and simulation FFT analysis result of i_{Vlow}

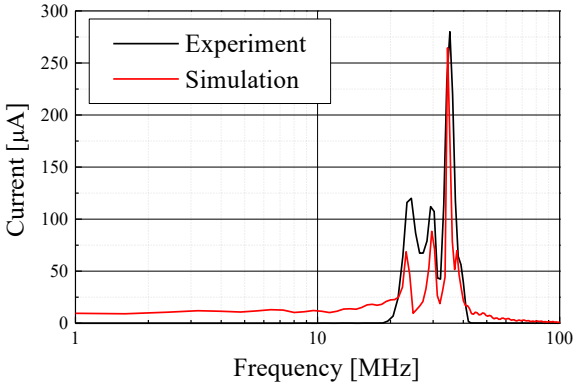

Fig. 7: Experimental and simulation FFT analysis result of i_{GNDlow}

TABLE II: The parameters of the high frequency equivalent circuits

i_{Vhigh}

f [MHz]	23.5	28.3	38.3
E_C [V]	35	35	35
i_{peak} [μA]	255	69	15.4
ω_n [Mrad/s]	148	178	239
Z_0 [kΩ]	137	507	2270
L_{a1},L_{a2},L_{a3} [μH]	927	2850	9490
C_{a1},C_{a2},C_{a3} [fF]	49.4	11.1	1.84
R_{a1},R_{a2},R_{a3} [kΩ]	3.0	9.0	2.0

$i_{GNDhigh}$

f [MHz]	23.5	28.3	35.1	38.3
E_C [V]	35	35	35	35
i_{peak} [μA]	48.6	23.6	31.8	46
ω_n [Mrad/s]	148	178	220	239
Z_0 [kΩ]	720	1490	1100	760
$L_{b1},L_{b2},L_{b3},L_{b4}$ [mH]	4.87	8.35	4.99	3.18
$C_{b1},C_{b2},C_{b3},C_{b4}$ [fF]	9.41	3.79	4.12	5.51
$R_{b1},R_{b2},R_{b3},R_{b4}$ [kΩ]	30	50	30	20

i_{Vlow}

f [MHz]	23.5	28.3	38.3
E_C [V]	35	35	35
i_{peak} [μA]	257	399	743
ω_n [Mrad/s]	148	189	239
Z_0 [kΩ]	136	87.7	47.1
L_{c1},L_{c2},L_{c3} [μH]	920	463	197
C_{c1},C_{c2},C_{c3} [fF]	49.8	60.3	88.9
R_{c1},R_{c2},R_{c3} [kΩ]	4.5	3.0	1.0

i_{GNDlow}

f [MHz]	23.5	30.1	35.1
E_C [V]	35	35	35
i_{peak} [μA]	255	399	743
ω_n [Mrad/s]	148	189	220
Z_0 [kΩ]	135	87.6	47.1
L_{d1},L_{d2},L_{d3} [μH]	927	463	214
C_{d1},C_{d2},C_{d3} [fF]	49.9	60.3	96.3
R_{d1},R_{d2},R_{d3} [kΩ]	3.0	2.8	0.6

Simulation Result

The conducted noise evaluation simulation circuit is shown in Fig. 8. The derived leakage currents equivalent circuit is inserted between the LISN and the LOAD part. The equivalent circuit configuration and parameters of the LISN are from the data sheet. [21] In addition, the equivalent circuit configuration and parameters of the LOAD and between LOAD and copper plate are decided from measurement result by impedance analyzer. Fig. 3 show simulation results of the leakage current flowing in the input and output side power lines (i_{Vhigh}, $i_{GNDhigh}$, i_{Vlow} and i_{GNDlow}). In Fig. 3, the attenuation of the leakage current flowing in the power line can be simulated. From Fig. 4 to Fig. 7 show the FFT analysis results of the simulation leakage currents (i_{Vhigh}, $i_{GNDhigh}$, i_{Vlow} and i_{GNDlow}). Compared the simulation result with the experimental result, the frequencies and amplitudes of the leakage currents in power lines are well simulated. Therefore, the conducted noise flowing in the input and output sides of the DC-DC converter is reproduced on the simulation.

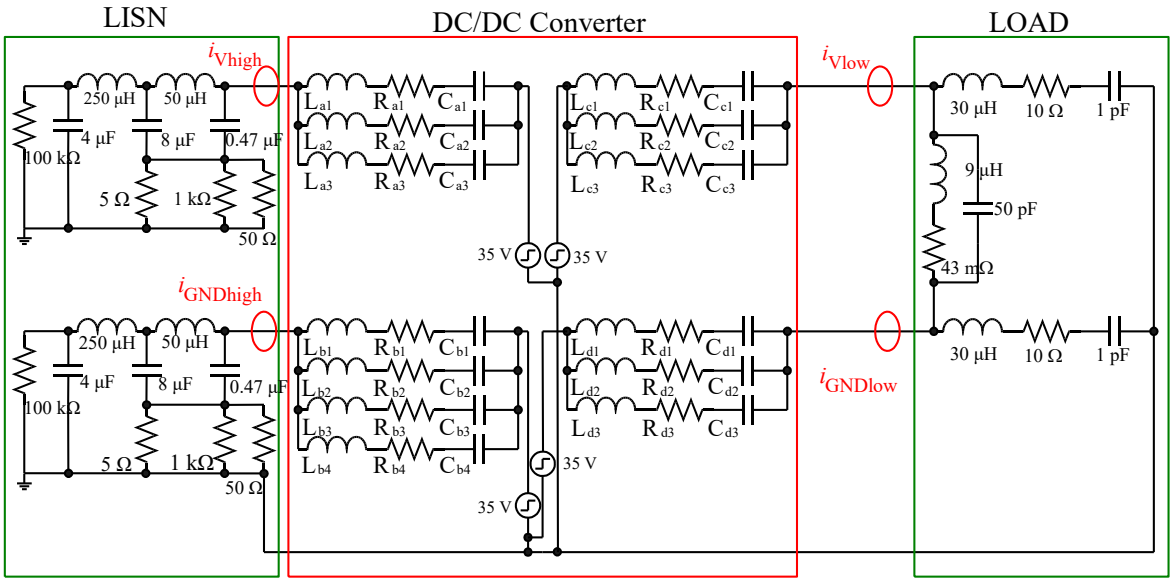

Fig. 8: Noise evaluation simulation circuit

Noise Evaluation Simulation and Experiment with EMI Filter

To confirm the usefulness of the proposed modeling method in this paper, the noise reduction effect of the EMI filter is simulated and then compared with the noise reduction effect of the EMI filter in the experiment.

Modeling EMI Filter

In this paper, Y-capacitors are used as EMI filters. Y-capacitor is inserted between the DC-DC converter and the LOAD to reduce conducted noise in the power line on the output side (i_{Vlow} and i_{GNDlow}). Inserting the Y-capacitor reduces the leakage current flowing in the output side power lines because the leakage current path is created through the capacitor instead of the load. Fig. 9 shows the impedance frequency characteristics of the Y-capacitor. The Y-capacitor with an impedance resonance point at 68 MHz is used for simulation and experiment. The impedance characteristics of Y-capacitor in the high frequency range can be modeled by RLC series circuit. The parameters of the RLC series circuit are matched from the frequency response data of the impedance of the capacitor. The parameters of Y-capacitor are as R_y = 3.00 Ω, C_y = 900 pF, L_y = 9.33 nH.

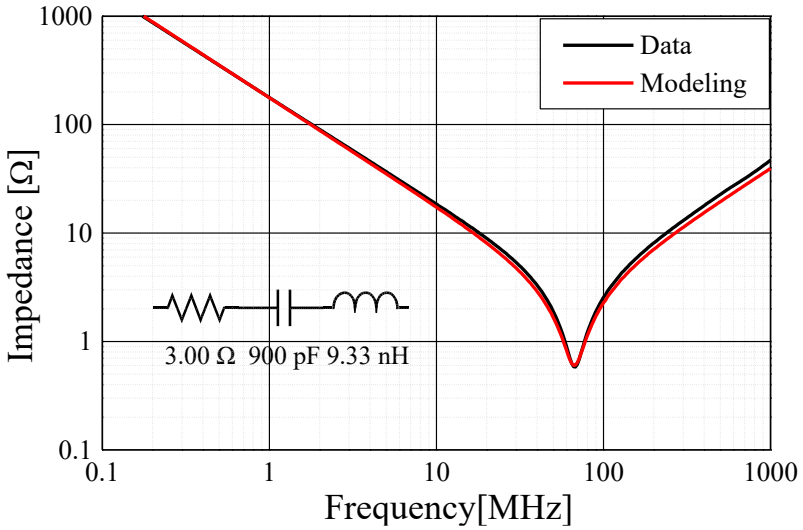

Fig. 9 Impedance Frequency Response of Y-Capacitor

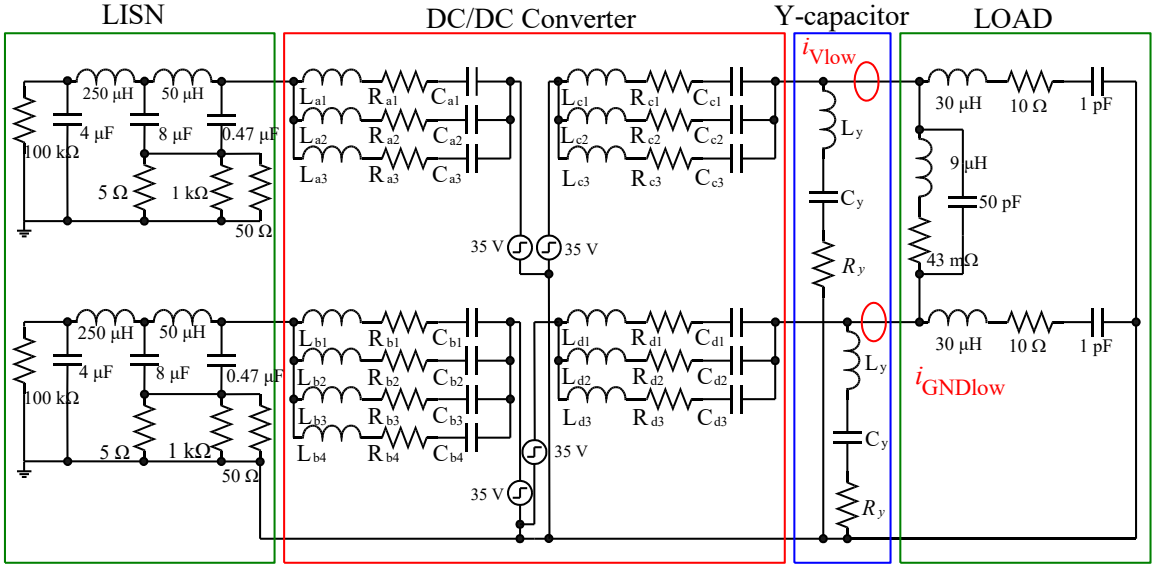

Fig. 10: Noise evaluation Simulation circuit with Y-capacitor

Noise Evaluation Simulation and Experiment Result

Fig. 10 shows the noise evaluation Simulation circuit with Y-capacitor. The Y-capacitor is inserted between DC-DC converter and LOAD part. The simulation results of the FFT analysis of the conducted noise in the output side power lines when the Y-capacitor is inserted are shown in Fig. 11 and 12 (i_{Vlow} and i_{GNDlow}). The Y-capacitor reduces the between 20 and 40 MHz conducted noise in the output side power lines in the simulation. The reduced effect of 200 μA is observed at the most reduced point. Next, the noise evaluation experiment is performed by inserting the Y-capacitor into the experimental circuit. Fig. 13 shows the experimental circuit when the Y-capacitor is inserted. As in the simulation, the Y-capacitor is inserted between the DC-DC converter and LOAD to reduce conducted noise on the output side power lines. Fig. 11 and 12 shows the experimental result of the FFT analysis of the conducted noise in the output side power lines when the Y-capacitor is inserted. From Fig. 11 and Fig.12, the Y-capacitor reduces the between 20 and 40 MHz conducted noise in the output side power lines in the experiment.

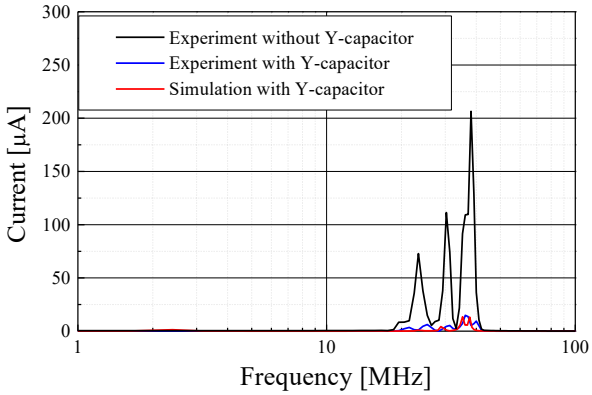

Fig. 11: Experimental and simulation FFT analysis result of i_{Vlow} with Y-capacitor

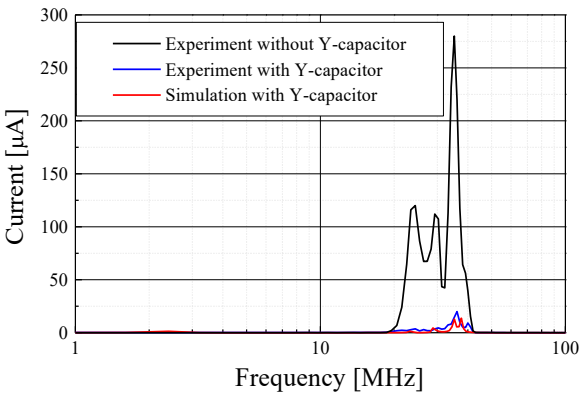

Fig. 12: Experimental and simulation FFT analysis result of i_{GNDlow} with Y-capacitor

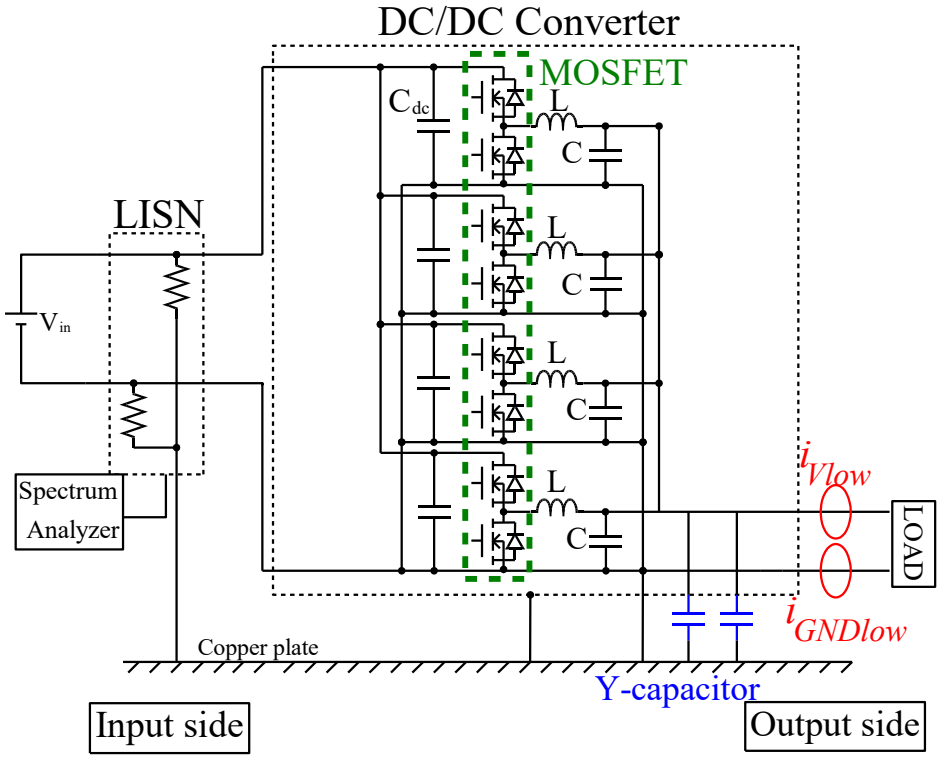

Fig. 13: Experimental circuit with Y-capacitor

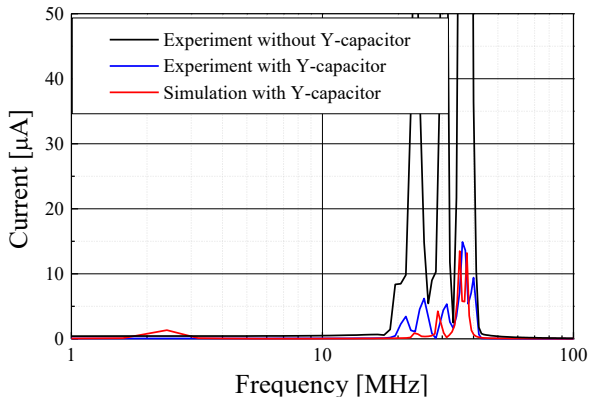

Fig. 14: Enlarged view of Experimental and simulation FFT analysis result of i_{Vlow} with Y-capacitor

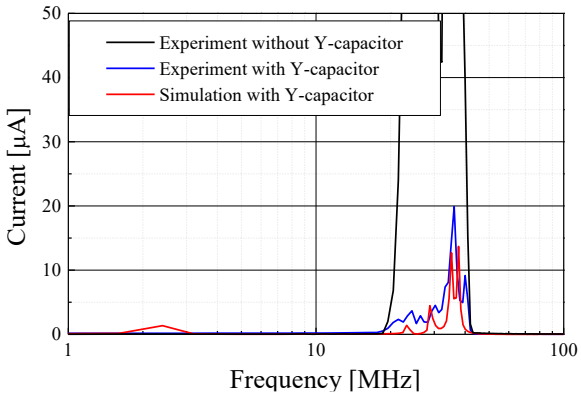

Fig. 15: Enlarged view of Experimental and simulation FFT analysis result of i_{GNDlow} with Y-capacitor

Comparing the simulation and experimental results of the leakage current FFT analysis in the output side (i_{Vlow}) in Fig. 11, the error in the reduction ratio is 0.3% at the most affected noise frequency of 35 MHz. In the same way, comparing the simulation and experimental results of the leakage current FFT analysis in the output side (i_{GNDlow}) in Fig. 12, the error in the reduction ratio is 2.6% at the most affected noise frequency of 38 MHz. Based on these results, simulations using the modeling method proposed in this paper are useful in confirming the effectiveness of noise reduction. Fig. 14 and Fig. 15 show the enlarged views of the FFT analysis results of the simulation and experiment of the leakage current in the output side power line of the DC-DC converter showed in Fig. 11 and 12. Comparing the simulation with the experiment when the Y-capacitor is inserted, there are frequencies of the leakage current that have been measured experimentally that have not been reproduced in the simulation. This is due to the lack of accuracy of the parameters of the leakage current equivalent circuit and the circuit configuration and circuit parameters of the load portion in the simulation circuit. Thus, the accuracy of the simulation can be enhanced by improving these simulation circuits.

Conclusion

This paper describes the modeling method of the conducted noise in the power lines of DC-DC converter. The noise evaluation by the leakage currents flowing in the input and output sides power lines enables bidirectional noise evaluation, which was not possible with the conventional noise evaluation of noise disturbance voltage. The noise evaluation simulation of leakage current flowing in power lines is performed by deriving the equivalent circuit from the leakage current measurement results. In the simulation results, the amplitude spectrum of the leakage current flowing in the power line (i_{Vhigh}, $i_{GNDhigh}$, i_{Vlow} and i_{GNDlow}) is well simulated. Furthermore, the simulation and experimentation were performed when Y-capacitor was inserted on the output side. The similar noise reduction effect with Y-capacitor in simulation and experiment with Y-capacitor. The usefulness of the simulation of noise evaluation using the modeling method proposed in this paper was confirmed. However, there is a difference in the peak frequency of the leakage current between simulation and experiment when a Y capacitor is inserted. In order to make the simulation using the modeling method in this paper practical in the future, the configuration and parameters of the simulation circuit should be reviewed to improve the accuracy.

References

[1] T. Kitamura, M. Yamada, S. Harada, M. Koyama, “Development of Highpower-density Interleaved DC/DC Converter with SiC Devices”, IEEJ Transactions on Industry Applications, Vol. 134, No. 11, pp. 956-961, 2014
[2] T. Shimizu, “Historical Review of EMI Measures in the Field of Power Electronics”, Annual Meeting Record, I.E.E Japan (CD-ROM), ROMBUNNO.S12-8, 2021

[3] C. Nan, R. Ayyanar and Y. Xi, “High frequency active-clamp buck converter for low power automotive applications,” 2014 IEEE Energy Conversion Congress and Exposition (ECCE), pp. 3780-3785, 2014
[4] L. Zhai, G. Hu, M. Lv, T. Zhang and R. Hou, “Comparison of Two Design Methods of EMI Filter for High Voltage Power Supply in DC-DC Converter of Electric Vehicle,” in IEEE Access, vol. 8, pp. 66564-66577, 2020
[5] M. Terasaki, Y. Oohashi, Y. Masuyama and T. Sudo, “Design and analysis for noise suppression of DC/DC converter,” 2014 IEEE Electrical Design of Advanced Packaging and Systems Symposium (EDAPS), pp. 109 - 112, 2014
[6] S. Maekawa, J. Tuda, A. Kuzumaki, S. Matsumoto, H. Mochikawa, H. Kubota, “EMI Prediction Method for SiC Inverter by Developing an Accurate Model of Power Device ”, IEEJ Transactions on Industry Applications, Vol. 134, No. 4, pp. 461-467, 2014
[7] E. Rondon-Pinilla, F. Morel, C. Vollaire and J. Schanen, “Modeling of a Buck Converter with a SiC JFET to Predict EMC Conducted Emissions,” in IEEE Transactions on Power Electronics, vol. 29, no. 5, pp. 2246-2260, May 2014
[8] D. Drozhzhin, V. Karakasli and G. Griepentrog, “Comprehensive Analysis of Converter Output Voltage for Conducted Noise Simulation,” 2019 International Symposium on Electromagnetic Compatibility – EMC EUROPE, pp. 42-47, 2019
[9] I. A. Makda and M. Nymand, “Common-mode noise analysis, modeling and filter design for a phase-shifted full-bridge forward converter,” 2015 IEEE 11th International Conference on Power Electronics and Drive Systems, pp. 1100-1105, 2015
[10] Y. Ishii et al., “Accurate Conducted EMI Simulation of a Buck Converter With a Compact Model for an SiC-MOSFET,” 2020 IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 2800-2805, 2020
[11] S. Takahashi, K. Wada, H. Ayano, S. Ogasawara, “Review of Modeling and Suppression Techniques for Electromagnetic Interference in power Conversion Systems”, 2022 IEEE Journal of Industry Applications, Vol. 11, No. 1, pp. 7-19 ,2022 The Institute of Electrical Engineer of Japan
[12] H. Tanaka, K. Suzuki, W. Kitagawa, T. Takeshita, “Conducted Noise Reduction on AC/DC Converter using SiC-MOSFET ”, 2016 IEEE International Conference on Renewable Energy Research and Applications (ICRERA), pp. 341-346, 2016
[13] H. Tanaka, K. Suzuki, W. Kitagawa and T. Takeshita,“Design for conducted noise reduction on AC/DC converter using SiC-MOSFET,” 2016 19th International Conference on Electrical Machines and Systems (ICEMS), pp. 1-6, 2016
[14] Y. Kawamura, H. Tanaka, K. Suzuki, W. Kitagawa and T. Takeshita, “Investigation of Modeling for Conducted Noise Reduction on Isolated AC/DC Converter using SiC Devices,” 2018 20th European Conference on Power Electronics and Applications (EPE’18 ECCE Europe), pp. 1- 10, 2018
[15] Y. Kawamura, H. Tanaka, K. Suzuki, W. Kitagawa and T. Takeshita, “Consideration of conducted noise reduction on isolated AC/DC converter using SiC devices,” 2017 IEEE 6th International Conference on Renewable Energy Research and Applications (ICRERA), pp. 359-364, 2017
[16] K. Kuwana, Y. Kawamura, W. Kitagawa and T. Takeshita, “Modeling for Conducted Noise Simulation Considering Switching Characteristics on AC/DC Converter,” 2019 10th International Conference on Power Electronics and ECCE Asia (ICPE 2019 - ECCE Asia), pp. 927-932, 2019
[17] W. Kitagawa, T.Kutsuna, K. Kuwana, Y. Kawamura, T. Takeshita, “Conducted Noise Simulation on AC/DC Converter using SiC-MOSFET,” in IEEE Transactions on Industry Applications, vol. 57, no. 2, pp. 1644- 1651, March-April 2021
[18] K. Mitani, W. Kitagawa and T. Takeshita, “Modeling for Conducted Noise on AC/DC Converter by Using Impedance Characteristic,” 2019 22nd International Conference on Electrical Machines and Systems (ICEMS), pp. 1-6, 2019
[19] K. Mitani, Y. Kawamura, W. Kitagawa and T. Takeshita, “Circuit Modeling for Common Mode Noise on AC/DC Converter Using SiC Device,” 2019 21st European Conference on Power Electronics and Applications (EPE ’19 ECCE Europe), pp. P.1-P.10, 2019
[20] W. Kitagawa, K. Mitani, Y. Kawamura and T. Takeshita, “Modeling and Simulation for Conducted Noise on AC/DC Converter Using SiCDevice,” 2019 10th International Conference on Power Electronics and ECCE Asia (ICPE 2019 - ECCE Asia), pp. 1-6, 2019
[21] Line Impedance Stabilisation Network data sheet, NSLK 8126, SCHWARZBECK MESS-ELEKTRONIK OHG, 2021. [online]. Available: http://www.schwarzbeck.de/Datenblatt/k8126.pdf