Design of a serial impingement cooling heatsink for a 30 kW PV string inverter

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Keywords

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Abstract

The design of a cooling solution for a 30 kW string inverter is detailed in this paper. As opposed to traditional solutions, a novel approach has been proposed, consisting of three pinfin copper heatsinks tightly arranged with mutual airflow. This solution has been characterized on a dedicated test bench, partly based on a $T_j(I_{DS},V_{DS})$ TSEP itself precisely calibrated, both being described in this paper. Comparisons between traditional solutions, expected solution, characterized solution, and perspective solutions have been conducted based on the CSPI indicator, reaching up to 34 $W.K^{-1}.L^{-1}$.

Introduction

Historically, Photovoltaic (PV) string inverters have been dedicated to low power installations, central inverters being of use for large-scale PV plants. However, in the recent years, the market of PV string and multi-string inverters has been increasing and these are now installed in a wide range of applications. Initial projects such as domestic production and low/medium power installations (canopies…) have been joined by large scale PV plants in the applications integrating string inverters. Huawei foresees an increase of this trend for the next years [1].

In addition to the increase of efficiency, the reduction of volume is critical for string inverters. Indeed, as these inverters are usually installed on the string frames, a smaller inverter allows saving time and manpower during the installation process, subsequently leading to a cost reduction for the installation. The heatsink being responsible, along with the passive components, of a huge part of the volume of converters, the thermal design of a string inverter has been addressed in this paper. Forced convection with off-the-shelf heatsinks have been considered, and all solutions are compared by using the Cooling System Performance Index (CSPI) [2]. This study is done for a 30 kW string inverter used to connect a 1217 V_{OC} PV array to a three phase 800 V_{LL} grid; the design of the full converter is not detailed in this paper, but for the sake of demonstration is oriented toward highest performances rather than cost management. A two-stage inverter topology has been selected, whose schematic diagram is shown in Fig. 1. Three PV strings of 10.4 kW_C (26 modules of 400 W_C per string) are connected to a capacitive DC bus fixed to 1400 V through a DC/DC stage; a single DC/DC with three paralleled PV strings or a multi-string DC/DC (one independent DC/DC per string) are possible. One 30 kW 3-level Flying Capacitor inverter is used to inject the power from the DC bus to the grid. This paper is focusing on the thermal design of the Flying Capacitor inverter. Regarding the semiconductors, as commercial power modules dedicated to the Flying Capacitor topology of this power range are not yet available, discrete 1200 V / 32 mΩ silicon carbide (SiC) MOSFETs (C3M0032120K from Wolfspeed) have been selected. Analytical calculations of the semiconductor losses to be dissipated are presented in the first section of this paper. The second section will address a comparison of the possible thermal designs. The experimental characterization of the 12 MOSFETs electrical parameters is developed in the third section. Finally, experimental validation of the selected design and perspectives are discussed in the last section.

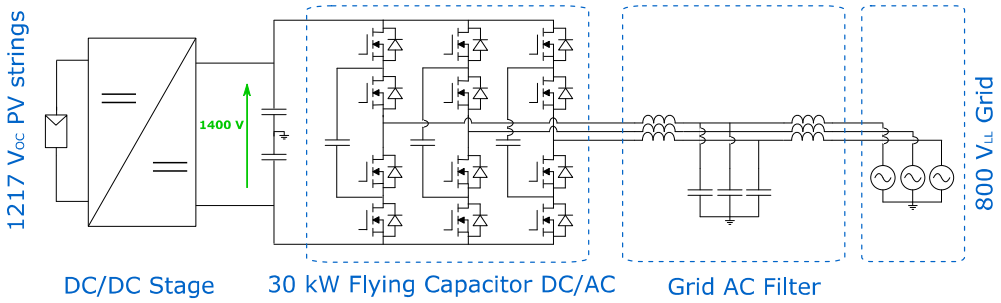


Fig. 1: Diagram of the considered PV inverter, this thermal design regarding its DC/AC stage

I. Analytical calculation of semiconductor losses

In many power electronics applications, semiconductor devices are the major contributors to overall power losses. For that reason, the cooling system must be carefully designed to ensure the safe thermal operation of these devices. However, semiconductor losses estimation is not a trivial problem and needs to be carried out with precision for the future thermal management. Switching and conduction losses estimations are described in two subsections, where both corresponding methods are exposed.

A. Switching losses estimation

The purpose of this subsection is to estimate the semiconductors switching losses. Predicting these losses is no trivial task, since they depend on numerous parameters like the Printed Circuit Board (PCB) and semiconductor packaging parasitics, gate driver circuit, etc. However, some methods derived from the manufacturer's datasheets have been proposed to efficiently estimate these semiconductor losses [3]. Another solution, widely used in literature, is to experimentally test the semiconductor devices by using the Double Pulse Test (DPT) [4]. This method is reliable but time consuming, on top of requiring dedicated and expensive measurement setup, especially for wide bandgap devices. Analytical calculation of losses being faster and easier to implement, this method have been retained in this work.

The flying capacitor voltage is fixed to 700 V (half of the DC bus voltage) to have the same voltage constraints on all MOSFETs; each one will switch a constant voltage of 700 V. Since the switching losses from the datasheet are given solely for 600 V and 800 V, a methodology, detailed in [3], has been used to interpolate the losses at 700 V. This method is quite precise since it considers various commutation mechanisms such as capacitive losses (voltage-dependent) and crossover losses (voltage and current -dependent). As the example in this reference is dedicated to a current source inverter, the equations have been adapted to the Flying Capacitor inverter, where a constant voltage and a sinus-modulated current are switched by the semiconductors. The datasheet's curve representing the switching energy as a function of the switched current is fitted by a second order polynomial equation. The switching energy E_{sw}, calculated over a grid period and for the two reference switched voltages from the datasheet, is calculated by using equation (1); $I_{SW}(t)$ being the sinusoidal grid current given by equation (2). A grid RMS current of 21.65 A per phase is considered with nominal grid voltage.

$$E_{sw}(V_{REFi}, I_{sw}) = \int_0^{T_{grid}} [a.I_{sw}(t)^2 + b.I_{sw}(t) + c]\, dt \quad (1)$$

$$I_{sw}(t) = I_{grid_{RMS}}\sqrt{2}\sin(\omega t) \quad (2)$$

Once the switching energy is calculated for the two voltage references, the switching energy at 700 V is interpolated as proposed in [3]. A switching energy of 137.5 µJ is finally calculated, which, given the 40 kHz switching frequency, yields an estimated 5.5 W of switching losses for each SiC MOSFET.

B. Conduction losses estimation

Regarding the conduction losses, electrothermal coupling has to be considered due to the strong non-linearity of SiC MOSFET R_{DSon} against T_j. Such a temperature consideration was not needed for switching losses calculation of unipolar devices since they are not substantially impacted by the junction temperature. This electrothermal consideration is applied by using equation (3). P_{sw} are the switching losses calculated in the previous subsection, P_{cond} are the conduction losses, $I_{sw,RMS}$ is the RMS current

in one MOSFET, $R_{th,jc}$ is the junction to case thermal resistance of one MOSFET defined in its datasheet (0.45 $K.W^{-1}$) and T_c is the case temperature. To avoid a too high junction temperature of the MOSFETs and in turn to limit their conduction losses and maximize converter efficiency and reliability, the maximum case temperature is defined to be 70°C. The RMS current being the same for all MOSFETs in the Flying Capacitor topology and being equal to $I_{grid,RMS}/\sqrt{2}$ [5], the calculated conduction losses are 8.1 W per MOSFET, regardless of its position. This total of 13.6 W per MOSFET gives a junction temperature of 76°C under these conditions. The total semiconductor losses to be dissipated for the three phases, $P_{SC,3\varphi}$ is therefore 163.2 W. These results are summarized in Table 1.

$$T_j = (P_{sw} + P_{cond}).R_{th,jc} + T_c = \left(P_{sw} + \left(\alpha.T_j^2 + \beta.T_j + \gamma\right).I_{sw,RMS}^2\right).R_{th,jc} + T_c \quad (3)$$

Table I: Results of calculations for SiC MOSFET C3M0032120K from Wolfspeed

Conditions	Per MOSFET	Full inverter (12 MOSFETs)
F_{sw} = 40 kHz	P_{sw} = 5.5 W	$P_{sw,3\varphi}$ = 66.1 W
T_j = 76 °C ; T_c = 70 °C	P_{cond} = 8.1 W	$P_{cond,3\varphi}$ = 97.2 W
V_{DC} = 1400 V ; $I_{grid,RMS}$ = 21.65 A	$P_{SC,1MOSFET}$ = 13.6 W	$P_{SC,3\varphi}$ = 163.2 W

II. Design and comparison of relevant thermal solutions

A. Choices and scope for the heatsink design

As semiconductors packaged in TO-247 have been chosen, the design of the converter's heatsink is quite open, as opposed to the design of a power module-based converter. As a consequence, several types of heatsinks have been considered, with the objective of minimizing the overall volume of the cooling solution, within defined thermal limits. So as to compare these solutions, the CSPI factor of merit, which is inversely proportional to heatsink plus fans volume and to baseplate-to-ambient thermal resistance, will be used. The higher the CSPI is, the higher the heatsink plus fans thermal performances are. Throughout this approach, it has been deemed necessary to retain several criteria that ensure the applicative validity of the designed cooling system.

Regarding the electrical insulation of each device, EN62109-2 standard applies given that the inverter under development is meant for use in PV systems. With the middle point of DC bus linked to heatsinks, the maximum DC voltage to be considered is 700 V (case of TO-247 baseplate being connected to the drain of the MOSFET), leading to a required creepage distance of 3.55 mm. Given the exact package of C3M0032120K, and given available off-the-shelf insulators, a Fischer Elektronik (AOS 218 247) Al_2O_3 ceramic insulator has been chosen, giving 4.6 mm of creepage (3 mm vertically through the insulator's hole, and 1.6 mm radially toward the discrete's baseplate). A thin layer of thermal paste (50 µm of considered thickness) with a thermal conductivity of 10 $W.m^{-1}.K^{-1}$ will be applied both on heatsink-side and on TO-247-side of the ceramic insulator.

It has been previously defined that the MOSFETs case temperature T_c will have to be kept below 70°C. The applicative in-cabinet maximum ambient temperature T_a is considered to be 50°C. These temperature limits and all thermal elements but the heatsinks being henceforth fixed, equation (4) gives $R_{th,sa,3\varphi}$, the allowed equivalent sink to ambient thermal resistance per 12 MOSFETs (forming the three phases). It has been chosen, from experience, to consider an equivalent spreading angle of 60° through the insulator in order to calculate equivalent surfaces receiving the thermal flux. The ensuing three-phases case to sink thermal resistance $R_{th,cs,3\varphi}$ is 32.6 $mK.W^{-1}$. Which, given the total semiconductor losses calculated in section I, $P_{SC,3\varphi}$ = 163.2 W, finally yields a maximum $R_{th,sa,3\varphi}$ of 90 $mK.W^{-1}$. The corresponding $R_{th,sa,1\varphi}$, for a single phase, is of 270 $mK.W^{-1}$.

$$R_{th,sa,3\varphi} = \frac{T_c - T_a}{P_{SC,3\varphi}} - R_{th,cs,3\varphi} \quad (4)$$

In order to restrict the design space, off-the-shelf heatsink references have been solely considered. Their masses are deemed not relevant, as a modern 30 kW PV inverter will generally fall far below the single person lifting limit, therefore allowing both aluminum and copper.

B. Comparison of linear fin and pin fin heatsink designs

Traditionally, for the thermal management of medium power converters, designers use linear fin heatsinks, associated with fans in case of forced convection. Benefits of this linear fin approach include the possible optimization of fins (height, width and spacing), in order to obtain better thermal performances. This type of heatsink relies on air-cooling the fins, which are heated by the baseplate, itself receiving and spreading energy from the components on its opposite side. As the same airflow orientation is applied to fins and to the baseplate itself, and due to fins/baseplate areas ratio, little power is drained directly from the baseplate. Fin thermal resistance is therefore a major contributor of a linear fins heatsink total thermal resistance and can hinder its performances.

An alternative to the usual linear fins heatsinks is known as pinfin, and quite rarely seen in power electronics. This second type of heatsink consists of a baseplate associated with column fins having cylindrical or polygonal base forms. Despite the fans disposition being quite open with this type of heatsink, optimal performances are generally achieved when using an airflow normal to the baseplate. The ensuing impingement effect allows to directly cool the baseplate, on top of cooling the fins, hence benefiting total thermal resistance.

Different thermal designs will now be compared in order to select the optimal design for our application.

The first design, quite classic, represented in Fig. 2.a, consists of reference LAV8-100-12, a 100x188x74 mm cooling aggregate with axial fans (3x 60x60x25 mm) and air buffer from Fischer Elektronik, hosting all three phases. It yields a thermal resistance of 67 $mK.W^{-1}$ according to datasheet values, with a CSPI calculated at 7.5. The total footprint of components (as 12 Al_2O_3 ceramic insulator surfaces) representing 34% of heatsink's baseplate, with 6300 mm^2, this solution is quite sub-optimal in terms of baseplate use.

Another approach with a linear fin heatsink per phase may help respect the criterion of compactness. One design represented in Fig. 2.b consists of W80-45W, an aluminum 80x80x45 mm linear heatsink from Alpha Novatech associated with two 40x40x15 mm fans, results in a thermal resistance of 260 $mK.W^{-1}$ at approximately 16 cfm. This solution matches with the one phase limit of 270 $mK.W^{-1}$ and yields a CSPI of 11.4. In this design, the surface occupation stays sub-optimal, at roughly 33%.

A third solution consists in considering a single pinfin heatsink ref. 3-575725RFA from Cool Innovations, a black anodized aluminum 145x145x63 mm heatsink, which, associated with a slim 120x120x25 mm fan placed normal to the baseplate (in impingement), displays 84 $mK.W^{-1}$ at 75 cfm, and gives a CSPI of 7.0. This solution is represented on Fig. 2.c and has a 30% surface occupation.

A fourth design, depicted on Fig. 2.d, uses a 4-626207U from the same manufacturer, a copper 156x156x18 mm heatsink, with a high performance 120x120x38 mm fan, yields somewhat less than 90 $mK.W^{-1}$ at 200 cfm, and gives a CSPI of 11.3. Its surface occupation is of 26%. In this last design, the fan represents 56% of the cooler volume, as opposed to respectively 13%, 14%, and 21% in designs a, b, and c.

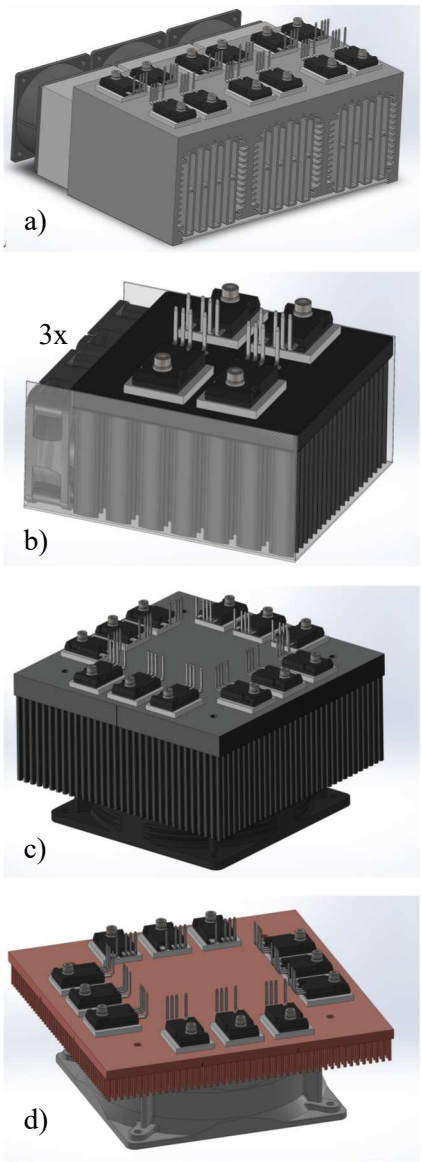


Fig. 2: Four possible designs

The drawback of pinfin heatsinks regarding compactness is therefore mainly their form factor, where the fan roughly matches the greatest surface of the heatsink, leading to lower CSPI and to generally higher fan consumption. To circumvent this drawback, it is proposed in this paper to use pinfin heatsinks in series, where the airflow from the fans benefits more than one heatsink, and where available baseplate surface can therefore exceed fans' footprint by a certain factor. A corresponding structure is proposed in Fig. 4, where each phase of the inverter (4 MOSFETs each) is cooled by one of the three heatsinks. The airflow is full in the central heatsink while it is distributed between the two external ones. Since the airflow gets divided between the two external heatsinks, these are the ones to be considered for the design of the cooling system. In this solution, the airflow is produced by three 38x38x28 mm high performance fans, which at 19 cfm apiece bring the 4-451508U (38x114x20 mm) Cool Innovations copper heatsink to 150 $mK.W^{-1}$, whereas the external heatsinks deliver 280 $mK.W^{-1}$ with the split airflow. The calculated total equivalent CSPI is 35.7, with the fans occupying 31% of the cooler volume. Another drawback however lies in the serial structure of this solution, where on top of being split, the airflow is already preheated when it reaches the external heatsinks. The extent of this issue can be asserted as limited, since a 3x19 cfm airflow absorbing a phase worth of losses (54 W) will undergo less than 2°C of temperature rise.

All of these designs are compared on Fig. 3. Focusing on volume, thermal resistance and therefore CSPI, the last design, in red, seems to be the best option. This innovative solution has various pros and cons, that need to be quantified in order to validate or not the presented theoretical design. This study is presented in section IV of this paper.

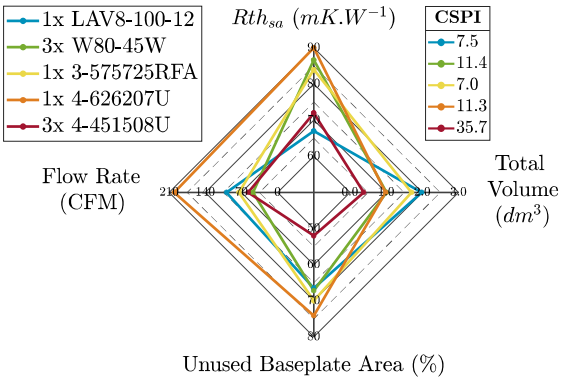
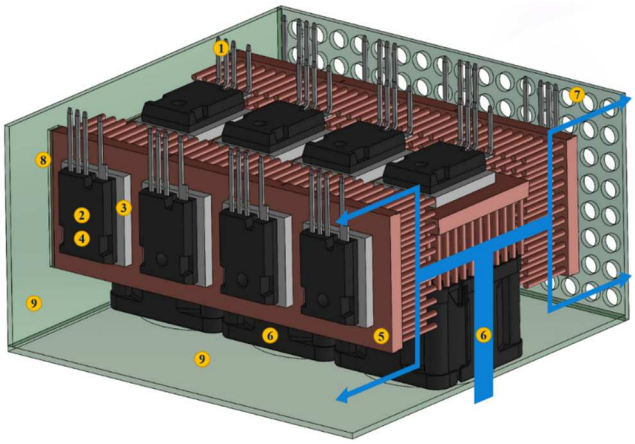


Fig. 3: Radar plot comparison of the five proposed three phases thermal designs



① : All 12 MOSFETs are to be soldered on a single PCB

② : 4 TO-247 MOSFETs are cooled by each heatsink

③ : Each discrete device is insulated from the heatsink by means of an Al_2O_3 plate and screws insulators

④ : The discretes are to be screwed to the heatsinks

⑤ : 3 copper pinfin heatsinks are used (38x114x20 mm, with 363 cylindrical pins of 1.7 mm each)

⑥ : 3 high performance 38 mm fans, sucking air from the bottom of the inverter are used; airflow's distribution is represented in blue

⑦ : Airflow outputs on 2 sides of the inverter

⑧ : Lateral plates, which can be PCBs, support the heatsinks and channel the airflow

⑨ : Components may be placed in hollow areas, flying or soldered on PCBs, to gain space and maximize airflow use

Fig. 4: Overall view and description of the proposed serial impingement cooling heatsink

III. Static characterization of discrete SiC MOSFETs against temperature

A. Junction temperature deduction for discrete power devices

As mentioned before, using discrete power devices gives some flexibility as of thermal management. One difficulty with discrete packages is however die temperature (T_j) estimation, whereas power modules may allow infrared (IR) measurements, or the placement of sensors on dies (or directly include a sensor on substrate, albeit with imprecision). As a result, an alternative method for estimating this parameter must be used. Several workarounds are identified in literature for estimating T_j in discrete devices, [6] summarizes some of these methods. Among those, a commonly cited and accessible approach, with IR measurements, can be ruled off for it is too imprecise with discrete components (measure on top of the package). Another approach, using temperature probes, is likewise ruled off. Temperature Sensitive Electrical Parameters (TSEP) therefore constitute an interesting alternative.

Three distinct TSEP categories can be found in literature, off-line TSEP which implies shutting down the converter, dynamic TSEP where a switching event of semiconductor is necessary (among which the temperature-induced variation of threshold voltage $V_{GS(th)}$), and finally static TSEP under normal operation. This last category, often used in power electronics field, consists in calibrating an electrical parameter of the component which is directly linked with T_j. The most classical static TSEP is the ON-state resistance R_{DSon}. New TSEPs emerge regularly in literature, where these continue to be compared against physical measurements [7]. Some authors emphasize the fact that static TSEPs require very precise calibration, which entails the development of dedicated test benches and of the ensuing characterization campaigns.

Whereas T_a can be directly measured at the inlet, it has therefore been chosen to deduce T_j from a TSEP, among which R_{DSon} is the best candidate for it is easily measurable and is highly sensitive against junction temperature [8]. Despite this TSEP being often described as subject to strong deviations depending on the measurement setup [9], it has been evaluated that in this static characterization, it would be possible to account for lead resistances and to set in place very precise measurements of V_{DS} and I_{DS}, in turn yielding precise R_{DSon} values. A characterization of this TSEP has therefore been conducted for each of the 12 MOSFETs of our setup. The corresponding test bench and experimental results are presented in the next sub-section.

B. Development of a test bench and presentation of experimental results

In order to assess the R_{DSon} change against T_j and I_{DS}, an accurate test bench has been developed and applied to the components that will be used during thermal characterization and final converter operation. Its purpose has been to calibrate this TSEP and secondly to quantify intrinsic differences between components. Using MOSFETs in a low $d(R_{DSon}/T_j)$ portion of their characteristic, underlines the necessity of very precise calibration, since the smallest increment in resistance value induces a substantial difference in junction temperature. Characterization test bench consists in measuring $R_{DSon}(I_{DS})$ with a high accuracy Keysight B1506A power device analyzer. During the measures, the 12 MOSFETs are placed in a custom enclosure both highly thermally capacitive (high inertia) and highly isolated (thermally) to regulate very precisely and homogeneously their temperature at several values of interest. Fig. 5 presents a synoptic diagram of the developed test bench, where one copper bar hosts the 12 MOSFETs on its upper face, and is heated on its bottom face by power resistors. Type K thermocouples and PT100 Resistance Temperature Detectors (RTD) are distributed on several locations in the enclosure (on copper bar, on packaging of MOSFETs, on power resistances, etc.), and are used to monitor temperature and regulate it thanks to power resistors.

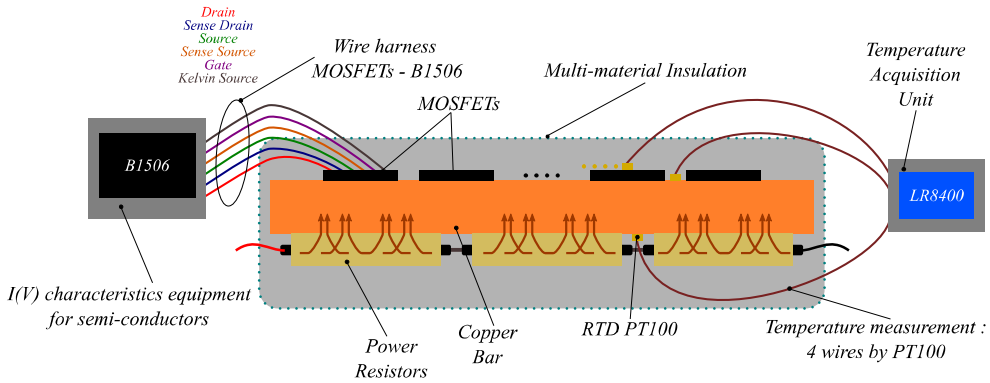


Fig. 5: MOSFETs static characterization against temperature test bench and description

This custom setup allowed the static characterization of the 12 MOSFETs at eight different temperature points, each regulated with a deviation lower than 1°C between probes. That, combined with the low duty cycle of current pulses (100µs pulses separated by 100ms pauses) which leads to negligible die self-heating, allows us to conclude that copper bar and die temperatures are nearly identical. This calibration has then been put into equations thanks to an interpolation between T_j, R_{DSon} and I_{DS}. The implementation of equation (5) in an optimization algorithm minimizing the 12 variables in orange provides the results of Fig. 6. With an average error on all 12 MOSFETs of 0.83°C (and a max of 3.35°C)

between experimental measurement and optimization results, interpolation of $T_j(V_{DS},I_{DS})$ is deemed correct. Another technique, not detailed in this paper, based on 4th order bi-polynomial interpolation gave approximately the same results regarding differences on measured points, but its highly dynamic behavior between points led us not to retain it.

$$T_j = a + b(R')^d + (e + f.R')I_{DS}^{(g+h.R')} + (i + j.R')I_{DS}^2 + k(R'.I_{DS})^l \text{ ; with } R' = R_{DSon} - c \quad (5)$$

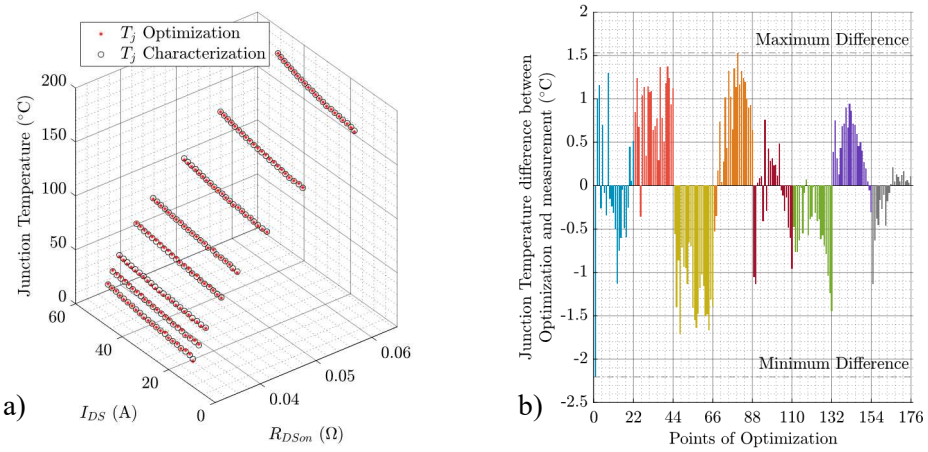


Fig. 6 : a) 3D plot results of static characterization and optimization algorithm for MOSFET no. 1 and b) residuals between characterization and optimization results for this MOSFET

IV. Thermal characterization of the serial impingement cooling solution

A. Presentation of the thermal characterization test bench

The thermal characterization of the presented cooling solution is based on the precise evaluation of the effective junction to ambient thermal resistance of the assembly, under nominal power and under augmented power. The required thermal flux is generated through the injection of a chosen DC current through the 12 MOSFETs temporarily placed in series. This current is chosen, and later adjusted, to be representative, once multiplied by each measured V_{DS}, of the per-MOSFET losses calculated in section I. Electrical properties of each MOSFET are measured using precise equipment, 34465A Keysight digital multimeters for voltages, with an added Burster precise shunt for I_{DS}. Several power supplies are used for generating the constant current (thermal flux), the PWM and power supply of fans, and the insulated gate supplies. The mechanical and electrical design of the thermal assembly, not detailed in this paper, is to be kept for the final converter. It is based on PCBs on all 6 sides : the upper PCB provides the connection of the 12 MOSFETs (in series here), the bottom PCB hosts the fans, and lateral PCBs either insure the connections between upper and lower PCBs or act as an IP2x air outlet. This test bench is described in Fig. 7 below.

① : IR camera
② : 20V-38A power supply
③ : MOSFETs control and V_{DS} measure selection daughter board
④ : Pressure measurements daughter board
⑤ : Fans PWM control and speed measurement daughter board
⑥ : Acquisition units for temperature probes
⑦ : Precision multimeters
⑧ : Hot air exhaust ducts
⑨ : Precision shunt for I_{DS} measurement
⑩ : Arbitrary waveform generator for PWM generation
⑪ : Thermal solution under characterization, based on 6 PCBs of 1.6mm-thick FR4 :

- Top PCB, 4-layer : 70µm external and 35µm internal;
- Lower PCB, 4-layer : 70µm external and 35µm internal;
- Front/back PCBs, 2-layer : 35µm;
- Lateral PCBs, not plated.

Fig. 7: Thermal characterization test bench for the proposed cooling solution and its description

In order to perform the chosen thermal characterization, and to avoid thermal runaway, several steps have been sequentially followed. Fans are powered and adjusted, MOSFETs are turned ON with V_{GS}=15V, DC current is injected and precisely adjusted with respect to equation (6) at thermal equilibrium, where the values of generated thermal flux are respected with a tolerance of 1‰ with respect to Table II. As the design has been constrained by restrictive ambient temperature and efficiency objectives (described in first sections), it becomes possible to carry out additional qualifications at augmented power (x times nominal injected power is denoted xPIn), which in turns should bring more precision to the calculations through the amplification of the thermal gradients. The 4 thermal fluxes are combined with 3 fan speeds (20, 50, 100%) to produce 12 possible campaigns (within safe limits).

Table II: Thermal flux level for thermal characterization

Naming	Values (in W)
0.5PIn	81.6
1PIn	163.2
2.1PIn	326.4
4PIn	571.8 to 649.2 (limits apply)

$$B_1 < \sum_{i=1}^{12} V_{DS_i} * I_{DS} < B_2 \; ; \; B = \begin{bmatrix} xPIn * (1 - 0.001) \\ xPIn * (1 + 0.001) \end{bmatrix} \quad (6)$$

B. Experimental results of the thermal characterization

As described in the previous sub-section, the main objective of this characterization is to obtain the thermal resistances of the cooling solution. Deducing these is however quite complex due to the disposition of the 12 MOSFETs on 3 partly-serial heatsinks. Our method consists in calculating 12 thermal resistances, each regarding a slice (from die to inlet air) of the cooling solution. Each slice can be different, the measures being carried out under nominal and therefore naturally (un)balanced thermal flux: i.e. a thermal resistance is calculated for each slice through the die-inlet ΔT and the die-injected power (V_{DS} times I_{DS}) whatever the thermal behaviour below. Each phase (a heatsink) is therefore composed of 4 slices (albeit different), and phase thermal resistance can easily be deduced. In this approach, T_j is estimated with the TSEP previously defined and inlet temperature is calculated according to equations (7) and (8) where Q represents the total airflow.

$$T_{air,in,heatsink_{center}} = T_{air,in,fans} + \frac{P_{fans}}{Q * C_{v,air}} \quad (7)$$

$$T_{air,in,heatsink_{lateral}} = T_{air,in,heatsink_{center}} + \frac{P_{center\ phase}}{Q * C_{v,air}} \quad (8)$$

All thermal boundaries and electrical values of interest being obtained, and using datasheet's value for $R_{th,jc}$ and previously calculated value for $R_{th,cs}$, it is now possible to calculate the equivalent thermal resistance per phase (per heatsink) based on equation (9).

$$R_{th,sa,1\varphi} = \left[\sum_{i=1}^{4}\left(\frac{1}{R_{th,sa_i}}\right)\right]^{-1} = \left[\sum_{i=1}^{4}\left(\frac{V_{DS_i} * I_{DS}}{T_{s_i} - T_{air,in,heatsink}}\right)\right]^{-1} \quad (9)$$
$$\text{where } T_{s_i} = T_{j_i} - \left(V_{DS_i} * I_{DS}\right) * \left(R_{th,jc} + R_{th,cs}\right)$$

Fig. 8 presents experimental results for impingement-oriented airflow, for one example MOSFET (no. 1), with a plurality of thermal fluxes (0.5PIn to 4PIn along graph's X-axis) and fan speeds (100%, 50%, 20% in resp. blue, green, yellow) as described in the previous sub-section. On top of the trivial observation of the reduced thermal resistance with an increasing airflow, a remarkable thermal behaviour can be witnessed. As depicted by the fitted non-linear curves, there is a decrease of $R_{th,sa,MOS1}$ when the injected power increases (at constant airflow). For instance, $R_{th,sa,MOS1}$ decreases by 20% with a doubled fan speed (50% to 100%) at 1PIn, but it also increases again by 52% with half the injected power (1PIn to 0.5PIn) at 100% speed.

This behaviour has yet to be thoroughly analyzed, as no clear explanation emerges. Indeed, the whole assembly is constituted of solid elements, measures have low tolerances, and usual parasitic phenomena (additional convection, radiative exchange…), even with exaggerated scopes, may not produce this much of an effect. Several leads are explored, such as an adverse effect of impingement, where strong airflow turbulences appear between fins, and might have a non-linear behaviour against temperature.

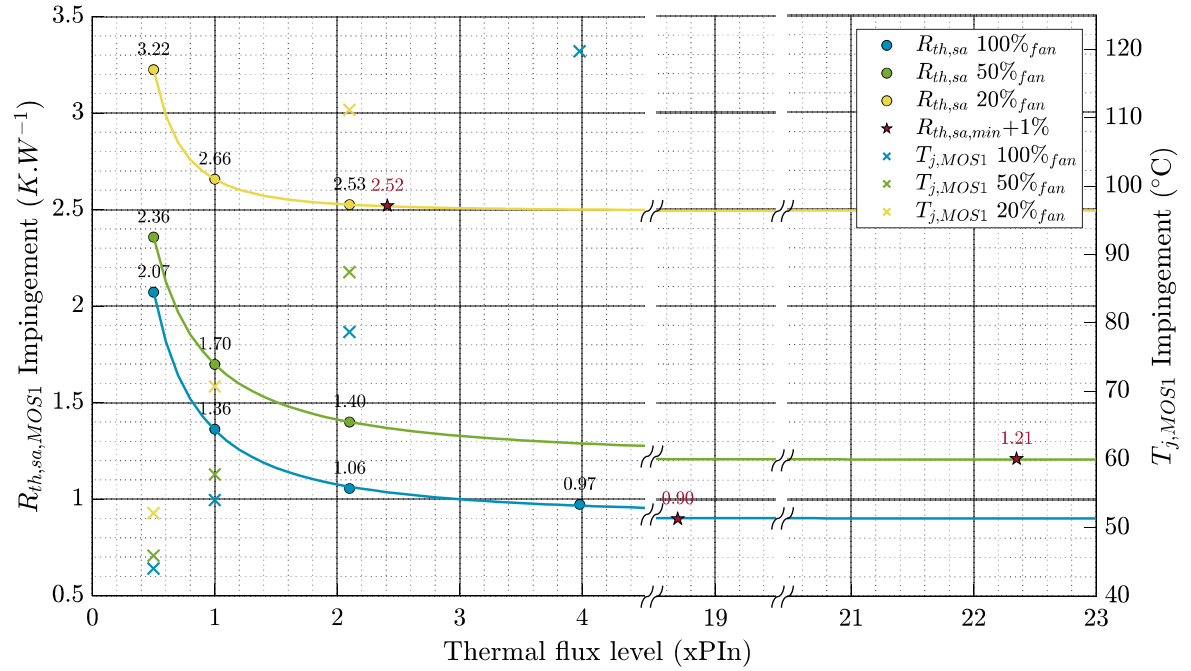


Fig. 8: Experimental results for MOSFET no. 1: $R_{th,sa}$ and T_j against injected power for three airflows

In the meanwhile, it has been chosen to study this system with regard to its asymptotic performances (injected-power-wise). The corresponding thermal resistances are depicted with red stars, at 1% above the asymptote of fitted functions of $R_{th,sa,MOS1}$ against injected power for each fan speed. These extrapolated values are reached for 2.5PIn to 22PIn (caused by the choice of only 1% above minimum).

Albeit solely shown for MOSFET no. 1, the above results are similar for the others. Fig. 9 illustrates the equivalent thermal resistances for each heatsink of the structure, obtained with equation (9). The color code is kept for the fan speeds, and the spreads of thermal resistances between the three heatsinks are illustrated with different markers (the difference between the best and the worst heatsink being shown). The asymptotic performances are also depicted on the right, whatever the actual value of PIn_{max}.

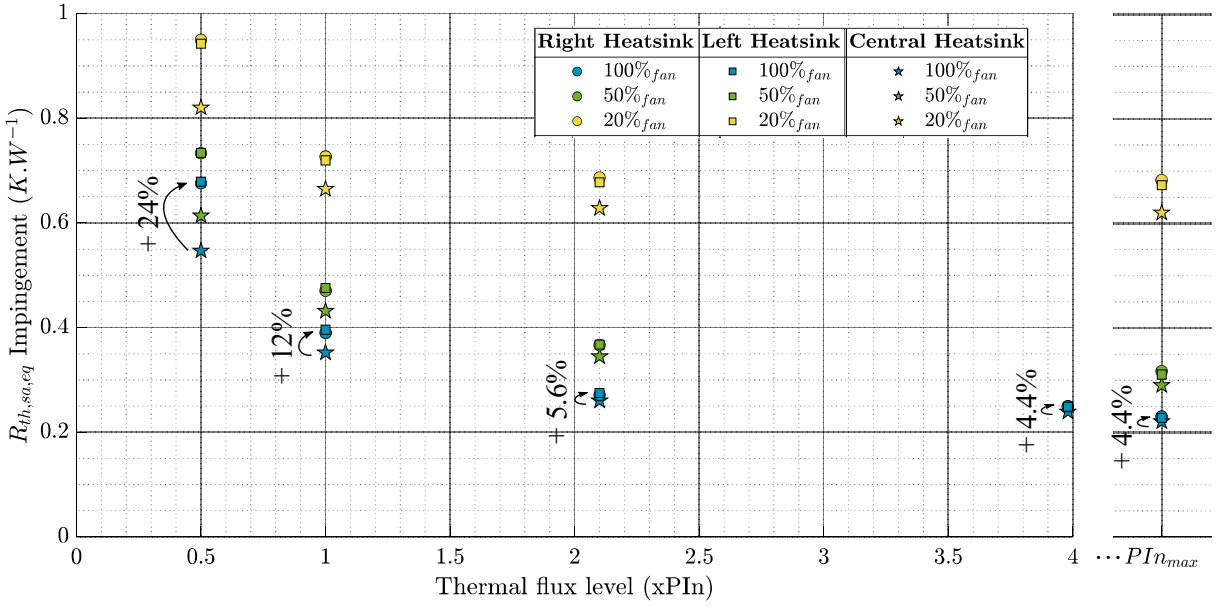


Fig. 9: Experimental per-phase results: Rth,sa,1φ against injected power for three airflows

In order to compare these experimental results to the theoretical design, we can refer to Table III which shows the corresponding per-phase thermal resistances. One can see that the central heatsink does performs better than the outer ones, albeit with a lower difference than expected. Indeed, even with half

the airflow, the added $R_{th,sa,1\varphi}$ on lateral heatsinks is of +12% at PIn and of +4% asymptotically, against the +87% that was expected in theory. This difference might be explained by the simplified approach used in subsection II.B. Indeed a halved airflow has been considered to be applied on the whole surface of each outer heatsink, but in reality each sees a concentrated airflow on part of its surface (an average of 7.3 $m.s^{-1}$ on 42% of baseplate surface, see assembly on Fig. 4). This surface hosting the MOSFETs (in the middle of heatsink's height), and pinfins being aligned between heatsinks, it is probable that this lower-than-expected difference emerges from a better-than-expected use of the halved airflow.

Table III: Thermal resistances and CSPI : theoretical, experimental and asymptotical results

In $mK.W^{-1}$ at 100% airflow	$R_{th,sa,1\varphi,theory}$	$R_{th,sa,1\varphi,1PIn}$	$R_{th,sa,1\varphi,asymptotic}$
Central Heatsink	150	352	221
Right Heatsink	280	390	231
Left Heatsink	280	396	228
Total CSPI	35.7	20.8	34.2

The experimental thermal resistances themselves stand higher than expected, with an excess of 39% to 135% at 1PIn compared to theory. The corresponding CSPI, adapted to multiple-heatsinks systems, is computed at 20.8 as indicated on Table III, standing 42% lower than its theoretical counterpart. It can however be highlighted that the asymptotical values are closer to our expectations, nay exceed them with a nearly perfect balance between all three heatsinks, in turns yielding a CSPI of 34.2, on par with theory. Reaching sufficiently low thermal resistances (and high CSPI) could involve obvious solutions such as increasing the airflow, or could focus on the asymptotic approach, an increase in thermal flux level having been shown to benefit thermal performances. However it also leads to higher junction temperatures and subsequent low efficiencies, which highlights the existence of an optimum between thermal system performances and inverter performances. Our scope for this design might well be too efficiency-oriented (with ensuing low losses) to fully benefit from this cooling system design.

Whereas the higher-than-expected performances of lateral heatsinks have already been detailed, the underperformances of the central heatsink conjure several leads, related to airflow inhomogeneity and turbulency or to power sources repartition. Both airflow problematics would be caused by the high-performances fans (with large hubs and high swirl) and might be hindering heatsink's performances by providing airflow solely to certain sections of it, which airflow might also not be normal to the baseplate thence creating more turbulence along pinfins. This could be solved by inserting an air buffer between fans and fins, in the form of a box with internal features, which could both allow airflow to spread below the hubs and straighten airflow's direction (the CSPI would be impacted by the augmented volume and the potentially reduced thermal resistance). The discrete repartition of power on baseplate's surface brings to the table the spreading contribution to the thermal resistances, which has been neglected in section II for lack of information. Potential countermeasures would include convection spreaders (the copper baseplate being already an excellent conductor), such as caloducs (placed along heatsink's length) or vapor chambers (covering the heatsink); or could include those consisting in using the free surfaces of the heatsink by bringing thermal fluxes from other components (capacitors or inductors).

Conclusion

The design of a cooling system for a Flying Capacitor inverter dedicated to PV applications has been described in this paper. After an estimation of switching and conduction losses of the topology, different thermal designs have been presented and compared, mainly based on CSPI figure of merit. A novel structure, based on a serial arrangement of pinfin heatsinks, has been proposed and characterized. In order to deduce thermal resistances through a precise estimation of die temperatures, a static characterization of a MOSFET TSEP has been conducted on a custom test bench. The cooling solution has been characterized on a dedicated test bench representing the real converter layout, at real and augmented thermal fluxes from the MOSFETs. Results have been discussed based on the satisfaction of each criterion and perspectives have been proposed for current drawbacks. In particular, it has been highlighted that although quite insufficient at nominal power, the asymptotic performances of this cooling system are up to our initial expectations, and could be well suited to another design scope, with higher losses to dissipate.

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