Verification of GaN-HEMT Spice Models Using an S-parameters Approach

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Keywords : « Gallium Nitride GaN», « Wide band gap », « Parasitic elements », « S-Parameters », « Transmission line », « Spice model», « De-embedding »

Abstract

This paper describes a complementary S-Parameters approach to verify the Spice model accuracy of power GaN-HEMT devices regarding their capacitive and inductive aspects represented in graphic Smith charts. This approach correlates the Smith charts of experimental and simulated results in order to provide insights to improve the model characteristics. The correlation is carried out by processing the experimental results and the Spice simulated data using the Smithplot Python library. Additionally, a complementary study considers the input and output reflection coefficients to stablish a connection between the measured and simulated parameters in frequency and voltage. Possibilities of dissociating both package parasitic elements and intrinsic GaN capacitances confirm the potential of S-parameters as a powerful tool for model verification and study of power GaN-HEMT devices using a radio-frequency approach.

1. Introduction

Current development of power GaN-HEMT devices has increased the performance of power transistors in the frequency domain [1]. Therefore, promising perspectives forecast a new generation of power converters with significant increase of the switching frequency at level of megahertz [2]. Therefore, the power electronics knowledge progressively requires complementary radio-frequency methodologies in order to facilitate the design of power converters based on GaN-HEMT [3]. In addition, given the high switching frequencies achieved by these power electronic devices, the parasitic elements associated to the package and the GaN-HEMT intrinsic capacitances are gradually fundamental in the design process [4]. In this context, verification of Spice models trends to be challenging given the high frequency phenomena and the interaction of the GaN-HEMT with their experimental setup [5]. Indeed, parasitic elements of test boards are not easily dissociable of the package parasitic elements and the device intrinsic capacitances [6][7]. Therefore, we propose through this paper a frequency domain methodology to partially verify GaN-HEMT Spice models by means of S-parameter simulations and measurements. Additionally, study results provide insights about the behavior of these power devices in a wide range of voltage and frequency.

The proposed approach begins with the design and characterization of the PCBs for the test fixtures, calibration standards, and Bias Tees. Then, a simplified model is implemented in Spice using a transmission line approach and the S-parameters measurements from test fixtures and the calibration standards. After, passive elements with accurate values are used to adjust the modeled test bench. Finally, considering several bias voltages, the experimental S-parameters from the GaN-HEMT test setup are compared with the associated Spice model. Given the S-parameters, a graphical comparison using Smith charts brings evidence about the Spice model performance regarding the capacitive, resistive and inductive aspects. These results highlight the potential of S-parameters to define and consequently improve the model accuracy using a methodology that requires a hardware and software low demanding to implement.

This document is organized as follows. Section 2 describes the proposed methodology based on S-Parameters. Section 3 explains the experimental setup and discusses the comparison results. Finally, conclusions and perspectives are reported.

2. Methodology for model verification using S-parameters

This section describes the proposed methodology to verify GaN-HEMT models using S-parameters. The focus of this approach is to use a conventional Spice simulation tool and measurements from a Vector Network Analyzer (VNA). Our proposed methodology based on S-parameters aims to provide insights about the model performance in the frequency domain using basic test boards modeled and characterized for further simulation in a well-known simulation tool in power electronics.

The S-parameters or Scattering parameters describe the electrical behavior of linear electrical networks when electrical signals propagate on it [8]. Two-port S-parameters are defined by considering a set of voltage traveling waves. When a voltage wave from a source is incident on a network, a portion of the voltage wave is transmitted through the network, and a portion is reflected back toward the source. Figure 1 shows a simplified diagram for S-parameters definition [9].

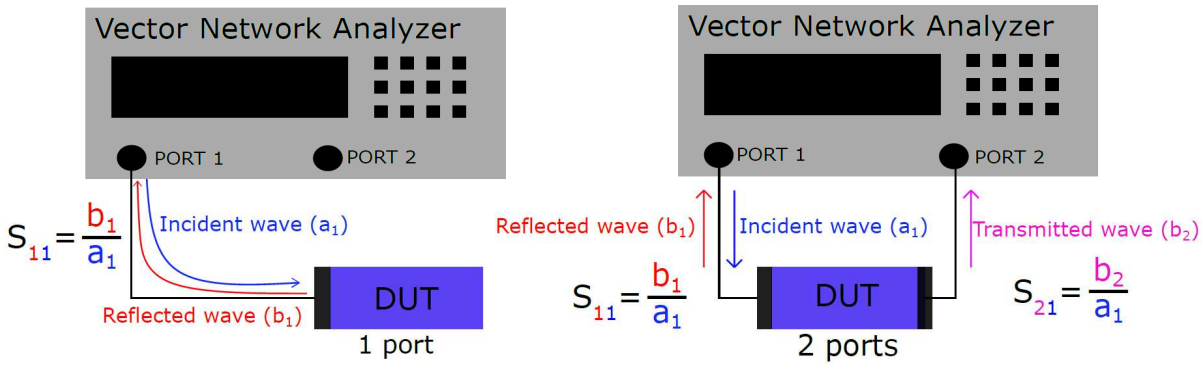

Fig. 1: S-parameters description

The relation between a_i and b_i (for i=1,2) can be written as a system of linear equations (see eq.(1)).

$$\begin{aligned} b_1 &= S_{11}a_1 + S_{12}a_2 \\ b_2 &= S_{21}a_1 + S_{22}a_2 \end{aligned} \tag{1}$$

Using VNA measurements, the physical meaning of S_{11} is the input reflection coefficient Γ_{in} with the output of the network terminated by a matched load ($a_2 = 0$). S_{21} is the forward transmission from port 1 to port 2. S_{12} is the reverse transmission (port 2 to port 1) and S_{22} is the output reflection coefficient Γ_{out}. From definition of the input reflection coefficient Γ_{in} and eq.(1), the relation between the S-parameter S_{11} and an unknown impedance Z_L connected to the generator of source and characteristic impedance Z_0 can be calculated using eq.(2).

$$S_{11} = \frac{b_1}{a_1}\Big|_{a_2=0} = \Gamma_{in} = \frac{Z_L - Z_0}{Z_L + Z_0} = \frac{Z-1}{Z+1}, \quad thus \quad S_{11} = \frac{Z-1}{Z+1} \tag{2}$$

$$where \ Z = Z_L/Z_0 \ is \ the \ normalized \ impedance \ and \ Z_0 \ is \ the \ characteristic \ impedance, ie. Z_0 = 50\Omega$$

As deduced from eq.(2), S-parameters can be transformed directly into equivalent normalized impedances. Therefore, many electrical properties of the Device Under Test (DUT) (such as inductance, capacitance, and resistance) may be expressed and studied using these parameters. Indeed, two-port S-parameters and the associated impedances can be traced on a Smith chart using polar co-ordinates for graphical analysis. Additionally, a set of S-parameters covering a wide range of frequencies and depicted on a Smith chart can be used to visually represent how capacitive or how inductive is an electrical network across the defined frequency range. Next, we describe the proposed methodology to verify Spice models of power GaN-HEMTs using and S-parameters approach.

Figure 2 depicts the proposed steps for the verification of GaN-HEMT Spice models using the S-parameters approach. In the first step, the PCB layout of the test fixture boards are designed for a characteristic impedance Z_0=50Ω. In addition, two calibration standards [6], Open and Thru, are designed to extract the equivalent C and L of each PCB trace using the definition of characteristic impedance in eq.(3).

$$Z_0 = \sqrt{\frac{L}{C}} \tag{3}$$

Second step aims to provide a simplified model of the PCBs traces by means of Pi networks to model them as transmission lines. This model is based on C and L parameters that are respectively measured from Open and Thru calibration boards. Furthermore, a resistive element R is added to compensate for an identified resistive offset measured by the VNA. The extraction of these parameters is a primordial step before applying the De-embedding on the device S-parameters.

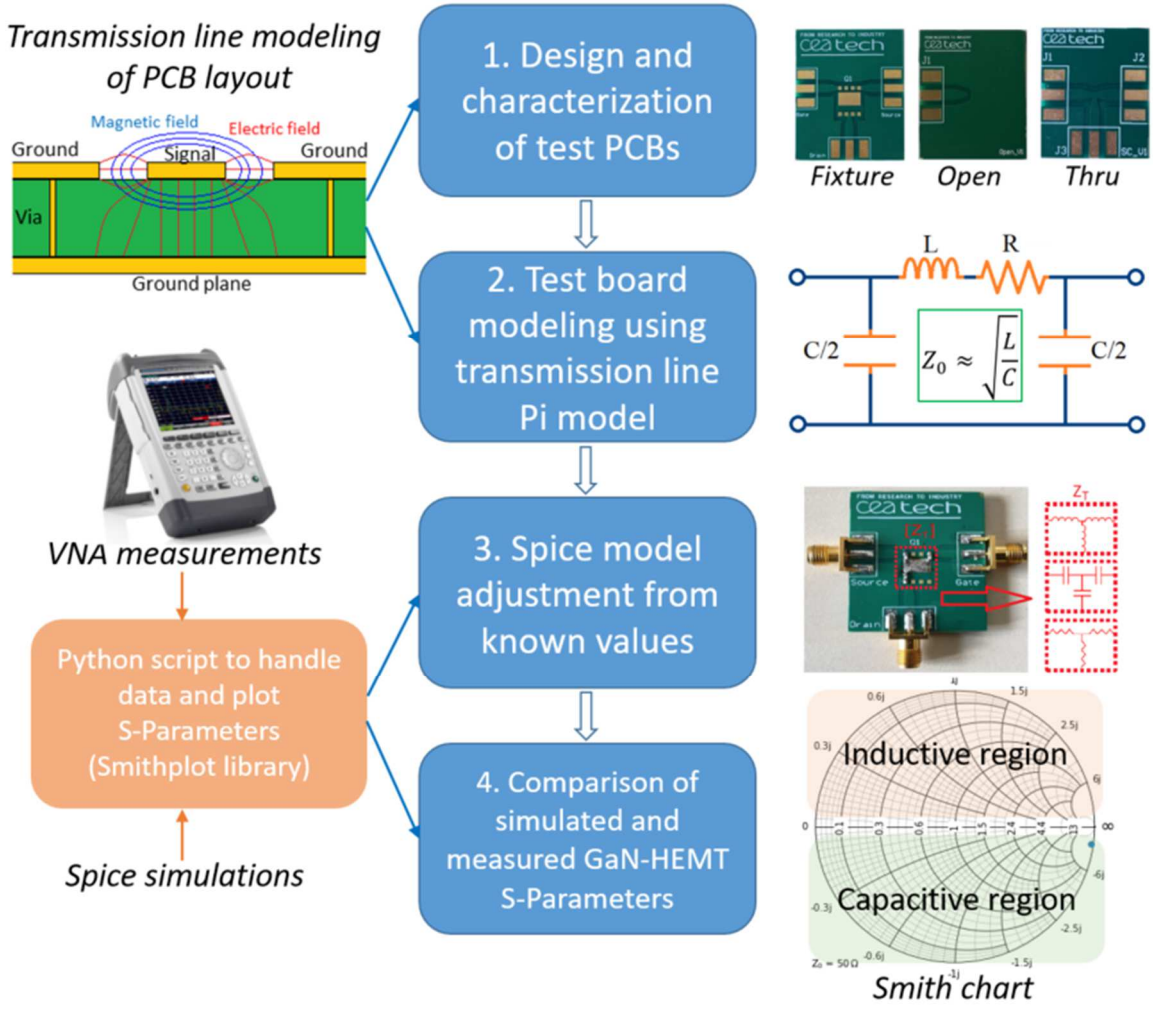

Fig. 2: Steps for power GaN-HEMT Spice model verification using S-parameters

The third step implements the simplified model of the fixture test board in a Spice simulation tool. Before measuring the GaN-HEMT S-parameters in the experimental setup, a calibration stage provides a fine adjustment of the Spice model using precision passive elements connected in a star configuration. Additionally, third step includes a characterized short circuit model to connect the Source terminal to ground. This configuration with unconnected Source terminal was selected given the flexibility to design several fixture test boards for different GaN-HEMT device footprints. Figure 3 shows details of the Pi networks used to model the PCB effect at the DUT accesses. The fixture test board of Figure 3 is designed according to guidelines proposed in [10].

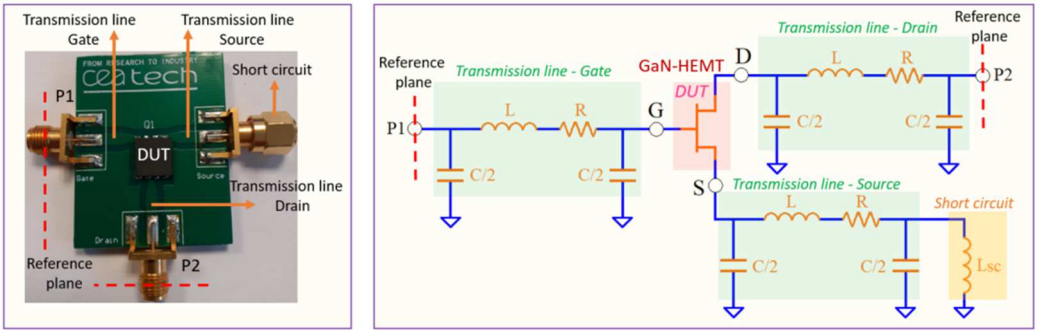

Fig. 3: a) Fixture test board b) Simplified model of fixture text board using Tline Pi model

In the fourth step, the S-parameters of the GaN-HEMT under test are measured using the test fixture board connected to a VNA. To do the same measurements for different biasing voltages for V_{DS} from 0V to 400V, the designed Bias Tees are connected between the test fixtures and the VNA on gate and drain accesses (as shown in Figure 4) [9]. This stage provides measurements of S-parameters in the Touchstone format which are processed using a Python script. The Python script is used to apply the de-embedding techniques on the device measured data after measuring the parameters of the calibration standards. These data joined with the simulated data are plotted using the Python Smithplot library in the Smith chart for a graphical comparison [11]. The comparison results bring evidence about the Spice model performance in the frequency domain regarding the capacitive, resistive and inductive aspects for several biasing voltages. Finally, conclusions would potentially lead to model validation and/or improvements.

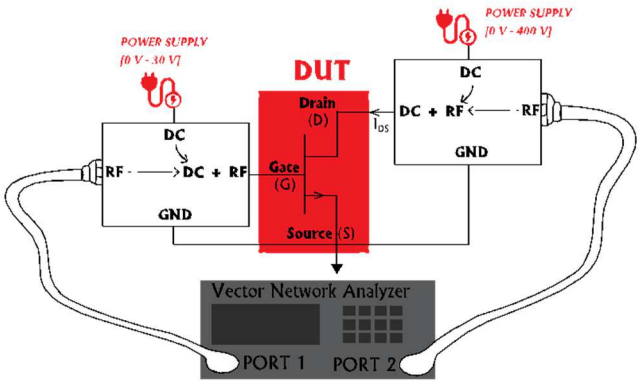

Fig. 4: Test bench schematic for S-parameters measurements under biasing voltages (V_{DS} from 0V to 400V)

3. Experimental results

This section shows the experimental and simulation results of comparing two GaN-HEMT devices from different commercial vendors using the proposed approach. The vendors are named Vendor 1 and Vendor 2. Additionally, the evaluated Spice models are available from the websites of each manufacturer. The experimental setup for this reported work uses as a main measurement equipment a VNA Rohde & Schwarz ZVH8 option ZVH-K42. Table I lists the configured setup parameters. In order to keep uniformity, the Spice simulation and the VNA are configured with similar setup parameters.

Table I: VNA parameters for all measurements

Parameter	Value
Start frequency	1MHz
Stop frequency	1GHz
Number of points	801
Tracking generator power	0 dBm
Resolution bandwidth	300Hz
Sweep time	4s
Characteristic impedance	50Ω

As a general description and following the connection ports, the parameter S_{11} is mainly associated to the loop around the Gate-Source terminals, the parameter S_{22} is mainly associated to the loop around the Drain-Source terminals, and the parameter S_{21} is mainly associated to the trajectory involved by the Gate-Drain terminals.

Figures 5 and 6 show that model provided by Vendor 1 is relatively close of experimental results in a wide range of frequencies and bias voltages of the transistor in OFF state (blocked canal: $V_{gs}<V_{th}$). Figure 7 confirms the tendency of intrinsic device capacitances to decrease when the V_{DS} voltage increases given the smaller curves into the Smith chart. However, the difference between experimental and simulation results in Figure 7 could be associated either to the model accuracy or potentially to the trapping effect caused by the sweep time not considered in the Spice approach. Figure 8 depicts the signal transmission through Gate-Drain terminals with a suitable impedance adaptation at high frequencies as expected. Therefore, this result agrees with a suitable modeling of the intrinsic capacitance C_{GD}.

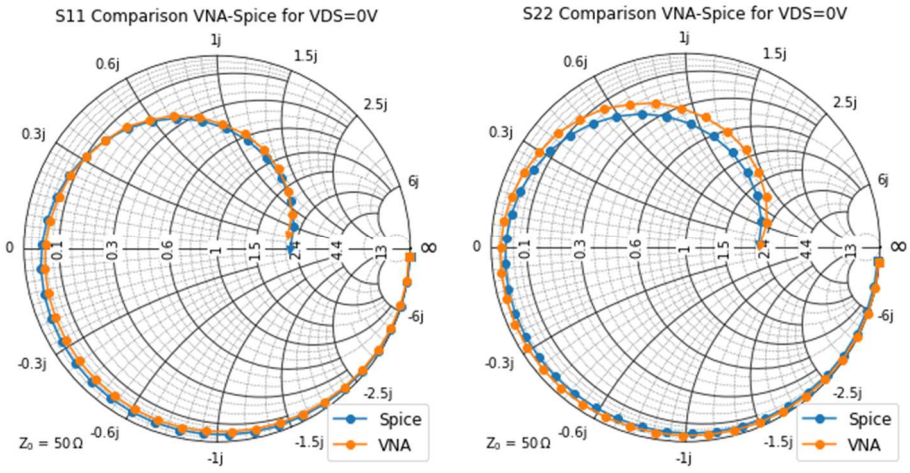

Fig. 5: S_{11} and S_{22} parameters for V_{DS} = 0V. Vendor 1.

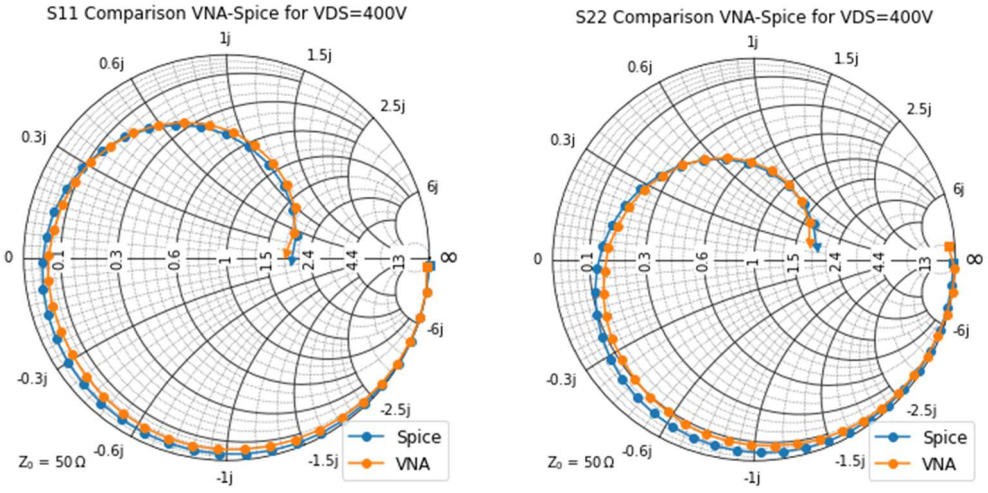

Fig. 6 : S_{11} and S_{22} parameters for V_{DS} = 400V. Vendor 1.

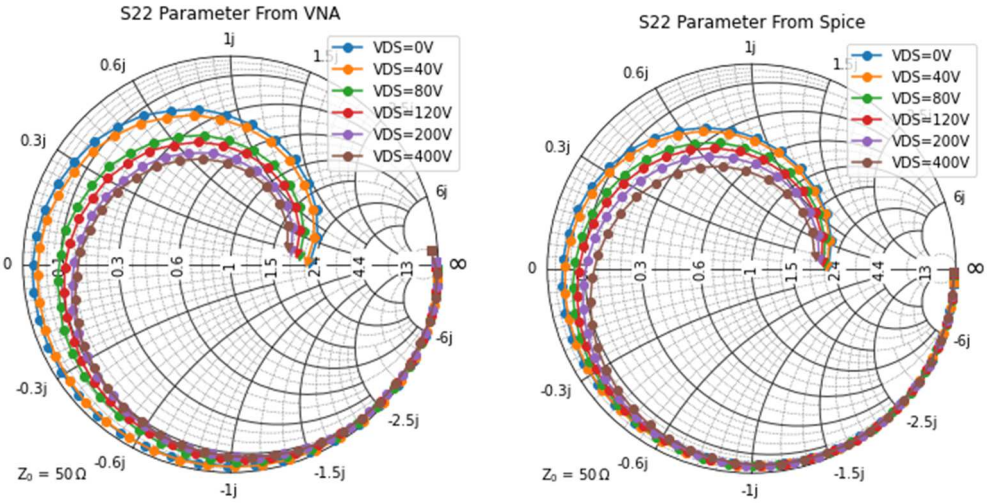

Fig. 7 : S_{22} parameter for several V_{DS} voltage. Vendor 1.

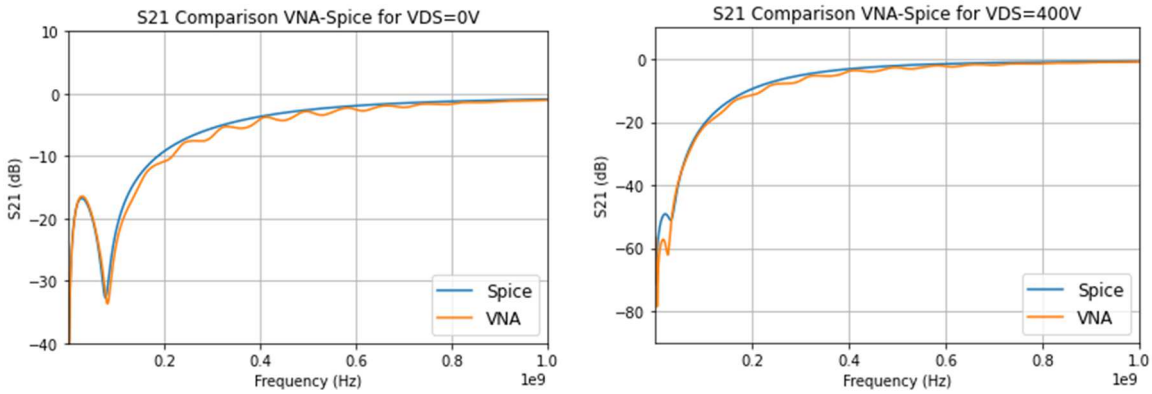

Fig. 8 : S_{22} parameter for V_{DS} = 0V and V_{DS} = 400V. Vendor 1.

In contrast, experimental and simulated results for parameter S_{11} in Figure 9 and Figure 10 show some notorious differences in model provided by Vendor 2. Indeed, some capacitive aspects could be potentially improved in the associated C_{GS} capacitance. Furthermore, the inductive effects could be improved by reducing the length of the transmission lines from the SMA connectors to the DUT accesses to increase the test setup accuracy. Figure 11 illustrates the model performance for parameter S_{21} with a suitable behavior for the C_{GD} capacitance model.

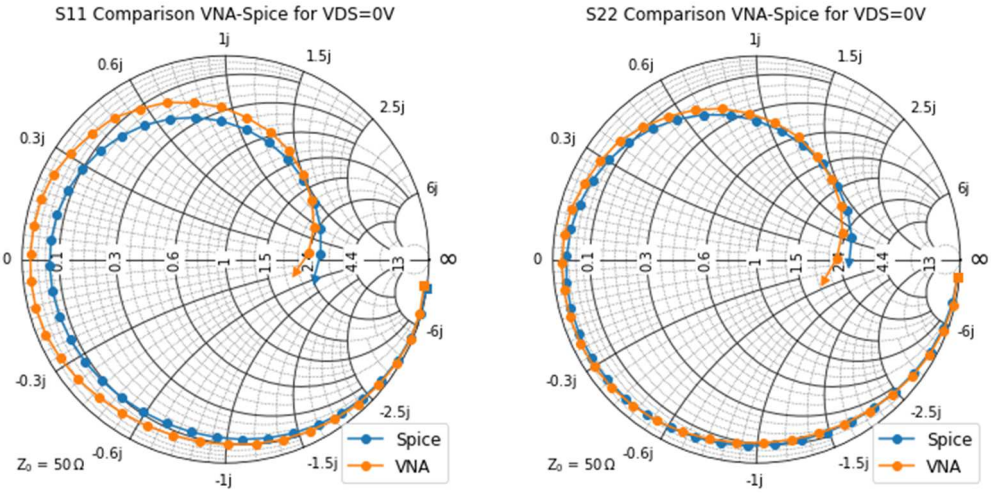

Fig. 9 : S_{11} and S_{22} parameters for V_{DS} = 0V. Vendor 2.

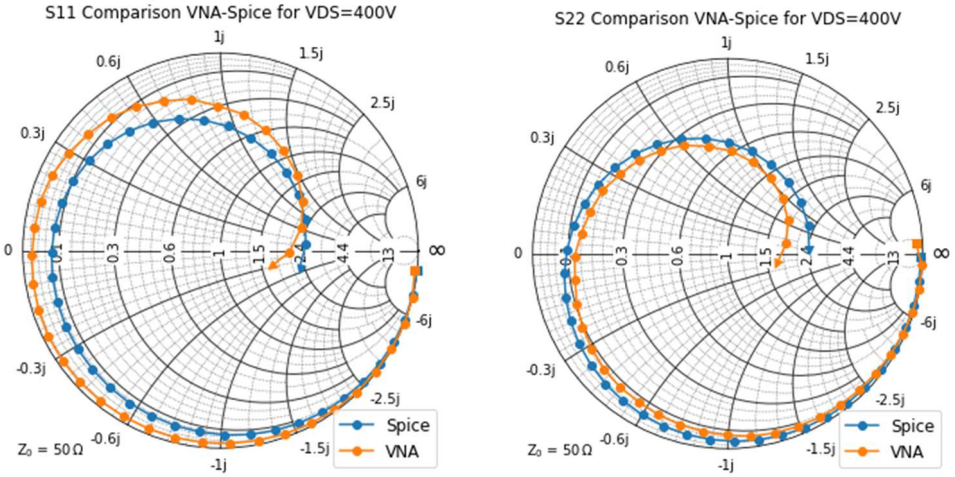

Fig. 10 : S_{11} and S_{22} parameters for V_{DS} = 400V. Vendor 2.

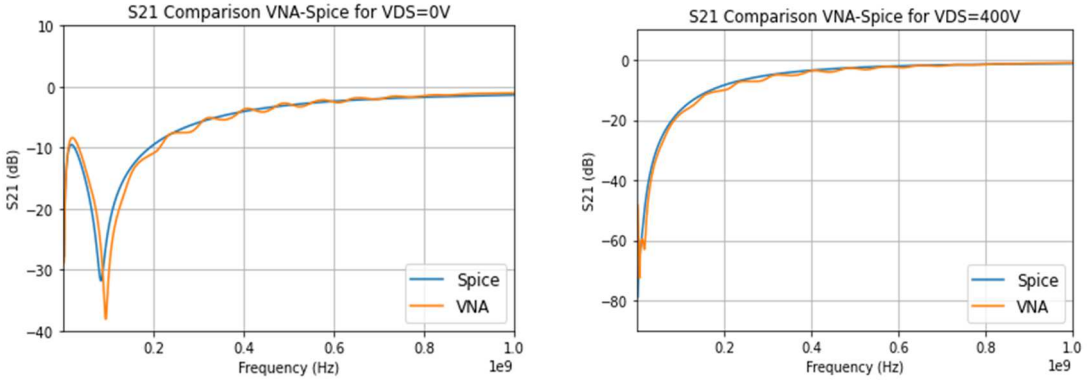

Fig. 11: S_{21} parameter for V_{DS} = 0V and V_{DS} = 400V. Vendor 2.

Given that results for Vendor 2 have shown more divergence between Spice simulations and VNA measurements, a complementary analysis is developed as follows. In eq.(2), the input and output reflection coefficients are complex numbers that consider the magnitude and phase of the S-parameters S_{11} and S_{22} and their relation with the unknown impedance. Thus, the relation between the unknown impedance and the reflection coefficient is given by eq.(4).

$$Z_L = Z_0 \frac{1+\Gamma}{1-\Gamma} \tag{4}$$

Figure 12 depicts the magnitude of the input reflection coefficient $|\Gamma_{in}|$ for a bias voltage V_{DS} = 400V. This figure shows that the Spice model underestimates the input reflection coefficient from frequencies between 1MHz and 650MHz. Therefore, the model in this frequency range will underestimate the associated impedance between the Gate-Source terminals. On the other hand, the Gate-Source impedance will be overestimated by the model in frequencies higher that 650MHz. Figure 13 shows a suitable agreement between the phase of the input reflection coefficients for experimental and simulation results.

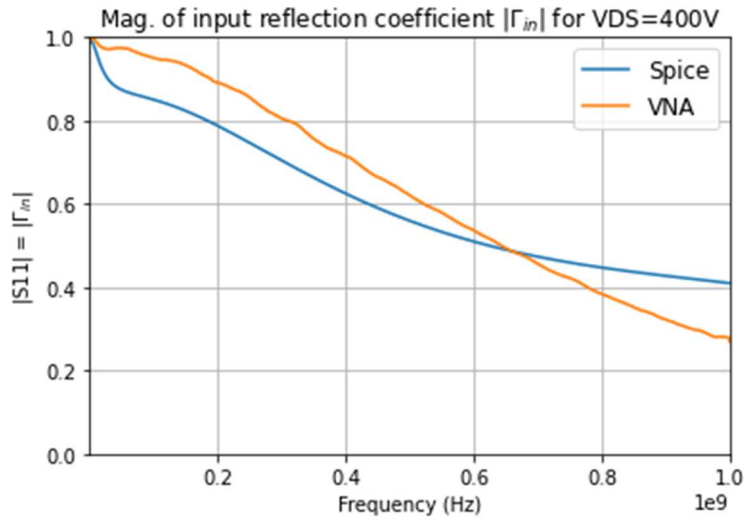

Fig. 12: Magnitude of input reflection coefficient $|\Gamma_{in}| = |S_{11}|$ for $V_{DS} = 400V$. Vendor 2.

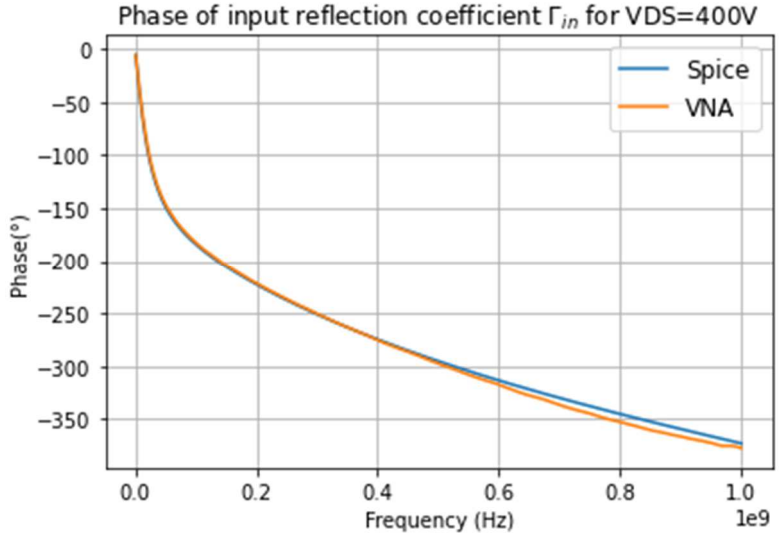

Fig. 13: Phase of input reflection coefficient $\angle\Gamma_{in} = \angle S_{11}$ for $V_{DS} = 400V$. Vendor 2.

Figure 14 illustrates the magnitude of the output reflection coefficient $|\Gamma_{out}|$ for a bias voltage $V_{DS} = 400V$. This figure highlights that the Spice model is higher than the VNA measurements for the output reflection coefficient in the frequencies range between 1MHz and 1GHz. Therefore, the model in this frequency range will overestimate the associated impedance between the Drain-Source terminals. Furthermore, Figure 15 shows a suitable agreement between the phase of the input reflection coefficients for experimental and simulation results.

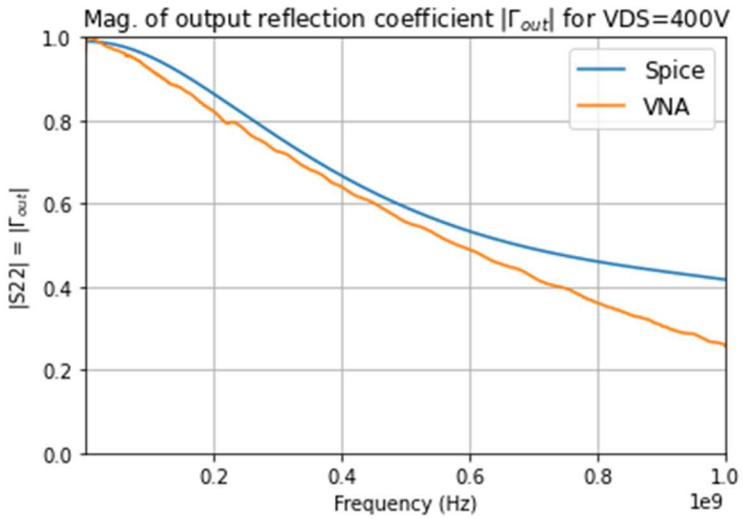

Fig. 14: Magnitude of output reflection coefficient $|\Gamma_{out}| = |S_{22}|$ for $V_{DS} = 400V$. Vendor 2.

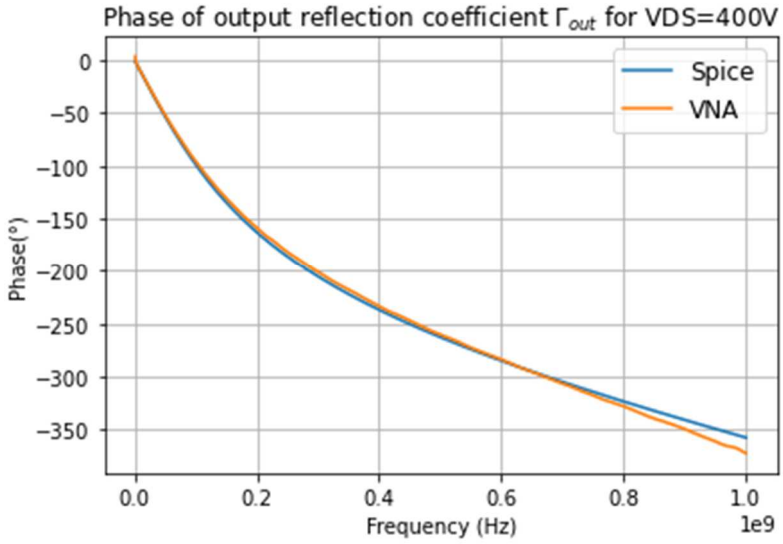

Fig. 15: Phase of input reflection coefficient $\angle\Gamma_{out} = \angle S_{22}$ for $V_{DS} = 400V$. Vendor 2.

To summarize, the results of this work highlight the potential of S-parameters to study the behavior of capacitive, inductive, and resistive elements of power GaN-HEMTs and their package in an extended span of frequencies and voltages. Indeed, the proposed approach has allowed the evaluation of power GaN models with an alternative perspective considering a radio-frequency approach and using an accessible power electronics simulator.

Conclusion

This work has described a radio-frequency technique based on S-parameters measurements and a Python library to verify and explore the characteristics of power GaN-HEMTs and their packaged in the frequency domain at several biasing voltages. The proposed approach has allowed the study of power GaN models with radio-frequency methodologies but using a well-known simulation tool in power electronics. This technique has required the implementation of a low complexity hardware setup to sweep the frequency and voltage at the same time. VNA measurements and Spice simulations were compared to evaluate Spice models from different commercial vendors suggesting potential improvements. The explored methodology confirmed the potential of S-parameters as a powerful tool to characterize power GaN-HEMTs and to build models including the parasitic effect of the package. Indeed, different elements of GaN-HEMT transistors could be extracted such as the parasitic aspects of the packaging in order to predict undesired oscillations and to improve the device reliability. Additionally, the device capacitive behavior could be determined in the frequency domain for different biasing voltages. The reflection coefficient allowed to verifying the Spice model accuracy in a wide range of frequencies.

The proposed methodology can be potentially extended to the study of more complex configurations such as Cascode or half-bridge interconnections. As a future work, a deeper result analysis will be discussed and their correlation with the time domain will be considered. Furthermore, pulsed DC and pulsed RF measurements can be done by adapting the same test bench in order to do reliability tests on power GaN devices.

References

[1] C. Bao and S. K. Mazumder, "GaN-HEMT Based Very-High-Frequency AC Power Supply for Electrosurgery," 2021 IEEE Applied Power Electronics Conference and Exposition (APEC), 2021, pp. 220-225.

[2] M. Baker, S. Jain and M. B. Shadmand, "GaN based High Frequency Power Electronic Interfaces: Challenges, Opportunities, and Research Roadmap," 2021 IEEE Power and Energy Conference at Illinois (PECI), 2021, doi: 10.1109/PECI51586.2021.9435203.

[3] R. Sun, J. Lai, W. Chen and B. Zhang, "GaN Power Integration for High Frequency and High Efficiency Power Applications: A Review," in IEEE Access, vol. 8, pp. 15529-15542, 2020, doi: 10.1109/ACCESS.2020.2967027.

[4] Z. Liu, X. Huang, F. C. Lee and Q. Li, "Package Parasitic Inductance Extraction and Simulation Model Development for the High-Voltage Cascode GaN HEMT," in IEEE Transactions on Power Electronics, 2014.

[5] S. Khandelwal, Y. S. Chauhan, J. Hodges and S. A. Albahrani, "Non-Linear RF Modeling of GaN HEMTs with Industry Standard ASM GaN Model," 2018 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS), 2018, pp. 93-97, doi: 10.1109/BCICTS.2018.8550974.

[6] L. Pace, " Caractérisation et Modélisation de Composants GaN pour la Conception des Convertisseurs Statiques Haute Fréquence," PhD thesis, Université de Lille, 2019.

[7] G. Curatola, G. Verzellesi, " Modelling of GaN HEMTs: From Device-Level Simulation to Virtual Prototyping, "In: Power GaN Devices, Power Electronics and Power Systems. Springer, Cham. 2017, doi.org/10.1007/978-3-319-43199-4_8

[8] A. J. Baden Fuller, " An Introduction to Microwave Theory and Techniques", Second Edition, Pergammon International Library, 1979, ISBN 0-08-024227-8.

[9] N. Said," Conception et Réalisation d'un Banc de Test pour la Caractérisation des Composants de Puissance GaN/Si et de Leur Packaging sous Stress Electrique," End-of-studies project, Master 2 - ESET, Université de Toulouse – CEA Tech Occitanie, 2021.

[10] L. Pace, N. Defrance, A. Videt, N. Idir, J.-C. De Jaeger, and V. Avramovic. "Extraction of Packaged GaN Power Transistors Parasitics using S-parameters". IEEE Transactions on Electron Devices, 2019.

[11] Pysmithplot project, repository at https://pypi.org/project/pysmithplot-fork/#files [Accessed: May 22, 2021]