A High-step-down Converter with Negative Output Voltage

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***Abstract*–This paper proposes a new high step-down converter with negative voltage output, which has the following advantages: (1) Compared to conventional buck-boost or SEPIC converters, the proposed converter operates with zero voltage turn-on function. (2) The voltage gain of this circuit does not contain non-linear components, and the control is simple and can be driven by existing buck control ICs. (3) Due to the DC blocking capacitor between the output and input terminals, the high voltage at the input will not pass through to the output when the converter fails to be controlled. The load is protected. Finally, a prototype is completed and the proposed method is verified to be feasible.**

I. INTRODUCTION

Most of the early desktop and server power supply designs were based on the 12V DC bus power supply architecture, which has matured over the years and is still in use today. However, with the rapid growth of high-performance computing and data storage, the power consumption of digital chips has not been able to keep up with the increase in the number of chips due to the process evolution. Google has proposed a 48 V power supply topology to improve the energy consumption problem of data centers. By switching from 12V DC bus to 48 V DC bus, the input current demand can be reduced by 4 times and the loss can be reduced 16 times. In addition, the automotive, 5G, and industrial applications are also transitioning to 48 V power distribution. Therefore, the 48V power converter ecosystem is growing rapidly.

The 48 V DC bus is generated by isolated AC-DC converters in communication equipment rooms and network communication rooms. Depending on the chip, such as a disk drive or SSD or FPGA, the power converter needs to provide several different voltage rails below 3.3 V. Traditional buck converters generate low output voltages directly from the 48 V DC bus, which often causes difficulties in controller design and high switching losses. Therefore, most industrial applications nowadays adopt a 2-stage buck architecture [1]-[4]. However, this method requires more active switches and components, as well as multiple independent control circuits, and the overall conversion efficiency is lower. The positive output high-step-down converter are presented [5]-[8]. However, in some industrial computer equipment with analog signal transmission and reception, and in many personal computers with analog input and output interfaces, these analog voltages often have symmetrical positive and negative supply rails for the operational amplifier ICs, usually ±12 V DC or ±5 V DC.

This paper proposes a new high step-down converter with negative voltage output, which has the following advantages: (1) The voltage gain of this circuit does not contain non-linear components, and the control is simple and can be driven by existing buck control ICs. (2) The output and input have a constant current blocking capacitor, so if any switch fails and continues to turn on, the high voltage at the input will not pass through to the output, and the load is protected to some extent. Finally, a prototype was completed and the proposed method was verified to be feasible.

II. PROPOSED CIRCUIT CONFIGURATION

The proposed high step-down converter with a single negative output voltage has three active switches: Q_1, Q_2, and Q_3, capacitors C_B and C_o, and a coupling inductor L with N_1 and N_2 windings as shown in Fig. 1. Q_2 and Q_3 can be driven synchronously, so the drive control signals can be shared. The next section describes the circuit operation.

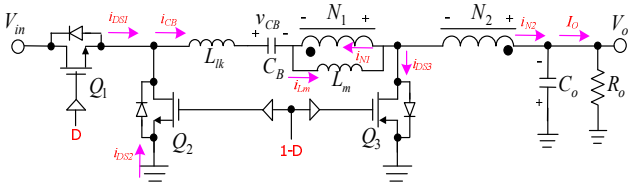


Fig. 1. The proposed negative output high-step-down converter

A. Operation States

The simulation waveforms of the proposed circuit is shown in Fig. 2. This circuit has eight operation steps, which are illustrated in Figs. 3(a) to 3(h).

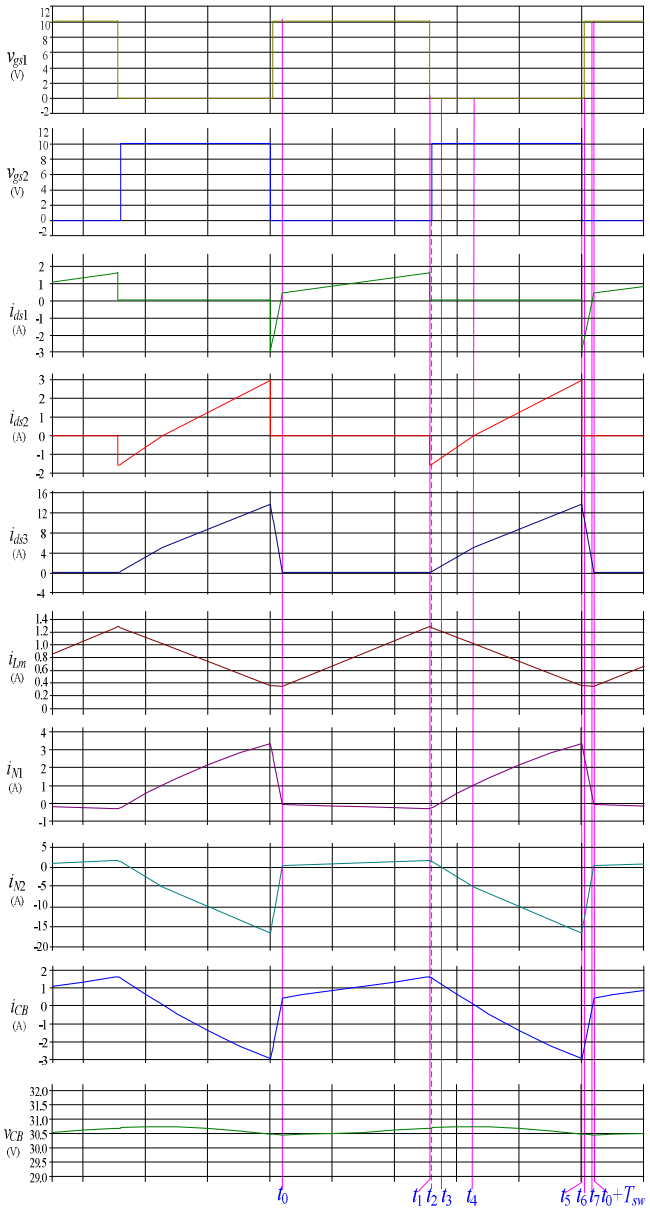


Fig. 2. Simulation waveforms of the proposed converter

State 1 [t_0, t_1]: As shown in Fig. 3(a), Q_1 is turned on, but Q_2 and Q_3 remain off-state. During this state, a positive voltage is imposed on the magnetizing inductor L_m and the leakage inductor L_{lk}, making L_m and L_{lk} magnetized. In this state, the capacitor C_B is being charged, and i_{N1} and i_{N2} in the windings N_1 and N_2 are increasing slowly.

$$i_{DS1} = i_{CB} = i_{lk} = i_{Lm} + i_{N1}$$
$$= i_{N2} = \frac{N_2}{N_1} i_{N1}$$

(1) $$\frac{di_{Lm}}{dt} = \frac{v_{Lm}}{L_m}$$

(2)

State 2 [t_1, t_2]**:** As shown in Fig. 3(b), Q_1 is turned off, and Q_2 and Q_3 are still turned off. During this dead time, the body diodes of the switches Q_2 and Q_3 are forward-biased by i_{lk}. Meanwhile, the voltage $V_o \times N_1 / N_2$ is imposed on L_m, causing L_m is demagnetized.

$$i_{DS2} = i_{CB} = i_{lk} \quad (3)$$

$$i_{Lm} = i_{CB} + i_{N1}$$
$$= i_{CB} + i_{N2} \cdot \frac{N_1}{N_2} \quad (4)$$

$$\frac{di_{Lm}}{dt} = \frac{v_{Lm}}{L_m} = \frac{V_{N1}}{L_m} = \frac{V_o \cdot (\frac{N_1}{N_2})}{L_m} \quad (5)$$

State 3 [t_2, t_3]**:** As shown in Fig. 3(c), Q_1 keeps off-state. Before the State 3 begins, there are currents flowing through the body diodes of Q_2 and Q_3. At this time, Q_2 and Q_3 can be turned on with zero voltage switching (ZVS). L_m is demagnetized as shown in (5). The corresponding equations are the same as those in State 2.

State 4 [t_3, t_4]**:** As shown in Fig. 3(d), Q_1 keeps off-state. Q_2 and Q_3 keep on-state. L_m is demagnetized as shown in (5). When i_{lk} is less than i_{Lm}, i_{N1} and i_{N2} are reversed. When i_{lk} is demagnetized to 0, it enters State 5.

State 5 [t_4, t_5]**:** As shown in Fig. 3(e), Q_1 keeps off-state. Q_2 and Q_3 keep on-state. During this state, the energy-transferring capacitor C_B is discharged, and the energy of C_B is released to the output terminal via the windings N_1 and N_2. The windings currents i_{N1} and i_{N2}, are increasing gradually. L_m is demagnetized as shown in (7).

$$i_{DS2} = i_{CB} = i_{lk}$$
(6)

$$i_{Lm} = i_{N1} - i_{CB} = i_{N2} \cdot \frac{N_1}{N_2} + i_{CB}$$
(7)

State 6 [t_5, t_6]**:** As shown in Fig. 3(f), Q_1 is turned on. Q_2 and Q_3 are turned off. Since this state is the dead time. The currents in the coupling inductor keep continuous. The body diodes of Q_1 and Q_3 are forward-biased. L_m is demagnetized as shown in (9).

$$i_{DS1} = i_{CB} = i_{lk}$$
(8)

$$i_{Lm} = i_{N1} + i_{DS1}$$
$$= i_{N2} \cdot \frac{N_1}{N_2} + i_{DS1}$$
$$= i_{N2} \cdot \frac{N_1}{N_2} + (i_{N2} - i_{DS3})$$
(9)

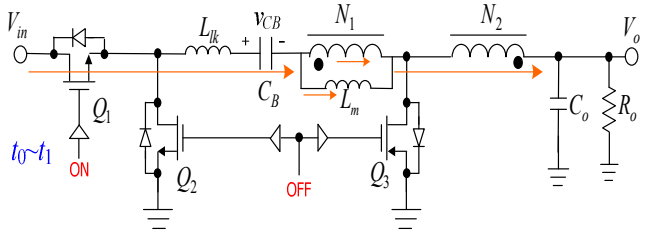
State 7 [t_6, t_7]**:** As shown in Fig. 3(g), Q_1 is keeps off-state. Q_2 and Q_3 keep off-state. Before the state 7 begins, there is a current flowing through the body diodes of Q_1. At this time, Q_1 can be turned on with ZVS.

State 8 [t_7, t_0]**:** As shown in Fig. 3(h), Q_1 is turned on. Q_2 and Q_3 keep off-state. During this state. V_{in} charges C_B. At the same time, i_{N2} and i_{CB} flow through the body diode of Q_3 with forward-biased. When i_{N2} falls and flows reversely, the current in the body of Q_3 stops flowing, and the operation state goes back to state 1.

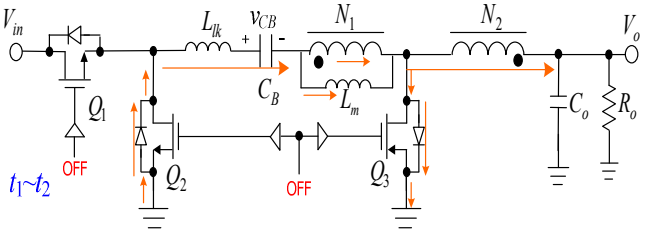
$$i_{DS1} = i_{CB} = i_{lk}$$
(10)

$$i_{Lm} = i_{CB} + i_{N1}$$
$$= i_{CB} + i_{N2} \cdot \frac{N_2}{N_1} \quad (11)$$

$$i_{DS3} = i_{DS1} + i_{N2} \quad (12)$$



(a)



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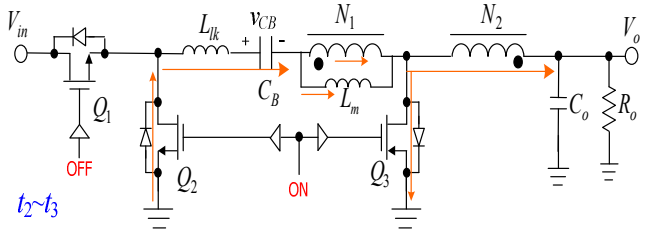
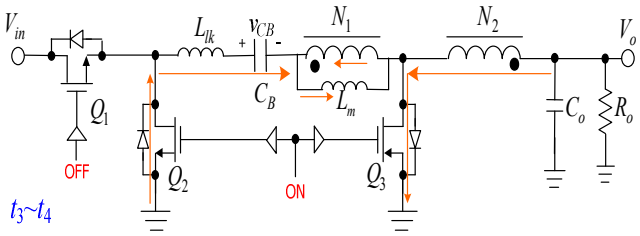
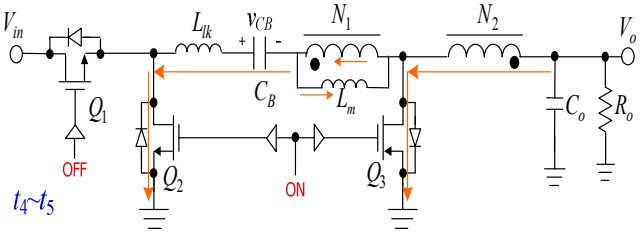


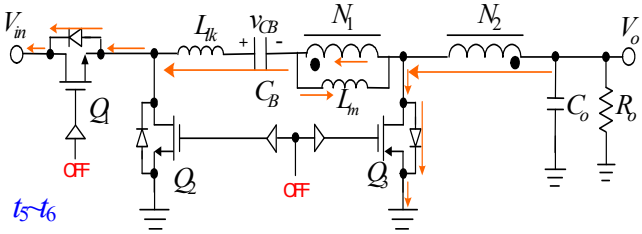
(c)



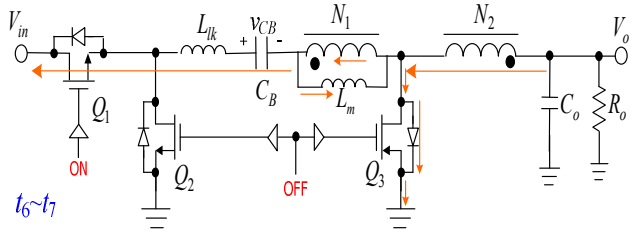
(d)



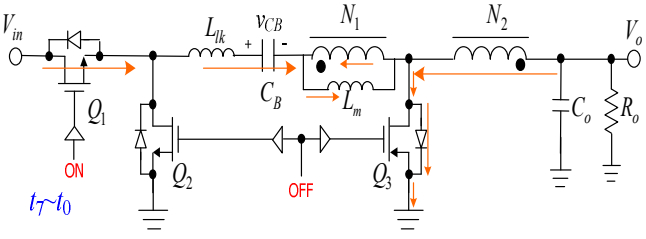
(e)



(f)



(g)



(h)

Fig. 3. The operation states of the proposed circuit: (a) state1; (b) state2; (c) state3; (d) state 4; (e) state 5; (f) state 6; (g) state 7; (h) state 8.

B. Derivation of Voltage Gain

The derivation of the voltage gain of the proposed circuit can be started from the voltage-second balance of L_m. Before this session, the coupled inductor L is assumed that there is no leakage inductance in windings N_1 and N_2.

ON states:

$$v_{N1} = V_{in} - v_{CB} + v_{N2} - V_o \tag{13}$$

$$v_{N2} = \frac{N_2}{N_1} \cdot v_{N1} \tag{14}$$

$$v_{N2} = V_{in} - v_{CB} + \frac{N_2}{N_1} \cdot v_{N1} - V_o \tag{15}$$

$$v_{N2} = V_{in} - v_{CB} + \frac{N_2}{N_1} \cdot v_{N1} - V_o \tag{16}$$

$$v_{N1} = \left(\frac{N_1}{N_1 - N_2} \right) \cdot V_{in} + \left(\frac{N_1}{N_2} \right) \cdot V_o \tag{17}$$

OFF state：

$$v_{N1} = 0 - v_{CB} + v_{N2} - V_o \tag{18}$$

$$v_{N1} = -v_{CB} = \frac{N_1}{N_2} \cdot v_{N2} = \frac{N_1}{N_2} \cdot V_o \tag{19}$$

$$v_{N2} = \frac{N_2}{N_1} \cdot v_{N1} = V_o \tag{20}$$

$$v_{CB} = -\frac{N_1}{N_2} \cdot V_o \tag{21}$$

Since $v_{CB} = -V_o \cdot \left(\frac{N_1}{N_2} \right)$, the volt-second balance equation of the winding N_1 can be represented as (22). Finally, (22) can be simplified to (23). The voltage gain of the proposed circuit is shown as (23).

$$\begin{aligned} & v_{N1(ON)} \cdot D + v_{N1(OFF)} \cdot (1-D) \\ & = D \cdot \left[\left(\frac{N_1}{N_1 - N_2} \right) \cdot V_{in} + \left(\frac{N_1}{N_2} \right) \cdot V_o \right] \\ & + (1-D) \cdot \left(\frac{N_1}{N_2} \cdot V_o \right) = 0 \end{aligned} \tag{22}$$

$$\frac{V_o}{V_{in}} = -D \cdot \left(\frac{N_2}{N_1 - N_2} \right) \tag{23}$$

III. EXPERIMENTAL RESULTS

The specification of the prototype circuit is shown in Table 1. Table 2 Shows the list of main components. Fig. 4 shows the simulation circuit.

Table I. The key specification of the prototype

Symbol	Specification
V_{in}	48 V
V_o	−5 V
$I_{o\text{-}rated}$	4 A
$I_{o\text{-}min}$	0.4 A
F_{sw}	100 kHz

Table II. Key feature of main component

Symbol	Part number/Key Feature	Manufacturer
Q_1, Q_2	PSMN008-75B(75 V/8.5 mΩ)	Nexperia
Q_3	IRL3705ZS(55 V/8 mΩ)	Infineon
Q_4	IRF4905 (−55 V/20 mΩ)	Infineon
C_{B1}, C_{B2}	parallel 2 x 10 μF (MLCC)	TDK
C_{in}	330 μF/63 V(E-cap)	Rubycon
C_{o1}, C_{o2}	270 μF /16 V (E-cap)	Panasonic
L_1	T90-M125; N_{11}:N_{12}=24:8; L_{m1}=51.1 μH, L_{lk1}=1.22 μH,	Micrometals
L_2	T90-M125; N_{21}:N_{22}=40:8; L_{m2}=144.6 μH , L_{lk2}=5.09 μH, $AL = 90\frac{nH}{N^2}$	Micrometals

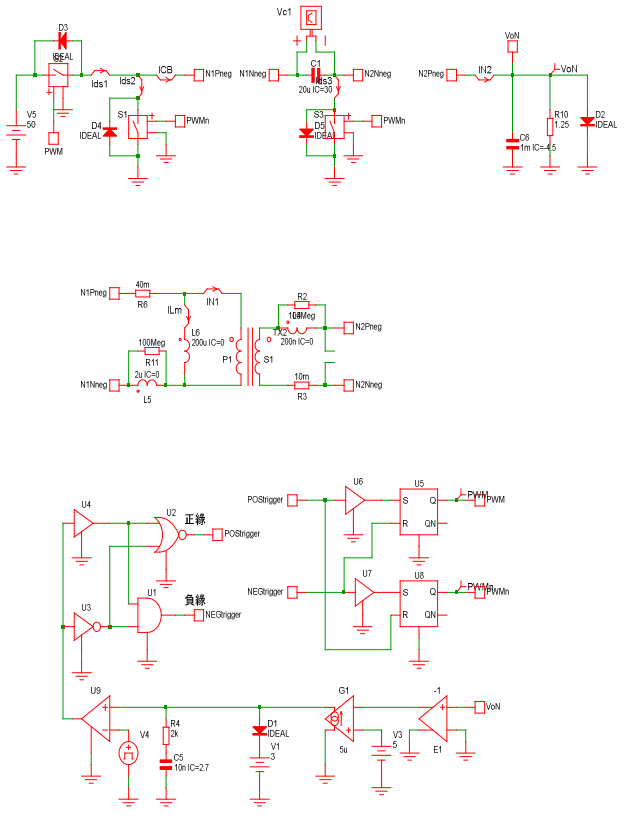
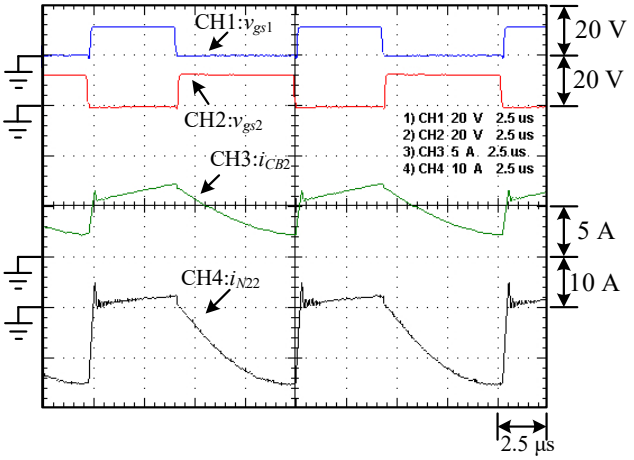
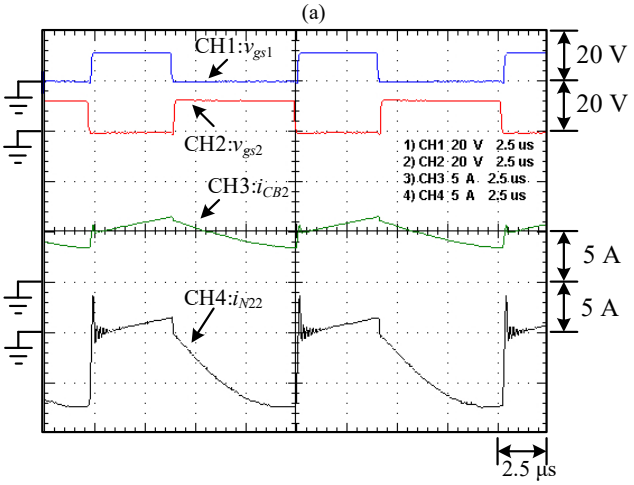


Fig. 4. Simulation circuit

Fig. 5(a) and (b) show the waveforms of v_{gs1}, v_{gs2}, i_{CB}, and i_{N2} when 50% and 100% of the load current are applied respectively, which are negative voltage outputs, so the DC output current should be negative. Fig. 6(a) and (b) show the waveforms of v_{gs1}, v_{CB}, and i_{CB} when 50% and 100% of the load current are applied respectively. The current in Fig. 6(b) is close to the simulated waveform in Fig. 2, and v_{CB} is also close to that in (21). Fig. 7 shows the conversion efficiency curve and it can be observed that the efficiency can reach 90% at full load and the maximum efficiency is 91% at half load.

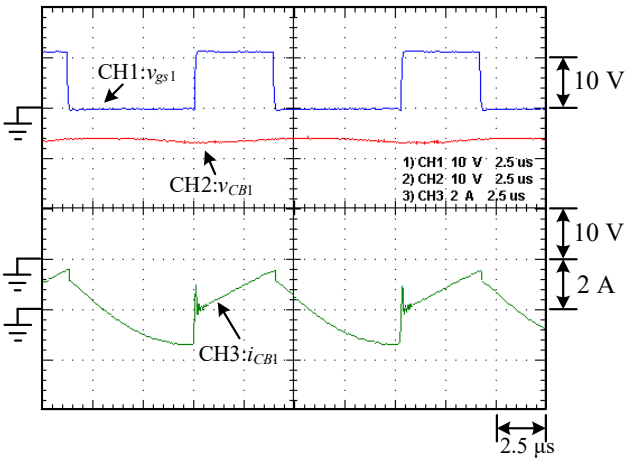


(a)

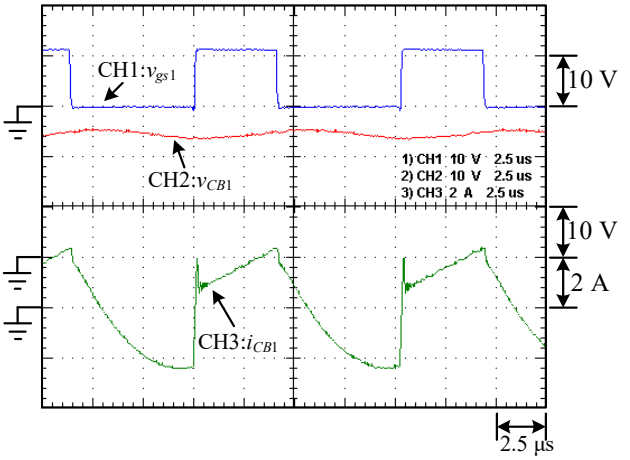


(b)

Fig. 5. v_{gs1}, v_{gs2}, i_{CB}, i_{N2}: (a) half load ; (b) full load



(a)



(b)

Fig. 6. v_{gs1}, v_{CB}, i_{CB}: (a) half load ; (b) full load

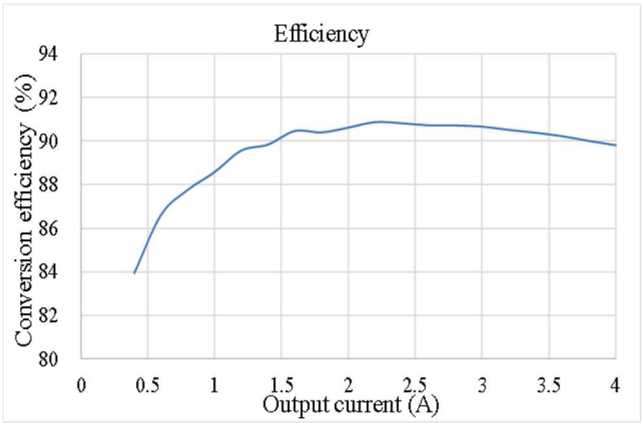


Fig. 7. Measured conversion efficiency

IV. CONCLUSION

This paper proposes a negative voltage output high step-down converter. Compare to the conventional topologies, the proposed converter provides zero voltage turn-on function. The voltage gain of this circuit is similar to buck converter.

There is a DC blocking capacitor between the output terminal and input terminal. If any switch fails and continues to turn on, the high voltage at the input will not pass through

to the output. The experimental result shows the proposed circuit provides high conversion efficiency of 90% and 91% at full load and half load, respectively.

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