Pulse Width Modulation Method for Reliability Improvement of DC-link Capacitors and Power Devices of NPC Inverter

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***Abstract*-- Power devices and DC-link capacitors are considered reliability-critical components in power converters. Thermal stress caused by power loss leads to wear-out failures of DC-link capacitors and power devices. Previous studies have proposed various PWM methods to reduce the thermal stress of DC-link capacitors and power devices, respectively. However, the existing methods did not consider the reduction of thermal stress of DC-link capacitors and power devices simultaneously. This paper proposes the PWM method for improving the reliability of the NPC inverter by decreasing the thermal stress of DC-link capacitors and power devices concurrently. Through the simulations and experiments, the feasibility and effectiveness of the proposed PWM method are verified.**

***Index Terms*-- pulse width modulation, 3-level NPC inverter, reliability, photovoltaic**

I. Introduction

The three-level neutral-pointed-clamped (NPC) inverter has been widely used in various power electronic applications because of its advantages, such as lower total harmonic distortion (THD) of the outputs and higher efficiency compared with the two-level inverter. Furthermore, as shown in Fig. 1, the three-level inverter allows using power devices with lower rated voltage because the DC-link voltage is divided across two power devices connected in series [1]-[3].

As the role of power electronic systems has been gradually more significant, their reliability is getting more attention. Much research has been conducted to improve the reliability of power electronic systems focusing on DC-link capacitors and power devices regarded as reliability-critical components [4]-[5].

Especially, various pulse width modulation (PWM) methods have been proposed to increase the lifetime of the DC-link capacitors and power devices by reducing their thermal loading, which is the critical stressor leading to dominant wear-out failure. In [6]-[7], the PWM methods are proposed for the NPC inverter to increase the lifetime of DC-link capacitors, where voltage vectors causing a high DC-link capacitor current are replaced with other voltage vectors for decreasing it and thereby reducing the thermal loading. Different modulation techniques for accomplishing the temperature stress redistribution among the power devices have been introduced, but these methods are applicable only under specific modulation index regions [8]-[9].

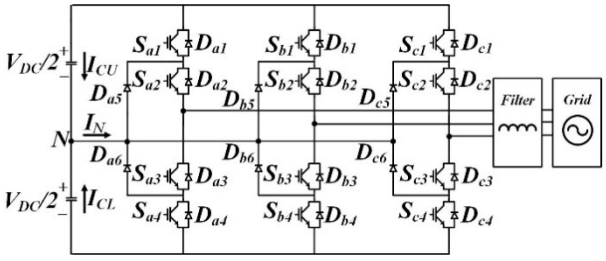

Fig. 1. Three-level NPC inverter.

The discontinuous PWM (DPWM) can increase the lifetime of the power devices of the NPC inverter by reducing their switching loss which results in lower thermal loadings [10]. However, as mentioned in [11], the lifetime of the DC-link capacitor is reduced under DPWM. Furthermore, existing methods focus on only one component, either the DC-link capacitor or the power device. Further, their effects on the reliability of the other reliability-critical components were not analyzed.

In this paper, the PWM method for improving the reliability of the NPC inverter is proposed. The proposed PWM method not only decreases the thermal loadings of the DC-link capacitors by reducing its current but also reduces the thermal loadings of the power devices having the highest junction temperature among the power devices of the NPC inverter. The feasibility and effectiveness of the proposed PWM method are validated by simulations and experiments.

II. Power Loss and Thermal Loading of Power Device and Capacitor

The power loss of the power device (P_{loss_d}) leads to the increase in the junction temperature of the power device (T_j). Since the power module is composed of various materials, having different coefficients of thermal expansion, the temperature variation in the power module applies the thermal-mechanical stress and finally leads to fatigue failures [12]-[13]. Therefore, minimizing the power loss for thermal loading reduction is the key method to improve the reliability of the power device.

An aluminum electrolytic capacitor is widely used for the DC-link of inverters, and electrolyte evaporation due to thermal stress is one of the typical wear-out failure mechanisms [15].

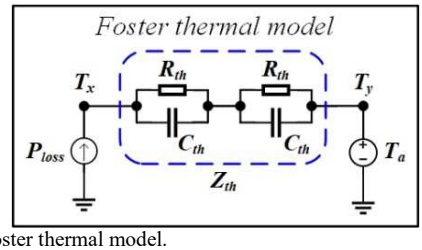

Fig. 2. Foster thermal model.

The capacitor current ripple causes power loss (P_{loss_c}) and thus increases the hot-spot temperature of the capacitor (T_{hot}). Therefore, its reduction plays a key role to improve the lifetime of the capacitor.

In this paper, the IGBT module and the aluminum electrolytic capacitor for the DC-link are considered for the NPC inverter.

A. Thermal Loading of Power Device

P_{loss_d} is determined by a sum of the conduction loss (P_{con}) and switching loss (P_{sw}), and it can be represented as

$$P_{loss\_d} = P_{con} + P_{sw} \tag{1}$$

When the power device is in its on-state and conducts current, the P_{con} occurs due to the voltage drop across the device. The P_{con} can be expressed as

$$P_{con} = V_{CE(sat)} \cdot I_C \cdot D_{on} \tag{2}$$

where $V_{CE(sat)}$ is the collector-emitter saturation voltage and I_C is the collector current, and D_{on} is the duty cycle of the switching period.

When the power device transitions from its on-state to its off-state or vice versa, P_{sw} occurs. Thus, P_{sw} can be represented as

$$P_{sw} = f_{sw} \cdot E_{sw} \tag{3}$$

where E_{sw} and f_{sw} are the switching energy and switching frequency, respectively.

The T_j is obtained as

$$T_j = P_{device} \cdot Z_{th(j-h)} + P_{module} \cdot Z_{th(h-a)} + T_a \tag{4}$$

where $Z_{th(j-h)}$ and $Z_{th(h-a)}$ represent the thermal impedance from the junction to heat-sink and from heat-sink to the ambient, respectively. P_{loss_m} is the total power loss of the IGBT module placed on the heat-sink.

The thermal impedance is modeled by the Foster model shown in Fig. 2 and expressed as

$$Z_{th}(t) = \sum_{i=1}^{n} R_{th_i}(1 - e^{-t/\tau_i}),\ (\tau_i = R_{th_i} \cdot C_{th_i}) \tag{5}$$

where R_{th} is the thermal resistance, C_{th} is the thermal capacitance, and i indicates the number of RC combinations of the Foster model.

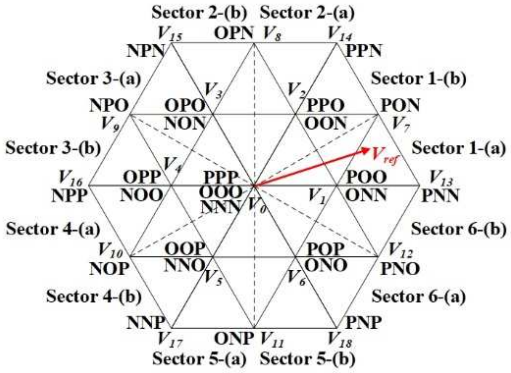

Fig. 3. Space vector diagram of the NPC inverter.

B. Thermal Loading of Capacitor

The thermal loading of the capacitor is mainly caused by the power loss due to the ripple current. P_{loss_c} can be calculated from the equivalent series resistance (R_{ESR}) and capacitor ripple current as

$$P_{loss\_c} = \sum_{i=1}^{m} \left[R_{ESR}(f_i, T_{hot}) \cdot I^2(f_i) \right] \tag{6}$$

where $I(f_i)$ is the root-mean-square value of the capacitor current at specific frequency f_i, and m is the number of the frequency components. Since R_{ESR} depends on both the frequency f_i and T_{hot}, both factors need to be taken into consideration for P_{loss_c}. R_{ESR} decreases as the frequency increases and thus has a relatively large value at low-frequency regions.

Then, T_{hot} of the capacitor is obtained as

$$T_{hot} = T_a + Z_{ha} \cdot P_{loss\_c} \tag{7}$$

where Z_{ha} is the thermal impedance of the capacitor between the hot-spot and ambient. It is also represented by the Foster thermal model.

III. Proposed PWM Method for Reliability Improvement of NPC Inverter

A. Conventional SVM

Each phase of the NPC inverter is able to have three switching states [P], [O], and [N]. Thus, it has a total of 27 combinations of switching states. Voltage vectors are classified into zero, small, medium, and large voltage vectors according to their magnitude. V_0 indicates the zero voltage vector, where its magnitude is zero. V_1–V_6 represent small voltage vectors and their magnitudes are $V_{DC}/3$. V_7–V_{12} and V_{13}–V_{18} denote the medium and large voltage vectors, and they have the magnitudes of $V_{DC}/\sqrt{3}$ and $2 \cdot V_{DC}/3$, respectively. The voltage vectors and the corresponding switching states are represented in the space vector diagram as illustrated in Fig. 3.

The DC-link of the NPC inverter is composed of two capacitors, the upper (C_U) and lower capacitors (C_L). The neutral point current (I_N) can be expressed by the upper capacitor current (I_{CU}) and lower capacitor current (I_{CL}) as

$$I_N = I_{CU} + I_{CL} \tag{8}$$

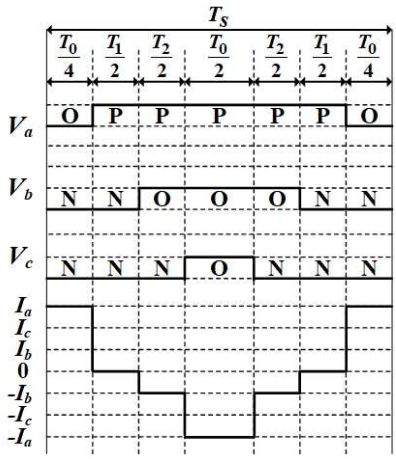

Fig. 4. Switching sequence and the corresponding neutral point current under the conventional SVM.

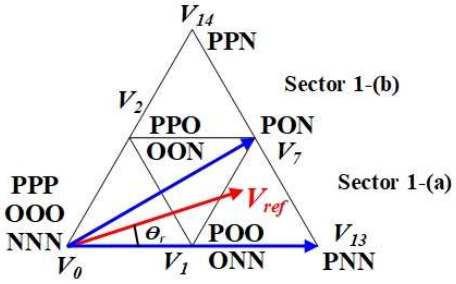

Fig. 5. Space vector diagram under proposed PWM method.

If the capacitances of upper and lower capacitors are identical, I_{CU} and I_{CL} have the same value but not at the same time. Thus, the reduction of I_N leads to decreases in the currents of the upper and lower capacitors.

The conventional SVM selects the voltage vectors closest to the reference voltage vector (V_{ref}). If V_{ref} is located in sector 1-(a) as shown in Fig. 3, V_1, V_7, and V_{13} are chosen to generate V_{ref}, and the switching sequence is formed as [ONN]-[PNN]-[PON]-[POO]-[PON]-[PNN]-[ONN] so that each phase changes its switching state twice during a switching cycle (T_s).

The voltage vectors have different effects on I_N since I_N is determined by currents of the specific phases connected to the neutral point. When the switching states are [POO] or [ONN], the largest current among the three phases, phase-A current (I_a), flows into the neutral point. In the case of the switching states [PNN] and [PON], I_N becomes zero and the phase-B current (I_b), respectively. It is seen from the above analysis that the small voltage vectors have the most significant effect on the DC-link current.

The switching sequence and corresponding I_N under the conventional SVM when the reference voltage vector (V_{ref}) is located in sector 1-(a) are given in Fig. 4. It is seen that I_N has the highest value when the switching states are [ONN] or [POO].

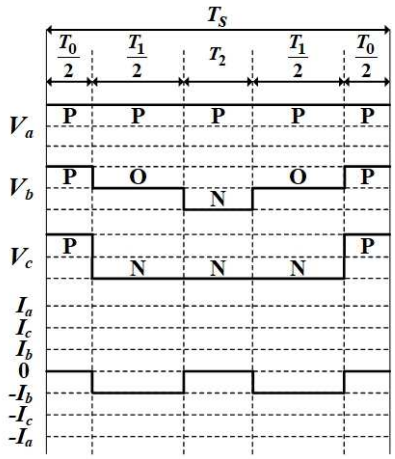

Fig. 6. Switching sequence and the corresponding neutral point current under the proposed PWM method.

TABLE I
SWITCHING SEQUENCES OF PROPOSED PWM METHOD

Sector	Subsector	Switching sequence
1	(a)	[PPP]-[PON]-[PNN]-[PON]-[PPP]
	(b)	[NNN]-[PON]-[PPN]-[PON]-[NNN]
2	(a)	[NNN]-[OPN]-[PPN]-[OPN]-[NNN]
	(b)	[PPP]-[OPN]-[NPN]-[OPN]-[PPP]
3	(a)	[PPP]-[NPO]-[NPN]-[NPO]-[PPP]
	(b)	[NNN]-[NPO]-[NPP]-[NPO]-[NNN]
4	(a)	[NNN]-[NOP]-[NPP]-[NOP]-[NNN]
	(b)	[PPP]-[NOP]-[NNP]-[NOP]-[PPP]
5	(a)	[PPP]-[ONP]-[NNP]-[ONP]-[PPP]
	(b)	[NNN]-[ONP]-[PNP]-[ONP]-[NNN]
6	(a)	[NNN]-[PNO]-[PNP]-[PNO]-[NNN]
	(b)	[PPP]-[PNO]-[PNN]-[PNO]-[PPP]

B. Proposed PWM Method

As analyzed in the previous section, the small voltage vectors make I_N become the maximum phase current under the SVM which cause a large DC-link current. Therefore, to decrease the power loss of the DC-link capacitor, the proposed PWM method replaces the small voltage with the adjacent zero and large voltage vectors so that V_{ref} is generated by using zero, medium and large voltage vectors. For example, if V_{ref} is located in sector 1-(a) as shown in Fig. 5, the proposed PWM method selects the voltage vectors V_0, V_7, and V_{13}, where the small voltage vector V_1 is replaced with V_0 and V_{13}. It is possible since the composition of V_0 and V_{13} is equal to V_1. For zero voltage vector V_0, there are three switching states of [PPP], [OOO], and [NNN]. In this case, if the switching state [PPP] is chosen, the switching sequence is established as [PPP]-[PON]-[PNN]-[PON]-[PPP] as shown in Fig. 6. The phase-A is fixed to [P] and therefore the switching losses of outer power devices of $S_{x(x=a, b, c)1}$ and S_{x4} are reduced. It results in a decrease in T_j S_{x1} and S_{x4}, and consequently, the lifetime is increased. Furthermore, only I_b, which is the smallest one among the three-phase currents becomes the neutral point current when the switching state is [PON]. Therefore, the reduction in DC-link capacitor current is achieved.

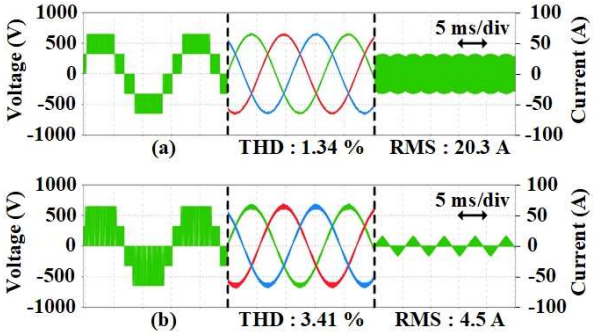

Fig. 7. Simulation results of line-to-line voltage (V_{AB}), the output currents, and the capacitor current (I_{CU}) under (a) conventional SVM (b) proposed PWM method.

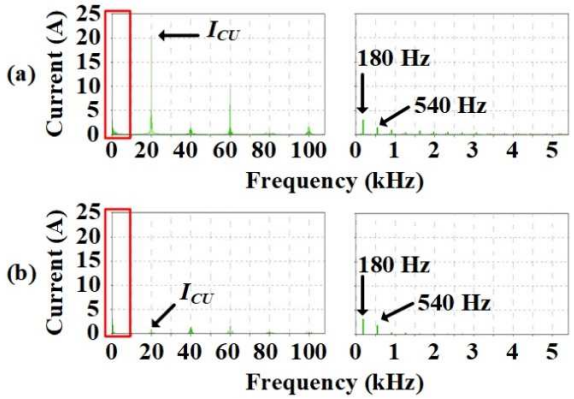

Fig. 8. Simulation results of the capacitor current (I_{CU}) in frequency domain under (a) conventional SVM (b) proposed PWM method.

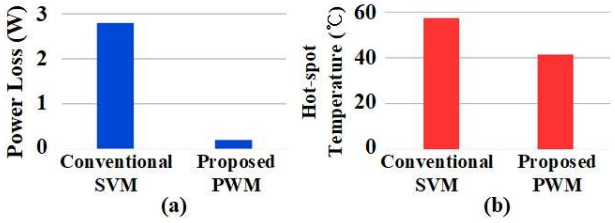

Fig. 9. Thermal loading analysis of DC-link capacitor under the conventional SVM and proposed PWM (a) power loss (b) hot-spot temperature.

However, the number of switching transitions in phase-B and phase-C increases but their effect on the P_{sw} is relatively minor because the phase currents I_b and I_c are small compared with I_a. The same principle and effect are valid for the other sub-sectors of the space vector diagram shown in Fig. 3. In addition, the proposed PWM method can be applied without the limitation of a modulation index.

The switching sequences of proposed PWM method in all sectors are given in TABLE I.

The dwell times of voltage vectors are calculated as (9) and (10), which can be applied to sub-regions (a) and (b) of all sectors, respectively.

$$T_1 = T_s\left[\frac{2\sqrt{3}\cdot|V_{ref}|\cdot\sin(\theta_r)}{V_{DC}}\right],$$
$$T_2 = T_s\left[\frac{3\cdot|V_{ref}|\cdot\cos(\theta_r+\pi/3)}{V_{DC}}\right], \quad (9)$$
$$T_0 = T_s - T_1 - T_2$$

$$T_1 = T_s\left[\frac{2\sqrt{3}\cdot|V_{ref}|\cdot\cos(\theta_r+\pi/6)}{V_{DC}}\right],$$
$$T_2 = T_s\left[\frac{3\cdot|V_{ref}|\cdot\sin(\theta_r-\pi/6)}{V_{DC}}\right], \quad (10)$$
$$T_0 = T_s - T_1 - T_2$$

where θ_r is the angle between V_{ref} and large vectors such as V_{13}-V_{18} ($0° \le \theta_r \le 60°$), and T_0, T_1, and T_2 are the dwell times of zero, medium, and large voltage vectors, respectively.

IV. Effect of Proposed PWM Method on DC-Link Capacitors and Power Devices

In this section, the effect of the proposed PWM method on the thermal loadings of the DC-link capacitors and power devices is comparatively analyzed against the conventional SVM. Simulations are carried out under the conditions as follows: rated output power (P_{rated}): 30 kW, DC-link voltage (V_{DC}): 650 V, switching frequency (f_{sw}): 20 kHz, DC-link capacitance (C_{DC}): 2100 μF, grid voltage (V_g): 220 V_{rms}, grid frequency (f_g): 60 Hz, filter inductor (L): 0.5 mH, ambient temperature (T_a): 40 °C. The considered IGBT module and DC-link capacitor for this study are F3L75R07W2E3_B11 from Infineon and DCMC142T550CC2B from CDM Cornell Dubilier. More details about the IGBT module and capacitor can be found in [17] and [18].

Fig. 7 (a) and (b) show line-to-line voltage V_{AB}, output currents, and I_N at the rated power under the conventional SVM and proposed PWM, respectively. The output current THD is 1.34 %, and the RMS value of the I_{CU} is 20.3 A. Fig. 8 (a) shows the Fast Fourier Transform (FFT) analysis of I_{CU} under the conventional SVM. The dominant ripple currents are 3 A, 20.5 A, and 9.5 A at 180 Hz, 20 kHz, and 60 kHz, respectively. Based on (6) and (7) considering all ripple currents, P_{loss_c} is obtained as 2.8 W, and its corresponding T_{hot} is 57.2 °C as illustrated in Fig. 9. Even though the proposed PWM method gives a negative effect on the output current THD which is increased to 3.41 %, the proposed PWM method reduces I_N significantly from 20.3 A to 4.5 A. Furthermore, as shown in Fig. 8 (b), the proposed PWM method reduces the ripple current at 20 kHz and 60 kHz compared to the conventional SVM, The ripple current is reduced from 20.5 A to 1 A at 20 kHz, and from 9.5 A to 1 A at 60 kHz. Therefore, as shown in Fig. 9, P_{loss_c} is also notably reduced from 2.8 W to 0.2 W. Consequently, T_{hot} decreases from 57.2 °C to 41.4 °C, and therefore, the increases in the lifetime of the DC-link capacitor is able to be expected.

The power loss and T_j distributions of the power devices under the conventional SVM are shown in Fig. 10 (a) and Fig. 11, respectively.

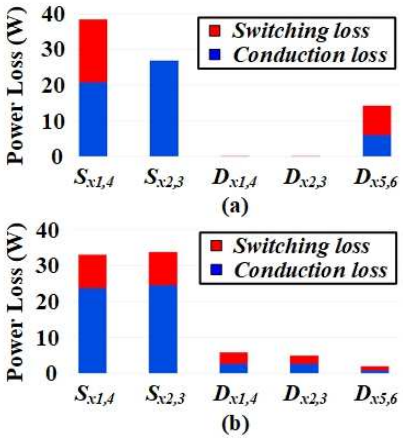

Fig. 10. The power loss distribution of the power devices under (a) conventional SVM (b) proposed PWM method.

S_{x1} and S_{x4} have the highest P_{loss_d} of 38.5 W, and thus the highest T_j of 115.5 °C. The inner power devices of S_{x2} and S_{x3} have a smaller P_{loss_d} of 27 W than that of S_{x1} and S_{x4}. Therefore, there is a T_j difference of about 15 °C between the outer power devices of S_{x1} and S_{x4} and the inner power devices of S_{x2} and S_{x3}. The clamping diodes D_{x5} and D_{x6} have a P_{loss_d} of 14.3 W, but the power loss of the other diodes is negligible. Since S_{x1} and S_{x4} have the highest T_j, they are regarded as the reliability-critical power devices and thus play a major role in the reliability of the NPC inverter. Therefore, the reliability improvement of the NPC inverter is able to be achieved by reducing their T_j.

The proposed PWM method reduces the P_{loss_d} of S_{x1} and S_{x4} from 38.5 W to 33 W as shown in Fig. 10 (b) due to the reduced switching loss. Therefore, the T_j of S_{x1} and S_{x4} is reduced from 115.5 °C to 108.1 °C. On the other hand, the P_{loss_d} of S_{x2} and S_{x3} increases due to higher switching loss caused by the increased number of switching transitions in the switching sequence of the proposed PWM method, but they have almost the same T_j with S_{x1} and S_{x4}. Thus, improved reliability of the power devices can be expected due to the reduced thermal loading of the most reliability-critical power devices. The P_{loss_d} of the clamping diodes of D_{x5} and D_{x6} decreases from 14.3 W to 1.9 W. Even though the power loss of the other diodes increases to 5.8 W, it does not affect reliability because their power loss is still low compared to the reliability-critical power devices, such as S_{x1} and S_{x4}. Additionally, the total power loss generated by the power devices under the proposed PWM is 238.2 W, which is comparable to that under the conventional SVM.

V. Experimental Results

Experiments are performed to verify the feasibility and effectiveness of the proposed PWM method under the following conditions: V_{DC}: 400 V, f_{sw}: 20 kHz, output frequency (f_{out}): 60 Hz, C_{DC}: 3300 μF, Load (R-L): 20 Ω, and 1.5 mH.

As shown in Fig. 12 (b), under the proposed PWM method, the pole voltages are fixed to [P] or [N] for 60 ° each when each phase current has the highest magnitude among three-phase currents. Therefore, the decrease in T_j

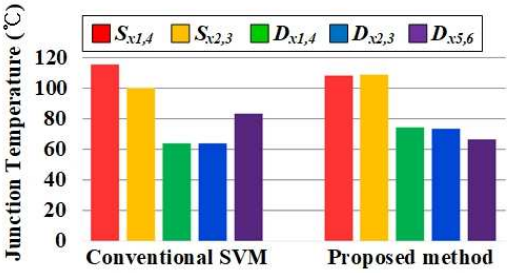

Fig. 11. The junction temperature distribution of the power devices under the conventional SVM and proposed PWM.

of S_{x1} and S_{x4} due to the reduced switching power loss can be expected. Furthermore, the RMS value of the I_N, which is 4.8 A under the conventional SVM is significantly reduced to 0.9 A, and the FFT analysis of the I_N is also reduced from 6 A to 0.3 A at 20 kHz as shown in Fig. 12 (a). It results in decreases in the T_{hot} of DC-link capacitors. The line-to-line voltage has a 5-level and there are no notable distortions in the output current. However, the harmonic current increases, especially at 20 kHz compared to the conventional SVM illustrated in Fig. 12 (a). Therefore, the proposed PWM method increases the THD of the output current. Nevertheless, the results show the advantages of the proposed PWM method in the reliability improvement of both the power devices and DC-link capacitors.

VI. Conclusion

In this paper, the PWM method for the reliability improvement of the NPC inverter is proposed. It is implemented by replacing the small voltage vectors with the adjacent large and zero voltage vectors, where the switching state of the zero voltage vector is chosen so that the switching state of the phase having the highest current is fixed. The proposed PWM method decreases the thermal loadings of the DC-link capacitor and reliability-critical power devices by reducing their power losses compared with the conventional SVM. Even though the output current THD increases, the proposed PWM method has obvious advantages in terms of reliability. The feasibility and effectiveness of the proposed PWM method are verified by the simulation and experiment results.

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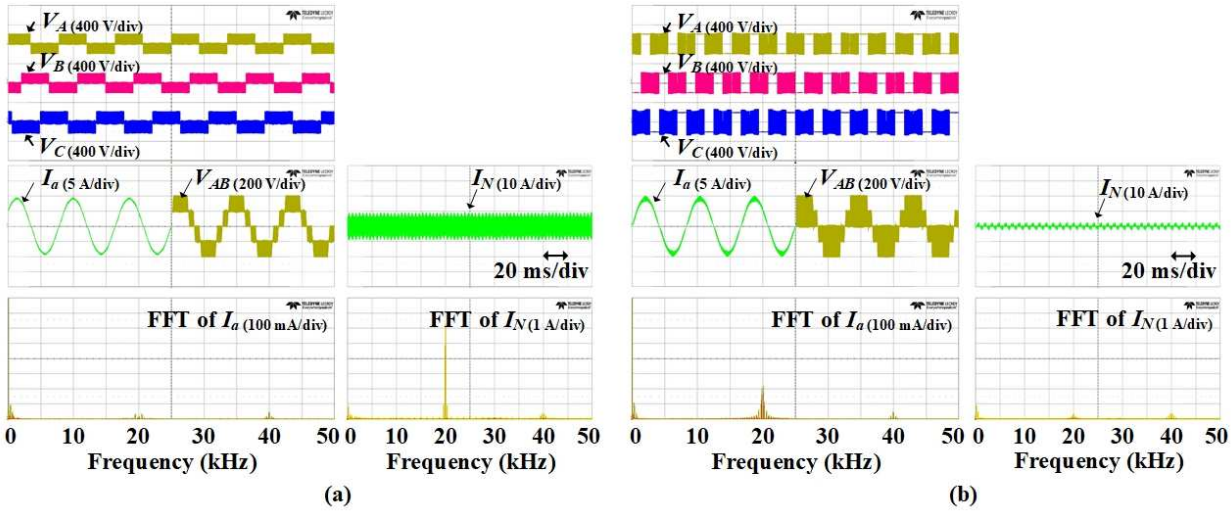

Fig. 12: Experimental results of the pole voltages, line-to-line voltage V_{AB}, the output current, and I_N in time and frequency domains (a) conventional SVM (b) proposed PWM method.

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