# Study on the gate loop design and its impact on switching characteristics of GaN Transistors

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## Keywords

«Parasitic inductance», «Gallium Nitride (GaN) », «Packaging», «Wide bandgap», «HEMT».

## Abstract

This paper studies design parameters for the gate loop of GaN-based transistors. To achieve stable and fast switching of the GaN transistors aiming at MHz-range operation, different layout factors and their influence on gate loop inductances are investigated in simulations and measurements. Experimental results demonstrating the impact of driver ICs and their packages on the switching characteristics are presented as well.

## Introduction

Wide bandgap gallium nitride (GaN)-based high-electron-mobility transistors (HEMTs) have low on-resistance and low parasitic capacitances compared with their Si-counterparts, which enable faster switching, lower losses, and smaller size of passive components [1]. These advantages make them increasingly preferred in high frequency and high efficiency converters. To achieve fast switching and take full advantage of GaN HEMTs aiming at MHz-range operation, both, the power loop and the gate loop have to be optimized. This paper focuses on the gate loop design. The gate loop inductance decreases the slew rate of the gate current and thus lowers the switching speed. Further, a large gate loop inductance forms a resonance circuit together with parasitic capacitances, causing overshoots and oscillations in the gate-source voltage. This degrades the electromagnetic interference (EMI) performance, efficiency, and device stability. The issue can be partially mitigated by large gate resistors damping critical oscillations, but this in turn limits the design of switching speed optimization [2, 3]. Generally, the gate loop inductance consists of the gate loop self-inductance and the common source inductance. The common source inductance quantifying the mutual interaction between the power and the gate loop has been studied in [4]. This paper focuses on the gate loop self-inductance $L_g$ which quantifies the induced voltage in the gate loop due to the time-variant gate loop current.

To reduce the gate loop inductance and achieve a compact design, some manufacturers integrate the driver with GaN transistors [5, 6]. However, most of the commercial GaN transistors are still discrete devices. Several well-known “rule of thumb” recommendations for a proper gate loop layout to reduce $L_g$ can be found in the driver IC datasheets or application notes [7, 8], e.g., placing the driver ICs close

to power devices and reducing the length of current paths. However, to the authors' best knowledge, no quantitative investigations on the cause of the gate-loop inductance have been carried out to identify the most influential factors for GaN transistors. In order to optimize switching performance of GaN-based devices, further investigations are needed to establish a more systematic guiding for the gate loop design with discrete gate drivers.

As a key element in the gate loop circuit, the driver device itself has a large impact on the switching characteristics of GaN transistors. First, the parasitic inductances of the driver IC package directly contribute to the gate loop inductance. Second, additional parameters, such as the sink and source current capability of the driver ICs, internal parasitic resistances, and the different internal driver circuits, influence the switching performance. In recent years, many studies on the modeling and quantification of parasitic inductances of GaN transistors packages have been reported [9, 10]. Experimental tests were performed in [9] to extract the package parasitic inductances of the wide band-gap transistor in a through-hole technology (THT) package. In [10], the parasitic inductances of a cascode GaN transistor in a THT package are extracted using the 3D FEM simulation tool Ansoft Q3D Extractor and then used to build a lumped-element Spice simulation model. However, so far, the impact of different driver packages has not been studied in detail. Besides, these methods are difficult to adapt to the GaN-transistor drivers, since these are commonly surface-mounted devices (SMD) whose dimensions are much smaller than THT packages. Furthermore, assembly details of internal lead-frame and bonding geometry are usually not published. In addition, although it is well-known that the driver affects the switching behavior, it has not been studied in detail how large this effect is for GaN transistors, especially considering drivers with similar ratings stated in their datasheets. Thus, in this paper, we compare the switching behavior of one selected transistor type combined with different driver ICs while the PCB layout is kept widely identical, and use the experimental results in real operation conditions to directly show the impact of drivers and gain more straightforward insight into them.

The paper is organized as follows: The impact of different layout-related parameters on the gate loop inductance is evaluated with measurements and 3D FEM simulations in section 2. Section 3 demonstrates the impact of the driver ICs and their packages on the switching behavior of GaN transistors with experimental results. Conclusions are indicated at the end.

## Parameter study of gate loop inductance

The gate loop self-inductance $L_g$ is a result of the PCB layout as well as the incorporated passive and active device packages or chip dies. In order to optimize the converter design and achieve fast and stable switching transients, it is important to quantify the gate loop inductances and the contribution of different parameters, especially when a compromise between them is required. Therefore, the following different cases are compared (**Table I**) considering the *1EDN7511B* gate driver with a commonly used SOT-23 package [12]. Case 1 aims to achieve an optimal reference design case, in which the components are placed densely, and the 2$^{nd}$ layer of a 4-layer PCB is used as a ground return to reduce the vertical cross-section area of the gate loop enabling effective flux compensation. In case 2, the bottom layer is used as a ground return in order to compare a 2-layer design with a multi-layer design. In case 3, the 2$^{nd}$ layer is again used as a ground return path, but the bypass capacitors are moved 5 mm away from the driver. Lastly, in case 4, the load capacitor emulating the GaN transistors input capacitance is moved 10 mm away from the driver. Case 3 and case 4 serve for evaluating the influence of the position and distance of the components on $L_g$. Both, measurements and simulations are conducted to quantify $L_g$ and to study the layout's impact.

Fig. 1 depicts the circuit diagram used for experimental investigation. In the measurement setup, the active GaN transistor is replaced by a fixed NP0 ceramic load capacitor $C_{load}$, which avoids the voltage-dependent nonlinearity of the transistor input capacitance and thus reduces complexity of the subsequent analysis. The load capacitor $C_{load}$=100 pF is in a similar range as the studied transistor's input capacitance $C_{iss}$ (Fig. 7) and as for other commercial GaN transistors [13] to ensure a representative behavior. The transient gate current $i_g$ is acquired through the voltage across the gate resistor $R_{on}$ and $R_{off}$, and the voltage is measured by a 1 GHz high bandwidth voltage probe TPP1000.

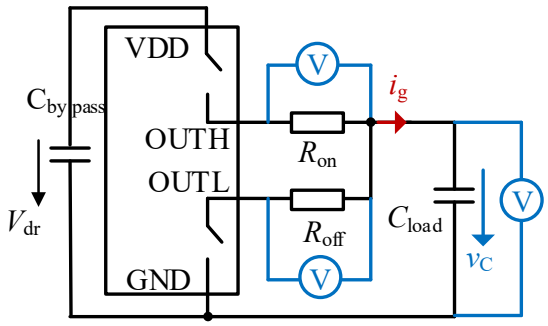



Fig. 1: Circuit diagram of the measurement setup

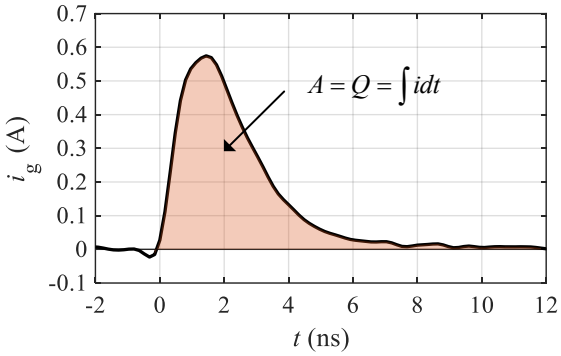



Fig. 2: Charge calculation using gate current at turn-on of case 1

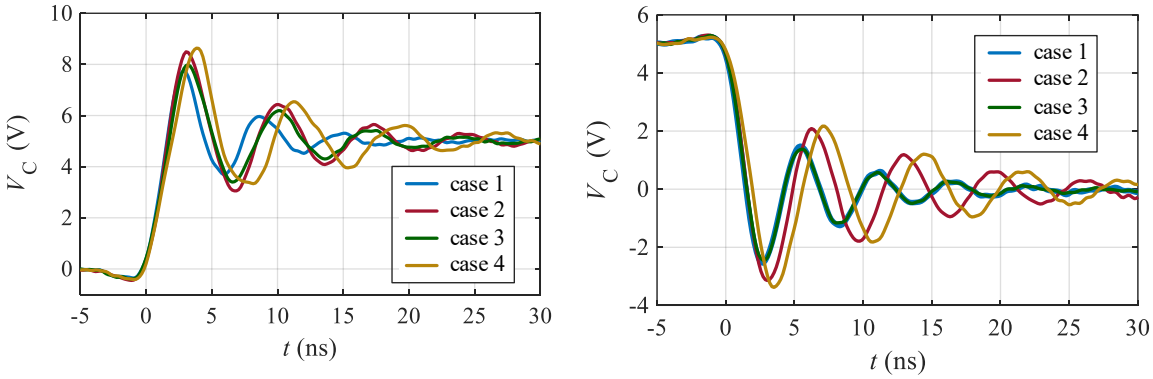



Fig. 3: Comparison of the experimental waveforms of $v_C$ at (a) turn-on and (b) turn-off in the different studied cases with a driver supply voltage $V_{dr}$=5 V, gate resistors $R_{on}$=$R_{off}$=1 Ω, and load capacitor $C_{load}$=100 pF.

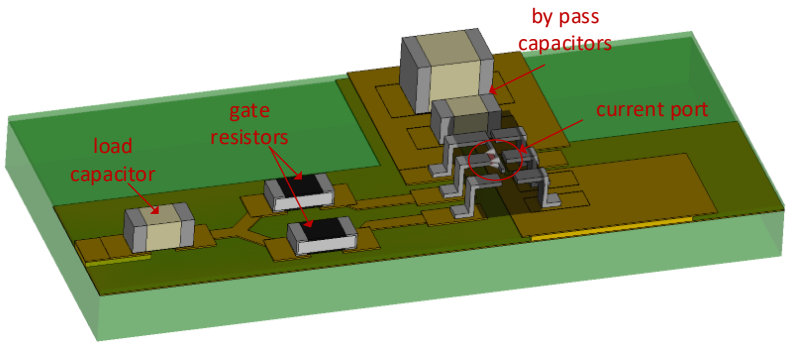



Fig. 4: 3D model of case 1 used in CST for parameter extraction

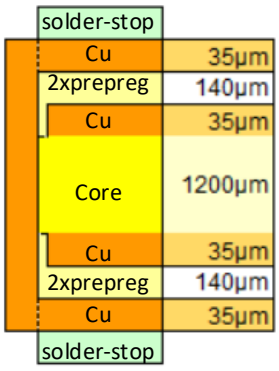



Fig. 5: Dimension of the used 4-layer PCB [15]

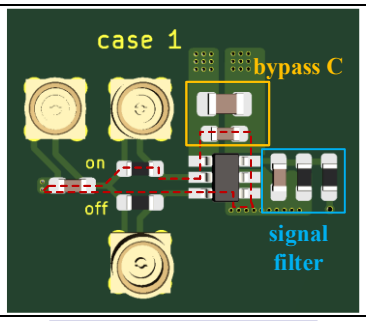
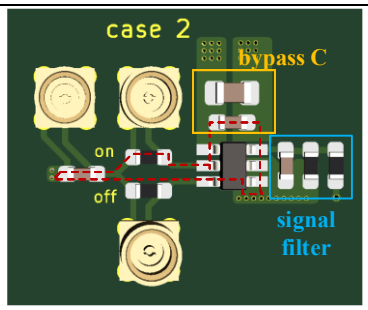
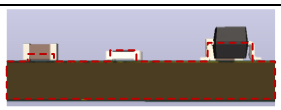
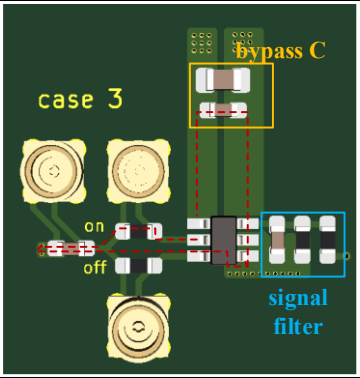
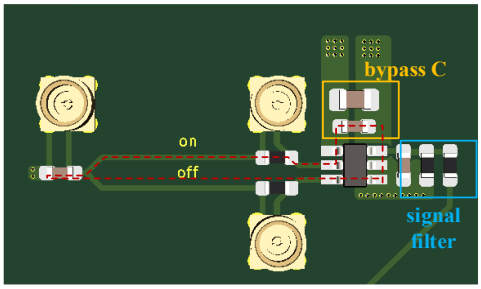
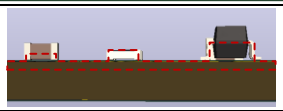
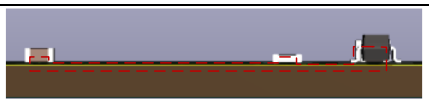
For an experimental characterization of the gate loop inductance, the voltage response (Fig. 3) to a turn-on and turn-off step signal at the driver output is measured. The gate loop forms a series RLC resonance network described by its transfer function

$$G(s) = \frac{Y(s)}{U(s)} = \frac{1}{s^2 LC + sRC + 1}. \quad (1)$$

where $s$ is the Laplace transform frequency parameter. The $R$ is the sum of the gate external resistor and the driver internal resistor which is unknown. Since $R$ and $L$ are both unknown parameters so far, $L$ is determined by fitting the transient gate current response using time-domain data and a known $C$ value. It should be noted here that $C$ is the sum of the load capacitance $C_{load}$, the parasitic capacitance resulting from the PCB $C_{par,PCB}$ , and the driver's parasitic output capacitance $C_{par,driver}$. For example, the extracted $C_{par,PCB}$ though FEM simulation equals 4 pF for case 1. The driver's $C_{par,driver}$ is measured with a Keithley parameter analyzer and equals 84 pF. Thus, the total $C$=188 pF can be calculated. To verify the results, the total charge is computed by integrating the transient gate current (Fig. 2). Using equation 2, $C$ results in 185 pF. The good agreement of these two values suggests a satisfying reliability in the analysis and results.

$$C = \frac{Q}{V} = \frac{\int idt}{V} \tag{2}$$

**Table I: Studied cases and extracted $L_g$**

| | **Case 1** | **Case 2** |
|---|---|---|
| Top view of layout and current paths |  |  |
| Cross-section of layout and current paths |  |  |
| $L_{g,meas}$ (turn on loop /turn off loop) | 4.2 nH/3.8 nH | 5.9 nH/5.5 nH |
| $L_{g,sim}$ (turn on/turn off, @100 MHz) | 3.9 nH/ 3.4 nH | 7.6 nH/6.6 nH |
| | **Case 3** | **Case 4** |
| Top view of layout and current paths |  |  |
| Cross-section of layout and current paths |  |  |
| $L_{g,meas}$ (turn on loop /turn off loop) | 5.7 nH/3.8 nH | 7.5 nH/6.7 nH |
| $L_{g,sim}$ (turn on/turn off, @100 MHz) | 5.4 nH/3.4 nH | 6.6 nH/6.1 nH |

To verify the measurement results, the parasitic parameters are also characterized in simulation. The 3D model of the layout is imported to the 3D FEM field simulation tool CST Studio Suite [14] to extract

the inductance values (Fig. 4). The vertical dimensions of the employed PCB are shown in Fig. 5 [15]. In this simulation, capacitors are built as solid copper blocks. The resistor models are built according to the datasheet specifications [16], consisting of a resistive layer on top (black), alumina ceramic substrate in the middle (white), and nickel terminations (silver) (Fig. 4). However, the accurate dimensions of each layer are not specified in the datasheet and thus they are only estimated, which potentially results in a slight inaccuracy of the 3D models. To reduce the meshing complexity, the cylindrical vias used to interconnect different copper layers are modeled by solid copper blocks. The structure inside the driver package and the signal path is not included in the model. The transistor die is assumed to be at the height of the lead frames and in the middle of package. A current port used for current excitation in the magnetoquasistatic simulation is therefore placed in the middle of the driver.

Based on this model, the impact of different factors can be studied. The simulation results agree well with the measurement results. The remaining difference can be attributed to the simplified driver-internal structure as well as the simplified models of the capacitors and resistors. Moreover, it is worth mentioning that $L_g$ differs between turn-on and turn-off gate loop, and thus they should be considered separately in the converter design. Case 1 shows the lowest $L_g$ as expected. Both, the experimental results $L_{g,meas}$ and simulation results $L_{g,sim}$ show that the multi-layer PCB can significantly reduce $L_g$ for both, turn-on and turn-off gate loop. However, the reduction in $L_g$ (approx. 30% in the measurement and approx. 50% in the simulation) is much smaller than the reduced distance between the power flow layer and the return ground layer (91%), which illustrates the contribution of the remaining active and passive circuit components to $L_g$. The bypass capacitors positioned further away results in an increased $L_g$ for the turn-on gate loop, but for turn-off this is less relevant. The reason is that, assuming a unipolar gate-voltage supply as in our case-study, only the turn-on gate current flows through the bypass capacitors. An extended distance of 5 mm from the bypass capacitors to the driver IC in a 4-layer vertical design leads to an increase by approx. 1.5 nH of the turn-on gate loop inductance. In contrast, the farther positioned load capacitor (emulating the GaN transistor) increases $L_g$ in both turn-on and turn off gate loop. A further extended distance of 10 mm between the load capacitor and the driver leads to an increase of $L_g$ by approx. 3 nH.

## Impact of the driver devices on switching characteristics

In this section, we show the impact of different driver ICs and their packages on the switching characteristics of GaN devices with experimental results in hard-switched double-pulse tests. The measurements are performed using 100 V/150 mΩ Schottky-gate type GaN transistors with −2.5 V threshold voltage fabricated by Ferdinand-Braun-Institute (FBH) [17]. To ensure comparability, driver ICs with similar ratings as given in the datasheets [7, 12, 18, 19] (**Table II**) are used in the measurements.

The investigated GaN transistors are fabricated with a Schottky gate, which means a parasitic Schottky diode is formed below the gate. Similar to the GaN Gate Injection Transistor (GIT), the non-insulating gate requires a continuous current sourced into the gate during on-state [20, 21]. The I-V curve of the GaN transistor's parasitic gate-source diode is shown in Fig. 6a. Considering commercially available driver ICs, the Panasonic driver *AN34092B* integrating a current source (Fig. 6b) or a conventional voltage source driver combined with an RC-type driver network as well as a NMOS aiming to discharge the boost $C_s$ (Fig. 6c) could be used to drive non-insulating gate-type GaN transistors [22]. The gate loop parameters used in the tests are listed in **Table III**.

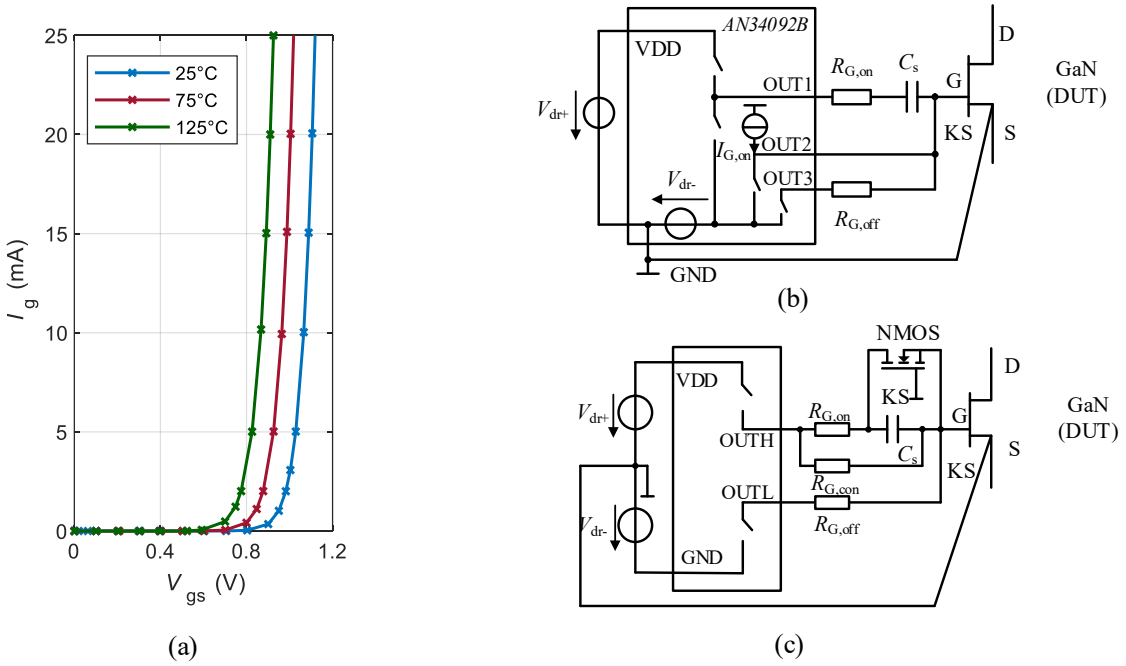
The driver type i.e. current source type driver or voltage source driver directly affects the switching behavior. Besides, even when using standard voltage source driver ICs with almost identical electrical ratings and assembled in the same package type, the switching transients appear to be notably different. Moreover, employing the same driver IC in different packages results in obvious differences in the switching transitions. To study the impact of these factors, the transient waveforms of the GaN transistor's gate-source voltage $v_{gs}$, drain-source voltage $v_{ds}$, and drain current $i_d$ with different driver ICs and packages but almost identical PCB layout are shown in Fig. 8. The comparison of switching characteristics such as the slew rates of the drain-source voltage $v_{ds}$ and drain-current $i_{d,}$ as well as the

peak value of $v_{ds}$ during turn-off and $i_d$ during turn-on are shown in Fig. 9, Fig. 10, and Fig. 11, respectively.

The current source driver IC *AN34092B* (Fig. 8b) achieves an obviously longer $v_{gs}$ rise time compared with the voltage source driver IC *1EDN7550B* (Fig. 8a), although the given maximal sourcing current of *AN34092B* is much higher and sourcing resistance is lower than *1EDN7550B* (**Table II**). The GaN transistor's absolute slew rate values of drain-source-voltage and drain-current during turn-on with *AN34092B* are thus significantly lower compared with *1EDN7550B* (Fig. 9). As for turn-off, the $v_{gs}$ with *AN34092B* shows more oscillations, which possibly results from the combination of two loops to turn the transistor off due to the active miller clamp function of the *AN34092B*, i.e., both OUT2 and OUT3 affect switching-off [19]. Consequently, $v_{ds}$ and $i_d$ exhibit stronger oscillations and higher peak values during turn-off transitions using *AN34092B*.

**Table II: Parameters of the drivers**

| | 1EDN7511 | UCC27511 | 1EDN7550B | 1EDN7550U | AN34092B |
|---|---|---|---|---|---|
| Package | SOT23-6 | SOT23-6 | SOT23-6 | TSNP-6 | HQFN-16 |
| Sourcing current | 4 A | 4 A | 4 A | 4 A | 6 A |
| Sinking current | -8 A | -8 A | -8 A | -8 A | -9 A (sum of $I_{OUT2}$ and $I_{OUT3}$) |
| Sourcing resistance | 0.85 Ω | 5 Ω | 0.85 Ω | 0.85 Ω | 0.8 Ω |
| Sinking resistance | 0.35 Ω | 0.45 Ω | 0.35 Ω | 0.35 Ω | 0.5 Ω (OUT2)<br>1 Ω (OUT3) |




(a) (b) (c)

Fig. 6: (a) The I-V characteristics of the parasitic gate-source diode with open drain terminal for Schottky-type Gate GaN transistor fabricated by FBH. (b) Gate drive circuits for non-insulating gate GaN transistors with the current source driver *AN34092B*. (c) Gate drive circuits for non-insulating gate GaN transistors with standard voltage source driver combined with RC-type driver network and active boost-capacitor discharge [22].

**Table III: Gate loop parameters**

| Parameters | Symbol | Value |
|---|---|---|
| Turn-on gate resistor | $R_{G,on}$ | 5.6 Ω |
| Turn-off gate resistor | $R_{G,off}$ | 2 Ω |
| Continuous gate resistor | $R_{G,con}$ | 3.9 Ω |
| Boost capacitor | $C_s$ | 330 pF |
| Continuous gate current turn-on | $I_{G,on}$ | 5 mA |
| Turn-on gate voltage | $V_{dr+}$ | 5 V |
| Turn-off gate voltage | $V_{dr-}$ | −5 V |

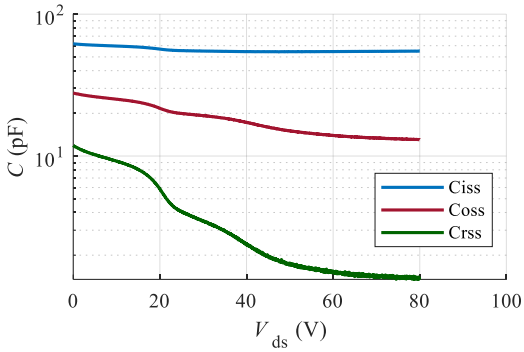



Fig. 7: Capacitance-voltage profile of the GaN transistor with $V_{GS}$=−6 V (100 kHz and 100 mV RMS small signal measurement with a Keithley parameter analyzer)

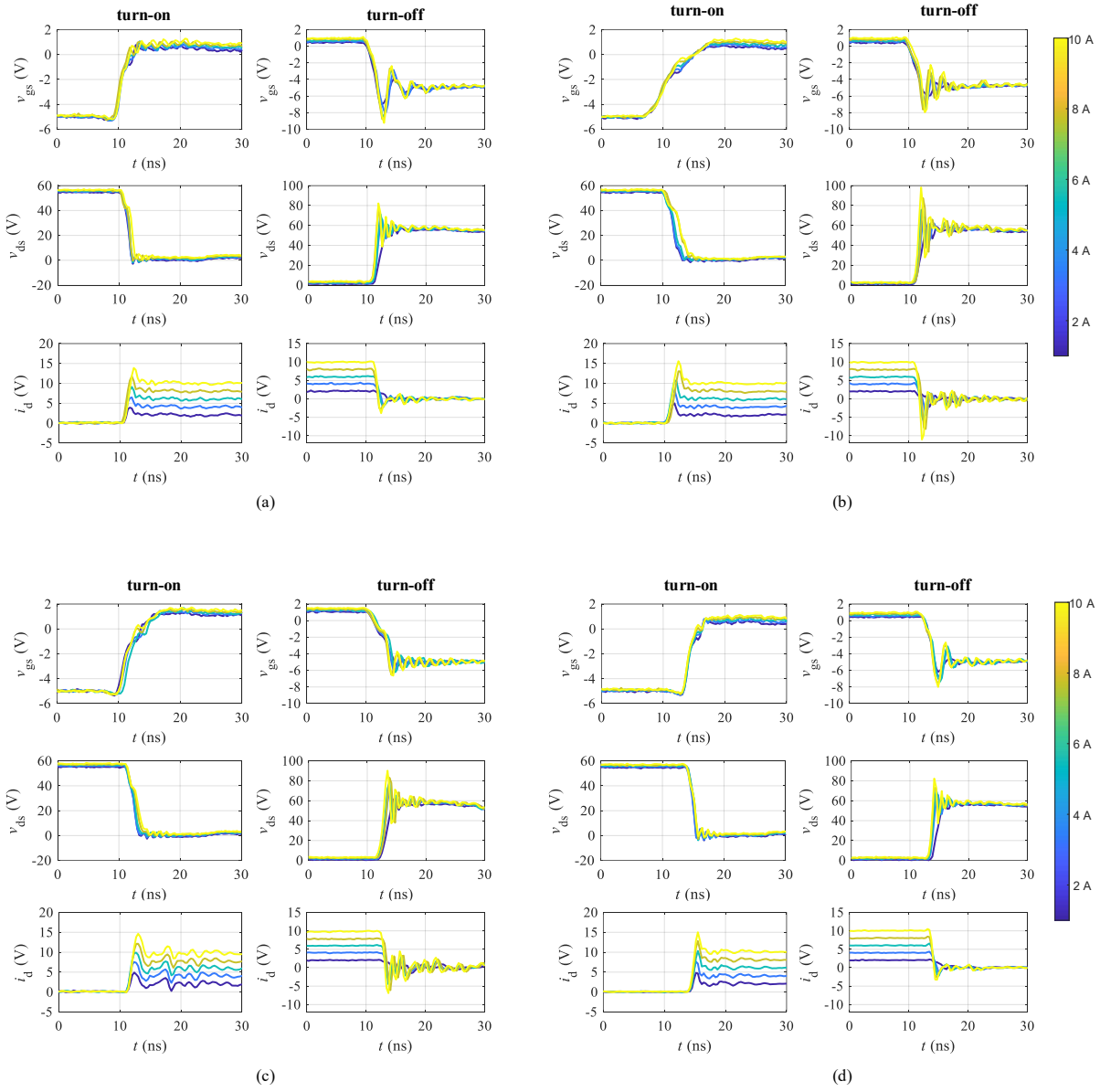



Fig. 8: Switching transitions of the GaN transistors at dc-link voltage $V_{dc}$=50 V, load current $I_L$=2…10 A with (a) driver *1EDN7550B* with SOT23-6 package, (b) driver *AN34092B* with HQFN package, (c) driver *UCC27511* with SOT23-6 package and (d) driver *1EDN7550U* with TSNP-6 package.

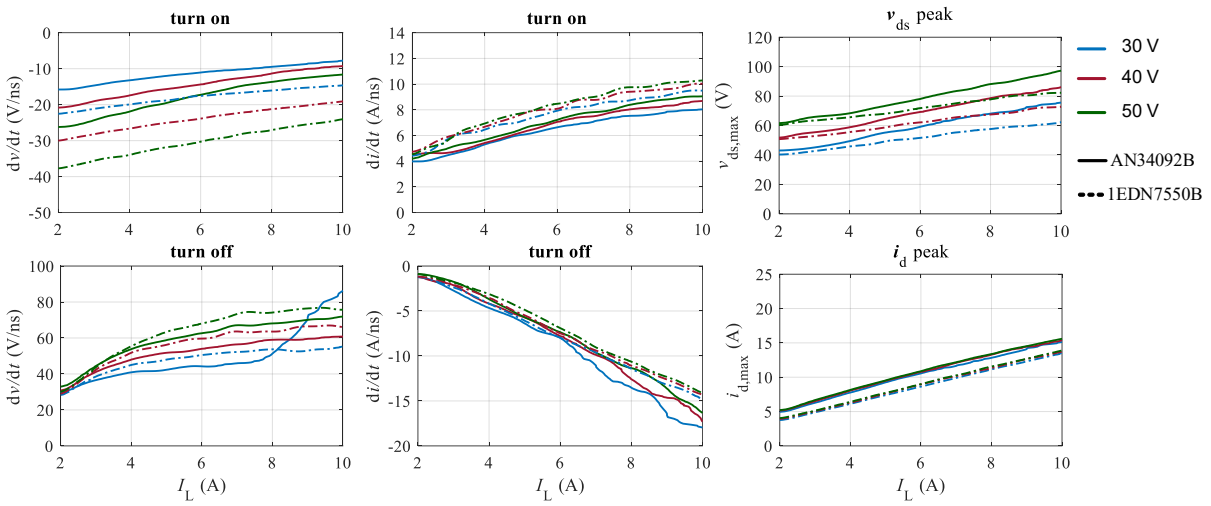



Fig. 9: Comparison of the switching characteristics between the current source driver and voltage source driver to drive non-insulating gate type GaN transistors for (a) slew rate of drain-source voltage $v_{ds}$, (b) slew rate of drain-current $i_d$ and (c) peak value of $v_{ds}$ and $i_d$.

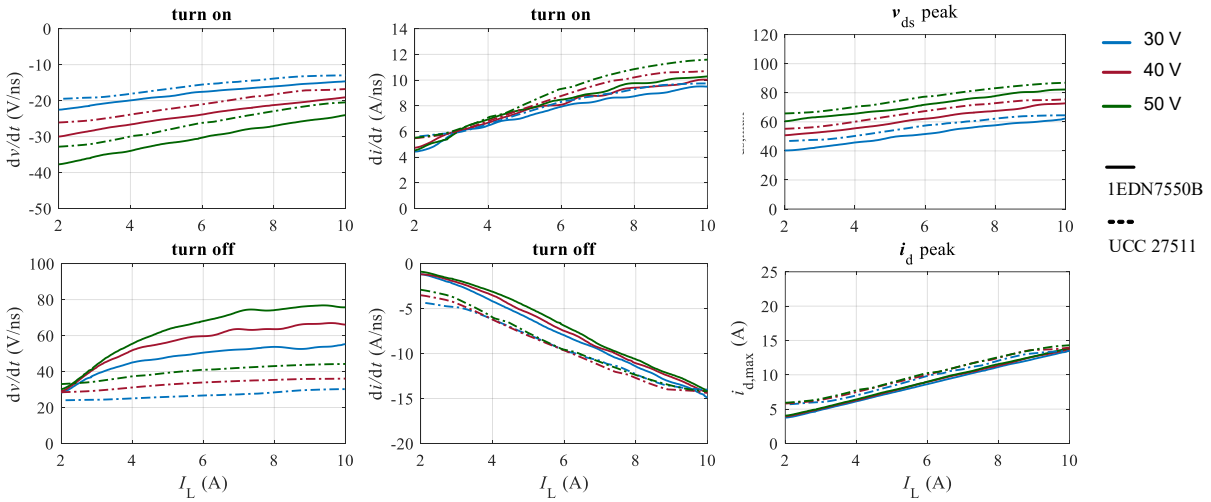



Fig. 10: Comparison of the switching characteristics between different voltage source driver ICs in the same package for (a) slew rate of drain-source voltage $v_{ds}$, (b) slew rate of drain current $i_d$ and (c) peak value of $v_{ds}$ and $i_d$.

Comparing the different standard voltage drivers with the same package, the slew rate of $v_{gs}$ in both, turn-on and turn-off transitions is lower for driver IC *UCC27511* (Fig. 8c) than for driver IC *1EDN7550B* (Fig. 8a). The slew rate of the drain-source-voltage $v_{ds}$ and drain current $i_d$ is thus higher using *1EDN7550B* (Fig. 10), especially at turn-off. However, the turn-off voltage overshoot is still lower and the $i_d$ in both turn-on and turn-off, as well as $v_{ds}$ at turn-off, show fewer oscillations (Fig. 8) which is likely related to the lower parasitic inductances of *1EDN7550B*. Since the PCB layouts are almost identical for the two drivers, the influence from this layout is neglectable. Thus, the observed deviation in switching characteristics can be mainly attributed to the driver's internal structure.

The impact of different driver packages is investigated by comparing *1EDN7550B* (Fig. 8a) and *1EDN7550U* (Fig. 8d). Both drivers are based on the same IC chip but are embedded into different packages, a larger SOT package and a smaller TPSN package. The gate-source voltage $v_{gs}$ for *1EDN7550U* in the smaller TPSN package shows slightly fewer oscillations at turn-on and an obvious lower negative peak value at turn-off (−8 V vs. −10 V). However, the drain-source voltage $v_{ds}$ for *1EDN7550U* shows slightly stronger oscillations than $v_{ds}$ for *1EDN7550B,* since the $v_{ds}$ slew rates with

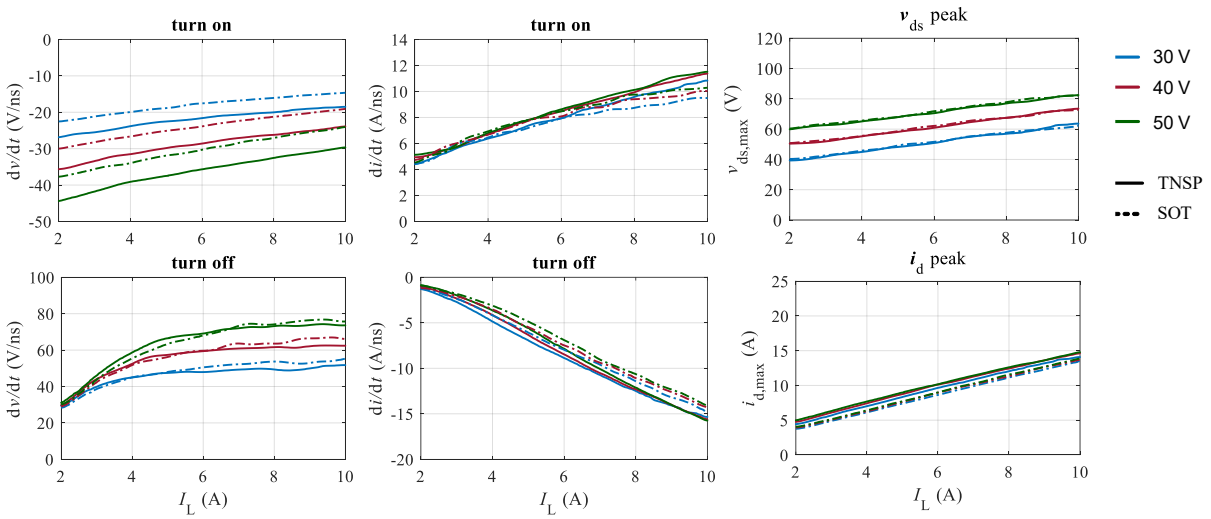
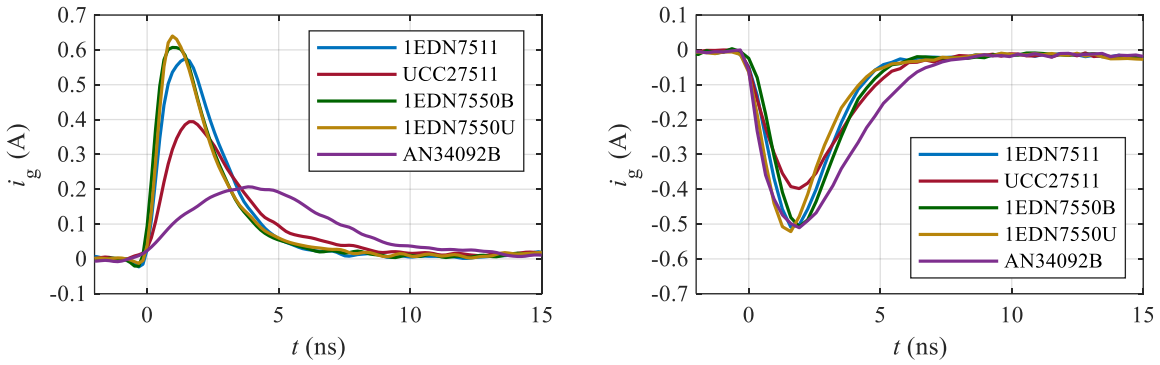



Fig. 11: Comparison of the switching characteristics between the same driver ICs in different packages: (a) slew rate of drain-source voltage $v_{ds}$, (b) slew rate of drain-current $i_d$ and (c) peak value of $v_{ds}$ and $i_d$.




(a) (b)

Fig. 12: Comparison of the (a) turn-on gate current and (b) turn-off gate current of the used drivers at a voltage difference ΔV =10 V, gate resistors $R_{on}$ =$R_{off}$ =10 Ω and load capacitor $C_{load}$ =100 pF in the measurement setup shown in Fig. 1.

*1EDN7550U* are higher (Fig. 11). Overall, the smaller driver package is beneficial not only to achieve a more compact design but also to achieve a stable and less oscillating gate-source voltage, and a faster switching.

To study the origins of the differences caused by the driver ICs and their packages, the gate currents are measured during turn-on and turn-off transitions using the measurement setup shown in Fig. 1. Fig. 12 demonstrates that different driver ICs achieve different peak values and slew rates of the gate current $i_g$. The different peak values suggest that despite the same current ratings, the drivers have different current capabilities and parasitic resistances. Moreover, in all driver ICs the achieved gate current peak value is much lower than the datasheet rating. The expected value should be around 1 A, considering a driver voltage of 10 V and external gate resistors of 10 Ω, while the current source driver IC *AN34092B* achieves only a peak value of 0.2 A. The different slew rates of the gate current suggest that the drivers have different internal inductances and different switching speed, despite the fact that the package type of *1EDN7550B, 1EDN7511* and *UCC27511* is the same. The area below the $i_g$-curve equals to the charge of the total capacitance *C*. Hence, differences in the calculated charge indicate different parasitic output capacitances of the driver ICs, as both, the load capacitance and the parasitic layout capacitance remain unchanged.

At turn-on, driver *1EDN7550B* achieves a higher gate current peak value and slew rate than drivers *UCC27511* and *AN34092B*. This agrees with the previously presented switching tests in hard-switched double-pulse mode, where *1EDN7550B* exhibits faster turn-on switching and fewer oscillations. The differences of the gate current during turn-off are smaller among the driver ICs (Fig. 12b), which coincides with the switching test results, which show a more pronounced difference at turn-on than at turn off (Fig. 9, Fig. 10, and Fig. 11).

To achieve fast switching of GaN transistors, a fast and high gate current after switching signals are applied is desirable. The results indicate the importance of proper driver selection concerning both, current capability as well as driver package in order to exploit the fast switching potential of GaN transistors.

## Conclusion

This work studies the gate loop design influencing parameters in order to achieve high switching performance of GaN transistors. The impact of a multi-layer PCB and the placement of devices and passive components on the gate inductance $L_g$ are quantitatively evaluated to enable a straightforward insight to the resulting $L_g$-increase. The effects of the driver ICs and their packages on the switching characteristics are shown with experimental results. Our investigations prove the significant influence of electrical gate driver parameters including parasitic inductances and capacitances as well as peak current capability on the switching behaviors.

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