Stability Analysis and Optimal Control Design for Dual-Loop Voltage-Controlled Grid-Connected Inverters

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***Abstract*-- This paper analyzes the stability of digitally dual-loop voltage-controlled inverters with consideration of grid impedance. It is revealed that both the digital delay and controller affect the system stability through adjusting the phase at the resonant frequency of the LCL filter. Then an optimal control for inner current loop is proposed to deal with different switching frequencies. Through tunning the feedback gain of inner current loop, the control scheme can cope with different switching frequencies or delays to keep system stable. Then the stable regions presented as the value range of current feedback gain are derived. Simulation and experiment validate the stability analysis and effectiveness of the proposed control.**

***Index Terms*—voltage-controlled inverter, dual-loop control, digital delay, stability analysis.**

I. Introduction

With grid-forming ability, the voltage-controlled inverters have advantages over current-controlled inverters when connected to weak grid[1],[2]. The research on grid-connected voltage-controlled inverters such as virtual synchronous generator and virtual synchronous machine[3],[4], have aroused great attention. Although the upper layer controls are different, the basic control is the same, which is the high-quality and effective voltage control. The existing research on the stability of voltage-controlled inverters mainly focus on the standalone mode, barely consider the effect of grid impedance. The LC filter of voltage-controlled inverter is changed to LCL filter when connected to the inductive grid, which lead to the deviation of resonant frequency.

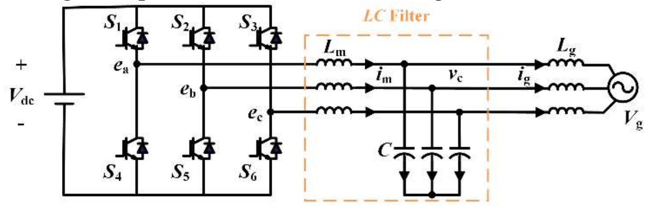
There are mainly two voltage regulation controls for voltage-controlled inverters: 1)single-loop voltage control[5-7] and 2)dual-loop voltage-current control.[8-10] The single-loop voltage control is simple but suffers from the issues of constrained loop bandwidth and lack of overcurrent protection.[10] On the other hand, by introducing the inner current loop, the dual-loop voltage-current can provide enhanced damping and solve the issues of single-loop voltage control. It has been shown that the t inner current loop is equivalent to a virtual impedance in parallel with the filter capacitor or in series with the filter inductor[11-13]. However, the virtual impedance is affected by the digital delay and the real part of the virtual impedance may become negative and cause instability[12]. It is revealed that the negative damping occurs above the one-sixth of sampling frequency($f_s/6$). Therefore, the dual-loop voltage-current control is constrained in the case of pulse ratio, which is caused by the increase of digital delay.[6]

To fill the gap of stability analysis of voltage-controlled grid-connected inverters and solve the deficiency of dual-loop voltage-current control under low pulse ratio, this paper analyzes the stability of digitally dual-loop voltage-controlled inverters with consideration of grid impedance. Based on the stability analysis, an optimal control for inner current loop is proposed to deal with different switching frequencies.

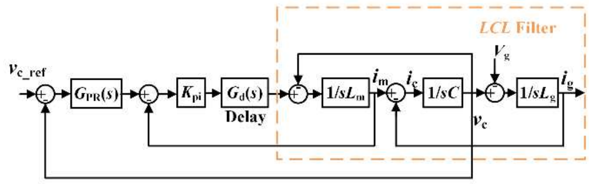
The remaining parts of this paper are organized as follows: Section II presents the topology and control scheme of the dual-loop voltage-controlled grid-connected inverters considering delay and grid inductance. Section III introduces the stability analysis and optimal control of the inner current loop, the stable regions in different switching frequencies are derived. Section IV shows the simulation and experiment results. The conclusions are drawn in the last section.

II. Dual-Loop Control Structure of Voltage-Controlled Grid-Connected Inverters

Fig.1 shows the topology and control scheme of voltage-controlled grid-connected inverter. The grid voltage is assumed balanced so per-phase diagrams used for analysis can be depicted in Fig.1(b). L_m and C are the inductor and capacitor of the LC filter to attenuate the switching harmonics. The grid is assumed inductive and L_g is the grid impedance. The LC filter and grid inductance



(a)



(b)

Fig. 1. Dual-loop voltage-controlled grid-connected inverters. (a)Topology. (b) Control scheme

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constitute the LCL filter. The parasitic resistance of the inductor and capacitor is neglected to consider the worst case scenario.

As Fig1.(b) shows, the upper layer control(such as droop control and VSG) will synthesize the voltage reference v_{c_ref}. Then the filter capacitor voltage v_c is fed back as the control variable of outer voltage loop while the filter inductor current i_m is fed back as the control variable of inner current loop. The voltage regulator $G_{PR}(s)$ adopts proportional- vector resonant controller, which can be expressed as (1)

$$G_{\mathrm{PR}}(s)=K_{\mathrm{PR}}+\frac{K_{\mathrm{r1}}}{s-\mathrm{j}\omega_1} \tag{1}$$

Where ω_1 is the fundamental frequency of output voltage. The vector resonant controller can ensure the voltage tracking at ω_1 without error. The current regulators is a proportional controller with gain of K_{pi}. $G_d(s)$ is the digital delay which is comprised of computation delay and PWM delay and can be expressed as (2)

$$G_{\mathrm{d}}(s)=e^{-1.5T_{\mathrm{s}}\cdot s} \tag{2}$$

Where T_S is the sampling period. Referring to Fig.1(b), the loop gain can be derived as (3)

$$\begin{aligned} T_1(s) &= \frac{\left[K_{\mathrm{pi}}\left(s^2L_{\mathrm{g}}C+1\right)+K_{\mathrm{pi}}G_{\mathrm{PR}}(s)\cdot sL_{\mathrm{g}}\right]e^{-1.5T_{\mathrm{s}}\cdot s}}{sL_{\mathrm{m}}L_{\mathrm{g}}C+s\left(L_{\mathrm{m}}+L_{\mathrm{g}}\right)} \\ &= \frac{\left[K_{\mathrm{pi}}\left(s^2L_{\mathrm{g}}C+1\right)+K_{\mathrm{pi}}G_{\mathrm{PR}}(s)\cdot sL_{\mathrm{g}}\right]e^{-1.5T_{\mathrm{s}}\cdot s}}{sL_{\mathrm{m}}L_{\mathrm{g}}C\left(s^2+\omega_{\mathrm{r}}^2\right)} \end{aligned} \tag{3}$$

Where ω_r is the LCL filter resonance angular frequency and can be expressed as (4).

$$\omega_r=\sqrt{\frac{L_m+L_g}{L_mL_gC}}=2\pi f_r \tag{4}$$

With the loop gain, the stability of the dual-loop voltage-controlled grid-connected inverters can be analyzed.

III. Stability Analysis and Optimal Control of Dual-Loop Voltage-Controlled Grid-Connected Inverters

A. Stability Analysis

The loop gain in (3) can be divided into two parts: the numerator and the denominator, which can be expressed as (5)

$$\begin{cases} G_{\mathrm{nu}}(s)=\left[K_{\mathrm{pi}}\left(s^2L_{\mathrm{g}}C+1\right)+K_{\mathrm{pi}}G_{\mathrm{PR}}(s)\cdot sL_{\mathrm{g}}\right]e^{-1.5T_{\mathrm{s}}\cdot s} \\ G_{\mathrm{de}}(s)=\dfrac{1}{sL_{\mathrm{m}}L_{\mathrm{g}}C\left(s^2+\omega_{\mathrm{r}}^2\right)} \end{cases} \tag{5}$$

$G_{de}(s)$ is the typical characteristic of LCL filter, whose bode plot is shown in Fig.2(a). It can be found that there is a resonant peak with phase crossing -180° at ω_r, which is naturally unstable. Therefore, $G_{nu}(s)$ plays a role of phase adjustment for $G_{de}(s)$ especially the phase at ω_r to avoid -180° phase crossing at the resonant peak. $G_{nu}(s)$ can also be divided into two parts: the controller part(in square brackets) and the delay part ($G_d(s)$), they can provide

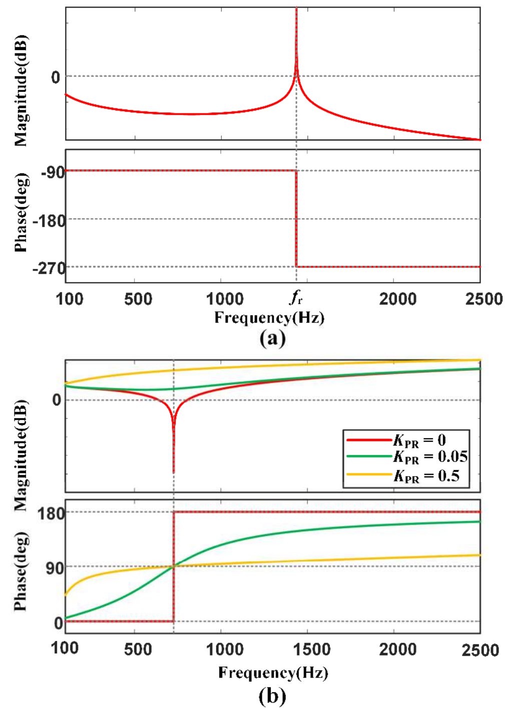

Fig. 2. Bode plot of $G_{de}(s)$ and controller parts of $G_{nu}(s)$ (a) $G_{de}(s)$. (b) Controller parts of $G_{nu}(s)$ with different K_{PR}

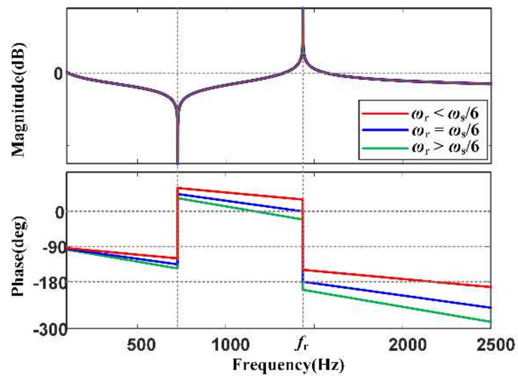

Fig. 3. Bode plot of $T(s)$ with different switching frequencies

different phase shift for $G_{de}(s)$ at ω_r and lead to different stable and unstable condition.

With the parameters listed in Table I, Fig.2(b) shows the bode plot of the controller part of $G_{nu}(s)$ with different K_{PR}. As shown in Fig.2(b), there is imaginary axis zero for the controller part of $G_{nu}(s)$ when K_{pr}=0, and 180° phase lead can be provided above the frequency of the zero in this case. However, with the increase of K_{pr}, the phase lead will increase below the zero frequency while the phase lead decreases above the zero frequency and the phase lead provided by the controller part will gradually approach 90° . Therefore, if the digital delay is not considered, the phase lead provided by the controller part will adjust the phase of LCL resonant peak to a critical stable state. But the delay part $G_d(s)$, on the other hand, will cause phase lag and make the system change from critical stability to instability. Instead, when K_{pr} = 0, the controller part can provide 180° phase lead for the LCL resonant peak, which extend the phase margin for the phase lag caused by delay. Generally, it can be seen that the proportional part K_{pr} of

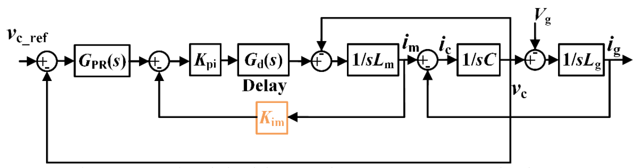

Fig. 4. Optimal dual-loop voltage-current control scheme

TABLE I
SYSTEM PARAMETERS

Parameter	*Symbol*	*Value*
Inverter-side inductor	L_m	1.2mH
Filter capacitor	C	12μF
Grid inductance	L_g	7mH
Resonant frequency	f_r	1.435kHZ
Fundamental frequency	f_1	50HZ
Switching frequency	f_{sw}	8/12kHZ
Sampling frequency	f_s	8/12kHZ
Vector resonant regulator gain	K_{r1}	100
Current regulator proportion	K_{pi}	2.5
DC-link voltage	V_{dc}	200V
Grid voltage	V_g	50V

the voltage controller has a negatively effect on the stability, which has been discussed in the existing researches[5]. Therefore, the voltage controller proportional part K_{pr} is set to 0 to better consider other parameters' effect on the stability in this paper.

Fig.3 shows the bode plot of T(s) with different switching frequencies. In Fig.3, f_c represents the frequency when the phase lag caused by the control delay reaches 90°. According to (2), f_c can be calculated as (6)

$$1.5T_s \cdot \omega_c = \frac{\pi}{2} \Rightarrow \omega_c = \frac{\omega_s}{6} = 2\pi f_c \tag{6}$$

It can be seen from Fig.3 that with the decrease of switching frequency, the phase lag at the LCL resonant frequency ω_r increase. When $\omega_r<\omega_s/6$, the phase lead provided by the controller part minus the phase lag caused by delay is larger than 90° at ω_r so that the LCL resonant peak can avoid -180° phase crossing. The phase of T(s) reaches -180° at ω_r when $\omega_r = \omega_s/6$ and the system is critical stable in this case. That's why $\omega_s/6$ is regarded as a critical frequency for stability in many researches. However, when $\omega_r > \omega_s/6$, the phase lead provided by G_{nu}(s) is less than 90°at ω_r, which lead to -180° phase crossing at the LCL resonant peak. Therefore, in the high power application where the switching frequency is relatively low and $\omega_r > \omega_s/6$ is likely to happen, the dual-loop voltage-current control is prone to be unstable.

B. Optimal Control of Inner Current Loop

To deal with the deficiency of dual-loop voltage-current control, some researches adopts lead-lag filter inserted along the inner current feedback path to compensate the digital delay. However, the digital lead-lag filter realized in the discrete time-domain may be distorted when filer corner frequency is relatively high especially in the case of low switching frequency. To cope with different switching frequencies, the optimal control for inner current loop is proposed and shown in Fig.4. Instead of lead-lag filter, a simple proportional gain K_{im} is inserted along the inner

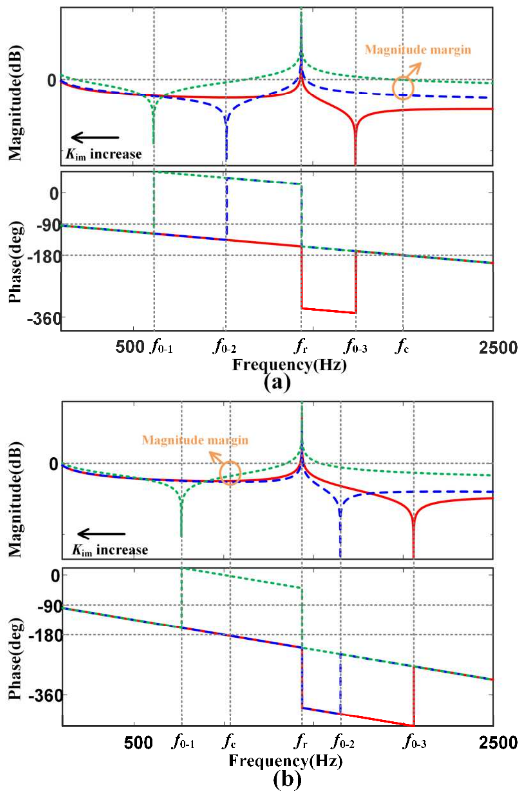

Fig. 5. Bode plot of T(s) with different K_{im}.
(a)$\omega_r < \omega_s/6$ (b) $\omega_r > \omega_s/6$

current feedback path. Referring to Fig.4, G_{de}(s) keeps the same as (5) while G_{nu}(s) can be fixed as (7)

$$\begin{aligned} G_{nu}(s) &= \left[K_{pi}K_{im}\left(s^2 L_g C + 1\right) + K_{pi}G_{PR}(s)\cdot sL_g\right]e^{-1.5T_s\cdot s} \\ &\approx K_{pi}K_{im}L_g C\left(s^2 + \frac{1}{L_g C} + \frac{K_{r1}}{K_{im}C}\right)e^{-1.5T_s\cdot s} \end{aligned} \tag{7}$$

It can be seen from (7) that G_{nu}(s) can also be divided into the controller part and delay part in which there are a pair of second-order zeros for controller part. The frequency of the second-order zeros are defined as ω_0 and can be expressed as (8)

$$\omega_0 = \sqrt{\frac{1}{L_g C} + \frac{K_{r1}}{K_{im}C}} = 2\pi f_0 \tag{8}$$

As mentioned before, with the second-order zeros, the the controller part doesn't cause phase shift when $\omega<\omega_0$ but provide 180° phase lead when $\omega>\omega_0$. Therefore, by tunning the K_{im}, the frequency of the second-order zero can be shifted and the phase lead provided by controller part at ω_r can be changed. Therefore, the core of the optimal control is how to tune K_{im} in different switching frequencies to keep the system stable.

Due to the critical frequency $\omega_s/6$, the cases are divided into $\omega_r < \omega_s/6$ and $\omega_r > \omega_s/6$ to present different switching frequencies. Fig.5(a) shows the bode plot of T(s) with different K_{im} in the case of $\omega_r < \omega_s/6$. It can be seen from Fig.5(a) that only when $\omega_0 < \omega_r$ the system can be possibly stable in this case. When $\omega_0 < \omega_r$, the 180° phase rising at frequency ω_0 help avoid -180° phase crossing at the resonant peak, the phase will cross -180° at the frequency ω_c. The system can keep stable when the amplitude at the frequency ω_c is smaller than 0dB. Therefore, the value range of K_{im} to keep system stable in the case of $\omega_r < \omega_s/6$ can be derived in (9)

$$K_{r1}L_m < K_{im} < \frac{36\omega_s\left(L_m + L_g\right) - \omega_s^3 L_m L_g C - 216K_{pi}K_{r1}L_g}{6K_{pi}\left(36 - \omega_s^2 L_g C\right)} \quad (9)$$

Define the two thresholds of K_{im} as (10)

$$\begin{cases} Threshold1 = K_{r1}L_m \\ Threshold2 = \dfrac{36\omega_s\left(L_m + L_g\right) - \omega_s^3 L_m L_g C - 216K_{pi}K_{r1}L_g}{6K_{pi}\left(36 - \omega_s^2 L_g C\right)} \end{cases} \quad (10)$$

Fig.5(b) shows the bode plot of $T(s)$ with different K_{im} in the case of $\omega_r > \omega_s/6$. It can be seen from Fig.6(b) that the system can be possible stable only when $\omega_0 > \omega_r$. In this case, the phase lag caused by delay is larger than 90°. Therefore, the phase lag can be utilized to avoid the -180° crossing at ω_r and this can be realized when $\omega_0 > \omega_r$. Similarly, the phase will cross -180° at the frequency ω_c. The system can keep stable when the amplitude at the frequency ω_c is smaller than 0dB. Therefore, the value range of K_{im} to keep system stable in the case of $\omega_r > \omega_s/6$ can be derived in (11)

$$\begin{cases} \left(K_{im} < Threshold1\right)\&\left(K_{im} < Threshold2\right), \left(\sqrt{\dfrac{1}{L_g C}} > \dfrac{\omega_s}{6}\right) \\ \left(Threshold2 < K_{im} < Threshold1\right)\&\left(K_{im} > 0\right), \left(\sqrt{\dfrac{1}{L_g C}} < \dfrac{\omega_s}{6}\right) \end{cases} \quad (11)$$

With the parameters shown in Table I, Fig.6 shows the stable region of system in different switching frequencies. It can be seen from Fig.6 that the stable region is relatively narrow when $\omega_r > \omega_s/6$ and the value range of K_{im} is shrink more when ω_r is closer to ω_r. However, when $\omega_r < \omega_s/6$, the stable region will get larger with the increase of switching frequency. Especially, when $\omega_r = \omega_c$, there is '*Threshold1* = *Threshold2*', which means the system is critical stable in this condition and the system can hardly keep stable in this case.

The effect of other parameters including the voltage controller parameter K_{r1} and the current controller parameter K_{pi} on the stable regions are also analyzed as shown in Fig.8 and Fig.9. It can be shown in Fig.8 that the increase of K_{pi} generally will reduce the stable regions no matter when $\omega_r < \omega_s/6$ and $\omega_r > \omega_s/6$. Fig.9 shows that the width of the stable region is almost unchanged and shift upwards as a whole with the increase of K_{r1} when $\omega_r < \omega_s/6$, but in the case of $\omega_r < \omega_s/6$, the stable region expands to some extent when K_{r1} increases due to *Threshold2* < 0 and '0' plays as the lower limit of the stable region..

Generally, with the stable region presented as the value range of K_{im}, the optimal control of inner current loop can be realized through tuning the current feedback proportion flexibly based on (9) and (11) to cope with different switching frequencies.

IV. Simulation and Experimental Results

To verify the stability analysis and the effectiveness of the optimal control, the parameters shown in Table I are adopted and the simulation and experiment are designed as follows

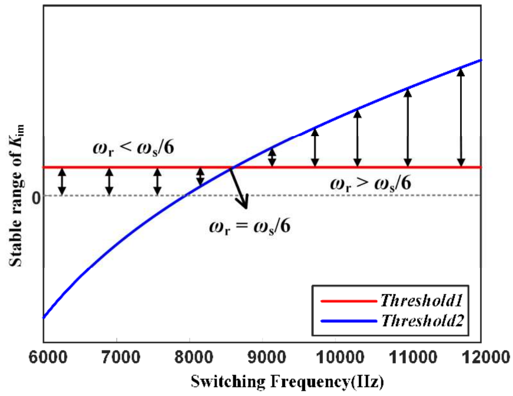

Fig. 6. Stable region with different switching frequencies

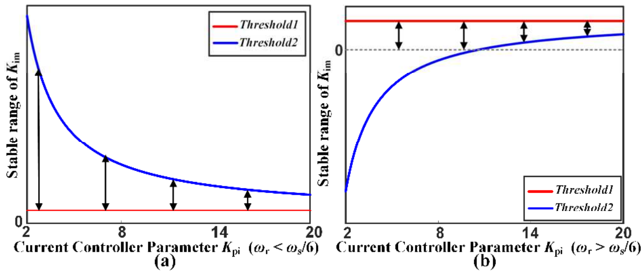

Fig. 7. Stable region with different K_{pi} (a) (a)$\omega_r < \omega_s/6$ (b) $\omega_r > \omega_s/6$

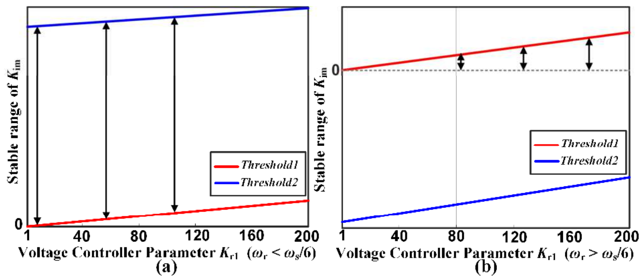

Fig. 8. Stable region with different K_{r1} (a)$\omega_r < \omega_s/6$ (b) $\omega_r > \omega_s/6$

A. Simulation Results

It can been seen from Table I that the LCL filter resonant frequency f_r is 1.435kHZ and f_c = 1.33kHZ when switching frequency is 8kHZ while f_c = 2kHZ when switching frequency is 12kHZ. According to (9) and (11), the value range of K_{im} to keep system stable should be [0.12, 3.22] when switching frequency is 12kHZ and [0, 0.12] when switching frequency is 8Khz. Therefore, the simulation are designed as follows.

1)Case1: f_s = 12kHZ, K_{im} is set to change from 1 to 0.11 at 2.0s and back to 1 at 2.04s

2)Case2: f_s = 12kHZ, K_{im} is set to change from 1 to 3.23 at 2.0s and back to 1 at 2.04s

3)Case3: f_s = 8kHZ, K_{im} is set to change from 0.1 to 0.13 at 2.0s and back to 1 at 2.04s

The simulation results are shown in Fig.9, in which Fig.9(a) and Fig.9(b) shows the grid current wave i_g and the oscillation frequency analysis of Case1 and Case3. It can be found that the system turns unstable when K_{im} changes at 2s and the oscillation frequencies of Case1 and Case3 are both around 1.435kHZ, which corresponds to the LCL resonant frequency f_r. The instability of Case1 can be explained by Fig.5(a) that the change of K_{im} from 1 to 0.11 results in $f_r < f_0$ but the phase lag caused by delay is

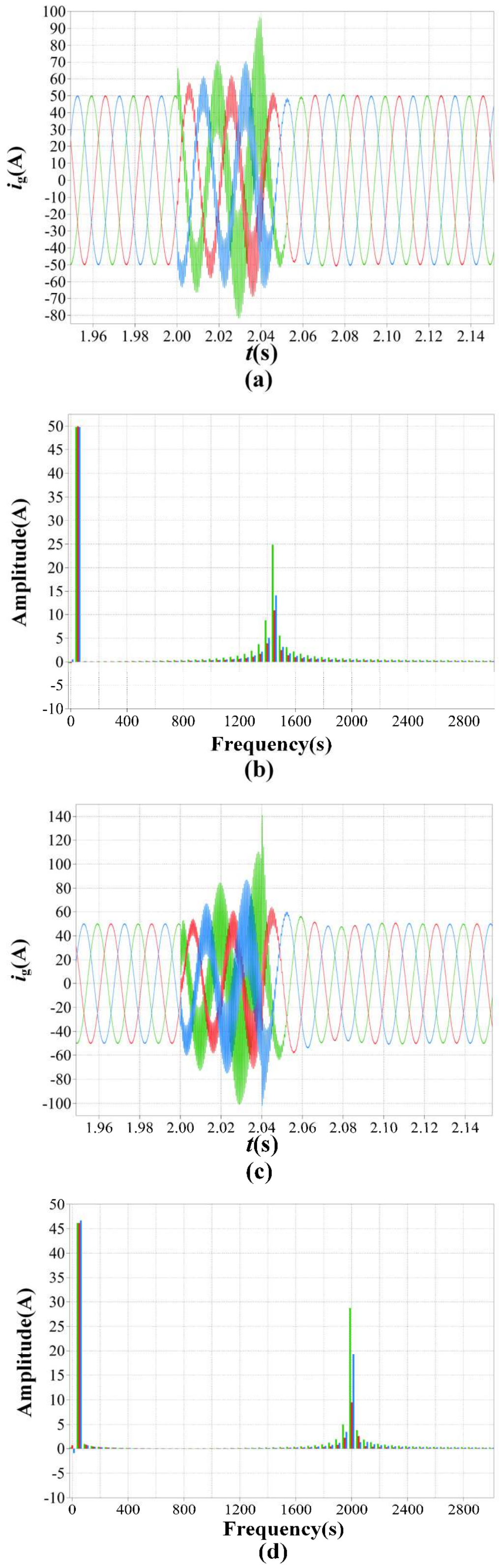

Fig. 9. Simulation results (a) Grid current wave of Case1 and Case3 (b) Oscillation frequency analysis of Case1 and Case3 (c) Grid current wave of Case2 (d) Oscillation frequency analysis of Case2

smaller than 90° thus lead to the -180° phase crossing at f_r. The instability of Case3 can be explained by Fig.5(b) that the change of K_{im} from 0.1 to 0.13 results in $f_r > f_0$ but the phase lag caused by delay is larger than 90° and

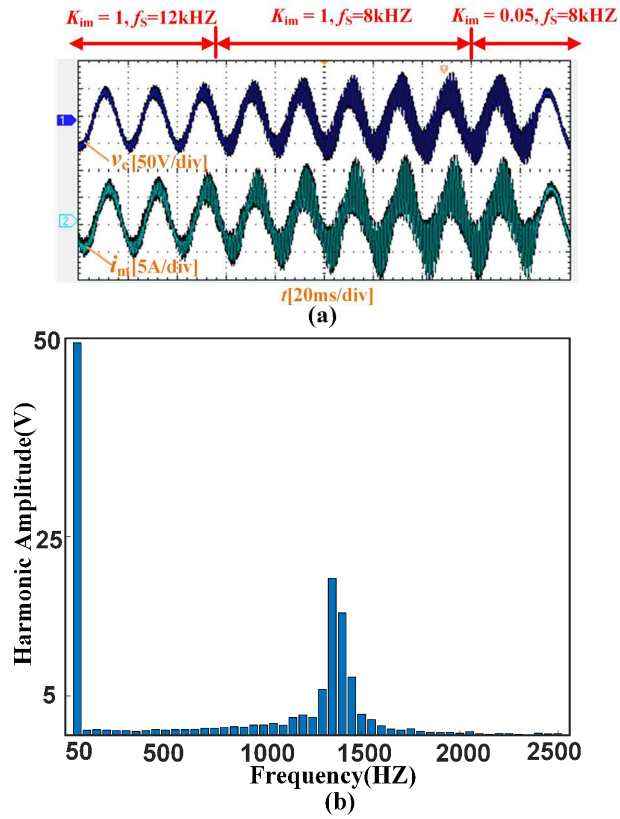

Fig. 10. Experiment results (a) Waveform of capacitor voltage and inverter-side inductor current (b) Oscillation frequency analysis of capacitor voltage

exceed the phase margin provided at f_0, also leading to -180° phase crossing at f_r.

Fig.9(c) and Fig.9(d) shows the grid current i_g wave and the oscillation frequency analysis of Case1. Similarly, the instability occurs at 2.0s but the oscillation frequencies are around 2kHZ, which is corresponding to f_c when f_s = 12kHZ. The instability can be explained by Fig.5(a) that the phase crosses -180° at f_c and the change of K_{im} from 1 to 3.23 will increase the magnitude to larger than 0dB at f_c, which causes the instability at f_c.

B. Experiment Results

To validate the effectiveness of the optimal control when coping with different switching frequencies, the experiments are designed as follows

1)The inner current feedback proportion K_{im} is set to 1 and the switching and sampling frequency f_s is set to change from 12kHZ to 8kHZ to verify the negative effect of low switching frequency on the stability of dual-loop voltage-current control.

2)Then the K_{im} is set to change from 1 to 0.05 to verify the effectiveness of tunning K_{im} to stabilize the system in the case of low switching frequency.

The experimental results are shown Fig10, in which Fig.10(a) presents the waveforms of capacitor voltage v_c and inverter-side inductor current i_m while Fig.10(b) is the oscillation frequency analysis of v_c. It can be seen from Fig.10(a) that when K_{im}=1, f_s=12kHZ, there are f_r<f_s/6 and f_0<f_r, thus the phase lead provided by f_0 can help stabilize the system. However, when K_{im}=1, f_s=8kHZ, there are

$f_r>f_s/6$ and $f_0<f_r$, the increase of digital delay will lead to instability. Fig10(b) shows that the main harmonic frequencies are near the LCL filter resonant frequency f_r , which indicated the -180° phase crossing at f_r. Then the K_{im} is changed from 1 to 0.05 and there is $f_0<f_r$, the phase lag caused by digital delay help avoid -180° crossing at f_r instead and the system turns stable.

V. CONCLUSIONS

This paper analyzes the stability of digitally dual-loop voltage-controlled inverters with consideration of grid impedance. It is revealed that both the digital delay and controller affect the system stability through adjusting the phase at the resonant frequency of the LCL filter. It is found that the dual-loop voltage-controlled inverter may have stability problem in the case of low switching frequency due to the increase of digital delay. Then an optimal control for inner current loop is proposed and can deal with different switching frequency through tunning the feedback proportion of current. The stable regions presented as the value range of current feedback proportion are derived in different switching frequencies. Simulation and experiment validate the stability analysis and effectiveness of the optimal control

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