Novel current balancing method for HF interleaved converters with reduced control effort

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Keywords

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Abstract

The Active Neutral Point Clamped (ANPC) topology as a three level inverter is particularly well suited for subdivision into fundamental switching semiconductors and modulating fast switching semiconductors. This allows each semiconductor to be selected for its best characteristics. One part of a hybrid ANPC inverter can be realized with high frequency interleaved stages based on wide bandgap power semiconductors. A challenge is the calculation effort of the duty cycle for this high switching frequency, especially due to the interleaved based stages. It is often considered that the reduction of the calculation effort has a negative impact on the current accounting. This paper proposes a simplified method for the balancing of the current in the interleaved stages with significantly reduced control frequency. An active current symmetry should be implemented, which would be easier due to the reduced control effort. In this paper, this method is experimentally validated without active current symmetry control.

Introduction

Multi-level inverter allows to use power semiconductor with less blocking voltage as the DC-Link voltage. This allows to use 650 V wide bandgap devices in a inverter with 800 V DC-Link. Wide bandgap devices allow a high frequency stage to reduce the size of the inverter. To increase the output power of the inverter, several HF stages can be connected in parallel. This also has the advantage that the interleaving concept can be used to reduce the output current ripple. The disadvantage of parallel stages is a higher control effort because of the necessity to implement a current balancing [1, 2, 3, 4]. In this paper an interleaved DC/AC converter with a reduced control afford is investigated. In the beginning, the hybrid ANPC topology is presented. Then the challenges of interleaved inverters are discussed and a method to significantly reduce the control effort of the inverter is presented. This method is validated with a measurement on the introduced inverter. The reduction in control effort should enable microcontrollers to be used in HF interleaved converters, avoiding the necessity for e.g. an FPGA.

1 Hybrid ANPC Topology

The ANPC Topology is especially well qualified for an interleaved DC/AC Converter and is shown in Fig. 1. It consists of a low frequency section (S1 - S4) which is switched with a fundamental frequency of $f_0 = 50\,\mathrm{Hz}$. For the positive halfwave the switches S_1 and S_3 are activated and for the negative halfwave the switches S_2 and S_4. The switches have almost only conduction losses because they switch with a low frequency and for restive load at zero current. With the switches S_5, S_6 and inductance L the output voltage will be modulated with a high switching frequency f_s. A additional buffer capacitor C_c is closely placed parallel to the high frequency switches to provied a low impedance path for HF current. Due to the separation into low frequency and high frequency section, the best semiconductor type for the respective parameters can be selected. The ANPC Topology is particularly benefitial for this case, because only four low frequency switches are needed. In the inverter, six HF bridges with GaN-HEMTs are used parallel with a switching frequency of $f_s = 200\,\mathrm{kHz}$ and four Si-IGBTs at the LF section [5].
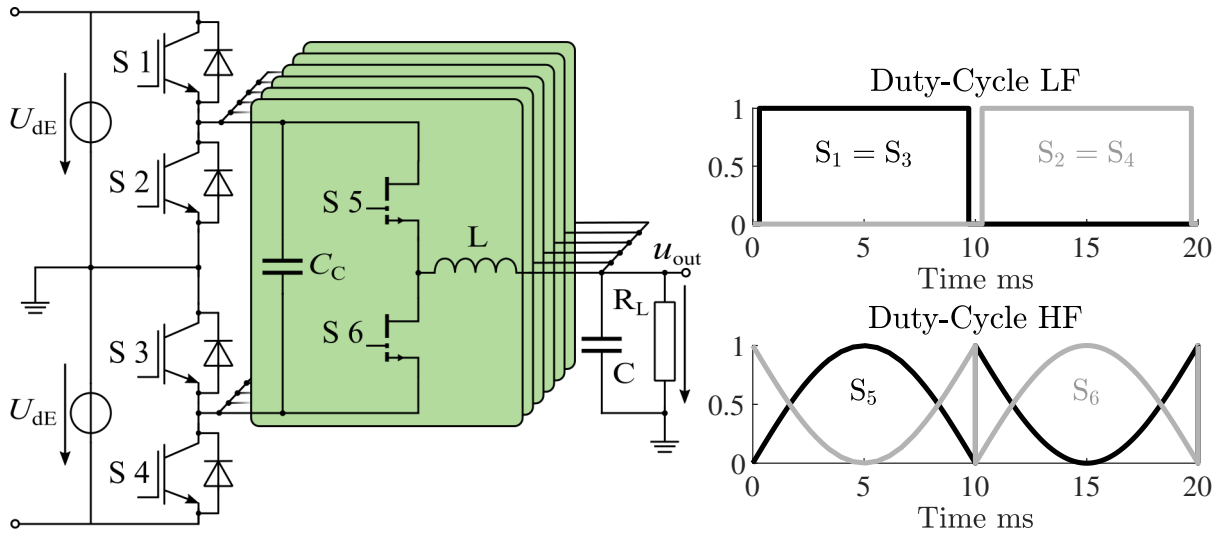

Fig. 1: The ANPC Topologie (left) and the associated control signals (right)

The increased output power and the lower filter effort are the advantages of the six parallel stages. The disadvantages are higher control effort and a possible current deviation between the stages. This arises due to small differences between the stages, for example a different switching speed, mismatched PWM-frequency or unequal inductance values. A current deviation leads to an unequal load distribution, so that an overload of the stage with the highest output power can result. To balance the stages, each current $i_{L,j}$ has to be measured to compensate the current error with an appropriate control strategy.

A current deviation between the stages has multiple reasons. The largest influence on the deviation is due to varying inductor parameters such as inductance and resistance value. Also unequal control signals like dead time, gate voltage, etc. have an influence, therefore a central duty cycle generation is [6].

Control requirements

To generate interleaved PWM signals that are as identical as possible, an FPGA or a microcontroller with independent PWM modules can be used. An FPGA has a higher calculation speed and can perform parallel tasks, which makes it suitable for this application. In this paper it is shown that even with limited calculation power it is possible to control this ANPC, using a microcontroller. Especially for grid application the normally high calculation effort has no advantage. To control the ANPC with the microcontroller, a high generation speed of the duty cycle is required, which corresponds to a compact C code. In the left part of Fig. 2 the generation of the duty cycle with optional current deviation is shown.

The duty cycle will be generated in a separate CLA task (Control Law Accelerator). Optionally a current deviation can be compensated. In this paper, the CLA frequency f_{cla} is the control frequency of the
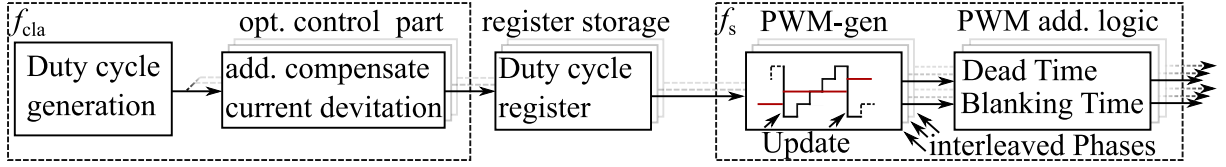
Fig. 2: Creating interleaved PWM signals with different control f_{cla} and switching frequency f_{s}

inverter. The duty cycle from each stage will be written in the duty cycle register. The generation of the PWM signals is shown in the right part of Fig 2. The duty cycles are refreshed in each switching period of the HF stage. In this example, the PWM signals are generated by a comparison between a triangular signal (up-counter) and the duty cycle which will be refreshed at the triangle counter zero. Therefore, the duty cycle signal is updated when the PWM signal is set high.

Each interleaved PWM module of the microcontroller updates from the Duty Cycle register once per switching period. With 6 stages this results in a control frequency of $f_{\mathrm{cla}} = 6 \cdot f_{\mathrm{s}} = 1.2\,\mathrm{MHz}$. This is shown in Fig 3 (middle), where colored values correspond to a refreshed duty cycle. But this high control frequency cannot be realized with normal microprocessors. A control with 6 predefined logic tables transmitting coordinated values from the DMA to the PWM modules will achieve this speed, but this makes current compensation or grid synchronization practically impossible and is therefore not attempted.

Reduction of control effort

This high control effort is not necessary for grid applications and will be reduced in this paper. To ensure a reduction in control frequency does not have a strong effect on current symmetry, although PWM module updated with old duty cycle values. With a reduction of the control frequency f_{cla} to the switching frequency f_{s}, always the same stage gets the updated duty cycle value. This method is shown in Fig. 3 (top) where stage one gets the updated value, visible by a colored number. The new duty cycle is always taken at the rising edge of the corresponding stage, and stages two to six (number marked in black) are given the last calculated delayed duty cycle from the stage with the color from the arrow.
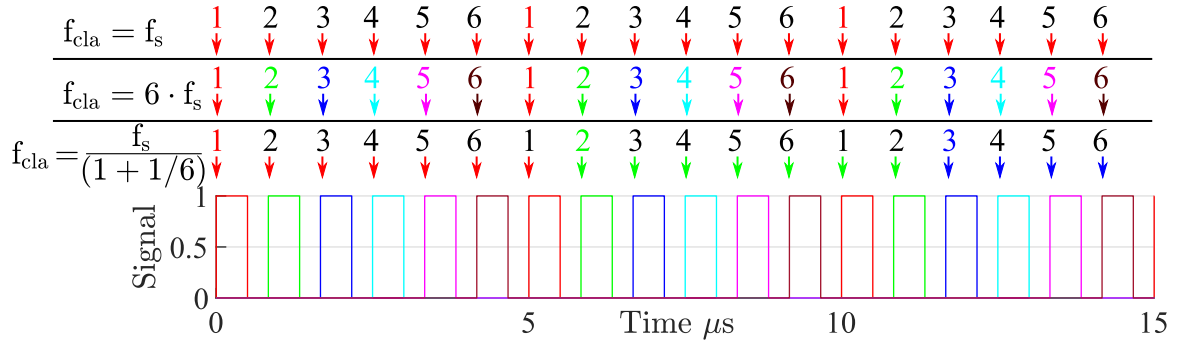

Fig. 3: Different control frequencys for a six stage interleaved converter. Each stage updates with the rising edge, colored stage numbers with a new duty cycle, black stage numbers with the last calculated

With $f_{\mathrm{cla}} = f_{\mathrm{s}}$ an asymmetrical refresh of all stages results, which leads to another reason for deviation from the target currents. By prioritizing the individual stages, it can be assumed that stage 1 has a larger current when the voltage slope is positive and a smaller current when the voltage slope is negative than the other stages. The last stage (in this case 6) has the opposite behavior to stage 1, since it experiences the increase/decrease of the duty cycle only with a delay. As a result, the output potential is already changed accordingly, whereby a smaller voltage time surface is present at the inductance 6. The simulated deviations for otherwise ideal components are shown in Fig. 4 (top). There all average inductor currents of the individual stages $\bar{i}_{\mathrm{L,s}}$ are shown and the deviation between Stage 1 and Stage 6 is up to $1.2\,\mathrm{A}$. The series of deviations corresponds to the delayed stage. The simulated output power of the converter is $16.6\,\mathrm{kW}$.
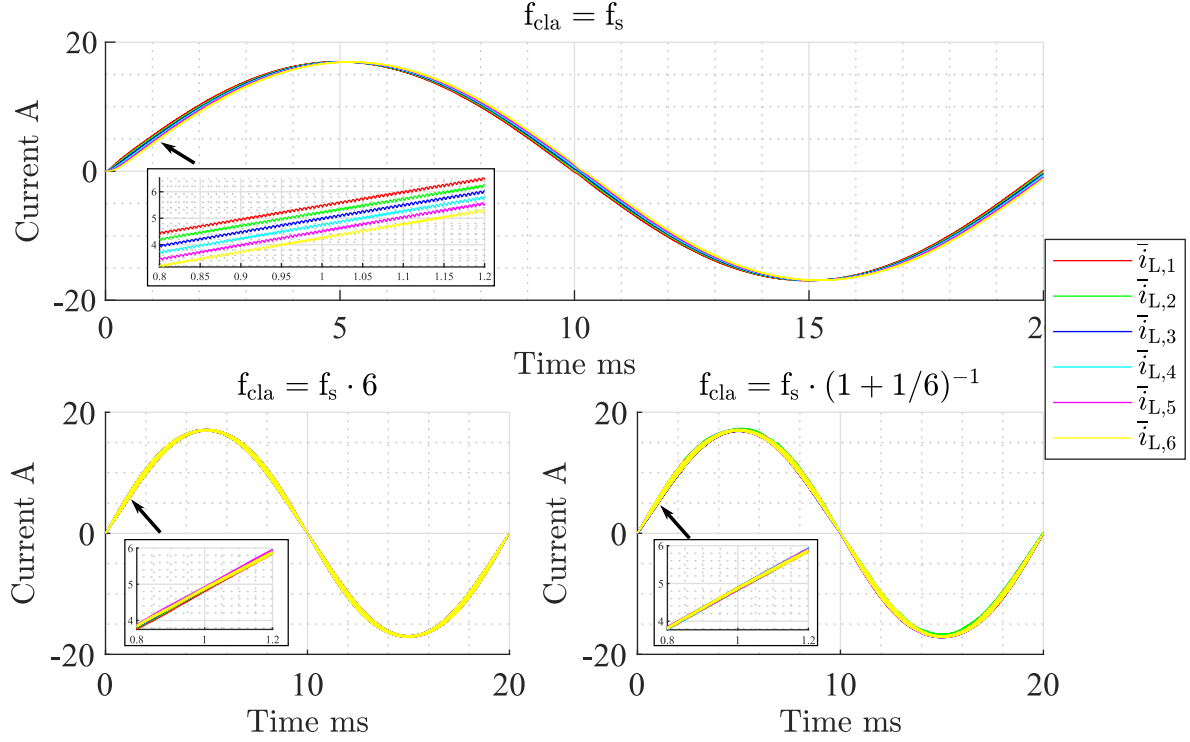
Fig. 4: Illustration of the simulated influence of the described control frequencies. The control frequency of $f_{cla} = f_s$ leads to a strong deviation of a symmetrical current load (top). The proposed method $f_{cla} = f_s \cdot (1 + 1/6)^{-1}$ (bottom right) leads to a symmetrical current load as well as a reduced control effort with a similar result as with a strongly increased control frequency $f_{cla} = 6 \cdot f_s$ (bottom left)

The asymmetry can be eliminated by increasing the control frequency according to the number of stages n. With 6 stages this results in a control frequency of $f_{cla} = 6 \cdot f_s = 1.2\,\text{MHz}$, so that each stage gets an updated duty cycle. This results in a symmetrical current in each stage, but also significantly increases the control effort. This method is shown in Fig 4 at the bottom, left side.

In this paper, it is proposed to set the control frequency of the inverter according to $f_{cla} = f_s \cdot (k \pm 1/n)^{-1}$. Here, n the number of stages and $k \in \mathbb{R}^+$ is a natural Number to reduce more the control frequency. With a control frequency of $f_{cla} = f_s \cdot (1 + 1/6)^{-1}$ the control effort is again lower than $f_{cla} = f_s$. Similar to method $f_{cla} = f_s$, one stage per switching frequency is updated with the refreshed duty cycle, but in the following period the next stage gets the refreshed duty cycle. So that each stage is handled equally and this is shown in Fig. 3 (bottom). With this approach, the simulation of the ANPC also leads to an quasi ideal superposition of the individual average currents of the inductor stages $\bar{i}_{L,s}$ shown in Fig. 4 at the bottom, right side.

Further possibilities of a more symmetrical control at a lower control frequency would be separately calculated duty cycle values for each stage. With the help of a linearization at the operating point, each stage could receive an approximate duty cycle. This method is not considered due to the additional calculation effort.

Measurement

In this section, different control frequencies f_{cla} are tested. All of the measurements were performed with the presented inverter in [5]. The measurements were carried out with the switching frequency of $f_s = 200\,\text{kHz}$ and an output voltage of $u_{out} = 230\,\text{V}$ at 50 Hz. The reasons for possible current deviations are minimised by a very symmetrical structure. A microcontroller generates all PWM signals leading to simular blanking and dead time for each stage. The gate loops are low inductive, low gate resistors and equal PCB design for each stage are realized.

Measurement of the Inductance

The deviations of each inductance of the HF stages are measured with a Bode 100. The inductances have a difference up to 4 µH. All the values of the inductors are shown in table I. In [2] the influence of a deviation in resistance of the inductance and semiconductors are analysed. A deviating in inductance resistance leads mainly to a deviation in the DC current. In the AC converter, the deviation are shown in the peaks of the sinusoidal output voltage. The influence of an inductance is reflected in the response time. A lower inductance leads to a faster change in current while the duty cycle changes. This deviation mainly happens near the zero crossing.

HF-Stage	inductivity	resistance	phase offset
1	28.788 µH	415 mΩ	$0\,°$
2	26.834 µH	304 mΩ	$60\,°$
3	29.621 µH	317 mΩ	$120\,°$
4	30.626 µH	319 mΩ	$180\,°$
5	28.596 µH	1623 mΩ	$240\,°$
6	29.703 µH	317 mΩ	$300\,°$

Table I: Measurement of the inductors of each HF stage by the switching frequency $f_s = 200\,\text{kHz}$. Phase offset is the PWM modul offset of each interleaved stage

Current Measurement results

In the following section a part of the measurement results is presented. To get a better comparison the error current of each stage with respect to the average current is used. The error current $\bar{e}_{c,k}$ is the deviation from each stage current to the targeted (average) stage current $\bar{e}_{c,k} = \bar{i}_{L,k} - \frac{\sum_{j=1}^{n} \bar{i}_{L,j}}{n}$. The output power of the inverter is $4.8\,\text{kW}$, so each stage should have a symmetric peak output current of 5 A by $u_{\text{out}} = 230\,\text{V}$.
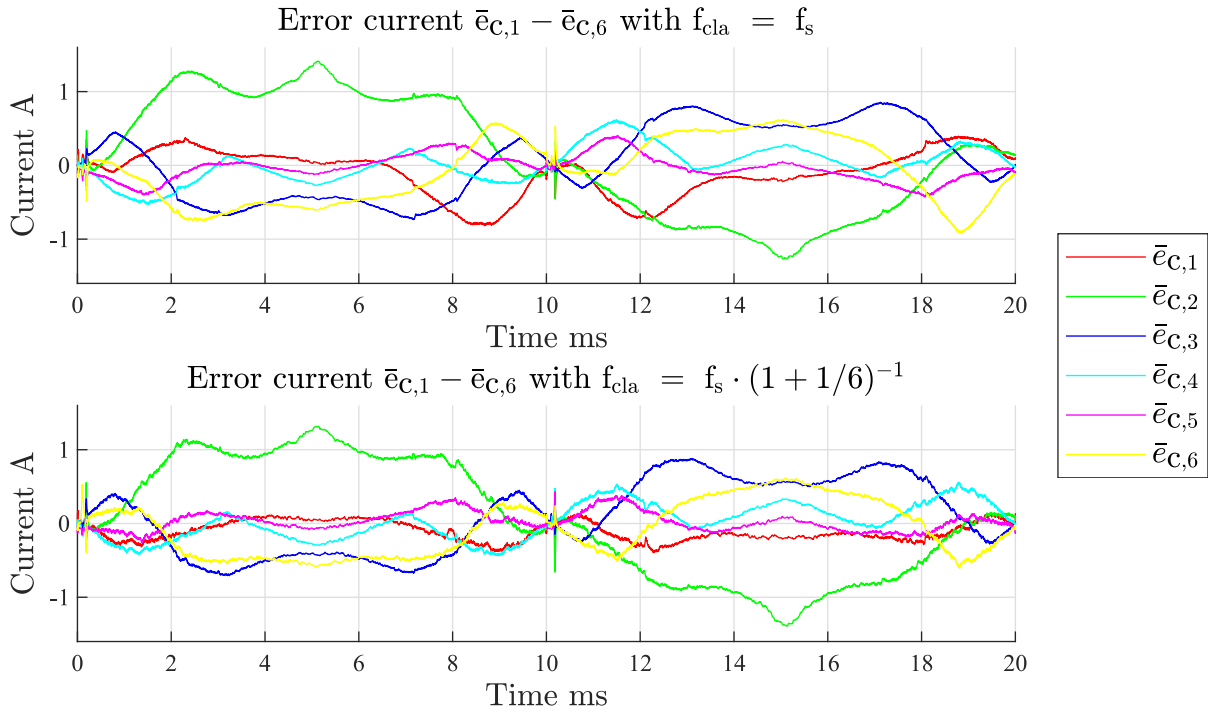

Fig. 5: Error current by a control frequency $f_{\text{cla}} = f_s$ (top) and $f_{\text{cla}} = f_s \cdot (1 + 1/6)^{-1}$ (bottom). The asymmetrical components have been strongly minimized by $f_{\text{cla}} = f_s \cdot (1 + 1/6)^{-1}$. No current feedback control is implemented

In Fig. 5 (top) the error current with $f_{cla} = f_s$ is shown and can be splitted into symmetric and asymmetric parts. In the Fig. 5 a strong asymmetry deviation at the current can be seen. Especially in the case of error current $\bar{e}_{c,1}$ and $\bar{e}_{c,6}$, a significant deviation can be seen in both half waves. With the proposed method $f_{cla} = f_s \cdot (1 + 1/6)^{-1}$ Fig. 5 (bottom), the asymmetric deviation could be greatly minimized. A slight widening of the average current of each stage can be seen. This can be explained by the partial delay of the duty cycle and by the resulting superposition of an oscillation with $f_{cla} = f_s \cdot (1 + 1/6)^{-1}$ frequency. This has no significant negative impact on the current symmetry itself. A comparison between Fig. 4 and Fig. 5 is difficult because other parasitic effects in the measurement dominate. In particular, the different values of the inductors (shown in Table I) make a direct comparison impossible. A more suitable comparison is performed in the following section.

Measurement comparison

In order to evaluate the symmetry of a sinusoidal wave, the mathematical symmetry condition equation 1 (left) be used with $\Delta\varphi = 5\,\text{ms}$ for the positive half wave and $\Delta\varphi = 15\,\text{ms}$ for the negative half wave.

$$f(t + \Delta\varphi) = f(-t + \Delta\varphi) \quad \Rightarrow \quad \Delta\bar{e}_{c,k}(t) = \bar{e}_{c,k}(t + \Delta\varphi) - \bar{e}_{c,k}(-t + \Delta\varphi) \tag{1}$$

The deviation between a symmetrical sinus and the measured stage current are calculated with 1 (right) and is shown in Fig. 6 on the left side for the positive half wave (pos HW) and for the negative in the right side (neg HW). A negative delta error at positive half wave describes a larger current contribution before the maximum of the sine. A positive delta error at negative half wave describes a larger current contribution before the minimum of the sine.

With $f_{cla} = f_s$ the current deviation is similar to the simulated deviation in Fig. 4. At the positive half wave the current of the first stage $\bar{e}_{c,1}$ has the largest asymmetric current percentage at the rising sine and the smallest at the falling sine. This can also be seen in Fig. 6 by the largest negative delta error $\Delta\bar{e}_{c,1}$. The order of the stages can also be seen, as the error current increases with the corresponding stage. Considering the negative current in the negative half wave, the measurement results also agree with the simulation results.
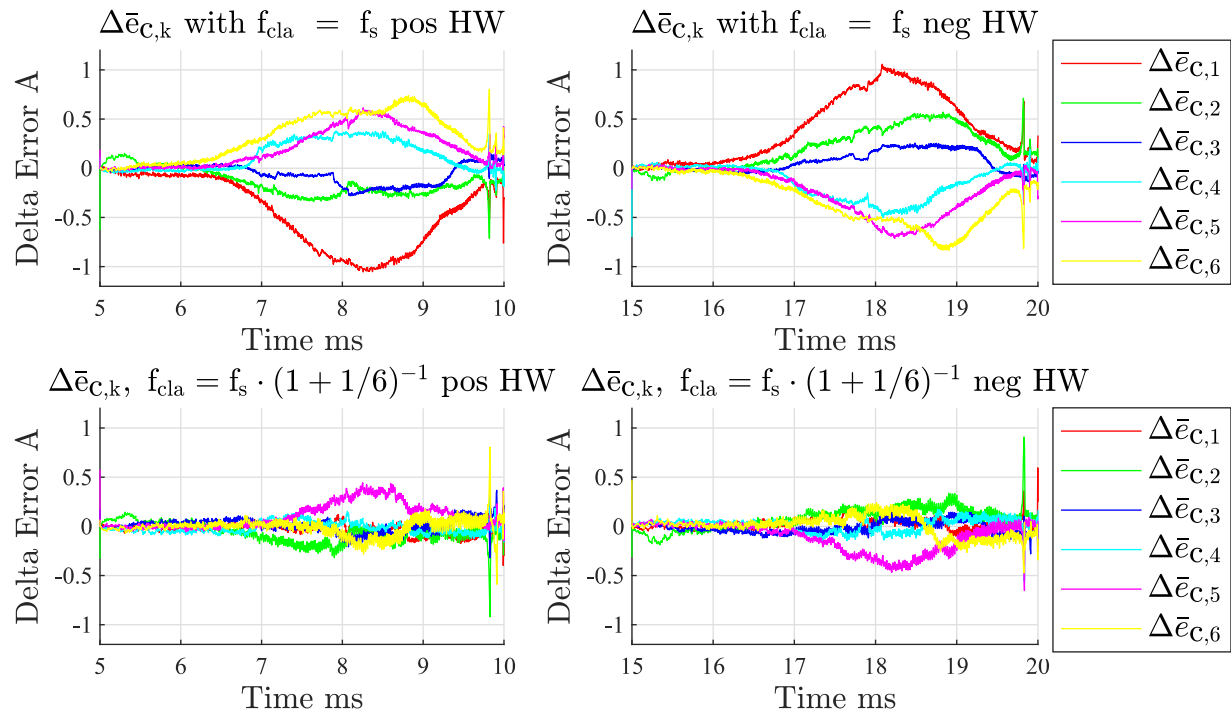

Fig. 6: Comparison of the asymmetric error current reduction with the control frequencies $f_{cla} = f_s$ and $f_{cla} = f_s \cdot (1 + 1/6)^{-1}$. The asymmetric current can be reduced with less control effort

The delta error with the lower control frequency $f_{cla} = f_s \cdot (1 + 1/6)^{-1}$ in both half waves can be significant reduced. Only the fifth stage has a current deviation of about 0.5 A, which is due to an higher resistance of inductor 5.

Conclusion

In this paper, a method has been presented to reduce the control effort without significantly affecting the current balance in interleaved converters. This was achieved by systematically adjusting the control frequency according to the presented equation. The improvements are shown in Fig. 6. This method was successfully tested with an interleaved converter with 6 stages and a switching frequency of $f_s = 200\,\text{kHz}$.

References

[1] Xunwei Zhou, Peng Xu and F. C. Lee, "A novel current-sharing control technique for low-voltage high-current voltage regulator module applications," in IEEE Transactions on Power Electronics, vol. 15, no. 6, pp. 1153-1162, Nov. 2000, doi: 10.1109/63.892830.

[2] J. A. Abu Qahouq, L. Huang and D. Huard, "Sensorless Current Sharing Analysis and Scheme For Multiphase Converters," in IEEE Transactions on Power Electronics, vol. 23, no. 5, pp. 2237-2247, Sept. 2008, doi: 10.1109/TPEL.2008.2001897.

[3] J. A. Abu-Qahouq, "Analysis and Design of N-Phase Current-Sharing Autotuning Controller," in IEEE Transactions on Power Electronics, vol. 25, no. 6, pp. 1641-1651, June 2010, doi: 10.1109/TPEL.2009.2037892.

[4] H. Kim, M. Falahi, T. M. Jahns and M. W. Degner, "Inductor Current Measurement and Regulation Using a Single DC Link Current Sensor for Interleaved DC–DC Converters," in IEEE Transactions on Power Electronics, vol. 26, no. 5, pp. 1503-1510, May 2011, doi: 10.1109/TPEL.2010.2084108.

[5] L. Fauth, C. Beckemeier and J. Friebe, "A Hybrid Active Neutral Point Clamped Converter consisting of Si IGBTs and GaN HEMTs for Auxiliary Systems of Electric Aircraft," 2021 IEEE Energy Conversion Congress and Exposition (ECCE), 2021, pp. 1917-1923, doi: 10.1109/ECCE47101.2021.9595512.

[6] J. A. Abu Qahouq, L. Huang and D. Huard, "Sensorless Current Sharing Analysis and Scheme For Multiphase Converters," in IEEE Transactions on Power Electronics, vol. 23, no. 5, pp. 2237-2247, Sept. 2008, doi: 10.1109/TPEL.2008.2001897.

[7] P. Antoszczuk, R. G. Retegui, M. Funes and D. Carrica, "Optimized Implementation of a Current Control Algorithm for Multiphase Interleaved Power Converters," in IEEE Transactions on Industrial Informatics, vol. 10, no. 4, pp. 2224-2232, Nov. 2014, doi: 10.1109/TII.2014.2362071.