Control of an Active Gate Driver for an Electric Vehicle Traction Inverter Using Artificial Neural Networks

Julius Wiesemann, Jacob Dumtzlaff, Axel Mertens
LEIBNIZ UNIVERSITY HANNOVER
Welfengarten 1
Hannover, Germany
Phone: +49 (0) 511 762-5224
Email: julius.wiesemann@ial.uni-hannover.de
URL: http://www.ial.uni-hannover.de

Keywords

≪Smart Gate Drivers≫, ≪Neural network≫, ≪EMC/EMI≫, ≪Silicon Carbide (SiC)≫, ≪Power converters for EV≫.

Abstract

Electric vehicle drivetrains using wide-bandgap semiconductors face challenges regarding EMI and accelerated machine aging due to the fast switching transients. This paper presents a method of controlling a variable-resistance active gate driver with the help of a neural network in order to reduce the drawbacks of fast switching while increasing efficiency. Measurements covering the whole MOSFET operating range and a sinusoidal inverter output current prove that the proposed method effectively reduces losses while also reducing switching speed and, in this way, reduces EMI issues and machine damage.

Introduction

The efficiency of drive systems in electric vehicles (EV) can be increased through the use of fast-switching power semiconductors like SiC MOSFETs. However, the steep gradients of the voltage pulses at the inverter outputs lead to increased electromagnetic interference (EMI) issues [1] in the vehicle and increased aging of the electrical machine, especially the winding insulation and machine bearings [2]. For this reason, extensive research has been performed with the objective of reducing these effects. The use of input and output filters is the most common method employed [3]. However, filters are bulky, heavy and increase the system losses. Active gate drivers (AGDs) offer another solution to the problem by influencing the switching behavior of MOSFETs or IGBTs through variation of the current that flows into the gate of the semiconductor [4, 5]. In this way, active gate drivers can reduce the switching speed of the MOSFET without substantially increasing the switching losses. In [6], a method to estimate the switching behavior of an IGBT driven by an AGD through a neural network is presented. Afterwards, an optimization of the switching behavior is performed using the neural network. However, this approach requires additional algorithms to find the optimum driver settings after the neural network has been fitted. Additionally, the method is limited to estimating only one operating point through the neural network. Another approach is presented in [7] where the switching behavior of a MOSFET is altered to minimize the switching losses while tolerating higher $\mathrm{d}v/\mathrm{d}t$ values. The output current range is divided into four stages, and in each stage a different driver setting is used. However, the variability of both the DC link voltage and the junction temperature are not accounted for and the division of the output current into just four ranges leaves room for improvement.

In this paper, a method to determine the optimal settings for an active gate driver using an artificial neural network (NN) in an electric vehicle drivetrain is presented. The network is trained to automatically

determine the optimum driver settings across a wide range of operating conditions. In the first section, the operating conditions in an EV are analyzed. Afterwards, the structure and basic control of the AGD used are explained and the neural-network-based control is introduced. In the following section, a measurement setup to derive training data for a neural network is presented. After introducing the training of the neural network, the validation of the control method in the operating range of the MOSFET and for sinusoidal inverter load currents is provided. Lastly, a conclusion is drawn and an outlook of future work is given.

Influence of Changing Operating Conditions in Electric Vehicles on the Switching Behavior of a SiC MOSFET

Drive inverters in electric vehicles face varying operating conditions. The load current vary across a wide range depending on the vehicle speed and acceleration, while the battery voltage, and thus the DC link voltage, varies with the load current and the battery's state of charge [8]. The junction temperature of a SiC MOSFET also mainly depends on the load current [9] and cooling conditions.
When designing an EV drivetrain, the switching behavior must be taken into account. The slope of the drain-source voltage v_{ds} at turn-on ($\mathrm{d}v/\mathrm{d}t_{\mathrm{on}}$) and turn-off ($\mathrm{d}v/\mathrm{d}t_{\mathrm{off}}$) and the switching energies E_{on} and E_{off} mainly influence the electromagnetic compatibility (EMC) and the efficiency of the inverter as well as the negative impacts on the electrical machine. For the design of the cooling system, the assessment of EMC, and the design of EMI filters, the worst-case values of switching energies and switching times have to be considered, which, however, leads to oversizing for other working conditions.

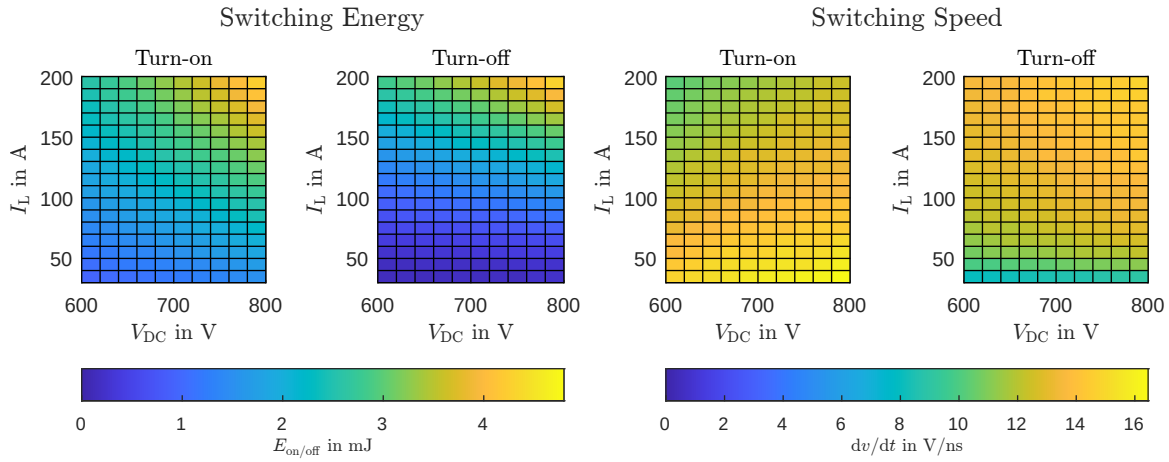

Fig. 1: Experimental results showing the variation of the switching behavior of an Infineon FF6MR12KM1 SiC MOSFET measured at $T_{\mathrm{j}} = 90\,^{\circ}\mathrm{C}$ with $R_{\mathrm{g,on}} = 2\,\Omega$ and $R_{\mathrm{g,off}} = 4\,\Omega$ at different operating points of DC link voltage and load current.

Fig. 1 shows how variations in operating conditions affect the switching performance of a SiC MOSFET. A changing load current especially leads to a significant variation in switching times and switching energies. An active gate driver can modulate the switching behavior of a SiC MOSFET and thus lead to a higher utilization of the maximum permissible $\mathrm{d}v/\mathrm{d}t$, keeping the losses low.

Active Gate Driver

The AGD used in this paper influences the switching behavior of the SiC MOSFET by using a variable gate resistance. It consists of four parallel gate resistors for turn-on and four parallel gate resistors for turn-off. Each gate resistor can be activated and deactivated with a timing accuracy of 2 ns through small-signal MOSFETs, driven by two four-channel auxiliary gate drivers and signal isolators. A detailed description of the gate driver can be found in [5]. A picture of the AGD can be seen in Fig. 4. To drive the MOSFET, the active gate driver uses the gate resistance vector $\mathbf{R_g} = [R_{\mathrm{g},1}; R_{\mathrm{g},2}]^T$. Following the initial activation of $R_{\mathrm{g},1}$, the gate resistor $R_{\mathrm{g},2}$ is activated after the variable time period t_{sw} has passed. By using

separate vectors for turn-on and turn-off, a small gate resistor is initially active during turn-on to reduce the rise time of the drain current i_D. Next, a large gate resistor is activated to increase the voltage fall time. The control during the turn-off works similarly, but in the opposite order: first, a large gate resistor is activated to slow down the voltage rise and this is then followed by a small gate resistor to reduce the current fall time.

Neural-Network-Based Control

The neural network is supposed to always choose the optimal t_{sw} settings for the AGD, based on load current, DC link voltage and MOSFET junction temperature. In order to fit the optimal driving data, a neural network with the structure shown in Fig. 2 is used.

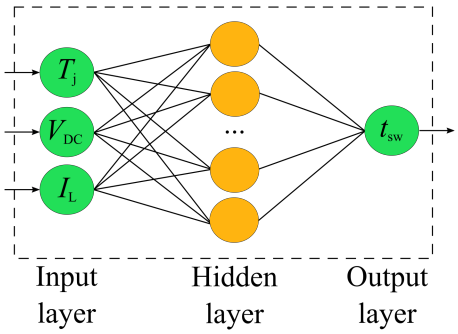

Fig. 2: Graphical representation of the neural network used to determine the optimal driver settings.

Two networks are trained, one for the turn-on and another for the turn-off process. The networks consist of three input neurons, a hidden layer of ten neurons, and a single output neuron to generate the variable switching time t_{sw}. The use of ten neurons in the hidden layer has proven to be a good compromise between fitting accuracy and complexity. The sigmoid function is used as the activation function. The network is created off-line for one specific MOSFET, which, due to the effort of training the network, makes it especially attractive for inverters that are produced in large numbers like automotive inverters. An adaption of the network during the operation of the inverter is not foreseen because it would require additional sensors and more computational power in the inverter, which reduces robustness and cost efficiency.

The training process for the neural network is shown in Fig. 3.

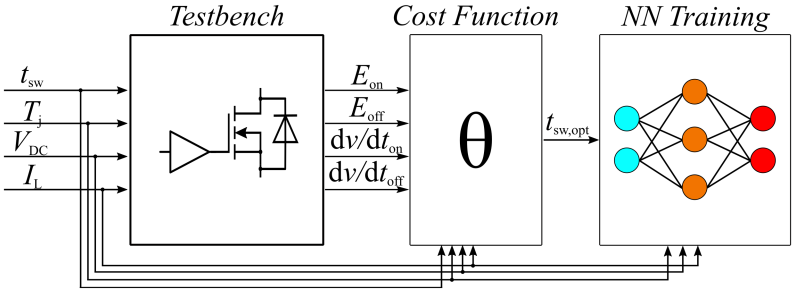

Fig. 3: Flow diagram for the neural network training process.

Test data is recorded across a wide range of operating conditions and t_{sw} settings and the cost function (1), similar to the one introduced in [5], is employed to find the optimal driving vector for each operating point. It is parameterized to determine the gate driver settings at which the $dv/dt_{on/off}$ is limited to a

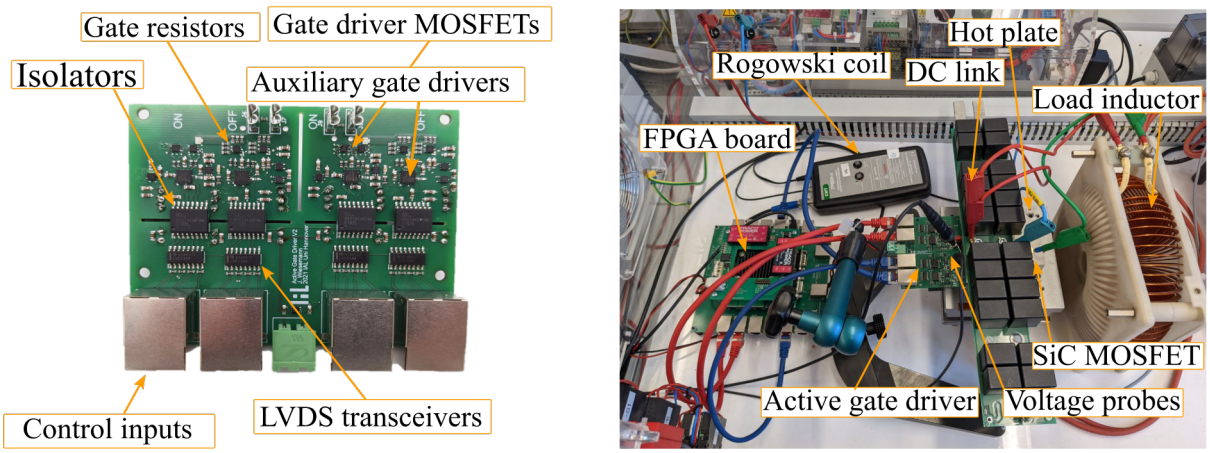

Fig. 4: Active gate driver and test bench with which the training and validation measurements were done.

setpoint $\mathrm{d}v/\mathrm{d}t_{\mathrm{set}}$:

$$\theta = \begin{cases} \left(1 + \frac{\sqrt{\left(\frac{\mathrm{d}v}{\mathrm{d}t_{\mathrm{set}}} - \frac{\mathrm{d}v}{\mathrm{d}t_{\mathrm{on}}}\right)^2}}{\frac{\mathrm{d}v}{\mathrm{d}t_{\mathrm{set}}}}\right)^3 & \text{for turn-on} \\ \left(1 + \frac{\sqrt{\left(\frac{\mathrm{d}v}{\mathrm{d}t_{\mathrm{set}}} - \frac{\mathrm{d}v}{\mathrm{d}t_{\mathrm{off}}}\right)^2}}{\frac{\mathrm{d}v}{\mathrm{d}t_{\mathrm{set}}}}\right)^3 & \text{for turn-off} \end{cases} \tag{1}$$

This way, the MOSFET will switch at the $\mathrm{d}v/\mathrm{d}t$ setpoint throughout the whole operating range. The value for $\mathrm{d}v/\mathrm{d}t_{\mathrm{set}}$ can be set according to the limits imposed by EMC and the electrical machine. After the optimal settings have been derived from the measured data using the cost function, the neural network is trained.

Derivation of Neural Network Training Data

The training data for the neural network was acquired in double-pulse tests using the variable-resistance active gate driver, an Infineon FF6MR12KM1 1200 V SiC MOSFET, and the test bench shown in Fig. 4. Different DC link voltages, load currents, baseplate temperatures and driving vectors for the active gate driver were tested. Table I shows the measurement conditions.

Table I: Measurement Conditions

Item	Symbol	Range
Load current	I_{L}	[20 A, 30 A, ... 200 A]
DC link voltage	V_{DC}	[600 V, 640 V, ... 800 V]
Junction temperature	T_{j}	[25 °C, 60 °C, ... 130 °C]
Turn-on gate resistor vector	$\mathbf{R_{g,on}}$	$[0.44\,\Omega; 4\,\Omega]^T$
Turn-off gate resistor vector	$\mathbf{R_{g,off}}$	$[8\,\Omega; 0.73\,\Omega]^T$
Switching time for turn-on	$t_{\mathrm{sw,on}}$	[2 ns, 4 ns, ... 102 ns]
Switching time for turn-off	$t_{\mathrm{sw,off}}$	[94 ns, 96 ns, ... 192 ns]

The drain current i_{D} was measured with a 30 MHz CWT UltraMini Rogowski coil. A Testec TT-HV 150 voltage probe with a bandwidth of 300 MHz was used to measure the drain-source voltage v_{DS}. All data were recorded using a 1 GHz LeCroy MDA810A oscilloscope. An example of the recorded waveforms for turn-on and turn-off can be seen in Fig. 5. Only selected variations of t_{sw} are shown for better clarity. The waveforms at the optimal value of t_{sw} are marked in red.

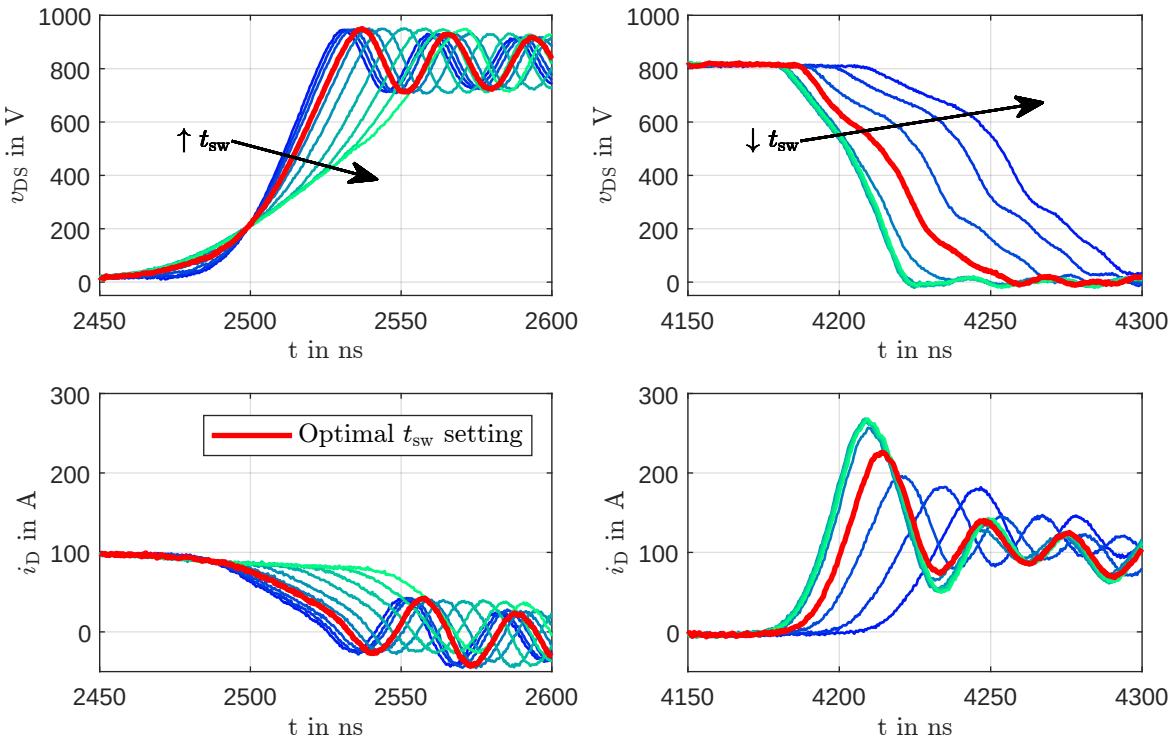

Fig. 5: Measured waveforms of v_{DS} and i_D at $V_{DC} = 800\,V$, $I_L = 100\,A$, $T_j = 60\,°C$ and at different values of t_{sw}. The optimal t_{sw} setting is marked in red. For a better overview, only every fifth variation of t_{sw} is shown.

Neural Network Training

After all the data points have been measured and evaluated by the cost function, only one value of both $t_{sw,on}$ and $t_{sw,off}$ is selected for each combination of V_{DC}, I_L, T_j, reducing the number of samples from its original 23256 to 456. These data are fed into a Matlab-based neural network training program that uses the Bayesian regularization algorithm to fit the neural network to the training data. 80 % of the data are used for training, while 10 % are used for validation and 10 % for testing.

Fig. 6 shows the input value of the neural network training process for turn-on and turn-off at two different temperatures. A gradual change in the optimal switching time between the different voltage, current and temperature values can be seen. For the turn-on, the optimal switching time rises with the current and decreases with the DC link voltage. The reason for this can be found in the switching behavior of

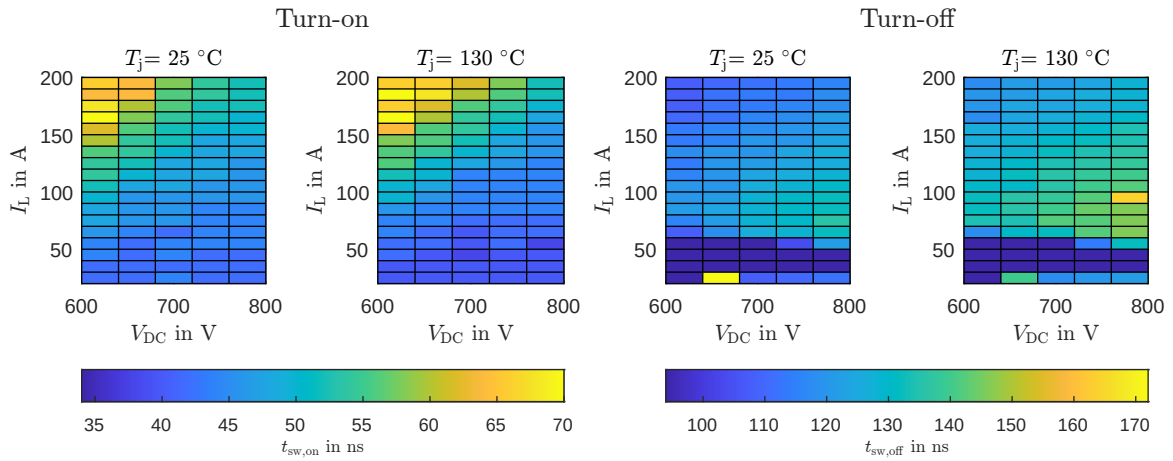

Fig. 6: Neural Network Training Data at $T_j = 25\,°C$ and $T_j = 130\,°C$.

the SiC MOSFET: first, the drain current rises before the voltage across the MOSFET drops. At high currents, the current rise phase takes longer, which requires $R_{g,1}$ to be active longer in order to speed up the current rise phase. The desired $\mathrm{d}v/\mathrm{d}t$ is set in the following voltage fall phase. Considering that the voltage slope at higher voltages is less steep (see Fig. 1), a lower setting for t_{sw} is sufficient to reach the desired $\mathrm{d}v/\mathrm{d}t$ at high DC link voltages. The optimal value of t_{sw} for the turn-off process, however, increases with the DC link voltage and shows a maximum at currents in the middle of the current range. At very low currents, the switching speed of the MOSFET cannot be influenced much by the AGD since it is limited by the charging rate of the semiconductor output capacitance [10]. As the voltage fall and current rise phase overlap more at turn-off than at turn-on (see Fig. 5), the optimal switching time is also influenced by the drain current charging the output capacitance.

Neural Network Validation

To test the neural-network-based control, double-pulse measurements were performed. Comparative measurements were also done with a conventional gate driver with different gate resistor values. Since the gate loop design has an influence on the switching behavior [11], using a different gate driver would lead to results which could not be compared. For this reason, the AGD was used with only one gate resistor activated during a double-pulse test to replicate the behavior of a CGD.
The neural network was exported as Matlab code from the training software and implemented on the Xilinx Zynq-700 SoC that controls the AGD using the Matlab Embedded Coder. The driver for the AGD is implemented in the FPGA part, while the neural network runs on the CPU. The main interrupt of the CPU is triggered at a frequency of 10 kHz. An analysis of the code runtime on the CPU shows that the calculation of one neural network takes 2.5 µs which means that the calculation of the six neural networks needed for a three-phase inverter requires 15 % of the total interrupt time. A deeper investigation shows that the majority (2.2 µs) of the time required to calculate the neural network output goes into the evaluation of the sigmoid activation function. If timing becomes critical, a replacement of the activation function through a lookup table could increase the calculation speed.

Constant Current Validation

Double-pulse tests at various voltages and currents spread throughout the whole operating range are conducted. The resulting $\mathrm{d}v/\mathrm{d}t$ can be seen in Fig. 7.

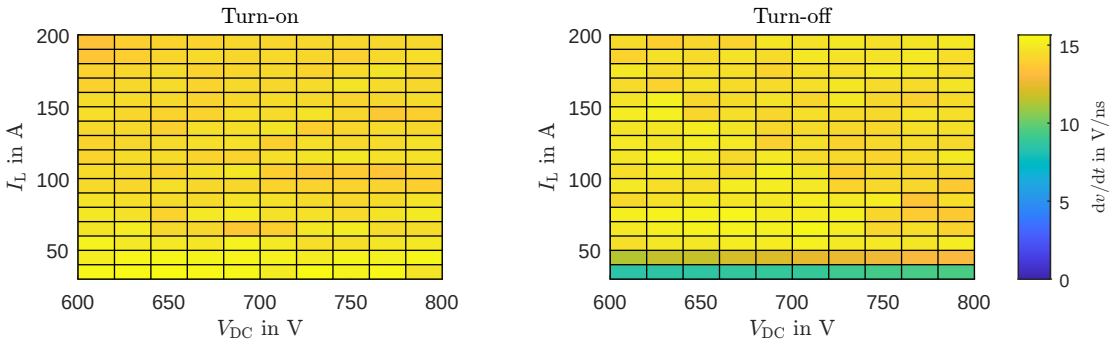

Fig. 7: Double-pulse test result with the AGD controlled by the neural network at different voltages and currents at $T_j = 90\,^{\circ}\mathrm{C}$ and a $\mathrm{d}v/\mathrm{d}t$ setting of 15 V/ns.

In comparison to Fig. 1, the turn-on process shows an almost constant $\mathrm{d}v/\mathrm{d}t$ throughout the whole operating range. At low currents during turn-off, the $\mathrm{d}v/\mathrm{d}t$ is reduced due to the slow charging of the output capacitance by the low drain current.
To evaluate the performance of the neural-network-driven AGD, it is compared to a CGD with $R_{G,on} = 2\,\Omega$ and $R_{G,off} = 4\,\Omega$. The differences in switching energies $\Delta E = E_{AGD} - E_{CGD}$ and switching speed $\Delta\mathrm{d}v/\mathrm{d}t = \mathrm{d}v/\mathrm{d}t_{AGD} - \mathrm{d}v/\mathrm{d}t_{CGD}$ are shown in Fig. 8.

The figure shows that especially the turn-on energies at high currents are reduced by the AGD. This is mostly achieved by increasing the $\mathrm{d}v/\mathrm{d}t$ at these currents, since the MOSFET's turn-on process at high

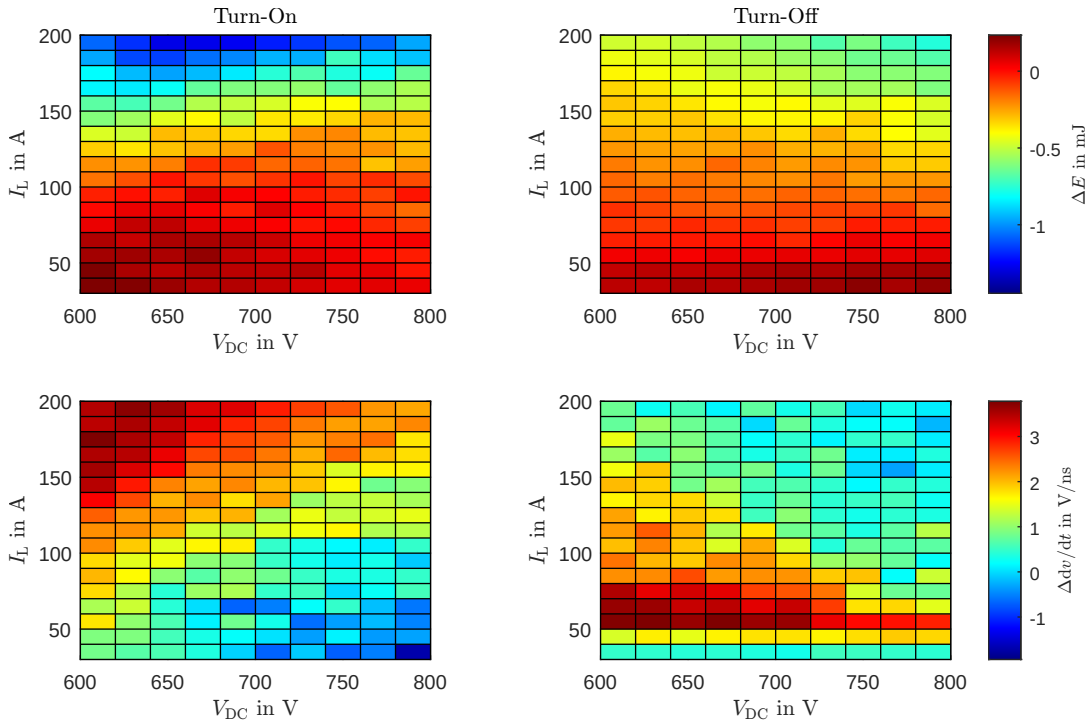

Fig. 8: Difference between the AGD controlled by the neural network and the CGD at different voltages and currents with $T_j = 90\,°C$, a dv/dt setting of $15\,V/ns$, $R_{G,on} = 2\,\Omega$ and $R_{G,off} = 4\,\Omega$.

currents is slower than the desired switching speed. At high DC link voltages and low currents, the CGD turns the MOSFET on faster than the desired rate of $15\,V/ns$. In this area, the AGD reduces the switching speed so as to avoid exceeding the maximum dv/dt.
The turn-off process behaves differently from the turn-on process, where the highest dv/dt occurs at high currents. However, the switching speed does not exceed the maximum dv/dt, which is why the AGD control does not influence the dv/dt. Even though the dv/dt is left almost unchanged, the switching energies are reduced through the use of the AGD. Although the switching speed is increased at low currents, since the switching energies at low currents are small, the increased switching speed does not influence the switching energy much.

Sinusoidal Current Validation

To evaluate the performance of the neural-network-based control in an EV drive inverter, double-pulse measurements were done to reproduce the behavior of the inverter. A virtual sinusoidal current defined by its RMS value I_{RMS}, a switching frequency f_s and an output current base frequency f_b was used to determine the currents at which the MOSFET in an inverter would switch during half of an output current period. Double-pulse experiments with the AGD and CGD were carried out at the pre-calculated currents. The gate resistor values of the CGD of $R_{G,on} = 2\,\Omega$ and $R_{G,off} = 4\,\Omega$ were chosen to limit the maximum dv/dt to around $15\,V/ns$ in the whole operating range.

The result of the validation measurements at a virtual load current of $I_{RMS} = 142\,A$ are shown in Fig. 9.

The switching times of the AGD show less dependence on the load current compared to the CGD. The switching energies are reduced, with a larger effect on the turn-on energy visible. The switching losses in a half bridge are calculated by adding up the switching losses at the predefined currents for the duration of one fundamental frequency period:

$$P_{sw} = f_g \cdot \sum_{0}^{f_g^{-1}} [E_{on} + E_{off}] \tag{2}$$

Since the reverse recovery losses in the complementary body diode are negligibly small compared to

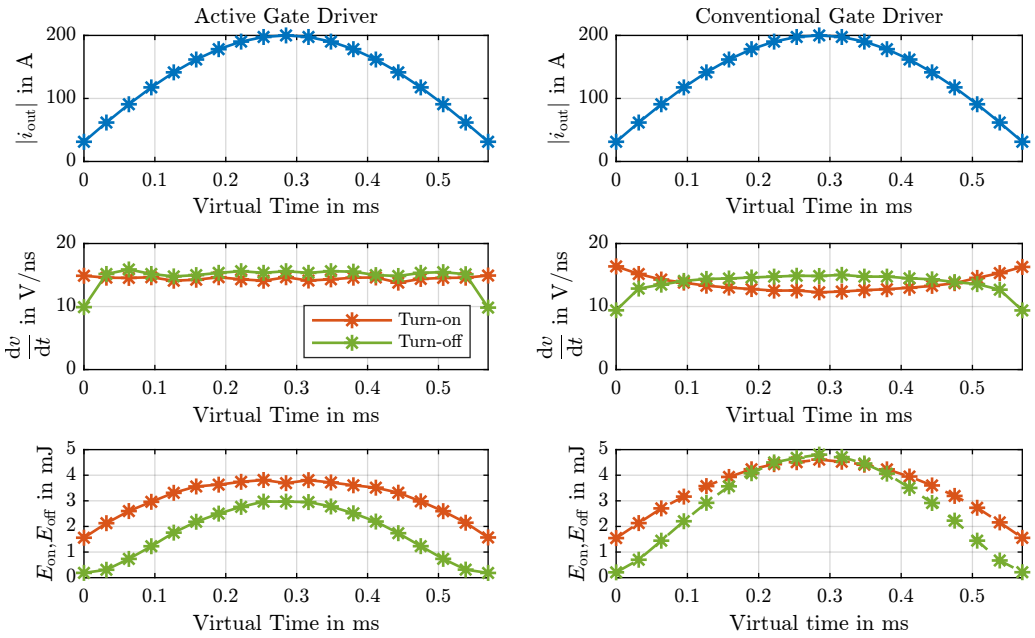

Fig. 9: Performance of the AGD in a virtual inverter with a sinusoidal output current with $T_j = 80\,°C$, $f_s = 24\,kHz$, $f_b = 600\,Hz$, and a DC link voltage of 800 V.

the switching losses, and hard to measure accurately, they are neglected [10]. The MOSFET and diode conduction losses are not influenced by the AGD and can thus be excluded from the comparison. The switching losses of the MOSFET driven by the AGD are 114 W, while the MOSFET driven by a CGD generates average switching losses of 142 W. The average dv/dt is 14.3 V/ns for the AGD and 13.7 V/ns for the CGD. The maximum dv/dt mainly responsible for EMI issues [1] is 15.2 V/ns for the AGD and 16.4 V/ns for the CGD.

Further measurements at DC link voltages of 600 V and 800 V and a sinusoidal load current of 142 A are carried out. The CGD measurements are carried out with different gate resistor combinations. Two AGD settings for dv/dt setpoints of 10 V/ns and 15 V/ns are used. The results can be seen in Fig. 10. The data show that at $V_{DC} = 800\,V$, the CGD version with $R_{on} = 1.3\,\Omega$ and $R_{on} = 2.6\,\Omega$ has losses similar to the AGD version with $dv/dt_{set} = 15\,V/ns$. However, the average and peak values of dv/dt are considerably higher for the CGD version. At $V_{DC} = 600\,V$, the differences in P_{loss} and $\overline{dv/dt}$ are reduced and only the dv/dt_{max} still shows a considerable difference, which means that there is still an influence on the EMC behavior of the inverter. If AGD and CGD at similar $\overline{dv/dt}$ are compared, the CGD with $R_{on} = 2\,\Omega$ and $R_{on} = 4\,\Omega$ shows a similar $\overline{dv/dt}$ compared to the 15 V/ns AGD. In this case, the CGD losses are higher than the AGD losses at $V_{DC} = 800\,V$. At $V_{DC} = 600\,V$, the $\overline{dv/dt}$ of the CGD decreases below the desired value of 15 V/ns. For this reason, the losses of the CGD are higher than the AGD losses since the CGD does not utilize the maximum permissible dv/dt.

Conclusion

In this paper, a method of controlling an AGD through an artificial neural network for use in an EV drive inverter is presented. The influence of changes in the working conditions of electric vehicle inverters, such as changing load currents, battery voltages or MOSFET junction temperatures, on the switching behavior of a SiC MOSFET is shown. After an introduction into the AGD used in this paper, a method of compensating for these changes using a neural network is introduced, and after deriving the optimal driver settings for all working conditions from data gathered in a double-pulse experiment, neural networks to control the AGD are trained. The network performance is tested in a double-pulse experiment throughout the whole operating range of the MOSFET and at current values matching the behavior of an EV inverter. Compared to a CGD, the switching losses are reduced, while almost constant switching times are achieved, meaning that throughout the operating area of the inverter, the SiC MOSFETs are

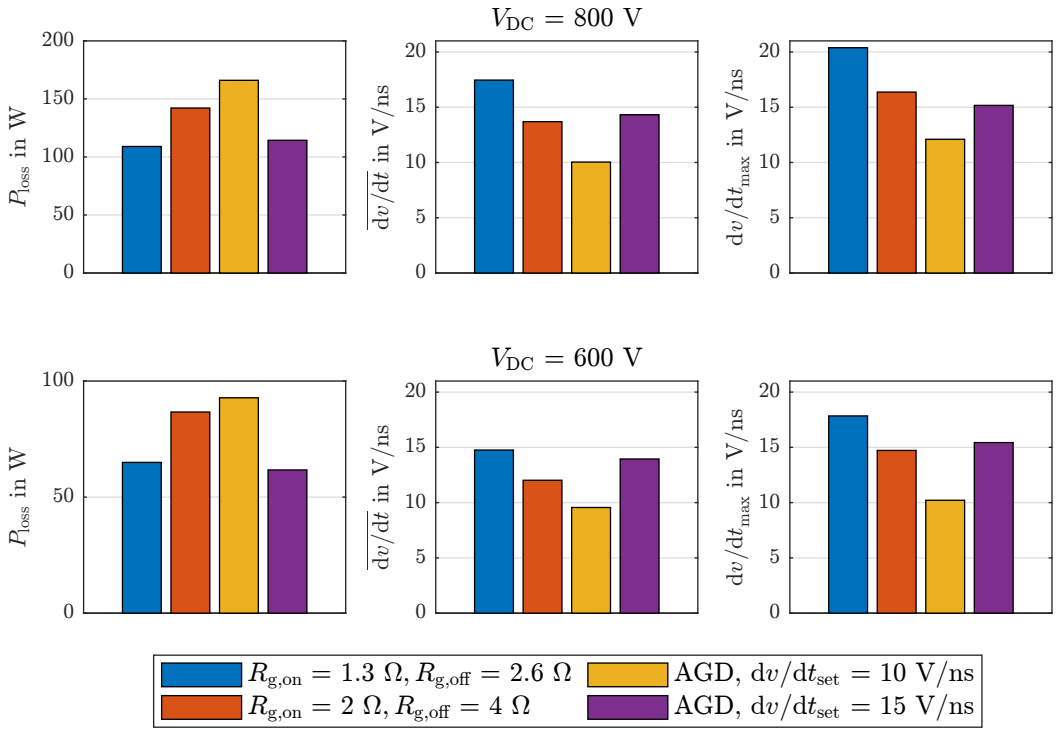

Fig. 10: Comparison of the performance of an AGD with different $\mathrm{d}v/\mathrm{d}t$ settings and a CGD with different gate resistors at various DC link voltages.

switching at the maximum $\mathrm{d}v/\mathrm{d}t$ imposed by the EMC requirements and machine characteristics. In future work, the effect of the AGD on the CM currents, EMC behavior and losses in an actual inverter will be investigated.

References

[1] R. Shirai, K. Wada, T. Shimizu, and D. Xu, "Suppressing emi noise to can communication by using active gate driver," in *2020 IEEE 9th International Power Electronics and Motion Control Conference (IPEMC2020-ECCE Asia)*, 2020, pp. 2648–2651.

[2] Y. Xu, X. Yuan, F. Ye, Z. Wang, Y. Zhang, M. Diab, and W. Zhou, "Impact of high switching speed and high switching frequency of wide-bandgap motor drives on electric machines," *IEEE Access*, vol. 9, pp. 82 866–82 880, 2021.

[3] H. Movagharnejad and A. Mertens, "Design methodology for dimensioning emi filters for traction drives with sic inverters," in *2021 23rd European Conference on Power Electronics and Applications (EPE'21 ECCE Europe)*, 2021, pp. 1–10.

[4] S. Zhao, X. Zhao, Y. Wei, Y. Zhao, and H. A. Mantooth, "A review of switching slew rate control for silicon carbide devices using active gate drivers," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 4, pp. 4096–4114, 2021.

[5] J. Wiesemann and A. Mertens, "An isolated variable-resistance active gate driver for use in sic-driven inverters," in *IECON 2021 – 47th Annual Conference of the IEEE Industrial Electronics Society*, 2021, pp. 1–6.

[6] Z. Meng, Y. Yang, Y. Gao, S. Ai, Y. Zhang, Y. Lv, Z. Zhang, Y. Wen, L. Wu, P. Zhang, and J. D. Thomson, "Prediction method of driving strategy of high-power igbt module based on mea-bp neural network," *IEEE Access*, vol. 8, pp. 94 731–94 747, 2020.

[7] J. D. Kagerbauer and T. M. Jahns, "Development of an active dv/dt control algorithm for reducing inverter conducted emi with minimal impact on switching losses," in *2007 IEEE Power Electronics Specialists Conference*, 2007, pp. 894–900.

[8] R. C. Kroeze and P. T. Krein, "Electrical battery model for use in dynamic electric vehicle simulations," in *2008 IEEE Power Electronics Specialists Conference*, 2008, pp. 1336–1342.

[9] E. Trancho, E. Ibarra, P. Prieto, A. Arias, A. Lis, and A. P. Pai, "Novel thermal management strategy for improved inverter reliability in electric vehicles," *Applied Sciences*, vol. 10, no. 22, 2020. [Online]. Available: https://www.mdpi.com/2076-3417/10/22/8024

[10] J. Ebersberger, J.-K. Mller, and A. Mertens, "Dynamic characterization of a sic-mosfet half bridge in hard- and soft-switching and investigation of current sensing technologies," in *2020 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe)*, 2020, pp. P.1–P.8.

[11] D. Han and B. Sarlioglu, "Study of the switching performance and emi signature of sic mosfets under the influence of parasitic inductance in an automotive dc-dc converter," in *2015 IEEE Transportation Electrification Conference and Expo (ITEC)*, 2015, pp. 1–8.