A Sectorized FCS-MPC Transformerless SST For Power Transmission Application

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Keywords

≪Multi-level converters≫, ≪Model predictive control≫, ≪High voltage power converters≫, ≪Solid-State Transformer≫, ≪Optimization algorithm≫.

Abstract

This work proposes a sectorized optimization with Graph Theory applied in cascaded multilevel transformerless SST. The sectorized optimization can reduce the FCS-MPC combinational explosion due to the multiple cascaded H-bridges cells, while the proposed control is capable to avoid the prohibitive states maintaining the converter controllability and power quality.

Introduction

The insertion of high-voltage and high-power industrial equipment [1], the rise of renewable sources transforming the world's energy matrix, and even the use of low-voltage low-power non-linear loads, tend to increase the distribution and transmission systems complexity [2]. Therefore, problems related to overload feeders, bidirectional power flow, voltage variation, and harmonic content have become an issue for distribution and transmission systems. Consequently, the electric power systems' behavior is changing, being before passive and static, and now becoming more active and dynamic [3]. In this context, the Solid-State Transformer (SST) comes up as an interesting alternative to the Line Frequency Transformer (LFT) since it can perform ancillary services, providing a dynamic control for distribution and transmission systems. The SST is lighter and less bulky, provides harmonic filtering ability, supports voltage variations, and presents controlled bidirectional active and reactive power flow [3]. Therefore, SSTs can be considered smart transformers, and are the key point for a change in electric power systems [4] [5].

To operate with a high-power demand, the SST topology should be able to synthesize high-voltage levels, which is impossible with conventional 2-level converters. Thus, several studies were proposed to overcome this issue, developing specific converters to meet the growing demand for high-power applications [1]. Multilevel converters have an inherent potential to disrupt the technological barrier for power semiconductors, mainly because of the advantages they present over conventional converters, such as synthesizing higher voltage levels using lower power devices, reducing voltage stress and switching frequency, presenting reduced harmonic content, and less common-mode noise generation [1]. The literature presents the Dual Active Bridge (DAB), a well-established module, which can constitute multilevel converters, and demonstrates the ease of control and a great use for application in microgrids [4]. However, this structure presents an increase in volume, weight, cost, and construction complexity of the SST by increasing the number of semiconductors used in conversion stages [2]. So, a possible alternative with the absence of the High Frequency Transformer (HFT) element and reduction of power loss, shows up as an interesting open field to be developed, which has already started to be studied by the authors [2] using only the Cascaded H-bridge modules (CHB) without galvanic isolation. This structure can be presented in back-to-back (B2B) configuration for more complex applications, in which the converter should be able to operate in all four quadrants, as for high-power applications, considering that the bidirectional power flow is indispensable [2].

In CHB-B2B, voltage levels can be established by the number of H-bridges modules used, and the type of association made, such as input-parallel output-parallel (IPOP), input-series output-parallel (ISOP), input-series output-series (ISOS), or input-parallel output-series (IPOS) [4]. All these configurations present a reduced components number when compared to other classic multilevel topologies [2]. However, as a disadvantage, because the proposed configuration does not present galvanic isolation provided by the HFT, several short-circuit switching states make it impossible for driving the CHB-B2B with classical control and PWM modulation. Therefore, a Finite Control Set Model-based Predictive Control (FCS-MPC) with a Graph Theory approach was proposed by the authors to define the possible switching matrix, eliminating the prohibitive states and, at the same time, ensuring the SST controllability and power quality. Graph Theory is a mathematical tool that facilitates the development of almost intuitive algorithmic rules [6], by the definition of structures called graphs, formed by vertex and arcs concepts. The correspondence between these elements can be related to various problems from different areas, providing the desired solutions. However, Graph Theory implementation in power electronics converters and systems is still in the exploring stage and an overview of this research topic is summarized in [7], approaching general application, milestones and benefits.

Nonetheless, due to computational effort issues, the proposed solution was limited to four H-bridges modules achieving only a 5-level high-voltage (HV) and two 3-level medium-voltage (MV) in an ISOP CHB-B2B configuration [2]. As a static switch can have two possible states, the converter switching possibilities will increase exponentially. Therefore, the more H-bridges modules in CHB structure are used, and consequently, the greater number of levels an SST has, the more challenging the implementation of FCS-MPC techniques will be, due to processing limitations, as the sampling period tends to be short [8]. Thus, to solve this problem, different approaches have been proposed. In [9], an equivalent cost function is used with only the possible output voltage vectors, reducing the prediction model dimension which implies that the computational burden is lower. The optimization stage is performed by an exhaustive searching algorithm. In [10], a modified cost function is implemented with a sphere decoding algorithm to optimize a problem in a new space unconstrained solution. In [11], a hierarchical method is used, splitting the optimization into two stages. The first stage analyzes only the possible output voltage vectors while the second stage uses the redundant stages. Alternatively, in this paperwork, the authors propose a different methodology to get around an exhausting search inside the FCS-MPC sample space. Although the FCS-MPC principles are maintained, the multilevel converter is sectorized, dividing it into smaller parts which significantly reduces the switching matrix to be evaluated. Thus, the computational cost of executing the algorithm is considerably reduced. Therefore, a 19-level 110 kV : 30 kV SST with reduced components and without HFT galvanic isolation, with multiple output windings composed of 18 H-bridges modules in ISOP back-to-back configuration is implemented to demonstrate the proposed

strategy applicability. The aforementioned FCS-MPC with Grapy Theory approach developed by the authors is also used in this work. Simulation results prove the proposed sectorized optimization FSC-MPC with Graph Theory effectiveness.

This paperwork is organized as follows: the proposed topology and Graph Theory analysis are provided first. The FCS-MPC equations are then presented, along with the proposed sectorized optimization. The findings of MatLab/Simulink are then displayed, followed by the conclusion.

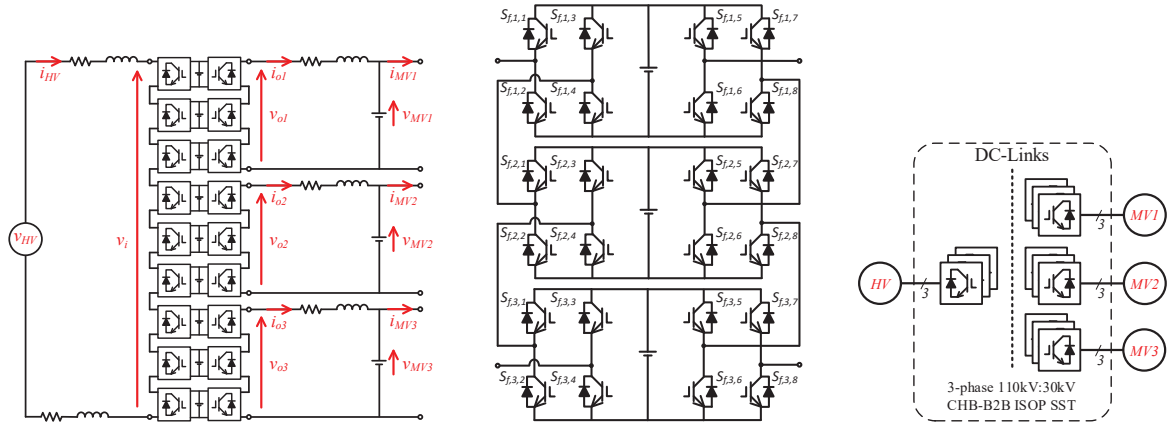
Proposed SST Topology and Graph Theory analysis

Currently, SSTs are mainly used at the distribution voltage level, which varies from 2.3 kV to 35 kV [4]. For transmission voltage levels, the H-bridges modules increment must be performed to achieve high-voltage and high-power applications. The Union for the Coordination of the Transmission of Electricity (UCTE) consists of the largest synchronously operated electrical grid. Thereby, this system is very important for the European and world economy, and its constant improvement is necessary. Some Distribution System Operators (DSOs) associated with UCTE, which partly operate in Europe high-voltage grids, work with 30 kV to 110 kV 50 Hz transmission lines. Considering the SSTs advantages and aiming to expand its application to high-voltage and high-power systems, this work presents a new topology to be applied in the UCTE grid. Fig. 1a presents the proposed SST topology, which uses a 9 H-bridges modules series connection in the HV stage, and 3 disassociated series connections with 3 H-bridges modules in the MV stage. In this arrangement, a naturally 3:1 transformation ratio becomes possible to be obtained. As the secondary MV side has multiple windings, the SST structure could be sectorized in three different parts, as highlighted in Fig. 1b. This sectorized structure should be used in the Graph Theory analysis and also in the proposed optimization process to reduce de computational effort. Fig. 1c shows the proposed simplified scheme in 3-phase way, although this paperwork is addressed only the results for one phase.

The CHB-B2B may generate internal short-circuits according to the switching state. The conditions that can lead to a short-circuit must be defined, which are: i) the terminals of each capacitor become shorted, and ii) the opposite terminals of a group of capacitors become connected, which implies a ring with series capacitor connections. A connected and undirected graph from Graph Theory can be modeled considering the electrical nodes as vertices, and electrical switches as edges [12]. Thus, by finding simple paths that interconnect vertices, that represent both capacitor terminals, it is possible to visualize part of the prohibitive states. The other part is obtained by joining disjoint paths that interconnect different pairs of opposite terminals for any number of capacitors. Fig. 1b presents the sectorized structure composed of 12 legs, providing 212 (4,096) combinations. When applying Graph Theory to this topology, it is observed that only 576 of these switching states are useful, with the other combinations causing short-circuit states. It is important to emphasize that, with only 14% of the possible states, the sectorized part of the SST manages to synthesize all 7-level voltages, showing the applicability of the proposed topology and the usefulness of Graph Theory in mapping prohibitive states.

FCS-MPC and sectorized optimization

The FCS-MPC has attracted attention in the power electronics research community, for being a simple and intuitive way to control the converters, besides its ability to handle multivariable goals, showing good controllability and fast dynamic response, and capacity to incorporate straightforwardly nonlinearities and constraints into the control law [8], as the proposed 19-level CHB-B2B prohibitive switching states. For this converter, the HV and MV stages have together 72 switches, presenting 2^{36} (68,719,476,736) possible switching states, due to the leg complementary switches. Even with Graph Theory application aiming to reduce this amount with the short-circuit states removal becomes infeasible, since the digital FCS-MPC implementation have to perform mathematical calculations for each of these states, and currently, there is no availability of hardware to meet these demand requirements. The solution adopted to allow the system's control is to sectorize the converter into three parts, as seen in Fig. 1b. Therefore, with a smaller composition, each sector presents 2^{12} (4,096) possible switching states, but within these, only



(a) (b) (c)

Fig. 1: New topology schematic. a) 19-level proposed SST topology, b) 7-level sectorized structure and c) 3-phase overview.

576 do not represent short-circuits. Thus, the new converter's switching matrix consists of the combination of the reduced switching matrices (S_s) obtained by Graph Theory, and thus, the converter control can be performed semi-independently for each sector, due to the MV control of each feeder haven't relations among themselves. However, the HV input current control is unique and a strategy that relates the three switching matrices adopted must be implemented. Therefore, the sampling space is drastically reduced, with the prediction of 3x576 (1,728) switching states, which represents a 99.99% reduction (1,728 / 68,719,476,736), making the control system practicable.

The FCS-MPC strategy implementation requires the dynamics equations for the DC-links, HV, and MV stages. The state of the H-bridge cell, with $S_{f,n,j}$ representing the jth S switch in the nth H-bridge cell of the fth feeder is represented by $d_{HVf,n}$ and $d_{MVf,n}$, for HV and MV stages respectively (see Fig. 1b), and are obtained by equations (1) and (2). Therefore, $d_{HVf,n}$ and $d_{MVf,n}$ can assume three logical values (1, 0, 1), according to the switches' state defined by different rows in S_s.

$$d_{HV,f,n} = S_{f,n,1}S_{f,n,4} - S_{f,n,2}S_{f,n,3} \tag{1}$$

$$d_{MV,f,n} = S_{f,n,5}S_{f,n,8} - S_{f,n,6}S_{f,n,7} \tag{2}$$

Analyzing Fig. 1a, the equation for nth DC-link voltage level of the fth feeder ($v_{dcf,n}$) can be obtained in (3), considering i_{of} the L filter current for the fth feeder and assuming that the values of the capacitors for each DC link (C_{dc}) are equal for a generalized equation. For MV predictive model, the controlled variables are the fth feeder's MV output (v_{MVf}) and the control loop is composed of the load connection point and LC output filter. Considering v_{of} as the fth feeder synthesized output voltage as described in (4), l_i the inductive components of inverters' LC filters, with r_i modeling its electrical losses, the following relationship (5) for i_{of} is found.

$$\frac{dv_{dcf,n}}{dt} = \frac{1}{C_{dc}}\left(d_{HVf,n}i_{HV} - d_{MVf,n}i_{o_f}\right) \tag{3}$$

$$v_{of} = \sum_{n=1}^{3} d_{MVf,n}v_{dcf,n} \tag{4}$$

$$\frac{di_{o_f}}{dt} = \frac{1}{l_i}\left(v_{of} - r_i i_{of} - v_{MVf}\right) \tag{5}$$

Relying on the dynamics of capacitive components in inverters' *LC* filters (C_i), the relationships of the control variables are presented in (6). In the HV stage, the controlled variable is its current (i_{HV}) and the control loop is formed by the grid voltage (v_{HV}) and the *L* filter, made up of r_r and l_r elements, the first one modeling electrical losses of the inductor. Using the same procedures as above and considering v_i as the HV synthesized output voltage, calculated through the summation in equation (7), the i_{HV} the relation is obtained and shown in (8).

$$\frac{dv_{MV_f}}{dt} = \frac{1}{C_i}\left(i_{o_f} - i_{MV_f}\right) \tag{6}$$

$$v_i = \sum_{f=1}^{3}\sum_{n=1}^{3} d_{HV_{f,n}} v_{dc_{f,n}} \tag{7}$$

$$\frac{di_{HV}}{dt} = \frac{1}{l_r}\left(v_{HV} - r_r i_{HV} - v_i\right) \tag{8}$$

The discrete equations necessary for the FCS-MPC application are obtained using the Euler numerical integration method in equations (3), (5), (6), and (8), in which [k] and [k+1] are the present and future instants respectively. To adapt equation (7) for the sectorized control strategy, the v_i term, which has 576 values possibilities according to switching, is replaced by *N*, a vector containing, in ascending order of values, the possible levels synthesized by the converter for nominal values of the DC-links. The discrete equations (9), (10), (11) and (12) infer different values for different switching. For example, an iteration with a variable *i* traversing all rows of S_s results in varying predicted values.

$$v_{dc_{f,n}}[k+1] = v_{dc_{f,n}}[k] + \frac{T_s}{C_{dc}}\left(d_{HV_{f,n}}[k]\, i_{HV}[k] - d_{MV_{f,n}} i_{o_f}\right) \tag{9}$$

$$i_{o_f}[k+1] = i_{o_f}[k] + \frac{T_s}{l_i}\left(v_{o_f}[k] - r_i i_{o_f}[k] - v_{MV_f}[k]\right) \tag{10}$$

$$v_{MV_f}[k+1] = v_{MV_f}[k] + \frac{T_s}{C_i}\left(i_{o_f}[k+1] - i_{MV_f}[k]\right) \tag{11}$$

$$i_{HV}[k+1] = i_{HV}[k] + \frac{T_s}{l_r}\left(N - r_r i_{HVk} - v_{HV}[k]\right) \tag{12}$$

The next step is to define the reference signals for the control variables, which for each feeder (v^*_{MV}) and DC-link (v^*_{dc}) consist of their respective nominal operating ratings (Table I). The HV current reference (i^*_{HV}) is obtained from PQ theory [13] together with a Second-Order Generalized Integrator (SOGI) [14]. Thus, preliminary cost functions (g_{pf}) can be defined for each feeder (13), considering only the DC-link and inverter stages, and calculating average DC-links voltages (14) for the proposed sectorized methodology. Weights are defined to designate which control object should be prioritized: v_{MVf} voltage synthesis (W_{MV}), regulation of DC-links (W_{dc}) or balance of DC-links (W_{bl}).

$$g_{pf} = W_{dc}\sum_{n=1}^{3}\left|v^*_{dc} - v_{dcf,n}[k+1]\right| + W_{bl}\sum_{n=1}^{3}\left|v_{av_f} - v_{dcf,n}[k+1]\right| + W_{MV}\left|v^*_{MV} - v_{MVf}[k+1]\right| \tag{13}$$

$$v_{avf} = \frac{1}{3}\sum_{n=1}^{3} v_{dcf,n}\,[k+1] \tag{14}$$

The most significant control challenge is to control the system's input current described in (12) as it is dependent on the voltage levels presented in DC-links ($v_{dcf,n}$) and their respective possible series interconnections forming v_i (see Fig. 1a). Typically, the FCS-MPC methodology would use the full converter switching matrix, leading to a computational explosion. However, as mentioned, the sectorized strategy uses a reduced switching matrix obtained by Graph Theory, in which a direct application cannot achieve one of the control objectives, which consists of regulating the i_{HV} current. Therefore, the principles proposed for the solution of this issue are to initially treat the voltage variables of the DC-links as controlled on nominal ratings, and the definition of an auxiliary's matrix set (M). Each auxiliary matrix represents one specific converter voltage level, and consequently, one N array row (totalizing 19 matrices), with its row's elements containing ascending ordered different logical states possibilities for HV stage ($d_{HVf,n}$ [k]: -1, 0, 1). They correspond too into switched H-bridges voltages levels ($-v_{dc}$, 0, v_{dc}), which, together, form the voltage level that each matrix is related. Thus, the greater the voltage modulus related to each of the matrices, smaller is the number of combination possibilities for logical switching. For example, the matrix associated to the minimum voltage level $-9v_{dc}$ has only one combination. For such, all H-bridges modules must switch $-v_{dc}$, corresponding to a final v_i equal to $-9v_{dc}$ (summation of $-9v_{dc}$ matrix rows).

$$-9v_{dc}\ matrix = \begin{bmatrix} -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 \end{bmatrix}$$

The proposed sectorized control strategy initially performs the same procedures as the FCS-MPC to control i_{HV}. However, instead of considering the sectorized switching matrix and, consequently, different switched voltages for each H-bridge module, it considers the voltage levels that can be synthesized by all of them (N elements) and selects the optimal voltage among the possible 19-levels. This can be done through the predictions of i_{HV}[k+1] using (12) and the minimization of another cost function (15), and therefore, it is defined which auxiliary matrix (M_{opt}) is used for a given instant of time. Meanwhile, each auxiliary matrix itself does not specify exactly the voltage level that each H-bridge module must switch; this is accomplished by analyzing the voltage level that each DC-link has at a given instant of time, the power flow (current direction) to which the modules are subjected, in addition to the others control objectives, as described in (13), since the rectifier v_i voltage corresponds to the selected optimal voltage.

$$g_r = |i^*_{HV} - i_{HV}\,[k+1]| \tag{15}$$

Analyzing equation (9), it is verified that the contribution of the HV side depends on the logic state of the H-Bridges and on the signal that the measured current i_{HV} have at a given instant of time. Being this positive, the capacitors must be charged if the logic state of the H-bridges ($d_{HV_{f,n}}$) corresponds to 1, discharged if this value corresponds to -1, and maintain their voltage levels for a logical value equal to 0. Contrary results should occur for the condition of $i_{HV} < 0$. Thus, a principle is defined that capacitors with a lower voltage level, below the nominal ratings, at a given instant of time, have charging priority over the others. Those that have a higher voltage level, above nominal ratings, must have priority to be discharged (provide the necessary power flow to the system's feeders). Based on these ideas, and once M_{opt} has been selected, each row must be reordered logically: The direction of i_{HV} current is analyzed. If it is positive, the DC-links are sorted ascending according to their voltage levels. Otherwise, the voltage levels of each module are sorted in descending. Relating each column of M_{opt} to a specific DC-link, each row is reordered according to the ordering of the DC-links, determining which capacitors needs to be charged and discharged, keeping the balance between them, thus forming an ordered matrix denominate OM. For example, considering the $-v_{dc}$ matrix, if at a certain point in time, $v_{dc2,1} < v_{dc3,1} < v_{dc1,2} < v_{dc1,1} < v_{dc3,2} < v_{dc3,3} < v_{dc1,3} < v_{dc2,3} < v_{dc2,2}$ and $i_{HV} > 0$, the ordered $-v_{dc}$ matrix consists as shown below.

$$M_{opt}\ (-v_{dc}) = \begin{array}{|cccccccc|c} v_{dc2,1} & v_{dc3,1} & v_{dc1,2} & v_{dc1,1} & v_{dc3,2} & v_{dc3,3} & v_{dc1,3} & v_{dc2,3} & v_{dc2,2} \\ \hline -1 & -1 & -1 & -1 & -1 & 1 & 1 & 1 & 1 \\ -1 & -1 & -1 & -1 & 0 & 0 & 1 & 1 & 1 \\ -1 & -1 & -1 & 0 & 0 & 0 & 0 & 1 & 1 \\ -1 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ \hline \end{array}$$

$$\downarrow$$

$$OM\ (-v_{dc}) = \begin{array}{|cccccccc|c} v_{dc1,1} & v_{dc1,2} & v_{dc1,3} & v_{dc2,1} & v_{dc2,2} & v_{dc2,3} & v_{dc3,1} & v_{dc3,2} & v_{dc3,3} \\ \hline -1 & -1 & 1 & -1 & 1 & 1 & -1 & -1 & 1 \\ -1 & -1 & 1 & -1 & 1 & 1 & -1 & 0 & 0 \\ 0 & -1 & 0 & -1 & 1 & 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & -1 & 1 & 0 & -1 & 0 & 0 \\ 0 & 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 \\ \hline OM_{1,1} & OM_{1,2} & OM_{1,3} & OM_{2,1} & OM_{2,2} & OM_{2,3} & OM_{3,1} & OM_{3,2} & OM_{3,3} \end{array}$$

$-1 \rightarrow$ *charge capacitors*; $0 \rightarrow$ *mantaining voltage level*; $1 \rightarrow$ *discharge capacitors*

Finally, the proposed algorithm must perform iterations that go through all rows of OM. At each iteration, new global cost functions g_{gf}, defined in (16), are calculated for each one of the feeders, through preliminary calculated cost functions g_{pf} and the comparison of each OM row's elements ($OM_{f,n}$) with a voltage level determined by the sectorized switching matrix (S_s) of each converter's sectors ($d_{HV_{f,n}} v_{dc_{f,n}}$). The W_{HV} weight is defined to assign i_{HV} control priority. At each iteration, is realized a minimization of the global cost functions g_{gf}, and a final cost function g_g is obtained through the summation of g_{gf} elements considering different feeders. Finally, after all iterations, the last minimization is performed in g_g to select which OM line is optimal for the switching. Therefore, it is possible to determine the optimal switching for each sector (S_{sopt_f}). Fig. 2 presents the overview operation of the sectorized FCS-MPC methodology applied to the proposed 19-level CHB-B2B, and Fig. 3 highlights the SST FCS-MPC algorithm.

$$g_{gf} = g_{pf} + W_{HV} \sum_{n=1}^{3} \left| OM_{f,n} v_{dc_{f,n}} - d_{HV_{f,n}} v_{dc_{f,n}} \right| \tag{16}$$

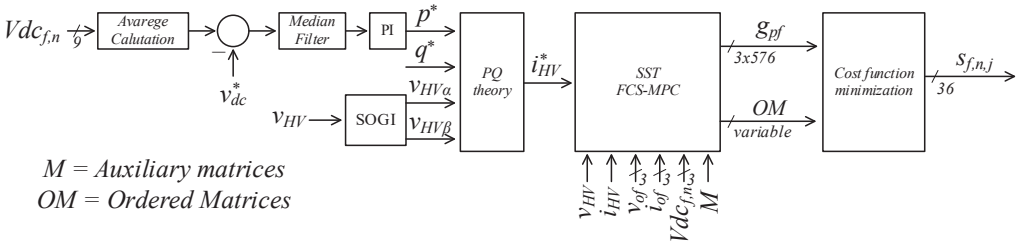


Fig. 2: Control diagram overview.

Simulation results

The steady-state and transient performance of the proposed 19-level ISOS CHB-B2B converter with the FCS-MPC optimization algorithm are verified by simulation, through Matlab/Simulink platform, and the parameters used for the circuit are described in Table I. The steady-state load scenario parameters are described in Table II, in which an apparent power demand of 10 MVA was defined for each one of the feeders, with an active power imbalance of 20% between the first and second feeders. Different load types are used for each feeder, representing high-power industrial equipment and non-linear loads, which brings this MV system closer to practical applications.

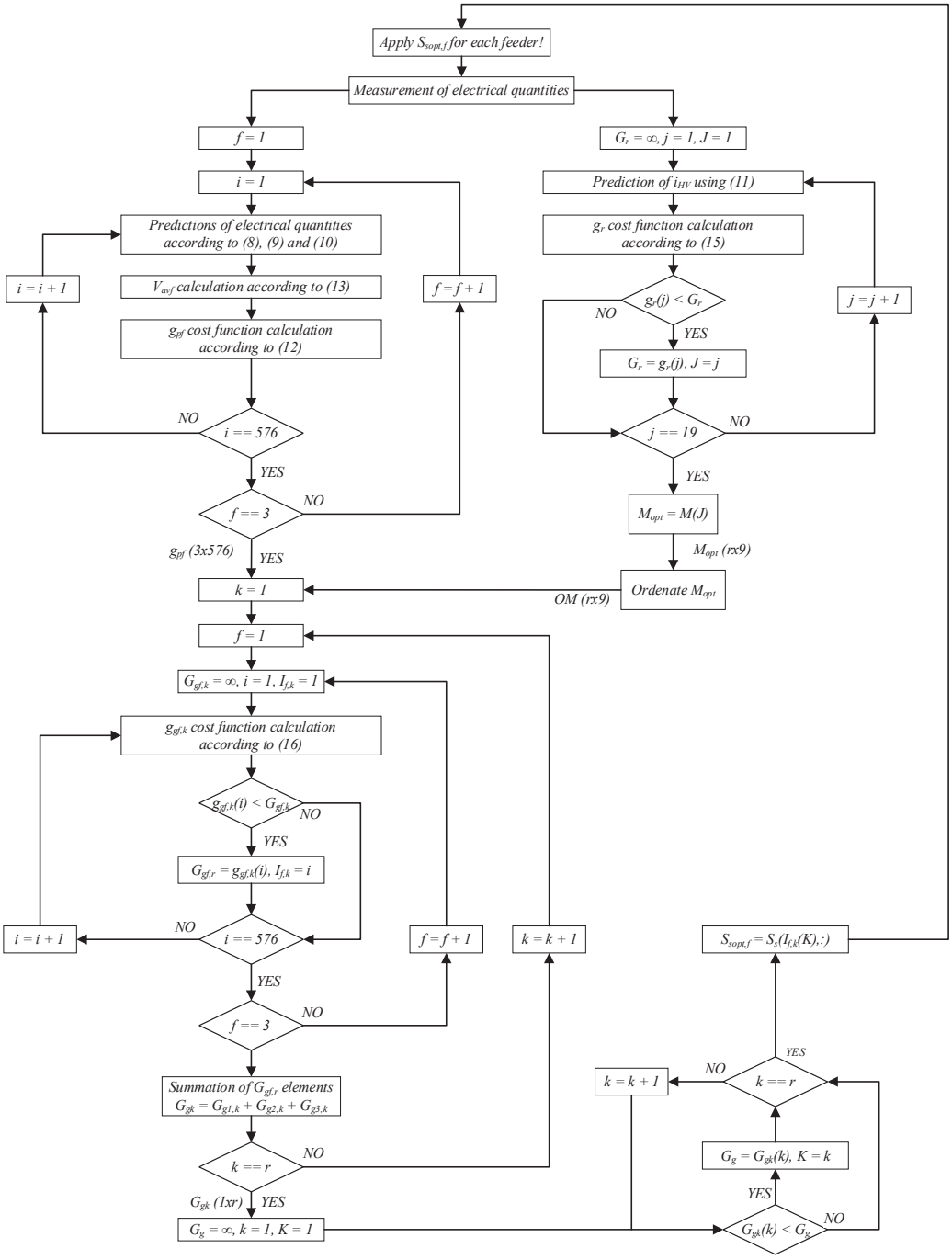


Fig. 3: SST FCS-MPC algorithm.

In Fig. 6, it can be observed the steady-state response of the FCS-MPC controlled variables: HV current (i_{HV}), DC-link voltages ($v_{dcf,n}$) and MV feeders (v_{MVf}). The voltage synthesized by the HV converter (v_i) and its reference calculated by the control system (N_{sel}) are also highlighted. As it can be seen in Fig. 4a, the sectorized FCS-MPC technique can synthesize a sinusoidal rectifier current that properly tracks the reference (i^*_{HV}), allowing the DC links regulation with a high power factor. It can also be noted in Fig. 4b that for synthesizing this current, the 19 possible voltage levels on the HV stage were achieved, which will guarantee a lower harmonic distortion (THD (i_{HV}) = 2.11%). Analyzing Fig. 4c, it is verified that all DC-link voltages are properly regulated with a maximum 0,54% oscillation at the nominal value, even for different feeders' load types, essential for the correct control functioning. Finally, is observed in Fig. 4d that all inverter output voltages can track the sinusoidal (v^*_{MV}) reference, even for non-linear load conditions (i_{MV3} current), ensuring a 110 kV:30 kV transformer voltage rating, as expected. Table

III shows the total harmonic distortion for the output voltages and currents, the first having an adequate harmonic content, reflecting in energy quality, since it is independent of the load. Therefore, THD results corroborate that the proposed 19-level ISOS CHB-B2B converter meets the IEEE Std 519™ required limits, namely a maximum of 8% THD for the feeders' output voltage and 5% for grid input current [15].

In Fig. 7, it can be observed the transient response of the FCS-MPC controlled variables. Initially, the specified loads expressed in Table II are operating in steady-state regime with the inductive load operating with 50% less reactive power. In 1.5s, the reactive power demand of the inductive load is increased by 50%. Later, at 1.55s, the resistive load is decreased by 20%. Fig. 5a shows that even with a load disturbance, the system's control is able to synthesize i_{HV} properly. Fig. 5b presents that the converter continues to switch the expected 19 voltage levels, while Fig. 5c shows that the DC-links continued to be balanced and controlled. Finally, Fig. 5d demonstrates that all voltage outputs from the feeders are still properly synthesized, in addition to changes in load currents according to the variation of the power demanded.

Table I: Simulation Parameters.

Parameter	**Symbol**	**Value**
HV voltage	v_{HV}	$110\sqrt{2}/\sqrt{3}\ kV$
MV voltage	$v_{MV,f}$	$30\sqrt{2}/\sqrt{3}\ kV$
DC-link nominal voltage	V_{dcn}	$10\ kV$
DC-link capacitance	C_{dcn}	$5\ mF$
Rectifier inductance	l_r	$100\ mH$
Rectifier resistance	r_r	$0.001\ m\Omega$
Inverter inductance	l_i	$7.5\ mH$
Inverter resistance	r_i	$1.5\ m\Omega$
Inverter capacitance	C_i	$3.54\ \mu F$
Grid frequency	f_{HV}	$50\ Hz$
The median filter window length	M	200
PI controller proportional gain	K_p	1
PI controller integral gain	K_i	50
Time Step	T_s	$50\ \mu s$
Input current weight	W_{HV}	1
Output voltage weight	W_{MV}	500
DC-link voltage weight	W_{dc}	10
Balance weight of DC-links	W_{bl}	5

Table II: Load Parameters.

Load type	**Feeder**	**Values**
Resistive	1	$90\ \Omega$
Inductive	2	$112.5\ \Omega\ /\ 477,46\ mH$
Nonlinear	3	$2\ mH\ (AC)\ \vert\ 70\ \Omega\ /\ 1\ H\ (DC)$

Table III: THD Analysis.

Feeder	**THD** (v_o)	**THD** (i_o)
1	1.36%	1.36%
2	1.34%	1.08%
3	1.67%	42.86%

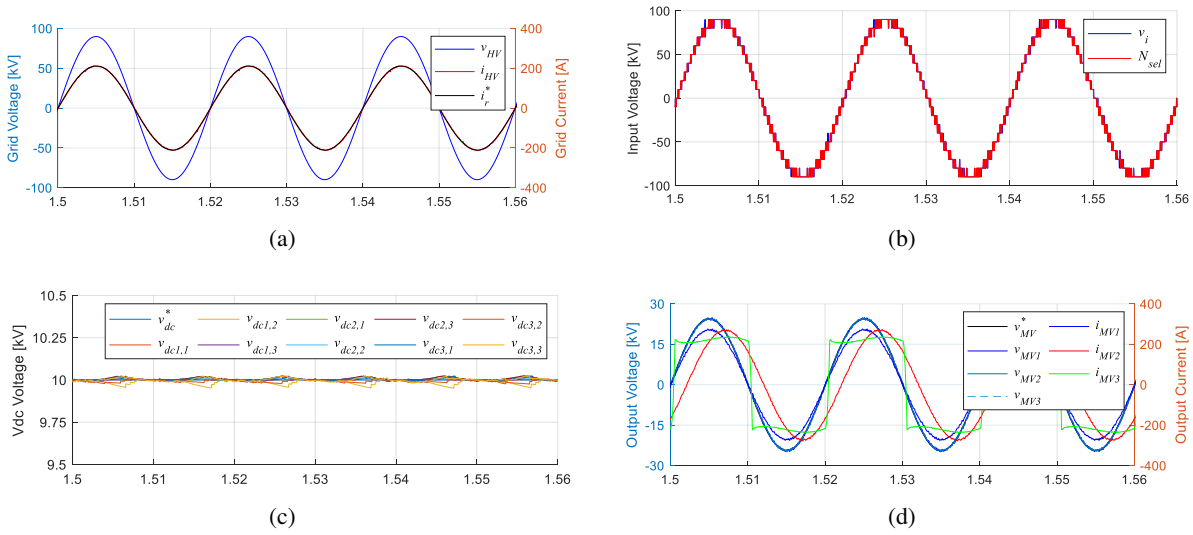


Fig. 4: Steady-state results. a) HV measurements b) HV converter stage, c) DC-links, and d) MV measurements.

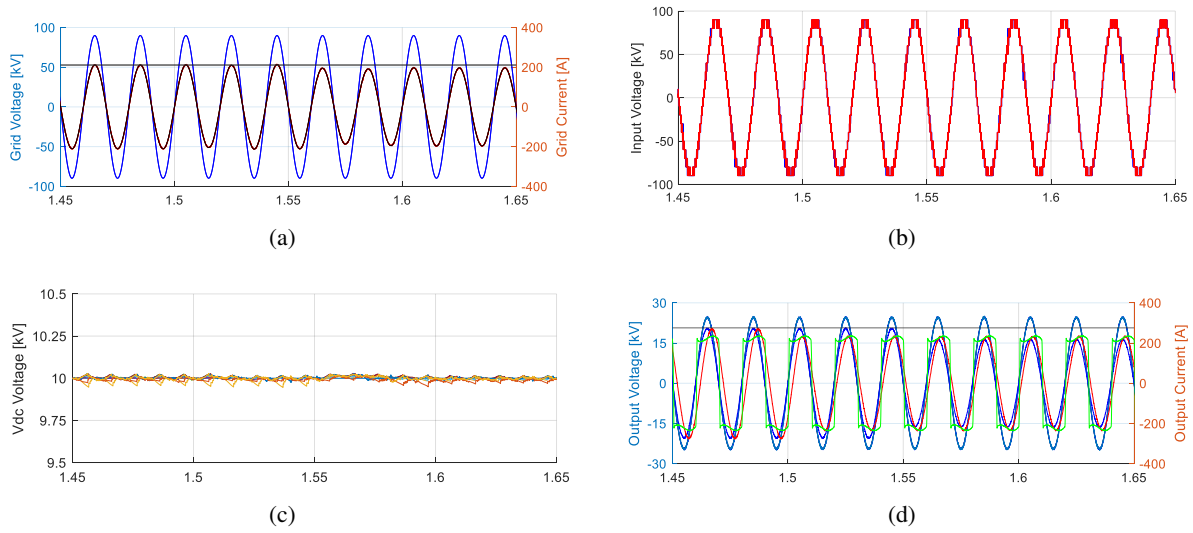


Fig. 5: Transient results. a) HV measurements b) HV converter stage, c) DC-links, and d) MV measurements.

Conclusion

Based on the steady-state results, the proposed sectorized FCS-MPC methodology for the 19-level CHB-B2B converter ensures a reduced computational effort, avoiding possible internal short-circuits, balancing DC-links voltage, and enabling HV current control and multiple windings MV output with low harmonic distortion, meeting the IEEE Std 519™ requirements, even in presence of non-linear loads. The proposed control algorithm also showed a good response to load disturbances, keeping all control variables regulated for active and reactive power demand variations.

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