DC-bus Neutral Voltage Balancing Based on DΣ Control Method

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Abstract - **This study proposes a half-bridge dc-bus spilt-capacitor voltage balancing circuit based on DΣ control. The circuit can be designed according to the load requirements and be connected to a three-phase four-wire inverter. The balancing circuit is used to eliminate dc offsets due to process errors in the upper and lower arm dc-bus capacitor voltages and to eliminate ac components due to unbalanced loads. In addition, this method incorporates the neutral current into the calculation, so that the capacitor voltages are effectively balanced regardless of the load phase or amplitude imbalance. Finally, a dynamic model of the voltage balancing system is derived and validated with Matlab / Simulink numerical analysis software.**

I. INTRODUCTION

In recent years, energy issues have received a lot of attention, and many experts have devoted themselves to research on related topics [1]-[5]. In the applications of three-phase converters, the three-phase three-wire converters are usually used in balanced load because they do not have a neutral circuit. On the contrary, they cause phase voltage imbalance. With a three-phase four-wire converter, there is a neutral wire for the unbalanced current, so the three-phase four-wire converter is more suitable for applications with unbalanced loads [6]-[9].

With the change of load pattern and mismatched upper and lower arm capacitors, the upper and lower arm capacitor voltages have dc offset and ac ripple components. It will increase the voltage stress of the power components, which will easily cause damage to the components.

Therefore, many experts are engaged in the research of split-capacitor balancing circuits, of which one of the methods is the use of the vector space modulation SVPWM technique [10]. Another method is to regulate the upper and lower arm voltages by adjusting the current on the ac side of the converter. In the case of voltage converters, the output current must be changed by adjusting the output voltage, which will affect the power quality of the output voltage. In the case of grid-connected converters, changing the output current directly will affect the power quality injected into the grid [11].

Another approach is to add a circuit on the dc side to regulate the upper and lower arm capacitance voltages. This circuit consists of two series-connected switches, and an inductor. In [10], a three-level neutral-clamping circuit is used and SVPWM is used to regulate the neutral voltage, but the neutral voltage control method is not fully decoupled. In [11], a dual-loop control strategy is used, in which the voltage error of the upper- and lower-capacitor arms is fed to a proportional controller in the outer loop control, and then the output is added as a dc component to the existing current controller to offset the unbalanced current flowing through the two capacitors. However, with this approach, the input power factor becomes poor. In [12], a three-level diode-clamped multilevel converter architecture is used for the converter and a multi-carrier is used for control. However, their neutral-voltage control method is not fully decoupled and affects the output power quality. In [13], a balanced circuit with passive components is proposed, although this control method only uses hardware to achieve voltage control of the spilt capacitor. However, the control strategy cannot be changed flexibly as the load changes.

To solve the above problem, this paper proposes to use a half-bridge, as the main circuit structure for the voltage balancing circuit, and the inductor between the upper- and lower-arm capacitors. In order to simplify the controller design, this paper adopts the DΣ control method to regulate the upper- and lower-arm voltages by simple derivation. To improve the problem of unbalanced upper- and lower-arm voltages when the three-phase load is unbalanced, the DΣ control is also adopted.

II. SYSTEM ARCHITECTURE

Fig. 1 shows the hardware architecture of the three-phase four-wire converter, including the half-bridge upper- and lower-arm voltage balancing circuit and the three-phase four-wire dc-ac converter. The half-bridge converter is redrawn as shown in

Fig. 2.

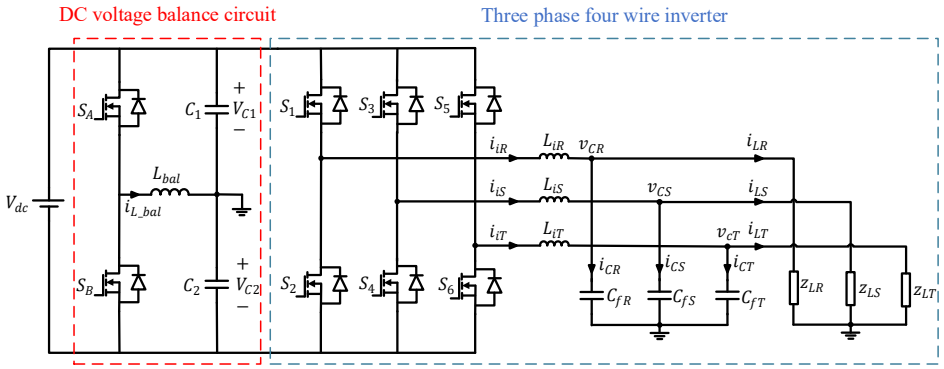

Fig. 1. Three-phase, four-wire system architecture

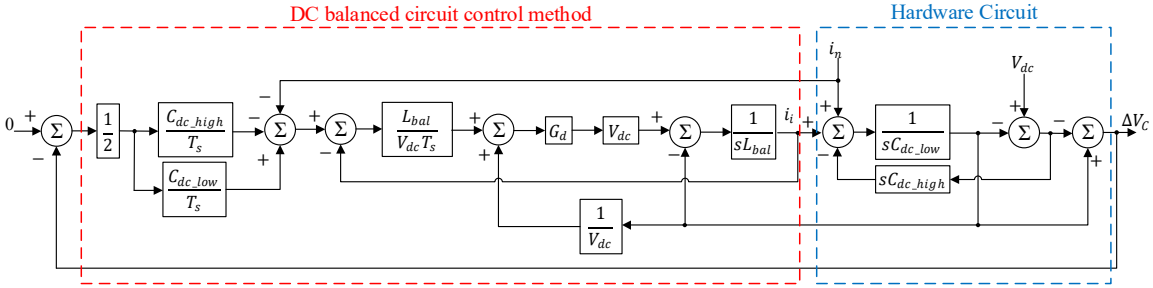

Fig. 2 Dynamic model of voltage balance circuit control

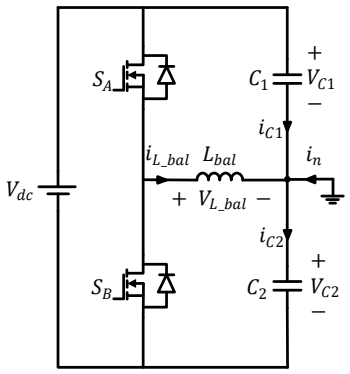

Fig. 3. Half-bridge balanced Circuit.

From Fig. 3, it can be deduced that the magnetization current variation $(\Delta i_{L\_bal}^{+})$ and the demagnetization current variation $(\Delta i_{L\_bal}^{-})$ of the energy storage inductor (L_{bal}) in the balanced circuit can be expressed as follows, where $\Delta i_{L\_bal}^{+}$ occurs when the switch S_A is on and S_B is off, and $\Delta i_{L\_bal}^{-}$ occurs when S_A is off and S_B is on.

Magnetization mode$(S_A = 1, S_B = 0)$:

$$\Delta i_{L\_bal}^{+} = \frac{V_{dc\_high}}{L_{bal}} \cdot DT_s \tag{1}$$

Demagnetization mode$(S_A = 0, S_B = 1)$:

$$\Delta i_{L\_bal}^{-} = \frac{-V_{dc\_low}}{L_{bal}} \cdot (1-D)T_s \tag{2}$$

(1)and (2) can be added together to obtain the current change over one cycle as follows:

$$\Delta i_{L\_bal} = \frac{V_{dc\_high}}{L_{bal}} \cdot DT_s - \frac{V_{dc\_low}}{L_{bal}} \cdot (1-D)T_s \tag{3}$$

After derivation, one can obtain the duty ratio:

$$D = \frac{V_{dc\_low}}{V_{dc}} + \frac{L_{bal}}{V_{dc}T_s}\Delta i_{L\_bal} \tag{4}$$

To balance the upper- and lower-arm capacitor voltages effectively, their voltages can be adjusted by the capacitor current compensation method. First, the difference between the balancing voltage and the actual capacitor voltage is measured to estimate the capacitor current to be compensated:

$$i_{C\_high}[n+1] = \frac{1}{2}\frac{C_{dc\_high}}{T_s}\left(-V_{dc\_high}[n] + V_{dc\_low}[n]\right) \tag{5}$$

$$i_{C\_low}[n+1] = \frac{1}{2}\frac{C_{dc\_low}}{T_s}\left(V_{dc\_high}[n] - V_{dc\_low}[n]\right) \tag{6}$$

where $V_{dc\_high}[n]$ and $V_{dc\_low}[n]$ are the voltages of the upper- and lower-arm capacitors, respectively.

Then, using the relation of KVL, thus, Δi_{L_bal} can be expressed as:

$$\Delta i_{L\_bal}[n+1] = \overbrace{-i_{C\_high}[n+1] + i_{C\_low}[n+1] - i_n[n]}^{reference} - \overbrace{i_{L\_bal}[n]}^{feedback} \tag{7}$$

where i_{C_high} and i_{C_low} are the estimated capacitor current commands in (5) and (6), respectively, i_n is the neutral current, and i_{L_bal} is

the controlled inductor current feedback value.

To simplify the design process, (5) and (6) are derived by defining the upper- and lower-arm capacitor voltage difference as:

$$\Delta V_C[n] = V_{dc\_low}[n] - V_{dc\_high}[n] \tag{8}$$

Finally, the control dynamic model can be derived, as shown in Fig. 2.

III. Balancing-Circuit Parameters Design

Generally, the neutral capacitor in a 3-phase 4-wire converter will cause imbalance in the upper- and lower-arm capacitor. With different degrees of amplitude or phase imbalances, they will cause different degrees of voltage imbalances in the upper and lower arm. When designing the upper- arm and lower-arm capacitance, it is assumed that their capacitance values are the same $\left(C_{dc\_high} = C_{dc\_low} = C_{bus}\right)$.

The neutral point of the three-phase four-wire is connected to the midpoint of the two capacitors. In general, the output current of a three-phase converter can be expressed as follows when the three-phase load is balanced. At this time, the neutral current is approximately "0":

$$\begin{aligned} i_{oa} &= I_p \sin(\omega_0 t) \\ i_{ob} &= I_p \sin\left(\omega_0 t + \frac{2}{3}\pi\right) \\ i_{oc} &= I_p \sin\left(\omega_0 t - \frac{2}{3}\pi\right) \end{aligned} \tag{9}$$

then,

$$i_n = i_{oa} + i_{ob} + i_{oc} \approx 0 \tag{10}$$

Next is the analysis of the neutral current when the phase and amplitude are unbalanced, and the three-phase current can be expressed as:

$$\begin{aligned} i_{oa} &= I_p \sin(\omega_0 t) \\ i_{ob} &= (1+\alpha) I_p \sin\left(\omega_0 t + \frac{2}{3}\pi + \beta\right) \\ i_{oc} &= (1-\alpha) I_p \sin\left(\omega_0 t - \frac{2}{3}\pi - \beta\right) \end{aligned} \tag{11}$$

$$\begin{aligned} i_{oa} &= I_p \sin(\omega_0 t) \\ i_{ob} &= (1+\alpha) I_p \left[\sin\left(\omega_0 t + \frac{2}{3}\pi\right) \cdot \cos(\beta) \right. \\ &\qquad \left. + \cos\left(\omega_0 t + \frac{2}{3}\pi\right) \cdot \sin(\beta)\right] \\ i_{oc} &= (1-\alpha) I_p \left[\sin\left(\omega_0 t - \frac{2}{3}\pi\right) \cdot \cos(-\beta) \right. \\ &\qquad \left. - \cos\left(\omega_0 t - \frac{2}{3}\pi\right) \cdot \sin(-\beta)\right] \end{aligned} \tag{12}$$

where α and β are the amplitude and phase imbalance coefficients, respectively.

To simplify the derivation process, $\cos(\beta)$ and $\sin(\beta)$ can be approximated as "1" and "β", assuming that β tends to be 0:

$$i_{oa} = I_p \sin(\omega_0 t) \tag{13}$$

$$\begin{aligned} i_{ob} \approx I_p \left[\left[\sin\left(\omega_0 t + \frac{2}{3}\pi\right) + \beta \cos\left(\omega_0 t + \frac{2}{3}\pi\right)\right] \right. \\ + \left[\alpha \sin\left(\omega_0 t + \frac{2}{3}\pi\right) \right. \\ \left. \left. + \alpha\beta \sin\left(\omega_0 t + \frac{2}{3}\pi\right)\right]\right] \\ i_{oc} \approx I_p \left[\left[\sin\left(\omega_0 t - \frac{2}{3}\pi\right) - \beta \cos\left(\omega_0 t - \frac{2}{3}\pi\right)\right] \right. \\ - \left[\alpha \sin\left(\omega_0 t - \frac{2}{3}\pi\right) \right. \\ \left. \left. - \alpha\beta \sin\left(\omega_0 t - \frac{2}{3}\pi\right)\right]\right] \end{aligned}$$

In this case, the neutral current can be expressed as:

$$\begin{aligned} i_n = I_p \sqrt{\left(\sqrt{3}\beta\right)^2 + \left(\sqrt{3}\alpha - \alpha\beta\right)^2} \sin\left(\omega_0 t \right. \\ \left. + \tan^{-1}\left(\frac{\sqrt{3}\alpha - \alpha\beta}{\sqrt{3}\beta}\right)\right) \end{aligned} \tag{14}$$

Next, the dynamic model of the converter voltage ripple is developed. For small signals, V_{dc} can be considered as a short circuit, so the upper- and lower-arm capacitors can be equivalently combined $(C_{tol} = C_{dc\_high} + C_{dc\_low})$, as shown in Fig. 4.

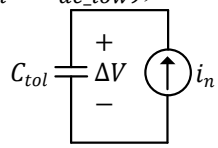

Fig. 4 Small-signal equivalent model of upper- and lower-arm capacitor voltage

where the dc-bus variation ΔV_{bus} can be expressed as :

$$\Delta V_{bus} = \int i_n \, dt + i_n(t_0) \tag{15}$$

From the derivation of (14) and (15), it can be seen that with the unbalanced phase and amplitude of the three-phase load, a non-zero neutral line current is generated, which in turn generates the ripple of the upper and lower arm dc-bus capacitor voltage. According to (10), when the three-phase load is balanced, i_n is close to "0", and the amplitude of the voltage ripple is very small. When the three-phase load is unbalanced, according to the derived neutral line current (14), i_n will cause voltage ripple. Therefore, when designing the d bus capacitor, the amplitude and phase imbalance coefficients in (14) should be taken into account in the design. Then, by substituting (14) into (15), the amplitude of the derived capacitor voltage ripple can be expressed as:

$$\Delta V_{bus} = \frac{I_p}{C_{bus}\omega_0} \sqrt{\left(\sqrt{3}\beta\right)^2 + \left(\sqrt{3}\alpha - \alpha\beta\right)^2} \tag{16}$$

Then, we design the inductance value, calculate the charge flowing through the capacitor according to the capacitance equation, and then calculate the capacitor voltage ripple of the voltage balancing circuit. In the steady state, the duty is 1/2, so the voltage ripple can be expressed as:

$$C_{bus}\Delta V_{bus} = \frac{1}{2}\cdot\frac{\Delta I_{L\_bal}}{2}\cdot\frac{T_s}{2} \tag{17}$$

The current variation of the balanced-circuit inductor ΔI_{L_bal} can be expressed as:

$$\Delta I_{L\_bal} = \frac{V_{dc}T_s}{4L_{bal}} \tag{18}$$

Substituting (18) into (17), the relationship of inductance, capacitance, and voltage ripple can be derived as:

$$L_{bal} = \frac{V_{dc}T_s^2}{32C_{bus}\Delta V_{bus}} \tag{19}$$

Next, we show the balancing circuit design. According to (18) and (19), the inductance and capacitance of the balancing circuit are highly dependent on the switching frequency and dc-bus voltage. Therefore, when designing the parameters, the required system parameters must be taken into account to ensure that the system meets the relevant electrical specifications.

$$C_{tol,min} > \frac{I_p}{\Delta V_{bus}\omega_0}\sqrt{\left(\sqrt{3}\beta\right)^2 + \left(\sqrt{3}\alpha - \alpha\beta\right)^2} \tag{20}$$

$$L_{bal,min} = Max\left\{\frac{V_{dc}T_s^2}{32C_{bus}\Delta V_{bus}}, \frac{V_{dc}T_s}{4\Delta I_{L_{bal}}}\right\} \tag{21}$$

IV. Design and Simulation Results

The balancing circuit parameters and are designed and simulation results are presented to validate the proposed control method. The system parameters are listed in Table 1. Followed by the phase and amplitude mismatch of the load current, the following results show a 10% mismatch of the upper- and lower-arm capacitor.

TABLE I
SYSTEM CONFIGURATION

Parameter	Value
DC bus voltage (V_{dc_high})	390 V
DC bus capacitor (C_{dc_high}, C_{dc_low})	200 μF
balance Inductance (L_{bal})	400 μH
Switching frequency (f_{sw})	50 kHz

Fig. 5 shows the mismatch between the upper- and lower-arm capacitors, the phase and amplitude imbalance coefficients defined in **Error! Reference source not found.**) with α and β set to 0. From the simulation results, the average values of the upper- and lower-arm capacitor voltages are 384.45 V and 376.12 V, respectively. Before compensation and after compensation, the average values of the upper- and lower-arm capacitor voltages are 380.55 V and 380.45 V, respectively.

Fig. 6 shows the load imbalance with α and β set to 0 and π/3, respectively, and the simulated results show that before compensation, the upper- and lower-arm capacitor voltages contain a sine wave component with an amplitude of 100.11 V. After compensation, the average values of the upper and lower arm capacitor voltages are 379.61 V and 381.69 V, respectively, with almost no ac component.

Fig. 7 shows the phase imbalance with α and β set to 0.2 and 0. The simulation results show that before compensation, the upper- and lower-arm capacitor voltages contain a sine wave component with the amplitude of 35.62 V. After compensation, the average values of the upper- and lower-arm capacitor voltages are 379.61 V and 381.69 V, respectively, and there is almost no ac component.

Finally, Fig. 8 shows the unbalanced phase and amplitude with α and β set to 0.2 and π/3, respectively, and the simulated results show that before compensation, the upper- and lower-arm capacitor voltages contain a sine wave component with the amplitude of 36.75 V. After compensation, the average values of the upper and lower arm capacitor voltages are 379.61 V and 381.69 V, respectively, with almost no ac component.

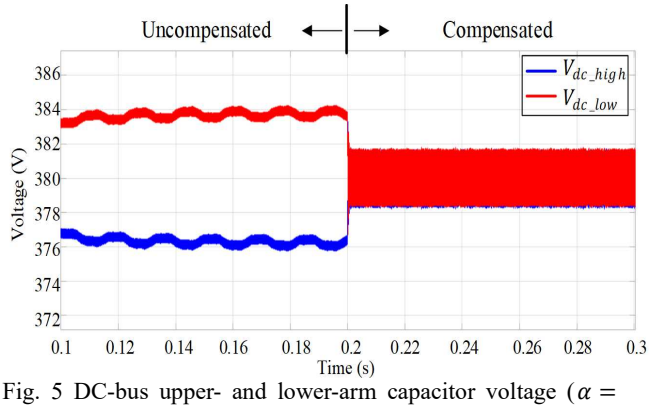

Fig. 5 DC-bus upper- and lower-arm capacitor voltage ($\alpha = 0, \beta = 0$)

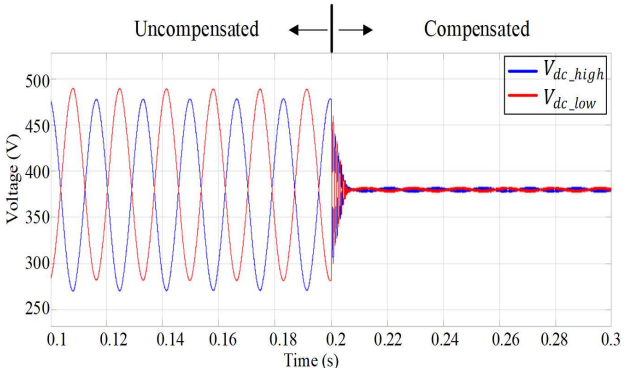

Fig. 6 DC-bus upper- and lower-arm capacitance voltage ($\alpha = 0, \beta = \pi/3$)

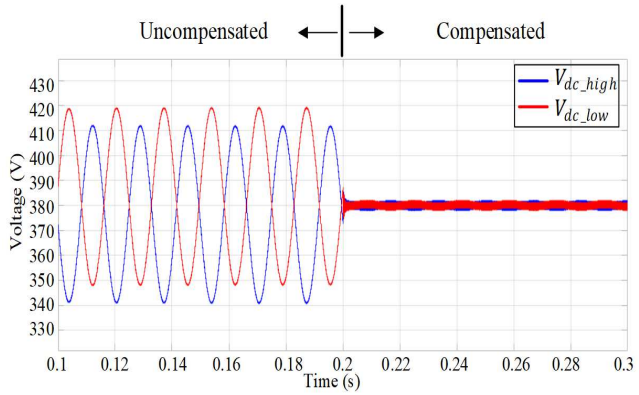

Fig. 7 DC-bus upper- and lower-arm capacitor voltage ($\alpha = 0.2, \beta = 0$)

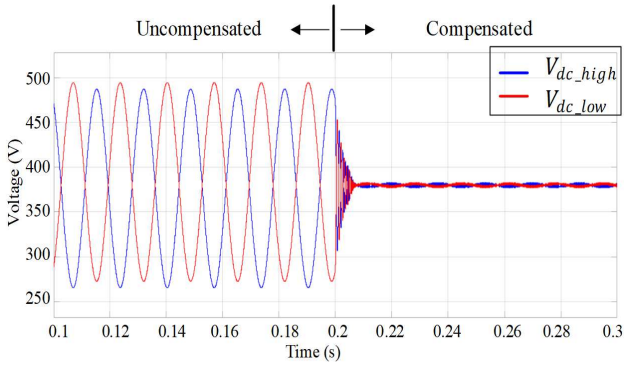

Fig. 8 DC-bus upper- and lower-arm capacitor voltage ($\alpha = 0.2, \beta = \pi/3$)

CONCLUSION

This paper presents a neutral-point voltage balancer for a three-phase four-wire converter. A half-bridge is used as the power stage architecture for the balanced circuit and a DΣ control method is used to derive the appropriate control dynamic model. This control method can be intuitively derived from the excitation and demagnetization currents of the inductor, which greatly simplifies the complexity. Voltage imbalance is a major drawback in the application of split capacitors. This paper mentions some of the conditions of voltage imbalance and suggests ways to improve them. Generally speaking, the capacitance values of the upper and lower arms differ due to the manufacturing process, resulting in the difference of the dc component of the upper- and lower-arm capacitor voltages. Then, due to the phase or amplitude imbalance of the three-phase load current, a non-zero current exists in the neutral line, resulting in an ac component voltage ripple. In converter applications, the upper- and lower-arm capacitors must be balanced to generate symmetrical voltages, so voltage balancing is an important issue. This paper proposes a voltage balancing circuit control method based on the DΣ control to balance the upper- and lower-arm capacitor voltages. The proposed control method incorporates the neutral current into the calculation to ensure that the upper- and lower-arm capacitor voltages can be regulated even when the three-phase load is unbalanced.

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