

# A Ripple Suppression Method Based Differential Spilt Capacitors for Two-stage Single-phase Inverter

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**Abstract--** This paper proposes an advanced ripple suppression scheme by controlling the bus voltage complementary with the dual active bridge (DAB) converters under extended phase shift (EPS) control without uncontrollable intervals. The existing differentiated capacitance design is based on the DAB converter under single phase shift (SPS) control, which has a limitation in parameter optimization. Meanwhile, to minimize the current stress of the DAB converters, an optimization method is designed, which considers the fluctuation of output voltage for accurate parameter selection. At the same time, this method achieves zero voltage soft (ZVS) in the DAB converters. The input-parallel output-series (IPOS) structure is adopted as the main circuit. Simulation results are provided to verify the effectiveness of the proposed scheme.

**Index Terms**--DAB converter; Differential split capacitance; Single-phase inverter; EPS

## I. INTRODUCTION

With the "double carbon target" proposed, the new energy industry is developing rapidly, in which two-stage single-phase inverters have been widely used. However, the inherent low-frequency ripple can cause harm to the pre-converter and DC power supply, reduce the power generation efficiency and increase the cost.

To address this issue, currently, there are several measures have been proposed to decrease low-frequency ripple. For the passive method, a bulk dc bus capacitor is applied to absorb the power, bringing huge size and high cost [1]-[2]. The second is to add additional topology to offset the current ripple. A bidirectional converter is used to provide current to the bus voltage port to compensate for the second harmonic. This scheme can reduce the capacitance of the capacitor by increasing the voltage fluctuation, therefore film capacitors can be used instead of electrolytic capacitors to reduce the risk to the equipment life [3]. Bidirectional converters provide compensating currents, so they can also be called Second Harmonic Current Compensator (SHCC). Large voltage fluctuations can affect the effectiveness of the second harmonic compensation and the SHCC needs to be controlled to accurately compensate for the harmonic current. According to the topology of the compensator, Buck bidirectional converter, Boost bidirectional converter, and Buck-Boost bidirectional converter can be used for SHCC. The literature [4] uses hysteresis loop control in the SHCC to output the compensation current, but the switching frequency is constantly switched, which is not conducive to the optimization of the circuit

parameters; the literature [5] calculates the duty cycle in real time to precisely control the SHCC to generate the compensation current, but at this time the SHCC works in intermittent mode and the current stress of the switching tubes is large, which generates large conduction losses.

The third method is to optimize the pre-stage DC/DC converter's control strategy. The differential power is provided by the bus capacitor. The literature [14] proposes that the output current of the pre-converter can be controlled by real-time adjustment of the shift ratio of the pre-converter DC/DC converter to precisely control the bus capacitor voltage to make it provide differential power. The voltage loop cutoff frequency is low to avoid the interaction between the modulated signals when the load jumps can cause large voltage fluctuations on the bus. The literature [7] proposes to effectively suppress the ripple in the pre-converter by introducing an inductive current inner loop and lowering the voltage outer loop cutoff frequency, which is still provided by the bus capacitor. Similarly, when the load jumps, a lower outer voltage loop results in larger waveform distortion or increased current stress.

Literature [8] proposes to use of bus differential split capacitors to provide ripple power and control the complementary differential split capacitor voltage ripple, due to the limited control freedom, which has a poor role in reducing the current stress. To address the issues, several techniques have been proposed. The Lagrange multiplier method and Karush-Kuhn-Tucker (KKT) conditions have been applied to get optimal organization under dual-phase-shift (DPS) modulation. Literature [9] introduced an image analysis method to get optimal organization for current stress minimum while achieving ZVS and full-cycle controllability by switching the DAB converter operating in different states. In this paper, the image analysis method is proposed to find optimal parameters organization due to the multiple work states of the DAB converter under EPS control.

## II. TECHNICAL WORK PREPARATION

The main circuit topology of a two-stage single-phase inverter is given in Fig.1.

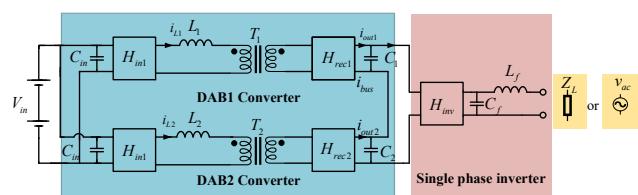


Fig. 1. Circuit topology of two-stage dual active bridge single-phase inverter.

The main function of the post-stage inverter is to convert the DC output voltage into AC power for the load, or into AC power with the same frequency and phase as the grid voltage to connect to the grid. Currently, there are two main types of single-phase inverters: half-bridge inverters and full-bridge inverters. When the input voltage on the DC side is the same, the output voltage of the half-bridge circuit is only half of the output voltage of the full-bridge inverter circuit, which means that the voltage utilization rate of the half-bridge circuit is lower; and under the same power conditions, the current of the half-bridge inverter circuit is twice that of the full-bridge inverter circuit, which increases the requirement for the current resistance level of the switching tubes. Therefore, after a comprehensive comparison, the full-bridge inverter circuit is selected for the inverter part.

In this paper, the DAB converters are controlled by EPS modulation. There is an inner phase shift  $D_1$  and an outer phase shift  $D_2$ . According to the relative sizes of  $D_1$  and  $D_2$ , the circuit has two operating states: when  $0 \leq D_1 \leq D_2 \leq 1$ , the converter works in state a; when  $0 \leq D_2 \leq D_1 \leq 1$ , the converter works in state b. The main operating waveforms of the DAB converter under EPS control are shown in Figure 2.  $i_L$  is the inductor's current and  $T_{hs}$  is half of a switching cycle.  $S_1 \sim S_8$  are the driving signals of the corresponding switching tubes. Comparing the two figures, it can be found that the DAB converter has two operating states according to the relative sizes of  $D_1$  and  $D_2$ , which finally affects the output characteristics of the converter.

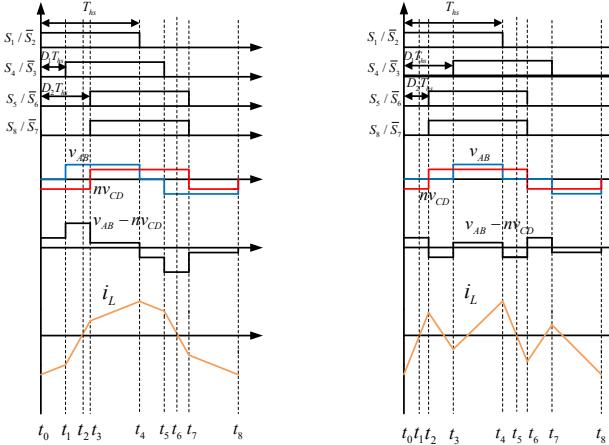


Fig. 2. Operating waveform of DAB converter.

The output power characteristics under EPS control are of the following forms:

$$P_a = \frac{V_{in} V_{out}}{4 L f_{hs}} \left[ (2D_2 - D_1) - (D_1^2 + 2D_2^2) + 2D_1 D_2 \right] \quad (1)$$

$$P_b = \frac{V_{in} V_{out}}{4 L f_{hs}} \left[ 2D_2 + D_1^2 - 2D_1 D_2 - D_1 \right] \quad (2)$$

The maximum output power will account for the

standardization of the formula to get the output power characteristics. From Figure 3, it can be seen that when the circuit is operating in state a, the converter transmits the power in the range [0,1], i.e., the circuit can transmit forward power. Also, there are various combinations of shifts compared to the same output power. When the circuit works in state b, the output power range of the converter is [-0.5,0.5], i.e., the converter can transmit reverse power in addition to forward power, but the transmitted power is only half of the maximum transmitted power at this time. The transmitted power characteristic of EPS modulation provides the possibility to achieve differential capacitive ripple suppression.

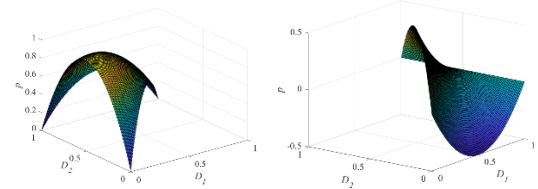


Fig. 3. Transmission power of DAB converter under EPS control.

The DAB converter can be controlled with two shifts to get the target current as described above. In this scheme,  $D_1$  is a fixed value and  $D_2$  is controllable in real-time.

### III. RIPPLE SUPPRESSION SCHEME

#### A. Traditional Ripple Suppression Scheme

In the traditional ripple suppression method, both DAB converters use single phase shift modulation, and their parameters are exactly equal  $C_1 = C_2$ , at this time the two capacitor voltages have equal two-frequency components, and the same frequency and phase, and the two superimposed on the bus voltage have large two-frequency ripple fluctuations, as shown in Figure 4. From the physical point of view, when the output power before the inverter is greater than the output power of the previous converter, the capacitor voltage releases energy to compensate for the difference in power, and the capacitor voltage drops; when the output power before the inverter is less than the output power of the previous converter, the capacitor voltage absorbs energy to dissipate the difference in power, and the capacitor voltage rises. Since the parameters of the DAB converter and shift are exactly equal compared with the bus capacitor, the compensated differential power is equally distributed on the two bus capacitors, and the capacitor voltage changes synchronously, which makes the bus voltage fluctuate more after superposition and the ripple suppression effect is insufficient.

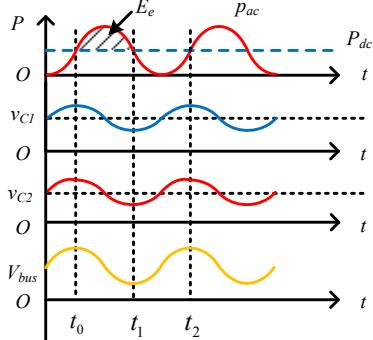


Fig. 4. Operating waveform of the traditional ripple suppression scheme.

According to Kirchhoff's current law (KCL) in the DAB1 circuit, we can get

$$i_{out1} = i_{bus} + i_{C1} \quad (3)$$

Obviously, the DAB converter only generates the DC component, and the diabatic energy is provided by the capacitors, making the same diabatic ripple on both capacitor voltages and a larger voltage ripple on the bus.

The capacitor current is solved as follows:

$$i_C = C \frac{dv_C}{dt} = -\frac{1}{2} MI_o \cos(2\omega t - \theta) \quad (4)$$

Where  $M = V_o/V_{bus}$ , is the regulating system of the post-stage single-phase inverter.

This leads to the capacitor voltage as well as the bus voltage.

$$v_{bus} = V_{bus} + v_{C1} = V_{bus} + \frac{V_o I_o}{4V_{bus} \omega C} \sin(2\omega t - \theta) \quad (5)$$

There is a dipole ripple in the bus voltage, whose amplitude is related to the regulating system of the inverter, the output current, the output frequency of the AC side, and the capacitance of the bus capacitor.

The bus voltage ripple content is as follows.

$$\frac{v_{C1}}{V_{bus}} = \frac{V_o I_o}{4V_{bus}^2 \omega C_1} \quad (6)$$

From the above equation, it is clear that harmonics in a two-stage single-phase inverter can be suppressed by increasing the bus capacitance to reduce the bus voltage ripple content. Since increasing the capacitance leads to an increase in the size and cost of the device and has a limited suppression effect, a more effective method is needed.

### B. Differential Split Capacitor Ripple Suppression Scheme

In this scheme, the differential power inherent in the two-stage single-phase inverter is provided by the bus capacitors  $C_1$  and  $C_2$ , but the two bus capacitors have different capacitance compared to the conventional scheme. The general idea is to keep the bus capacitor voltages  $v_{C1}$  and  $v_{C2}$  ripple complementary to reduce the bus ripple significantly.

For the two-stage single-phase inverter, the operating waveform in the differential split capacitors ripple suppression scheme is shown in Fig.5.

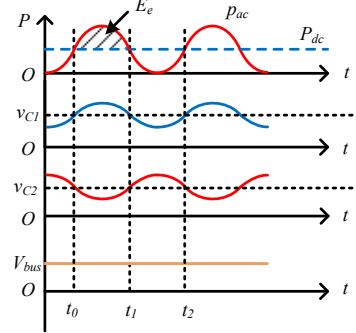


Fig. 5. Operating waveform of the differential split capacitors ripple suppression scheme.

In terms of physical mechanism, controlling the ripple complementarity of capacitor voltages requires precise control of the charging and discharging charges on the capacitors to ensure that the voltages of the two capacitors change to complementary states. According to KCL, for the IPOS structure of the DAB converter, the structure and parameters of the two modules are the same, and to generate ripple complementary capacitor voltages, it is necessary to control the shift compared to the two DAB converters separately to generate the appropriate charging and discharging currents to achieve the precise deployment of charges.

According to the law of energy conservation and ripple complementarity, the bus capacitors' characteristics are given by

$$\begin{cases} v_{C1} = \frac{V_{bus}}{2} - \Delta v \\ v_{C2} = \frac{V_{bus}}{2} + \Delta v \end{cases} \quad (7)$$

$$P_{C1} + P_{C2} = P_e \quad (8)$$

Where  $\Delta v$  is the ripple of the bus capacitors.

According to KCL, the target currents of the pre-stage circuit can be obtained by associating the above equations, which can precisely control the bus split capacitor charging and discharging, thus making the ripple of two split capacitors' voltage complementary and achieving the effect of bus ripple suppression.

$$\begin{aligned} i_{out1} &= i_{C1} + i_{bus} \\ &= \frac{1}{2} MI_o (\cos \theta + \cos(2\omega t - \theta)) \frac{C_1 + C_2}{C_1 - C_2} \end{aligned} \quad (9)$$

$$\begin{aligned} i_{out2} &= i_{C2} + i_{bus} \\ &= \frac{1}{2} MI_o (\cos \theta + \cos(2\omega t - \theta)) \frac{C_1 + C_2}{C_2 - C_1} \end{aligned} \quad (10)$$

## IV. OPTIMIZATION SCHEME OF THE MAIN CIRCUIT

### A. Full-cycle Controllable Analysis

According to the characteristics of EPS modulation, full-cycle control can be achieved by optimizing

parameters. The constraint for the DAB converter operating in state a is  $0 \leq D_1 \leq D_2 \leq 1$  and in state b is  $0 \leq D_2 \leq D_1 \leq 1$ .

There are two shifts in the DAB converter, the change range is  $0 \leq D_1 \leq 1$ ,  $0 \leq D_2 \leq 1$ , and the value of  $D_1$  should be selected between  $[0,1]$ , but  $D_1$  in a certain range,  $D_2$  would be beyond the range of the interval, at this time the output current of the DAB converter is a constant maximum output current, lost the regulation of the bus split capacitor voltage, that is, there is an uncontrollable interval of the DAB converter. To achieve accurate regulation of the bus capacitor voltage, the DAB converter should be full-cycle controllable. According to the above analysis, the realization of full-cycle controllability is related to the selection of shift  $D_1$  in the DAB converter. The controllable interval of DAB1 is analyzed below, and the controllable interval of DAB2 is analyzed in a similar way to that of DAB1, which is not repeated here.

When DAB1 works in state a, to make DAB1 in full-cycle controllable, the constraint is  $0 \leq D_1 \leq D_2 \leq 1$ .

When DAB1 operates in state b, to make DAB1 in full-cycle controllable, the constraints are discussed as follows. For a DAB circuit operating in state b, the transmitted power range is  $[-0.5, 0.5]$ . This scheme requires that the output current be negative when the circuit operates in state b. Then, let  $i_{out} \leq 0$ , and get the constraint  $D_2 \leq D_1/2$ , and another constraint  $0 \leq D_2 \leq D_1 \leq 1$  combined calculation can be obtained as follows

$$0 \leq 2D_2 \leq D_1 \leq 1 \quad (11)$$

Solving the above equation gives  $D_{1a}=0$ .

In the working conditions in this paper, the range of values of  $D_{1b}$  can be solved as  $[0.018, 0.982]$ .

### B. Zero Voltage Switching Analysis

Since the DAB converter operates at a high frequency, it generates large switching losses and greatly impacts the output power. The high-frequency switching also generates ripple and high-frequency noise at the same frequency, which makes the bus voltage fluctuates greatly. To reduce the impact of high-frequency switching on the transmitted power, it is necessary to make each switch as far as possible to achieve zero-voltage switch (ZVS). When the switch is triggered, if the diode in anti-parallel with it is already on, the voltage added to the switch has been clamped to zero, it can be considered that the switch has achieved ZVS. According to the above analysis, the conditions of ZVS can be discussed separately for DAB converters under EPS control in different operating states.

$$\begin{cases} i_L(t_1) \leq 0 \\ i_L(t_3) \geq 0 \end{cases} \quad (12)$$

Finally, we can get the following limitations.

$$\begin{cases} D_2 \geq \frac{(K+2)D_1 + 1 - K}{2} \\ D_2 \geq \frac{KD_1 - 1 + K}{2K} \end{cases} \quad (13)$$

Similar to the above analysis, and combined with the characteristics of the variation of the inductor current in one cycle, the conditions for the DAB circuit to operate in state b to achieve ZVS for all switching tubes can be obtained as

$$\begin{cases} i_L(t_1) \geq 0 \\ i_L(t_3) \leq 0 \end{cases} \quad (14)$$

Similarly, we can get the limitations when the DAB converter works in state b.

$$\begin{cases} D_1 \geq \frac{K-1}{K} \\ D_2 \leq \frac{2D_1 - 1 + K - KD_1}{2K} \end{cases} \quad (15)$$

In this scheme, taking  $K=1$ , the ZVS condition is

$$\begin{cases} D_2 \geq \frac{3D_1}{2} & 0 \leq D_1 \leq D_2 \leq 1 \\ D_2 \leq \frac{D_1}{2} & 0 \leq D_2 \leq D_1 \leq 1 \end{cases} \quad (16)$$

### C. Current Stress Minimization Analysis

To achieve efficient transmission and avoid damage to the motor devices, the current stress optimization strategy is proposed to reduce current stress while satisfying the target current.

First, the inductor has the following constraints from the controllable interval analysis and ZVS analysis above.

$$\begin{cases} L \leq \frac{T_{hs}V_{in}}{4MI_o(\cos\theta + \frac{1+\alpha}{1-\alpha})} \\ L \leq \frac{T_{hs}V_{in}}{8MI_o(\frac{1+\alpha}{1-\alpha} - \cos\theta)} \\ L \leq \frac{T_{hs}V_{in}}{8MI_o(\cos\theta + \frac{1+\alpha}{1-\alpha})} \end{cases} \quad (17)$$

When the variation of capacitors voltage is under consideration, the current stress of the DAB converter is of the following forms:

Calculate the maximum value of current stress in a

second harmonic period. Since the expressions for the current in the DAB converter are different in different operating states, the current values need to be calculated separately as

$$i_{L\_b} = \max \left\{ \frac{nV_{out}}{4f_s L} (2D_2 - D_1), \frac{nV_{out} D_1}{4f_s L} \right\} \quad (18)$$

$$i_{L\_a} = \frac{nV_{out}}{4f_s L} [K(1-D_1) + (2D_2 - 1)] \quad (19)$$

According to the above analysis and calculation, the calculated expressions for the current stress when the DAB converter is operated in different operating states are different. We need to minimize the current stress, i.e., find out the maximum value of current stress and then minimize it. Observing the above equation, it can be found that the current stress at state a is related to the inductance and capacitance ratio, and the current stress at state b is related to the shift ratio  $D_{lb}$ , inductance and capacitance ratio. For this reason, the curves of current stress in different states of the DAB converter operation are plotted in the three-dimensional coordinate system. The x-axis and y-axis are the inductance and capacitance ratios, respectively, and the red surface is the current stress in the state a. The other surfaces are the current stresses corresponding to different shifts compared to  $D_{lb}$  in state b. In this case, the intersection of the current curves of state a and state b is the maximum current stress corresponding to different  $D_{lb}$ , and the minimum value point exists, which corresponds to the best inductance and  $D_{lb}$ , thus minimizing the current stress.

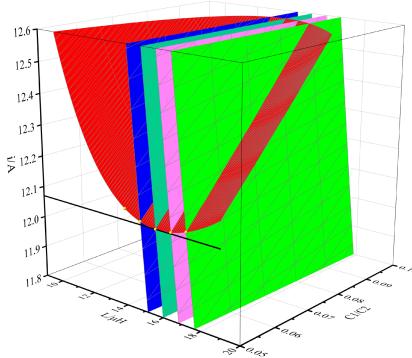


Fig. 6. Current Stress at 2 kW with Varied Inductance and Capacitance Ratio.

To verify the feasibility and effectiveness of the proposed strategy, a 2kW system simulation model is built in PLECS. The main parameters are shown in Table I.

TABLE I  
SIMULATION DESIGN PARAMETERS

Parameter	Value
$V_{dc}$	200V
$f_s$	50kHz
$n:1$	1:1

C	2000μF
$V_{bus}$	400V
$V_{out}$	311V
$f_{out}$	50Hz
$p_e$	2kW
$C_1/C_2$	1/9
$L_f$	15μH

In the conventional low-frequency ripple suppression scheme, the capacitance of the two capacitors on the bus is the same, i.e.,  $C_1=C_2=1000\mu F$ , and the parameters of the two DAB converters are the same, with the equivalent inductance  $L$  being  $45\mu H$ . The simulation results yield the bus voltage, capacitor voltage waveforms, and inverter output voltage waveforms as shown in Figure 7 below, which shows that the two capacitor voltages are the same, and the bus voltage fluctuates significantly after superposition. The peak value of the bus voltage is 31.99V, and the ripple content is 4%. The inverter output voltage waveform is distorted and the measured THD=4.08%.

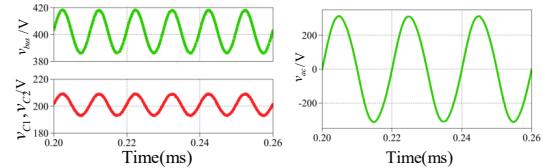


Fig. 7. Bus operating waveform of the conventional ripple suppression scheme.

The bus voltage and split capacitor voltage waveforms are shown in Figure 8. It can be seen that  $v_{c1}$  and  $v_{c2}$  waveforms are complementary, the DC bus voltage is stable, the peak value of the bus split capacitor voltage is 19.7V, and the peak value of the bus voltage differential ripple is 1.02V, with a ripple content of 0.13%. The output voltage of the inverter side is shown below, and there is no obvious distortion in the waveform, and the measured THD=0.066%.

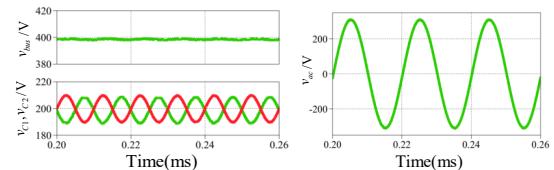


Fig. 8. Bus operating waveform of the differential split capacitor ripple suppression scheme.

The table II compares the simulation results of the traditional low-frequency ripple suppression scheme and the differential split capacitor ripple suppression scheme. The results show that by using the differential split capacitor ripple suppression scheme based on EPS modulation, the bus voltage ripple is significantly reduced, the bus ripple content is significantly reduced, the AC measurement output power quality is greatly increased, and the ripple suppression effect is obvious.

TABLE II  
COMPARISON OF SIMULATION RESULTS

Parameter	The scheme in this paper	Traditional Solution	Effects
Bus voltage ripple content	0.13%	4%	Reduced by 96.75%
Inverter output voltage distortion rate	0.066%	4.08%	Reduced by 98.38%

The table III compares the simulation results of the ripple suppression scheme under SPS control and the scheme in this paper. It is obvious that the current stress is significantly reduced in this scheme.

TABLE III  
COMPARISON OF SIMULATION RESULTS

Parameter	The scheme in this paper	SPS Solution	Effects
Current stress/A	13.0749	24.1559	Reduced by 45.87%

## V. CONCLUSIONS

A two-stage single-phase inverter with ripple elimination on the dc side is proposed. Voltage-complementary control and characteristics of DAB under EPS control have been analyzed to achieve ripple suppression. Mathematical analysis has been carried out to achieve current stress minimization. Simulation results demonstrate that the proposed scheme is effective in ripple suppression and current stress reduction.

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