Analysis and Implementation of Effective Placement of EMC Capacitors for WBG Modules

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July 11, 2022

Keywords

≪Common mode choke (CMC)≫, ≪Displacement current≫, ≪Electromagnetic capability (EMC)≫, ≪Wide band-gap (WBG)≫

Abstract

This paper proposes an optimum placement of the electromagnetic capability (EMC) capacitors for the wide band-gap (WBG) devices (SiC). To minimize electromagnetic interference (EMI), the solution of using EMC capacitors near the power module is proposed. Two different EMC capacitor placement scenarios are examined to show how the displacement current is affected. The suggested method reduces the capacitive displacement current during the high slew rate of the drain-source voltage (dv/dt), which then helps to minimize the size and overall cost of the common mode choke (CMC). The proposed methods are simple to construct and easy to implement with a faster switching response. The proposed method is experimentally implemented for a half-bridge SiC power module with the heat sink.

Introduction

The common-mode (CM) EMI noise is introduced due to the parasitic capacitance between high dv/dt nodes and the ground in the power electronic system. The CM current is generated because of the charging and discharging of the parasitic capacitance. The heat generated from the conduction power loss is dissipated to the air via heat sinks. The power module terminals and the heat sinks have introduced the large parasitic capacitance, which plays a key role in EMI filter design. The larger parasitic capacitance leads to the higher displacement current between the high dv/dt nodes and the heat sink. For safety reasons, the heat sinks are connected directly to the ground and cannot be reached from the outside and most of the noise current can flow directly back to the circuits. The goal of minimizing the capacitive displacement current is to reduce the overall size, volume, and cost of the EMI filters and increase the power density according to the standards and keep a higher switching speed. In [1], the authors propose two methods of generating the negative capacitance to cancel the parasitic capacitance, which is based on the mutual capacitance theory and the second one is the mutual inductance. The separated heat sinks combined with the damping snubbers are used in [2] to improve both CM and differential mode (DM) conducted for the EMI/EMC performance for a SiC JFET-based inverter. A CM quantitative model is proposed in [3], to identify the simpler and alternative method to attenuate the baseplate current in the system, which involves placing a single capacitor between the neutral point and the system ground near the module baseplate. This method significantly reduces the CM current through the module baseplate as expected by the module [3].

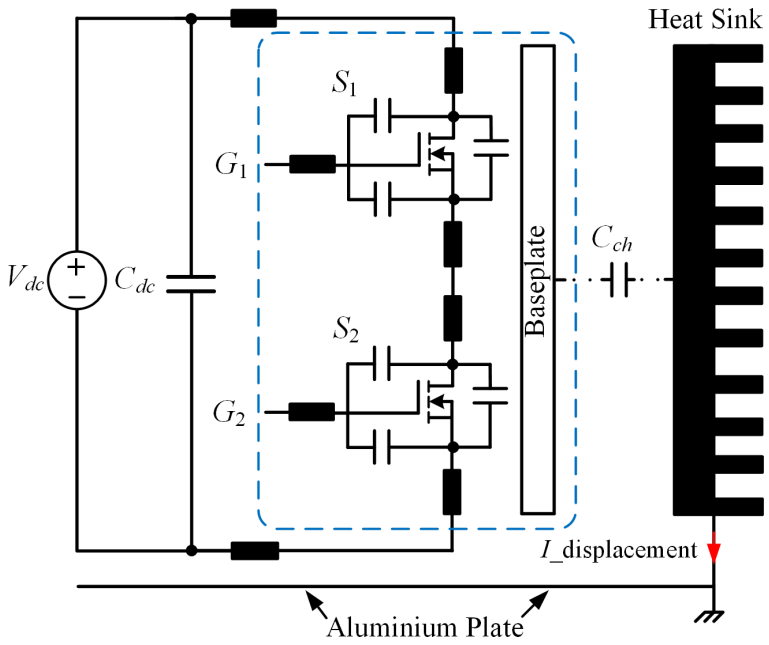


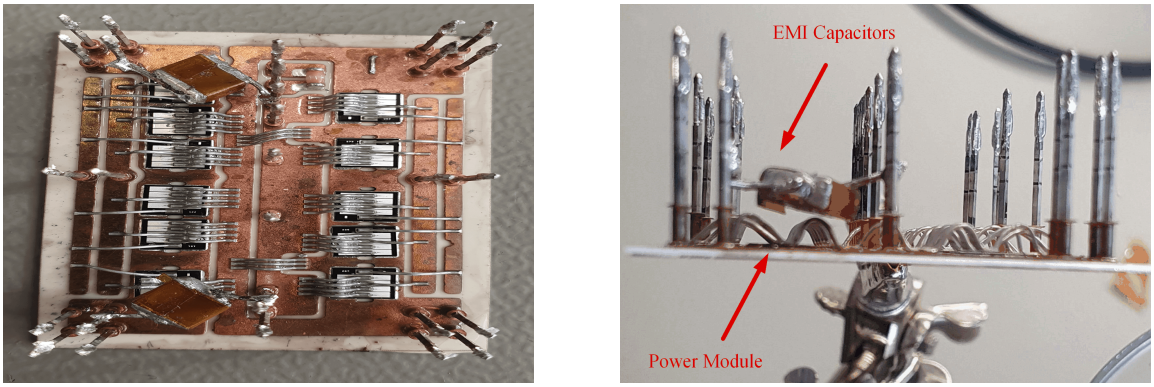
Fig. 1: The equivalent configuration of the H-bridge SiC Module with the parasitic components and the heat sink

A model-based approach is proposed in [4] to identify the effect of the anti-resonance formed by the AC-side of the baseplate capacitance of the power modules and the inductive load. This technique results in low inductance and low capacitance filters where the low capacitance can be beneficial for the ungrounded systems to minimize the line-to-ground capacitance [4]. An extra output filter stage is implemented to reduce the leakage current proposed in [5, 6]. Two complex modulations are proposed to mitigate the common-mode leakage current for a three-phase inverter as reported by [7, 8]. The conducted CM EMI emission of a pulse width modulation inverter-based motor drive investigates and quantifies the increase in [9]. The numerical predictions are used in [10] to generate a set of design guidelines for heat sinks of various sizes and emphasized that changing heat-sink gasket materials as an EMI mitigation strategy is limited to cases in which the heat-sink patch resonance constitutes a significant part of the overall coupling mechanism. The impacts of the printed circuit board (PCB) [11] and system layouts, such as shielded cables and unshielded cables on CM EMI noise of SiC electric vehicle powertrains are introduced in [12, 13].

This paper proposes the effective placement, implementation, and analysis of the EMC capacitors inside the power module. Moreover, a pair of two capacitors in parallel are implemented outside the power module between the DC+/DC- power module terminals with the heat sink. A comparative analysis is presented to reduce the displacement current between the parasitic capacitance of the high dv/dt nodes and the heat sink for the above-mentioned approach.

Minimization of the capacitive displacement current

Fig. 1 illustrates the equivalent circuit configuration of the parasitic capacitance and stray inductance of the half-bridge power module with the heat sink. Fig. 1 shows the typical configuration of the H-bridge where parasitic capacitance C_{dh} is between the heat sink and the power module baseplate and C_{gh} is between the heat sink and the ground. Moreover, the parasitic capacitance C1 is between DC+ terminal and ground, C2 is AC terminal, and ground where C3 is between DC- and ground. The combination of these parasitic capacitance results in a path for the flow of the displacement current. This coupling path has a strong influence on generating the EMI emission during the switching of the power electronic devices. The displacement current needs to be minimized, keeping the high dv/dt, which then helps in smaller switching loss and results in smaller filter sizes with higher power density. Two methods have been proposed to reduce the displacement current. The first method is the placement of the two



(a) (b)

Fig. 2: EMI capacitors; (a) inside the power module, (b) inside the power module with the smallest space to the chips

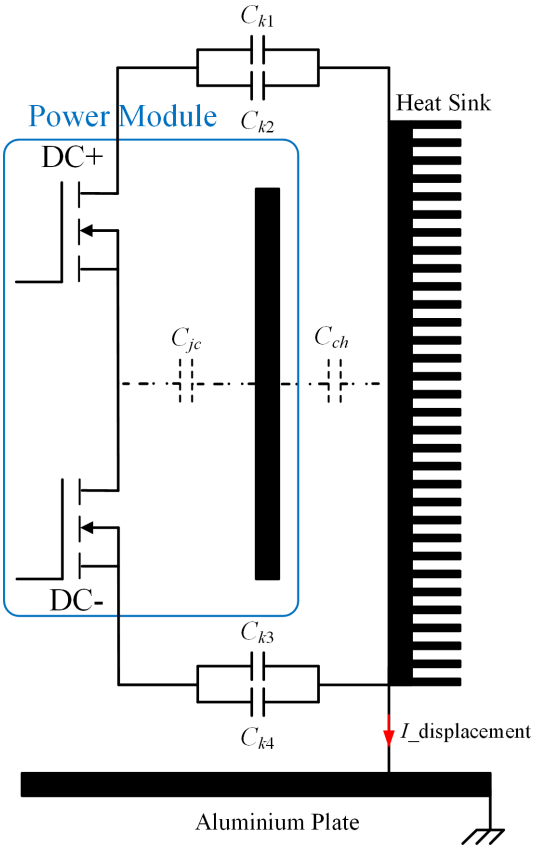


Fig. 3: Placement of two capacitors of 100nF in parallel between the DC+/DC- and heat sink

capacitors of 100nF between DC+ and DC-.

Fig. 2 depicts the experimental implementation of the placement of the capacitors inside the power module. It can be seen that the capacitors are in full contact with the power module with negligible space between them. The goal is to reduce the stray inductance as small as possible and the effect is analyzed on the displacement current. The second method depicted in Fig. 3 is the placement of two capacitors of 100nF in parallel between the DC+/DC- and heat sink. Fig. 4 shows the experimental implementation of the proposed approach. The objective is to create two loops for the displacement current between the DC+/DC- and the heat sink. This approach results in the reduced flow of the displacement current through the heat sink and the ground and forces the displacement current to flow in two loops. This method helps in attenuating the displacement current.

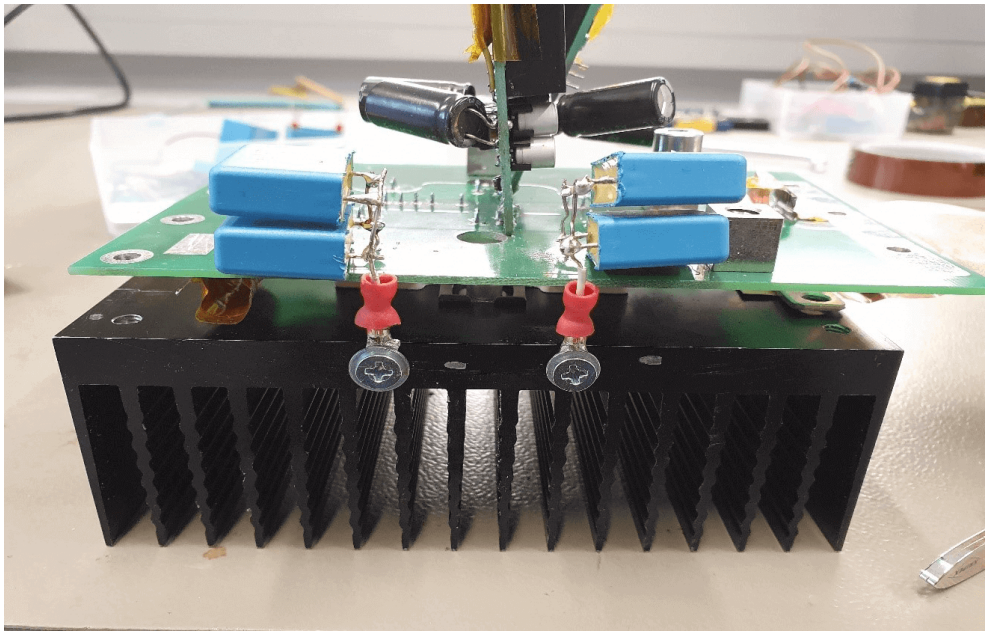
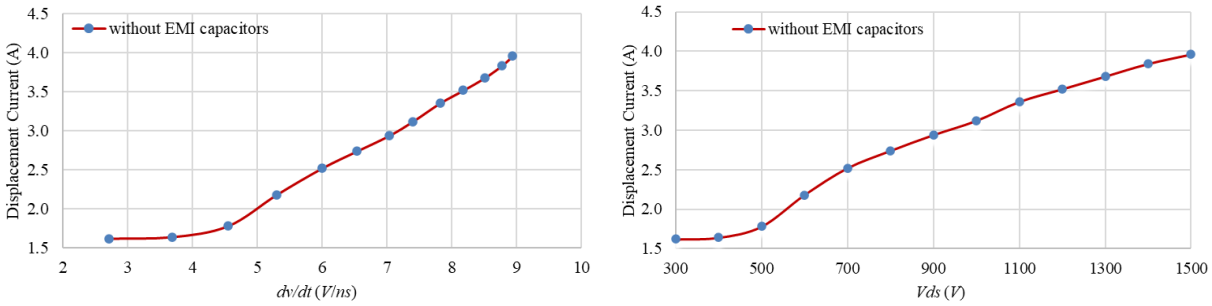


Fig. 4: The placement of the EMI capacitors outside the power module



(a) (b)

Fig. 5: Displacement current; (a) by voltage gradient, (b) by drain-source voltage

Experimental implementation

Without any EMI capacitors

Fig. 5 shows the experimental results of the voltage gradient and the displacement current. In Fig. 5a, it can be seen that with the higher dv/dt (V/ns), the displacement current also increases. In Fig. 5b, the displacement current increases with the higher drain-source voltage (V_{ds}). The operating V_{ds} voltage is set from 300 V to 1500 V. In this V_{ds} operating range, the measured voltage gradient dv/dt is between 2.71 and 8.49 V/ns at turn-off and turn-on respectively. In Fig. 5b, at the 1500 V_{ds}, the displacement current is 3.96 A (peak to peak). The displacement current flows from the heat sink to the system ground (aluminum plate). It can be seen that the higher displacement current at higher V_{ds} flows, which then results in higher EMI emissions with a larger EMI filter, higher cost, and size of the power electronic devices. This paper proposes two methods to mitigate the displacement current by keeping higher dv/dt.

Ceramic capacitors inside power module

Fig. 6 depicts the experimental results of the voltage gradient and the displacement current, which has been implemented as in Fig. 2. Two ceramic capacitors of 0.1 μF are placed inside the power module between the DC+ and DC- terminals. The ceramic capacitors are selected because of their smaller size, which results in faster energy transfer, and are available at the higher voltage of 1.5 kV. As already explained, this approach is executed to reduce the stray inductance and the distance between the

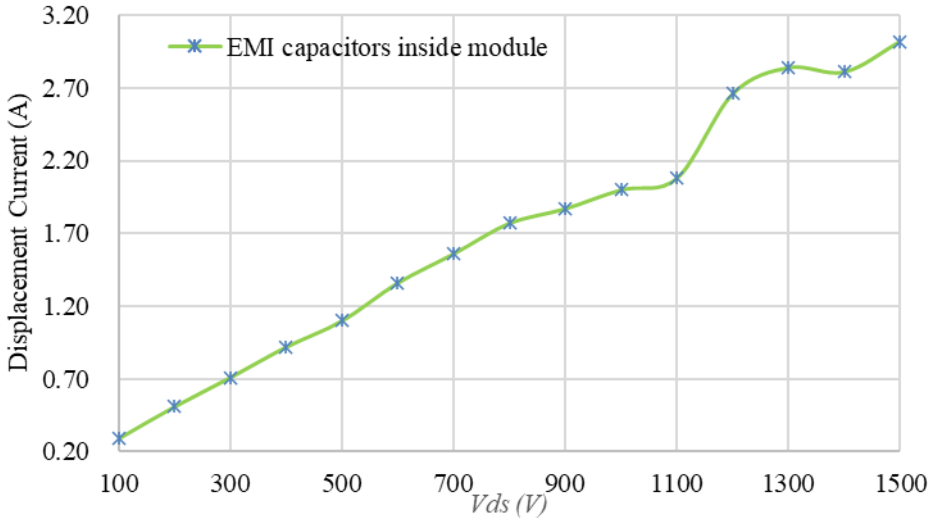


Fig. 6: Displacement current with EMI capacitors inside the power module

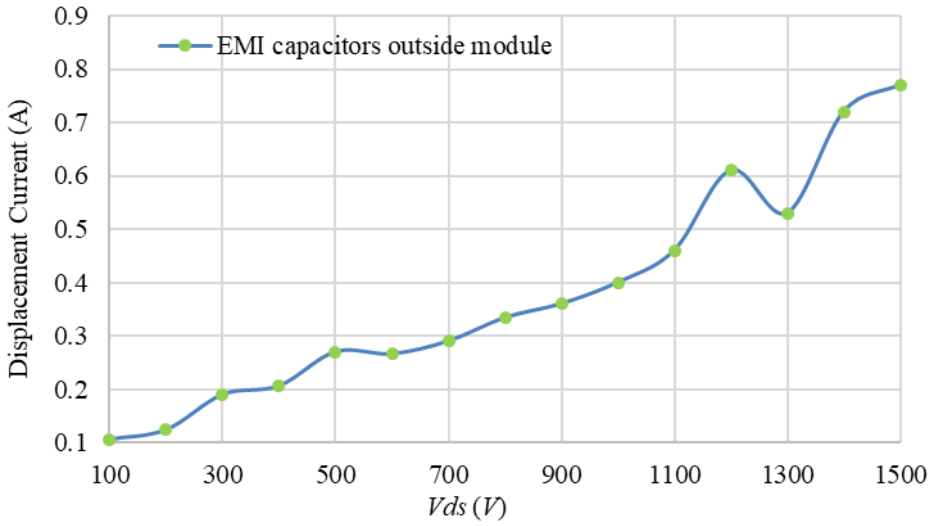


Fig. 7: Displacement current with EMI capacitors outside the power module

connected capacitors and the SiC chips module is less than 1.5mm. The displacement current is reduced to 3.1 A (peak to peak) at 1.5 kV in comparison to Fig. 5a. The displacement current is attenuated up to 22% in comparison to the typical experimental results without any EMI capacitors. The drawback of this approach is that the SiC module has a higher operating temperature (150 $^{\circ}C$ -175 $^{\circ}C$), where the operating temperature of the ceramic capacitors is in the range of (55 $^{\circ}C$ to +125 $^{\circ}C$). The ceramic capacitors can not be used for a longer time due to their higher difference in operating temperature ranges.

Film capacitors near power module

Fig. 7 presents the experimental results of the voltage gradient and the displacement current, which has been implemented as in Fig. 4. In this configuration, two Polypropylene (PP) film capacitors of 100nF are connected in parallel to the DC+/DC- and the heat sink. The most important advantage of the PP film capacitors is the reduced resistive losses (ESR) and the parasitic inductance of the capacitors (ESL) due to their internal structure. The reason for connecting two capacitors in parallel is to create a path of low impedance for the flow of the displacement current. The displacement current is reduced to 0.72 A at 1.5 kV at the proposed method as shown in Fig. 7. This approach is more effective than the other two methods mentioned in sections 1 and 2. This proposed approach attenuates the displacement current up to 80% compared to the no connection of the EMI capacitors.

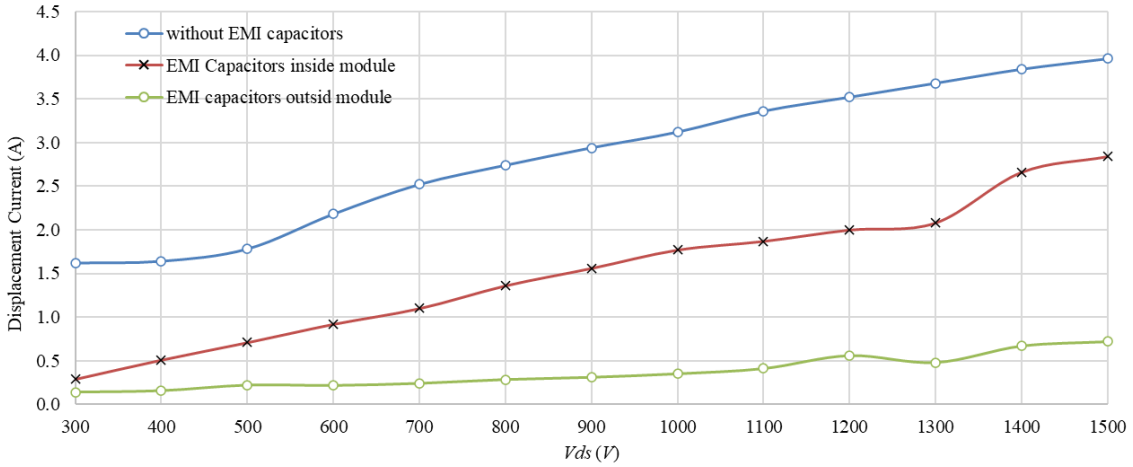


Fig. 8: Comparison of the displacement current for the proposed approach

This method is easier to implement, cost-effective, and results in a smaller EMI filter, which then helps in lower switching losses at higher dv/dt and higher power density. Fig. 8 compares the displacement current to the V_{ds}, where the proposed method of implementing the EMI capacitors in section 3 (green) has higher damping power than the capacitors connected inside the power module (blue) and no EMI capacitors (red) respectively.

Conclusion

This paper proposed a novel approach for the optimum placement of the EMI capacitors. The EMI capacitors were placed inside the power module and are compared with the no placement of the EMI capacitors, which shows the reduction of the displacement current. The novel approach is to place two EMI capacitors in parallel between the DC+/- and the heat sink. The experimental results of the suggested methodology are compared with the results of placing no capacitors and the placement of the EMI capacitors inside the power module. The indicated results of the parallel configuration of the EMI capacitors show sufficient mitigation of the displacement current by 80% up to 0.72 A at 1.5 kV compared to the capacitors placed inside the power module, which is 3.1 A at 1.5 kV respectively. The attenuation of the displacement current helps in the overall reduction of the EMI filters keeping higher dv/dt with lower switching losses and realizing higher power density for the wide-bandgap modules.

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