Analysis of Opportunities and Restrictions of a 3-Level Active Neutral Point Clamped Traction Inverter for 800V Battery Electric Vehicles

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Abstract— **Increasing dc-link voltage levels of battery electric vehicles implicate new requirements for traction inverters. Besides the application of higher-blocking wide-bandgap semiconductors, further technological solutions can contribute to highly efficient, low-cost inverter designs. 3-level inverters comprise the potential to improve future electric powertrains and thus need to be investigated concerning this application. This paper gives an overview over restrictions and opportunities of using a 3-level inverter in 800 V electric powertrains with focus on the ANPC structure. The discussed aspects include losses, harmonic performance, modulation, and especially the operation under fault condition.**

Index Terms— **ANPC Inverter, Battery Electric Vehicles, Multilevel Inverters, 800 V Powertrain**

I. Introduction

One of the key challenges of all industry branches including the automotive sector is to reduce carbon dioxide emissions. The electrification of vehicles is one of the most important and substantial instruments to achieve this objective [1]. Therefore, many approaches and solutions to improve performance and efficiency of electric powertrains emerged during the last years. Many of these approaches refer to single components while others consider a more holistic attempt. One of the latter concerns the dc-link voltage level with impact on battery, wiring, inverter, and the machine [2]. High voltage batteries in a modern battery electric vehicle (BEV) are usually in the range of 250-450 V but there is a trend of increasing battery voltage levels up to 800 V [2, 3]. Aside from negative consequences like higher requirements for the isolation, many positive effects come along with this adaption. A higher dc-link voltage allows lower current and therefore reduced cable losses or diameters [2]. On the other hand, charging times can be highly improved when using 800 V instead of 400 V rapid charging stations where the charging power is limited by the maximum current. A higher dc-link voltage directly affects the design of the traction inverter. On the one hand, high-blocking wide-bandgap semiconductors like SiC-MOSFETs accomplish the increased blocking voltage capability. On the other hand, certain kinds of multilevel inverter structures enable the application of 650 V devices despite a higher dc-link voltage. This advantage applies to the Neutral Point Clamped (NPC) inverter and some of its derivatives such as Active Neutral Point Clamped (ANPC) and Flying Capacitor (FC) inverter. Other three-level topologies like the T-Type NPC (T-NPC) inverter still require 1200 V semiconductors for a dc-link voltage of 800 V. Consequently, three-level inverters are commonly used in low and medium voltage applications, especially for photovoltaic (PV) or wind turbine energy transmission systems. Nevertheless, the operating conditions of an electric vehicle differ a lot from the requirements profile of a PV system. Detailed investigations indicate that especially the ANPC inverter which was first introduced in [4] has advantages regarding its performance at start-up and its efficiency in the operating range of traction applications [5, 6]. Moreover, the ANPC inverter is the only known topology among all two- and three-level inverters that offers full fail-operational fault tolerance regarding any single switch short circuit or open failure without the need of additional components [7]. Especially in the context of autonomous driving, reliability is a key factor in the design of future electric vehicles. Therefore, this paper addresses the most important restrictions and opportunities that arise when using an ANPC inverter in a BEV powertrain. In contrast to other available literature, a system cost analysis is done not only for one specific type of vehicle but for a wide range of vehicles from low to high power with different battery capacities. Furthermore, a short introduction to other possible 3-level structures with their specific properties is included. Thus, this paper gives useful information for the first steps of choosing the best fitting inverter structure for an 800 V BEV, depending on the manufacturer's boundary conditions.

II. 3-Level Inverters in Electric Vehicle Powertrains

Multilevel inverters have several advantages compared to the contemporary used 2-level six-pulse bridge (B6) inverter. They are highly efficient and offer less harmonics in the output current what is indicated by low total harmonic distortion (THD). To generalize the results shown in this paper, the mentioned inverter structures are operated at an adjusted switching frequency so the phase current THD (THD-i) is kept constant. Otherwise, additional machine losses due to eddy currents and iron losses would depend on the inverter type [8]. With an adjusted switching frequency and the assumption of constant machine losses at constant THD, all changes in the system loss refer to the inverter structure and the

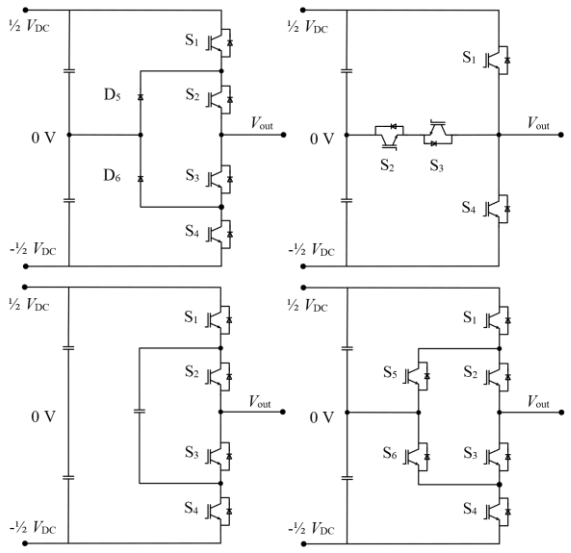

Fig. 1. 3-level inverter types: NPC (top left), T-NPC (top right), FC (bottom left) and ANPC (bottom right) structure.

machine can be ignored for the investigations. In other words, the switching frequency of a 3-level inverter is lower for same THD-i what leads to lower switching losses. 3-level structures also bring along disadvantages like increased number of components and higher control effort. Also, the failure probability increases with the number of components (including drivers and switches) which reduces lifetime expectations as well as system reliability. In contrast, the higher number of components generates redundant switching states, allows responses to failure events, and therefore holds the option of fault-tolerant operation. The extent of the fault tolerance potential highly depends on the inverter structure. [9] Therefore, the following sections give an overview of different 3-level inverter structures to be used in an electric vehicle powertrain and shortly explain their individual restrictions and opportunities.

A. NPC inverter

The NPC inverter structure consists of four active switches and two clamping diodes per phase (see Fig. 1). The diodes are connected to the neutral point and ensure that the maximum voltage stress for any device does not exceed $1/2 \cdot V_{\mathrm{DC}}$. Table I includes the switching states of the three output voltage levels P ($V_{\mathrm{out}} = +1/2 \cdot V_{\mathrm{DC}}$), 0 ($V_{\mathrm{out}} = 0$ V) and N ($V_{\mathrm{out}} = -1/2 \cdot V_{\mathrm{DC}}$). Since there are no redundant switching states, there is no option to affect the switching losses what leads to unbalances in loss distribution and junction temperatures, depending on the operating point. This is especially problematic for the application in BEVs because it is not sufficient to design the switches for only one operating point. Instead, the entire operating area of the vehicle must be covered. The NPC structure offers the option to adopt its modulation in case of a semiconductor failure so that an ongoing operation in some failure types is ensured [7].

TABLE I
SWITCHING STATES OF THE NPC INVERTER

State	S_1	S_2	S_3	S_4
P	1	1	0	0
0	0	1	1	0
N	0	0	1	1

B. T-NPC inverter

The T-Type NPC inverter is the inverter structure with the smallest number of required components. However, in contrast to the NPC inverter, only S_2 and S_3 can be designed with reduced blocking voltage while S_1 and S_4 must withstand the full dc-link voltage. The switching states are listed in Table II. Analogously to the NPC structure, the loss distribution depends on the operating point but cannot be adjusted during operation. A failure mode operation is also possible for some failure scenarios [7].

TABLE II
SWITCHING STATES OF THE T-NPC INVERTER

State	S_1	S_2	S_3	S_4
P	1	1	0	0
0	0	1	1	0
N	0	0	1	1

C. FC inverter

Like the T-NPC inverter, a 3-level flying capacitor inverter only requires four active switches. Instead of a neutral point connection, the zero-voltage state is generated by an additional capacitor which is charged to $1/2 \cdot V_{\mathrm{DC}}$. This allows two zero-sequence states, which are listed in Table III. These states must be used to balance the capacitor voltage and furthermore lead to a well-balanced loss distribution among all switches. However, the FC inverter offers less potential for fault tolerant modulation strategies than the other 3-level structures discussed in this paper [7].

TABLE III
SWITCHING STATES OF THE FC INVERTER

State	S_1	S_2	S_3	S_4
P	1	1	0	0
0_1	0	1	0	1
0_2	1	0	1	0
N	0	0	1	1

D. ANPC inverter

Regarding the number of components, the ANPC inverter structure with six active switches is the most complex one out of the types shown in Fig. 1. Due to the high number of switches, redundant states can be applied during zero-voltage sequence, depending on the selection of the zero-state 0_1, 0_2 or 0_3 from Table IV. Thus, the distribution of switching as well as conduction losses can be adjusted either static for one specific application or during real time operation [4]. This leads to an increased power density of the inverter because losses can be redistributed according to the actual operating point.

However, in an automotive environment, this approach can only be realized by a predefined modulation because the real time measurement of every junction temperature is not applicable. Therefore, this paper analyzes the ANPC inverter behavior with one static zero-sequence state or predefined loss balancing. The modulation scheme using 0_1 during the positive half cycle is defined as MS1. Analogously, MS2 uses 0_2 and MS3 operates by applying zero-state 0_3. During the negative half cycle, the zero-states of MS1 and MS2 are swapped and MS1 alternates between N and 0_2. Consequently, the commutation paths of MS1 are shorter than those of MS2. MS3 has another advantage because of the two parallel current paths during 0_3 which lead to reduced conduction losses, especially at low speed with small modulation index what is beneficial for a typical automotive drive cycle. Moreover, the ANPC structure offers full fault tolerant capability in case of any semiconductor failure by permanently connecting the faulty phase with the neutral point and adjusting the modulation strategy [7].

TABLE IV
SWITCHING STATES OF THE ANPC INVERTER

State	S_1	S_2	S_3	S_4	S_5	S_6
P	1	1	0	0	0	1
0_1	0	1	0	1	1	0
0_2	1	0	1	0	0	1
0_3	0	1	1	0	1	1
N	0	0	1	1	1	0

Despite the high number of components, the ANPC structure offers the highest potential for the design of an efficient and fault tolerant inverter for 800 V BEVs with 650 V semiconductors for high power density. The further chapters will address this inverter type in detail by showing the results of calculations, simulations as well as measurement data. All general statements are made as universal as possible to avoid application specific divergence. Thus, the given results can be adopted to any configuration of electric drive train and presented methods can be used to decide about the suitability of a 3-level (ANPC) inverter for several specific applications.

III. ANPC INVERTER OPERATING CONDITIONS

The main disadvantage of most of the mentioned types of multilevel inverters – including the ANPC structure – is an unequal loss distribution among the high number of switches which depends on the operating point of the inverter. When using MS1 where S_1 takes over a major part

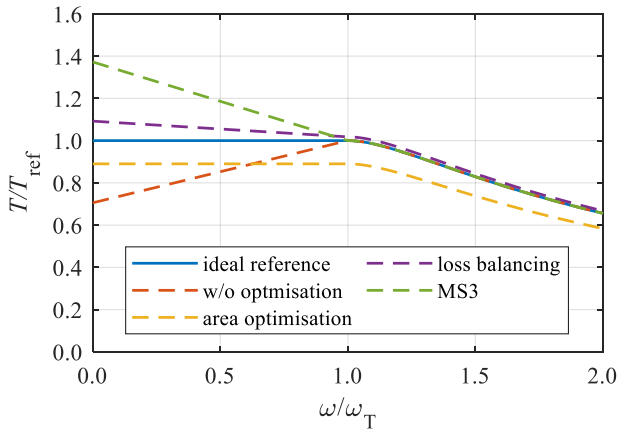

Fig. 2. Simulated impact of optimization strategies on the torque-speed operating range of an ANPC inverter with a permanent magnet synchronous machine.

of the switching losses, this switch becomes the hottest switch in the operating point selected for Fig. 3. The three plots show the calculated and measured losses for an ANPC inverter with MS1, MS2 and MS3 in the same operating point. By introducing the denotation S_{xy} which implies both S_x and S_y, symmetrically operating switches can be mentioned simultaneously which is possible due to the phase leg symmetry regarding the neutral point. The analytic calculation was performed based on the approach in [10] and the measurement was done with the hardware testbench presented in chapter V. It can be clearly seen that the modulation scheme has a high impact on the loss distribution and that the lowest overall losses are generated by using MS3 with two parallel paths during zero-voltage state. Hence, depending on the modulation scheme and operating point, some switches reach their maximum junction temperature at lower phase current than others do. This causes restrictions and opportunities for the operating range.

One restriction is a reduced start-up current when applying MS1 or MS2 for an ANPC inverter with Si-IGBTs and Si-diodes (which are the limiting components when continuously conducting during zero-voltage state). In contrast, when applying MS3, the start-up current and therefore the start-up torque is increased compared to the maximum current in the field weakening area. This is a result of the parallel current paths at low modulation index. Together with the influence of other optimization strategies like an active loss balancing approach based on [4] or optimized semiconductor areas according to [5], this effect is shown in Fig. 4. Consequently, an ANPC inverter with MS3 can offer higher starting torque what is

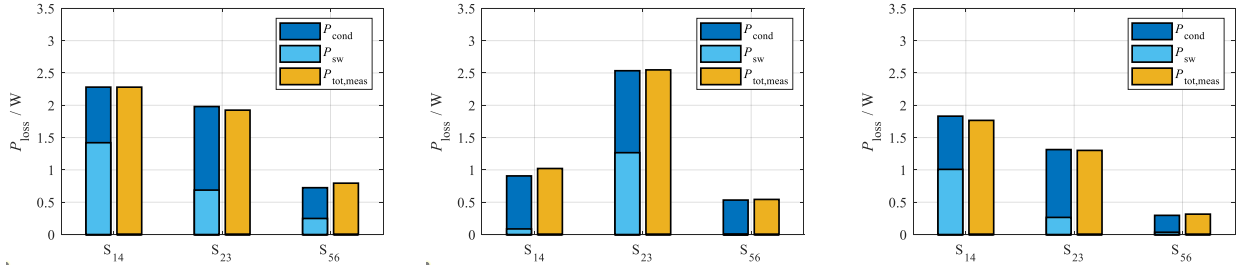

Fig. 3. Calculated and measured losses for MS1 (left), MS2 (middle) and MS3 (right) for m = 75 %, I_{rms} = 11 A, $cos(\varphi)$ = 1.

beneficial for the operation of an electric vehicle. The effect of an active loss balancing using MS1 and MS2 is smaller. An inverter with individually scaled die sizes for any topological switch counteracts the start-up current reduction but leads to an overall reduction of the maximum torque. A more detailed discussion of the mentioned optimization strategies is given by [5].

Another approach to increase efficiency and reduce installed semiconductor area is the combination of different semiconductor types for any switch in a hybrid ANPC inverter. Depending on the modulation scheme, some switches operate at high switching frequency while others operate at fundamental frequency. Thus, Si-IGBTs can be used for low frequency switches whereas SiC-MOSFETs are used for high frequency switches. [11] As a result, total losses are reduced and loss distribution becomes more equal. However, compared to a full-Si inverter the semiconductor cost increases by using more expensive SiC-MOSFETs. On the other hand, a hybrid ANPC inverter is less expensive than a full-SiC inverter. The overall suitability depends a lot on the specific application, what is also discussed in chapter VI and has not been analyzed by other authors for electric vehicle traction inverters yet.

As mentioned above, the phase current THD of 3-level inverters is reduced compared to 2-level inverters what is also valid for the implemented 3-level pulse width modulation (PWM) control of the hardware setup which is presented in chapter V (see Fig. 8). The measurement results show that the ANPC inverters THD-i is especially improved for high modulation index which affects the efficiency at higher speed. To simplify the loss analysis, in all analytical calculations the ANPC inverter operates at half switching frequency compared to a 2-level inverter what is concluded from Fig. 4. This is not an ideal method which is valid without error for any operating point, but it is the best approach to compare both 2- and 3-level inverters by using constant switching frequencies. For the manufacturer, as a rule-of-thumb it can be concluded that the switching frequency can approximately be halved when applying a 3-level inverter instead of a 2-level inverter for similar machine losses.

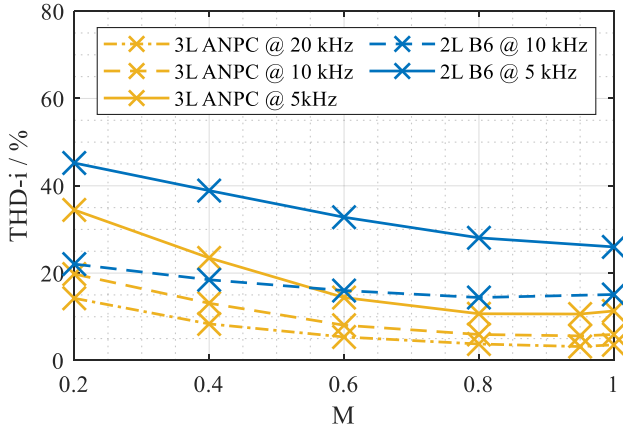

Fig. 4. Measured THD-i for 2-level B6 inverter and 3-level ANPC inverter at different switching frequencies over the modulation index.

IV. Fault Tolerant Behavior

The ability to adjust the inverter control in case of a semiconductor failure and continue operation in a degraded mode is a major advantage of the ANPC structure. Especially for autonomous driving but also for highly available non-autonomous electric vehicles. The failure mode is applied by a reconfiguration of the inverter structure using the remaining healthy switches. When the faulty switch is detected, the adjacent switches are turned off and a neutral point connection is applied by one of both zero-sequence paths 0_1 or 0_2 depending on the position of the failed semiconductor. Therefore, the maximum output voltage is halved but the inverter can still offer the full phase current [12]. The space vector diagrams before and after a failure mode reconfiguration (with exemplary failure in phase leg A) are given by Fig. 5.

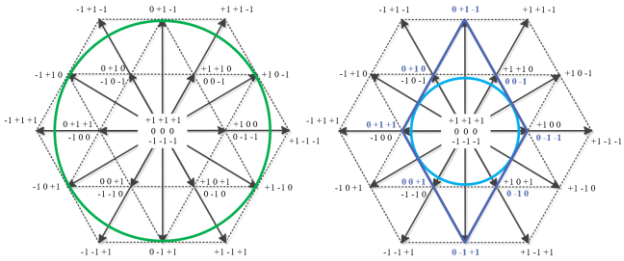

Fig. 5. Space vector diagrams for normal operation (left) and reconfigured failure mode operation with failure in phase leg A (right).

Due to the reduced maximum output voltage, the transition to the field weakening range is shifted towards lower speeds. Thus, the maximum torque is reduced at higher speeds [12]. Another restriction is given by the dc-link capacitance. The smaller the capacitors, the bigger is the neutral point voltage ripple which is depicted in Fig. 7. The measurement result is in good accordance to the expected voltage ripple. Especially at low speeds where the neutral point stress is high during any half cycle, this is a limiting factor for the maximum current [13]. Also, there is no option to balance the neutral point voltage by using redundant switching states, anymore. Instead, the inverter control must be adjusted to compensate unbalances. Fig. 6 shows the phase currents and voltages for normal operation at reduced dc-link voltage of 100 V due to restrictions in the passive ohmic inductive load. The applied switching frequency is 10 kHz and the modulation index is $m = 0.5$. In Fig. 7, the same operating point is shown for the reconfigured failure mode operation. Since only small vectors remain, the maximum allowed modulation index is $m = 0.5$. Thus, the inverter operates at its maximum voltage. The measurement shows a neutral point voltage ripple of ± 2 V. Due to the omission of all space vectors with high amplitude, the resulting modulation is similar to a 2-level modulation what can be seen in the line-to-line voltages, even though the symmetry between the voltages including the faulty phase is different from the one between both healthy phase legs.

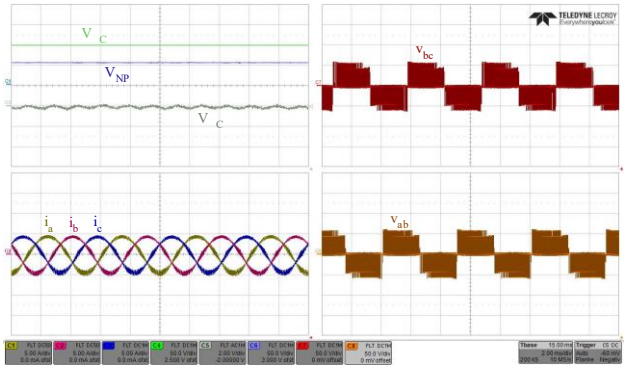

Fig. 6. Measured ANPC inverter parameters for normal operation. C1-3: phase currents, C4: dc-link voltage, C5: neutral point ripple (ac-coupling), C6: neutral point voltage, C7-8: line-to line-voltages.

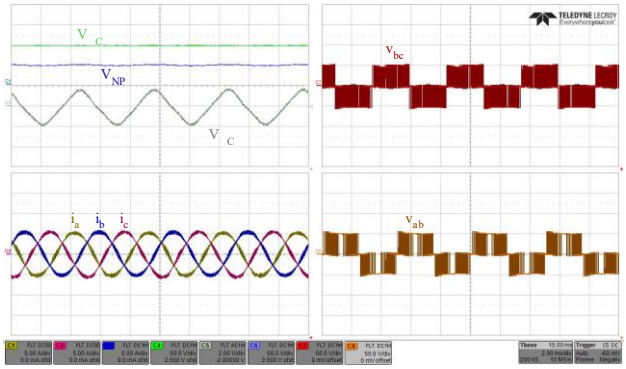

Fig. 7. Measured ANPC inverter parameters for failure mode operation. C1-3: phase currents, C4: dc-link voltage, C5: neutral point ripple (ac-coupling), C6: neutral point voltage, C7-8: line-to-line voltages.

V. Hardware Measurement Setup

The validation of the analytically and numerically simulated impact of using an ANPC inverter in a BEV powertrain is done by measurement using a scaled down 3-phase 3-level ANPC inverter (see Fig. 8) at passive ohmic inductive load as well as an electric machine testbench. The inverter prototype is designed with three parallel discrete TO-247 SiC-MOSFETs for each topological switch. With an infrared camera, losses can be measured individually for every switch and therefore, different modulation techniques can be evaluated due to their efficiency, loss distribution and limitation of the operating area. Due to its symmetry regarding the neutral point, only the switches S1, S2 and S5 must be observed when analyzing losses and switching behavior since the three lower switches act analogously.

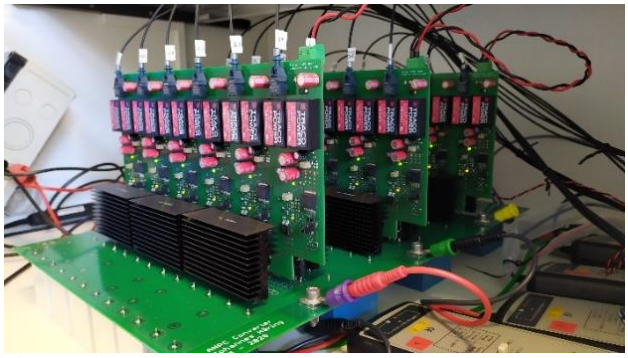
Fig. 8. 3-phase 3-level ANPC inverter setup.

The setup is designed for a dc-link voltage of 800 V and a current of 30 A. Due to restrictions in the passive load and the coupled integrated permanent magnet synchronous machine (IPMSM), some experiments must be performed with reduced dc-link voltage. Nevertheless, all relevant theoretical statements made in this paper can be analyzed and verified by measurement (see Fig. 3, Fig. 4, Fig. 6 and Fig. 7).

VI. ANPC Inverter Cost Analysis

Using analytical equations based on [10] for conduction and switching losses of any single switch in an ANPC inverter, the required semiconductor area and the efficiency in the *Worldwide Harmonized Light Vehicles Test Drive Cycle* (WLTC) are calculated. The performance at maximum current at start-up and nominal speed is used to determine the semiconductor cost K_{Chip} for the inverter (1). Furthermore, by applying (2) the WLTC efficiency η_{WLTC} defines the required additional battery cost $K_{\mathrm{Bat,add}}$ (when assuming an extra need of battery capacity for an inverter with efficiency $\eta_{\mathrm{WLTC}} < 1$ to reach the same driving range with every inverter type). The sum of both cost shares results in the total cost K_{total} which is given by (3). $k_{\mathrm{Si,SiC}}$ is the specific semiconductor cost for silicon (Si) or silicon carbide (SiC) per chip area and k_{Bat} is the battery cost per kWh. A_{Chip} is the total required semiconductor area for the entire inverter and C_{Bat} is the battery capacity which defines the driving range for an inverter without losses.

$$K_{\mathrm{chip}} = A_{\mathrm{Chip}} \cdot k_{\mathrm{Si,SiC}} \tag{1}$$

$$K_{\mathrm{Bat,add}} = \frac{1-\eta_{\mathrm{WLTC}}}{\eta_{\mathrm{WLTC}}} \cdot C_{\mathrm{Bat}} \cdot k_{\mathrm{Bat}} \tag{2}$$

$$K_{\mathrm{total}} = K_{\mathrm{Chip}} + K_{\mathrm{Bat,add}} \tag{3}$$

Taking these two cost factors into account, a simplified system cost analysis can be performed. The result is shown in Fig. 9 where each color indicates one inverter structure with the least expensive system cost for the given parameters.

All semiconductor parameters are scaled to the same power module conditions for best comparability. In the next step, all observed inverter structures with customized modulation and optimization strategies are designed for given apparent output power S_{out}. Then losses and efficiency are determined in WLTC drive cycle. This scaling and dimensioning approach is specified more detailed in [5]. As an extension to the results given in [5], a variation of output power and battery capacity is performed in this paper. This approach shows the trend towards SiC inverters for electric vehicles with lower maximum power but large driving range and therefore high battery capacity. The 3-level ANPC inverter with die size optimized Si-IGBTs and MS3 performs best for powerful inverters with smaller battery because of the

reduced semiconductor cost compared to SiC-inverters. Hybrid inverters with Si-IGBTs for the low frequency switches S_{23} and SiC-MOSFETs for all other switches are only competitive at high power and high battery capacity. A hybrid inverter with MS1 and four Si-IGBTs is also investigated but does not appear among the least expensive structures. Since the focus of this paper is on the ANPC structure, other 3-level structures are not included in this comparison. Further studies showed that especially the T-NPC structure is another very promising inverter type regarding efficiency and semiconductor cost but without the option of full fault-tolerance and only by using 1200 V devices. The calculation of the cost matrix is done by the following cost estimations which are extracted from recent literature [14–16]. For a more general approach, all costs were defined in monetary units (MU).

TABLE V
COST FACTORS FOR OVERALL COST CALCULATION

Cost factor	Value	Unit
k_{Si}	1	MU/cm^2
k_{SiC}	10	MU/cm^2
k_{Bat}	80	MU/kWh

With the information generated by Fig. 9, further cost estimations regarding number of components, control effort, volume, etc. can be added to find the cost optimum for a specific design in a certain BEV. However, the chosen cost factors are volatile and will change in the next years. The semiconductor cost for Si is expected to stay relatively constant while k_{SiC} and k_{Bat} are most likely to decrease with increasing market share. Consequently, the boundaries between the observed structures in Fig. 9 will shift in future, depending on the development of semiconductor and battery prizes but the general outcomes will still be valid.

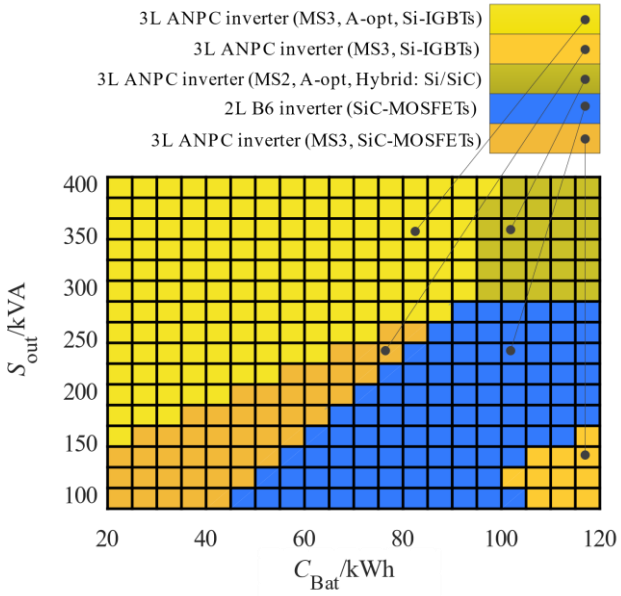

Fig. 9. Matrix with least expensive inverter structure depending on output power and battery capacity for given chip and battery cost estimation.

VII. CONCLUSIONS

This paper gives an overview over general restrictions and opportunities of 3-level inverters in BEVs and focuses on key aspects for the operation of a 3-level ANPC inverter. It addresses advantages which lead to new design opportunities for the entire powertrain but also shows why 3-level inverters are not yet used in BEVs today. The high number of components and an unequal loss distribution are identified as major disadvantages. On the other hand, increased efficiency, fault tolerant behavior and the opportunity to increase the start-up current bring along new degrees of freedom in the inverter design. In contrast to other publications, this paper provides a holistic analysis of the ANPC structure for BEVs as a concrete field of application. Furthermore, it can be used as a guidance to estimate the system cost of a 3-level ANPC inverter for BEVs with specific boundary conditions when designing a new 800 V BEV drive train.

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