Design Method of a High Frequency GaN-based Half-Bridge with Bottom-Side Cooled Transistors Using Multi-PCB Assembly

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Keywords

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Abstract

This paper proposes a Multi-PCB (M-PCB) design of a half-bridge using bottom-side cooled GaN transistors with optimal layout and thermal management. The fabrication process only requires limited technological capabilities and is well-suited for industrial applications. Electrical and thermal performances are evaluated by measurements and simulation and compared with previous works.

Introduction

The constant growth in the demand for embedded static converters with high power density and high efficiency requires the development of new design approaches. Operating at higher frequencies (over 1 MHz) while reducing power losses are the key solutions to improve efficiency and miniaturize power converters. The advantages of GaN power transistors in terms of electron mobility and intrinsic parasitics make them the ideal candidates for High Frequency (HF) power conversion [1]. Recent works have highlighted the benefits brought by GaN devices in designing efficient and compact power converters for various applications in domains such as automotive, aeronautics, servers… [2]-[5].

Although GaN transistors have attractive characteristics for high frequency power conversion, their switching times in the range of nanosecond causes high overvoltage and ringing due to the parasitic elements of the commutation cells. In order to avoid a dual impact on efficiency and cooling systems of the power devices, it is necessary to reduce the commutation loop parasitic inductances. To achieve this goal, Printed Circuit Board (PCB) embedded power converters based on Electronic Design Automation (EDA) techniques have emerged these last years [6].

When designing power converters on PCB using bottom-side cooled GaN transistors, their thermal management can be easily improved by designing thermal vias through the FR4 substrate and optimizing their layout [7]. This method has been widely used for the PCB integration of unpackaged power chips [8], [9]. The recent improvements in GaN transistors packaging allow to consider applying equivalent design methods for the integration of packaged power devices in PCB assemblies. Also, it has been demonstrated that vertical commutation loops can consequently reduce the total parasitic inductances by limiting the loop area and canceling a part of the magnetic flux [10], [11]. These results lead to lower power losses and lower Electromagnetic Interferences (EMI). However, authors in [10] have highlighted that the design of a vertical loop and thermal vias were not compatible on a single PCB.

In this context, this work proposes the Multi-PCB (M-PCB) design for GaN-based half-bridge using a three-layer PCB assembly. The proposed solution allows the combination of an optimized commutation loop design with an optimized thermal management for bottom-side cooled GaN transistors. The second section of this paper details the fabrication process while Section III and IV give the Electromagnetic (EM) and thermal analysis of the proposed structure. In section V, the switching waveforms of the DC-DC converter are analyzed while operating at 1 MHz, 300 V input voltage and 6 A output current. The experimental results are compared with EM/circuit simulations. The advantages of the proposed solution are then highlighted by testing the power converter in continuous mode and

comparing the obtained thermal results with previous work using the same devices in equivalent conditions. Finally, a discussion about future improvements is proposed in the conclusion.

Design of the M-PCB Half-Bridge

The electrical scheme of the considered GaN-based half-bridge is presented in Fig. 1(a). The commutation cell is constituted of two bottom-side cooled p-GaN HEMT (GS66502B: 650 V - 8 A @ 25 °C) and DC-link ceramic capacitors. Finally, two isolated single gate drivers SI8271 are used to control the power transistors. This enables the optimization of the gate loop design for the GaN devices. It should be noted that the following design is also compatible with a half-bridge gate driver but not proposed in this study.

In order to optimize the commutation loop design while offering the best thermal performances for these devices, it is proposed to separate electrical and thermal paths by achieving the three-layer PCB assembly as shown in Fig. 1(b). A vertical commutation loop is realized between the DC-link capacitor located on the top layer and the GaN transistors located on the intermediate layer. The heat transfer is performed from the bottom side of the GaN transistors packaging (source) to the bottom layer by means of thermal vias. An Aluminum Nitride (AlN) substrate is inserted between the bottom layer of the assembly and the heat sink to ensure dielectric insulation while ensuring the best thermal conductivity and spreading the heat on the heat sink area.

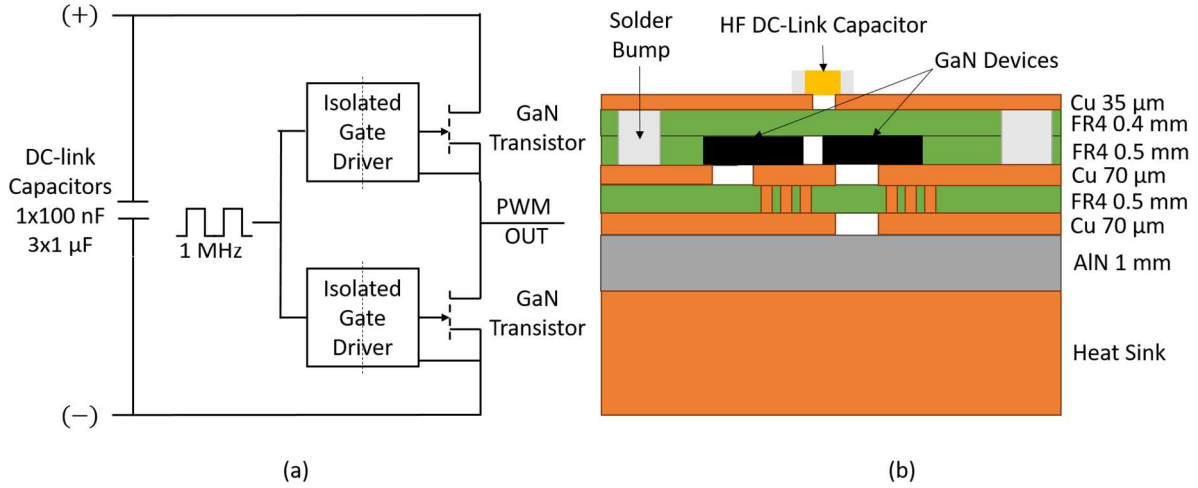

Fig. 1: Presentation of the proposed M-PCB half-bridge (a) simplified electrical scheme (b) 3-layer design (cross-sectional view)

The manufacturing process of the structure described in Fig. 1(b) is divided into four steps as shown in Fig. 2:

1. Fabrication of the circuit for the GaN transistors on a double-sided PCB (FR4: 0.5 mm, Cu: 70 µm) with metalized thermal vias (Fig. 2(a)).
2. Deposit of a tin layer on gate, drain, source connections of each devices and soldering of the transistors (Fig. 2(b)).
3. Fabrication of a 0.5 mm FR4 windowed layer and fixation on the previous PCB to reach the height of the transistors (Fig. 2(c)).
4. Assembly of the upper single-sided PCB (FR4: 0.4 mm, Cu: 35 µm) including the half-bridge circuit on the structure. Soldering of gate, drain and source connections of each transistor on the top side circuit (Fig. 2(d)).

Fig. 3 shows the fabricated parts of the M-PCB half-bridge and its final assembly. In the next sections the electrical and thermal performances of the proposed structure are analyzed through simulations and measurements.

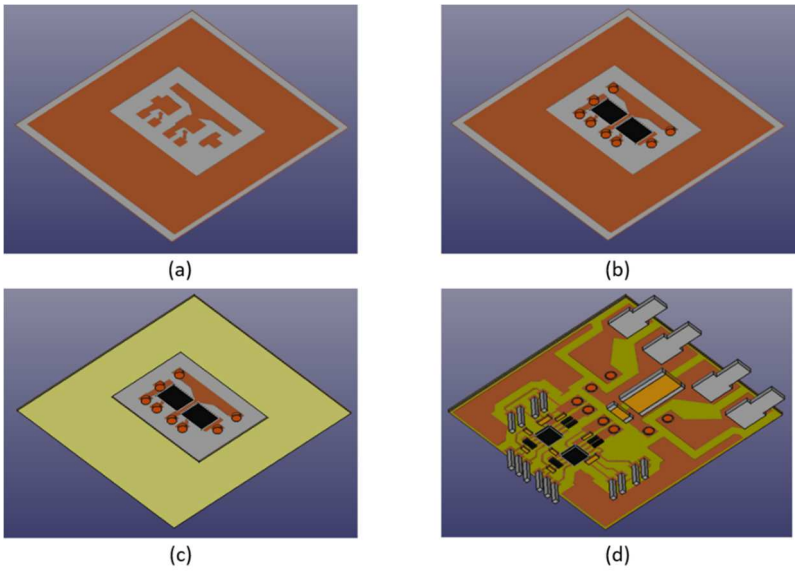

Fig. 2: M-PCB half-bridge fabrication process

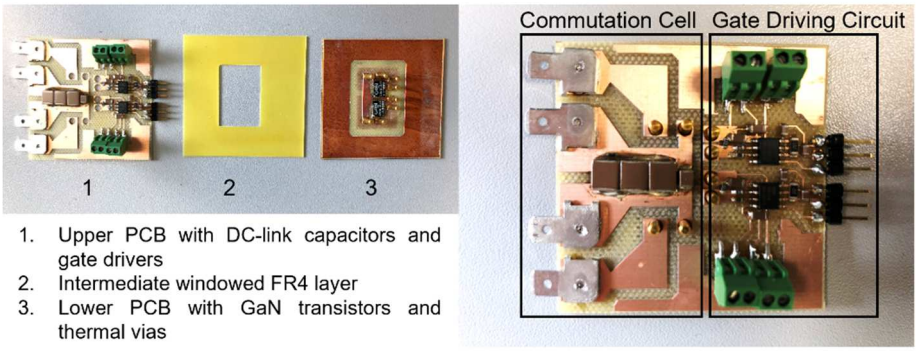

Fig. 3: Presentation of the fabricated parts and the assembly of the proposed M-PCB half-bridge

Loop Inductances Characterization

The design optimization of the considered converter is carried out by simulation. Thus, an EM modeling of the M-PCB half-bridge is performed using Advance Design System (ADS®) software in order to extract the parasitic inductance values of the commutation and gate loops. The design of the PCB implemented in the software is presented in Fig. 4(a). As shown in Fig. 4(b), the tin vias connecting transistors terminals to the rest of the circuit are modeled by 2 mm diameter cylinders and the thermal vias are modeled by 0.4 mm hollow cylinders with 20 µm copper filing. In order to get the best accuracy for the determination of the parasitic inductances, the EM model of the transistors packaging proposed in [11] is added to the simulation. The EM simulation is performed from 1 MHz to 100 MHz with logarithmic frequency sweep and from 1 Hz to 2 GHz with an adaptive frequency sweep.

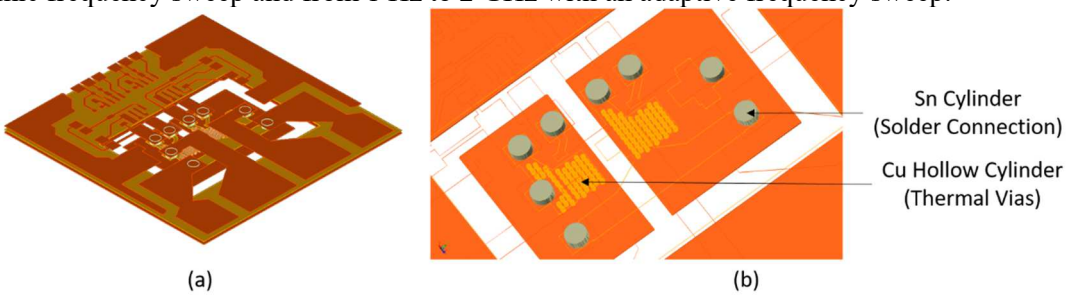

Fig. 4: PCB implementation in ADS software (a) 3D global view (b) geometries for the different vias

1-Port S-parameter EM/circuit co-simulations are then performed to characterize the different converter loops in the circuit. For each simulation, the loop inductance L_{loop} is obtained from the

simulated S_{11} parameter using (1). Fig. 5 gives the commutation loop and the two gate loop inductances evolutions over frequency from 1 MHz to 100 MHz.

$$L_{loop} = \frac{Im\left(Z_0 \left(\frac{1+S_{11}}{1-S_{11}}\right)\right)}{\omega} \quad (1)$$

Where, ω is the pulsation in rad/s and Z_0 is the 50 Ω characteristic impedance.

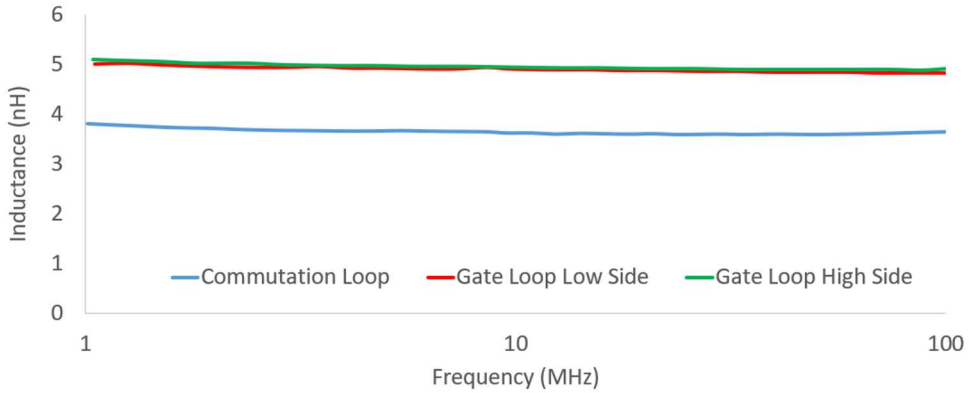

Fig. 5: Simulation results of the converter loop parasitic inductances versus frequency

For the half-bridge configuration, Table I compares the extracted commutation loop inductance at 1 MHz with the obtained values in lateral and vertical design given in [11]. The proposed optimized design of the commutation loop offers drastically lower inductance value than the lateral and vertical design in [11]. It should be noted that the encapsulation inductance of a single GaN transistor has been measured to 2.5 nH using S-parameters [11].

TABLE I
SIMULATED COMMUTATION LOOP INDUCTANCE AT 1 MHZ

Lateral Layout (nH) [11]	Vertical Layout (nH) [11]	Optimized Vertical Layout (nH, This Work)
13	4.4	3.8

Thermal Analysis of the M-PCB Half-Bridge

The geometry of the M-PCB half-bridge is implemented in COMSOL® software to evaluate the temperature of the GaN transistors for different dissipated power levels. Fig. 6(a) shows the temperature distribution obtained for a dissipated power of 5 W in each GaN transistor. The obtained power-temperature relation is also experimentally analyzed using a Fluke TI-32 thermal imaging camera as shown in Fig. 6(b).

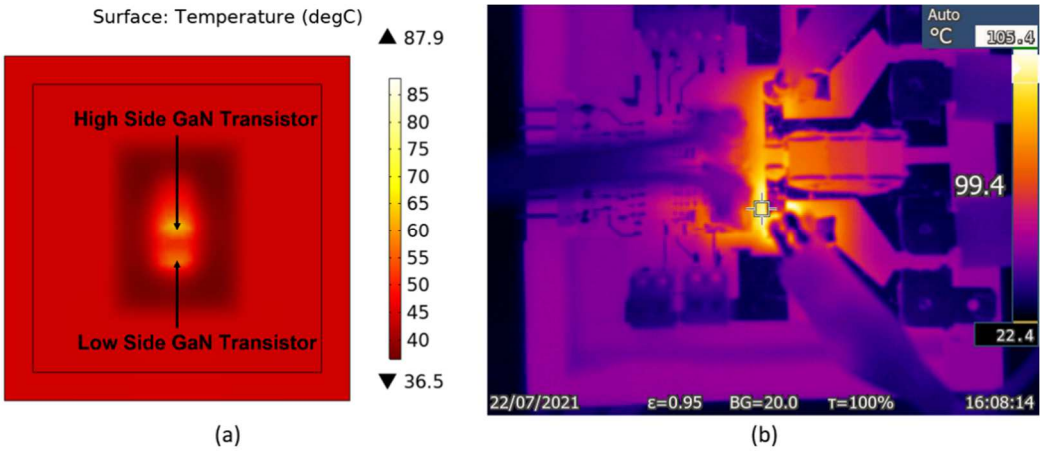

Fig. 6: Analysis of the GaN transistors temperature (a) COMSOL simulation (b) measurement

For measurements, the V_{GS} of the transistors are set to 6 V using two isolated power supply, the DC-link voltage is adjusted to inject a controlled DC current and reach different dissipated power levels in the devices. The obtained simulation results are compared to experimental data for different dissipated power in the GaN transistors (Fig. 7).

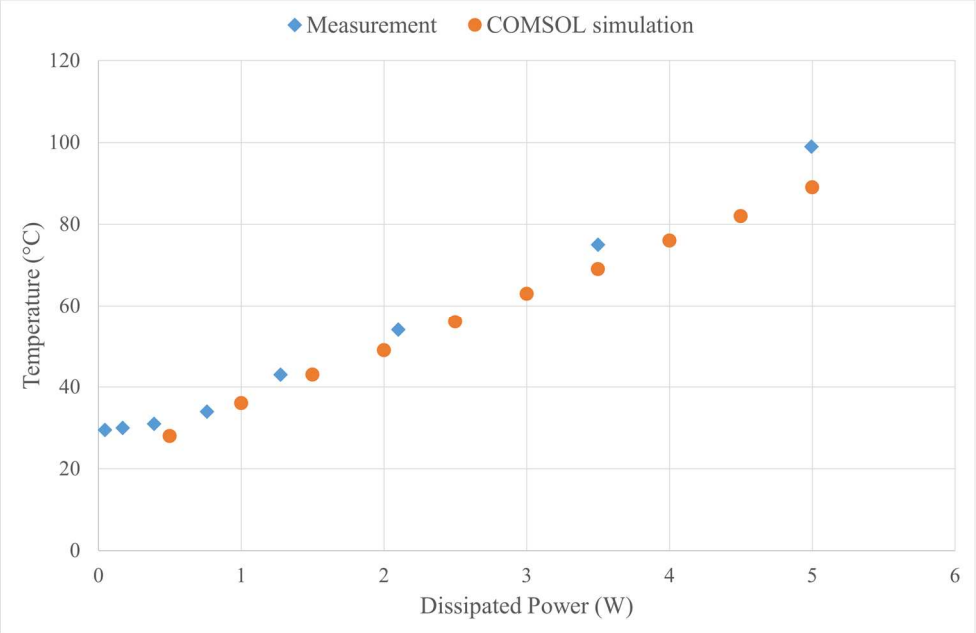

Fig. 7: Measured and simulated temperature of the low-side GaN transistor for different dissipated power levels

These results show slight differences between measurement and simulation when increasing the dissipated power. This could be explained by a non-homogenous convective environment in the experimental setup. In the simulation, a convective heat flux using external natural convection by air with spherical geometry is considered. In the experiment, the prototype is placed on a table. From these results, the thermal resistance from case to ambient is 12 °C/W by simulation and 15 °C/W by measurement.

Converter Performances Evaluation in DC-DC Operation

The DC-DC converter is first tested in burst mode at 1 MHz. Fig. 8 gives the obtained switching waveforms for both low and high side GaN transistors after reaching the electrical steady state (10 periods). The DC-link voltage is 300 V and the switched current is 6 A. The duty cycle is set to 50 % and the dead times are 50 ns (10 % of the switching period in total). Gate driving voltages are -3/+6 V and gate resistances are 27 Ω for turn-on and 2.2 Ω for turn-off. V_{GS} and V_{DS} voltages are measured using optically isolated voltage probes IsoVu®. The currents in the transistors were not measured because the current probe introduction would drastically modify the parasitic inductance of the commutation loop. The output load consists of an 80 µH inductor in series with a 25 Ω resistor.

Fig. 9 and Fig. 10 show the comparison between measured and simulated waveforms at turn-on and turn-off of the low side and high side transistor respectively. The simulations are performed in ADS® by coupling circuit models of the components and an EM model of the PCB as detailed by authors in [11], [12]. The PCB fabrication files are imported in the software and an EM simulation (Momentum in ADS software) is performed taking into account interconnects parasitic elements as well as inductive and capacitive couplings between layers. The GaN transistor model for device GS66502B obtained using S-parameter and static I(V) characterization as described in [12] is used in this work. Passive components such as DC link capacitors and RL load have been modeled based on impedance characterizations up to 110 MHz using the impedance analyzer 4294A. The gate driver model considers internal resistances as well as rise and fall times according to the datasheet.

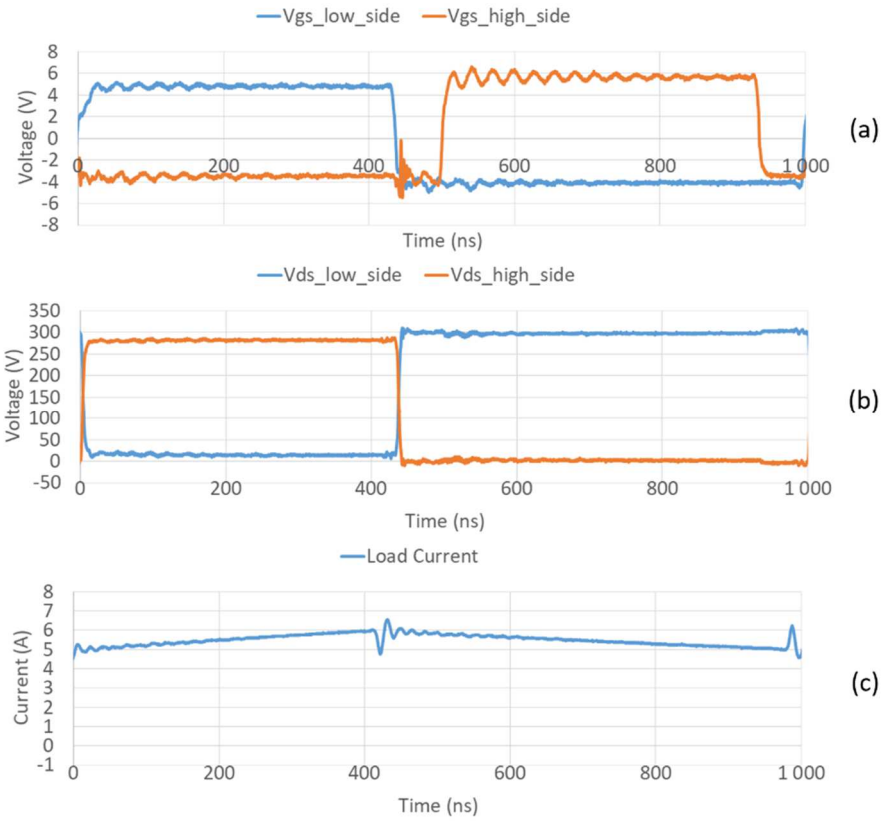

Fig. 8: Switching waveforms at 1 kW / 1 MHz (a) low and high side V_{GS} (b) low and high side V_{DS} (c) load current

Good agreement is observed between experimental and simulation results (Fig. 9 and Fig. 10). One can observe that rise and fall times of V_{GS} and V_{DS} of both transistors are in good accordance between measurement and simulation except at turn-on of the high-side GaN transistor. Authors assumed that the slight different observed could be attributed to a specific behavior of the gate driver in these test conditions.

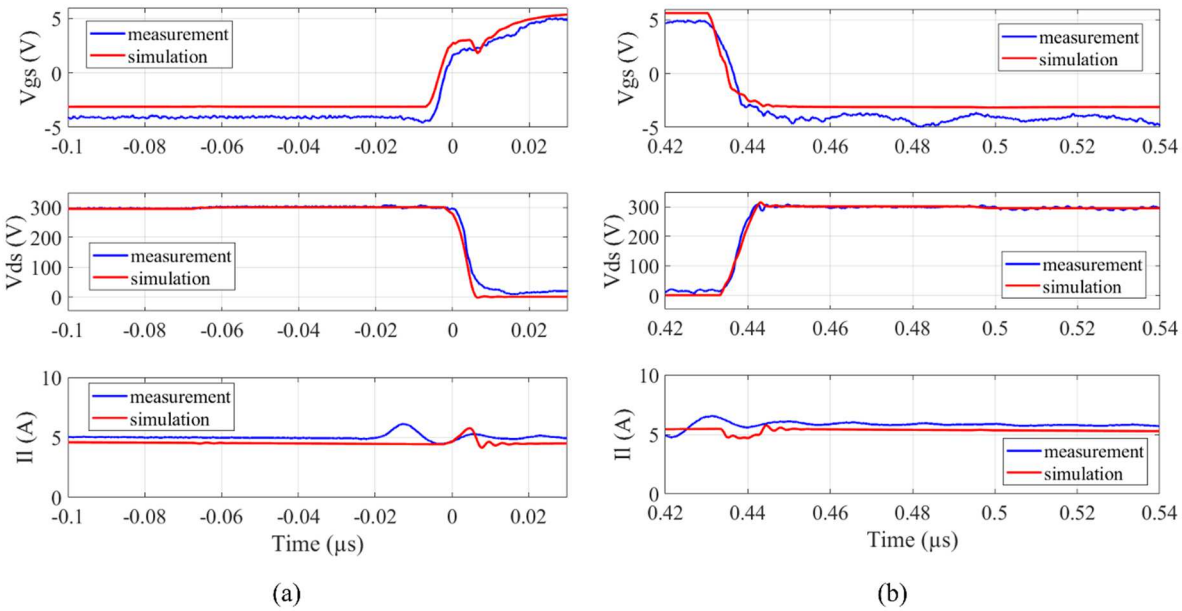

Fig. 9: Waveforms of the low-side GaN transistor and load current at (a) turn-on and (b) turn-off of the device

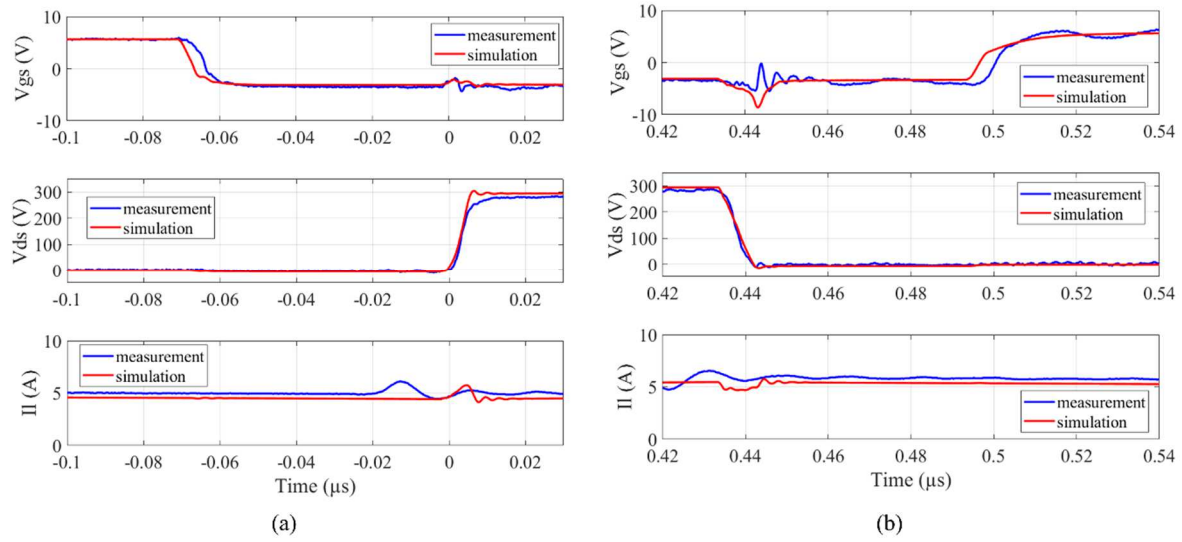

Fig. 10: Waveforms of the high-side GaN transistor and load current at (a) turn-off and (b) turn-on of the device

The switching waveforms of the GaN transistors are obtained with a maximal V_{DS} overshoot of 4 % and a maximal V_{GS} overshoot of 6 %. This confirms the advantage of the M-PCB converter design method in the optimization of the commutation loop. The V_{DS} voltage slew rate is approximatively 50 V/ns for an output current of 6 A.

The converter is then tested in continuous mode with an operating frequency of 1 MHz. The DC-link voltage is 200 V and the output current is 2 A. The duty cycle is set to 50 % and the dead times are 50 ns. The temperature steady state is reached after 15 minutes. The temperature of the GaN transistors is measured at 70 °C in steady state as shown in Fig. 11. Compared with results in [12], where the same GaN device is used in the same test conditions (power, frequency), the device temperature is 20 °C lower in this work. This enhancement is mainly due to lower switching losses and a more efficient thermal design in the proposed M-PCB converter. However, it should be noted that in [12] the GaN power transistor is tested in association with a SiC diode and not in Half-Bridge conditions.

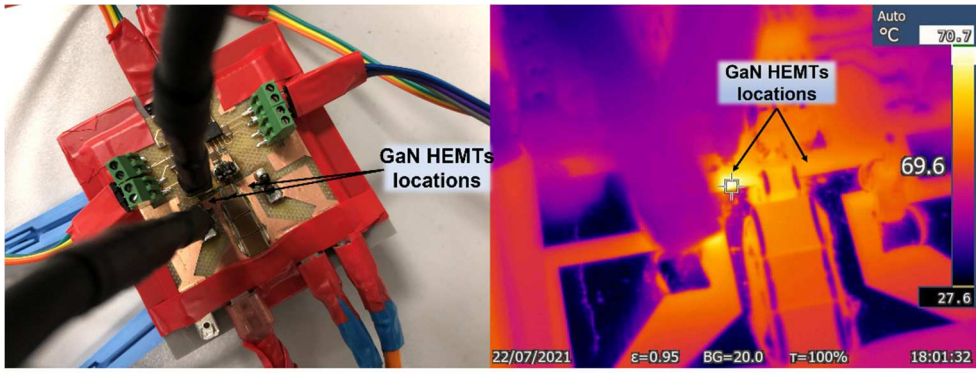

Fig. 11: Steady state GaN devices temperature at 200 W / 1 MHz (a) test setup (b) thermal measurements

Conclusion

In this paper a M-PCB design method of a half-bridge based on bottom-side cooled GaN-HEMT transistors is proposed for high frequency power conversion. The presented multi-layer PCB assembly has allowed to reduce the parasitic inductance of the commutation loop while offering an efficient cooling by thermal vias. The power converter has been electrically and thermally characterized using EM/circuit and 3D thermal simulations. A good accordance has been found between simulation and experimental results showing the possibility to optimize the design of power converters by simulation for power electronics designers. Finally, the tests of the converter that operating at 1 MHz have

highlighted the benefits of the proposed solution compared with previous ones in terms of switching losses and temperature of the GaN transistors. Future work will focus on designing the GaN devices circuit (lower PCB) on an AlN substrate in order to overtake the thermal performances of thermal vias by combining lower thermal resistance and dielectric insulation.

References

[1] I. Omura, W. Saito, T. Domon and K. Tsuda, "Gallium Nitride power HEMT for high switching frequency power electronics," in 2007 International Workshop on Physics of Semiconductor Devices, Mumbai, India, 16-20 Dec. 2007 .

[2] X. Zhou, B. Sheng, W. Liu, Y. Chen, L. Wang, Y.-F. Liu and P. C. Sen, "A High-Efficiency High-Power-Density On-Board Low-Voltage DC–DC Converter for Electric Vehicles Application," IEEE Transactions on Power Electronics, vol. 36, no. 11, pp. 12781 - 12794, Nov. 2021.

[3] M. Schiestl, F. Marcolini, M. Incurvati, F. G. Capponi, R. Stärz, F. Caricchi, A. S. Rodríguez and L. Wild, "Development of a High Power Density Drive System for Unmanned Aerial Vehicles," IEEE Transactions on Power Electronics, vol. 36, no. 3, pp. 3159 - 3171, March 2021.

[4] M. H. Ahmed, M. A. d. Rooij and J. Wang, "High-Power Density, 900-W LLC Converters for Servers Using GaN FETs: Toward Greater Efficiency and Power Density in 48 V to 6√12 V Converters," IEEE Power Electronics Magazine, vol. 6, no. 1, pp. 40 - 47, March 2019.

[5] F. Salomez, S. Vienot, B. Zaidi, A. Videt, T. Duquesne, H. Pichon, E. Semail and N. Idir, "Design of an integrated GaN inverter into a multiphase PMSM," in 2020 IEEE Vehicle Power and Propulsion Conference (VPPC), Gijon, Spain, 18 Nov.-16 Dec. 2020.

[6] C. Buttay, C. Martin, F. Morel, R. Caillaud, J. L. Leslé, R. Mrad, N. Degrenne and S. Mollov, "Application of the PCB-Embedding Technology in Power Electronics – State of the Art and Proposed Development," in 2018 Second International Symposium on 3D Power Electronics Integration and Manufacturing (3D-PEIM), College Park, MD, USA, 25-27 June 2018.

[7] S. Zhang, E. Laboure, D. Labrousse and S. Lefebvre, "Thermal management for GaN power devices mounted on PCB substrates," in 2017 IEEE International Workshop On Integrated Power Packaging (IWIPP), Delft, Netherlands, 5-7 April 2017.

[8] S. Moench, R. Reiner, P. Waltereit and a. al., "PCB-Embedded GaN-on-Si Half-Bridge and Driver ICs With On-Package Gate and DC-Link Capacitors," IEEE Transactions on Power Electronics, vol. 36, no. 1, pp. 83 - 86, Jan. 2021.

[9] B. Weiss, R. Reiner, P. Waltereit, R. Quay and O. Ambacher, "Operation of PCB-embedded, high-voltage multilevel-converter GaN-IC," in 2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Albuquerque, NM, USA, 30 Oct.-1 Nov. 2017.

[10] B. Sun, K. L. Jørgensen, Z. Zhang and M. A. Andersen, "Research of Power Loop Layout and Parasitic Inductance in GaN Transistor Implementation," IEEE Transactions on Industry Applications, vol. 57, no. 2, pp. 1677 - 1687, March-April 2021.

[11] L. Pace, N. Idir, T. Duquesne and J.-C. D. Jaeger, "Parasitic loop inductances reduction in the PCB layout in GaN-based power converters using S-parameters and EM simulations," Energies, vol. 14, no. 5, p. 1495, March 2021.

[12] L. Pace, F. Chevalier, A. Videt, N. Defrance, N. Idir and J.-C. D. Jaeger, "Electrothermal Modeling of GaN Power Transistor for High Frequency Power Converter Design," in 2020 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe), Lyon, France, 7-11 Sept. 2020.