An Efficiency Improvement Method of High-step-down Converter

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***Abstract*–The power supplies for data centers and telecom station are replaced complex and expensive isolated 48 V/54 V step-down converters with more efficient non-isolated, high-density step-down regulators. Replacing the isolated converter with a non-isolated step-down converter can significantly simplify the design, reduce costs and board space. A novel high-step down converter is proposed with three advantages: (1) Zero voltage switching turn-on; (2) It only needed one extra coupling inductor, a ground reference active switch, and a capacitor; (3) it can be driven by the buck control IC. In this paper, an efficiency improvement method is presented.**

I. INTRODUCTION

The power supply structure of data centers and telecom systems has changed significantly. Major manufacturers are replacing complex and expensive isolated 48 V/54 V step-down converters with more efficient non-isolated, high-density step-down regulators. Isolation is not required in the power supply, because the upstream input of 48 V or 54 V is already isolated from the hazardous AC supply. Replacing the isolated converter with a non-isolated step-down converter can significantly simplify the design, reduce costs and board space.

The method proposed in papers [1-7] uses coupled inductors to achieve a low gain ratio. They are relatively simple, but a passive snubber must be needed to suppress the high voltage spike, which comes from the leakage inductor. In [7, 8], active snubber is proposed to recycle winding leakage energy, but the circuit is complicated and costly. In papers [2, 9-11], there are many components and the cost is high. The solution proposed in papers [2, 6, 9, 12, 13] requires the use of expensive floating drives. This method of [14] requires more passive components, which occupy board space.

The topologies proposed in previous papers [15-17] have three advantages: (1) it has a zero voltage switching (ZVS) turn-on, which can significantly reduce switching losses and voltage spike of the main switches; (2) Compared to the conventional buck converter, it only needed one extra coupling inductor, a ground reference active switch, and a capacitor with low capacitance; (3) it can be driven by the existing buck control IC. In this paper,
an efficiency improvement method is presented to improve the conversion efficiency and finally complete a prototype circuit for verification.

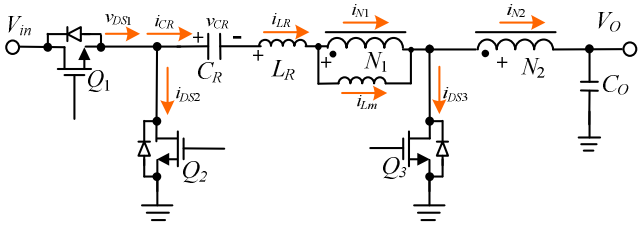


Fig. 1. The proposed negative output high-step-down converter.

II. PROPOSED CIRCUIT CONFIGURATION

There are 8 operation states in the proposed circuit, which are explained in Figs. 2(a) to 2(h). The simulation waveforms are shown in Fig. 3.

State 1 [$t_0 \sim t_1$]: As shown in Fig. 2(a). Q_1 is turned on, but Q_2 and Q_3 remain off-state.
V_{in} charges C_R, and magnetize L_m by coupling windings N_1 and N_2 to raise i_{Lm} continuously. V_{in} transmits energy to the output terminal V_O through the coupling windings N_1 and N_2. At this time, v_{ds2} is equal to V_{in}.

$$v_{ds3} = V_O + (V_{in} - v_{CB} - V_O) \cdot \left(\frac{N_2}{N_1 + N_2} \right) \tag{1}$$

State 2 [$t_1 \sim t_2$]: As shown in Fig. 2(b), Q_1 is turned off. Q_2 and Q_3 still remain off-state. Additionally, i_{N2} flows through the body diode of Q_2. However, the body diode of Q_3 still has no forward biased current at this time.
State 3 [$t_2 \sim t_3$]**:** As shown in Fig. 2(c), Q_1 and Q_3 remain off-state. Q_2 is turned on. i_{N1} and i_{N2} flow continuously. i_{LR} is demagnetized and eventually drops to zero. The i_{ds3} raise from zero to turn the body diode of Q_3 on and cause v_{ds3} to zero. The circuit to enter the next state.
State 4 [$t_3 \sim t_4$]**:** As shown in Fig. 2(d), Q_1 remains off-state. Q_2 remains on-state. After a short period of time when v_{ds3} is discharged to zero, Q_3 is turned on to achieve ZVS turn-on with synchronous rectifier (SR), which improves the

conversion efficiency.

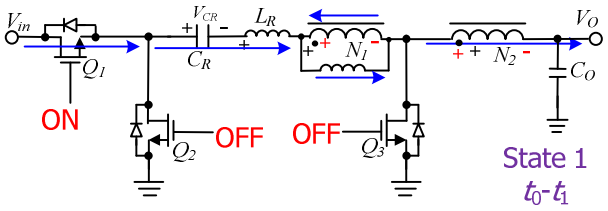
State 5 [t_4~ t_5]**:** As shown in Fig. 2(e), Q_1 remains off-state. Q_2 and Q_3 remain on-state. At this time, the storage energy in C_R magnetizes the winding N_1 reversely and transfer the energy to the N_2 winding to the output via N_1 in transformer mode, so the i_{N1} and i_{N2} currents increase.

$$v_{CB} = V_O \cdot \left(\frac{N_1}{N_2} \right) \tag{2}$$

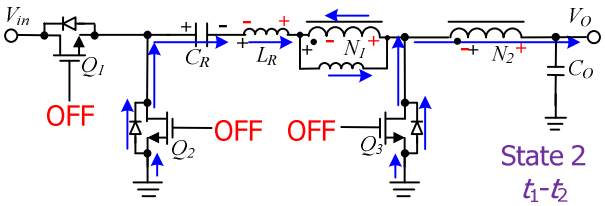
State 6 [t_5~ t_6]**:** As shown in Fig. 2(f), Q_1 remains off-state. Q_3 remains on-state. Q_2 is turned on. At this time, i_{N1} flows through the body diode of Q_1 to drop v_{ds1} to zero. Since Q_3 remains on-state, i_{N1} continues to flow through Q_3 for synchronous rectification.

State 7 [t_6~ t_7]**:** As shown in Fig. 2(g), Q_2 and Q_3 remain off-state. Q_1 is turned on. Although i_{N1} is still flowing through Q_3, it is safer to turn Q_3 off because Q_1 and Q_3 are still on-state at the same time. Turning Q_1 on at this time obtains ZVS turn-on. Although Q_1 is turned-on, i_{LR} is demagnetized continuously and the energy of L_R is sent back to V_{in} and gradually decreases.

State 8 [t_7~ t_0]**:** As shown in Fig. 2(h), Q_1 remains on-state. Q_2 and Q_3 remain off-state. V_{in} magnetizes N_1 and charges C_B. Due to L_R, i_{N1} is under i_{N2}, there is partial current flowing through Q_3. However, by this time, Q_3 is already cut off to make the body diode of Q_3 turned-on. When i_{N1} is equal to i_{N2}, the current no longer flows through the body diode of Q_3 and returns to State 1.



(a)



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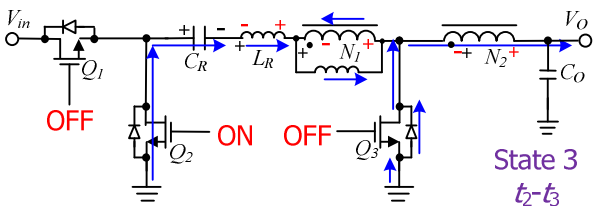
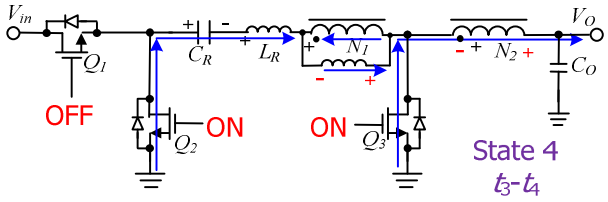


(c)



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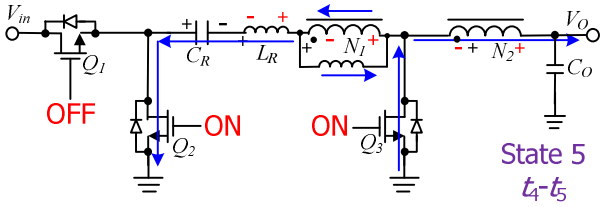

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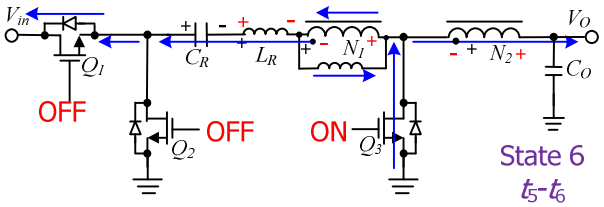
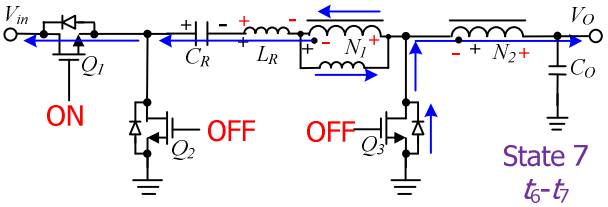
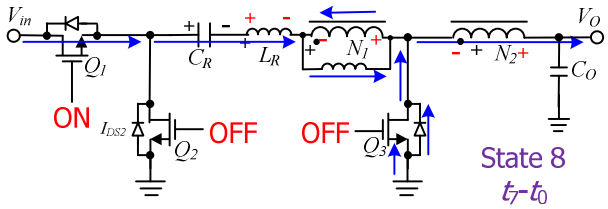


(f)



(g)



(h)

Fig. 3. Operation states of the proposed method: (a)state 1; (b)state 2; (c)state 3; (d)state 4; (e)state 5; (f)state 6; (g)state 7; (h)state 8.

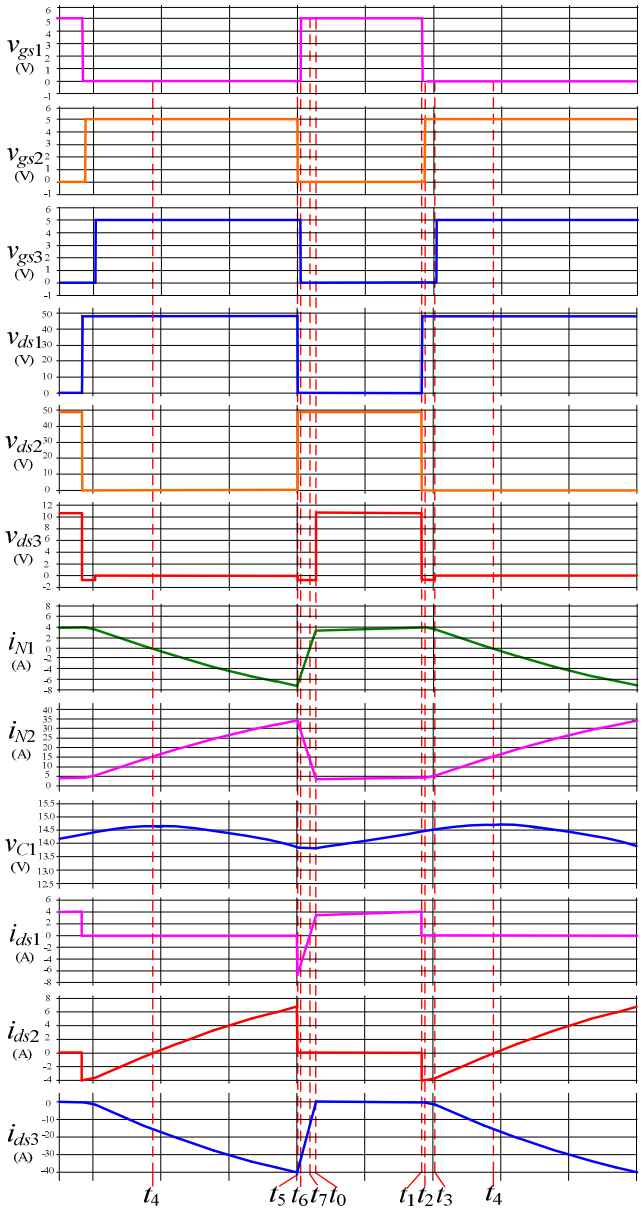


Fig. 3. Simulation waveforms of the proposed converter.

III. EXPERIMENTAL RESULTS

The specification of the prototype circuit is list as follow: the input voltage 48 V, output voltage 3.3 V, and rated output current 15 A. the switching frequency is 100 kHz. Table 1 shows the list of main components.

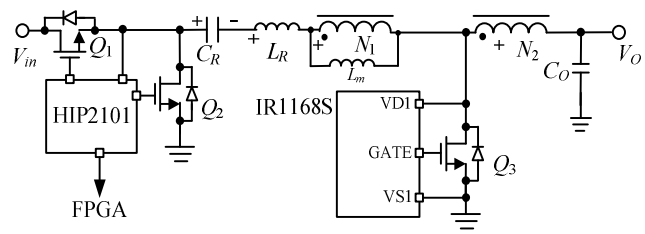
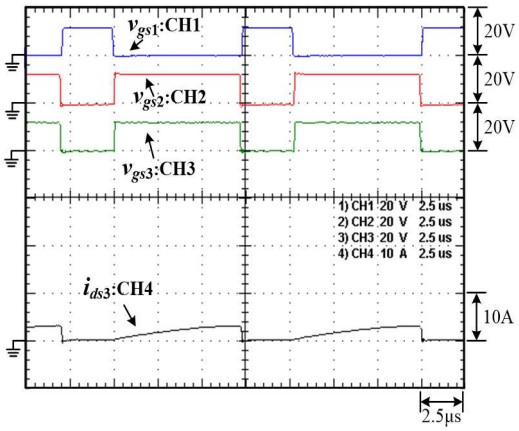


Fig. 4. Power stage of the proposed circuit.

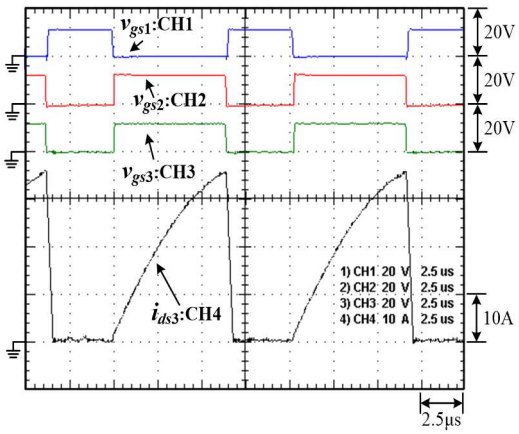
Table I. Key feature of main components.

Symbol	Part number/Key Feature	Manufacturer
Q_1, Q_2	AOT474(80 V/11.3 mΩ)	Alpha and Omega Semiconductor
Q_3	IRLR8113(30 V/6 mΩ)	Infineon AG
SR controller of Q_3	IR1168S	Infineon AG
C_B	parallel 2 × 10 μF (MLCC)	TDK
C_{in}	330 μF/63 V(E-cap)	NCC
C_o	parallel 3×470 μF /16V	NCC
L_1	T106-M125; N_1:N_2=24:8; L_m=41.13 μH, L_R=3.38 μH, A_L=157 nH/N^2	Micrometals
Driver of Q_1 and Q_2	HIP2101	Renesas

Fig. 5 shows the experimental waveforms of v_{gs1}, v_{gs2}, v_{gs3} and i_{ds3} of the traditional high step-down [16, 17] converter at different loads. Fig. 6 shows the rising edge waveforms of v_{gs1}, v_{gs2}, v_{gs3} and i_{ds3} of the traditional converter at different loads. It can be seen that v_{gs3} (equal to v_{gs2}) is driven synchronously. After v_{gs3} is turned-off, i_{ds3} still has a period of time to flow through Q_3, the more load current, the more i_{ds3} flows through the body diode of Q_3. In the traditional converter, Q_3 and Q_2 are controlled by FPGA for synchronous timing, so Q_3 and Q_2 have exactly the same rising timing as in Fig. 7. And since Q_2 must maintain a certain deadtime with Q_1 to avoid conduction of the same arm, the timing of Q_3 also passively follows that of Q_2.

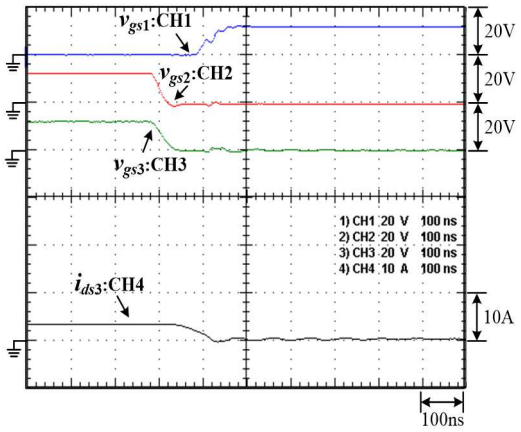


(a)



(b)

Fig. 5. Measured waveforms of v_{gs1}, v_{gs2}, v_{gs3}, and i_{ds3} of the previous method: (a) at 1.5 A; (b) at 15 A.



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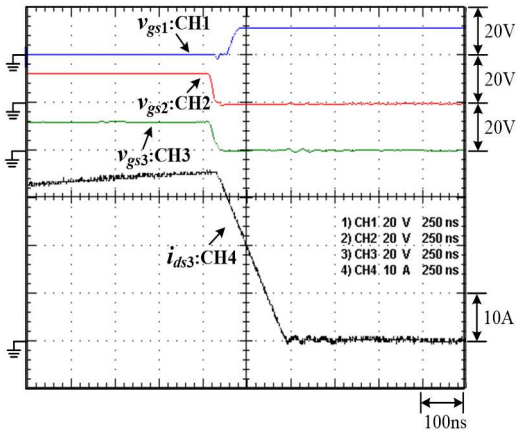
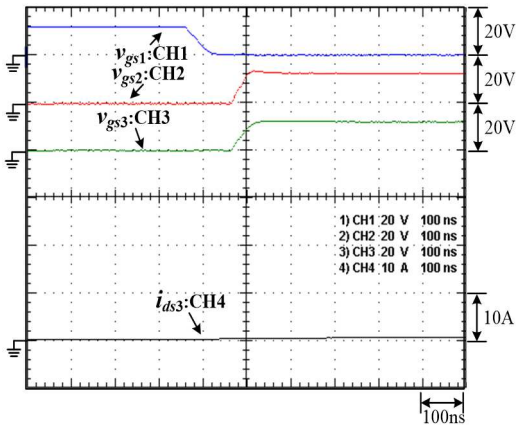
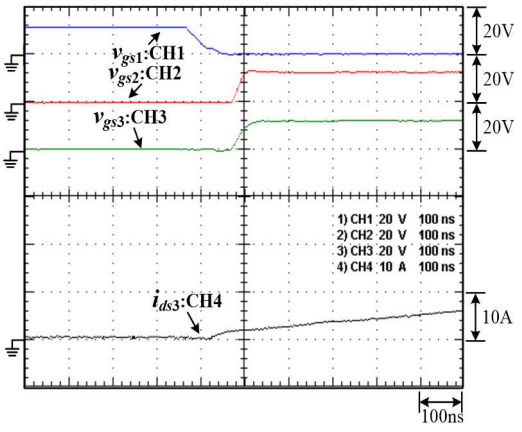


(b)

Fig. 6. Waveforms of v_{gs1}, v_{gs2}, v_{gs3}, and i_{ds3} at rising edge of previous method: (a) at 1.5 A; (b) at 15 A.



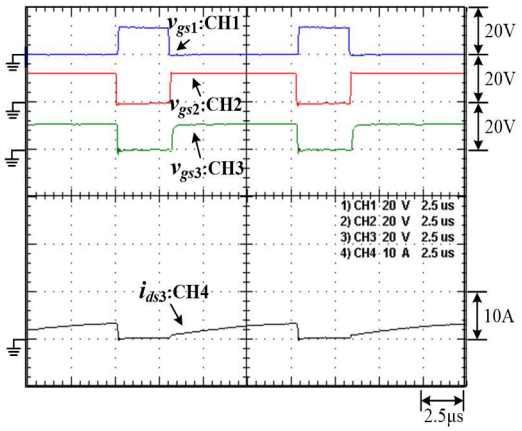
(a)



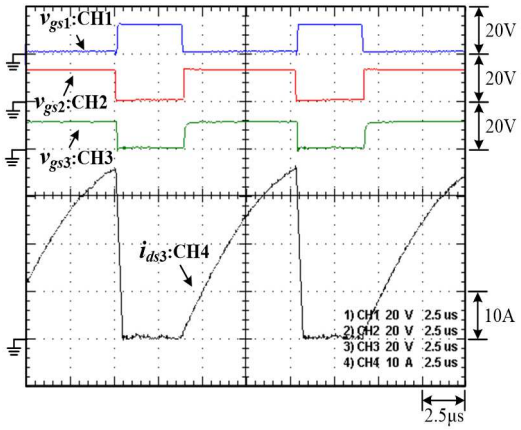
(b)

Fig. 7. Waveforms of v_{gs1}, v_{gs2}, v_{gs3}, and i_{ds3} at falling edge of previous method: (a) at 1.5 A; (b) at 15 A.

Fig. 8 shows the experimental waveforms of v_{gs1}, v_{gs2}, v_{gs3}, and i_{ds3} of the proposed method under different loads, while Fig. 9 shows the enlarged rising edge waveforms of v_{gs1}, v_{gs2}, v_{gs3}, and i_{ds3} under different loads. v_{gs2} and v_{gs3} are not driven synchronously, and Q_3 timing is controlled independently by IR1168S. After detecting that v_{ds3} is below the set threshold, the IR1168S turns off Q_3 to reduce the time for i_{ds3} to flow through the back-connected diode of Q_3 to enhance the conversion efficiency, which can be seen that Q_3 will be 100 ns slower than Q_2 before turning off. When Q_3 off-state in Fig. 9, it can be found that i_{ds3} flows through the body diode of Q_3, due to the turned-off threshold voltage is −6 mV. Although Q_3 is turned off earlier than expected to achieve the ideal synchronous rectification effect, it still significantly improves the conversion efficiency. In the proposed circuit, the SR controller IC detects that v_{ds3} is above the threshold voltage −140 mV on the body diode of Q_3, which will be turned on after a default delay of 60 to 120 ns. When the load increases, the turn-on time of Q_3 will gradually approach that of Q_2, as shown in Fig. 10.

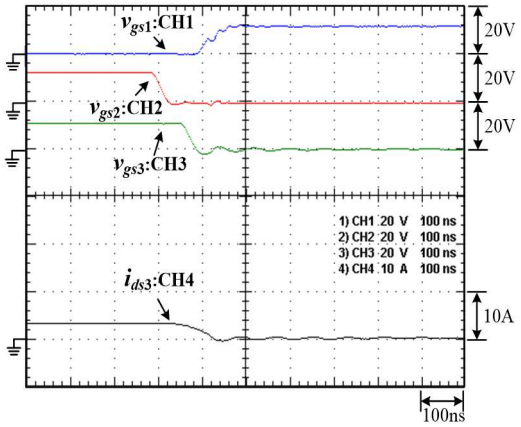


(a)

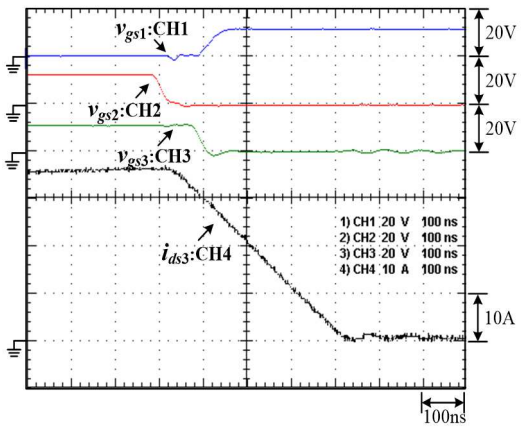


(b)

Fig. 8. Measured waveforms of v_{gs1}, v_{gs2}, v_{gs3}, and i_{ds3} of the proposed method: (a) at 1.5 A; (b) at 15 A.

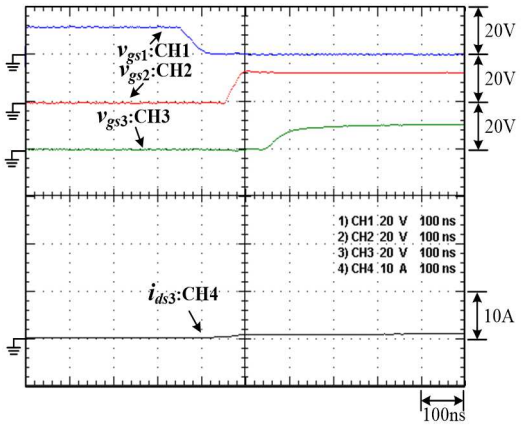


(a)

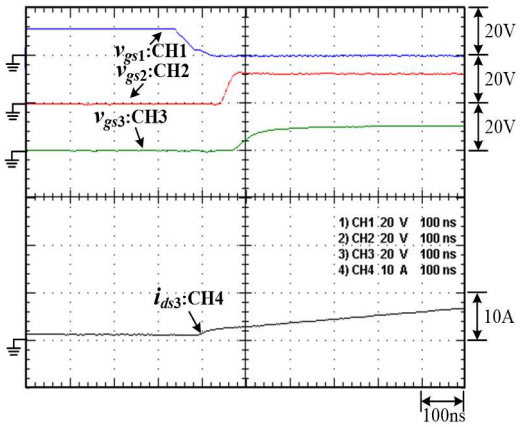


(b)

Fig. 9. Waveforms of v_{gs1}, v_{gs2}, v_{gs3}, and i_{ds3} at rising edge of previous method: (a) at 1.5 A; (b) at 15 A.



(a)



(b)

Fig. 10. Waveforms of v_{gs1}, v_{gs2}, v_{gs3}, and i_{ds3} at falling edge of proposed method: (a) at 1.5 A; (b) at 15 A.

Fig. 11 shows the measurement results of the conversion efficiency. Compared with the traditional method [16], the proposed method can improve the efficiency by 0.14%, 0.54%, and 2.5% at 20% load, 50% load, and full load, respectively, under an input voltage of 36 V. When the input voltage is 60 V, the proposed method can improve the efficiency by 0.1%, 0.35%, and 0.6% at 20% load, 50% load, and full load, respectively.

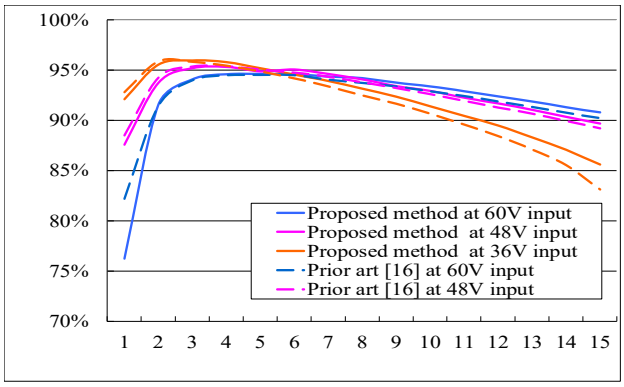


Fig. 11. Measured conversion efficiency.

IV. CONCLUSION

This paper presents an efficiency improvement method for a high step-down converter. The proposed control time sequence can optimize the usage of Q_3 to reduce the condition loss of body diode of Q_3. The proposed method can raise the conversion efficiency up to 2.5% at full load under the condition of a low input voltage without modification of the main power stage and additional cost.

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