

Response of IGBT chip characteristics due to critical stress

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Abstract

Focusing on the change in power semiconductor chip characteristics in response to mechanical stress applied to the chip, we confirmed the change of IGBT (Insulated Gate Bipolar Transistor) characteristics by bending test using a PCB (Printed Circuit Board) substrate to which an IGBT chip was mounted. The critical stress under which IGBT chip would fail was calculated by mechanical stress simulation, and the corresponding bending deformation was then applied to the PCB board and the characteristics of the IGBT chip has been investigated. Specifically gate capacitance has decreased after critical tensile stress loaded. By considering the stress direction of the each bending test and the structure of the IGBT chip, some hypothesis that can explain the mechanism of the characteristics change was suggested. As the next step, this hypothesis will be tested and the research regarding this chip characteristics change will be continued.

Keywords

«Condition Monitoring», «IGBT», «Lifetime», «Power semiconductor device», «Reliability».

Introduction

In an effort to realize a sustainable society, the electrification of automobiles is progressing based on the CO₂ reduction target. Especially the demand of power modules for traction inverter used in automobiles are growing at a phenomenal rate. As the size of power modules continue to shrink and become more multifunctional, the technologies of handling chips efficiently, lifetime diagnosis, and lifetime control are becoming more important [1-9]. Conventionally, it has been considered that the chip characteristics do not change if a local and direct mechanical load is applied to a chip itself [10-11]. However, since the situation has changed from the past in a trend that the chip become thinner and more multifunctional, the thin Si chip was investigated whether its characteristics would change with respect to the failure limit bending stress. Although IGBT chip is mounted in module for survey purpose, in this investigation IGBT chips is mounted on PCB board.

1. Experimental methods and modeling

1-1. Experimental model

Fig. 1 shows an IGBT mounted PCB board used for the experimental test. The PCB board is made of a high heat-resistant resin material that can cope with the soldering temperature, and its thickness is

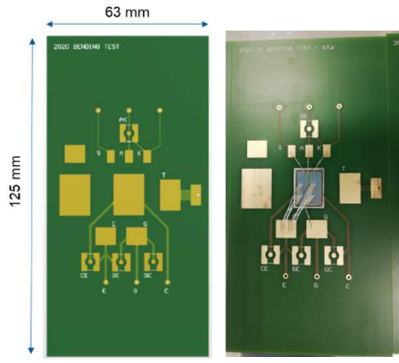


Fig. 1 PCB model and experimental sample.

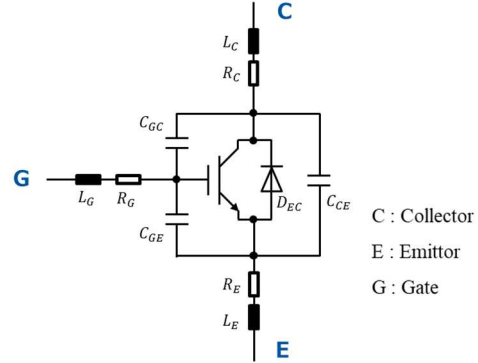


Fig. 2 Electrical model of RC-IGBT.

optimized according to the bending test deformation. The IGBT chips used in this samples are thin chips made of Si material and are soldered to the mounting board using lead-free high strength solder. The IGBT chip is in the center of the board. The gate, sense, and emitter wires are connected to the electrode pads on the PCB substrate by wire bonding. Metal pins are soldered to through holes in the substrate to provide external connections.

1-2. Chip characteristics analysis method

In this study, impedances have taken into account as a composite parameter to represent the characteristic changes in chip. Fig. 2 shows the electrical circuit model of the chip applied in this study. Since RC-IGBT (Reverse Conducting IGBT) chip, which is FWD is built in IGBT is used, a diode is built into the electrical circuit. The gate (G), collector (C) and emitter (E) are connected respectively on the impedance measurement and totally 6 impedances are measured with one module (G-E, E-G, G-C, C-G, C-E, E-C). After the bending test, impedances (analysis frequency from 100 Hz to 100 MHz) were measured using the impedance analyzer (Keysight 4294A) as shown in Fig. 3 and Fig. 4. The absolute and phase values of the impedance at each frequency are obtained by frequency analysis.

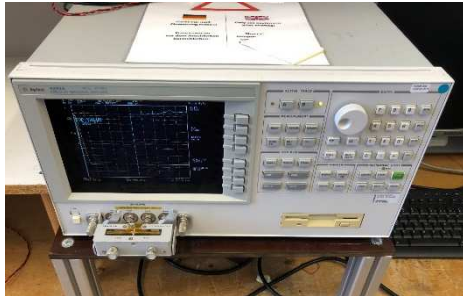


Fig. 3 Impedance analyzer (4294A).

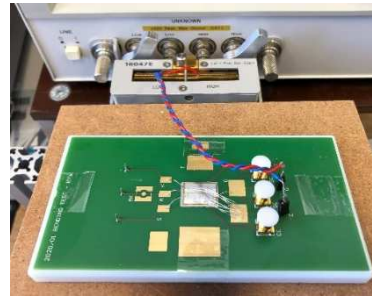


Fig. 4 Impedance measuring of experimental sample.

1-3. Chip characteristics comparing method

To analyze the chip characteristics in detail, various resistance and capacitance values inside the chip were extracted and each values were compared before and after the bending test. Since the impedance acquired by the impedance analyzer is calculated as a composite impedance value including the RLC values present in the electrical circuit, it is difficult to identify which RLC values have changed. Therefore, extraction calculations were carried out according to the flow shown in Fig. 5 and all the RLC values shown in Fig. 2 were extracted. The extraction process involves reworking the assumed electrical circuit into an equation showing the impedance for each connection, substituting appropriate values for each RLC values, comparing the calculated composite impedance with the measured impedance and performing an optimization calculation to make the difference smaller, thereby obtaining appropriate RLC values. As shown in Fig. 2, a total of 13 RLCs were used as variables (outputs), and six types of composite impedance (GE, EG, GC, CG, CE and EC) and 2 types of impedance data

(absolute and phase value) were used as 12 input data to represent in terms of entire impedance values. 12 impedance data were set as inputs and the impedance equations for each connection were set up by combining theoretical and experimental values. Some of the equations are shown in Equations (1) and (2), and the results of the optimization calculations are shown in Fig. 6. The dotted line shows the measured data and the solid line shows the data calculated by the optimization calculations. It was confirmed that the measured and optimized data matched well and that the circuit was set up appropriately.

$$Z_{GE} = \frac{1}{2\pi f j (C_{GE} + \frac{1}{\frac{1}{C_{GC}} + \frac{1}{C_{CE}}})} + (R_G + R_E) + 2\pi f j (L_G + L_E) \dots (1)$$

$$Z_{EG} = \frac{1}{2\pi f j (C_{EG} + \frac{1}{\frac{1}{C_{CG}} + \frac{1}{C_{EC} + 1/(2\pi f j * D_{EC})}})} + (R_G + R_E) + 2\pi f j (L_G + L_E) \dots (2)$$

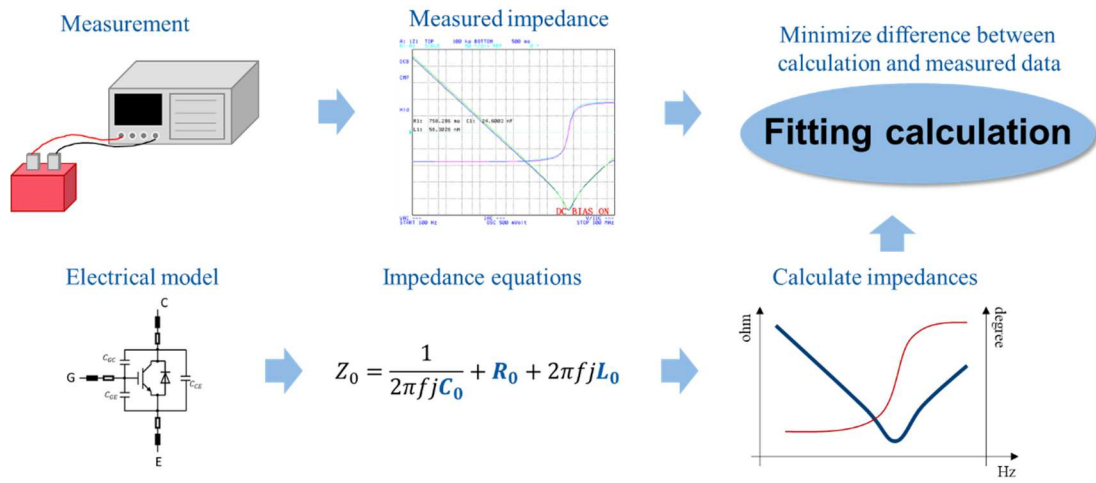


Fig. 5 RLC values extracting calculation flow. Comparing measured impedance data and calculated impedance based on the electrical model and equations.

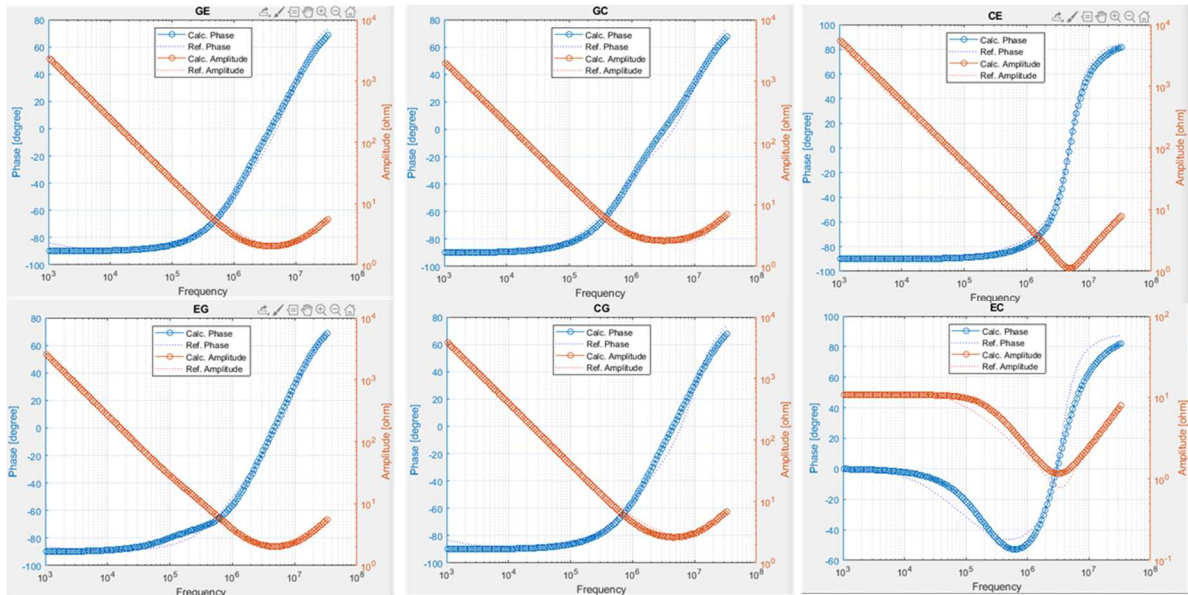


Fig. 6 Comparing measured impedance data and calculated impedance data by optimization calculation using GA with MATLAB.

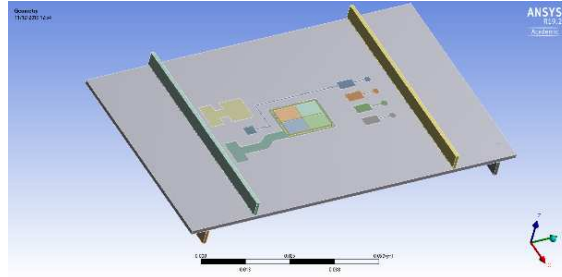


Fig. 7 Bending stress simulation model with detailed chip model.

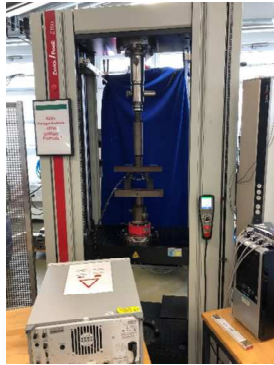


Fig. 8 Bending test equipment (Zwick/Roell Z150).



Fig. 9 A photograph taken during four point bending test.

1-4. Mechanical calculation model

Fig. 7 shows the model used for the bending stress simulation. Basically, the model reproduces the same shape as the experimental test sample shown in Fig. 1. One of the features of the model is that the electrodes and insulation structure of the chip are taken into consideration so that detailed stress changes inside the IGBT chip can be confirmed in response to bending stresses.

1-5. Bending test method

Fig. 2 shows the bending test equipment used for the bending tests. The compressive stress test by four point bending test is shown in Fig. 4, and the tensile stress test by three point bending test is performed with same equipment. After the bending test, impedances (analysis frequency from 100 Hz to 100 MHz) were measured using the impedance analyzer (Keysight 4294A).

2. Bending stress simulation result

Bending stress was calculated to obtain the correlation between the bending stress applied to the IGBT chip and the bending deformation of the entire PCB substrate. Fig. 10 shows the results of compressive stress simulation by four point bending test. There are four fulcrum points, which are in contact with the PCB substrate but they are not adhesive, in order to simulate the actual bending test by applying an appropriate amount of friction. The results of the three-point bending stress simulation are shown in Fig. 11. The required amount of deformation was obtained by increasing the amount of bending deformation until it reached the reference value of the chip failure. In the case of the three point bending test, the same simulation method was used to obtain the required amount of applied bending. Fig. 12 shows stress distribution of IGBT device and the other materials. This stress distribution confirmed that the Si layer of the IGBT chip can reaches to failure critical state.

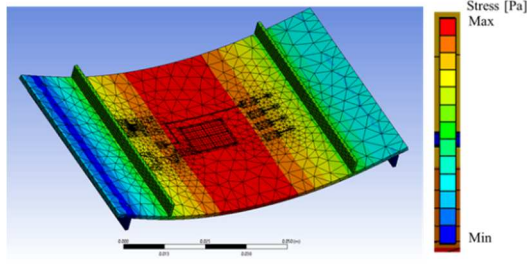


Fig. 10 Compressive stress simulation result of four point bending test.

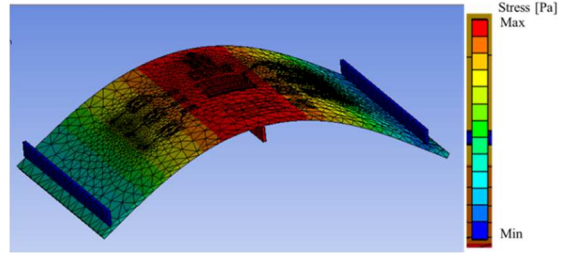


Fig. 11 Tensile stress simulation result of three point bending test.

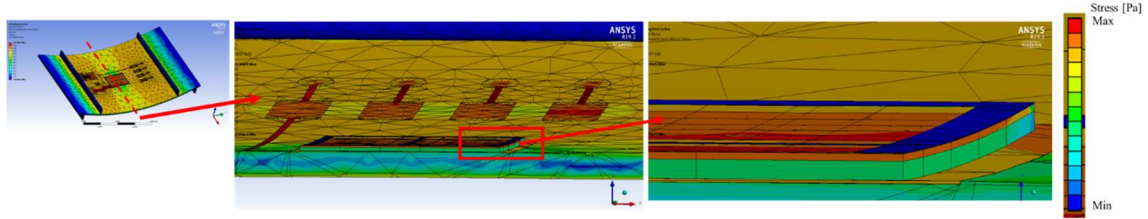


Fig. 12 Stress distribution in IGBT device under bending test deformation.

3. Experimental bending test result

3-1. Bending test result

Bending tests were carried out with the electromechanical tensile and compression testing machine (Zwick/Roell Z150), the specific attachment shown in Fig. 13. The bending test in progress is shown in Fig. 14. In order to verify that the applied bending deformation obtained from the bending stress simulation was appropriate, the simulated bending deformation which can provide critical stress against IGBT chip was loaded to the experimental sample and it was confirmed that the test sample has broken as shown in Fig. 15.

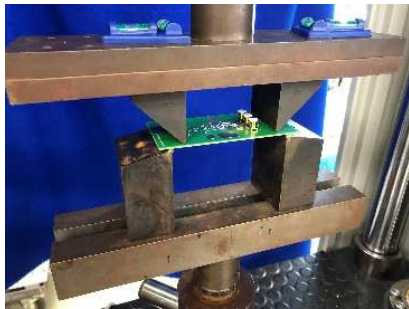
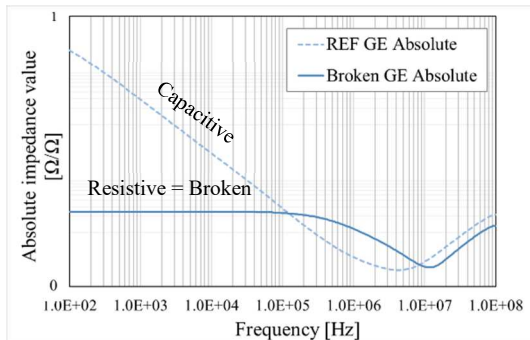


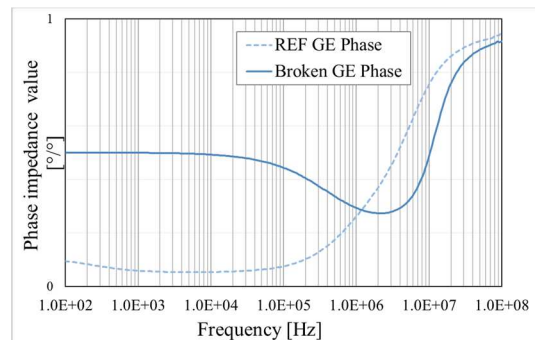
Fig. 13 Specific attachment for bending test.



Fig. 14 State under four point bending test.



(a) Absolute impedance value comparison.



(b) Phase impedance value comparison.

Fig. 15 Impedance value comparison normal status and broken status by bending test.

3-2. Measured impedance and RLC values comparison

Fig. 16 shows the absolute value and phase values of the frequency dependence impedance measured before and after the tensile bending test. Analysis samples are subjected to stress at the fracture limit and evaluated the status prior to complete fracture. Impedance was measured at 6 patterns according to electrical circuit diagram of Fig. 2. GE impedance measurement results show an increase in absolute impedance in the low-frequency range. The increase in impedance is expected to indicate a high possibility that the synthetic capacitance value is decreasing. No significant change was observed in other measured impedance results. Since this comparison does not show quantitatively how much the impedance changed, the resistance and capacitance values are extracted from the impedance curve and compared in Fig. 17 based on the RLC extraction calculation as explained at 1-3. Focusing on the gate resistance, it showed a slight increasing trend after compressive stress was applied, and a decreasing trend after tensile stress was applied. As for the gate capacitance value, it was almost unchanged after compressive stress was applied, but showed a decreasing trend after tensile stress was applied. From the above, it was confirmed that the chip characteristics changed after loaded critical stress.

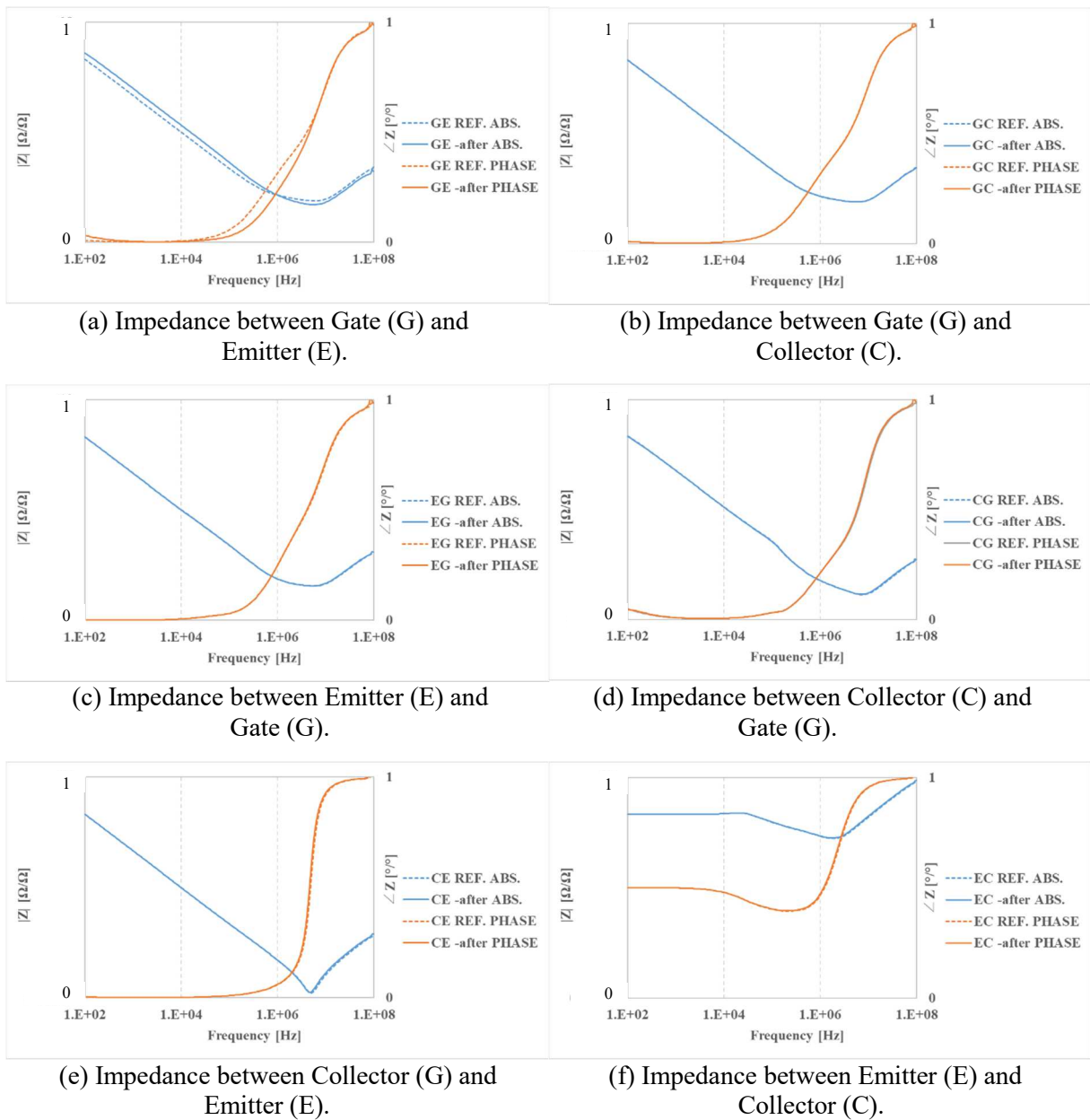
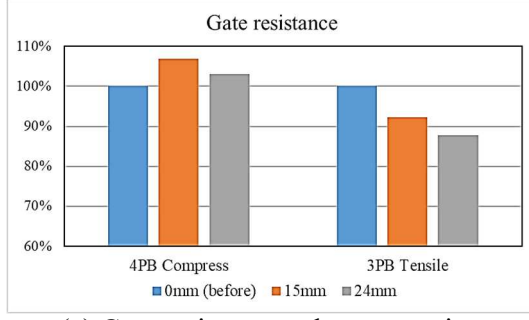
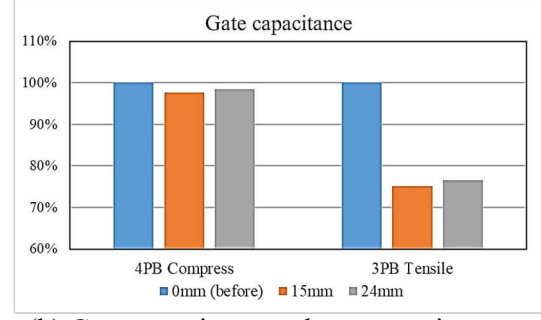


Fig. 16 Impedance values comparison before and after tensile stress loading at each connection of Gate, Collector and Emitter.



(a) Gate resistance value comparison.



(b) Gate capacitance value comparison.

Fig. 17 Gate resistance value comparison among bending deformation 0 mm (start), 15mm and 24 mm.

4. Discussion

In order to verify if this change was caused by something other than the chip, such as solder deformation or PCB deformation, the amount of warpage of the entire PCB board after the bending test was measured and verified. Fig. 18 shows a total 3D position of entire PCB and the center zone shows the area where IGBT chip is positioned, and measure deformation through the bending test. Few μm was measured as entire deformation but if the center area was focused, there was almost none deformation.

In addition to considering PCB deformation, ion concentration effect has investigated. Tested samples have passed through over 250 °C thermal process to dissipate ions inside of IGBT chip and impedance has measured and RC values have compared as shown in Fig 19. From the above discussion it was unlikely that the characteristics changed due to the influence of the other components.

The results of the change in resistance and capacitance values in response to compressive and tensile stresses are discussed in terms of the relationship between the structure of the IGBT chip and the physical properties. Fig. 13 shows the status of each stress loaded and the cross-sectional scheme of the IGBT with stress vectors. The formula for calculating the capacitance value is shown in Equation (3).

$$C = \epsilon \frac{A}{d} \cdot (3)$$

ϵ indicates the $\epsilon_0 \epsilon_r$ (relative permittivity) and d is the thickness of the insulate layer which also means the distance between electrodes, and A is the surface area. The situation of the IGBT trench while the compressive stress loading with the four point bending test is depicted using the cross-sectional view of the IGBT trench structure. When compressive stress is applied, each part is expected to shrink as it tends to compress. Therefore, the distance d tends to shorten and the surface area A tends to decrease, and the permittivity ϵ is expected to increase due to compression. On the other hand, when tensile stress is applied by the three point bending test, d and A tend to expand, and the permittivity is expected to decrease.

In addition, since the bending stress which is very critical for breakdown in the bending test was applied, it can be inferred that the permittivity tends to decrease more prominently. This is because slight degraded but almost broken parts can appear in the insulating layer before the complete failure. Furthermore the thickness and the surface area also can change if the IGBT structure has deformed. However, the cross section investigation of after bending test sample confirmed that the IGBT structure didn't change significantly.

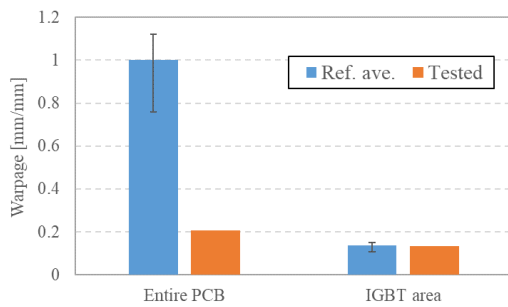


Fig. 18 Deformation of test samples before and after bending test.

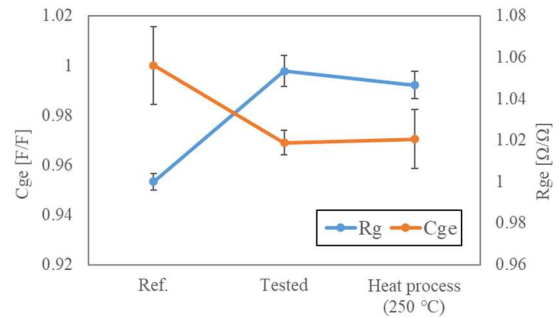
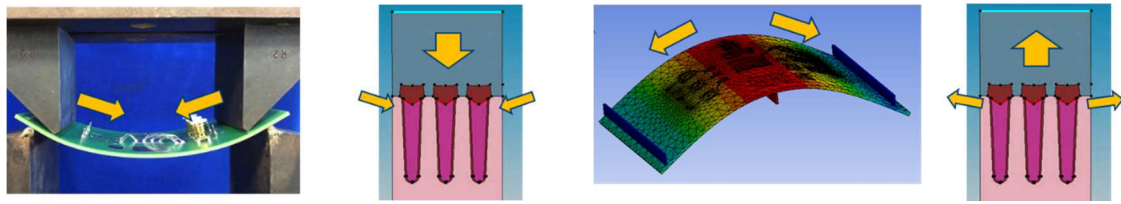


Fig. 19 Rg values trend through bending test and thermal process (250 °C).



(a) Compression stress loaded status.

(b) Tensile stress loaded status.

Fig. 20 Compression and tensile stress loading state by four and three point bending test with corresponding cross section of IGBT structure.

Conclusion

The chip characteristics under the state just before electrical breakdown were evaluated by applying critical mechanical stress, which is calculated by the bending stress simulation, to the experimental sample. No significant change was observed in the chip characteristics after compressive stress was applied by four point bending test, but the gate capacitance decreased after tensile stress was applied by three point bending test. Under tensile stress, capacitance decrease is considered as a result of relative permittivity decrease, since the IGBT chip has a possibility to introduce micro cracks in insulation layer under this critical stress. Based on the current findings in this paper, in order to develop a method to predict module lifetime, we will investigate characteristic changes under electrical stress during long-term reliability test at the next step.

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References

- [1] Gu B.: Condition monitoring of press-pack IGBT devices using Deformation Detection Approach, PEMD 2020
- [2] Colla E. L.: Characterisation of the fatigued state of ferroelectric PZT thin-film capacitors, *Microelectronic Engineering* 29, 1995, pp. 145-148
- [3] Timothy A.: Designing Power Modules for Degradation Sensing, ECCE 2019
- [4] van der Broeck C. H.: Monitoring 3-D Temperature Distributions and Device Losses in Power Electronics Modules, *IEEE transactions on Power Electronics* vol. 34, no. 8, pp. 7983-7995
- [5] Stippich A.: Significance of Thermal Cross-Coupling Effects in Power Semiconductor Modules, SPEC 2016
- [6] Baker N.: IGBT Junction Temperature Measurement via Peak Gate Current, *IEEE transactions on power electronics*, vol. 31, no. 5, pp. 3784-3793
- [7] Ye X.: Online Condition Monitoring of Power MOSFET Gate Oxide Degradation Based on Miller Platform Voltage, *IEEE transactions on power electronics*, vol. 32, no. 6, pp. 4776-4784
- [8] van der Broeck C. H.: In-situ Thermal Impedance Spectroscopy of Power Electronic Modules for Localized Degradation Identification, PCIM 2019
- [9] Kalker S.: Reviewing Thermal Monitoring Techniques for Smart Power Modules, *IEEE Journal of Emerging and Selected Topics in Power Electronics*
- [10] Tepper T.: Correlation between microstructure particle size dielectric constant and electrical resistivity of nano-size amorphous SiO₂ powder, *NanoStructured Materials* 1999, vol. 11, no. 8, pp. 1081-1089
- [11] Kahn H.: Mechanical fatigue of polysilicon: Effects of mean stress and stress amplitude, *Acta Materialia* 2006, vol. 54, pp. 667-678