An Optimized Compensation Strategy of Direct Matrix Converter-Fed PMSM Drives with Field Weakening under Unbalanced Supply Conditions

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Keywords

≪Direct matrix converter≫, ≪AC-AC converter≫, ≪Unbalanced AC grid≫, ≪Permanent magnet motor≫, ≪Field Oriented Control≫

Abstract

This paper presents an optimized compensation strategy for direct matrix converter (DMC) - fed permanent magnet synchronous motor (PMSM) drives with special consideration of the modification in field weakening control under unbalanced supply conditions. The imbalance of input voltage conditions in a three wire system are analysed and considered to be composed of positive and negative sequence components. To determine unbalance factor of the grid and decompose the positive and negative sequence components, the dual second order generalized integrator (DSOGI) and positive sequence calculator (PSC) algorithm are introduced. In order to achieve balanced output while optimizing the input current to be sinusoidal, the modulation index based on direct modulation method and the field weakening regulator are then adjusted according to unbalance factor of the input voltage conditions. The principle of the proposed compensation strategy is explained in detail. Simulation results are used to verify this proposed strategy. A low voltage laboratory platform consisting of DMC and servo motor is implemented and controlled using hybrid hardware concept based on field-programmable gate array (FPGA) and digital signal processor (DSP). Experimental studies on the laboratory prototype confirm the feasibility and effectiveness of the proposed method.

Introduction

The three-phase DMC is an alternative topology of direct AC-AC conversion without any bulky energy storage elements in an intermediate link [1,2]. This topology currently attracts many research interests in power electronics due to its compact size, bidirectional energy-flow capability and longtime durability, especially in adjustable speed drives applications.

On the other hand, because of the absence of DC-link energy storage components, the input and output sides of DMC are directly coupled. Any distortion, imbalance or voltage sag in input voltage conditions will reflect to the load side instantly, which results in harmonics in input currents and output voltages [3, 7]. Furthermore, as discussed in [7, 9, 10], the imbalance in input voltage conditions also reduces amplitude of the maximum achievable balanced output voltage, which is verified in the presented strategy as well.

Several methods have been proposed to mitigate the impact of unbalanced input voltage conditions under respective control strategies for DMC. In [3,4], the harmonic content in input current is analytically evaluated and minimised by controlling the input current displacement angle using direct space vector modulation (SVM) technique. In [7], the method with special consideration when desired output voltage greater than maximum attainable balanced output voltage is discussed, by means of solving optimization problems. In [8], a modified indirect SVM technique is used to determine the modulation index. However, the limitation of balanced output voltage is left undiscussed. In [5], a similar compensation strategy is proposed by using positive and negative sequence components of the input voltage under direct modulation technique. However, the method of how to decompose the positive and negative sequence components is not mentioned. In [6], a compensation method based on fuzzy logic control is discussed, which increases the complexity of calculating the modulation index.

In this paper, an optimized compensation strategy for DMC-fed PMSM drives with special consideration of the modification in field weakening control under unbalanced input voltage conditions is proposed. The modulation index m based on direct modulation method is determined by the desired modulation factor m_m and the compensation factor m_c. The desired modulation factor m_m is derived based on motor demands from the closed cascade control loops using field oriented control (FOC) method. The compensation factor m_c is calculated using amplitude of the instantaneous input voltages and the designed input phase displacement angle. Compared with previous research, the main features of the proposed strategy are as follows:

- It provides an optimized compensation method as a simple but practical solution to not only eliminate impact of unbalanced input voltages on output side of DMC, but also optimized the input current quality to be sinusoidal.
- It employs a method to decompose the measured instantaneous input voltage into positive and negative sequence components by introducing the algorithm of DSOGI with PSC, which are widely used in synchronisation of power systems [11–13].
- It dynamically adjusts the upper limit of the modulation factor m_m and the field weakening regulator according to unbalance factor of the input voltage conditions. While increasing the voltage transfer ratio under field weakening as much as possible, the modulation index m is ensured not to exceed the limitation of 1.

The rest of this paper is organized as follows. In section II, a brief introduction of the system topology together with the control scheme is presented. The proposed strategy is subsequently addressed in section III. Simulation results verifying the performance of the proposed strategy are demonstrated in section IV. In section V, experimental studies on the laboratory prototype confirm the feasibility and effectiveness of the proposed compensation method. Finally, this study is summarized in section VI.

System topology and control scheme

The system topology of three-phase to three-phase DMC-fed PMSM drives is shown in Fig. 1, which consists of power supply, input *LC* filter, DMC switching array, PMSM drive system and a protection circuit.

A. Topology of DMC

The DMC is composed of nine bidirectional switches (BDS) as a 3×3 matrix, which connects the grid to the PMSM drives. Each BDS should have the capability to block voltage and conduct current in both directions. There are many configurations for the realization [17]. One possibility could be two power semiconductor switches in back-to-back arrangement, which is shown in Fig. 1. The power semiconductor switch could be anti-parallel insulated gate bipolar transistor (IGBT) or metal–oxide–semiconductor field-effect transistor (MOSFET). The input *LC*-Filter is necessary to reduce high-frequency current harmonics and voltage fluctuation. It also removes the zero sequence component of the grid voltage. Many topologies of input filter for DMC have been proposed [15]. In this study, the damped *LC* filter is employed, in which the filter capacitor C_f is parallel with a *RC* damping circuit. It is worth noticing that, if the grid impedance $(R_N + jX_{L_N})$ can be precisely determined, it is possible to use grid inductance L_N

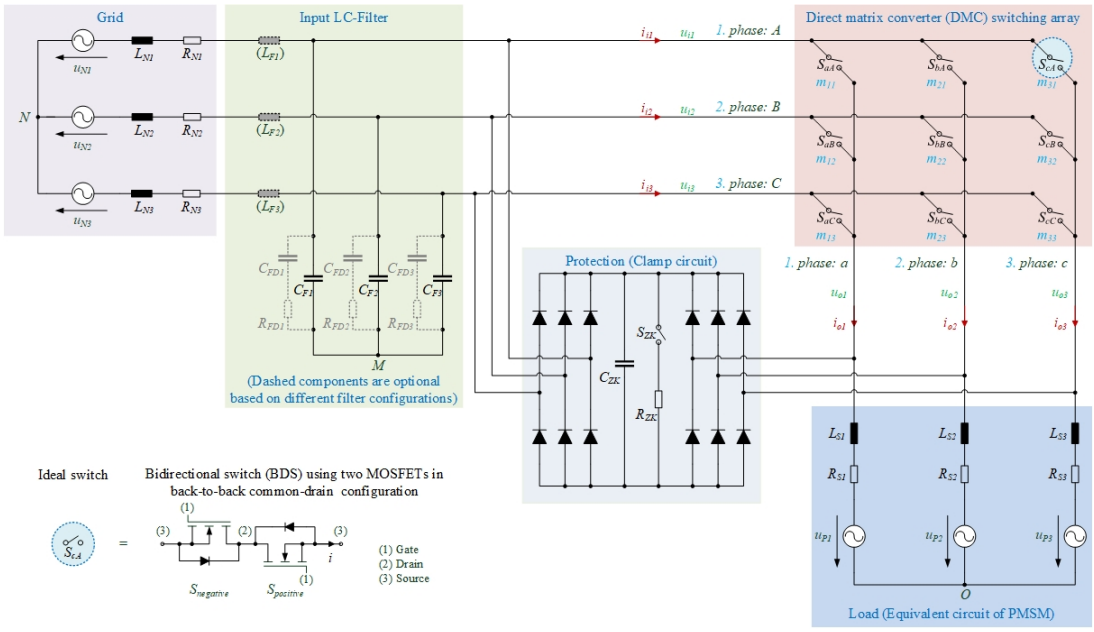

Fig. 1: System topology of three-phase to three-phase DMC-fed PMSM drives

instead of the normal filter inductance L_f within the permissible resonance frequency range. The output filter is commonly neglected due to the inductive nature of PMSM drive system. The clamping circuit is frequently implemented as an overvoltage protection circuit, which makes up the deficiencies of DMC for absence of passive free-wheeling paths [16]. It consists of 12 fast-recovery diodes and connects the input and output of DMC using double three-phase diode bridge (B6). The double B6 diode bridge are connected by a DC-link capacitor C_{ZK}, which is determined proportional to the energy stored in PMSM drives [16]. A switchable resistor R_{ZK} is typically in parallel to the DC-link capacitor to share the engergy and prevent overvoltage, which also allows to further reduce the size of the DC-link capacitor.

B. Model of PMSM drive system

Since no output filter is required, the motor voltages and currents are actually the output voltages $\vec{u}_o$ and currents $\vec{i}_o$ of DMC. The continuous-time model of the PMSM is given in dq-coordinate in (1):

$$\begin{cases} u_d = R_s i_d - \omega_e \cdot \psi_q + \frac{d\psi_d}{dt} \\ u_q = R_s i_q + \omega_e \cdot \psi_d + \frac{d\psi_q}{dt} \end{cases} \quad , \quad \begin{cases} \psi_d = L_d i_d + \psi_m \\ \psi_q = L_q i_q \end{cases} \tag{1}$$

The electromagnetic torque m_i and mechanical dynamics of PMSM can be estimated in (2):

$$m_i = \frac{3}{2} P_p (\psi_d i_q - \psi_q i_d) \quad , \quad m_i - m_l - m_r = \frac{1}{J} \frac{d\omega_m}{dt} \quad , \quad m_r = k_r \omega_m \quad , \quad \omega_e = P_p \cdot \omega_m \tag{2}$$

where u_d and u_q, i_d and i_q, ψ_d and ψ_q, L_d and L_q represent stator voltages $\vec{u}_o$, stator currents $\vec{i}_o$, magnet flux and stator inductance in dq-coordinate, respectively; ψ_m represents the magnet flux linkage of PMSM; R_s is the resistance of stator; P_p is the number of pole pairs; J is the moment of inertia; ω_e and ω_m are the electrical and mechanical angular frequency of PMSM, respectively; m_l is the load moment and m_r is the frictional moment, which is proportional to the mechanische angular frequency with the friction coefficient k_r.

C. Decompose positive and negative sequence components using DSOGI-PSC algorithm

To obtain the positive and negative sequence components under unbalanced input voltage conditions, the DSOGI-PSC algorithm is introduced. This strategy is presented in [14, 18] in detail and the main content is summarized as follows with slight modifications.

The DSOGI-PSC algorithm requires two components in quadrature. To achieve this, Clark transforma-

tion is used to transfer the input voltage $\vec{u}_{i,abc}$ to αβ-coordinate $\vec{u}_{i,\alpha\beta}$. For each voltage component $u_{i,\alpha}$ and $u_{i,\beta}$, a single SOGI structure is employed, which leads to the output voltage signals $u'_{i,\alpha}$ and $u'_{i,\beta}$. The transfer function of voltage $u'_{i,\alpha\beta}$ to $u_{i,\alpha\beta}$ is described in (3) as $D(s)$, which corresponds to a band-pass filter (BPF). The voltage signals $u'_{i,\alpha\beta}$ are then lagged by 90°, which are described as $q \cdot u'_{i,\alpha}$ and $q \cdot u'_{i,\beta}$, where q is $e^{-j(\pi/2)}$. In this way, a pair of quadrature signals $u'_{i,\alpha\beta}$ and $q \cdot u'_{i,\alpha\beta}$ are formed. The transfer function of voltage $q \cdot u'_{i,\alpha\beta}$ to $u_{i,\alpha\beta}$ is described in (3) as $Q(s)$, which corresponds to a low-pass filter (LPF).

$$D(s) = \frac{u'_{i,\alpha\beta}}{u_{i,\alpha\beta}}(s) = \frac{k\omega' s}{s^2 + k\omega' s + \omega'^2} \quad , \quad Q(s) = \frac{q \cdot u'_{i,\alpha\beta}}{u_{i,\alpha\beta}}(s) = \frac{k\omega'^2}{s^2 + k\omega' s + \omega'^2} \tag{3}$$

where ω' is the angular frequency of input voltage, which is estimated from the synchronous reference frame (SRF) phase locked loop (PLL) structure and k is the gain factor of SOGI. The quadrature signals $u'_{i,\alpha\beta}$ and $q \cdot u'_{i,\alpha\beta}$ are then decomposed into positive $u_{p,\alpha\beta}$ and negative $u_{n,\alpha\beta}$ sequence components in the PSC structure, which is expressed in (4).

$$\begin{bmatrix} u_{p,\alpha} \\ u_{p,\beta} \\ u_{n,\alpha} \\ u_{n,\beta} \end{bmatrix} = \frac{1}{2} \begin{bmatrix} 1 & -q \\ q & 1 \\ 1 & q \\ -q & 1 \end{bmatrix} \cdot \begin{bmatrix} u'_{i,\alpha} \\ u'_{i,\beta} \end{bmatrix} \quad , \quad q = e^{-j(\pi/2)} \quad , \quad \begin{bmatrix} u_{i,\alpha} \\ u_{i,\beta} \end{bmatrix} = \begin{bmatrix} u_{p,\alpha} \\ u_{p,\beta} \end{bmatrix} + \begin{bmatrix} u_{n,\alpha} \\ u_{n,\beta} \end{bmatrix} \tag{4}$$

The block diagram of DSOGI-PSC-SRF-PLL is shown in Fig. 2:

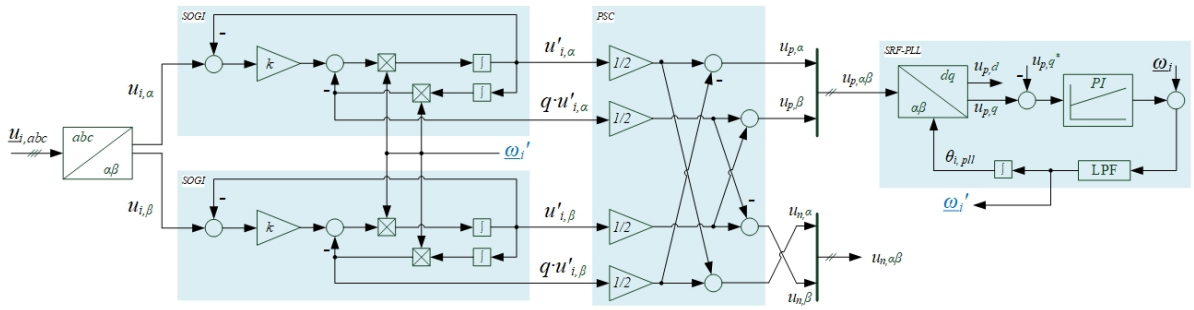

Fig. 2: Block diagram of the DSOGI-PSC-SRF-PLL algorithm [14, 18]

Proposed control strategy

The control scheme for the DMC-fed PMSM drive system with field weakening control is shown in Fig. 3. The PMSM drive system is controlled based on FOC algorithm in closed cascade control loops. The DMC is controlled using direct modulation strategy, namely the optimized Venturini's method, because of its convenience and straightforward of understanding the basics of DMC.

In outer loop, the motor speed n is estimated and regulated by proportional-integral (PI) controller. The output of speed controller is the reference value of torque producing current i_q^*. In inner loop, the magnetizing current i_d^* is set to zero before field weakening and is set to be negative during field weakening in order to further increase the motor speed. In the mean while, as the magnetizing current i_d^* increases, the reference value of torque producing current i_q^* is restricted by the maximum load current I_{max} in (5).

$$|i_q^*| \leq \sqrt{(I_{max})^2 - (i_d^*)^2} \quad , \quad {u_d}^2 + {u_q}^2 \leq \hat{U}_{o,max}^2 \tag{5}$$

Suppose the positive $\vec{u}_{i,p}$, negative $\vec{u}_{i,n}$ sequence components of the input voltages and the unbalance

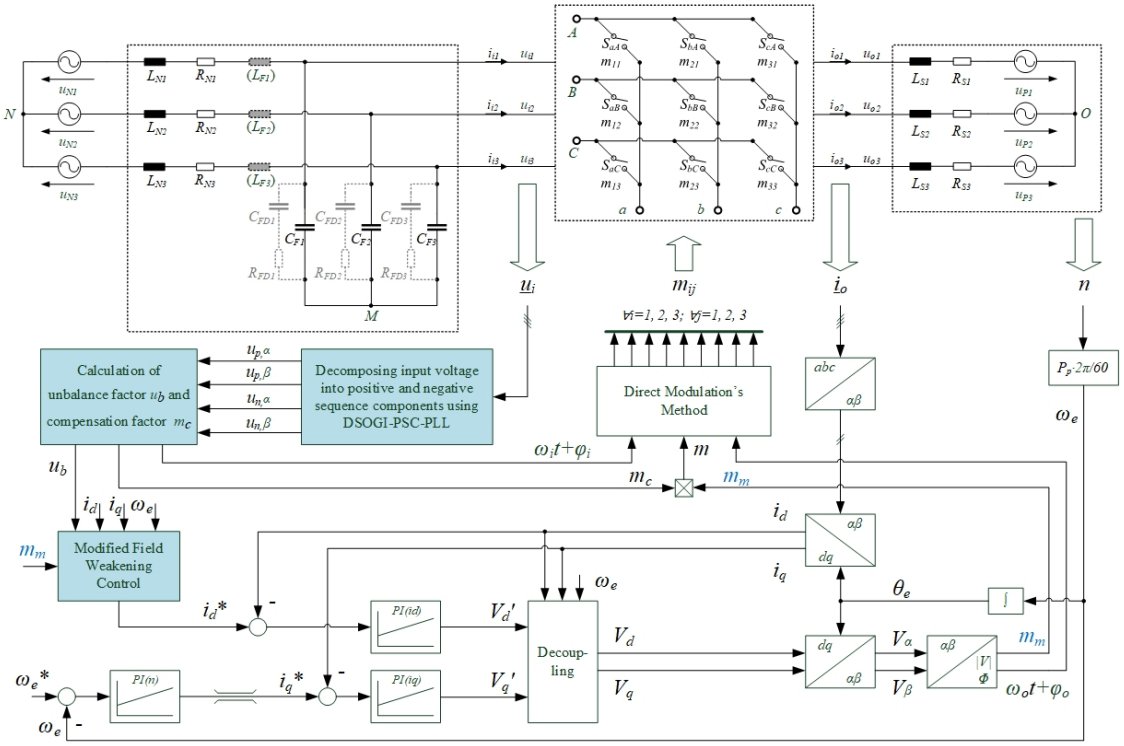

Fig. 3: Control scheme of DMC-fed PMSM drive system with field weakening

faktor u_b are defined in (6):

$$\vec{u}_{i,p} = \begin{bmatrix} \hat{U}_p cos(\omega_i t + \phi_p) \\ \hat{U}_p cos(\omega_i t - \frac{2\pi}{3} + \phi_p) \\ \hat{U}_p cos(\omega_i t + \frac{2\pi}{3} + \phi_p) \end{bmatrix} \quad , \quad \vec{u}_{i,n} = \begin{bmatrix} \hat{U}_n cos(\omega_i t + \phi_n) \\ \hat{U}_n cos(\omega_i t + \frac{2\pi}{3} + \phi_n) \\ \hat{U}_n cos(\omega_i t - \frac{2\pi}{3} + \phi_n) \end{bmatrix} \quad , \quad u_b = \frac{\hat{U}_n}{\hat{U}_p} \tag{6}$$

where ω_i is the angular frequency of input voltage, $\hat{U}_p$ and $\hat{U}_n$ are the amplitude of positive and negative sequence components of input voltage. ϕ_p and ϕ_n are the phase displacement angle of the positive and negative sequence components respectively.

The unbalanced input voltage $\vec{u}_i$ is considered to be sum of positive and negative sequence components as described in (7) using Fortescue's theorem. The zero sequence component is neglected in a three wire system.

$$\vec{u}_i = \vec{u}_{i,p} + \vec{u}_{i,n} = \begin{bmatrix} \hat{U}_p cos(\omega_i t + \phi_p) \\ \hat{U}_p cos(\omega_i t - \frac{2\pi}{3} + \phi_p) \\ \hat{U}_p cos(\omega_i t + \frac{2\pi}{3} + \phi_p) \end{bmatrix} + \begin{bmatrix} \hat{U}_n cos(\omega_i t + \phi_n) \\ \hat{U}_n cos(\omega_i t + \frac{2\pi}{3} + \phi_n) \\ \hat{U}_n cos(\omega_i t - \frac{2\pi}{3} + \phi_n) \end{bmatrix} \tag{7}$$

The amplitude $\hat{U}_i$ of input voltage $\vec{u}_i$ can be expressed using instantaneous input voltages after Clarke and Cartesian-Polar transformation, which can be further described using $\vec{u}_{i,p}$ and $\vec{u}_{i,n}$ as shown in (8).

$$\hat{U}_i = \sqrt{\frac{2}{3}(u_{i1}^2 + u_{i2}^2 + u_{i3}^2)} = \sqrt{\hat{U}_p^2 + \hat{U}_n^2 + 2\hat{U}_p\hat{U}_n cos(2\omega_i t + \phi_p + \phi_n)} \tag{8}$$

The phase angle θ_{ui} of input voltage $\vec{u}_i$ is shown in (9):

$$\theta_{ui} = tan^{-1}\left(\frac{\hat{U}_p sin(\omega_i t + \phi_p) - \hat{U}_n sin(\omega_i t + \phi_n)}{\hat{U}_p cos(\omega_i t + \phi_p) + \hat{U}_n cos(\omega_i t + \phi_n)}\right) \tag{9}$$

In average value model of DMC, the instantaneous output voltage $\underline{u}_o$ can be expressed as (10):

$$\underline{u}_o = \hat{U}_o e^{j\omega_o t} = \hat{U}_i \cdot \frac{\sqrt{3}}{2} \cdot m \cdot cos(\phi_i) e^{j\omega_o t} \quad , \quad 0 \leq m \leq 1 \tag{10}$$

where ω_o is the angular frequency of output voltage, $cos(\phi_i)$ is the input power factor with ϕ_i the input phase displacement angle, $m = \frac{q}{\sqrt{3}/2}$ is the modulation index with a range from 0 to 1 and q the corresponding voltage transfer ratio between output and input side of DMC. Introducing (8) in (10), leads to the following equation (11):

$$\underline{u}_o = \sqrt{\hat{U}_p^2 + \hat{U}_n^2 + 2\hat{U}_p\hat{U}_n cos(2\omega_i t + \phi_p + \phi_n)} \cdot \frac{\sqrt{3}}{2} \cdot m \cdot cos(\phi_i) e^{j\omega_o t} \tag{11}$$

Equation (11) shows, under unbalanced input voltage conditions, the amplitude of the input voltage $\hat{U}_i$ oscillates with twice the input frequency due to presence of the negative sequence component $u_{i,n}$, which results in harmonics to the output side of DMC.

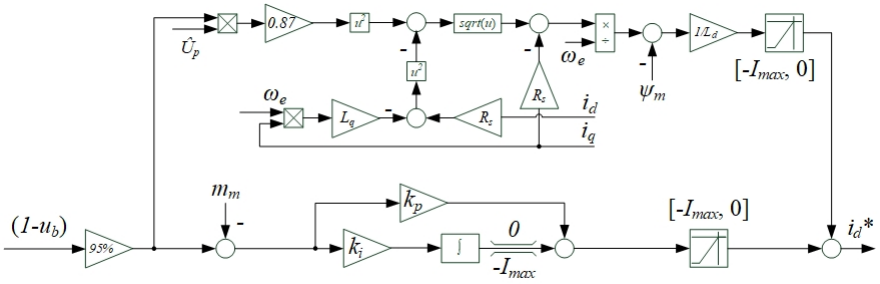

Fig. 4: Block diagram of the modified field weakening control

In order to eliminate the oscillation in the output of DMC, the simplest method is to modify the modulation index m through two factors m_m and m_c in such a way that:

- the modulation factor m_m keeps the modulation depth according to the desired motor demands.
- the compensation factor m_c compensates the oscillation of input voltage amplitude $\hat{U}_i$ while keeping the positive sequence component $u_{i,p}$ as maximal achievable balanced output voltage.
- the input phase displacement angle ϕ_i is determined to be the phase angle of voltage $(u_{i,p} - u_{i,n})$, so that the amplitude of input current oscillates exactly in the opposite direction of input voltage, meanwhile keeps the input power factor $cos(\phi_i)$ to be unity every time when amplitude of input voltage reaches $(\hat{U}_p + \hat{U}_n)$ or $(\hat{U}_p - \hat{U}_n)$ and ensures the input current to be sinusoidal.
- the input power factor $cos(\phi_i)$ is then divided in compensation factor m_c to eliminate the oscillation and keep the amplitude of output voltage relative constant.

To achieve this, the modulation index m is expressed in (12):

$$m = m_m \cdot m_c = m_m \cdot \left(\frac{\hat{U}_p}{\sqrt{\hat{U}_p^2 + \hat{U}_n^2 + 2\hat{U}_p\hat{U}_n cos(2\omega_i t + \phi_p + \phi_n)}} \cdot \frac{1}{cos(\phi_i)} \right) \leq 1 \tag{12}$$

Since the modulation index m can't exceed 1, which is the intrinsic limitation, the range of the compensation factor m_c is $[\frac{\hat{U}_p}{\hat{U}_p+\hat{U}_n}, \frac{\hat{U}_p}{\hat{U}_p-\hat{U}_n}]$ or $[\frac{1}{1+u_b}, \frac{1}{1-u_b}]$. Thus, m_m should be smaller than the minimal value of $\frac{1}{m_c}$, which is $(1-u_b)$.

Introducing (12) in (11), the equivalent equation of balanced output voltage of DMC can be expressed in (13).

$$\underline{u}_o = \hat{U}_p \frac{\sqrt{3}}{2} \cdot m_m \, e^{j\omega_o t} \quad , \quad 0 \leq m_m \leq (1-u_b) \tag{13}$$

Equation (13) shows that under unbalanced input voltage conditions, the balanced output voltage can be achieved using the proposed compensation strategy, but the maximal modulation depth is reduced to $(1-u_b)$, compared with 1 under balanced supply conditions. The amplitude of maximal output voltage $\hat{U}_{o,max}$ is then $\frac{\sqrt{3}}{2}\hat{U}_p(1-u_b)$ or $\frac{\sqrt{3}}{2}(\hat{U}_p-\hat{U}_n)$.

Because the maximal achievable balanced output voltage is reduced, the field weakening control of PMSM drive system needs to be adjusted as well in order to get rid of any over modulation according to the reduced maximal modulation depth.

The block diagram of a modified field weakening control with feedforward is described in Fig. 4. The field weakening control is based on PI controller. A feedforward loop is employed to help increase the dynamic response and determine the reference magnetizing current i_d^* as shown in (14), which is derived from model of PMSM as described in (1) together with the voltage limitation shown in (5).

$$i_d^* = \frac{1}{L_d}\left(\frac{\sqrt{\left(\frac{\sqrt{3}}{2}\hat{U}_p(1-u_b)\right)^2-(R_s i_d-\omega_e L_q i_q)^2}-R_s i_q}{\omega_e}-\psi_m\right) \tag{14}$$

In the block diagram, the gain of 95% is determined from experience for ensurance of the controllability.

Simulation results

Simulation results in Fig. 5 are used to verify the effectiveness of the proposed method using MATLAB. The parameters of the system are shown in Table I.

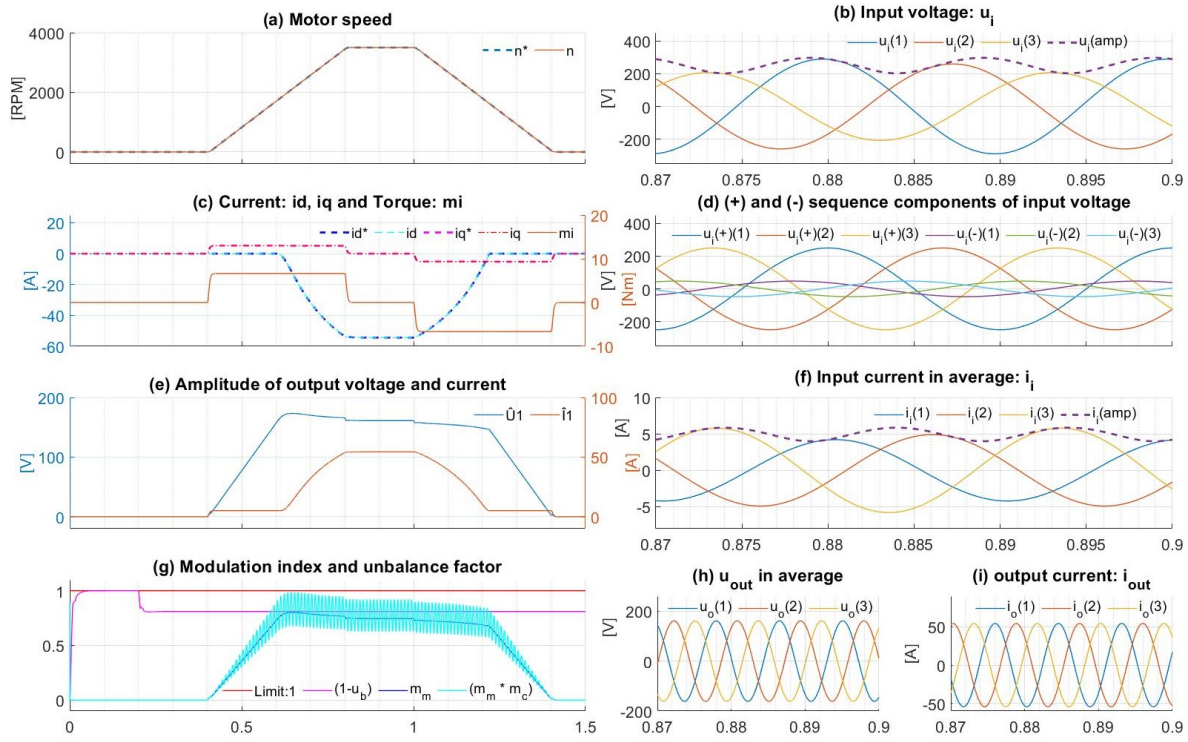

Fig. 5: Simulation results: (a) Motor speed. (b) Input Voltages. (c) Output currents in dq-Coordinate and the Torque. (d) Estimated positive and negative sequence components. (e) Amplitude of output voltage and current. (f) Input Current in average. (g) Modulation index and unbalance factor. (h) Output voltage in average. (i) Output current.

Table I: System parameter in simulation

Symbol	Value	Symbol	Value
$U_{N0,RMS}$	$230V$	f_N	$50Hz$
P_p	2	L_d, L_q	$4mH$
R_s	0.4Ω	J	$0.007kg \cdot m^2$
f_p	$20kHz$	I_{max}	$70A$
ψ_m	$0.4V/(rad \cdot s^{-1})$	k	$\sqrt{2}$

In the simulation, the imbalanced grid voltages $\vec{u}_{N,imbalanced}$ are defined in (15):

$$\vec{u}_{N,imbalanced} = \begin{bmatrix} 230\sqrt{2}\ cos(100\pi t) \\ 230\sqrt{2} \cdot 80\%\ cos(100\pi t - \frac{2\pi}{3}) \\ 230\sqrt{2} \cdot 50\%\ cos(100\pi t + \frac{2\pi}{3}) \end{bmatrix} \tag{15}$$

Through input *LC*-Filter, the zero sequence component of the grid voltage is removed. The input voltages of DMC are then the sum of positive and negative sequence components as shown in (16).

$$\vec{u}_{N,imbalanced} - \frac{1}{3}\sum(u_{N1} + u_{N2} + u_{N3}) = \vec{u}_i = \vec{u}_{i,p} + \vec{u}_{i,n} \tag{16}$$

The input voltages $\vec{u}_i$ start to be unbalanced from $t = 0.2s$. It can be noticed in (g) that the upper limit of maximal available modulation depth m_m reduced from 1 to be $1 - u_b$. It takes in this simulation environment around $60ms$ for the DSOGI structure to estimate these positive and negative sequence components of input voltage ($\vec{u}_{i,p}$ and $\vec{u}_{i,n}$) based on the configuration set in DSOGI and the estimated result is shown in (d).

The oscillation of input voltage amplitude with doubled grid frequency is shown in (b). The quality of input current is optimized to be sinusoidal in (f) by adjusting the input phase displacement angle ϕ_i. By employing the proposed compensation factor m_c to desired modulation depth m_m, the total modulation index m is not exceeding the intrinsic limitation 1 of DMC as shown in (g) and the output voltage and current is balanced, which are shown in (h) and (i).

The PMSM drive is accelerated by $t = 0.5s$ from static state to be $3500RPM$. After keeping the maximal speed for short and then braked to be zero speed. The field weakening region starts by around $1795RPM$, where the magnetizing current i_d starts to be negative to further increase the motor speed. By employing the proposed field weakening control, the torque producing current i_q^* and motor torque keep relative constant as shown in (c).

Experimental results

A low voltage laboratory platform consisting of a DMC and a servo motor is implemented. A hybrid hardware architecture based on FPGA and DSP is employed to control the demonstrator and the experimental results are shown in Fig. 6 (a).

The unbalanced input voltages are generated by a three phase DC-link voltage source inverter (VSI) as shown in (b), which consists of a positive sequence modulator with $50Hz$ and a negative sequence modulator with frequency $-50Hz$.

The output voltages and currents are shown in (c) and (d) and are measured at the operation point of motor speed by $-500RPM$.

As can be seen in the measurement results, the output voltage and current are sinusoidal and balanced, which verified the effectiveness of the proposed compensation method.

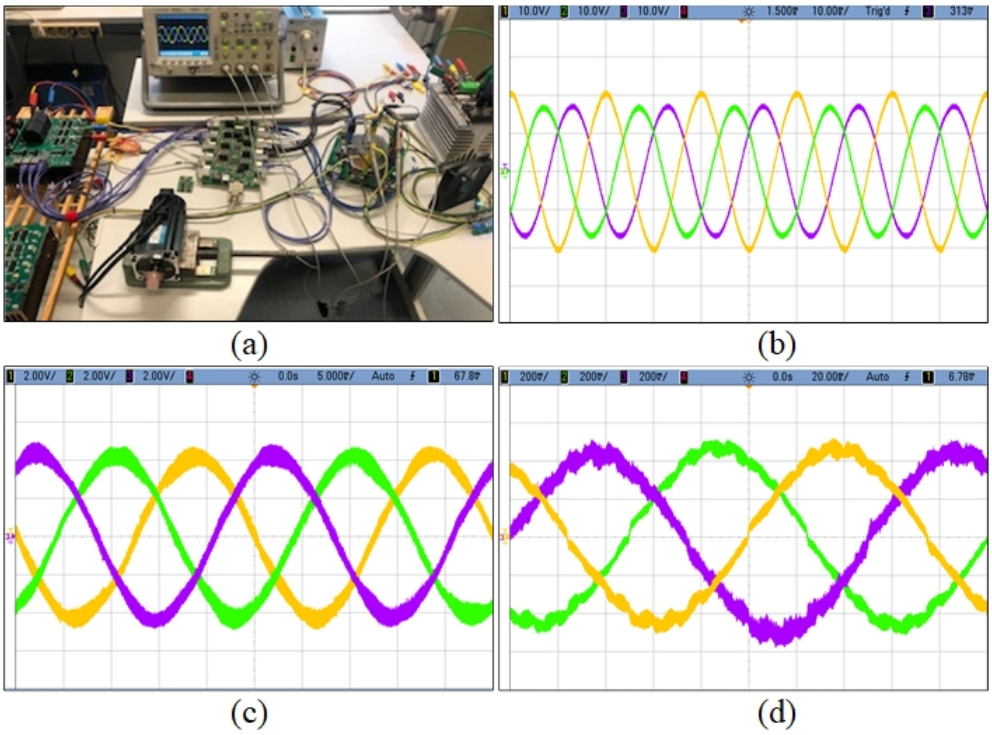

Fig. 6: (a) Demonstrator. (b) Unbalanced input voltage. (c) output voltage. (d) output current.

Conclusion

In this paper, an optimized compensation strategy for DMC-fed PMSM drives with special consideration of field weakening control under unbalanced input voltage conditions is presented. By employing the presented method, the impact of unbalanced input voltages is eliminated and the output voltages and currents are balanced. Meanwhile, the quality of input currents is optimized to be sinusoidal. The impacts on maximal achievable balanced output voltage and the upper limitation in field weakening regulator are discussed. Simulation and experiment results confirm the validity of the proposed strategy.

References

[1] Alesina, A. and Venturini, M.: Solid-state power conversion: A Fourier analysis approach to generalized transformer synthesis, IEEE Transactions on Circuits and Systems, Vol 28 no 4, pp. 319-330, 1981.

[2] Alesina, A. and Venturini, M.G.B.: Analysis and design of optimum-amplitude nine-switch direct AC-AC converters, IEEE Transactions on Power Electronics, Vol 4 no 1, pp. 101-112, 1989.

[3] Casadei, D. and Serra, G. and Tani, A.: A general approach for the analysis of the input power quality in matrix converters, IEEE Transactions on Power Electronics, Vol 13 no 5, pp. 882-891, 1998.

[4] Casadei, D. and Serra, G. and Tani, A.: Reduction of the input current harmonic content in matrix converters under input/output unbalance, IEEE Transactions on Industrial Electronics, Vol 45 no 3, pp. 401-411, 1998.

[5] Dastfan, A. and Haghshenas, M.: Design and Simulation of A Power Supply Based on A Matrix Converter Under Unbalanced Input Voltage, 41st IUPEC, Vol 2, pp. 569-573, 2006.

[6] Karaca, H. and Akkaya, R. and Dogan, H.: A novel compensation method based on fuzzy logic control for matrix converter under distorted input voltage conditions, 18th ICEM, pp. 1-5, 2008.

[7] Dasika, J. D. and Saeedifard, M.: A modulation strategy to control the Matrix Converter under unbalanced input voltage conditions, IEEE APEC, pp. 1556-1563, 2015.

[8] Patel, P. and Mulla, M. A.: Modified Space Vector Modulated Three-phase to Three-phase Matrix Converter Under Unbalanced Supply Conditions, 8th IICPE, pp. 1-6, 2018.

[9] Wei, L. and Matsushita, Y. and Lipo, T.A.: Investigation of dual-bridge matrix converter operating under unbalanced source voltages, IEEE PESC '03., Vol 3, pp. 1293-1298, 2003.

[10] Satish, T. and Mohapatra, K.K. and Mohan, N.: Modulation methods based on a novel carrier-based PWM scheme for matrix converter operation under unbalanced input voltages, APEC '06., pp. 127-132, 2006.

[11] Patil, K. R. and Patel, H. H.: Modified dual second-order generalised integrator FLL for synchronization of a distributed generator to a weak grid, EEEIC '16., pp. 1-5, 2016.

[12] Zhang, C. and Føyen, S. and Suul, J. A. and Molinas, M.: Modeling and Analysis of SOGI-PLL/FLL-Based Synchronization Units: Stability Impacts of Different Frequency-Feedback Paths, IEEE Transactions on Energy Conversion, Vol 36 no 3, pp. 2047-2058, 2021.
[13] R. Izah and S. Subiyanto and D. Prastiyanto: Improvement of DSOGI PLL Synchronization Algorithm with Filter on Three-Phase Grid-connected Photovoltaic System, Jurnal Elektronika dan Telekomunikasi, Vol 18 no 1, pp. 35-45, 2018.
[14] Q. Cheng and F. Tan and J. Gao and Y. Zhang and D. Yu: The separation of positive and negative sequence component based on SOGI and cascade DSC and its application at unbalanced PWM rectifier, IEEE 29th CCDC, pp. 5804-5808, 2017.
[15] She, Hongwu and Lin, Hua and Wang, Xingwei and Yue, Limin: Damped input filter design of matrix converter, PEDS, pp. 672-677, 2009.
[16] Costa, L. A. and Fan, B. and Burgos, R. and Boroyevich, D. and Chen, W. and Blasko, V.: The Fast Overvoltage Protection Consideration and Design for SiC-based Matrix Converters, APEC, pp. 1567-1574, 2020.
[17] Wheeler, P.W. and Rodriguez, J. and Clare, J.C. and Empringham, L. and Weinstein, A.: Matrix converters: a technology review, IEEE Transactions on Industrial Electronics, Vol 49 no 2, pp. 276-288, 2002.
[18] P. Rodríguez, A. Luna, R. S. Munoz-Aguilar, I. Etxeberria-Otadui, R. Teodorescu, and F. Blaabjerg: A stationary reference frame grid synchronization system for three-phase grid-connected power converters under adverse grid conditions, IEEE Transactions on Power Electronics, vol. 27, no. 1, pp. 99–112, 2012.