A Wide-Input-Voltage-Range 50W Series-Capacitor Buck Converter with Ancillary Voltage Bus for Fast Transient Response in 48V PoL Applications

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Keywords

≪Automotive applications≫, ≪DC-DC converter≫, ≪High frequency power converter≫, ≪Voltage Regulator Modules (VRM)≫, ≪Power converters for EV≫, ≪Multi-Level converters≫

Abstract

This paper presents an auxiliary-assisted 5:1 Series-Capacitor (SC) buck converter for fast transient response in 48V Point-of-Load (PoL) automotive applications. The 5:1 SC buck converter, which is implemented as the main hybrid stage, regulates the auxiliary buffer capacitor voltage, V_{AUX}, and consequently, delivers the average load power. By regulating V_{AUX}, the main hybrid stage facilitates the creation of an ancillary voltage bus for on-board electronics. The high-frequency auxiliary stage precisely regulates the output voltage, V_{OUT} with a Ripple-Based Constant On-Time (RB-COT) control scheme, by utilizing the energy stored in the buffer capacitor, C_{AUX}. With no stringent transient requirements on V_{AUX}, the main stage is optimized to deliver the average load power, while the auxiliary stage is designed for high-frequency operation. A 50W, 48V-to-0.8V experimental prototype was built to validate the proposed architecture. Load transients from 5 A to 29 A were applied to the prototype, resulting in an output voltage deviation of 60 mV. The system achieves a peak efficiency of 89.5% with an output capacitance of only 720 µF and an auxiliary capacitance of 120 µF.

Introduction

The proliferation of on-board electronics in Electric Vehicles (EVs) has constrained power delivery and led to the adoption of 48V voltage distribution networks [1]. Furthermore, the stringent transient regulation tolerances of automotive processors are currently achieved using large, costly decoupling capacitors. These challenges necessitate an efficient Point-of-Load (PoL) power architecture capable of delivering the increasing power demands of automotive processors from a variable high-voltage bus (24 V - 70 V) to the sub-1V processor core voltage (0.675 V - 0.8 V). Hybrid switched-capacitor converters [2, 3] are promising candidates for efficient 48V PoL converters due to their large native conversion ratio and higher energy density compared to magnetic-based converters. Despite these benefits, fast transient response in 48V PoL converters remains a challenge and has not been suitably addressed in past literature.

To improve the transient response in dc-dc converters, low-cost auxiliary converters have been employed to assist the main stage during load transients [4, 5]. By using a smaller inductor than in the main-stage, auxiliary converters alleviate the physical limit imposed by the main-stage LC-filter on the system

transient response. 48V distribution networks present challenges for auxiliary converters due to the small duty-cycle requirements, with on-times that are often not practical with state-of-the-art power stages. A separate, lower-voltage bus can supply the auxiliary converter, at the expense of additional cost and volume which remain as concerns for space-critical automotive applications. Given these challenges, a power-stage architecture that minimizes the cost of the auxiliary converter by using only low-voltage devices while also providing a loosely regulated ancillary bus for on-board electronics is desirable.

The auxiliary converter presented in [6] provides charge to the output during load transients from a buffer capacitor that is decoupled from the input-voltage bus. By pre-charging the buffer capacitor based on the largest expected load transient, the auxiliary converter provides the necessary charge to satisfy the core voltage transient tolerances. While [6] replenishes the charge in the buffer capacitor, sporadic regulation of the auxiliary capacitor voltage prevents its use as a secondary voltage bus. An active electronic capacitor is proposed in [7] that behaves as a bi-directional current source. The active capacitor is implemented as a Gyrator Resonant Switched-Capacitor Converter, which constrains the conversion ratio for optimal efficiency and requires five additional switches. While both works propose a bi-directional auxiliary converter for fast transient response, the regulation of the auxiliary voltage, V_{AUX}, for ancillary on-board electronics has not been covered by past literature.

In this work, an auxiliary-assisted power architecture is proposed to regulate the auxiliary capacitor voltage, V_{AUX}, using the main hybrid dc-dc stage, while output voltage regulation is provided by the auxiliary stage, as shown in Fig. 1. With the proposed approach, the main hybrid dc-dc stage provides the steady-state load current, I_{LOAD}, the current drawn by the auxiliary-stage losses, and the auxiliary load current, $I_{LOAD,AUX}$. With no stringent transient requirements on V_{AUX}, the main stage can be optimized for DC power delivery, while the auxiliary stage can be designed for high-frequency operation. In addition, creating an ancillary bus from V_{OUT} provides a more efficient conversion stage compared to a voltage bus created by a V_{IN}-tapped power stage.

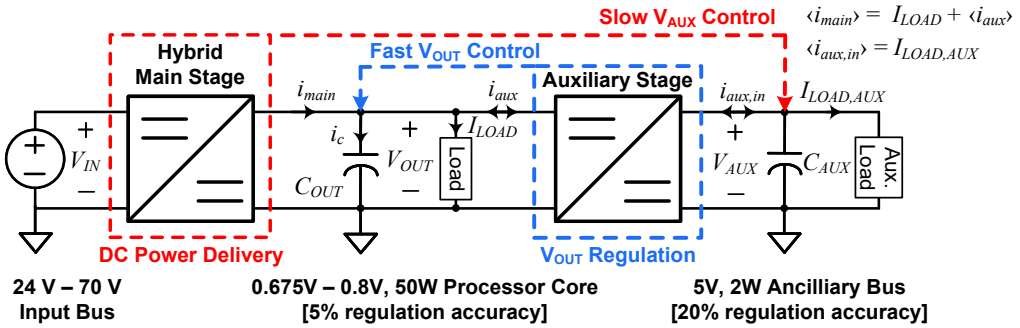


Fig. 1: Proposed auxiliary-assisted power architecture.

This paper is organized as follows. The system architecture, theory of operation, and Power-Delivery-Network (PDN) design are first presented. The proposed system is validated using closed-loop simulation results. An experimental prototype is then presented to characterize the dynamic performance and efficiency of the proposed system. Finally, conclusions are presented at the end of the paper.

System Architecture

The key system parameters and power-stage architecture are presented in Table I and Fig. 2(a), respectively. For the main stage, a 5:1 Series-Capacitor (SC) buck converter was selected for its high native conversion ratio, inherent current sharing, and high output-current capability [8, 9], with its ideal steady-state operating waveforms presented in Fig. 2(b). For the auxiliary converter, a bi-directional two-level converter was selected to minimize cost and size. Typically, auxiliary converters only operate during load transients to provide output charge, whereas in this work, the auxiliary converter operates continuously to regulate V_{OUT}. For fast transient response, the auxiliary-stage switching frequency, $f_{sw,aux}$, was maximized to accommodate a small auxiliary inductor, L_{AUX}, and consequently, increase the inductor

current slew rate, $m_{f,aux}$. A Ripple-Based Constant On-Time (RB-COT) control scheme, similar to [10], was chosen for V_{OUT} regulation due to its simplicity, minimal control delay, and V_{OUT}-based sensing. The inherent current sharing of the SC-buck converter enables the use of a fixed-frequency voltage-mode PWM control scheme for V_{AUX} regulation.

Table I: System Parameters

V_{in} [V]	V_{out} [V]	I_{load} [A]	P_{load} [W]	C_{out} [µF]	$f_{sw,main}$ [kHz]	L_{1-5} [nH]	C_{1-4} [µF]	$f_{sw,aux}$ [MHz]	L_{aux} [nH]	V_{aux} [V]	C_{aux} [µF]
24 - 70	0.675 - 0.8	62.5	50	720	160	470	10	1.6	36	5	120

As the transient requirements on V_{AUX} are less stringent than at V_{OUT}, the SC-buck switching frequency, $f_{sw,main}$, can be relaxed to optimize the main stage for efficient DC power delivery by selecting reliable Silicon (Si) devices with low $R_{ds,on}$ for M_{1-10}. Likewise, the low steady-state current of the auxiliary stage enables the use of higher-$R_{ds,on}$, and therefore low-Q_g, devices for $M_{11,12}$ to minimize switching losses at a higher switching frequency. Typically, auxiliary converters provide charge from the high input voltage bus resulting in a requirement for high-FOM devices. With V_{AUX} being regulated by the main stage, a low V_{AUX} can be set for high $f_{sw,aux}$ and the use of low-FOM silicon devices for $M_{11,12}$.

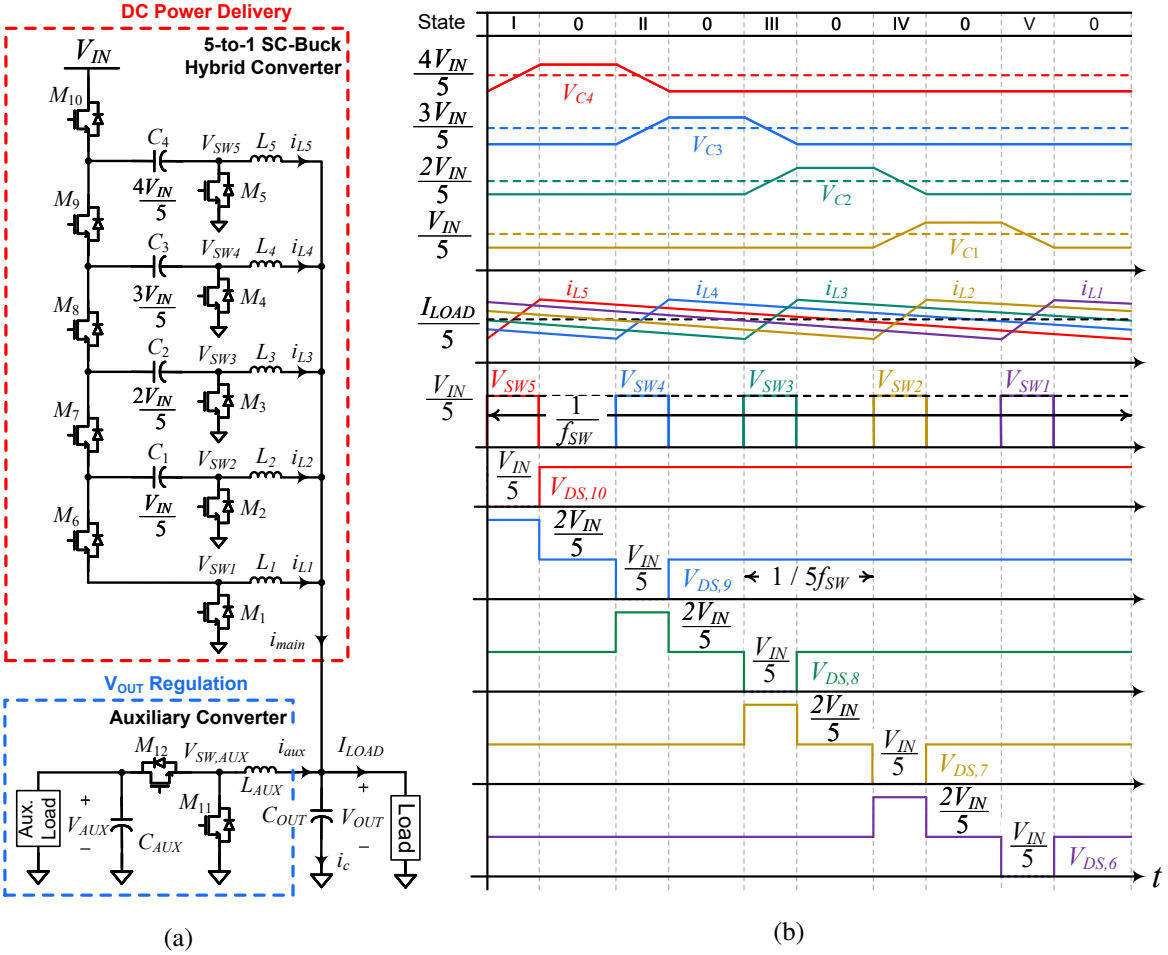


Fig. 2: (a) Auxiliary-assisted power architecture. (b) Ideal steady-state operating waveforms of 5:1 SC-buck converter.

Theory of Operation

The proposed system is dependent on the seamless interdependent operation of the V_{OUT} and V_{AUX} control loops, which are presented in Fig. 3(a). As such, the control bandwidth of each loop must be carefully selected to ensure system stability. The closed-loop operating waveforms of the proposed system during

load transients are shown in Fig. 3(b). When a load step-up transient occurs, V_{OUT} decreases, which is detected by the RB-COT control scheme. The auxiliary converter increases its output current, I_{AUX}, to prevent further charge removal from C_{OUT}, which restores V_{OUT} to $V_{OUT,ref}$. The auxiliary converter continues to provide the transient current, I_2 - I_1, from C_{AUX}, which consequently, creates a deviation on V_{AUX}. The auxiliary regulation loop detect the change in V_{AUX} and adjust i_{main} until V_{AUX} = $V_{AUX,ref}$.

With the auxiliary converter providing V_{OUT} regulation, the main stage regulates V_{AUX}, which creates a regulated ancillary voltage bus. It is important to note that the main stage is not directly connected to C_{AUX} and is dependent on the high control bandwidth of the auxiliary stage to transfer charge to C_{AUX}. Due to the dependence of the auxiliary voltage loop on the COT-based control loop, stability analysis is required to fully optimize the auxiliary voltage control loop, which is beyond the scope of this paper.

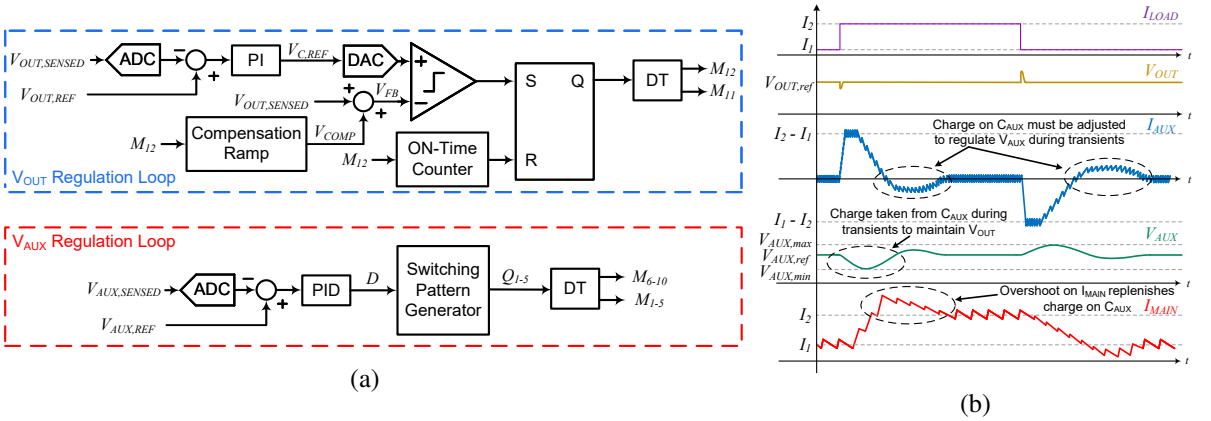


Fig. 3: (a) Control architecture of the proposed auxiliary-assisted dc-dc converter. (b) Representative closed-loop operating waveforms of the proposed system.

Design of Power Delivery Network (PDN)

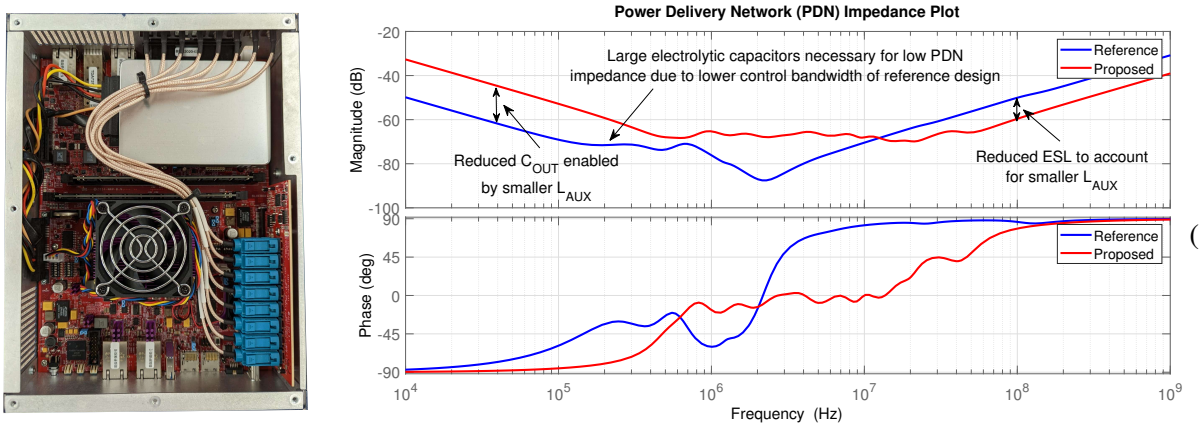
While the output capacitance, C_{OUT}, is selected to satisfy the stringent transient requirements during load transients, the high-frequency impedance of the Power Delivery Network (PDN), must also be carefully designed. A poorly designed PDN causes large voltage deviations, ΔV_{ESL}, to occur during steady-state operation due to the inductive divider between the Equivalent Series Inductance (ESL) of C_{OUT} and the power-stage inductors, L_{MAIN} and L_{AUX}. The ΔV_{ESL} due to the main and auxiliary stages can be calculated as follows:

$$\Delta V_{ESL,main} = \frac{V_{IN}/N}{1+\frac{L_{MAIN}}{ESL}}, \Delta V_{ESL,aux} = \frac{V_{AUX}}{1+\frac{L_{AUX}}{ESL}}, \quad (1)$$

where N is the native conversion ratio of the hybrid dc-dc converter. Based on (1), ΔV_{ESL}, is determined by the ratio of L_{MAIN} and L_{AUX} to the ESL, V_{IN}, and V_{AUX}. To analyze the PDN of a typical processor, a commercial autonomous-driving development platform, shown in Fig. 4(a), which houses an automotive-grade processor, is selected as a reference design, with its PDN impedance plot shown in Fig. 4(b). Due to a large L_{MAIN}, the reference design is less sensitive to the ESL of C_{OUT}. Conversely, the large power-stage inductor limits the system transient response, which large costly decoupling capacitors to reduce the PDN impedance at low frequencies.

In the proposed architecture, a high-frequency two-level converter with a small auxiliary inductor, L_{AUX}, of 36 nH are used to improve the system transient response. As a result, the proposed system reduces the required amount of large decoupling capacitors but the resultant ratio of L_{AUX} to ESL is much higher than the ratio of L_{MAIN} to ESL. Thus, high-frequency decoupling capacitors must be included in the proposed system to reduce the ESL of C_{OUT}, as shown in Fig. 4(b). There is a tradeoff between low-frequency, large bulky electrolytic capacitors for load-transient-based voltage deviation and high-frequency, small ceramic capacitors for ESL-based voltage deviation. Given that processors already require high-frequency ceramic capacitors to compensate for the socket inductance amongst other parasitic

inductive effects, it is more desirable to reduce costly and bulky low-frequency electrolytic capacitors.

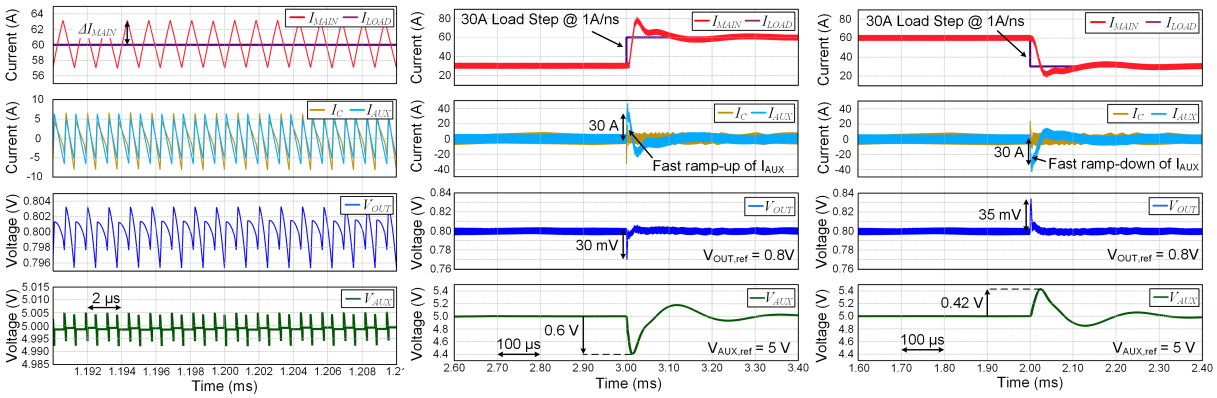


(a) (b)

Fig. 4: (a) Reference autonomous-driving development platform with a 45W automotive-grade processor. (b) Calculated PDN impedance plots of reference design and proposed system.

Simulation Results

The system was first verified using a PLECS closed-loop simulation. The steady-state waveforms are shown in Fig. 5(a). The main-stage current ripple, ΔI_{MAIN}, creates a disturbance in V_{OUT} at $5\times f_{sw,main}$ which the auxiliary converter attempts to correct by adjusting I_{AUX}. Load steps from 30 A to 60 A were applied to demonstrate the fast transient response and voltage regulation of the ancillary bus, as shown in Fig. 5(b) and (c). During load step-up transients, with C_{AUX} = 120 µF, an output voltage deviation of 30 mV is observed while V_{AUX} decreases by 0.6 V before the main SC-buck stage replenishes the charge on C_{AUX}. During load step-down transients, an output voltage deviation of 35 mV is observed, while V_{AUX} increases by 0.42 V before the SC-buck main stage responds. Using the Time-Optimal Control (TOC) comparison presented in [11], adding the auxiliary converter allows the output capacitance to be reduced by 62% compared to operating only a TOC-based main stage.



(a) (b) (c)

Fig. 5: Simulated closed-loop operating waveforms of the proposed system at 48V-to-0.8V conversion ratio during: (a) steady-state, (b) load step-up transient from 30 A to 60 A and (c) load step-down transient from 60 A to 30 A.

Experimental Results

The power consumption of the automotive-grade processor from the autonomous-driving development platform, shown in Fig. 4(a), was measured to determine its typical profile, as shown in Fig. 6. The load

profile was determined by measuring the main-stage inductor current based on the DCR current sensing capacitor. To remove the ESL voltage ripple and observe the low-frequency load profile, the measured capacitor voltage was filtered using a Savitzky-Golay filter. The 45W automotive-grade processor continuously performs computationally intensive tasks and generates dynamic load profiles.

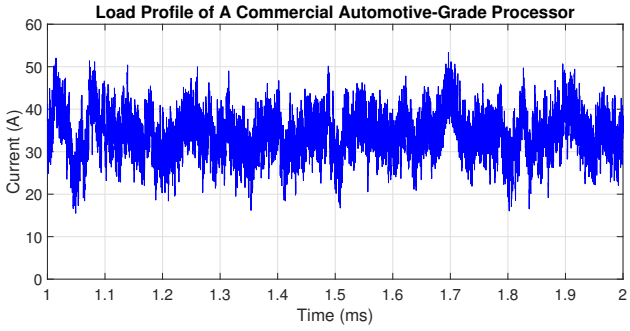


Fig. 6: Measured load profile of the automotive-grade processor from the commercial autonomous-driving development platform.

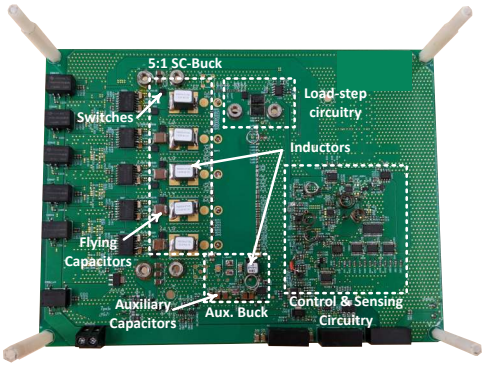
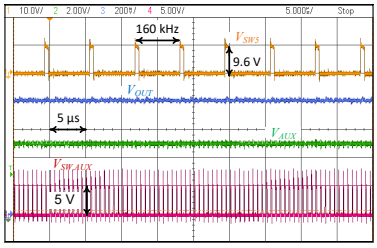
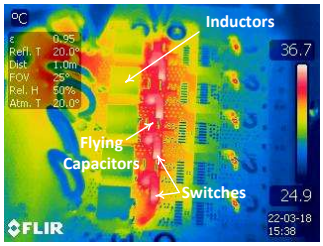


Fig. 7: Experimental prototype of the proposed system.

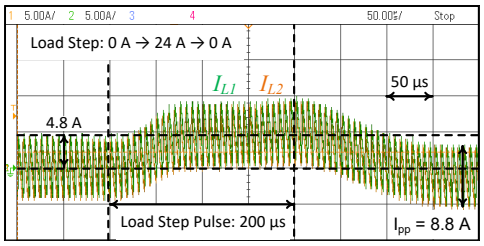
A prototype composed of the 5:1 SC-buck stage, auxiliary stage, and control circuitry was built, as shown in Fig. 7, to characterize the dynamic response and efficiency of the proposed system. A high di/dt load-step circuit was implemented on the PCB. For M_{6-10}, the switches are implemented using 60V, 3.3mΩ BSZ040N06LS5 devices, while 25V, 1.3mΩ NTTFS1D8N02P1E devices are used for M_{1-5}. For the auxiliary converter, a 16V integrated silicon power module, CSD95377Q4M, was selected for its low-inductance package, making it suitable for a high-frequency operation of 1.6 MHz. The COT-based control circuitry was placed on the right side of the board, as shown in Fig. 7, while the digital PID controller for V_{AUX} regulation was implemented on the FPGA on the PCB backside.



(a)



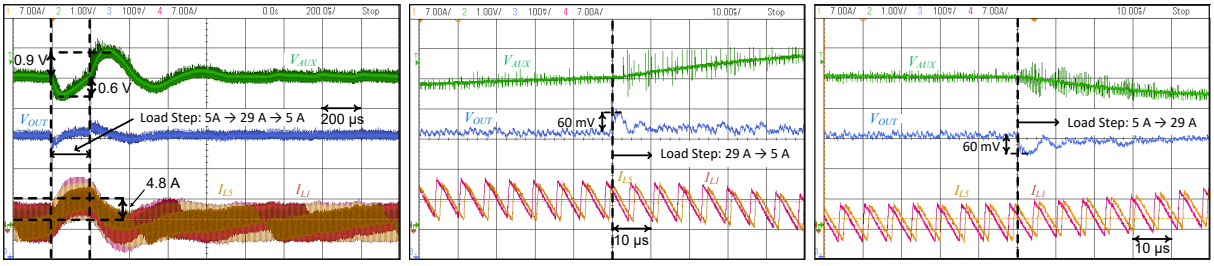
(b)



(c)

Fig. 8: (a) Measured steady-state waveforms of the proposed system at 48V-to-0.8V conversion ratio at 30 A. (b) Thermal image of the 5:1 SC-buck converter at 50 W and 48V-to-0.8V conversion ratio. (c) Measured current waveforms of the 5:1 SC-buck converter during load transient from 0 A to 24 A.

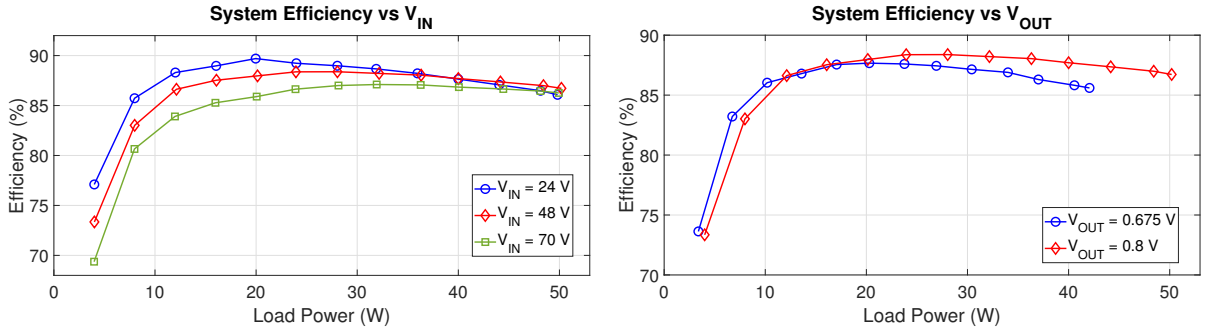
The measured steady-state waveforms of the proposed system are shown in Fig. 8(a). The prototype was operated at 50 W with forced air-cooling until the system reached thermal steady-state, as shown in Fig. 8(b). The peak temperature in the system was 36.7°C and was observed on the high-side SC-buck switches. To highlight the inherent current-sharing of the SC-buck converter, the inductor phase currents during load transients are shown in Fig. 8(c). To demonstrate the voltage regulation of V_{AUX}, the high-speed load-step circuitry, shown in Fig. 7, is used to apply load steps from 5 A to 29 A for 200 µs. The resulting step response on V_{AUX} is shown in Fig. 9(a). The main stage detects the disturbance on V_{AUX} and adjusts i_{main} to correct the auxiliary capacitor voltage with V_{AUX} settling within 0.8 ms. A deviation of -0.6V and +0.9V is observed during transients, which is within 20% of the steady-state value of 5 V. Magnified versions of Fig 9(a) are presented as Fig. 9(b) and 9(c) to demonstrate the fast transient response of the high-speed COT-based auxiliary converter. A maximum output voltage deviation of 60 mV is observed during either load-step transition. Furthermore, due to the high bandwidth of the COT control loop, V_{AUX} is regulated without creating significant disturbances on V_{OUT}.



(a) (b) (c)

Fig. 9: (a) Operating waveforms of the proposed system during load-step transients from 5 A to 29 A. Magnified (b) step-down and (c) step-up load transient waveforms from 5 A to 29 A.

The measured system efficiency versus load power for varying input voltage, V_{IN}, is shown in Fig. 10(a). The system achieves a peak efficiency of 89.5% and an efficiency of 86.8% at the rated output power and nominal conversion ratio of 48V-to-0.8V. As expected, the efficiency improves with lower V_{IN} due to reduced switching and core losses. The measured system efficiency for varying V_{OUT} is also shown in Fig. 10(b). At V_{OUT} = 0.675 V, a peak efficiency of 87.8% is achieved at P_{LOAD} = 17 W while an efficiency of 86.5% is achieved at P_{LOAD} = 42 W.



(a) (b)

Fig. 10: Measured system efficiency for varying: (a) V_{IN} at V_{OUT} = 0.8 V and (b) V_{OUT} at V_{IN} = 48 V.

The proposed system is compared to state-of-the-art auxiliary-assisted converters in Table II. With the highest conversion ratio and highest current rating, this work leverages an auxiliary inductor current slew rate of 22.2 A/µs to minimize the output capacitance, while achieving high efficiency in the main stage.

Table II: State-of-the-Art Auxiliary-Assisted Converters

Year	V_{in} [V]	V_{out} [V]	I_{load} [A]	C_{out} [µF]	L_{aux} [nH]	$m_{f,aux}$ [A/µs]	ΔI_{load} [A]	ΔV_{out} [mV]	V_{aux} [V]	C_{aux} [µF]
This Work	48	0.8	62.5	720	36	22.2	24	60	5	120
2021 [4]	15	3.3	15	220	500	6.6	11	62	15	-
2013 [6]	12	5	10	47	420	11.9	9	388	8.5 - 10	40
2015 [7]	12	1.5	20	200	20	-	15	100	3	30
2015 [12]	5	1.5	15	140	100	15	8.2	45	5	-

Conclusion

An auxiliary-assisted control scheme for a wide-input-voltage-range 50W 5:1 SC-Buck converter was presented for 48V-to-0.8V PoL applications. The auxiliary converter provides V_{OUT} regulation for fast transient response while the 5:1 SC-buck stage efficiently delivers the dc load power and regulates V_{AUX} to create an ancillary voltage bus for on-board electronics. The system achieves a peak efficiency of

89.5% with only 720 µF of output capacitance and 120 µF of auxiliary capacitance. During load steps of 24 A, a maximum ΔV_{OUT} of 60 mV and a ΔV_{AUX} of 0.9V is observed.

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