

Evaluation of common-mode leakage current of Aalborg-type transformerless PV inverters

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Keywords

«Grid-connected inverter», «Transformerless PV inverter», «Dual-mode time-sharing inverter», «Buck in Buck, Boost in Boost inverter», «Step-up inverter», «Rectified sine wave DC-link voltage», «Aalborg inverter», «Common-mode current», «Ground leakage current».

Abstract

Single-phase transformerless photovoltaic (PV) inverters with voltage step-up capability are widely employed for integrating PV generation to the electric grid. Transformerless PV inverter topologies include special features to suppress common-mode (CM) leakage currents that can flow through parasitic capacitances that appear between the PV array and the ground. The Aalborg inverter belongs to the family of dual-mode time-sharing PV inverters, in which a voltage step-up (Boost) stage operates alternatively to a step-down (Buck) stage to create a rectified sine wave DC-link voltage, which is then unfolded to the grid. This paper analyses, quantifies and improves CM leakage current generation for Aalborg-type transformerless PV inverters. It highlights the factors that can lead to high peak and RMS values of leakage current for these topologies and proposes an output filter modification to reduce them by up to 70%. The analytical results are supported by simulation in MATLAB-Simulink and are applicable to other topologies with rectified sine wave DC-link voltages.

1. Introduction

Single-phase transformerless inverter topologies have found great acceptance in the field of integration of photovoltaic (PV) systems to the electric grid, due to their high efficiency and the benefits they provide in terms of size, weight and cost [1, 2]. The transformerless inverter (that is, the DC/AC conversion) stage in relevant commercial products is normally preceded by one (or more) voltage step-up (i.e. Boost) stage, which is responsible for performing the PV array Maximum Power Point Tracking (MPPT) process and providing the inverter with an adequate DC-link voltage, even at low solar irradiance and/or high ambient temperature operating conditions.

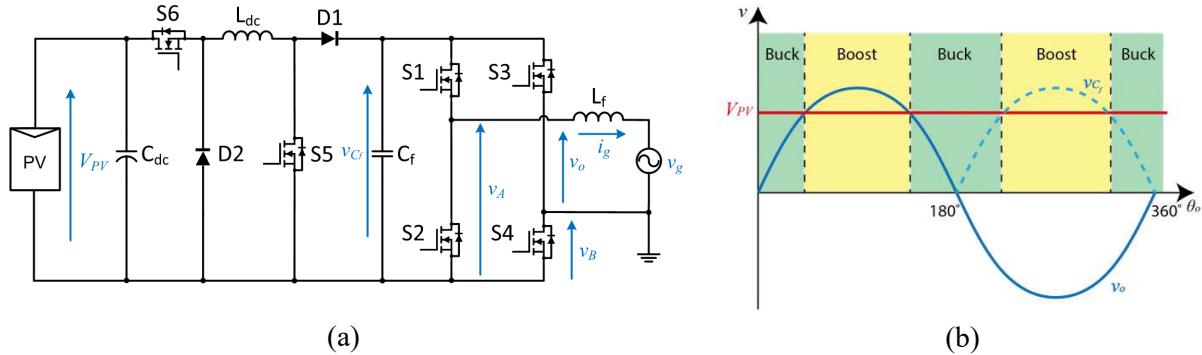


Fig. 1: (a) Aalborg full-bridge inverter topology, (b) Regions of Buck/Boost mode [5].

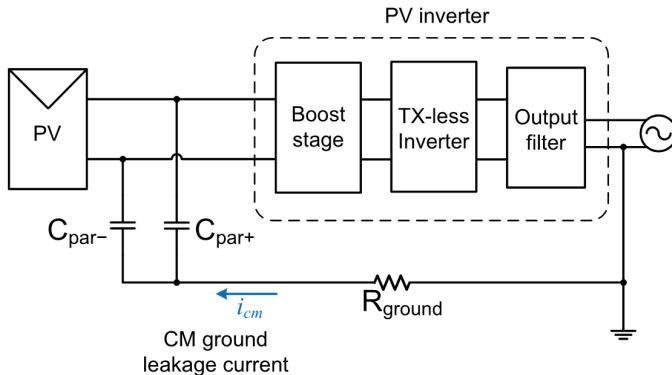


Fig. 2: Common-mode ground leakage current circulation path.

The Boost and the inverter stages are traditionally controlled with the aim of maintaining a stable DC-link voltage. Nevertheless, according to a different concept for two-stage transformerless PV inverters, the DC-link voltage waveform has the form of a rectified sine wave [2]. This waveform is generated by a DC-DC conversion stage, while an H-bridge simply “unfolds” it and supplies it to the grid. A family of PV inverters operating according to this concept are the dual-mode time-sharing inverters [3, 4]. These inverters operate in Buck or Boost mode depending on the instantaneous value of their output voltage, v_o , in relation to the PV array voltage, V_{PV} , as shown in Figure 1(b). Among them, the full-bridge Aalborg inverter, shown in Figure 1(a) [5] and its variants presented in [6, 7] exhibit high efficiency due to the elimination of one inductor as compared to other dual-mode time-sharing topologies, and the operation of only one power switch at high switching frequency at each moment.

In addition to high efficiency, a significant requirement for PV inverters relates to the suppression of common-mode (CM) ground leakage currents. Ground leakage currents can flow in transformerless inverter systems due to the existence of parasitic capacitances between the solar cells of the PV array and the ground. They circulate through the normally grounded electric grid neutral, as illustrated in Figure 2, and cause deterioration of the PV cells and safety hazards. Transformerless PV inverters apply a number of different techniques to suppress CM currents. These techniques and their effectiveness have been studied in the literature [1, 8 – 11] for other transformerless PV inverter topologies, but not for dual-mode time-sharing topologies.

This paper makes the following contributions: (a) analyses the CM leakage current generation mechanism for the full-bridge Aalborg inverter, which also applies to other dual-mode time-sharing

topologies, (b) proposes an output filter modification which can lead to significant reduction of CM leakage current, (c) derives analytical expressions for the RMS value of the CM currents, for the original and the modified filter configurations, (d) quantifies the generated CM current under different inverter operating conditions in comparison with a well-known transformerless topology used as a benchmark, and (e) assesses the effect of each filter parameter on the generated CM current. The presented analysis is supported by simulations in MATLAB-Simulink.

2. CM current generation mechanism

2.1 Characteristics of generated CM voltage

The CM voltage, v_{cm} , of a single-phase inverter topology is calculated as:

$$v_{cm} = \frac{v_A + v_B}{2} \quad (1)$$

where v_A and v_B are the voltages of the two output terminals with respect to the negative DC-bus terminal, shown in Figure 1(a). In a conventional H-bridge inverter, these voltages have a Pulse Width Modulated (PWM) waveform, which results in fast variation of the CM voltage and flow of leakage currents through the parasitic capacitances of the PV array. For the topology of Figure 1(a), however, the H-bridge consisting of S1 to S4, simply switches at the grid frequency to unfold the voltage of capacitor C_f . The H-bridge can only be at two different switching states (not four, since the zero states are not used), namely S1-S4 or S2-S3. It can be shown that for both states, the CM voltage generated by the topology is equal to $v_{cf} / 2$. Given that C_f is the output filter capacitor for the preceding Buck/Boost converter, the CM voltage of this inverter is not pulsating. Instead, it (ideally) has the form of a rectified sine wave, with half the amplitude of v_{cf} , which is shown in Figure 1(b). Since a rectified sine wave voltage does not exhibit sudden variations (i.e., high values of dv/dt), the topology is fundamentally expected to generate minimal values of CM leakage current. Nevertheless, v_{cf} also contains different types of distortion that do result in the generation of CM leakage current. The appearing types of distortion depend on whether the inverter operates in Buck or Boost mode, as it will be discussed below.

Buck mode

When the inverter operates in Buck mode, the following two types of distortion appear:

- I. Capacitor voltage ripple: Since capacitor C_f acts as an LC filter capacitor for the Buck converter, an amount of voltage ripple is expected to appear at the converter switching frequency. The amplitude of this voltage ripple depends on the values of L_{dc} and C_f , as well as the switching frequency and duty cycle of the Buck converter. In the present topology, a typical peak-peak value for this ripple is in the range of 1% of the peak grid voltage.
- II. Voltage distortion at grid voltage zero-crossings: The topology of Figure 1(a) is designed to operate only with a unity power factor. In practice, though, due to the phase lag introduced to the output current by the filter inductors, the voltage of capacitor C_f does not exactly follow a rectified sine wave in the area of zero-crossings of the grid voltage. Namely, fast voltage transients appear as a result of the capacitor current changing direction before the capacitor voltage reaches the value of zero.

Boost mode

When the inverter operates in Boost mode, or transitions between Buck and Boost mode, the following types of distortion appear:

- III. High capacitor voltage ripple: Capacitor C_f acts as an output capacitor for the Boost converter, too. The same capacitor will have several times higher voltage ripple when used with a Boost converter as compared to a Buck converter, due to the pulsating form and higher peak values of the current that the Boost converter supplies it with. Hence, when the inverter operates in Boost mode, the variation of the capacitor voltage is significantly higher, reaching up to approximately 15% of the peak grid voltage.

- IV. Voltage distortion at the transitions between the two modes: Capacitor voltage distortion is observed at the points of the transitions between the Buck and Boost modes. The characteristics (e.g. magnitude and duration) of this type of distortion depend on the inverter control strategy and the method (if any) applied to ensure a smooth transition between the two modes.

2.2 Equivalent circuits for CM current generation

With reference to Figure 1(a), during state S1-S4, the grounded neutral of the grid is connected to the negative terminal of the PV array through S4, thus fixing the voltages of the parasitic capacitors C_{par-} and C_{par+} to 0 and V_{PV} , respectively. This direct connection eliminates the flow of leakage currents during state S1-S4, that is, approximately for the duration of each positive half cycle of the grid voltage. On the other hand, during state S2-S3, the neutral of the grid is connected to the positive terminal of C_f , rendering the voltages of the parasitic capacitors C_{par-} and C_{par+} dependent on v_{Cf} . The CM equivalent circuits for the two states are presented in Figure 3(a) and 3(b), respectively.

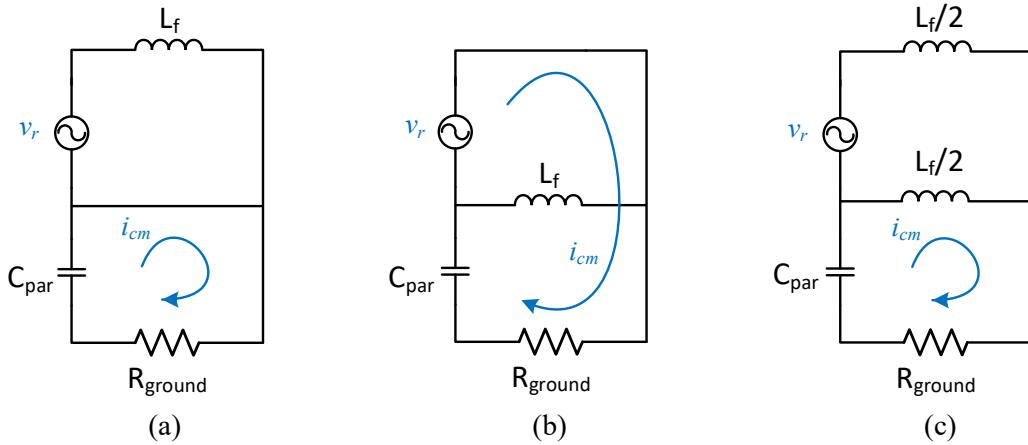


Fig. 3: Common-mode equivalent circuits for (a) state S1-S4, (b) state S2-S3, (c) proposed filter configuration.

Regarding distortion types I and III, if the RMS value of the switching-frequency ripple on v_{Cf} is equal to $V_{r,RMS}$ (abbreviation of $V_{Cf,ripple,RMS}$), then:

$$I_{cm,r,RMS,1-4} = 0, \text{ during state S1-S4} \quad (2)$$

$$I_{cm,r,RMS,2-3} = V_{r,RMS} / \sqrt{R_{ground}^2 + 1/(\omega_s C_{par})^2}, \text{ during state S2-S3} \quad (3)$$

where $\omega_s = 2\pi f_s$, with f_s being the switching frequency of the Buck/Boost stage, and C_{par} is the total parasitic capacitance to ground.

Given that the duration of each state is equal to half of the fundamental period, the overall RMS value of the switching-frequency CM current is as follows:

$$I_{cm,r,RMS} = V_{r,RMS} / \sqrt{2 [R_{ground}^2 + 1/(\omega_s C_{par})^2]} \quad (4)$$

Moreover, it is noted that the CM current contains a component at the fundamental frequency of the grid, due to the relevant (i.e. rectified sine wave) variation of v_{Cf} , which can be shown to also appear only during state S2-S3. The RMS value of this component is given by Eq. (5), and is normally low or even negligible as compared to $I_{cm,r,RMS}$:

$$I_{cm,f,RMS} = V_{g,RMS} / \sqrt{2 [R_{ground}^2 + 1/(\omega_g C_{par})^2]} \approx V_{g,RMS} \omega_g C_{par} / \sqrt{2} \quad (5)$$

where $\omega_g = 2\pi f_g$, with f_g being the fundamental frequency of the grid (50/60Hz), and $V_{g,RMS}$ is the RMS value of the grid phase voltage. The effect of R_{ground} can always be neglected in this expression.

3. Proposed output filter modification

With the aim of reducing the CM current generated by the full-bridge Aalborg inverter, a simple modification of its output filter is proposed in this paper. Namely, the inverter output filter inductor, L_f , is split to two inductors connected as shown in Figure 4, each having half of the original inductance value.

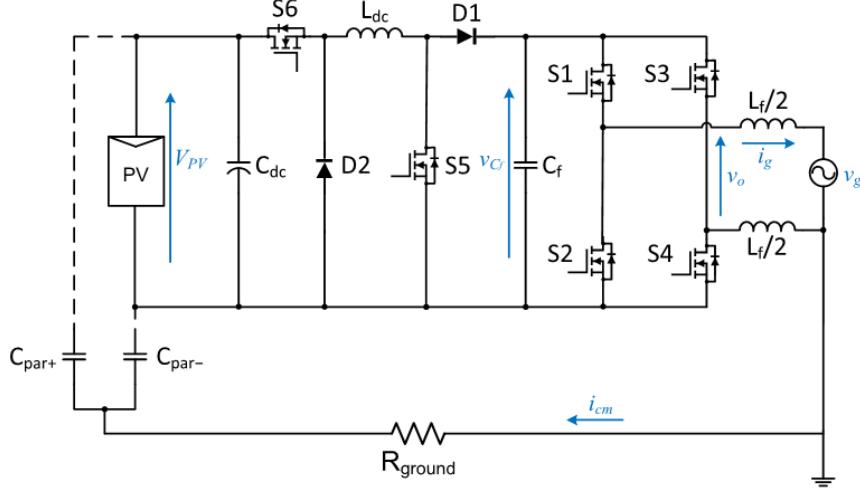


Fig. 4: Topology with the proposed modification, shown with the leakage ground current circulation path.

This configuration for the output filter was found to drastically reduce the peaks of the leakage currents at the zero-crossings of the grid voltage (distortion type II), since it inserts an inductor in a former zero-inductance CM current circulation path. With reference to distortion types I and III, due to the insertion of this inductor, the neutral of the grid is no longer connected to the negative DC-link terminal during H-bridge state S1-S4. Thus, CM current flows in this topology during both grid voltage half-cycles.

The modification of the output filter does not affect the value of $V_{r,RMS}$. The RMS value of the CM current can be derived based on the equivalent circuit of Figure 3(c), which holds for both inverter states. Neglecting the effect of R_{ground} with the aim of simplifying the analytical derivation, the RMS value of the switching-frequency CM current for the proposed filter configuration is as follows:

$$I'_{cm,r,RMS} = V_{r,RMS} \cdot 2\omega_s C_{par} / |4 - \omega_s^2 L_f C_{par}| \quad (6)$$

According to Eq. (6), resonance will occur if L_f takes the following value:

$$L_{f,res} = \frac{4}{\omega_s^2 C_{par}} \quad (7)$$

Moreover, comparison of $I'_{cm,r,RMS}$ from Eq. (6) with $I_{cm,r,RMS}$ from Eq. (4), neglecting R_{ground} , reveals that the ratio between the two currents is:

$$\frac{I'_{cm,r,RMS}}{I_{cm,r,RMS}} = \frac{2\sqrt{2}}{|4 - \omega_s^2 L_f C_{par}|} \quad (8)$$

The RMS value of the fundamental-frequency component of the CM current is again given by Eq. (5). Consequently, inductor L_f must have at least a certain value, $L_{f,min}$, below, for the modified filter configuration to result in a lower RMS value of CM current than the original one:

$$L_{f,min} = \frac{4+2\sqrt{2}}{\omega_s^2 C_{par}} \quad (9)$$

4. Simulation results

Simulations results are presented in this section to illustrate the discussed CM current characteristics and verify the analytical expressions derived for the original and the proposed filter configurations.

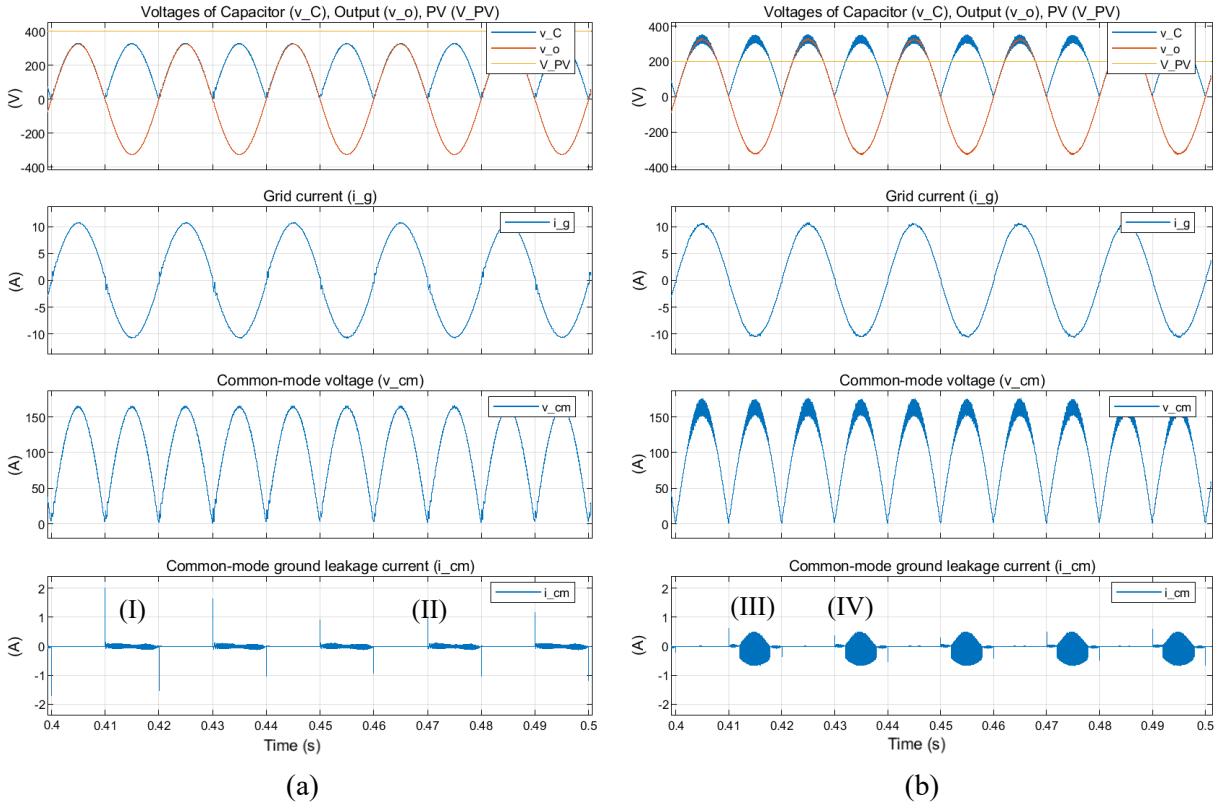


Fig. 5: Simulation results illustrating the operation of the full-bridge Aalborg inverter with: (a) Buck only operation, and (b) Buck-Boost operation. The RMS values of the CM ground leakage current are 38mA/218mA.

The topology of Figure 1(a) was modeled in MATLAB/Simulink as a 2kVA PV inverter switched at 30kHz, with $L_{dc} = 1\text{mH}$, $L_f = 1.2\text{mH}$ and $C_f = 3\mu\text{F}$. The PV array was simulated as a DC source with $V_{PV} = 400\text{V}$ for inverter operation in Buck only mode and $V_{PV} = 200\text{V}$ for operation in Buck-Boost mode. The parasitic capacitances to ground were given values of $C_{par+} = C_{par-} = 100\text{nF}$ (giving a total of $C_{par} = 200\text{nF}$ per PV array kW), while the ground resistance R_{ground} was assumed to have a value of 0.5Ω . The inverter was connected to a 230V/50Hz grid.

Figure 5(a) illustrates a set of waveforms during Buck operation ($v_{o,pk} < V_{PV}$), while 5(b) illustrates the respective waveforms during Buck-Boost operation. The CM current resulting from the four types of capacitor C_f voltage distortion is marked in the two bottom graphs, using symbols I – IV. The following main observations can be noted:

- Although CM voltage distortion of types I and III appears uniformly during both grid voltage half-cycles, CM current flows only during the negative half-cycles. As explained earlier, this is because of the direct connection of the grid neutral to the negative DC-link terminal during the positive half-cycles.
- High peak values of CM current appear at the zero crossings of the grid voltage. These CM currents originate from the CM voltage distortion of type II and exhibit high peak values due to the lack of inductance in their circulation path (which includes the capacitor C_f , the connection to the grid neutral, the ground resistance and the parasitic capacitances).
- The CM voltage distortion of type IV and the resulting CM current are unnoticeable, which is owing to the fact that the applied control strategy [12] is designed to smoothen the transients appearing when switching between the Buck and Boost modes.

The RMS values of the CM current in these results are 38mA for the Buck mode and 218mA for the Buck-Boost mode, while its peak values are in the order of 0.5 to 2A.

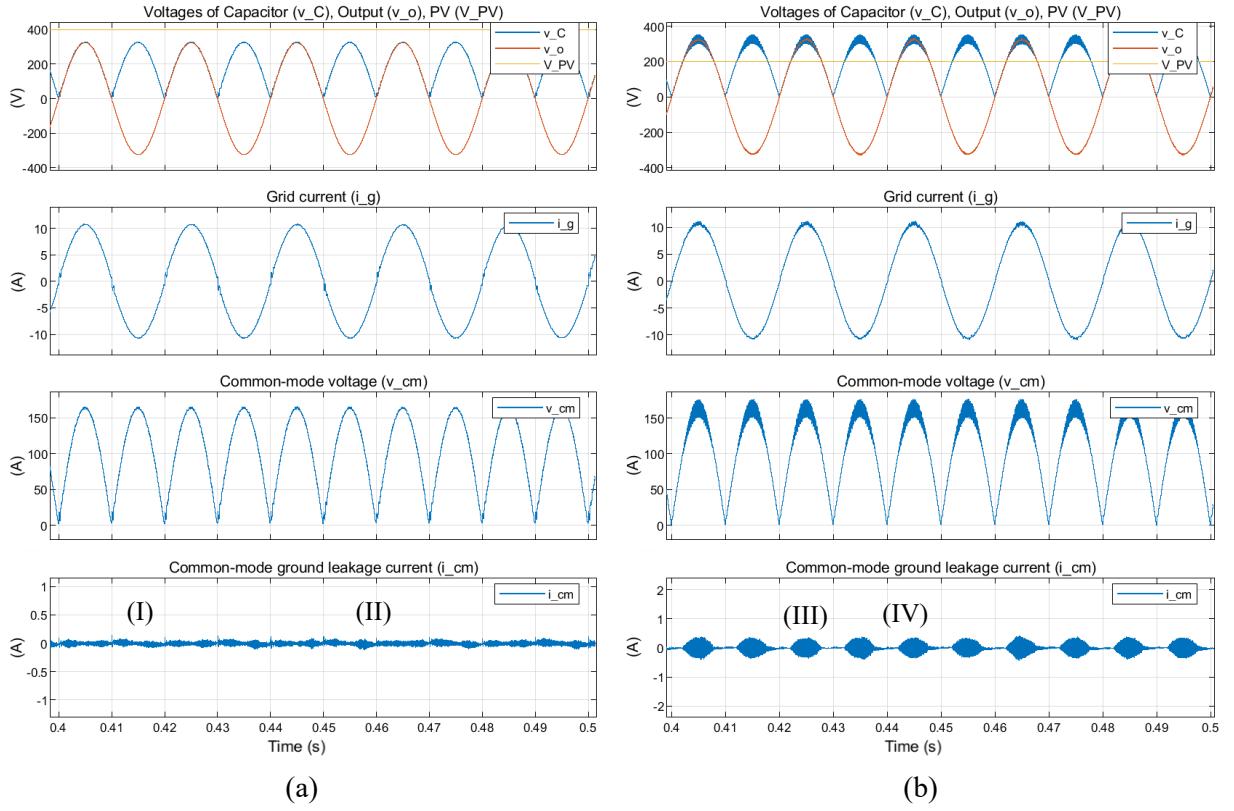


Fig. 6: Comparative simulation results illustrating the operation of the topology with the proposed output filter modification for: (a) Buck only operation, and (b) Buck-Boost operation. The RMS values of the CM ground leakage current are 27mA/129mA.

Figure 6 presents the respective waveforms for the proposed filter configuration. The following observations can be made in this case:

- CM current flows during both grid voltage half-cycles, as shown in the bottom graphs of Figure 6. As mentioned in Section 3, this is because the neutral of the grid is not directly connected to the negative DC-link terminal during H-bridge state S1-S4.
- No high peak values of CM current appear at the zero crossings of the grid voltage, due to the existence of inductance in both the line and neutral connections to the grid.

The resulting RMS values of CM current under the same conditions are reduced to 27mA for the Buck mode and 129mA for the Buck-Boost mode. This reduction agrees with the ratio of Eq. (8), which is equal to 0.62 for the given values of ω_s , L_f and C_{par} .

Table I: CM current for the two filter configurations

PV voltage [V]	PV power [W]	Original [mA]	Modified [mA]	Ratio
200	2000	247.8	142.6	0.58
	1000	124.6	71.3	0.57
	500	64.2	37.7	0.59
	250	36.7	21.8	0.60
400	2000	37.7	22.9	0.61
	1000	35.6	22.9	0.64
	500	34.6	22.9	0.66
	250	34.6	22.9	0.66

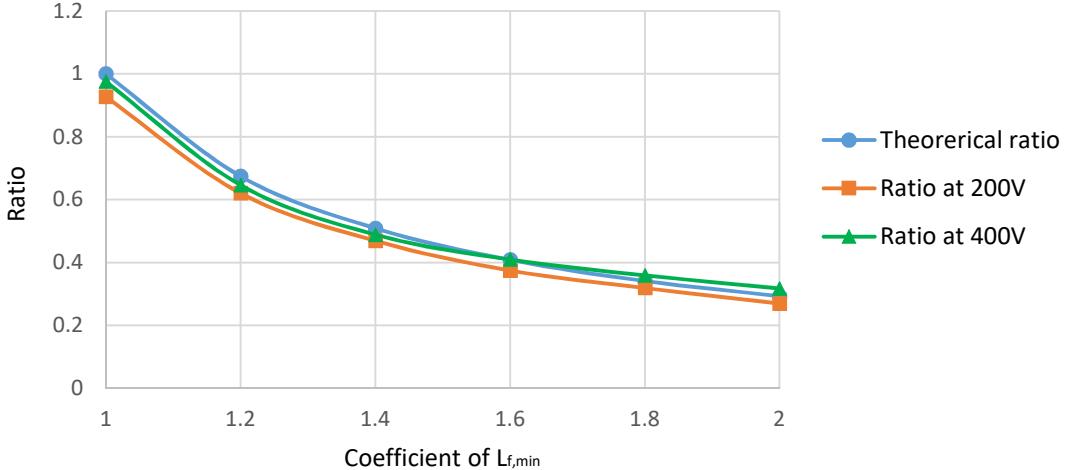


Fig. 7: Comparison of the theoretical ratio from Eq. (8), with ratios from simulations at 200 and 400V, for different values of L_f , ranging from $L_{f,\min}$ to $2 \cdot L_{f,\min}$.

Additional simulations were performed to compare the RMS value of the CM current for the original and the modified filter configuration under different inverter operating conditions, namely PV array voltage and power (current). The results are presented in Table I. The calculated ratio of $I'_{cm,r,RMS}$ over $I_{cm,r,RMS}$ is shown in the last column, and can be observed to remain within $-5/+8\%$ from the theoretically calculated value of 0.62. The deviations are due to the neglection of R_{ground} in the derivation of Eq. (6).

To provide a comparison, according to further simulations, a HERIC inverter [13] supplied by a Boost converter generates 18mA of RMS leakage current under all the conditions of Table I. Nevertheless, this value refers to a HERIC inverter with an L output filter, in the form of two separate inductors (at the line and neutral connections to the grid), each with inductance $L_f/2 = 600\mu\text{H}$. If, with the aim of reducing the grid current distortion to the level of the topology in Figure 4 ($\text{THD}_I < 2\%$), an LCL filter is used instead (with four separate inductors of $L = L_f/2$, and $C = C_f = 3\mu\text{F}$), the generated CM current RMS value increases significantly, to around 100mA.

Again with reference to the topologies of Figures 1(a) and 4, other values of L_f , from $L_{f,\min}$, which has a value of $961\mu\text{H}$ according to Eq. (9), up to $2 \cdot L_{f,\min}$, were tried in simulation for inverter operation at 2000W and 200V/400V, to further validate the derived expressions. The resulting ratios of generated CM currents are plotted as a function of L_f in Figure 7. It can be observed that both curves closely follow the expected ratio, derived from Eq. (8).

Finally, the effect of the values of L_{dc} and C_f on the generated CM current was examined by simulation. As it was expected, for both filter configurations, the RMS value of the CM current is inversely proportional to the values of L_{dc} and C_f . This is due to the fact that the switching-frequency ripple on v_{cf} , which generates CM current according to Eq. (4) and (6), is primarily determined by these two parameters and reduces proportionally to them.

5. Discussion

It becomes apparent from the results presented in Section 4 that the proposed filter modification can significantly reduce the generated CM current, if a grid-side inductor with adequately high inductance is selected. Alternatively, CM current reduction could be achieved by increasing the value of the Buck/Boost inductor, L_{dc} , and/or the Buck/Boost output filter capacitor, C_f .

Nevertheless, the increment of L_{dc} is not preferable for the following reasons: a) L_{dc} is rated at a higher current (typically around 2 – 3 times) than L_f , as it supports the operation in Boost mode, b) L_{dc} is subject to higher copper and core losses, because it carries the switching-frequency ripple current generated by the Buck and Boost stages (whereas the current through L_f contains minimal switching-frequency ripple), c) Due to the switching-frequency ripple, L_{dc} must be wound on a low-loss (e.g. ferrite) core, while L_f can be manufactured as a common, line-frequency inductor, and d) Increment of

L_{dc} by a factor of 2 will reduce the CM current to 0.5 of its original value, while increment of L_f by a factor of 2 reduces the CM current to less than 0.3 of its original value, as shown in Figure 7. Thus, increment of L_{dc} instead of L_f would incur higher cost, volume and weight, and result in more losses and lower CM current suppression.

On the other hand, the alternative of increasing the capacitance C_f could be valid, since it can lower $V_{r,RMS}$ and thus the RMS value of the CM current with minor additional cost. However, in the full-bridge Aalborg inverter as well as in other topologies with rectified sine wave DC-link voltage, the increment of C_f increases the grid current distortion around the zero-crossings of the grid voltage. The distortion relates to the voltage “unfolding” and the restriction for unity power factor, discussed in [12]. It becomes more evident when the inverter operates at low power and practically imposes a limit on the size of C_f .

Given the value of C_f , the proposed filter configuration therefore offers a preferred method for reducing the CM current generated by the full-bridge Aalborg inverter or similar topologies. It should be noted, however, that application of the method requires knowledge (approximate, obtained based on PV panel characteristics or measurement) of the parasitic capacitance C_{par} , since this is required to select a suitable value for L_f , according to Eq. (9). Finally, the grid impedance, which has not been considered in this study, will add to L_f and act favourably with respect to CM current suppression.

6. Conclusion

In this paper, the CM leakage current generation mechanism for an Aalborg-type PV inverter was analysed and an output filter modification was proposed which can reduce the generated CM leakage ground current RMS value by approximately 70%. Analytical expressions were derived and verified by extensive simulations in MATLAB-Simulink, over a wide range of inverter operating conditions and filter parameter values. The presented results are significant because they can also be applied to other topologies belonging in the family of rectified sine-wave DC-link voltage transformerless PV inverters.

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