

# High-Performance Discontinuous Pulse Width Modulation Strategy for 3-level Asymmetric T-NPC Inverter

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**Abstract**-- Discontinuous mode pulse width modulation (DPWM) is commonly used to improve switching losses for three-phase converters. This paper studies the DPWM strategies for the 3-level asymmetrical T-NPC (AT-NPC) inverter. First, a carrier-based DPWM technique with an offset function is introduced. Secondly, a space vector DPWM strategy is proposed based on the three nearest voltage vectors principle. The PWM control performance of the proposed modulation methods is then verified by simulation and experimental results. A detailed comparison between the two methods is also conducted.

**Index Terms**-- Asymmetric inverter, discontinuous PWM, space vector PWM, T-NPC 3-level.

## I. INTRODUCTION

The 3-level inverters are increasingly popular in practical applications because of their advantages over 2-level inverters, such as better output voltage quality, higher efficiency, and reduced voltage stress on power devices. They can be classified into neutral point clamped (NPC), cascaded H-bridge (CHB), and flying capacitor (FLC) inverters. However, the 3-level configuration uses even more than twice as many components as the 2-level inverter, resulting in a significant increase in cost. An approach of economical three-level inverter configurations has been proposed. In [1,2], the 3-level diode NPC inverter structure using two legs for 3-phase was introduced. A similar structure without diodes is presented in the form of T-NPC [3]. However, the practical applications of these configurations are restricted because their output voltage range is only 1/2 that of conventional 3-level structures.

Recently, the 3-level asymmetric T-NPC (AT-NPC) inverter topology, which uses fewer switches but has the same output voltage range and good THD performance compared with conventional 3-level inverters, was introduced in [4, 5]. There are few published studies on suitable PWM modulation strategies for this configuration. In this paper, a high-performance DPWM modulation technique for the 3-level T-NPC inverter configuration is proposed. The switching vectors are designed based on the three nearest vectors principle to achieve low harmonics content in the output voltages. The content of the article consists of 5 sections. The introduction is presented in Section I. The analysis of the 3-level AT-NPC inverter is described in Section II. In Section III, both the carrier-based DPWM (CB-DPWM) and space vector DPWM (SV-DPWM) techniques for the 3-level AT-NPC inverter are described. Regarding the SV-DPWM method, determining the region of the reference vector, designing the switching pattern, and calculating the duty ratios are interpreted in

detail. Section IV provides the analysis and evaluation of the simulation and experimental results. Conclusions in Section V.

## II. THE 3-LEVEL ASYMMETRIC T-NPC INVERTER TOPOLOGY

The 3-level asymmetric T-NPC topology is illustrated in Fig. 1, where each phase A and C consists of 4 IGBTs connected in a 3-level T-type, and phase B is a half-bridge; the front-end 12-pulse rectifier is directly connected to the DC-link capacitor; the output terminals are connected to the R-L load.

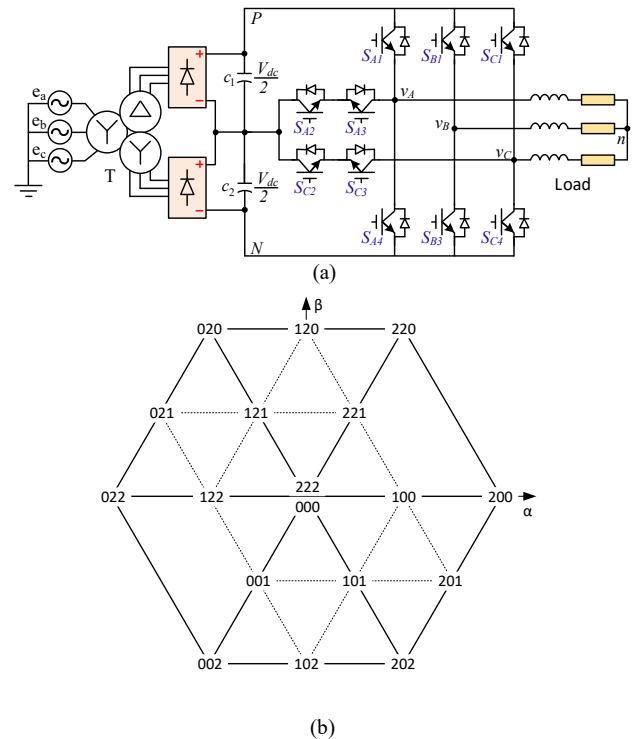


Fig. 1. (a) The topology and (b) the space vector of the 3-level AT-NPC

## III. DPWM FOR THE 3-LEVEL ASYMMETRIC T-NPC INVERTER

### A. The CB-DPWM for the 3-level AT-NPC inverter

From the theory of two-level discontinuous modulation [6], the same strategies modulation has also been extended to the 3-level inverter [7]. Similarly, the proposed CB-DPWM technique for the 3-level AT-NPC inverter with the output voltage clamped to the positive and negative terminals of the DC-link for 60° during peak and valley of the signal references, respectively, as illustrated in Fig. 2. The offset function is defined as following:

$$\begin{cases} v_{off} = (V_{dc} - v_{max}) & \text{if } (v_{max} > |v_{min}|) \\ v_{off} = (-v_{min}) & \text{if } (v_{max} < |v_{min}|) \end{cases} \quad (1)$$

where  $v_{max} = \max(v_{A1}^*, v_{B1}^*, v_{C1}^*)$  and  $v_{min} = \min(v_{A1}^*, v_{B1}^*, v_{C1}^*)$ ; and  $v_{A1}^*$ ,  $v_{B1}^*$ ,  $v_{C1}^*$  are the reference phase voltages.

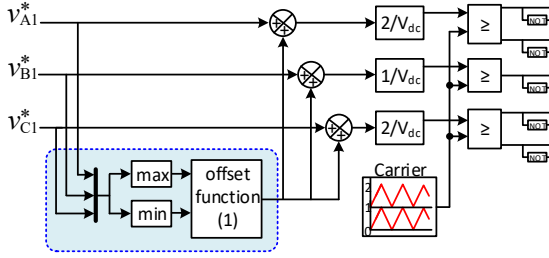


Fig. 2. Implementation of proposed CB-DPWM

#### B. The proposed SV-DPWM for the AT-NPC inverter

The PWM method for the 3-level AT-NPC inverter configuration is proposed based on the space vector technique with the following mandatory requirements: ① the switching pattern is designed in the discontinuous mode, with a maximum of 4 switching actions per cycle. ② use the 3 nearest vector principle to achieve good THD quality. The algorithm design is presented in the following steps:

##### B1. Region division

The space vector of the 3-level AT-NPC inverter is divided into six sectors, in which sectors II, III, V, and VI have the same distributed voltage vectors that of the conventional 3-level inverter. Therefore, the region division for these sectors is performed similarly to the traditional 3-level, as shown in Fig. 3a. The medium voltage vector is not generated from the available switching state combinations of this 3-level inverter in sectors I and IV, so a different division is required. For example, the proposed region division for sector I is as follows: The shape of region 1 is shown in Fig. 3b; it can be seen that the combination of the nearest vectors (000/222, 100, 221) cannot be combined into any discontinuous-mode switching pattern, the requirement ① is not satisfied. So, an SVPWM combined with 2 nearest vectors and 1 far vector can become satisfied with the requirement ①. Two discontinuous switching combinations (000, 100, 120) and (222, 221, 201) are generated when combined with one of the vectors 120 and 201 of the adjacent sector. Vectors 000 and 100 belong to region 1A, so the switching model to synthesize into a reference voltage vector will be performed by the combination (000, 100, 120). Similarly, the combination (222, 221, 201) will be performed for region 1B. Regions 3 and 4 are divided as shown in Fig. 3c using the implementation vector combinations (100, 200, 220) and (221, 220, 200), respectively. The remaining region 2 is divided into 2A and 2B, as shown in Fig. 3d. The implementation vector combinations for regions of sector I are listed in Table 1. Division for sector IV is done similarly.

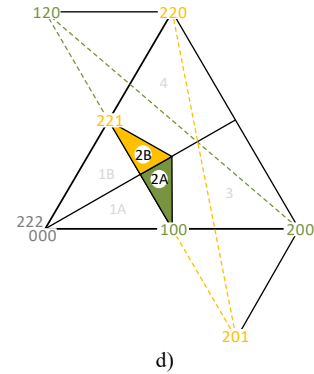
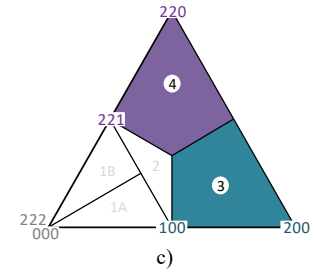
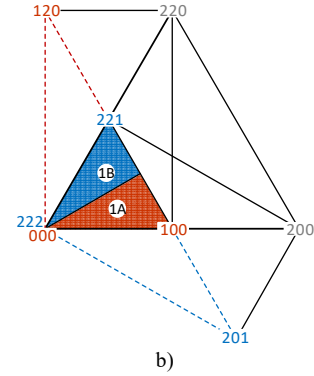
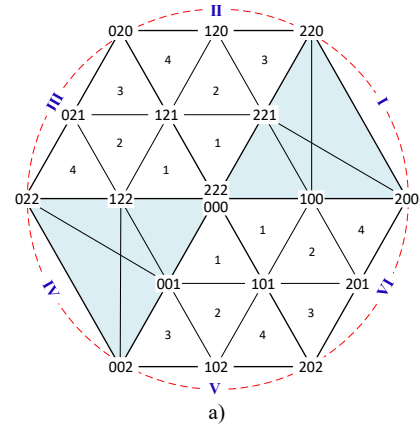


Fig. 3. (a) Region division for sectors II, III, V, and VI. Region division for (b) region 1, (c) regions 3 and 4, (d) region 2 of sector I.

TABLE I  
IMPLEMENTATION VECTOR COMBINATIONS FOR SECTOR I

Working Region	Implementation vector
1A	000, 100, 120
1B	222, 221, 201
2A	100, 200, 120
2B	221, 220, 201
3	100, 200, 220
4	221, 220, 200

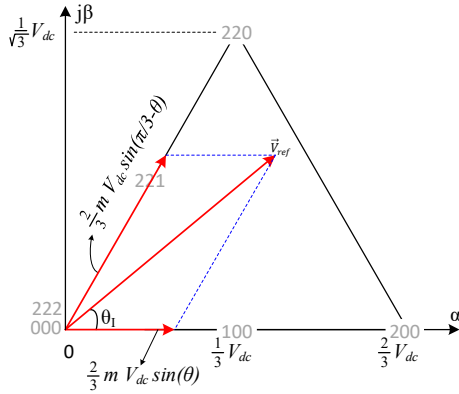


Fig. 4. Representation of the reference vector in sector I

## B2. Region identification of the reference voltage vector

The reference vector can be represented as amplitude and phase angle  $\theta$  as:

$$\vec{V}_{ref} = \frac{mV_{dc}}{\sqrt{3}} e^{j\theta} \quad (2)$$

where  $m$  is modulation index.

The region of the reference vector position in sector I, as illustrated in Fig. 4, can be determined based on the relationship between the two variables  $d_1$  and  $d_2$  [8], which is defined in relative units, with the base unit is  $\frac{2}{3}V_{dc}$  as follows:

$$\begin{cases} d_1 = m \sin(\pi/3 - \theta) \\ d_2 = m \sin(\theta) \end{cases} \quad (3)$$

The regions (1A, 2A, 3) and (1B, 2b, 4) of sector I are detected by three straight boundary (L1, L2, L3) and (L1, L2, L4), as presented in Fig. 5. These straight are defined as following:

$$\begin{cases} L1: d_1 - d_2 = 0 \\ L2: d_1 + d_2 - 0.5 = 0 \\ L3: 2d_1 + d_2 - 1 = 0 \\ L4: d_1 + 2d_2 - 1 = 0 \end{cases} \quad (4)$$

Conditions for determining the regions of sector I:

if (L1 > 0)  
     if (L2 < 0) then Region-1A  
     if (L3 < 0) then Region-2A  
     else Region-3  
 else  
     if (L2 < 0) then Region-1B  
     if (L4 < 0) then Region-2B  
     else Region-4

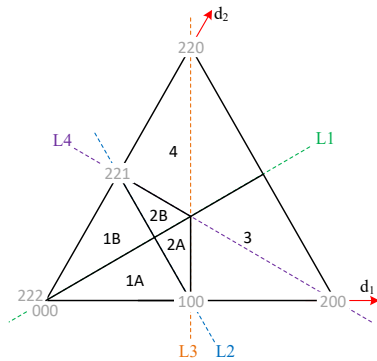


Fig. 5. Region identification of the reference voltage vector for sector I

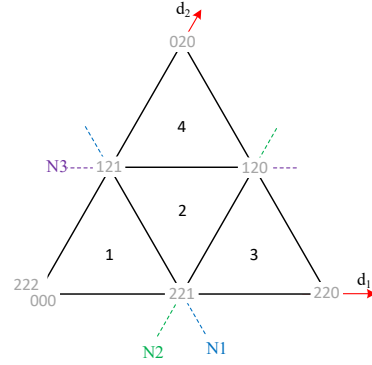


Fig. 6. Determine the regions for sector II after converting to sector I

For simplicity, the determination of regions for other sectors is done similarly by converting to sector I. The angle of the reference vector will be rescaled in the range from  $0 - \pi/3$  as follows:

$$\theta = \theta_i - (i - 1)\frac{\pi}{3} \quad (5)$$

where  $i = 2, 3, \dots, 6$  corresponds to sectors II, III, ..., VI.

Taking sector II as an example, as shown in Fig. 6, the regions will be detected by straight (N1, N2, N3) as:

$$\begin{cases} N1: d_1 + d_2 - 0.5 = 0 \\ N2: d_1 - 0.5 = 0 \\ N3: d_2 - 0.5 = 0 \end{cases} \quad (6)$$

The regions of sector II are determined based on the following conditions:

if (N1 < 0) then Region-1  
 if (N2 > 0) then Region-3  
 if (N3 > 0) then Region-4  
 else Region-2

## B3. Duty ratio calculation

In general SVPWM, the reference vector is synthesized by 3 vectors  $\vec{V}_a$ ,  $\vec{V}_b$ , and  $\vec{V}_c$  with the duty coefficients  $d_a$ ,  $d_b$  and  $d_c$  respectively, satisfying the equation below:

$$\begin{cases} d_a \vec{V}_a + d_b \vec{V}_b + d_c \vec{V}_c = \vec{V}_{ref} \\ d_a + d_b + d_c = 1 \end{cases} \quad (7)$$

For example, in the case of region I-1A as shown in Fig. 7, the reference vector is synthesized by 3 vectors  $\vec{V}_{000}$ ,  $\vec{V}_{100}$ , and  $\vec{V}_{120}$  as follows:

$$\begin{cases} d_a \vec{V}_{000} + d_b \vec{V}_{100} + d_c \vec{V}_{120} = \vec{V}_{ref} \\ d_a + d_b + d_c = 1 \end{cases} \quad (8)$$

Substitute the corresponding amplitude values of the vectors in (8), separate the real and imaginary parts as follows:

$$\begin{bmatrix} 0 & \frac{1}{3} & 0 \\ 0 & 0 & \frac{1}{\sqrt{3}} \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} d_a \\ d_b \\ d_c \end{bmatrix} = \begin{bmatrix} m \cos(\theta)/\sqrt{3} \\ m \sin(\theta)/\sqrt{3} \\ 1 \end{bmatrix} \quad (9)$$

Solving equation (9), the result is rewritten according to the variables defined in (3) as follows:

$$\begin{bmatrix} d_a \\ d_b \\ d_c \end{bmatrix} = \begin{bmatrix} 1 - 2(d_1 + d_2) \\ 2d_1 + d_2 \\ d_2 \end{bmatrix} \quad (10)$$

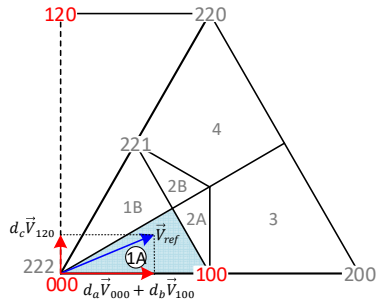


Fig. 7. Duty factor calculation for region I-1A

Similar calculations for all remaining regions, the duty coefficients are summarized in Table 2.

TABLE 2  
DUTY RATIO FOR REALIZED VECTORS

Region	Voltage vector	Duty ratio	Region	Voltage vector	Duty ratio
I-1A	000	$1 - 2(d_2 + d_1)$	I-1B	222	$1 - 2(d_1 + d_2)$
	100	$2d_1 + d_2$		221	$d_1 + 2d_2$
	120	$d_2$		201	$d_1$
I-2A	120	$d_2$	I-2B	201	$d_1$
	100	$2 - 2d_1 - 3d_2$		221	$2 - 3d_1 - 2d_2$
	200	$2(d_1 + d_2) - 1$		220	$2(d_1 + d_2) - 1$
I-3	100	$2 - 2(d_1 + d_2)$	I-4	221	$d_1$
	200	$2d_1 + d_2 - 1$		220	$2d_2 + d_1 - 1$
	220	$d_2$		200	$2 - 2(d_1 + d_2)$
II-1	222	$1 - 2(d_2 + d_1)$	II-3	221	$2 - 2(d_1 + d_2)$
	221	$2d_1$		220	$2d_1 - 1$
	121	$2d_2$		120	$2d_2$
II-2	221	$1 - 2d_2$	II-4	121	$2 - 2(d_1 + d_2)$
	121	$1 - 2d_1$		120	$2d_1$
	120	$2(d_1 + d_2) - 1$		020	$2d_2 - 1$
III-1	222	$1 - 2(d_1 + d_2)$	III-3	121	$2 - 2(d_1 + d_2)$
	122	$2d_2$		021	$2d_2$
	121	$2d_1$		020	$2d_1 - 1$
III-2	122	$1 - 2d_1$	III-4	122	$2 - 2(d_1 + d_2)$
	121	$1 - 2d_2$		022	$2d_2 - 1$
	021	$2(d_1 + d_2) - 1$		021	$2d_1$
IV-1A	222	$1 - 2(d_2 + d_1)$	IV-1B	000	$1 - 2(d_1 + d_2)$
	122	$2d_1 + d_2$		001	$d_1 + 2d_2$
	102	$d_2$		021	$d_1$
IV-2A	102	$d_2$	IV-2B	021	$d_1$
	122	$2 - 2d_1 - 3d_2$		001	$2 - 3d_1 - 2d_2$
	022	$2(d_1 + d_2) - 1$		002	$2(d_1 + d_2) - 1$
IV-3	122	$2 - 2(d_1 + d_2)$	IV-4	001	$d_1$
	022	$2d_1 + d_2 - 1$		002	$2d_2 + d_1 - 1$
	002	$d_2$		022	$2 - 2(d_1 + d_2)$
V-1	000	$1 - 2(d_2 + d_1)$	V-3	001	$2 - 2(d_1 + d_2)$
	001	$2d_1$		002	$2d_1 - 1$
	101	$2d_2$		102	$2d_2$
V-2	001	$1 - 2d_2$	V-4	101	$2 - 2(d_1 + d_2)$
	101	$1 - 2d_1$		102	$2d_1$
	102	$2(d_1 + d_2) - 1$		202	$2d_2 - 1$
VI-1	000	$1 - 2(d_1 + d_2)$	VI-3	101	$2 - 2(d_1 + d_2)$
	100	$2d_2$		201	$2d_2$
	101	$2d_1$		202	$2d_1 - 1$

VI-2	100	$1 - 2d_1$	VI-4	100	$2 - 2(d_1 + d_2)$
	101	$1 - 2d_2$		200	$2d_2 - 1$
	201	$2(d_1 + d_2) - 1$		201	$2d_1$

#### B4. Design the switching state pattern

The switching state pattern for all regions is designed in discontinuous mode using the three nearest vectors, as listed in Table 2, with 4 switching actions per cycle. For sectors I, II, V, and VI, it can be seen that all regions can realize the discontinuous switching pattern using the triangular vertex vectors. For example, region II-2 is shaped by three vectors (120, 121, 221); the switching order for the least number of switches 221-121-120-121-221 is selected. For sector I, the transformation model is performed using the vector combination listed in Table 2. For example, two switching state sequences 000-100-120-100-000 and 222-221-201-221-222 are applied for regions I-1A and I-1B, respectively. Similarly, the switching patterns for all regions are listed in Table 3.

TABLE 3  
SWITCHING STATE SEQUENCE

Region	Switching sequence	Region	Switching sequence
I-1A	000-100-120-100-000	IV-1A	222-122-102-122-222
I-1B	222-221-201-221-222	IV-1B	000-001-021-001-000
I-2A	120-100-200-100-120	IV-2A	102-122-022-122-102
I-2B	201-221-220-221-201	IV-2B	021-001-002-001-021
I-3	100-200-220-200-100	IV-3	122-022-002-022-122
I-4	221-220-200-220-221	IV-4	001-002-022-002-001
II-1	222-221-121-221-222	V-1	000-001-101-001-000
II-2	221-121-120-121-221	V-2	001-101-102-101-001
II-3	221-220-120-220-221	V-3	001-002-102-002-001
II-4	121-120-020-120-121	V-4	101-102-202-102-101
III-1	222-122-121-122-222	VI-1	000-100-101-100-000
III-2	122-121-021-121-122	VI-2	100-101-201-101-100
III-3	121-021-020-021-121	VI-3	101-201-202-201-101
III-4	122-022-021-022-122	VI-4	100-200-201-200-100

#### IV. SIMULATION AND EXPERIMENTAL VERIFICATION

To evaluate the control performance of proposed CB-DPWM and SV-DPWM for the 3-level AT-NPC, simulation and experiment are performed under the parameters listed in Table 4.

The simulation results of the CB-DPWM and SV-DPWM techniques for the 3-level AT-NPC inverter are demonstrated in Fig. 8a and 8b, respectively. In which, the line voltage between the 3-level legs is called V33; V32 is the line voltage between the 3-level leg and the 2-level leg. The THD quality of the V33 under both DPWM strategies is equivalent. For the CB-DPWM technique, the quality of the V32 output voltage is greatly reduced. It is significantly improved when applied SV-DPWM algorithm. For example, at modulation index  $m = 0.4$ , the THD of V32 is 85.8% and 128.9% for SV-DPWM and CB-DPWM, respectively, an improvement of about 34%. Similarly, the reduction is about 14% for the SV-DPWM method at index mode  $m = 0.9$ .

TABLE 4  
PARAMETERS FOR SIMULATION AND EXPERIMENTAL

Parameter	Variable	Simulation	Experiment
DC supply source	$V_{dc}$	300 V	200V
Load resistance	$R$	1.5 $\Omega$	16 $\Omega$
Load inductance	$L$	3 mH	50 mH
Switching frequency	$f_{sw}$	5 KHz	5 KHz
Fundamental frequency	$f_0$	50 Hz	50 Hz

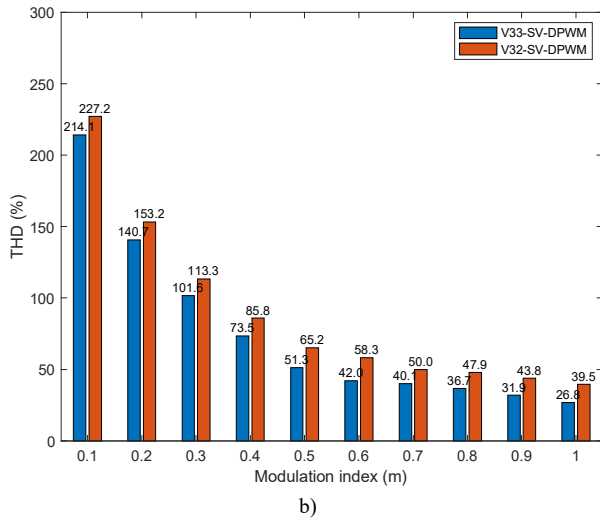
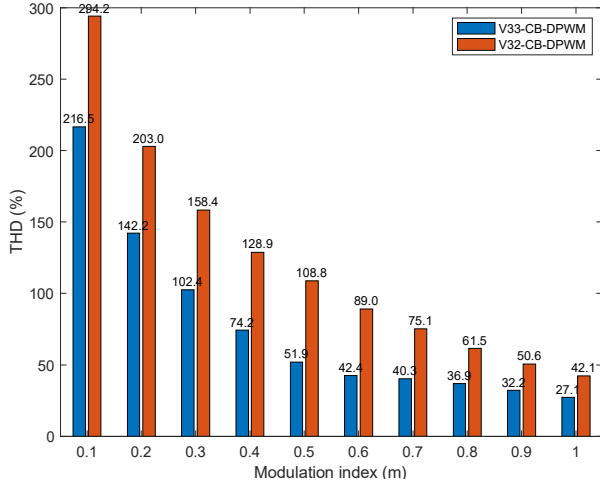


Fig. 8. The voltage THD of 3-level AT-NPC under (a) CB-DPWM, (b) SV-DPWM.

The average THD quality of line voltages can be defined by the following formula:

$$\overline{THD} = \sqrt{\frac{THD_{V_{AB}}^2 + THD_{V_{BC}}^2 + THD_{V_{CA}}^2}{3}} \quad (11)$$

The comparison graph of average THD between conventional 3-level T-NPC under the CB-DPWM technique and 3-level AT-NPC inverter under both proposed DPWM techniques is presented in Fig. 9. The CB-DPWM method provides good performance for conventional 3-level but not for 3-level AT-NPC inverter. For example, at modulation index  $m = 0.4$ , the average voltage THD is 74.2 % and 113.6 % for conventional 3-level and asymmetric 3-level, respectively.

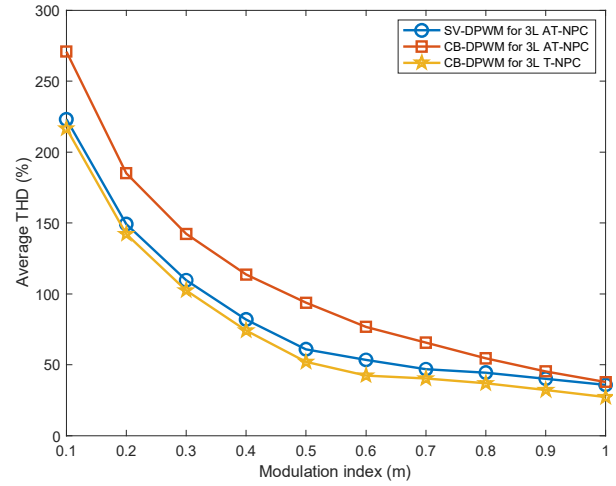


Fig. 9. THD comparison graph between traditional 3-level T-NPC under CB-DPWM and 3-level AT-NPC under CB-DPWM and SV-DPWM techniques.

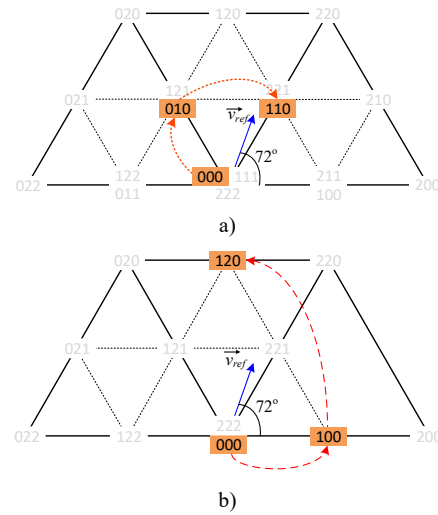


Fig. 10. The transition trajectory for (a) conventional 3-level T-NPC, (b) 3-level AT-NPC.

Observing the transition trajectories between voltage vectors in vector space, as illustrated in Fig. 10a at instant  $72^\circ$  with  $m = 0.4$ , the CB-DPWM technique for the traditional 3-level configuration synthesizes the reference vector in terms of the three nearest vectors. But when applying this technique for the AT-NPC configuration, the THD quality is worse because the reference vector is no longer synthesized by the three nearest vectors, as depicted in Fig. 10b. For the proposed SV-DPWM strategy, the discontinuous switching pattern is designed to ensure that the reference voltage vector is synthesized by the three nearest vectors. As a result, the THD quality is improved to almost equal to the conventional 3-levels.

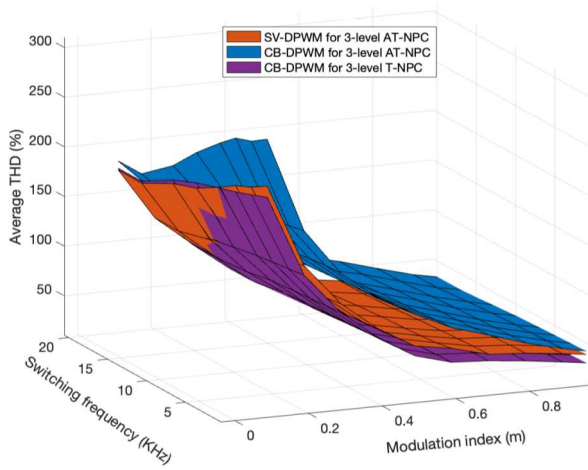


Fig. 11. Comparison of average THD characteristics in relation to modulation index and switching frequency.

The graph comparison of average THD characteristics related to modulation index and switching frequency is indicated in Fig. 11. As observed, the CB-DPWM strategy gives good THD performance for conventional 3-level T-NPC but not for 3-level AT-NPC. The THD quality of AT-NPC is improved almost equivalent to that of the conventional 3-level when applying the proposed SV-DPWM technique.

Similar tests on the experimental model are also conducted to verify the proposed algorithms. Figures 12 and 13 show the line voltage and current waveforms at modulation index  $m = 0.4$  and  $m = 0.9$ , respectively.

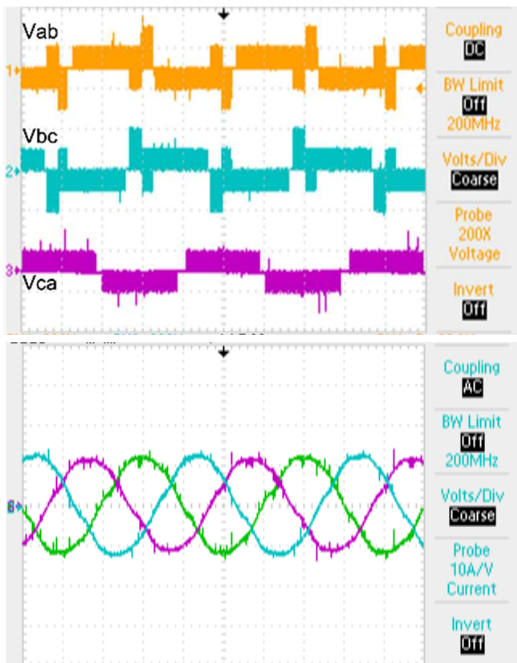


Fig. 12. Experimental waveform results of 3-level AT-NPC inverter under SV-DPWM technique at  $m=0.4$

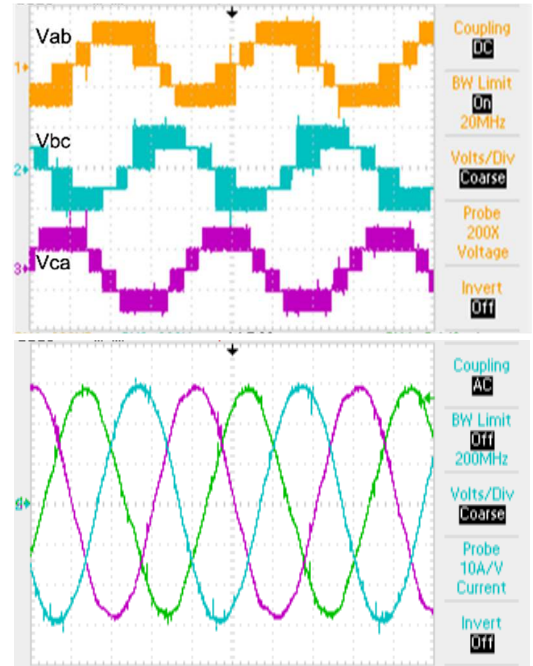


Fig. 13. Experimental waveform results of 3-level AT-NPC inverter under SV-DPWM technique at  $m=0.9$

The graph comparison of the line voltage quality of CB-DPWM and SV-DPWM for the 3-level AT-NPC inverter is shown in Fig. 14. Experimental results also show that the THD quality of V33 is similar for both methods, and V32 of the SV-DPWM technique is significantly improved compared to CB-DPWM method. For example, at modulation index  $m = 0.6$ , the THD of V33 is about 46%, and the THD of V32 is about 55% and 80% for SV-DPWM and CB-DPWM techniques, respectively.

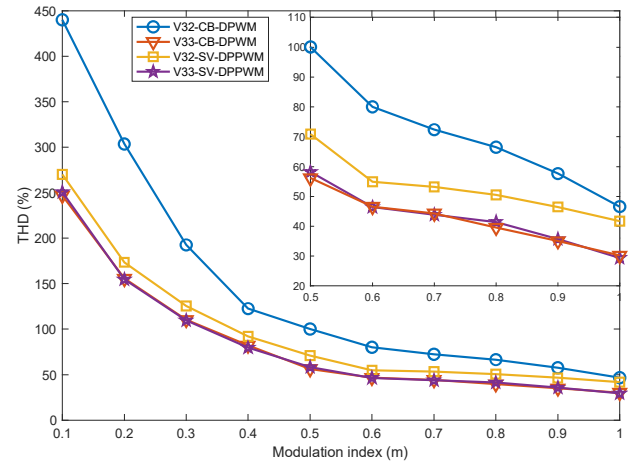


Fig. 14. THD comparison between CB-DPWM and SV-DPWM techniques for AT-NPC inverter

## V. CONCLUSION

This paper studies discontinuous PWM techniques for 3-level asymmetrical T-NPC inverter configuration. First, the model of the AT-NPC 3-level inverter is presented. Next, the offset function calculation and CB-DPWM implementation method are introduced. Another proposal based on the SV-DPWM strategy using the three nearest vectors is presented in detail. Finally, the analysis and evaluation of the performance of each method through

simulation and experimental results are discussed. A comparison between the two methods for 3-level AT-NPC inverter with 3-level T-NPC inverter using the CB-DPWM technique was also conducted. The SV-DPWM control performance for AT-NPC 3-level inverter can achieve close THD quality of conventional 3-level inverter.

#### ACKNOWLEDGMENT

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