Extended Balancing and Dimensioning of Capacitors in MMC Double Submodules

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***Abstract*—The Double-Zero Submodule in Double Connection (DZDCSM) is one of the most promising submodule topologies for future Modular Multilevel Converter (MMC) applications. Internal paralleling of semiconductors and capacitors in the DZDCSM during the time spans of high load currents results in low losses and reduced energy pulsation. Furthermore, full controllability of the capacitors enables their critical balancing in a passive and lossless manner. This paper presents an analytical investigation of the internal balancing process as well as the energy pulsation reduction in the full operating range of the MMC utilizing the DZDCSM. A simulation, applying the nearest level modulation and a basic sorting algorithm, verifies the general energy pulsation reduction in comparison to a conventional Full-Bridge Submodule (FBSM).**

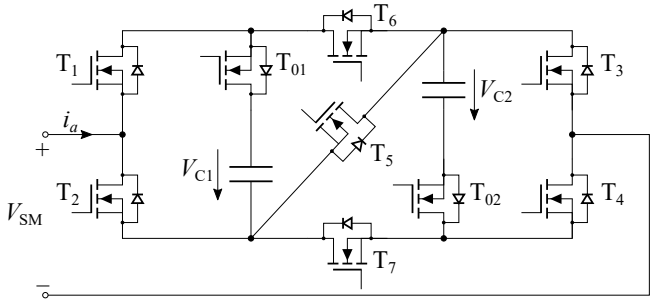


Fig. 1. Topology of the Double-Zero Submodule in Double-Connection equipped with SiC-MOSFET

I. Introduction

The Modular Multilevel Converter (MMC) has proven itself as the most reliable Voltage-Source Converter (VSC) for high-voltage applications and provides technical freedom to fulfill requirements of future meshed HVDC and MVDC grids [1]. On this account, advanced submodule topologies have been introduced that aim at reducing power losses and capacitor size while maintaining the DC fault blocking capability, as well as enhancing the submodule reliability [2]–[5]. One promising topology is that of the Double-Zero Submodule (DZSM), which has a full-bridge functionality and a controllable capacitor, offering a reduction of power losses, especially when employing SiC semiconductors [6]–[8]. In addition, the switchable capacitor offers an improved electronic protection against failures within the submodule.

Further reduction of semiconductor losses as well as reduction of capacitor energy pulsation can be achieved when applying the principle of a double connection of two DZSM resulting in the Double-Zero Submodule in Double Connection (DZDCSM). This topology is shown in Fig. 1 and features four terminal voltage levels (state (2): $+2V_C$, state (1): $+V_C$, state (0): 0 V, state (-1): $-V_C$) [5], [7]. The switching states are illustrated in Fig. 2 for both arm current directions. The switching state (2), where both capacitors C_1 and C_2 are connected in series, can cause a voltage imbalance between the capacitors due to capacitance tolerances. However, C_1 and C_2 can be passively balanced in the following switching state (1). Considering the initial condition $V_{C1} > V_{C2}$ at the beginning of state (1), the capacitor C_2 will be charged during state (1) (blue current path in Fig. 2), if the arm current is positive ($T_{6,7} = 1$, $T_{01,02} = 0$). On the other hand, the capacitor C_1 will be discharged during state (1) (green current path in Fig. 2), if the arm current is negative ($T_{6,7} = 0$, $T_{01,02} = 1$). The soft paralleling ($T_{6,7,01,02} = 1$) can be initiated at almost zero voltage difference, resulting in neglectable commutation and equalization losses [8]. The capacitor voltages can also be balanced in state (-1) but only for a negative arm current. If there is a remaining voltage difference between C_1 and C_2 when switching to state (-1) at a positive arm current, parallel connection of the capacitors can only be achieved by hard paralleling. This would result in high equalization currents that should be avoided in order to keep the semiconductor devices within the safe operating area.

In this paper, a detailed study of the balancing capability of the DZDCSM is carried out, covering the complete area of practically relevant operating points. Furthermore, different mechanisms are proposed to avoid hard paralleling in case state (1) ends with unbalanced voltages. Finally, a general analytical investigation of the energy pulsation is presented and put in perspective with a simulation of an MMC arm. In this manner, a universal comparison regarding the capacitor size of the DZDCSM and a conventional Full-Bridge Submodule (FBSM) will be extracted.

II. Balancing of capacitor voltages

Assuming capacitors with a nominal capacitance C_0 and a relative tolerance $\pm\epsilon$, the capacitor voltages and the voltage

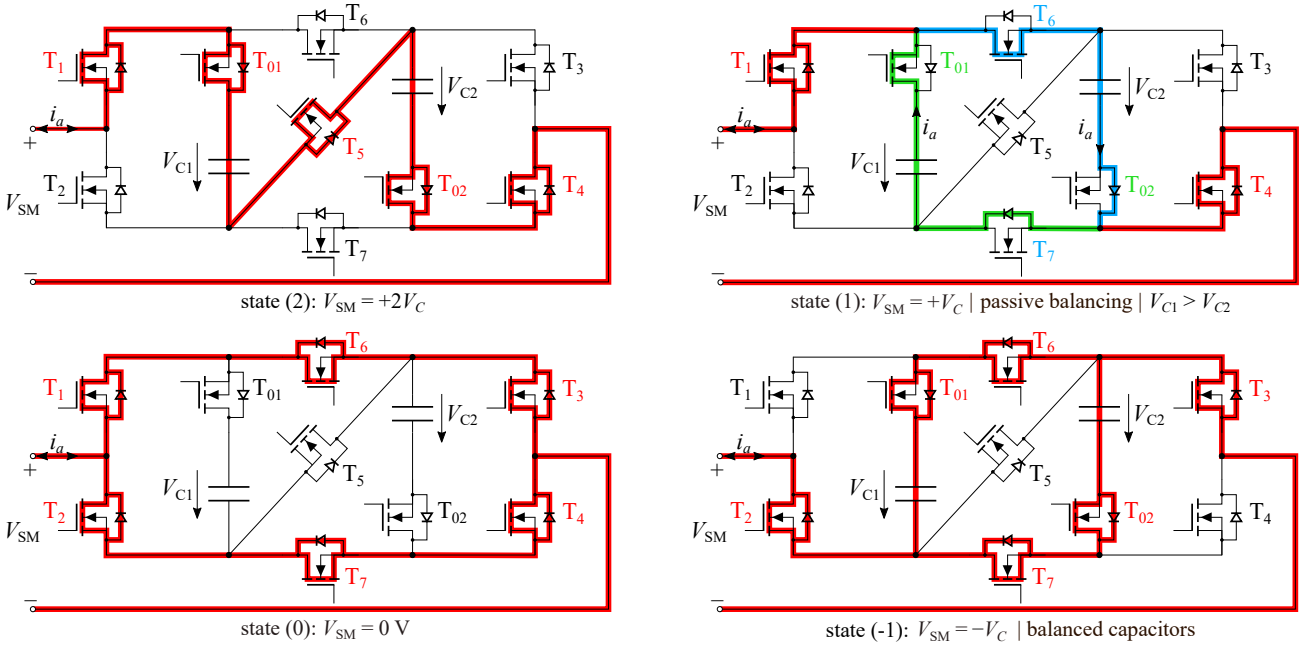


Fig. 2. Switching states of the DZDCSM

imbalance at the end of state (2) can be expressed as

$$\frac{V_{C1}|_{t_{x1}}}{\hat{i}_{\mathrm{AC}}/C_0} = (1+\epsilon)\int_{t_{x0}}^{t_{x1}} i'_{\mathrm{a}}(t)\,dt + \frac{v_C|_{t_{x0}}}{\hat{i}_{\mathrm{AC}}/C_0}, \tag{1}$$

$$\frac{V_{C2}|_{t_{x1}}}{\hat{i}_{\mathrm{AC}}/C_0} = (1-\epsilon)\int_{t_{x0}}^{t_{x1}} i'_{\mathrm{a}}(t)\,dt + \frac{v_C|_{t_{x0}}}{\hat{i}_{\mathrm{AC}}/C_0}, \tag{2}$$

$$\frac{\Delta V_C|_{t_{x1}}}{\hat{i}_{\mathrm{AC}}/C_0} = 2\epsilon\int_{t_{x0}}^{t_{x1}} i'_{\mathrm{a}}(t)\,dt, \tag{3}$$

where i'_{a} is the arm current (example: upper arm)

$$i'_{\mathrm{a}}(t) = \frac{i_a(t)}{\hat{i}_{\mathrm{AC}}} = \frac{1}{4}k\cos(\varphi_i) + \frac{1}{2}\sin(\omega t - \varphi_i) \tag{4}$$

normalized to the peak value of the AC current, neglecting the circulating currents. The modulation factor k is defined as the ratio of the fundamental AC-voltage peak value ($\hat{v}_{\mathrm{SM,AC},1}$) to the DC voltage ($V_{\mathrm{SM,DC}}$) generated by the submodule and the arm [7]

$$k = \frac{\hat{v}_{\mathrm{SM,AC},1}}{V_{\mathrm{SM,DC}}} = \frac{\hat{v}_{\mathrm{a,AC},1}}{V_{\mathrm{a,DC}}}. \tag{5}$$

Assuming a basic 4-level pulse pattern (see Fig. 4a), the generated voltage difference ΔV_C during state (2) can be nullified in the following state (1). This can be achieved if a charge ΔQ_{bal} is fed into the capacitor with the smaller voltage or extracted from the one with the higher voltage for the balancing. Since their capacitances are not equal, ΔQ_{bal} differs depending on the current direction

$$\mathrm{sgn}(\Delta Q_{\mathrm{bal}}) = \begin{cases} +1 & , i'_{\mathrm{a}} > 0 \\ -1 & , i'_{\mathrm{a}} < 0. \end{cases} \tag{6}$$

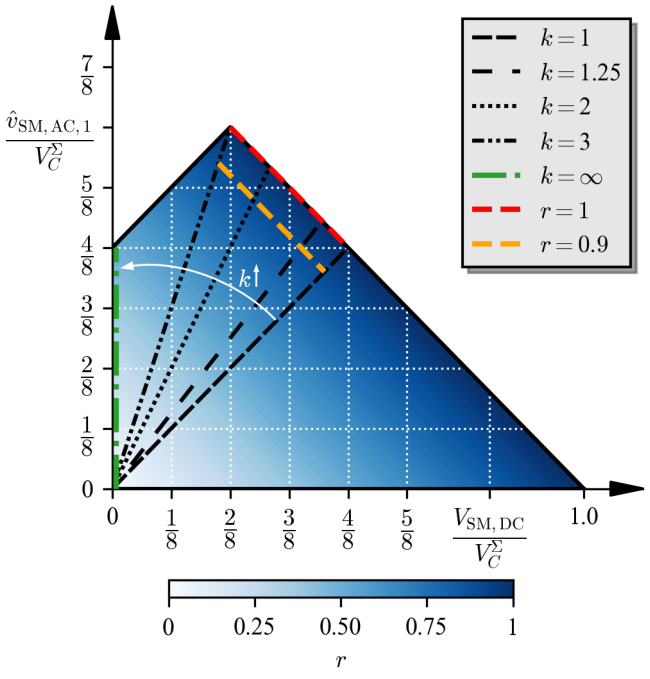
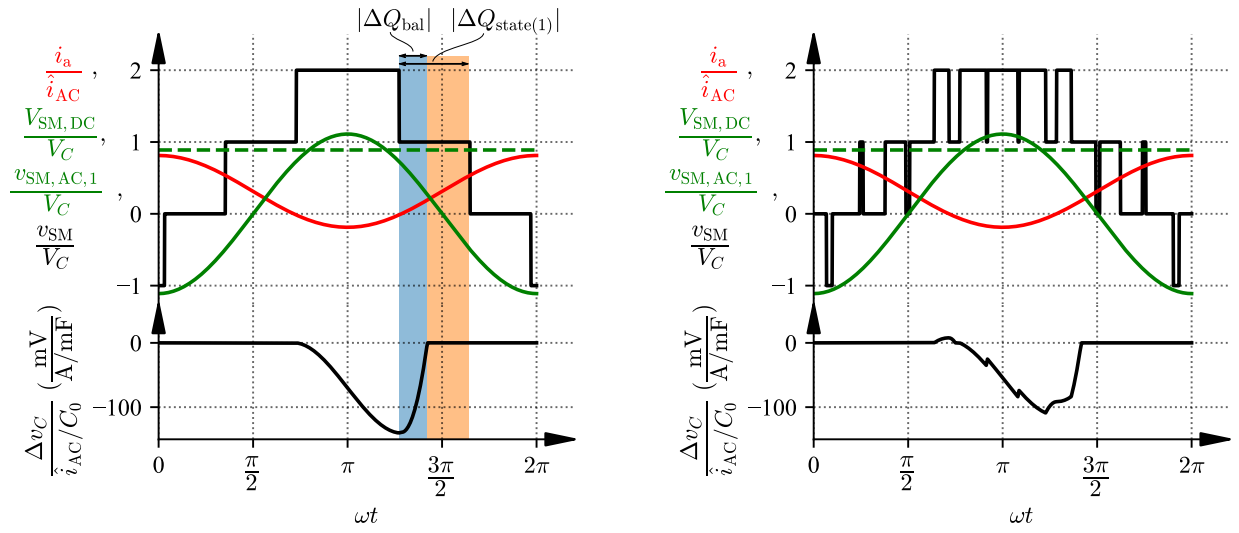


Fig. 3. Operation range of the DZDCSM applying a linear modulation scheme, the color map denotes the utilization factor of the DZDCSM

ΔQ_{bal} can be normalized to the net charge available in state (1)

$$|\Delta Q'_{\mathrm{bal}}| = \frac{|\Delta Q_{\mathrm{bal}}|}{|\Delta Q_{\mathrm{state(1)}}|}. \tag{7}$$

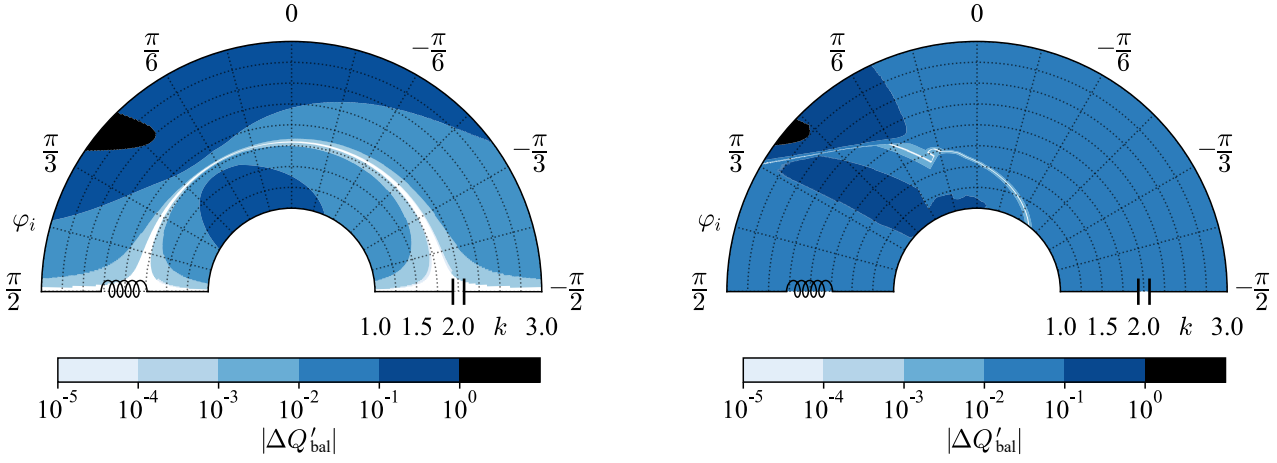
For a better clarity, the time spans of $|\Delta Q_{\mathrm{bal}}|$ and $|\Delta Q_{\mathrm{state(1)}}|$



(a) Block modulation

(b) PSC-PWM

Fig. 4. Example of a balancing process applying different modulation schemes with the same utilization factor | $k = 1.25$, $r = 1$, $\cos\varphi_i = 1$, $\epsilon = 10\%$



(a) Block modulation

(b) PSC-PWM

Fig. 5. Charge amount required to balance the capacitors in state (1) normalized to the net charge available in state (1) (see Eq. 7) | $\epsilon = 10\%$, operating points according to dashed red line in Fig. 2

are indicated exemplary in Fig. 4a. It can be noted, that in this operating point the ratio $|\Delta Q'_{\mathrm{bal}}|$ is less than unity and therefore a complete balancing is achieved in state (1).

A. Evaluation of the balancing capability

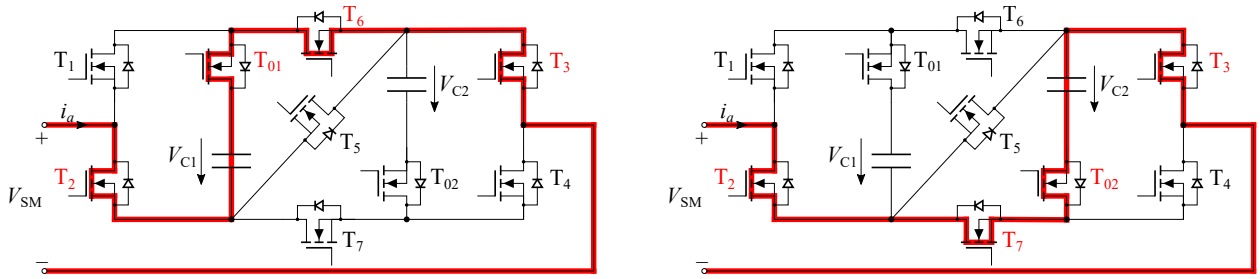
In order to quantify the balancing capability of the DZ-DCSM, operating points have to be defined. Fig. 3 illustrates the operating region of the submodule when using a linear modulation scheme such as phase-shifted carrier modulation (PSC-PWM). The operating points along the red dashed line are chosen for this investigation, where the generated AC and DC voltages for a given k and the voltage imbalance generated in state (2) are maximized (worst case for the balancing process). The blue color gradient denotes the utilization factor of the submodule

$$r = \frac{\hat{v}_{\mathrm{SM,AC,1}} + V_{\mathrm{SM,DC}}}{V_C^{\Sigma}} = \frac{\hat{v}_{\mathrm{a,AC,1}} + V_{\mathrm{a,DC}}}{n_{\mathrm{SM}} \cdot V_C^{\Sigma}}, \tag{8}$$

where V_C^{Σ} describes the the sum of submodule capacitor voltages within one submodule and n_{SM} the number of submodules within an arm.

Fig. 4a and Fig. 4b show normalized waveforms of submodule terminal voltages and arm currents, calculated for a typical operating point applying block modulation and PSC-PWM, respectively. Note, that both schemes generate the same DC and AC voltage levels. As can be seen, the voltage difference generated in state (2) is balanced out during state (1) before coming to the switching state (-1).

In Fig. 5 $|Q'_{\mathrm{bal}}|$ is plotted as a function of k and φ_i for a wide range of operating points applying block modulation



(a) $V_{C1} < V_{C2}$ (b) $V_{C1} > V_{C2}$

Fig. 6. Additional switching states for inserting the submodule in state (-1) with unbalanced voltages and $i_a > 0$

and PSC-PWM. The blue color gradient denotes the success of the balancing process within state (1). Solely in the black colored areas of the operating region, the balancing process does not finish during state (1). Note, that a good design of an MMC, equipped with submodules that have full-bridge functionality, is typically in the range $1.0 < k < 1.5$ where the arm energy pulsation, crucial for the capacitor size, and the semiconductor losses, are low. In this region the balancing process ends successfully and efficiently. However, the "black" region is present at $k > 2.3$ and $\frac{\pi}{6} > \varphi_i > \frac{\pi}{3}$ for both schemes investigated. These are not typical operating points but might be encountered during transients. Also during DC side failures, where the MMC can work as a STATCOM while maintaining the AC voltage and driving the DC voltage to zero (e.g. this corresponds to a horizontal line in Fig. 3 drawn from $k = 1.25 \mid r = 0.9$ to $k = \infty$), the normal passive balancing performs well. However, in order to deal with the problem of unbalanced capacitors in the "black" region, mechanisms to force the balancing need to be considered. This is important for enhancing the submodule availability over all operating points.

B. Mechanisms to avoid hard paralleling of C_1 and C_2 in state (-1)

As already mentioned, state (1) can be utilized to balance the capacitor voltages in a wide area of MMC operating points. Nonetheless, procedures to deal with incompletely balanced voltages have to be considered to avoid a hard paralleling of C_1 and C_2 in state (-1). Therefore, three possible approaches will be investigated in the following.

1) Inserting only one capacitor in state (-1): A straightforward approach to avoid a hard paralleling in state (-1) due to unbalanced capacitor voltages and $i_a > 0$ would be to insert only one capacitor instead of the parallel connection of C_1 and C_2. Considering that, there exist two possible switching states, illustrated in Fig. 6, for $V_{C1} < V_{C2}$ and $V_{C1} > V_{C2}$. As can be seen, only the capacitor with the smaller voltage can be inserted and, as a result, the remaining ΔV_C from state (1) will be increased instead of decreased, unfortunately.

Fig. 7 illustrates this issue for an operating point from the "black" region of Fig. 5a, where the lower diagram indicates the voltage imbalance in the initial period as a solid line and in the following period as a dashed line, i.e. its initial value

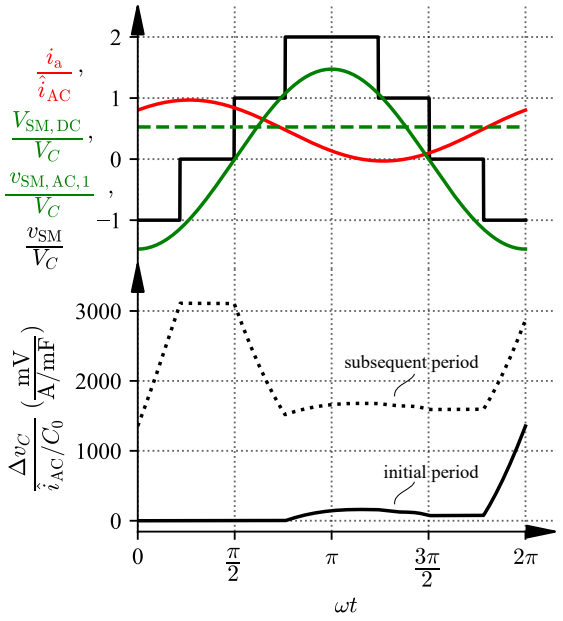


Fig. 7. Inserting only one capacitor of the DZDCSM in state (-1) with existing voltage imbalance | operating point from the "black" region of Fig. 5a according to Tab. I

is given from the previous period. Since the current-time area of the arm current is larger during state (-1) in contrast to state (1), the voltage imbalance would continue to increase over the periods, e.g. $\Delta V_C/V_{C0}$ would be 20 % at the end of the initial period for $\hat{i}_{AC} = 1.5$ kA and $V_{C0} = 2$ kV. Hence, this approach is not suitable for the voltage balancing. Note, that inserting the capacitor with the higher voltage (activating $T_{7,02}$ instead of $T_{6,01}$ in Fig. 6a) leaves no remaining diode in the blocking direction and thus leads to a high equalization current, which is not an option here.

2) Applying an extended balancing control: Considering an MMC arm equipped with DZDCSM, it is possible to extend the voltage-balancing algorithm used for inserting the submodules with a control scheme that ensures the passive balancing of each submodule over a complete period. For explanation, an MMC arm will be investigated in an operating point from the "black" region of Fig. 5a, see Tab. I.

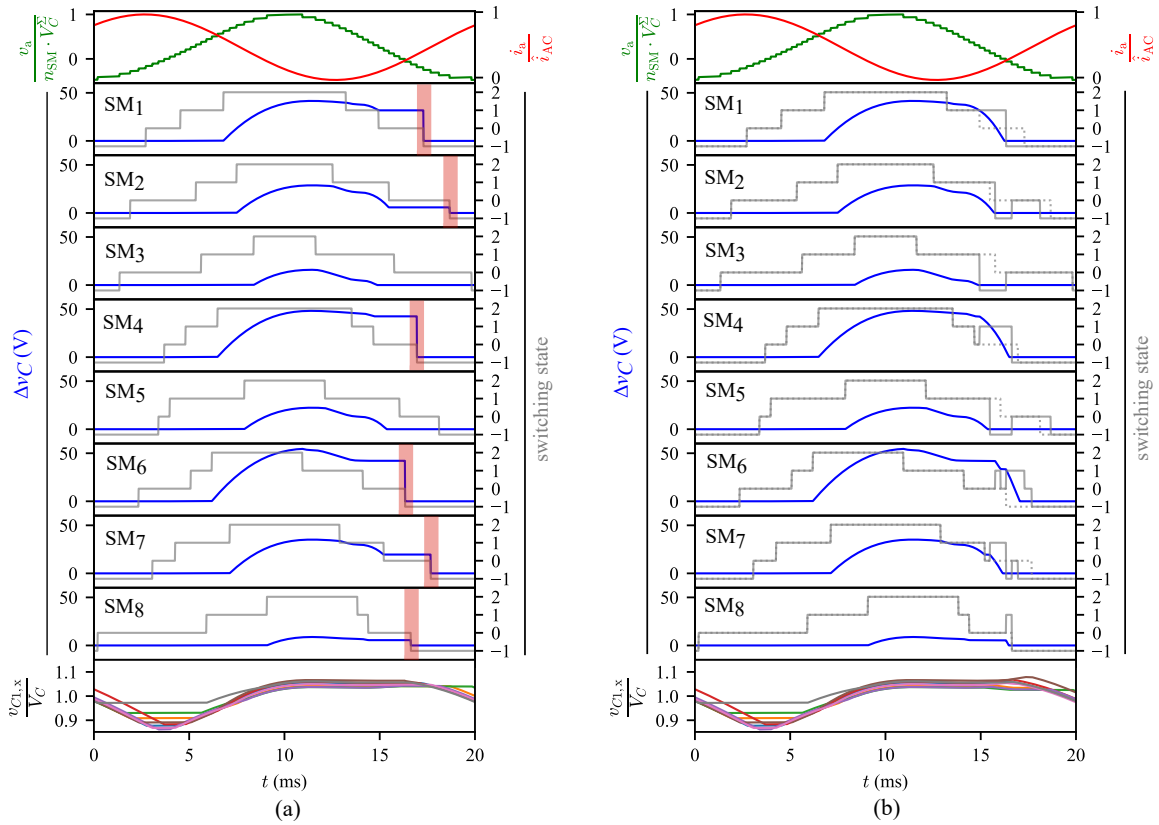


Fig. 8. (a): Operation of an MMC arm in the operating point specified in Tab. I, where the normal passive balancing does not finish successfully, (b): extending the voltage-balancing algorithm with a control scheme to enable the passive balancing (dashed line: original pulse pattern, solid line: modified pulse pattern)

TABLE I
OPERATING POINT FROM THE "BLACK" REGION OF FIG. 5A FOR INVESTIGATING ALTERNATIVE BALANCING STRATEGIES FOR THE DZDCSM

Parameter	Value
k	2.8
φ_i	48°
n_{SM}	8
ϵ	10 %
C_0	5 mF
C_1	4.54 mF
C_2	5.5 mF

The upper, middle and lower sections of Fig. 8a illustrate waveforms of the arm current and modulated voltage, the switching states of each submodule with the corresponding capacitor voltage imbalance and the submodule voltages, respectively. The nearest-level modulation (NLM) is used to realize a minimal submodule switching frequency of 150 Hz. A voltage-balancing algorithm within the arm for sorting the capacitor voltages is applied to keep the average of submodule capacitor voltages at a constant value. As can be seen from Fig. 8a, six submodules are switched to the state (0), while ΔV_C is not completely nullified. In the following state (-1) the capacitors are inserted in parallel resulting in high equalization currents due to the remaining ΔV_C that should be avoided. The voltage-balancing algorithm should be adjusted in such a way, that the submodules are enabled to complete the balancing of their capacitors before entering the switching state (-1).

To achieve this objective, when the modulation triggers a reduction of one level of the modulated voltage, then only balanced submodules should be first switched from state (1) to (0) or to (-1) to let unbalanced submodules complete balancing their capacitors by remaining in state (1) or switching from state (0) back to (1). As can be seen from Fig. 8b, the balanced SM_3 is switched from state (1) to (-1) while SM_1 is retained in state (1) for the balancing together with SM_4, which is switched back from state (0) to (1). In the same manner, many switching operations can be performed for the purpose of balancing, when the modulation triggers. However, the net level reduction should be always equal to unity. Following this approach, a complete passive and lossless balancing can be achieved by the end of the period. The strategy leads to an increase of the average submodule switching frequency (in this example from 150 Hz to 200 Hz). However, as mentioned above, this is not a typical operating point of the MMC but could only occurs in infrequent situations such as transient events.

3) Equipping the DZDCSM with discharging resistors: The DZDCSM can be extended with two switchable resistors (see Fig. 9), that can be used

- to enable a voltage balancing of the capacitors by dis-

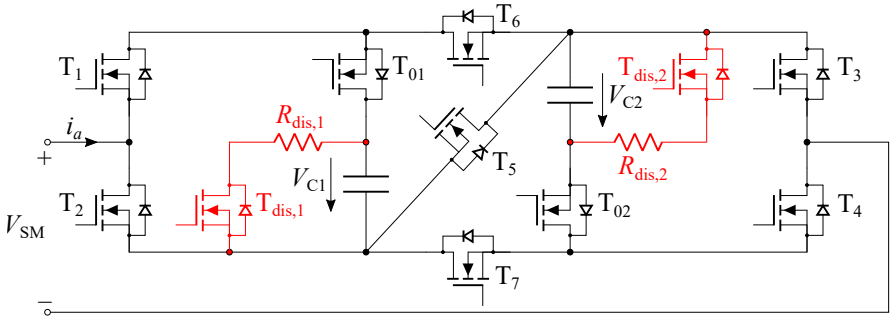


Fig. 9. The Double-Zero Submodule in Double-Connection extended with two switchable discharging resistors highlighted in red

charging the capacitor with the higher voltage to the level of the other one and

- for discharging the capacitors after a failure within the submodule for enhancing the submodule reliability.

The capacitor balancing using the discharging resistors should take place in state (0) in case state (1) ends with unbalanced capacitor voltages. Defining a time span t_{dis} for the balancing process, the required resistance can be calculated by

$$R_{\mathrm{dis,i}} = \frac{t_{\mathrm{dis}}}{C_{\mathrm{i}} \cdot \ln\left(\frac{V_{C_{\mathrm{i0}}}}{V_{C_{\mathrm{i0}}} - \Delta V_C}\right)}, \tag{9}$$

where $\mathrm{i} = 1, 2$. In this time an energy amount of

$$E_{\mathrm{dis,i}} = \frac{1}{2} \cdot C_{\mathrm{i}} \cdot \left(V_{C\mathrm{i}}^2(t_0) - V_{C\mathrm{i}}^2(t_0 + t_{\mathrm{dis}})\right) \tag{10}$$

would be dissipated over the resistor. If designed to dissipate the total capacitor energy after a failure within the submodule, the resistors should be able to handle the balancing power during transients for a sufficient amount of time.

To give an estimation of the energy loss, the example of the balancing shown in Fig. 8 will be used. Thereby, the submodules switched to state (0) with existing voltage imbalance between their capacitors will use the discharging resistors for the balancing. The sum of the discharging losses can be normalized to the total arm capacitor energy

$$E'_{\mathrm{dis}} = \frac{\sum E_{\mathrm{dis}}}{n_{\mathrm{SM}} \cdot \frac{1}{1-\epsilon^2} \cdot C_0 \cdot V_{C_0}^2} = 0.88\ \%. \tag{11}$$

This value depends also on $\hat{\imath}_{\mathrm{AC}}$, that drives the magnitude of ΔV_C.

After introducing the three strategies for the balancing, it can be concluded that only the strategies of *2)* and *3)* can be applied. Both strategies *2)* and *3)* cause little extra losses. Introducing discharging resistors is generally valuable in terms of enhancing the submodule reliability and solving the balancing on submodule level. For pure balancing purposes, the extended balancing algorithm also performs well.

III. Investigation of Submodule Capacitor Energy Pulsation

As already mentioned in the introduction of this paper, the DZDCSM offers many benefits in comparison to conventional FBSM such as the reduction of power losses, enhancing the submodule reliability against failures through electronic protection as well as reducing the capacitor size. In [9] an analysis was carried out for comparing the energy pulsation – which has a direct impact on determining the capacitor size [10]–[13] – of one DZDCSM with two FBSM connected in series based on predefined pulse patterns for switching the submodules. It was assumed that all submodules within the arm are switched in the same manner as the investigated submodules. It was shown, that the capacitor size of the DZDCSM can be reduced by 50% compared to FBSM at specific operating points. However, in practical applications the switching states of the submodules for synthesizing the arm voltage are set by the voltage-balancing algorithm. The main task of this procedure is to ensure the equal share of power between all submodules while maintaining a constant switching frequency of the submodules. In this section an analysis for calculating the energy pulsation is introduced, considering all submodules within one MMC arm and taking the working principle of the voltage-balancing algorithm into account. The analysis results will be compared with simulation results.

A. Calculation of normalized arm power

In order to generalize the analysis, calculating the power of an MMC arm in a normalized form is fundamental, viz.

$$p'_a(t) = v'_a(t) \cdot i'_a(t). \tag{12}$$

The normalized arm current i'_a was already given in (4). The arm voltage v_a consists of an AC und DC component

$$v_a(t) = V_{\mathrm{a,DC}} - \hat{v}_{\mathrm{a,AC,1}} \sin(\omega t). \tag{13}$$

The DC component and AC-peak value can be described as functions of the peak value of the arm voltage $\hat{v}_a$ and the modulation factor k

$$V_{\mathrm{a,DC}} = \frac{1}{k+1} \hat{v}_a, \tag{14}$$

$$\hat{v}_{\mathrm{a,AC,1}} = \frac{k}{k+1} \hat{v}_a. \tag{15}$$

Substituting (14) and (15) into (13) yields

$$v_a(t) = \frac{1}{k+1} \hat{v}_a (1 - k \cdot \sin(\omega t)). \tag{16}$$

$v_a(t)$ can be normalized to the sum of installed arm capacitor voltages

$$v'_a(t) = \frac{1}{(k+1)} \frac{\hat{v}_a}{n_{\mathrm{SM}} \cdot V_C^{\Sigma}} (1 - k \cdot \sin(\omega t)). \tag{17}$$

Applying (8) in (17) simplifies the equation of the normalized arm voltage further,

$$v'_a(t) = \frac{r}{k+1} (1 - k \cdot \sin(\omega t)), \tag{18}$$

which will be used in (12) to calculate the normalized arm power

$$p'_a(t) = \frac{r}{k+1} \Big[-\frac{1}{4} k^2 \cos(\varphi_i) \sin(\omega t) + \frac{1}{4} k \cos(2\omega t - \varphi_i) + \frac{1}{2} \sin(\omega t - \varphi_i) \Big]. \tag{19}$$

Fig. 10a illustrates the waveform of p'_a for a typical operating point of the MMC.

B. Definition of the insertion index

The insertion index a defines the ratio of inserted submodules within the arm ($V_{\mathrm{SM}} \neq 0$ V) to the number of installed submodules. For an arm equipped with FBSM the insertion index is defined as

$$a_{\mathrm{FBSM}}(t) = \frac{|v_{\mathrm{a}}(t)|}{n_{\mathrm{SM}} \cdot V_C^{\Sigma}}. \tag{20}$$

V_C^{Σ} describes the sum of submodule capacitor voltages within one submodule. Note, that the DZDCSM has to be compared to a series connection of two FBSM and therefore a differentiation of V_C^{Σ} has to be done, viz.

$$V_C^{\Sigma} = \begin{cases} V_C & \text{for FBSM,} \\ 2V_C & \text{for DZDCSM.} \end{cases} \tag{21}$$

The blue waveform in Fig. 10b illustrates a_{FBSM} according to (20).

Defining the insertion index for an MMC arm equipped with DZDCSM cannot be done straightforward as with FBSM, because there are two groups of DZDCSM that need to be considered when calculating the insertion index:

- $\mathrm{DZDCSM}_{\mathrm{parallel}}$: submodules whose capacitors are inserted in parallel (state (-1) and (1))
- $\mathrm{DZDCSM}_{\mathrm{series}}$: submodules whose capacitors are inserted in series (state (2))

Hence, two insertion indices will be defined, one for each group. The insertion index of the first group is defined as

$$a^{\mathrm{parallel}}_{\mathrm{DZDCSM}}(t) = \begin{cases} 2\frac{|v_{\mathrm{a}}(t)|}{n_{\mathrm{SM}} V_C^{\Sigma}} & , v_a(t) \leqslant \frac{1}{2} n_{\mathrm{SM}} V_C^{\Sigma}, \\ 2 - 2\frac{|v_{\mathrm{a}}(t)|}{n_{\mathrm{SM}} V_C^{\Sigma}} & , v_a(t) > \frac{1}{2} n_{\mathrm{SM}} V_C^{\Sigma}, \end{cases} \tag{22}$$

and its waveform can be seen in Fig. 10b (green waveform). At the instant $v_a(t) = \frac{1}{2} \cdot n_{\mathrm{SM}} \cdot V_C^{\Sigma}$ all submodules are inserted with parallel capacitors. When exceeding this point, some of those submodules will also be inserted with series-connected capacitors. Thus, the group $\mathrm{DZDCSM}_{\mathrm{series}}$ exists only when the modulated voltage is greater than the half of the total installed arm voltage

$$a^{\mathrm{series}}_{\mathrm{DZDCSM}}(t) = \begin{cases} 0 & , v_a(t) \leqslant \frac{1}{2} n_{\mathrm{SM}} V_C^{\Sigma}, \\ 2\frac{|v_{\mathrm{a}}(t)|}{n_{\mathrm{SM}} V_C^{\Sigma}} - 1 & , v_a(t) > \frac{1}{2} n_{\mathrm{SM}} V_C^{\Sigma}, \end{cases} \tag{23}$$

as can be seen from the orange waveform in Fig. 10b. Finally, the hybrid power share, illustrated in Fig. 10c, of both groups can be defined

$$p'(a^{\mathrm{series}}_{\mathrm{DZDCSM}}, t) = \frac{2a^{\mathrm{series}}_{\mathrm{DZDCSM}}(t)}{2a^{\mathrm{series}}_{\mathrm{DZDCSM}}(t) + a^{\mathrm{parallel}}_{\mathrm{DZDCSM}}(t)} p'_a(t), \tag{24}$$

$$p'(a^{\mathrm{parallel}}_{\mathrm{DZDCSM}}, t) = \frac{a^{\mathrm{parallel}}_{\mathrm{DZDCSM}}(t)}{2a^{\mathrm{series}}_{\mathrm{DZDCSM}}(t) + a^{\mathrm{parallel}}_{\mathrm{DZDCSM}}(t)} p'_a(t). \tag{25}$$

C. Analytical approach for calculating the energy pulsation

Considering an MMC arm, the task of the voltage modulation is to synthesize the arm voltage from the available voltage levels. The dynamic insertion of the submodules is carried out by the voltage-balancing algorithm that aims at keeping the mean voltage of the submodule capacitors at a constant value over the time. When applying a high switching frequency per submodule, the ripple of capacitor voltages can be reduced to considerably low values. However, if the submodule switching frequency is decreased towards the minimum, the ripple of capacitor voltages would increase as well as the deviation between the submodule voltages.

For a reasonable capacitor design, two insertion strategies will be introduced to estimate a potential range of the capacitor energy pulsation. The analytical approach will be first explained on the basis of a FBSM equipped MMC arm. The boundary conditions of this analysis are the following:

1) The MMC arm consists of a high number of submodules, so that the modulated voltage can be assumed to be continuous.
2) The submodules are switched with the minimal switching frequency, i.e. 50 Hz or 100 Hz for FBSM.

FBSM: In order to estimate the energy pulsation of the capacitors, the instantaneous power share of the inserted submodules within the arm has to be considered. This can be calculated by dividing the arm power by the associated insertion index

$$p'_{\mathrm{FBSM}}(t) = \frac{p'_{\mathrm{a}}(t)}{a_{\mathrm{FBSM}}(t)}. \tag{26}$$

The inserted submodules from time t_β to time t_γ (compare Fig. 10) would encounter a positive or negative alteration of their stored energy

$$\begin{aligned} \Delta \tilde{W}'_{\mathrm{FBSM}} &= \frac{1}{T_1} \int_{t_\beta}^{t_\gamma} p'_{\mathrm{FBSM}}(t) dt \\ &= \tilde{w}'_{\mathrm{FBSM}}(t_\gamma) - \tilde{w}'_{\mathrm{FBSM}}(t_\beta) \end{aligned}, \tag{27}$$

where T_1 is the fundamental period. The next step is to determine the dwell time of the inserted submodules (t_β and

t_γ). Since the minimum submodule switching frequency is presumed here, inserting the submodules with positive or negative terminal voltages happens only when the absolute arm voltage $|v_\mathrm{a}|$ increases. The inserted submodules can be bypassed only when the absolute arm voltage starts decreasing. Based upon the definition of t_β and t_γ, two cases (best case and worst case of the encountered energy pulsation) will be investigated.

The best case scenario will be explained using Fig. 10d. Assume that the first submodule is inserted at $v_\mathrm{a}(t_\beta) = 0$ when $|v_\mathrm{a}|$ starts increasing. This submodule can then be bypassed only when $|v_\mathrm{a}|$ reaches its maximum at t_γ. The maximum energy alteration ($\Delta\tilde{W}'^{min}_\mathrm{FBSM}$) encountered by this submodule during this period in the positive ($\Delta\tilde{W}'^{min+}_\mathrm{FBSM}$) or negative ($\Delta\tilde{W}'^{min-}_\mathrm{FBSM}$) range of v_a is the largest single energy rise, which is unavoidable. All other submodules inserted and bypassed later during the investigated fundamental period experience smaller energy pulsations. However, since the net energy exchange over the fundamental period per submodule is not necessarily zero – as it is for the complete converter arm during steady state – the energy levels of the individual submodules are slowly shifted and the voltage-balancing algorithm cannot limit the energy pulsation of the submodules to $\Delta\tilde{W}'^{min}_\mathrm{FBSM}$. Hence, the considered case is a boundary condition that cannot be avoided.

In the same manner, a maximum energy pulsation ($\Delta\tilde{W}'^{max}_\mathrm{FBSM}$) can be determined, that might not be exceeded during operation. This corresponds to inserting a submodule for the complete dwell time between two zero crossing points of the arm voltage allowing a high energy pulsation, see Fig. 10e. At this operating point $\Delta\tilde{W}'^{max}_\mathrm{FBSM}$ is located in the negative voltage range ($\Delta\tilde{W}'^{max-}_\mathrm{FBSM}$), Finally, the real energy pulsation of a FBSM within an MMC arm equipped with an integer number of submodules is expected to be between $\Delta\tilde{W}'^{min}_\mathrm{FBSM}$ and $\Delta\tilde{W}'^{max}_\mathrm{FBSM}$.

DZDCSM: Determining a maximum and a minimum band for the energy pulsation ($\Delta\tilde{W}'^{min}_\mathrm{DZDCSM}$ and $\Delta\tilde{W}'^{max}_\mathrm{DZDCSM}$) of the DZDCSM is far more complex. When speaking about the energy pulsation of the DZDCSM, only one of its capacitors is considered.

In Section III-B the insertion indices of the submodules inserted with parallel capacitors (group $\mathrm{DZDCSM_{parallel}}$) and with series capacitors (group $\mathrm{DZDCSM_{series}}$) as well as their power share within the arm were introduced. For determining $\Delta\tilde{W}'^{min}_\mathrm{DZDCSM}$ and $\Delta\tilde{W}'^{max}_\mathrm{DZDCSM}$ not only the inserting time of the submodule t_β as well as the bypassing time t_γ are important to know, but also the selection of the instantaneous group should be taken into account. Therefore, the time t_θ for switching the submodule from group $\mathrm{DZDCSM_{parallel}}$ to group $\mathrm{DZDCSM_{series}}$ as well as the time t_σ for switching it back to group $\mathrm{DZDCSM_{parallel}}$ should be defined.

For the best case scenario ($\Delta\tilde{W}'^{min}_\mathrm{DZDCSM}$) it is assumed that a submodule is switched on at $v_\mathrm{a}(t_\beta) = 0$ in the positive range of v_a. At the instant t_θ where the group $\mathrm{DZDCSM_{series}}$ starts to exist, the submodule is switched to the series connection until t_σ where it is switched back to group $\mathrm{DZDCSM_{parallel}}$. t_σ is

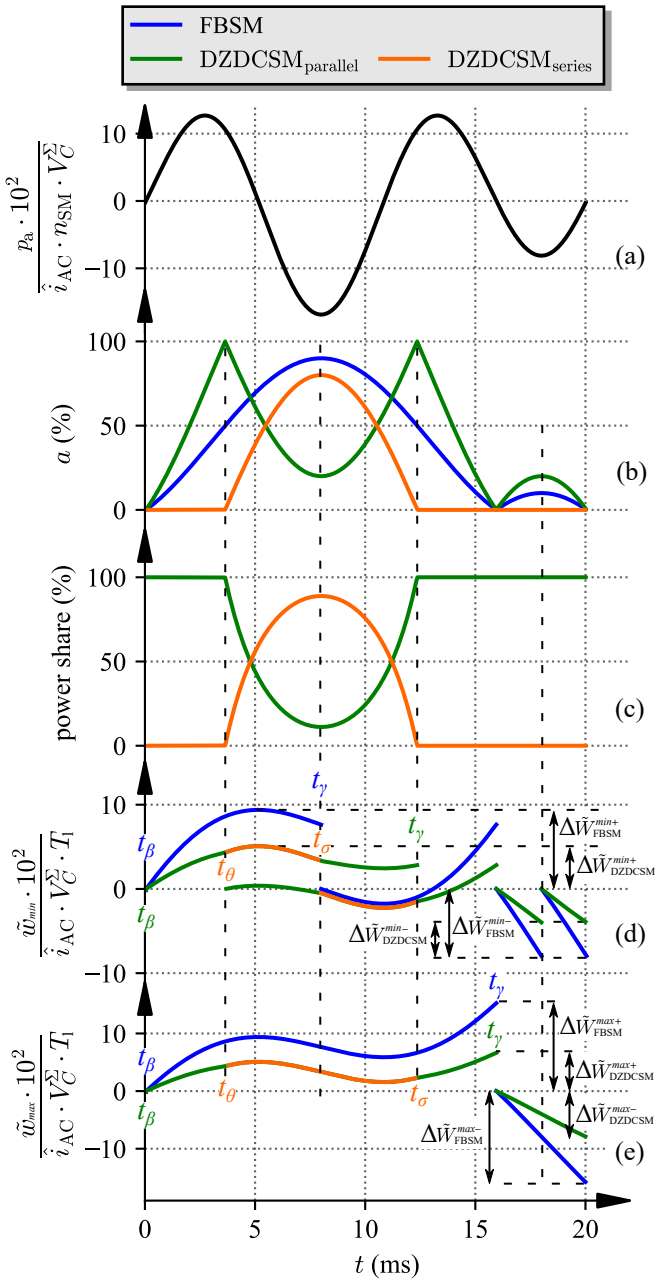


Fig. 10. (a): normalized arm power | (b): insertion indices of FBSM and DZDCSM | (c): percentage power share of the DZDCSM inserted with parallel and series connected capacitors within an arm | (d): minimum energy pulsation | (e): maximum energy pulsation | operating point: $k = 1.25, r = 0.9, \cos(\varphi) = 1$

the instant, where the group $\mathrm{DZDCSM_{series}}$ starts decreasing. The next time, where the submodule can be bypassed, is the time t_γ, where all submodules in group $\mathrm{DZDCSM_{series}}$ are switched back to group $\mathrm{DZDCSM_{parallel}}$ and the last one starts decreasing, see Fig. 10d. Thus, the submodule that sees the largest unavoidable energy pulsation during parallel insertion is selected, with the largest unavoidable pulsation during series insertion added on top. This is close, but not

precisely the best case. The variety of possible combinations during different operating conditions makes an analytical and general identification of the actual best case nearly impossible. The energy pulsation in the negative range of v_a can be calculated similar to FBSM, since in the negative range only the group DZDCSM$_\mathrm{parallel}$ exists. In Fig. 10d can be seen, that $\Delta\tilde{W}'^{min}_\mathrm{DZDCSM}$ exists in the positive range of v_a at the current operating point.

For defining the maximum energy pulsation $\Delta\tilde{W}'^{max}_\mathrm{DZDCSM}$ it is assumed that a submodule is inserted for the complete dwell time between two zero crossing points of the arm voltage. Furthermore, it will be switched to the group DZDCSM$_\mathrm{series}$, as long as this group exists allowing a high energy pulsation, see Fig. 10e. At this operating point $\Delta\tilde{W}'^{max}_\mathrm{DZDCSM}$ is located in the negative voltage range ($\Delta\tilde{W}'^{max-}_\mathrm{DZDCSM}$). Similar to the FBSM, it is expected for the energy pulsation of a DZDCSM within an MMC arm to be located between $\Delta\tilde{W}'^{min}_\mathrm{DZDCSM}$ and $\Delta\tilde{W}'^{max}_\mathrm{DZDCSM}$.

D. Comparison with the simulation

In this section the capacitor energy pulsation calculated using the analytical approach introduced above will be compared to simulation results. Fig. 11 illustrates the calculated upper and lower limits of the energy pulsation for the FBSM (▬ ▬) and for the DZDCSM (▬ ▬). As already mentioned, it is expected for the simulation results of every topology to be included in between the associated limits. The results of the simulation, which is performed using 16 FBSM (■) and 8 DZDCSM (■) applying NLM and a voltage-balancing algorithm are also illustrated in Fig. 11. The simulation results are generally placed between the proposed upper and lower limits of the energy pulsation – which verifies the consideration of the proposed approach – except in one operating point at $k = 1$ for the FBSM. This deviation is due to the fact, that in the simulation the arm voltage is modulated using 16 submodules and thus contains harmonics. These harmonics could be useful in terms of reducing the energy pulsation in some operating points like this one. Injecting harmonic components to the arm voltage and its impact on reducing the energy pulsation was not included in the proposed analytical approach.

For comparison, Fig. 11 also shows the energy pulsation of the DZDCSM according to the analytical approach of [9] (green curve), where a pulse pattern for switching one DZDCSM with 150 Hz is used to calculate the energy pulsation. The black curve in Fig. 11 indicates the ideal energy pulsation, assuming that all submodules take their power share synchronously at every instant (dividing the energy pulsation of the arm by the number of installed capacitors) [9]. This could theoretically be achieved, if the submodule switching frequency were infinite. The limits for the energy pulsation calculated with the proposed method are higher than the ideal energy pulsation. This is logical, because the submodules cannot share the power of the arm equally at every moment, if the switching frequency of the submodules is limited. The energy pulsations calculated following [9] are also similar to

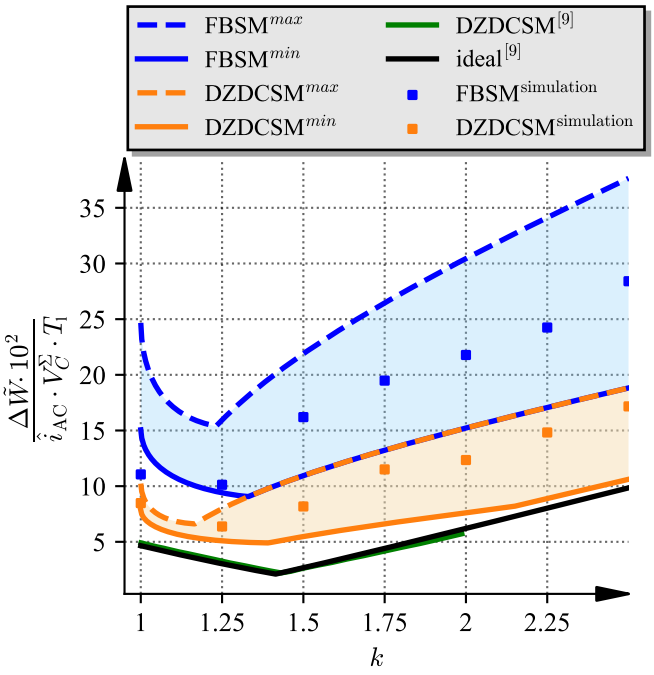


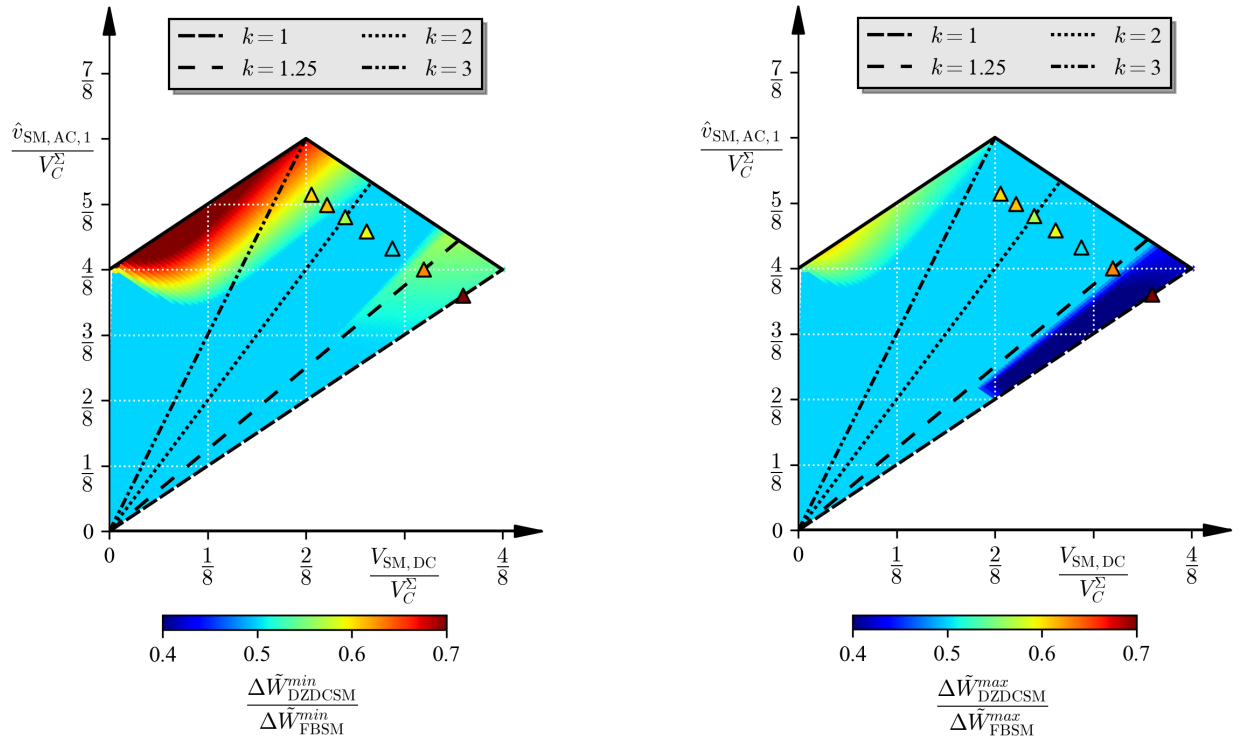
Fig. 11. Comparison of the introduced analytical approach for calculating an upper and lower limit for the energy pulsation with simulation results | $\cos(\varphi_i) = 1$ | $r = 0.9$

the ideal values, because all submodules within the arm are assumed to be switched with the same pattern.

Finally, the ratio of the energy pulsation of the DZDCSM to this of the FBSM is compared in Fig. 12a using the lower limits of the energy pulsation and in Fig. 12b using the upper limits. The ratio of the simulation results is also plotted in triangles using the same color scaling. It is evident, that the energy pulsation of the DZDCSM is generally smaller than the one of the FBSM. It can be noted, that the ratio is generally higher in the range where the modulation factor is also high. However, this is not a typical operating range for designing the MMC. The ratios calculated from the simulation are also higher than those from the analytical approach. This deviation is due to the fact, that only a limited number of submodules were used in the simulation and the impact of harmonics in the arm voltage on the energy pulsation was not considered in the analysis. Still, at a typical operating point, e.g. k = 1.25 | r = 0.9, the energy pulsation, and thus the capacitor size, could be reduced by 63% in the simulation and up to 50% according to the analytical approach compared to FBSM, if the arm consists of high number of submodules.

IV. Conclusion

The DZDCSM has shown an efficient voltage balancing capability of its capacitors in a wide area of MMC operating points. Still, there are operating points, where the arm voltage and current are phase shifted in such a way, that the voltage imbalance generated in state (2) cannot be passively and completely nullified in the following state (1). In order to avoid a hard paralleling of the capacitors, solutions to enable



(a) (b)

Fig. 12. Ratio of the energy pulsation of the DZDCSM and the FBSM calculated with the proposed approach | triangles denote the ratio calculated from the simulation results illustrated in Fig. 11 | $\cos(\varphi_i) = 1$

a complete balancing were introduced. Discharging resistors for dissipating the capacitor energies after a failure within the submodule can be also utilized for the voltage balancing. The introduced extended balancing algorithm is capable of achieving a passive balancing and ensuring a safe operation without the existence of equalization currents.

The capacitor energy pulsation of the DZDCSM was investigated and compared to this of the FBSM following an analytical approach, which defines an upper and lower limit for the energy pulsation. The results show that the energy pulsation of one capacitor of the DZDCSM is always smaller compared to this of the FBSM. In typical operating range of the MMC, the energy pulsation and thus the capacitor size reduction can be up to 50 %.

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