Impact of Bond Wire Configuration on the Power Cycling Capability of Discrete SiC-MOSFET Devices

Patrick Heimler, Nick Thönelt, Josef Lutz, Thomas Basler
CHEMNITZ UNIVERSITY OF TECHNOLOGY
Reichenhainer Straße 70
Chemnitz, Germany
Tel.: +49 / (0) 371–531 37907
Fax: +49 / (0) 371–531 837907
E-Mail: patrick.heimler@etit.tu-chemnitz.de
URL: https://www.tu-chemnitz.de/etit/le/

Keywords

«Power Cycling », «Discrete Power Device», «Reliability», «Silicon Carbide (SiC)», «MOSFET»

Abstract

This work investigates the power cycling capability of SiC MOSFETs (60 mΩ/1200 V) in TO-247-packages with two different bonding configurations. As a result, a difference in lifetime by a factor of 1.5 to 2 is determined. The failure mode was an increase in forward voltage drop by degradation of the bond wire connection. The ANSYS simulations (thermal-electrical and mechanical) confirm that several thinner bond wires have a higher power cycling capability compared to a few bond wires with larger diameters.

Introduction

In a power converter, SiC MOSFET devices achieve a higher efficiency compared to their Si equivalents [1]. Furthermore, the temperature dependency of $R_{DS(ON)}$ plays a major role in the application. It was found that SiC MOSFET devices exhibit a smaller increase in resistance compared to their Si counterparts for a temperature rise from 25 °C to 100 °C as an example [2]. Beside these advantages, reliability plays a decisive role. The power cycling test is an important method for accelerated lifetime investigations in order to evaluate the durability of interconnect technologies. This test is used for power modules as well as discrete devices. Therefore, 1.2 kV SiC MOSFETs with the same $R_{DS(ON)}$ and different bond wire configuration in discrete packages were investigated to evaluate their power cycling capability.

Test specimens

SiC MOSFETs from one manufacturer with two different numbers of bond wires and correspondingly different diameters in TO-247-package (see Figure 1) have been selected as test specimens. They have an identical blocking voltage of 1200 V, an $R_{DS(ON)}$ of 60 mΩ and a nominal current of 13 A, respectively. The configuration of the bond wires for test series A consists of 2*375 µm and for B of 3*250 µm bond wires.

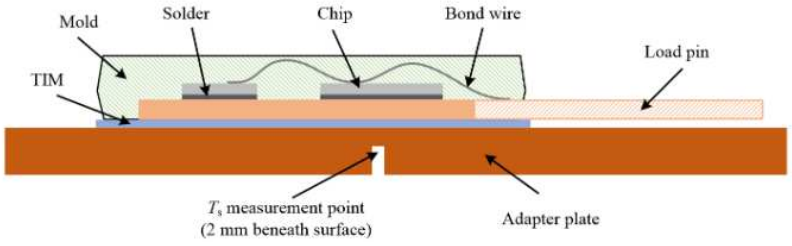

Figure 1: Schematic picture of a cross-section of TO-247 package. Figure from [3]

Results and Discussion

Junction temperature determination

The precise determination of the virtual junction temperature (T_{vj}) is an essential part of the power cycling test to ensure that statements on the determined lifetime are sufficiently accurate. This measurement is done during the test via the body diode with fully closed n-channel by using the $V_{CE}(T)$-method adapted to MOSFETs [4, 5, 6]. An insufficient low off-state gate voltage leads to shifts in the calibration curves during the test, depending on the test mode (Diode or MOSFET) and accordingly to incorrect temperature measurements [7]. Therefore, forward measurements of the body diode at different gate voltages (V_{GS} = 0 … -11 V) and temperatures (60 °C and 150 °C) have been carried out before the test with the Keysight B2901A SMU. These results are shown in Figure 2 for a device of test series A. The measurements allow to conclude that a gate voltage of V_{GS} = -8 V is sufficient to close the n-channel for these devices. Therefore, it is of major importance that a verification of the closed channel in the test range has been carried out, especially with the temperatures of T_{jmin} and T_{jmax}. However, the required gate voltage may differ from manufacturer to manufacturer [8] and the minimal allowed values specified in the respective data sheets should be taken into account.

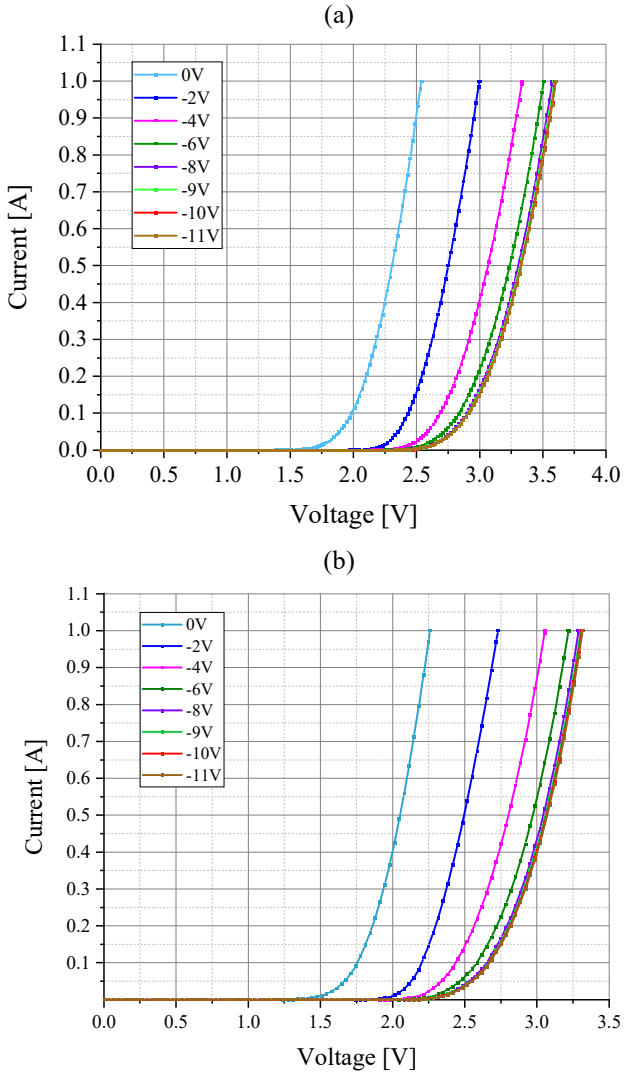

Figure 2: Forward characteristic of the body diode at different gate voltages (V_{GS} = 0 … -11 V) at a temperature of 60 °C (a) and 150 °C (b) of test series A

Before and after the power cycling test, temperature calibration curves for the adapted $V_{CE}(T)$ method have been measured in the range from about 50°C to 160°C at constant gate voltage of -8 V. An example for a device of test series A is given in Figure 3. The maximum deviation between the two curves is approx. 1.2 K, but the measurement accuracy of the thermocouple should be considered. It can be stated that there were no changes in the calibration curves and therefore, no incorrect measurements in the temperature determination.

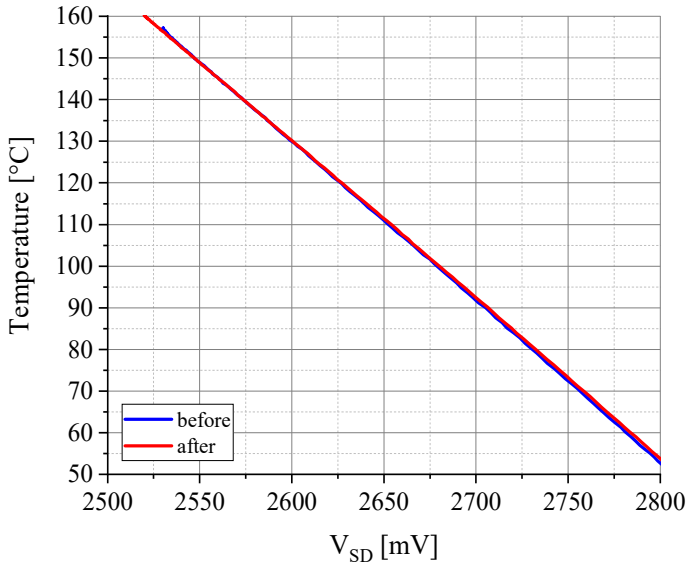

Figure 3: Temperature calibration curves before and after the power cycling test at a gate voltage of V_{GS} = - 8 V for a device from test series A with measurement current I_{mess} = 100 mA

Power cycling capability

The power cycling test was performed for the two test series with the same on-time of t_{on} = 2 s, temperature swing ΔT_j of about 90 K and a maximum junction temperature T_{jmax} of approximately 150 °C. The load current I_{Load} was 21.1 A for test series A and 23.2 A for B, respectively. The gate voltage was set in the range of 14-18 V in order to achieve similar test conditions, such as temperature swing. This means also that the power cycling tests were executed above the temperature compensation point (TCP) and there was a positive temperature coefficient of the $R_{DS(ON)}$. The maximum junction temperature T_{jmax} has been measured 160 µs after switching off the load current and this measurement delay results in an offset of T_{jmax} of approx. 7.5 K, which has been calculated with the square-root-t-method. [9, 10, 11]. The test specimens were attached to the heat sink adapter plates with standard mounting clips. An overview of the test conditions without delay time correction is given in Table 1.

Table 1: Overview of the test conditions for the two test series A and B in the power cycling test

	A	B
T_{jmax} [°C]	146-150	148-151
ΔT_j [K]	87-90	89-92
I_{load} [A]	21.1	23.2
I_{load} per bond or I_{load} per bond foot [A]	10.55	7.73
bond config.	2*375µm	3*250µm
t_{on} [s]	2	
t_{off} [s]	4	
T_{inlet} [°C]	55	
$V_{GS(on)}$ [V]	14-15	15-18
$V_{GS(off)}$ [V]	-8	

Between the two test series, a difference of 100% in power cycling capability can be observed. The development of V_{DS} and R_{thjhs} (junction to heatsink) is shown for one device of each test series in Figure 4 as example. All devices failed with an increase of V_{DS} of + 5 %. The decrease in $R_{th,jhs}$ can be attributed to the run-in behavior of the used thermal conducting foil (Kerafol 86/60), which also serves as an electrical isolation between devices and adapter plates.

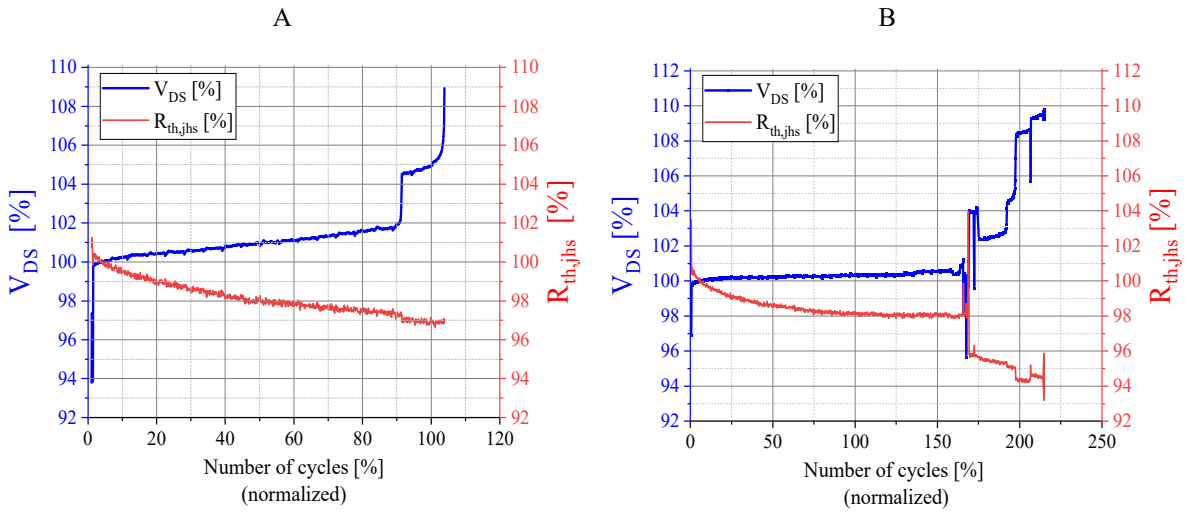

Figure 4: Power cycling test results for the test series A and B

The cycles achieved (raw data) are presented in Figure 5(a). A difference in lifetime by a factor of 1.5 to 2 between the two variants can be observed although the current density per bond of B is higher. For a clearer comparison, the test results are normalized to a temperature swing of 90 K, mean temperature of 105 °C and an application-near nominal current of 13 A according to the data sheet with a lifetime model for discrete devices [3]. This nominal current results in a current per bond or current per bond foot of 6.5 A for A and 4.33 A for B. According to this values, a normalization of the measured current per bond foot was done. The results of this normalization are shown in Figure 5(b) indicating that lifetime of the test series B is two to three times higher than that of the test series A. Furthermore, there is no difference in lifetime between DC power cycling tested SiC MOSFET devices as well as those with additional switching losses [12].

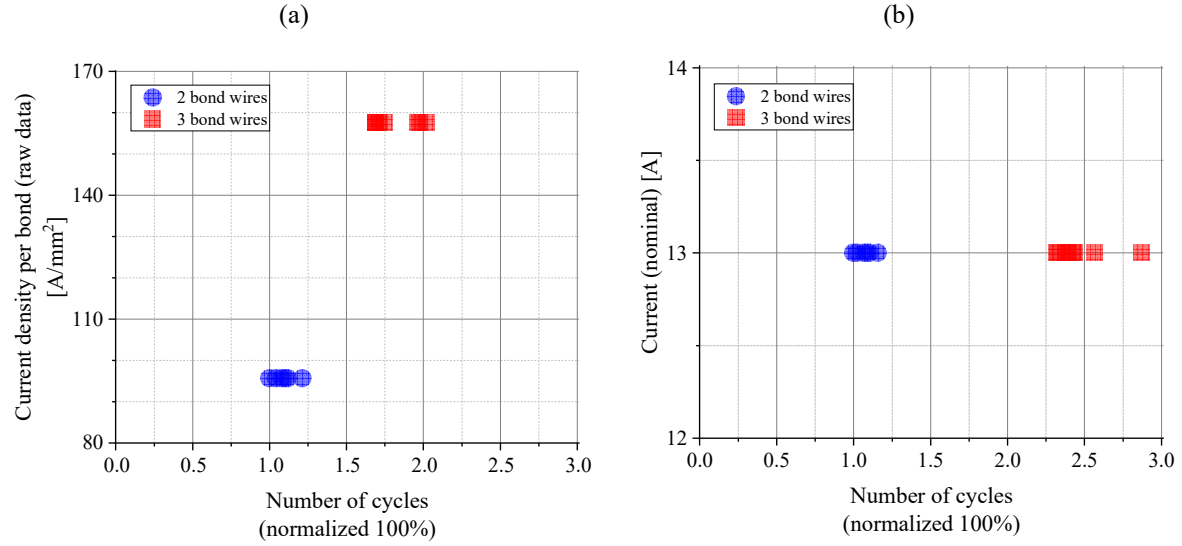

Figure 5: Cycles until EoL: (a) raw data and (b) normalized to the same temperature swing of 90 K, mean temperature of 105 °C and nominal current of 13 A

The normalization was performed according to the following equation with the specific parameters for discrete Si IGBT devices from [3]:

$$N_{\mathrm{f,\,normalized}\,(\Delta T_{\mathrm{j}},\,T_{\mathrm{jm}},I_{\mathrm{b}})} = N_{\mathrm{f,\,measured}} \cdot \frac{\Delta T_{\mathrm{j,\,desired}}^{\alpha}}{\Delta T_{\mathrm{j,\,measured}}^{\alpha}} \cdot \frac{e^{\frac{E_{\mathrm{A}}}{k \cdot T_{\mathrm{jm,\,desired}}}}}{e^{\frac{E_{\mathrm{A}}}{k \cdot T_{\mathrm{jm,\,measured}}}}} \cdot \frac{I_{\mathrm{b,\,desired}}^{\gamma}}{I_{\mathrm{b,\,measured}}^{\gamma}} \qquad (1)$$

Failure analysis

After the power cycling test, a failure analysis has been performed to determine the cause of failure. In the first step, Scanning Acoustic Microscopy (SAM) images with focus on the bonding wires and the solder layer, respectively, were generated for both test series (see Figure 6). No solder deterioration is observed, but both test series show bond feet degradation.

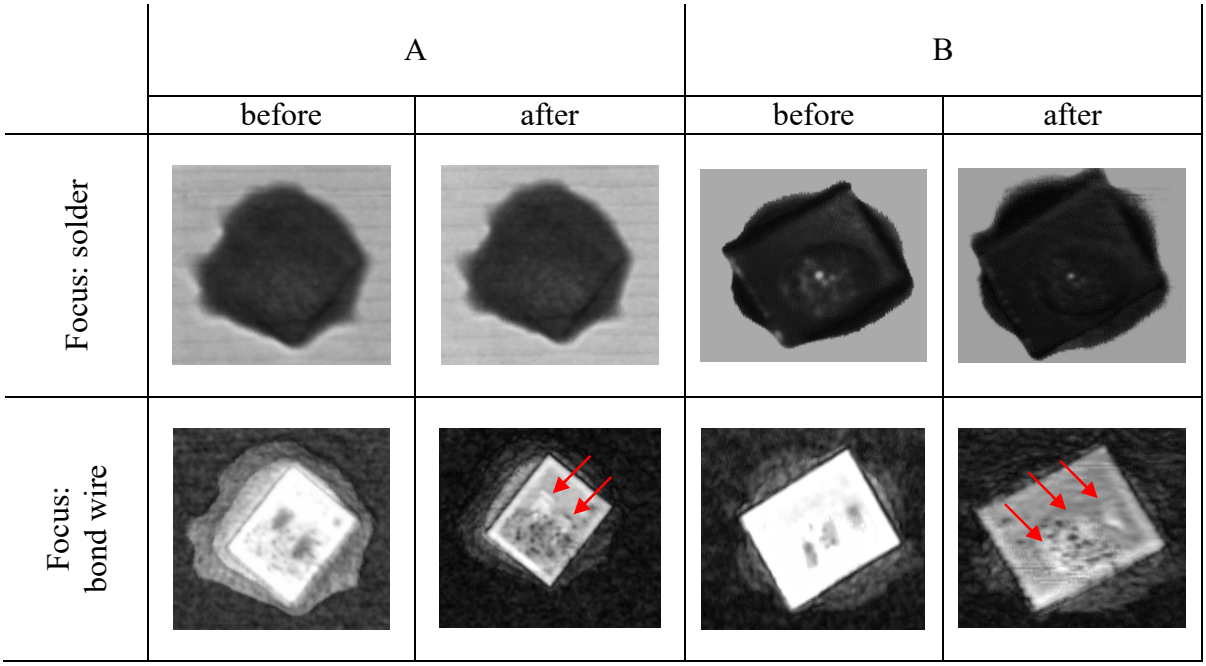

Figure 6: SAM images of both test series with focus on the bond wires and the solder layer

To be able to determine whether the specimen was affected by a bond wire lift off or a heel crack, the failed parts were opened. In test series A, only bond wire lift offs occurred, whereas in test series B both, bond wire lift offs and heel cracks were detected. Such failure modes are also observed with Si IGBTs or diodes in discrete packages [3, 13, 14].

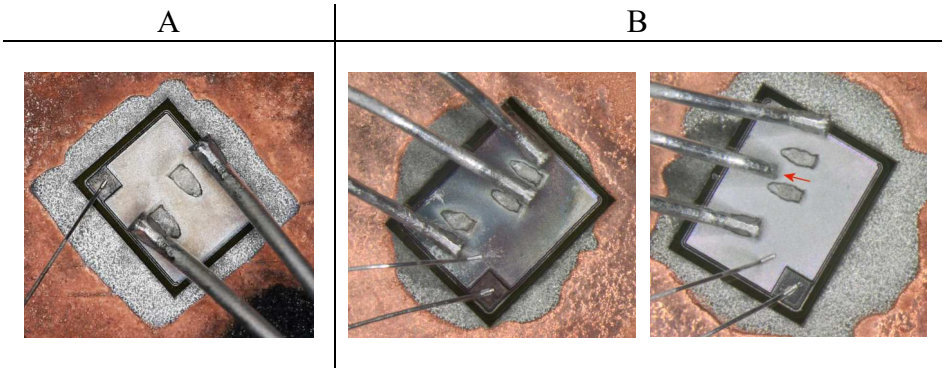

Figure 7: Bond wire lift off and heel crack (red arrow)

Simulation results

In order to gain further insight into the behavior of the test specimens, simulation models were created in ANSYS for both configurations (see Figure 8). The material properties of the individual layers are identical for both models. Only the position of the chip and the bond wire setup have been adapted to the test specimens. 10 cycles were simulated until the system reached a steady state.

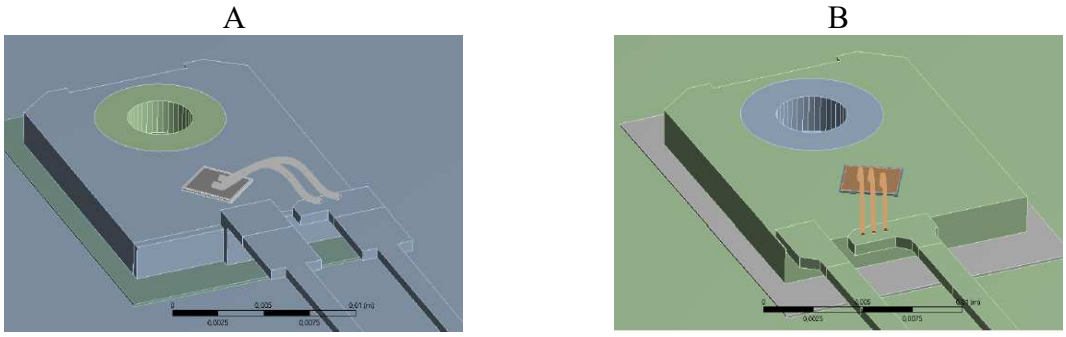

Figure 8. Simulation model for both bond wire configurations (A and B)

The cross-sections along one bond wire are shown in Figure 9. A more homogeneous temperature distribution for the configuration with three bond wires can be observed. The two bond wire configuration results in a more concentrated heat transfer and consequently in a heavily inhomogenious temperature distribution. Therefore, the lower thermal stress due to the temperature distribution of the configuration B correlates with the higher lifetime found in the experiments.

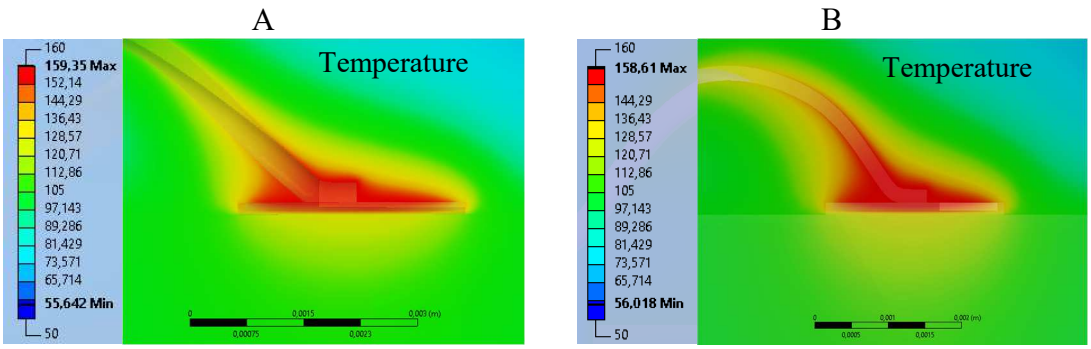

Figure 9: Cross section after the tenth heating cycle (56 s) reaching a steady state along the bond wire for both bond wire configurations (A and B)

The temperature distribution with focus on the chip surface and bond feet for both configurations is presented in Figure 10. At a similar maximum junction temperature of 150 °C, the maximum and minimum temperatures on the chip surface are almost identical for both configurations. The temperature gradient along the corresponding bond feet at A is larger than at B. In addition, the temperature gradient over the bond foot at B is more depending on the position on the chip.

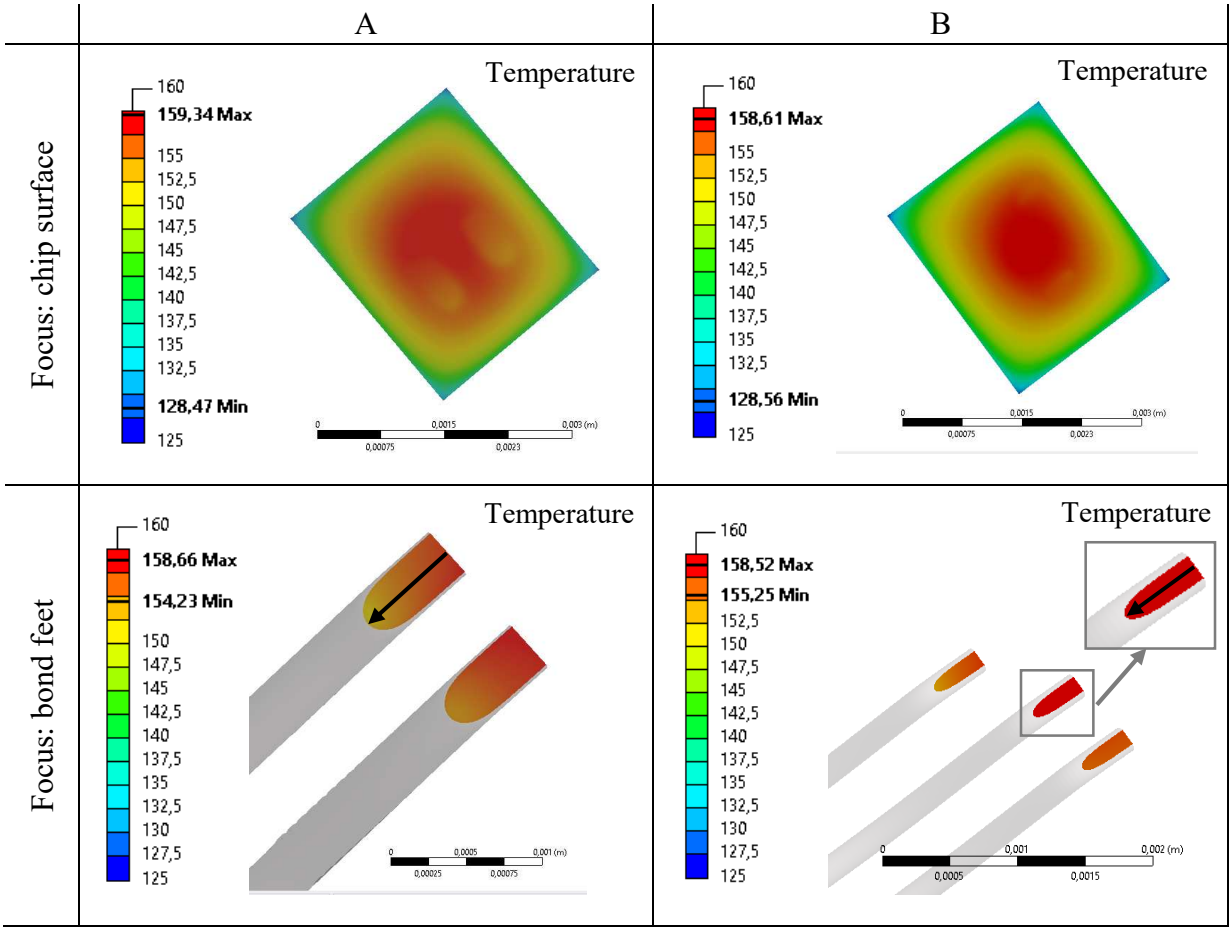

Figure 10: Temperature distribution with focus on the chip surface and bond feet for both bond wire configurations (A and B) after the tenth heating cycle (56 s) reaching steady state

Figure 11 provides a more detailed analysis of the temperature gradient across a selected bond foot for both bond wire configurations. The temperature is plotted along a path according to the black arrows in Figure 10. It is found that the temperature difference for A is approx. 3 K and for B approx. 0.5 K.

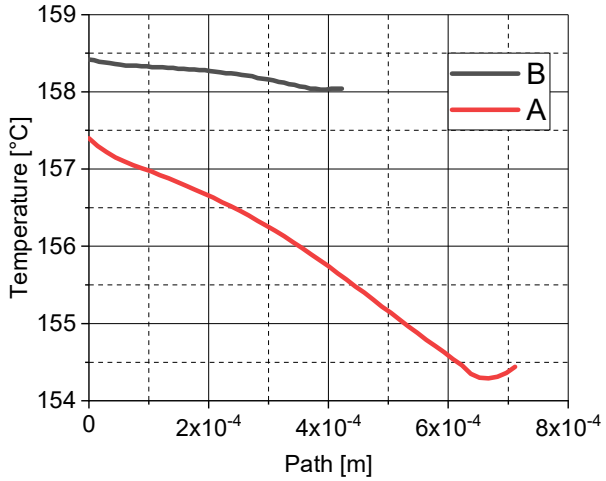

Figure 11: Temperature along the path (according to the black arrows in Figure 10) for both bond wire configurations (A and B) after the tenth heating cycle (56 s) reaching steady state

The total strain per cycle with focus on the metallization is presented in Figure 12 for both configurations (A and B) from the results of [12]. An important factor in these static structural (mechanical) simulation is that the Anand model was used for the solder layer [15] and a model with nonlinear stress-strain-temperature behavior for the metallization and bond wires [16]. Configuration A results in a maximum total strain per power cycling swing of ε = 3,88 m/mm and B of ε = 1,96 mm/m [12]. This means that the maximum strain at B is about two times lower than at A [12]. Therefore, these mechanical simulation findings are being added on top of the more homogenous temperature gradient in the thinner bond wire and confirm the experimental measurement results. Consequently, it follows that three bond wires with a smaller diameter have a higher power cycling capability than two bond wires with a larger diameter.

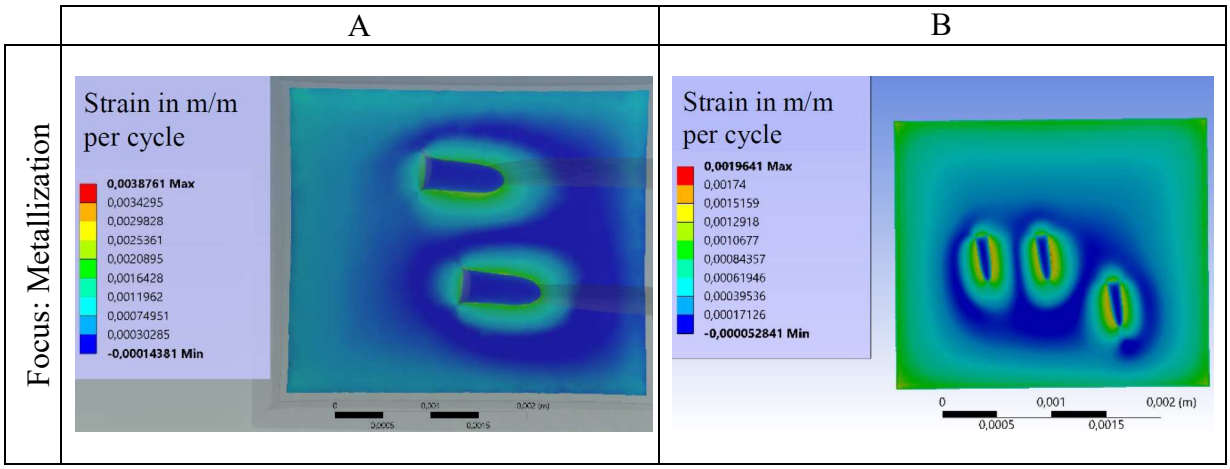

Figure 12: Total strain analysis per power cycling swing for A and B with focus on the metallization. Figures from [12]. Note: The scale is not equal

Conclusion

An influence of the bond wire configuration on the power cycling capability of SiC MOSFETs in TO-247 was found. The lifetime of the test series B with three thinner bond wires is two to three times higher than that of the test series A with two thicker bond wires although the current density per bond of A is smaller after the normalization. This corresponds to the findings for MOSFETs in modules [17]. As cause of failure, an increase of V_{DS} + 5 % has occurred for all test specimens and bond wire fatigue has been verified as the dominant mechanism by failure analysis. The ANSYS simulation shows a more homogeneous temperature distribution for the three bond wire configuration than for the two bond wire configuration. Also the mechanical simulation shows a higher total strain per power cycling swing for the 2 bond wire configuration. Therefore, the number and the associated different diameter of the bond wires have a significant influence on the power cycling capability and should be considered during the chip and package design.

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