Unsymmetrical fault behavior of PLL based grid-connected converters

Philipp Hackl, Ziqian Zhang, Robert Schuerhuber
Institute of Electrical Power Systems, TU Graz, Austria
Tel.: +43 (0) 316 873 - 7567
E-Mail: philipp.hackl@tugraz.at
URL: https://www.tugraz.at/institute/iean

Keywords

«Grid-connected converter», «Stability analysis», «Transient analysis», «PLL», «Fault ride-through»

Abstract

The fault behavior of converters is essential for stable operation of converter-driven power grids. This paper introduces a stability criterion of unsymmetrical faults for phase-locked loop (PLL) based grid-connected converters. The focus lies on the stability of the PLL considering the grid conditions and the converter feed-in power during the fault. For this purpose, the approach is based on the phase portrait method where several situations are examined in theory. Finally, the stability criterion is validated with real-time system experiments.

Introduction

Due to the expansion of renewable energy sources, more and more converter-based systems are connected to the grid. This tends to reduce the short-circuit power of the grid and thus the stability of the converter is significantly affected negatively. A particularly critical case is the operation ride-through a short-circuit fault. In this case, the grid codes require the injection of reactive current into the grid to support the grid voltage and also for supplying sufficient current for protection relaying.

The converter control algorithm and the corresponding parameters dominate the stability of the converter-based generation. Thereby, a successful synchronization to the grid is achieved by different methods, which are reviewed in [1] without an analysis in the fault case. In most converters, a phase-locked loop (PLL) unit is used, which serves as base for the control algorithm and must remain stable during and after the fault to successfully ride-through a fault. In the literature numerous studies of PLL stability investigations concerning symmetrical faults exist, which are generally regarded as the most severe faults with the highest short-circuit current. In [2] a detailed design-oriented investigation of different PLL parameters with validations in experiments are examined, but only the transient stability of converters with equilibrium points are considered. Whereby [3] introduces a steady-state and transient stability criterion depending on the grid topology, grid voltage and injected converter current.

However, unsymmetrical faults occur far more frequently in power systems. In this case, a standard approach is to transform the investigated grid topology into an equivalent circuit in symmetrical component representation. This enables converters to fulfill the requirement of most grid codes e.g. [4] that require not only injection of positive sequence reactive power into the grid, but also negative sequence reactive power. In [5] the authors describe the coupling of the sequences in different grid faults and examine positive and negative sequence dominated instabilities. Although a steady-state stability criterion is defined, the theoretical approach investigating the transient stability is not specified in detail.

This paper introduces a steady-state and transient stability criterion of PLL based grid-connected converters under unsymmetrical faults. Thereby, it considers positive and negative sequence coupling with different current injection strategies. For this purpose, the synchronization method of the converter is explained, followed by a description of the influence of the grid topology. Subsequently, the relation of the power grid with the converter is introduced and the stability criterion is examined.

Finally, the stability criterion is validated with experiments using a real-time-system as described in [6]. Therefore, a typical single overhead line grid model with a converter and a Dy transformer, shown in Fig. 1, is used.

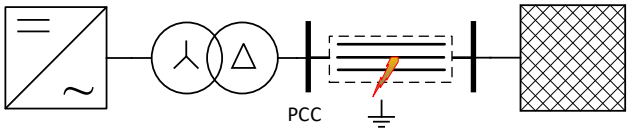

Fig. 1: Overview of investigated grid topology

In this paper the following conventions for notations are used.

X^+	positive sequence variable	ϑ_{index}	phase angle of complex variable
X^-	negative sequence variable	X_{index}	amplitude of complex variable
X^0	zero sequence variable	x_{d}	direct component of a variable
$\underline{X}_{\text{index}}$	complex variable	x_{q}	quadrature component of a variable

Modelling of converter control in relation to grid topology

The control strategies of most currently used converters require the terminal voltage as control quantity to feed-in the desired power. A phase-locked loop (PLL) is used for this purpose, whereby its stability is essential for the entire control algorithm. The importance of this reference phase angle of the PLL for the stability in symmetrical faults has already been discussed in detail in [3]. However, in the case of unsymmetrical faults, grid codes also require the injection of negative sequence reactive current into the grid voltage. Therefore, the negative sequence`s phase angle of the terminal voltage is also necessary for a successful fault-ride-through (FRT) control.

In order to enable the converter to operate stable in an unsymmetrical grid, there are various PLL strategies available [1]. A common used strategy is to control the positive and negative sequence current separately, which is shown in Fig. 2 for a single line-to-earth fault (red) and a line-to-line fault (green). Here it can be seen how the reference phase angles are obtained from the converter terminal voltage $\underline{U}$ through two separate PLLs. Each PLL controls the q-axis component of the voltages in a closed loop to get the reference phase angles.

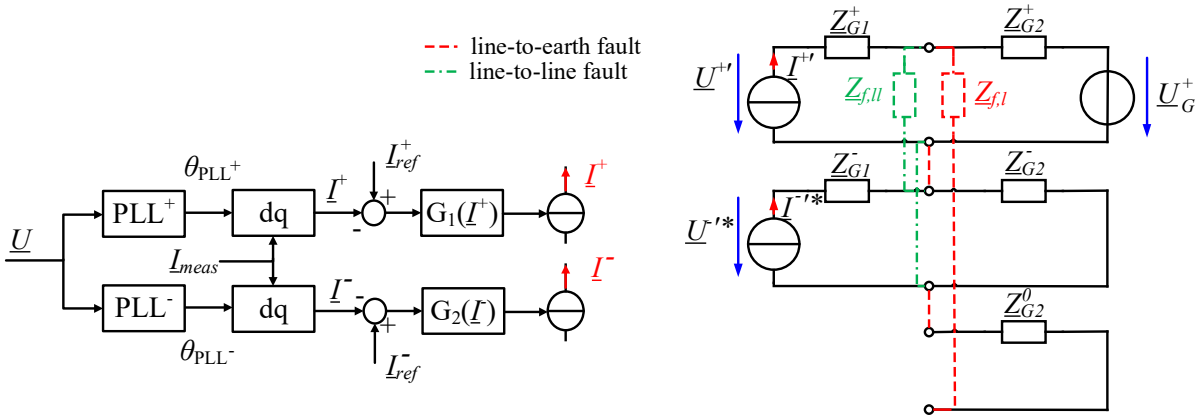

Fig. 2: (left) Block diagram of converter controller in positive and negative sequence (right) Grid topology using symmetrical components

With these phase angles it is possible to decouple the converter current in a positive and negative sequence control algorithm. These currents can then be controlled through decoupled current controllers to the given reference currents. In this paper the research on the PLLs stability is mainly of interest, therefore the current control loops, G_1 and G_2 in Fig. 2, are assumed to be ideal. The converter is simplified as two controlled current sources, $\underline{I}^+, \underline{I}^-$, with reference currents $\underline{I}^+_{ref}, \underline{I}^-_{ref}$.

The following three factors mainly influence the voltage at the converter terminals: grid topology, fault type and fault location. Therefore, the grid topology from Fig. 1 is transformed into symmetrical components, shown in Fig. 2, to evaluate the resulting voltage during unsymmetrical faults at the converter terminals. These are connected in different configurations depending on the assumed unsymmetrical fault condition. The zero-sequence system of the converter voltage is decoupled via the delta-wye transformer.

In Fig. 2, the grid is represented by a Thevenin equivalent circuit, where Z_{G2} summarize the grid impedance and the impedance of the transmission line from the grid to the fault location. The converter is represented by an ideal current source with a series impedance Z_{G1} which include the impedances of the transformer and the transmission line from the converter to the fault location.

To calculate the converter terminal voltages, the grid voltage, grid impedance and also the converter output current must be considered. The positive and negative sequence is considered by the superposition principle. This results in the set of equations (1) on the high-voltage side, which are valid for all kinds of grid faults and topologies.

$$\underline{U}^{+'} = \underline{K}_1 \cdot \underline{U}_G^{+} + \underline{Z}_{11} \cdot \underline{I}^{+'} + \underline{Z}_{12} \cdot \underline{I}^{-'*} \qquad (1a)$$

$$\underline{U}^{-'*} = \underline{K}_2 \cdot \underline{U}_G^{+} + \underline{Z}_{21} \cdot \underline{I}^{+'} + \underline{Z}_{22} \cdot \underline{I}^{-'*} \qquad (1b)$$

The factors depend on the grid topology and the actual fault, whereby $\underline{K}_1, \underline{K}_2$ indicate the influence of the grid voltage on the positive/negative sequence voltage. $\underline{Z}_{11}, \underline{Z}_{22}$ define the impact of the positive/negative sequence current on the voltage of the same sequence, whereby $\underline{Z}_{12}, \underline{Z}_{21}$ are transfer impedance, coupling the positive and negative sequence systems. The variables $\underline{I}^{-'*}, \underline{U}^{-'*}$ are the conjugate complex values as explained in [7] [8].

To ensure proper operation of the converter, the measured converter terminal voltage must be converted to the dq reference frame. For this purpose, the determined phase angles of the PLLs are used.

$$u_d^{+} + \mathrm{j} \cdot u_q^{+} = \underline{U}^{+} \cdot \mathrm{e}^{\mathrm{j} \cdot \theta_{PLL^+}} \qquad (2a)$$

$$u_d^{-} + \mathrm{j} \cdot u_q^{-} = \underline{U}^{-^*} \cdot \mathrm{e}^{-\mathrm{j} \cdot \theta_{PLL^-}} \qquad (2b)$$

These expressions combined with (1) leads to the relation of the grid topology including the PLL, in (3). $\theta_{K_1}, \theta_{K_2}, \theta_{Z_{11}}, \theta_{Z_{22}}, \theta_{Z_{12}}, \theta_{Z_{21}}$ indicate the phase angle of the complex factors from (1), $\theta_{PLL^+}, \theta_{PLL^-}$ are the phase angles of the PLLs and $\theta_{I^+}, \theta_{I^-}$ are the phase angles of the positive and negative sequence converter currents.

$$u_d^{+} + \mathrm{j} \cdot u_q^{+} = K_1 \cdot U_G^{+} \cdot \mathrm{e}^{\mathrm{j}(\theta_{K_1} - \theta_{PLL^+})} + Z_{11} \cdot I^{+} \cdot \mathrm{e}^{\mathrm{j}(\theta_{Z_{11}} + \theta_{I^+})} + Z_{12} \cdot I^{-} \cdot \mathrm{e}^{\mathrm{j}(\theta_{Z_{12}} - \theta_{1PLL} + \theta_{PLL^-} + \theta_{I^-})} \qquad (3a)$$

$$u_d^{-} + \mathrm{j} \cdot u_q^{-} = K_2 \cdot U_G^{+} \cdot \mathrm{e}^{\mathrm{j}(\theta_{K_2} - \theta_{PLL^-})} + Z_{22} \cdot I^{-} \cdot \mathrm{e}^{\mathrm{j}(\theta_{Z_{22}} + \theta_{I^-})} + Z_{21} \cdot I^{+} \cdot \mathrm{e}^{\mathrm{j}(\theta_{Z_{21}} + \theta_{PLL^+} - \theta_{PLL^-} + \theta_{I^+})} \qquad (3b)$$

If the imaginary part of the voltage is shown separately and the time dependence of the PLLs are marked explicitly, the following expressions (4) are derived.

$$u_q^{+}\left(\theta_{PLL^+}(t)\right) = K_1 \cdot U_G^{+} \cdot \sin\left(\theta_{K_1} - \theta_{PLL^+}(t)\right) + Z_{11} \cdot I^{+} \cdot \sin\left(\theta_{Z_{11}} + \theta_{I^+}\right) + Z_{12} \cdot I^{-} \cdot \sin\left(\theta_{Z_{12}} - \theta_{PLL^+} + \theta_{PLL^-} + \theta_{I^-}\right) \qquad (4a)$$

$$u_q^{-}\left(\theta_{PLL^-}(t)\right) = K_2 \cdot U_G^{+} \cdot \sin\left(\theta_{K_2} - \theta_{PLL^-}(t)\right) + Z_{22} \cdot I^{-} \cdot \sin\left(\theta_{Z_{22}} + \theta_{I^-}\right) + Z_{21} \cdot I^{+} \cdot \sin\left(\theta_{Z_{21}} + \theta_{PLL^+} - \theta_{PLL^-} + \theta_{I^+}\right) \qquad (4b)$$

If the coupling between positive and negative sequence PLLs is neglected, which can be argued in grid conditions where $\underline{Z}_{12} \ll \underline{Z}_{11}$ and $\underline{Z}_{21} \ll \underline{Z}_{22}$ this results in (5).

$$u_q^+\left(\theta_{PLL^+}(t)\right) = K_1 \cdot U_G^+ \cdot \sin\left(\theta_{K_1} - \theta_{PLL^+}(t)\right) + Z_{11} \cdot I^+ \cdot \sin\left(\theta_{Z_{11}} + \theta_{I^+}\right) \quad (5a)$$

$$u_q^-\left(\theta_{PLL^-}(t)\right) = K_2 \cdot U_G^+ \cdot \sin\left(\theta_{K_2} - \theta_{PLL^-}(t)\right) + Z_{22} \cdot I^- \cdot \sin\left(\theta_{Z_{22}} + \theta_{I^-}\right) \quad (5b)$$

For a successful synchronization of the PLLs to the grid, the PLLs control the imaginary part of the terminal voltages to zero, explained in [3]. Therefore, a stable equilibrium point (SEP) of the PLLs can only be achieved, if the equation's (5) output is zero. This results to the analytical solution (6), if it is solved for the phase angles of the PLLs ($\theta_{PLL^+,sep}$, $\theta_{PLL^-,sep}$). Whereby the factor n (0, 1, 2, 3, …) indicates that there exist periodically solutions.

$$\theta_{PLL^+,sep} = \theta_{K_1} + \arcsin\left(\frac{Z_{11} \cdot I^+ \cdot \sin\left(\theta_{Z_{11}} + \theta_{I^+}\right)}{K_1 \cdot U_G^+}\right) \pm n \cdot 2\pi \quad (6a)$$

$$\theta_{PLL^-,sep} = \theta_{K_2} + \arcsin\left(\frac{Z_{22} \cdot I^- \cdot \sin\left(\theta_{Z_{22}} + \theta_{I^-}\right)}{K_2 \cdot U_G^+}\right) \pm n \cdot 2\pi \quad (6b)$$

To obtain a real number as phase angle the argument of the arcsin must be between -1 to 1. An equilibrium point can thus only be defined by the following conditions (7).

$$K_1 \cdot U_G^+ \geq Z_{11} \cdot I^+ \cdot \sin(\theta_{Z_{11}} + \theta_{I^+}) \quad (7a)$$

$$K_2 \cdot U_G^+ \geq Z_{22} \cdot I^- \cdot \sin(\theta_{Z_{22}} + \theta_{I^-}) \quad (7b)$$

In (3) and (4) it can be seen that the q-axes of the converter terminal voltages u_q are in a sinusoidal relation to the reference phase angles from the PLLs. For closer investigation (3) can be divided into three parts. The first parts, e.g. $K_1 \cdot U_G^+ \cdot \sin\left(\theta_{K_1} - \theta_{PLL^+}(t)\right)$, depend on the phase angle of the PLL and define the amplitudes regarding the grid voltage factors and the grid voltage itself. The second parts, e.g. $Z_{11} \cdot I^+ \cdot \sin\left(\theta_{Z_{22}} + \theta_{I^+}\right)$, are independent of the PLLs output. This leads to an offset of the function, which depends on the grid parameters and the injected currents of the converter. Finally, the third parts, e.g. $Z_{12} \cdot I^- \cdot \sin\left(\theta_{Z_{12}} - \theta_{PLL^+} + \theta_{PLL^-} + \theta_{I^-}\right)$, show the coupling of the positive and negative sequence grid factors, converter currents and PLL phase angles. This influences the phase shifts and also the amplitudes of the quadrature parts of the voltage u_q.

Fig. 3 shows the relation of the converter terminal voltage and phase angle of the positive sequence PLL for different grid conditions, depending on the aforementioned grid factors in (1). The phase angle of the PLL can only be stable at intersection points with the abscissa. These results for different grid conditions in either two equilibrium points (EP), one EP or no EP. If there are two EPs, a distinction must be made between stable equilibrium points (SEP) and unstable equilibrium points (USEP), as in [3].

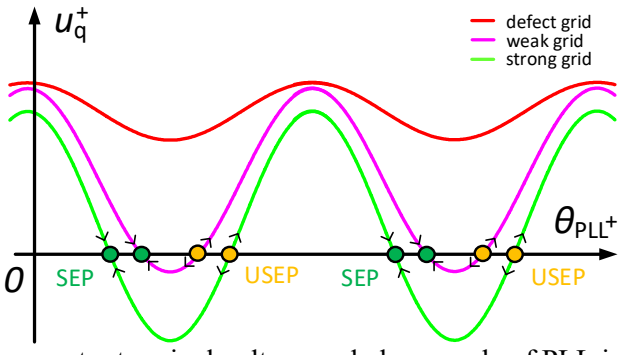

Fig. 3: Relation of converter terminal voltage and phase angle of PLL in positive sequence

Furthermore, Fig. 3 shows that a stronger grid (green curve) results in a small offset leading to a large negative u_q zone. On the other hand, a weak grid (purple curve) has a larger offset which leads to a smaller negative u_q zone. At certain grid conditions (red curve) it may happen that there is no intersection with the abscissa, whereby no SEP for the PLL exists. This leads to a criterion to determine if there is a SEP that can be reached by the PLL control. For example, the offset implies that the PLL control in a stronger grid has more chance to stabilize at the nearest SEP than for weaker grids. Due to the varying control structures and parameters of PLLs this leads to different dynamic behaviors even at same grid conditions. This can cause converter fail to operate, while others are able to withstand the same disturbance without any issues.

Steady-state and transient stability criterion during fault

This stability criterion shows under which conditions a PLL based converter can reach a stable equilibrium point (SEP) during an unsymmetrical fault. The applications are based on the values of table I with the topology shown in Fig. 1 during a line-to-line short circuit. The quadrature components of the terminal voltage in positive (left) and negative (right) sequence are shown in following figures (blue curves) according the equation (5). The figures also show the considering of the coupling of the PLLs (red curves) as mentioned in (4). The intersections of the curves with the abscissa are the possible equilibrium points, whereby the analytical solutions for the SEP by means of (6) are marked with a circle.

On the left side of Fig. 4, the sinusoidal relation of u_q^+ to the phase angle of the positive sequence PLL with an active power feed-in of 1 p.u. is shown. It can be seen, that during the fault because of the high active current injection and the weak grid there is a big offset. This reduces the negative u_q zone of the PLL and it is possible that PLLs with a high cut-off frequency can get unstable already. Because of the low current injection in the negative sequence, the coupling of the PLLs for u_q^+ is neglectable. For u_q^- there are safely reachable SEPs with and without the coupling of θ_{PLL^+}. Under these conditions it can be assumed that general well-tuned PLLs remain stable during the fault.

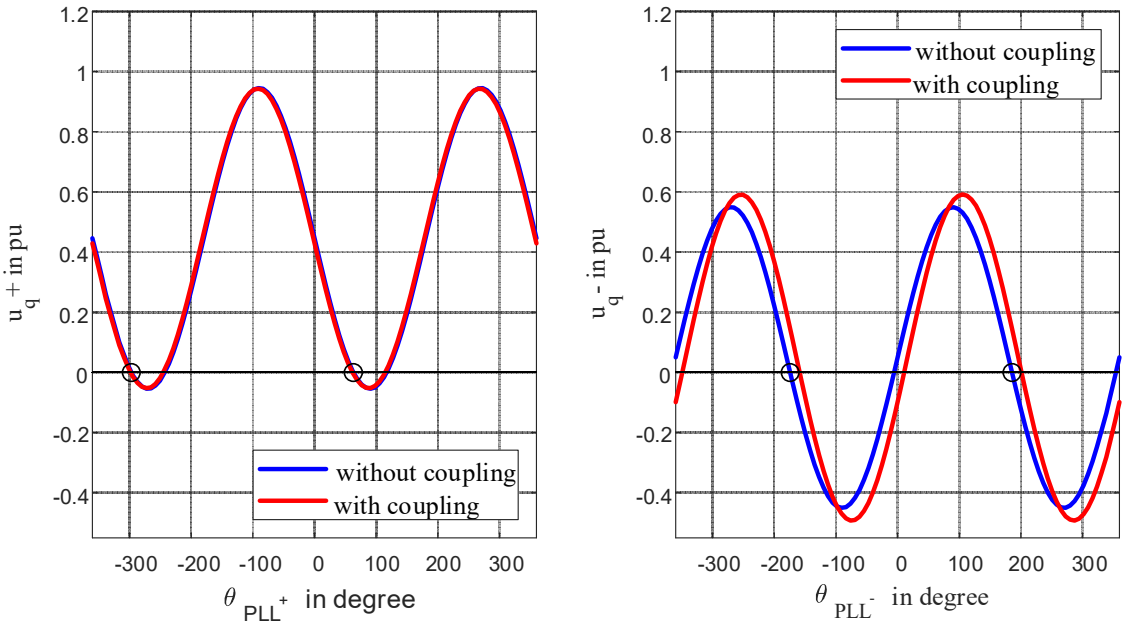

Fig. 4: Terminal voltage in relation to phase angle of PLLs with $I_d^+ = 1$ p.u. injection

With an injection of 1.2 p.u. as active power in the positive sequence, there is no longer an intersection of u_q^+ with the abscissa resulting in no SEP during the fault situation, seen in Fig. 5. The converter becomes unstable even if the negative sequence could reach a SEP.

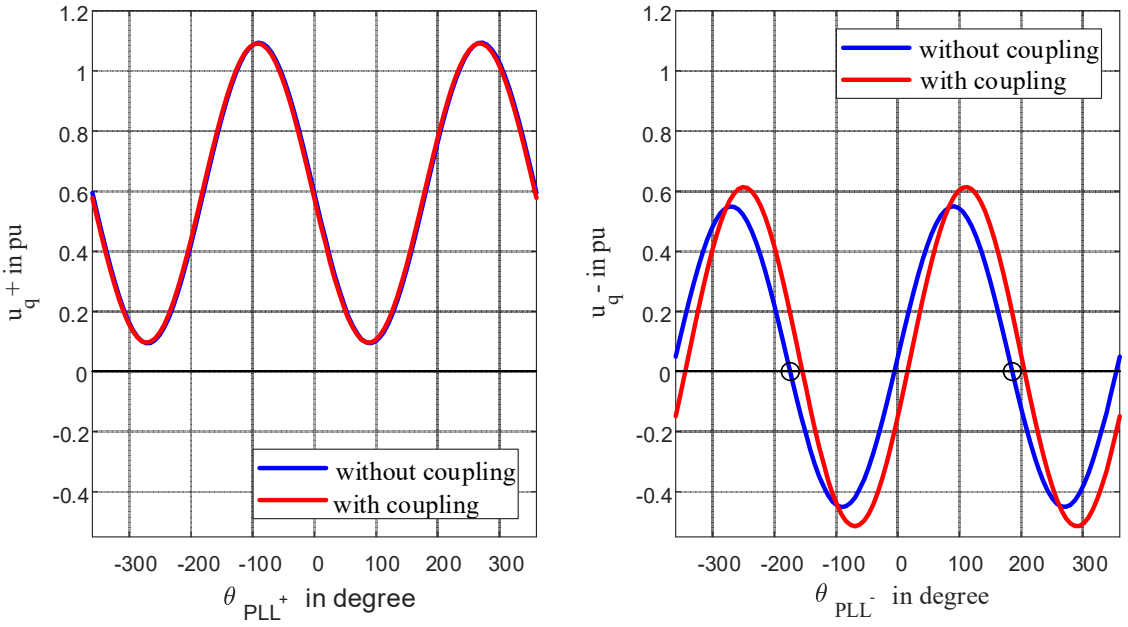

Fig. 5: Terminal voltage in relation to phase angle of PLLs with $I_d^+ = 1.2$ p.u. injection

Assuming the same active power feed-in of 1.2 p.u. in the positive sequence and an additional reactive power injection in the negative sequence, the coupling of the systems results in a SEP in the positive sequence, seen in Fig. 6. In case of a well-tuned PLL, the converter can continue to operate stable under this fault conditions. With less accurate PLLs, the positive sequence phase angle moves along this red line.

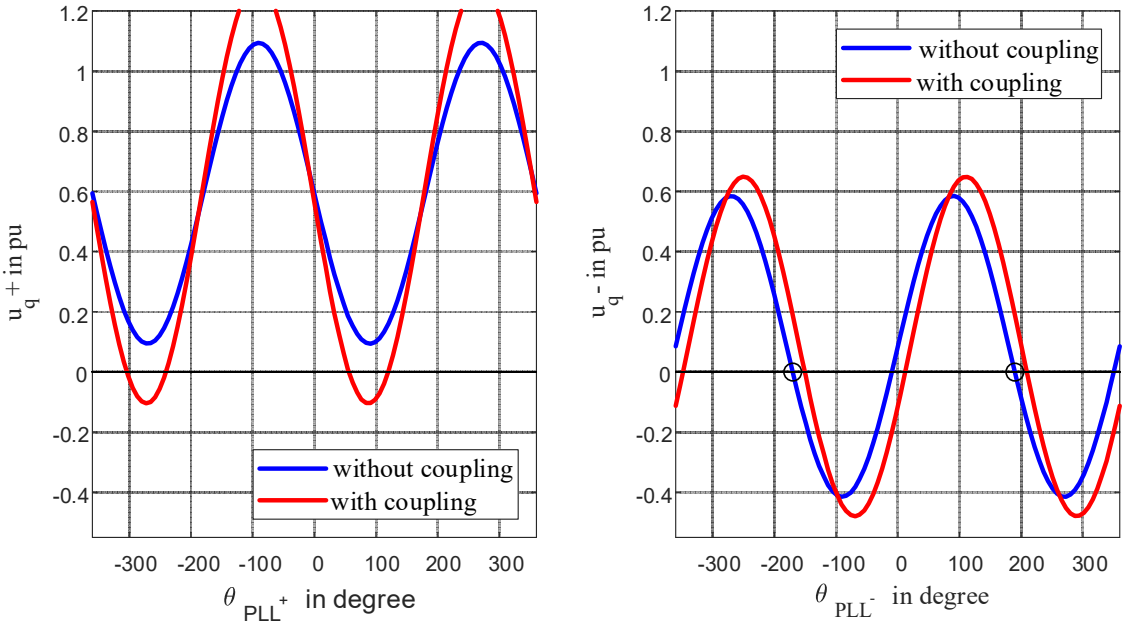

Fig. 6: Terminal voltage in relation to phase angle of PLLs with $I_d^+ = 1.2$ p.u. and $I_q^- = 1.2$ p.u. injection

The phase portrait method is an approach where the angular velocity (derivative of the phase angle over time) is plotted on the y-axis and the phase angle is plotted on the x-axis [9] [10], e.g. seen in Fig. 7. The black upper and lower curves limit the domain of attraction (DOA) in which any point, defined uniquely by its phase angle and angular velocity, moves towards a stable equilibrium point (SEP) in a reasonable time. Different DOAs are marked in different colors, each with a SEP inside.

If there is no intersection of u_q with the abscissa during the fault (no EP), then the phase angle of the PLL accelerates away from the pre-fault SEP along the red curve in Fig. 7. If the fault is cleared soon enough (e.g. 1), the SEP before the fault state can be reached quickly. If the fault is cleared later (e.g. 2), the next SEP is obtained, which takes longer. If the fault is cleared too late (in blue area, e.g. 3), no SEP can be reached and the converter becomes unstable. If there is a SEP during the fault, but it cannot be reached by the control the PLL accelerates and decelerates and circles around this SEP, as shown by the blue curve in Fig. 7. After the fault, the PLL converge very quickly to this SEP (e.g. 4 in Fig. 7) and the system remains stable.

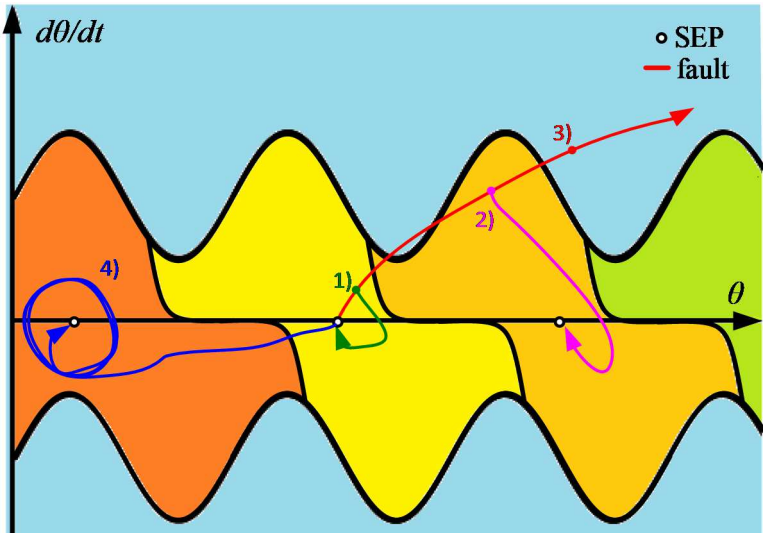

Fig. 7: Phase portrait method with stable regions (DOAs in different colors) and unstable region during fault and after fault clearing

Validation in Real-Time-System Experiments

To validate the stability criterion mentioned above, experiments are carried out. The grid topology (seen in Fig. 1) is emulated in a real-time simulation and the converter is based on the grid following control concept. Thereby a dual second order generalized integrator phase-locked loop (DSOGI-PLL) [11] is used to obtain the positive and negative sequence reference phase angles as base for the controlled current sources. The results show the line-to-line short-circuit between phase 2 and 3 with a fault duration of 0.4 s occurring at 0.2 s in the middle of the line. The transformer has a Dyg5 vector group and is assumed to be ideal. The low voltage side is solidly grounded and the high voltage side is operated slightly unbalanced (U_{L3} = 1.02 p.u.). The table I summarizes the most important parameters.

Table I: Parameters of real-time-system experiments

U_{HV} = 14 kV	U_{LV} = 690 V	$PLL^{+}_{cut\_off}$ = 20 Hz	fault time = 0.4 s
SCR = 1.5	P_{rated} = 10 MW	$PLL^{-}_{cut\_off}$ = 20 Hz	Z_{fault} = 0 Ω
XR_{ratio} = 7	f = 50 Hz	f_{RTS} = 10 kHz	Fault position = 50 %

For the first application, the PLL based converter continues to inject the nominal active power from the pre-fault state during the fault condition (seen in Fig. 8). In this case, the plot in the bottom left corner shows the transient response of the voltages u_q^+ and u_q^- in the fault case, although the PLL converges to a SEP. This corresponds to the steady-state results in Fig. 4. The phase portrait plot (right) shows how the trajectory from the pre-fault state travels towards a new SEP during the fault (red) and returns to the original SEP after the fault has been cleared. The negative sequence θ_{PLL^-} moves towards a new SEP during the fault and stays close at a new SEP after fault clearing.

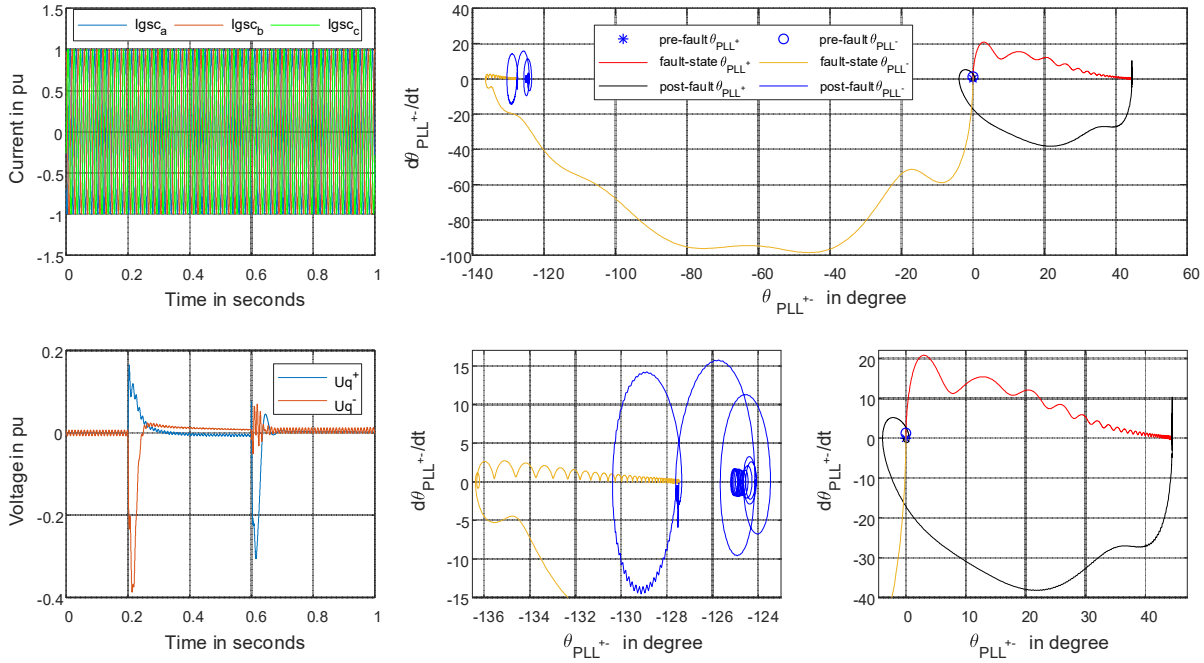

Fig. 8: Experimental validation of stability criterion with nominal active power injection during fault ($I_d^+ = 1$ p.u.)

Fig. 9 shows the current injection of 1 p.u. in pre- and post-fault state while during the fault the current feed-in is 1.2 p.u. as positive sequence active power. In this case, the increase in current can be seen in the upper left corner. Furthermore, in the fault case the voltage u_q^+ no longer intersects with the abscissa, whereby it is not possible to lead to a SEP under these conditions. This results to an acceleration of θ_{PLL^+} during the fault and consequently no SEP is reached after the fault clearing, in which case a SEP would be present again, which leads θ_{PLL^+} to become unstable. Due to the coupling of the PLLs, θ_{PLL^-} cannot reach its SEP during and after the fault, so it circles around a SEP.

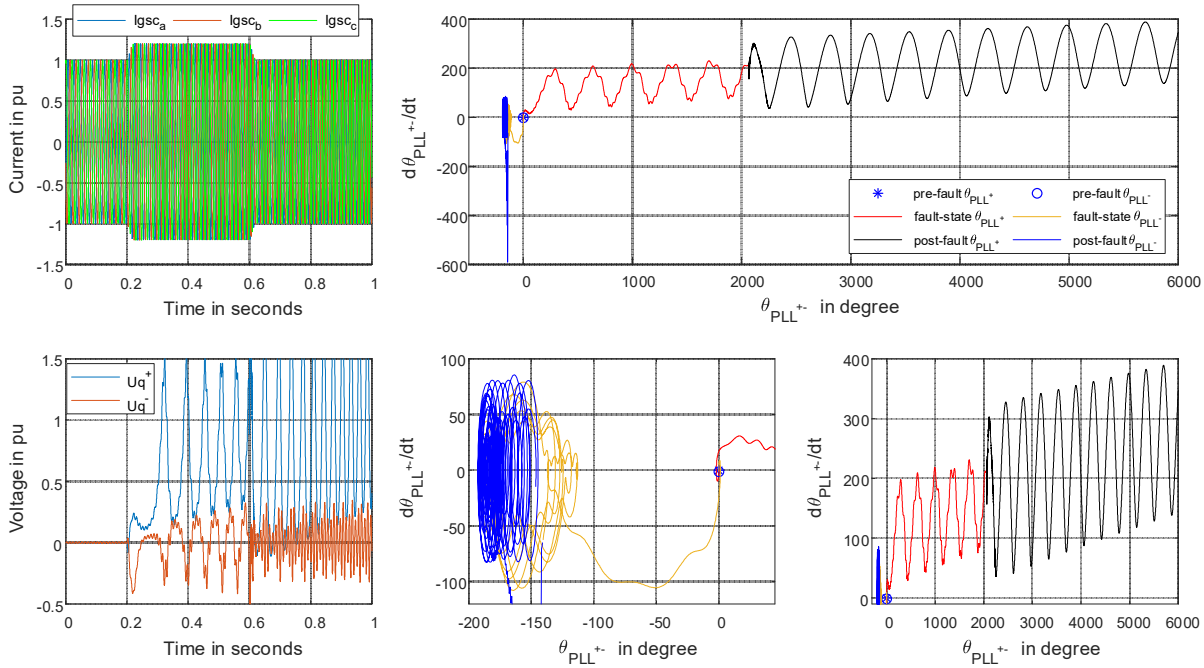

Fig. 9: Experimental validation of stability criterion with high active power injection during fault (I_d^+ = 1.2 p.u.)

The final application is that during the fault state, again as before, an increased positive sequence active power current, but also reactive power in the negative sequence is injected, seen in Fig. 10. This leads to the fact that, according to Fig. 6, the coupling of the PLLs results in a SEP through the reactive power injection. An optimal tuned PLL could thus also reach the SEP in the fault state. Unfortunately, the negative u_q zone for the selected parameters of the PLLs are to small to reach a SEP. However, the reactive power ensures that $\theta_{PLL}+$ does not accelerate excessively and consequently circles around a SEP in positive and negative sequence. After the fault clearing, a SEP can thus be reached very quickly in both instances, whereby the $\theta_{PLL}+$ also returns to the pre-fault state.

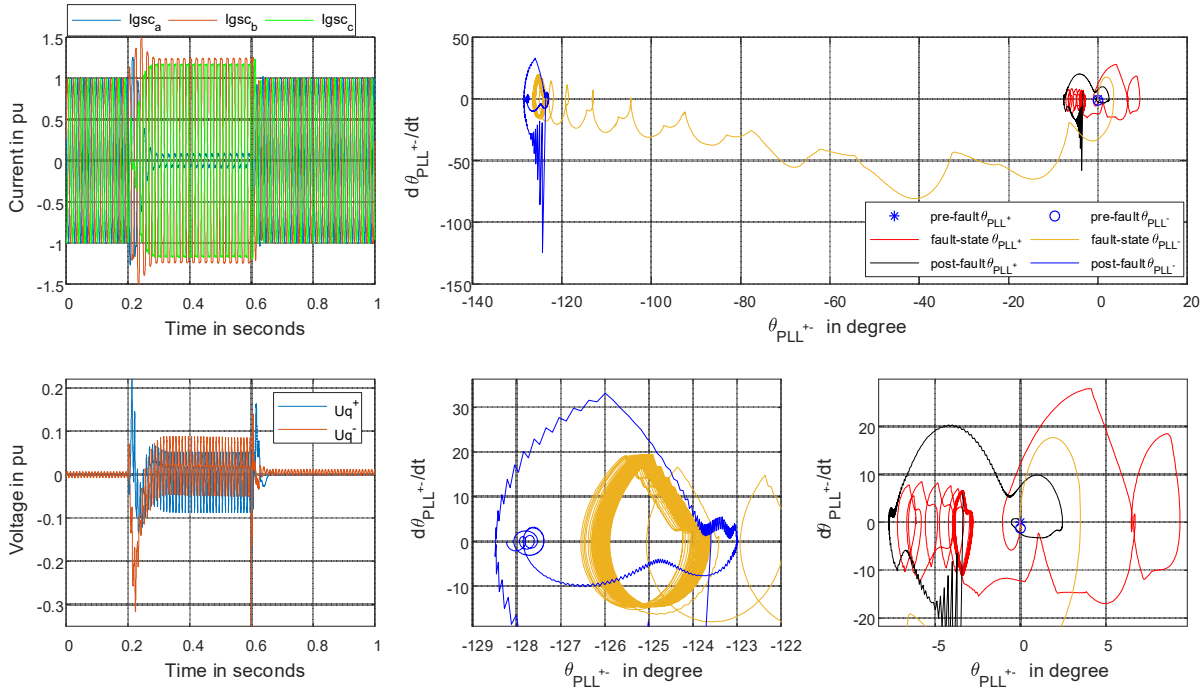

Fig. 10: Experimental validation of stability criterion with high active power and negative sequence reactive power injection during fault (I_d^+ = 1.2 p.u., I_q^- = 1.2 p.u.)

Conclusion

This paper investigates the fault behavior of PLL based grid-connected converters for unsymmetrical faults. The theoretical relation of stable equilibrium points (SEP) for the PLL is derived and leads to a stability criterion based on the grid conditions and converter feed-in power. It can be seen that with weaker grids it becomes more difficult for the PLL to stay stable during faults. Furthermore, the positive and negative sequence PLL are coupled through a grid factor and the converter feed-in current. On the one hand, the neglection of the coupling for low unsymmetrical grids results in a quite accurate analytical solution of the periodically SEP.

On the other hand, the coupling cannot be neglected during an unsymmetrical fault-state with a high injection of negative sequence current. For example, it is shown that a reactive current feed-in at the negative sequence can help to reach a SEP for the positive sequence PLL. In order to investigate the transient process of the pre-fault, fault and post-fault conditions accurately, the phase portrait method is been introduced. Subsequently, the stability criterium is evaluated for a line-to-line short-circuit through varying current injections. Finally, the stability criterion was validated with real-time-system experiments. It can be concluded that the approach is accurate to investigate the availability of SEPs for unsymmetrical grid faults. In future works, the behavior of different PLL algorithms and converter controllers will be investigated in more detail.

References

[1] N. Jaalam, N. A. Rahim, A. Bakar, C. Tan, and A. M. Haidar, “A comprehensive review of synchronization methods for grid-connected converters of renewable energy source,” Renewable and Sustainable Energy Reviews, vol. 59, pp. 1471–1481, 2016, doi: 10.1016/j.rser.2016.01.066.

[2] H. Wu and X. Wang, "Design-Oriented Transient Stability Analysis of PLL-Synchronized Voltage-Source Converters," in IEEE Transactions on Power Electronics, vol. 35, no. 4, pp. 3573-3589, April 2020

[3] Z. Zhang, R. Schuerhuber, L. Fickert and K. Friedl, "Study of stability after low voltage ride-through caused by phase-locked loop of grid-side converter", in International Journal of Electrical Power & Energy Systems, Volume 129, 2021

[4] VDE/FNN, "Technical Requirements for the Connection and Operation of Customer Installations to the High Voltage Network (TAR High Voltage)", 2017

[5] X. He, C. He, S. Pan, H. Geng, and F. Liu, “Synchronization Instability of Inverter-Based Generation During Asymmetrical Grid Faults,” IEEE Trans. Power Syst., vol. 37, no. 2, pp. 1018–1031, 2022, doi: 10.1109/TPWRS.2021.3098393.

[6] Z. Zhang, C. Lehmal, P. Hackl, and R. Schuerhuber, “Transient Stability Analysis and Post-Fault Restart Strategy for Current-Limited Grid-Forming Converter,” Energies, vol. 15, no. 10, p. 3552, 2022, doi: 10.3390/en15103552.

[7] L. Harnefors, "Modeling of Three-Phase Dynamic Systems Using Complex Transfer Functions and Transfer Matrices," in IEEE Transactions on Industrial Electronics, vol. 54, no. 4, pp. 2239-2248, Aug. 2007

[8] B. Wang, S. Wang and J. Hu, "Dynamic Modeling of Asymmetrical-Faulted Grid by Decomposing Coupled Sequences via Complex Vector," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 9, no. 2, pp. 2452-2464, April 2021

[9] Z. Zhang, R. Schuerhuber, L. Fickert, F. Katrin, C. Guochu, and Z. Yongming, “Domain of Attraction`s Estimation for Grid Connected Converters with Phase-Locked Loop,” IEEE Trans. Power Syst., p. 1, 2021, doi: 10.1109/TPWRS.2021.3098960.

[10] H. Wu and X. Wang, “Transient Stability Impact of the Phase-Locked Loop on Grid-Connected Voltage Source Converters,” in 2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia), Niigata, 52018, pp. 2673–2680.

[11] A. A. Nazib, D. G. Holmes, and B. P. McGrath, “Decoupled DSOGI-PLL for Improved Three Phase Grid Synchronisation,” in 2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia), Niigata, 52018, pp. 3670–3677.