Study on Commutation Loop Inductance and Current Distribution to DC-link Capacitors in a GaN Half-bridge

Benedikt Kohlhepp, Samuel Faber, Jeremias Kaiser and Thomas Dürbaum
Electromagnetic Fields, Friedrich-Alexander University Erlangen-Nürnberg (FAU)
Konrad-Zuse-Strasse 3/5
91052 Erlangen, Germany
Tel.: +49 (0)9131 85 28951
Fax: +49 (0)9131 85 27787
E-Mail: benedikt.kohlhepp@fau.de
URL: https://www.emf.tf.fau.de/

Keywords

«Parasitic inductance», «Gallium Nitride (GaN)», «Half-bridge».

Abstract

Modern wide bandgap power semiconductors allow for increased efficiency compared to conventional semiconductors by faster switching transients. In order to harness the full performance from these components, parasitic inductances must be minimized. FEM simulations can deliver the parasitic inductances and thus, can be used to optimize the PCB layout and the placement of semiconductors and DC-link capacitors. Also cost constraints apply to most of the power electronic circuits. FEM simulations can facilitate the determination of cost optimized designs by reducing the amount of DC-link capacitors. Therefore, the current distribution incorporating the DC-link capacitors is required. An analysis of a GaN half-bridge shows the potential to omit one poorly utilized MLCC capacitor.

Introduction

Today's demands regarding power electronic circuits, high efficiency and power density as well as low cost call for advanced circuit topologies and modern power electronic components [1]. Thus, wide bandgap (WBG) semiconductors are inevitably required to increase the efficiency [2]. In order to estimate the efficiency, accurate loss predictions are necessary for each component involved [3] [4]. While conduction loss calculation of power semiconductor devices is relatively easy [2], switching loss estimation is quite challenging especially for WBG semiconductors [5] [6] [7]. As WBG devices can feature extremely fast switching transitions, circuit parasitics stemming from the device's package, the DC-link capacitor's interconnection, and the printed circuit board (PCB) layout become more prominent. For a profitable application of WBG semiconductors, circuit parasitics have to be reduced in order to fully exploit their advantages with regard to fast switching. Current GaN power semiconductors feature extremely low inductive packages as these are ball grid array (BGA) packages, also called chip scale package [8]. Due to these optimized packages, the resulting switching transients mainly depend on the inductances induced by the PCB interconnection and DC-link capacitors [9]. During the switching transitions, the commutation loop inductance causes overvoltages [10]. Furthermore, the semiconductor's output capacitance in conjunction with the commutation loop's inductance induces oscillations in the power loop. Overvoltages as well as the oscillations can lead to increased switching losses and deteriorate the electromagnetic interference (EMI) behavior [11].

Low cost means using the right (optimized) components, which are driven to their limits. Thus, in case several DC-link capacitors connected in parallel are used, the current distribution to the individual capacitor is of relevance. This allows an evaluation of the component utilization. Therefore, the current distribution to the capacitors can be used to find the optimal placement of the capacitors. In the best case scenario, this can lead to savings in components and hence, to lower cost.

In order to gain the required information regarding the commutation loop inductance, different measurement methods like vector network analyzers (VNA) [12], time domain reflectometry (TDR) [13]

or impedance measurements [14] can be applied. Another possibility is to use numerical simulations [9] [15] exploiting e.g. FEM, which also allow to study the current distribution within the PCB and components. Therefore, this paper first introduces the half-bridge circuit and the modeling of all components involved within the simulation. Then, the commutation loop inductance is studied for different models of the DC-link capacitors. After that, the current distribution to the DC-link capacitors is studied depending on the frequency and also for different models of the DC-link capacitors. The paper also shows the current density on the PCB's copper layers.

Half-Bridge Configuration

As a basic building block for power electronic converters, the half-bridge circuit is used for the study of the parasitic inductances of the PCB and the current distribution. Fig. 1 (left) depicts the schematic of the half-bridge with both semiconductors T_{HS} and T_{LS}, the accompanying gate circuits and DC-link capacitor C_{DC}. The gate circuits comprise separated connections for turn-on and –off with $R_{\mathrm{g,HS,On}}$, $R_{\mathrm{g,LS,On}}$ and $R_{\mathrm{g,HS,Off}}$, $R_{\mathrm{g,LS,Off}}$. The schematic includes the boot-strap C_{Boot} as well as the bypass capacitor C_{Bypass}. Fig. 2 (left) shows the section of the half-bridge of the PCB layout which is derived from the schematic as top and side view. As can be seen from Fig. 2 (left), the PCB is made up from a 4-layer stackup with a copper thickness of 70 µm. The power semiconductors feature a low inductive BGA package and are 100 V GaN-HEMTs. The gate-driver also comes in a BGA package, allowing low inductive interconnections.

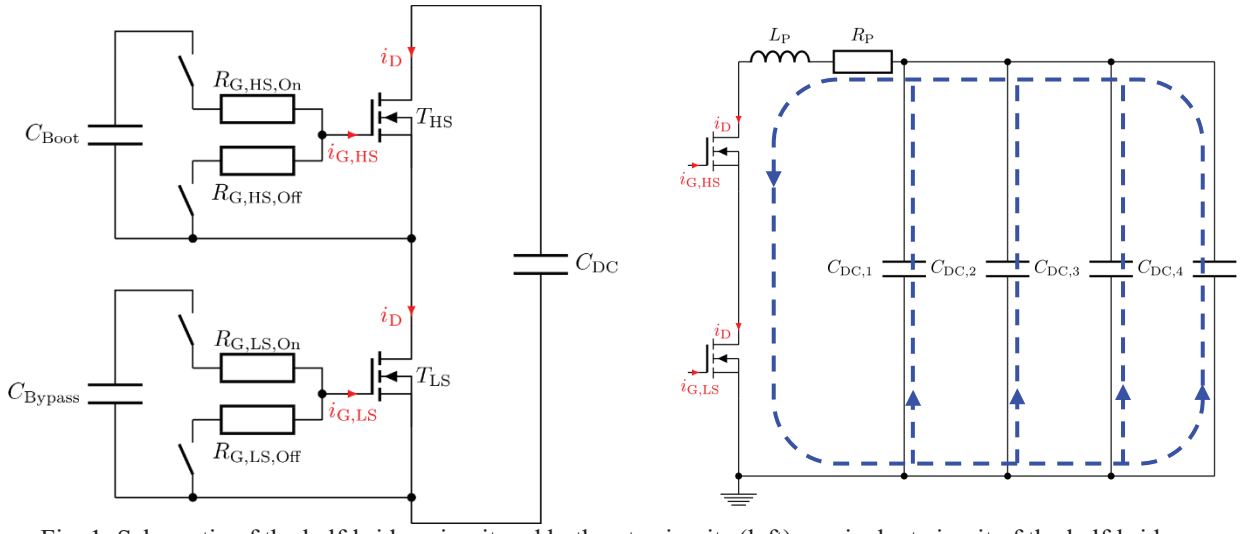

Fig. 1: Schematic of the half-bridge circuit and both gate circuits (left); equivalent circuit of the half-bridge (right)

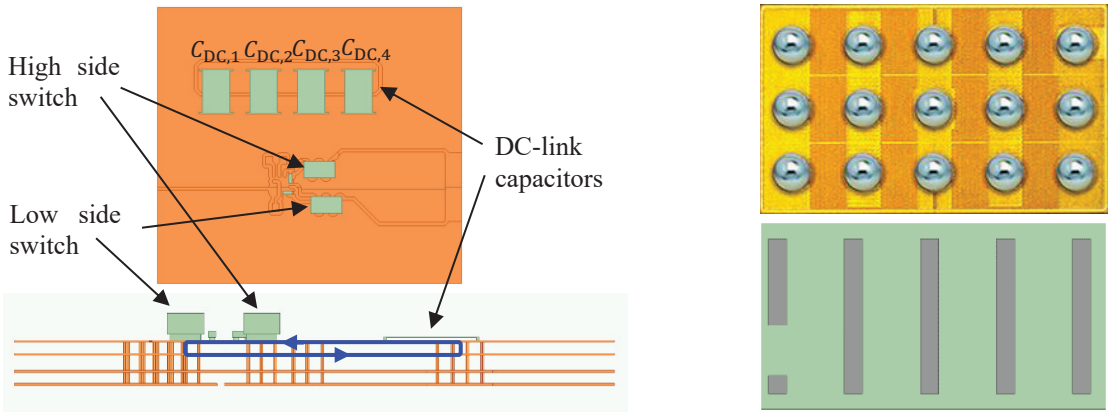

Fig. 2: Layout of the half-bridge circuit and both gate circuits; top view (upper) and side view (lower) (left); solder bump view of the studied device *[8]* and simulation model for the device (right)

All components are mounted on the top layer of the PCB as SMD devices. The DC-link capacitors $C_{\mathrm{DC,1}}$, $C_{\mathrm{DC,2}}$, $C_{\mathrm{DC,3}}$, $C_{\mathrm{DC,4}}$ (see Fig. 2 (left)), are placed directly next to the half-bridge semiconductors. The half-

bridge's commutation loop starts at the lower pads (positive terminals) of the DC-link capacitors and connects to the drain of the upper switch on the top layer. A copper polygon on the top layer links both half-bridge semiconductors and forms the half-bridge midpoint. Filled vias within the source pads of the lower switch bring the commutation loop to the first inner layer (distance 360 µm). In this layer, the commutation loop passes back to the DC-link capacitors again. The ground pads of the DC-link capacitors also feature filled vias, and thus, close the commutation loop. As only the first two layers are used for commutation loop design, low commutation loop inductance can be expected [16]. On the top layer the gate loops are also routed. These do not have discrete (external) gate resistors, which ensures small gate loops. In general, for each loop inductances can be defined. Furthermore, mutual couplings must be considered, which represent the interaction between the loops. In some literature, this fact is neglected, but for an accurate study, it is vital [15]. In this paper, only the overall commutation loop inductance L_P shall be studied. The resulting equivalent circuit shows Fig. 1 (right). In addition to the commutation inductance, [9] also examines the inductance of the gate circuits and the mutual coupling.

Component Models

Suitable models for all components are crucial for gaining the circuit parasitics of the PCB. The DC-link capacitors consist of four SMD ceramic capacitors in a 1210 case and are located relatively close to the semiconductors. As their impedance decreases with higher frequencies, they are replaced by a short in simulation. In order to study the impact of the capacitor's shape, four different models are used. The first one is a thin copper yoke with a thickness of 100 µm and a distance of 100 µm above the PCB surface, which can be seen in Fig. 3 (a). Secondly, a copper yoke is used which has the same dimensions with respect to the pads as the MLCC capacitors (see Fig. 3 (b)). The height is chosen so that the thickness of the conductive material is in the range of twice the skin depth at 100 MHz. An approximation of the skin depth δ gives:

$$\delta = \sqrt{\frac{2}{2\pi f \mu \kappa}} \tag{1}$$

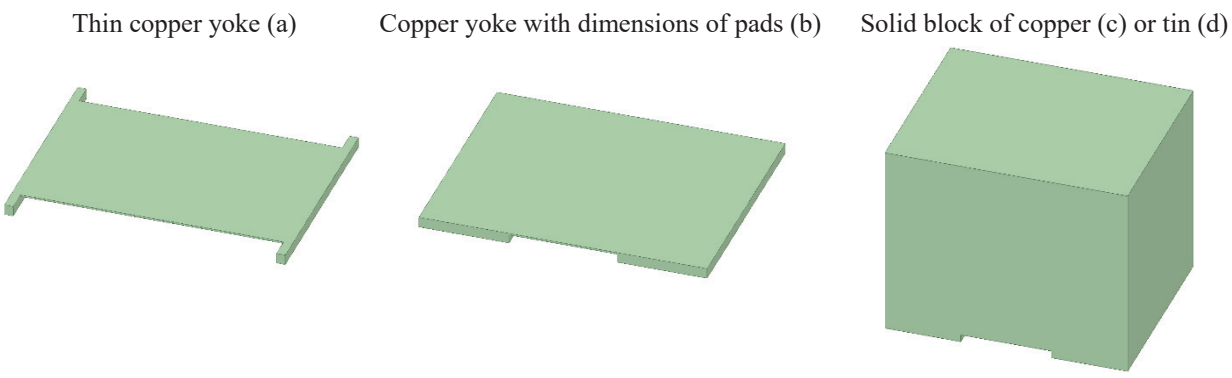

Fig. 3: Different models for the MLCC DC-link capacitors

Equation (1) uses the permeability μ and the electrical conductivity κ [17]. Thus, Fig. 3 (b) represents a rough estimation of an "averaged" current path through the capacitors at high frequencies. Configuration (c) and (d) in Fig. 3 are solid blocks with the dimensions of the MLCC capacitors. There is a groove on the bottom side of the blocks, which forms two contact surfaces (pads) of the capacitor. These have the same size as the pads of the capacitors. (c) is a copper block ($58 \cdot 10^6$ 1/Ωm). Obviously, modeling the MLCC capacitors by solid conductive blocks is not realistic. As the current distribution depends on the electrical conductivity of the materials, two different materials with different electrical conductivity should be studied. The cause for this behavior is the skin as well as the proximity effect, which impact the current distribution within conductive materials at high frequencies. This is why tin with an electrical conductivity of $8.7 \cdot 10^6$ 1/Ωm is studied as well. It has a significantly lower electrical conductivity compared to copper. Furthermore, accurate models for the GaN devices are necessary. In on-state the semiconductors can be modeled by copper blocks with identical dimensions. These devices feature an extremely low inductance as they come in a ball grid array (BGA) package. The solder bumps (balls) must be considered as well, as their size is not negligible compared to the packages. The drain's and source's balls are column wise

connected together to cuboids. The bump for the gate is also cubic. Fig. 2 shows on the right side the solder bump view of the device as well as the solder bump representation (grey) within the simulation model (green).

Study on Commutation Loop Inductance

This section studies the commutation loop inductance of the GaN-half-bridge circuit. For the analysis, ANSYS Maxwell3D eddy current is applied, which uses the quasi-stationary approximation of the Maxwell equations to solve field problems [18]. This analysis neglects displacement currents and thus wave propagation. It allows to obtain the current distribution within conductive material by using the finite element method (FEM). From the current distribution, the DC and AC inductance for the frequencies of interest can be obtained.

Fig. 4 (left) shows the commutation loop's inductance depending on the frequency from 10 kHz up to 100 MHz for the four configurations (a) to (d) given in Fig. 3. All curves drop with rising frequency, as for low frequencies, the inductance comprises the inner as well as the outer inductance. The inner inductance results from the energy stored within the conductor. As a consequence of the skin effect within the conductors (PCB traces and planes) the current is superseded to its surface with increasing frequency. For 10 kHz, the skin depth, according to (1), is much higher than the PCB traces' thickness (70 µm). The PCB interconnections are made of copper with $\kappa = 58 \cdot 10^6$ 1/Ωm. Thus, the skin effect's impact is relatively small for low frequency. At 1 MHz, the copper thickness and skin depth according to (1) are in the same range and for high frequencies (100 MHz), it is well below the copper thickness. As a consequence, with rising frequency, the inner inductance vanishes.

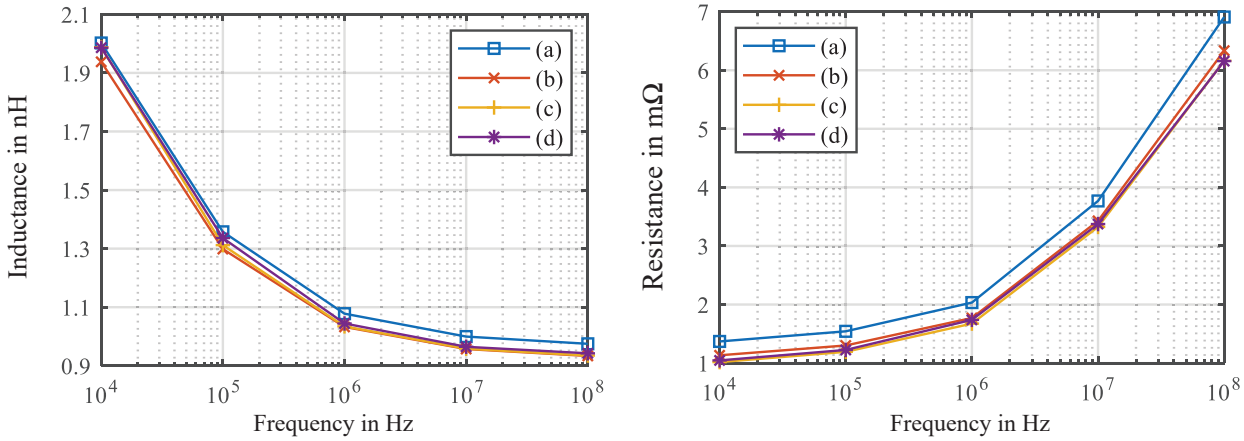

Fig. 4: Comparison of the commutation loop's self inductance depending on the frequency (left); comparison of the commutation loop's resistance depending on the frequency (right)

A second effect also impacts the resulting inductance. With rising frequency, the current distribution within the loop changes. This results in a current distribution that minimizes the inductance. Thus, the self-inductance typically drops with rising frequency. For low frequency, configuration (a) has the highest inductance for all frequencies studied, as the contact surface of the model (a) is only a narrow web. Furthermore, (a), (c), and (d) exhibit higher inductance compared to (b), as the current path is longer. For high frequencies, the inductance of (b), (c), and (d) are approximately the same, since the current is restricted to the lower part of the solid conductive blocks of (c) and (d) to minimize inductance. Thus, the current paths of this three models are nearly the same. All in all, the deviation in inductance is less than 50 pH. This study shows that the modeling of the capacitors has only a negligible effect on the inductance at high frequencies. Of course, the layer thickness of the copper also impacts the resulting inductance. For the intended application, 70µm copper thickness is chosen, as relatively high currents occur. Furthermore, [19] confirms the results gained by the study conducted here. [19] reports a slightly lower inductance, but due to manufacturing reasons, the commutation loop studied here has larger dimensions resulting in higher inductance. Hence, other reasons may impact the selection of the capacitor model used. This could be, for example, the computational effort (simulation time) or the memory consumption. Solid blocks (c) and (d) typically require more memory because the entire volume must be finer discretized by FEM. Fig. 4 (right) shows the commutation loop's resistance depending on the frequency for the four configurations of Fig. 3.

Studying the resistance shows, that (a)'s resistance is slightly higher for the complete frequency range under investigation. This results from the longer current path and the thin conductive structure of the yoke (a). All curves increase with rising frequency, which stems from the skin and proximity effect.

Study on Current Distribution of Capacitors

This section studies the current distribution to the MLCC capacitors. Firstly, configuration (c) (solid copper blocks), is used to model the capacitors. In order to ensure accurate simulation results, the mesh should be fine at the capacitor's cross sections and the commutation loop. Fig. 5 depicts the current density on the capacitor's cross section (in the middle between both pads) at 10 kHz (upper) and 10 MHz (lower). Using a frequency of 10 kHz shows that the current nearly fully utilizes the cross section of the capacitors. An increased current density is visible near the first copper layer of the PCB (lower part of the capacitors). However, if a significantly higher frequency is set, the current is displaced to the lower part of the surface. This results in a higher current density in the lower part than at the top. This result gained by simulation corresponds to the expectations, since the current flows at high frequencies in such a way that the loop area, i.e. the inductance, is low. It can also be seen from this figure that capacitors 3 and 4 carry a higher current than capacitors 1 and 2. This applies regardless of the frequency investigated.

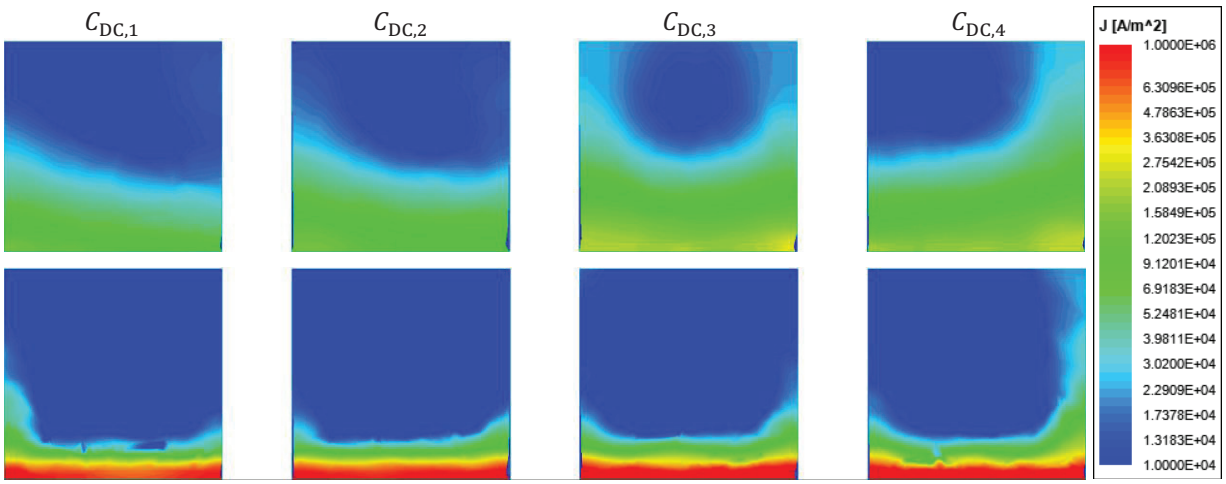

Fig. 5: Current density (logarithmic) on the DC-link capacitor's cross section for the four capacitors at 10 kHz (upper); current density on the DC-link capacitor's cross section for the four capacitors at 1 MHz (lower)

For a quantitative assessment of the current distribution along the capacitors, the current density must be integrated over the cross section of each individual capacitor. Therefore, the normal component $\hat{J}_y$ of the current density is integrated:

$$\hat{\imath} = \left| \iint_A \hat{\underline{J}} \cdot \mathrm{d}\vec{A} \right| = \left| \iint_A \hat{J}_y \mathrm{d}A \right| \tag{2}$$

A is the cross section of the individual capacitor. These calculations are directly carried out using the calculation tool provided by ANSYS Maxwell3D. Fig. 6(left) shows the current distribution of the four MLCC capacitors using configuration (c) in the range of 10 kHz up to 100 MHz. Regardless of the frequency, capacitor 1 takes less than 16 % and capacitor 2 conducts approximately 20 % of the overall current. Studying the current shares of capacitor 3 and 4 shows that these components together carry roughly 2/3 of the overall current regardless of the frequency studied.

In order to better understand the current distribution of the capacitors, the current density on the surface of the PCB can also be analyzed. Fig. 7 in the upper part shows the current density at the PCB's top layer for 10 kHz, 1 MHz, and 100 MHz for configuration (c) (solid copper blocks). In order to see the return path of the commutation loop, the first inner layer must be displayed as well. The lower part of Fig. 7 depicts the first inner layer also for solid copper blocks. The MLCC DC-link capacitors are indicated by dashed red rectangles in all six plots. All field distributions of Fig. 7 show a top view to the PCB. These current density distributions can then be used to draw conclusions about the current paths on the PCB. It can be seen that, regardless of the frequency, a very high current density occurs at the finger-like structure of the power semiconductors (top layer), which is due to the fact that the conductive surface is small there. At a

frequency of 100 MHz, the current flows mainly at the edges of the finger-like structure of the half-bridge switches. Thus it seems that the total current in the loop is smaller than at lower frequencies. For all simulations a current of 1 A is used. Studying the top layer at 10 kHz confirms that capacitor 3 takes the highest portion of the overall current, as the current density is highest at its terminals compared to all other capacitors. Furthermore, from the top layer at 10 kHz it can be seen that the PCB area between the upper half-bridge switch and capacitor 3 has the highest current density (it occurs in light blue and green). For higher frequencies, the current shifts more and more to capacitor 4 (see Fig. 6 (left)), which can also be verified by the field plots of PCB's top layer for 1 MHz and 100 MHz. For 100 MHz, the field plot is a little bit blurred, as the mesh is not fine enough to plot the current density. Nevertheless, the variation in results for a more detailed mesh will not give better results, but significantly enhances computational effort. When looking at the current density within the first inner layer of the PCB (see Fig. 7 (lower)), there is an area looking like a 'hole', which is a recess in the first inner layer of the board, as there are vias connecting the top layer to the bottom of the board. These are mainly needed for heat dissipation (thermal vias) ensuring sufficient cooling of the upper half-bridge switch during operation. As this "conductive material free" zone directly lies between the upper half-bridge switch and capacitor 3, this is one reason, why capacitor 4 takes the largest portion of the overall current.

Secondly, the current distribution on the capacitors will also be studied for the different configurations from Fig. 3. This study can give an indication of whether the current distribution on the PCB in the simulation changes with different models of the capacitors. If it remains approximately the same with different MLCC capacitor models, it can be concluded that the modeling of the capacitors has only a minor influence on the current distribution resulting in the simulation. Thus, Fig. 6 (right) depicts the current distribution to the capacitors at 1 MHz for the different capacitor models (a) to (d) given in Fig. 3. In principle, the distribution remains constant regardless of the model used for the capacitors. Models (b) to (d) in particular show almost the same results. For (a) there is a little deviation from the others visible. This model consists of only one thin copper bar, thus introducing more inductance compared to the other models. This can already be seen from the evaluation of the commutation inductance in Fig. 4 (left). For this reason, the current is more evenly distributed among the four capacitors, since their connection to the half-bridge switches concerning the inductance is now no longer dominated by their position on the board, but rather by the capacitor model.

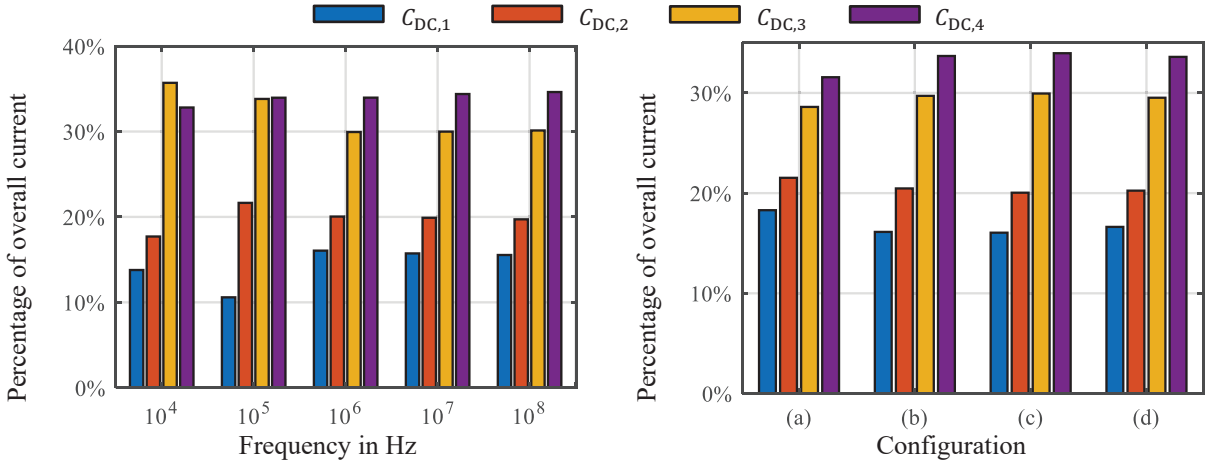

Fig. 6: Current distribution for the DC-link capacitors depending on the frequency for configuration (c) (left); comparison of different configurations at 1 MHz (right)

Discussion

From the study, one can conclude that the model used for the capacitors has only a minor impact on the resulting commutation loop inductance as well as on the current distribution to the paralleled DC-link capacitors within the studied PCB layout.

On the basis of this study, it can now be considered how the capacitors should ideally be placed. Since capacitor 1 only takes a very small proportion of the total current, this component may be omitted. This measure reduces the cost of the capacitors by 25 %. However, it should be noted that it must be verified whether the total capacitance of the parallel connection of 3 capacitors is still sufficient for the application.

In addition to the capacitance value itself, the capacitors must also be capable of handling the ripple current induced by the half-bridge operation.

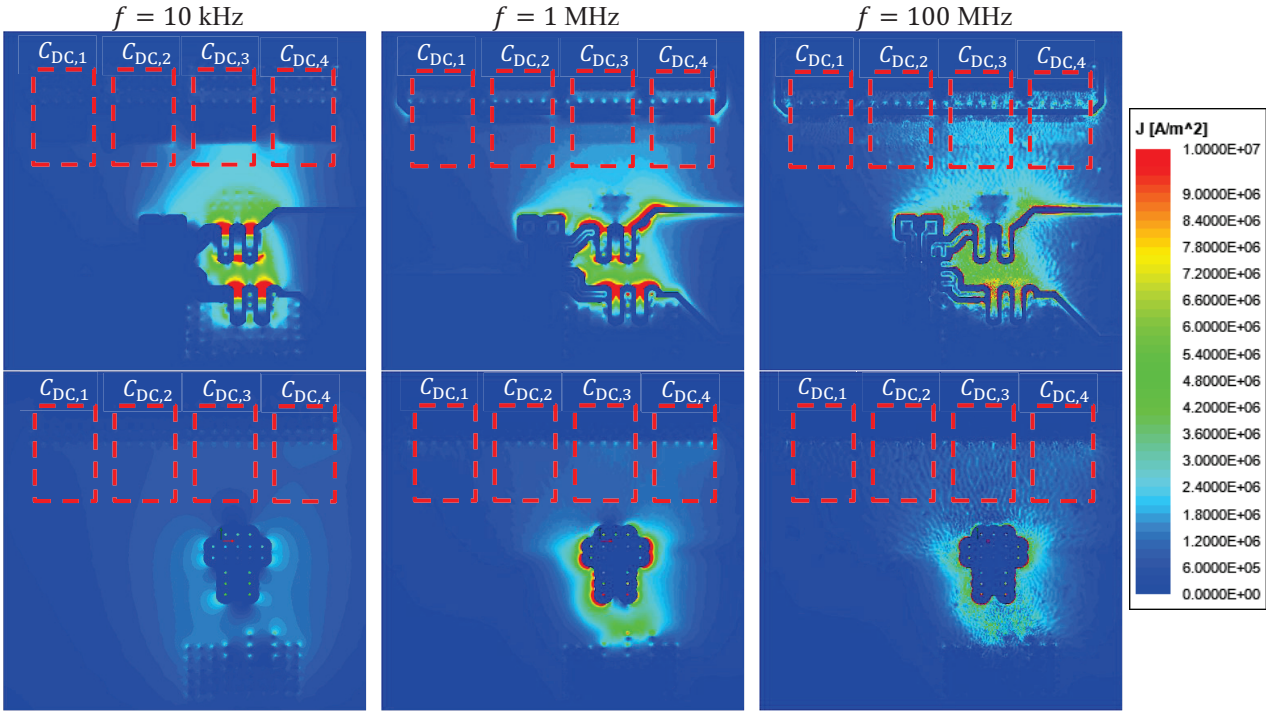

Fig. 7: Current density within the top layer (top view) of the PCB for different frequencies (upper); current density within the first inner layer (top view) of the PCB for different frequencies (lower)

Conclusion

In order to gain full performance from fast switching semiconductors like GaN, parasitic elements within the commutation cell must be minimized. As these inductances are in the sub-nH range, measuring them is quite difficult. Thus, FEM simulations of the PCB is the only way to obtain this information. In a GaN half-bridge circuit, the parasitic inductances are studied for different models of the MLCC DC-link capacitors. The commutation loop's inductance, which is one of the relevant inductances concerning the switching behavior, shows only a small impact (930 pH to 970 pH) depending on the capacitor's model. In order to build a cost effective design, the current distribution to the DC-link capacitors must also be investigated if several are connected in parallel. The analysis gives recommendations for further actions concerning component savings.

References

[1] B. Kohlhepp, J. Heubeck, and T. Duerbaum, "Non-ideal Behavior of ZVS Inverter Comprising Variable and Fixed Frequency Operation: Analysis, Compensation, and Verification," *Power Electronic Devices and Components*, p. 100007, Apr. 2022, doi: 10.1016/j.pedc.2022.100007.

[2] B. Kohlhepp, D. Kübrich, M. Tannhäuser, A. Hoffmann, and T. Dürbaum, "Test Setup for Dynamic ON-State Resistance Measurement of High- and Low-Voltage GaN-HEMTs Under Hard and Soft Switching Operations," *IEEE Transactions on Instrumentation and Measurement*, vol. 69, no. 10, pp. 7740–7751, Oct. 2020, doi: 10.1109/TIM.2020.2985186.

[3] B. Kohlhepp, M. Barwig, and T. Dürbaum, "Efficiency Comparison of an Asymmetrical Half-Bridge PWM Converter with Schottky and Synchronous Rectification," in *2018 53rd International Universities Power Engineering Conference (UPEC)*, Sep. 2018, pp. 1–6, doi: 10.1109/UPEC.2018.8542033.

[4] B. Kohlhepp, D. Kuebrich, S. Peller, and T. Duerbaum, "Test setup using DC metering approach for loss measurements of inductive components – principle, characterization, validation and application," *IET power electron.*, pp. 1–15, Jun. 2021, doi: 10.1049/pel2.12155.

[5] B. Kohlhepp, D. Kübrich, R. Schwanninger, and T. Dürbaum, "Switching Loss Estimation of GaN-HEMTs by Thermal Measurement Procedure," in *PCIM Europe digital days 2021; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, May 2021, pp. 1–8.

[6] B. Kohlhepp, D. Kübrich, and T. Dürbaum, “Switching Loss Measurement – A Thermal Approach Applied to GaN-Half-Bridge Configuration,” in *2021 23st European Conference on Power Electronics and Applications (EPE ’21 ECCE Europe)*, Sep. 2021, pp. 1–8.
[7] B. Kohlhepp, D. Kuebrich, and T. Duerbaum, “Experimental Study of the Coss-Losses Occurring During ZVS Transitions – Emphasis on Low and High Voltage GaN-HEMTs,” in *CIPS 2020; 11th International Conference on Integrated Power Electronics Systems*, Mar. 2020, pp. 1–6.
[8] Efficient Power Conversion Corporation, “Datasheet EPC2045 – Enhancement Mode Power Transistor.” El Segundo, 2018.
[9] B. Kohlhepp, S. Faber, J. Kaiser, and T. Dürbaum, “Extraction of Parasitic Elements of a Printed Circuit Board applied to a GaN Half-Bridge,” in *PCIM Europe digital days 2022; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, May 2022, pp. 1–8.
[10] Efficient Power Conversion Corporation, “Application Note - How to Design an eGaN FET-Based Power Stage with an Optimal Layout.” El Segundo, 2018.
[11] Y. Shen, J. Jiang, Y. Xiong, Y. Deng, X. He, and Z. Zeng, “Parasitic Inductance Effects on the Switching Loss Measurement of Power Semiconductor Devices,” in *2006 IEEE International Symposium on Industrial Electronics*, Montreal, Que., Jul. 2006, pp. 847–852, doi: 10.1109/ISIE.2006.295745.
[12] T. Liu, T. T. Y. Wong, and Z. J. Shen, “A New Characterization Technique for Extracting Parasitic Inductances of SiC Power MOSFETs in Discrete and Module Packages Based on Two-Port S-Parameters Measurement,” *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9819–9833, Nov. 2018, doi: 10.1109/TPEL.2017.2789240.
[13] S. Hashino and S. Toshihisa, “Separation measurement of parasitic impedance on a power electronics circuit board using TDR,” in *2010 IEEE Energy Conversion Congress and Exposition*, Atlanta, GA, Sep. 2010, pp. 2700–2705, doi: 10.1109/ECCE.2010.5618046.
[14] R. S. Krishna Moorthy *et al.*, “Estimation, Minimization, and Validation of Commutation Loop Inductance for a 135-kW SiC EV Traction Inverter,” *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 286–297, Mar. 2020, doi: 10.1109/JESTPE.2019.2952884.
[15] X. Geng, K. Kuring, M. Wolf, O. Hilt, J. Würfl, and S. Diekerhoff, “Study on the Optimization of the Common Source Inductance for GaN Transistors,” in *2021 23st European Conference on Power Electronics and Applications (EPE ’21 ECCE Europe)*, Sep. 2021, p. P.1-P.10, doi: to be published.
[16] Efficient Power Conversion Corporation, “White paper - Optimizing PCB Layout.” El Segundo, 2019.
[17] M. Albach, “Induktivitäten in der Leistungselektronik.” Wiesbaden: Springer Fachmedien, 2017.
[18] ANSYS Inc., “Maxwell3D Help.” Canonsburg, 2020.
[19] D. Reusch and J. Strydom, “Understanding the Effect of PCB Layout on Circuit Performance in a High-Frequency Gallium-Nitride-Based Point of Load Converter,” *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 2008–2015, Apr. 2014, doi: 10.1109/TPEL.2013.2266103.