Function Blocks of a Highly-Integrated All-in-GaN Power IC for DC-DC Conversion

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Keywords

«Emerging technology», «Gallium Nitride (GaN)», «Monolithic power integration», «Power integrated circuit», «DC-DC converter».

Abstract

GaN-on-Si technology is on the advance for the use in power ICs thanks to wide bandgap performance combined with a lateral structure and a low-cost carrier substrate. A common GaN power IC platform with several active and passive devices, as well as analog and digital circuits is presented. This platform is used to integrate periphery function blocks of power electronics circuits, such as driving, sensing, protection, and control. In detail, an efficient GaN-based gate driver with integrated bootstrap capacitances is realized, which has a current consumption of only 2.2 mA at a supply voltage of 5 V and a switching frequency of 1 MHz. Furthermore, a GaN-based voltage mode control is described based on a PWM generator with error amplifier and verified with measurements. Finally, the circuit design of an all-in-GaN power IC for DC-DC conversion with half-bridge, driver, level shifter, dead time and voltage mode control is presented. With small additional chip area, further function blocks can be integrated to the power device(s) to realize a modern highly-efficient and highly-functional GaN-based conversion component for the next generation of power electronics.

Introduction

Gallium nitride (GaN) technology is increasingly used in power integrated circuits (ICs) due to its superior physical properties combined with its lateral structure. These characteristics enable the rapid development of a new generation of power electronics, progressively reducing the size, losses and costs of these systems and their applications. In this way, first GaN power ICs on low-cost Silicon (Si) substrates have been successfully launched on the market [1–3]. Usually, Si-based BCD (Bipolar-CMOS-DMOS) technologies are used for power or power management ICs. However, the next generation of power IC platforms require more area-efficient power devices. This offers the GaN-on-Si technology with a similar range of active and passive devices to give designers the greatest possible flexibility. GaN power ICs consisting of power devices with additional periphery or function blocks such as gate driver, sensing, protection circuity and even control can lead to an increased performance.

The development of GaN power ICs was initiated over a decade ago by academia and then driven and accelerated by industry, with GaN power ICs recently being made commercially available. Especially the companies Efficient Power Conversion EPC, Navitas Semiconductor, and Innoscience as well as start-ups like Wise-Integration, GaNPower International, and Cambridge GaN Devices CGD offer GaN

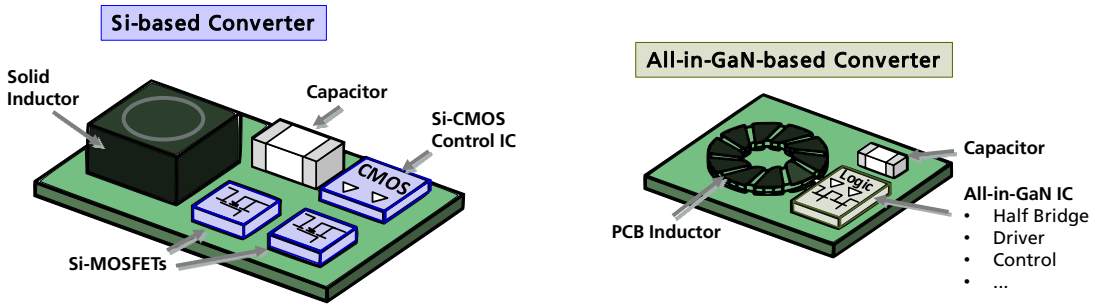

Fig. 1: Low-voltage DC-DC converter: (Left) State of the art with Si power MOSFETs, discrete Si-based driver and control and (right) vision of the future with an all-in-GaN-based converter with GaN power IC, which integrated power devices, driver and control.

ICs with several function blocks such as gate driver, sensing and protection circuits [1]. In particular, EPC's ePower™ Stage includes a half-bridge with driver, level shifter, logic and under-voltage lockout (UVLO) [3]. This GaN IC should be suitable for 48 V systems in battery-powered and motor applications, in the automotive or industrial sector, and in IT infrastructures. The interest in the introduction of 48 V system is the reduction of power consumption and cabling volume compared to 12 V solutions. Usually low-voltage DC-DC converters or point-of-load (PoL) converter consist of two Si-based power MOSFETs configured to a half-bridge with drivers and control in CMOS technology as well as a solid power inductor, shown in Fig. 1. Recent DC-DC converters with higher power density resulting from higher switching frequencies mostly use GaN-based power semiconductors as a single device or as a half-bridge [4]. The next step for even more compact systems with higher functionality is the integration of the control into the GaN IC, in addition to the power devices and drivers, as an all-in-GaN-based converter, shown in Fig. 1.

This work presents two function blocks, a gate driver with integrated bootstrap capacitors, and a GaN-based voltage mode control of a monolithic all-in-GaN power IC for DC-DC conversions up to 48 V. The used GaN technology is described and the design of the two function blocks as well as the all-in-GaN power IC is presented. Measurements of the functional parts are shown. The all-in-GaN IC shows a higher level of integration into GaN technology with higher functionality and power density in the future.

GaN Power IC Platform

The epitaxial structures of the GaN-on-Si technology starts with a conductive Si substrate. A multilayer GaN buffer and an AlGaN barrier are grown above. The AlGaN/GaN heterojunction establishes a highly conductive two-dimensional electron gas (2DEG) with a sheet resistance of ~600-800 Ω/□, which is used as drift and depletion zone for the high-electron-mobility Transistors (HEMT) and other devices. A p-GaN layer caps the devices and is structured into the p-GaN gate. The p-GaN layer shifts the threshold voltage of the standard Schottky gate into positive values. Four metallization with corresponding passivations are used for ohmic contacts, interconnections and field plates. Fig. 2 shows a simplified cross-section of the GaN power IC platform with several active and passive devices.

The active devices are enhancement-/depletion-mode (e-/d-mode) HEMTs, Schottky barrier diodes (SBDs), and lateral field-effect rectifiers (LFERs) [5] for low-voltage (LV) or high-voltage (HV) applications from 12 – 650 V. To increase the operating voltage, the depletion zone must be extended, which in turn increases the drift zone and the on-resistance. The field plate allows the depletion zone to be reduced while maintaining the same breakdown voltage. As an example, the gate-width scaled on-resistance result in 6.5 Ω×mm for a 12 V-class and 15.1 Ω×mm for a 650 V-class e-mode HEMT. Layout structures are also being investigated that enable area-efficient power devices for low-voltage applications [6].

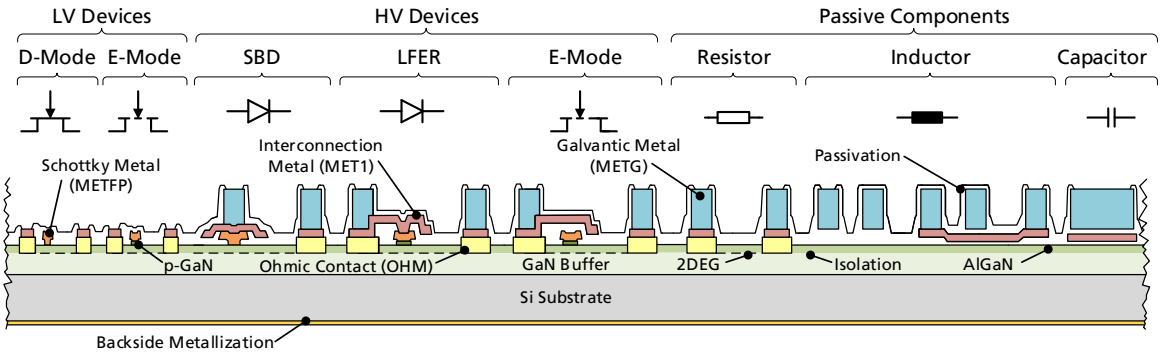

Fig. 2: Simplified cross-section of the GaN-on-Si technology as GaN power IC platform. In the platform, there are several active devices such as e-/d-mode HEMTs, Schottky barrier diodes (SBDs), and lateral field-effect rectifiers (LFERs) as low-voltage (LV) or high-voltage (HV) devices. In addition, there are passive components such as resistors, inductors, and capacitors.

Passive components can also be integrated into the technology. Resistors can be realized by the four metal layers or the 2DEG. On-chip capacitors can be realized as metal-insulator-metal (MIM) structures or can be extended by stacking resulting in a capacitance density of 0.22 – 1.16 fF/µm^2. The p-GaN gate capacitors offer the counterpart to MOS capacitors from Si-based IC technologies. This capacitor has a high capacitance density of 1.19 fF/µm^2, but it is highly non-linear with a low voltage range from the threshold voltage up to ~6.5 V. In addition, on-chip spiral inductors are designed with inductances of <50 nH. The use as power inductors was investigated in [7] with associated thermal considerations.

The work uses a digital and analog library previously created by the authors, which includes area-efficient standard cells for layout design, as well as schematic symbol and simulation models based on measurement data, which allows a complete design flow. The technology is limited to the direct-coupled FET logic (DCFL) due to the lack of p-type devices. Unlike CMOS logic, DCFL has large static currents, limiting the amount of GaN logic that can be practically integrated. The digital library (NOT, NOR, NAND, AND, OR, RS flip-flop, Schmitt-Trigger) have a miniaturized standard cell with a height of 50 µm, supply voltage of 5 V, max. static currents of ≤0.3 mA, and high noise margins. The analog building blocks include differential amplifiers and comparators with e-/d-mode differential pair for sensing, protection circuits or analog controls. In addition, voltage references with and without temperature compensation, current mirrors and linear regulators are also included in the analog library [8].

With these devices and building blocks in this GaN power IC platform, power electronic circuits with power devices and additional function blocks such as gate driver, protection and sensing circuits and even control can be realized and monolithically integrated.

GaN-Based Gate Driver

GaN power devices with integrated gate drivers allow to increase the switching frequency by reducing the gate loop inductance. Furthermore, critical ringing and overshoot can be reduced. There are different gate driver concepts: first approaches started with a push-pull stage [9], over approaches with additional logic inverters or NOT gates [10] up to drivers with boot-strapping concepts [10, 11] and even with *dV*/*dt* control [12, 13], temperature compensation [14], and over-current protection (OCP) [15–18]. All these gate drivers have the same push-pull output stage (consisting of two e-mode transistors in series). The push-pull stage has the disadvantage, if the pull-up transistor is turned-on with the supply voltage V_{DD}, that the output swing is reduced by the threshold voltage $V_{TH,E}$. There are three possibilities to avoid the output voltage drop and to ensure a rail-to-rail output: First, V_{DD} can be increased, which in turn causes higher gate stress and additionally degradation as well as positive V_{DD}-shift of the p-GaN gates [10]. Second, the output voltage is pulled-up to V_{DD} with a bootstrap circuit with one supply voltage [10, 11]. Last possibility, the pull-up transistor is either turned-on with $2\times V_{DD}$ with an additionally generated second supply voltages [15], e.g. also realized by bootstrapping.

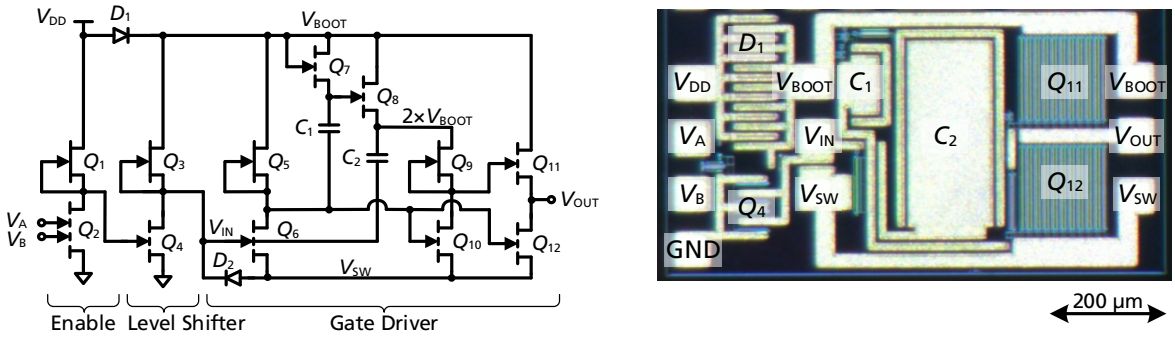

Fig. 3: (Left) Schematic and (right) chip photo of a bootstrap-based gate driver additionally with level shifter, bootstrap diode for bootstrap supply for high-side gate driver and input logic for enabling.

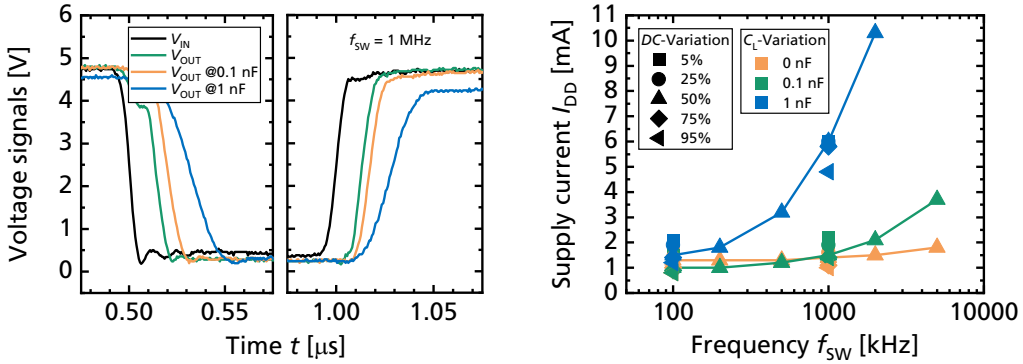

Fig. 4: (Left) Falling and rising edge of the gate driver with f_{SW} = 1 MHz, V_{BOOT} = 5 V and three different load capacitors of C_L = 0/0.1/1 nF. (Right) Power supply current I_{DD} as function of the frequency f_{SW} with different duty-cycles and load capacitors.

In the GaN power IC platform of this work, a gate driver has been implemented according to [15]. Fig. 3 shows the schematic and layout of the bootstrap-based gate driver additionally with a level shifter, bootstrap diode for high-side gate driver and an input logic for enabling. The circuit is realized on a small chip area of 865×455 µm^2 with pads. The transistors of the gate driver are all e-mode HEMTs of the 12 V-class. Here Q_5 and Q_6 form a logic inverter, Q_7, Q_8 with C_1 and C_2 a bootstrap circuit and Q_9-Q_{12} a single input inverted buffer. This bootstrap circuit provides a voltage of $2\times V_{DD}$ instead of $2\times V_{DD}$-V_{T0} for the not gate of the single inverted input buffer, whereby V_{DD} is here equal to V_{BOOT} and V_{T0} is the turn-on voltage in case of only a bootstrap diode. The stacked MIM capacitor C_1 and C_2 have a capacitance of approx. 5 pF and 50 pF. The gate widths of the push-pull stage are 3 mm and of the two NOT gate 10/100 μm for pull-up/down device. The gate driver can be used for high-side (HS) and low-side (LS) and has been designed and optimized for low power-consumption.

Fig. 4 shows the measured falling and rising edge of the input V_{IN} and output V_{OUT} of the fabricated gate driver with f_{SW} = 1 MHz, V_{BOOT} = 5 V and three different load capacitors of C_L = 0/0.1/1 nF. Without load capacitor, the propagation delay for on $t_{D,ON}$ and off $t_{D,OFF}$ is about 13 ns each, resulting mainly from the multi-stage approach. These delays increase with larger load capacitance: 17.32 ns and 19.71 ns for 0.1 nF and 28.55 ns and 30.65 ns for 1 nF. Fig. 4 also shows the power supply current I_{DD} as function of the frequency f_{SW} with different duty-cycles DC and load capacitors. The supply current increases with increasing frequency and load capacitor. However, as DC increases, the current decreases, because more energy is shorted at the gate. The max. switching frequency of the gate driver is >5 MHz. The typical input capacitance of the main GaN power transistors of the half-bridge is about 100 pF. At a switching frequency of 1 MHz, the max. supply current with 0.1 nF is 2.2 mA, which is efficient. The quiescent supply current is about 1.6 mA, mainly from the static currents of the logic circuit which is realized without a CMOS technology. In comparison, the EPC2152 ePower™ Stage with GaN half-

bridge driver, logic and UVLO has a quiescent current of 22 mA and a current consumption of 29 mA at a switching frequency of 1 MHz [19]. Due to the high quiescent currents in GaN compared to CMOS drivers, an external series cut-off circuit is proposed in [20]. Compared with CMOS drivers, the quiescent currents are increased, but the current consumption with higher frequencies is smaller with GaN drivers [21, 22].

GaN-Based Voltage Mode Control

The voltage mode control (VMC) is the most widespread control method of a synchronous buck converter due to its simplicity. The output voltage of the power stage is compared with a reference voltage V_{REF} and the duty-cycle is adjusted based on the error. There are already publications on GaN-based control, such as voltage mode control with duty-cycle switcher [16] or the cycle-by-cycle peak current control [17]. Also PWM generators based on a comparator and sawtooth generator have been published [23–25]. For closed loop control, a compensation network for the error amplifier is used to ensure stable operation of the synchronous buck converter.

In the GaN power IC platform of this work, a voltage mode control has been implemented according to [24] with error amplifier, which are shown in Fig. 5. The sawtooth generator in turn consists of a hysteresis comparator with two external resistors R_1, R_{FB} for the feedback network and a charging unit (NOT gate) with external sawtooth capacitor C_{SAW}. The error amplifier as well as comparator also for the sawtooth generator is a two-stage amplifier consisting of a differential amplifier with source follower, which were already presented in [8]. The circuit is realized on a not fully filled test IC with chip area of 1×1 mm^2 and pads for higher flexibility. The transistors and diodes are all devices of the 12 V-class.

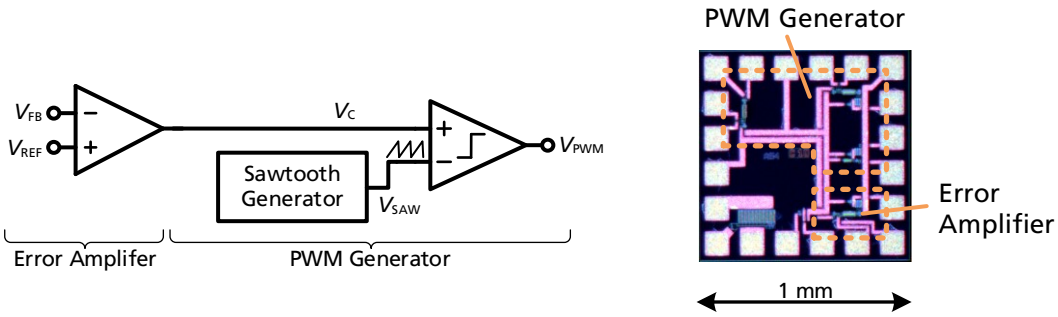

Fig. 5: (Left) Schematic and (right) chip photo of a voltage mode control based on an error amplifier and PWM generator consisting of a sawtooth generator and comparator.

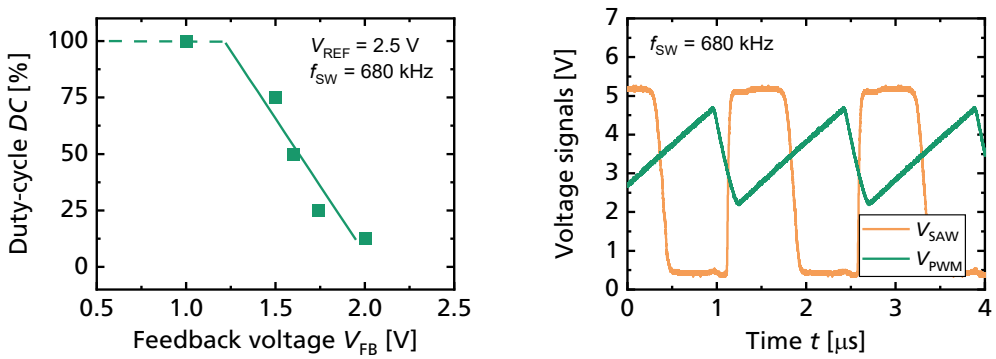

Fig. 6: (Left) Duty cycle DC of the PWM generator as function of the feedback voltage V_{FB} of the error amplifier at five measured points and linear fit over the $DC < 100\%$. (Right) Sawtooth and PWM time signals with duty-cycle of 50%.

The sawtooth generator has the following external components: R_{FB} = 100 kΩ, R_1 = 15 kΩ, C_{SAW} = 470 pF. These components can change the sawtooth frequency f_{SW} as well as the amplitude of the sawtooth as analyzed in [23–25]. Depending on the values, the amplitude of the sawtooth increases up to a maximum of 6 V with increased sawtooth capacitance and covers sawtooth frequencies of about 0.5-1.5 MHz. Fig. 6 shows the measured and resulting duty-cycle *DC* of the PWM generator as function of the feedback (input) voltage V_{FB} and V_{REF} = 2.5 V at five measured points and a linear fit over the DC < 100%. The measured frequency f_{SW} = 680 kHz results from the R_{FB}, R_1, C_{SAW} dimensioning. The min. *DC* is limited by the falling edge of the sawtooth and is 12% in this operating point. Fig. 6 also shows the PWM and sawtooth time signals at *DC* = 50% and f_{SW} = 680 kHz. The PWM generator and the error amplifier require a supply voltage of 12 V. The current consumption is ~10 mA ±2 mA depending on the operation point. The power consumption of this circuit can be further reduced by smaller dimensioning of the resistors, or using other means to increase the resistance (for lower static consumption) of the logic devices.

All-in-GaN Power IC for DC-DC Conversion

The all-in-GaN power IC integrates a symmetrical half-bridge, driver for HS and LS switch, bootstrap diode, level shifter, dead time and voltage mode control. This GaN IC was designed for a synchronous buck converter with DC-DC conversion up to 48 V. The chip is realized on an area of 3×2.5 mm^2 with the presented GaN power IC platform and is shown in Fig. 7.

The half bridge consists of HS and LS HEMT with a gate width of 105 mm, a channel length of 4.7 µm and comb layout. The half-bridge is suitable up to 48 V with breakdown voltage over 80 V. The HS gate driver is shown in Fig. 8. Both gate drivers are based on a DCLF inverter Q_1/Q_2, a bootstrapped DCFL inverter Q_3/Q_4, D_2, C_1 and a push-pull stage Q_5/Q_6 (different to the previously presented GaN-based gate driver). The push-pull stage has the disadvantage, if the pull-up transistor is turned-on with the supply voltage V_{DD}, that in the high-level output voltage has a voltage drop of the threshold voltage. A bootstrap circuit of the previous DCFL inverter consisting of diode D_2 and capacitor C_1 avoids this voltage drop,

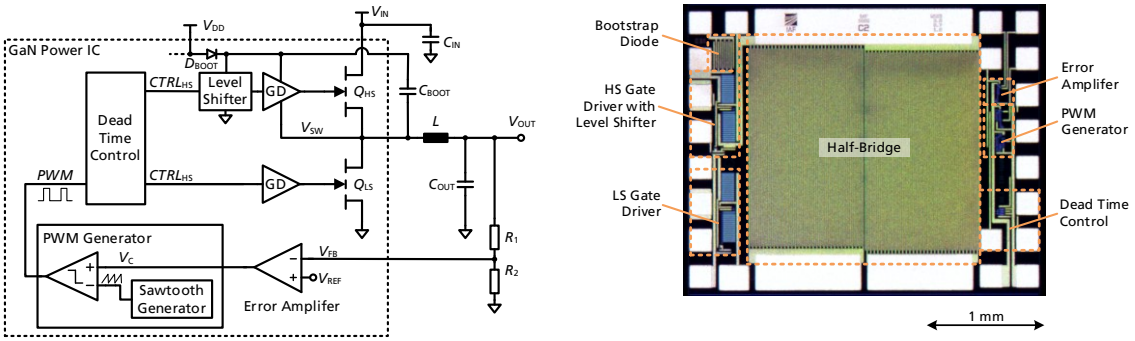

Fig. 7: GaN Power IC for a synchronous buck converter consisting of a half-bridge with driver, level shifter, dead time control, and voltage mode control. (Left) Schematic and (right) chip photo.

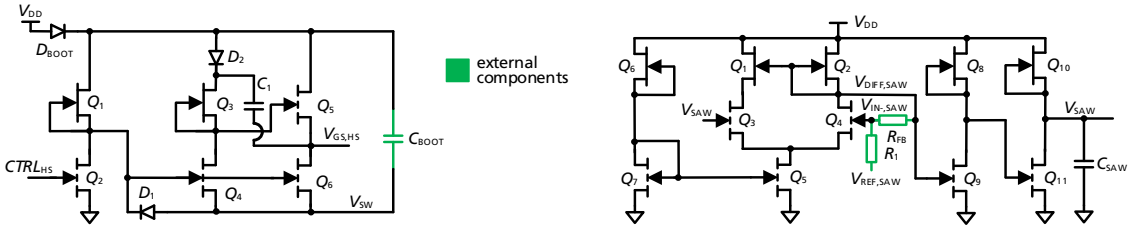

Fig. 8: Schematic of (left) HS gate driver with bootstrap voltage supply and (right) sawtooth generator consisting of a hysteresis comparator and a charging unit.

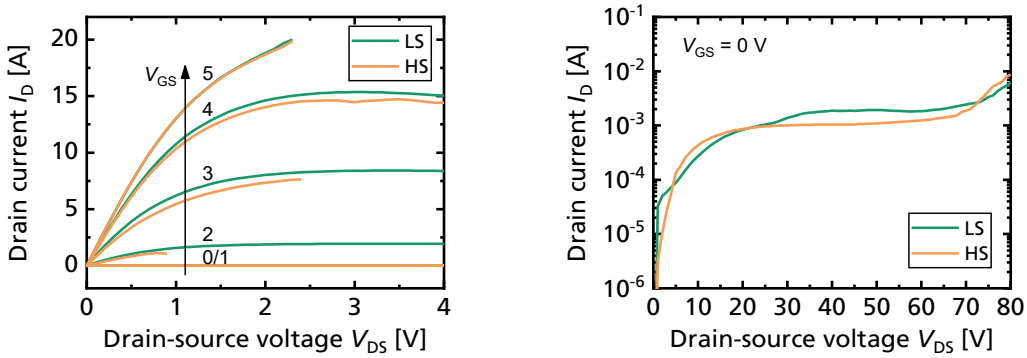

Fig. 9: Symmetrical half-bridge consisting HS/LS HEMT with comb layout: (Left) Output characteristic with different gate-source voltages from 0 V to 5 V and (Right) breakdown characteristic at V_{GS} = 0 V.

as described before. These capacitors C_1 in the HS and LS gate driver are also integrated in the GaN IC, such that no external capacitors are required for the gate drivers. In addition, compared to the layout in Fig. 3, the capacitors are further area-optimized by realizing them as stacked MIM capacitors under a connection pad, which increases the area efficiency and reduces the external number of components. The first DCFL inverter is used in the HS gate driver for the level shifting of the signal. In addition, this level shifter has a protection diode D_1 to limit the input of the gate driver in off-state. This gate driver approach based on three stages has the advantage of a non-inverting single input, unipolar supply, and rail-to-rail output. For a bootstrap supply of the HS gate driver, an additional diode D_{BOOT} was integrated. However, the bootstrap capacitor C_{BOOT} must be wired externally due to the high capacitance value, shown in Fig. 7. The dead time is realized by logic gates and integrated MIM capacitors. The voltage mode control is based on a PWM generator consisting of comparator and sawtooth generator and an error amplifier with external type III compensation network. The sawtooth comparator in turn consists of a hysteresis comparator and a charging unit, shown in Fig. 8 and similar to the previously presented GaN-based voltage mode control. The feedback network of the hysteresis comparator R_{FB} and R_1 is wired externally, but the capacitor for the sawtooth comparator C_{SAW} is again integrated. The hysteresis band or amplitude and output voltages of the sawtooth generator can adjusted by the resistance ratio R_{FB}/R_1 or R_1/R_{FB} and the reference voltage $V_{REF,SAW}$ of the used comparator. All periphery of the GaN IC has a supply voltage of 5 V.

The IC has already been processed and statically characterized. Fig. 9 shows experimental on-wafer pre-characterization of the symmetrical half-bridge. The output characteristic shows different curves with a gate-source voltage from 0 V to 5 V. The on-resistance is 68 mΩ at V_{DS} = 0.5 V and V_{GS} = 5 V. The drain current I_D in blocking mode with V_{GS} = 0 V is <2 mA at V_{DS} = 50 V. Depending on the thermal management and the output voltage, this IC can provide an output power >120 W at an output voltage of 24 V depending on the output current.

The integrated GaN synchronous buck converter demonstrates a higher level of integration into the GaN technology with higher functionality resulting in low system cost or bill of materials (BOM). At the same time, the losses can be further reduced, especially the losses of the driver and the control, and a higher power density of the system can be realized. The area of the driver, sensing, and control is only 28.6% while the power devices (in this case the half-bridge) is 71.4% of the chip area. This is a small additional area to the power devices for further functionality and higher compactness. Furthermore, the area of the control has several pads for higher flexibility, which has a negative effect on the area utilization. However, the IC can also be used without the control or in boost converter configuration. Thus, the power electronic designer has a higher flexibility and can use the individual function blocks independently.

Conclusion

This work presents function blocks of a highly-integrated all-in-GaN power IC for DC-DC conversion. Therefore, a GaN power IC platform is shown with several active devices such as e-/d-mode HEMT, SBD, LFER for low and high voltages and passive components such as resistors, capacitors and inductors. In addition, digital and analog libraries are described. With the help of this GaN power IC platform two function blocks are designed. On the one hand a highly-integrated gate driver with a bootstrapping approach and on the other hand a voltage mode control. The gate driver is characterized by its low power consumption, e.g. 1.6 mA quiescent supply current and 2.2 mA at a switching frequency of 1 MHz and a load capacitance of 0.1 nF. The voltage mode control integrates of a PWM generator consisting of sawtooth generator and comparator, and error amplifier. Exemplary measurements are shown at a switching frequency of 680 kHz. Finally, a circuit design of an all-in-GaN power IC consisting of symmetrical half-bridge, half-bridge gate driver, level shifter, dead time control and voltage mode control is described. IV measurements of the half-bridge are shown as a first verification. Thus, this highly-integrated GaN IC shows an example of a modern highly-functional and highly-efficient GaN-based power conversion component for the next generation of power electronics resulting in low system cost or bill of materials.

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