

# Solving Duty-ratio Limitation for Four-phase Input-Parallel Output-Series DC-DC Converter with Asymmetrical PWM Scheme

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**Abstract--** The literature has conducted many studies on the input-parallel output-series (IPOS) converter. To increase the voltage gain, by synthesizing two single IPOS converters, a four-phase input-parallel output-series (4P-IPOS) converter was introduced recently. However, the duty ratio must be greater than 0.5 (i.e.,  $D > 0.5$ ) for the converter to work correctly, so it suffers from duty-ratio limitation. Moreover, there was no study on using a bipolar DC grid or a dual-output configuration. This paper proposed an asymmetrical PWM scheme, which easily implements to solve the duty-ratio limitation of the 4P-IPOS converter. Additionally, the use of a dual-output connection is studied. As a result, the converter not only can work with  $D < 0.5$  and maintains the high voltage gain (i.e.,  $\frac{V_o}{V_{in}} = \frac{4}{1-D}$ ), but also achieve outputs voltage balancing (i.e.,  $V_{o1} = V_{o2}$ ) as well as currents balancing (i.e.,  $I_{L1} = I_{L2}, I_{L3} = I_{L4}$ ). An 800-W prototype converter is used in simulation and experimentation to validate the suggested PWM technique.

**Index Terms--** Asymmetrical pulse-width modulation (PWM), boost converter, current balancing, dual-output, high step-up converter, input-parallel output-series (IPOS) converter, voltage balancing.

## I. INTRODUCTION

With the increasing acquisition of renewable energy sources, the high voltage gain non-isolated DC-DC boost converter has recently been researched in the literature. High voltage gain means high input current and high output voltage. Due to the input current and the output voltage being shared between inductors and capacitors, respectively, the input-parallel output-series (IPOS) converter (see Fig. 1) [1]-[7] is a potential structure. The switches' ( $S_2$  and  $D_2$ ) voltage stresses are half the total output voltage ( $V_o$ ). And the voltage gain of the IPOS converter is a double step-up function (i.e.,  $\frac{V_o}{V_{in}} = \frac{2}{1-D}$ ).

Recently, the four-phase input-parallel output series (4P-IPOS) converter was created to raise the voltage gain to double its previous level by synthesizing two block IPOS converters [8]. The main advantages of the topology are the high voltage gain (i.e.,  $\frac{V_o}{V_{in}} = \frac{4}{1-D}$ ) and currents balancing (i.e.,  $I_{L1} = I_{L2}, I_{L3} = I_{L4}$ ). However, there was no research on using a bipolar DC grid or a dual-output loads connection. Because bipolar configuration provides two

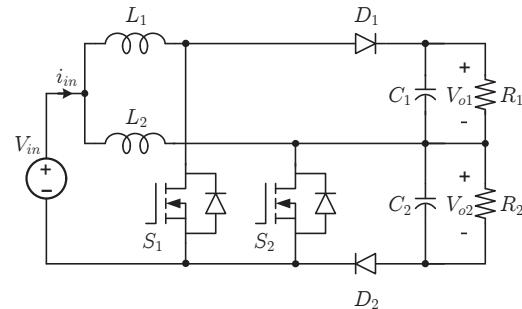


Fig. 1. Input-parallel output-series (IPOS) converter [1-7].

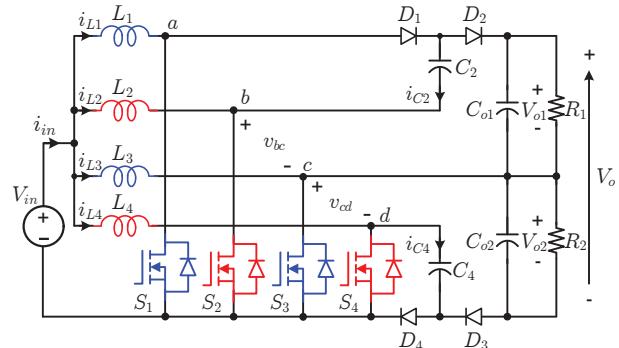


Fig. 2. Four-phase input-parallel output-series (4P-IPOS) converter.

voltage levels, it is flexible and simpler to interface with dc loads with varied power ratings than unipolar one, which is typically required for industrial applications. Due to the two accessible poles that enable a reduction in the distribution voltage with respect to ground, which increases system safety, bipolar systems are also more reliable than unipolar ones. It also enables operation under a line fault and is easily detected and quickly cleared [9]-[13].

Moreover, the converter only works properly when the duty ratio ( $D$ ) is larger than 0.5, so it suffers from duty-ratio limitation [8]. The asymmetrical PWM scheme was introduced recently for series-capacitor (SC) and IPOS converters [14]-[18]. In order to overcome the recommended converter's duty-ratio constraint, this study offered another asymmetrical technique for the 4P-IPOS

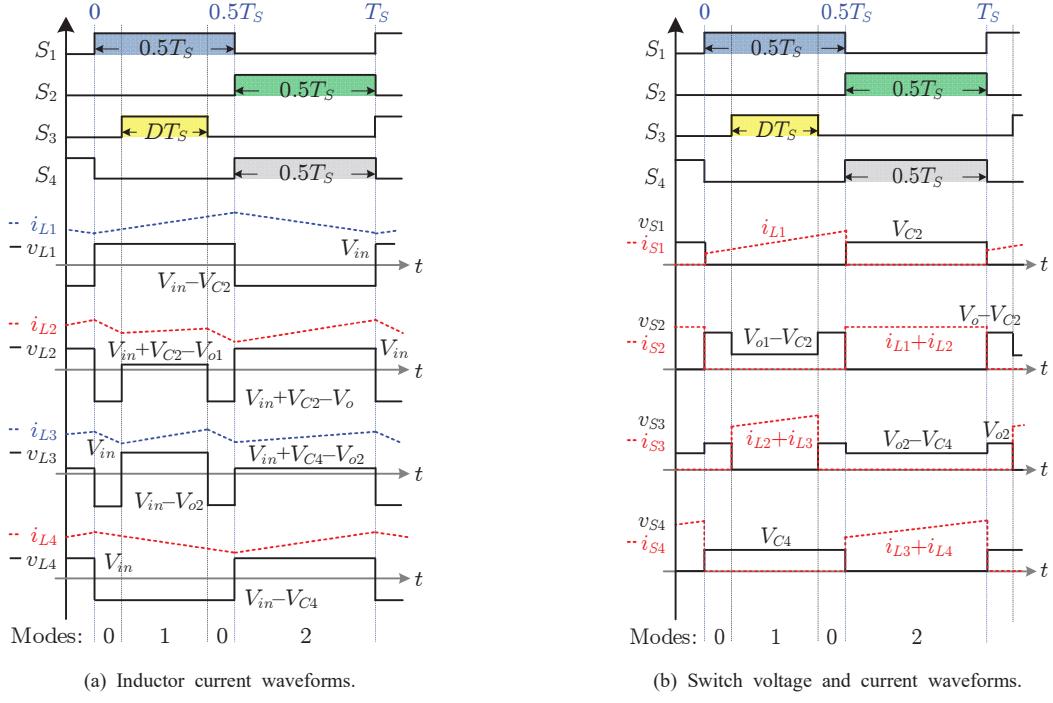


Fig. 3. Key waveforms of the proposed converter. (a) Inductor currents waveforms. (b) Device voltage and current waveforms.

converter. And the operation with a dual-output connection with  $D < 0.5$  is investigated [see Fig. 2]. With the proposed scheme, the converter not only retains all main merits (i.e.,  $\frac{V_o}{V_{in}} = \frac{4}{1-D}$ ) and currents balancing (i.e.,  $I_{L1}=I_{L2}$ ,  $I_{L3}=I_{L4}$ ), but also achieves outputs voltage balancing (i.e.,  $V_{o1}=V_{o2}$ ). All mentioned advantages can be achieved when  $D < 0.5$  or the duty-ratio limitation is eliminated.

The proposed scheme and operation modes of the converter are introduced in Section II. The converter's characteristics can be found in Section III. Sections IV and V present the experimental results and the conclusion, respectively. To validate how well the converter would work with the suggested PWM scheme, an 800-W prototype was created and tested.

## II. PROPOSED ASYMMETRICAL PWM SCHEME AND OPERATION OF THE CONVERTER

The proposed PWM with  $D < 0.5$  is shown in Fig. 3(a). As shown, the duty ratios of the switches are not same. Except for switch  $S_3$ , the duty ratios of other switches are set to 0.5, which can be easily implemented using dual-edge carriers. The gate signals of  $S_2$  and  $S_4$  are in phase and  $180^\circ$  phase-shifted with the  $S_1$  gate signal. The operation of the converter with the proposed PWM scheme when  $D < 0.5$  is illustrated in Figs. 4 and 5, and a detailed analysis is explained as follows. The switch voltage and current waveforms are shown in Fig. 3(b).

- 1) *Mode 0* [Fig. 4(a)]:  $S_1$  is turned-ON, whereas  $S_2$ ,  $S_3$ , and  $S_4$  are turned-OFF.  $L_1$  is charged through  $S_1$ , whereas  $L_2$ ,  $L_3$ , and  $L_4$  are discharged. As shown in

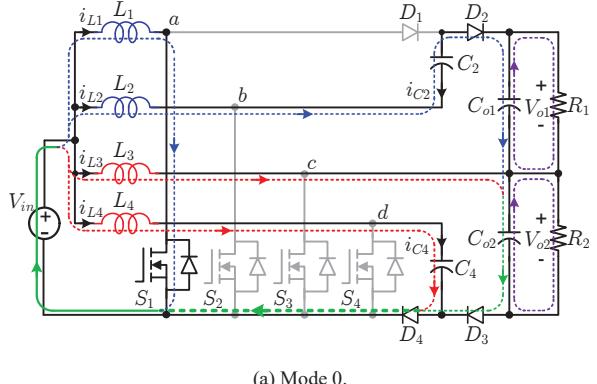


Fig. 4. Operation modes (modes 0 and 1) analysis of the 4P-IPOS converter.

Fig. 6(b), the voltages  $v_{bc}$  and  $v_{cd}$  equal ( $V_{C4} - V_{o2}$ ) and ( $V_{o2} - V_{C4}$ ), respectively.

- 2) *Mode 1* [Fig. 4(b)]:  $S_1$  and  $S_3$  are kept ON, whereas  $S_2$  and  $S_4$  are turned-OFF. Thus,  $L_1$  and  $L_3$  are charged, whereas  $L_2$  releases the energy to load 1 through  $C_2$  and  $D_2$ . The inductor current ( $i_{L4}$ ) flows through  $D_4$  and  $C_4$ . The sum of inductor currents ( $i_{L2}$  and  $i_{L3}$ ) flows through  $S_3$ . The applied voltages ( $v_{bc}$  and  $v_{cd}$ ) are equal to ( $V_{o1} - V_{C2}$ ) and ( $-V_{C4}$ ), respectively.
- 3) *Mode 2* [Fig. 5]:  $S_2$  and  $S_4$  are ON, whereas  $S_1$  and  $S_3$  are OFF. The inductor current ( $i_{L1}$ ) flows through ( $D_1$ ,  $C_2$ ), and inductors  $L_2$  and  $L_4$  are charged, whereas  $L_3$  discharges the energy to load 2.  $S_2$  has sustained the sum of inductor currents ( $i_{L1}$  and  $i_{L2}$ ) and a sum of  $i_{L3}$  and  $i_{L4}$  flow through  $S_4$ . While capacitor  $C_2$  is charged by  $i_{L1}$ , capacitor  $C_4$  is discharged by  $i_{L3}$ . The voltage  $v_{bc}$  equals ( $V_{C4} - V_{o2}$ ) and  $v_{cd}$  equals ( $V_{o2} - V_{C4}$ ), which are the same as mode 0, as shown in Fig. 6(b).

### III. CHARACTERISTICS OF THE CONVERTER WITH THE PROPOSED METHOD

The fundamental waveforms of the proposed converter are shown in Fig. 3(a). The switch current and voltage stresses are shown in Fig. 3, and Fig. 6 shows the waveforms for investigating voltage and current balance. The characteristics of the 4P-IPOS converter with the proposed method are summarized in Table I.

#### A. Output Voltage Balancing ( $V_{o1}=V_{o2}$ )

The capacitor voltages ( $V_{C2}$  and  $V_{C4}$ ) can be determined using the flux (volt-sec) balance condition from the on the inductors ( $L_4$  and  $L_1$ ), as illustrated in Fig. 3(a), and they can be calculated as follows.

$$V_{C2} = V_{C4} = 2V_{in} \quad (1)$$

The voltage waveform on inductor  $L_{23}$  (i.e.,  $v_{bc}$ ) is shown in Fig. 6. The two areas ( $B_1$  and  $B_2$ ) must be same according to the inductor flux (volt-sec) balance condition. The time intervals of  $B_1$  and  $B_2$  are equal to  $0.5T_s$  under the proposed asymmetrical PWM system, yielding the equation below.

$$V_{o1} - V_{C2} = V_{o2} - V_{C4} \quad (2)$$

From (1) and (2), two output voltages ( $V_{o1}$  and  $V_{o2}$ ) are automatically balanced, as indicated in (3). Furthermore, the balancing is guaranteed by the flux balancing of the inductors, which ensures that it is unaffected by the load configurations or device tolerance.

$$V_{o1} = V_{o2} \quad (3)$$

#### B. Voltage Gain Ratio

The output voltage ( $V_{o2}$ ) can be derived as follows utilizing the flux (volt-sec) balance condition from the voltage waveform on inductor  $L_{34}$  ( $v_{cd}$ ), as illustrated in Fig. 6.

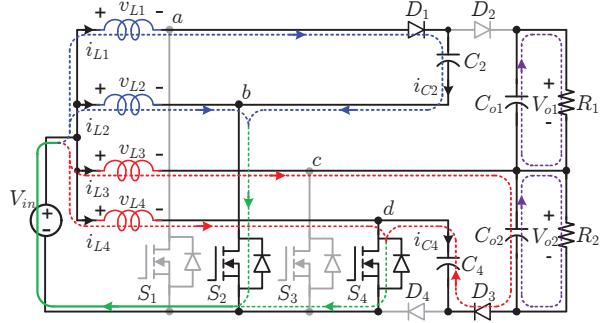
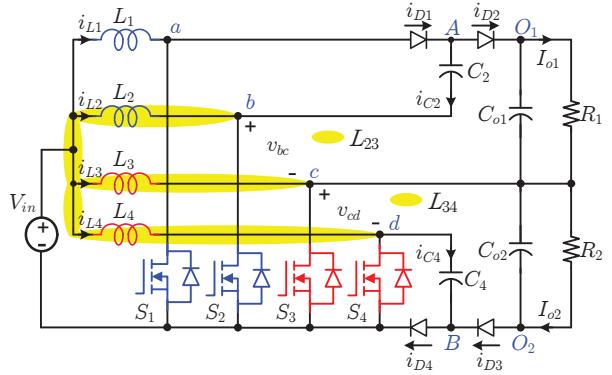
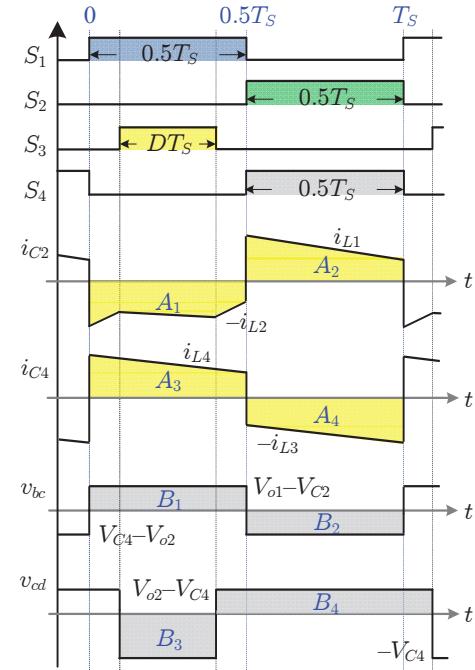


Fig. 5. Operation mode (mode 2) analysis of the 4P-IPOS converter.



(a) Analysis of output voltage and inductor current balancing.



(b) Capacitor current and inductor voltage waveforms

Fig. 6. Analysis of output voltage and inductor current balancing.

TABLE I  
CHARACTERISTICS OF THE CONVERTER WITH THE PROPOSED  
METHOD

Duty ratio ( $D$ )	$D < 0.5$
Voltage gain ( $V_o/V_{in}$ )	$4/(1-D)$
Output voltages balancing	Yes
Inductor currents balancing	Yes
Capacitors voltage ( $V_{C2}, V_{C4}$ )	$2V_{in}$
$i_{S1}, i_{S2}$	$2I_o; 4I_o$
$i_{S3}, i_{S4}$	$2I_o/(1-D)$
Current stress	$i_{D1}, i_{D2}$ $i_{D3}, i_{D4}$
	$2I_o$ $2I_o/(1-D); 2I_o(1+D)/(1-D)$
Voltage stress	$v_{S1}, v_{S2}$ $v_{S3}, v_{S4}$ $v_{P1}, v_{P4}$ $v_{P2}, v_{P3}$
	$0.5V_o(1-D); 0.5V_o(1+D)$ $0.5V_o; 0.5V_o(1-D)$ $V_o; 0.5V_o(1-D)$ $DV_o; 0.5DV_o$
Inductor current ripple	$\Delta I_{L1-2}, \Delta I_{L4}$ $\Delta I_{L3}$
	$0.5(1-D)V_o/(4Lf_s)$ $D(1-D)V_o/(4Lf_s)$
Input current ripple	$\Delta I_{in}$
	$\frac{V_o}{4Lf_s}(1-2D)$
Output voltage ripple	$\Delta V_{Co1}$ $\Delta V_{Co2}$
	$0.5I_{o1}/(Cf_s)$ $DI_{o2}/(Cf_s)$

$$V_{o2} = \frac{V_{C4}}{1-D} \quad (4)$$

The output voltages may be determined using (1), (3), and (4) as follows. The voltage gain ratio is high and twice that of the IPOS converter.

$$V_{o1} = V_{o2} = \frac{2V_{in}}{1-D}; \quad (5)$$

$$\frac{V_o}{V_{in}} = \frac{4}{1-D}$$

### C. Inductor Currents Balancing ( $I_{L1}=I_{L2}; I_{L3}=I_{L4}$ )

The charge (amp-sec) balancing condition on capacitor  $C_2$  may be applied to the waveforms of  $i_{C2}$ , as illustrated in Fig. 6, to determine that the charging and discharging regions must match ( $A_1=A_2$ ). These regions have the same time intervals (i.e.,  $0.5T_s$ ), as illustrated in Fig. 6; hence the inductor currents are equal.

$$I_{L1} = I_{L2} \quad (6)$$

The same analysis can apply to the current waveform of capacitor  $C_4$ . The inductor currents are balanced because of the relationship shown below.

$$I_{L3} = I_{L4} \quad (6)$$

The capacitor charge balancing guarantees the current balancing of the inductors ( $I_{L1}=I_{L2}$  and  $I_{L3}=I_{L4}$ ) such that it is unaffected by device tolerance or load configurations.

## IV. SIMULATION AND EXPERIMENTAL RESULTS

The specifications listed in Table II are used to manufacture an 800 W prototype. In Figs. 7–10, the experimental waveforms are displayed. ( $V_{in}=60$  V,  $V_o=400$  V,  $D=0.4$ ). The experimental waveforms with imbalanced loads are shown in Fig. 7 ( $R_1=200$   $\Omega$ ,  $R_2=100$   $\Omega$ ).

TABLE II  
CIRCUIT PARAMETERS

Symbol	Value	Symbol	Value
$V_{in}$	50~75 V	$C_{o1}, C_{o2}$	200 $\mu$ F
$V_o$	400 V	$C_{24}$	20 $\mu$ F
$P_o$	800 W	Switch	IXFH26N65X2
$f_{sw}$	50 kHz	Diode	RHRG3060
Inductors	230 $\mu$ H	$R_{1-2}$	100 $\Omega$

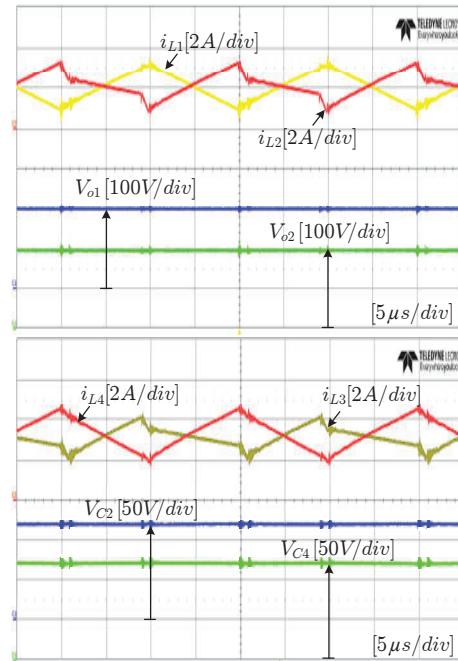


Fig. 7. Experimental waveforms with unbalanced loads ( $V_{in}=60$  V,  $D=0.4$ ,  $V_o=400$  V,  $R_1=200$   $\Omega$ ,  $R_2=100$   $\Omega$ ).

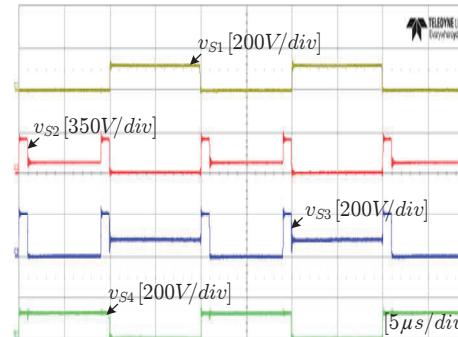


Fig. 8. Switch voltage waveform ( $V_{in}=60$  V,  $D=0.4$ ,  $V_o=400$  V,  $R_1=200$   $\Omega$ ,  $R_2=100$   $\Omega$ ).

As shown, the capacitor voltages are equivalent to double the input voltage, as analysis (i.e.,  $V_{C2}=V_{C4}=2V_{in}=120$  V). Even with imbalanced loads, the inductor currents are evenly balanced ( $I_{L1}=I_{L2}$ , and  $I_{L3}=I_{L4}$ ). In addition, the output voltages are naturally identical as anticipated (i.e.,  $V_{o1}=V_{o2}=60 \frac{2}{1-0.4}=200$  V).

The switch's voltages waveforms are shown in Fig. 8 ( $V_{in} = 60$  V,  $V_o = 400$  V,  $D = 0.4$ ). As can be seen, the outcomes are comparable to the analysis waveforms in Fig. 3. (b). The  $S_3$  voltage stress is half the total output voltage (i.e.,  $0.5V_o$ ). Additionally, the voltage stresses on switches  $S_1$  and  $S_4$  are equal to the voltages on capacitors (i.e.,  $V_{C2} = V_{C4} = 120$  V). Thus, they are lower than the output voltages (i.e.,  $V_{o1} = V_{o2} = 200$  V;  $V_o = 400$  V).

The image of the 800-W prototype converter is depicted in Fig. 9. And Fig. 10 shows the measurement efficiency in relation to output power ( $V_{in} = 60$  V,  $V_o = 400$  V,  $D = 0.4$ ). The converter reaches 95 % efficiency at full power, and the maximum efficiency is 95.9 %.

## V. CONCLUSIONS

This study suggests an easily implementable asymmetrical PWM approach to address the 4P-IPOS converter's duty ratio constraint. The converter using the recommended technique offers the following benefits:

- 1) The converter achieves a high voltage gain (i.e.,  $\frac{4}{1-D}$ ). Compared to the IPOS converter, the voltage gain is double.
- 2) Even with an imbalanced load connection, the inductor currents are naturally balanced (i.e.,  $I_{L1} = I_{L2}$ , and  $I_{L3} = I_{L4}$ ).
- 3) When  $D < 0.5$ , working with a dual-output configuration is studied. Balancing output voltages (i.e.,  $V_{o1} = V_{o2}$ ) is achieved even with imbalanced loads condition.
- 4) With the proposed PWM scheme, all mentioned merits can be obtained when  $D \leq 0.5$ .

Therefore, the proposed approach maintains the core benefits of the 4P-IPOS converter. Additionally, the output voltages are naturally balanced, and the duty-ratio restriction is totally removed. The performance of the proposed technique is tested and validated using an 800-W prototype.

## ACKNOWLEDGMENT

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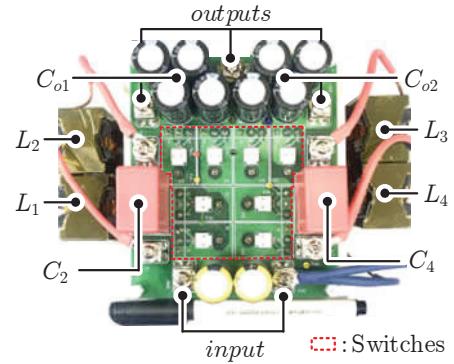


Fig. 9. Photograph of the 800-W prototype.

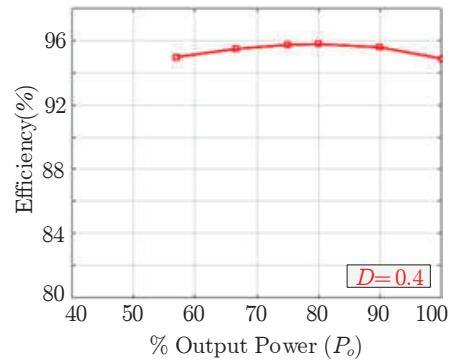


Fig. 10. Efficiency vs. output power ( $V_{in} = 60$  V,  $V_o = 400$  V,  $D = 0.4$ ).

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