Analysis of Capacitor Parasitic Effects on Output Voltage Ripple and Load Transient of DAB Converters

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***Abstract*—The output filter is an essential component of the dual-active-bridge converter (DAB) because it has a direct effect on the output performance and volume of the circuit. In most studies, the output filter capacitor is considered ideal, and the parasitic effects and characteristics of commercial components are not seriously considered. Based on the detailed mathematical analysis of voltage ripple at steady state and overshoot and undershoot voltage at load transients with the output filter including parasitic effects, this paper provides a method for designing the practical output filter capacitor component to ensure acceptable output voltage quality for the DAB converter. Simulation of for a 10 kW converter prototype confirms the results.**

***Index Terms*—Dual active bridge converter, output filter design.**

I. Introduction

The dual-active-bridge converter (DAB) is one of the most popular converters for various applications, such as solid-state transformers, multiple-input converters, and other applications, because it has zero-voltage switching and wide voltage gain regulation, as well as bi-directional and symmetrical structure [1], [2], [3]. The output filter is especially important since it takes a direct effect on the performance and power density of DAB converter [2], [4]. However, in most DAB converter design, the output filter components are regarded as ideal, which makes the design results not so useful for choosing the commercial components. The high pulsating capacitor current of the DAB converter makes the output voltage very sensitive to the parasitic elements of the output filter capacitor. Therefore, the output voltage ripple equations in steady state and output voltage overshoot/undershoot in load transients should take into account the equivalent series resistance (ESR) and equivalent series inductance (ESL), which is not considered in the literature about the DAB converter design procedure [1], [5], [6], [7], [8], [2], [3]. Since the ESL in a capacitor is usually small, thus effect of ESL can be ignored in the analysis, but the ESR effects are difficult to be ignored.

In this study, an analysis of the output ripple of DAB is performed taking the ESR into consideration. The formula for critical dielectric loss tangent, the output voltage ripple, and the output voltage overshoot/undershoot are found, which can be used for choosing commercial capacitor product as the output filter while considering both the steady state and load transients.

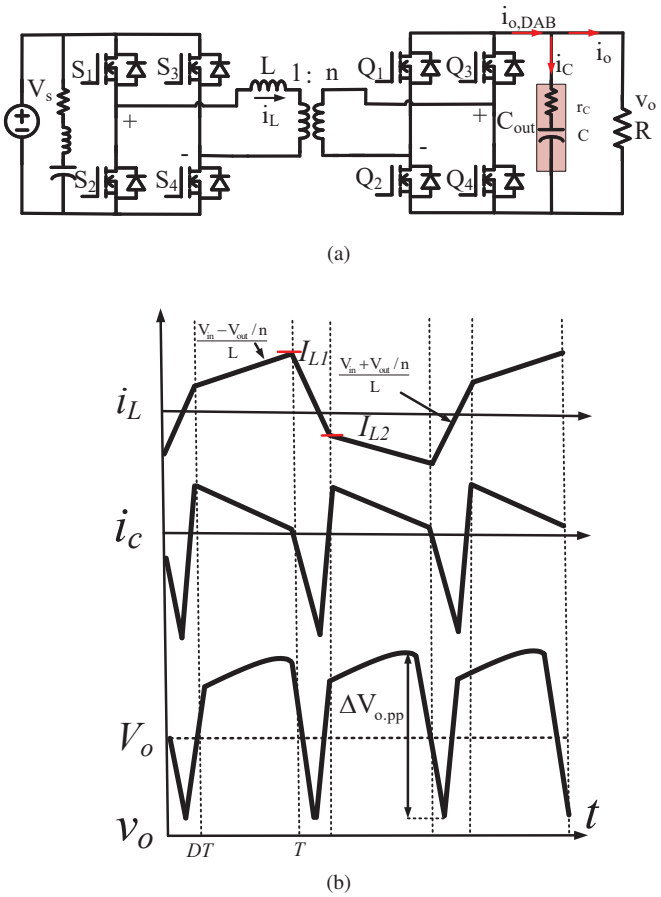

Fig. 1. (a) DAB converter (b) typical waveforms of DAB converter.

The remaining parts of this paper are organized as follows: the steady-state ripple analysis of the DAB converter is presented in Section II, the load transient analysis of the DAB converter is presented in Section III, the output filter design procedure is shown in Section IV, and Section V contains the simulation verification. The conclusion of the paper is summarized in Section VI.

II. Steady-State Ripple Analysis

Fig. 1(a) shows the DAB converter, including the r_C in output filter capacitor. The steady state waveform of DAB converter is shown in Fig. 1(b), the function of the inductor current i_L can be described by small ripple approximation as

$$i_L(t) = \begin{cases} \frac{(V_s+V_o/n)}{L}t - I_{L1} & 0 \le t \le DT \\ \frac{(V_s-V_o/n)}{L}(t-DT) + I_{L2} & DT \le t \le T \end{cases} \tag{1}$$

where V_o is the average output voltage. The inductor current function can be used to calculate the capacitor current function, and it can be provided by

$$i_c(t) = \begin{cases} \left(-\frac{(V_s+V_o/n)}{L}t + I_{L1}\right)\frac{1}{n} - I_o & 0 \le t \le DT \\ \left(\frac{(V_s-V_o/n)}{L}(t-DT) + I_{L2}\right)\frac{1}{n} - I_o & DT \le t \le T. \end{cases} \tag{2}$$

This allows us to express the output voltage function as

$$v_o(t) = \begin{cases} r_C i_c + v_c(0) + \frac{1}{C}\int_0^t i_c(\tau)\,d\tau & 0 \le t \le DT \\ r_C i_c + v_c(DT) + \frac{1}{C}\int_{DT}^t i_c(\tau)\,d\tau & DT \le t \le T. \end{cases} \tag{3}$$

By calculating the derivative of the output voltage with respect to time

$$\frac{\partial v_o(t)}{\partial t} = 0, \tag{4}$$

we can determine when the voltage is at its highest and lowest value. The two instants of time are shown:

$$t = \begin{cases} \tau_1 - C \cdot r_C & 0 \le t \le DT \\ \tau_2 - C \cdot r_C & DT \le t \le T \end{cases} \tag{5}$$

where

$$\begin{aligned} \tau_1 &= \frac{I_{L1} - nI_o}{V_s + V_o/n}L \\ \tau_2 &= DT + \frac{nI_o - I_{L2}}{V_s - V_o/n}L. \end{aligned} \tag{6}$$

Therefore, by substituting (5) and (6) to (3). The formula for the highest and lowest output voltages can be obtained by

$$\begin{cases} v_{o\_\min} = V_o + \frac{V_s+V_o/n}{2Ln}\left(C \cdot r_C^2\right) - \frac{\Delta v_c}{2} & 0 \le t \le DT \\ v_{o\_\max} = V_o + \frac{V_s-V_o/n}{2Ln}\left(C \cdot r_C^2\right) + \frac{\Delta v_c}{2} & DT \le t \le T \end{cases} \tag{7}$$

where

$$\begin{aligned} \Delta v_c &= \frac{1}{C}\int_{\tau_1}^{\tau_2} i_c(\tau)d\tau \\ &= \frac{1}{C}\left(\int_{\tau_1}^{DT} i_c(\tau)d\tau + \int_{DT}^{\tau_2} i_c(\tau)d\tau\right) \\ &= \frac{K}{C} \end{aligned} \tag{8}$$

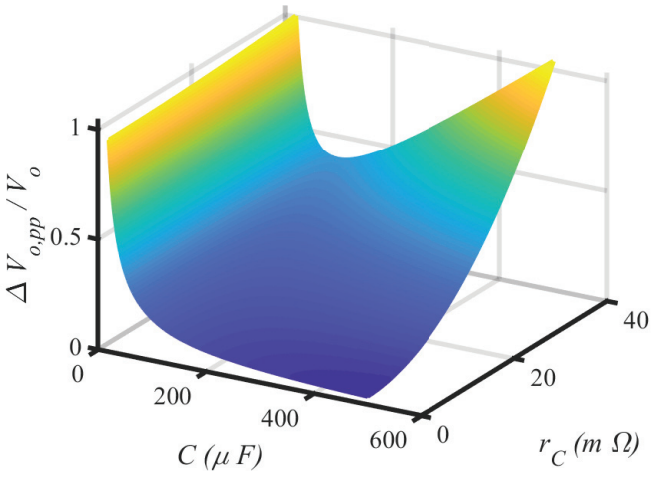

Fig. 2. 3D plot the normalized peak-to-peak output voltage as a function of r_C and C of the output filter capacitor.

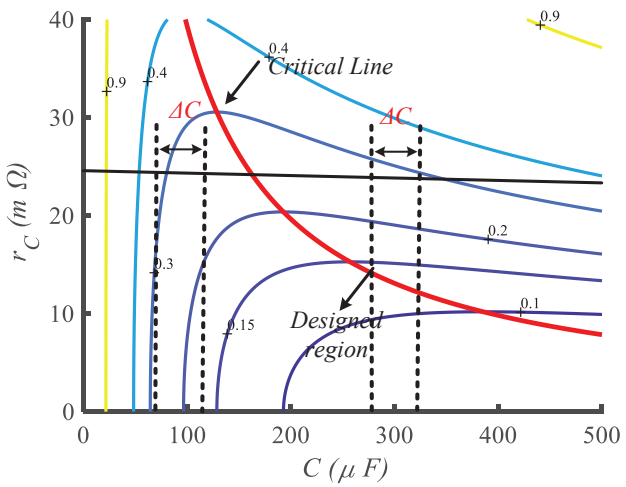

Fig. 3. Critical capacitance curve.

and K is given by (10). Finally, the peak-to-peak output voltage in steady-state is derived as follows.

$$\begin{aligned} \Delta V_{o,SS} &= v_{o\_\max} - v_{o\_\min} \\ &= \frac{V_o}{Ln^2}\left(C \cdot r_C^2\right) + \frac{K}{C} \end{aligned} \tag{9}$$

According to the analysis, Fig. 2 shows the normalized output peak-to-peak voltage versus r_C and capacitance of the output filter. This demonstrates that with a smaller r_C and a larger C, the peak-to-peak value of the output voltage can be reduced. The critical capacitance value can be determined by taking the partial derivative of the peak-to-peak voltage with respect to the capacitance

$$\frac{\partial \Delta V_{o,SS}(t)}{\partial C} = 0 \tag{11}$$

$$K = \left(\left(-\left(V_s + V_o/n\right)\left(DT - \tau_1\right)^2 + \left(V_s - V_o/n\right)\left(\tau_2 - DT\right)\left(\tau_2 - 3DT\right) \right) \frac{1}{2nL} + \left(\frac{I_{L1}+I_{L2}}{n} - I_o \right)\left(\tau_2 - \tau_1\right) \right) \tag{10}$$

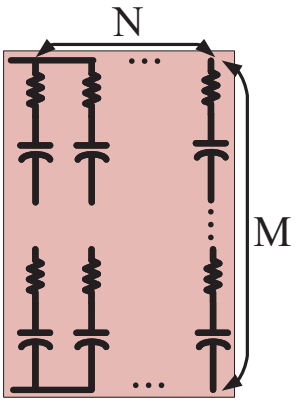

Fig. 4. N by M capacitor bank.

and thus the critical capacitance can be expressed by

$$C_{critical} = \frac{n}{r_C}\sqrt{\frac{KL}{V_o}}. \tag{12}$$

Because the increment in capacitance can significantly reduces the output voltage ripple in the region when the capacitance is smaller than the critical value as illustrated in Fig. 3, it is recommended that the design region should be placed to the left of the critical line. Recalling that the dielectric loss tangent of the capacitor $\tan\delta = 2\pi f_s C \cdot r_C$, the critical dielectric loss tangent of material can be determined by

$$\tan\delta_{critical} = 2\pi n f_s \sqrt{\frac{KL}{V_o}}. \tag{13}$$

This formula can be used to choose the dielectric material of the capacitor.

To further reduce r_C and increase capacitance, the capacitor is usually connected in parallel. The impedance of a capacitor bank in a system with N identical capacitors in parallel and M in series, as shown in Fig. 4, is shown as follows.

$$Z_{cap}(f_s) = \frac{M}{N}\left(r_C - j\frac{1}{2\pi f_s C}\right). \tag{14}$$

It should be noted that the critical dielectric loss tangent does not change even in this case.

III. Load Transients Analysis

Voltage regulation is necessary even for load transient condition. In DAB converter, controller bandwidth and the output filter capacitor are two crucial factor in suppressing overshoot/undershoot for load transients condition with a load step change. Using the simplified DAB converter illustrated in Fig. 5, the pulse step source current $I_{o,DAB}$ is not instantly reacting to the load step change due to the limited bandwidth of the controller. Therefore, the output voltage is mainly

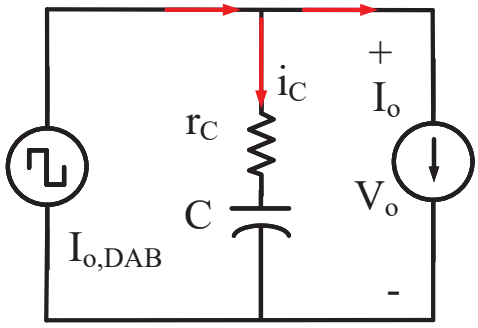

Fig. 5. A simplified DAB converter.

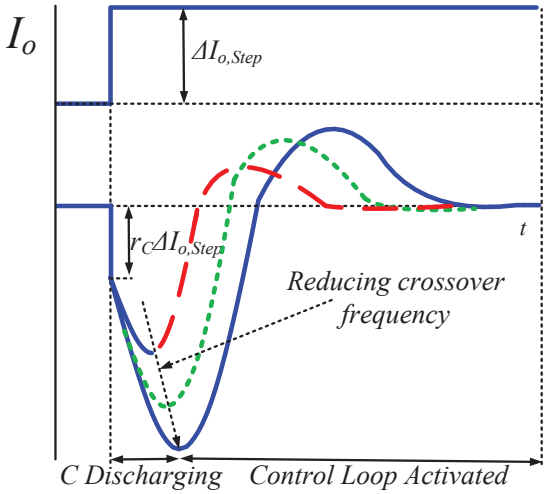

Fig. 6. Output voltage and current transient.

affected by the capacitor's r_C and C of capacitor filter to cope to the instant load current change. The first droop voltage is caused by the capacitor's r_C, whereas the second one is caused by pure capacitive contribution. According to Fig. 6, Since the controller's crossover frequency f_c determines the discharging time of capacitor, a higher f_c results in a smaller undershoot voltage [9].

For accounting for the effects of such characteristics, the DAB converter's open loop output impedance is taken into account and approximated as follows

$$Z_o(s) \approx r_C + \frac{1}{sC}. \tag{15}$$

Where the impedance of the $I_{o,DAB}$ is regarded as infinite. Open loop output impedance magnitude can be plotted as shown in Fig. 7 and the closed-loop output impedance is given by

$$Z_{o,CL}(s) = \frac{Z_o(s)}{1 + T(s)}. \tag{16}$$

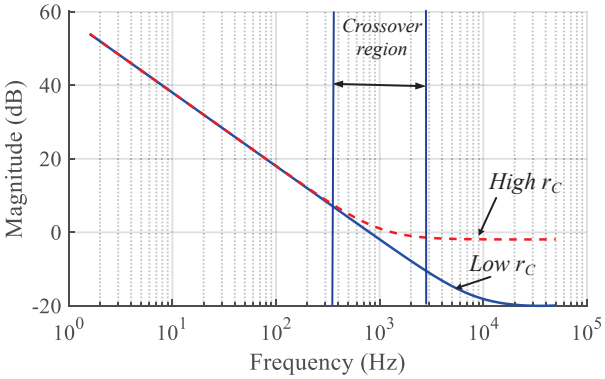

Fig. 7. Open loop converter output impedance amplitude.

Following the small signal modeling of DAB converter in [10], [11], loop gain $T(s)$ is stated as

$$T(s) = G_c(s) G_{i\theta} Z_o(s) \tag{17}$$

where

$$G_c(s) = K_p + \frac{K_i}{s} \tag{18}$$

$$G_{i\theta} = \frac{nV_s}{2\pi f_s L}\left(1 - \frac{2\theta}{\pi}\right) \tag{19}$$

where $G_c(s)$ is proportional-integral (PI) controller transfer function and $G_{i\theta}$ is phase angle to the output current function. By substituting (17) into (16), the closed-loop output impedance is expressed as

$$Z_{o,CL}(s) = \frac{r_C + \frac{1}{sC}}{1 + \left(K_p + \frac{K_i}{s}\right) G_{i\theta}\left(r_C + \frac{1}{sC}\right)} \tag{20}$$

$$= Z_f || R_e || sL_e \tag{21}$$

where

$$Z_f = r_C + \frac{1}{sC} \tag{22}$$

$$R_e = \frac{1}{K_p G_{i\theta}} \tag{23}$$

$$L_e = \frac{1}{K_i G_{i\theta}} \tag{24}$$

Therefore, the simplified DAB converter in closed-loop is shown in Fig. (8). The transient response of the output voltage as a result of the step load change $\Delta I_{o,Step}$ is given as

$$\Delta v_o(t) = \mathcal{L}^{-1}\left(\frac{\Delta I_{o,step}}{s} Z_f || R_e || sL_e\right). \tag{25}$$

The result of output voltage with the function of the time is given by (26). Therefore, the first droop voltage in closed-loop ($t = 0$) can be calculated by

$$\Delta v_o(0) = \Delta \mathrm{I}_{\mathrm{o,step}} R_e || r_C, \tag{27}$$

by adding the term R_e in the output impedance, the first droop voltage in the closed loop is reduced compared to the open loop.

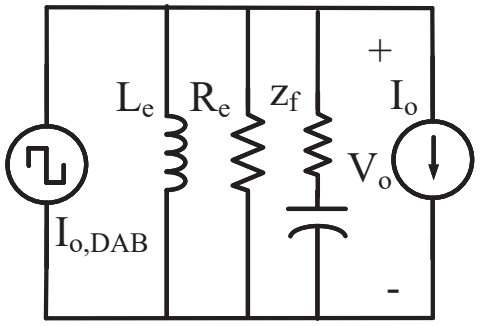

Fig. 8. A simplified DAB converter in closed-loop with PI controller.

In second droop voltage, the influence of r_C can be omitted, with $r_C = 0$, so (26) can be simplified as

$$\Delta v_o(t) = \frac{2\Delta \mathrm{I}_{\mathrm{o,step}} \mathrm{R_e} \mathrm{e}^{-\alpha t} \sinh\left(t\sqrt{\alpha^2 - \left(\frac{\alpha}{\varsigma}\right)^2}\right)}{\sqrt{1 - \frac{1}{\varsigma^2}}} \tag{28}$$

$$\alpha = \frac{1}{2R_e C} \tag{29}$$

$$\zeta = \frac{1}{2R_e}\sqrt{\frac{L_e}{C}} \tag{30}$$

where α and ζ are attenuation and damping factor, respectively. Taking partial derivative of the output voltage respect to time

$$\frac{\partial \Delta v_o(t)}{\partial t} = \frac{\Delta \mathrm{I}_{\mathrm{step}} \mathrm{e}^{-\alpha t}}{\mathrm{C}}\left(\cosh\left(t\sqrt{\alpha^2 - \left(\frac{\alpha}{\varsigma}\right)^2}\right) - \frac{\sinh\left(t\sqrt{\alpha^2 - \left(\frac{\alpha}{\varsigma}\right)^2}\right)}{\sqrt{1 - \frac{1}{\varsigma^2}}}\right) \tag{31}$$

and setting the derivative equal to zero yield

$$\tanh\left(t\sqrt{\alpha^2 - \left(\frac{\alpha}{\varsigma}\right)^2}\right) = \sqrt{1 - \frac{1}{\varsigma^2}}. \tag{32}$$

The time instant of maximum overshoot voltage is thus given by

$$t_{Step} = \frac{1}{2\sqrt{\alpha^2 - \left(\frac{\alpha}{\varsigma}\right)^2}} \ln\left(\frac{1 + \sqrt{1 - \frac{1}{\varsigma^2}}}{1 - \sqrt{1 - \frac{1}{\varsigma^2}}}\right). \tag{33}$$

Substituting (33) to (28), the second droop voltage can be expressed as

$$\Delta v_o(t_{Step}) = \frac{2\Delta \mathrm{I}_{\mathrm{o,step}} \mathrm{R_e}\left(\frac{1+\sqrt{1-\frac{1}{\varsigma^2}}}{1-\sqrt{1-\frac{1}{\varsigma^2}}}\right)^{-\frac{1}{2\sqrt{1-\frac{1}{\varsigma^2}}}} \sinh\left(\frac{1}{2}\ln\left(\frac{1+\sqrt{1-\frac{1}{\varsigma^2}}}{1-\sqrt{1-\frac{1}{\varsigma^2}}}\right)\right)}{\sqrt{1-\frac{1}{\varsigma^2}}} \tag{34}$$

The total undershoot voltage is equal to the sum of the first droop voltage and the second droop voltage and it is given by

$$\Delta V_{o,Step} = \Delta v_o(0) + \Delta v_o(t_{Step}). \tag{35}$$

$$\Delta v_o(t) = \frac{\mathrm{I_{o,step}R_e r_C e}^{-\frac{(\mathrm{L_e}+C\mathrm{R_e r_C})}{2C\mathrm{L_e}(\mathrm{R_e}+\mathrm{r_C})}t}\left(\begin{array}{l}\cosh\left(\frac{t\sqrt{C^2\mathrm{R_e}^2\mathrm{r_C}^2-4C\mathrm{L_eR_e}^2-2C\mathrm{L_eR_e r_C}+\mathrm{L_e}^2}}{2C\mathrm{L_e}(\mathrm{R_e}+\mathrm{r_C})}\right) \\ +\frac{\sinh\left(\frac{t\sqrt{C^2\mathrm{R_e}^2\mathrm{r_C}^2-4C\mathrm{L_eR_e}^2-2C\mathrm{L_eR_e r_C}+\mathrm{L_e}^2}}{2C\mathrm{L_e}(\mathrm{R_e}+\mathrm{r_C})}\right)\left(-C\mathrm{R_e r_C}^2+\mathrm{L_e r_C}+2\mathrm{L_eR_e}\right)}{\mathrm{r_C}\sqrt{C^2\mathrm{R_e}^2\mathrm{r_C}^2-4C\mathrm{L_eR_e}^2-2C\mathrm{L_eR_e r_C}+\mathrm{L_e}^2}}\end{array}\right)}{\mathrm{R_e}+\mathrm{r_C}} \tag{26}$$

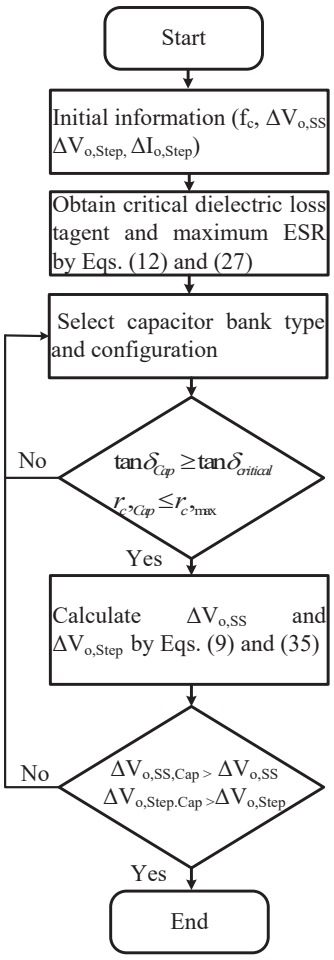

Fig. 9. Output filter design procedure.

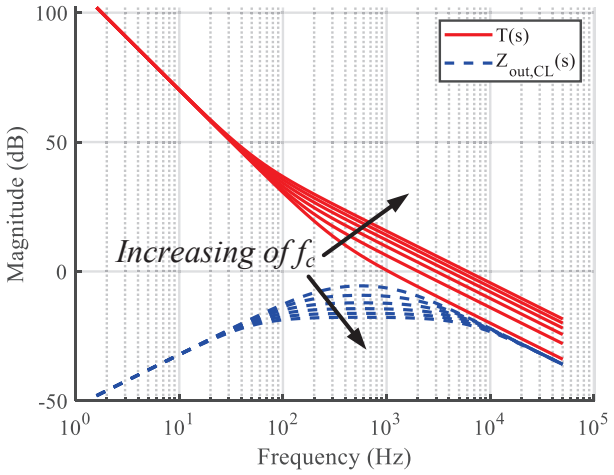

Fig. 10. Magnitude of converter loop gain and closed-loop output impedance.

TABLE I
THE SYSTEM PARAMETERS

Symbol	Parameters	Values	Unit
V_s	Input voltage	400	V
V_o	Output voltage	800	V
$\Delta V_{o,SS}/V_o$	Maximum output voltage ripple at steady-state	0.1	%
$\Delta V_{o,Step}/V_{out}$	Maximum overshoot/undershoot at load-transient	1	%
n	Transformer ratio	1:2	
L	Auxiliary inductor	20	μH
f_s	Switching frequency	50	kHz
$\Delta I_{o,Step}$	Step change of load current	11	A

IV. Output Filter Design Procedure

According to the discussion in Sections II and III, the method of designing the output filter with the allowable output voltage ripple at steady state and the acceptable overshoot/undershoot voltage at load transients can be summarized as follows. First, (12) and (27) can be used to determine the critical dielectric loss tangent and the maximum r_C of a capacitor. This information can be used to select both the output filter capacitor component and its series and parallel the configuration. Once the type, configuration, and capacitance of the output capacitor are selected, (9) and (35) can be used to determine the voltage ripple in steady state and the overshoot/undershoot voltage at load transients. These values are compared to the maximum permissible value. If they do not meet the original requirement, the capacitance must be increased to meet the requirement. Finally, the information from the capacitor's datasheet can be used to verify the calculation through simulation. Fig. 9 shows a summary of the output filter design procedure.

V. Simulation Verification

To validate the analysis, a simulation is performed. The system parameters are listed in the Table I. The maximum

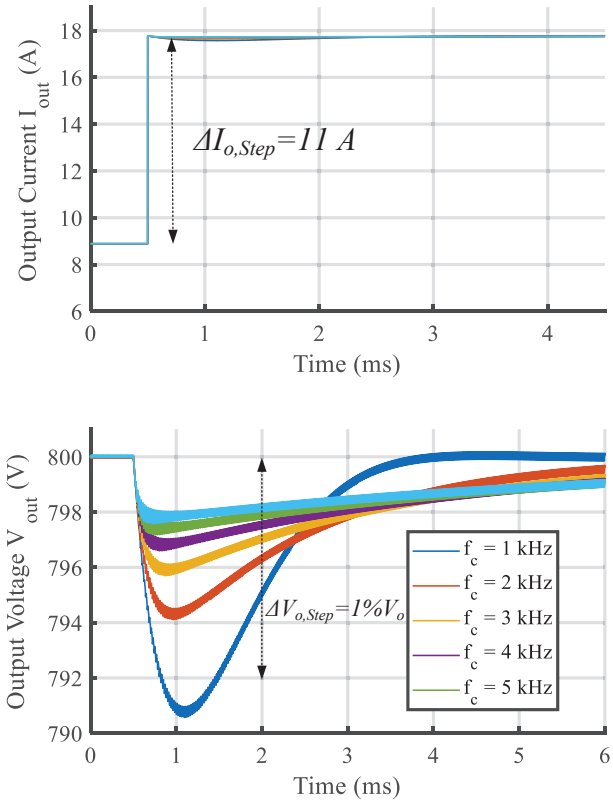

Fig. 11. Simulation results of load step-up condition with different crossover frequency f_c.

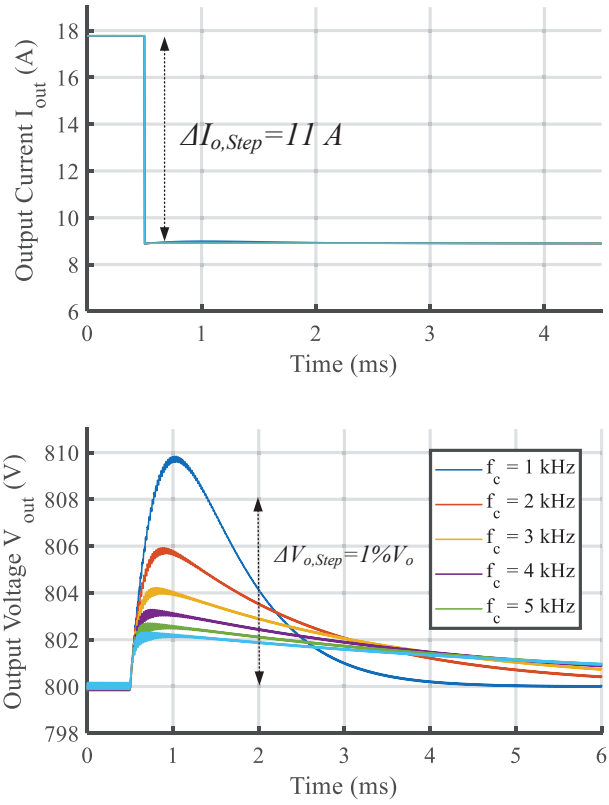

Fig. 12. Simulation results of load step-down condition with different crossover frequency f_c.

allowable peak-to-peak output voltage ripple at steady state is 0.1 % of the output voltage, and the critical dielectric loss tangent can be calculated to be 0.85 using (13). To achieve 1 % overshoot/undershoot of the output voltage at load transient $\Delta I_{o,Step} = 11\ A$, aluminum electrolytic capacitor from Nichicon (LGW) series with a high current ripple current capability with dielectric loss tangent of 0.15 can be selected. 2 by 2 capacitor bank structure (M=N=2) each with $C = 200\ \mu F$, $r_C = 1.5\ m\Omega$ are used. (35) can be used to calculate the voltage ripple $\Delta V_{o,Step}$, since the crossover calculation result should be greater than 1 kHz to satisfy the output ripple voltage requirement. The loop gain $T(s)$ and the output impedance of the closed loop at a crossover frequency of 1 kHz to 5 kHz are shown in Fig. 10, which shows that the amplitude of the closed-loop output impedance decreases as the crossover frequency f_c increases. The steady-state ripple voltage is 0.5 % of the output voltage, and the overshoot/undershoot voltages are less than 1 % of the output voltage for $f_c > 1\ kHz$ at both step-up and step-down loads, as shown in Figs. 11 and 12, which satisfies the requirements. Fig. 13 shows the comparison of calculation and simulation results with different crossover frequencies. It can be seen that the simulation results agree well with the calculation results.

VI. Conclusion

In this work, the influence of the parasitic effect of the output filter capacitor on the output voltage of the DAB converter was analyzed. The value of the capacitor and dielectric material can be determined using the peak-to-peak ripple of the output voltage and the critical dielectric loss tangent. The required capacitance value of the output capacitor for load transients with given overshoot/undershoot voltage is also presented, which depends on the crossover frequency of the regulator. A simulation is performed to verify the analysis and it agrees well with the analysis.

ACKNOWLEDGEMENT

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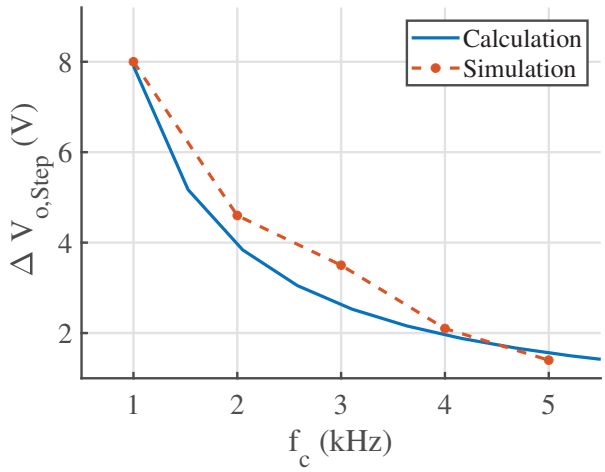

Fig. 13. Comparison between simulation and calculation results of undershoot/overshoot voltage $\Delta V_{o,Step}$ with different crossover frequency f_c.

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