

An Accurate and Fast Model of Three-Level Three-Phase Dual-Active Bridge Converters in Real-Time Simulation

Ming Jia, Philipp Joeßges, Rik W. De Doncker
Institute for Power Generation and Storage Systems
E.ON Energy Research Center
RWTH Aachen University
Mathieustrasse 10, 52074
Aachen, Germany
Email: post_pgs@eonerc.rwth-aachen.de

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Keywords

«Dual Active Bridge (DAB)», «Modelling», «Real-time simulation», «Stability analysis»

Abstract

This paper proposes a C-code average model for an efficient real-time simulation of a three-level three-phase dual-active bridge (DAB) dc-dc converter. To evaluate the model and the control algorithms, the simulations and control hardware-in-the-loop emulators are used, for example, testing a 5000 V dc-link DAB converter with up to 30-degree phase shift between the primary and secondary sides of a transformer. From the results of the hardware-in-the-loop test, it can be concluded that the model proposed in this work is numerically stable and is executed considerably faster than the state-of-the-art proposed auto-generated models.

Introduction

Reliable power electronic systems with dynamic behavior combined with shorter development cycles are increasingly demanded. This necessitates the development of a flexible evaluation tool for the control algorithm. Hence, a platform is needed for its execution, particularly to access its behavior under fault situations. In control-hardware-in-the-loop (CHIL) scenarios, a physical controller is connected to a virtual plant in a real-time (RT) simulator instead of a physical plant [1]. Performing offline simulations requires results as accurate as possible. A variable-step solver is often implemented, so that the step size is decreased when the states of the model change rapidly, whereas the step size increases when the model changes slowly. Ultimately, the accuracy of the simulation results is determined solely by the computational power and the mathematical model of the system. In a real-time simulation environment, however, discrete execution typically has a fixed step size. The accuracy of the results and the time required to simulate the system decreases as the step size increases. Consequently, the accuracy of the computations is also determined by the step time used to produce the results.

Average models are already implemented as basic circuit units in the software PLECS. However, the generated code is extensive and complex, and the execution time of this model in the RT simulator is not optimized. Furthermore, these average models are not investigated for dc-dc converters. [2] proposed a self-developed C-code model for a two-level converter. It considered a half-bridge consisting of two

Insulated Gate Bipolar Transistor (IGBT) modules as the modeling unit. The results demonstrated that the C-code model is more efficient and has a similar level of accuracy as the auto-generated models. In this work, a self-developed C-code-based average model for a three-level three-phase dual-active bridge dc-dc converter (3L-DAB3) is further investigated. The model uses neutral-point clamped half-bridge as the modeling unit to simulate the converter. The following sections focus on the calculation of these switching signals.

Another improvement in this work is that both the simplified transformer model and the three single-phase models are implemented. In [2], only the simplified transformer model is investigated. Incorporating a three single-phase transformer into the model significantly enhances the precision of the proposed model. Both models are compared with the corresponding PLECS model to validate the accuracy and operating speed in the RT simulator. The implementation of self-defined C-code model reduces the size of the model description and expedites the calculation and execution of the RT simulation. The efficiency of the RT simulation is improved, and the numerical stability is investigated.

C-Code Average Model of a 3L-DAB3

Modeling Methodology

The PLECS average model of a half-bridge consists of controlled current and voltage sources and a pair of diodes. It is able to process switching gate signals in decimal format. Fig. 1 exemplifies a commutation from the bottom switch to the top switch of one phase-leg. The red lines S_{top} and S_{bot} indicate the actual upper and lower gate signals of the switch model. In a fixed time-step simulation, it is impossible to capture the precise moment at which the current changes direction during a sampling period. The current values are updated only at the beginning of each time step T . The blue lines with shaded areas \bar{S}_{top} and \bar{S}_{bot} show the averaged gate signals over a time step with dead time.

The RT simulator AixControl XRS7070 consists of a Field Programmable Gate Arrays (FPGA) and a Digital Signal Processor (DSP), thus combining the speed of sampling the switching signals in an FPGA with the flexibility and computational capability of a DSP. Fig. 2 presents the whole PWM processing. The FPGA receives the PWM signals from the external control module simultaneously, which is either 0 or 1. The FPGA samples the continuous PWM signals every 20 ns and then passes the average value over a 10 μ s time step to the DSP for calculation. After that the FPGA samples the signals, the PWM signals are real numbers within the range [0,1] instead of 0 and 1.

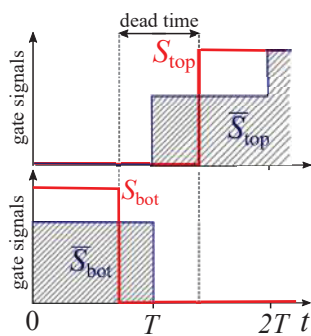


Fig. 1: A switching state of one phase-leg

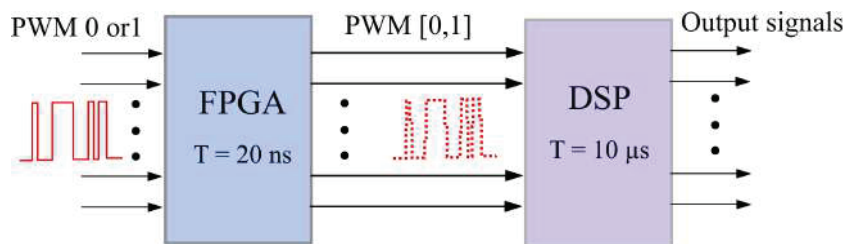


Fig. 2: PWM signals in an RT simulator

Modeling for 3L-DAB3

A 3L-DAB3 consists of two three-level neutral-point-clamped (NPC) converters with a transformer as the ac link [3][4]. A mathematical model for the 3L-DAB3 is derived from the half-bridge model introduced in [5]. The parameter k_{xp} is introduced to represent the direction of the current in the average model. It is either one for a positive ac currents or zero for a negative ac current. Fig. 4 depicts the calculation procedure of the C-code average model. The parameter $x \in \{a, b, c\}$ represents the phase-leg a , b and

c. The calculation begins with the capacitor voltages and the phase currents. With the knowledge of gate signals and phase current directions, the phase voltages and arm currents can be obtained. The capacitor voltages and phase currents in the subsequent time step can be determined by integrating the phase voltages and arm currents.

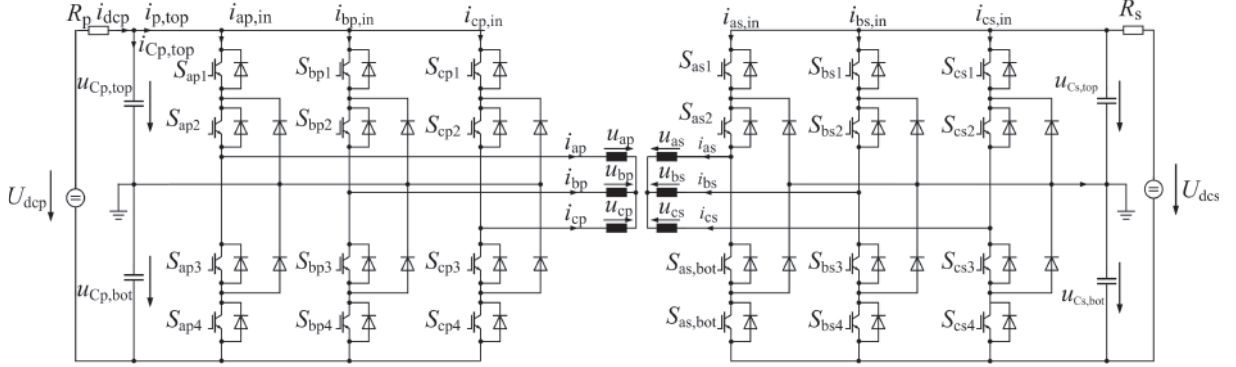


Fig. 3: Circuit diagram of a 3L-DAB3 converter

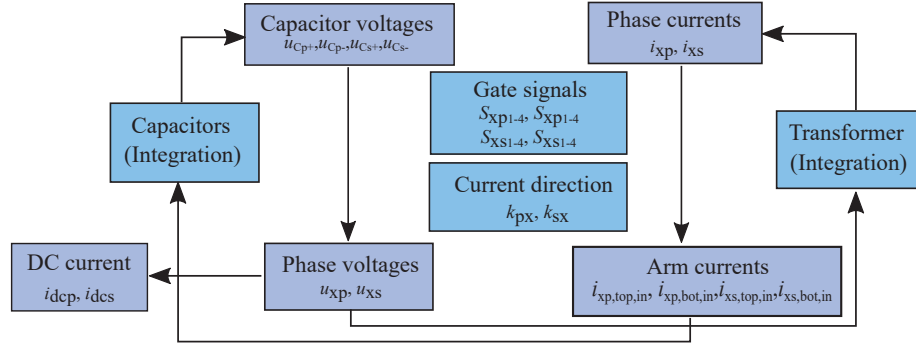


Fig. 4: Flowchart of the C-code realization for a 3L-DAB3 converter

The ac voltages at the primary side can be expressed as

$$\begin{aligned} u_{xp} &= [\min(\bar{S}_{xp1}, \bar{S}_{xp2}) \cdot u_{Cp,top} - (1 - \bar{S}_{xp2}) \cdot u_{Cp,bot}] \cdot k_{xp} \\ &\quad - [(1 - \bar{S}_{xp3}) \cdot u_{Cp,top} - \min(\bar{S}_{xp3}, \bar{S}_{xp4}) \cdot u_{Cp,bot}] \cdot (1 - k_{xp}) \\ &= \bar{S}_{uxp,top} \cdot u_{Cp,top} + \bar{S}_{uxp,bot} \cdot u_{Cp,bot}. \end{aligned} \quad (1)$$

In the voltage calculation, the parameters $\bar{S}_{uxp,top}$ and $\bar{S}_{uxp,bot}$ represent the averaged switching signals for the top and bottom switches, respectively, in one phase-leg of the primary side. They can be calculated as follows:

$$\bar{S}_{uxp,top} = \min(\bar{S}_{xp1}, \bar{S}_{xp2}) \cdot k_{xp} - (1 - \bar{S}_{xp3})(1 - k_{xp}) \quad (2)$$

$$\bar{S}_{uxp,bot} = (1 - \bar{S}_{xp2}) \cdot k_{xp} - \min(\bar{S}_{xp3}, \bar{S}_{xp4}) \cdot (1 - k_{xp}). \quad (3)$$

The switching signals $\bar{S}_{uxp,top}$ and $\bar{S}_{uxp,bot}$, which are expressed in an abc reference frame, are implemented in the model. However, for the evaluation of the stability of the model, a transformation to the $\alpha\beta$ reference frame is required to decouple the variables. The corresponding transformed switching signals can be derived as:

$$\bar{S}_{u\alpha p,top} = \bar{S}_{ap,top} - 0.5 \cdot \bar{S}_{bp,top} - 0.5 \cdot \bar{S}_{cp,top} \quad (4)$$

$$\bar{S}_{u\beta p,top} = \bar{S}_{bp,top} - 0.5 \cdot \bar{S}_{cp,top}. \quad (5)$$

The expression is likewise applicable to the bottom switches. The current flowing through the phase-leg

at the primary side of the converter can be expressed as

$$i_{xp,in,top} = [\min(\bar{S}_{xp1}, \bar{S}_{xp2}) \cdot k_{xp} + (1 - k_{xp}) \cdot (1 - \bar{S}_{xp3})] \cdot i_{xp} = \bar{S}_{ixp,top} \cdot i_{xp} \quad (6)$$

$$i_{xp,in,bot} = [(1 - \bar{S}_{xp3}) \cdot k_{xp} + (1 - k_{xp}) \cdot \min(\bar{S}_{xp1}, \bar{S}_{xp2})] \cdot i_{xp} = \bar{S}_{ixp,bot} \cdot i_{xp}. \quad (7)$$

The parameters $\bar{S}_{ixp,top}$ and $\bar{S}_{ixp,bot}$ represent the average switching signals for the top and bottom switches in one phase-leg of the primary side in the current calculation.

$$\bar{S}_{ixp,top} = \min(\bar{S}_{xp1}, \bar{S}_{xp2}) \cdot k_{ixp} - (1 - \bar{S}_{xp3})(1 - k_{ixp}) \quad (8)$$

$$\bar{S}_{ixp,bot} = \min(\bar{S}_{xp1}, \bar{S}_{xp2})(1 - k_{ixp}) - (1 - \bar{S}_{xp3}) \cdot k_{ixp} \quad (9)$$

They can be transformed in the $\alpha\beta$ frame as follows:

$$\bar{S}_{i\alpha p,top} = \bar{S}_{iap,top} - 0.5 \cdot \bar{S}_{ibp,top} - 0.5 \cdot \bar{S}_{icp,top} \quad (10)$$

$$\bar{S}_{i\beta p,top} = \bar{S}_{ibp,top} - 0.5 \cdot \bar{S}_{icp,top}. \quad (11)$$

Simplified Transformer with Infinite Mutual Inductance

The power transfer in the 3L-DAB3 converter is determined by the voltages across the leakage inductance of the transformer. Thus, the transformer is simplified as series-connected inductors between the primary and secondary sides. The main inductances between the primary and secondary sides are omitted, as shown in Fig. 5. The transformer is converted to the primary side with the total leakage inductance $L_{x\sigma} = L_{xh} + L'_{xh}$, where L_{xh} is the leakage inductance of the primary side and L'_{xh} is the normalized leakage inductance of the secondary side. This is analogous for the copper resistance $R_{xw} = R_{xs} + R'_{xs}$. To simplify, the total leakage inductances and copper resistances of three phases are identical to be L_σ and R_w . The following equation can be derived for the α component of the phase current.

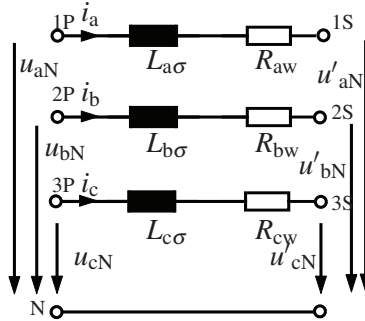


Fig. 5: Equivalent circuit of a simplified three-phase transformer

$$\begin{aligned} L_\sigma \cdot \frac{di_\alpha}{dt} &= u_{\alpha p} - N \cdot u_{\alpha s} - R_w \cdot i_\alpha \\ \Leftrightarrow \frac{di_\alpha}{dt} &= \frac{\bar{S}_{u\alpha p,top}}{L_\sigma} \cdot u_{Cp,top} + \frac{\bar{S}_{u\alpha p,bot}}{L_\sigma} \cdot u_{Cp,bot} \\ &\quad - N \cdot \frac{\bar{S}_{u\alpha s,top}}{L_\sigma} \cdot u_{Cs,top} - N \cdot \frac{\bar{S}_{u\alpha s,bot}}{L_\sigma} \cdot u_{Cs,bot} - \frac{R_w}{L_\sigma} \cdot i_\alpha \end{aligned} \quad (12)$$

It can be derived analogously for the β component of the phase current.

$$\frac{di_\beta}{dt} = \frac{\bar{S}_{u\beta p,top}}{L_\sigma} \cdot u_{Cp,top} + \frac{\bar{S}_{u\beta p,bot}}{L_\sigma} \cdot u_{Cp,bot} - N \cdot \frac{\bar{S}_{u\beta s,top}}{L_\sigma} \cdot u_{Cs,top} - N \cdot \frac{\bar{S}_{u\beta s,bot}}{L_\sigma} \cdot u_{Cs,bot} - \frac{R_w}{L_\sigma} \cdot i_\beta \quad (13)$$

Three Single-Phase Transformers in Y-Y Connection

To include the influence of both the main inductances L_{xh} and the leakage inductances L_{xs} , three single-phase transformers in Y-Y connection is built, as shown in Fig. 6.

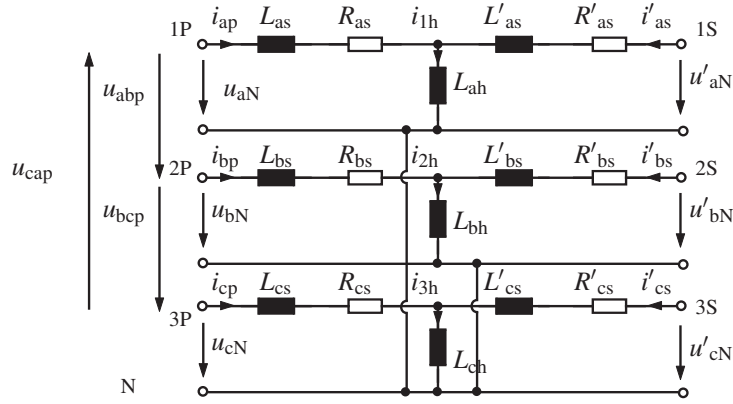


Fig. 6: Equivalent circuit of three single-phase transformers in Y-Y connection

By applying Kirchhoff's voltage law (KVL) to the primary side of the equivalent circuit, the following equations can be derived in the abc reference frame.

$$\begin{aligned} & \bar{S}_{uap,top} \cdot u_{Cp,top} + \bar{S}_{uap,bot} \cdot u_{Cp,bot} - N \cdot \bar{S}_{ubs,top} \cdot u_{Cs,top} + N \cdot \bar{S}_{ubs,bot} \cdot u_{Cs,bot} \\ & = i_{ap} \cdot R_{as} + (L_{as} + L_{ah}) \cdot \frac{di_{ap}}{dt} + L_{ah} \cdot \frac{di'_{as}}{dt} - i_{bp} \cdot R_{bs} - (L_{bs} + L_{bh}) \cdot \frac{di_{bp}}{dt} - L_{bh} \cdot \frac{di'_{bs}}{dt} \end{aligned} \quad (14)$$

$$\begin{aligned} & \bar{S}_{ubp,top} \cdot u_{Cp,top} + \bar{S}_{ubp,bot} \cdot u_{Cp,bot} - N \cdot \bar{S}_{ucs,top} \cdot u_{Cs,top} + N \cdot \bar{S}_{ucs,bot} \cdot u_{Cs,bot} \\ & = i_{bp} \cdot R_{bs} + (L_{bs} + L_{ah}) \cdot \frac{di_{ap}}{dt} + L_{ah} \cdot \frac{di'_{as}}{dt} - i_{bp} \cdot R_{as} - (L_{bs} + L_{bh}) \cdot \frac{di_{bp}}{dt} - L_{bh} \cdot \frac{di'_{bs}}{dt} \end{aligned} \quad (15)$$

The parameter N represents the turn ratio of the transformer. The parameters R_{xp} and i_{xp} represent the parasitic resistances and the currents at the primary side of the transformer, respectively. The parameters R_{xs} and i_{xs} are correspondingly the variables at the secondary side. By applying Kirchhoff's circuit law (KCL) to the primary side of the equivalent circuit, the following equation can be derived.

$$0 = \frac{di_{ap}}{dt} + \frac{di_{bp}}{dt} + \frac{di_{cp}}{dt} \quad (16)$$

DC-Link Capacitor

According to Kirchhoff's voltage law (KVL), the current on the top side $i_{Cp,top}$ can be expressed by the dc current i_{dcp} and the sum of the half-bridge currents $i_{p,top}$ as,

$$i_{Cp,top} = C_p \cdot \frac{du_{Cp,top}}{dt} = i_{dcp} - i_{p,top}. \quad (17)$$

The expressions for i_{dcp} and $i_{p,top}$ in (17) are as follows:

$$i_{dcp} = \frac{U_{dcp} - u_{Cp,top} - u_{Cp,bot}}{R_p} \quad (18)$$

$$i_{p,top} = i_{\alpha p} \cdot \bar{S}_{i\alpha p,top} + i_{\beta p} \cdot \bar{S}_{i\beta p,top} \quad (19)$$

with $i_{\alpha p}$ and $i_{\beta p}$ equal to i_{α} and i_{β} . Substituting (18) and (19) into (17) results in

$$\begin{aligned}\frac{du_{Cp,top}}{dt} &= -\frac{1}{C_{p1} \cdot R_p} \cdot (U_{dcp} - u_{Cp,top} - u_{Cp,bot}) - \frac{1}{C_{p1}} \cdot (i_{ap} \cdot \bar{S}_{iap,top} + i_{bp} \cdot \bar{S}_{ibp,top} + i_{cp} \cdot \bar{S}_{icp,top}) \\ &= -\frac{1}{C_{p1} \cdot R_p} \cdot u_{Cp,top} - \frac{1}{C_{p1} \cdot R_p} \cdot u_{Cp,bot} \\ &\quad - \frac{1}{C_{p1}} \cdot \bar{S}_{iap,top} \cdot i_{\alpha} - \frac{1}{C_{p1}} \cdot \bar{S}_{ibp,top} \cdot i_{\beta} + \frac{1}{C_{p1} \cdot R_p} \cdot U_{dcp}\end{aligned}\quad (20)$$

$$\begin{aligned}\frac{du_{Cp,bot}}{dt} &= -\frac{1}{C_{p2} \cdot R_p} \cdot (U_{dcp} - u_{Cp,top} - u_{Cp,bot}) - \frac{1}{C_{p2}} \cdot (i_{ap} \cdot \bar{S}_{iap,bot} + i_{bp} \cdot \bar{S}_{ibp,bot} + i_{cp} \cdot \bar{S}_{icp,bot}) \\ &= -\frac{1}{C_{p2} \cdot R_p} \cdot u_{Cp,top} - \frac{1}{C_{p2} \cdot R_p} \cdot u_{Cp,bot} \\ &\quad - \frac{1}{C_{p2}} \cdot \bar{S}_{iap,bot} \cdot i_{\alpha} - \frac{1}{C_{p2}} \cdot \bar{S}_{ibp,bot} \cdot i_{\beta} + \frac{1}{C_{p2} \cdot R_p} \cdot U_{dcp}\end{aligned}\quad (21)$$

The equations above can be applied analogously to the secondary side of the converter.

Simulation Results

The optimal integration approach for the modulation method provided in [8] has been validated by simulations using the software PLECS. The simulation parameters are listed in Table I.

Table I: Parameters of the simulation

Parameters	Values	Parameters	Values
dc-link voltage at the primary side	5 kV	dc-link voltage at the secondary side	5.5 kV
Main inductance	10 mH	Leakage inductance	67.5 μ H
dc-link capacitor	5 mF	Switching frequency	1 kHz
Phase shift	30°	Resistance	0.1 m Ω
Sampling time	1 μ s	Duty cycle	0.5

The PLECS average model using the simplified transformer model is compared with the self-defined code average model, in respect of phase voltages and ac currents, as shown in Fig. 7. Both errors of the phase voltages are small enough to be neglected. The errors of the ac currents are smallest with the trapezoidal integration method.

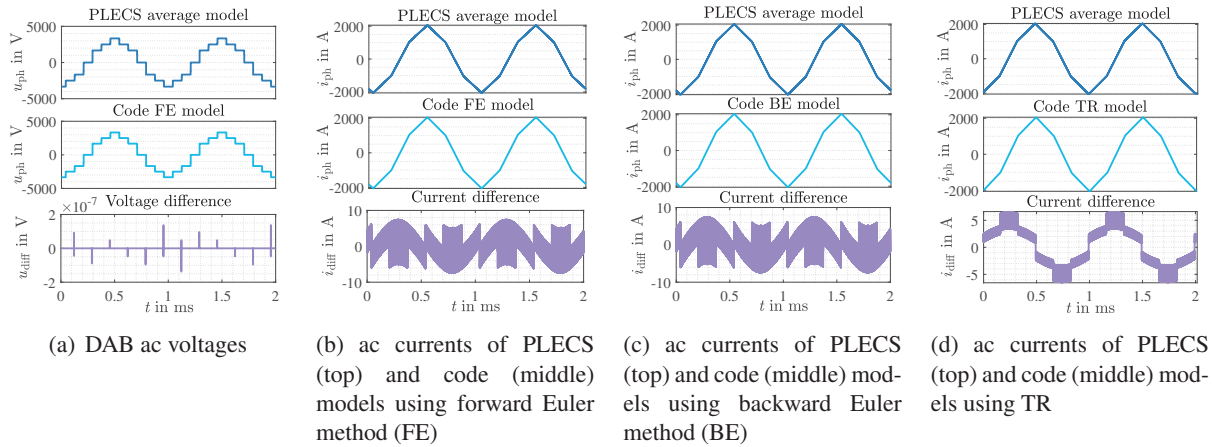
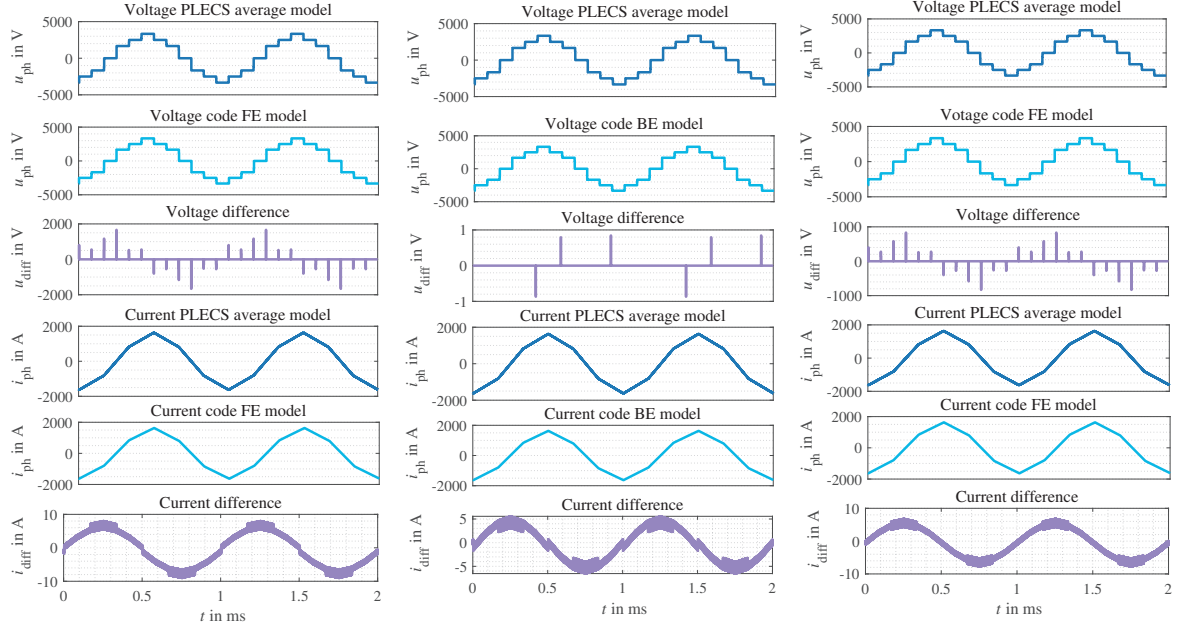


Fig. 7: Simulation results of the implemented 3L-DAB3 models with the simplified transformer model

The PLECS average model compares to the self-defined code average model using the three single-phase transformer in Y-Y connection, as shown in Fig. 8. The phase voltages using this model differ from those generated using the simplified model. During the switching transition for $1\ \mu\text{s}$, there are maximum 800 V and 1800 V differences for TR and FE, respectively. The voltages of the simplified model are estimated based on the state of the switches without integrating the currents. In contrast, the three single-phase transformer is determined by integrating the phase currents. The application of the integration methods only has an impact during switching transitions. Throughout all other time periods, the errors are less than 0.01%.



(a) DAB ac voltages and currents using FE (b) DAB ac voltages and currents using BE (c) DAB ac voltages and currents using TR

Fig. 8: Simulation results of the implemented 3L-DAB3 models with three single-phase transformers in Y-Y connection

HIL Verification

An HIL test setup for the models using an RT simulator XRS7070 of AixControl is shown in Fig. 9. The RT controller sends PWM signals to the RT simulator. The simulator calculates the voltages and currents and sends the results back to the RT controller. The 3L-DAB3 average model can be implemented either directly by the PLECS average model or by the self-defined C-code average model using the aforementioned modeling methodology. The C-code is automatically generated from PLECS models and can be subsequently downloaded into the RT simulator [6]. The test parameters are the same as that used in the simulation, as summarized in Table I.

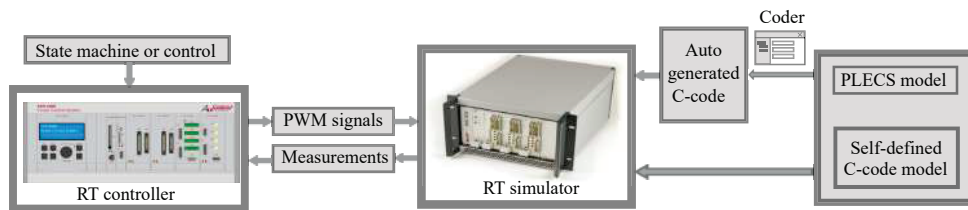


Fig. 9: Setup of the HIL test for a 3L-DAB3 converter

The HIL results with both the PLECS models and the self-defined C-code average models with an RT

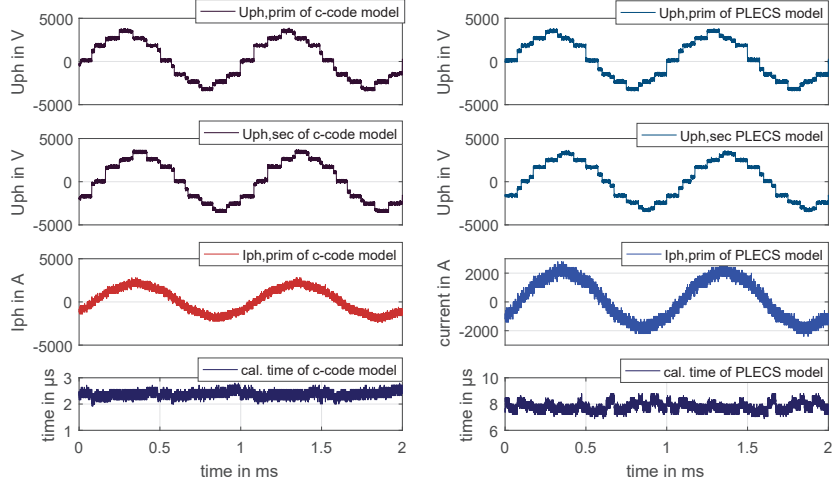


Fig. 10: Results of simulator XRS7070 using the simplified transformer model and TR method

simulator are shown in Fig. 10. The phase voltages and ac currents of both models coincide with each other. The calculation time for the C-code average model is approximately 2.5 s, which is 75% faster than that one of the PLECS model. An overall comparison of the applied models is provided in Table II. The auto-generated C-code from the PLECS model comprises 70,000 lines of code, whereas the self-defined C-code model has only less than 600 lines of code. The total run time includes the time spent communicating input and output as well as for the computation of the model. To ensure that the entire procedure is completed within one time step, the step size T should be greater than the total time. This prevents the RT simulation from overrunning. As a result, the minimum step time of the PLECS model is 25 μ s, which is 47% longer than for the C-code model. In the RT simulator, the calculation time of the C-code model is 68% faster than that of the PLECS model. The time for input and output communication does not differ significantly, since they are determined almost entirely by the number of ports and slots used. Therefore, the difference in total time is not significantly higher than the difference in the calculation time.

Table II: Comparison between the C-code model and the PLECS model of the 3L-DAB3 in the RT simulator (in μ s)

	C-code model	PLECS model
Code lines	<600	>70000
Time-step	17 μ s	25 μ s
Solver	fixed-step RADAU	fixed-step RADAU
Integration method	TR	unknown
Calculation time	<3 μ s	<8.5 μ s
Total time	<15 μ s	20 μ s

Numerical Stability Analysis of C-Code Average Model

In this section, the numerical stability of the C-code average model for 3L-DAB3 using different integration is analyzed. By using the preceding equations, a state-space model representing the 3L-DAB3 topology can be obtained. The top and bottom dc-link voltages of the primary side $u_{Cp,top}$ and $u_{Cp,bot}$, the top and bottom dc-link voltages of the secondary side $u_{Cs,top}$ and $u_{Cs,bot}$ and the ac currents i_α and i_β are taken as the state variables. Input variables are the dc-link voltages of the primary and secondary sides

U_{dcp} and U_{dcs} , respectively. A state-space model of the 3L-DAB3 can be expressed as

$$\dot{x} = A \cdot x + B \cdot u \quad (22)$$

$$y = C \cdot x + D \cdot u \quad (23)$$

with the state variables $x = \begin{bmatrix} u_{\text{Cp,top}} \\ u_{\text{Cp,bot}} \\ u_{\text{Cs,top}} \\ u_{\text{Cs,bot}} \\ i_\alpha \\ i_\beta \end{bmatrix}$, the inputs $u = \begin{bmatrix} U_{\text{dcp}} \\ U_{\text{dcs}} \end{bmatrix}$ and the outputs $y = \begin{bmatrix} u_{\alpha p} \\ u_{\beta p} \\ u_{\alpha s} \\ u_{\beta s} \end{bmatrix}$.

$$A = \begin{bmatrix} -\frac{1}{C_{p1}R_p} & -\frac{1}{C_{p1}R_p} & 0 & 0 & -\frac{\bar{S}_{i\alpha p,\text{top}}}{C_{p1}} & -\frac{\bar{S}_{i\beta p,\text{top}}}{C_{p1}} \\ -\frac{1}{C_{p2}R_p} & -\frac{1}{C_{p2}R_p} & 0 & 0 & -\frac{\bar{S}_{i\alpha p,\text{bot}}}{C_{p2}} & -\frac{\bar{S}_{i\beta p,\text{bot}}}{C_{p2}} \\ 0 & 0 & -\frac{1}{C_{s1}R_s} & -\frac{1}{C_{s1}R_s} & \frac{\bar{S}_{i\alpha s,\text{top}}}{C_{s1}} & \frac{\bar{S}_{i\beta s,\text{top}}}{C_{s1}} \\ 0 & 0 & -\frac{1}{C_{s2}R_s} & -\frac{1}{C_{s2}R_s} & \frac{\bar{S}_{i\alpha s,\text{bot}}}{C_{s2}} & \frac{\bar{S}_{i\beta s,\text{bot}}}{C_{s2}} \\ \frac{\bar{S}_{u\alpha p,\text{top}}}{L_\sigma} & \frac{\bar{S}_{u\alpha p,\text{bot}}}{L_\sigma} & -N \cdot \frac{\bar{S}_{u\alpha s,\text{top}}}{L_\sigma} & -N \cdot \frac{\bar{S}_{u\alpha s,\text{bot}}}{L_\sigma} & -\frac{R_w}{L_\sigma} & 0 \\ \frac{\bar{S}_{u\beta p,\text{top}}}{L_\sigma} & \frac{\bar{S}_{u\beta p,\text{bot}}}{L_\sigma} & -N \cdot \frac{\bar{S}_{u\beta s,\text{top}}}{L_\sigma} & -N \cdot \frac{\bar{S}_{u\beta s,\text{bot}}}{L_\sigma} & 0 & -\frac{R_w}{L_\sigma} \end{bmatrix}, B = \begin{bmatrix} \frac{1}{C_{p1} \cdot R_p} & 0 \\ \frac{1}{C_{p2} \cdot R_p} & 0 \\ 0 & \frac{1}{C_{s1} \cdot R_s} \\ 0 & \frac{1}{C_{s2} \cdot R_s} \\ 0 & 0 \\ 0 & 0 \end{bmatrix},$$

$$C = \begin{bmatrix} \bar{S}_{u\alpha p,\text{top}} & \bar{S}_{u\alpha p,\text{bot}} & 0 & 0 & 0 & 0 \\ \bar{S}_{u\alpha p,\text{top}} & \bar{S}_{u\alpha p,\text{bot}} & 0 & 0 & 0 & 0 \\ 0 & 0 & \bar{S}_{u\beta s,\text{top}} & \bar{S}_{u\beta s,\text{bot}} & 0 & 0 \\ 0 & 0 & \bar{S}_{u\beta s,\text{top}} & \bar{S}_{u\beta s,\text{bot}} & 0 & 0 \end{bmatrix}, D = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}$$

The model above must be discretized to be processed on a digital processor. In this work, FE, BE, and TR are implemented to discretize the state-space model in the format:

$$x[n+1] = F \cdot x[n] + G \cdot u[n] \quad (24)$$

Based on the stability criterion, a discrete-time system is analytical stable if and only if all of its eigenvalues are located inside a unit circle. The three integration methods have the same matrix A , but they have different stability regions according to A . To normalize the stability region, the continuous state-space matrix A is transferred to the discrete state-space matrix F . The stable region for each integration method is transferred to be a unit circle about the origin point with the matrix F . The relationship between the current and voltage variables in the next time step using the FE, BE, and TR integration are respectively derived in (25), (26) and (27). The matrix F for each integration method can be concluded as:

$$\begin{aligned} x(t+h) &= x(t) + \dot{x}(t) \cdot T \\ \Leftrightarrow x(t+T) &= (1 + h \cdot A) \cdot x(t) \Rightarrow F_{\text{FE}} = 1 + T \cdot A \end{aligned} \quad (25)$$

$$\begin{aligned} x(t+T) &= x(t) + \dot{x}(t+T) \cdot T \\ \Leftrightarrow x(t+T) &= (1 - T \cdot A)^{-1} \cdot x(t) \Rightarrow F_{\text{BE}} = (1 - T \cdot A)^{-1} \end{aligned} \quad (26)$$

$$\begin{aligned} x(t+T) - x(t) &= \frac{1}{2} \cdot [\dot{x}(t+T) + \dot{x}(t)] \cdot T \\ \Leftrightarrow x(t+T) &= \frac{1 + \frac{1}{2} \cdot T \cdot A}{1 - \frac{1}{2} \cdot T \cdot A} \cdot x(t) \Rightarrow F_{\text{TR}} = \frac{1 + \frac{1}{2} \cdot T \cdot A}{1 - \frac{1}{2} \cdot T \cdot A}. \end{aligned} \quad (27)$$

Apart from an optimized simulation, the derived mathematical description further allows for an analysis

of the numerical stability for different discretization methods and time steps [7]. The eigenvalues can be obtained from the matrix F of the state-space model and used to analyze the stability of the system. Fig. 11 depicts the eigenvalues of discrete matrices of the 3L-DAB3 converter for different discretization approaches with the extended parameter range. The location of the poles is indicative of the dynamics and stability of the system. Fig. 11 illustrates, that both BE and TR are stable with an extended range of parameters.

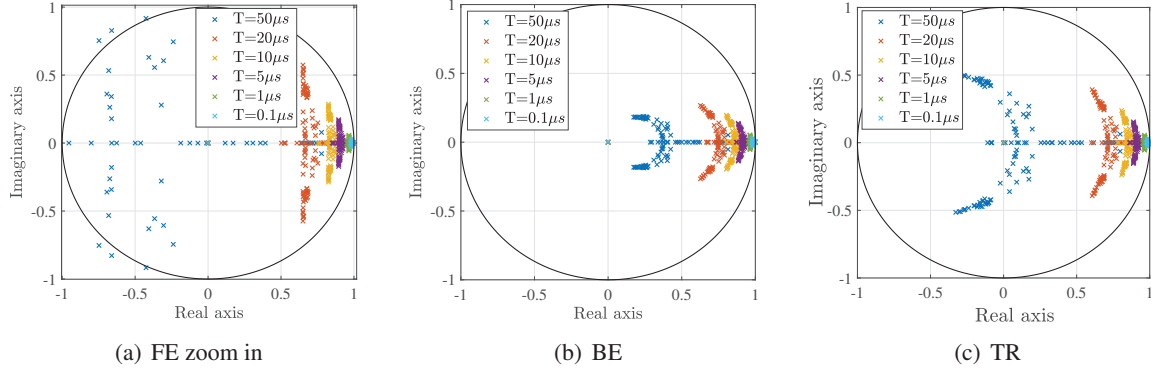


Fig. 11: Stability test of the 3L-DAB3 C-code average model with an extended range of specifications

The natural frequency (around the boundary) and the damping ratio (along the radius) are depicted in Fig. 11. There are more unstable poles with a larger time-step (light colour in Fig. 11) than with a smaller time-step (dark blue in Fig. 11). There are 1,824 out of 28,416 poles unstable with step size $1 \mu s$ and FE integration. The unstable poles are far away from the unit circle and are therefore not completely included in the Fig. 11. No poles with BE or with TR are unstable. Although the model with a smaller step time has poles intuitively closer to the unit circle boundary, it has a better dynamic performance than the system of larger time steps. Both BE and TR are suitable for the code average model of the 3L-DAB3 converter with the specified parameters.

Conclusion

The C-code average model of the 3L-DAB3 converter is more efficient than the PLECS average model. In the RT simulation, the model is valid with a reduced time step and requires less calculation steps and offers shorter execution time. Of the three integration algorithms, the trapezoidal integration offers the best precision. The T-equivalent transformer model is more accurate than the simplified transformer model but requires more computation time on the simulator. By introducing a self-defined C-code average model, the real-time model of the 3L-DAB3 converter can be used for CHIL testing of DAB converters with higher switching frequencies.

References

- [1] Seung Tae, Cha, Qiuwei Wu, Arne Hejde Nielsen, Jacob: Real-Time Hardware-in-the-Loop (HIL) Testing for Power Electronics Controllers
- [2] Ming Jia and Philipp Joebges and R. W. De Doncker: A Fast and Robust Model of Dual-Active Bridge Converters in Real-Time Simulation, 2020 22nd European Conference on Power Electronics and Applications, 2020
- [3] Hafiz Abu Bakar Siddique: The Three-Phase Dual-Active Bridge Converter Family Modeling, Analysis, Optimization and Comparison of Two-Level and Three-Level Converter Variants, Dissertation, RWTH Aachen, DOI: 10.18154/RWTH-2020-01205, 2019
- [4] Stephan Thomas: A Medium-Voltage Multi-level DC/DC Converter with High Voltage Transformation Ratio, Dissertation, RWTH Aachen, 2014
- [5] Jost Allmeling, Niklaus Felderer and Min Luo: High Fidelity Real-Time Simulation of Multi-Level Converters, The 2018 International Power Electronics Conference, 2018
- [6] Philipp Joebges: Distributed Real-Time Simulation of Modular Bidirectional DC-DC Converters for Control-Hardware-in-the-Loop, Dissertation RWTH Aachen University, DOI: 10.18154/RWTH-2021-10060, 2021

- [7] Robert Uhl and Amir Arasteh and Antonello Monti and Arne Hinz and Rik W. De Doncker: Nodal-Reduced Modeling of Three-Phase Dual-Active Converters for EMTP-type Simulations, 2017 IEEE 26th International Symposium on Industrial Electronics (ISIE), 2017
- [8] Philipp Joebges and Anton Gorodnichev and R. W. De Doncker: Modulation and Active Midpoint Control of a Three-Level Three-Phase Dual-Active Bridge DC-DC Converter under Non-Symmetrical Load, 2018 International Power Electronics Conference, 2018