High Switching Frequency Operation of a Single-Phase Five-Level Hybrid Active Neutral Point Clamped Inverter with a Model Predictive Control Approach

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Keywords

«Voltage Source Inverter (VSI)», «Model Predictive Control», «Multi-level converters», «Silicon Carbide (SiC)», « Capacitor voltage balancing».

Abstract

Wide bandgap (WBG) devices such as Silicon-Carbide (SiC) MOSFETs can be utilized to increase the switching frequency of power electronic converters. The size of passive components of an output filter can be reduced by increasing the switching frequency of converters or the number of output levels thorough the employment of multilevel topologies. Therefore, the combination of multilevel converters and WBG switches with a high switching frequency can improve the dynamic of converters. Meanwhile, a high bandwidth controller is also required to achieve a fast dynamic response of the system. In this paper, an advanced model predictive control (MPC) approach, based on the concept of hysteresis current control, is presented for a single-phase five-level hybrid active neutral point clamped (ANPC) inverter. A hybrid modulation technique with different switching frequencies is considered in this paper. As a result, different semiconductor technologies including SiC and Si are employed in the structure of the converter. Considering the AC and DC sides mathematical modeling of the converter, an MPC with the ability to control the neutral point (NP) voltage is designed. Finally, experimental results show that by utilizing the SiC MOSFETs and the proposed advanced MPC structure, the inverter's switching frequency is increased, with lower current ripple and fast dynamic performance.

Introduction

Multilevel converters offer lower *dv/dt*, common-mode voltage, current and voltage total harmonic distortion (THD), and smaller filter inductance compared to the conventional two-level converter [1]–[3]. Among the different utilizations of multilevel converters, single-phase power converters have been employed in photovoltaic (PV), electric railway traction, and power factor correction applications [4]–[9]. One interesting topology for these applications is the hybrid active neutral-point-clamped (H-ANPC) converter. In the converter structure, eight switches are utilized and can generate up to five output voltage levels [6], [10], [11].

Different control strategies have been proposed for single-phase applications. Meanwhile, with the development of advanced and fast microprocessors, the implementation of complex control algorithms such as model predictive control can be considered. The main concept of MPC control is based on the utilization of the discrete characteristics of power electronic converters. The system outputs' future behavior is predicted based on the mathematical model of the system and present values of converter outputs. In addition, system constraints and purposes are employed through a cost function. At each sampling time, the cost function is evaluated for different switching states, and the optimized solution will be utilized to determine the next switching state of the converter [12]–[14].

Among various MPC techniques, finite control set MPC (FCS-MPC) is a popular MPC strategy. In this strategy, the output voltage vectors of a converter are considered as the control inputs, which are applied to handle the optimal control problem [10], [15]–[17]. Fast-dynamic response, simple implementation, and the ability to integrate advanced control objectives in the design of its cost function can be counted as the features of FCS-MPC [13], [14], [18]. Considering the elimination of switching modulators and inner control loops and their delays by employing the FCS-MPC, the system can be operated with higher bandwidth [19].

In this paper, an MPC based on hysteresis current control is proposed for a single-phase five-level hybrid ANPC inverter. A hysteresis band for the current of the filter inductor is defined to limit the current ripple. The proposed method is implemented by utilizing both a microprocessor and an FPGA. Thus, the overall sampling frequency of the controller is set to 100 kHz. A prototype inverter with two different switch technologies, including Si and SiC MOSFETs, is selected to validate the controller.

Structure of single-phase five-level Hybrid ANPC Inverter

The structure of the single-phase hybrid ANPC is shown in Fig.1. The converter is comprised of eight switches and two dc-link capacitors. The hybrid switching states of this converter are listed in Table I. As it can be seen in Table I, five voltage levels at the output (v_{ab}) of the converter can be obtained. During the positive half cycle S_5 and S_8 are conducting, while S_6 and S_7 are in on-state condition at the negative half cycle. Thus, the switching frequency of S_5-S_8 is fundamental (low frequency switches). Meanwhile, during the positive and negative half cycles, the switching states of S_1-S_4 (high frequency switches) are altered to obtain different output voltage levels. Due to devices switching frequencies, two different switch technologies can be considered for low and high frequency switches. In this study, SiC and Si MOSFETs are employed in the structure of the converter.

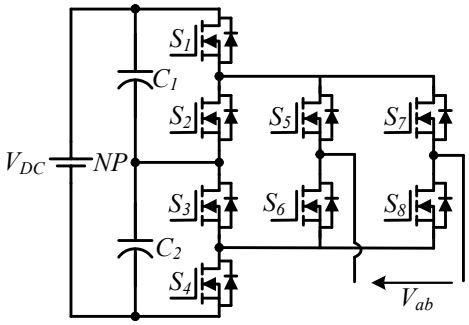


Fig. 1: The structure of the hybrid active neutral point clamped inverter.

Table I: The switching states of 5-level single-phase ANPC

Output Vector	Switching states								v_{ab}
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	
V_1	1	0	0	1	1	0	0	1	V_{dc}
V_2	1	0	1	0	1	0	0	1	$V_{dc}/2$
V_3	0	1	0	1	1	0	0	1	$V_{dc}/2$
V_4	0	1	1	0	1	0	0	1	0
V_5	0	1	1	0	0	1	1	0	0
V_6	1	0	1	0	0	1	1	0	$-V_{dc}/2$
V_7	0	1	0	1	0	1	1	0	$-V_{dc}/2$
V_8	1	0	0	1	0	1	1	0	$-V_{dc}$

The general schematic of the system is shown in Fig. 2. As it can be seen, the load is supplied through an LC filter. To control the NP voltage, the effect of each vector on the NP voltage variation should be considered. The output vectors can be divided into three groups: large, small, and zero vectors. The large

(V_1, V_8) and zero (V_4, V_5) do not affect the NP voltage. Meanwhile, the small vectors (V_2, V_3, V_5, V_6) can change the NP voltage, in which the output current passes through one of the dc-link capacitors. Table II shows the effect of small vectors on the NP voltage [10].

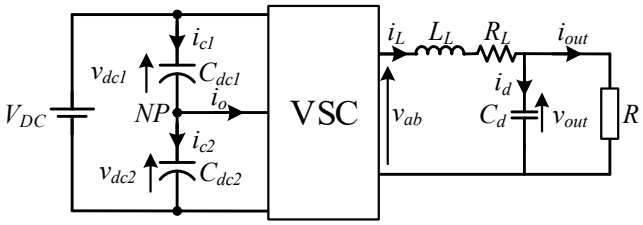


Fig. 2: The general schematic of the system.

Table II: The effect of small vectors on the NP voltage.

Vector	Output current	$v_{NP}=v_{dc1}-v_{dc2}$
$\mathbf{V_2}$	$i_L>0$	↓
	$i_L<0$	↑
$\mathbf{V_3}$	$i_L>0$	↑
	$i_L<0$	↓
$\mathbf{V_6}$	$i_L>0$	↑
	$i_L<0$	↓
$\mathbf{V_7}$	$i_L>0$	↓
	$i_L<0$	↑

Mathematical Modeling of the System

The mathematical model of the converter, including AC and DC sides, should be obtained to develop an MPC system. Considering the schematic of the system shown in Fig. 2, the voltage across the load (v_{out}) and filter inductor current (i_L) can be shown as state-space as follows [10]:

$$\frac{d}{dt}\begin{bmatrix} i_L \\ v_{out} \end{bmatrix} = A\begin{bmatrix} i_L \\ v_{out} \end{bmatrix} + B\begin{bmatrix} v_{ab} \\ i_{out} \end{bmatrix} \quad A = \begin{bmatrix} -\frac{R_L}{L_L} & -\frac{1}{L_L} \\ \frac{1}{C_d} & 0 \end{bmatrix}, B = \begin{bmatrix} \frac{1}{L_L} & 0 \\ 0 & -\frac{1}{C_d} \end{bmatrix} \tag{1}$$

where L_L, R_L are the inductance and resistance of filter inductor, and C_d is the value of the filter capacitor.

For the DC side of the converter, whenever the small vectors are applied the NP current (i_o) is equal to the filter inductor current. Thus, the voltage of dc-link capacitors can be obtained through the following equations [10]:

$$i_{c1} = C_{dc1} dv_{dc1}/dt \tag{2}$$

$$i_{c2} = C_{dc2} dv_{dc2}/dt \tag{3}$$

Moreover, the NP voltage is defined as:

$$v_{NP} = v_{dc1} - v_{dc2} \tag{4}$$

Assuming the sampling frequency is relatively high, the equations can be discretized based on the discrete step time of T_s. For example, the voltages of dc-link capacitors are discretized as follows:

$$v_{dc1}(k+1) = v_{dc1}(k) + \frac{T_s}{C_{dc1}} i_{c1}(k) \tag{5}$$

$$v_{dc2}(k+1) = v_{dc2}(k) + \frac{T_s}{C_{dc2}} i_{c2}(k) \tag{6}$$

which $v_{dc1}(k+1)$ and $v_{dc2}(k+1)$ are the predictive voltages of upper and lower dc-link capacitors at the $(k+1)^{th}$ instant.

MPC Algorithm

The cost function for MPC should be defined to achieve the desired purposes, such as tracking the reference voltage, keeping the current ripple of the filter inductor in the hysteresis band, and regulating the NP voltage. Consequently, the cost function is comprised of three subfunctions defined as follows:

$$CF: |v_{out}(n+1)^* - v_{out}(n+1)| + \lambda_1(|v_{dc1}(n+1) - v_{dc2}(n+1)|) + hys(n+1) \tag{7}$$

where λ_1 is the weighting factor to balance the NP voltage. The first subfunction is used for tracking the reference voltage. The aim of the second subfunction is to keep the NP voltage constant and zero. The subfunction of $hys(n+1)$ is employed to reduce the current ripple in the filter inductor, which is defined as follows:

$$hys(n+1) = \begin{cases} \infty, & \text{if } |i_L(k+1)| > |i_L{}^*(k+1)| + lim \ \ \& \ \ |i_L(k+1)| < |i_L{}^*(k+1)| - lim \\ 0, & \text{if } |i_L(k+1)| < |i_L{}^*(k+1)| + lim \ \ \& \ \ |i_L(k+1)| > |i_L{}^*(k+1)| - lim \end{cases} \tag{8}$$

where *lim* is the hysteresis band as it is shown in Fig. 3.

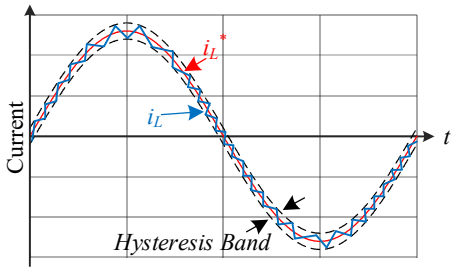


Fig. 3: The defined hysteresis band of the filter inductor current

Each of the output vectors (V_i, i=1-8) has a different effect on the value of the cost function (7) through (1), in which v_{ab} is replaced with the output voltage vectors. As mentioned earlier, the small vectors change the NP voltage and, consequently, the value of the cost function through (2) and (3). In each step, the value of the cost function is calculated for all the vectors, and a vector with the minimum related cost function is chosen to apply.

Experimental Results

To verify the performance of the proposed MPC, different experiments are performed. The prototype of the converter, including an LC filter, is shown in Fig. 4. To control the converter, dSPACE Micro-Lab Box ds1202 is used. The suggested method is implemented in the dSPACE microprocessor with a frequency of 100 kHz. Meanwhile, the dSPACE FPGA is employed to apply the selected vector with consideration of deadtimes between switches. The parameters of the built system are listed in Table III.

The steady-state experimental results of the system are shown in Fig. 5. Fig. 5(a) shows the output voltage (v_{out}), the inductor current (i_L), and the load current (i_{out}). In addition, Fig. 5(a) includes a zoomed view of the inductor current during the peak current.

The voltages of dc-link upper and lower capacitors (v_{dc1}, v_{dc2}) and the output of the converter (v_{ab}) are shown in Fig. 5 (b). It can be seen, the proposed MPC regulates the NP voltage and controls the output voltage of the converter.

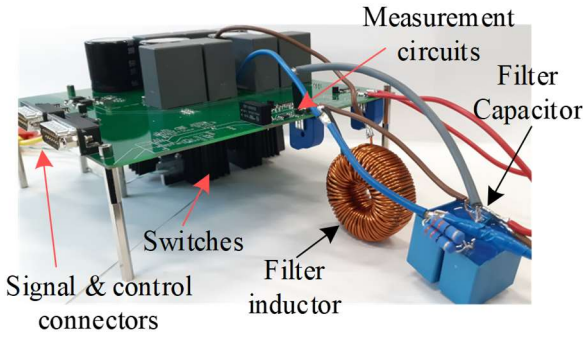
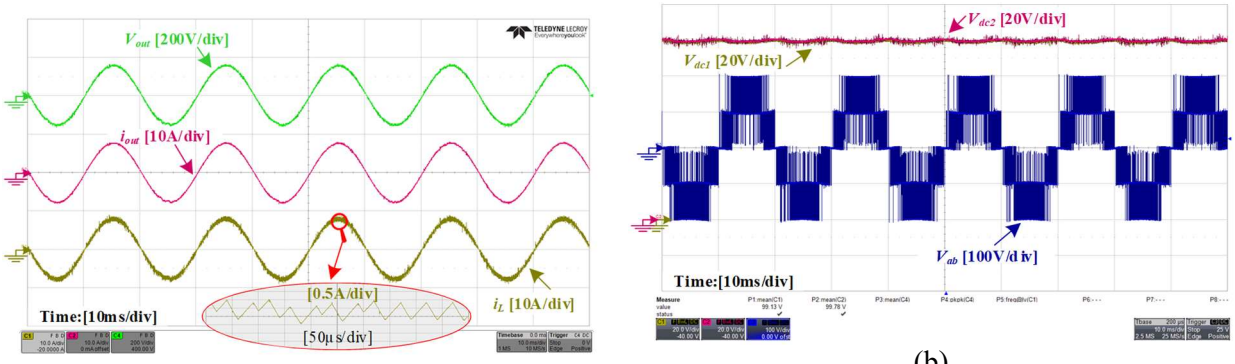


Fig. 4: The single-phase 5-level hybrid ANPC inverter with an LC filter.

Table III: The system parameters

Parameter	Definition	value
V_{DC}	DC supply voltage	200 V
V_{out}	The voltage across the load	110 V (rms)
C_1, C_2	DC-link capacitors	1 mF
L	Filter inductance	600 µH
R_L	The resistance of filter inductor	0.1 Ω
C_d	Filter capacitor	2 µF
R	Load	20 Ω
f	Reference output frequency	50 Hz
T_s	Sampling time	10 µs



(a) (b)

Fig. 5: The steady-state results of proposed MPC (a) The inductor current, output voltage, and load current, (b) the voltages of dc-link upper and lower capacitors and output voltage of the converter.

The harmonics spectrum of load current is shown in Fig. 6. The main harmonics are in the frequency range up to 30kHz.

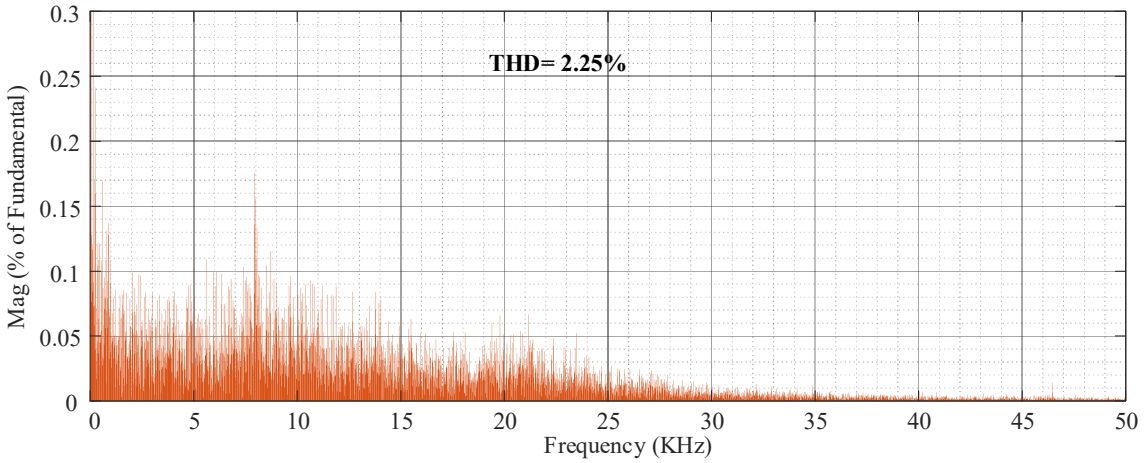


Fig. 6: The harmonics spectrum of output current.

To evaluate the performance of the suggested method during the transition, a step-change in the load value is introduced. The output voltage, the current of the filter inductor and the load are shown in Fig. 7. As it can be seen, the proposed MPC is able to keep the output voltage constant quickly and to follow the reference waveform.

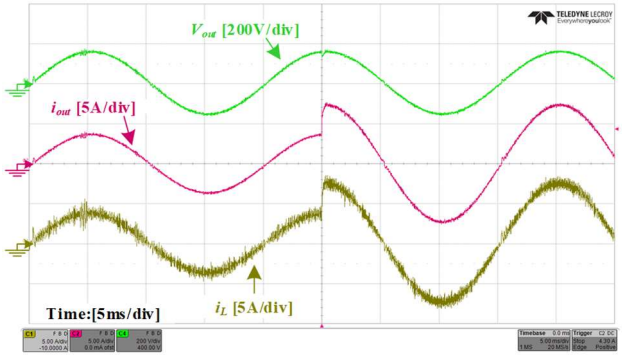


Fig. 7: The dynamic experimental results of proposed MPC when the load is changed.

Conclusion

In this paper, an MPC based on the hysteresis current control for a single-phase 5-level hybrid ANPC has been proposed. In the structure of the converter, SiC MOSFETs are utilized to increase the switching frequency of the converter in order to reduce the size of the filter and current ripples. The proposed MPC was implemented with an FPGA to have superior performance and fast dynamic response. Experimental results verify the performance of the proposed MPC both at steady-state and transition conditions.

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