A PFC boost converter with reduced switching losses operating at a fixed switching frequency

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Keywords

«Power factor correction», «Switching losses», «Zero-voltage switching», «AC-DC converter», «Boost»

Abstract

A single-phase fixed-frequency operated power factor correction circuit with reduced switching losses is proposed. The circuit uses the combination of a boost converter with an added clamp-switch, a pulse wave shaping circuit, and a standard control IC to discharge the transistor's output capacitance prior to its turn-on. In this way, a very low-complexity control circuit implementation to reduce switching losses or even achieve complete zero-voltage switching without additional sensors is possible. Moreover, this operation method is achieved at a constant switching frequency, possibly simplifying the design of the EMI filter and the converter's inductor. Experimental test results for a 100 W prototype converter are presented to validate the feasibility of the proposed operating method and corresponding circuit structure.

Introduction

Soft-switching converters are commonly employed to reduce switching losses, mitigate EMI emissions, increase the operating frequency, and reduce the size of power conversion systems. E.g., for single-phase ac/dc converters in the lower to medium power range (i.e., below power levels of several hundred watts), critical conduction mode (CrM) or transition mode (TM) power factor correction (PFC) circuits, based on boost dc/dc converters, are commonly employed [1][2][3][4]. In these converters switching losses are reduced by turning the output diode off at zero current and afterward turning the main transistor on, in a quasi-resonant manner, at a low voltage. A drawback of this approach is that the converter operates at a varying switching frequency, depending on the output load and the momentary input voltage value. This variation in the switching frequency can complicate the inductor and input EMI filter design. Additionally, the minimum voltage at turn-on of the main switch depends on the momentary input to output voltage ratio. Therefore, zero-voltage switching (ZVS) is lost for high input voltages, as ZVS can be achieved in this type of converter only if $V_{in} < V_{out}/2$. For PFC circuits operating with input voltages at mains levels of 230 V (RMS) and a typical V_{out} of 380 V to 400 V, the ZVS operation is therefore limited to parts of the mains cycle. Also, this type of CrM converter often requires a detection circuit to achieve (partial) soft-switching.

Other approaches which allow a full ZVS operation independent of the input voltage level were presented in [5] and [6]. In [5], a four-switch buck-boost converter is proposed to achieve ZVS, and in [6], a triangular current mode (TCM) operation scheme for a bridgeless boost converter is presented. Both approaches rely on a varying switching frequency and more complicated control and sensor circuits which cannot be directly implemented using standard, off-the-shelf, PFC control ICs.

For the mitigation of some of the restrictions mentioned before, this article proposes a method to reduce switching losses or even achieve ZVS for single-phase PFC circuits, which allows the use of standard PFC control ICs and maintains a fixed operating frequency. This approach is based on a clamp-switch ZVS boost converter as presented in [7][8] and extends this operation method to single-phase active PFC systems.

Converter Circuit and Operation

Proposed Converter Circuit

A simplified schematic of the proposed single-phase PFC circuit, corresponding to the prototype presented later, is shown in Fig. 1. It is centered around the ZVS boost type dc/dc converter proposed in [7], which is used instead of a standard hard-switching boost topology to control the inductor current waveform and, therefore, the line current. Similar to the boost converter presented in [7], a clamp-switch network comprised of transistor T_{cl}, diode D_{cl}, and an additional clamp-capacitor C_{cl} in parallel to the converter's inductor L is added to a boost converter to reduce the switching losses and/or achieve soft-switching. Capacitor C_{cl} is added to the clamp-switch to adjust the ZVS range, as described in [7], allowing a ZVS operation even if $V_{out} < 2v_{in}$ and without any additional sensor circuitry.
Capacitors C_{in} and C_{out} are used in the same way as in a standard active PFC circuit. I.e., C_{in} is small in value, to only filter the high-frequency components in the inductor current i_L and capacitor C_{out} performs the low-frequency energy storage function at twice the mains frequency. Essentially the operation of this power stage can be traced back to the operating principle introduced in [7], with significant differences being here the continually varying rectified mains voltage as input and the added mains EMI filter. The latter also provides the required high-frequency differential mode filtering due to the large inductor current variation at the switching frequency in the proposed operating scheme.

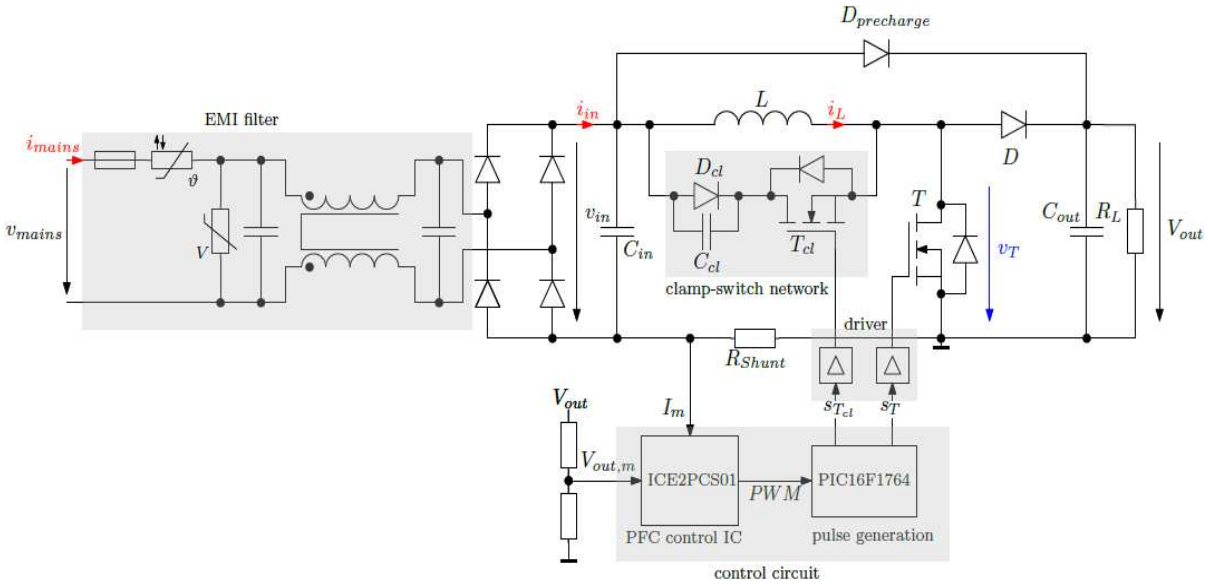

Fig. 1: Proposed clamp-switch single-phase boost type PFC rectifier

Basic Operation

Based on the more detailed description given in [7], a summary of the converter operation is presented in this paragraph.
The converter is designed to operate with discontinuous conduction mode (DCM) over the complete mains cycle if the clamp-switch is deactivated, by selecting a small inductance value L. The two transistors, T (main switch) and T_{cl} (clamp-switch), are driven with complementary pulse width modulated (PWM) signals at a fixed frequency, as shown in Fig. 2. Assuming a constant value of V_{in} during the switching period, eight different intervals can be identified. Here a possible ninth interval, where the body diode of the main transistor T conducts the current prior to T's turn-on, is omitted.

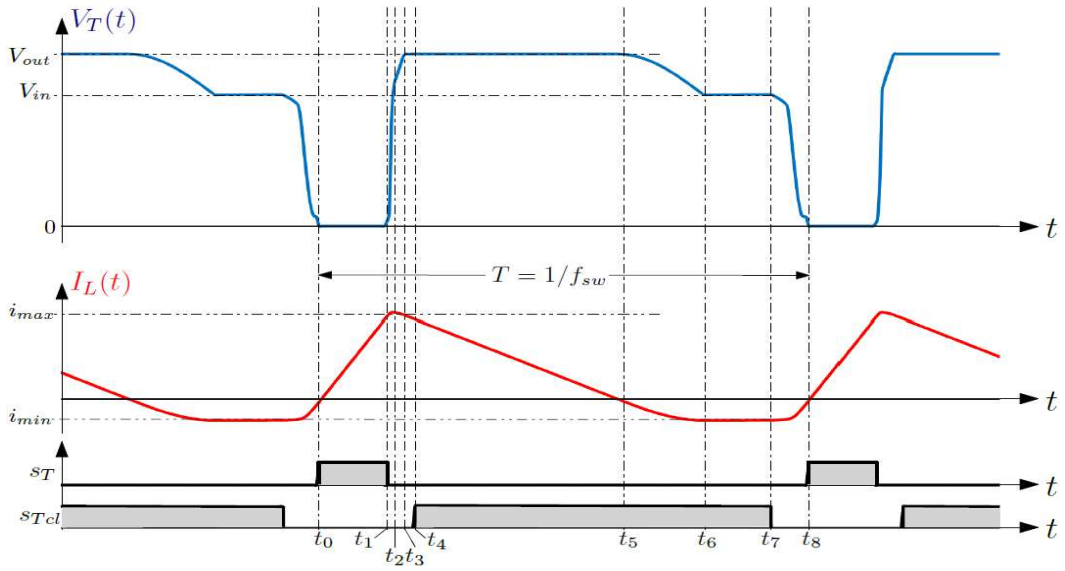

Fig. 2: Major simulated boost power stage waveforms during one high-frequency switching cycle

Interval 1 [$t_0 < t < t_1$]:
The switching cycle starts by turning on the main transistor at t_0, ideally a zero current. The turn-on time t_1 - t_0 is varied to control the primary power conversion operation, similar to a standard boost converter.
Interval 2 [$t_1 < t < t_2$]:
After T is turned-off at t_1, the inductor current will start to charge the total effective capacitance C_p at T's drain connection with the approximately constant maximum inductor current i_{max}. Voltage v_T will increase accordingly.
Interval 3 [$t_2 < t < t_3$]:
At t_2, the transistor voltage v_T reaches the value of V_{in}, causing the body diode of T_{cl} to turn on. This change in the switching state leads to an increase in the effective capacitance at the switch node. I.e., in the clamp-switch path, the resultant capacitance is no longer determined by the series connection of the capacitances of T_{cl} and C_{cl} (in parallel with D_{cl}'s capacitance C_{Dcl}) but then determined by resultant capacitance across the clamp diode D_{cl}. Therefore, the voltage slew rate of v_T will decrease.
Interval 4 [$t_3 < t < t_4$]:
The output diode D starts conducting at t_3 as the voltage v_T reaches V_{out}. The output capacitor will be charged, and the current i_L will decrease.
Interval 5 [$t_4 < t < t_5$]:
The clamp-switch T_{cl} is turned on at instant t_4 between t_3 and t_5. This process will not change the converter operation compared to the previous state but is necessary to allow a proper freewheeling during the following states. I.e., clamp-switch T_{cl} has to be turned on prior to t_5.
Interval 6 [$t_5 < t < t_6$]:
Diode D turns off at t_5 at the zero-crossing of i_L, comparable to the normal diode conduction state in a boost converter. Then, a resonant transition of v_T occurs, and inductor L resonates with the effective capacitance at the switch node during this interval. If the value C_{cl} is much larger than the other capacitances, C_{cl} will dominate this process and is used to set the minimum (negative) inductor i_{min} [7].
Interval 7 [$t_6 < t < t_7$]:
The resonant transition ends if the voltage v_T reaches the value V_{in}, as then diode D_{cl} gets forward biased. Therefore, the inductor current will freewheel, at a negative current value i_{min}, through the series connection of clamp-switch diode D_{cl} and transistor T_{cl}. In this way, energy is stored in the inductor to discharge later the transistor's effective capacitance at t_7.
Interval 8 [$t_7 < t < t_8$]:
At instant t_7, the clamp-switch T_{cl} turns off, and another resonant (discharge) transition of voltage v_T will be initiated. This will continue the discharge of the (parasitic) capacitances connected to the switch node prior to the turn-on of T. If this turn-on occurs after one-quarter of the resonant period, main switch T can be turned on at t_8 at the minimum voltage value $v_T(t)$. Thus, switching losses are reduced, and if v_T reaches approximately zero, even a ZVS turn-on is possible.

ZVS Condition at Varying Input Voltage

ZVS can be achieved in the converter if the minimum inductor current i_{min} has a sufficiently negative value to discharge the equivalent lumped parasitic capacitance C_p at the switch node during time interval six by an amount of V_{in}. I.e., the energy stored in the inductor at the end of the freewheeling phase at t_6 must be larger than the change in stored energy in the capacitor. Therefore, the ZVS condition can be written based on an energy balance as

$$L \cdot i_{min}^2 \geq C_p \cdot v_{in}^2 \tag{1}$$

In a PFC converter, the input voltage varies, during the line cycle, as

$$v_{in}(t) = \hat{v}_{in} \cdot |\sin(2\pi \cdot f \cdot t)| \tag{2}$$

This variation in $v_{in}(t)$ also changes the minimum inductor current value (c.f. i_{min} in Fig. 2) during the mains cycle. Using eq. (9) from [7] and substituting (2), $i_{min}(t)$ can be written as

$$i_{min}(t) = (\hat{v}_{in} \cdot |\sin(2\pi \cdot f \cdot t)| - V_{out}) \cdot \sqrt{\frac{C_{cl}+C_p}{L}} \tag{3}$$

As both $i_{min}(t)$ and $v_{in}(t)$, according to (1), determine if ZVS is possible, the condition to achieve a soft-switching will therefore vary across the mains cycle. The worst-case operating point regarding ZVS will be when $v_{in}(t)$ reaches its maximum value $\hat{v}_{in}$ at $t = 1/(2f)$. At this instant, the required energy to achieve ZVS, according to (1), has at its maximum value. In contrast, the current $|i_{min}(t)|$ will be at the lowest value, and therefore, the stored energy in L is also at its minimal value. The minimum current, in this case, will be

$$i_{min}\left(t = \frac{1}{2f}\right) = (\hat{v}_{in} - V_{out}) \cdot \sqrt{\frac{C_{cl}+C_p}{L}} \tag{4}$$

Substituting the (4) in (1) and simplifying yields the following ZVS condition for the converter

$$\left(1 - \frac{V_{out}}{\hat{v}_{in}}\right)^2 \left(\frac{C_{cl}}{C_p} + 1\right) - 1 > 0 \tag{5}$$

If (5) is solved for C_{cl}, the following design equation to select C_{cl} to achieve ZVS is derived:

$$C_{cl} > \left(\frac{1}{\left(1 - \frac{V_{out}}{\hat{v}_{in}}\right)^2} - 1\right) \cdot C_p \tag{6}$$

This last equation is valid for $V_{out} < 2\hat{v}_{in}$. If $V_{out} > 2\hat{v}_{in}$, then the evaluation of (6) leads to a negative value, indicating that a ZVS is in this case, at least in theory, possible even if C_{cl} is omitted. Therefore, by a suitable choice of C_{cl}, a ZVS operation over the whole mains cycle can (theoretically) be achieved. For a practical PFC converter at a nominal (European) mains voltage level of $\hat{v}_{in} = \sqrt{2} \cdot 230\ V$ and V_{out} in the range of 380 V to 400 V, the ratio $V_{out} / \hat{v}_{in}$ is 1.15...1.25. In this case, the required capacitance value C_{cl}, predicted by (6), would be about 16 to 44 times the value of C_p. Selecting such a large value increases the negative inductor current's absolute value and leads to increasing losses (e.g., inductor and semiconductor conduction losses), which could offset the loss reduction gained by achieving ZVS. Therefore, it is suggested to choose a smaller value for C_{cl} than predicted by (6), even if ZVS is only achieved over parts of the mains cycle.

The discussion of the ZVS range above assumes a lossless converter and linear capacitances values. In particular, the decrease of the stored energy in the inductor during the freewheeling phase due to voltage drop of the clamp-switch diode and transistor is neglected.

PFC Control Method and Line Current Distortion

A low-complexity control implementation for the converter circuit is proposed by using a standard PFC control IC and complementing it with a pulse waveform generator circuit. The latter converts the single-ended PWM drive signal of a standard PFC IC into two complementary drive signals with inserted dead times. (a suitable gate driver circuit could also perform this task). A possible scheme is presented in Fig. 3. Here, an IC employing a multiplier free control law (c.f. to [9-11]), which is commonly employed in continuous conduction mode (CCM) PFC circuits, is used.

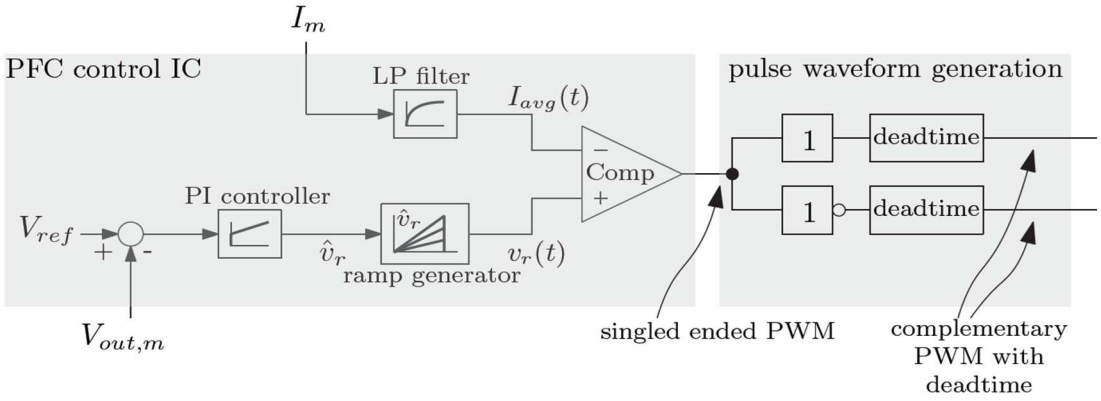

Fig. 3: Possible implementation of a PFC control scheme according to the proposed operation mode

In this control approach, a measured inductor current value $I_M = k_m \cdot I_L$ is first low-pass filtered to extract a value $I_{avg}(t)$ proportional to the moving average $\bar{\imath}_L$ of the inductor current. This value is compared to a sawtooth carrier signal with variable amplitude $\hat{v}_R$ to generate the main transistor's relative off time $d_{off} = t_{off} / T$. Therefore, $d_{off} = k \cdot I_{avg}$ is proportional to the average inductor current, and as it has been shown by Ben-Yaakov et al. in [9] (c.f. eq. (2) in [9]), the following applies for a PFC based on a CCM boost converter

$$\frac{v_{in}}{i_{in}} = \frac{d_{off}}{I_{avg}} \cdot V_{out} = k \cdot V_{out} \tag{7}$$

The factor k in (7) is the ratio of current measurement gain k_m to the amplitude $\hat{v}_R$ of the sawtooth,

$$k = \frac{k_m}{\hat{v}_R} \tag{8}$$

The converter will therefore show a resistive input characteristic in this case if V_{out} is approximately constant. The outer voltage loop controller determines the amplitude $\hat{v}_R$. Therefore, the average inductor current for a boost converter operating in CCM follows the rectified input voltage v_{in}, and a simple PFC functionality can be achieved [9-11].

The described operation method is intended to control a CCM boost converter; therefore, as the power stage is more comparable to a DCM converter, additional line current distortions will be introduced. The resulting distortions can be roughly estimated when evaluating the control law (7) for a DCM operating boost converter. Therefore, by neglecting the negative part of $i_L(t)$ and assuming an idealized DCM inductor current waveform during the high-frequency switching cycles, the moving average current $\bar{\imath}_L(t)$ is expressed as

$$\bar{\imath}_L(t) = \frac{1}{k} \cdot \left[\zeta(t, \hat{v}_{in}, k) + 1 - \sqrt{\zeta(t, \hat{v}_{in}, k) \cdot (2 + \zeta(t, \hat{v}_{in}, k))}\right] \tag{9}$$

with

$$\zeta(t, \hat{v}_{in}, k) = \frac{L \cdot f_{sw}}{k} \cdot \left(\frac{1}{\hat{v}_{in} \cdot |\sin(2\pi \cdot f \cdot t)|} - \frac{1}{V_{out}}\right) \tag{10}$$

Fig. 4 depicts the distorted average line current predicted by (9) for different values of k, representing different output load conditions. The distortion will be less severe in a practical converter, as the average value is reduced due to the negative part of $i_L(t)$. Besides this distortion, the converter will still show a high power factor, as shown later in the experimental results section.

It should be mentioned that the introduced distortion is not inherent to the clamp-switch operation method proposed here but would also occur in a DCM working boost converter as PFC if operated with a control scheme according to [9-11]. The selection of a different control scheme, e.g., average current mode control with mains derived reference signal and multiplier, could be used to avoid this distortion.

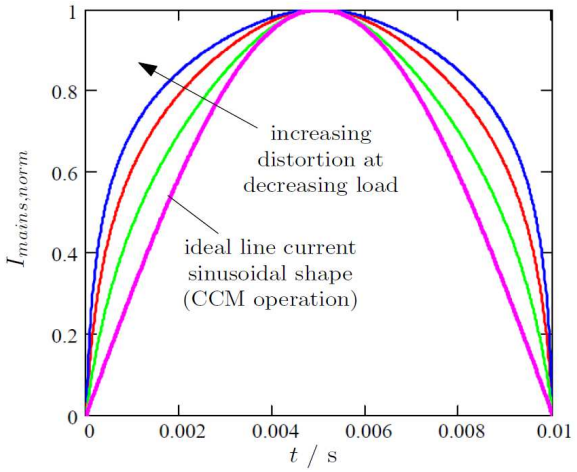

Fig. 4: Normalized estimated line current for different values k for multiplier free PFC control law

Prototype Converter and Experimental Results

For validation a *100* W prototype converter with $V_{out} = 375$ V and $V_{mains} = 230\ V$ ($f = 50\ Hz$) operating at $f_{SW} \approx 240\ kHz$ has been built. The converter employs SiC cascode transistors due to the low stored energy E_{oss} in the output capacitance to reduce switching losses if a ZVS turn-on is not achieved. Some major prototype components are listed in Table 1. The PCB of the power stage is portrayed in Fig. 5; the additional control board, containing the PFC control IC and the wave shaping circuit, is not shown.

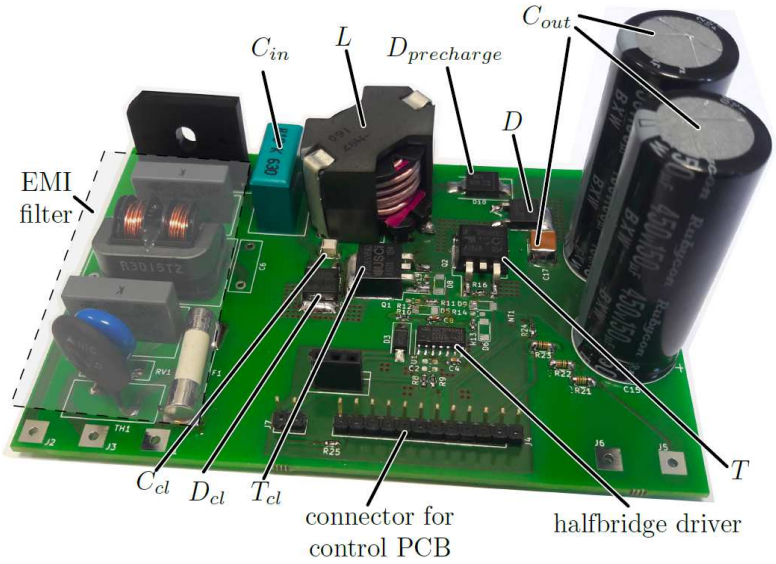

Fig. 5: Prototype PCB without external control board

Table I: Prototype Components

Component	Value and Manufacturer
Transistors T, T_{cl}	SiC FET UF3C065080B3 United SiC/Qorvo
Diodes D,D_{cl}	SiC Schottky Diode C6D04065E Wolfspeed/Cree
Inductor L	custom wound 75 µH core: RM10 material: N87 TDK-EPCOS
Halfbridge driver	2ED21814S06J Infineon
PFC control IC	ICE2PCS01 Infineon
Microcontroller (pulse shaping)	PIC16F1764 Microchip

The measured efficiency, power factor, and THD in the power range from 10 W to 100 W are shown in Fig. 6. The measured efficiency includes the losses in EMI filter and protection devices (i.e., fuse, common mode choke, varistor, inrush-current limiter). It, therefore, presents a realistic estimation of the total power stage losses, but the supply power for the control circuits is not considered.
Fig. 7 and 8 depict measured converter waveforms. On the left side in Fig. 7a) the measured mains current and voltage for an entire line cycle are shown, indicating that although the described line current distortion is visible, a PFC functionality with a high power factor of 0.982 is achieved. Figure 7b) shows the measured voltage across the main transistor T and the inductor current over a line cycle. The current waveform shows that the negative inductor current i_{min} varies over the mains cycle as predicted by Eq. (4). Magnified views of the transistor voltage and the inductor current for three different line voltage values are presented in Fig. 8 to illustrate the operation of the converter during a high-frequency switching cycle depending on the current time instant in the mains cycle. These show that a ZVS at low-line voltages, but for $V_{in} > V_{out}/2$, is achieved (c.f. Fig. 8a) and b)) and that at high line voltages (c.f. Fig. 8c), switching losses are reduced by turning on at the minimum value of v_T. In all cases, the converter is operated at a constant switching frequency, and parasitic ringing in the transistor voltage is reduced due to the clamp-switch operation.
As already mentioned, the ZVS range could be extended by using a larger C_{cl} capacitor (in the actual prototype $C_{cl} = 2.2$ nF), but this would also increase the losses in the clamp-switch network and the inductor, which offsets the effect of the reduced switching losses. Therefore, a ZVS operation for the entire line cycle of the converter could be possible, but a compromise is taken here to optimize the overall system efficiency.

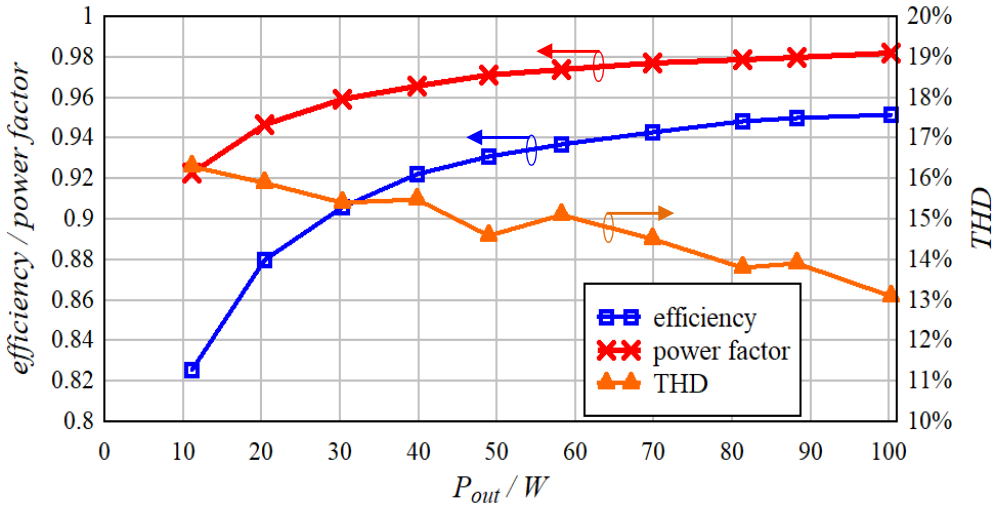

Fig. 6: measured efficiency, power factor and THD vs. P_{out}

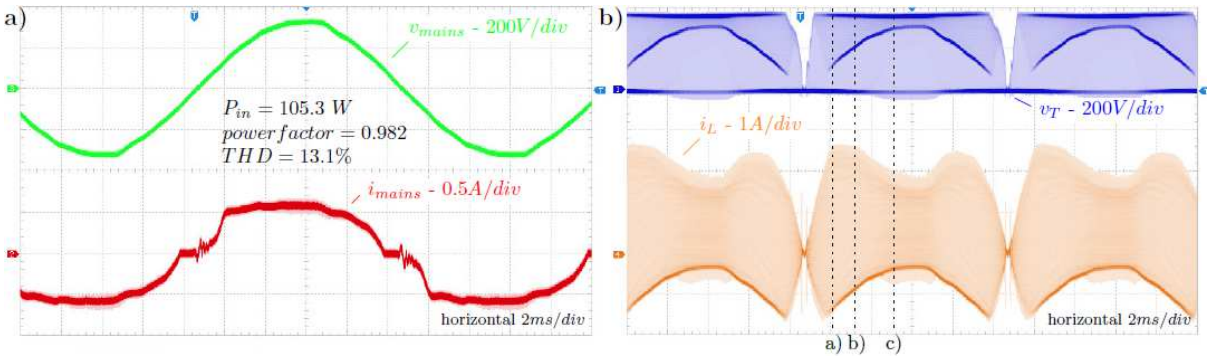

Fig. 7: a) mains voltage v_{mains} and current i_{mains} and b) switch voltage v_T and inductor current i_L over mains cycle

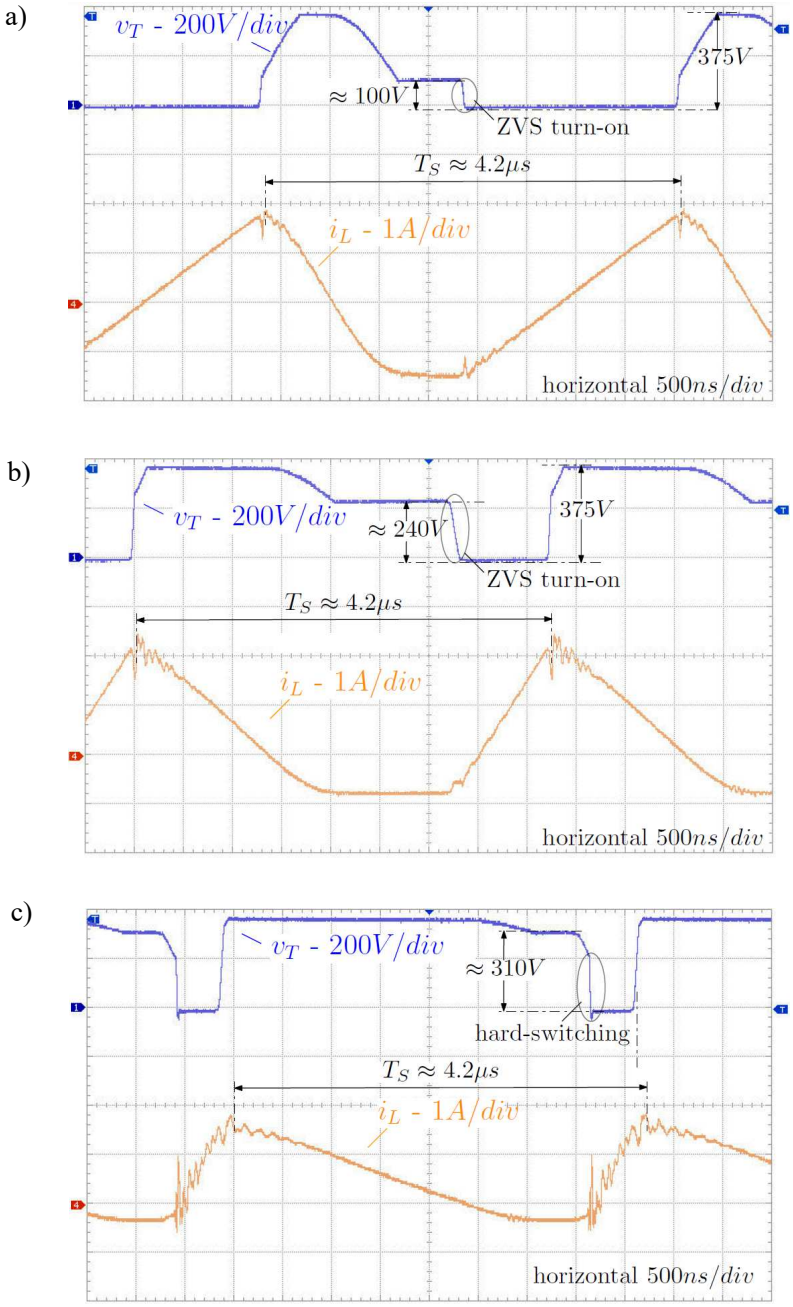

Fig. 8: Detail view of current i_L and voltage v_T for different V_{in} values a) 100 V, b) 240 V and c) 310 V corresponding to the instants marked with a), b) and c) in Fig. 7.

Conclusion

A method is presented to operate a single-phase boost converter PFC at a constant switching frequency to reduce switching losses and achieve ZVS at lower line voltages. The novelty of the approach presented here lies in the combination of the clamp-switch boost operating principle, which does not require any sensor circuitry to achieve reduced switching losses or ZVS with a control circuit based on a standard PFC control IC. This combined approach has not been reported in the literature. Also, it is shown that the multiplier-free approach for average current mode control [9] exhibits line distortions but is still usable in this application. Therefore, a low-cost and straightforward control circuit implementation is possible. The benefit of the proposed method is the utilization of a constant switching frequency and an operation similar to a DCM converter, which leads to a small required inductance value and can also help to ease the design of the inductor and EMI filter components.

Experimental results indicate the approach's feasibility and show that high efficiency and a high power factor at an output power level of 100 W are possible.

Although the implementation used here will introduce some additional line current distortions, this is due to the specific PFC control principle used and not inherent to the presented converter operation. A possible mitigation is using another standard IC for the control law implementation, e.g., an average current control mode PFC IC with input voltage sensing and a multiplier-based control algorithm.

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