A Condition Monitoring Scheme for Semiconductor Devices in Modular Multilevel Converters With Cascaded H-Bridge Submodules

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Keywords

≪Cascaded H-Bridge≫, ≪Condition monitoring≫, ≪Degradation≫, ≪Device characterisation≫, ≪Diagnostics≫, ≪Estimation technique≫, ≪FACTS≫, ≪Modular Multilevel Converters (MMC)≫, ≪Reliability≫. ≪Semiconductor device≫, ≪Thermal model≫

Abstract

In this paper, a novel online semiconductor device monitoring scheme is presented. The condition monitoring (CM) scheme is based on measuring the ON-state voltage drop of semiconductor devices, and tracking the changes in their ON-state resistance. The proposed solution measures the ON-state voltage of semiconductor devices at a controlled and readily measurable temperature. This allows for accurate CM of semiconductors as it decouples temperature related and degradation related changes in the ON-state voltage. The temperature decoupling is achieved using natural switching redundancies available to modular multilevel converter systems. Hence, the proposed CM scheme does not interfere with the output voltages and currents generated by the converter.

Introduction

Modular multilevel converters (MMCs) have long been the preferred topology for high-voltage and high-power grid-connected applications. This is mainly due to their high efficiency, and high quality voltage and current outputs [1–6]. Specifically, static synchronous compensators (STATCOMs) that are based on the cascaded H-bridge modular multilevel converter (CHB-MMC) are proven to be effective in providing stability to the power grid, increasing the overall power quality of the power network, regulating the grid voltage, and in some cases, regulating the grid frequency as well [1, 3, 5, 7, 8].

CHB-MMC STATCOMs utilize a string of series connected submodules to improve the harmonic performance of the output voltage and current, and reduce potential issues caused by electromagnetic interferences. In STATCOM applications, the submodules are typically based on the full-bridge topology to allow operation in all four operating quadrants. Each CHB-MMC submodule is usually equipped with a dc capacitor unit. These dc capacitors are typically in the millifarad range, resulting in stored energy levels in the tens to hundreds of kilojoules [9, 10]. Hence, in case of a semiconductor device failure, the entire energy of the dc link capacitor will discharge in the semiconductors. If left unprotected, the semiconductor modules can explode leading to a catastrophic failure in the submodule [11, 12]. Therefore, having knowledge of the health state of the semiconductors is very valuable, and can help avoid such events. Both the dc capacitor and the semiconductors are subject to high currents, and are prone to thermal degradation. Accurate online condition monitoring (CM) methods for dc capacitors in CHB-MMCs have been addressed in the literature [9, 13]. Additionally, in [14] a general monitoring of semiconductors in MMCs has been presented, where the ON-state collector-emitter voltage ($v_{CE,\mathrm{ON}}$) is used as the monitoring parameter. The study presents a solution for parameter estimation in noisy environments, but does not address the effect of temperature on $v_{CE,\mathrm{ON}}$. In IGBTs, $v_{CE,\mathrm{ON}}$ can vary both as a result of

degradation, and also when subjected to temperature variations. Hence, in order to accurately monitor the condition of semiconductors, these two effects must be decoupled [15]. Temperature-sensitive electrical parameters (TSEP) have shown to accurately estimate the junction temperature of semiconductor devices [16–19]. These methods typically require an initial measurement characterization, and may not be suitable when the device parameters change due to degradation [20]. Although tracking the junction temperature itself is also a suitable method for CM [21], it is complicated to directly measure the junction temperature of semiconductor devices online. Consequently, a more accurate method is needed for decoupling CM parameters from temperature variations.

The ON-state resistance of semiconductors varies as a result of gate-oxide and package-related degradation. On the other hand, changes in the threshold voltage is shown to be mainly a result of gate oxide related issues [21, 22]. Package-related degradation can be in the form of bond wire lift-off, and solder fatigue [23, 24], both of which result in an increased effective resistance of the semiconductors [23–26]. The ON-state voltage drop can be monitored online using added circuitry that isolates the measurement circuit from high voltages when the device is in OFF-state [27]. The measured ON-state resistance can then be extracted from the slope of the $v_{CE} - i_C$ curve using recursive estimation algorithms [23].

In conventional 2-level and 3-level converters, it is difficult to keep the temperature of the semiconductors constant during normal operation of the converter. This is because there are not enough switching redundancies that allow for isolation of specific semiconductors while the converter is in operation. On the contrary, modular multilevel converters exhibit many redundant switching patterns that result in the same modulated voltage. This paper shows how these redundancies enable accurate CM of semiconductors at a known temperature. Although this study focuses on accurate estimation of the ON-state resistance of semiconductors, the proposed solution can be used to measure any other CM parameter of semiconductors at a constant temperature.

System Description

The CM scheme proposed in this paper is mainly intended for CHB-MMC STATCOMs. This family of STATCOMs are offered in various topologies [7, 28, 29]. The common feature in all these topologies is the existence of multiple arms consisting of series-connected full-bridge submodules. The proposed CM algorithm can be implemented on each arm separately. Hence, the proposed solution can be used for all CHB-MMC topologies. In this paper, a single-phase grid-connected STATCOM consisting of only one arm is considered. In STATCOMs there are typically a few redundant submodules per arm in order to continue the operation in case of failure of one or more submodules [30]. Moreover, the full voltage rating of STATCOMs is only needed when they are operating in full capacitive mode of operation. Therefore, in the majority of operational scenarios, a few of the submodules are redundant, which provide redundant switching. Of the many switching redundancies, one simple solution is to temporarily bypass one submodule and operate the converter using the remaining submodules in the system. In this study, this specific redundancy is used to isolate the semiconductor device of interest, and estimate its ON-state resistance online.

This study is conducted on a single-phase STATCOM with full-bridge submodules, as depicted in Fig. 1(a), and with the system parameters summarized in Table I. A simplified schematic diagram of the full-bridge submodule is shown in Fig .1(b), where the parameter s_i, $i \in \{1,2,3,4\}$ represents the switching command of the corresponding switch. Hence, $s_i = 1$ and $s_i = 0$ correspond to the ON-state and OFF-state of the switch s_i, respectively.

STATCOMs can control the voltage at the point of common coupling (PCC) through injection of reactive power [31]. In order to achieve a desired voltage at the PCC, a reference current is injected into the network. The injected current together with the arm inductance define the required voltage that is generated by the converter. This behaviour is summarized in the following Kirchhoff's voltage law (KVL)

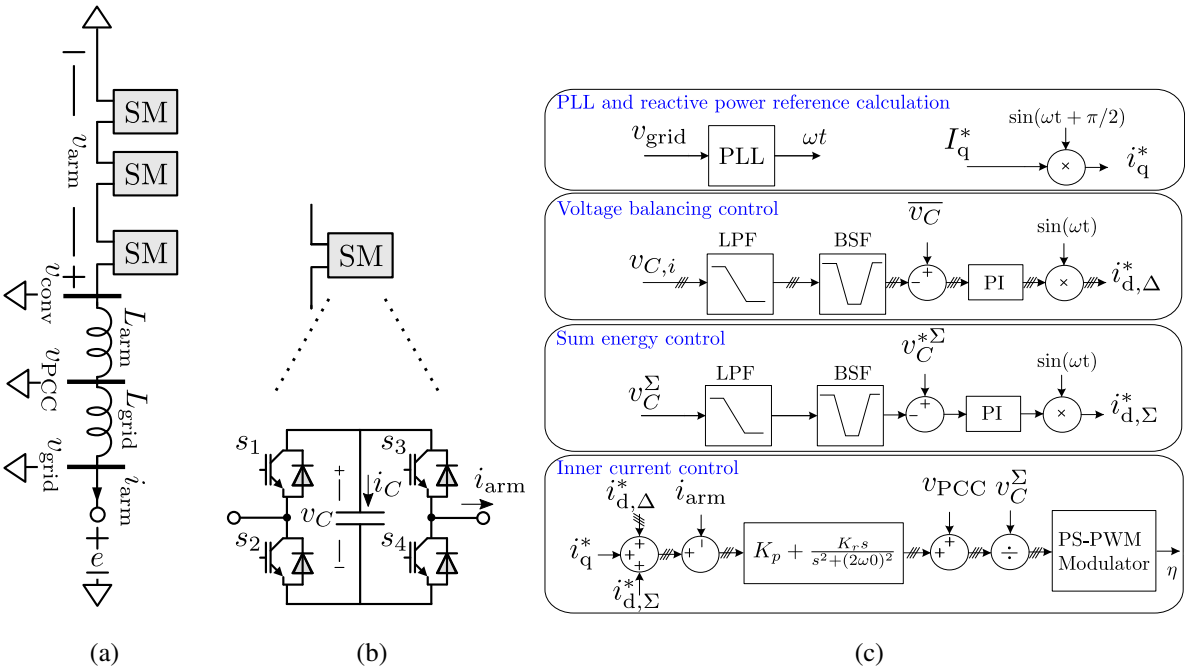
$$v_{\mathrm{PCC}} = v_{\mathrm{conv}} - L_{\mathrm{arm}} \frac{\mathrm{d}i_{\mathrm{arm}}}{\mathrm{d}t} = v_{\mathrm{grid}} + L_{\mathrm{grid}} \frac{\mathrm{d}i_{\mathrm{arm}}}{\mathrm{d}t}, \tag{1}$$

where L_{arm} and i_{arm} represent the arm inductance and arm current, respectively.

Table I: System parameters

Parameter	Symbol	Value	Unit
Nominal power	S_{base}	33	MVA
Nominal arm current (RMS)	i_{base}	0.6	kA
Submodule capacitance	C_{cell}	10	mF
Carrier frequency	f_{c}	87.5	Hz
Number of submodules	N	22	–

The STATCOM shown in Fig. 1(a) is operated in current control mode using a proportional resonant controller as depicted in Fig. 1(c). Moreover, the converter is equipped with an overall energy control using the sum voltage of all submodule dc capacitors. All capacitor voltages are also controlled to their mean value using a voltage balancing control scheme. The modulation scheme used for this study is the phase-shifted pulse width modulation (PS-PWM); however, the proposed method can be used together with any other modulation scheme as well. The parameters opted for this study are based on the 5SNA0800N330100 HiPak module from Hitachi Energy.



(a) (b) (c)

Fig. 1: (a) Single phase CHB-MMC STATCOM. (b) Full-bridge submodule. (c) Closed-loop control system.

Online Condition Monitoring Scheme

The proposed online monitoring scheme is based on online curve tracing of semiconductor devices in CHB-MMCs. The procedure for this curve tracing is as follows:

1. Bypass the selected submodule though (s_1, s_3) or (s_2, s_4) semiconductors.
2. Re-arrange the phase-shifted carriers in the remaining submodules in order to maintain a low total harmonic distortion (THD).
3. Actively discharge the selected submodule to a desired voltage.
4. Bypass the selected submodule through (s_1, s_3) or (s_2, s_4) semiconductors and wait for the non-conducting semiconductor to cool down to a known temperature.
5. Periodically insert the non-conducting semiconductor for short durations.

6. Measure the ON-state voltage during each short ON-state duration.
7. Recharge the submodule to its nominal value.
8. Change the modulation to its initial state where all submodules are actively operated.

These steps are explained in the following subsections.

Submodule Isolation

The PS-PWM scheme in MMCs provides a modulated signal with low harmonic content. In full-bridge MMCs, this low THD is achieved when carrier signals of the submodules are shifted by $180^\circ/N$, where N is the number of submodules in each arm. In order to maintain a low THD, the carriers must be rearranged after a submodule is bypassed. Hence, after bypassing a submodule, the carrier signals of the active submodules are phase shifted by $180^\circ/(N-1)$ instead. In this study, the transition of the carrier phases is done linearly and over a predefined time period of one millisecond.

After bypassing the submodule and rearranging the carrier signals, the junction temperature of its non-conducting switches will cool down to the case temperature of the device in a matter of seconds. This is due to the small thermal capacity of industrial-type semiconductor device modules. Unlike the junction temperature, measuring the case temperature or heat sink temperature is trivial. This is mainly because the heat sink is accessible, and it is not expected to have fast temperature changes. After allowing the junction temperature of the device to settle to the temperature of the heat sink, it is possible to extract its ON-state voltage at a known junction temperature. The proposed procedure for conducting this measurement is to temporarily toggle from one bypass switch group to the other, sample the ON-state voltage, and toggle back to the initial state. For example, if s_4 in Fig. 1(b) is to be monitored, initially the switch group (s_1, s_3) are ON and the switch group (s_2, s_4) are OFF. Then, for the purpose of sampling the ON-state voltage of s_4, (s_1, s_3) are turned OFF and (s_2, s_4) are turned ON for a short period. This procedure is shown in Fig. 2. Repeating this process at different arm current levels allows for online curve tracing of the semiconductor at a known temperature.

After a cell is bypassed, the sum energy and voltage balancing controllers of Fig. 1(c) must be manipulated accordingly. For the sum energy control, the direct voltage of the bypassed cell must be replaced with its reference value in ${v_C}^{\Sigma}$. Moreover, the direct voltage of the bypassed submodule must be replaced with the average voltage of the remaining active submodules in $\overline{v_C}$. These manipulations allow for the active submodules to operate independently from the bypassed submodule.

Although it is possible to conduct the sampling procedure of Fig. 2 when the bypassed submodule is at rated voltage, the switching losses that occur as a result of $v_{CE,\mathrm{ON}}$ sampling can increase the junction temperature and reduce the accuracy of the measurements. Hence, it is beneficial to reduce the submodule voltage prior to sampling $v_{CE,\mathrm{ON}}$. After bypassing, the remaining $N-1$ active submodules are continuously operated in current control mode, while the bypassed submodule can be independently operated. In order to discharge the submodule of interest, it can be temporarily forced to provide a modulated sinusoidal voltage that is 180° out of phase with respect to the arm current. As a result of this modulation, the selected submodule gradually discharges. In order to allow selective conducting and non-conducting switch groups of (s_1, s_3) and (s_2, s_4), complete discharge of the submodule should be avoided.

The temporary discharge operation is shown in Fig. 3, where the capacitor voltage of one selected submodule is lowered actively. The procedure is divided into six phases. In P_1, the submodule of interest is bypassed. During P_2, the submodule is actively discharged. In P_3, the ON-state voltage sampling according to Fig. 2 is conducted. Once the data acquisition is finalized, the submodule is actively recharged in P_4, temporarily bypassed in P_5, and actively operated in normal condition in P_6. It is best to conduct the sampling procedure of Fig. 2 at different current levels. Doing so replicates a similar procedure to how commercial curve tracers extract the $v_{CE} - i_C$ data curves. In order to not heat up the semiconductor during the data acquisition process, it is essential to keep the duration of the sampling pulse short. The length of this pulse can vary depending on the size of the semiconductor module. In this study, a sampling pulse of 50 μs is considered. Once the online data acquisition for the two non-conducting semiconductors is finalized, the function of the upper and lower semiconductors can be switched, and the second set of previously conducting semiconductors can now be curve traced. Applying this method

one submodule at a time allows for accurate online monitoring of semiconductors at readily measurable temperatures.

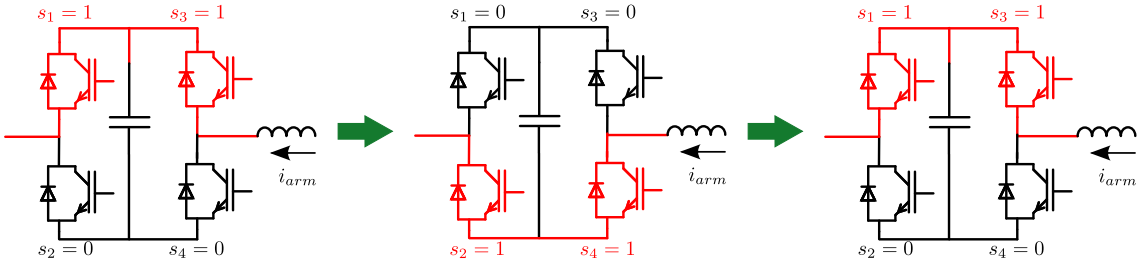


Fig. 2: Procedure for sampling $v_{CE,\mathrm{ON}}$ in a bypassed submodule

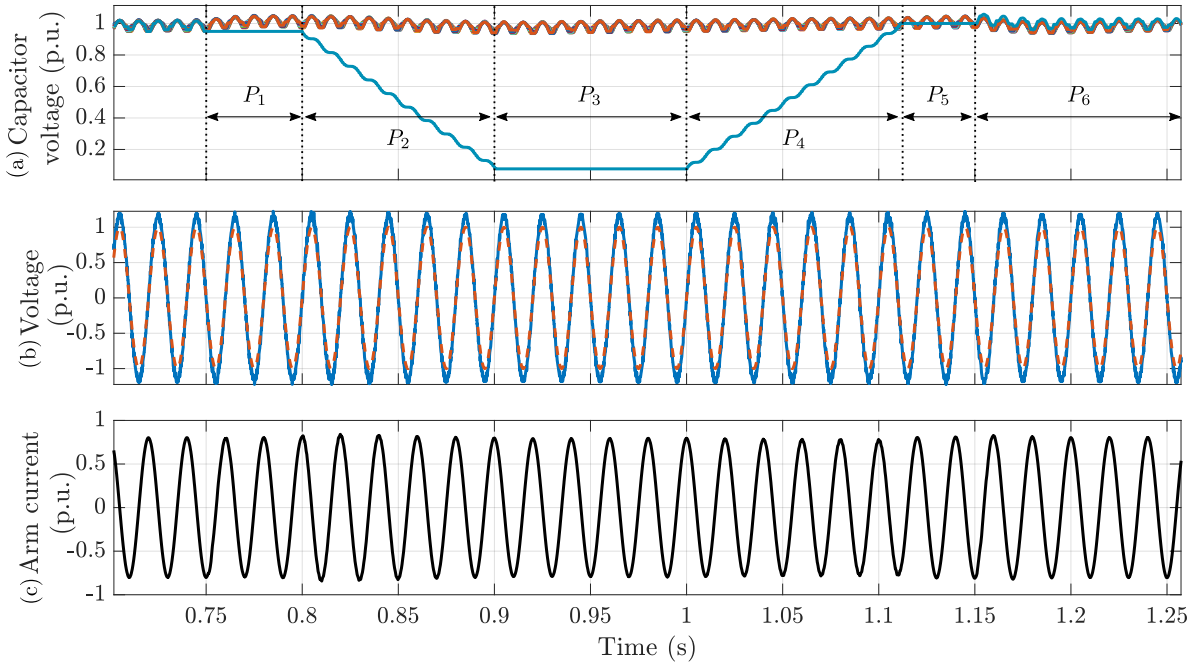


Fig. 3: Selective submodule bypass (P_1), discharge (P_2), sampling (P_3), and recharge (P_4), during normal operation of the converter. a) Capacitor voltages with selected module discharged to 10% nominal value. b) Grid voltage (dashed line) and converter voltage (solid line). c) Arm current of the converter at 0.8 p.u., capacitive.

Loss and Thermal Analysis

In this study, the $v_{CE} - i_C$ curve of the semiconductor is extracted from the data sheet and placed as a lookup table inside the simulation model in MATLAB/Simulink as shown in Fig. 4(a). Hence, the ON-state voltage of each semiconductor module changes in the simulation according to the data sheet parameters. In the simulation model, the semiconductor data are sampled at a predefined frequency. The sampling frequency should not be an integer multiple of the fundamental frequency of the network. With this choice, the ON-state voltages are naturally sampled at different points in the converter's current waveform. As a result, a $v_{CE} - i_C$ curve is traced online. Due to the small duration of the sampling pulse, small power losses are expected in the semiconductor. The losses of the semiconductor under test (SUT) are divided into switching losses and conduction losses. The conduction and switching losses are defined

as

$$P_{\text{cond}}(t,T_j) = v_{CE,\text{ON}}(t,T_j).i_{CE}(t) \tag{2}$$

$$E_{\text{sw}}(t,T_j) = E_{\text{sw}}(T_{j,\text{ref}}, v_{CE,\text{ref}}, i_C).(1+k_{T_1}.(T_j(t)-T_{\text{ref}})).(\frac{v_{CE}}{v_{\text{ref}}})^{k_v}, \tag{3}$$

where k_{T_1} and k_v are extracted from the data sheet [32].

The ON-state voltage $v_{CE,\text{ON}}$ in (2) can be simplified as,

$$v_{CE,\text{ON}}(t,T_j) = v_{CE,0}(1+k_{T_2}.(T_j(t)-T_{\text{ref}})) + r_{CE}(1+k_{T_3}.(T_j(t)-T_{\text{ref}})).i_{CE}(t), \tag{4}$$

where k_{T_2} and k_{T_3} represent the temperature coefficient of the intercept and slope of the $v_{CE}-i_C$ curve, respectively.

According to (3), a lower voltage over the semiconductor results in lower switching losses. This is the main reason for reducing the voltage of the submodule prior to sampling the SUT. Moreover, due to the short period of the sampling instant, the conduction losses are negligible. The conduction and switching losses are implemented in the MATLAB/Simulink simulation environment. In the simulation model, the TSEPs of (2) and (3) are dynamically updated based on their calculated temperature from the previous simulation time step.

The thermal model of the 5SNA0800N330100 IGBT is shown in Fig. 5(a) with parameters summarized in Table II. The thermal model from junction to case is typically provided in the data sheet in the Foster representation. The thermal model and parameters shown in this paper are based on the equivalent Cauer model using the Foster model parameters. A heat sink with a coolant temperature of 25°C is assumed in this study. The coolant temperature is typically higher in practice. Nevertheless, the purpose of this study is to show that the junction temperature does not vary significantly from the initially stabilized coolant temperature as a result of sampling with the proposed method. Consequently, the hypothesis holds regardless of the initial coolant temperature.

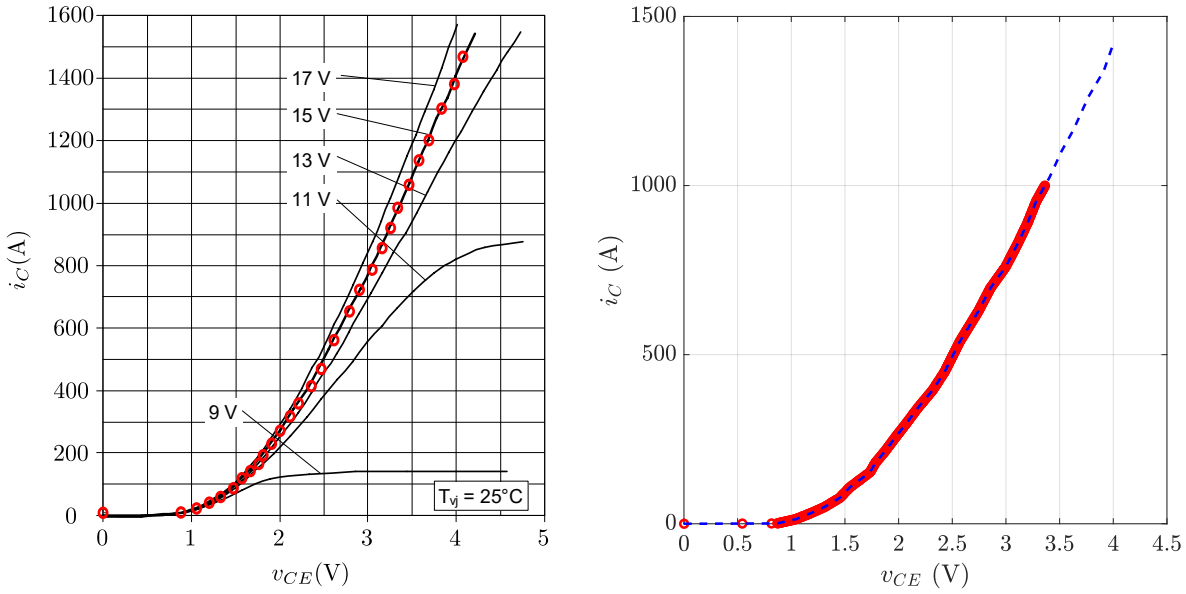
Table II: Thermal model parameters of the 5SNA0800N330100

Symbol	Value	Unit
$R_{th,1}$	2.5	K/kW
$R_{th,2}$	4.7	K/kW
$R_{th,3}$	1.9	K/kW
$R_{th,4}$	0.7	K/kW
$C_{th,1}$	1.8	J/K
$C_{th,2}$	9.5	J/K
$C_{th,3}$	192	J/K
$C_{th,4}$	4913	J/K

Simulation results in Fig. 5(b) reveal that for a sampling pulse duration of 50 μs, and a sampling frequency of 10.37 Hz, the increase in semiconductor chip temperature is negligible. Hence, it can be assumed that all sampled points are achieved at a fixed temperature of the semiconductor's heat sink. The sampled voltage and current data can then be used to identify the $v_{CE}-i_C$ curve of each semiconductor online. This is shown in Fig. 4(b). In this simulation, the effect of noise is omitted; however, in the presence of large noise levels, it is possible to fit a linear curve to the resistive part of the $v_{CE}-i_C$ curve and extract the ON-state resistance of the device [14].

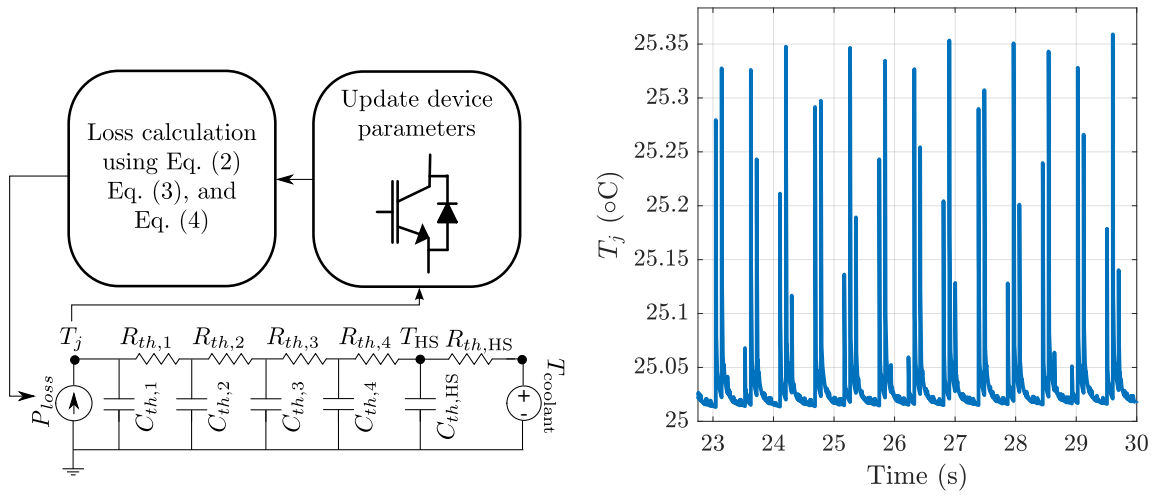
Conclusion

In this paper, a novel method of online health monitoring of semiconductors in CHB-MMCs is presented. The proposed method has the advantage of curve tracing semiconductors at a known and easily



(a) (b)

Fig. 4: (a) $v_{CE} - i_C$ characteristics of 5SNA0800N330100 extracted from the datasheet (b) $v_{CE} - i_C$ characteristics of 5SNA0800N330100 at VGE = 15 V, and T_j = 25 °C from datasheet (blue) and through online estimation (red).



(a) (b)

Fig. 5: (a) Thermal model of 5SNA0800N330100. (b) Semiconductor junction temperature variations when a peak arm current of 1 kA, a reduced submodule voltage of 200 V, a sampling frequency of 10.37 Hz, and a sampling period of 50 μs is considered.

measurable temperature. Therefore, variations in the ON-state resistance of semiconductors caused by degradation can be separated from that caused by temperature variations. Although the proposed method has been investigated for CHB-MMCs in STATCOM applications, it can be applied to all MMC-based topologies that comprise full-bridge submodules.

References

[1] S. Sirisukprasert, A. Huang, and J.-S. Lai, "Modeling, analysis and control of cascaded-multilevel converter-based STATCOM," in *IEEE Power Engineering Society General Meeting*, vol. 4, 2003, pp. 2561–2568.

[2] F. Peng and J. Wang, "A universal STATCOM with delta-connected cascade multilevel inverter," in *IEEE 35th Annual Power Electronics Specialists Conference*, vol. 5, 2004, pp. 3529–3533.

[3] F. Z. Peng and Jin Wang, "A universal STATCOM with delta-connected cascade multilevel inverter," in *IEEE 35th Annual Power Electronics Specialists Conference*, vol. 5, 2004, pp. 3529–3533.

[4] S. Chou, B. Wang, S. Chen, C. Lee, P. Cheng, H. Akagi, and P. Barbosa, "Average power balancing control of a STATCOM based on the cascaded H-bridge PWM converter with star configuration," in *IEEE Energy Conversion Congress and Exposition*, 2013, pp. 970–977.

[5] N. Thitichaiworakorn, M. Hagiwara, and H. Akagi, "Experimental verification of a modular multilevel cascade inverter based on double-star bridge cells," *IEEE Trans. Ind. App.*, vol. 50, no. 1, pp. 509–519, Jan.-Feb. 2014.

[6] S. Sinsel, I. Ramsay, W. Hörger, A. Janke, and M. A. Alegria, "Multilevel STATCOMs — a new converter topology that opens up the market," in *IEEE PES T&D Conference and Exposition*, 2014, pp. 1–5.

[7] T. Soong and P. W. Lehn, "Evaluation of emerging modular multilevel converters for BESS applications," *IEEE Trans. Power Deliv.*, vol. 29, no. 5, pp. 2086–2094, Oct. 2014.

[8] ——, "Control of energy storage enabled modular multilevel converters with reduced storage requirements," in *15th Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2014, pp. 1–7.

[9] M. Asoodar, M. Nahalparvari, C. Danielsson, R. Söderström, and H.-P. Nee, "Online health monitoring of dc-link capacitors in modular multilevel converters for FACTS and HVDC applications," *IEEE Trans. Power Electron.*, vol. 36, no. 12, pp. 13 489–13 503, Dec. 2021.

[10] K. Ilves, S. Norrga, L. Harnefors, and H.-P. Nee, "On energy storage requirements in modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 77–88, Jan. 2014.

[11] D. Li, F. Qi, M. Packwood, A. Islam, L. Coulbeck, X. Li, Y. Wang, H. Luo, X. Dai, and G. Liu, "Explosion mechanism investigation of high power IGBT module," in *19th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE)*, 2018, pp. 1–5.

[12] M. Billmann, D. Malipaard, and H. Gambach, "Explosion proof housings for IGBT module based high power inverters in HVDC transmission application," in *Proc. PCIM Eur. Conf., Nuremberg*, 2009, pp. 352–257.

[13] C. Liu, F. Deng, Q. Yu, Y. Wang, F. Blaabjerg, and X. Cai, "Submodule capacitance monitoring strategy for phase-shifted carrier pulsewidth-modulation-based modular multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 68, no. 9, pp. 8753–8767, Sep. 2021.

[14] S. Chen, S. Ji, L. Pan, C. Liu, and L. Zhu, "An on-state voltage calculation scheme of MMC submodule IGBT," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7996–8007, Aug. 2019.

[15] V. Smet, F. Forest, J.-J. Huselstein, A. Rashed, and F. Richardeau, "Evaluation of V_{ce} monitoring as a real-time method to estimate aging of bond wire-IGBT modules stressed by power cycling," *IEEE Trans. Ind. Electron.*, vol. 60, no. 7, pp. 2760–2770, Jul. 2013.

[16] H. Luo, W. Li, F. Iannuzzo, X. He, and F. Blaabjerg, "Enabling junction temperature estimation via collector-side thermo-sensitive electrical parameters through emitter stray inductance in high-power IGBT modules," *IEEE Trans. Ind. Electron.*, vol. 65, no. 6, pp. 4724–4738, Jun. 2018.

[17] N. Baker, S. Munk-Nielsen, F. Iannuzzo, and M. Liserre, "IGBT junction temperature measurement via peak gate current," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3784–3793, May 2016.

[18] Y. Avenas, L. Dupont, and Z. Khatir, "Temperature measurement of power semiconductor devices by thermo-sensitive electrical parameters—a review," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 3081–3092, Jun. 2012.

[19] V. Sundaramoorthy, E. Bianda, R. Bloch, D. Angelosante, I. Nistor, G. Riedel, F. Zurfluh, G. Knapp, and A. Heinemann, "A study on IGBT junction temperature (Tj) online estimation using gate-emitter voltage (Vge) at turn-off," *Microelectron. Rel.*, vol. 54, no. 11, pp. 2423–2431, Nov. 2014.

[20] F. Yang, E. Ugur, and B. Akin, "Evaluation of aging's effect on temperature-sensitive electrical parameters in SiC MOSFETs," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 6315–6331, Jun. 2020.

[21] H. Oh, B. Han, P. McCluskey, C. Han, and B. D. Youn, "Physics-of-failure, condition monitoring, and prognostics of insulated gate bipolar transistor modules: A review," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2413–2426, May 2015.

[22] E. Ugur, C. Xu, F. Yang, S. Pu, and B. Akin, "A new complete condition monitoring method for SiC power MOSFETs," *IEEE Trans. Ind. Electron.*, vol. 68, no. 2, pp. 1654–1664, Feb. 2021.

[23] M. A. Eleffendi and C. M. Johnson, "In-service diagnostics for wire-bond lift-off and solder fatigue of power semiconductor packages," *IEEE Trans. Power Electron.*, vol. 32, no. 9, pp. 7187–7198, Sep. 2017.

[24] G. J. Riedel and M. Valov, "Simultaneous testing of wirebond and solder fatigue in IGBT modules," in *8th International Conference on Integrated Power Electronics Systems*, 2014, pp. 1–5.

[25] U.-M. Choi, F. Blaabjerg, S. Jørgensen, S. Munk-Nielsen, and B. Rannestad, "Reliability improvement of power converters by means of condition monitoring of IGBT modules," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7990–7997, Oct 2017.

[26] J. M. Anderson and R. W. Cox, "On-line condition monitoring for MOSFET and IGBT switches in digitally controlled drives," in *IEEE Energy Conversion Congress and Exposition*, 2011, pp. 3920–3927.

[27] Y. Peng and H. Wang, "A comparative study on converter-level on-state voltage measurement circuits for power semiconductor devices," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2021, pp. 3638–3643.

[28] P.-H. Wu, H.-C. Chen, Y.-T. Chang, and P.-T. Cheng, "Delta-connected cascaded H-bridge converter application in unbalanced load compensation," *IEEE Trans. Ind. App.*, vol. 53, no. 2, pp. 1254–1262, Nov. 2017.

[29] C. D. Townsend, R. A. Baraciarte, Y. Yu, D. Tormo, H. Z. de La Parra, G. D. Demetriades, and V. G. Agelidis, "Heuristic model predictive modulation for high-power cascaded multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 63, no. 8, pp. 5263–5275, Aug. 2016.

[30] W. Song and A. Q. Huang, "Fault-tolerant design and control strategy for cascaded H-Bridge multilevel converter-based STATCOM," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2700–2708, Aug. 2010.

[31] M. Nahalparvari, M. Asoodar, L. Bessegato, S. Norrga, and H.-P. Nee, "Modeling and shaping of the dc-side admittance of a modular multilevel converter under closed-loop voltage control," *IEEE Trans. Power Electron.*, vol. 36, no. 6, pp. 7294–7306, Jun. 2021.

[32] Y. Zhang, H. Wang, Z. Wang, Y. Yang, and F. Blaabjerg, "Simplified thermal modeling for IGBT modules with periodic power loss profiles in modular multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 66, no. 3, pp. 2323–2332, Mar. 2019.