# Boost-SEPIC Interleaved PFC Converter

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***Abstract*—This paper proposes a new power factor correction (PFC) converter based on the boost-SEPIC interleaved (BSI) structure. The inductor current of conventional interleaved boost PFC (IB-PFC) can easily become unbalanced due to the tolerance of components. The proposed PFC converter allows operation with the automatic balancing of phase currents without the complex balancing methods. This is achieved by the interleaved structure that combines boost and SEPIC circuits. Only one current sensor is required to control the input current of the PFC, reducing the complexity of hardware and increasing the reliability of the circuit. Moreover, with high voltage gain and low voltage stress on semiconductor devices, the proposed PFC converter can achieve higher efficiency than conventional IB-PFC. The above advantages make the proposed structure an attractive solution with practical PFC applications. A 1.6 *kW* prototype was built to evaluate the performance of the proposed converter.**

***Index Terms*—boost-SEPIC interleaved converter, current balancing, interleaved boost, power factor correction.**

## I. INTRODUCTION

PFC is an important application of power electronic converters; it allows the input current of electronic devices to repeat the shape of the input voltage with low harmonics and unity power factor, thereby improving the performance and quality of the power system [1]. Traditional rectifier circuits consist of a diode bridge and filter capacitor causing a problem known as current distortion. A dc-dc converter is added between the rectifier bridge and dc capacitor forming the typical structure of a PFC converter. By controlling the operation of the dc-dc converter, the input current of the rectifier can be adjusted to achieve the unity power factor, and the dc output voltage on the capacitor is also regulated [2]. Among many dc-dc converters for PFC, the interleaved boost converter is the commonly used topology with advantages such as simple structure, high power capability, reduced input current ripple, small EMI filter size, reduced current stress for switches [3], [4], [5]. Fig. 1 illustrates the power stage of an interleaved boost PFC converter (IB-PFC).

Under ideal conditions, the average current of phases equals 1/N times the input current, where N is the number of phases. However, due to various reasons, such as the manufacturing tolerance of components or aging over time, the inductor currents of IB-PFC are not balanced [3], [6], [7], [8]. Since the total current remains constant, any unbalancing of current results in one of the phases having

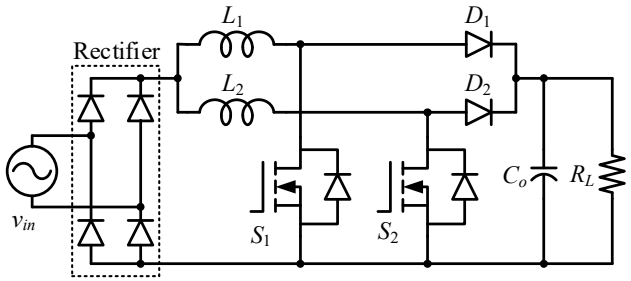


Fig. 1. Interleaved boost PFC converter (IB-PFC).

to operate under more severe conditions than designed, with greater losses, causing overheating on the components of that phase, reducing the reliability and lifespan of the circuit.

To overcome this problem, instead of only focusing on the total input current, the current of each phase is sensed and controlled through a separate current sensor [9], [10], [11], [7]. This approach requires the use of multiple sensors and controllers, and furthermore, it is difficult to sense the current of each phase by using a shunt resistor connected to the low-side, so high-side current sensors with higher cost need to be used. Some solutions have been proposed in the literature to reduce the number of current sensors or eliminate the need for current sensors [3], [7], [12]. In general, these works all require complex calculations and/or accurate models of the converter, which decreases the reliability of the circuit and makes it difficult to implement on a large scale in commercial products.

Another approach is to use converters based on the series capacitor structure that has the ability to automatic balancing the currents [13], [14]. However, the limitation is that when the duty ratio drops below 0.5, the current through inductors is no longer balanced. The asymmetric PWM method allows the operating range of series capacitor-based structures to be extended, with the current balancing characteristic maintained throughout the operating range of the circuit [15], [16], [17].

All the switching devices of IB-PFC must withstand a high output voltage, with a large duty ratio, especially at a low input voltage. It makes the converter cannot achieve high efficiency. To address this, many high-gain boost topologies have been introduced in [18], [13].

Based on the boost-SEPIC interleaved structure (formerly named as the modified double-dual-boost converter) in [19], this paper presents a boost-SEPIC

interleaved PFC converter (BSI-PFC) with the characteristic of automatic balancing of inductor currents over the entire operating range. Therefore, only one current sensor is required to control the input current of the PFC without encountering current balancing issues as with conventional interleaved boost circuits, while the current controller is still maintained. This helps to increase the reliability, as well as the potential for practical application of the proposed structure. Moreover, the proposed BSI-PFC converter has high voltage gain with draws lower voltage stress on switching devices, making the conversion performance of the converter improved compared to the IB-PFC. Although the BSI-PFC circuit requires three inductors $L_1$, $L_2$, and $L_3$, the inductors $L_2$ and $L_3$ can be integrated into a single inductor $L_{23}$, there is no increase in magnetic volume.

Section II presents the operation and characteristics of the BSI-PFC converter; the control structure of the proposed PFC is also discussed in this section. Thereafter the experimental results of a 1.6 *kW* prototype of the BSI-PFC converter are presented in Section III. Finally, conclusions are drawn in Section IV.

## II. BSI-PFC Converter

### *A. Proposed structure and principle of operation*

The power stage of the proposed BSI-PFC converter is shown in Fig. 2. It consists of a diode bridge rectifying the ac input voltage $v_{in}$ to the dc voltage $v_{rec} = |v_{in}|$, followed by the boost-SEPIC interleaved converter [19], which again converts $v_{rec}$ into the dc output voltage $V_o$ to supply the load $R_L$. In the circuit, the $L_1$, $S_1$, $D_1$, and $C_1$ form the boost part of the converter, while the SEPIC part includes $L_2$, $S_2$, $C_2$, $L_3$, and $D_2$. With $L_1$, $L_2$ are input inductors, switches $S_1$, $S_2$ operate out of phase by 180° creating the interleaving effect of input current. In addition, to reduce the volume of the converter, $L_2$ and $L_3$ are coupled into a single magnetics core $L_{23}$.

Since the switching frequency is much higher than the grid frequency, it is assumed that during a switching period, the dc voltage after the rectifier is constant $v_{rec} = V_{rec}$ (pseudo-static assumption). Therefore, it is possible to analyze the operation of the circuit as a dc-dc converter.

The working principle of the proposed BSI-PFC is a combination of boost and SEPIC converters with four modes. Figs. 3 and 4 depict the working states and major waveforms of the converter in a switching period.

*Mode 0:* Fig. 3(a), ($S_1$, $S_2$) are ON, ($D_1$, $D_2$) are OFF. Capacitor $C_1$ is discharged, along with that capacitor $C_2$ is charged through the same path $C_1$–$L_3$–$C_2$–$S_2$.

*Mode 1:* Fig. 3(b) ($S_1$, $D_2$) are ON, ($S_2$, $D_1$) are OFF. Both capacitors $C_1$ and $C_2$ discharge through the path $C_1$–$L_3$–$D_2$–$V_o$ and $C_2$–$D_2$–$V_o$–$V_{rec}$–$L_2$, respectively.

*Mode 2:* Fig. 3(c) ($D_1$, $D_2$) are ON, ($S_1$, $S_2$) are OFF. Capacitor $C_1$ is charged by $L_1$ through the path $C_1$–$V_{rec}$–$L_1$–$D_1$, and $C_2$ is discharged through the path $C_2$–$D_2$–$V_o$–$V_{rec}$–$L_2$.

*Mode 3:* Fig. 3(d) ($S_2$, $D_1$) are ON, ($S_1$, $D_2$) are OFF. $C_1$ is charged through the path $C_1$–$V_{rec}$–$L_1$–$D_1$, and $C_2$ is charged through the path $C_2$–$S_2$–$V_{rec}$–$L_1$–$D_1$–$L_3$.

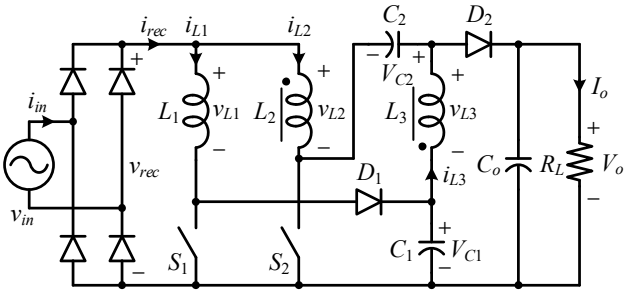


Fig. 2. Proposed BSI-PFC converter.

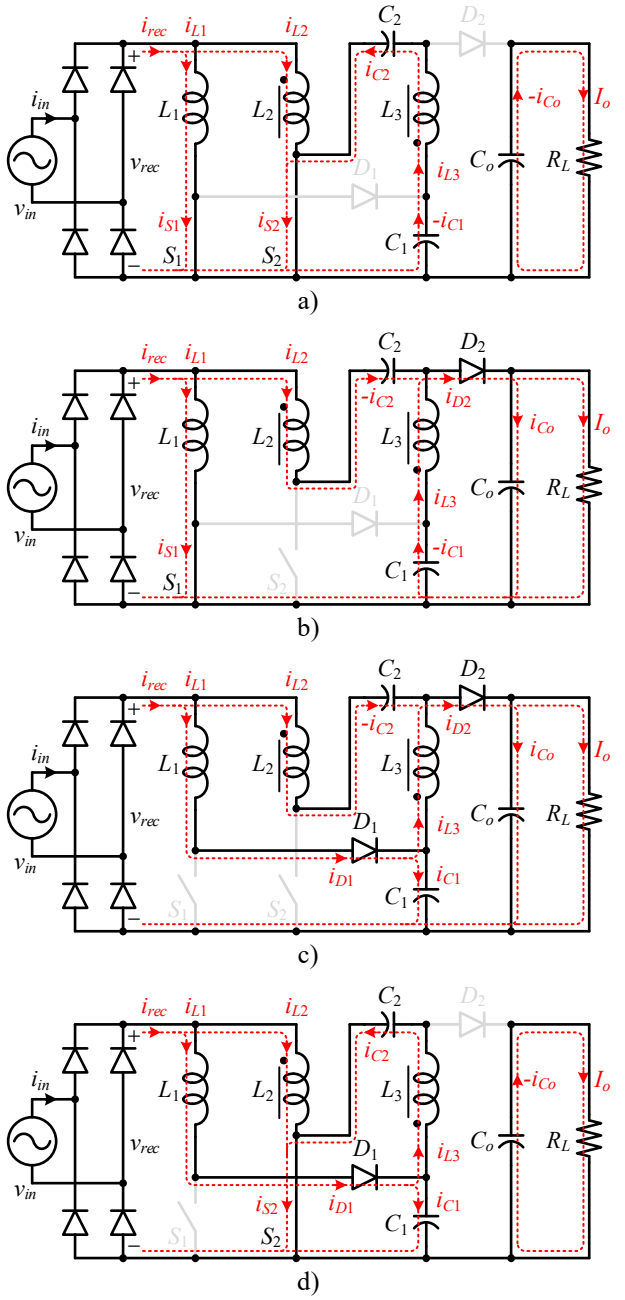


Fig. 3. Operation of the proposed BSI-PFC converter. (a) Mode 0. (b) Mode 1. (c) Mode 2. (d) Mode 3.

*B. Automatic balancing of the inductor current*

One of the most outstanding features of the BSI-PFC converter is the ability to automatic (or self) balancing of the currents among three inductors, which is especially useful in practical applications. From the waveform of the current through capacitor $C_1$ in Fig. 4, applying the principle of charge balance on the capacitor in a switching cycle:

$$\begin{aligned} I_{L3}DT_s &= (I_{L1}-I_{L3})(1-D)T_s \\ I_{L1} &= \frac{1}{1-D}I_{L3} \end{aligned} \tag{1}$$

Applying the same principle to capacitor $C_2$:

$$\begin{aligned} I_{L3}DT_s &= I_{L2}(1-D)T_s \\ I_{L2} &= \frac{D}{1-D}I_{L3} \end{aligned} \tag{2}$$

Thus, the average current through inductors is given by:

$$I_{L2} = DI_{L1} \tag{3}$$

$$I_{L1} = \frac{I_{rec}}{1+D},\ I_{L2} = \frac{DI_{rec}}{1+D},\ I_{L3} = \frac{(1-D)I_{rec}}{1+D} \tag{4}$$

Equations (3), (4) show that the average current of two input inductors is automatically distributed depending on the value of duty ratio $D$. In other words, unlike interleaved boost circuit, dedicated current balancing control is not necessary for the proposed BSI-PFC converter. The consequence is that only controlling the input current of the PFC $i_{rec}$ is required, without the need for a current control loop of each phase, thus reducing the number of current sensors to one sensor and the complexity of the controller.

The current balancing mechanism can be explained as follows: capacitor $C_2$ acts as a blocking capacitor, which automatically balances the average current of inductors $L_2$ and $L_3$ according to the relationship in (2). On the other hand, the current $I_{L3}$ acts as the load of the boost part of the circuit, so the relationship between $I_{L1}$ and $I_{L3}$ is ensured by (1). Therefore, although interleaved, the phases are not connected in parallel as in the interleaved boost structure but in a cascade form, ensuring current balance in the circuit.

*C. Voltage gain and voltage stress*

From the inductor voltage waveforms of the three inductors shown in Fig. 4, the output and capacitor voltages of the BSI-PFC converter can be calculated by applying the flux (volt-sec) balance condition:

$$V_o = \frac{(1+D)V_{rec}}{1-D},\ V_{C1} = \frac{V_o}{1+D},\ V_{C2} = \frac{DV_o}{1+D} \tag{5}$$

As shown in Fig. 5, the voltage gain of the BSI-PFC converter is higher than that of the IB-PFC. Thus, under the same conversion ratio, the latter must operate at a higher duty cycle than the former. It is well known that the

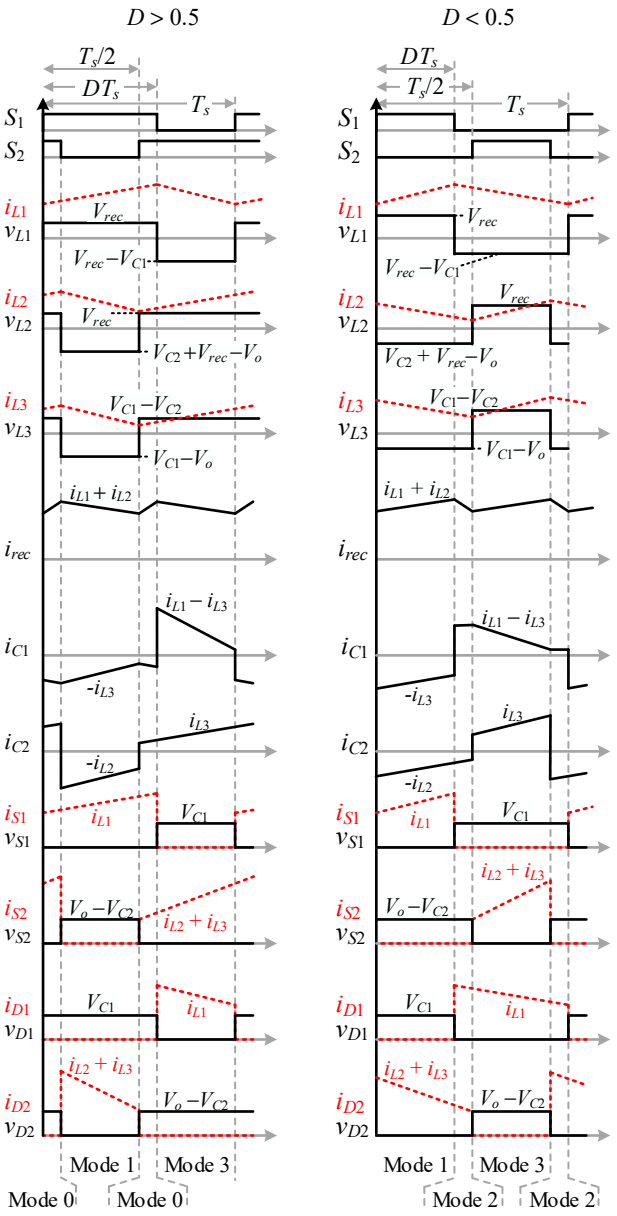


Fig. 4. Key waveforms of the proposed BSI-PFC converter.

conduction loss of a boost-type converter increases when the duty cycle increases. Moreover, from (5) and the voltage waveforms on semiconductor devices shown in Fig. 4, the voltage stresses on switches and diodes are expressed as $V_o/(1 + D)$. Compared with the voltage stress in the IB-PFC, which is always fixed at $V_o$, the reduced voltage stress of devices in the BSI-PFC converter makes the switching losses of switches and diodes can be reduced. Therefore, the efficiency of the proposed PFC is improved compared to the IB-PFC.

The main characteristics of the proposed BSI-PFC are summarized in Table I.

*D. Control of BSI-PFC converter*

In this section, the control design of PFC based on the proposed power stage will be discussed. The control diagram is shown in Fig. 6. It is similar to conventional

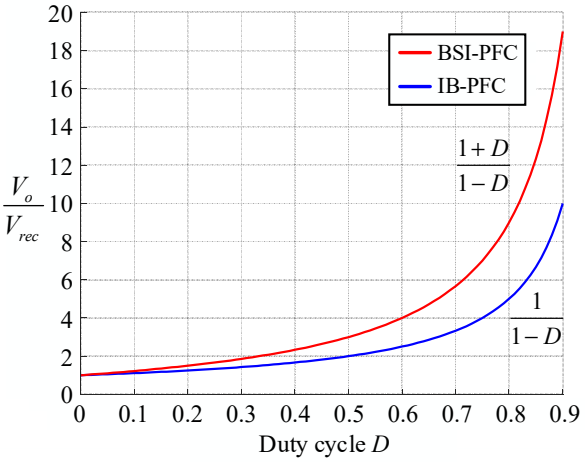


Fig. 5. Voltage gains of the IB-PFC and the proposed BSI-PFC converters.

TABLE I
CHARACTERISTICS OF THE BSI-PFC CONVERTER

| Symbol | Value |
|---|---|
| Voltage gain ($V_o/V_{rec}$) | $(1+D)/(1-D)$ |
| Self balancing of inductor current | Yes |
| $I_{L1}$ | $I_{rec}/(1+D)$ |
| $I_{L2}$ | $DI_{rec}/(1+D)$ |
| $I_{L3}$ | $(1-D)I_{rec}/(1+D)$ |
| $V_{C1}$ | $V_o/(1+D)$ |
| $V_{C2}$ | $DV_o/(1+D)$ |
| Voltage stress ($S_1$, $S_2$, $D_1$, $D_2$) | $V_o/(1+D)$ |
| Current stress ($S_1$, $S_2$, $D_1$, $D_2$) | $I_{rec}/(1-D)$ |

PFCs [1] with two control loops: the current loop and the voltage loop.

The rectifier current $i_{rec}$ is sensed by a current sensing network and compared with the reference current signal $i_{ref}$. The current controller generates interleaved signals for switches $S_1$ and $S_2$ (through PWM and gate drivers) so that the $i_{rec}$ follows $i_{ref}$ without error. On the other hand, the reference signal for the inner current loop is semi-sinusoidal, in phase with the rectifier voltage $v_{rec}$, and with an amplitude that depends on the required power of the circuit. Therefore, the input current $i_{in}$ is sinusoidal and in phase with the input voltage $v_{in}$, the input to the converter will appear to be resistive with unity power factor. The current compensator is given in (6), it is a PI-type controller with a zero placed at or near the crossover frequency of current loop gain, which boosts the phase of the system, thereby increasing the phase margin of the current loop, guaranteeing the stability of the system when there is a fluctuation in the transfer function due to the change of the operating point:

$$C_I(s)=\frac{K_I\left(1+s/\omega_{zi}\right)}{s\left(1+s/\omega_{pi}\right)} \tag{6}$$

The outer voltage loop regulates the output voltage of

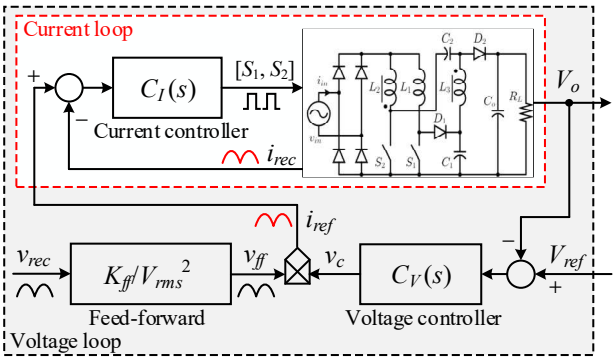


Fig. 6. Control structure of the proposed BSI-PFC converter.

PFC $V_o$ at the pre-determined value $V_{ref}$ by adjusting the magnitude of the current reference signal. The feed-forward is added to accelerate the response of PFC. When the input voltage increases, by dividing by the square of the average rectifier voltage, the product of the feed-forward signal $v_{ff}$ and the output of the voltage controller $v_C$ reduces, and thereby the input current is reduced proportional to the increment of voltage, keeping the input power constant. It is assumed that the dynamic of the voltage loop is slow enough compared to the current loop, with a bandwidth less than half of the grid frequency. It is possible to design two control loops separately, the voltage controller has the form [1]:

$$C_V(s)=\frac{K_v}{1+s/\omega_{pv}} \tag{7}$$

The current loop should run at a much faster rate than the voltage loop. The bandwidth of the current compensator should be higher than twice of the input frequency to correctly track the semi-sinusoidal waveform. Usually, the bandwidth of the current compensator is selected at about 1/10 of the switching frequency. The inner current loop with a fast dynamic maintains the sinusoidal input current at desired amplitude. The outer voltage loop regulates the output voltage of PFC at a pre-determined value.

## III. EXPERIMENTAL RESULTS

To verify the above theoretical analyses of the proposed BSI-PFC converter, a laboratory prototype is constructed and tested. Fig. 7 shows the 1.6 *kW* hardware prototype, the input ac voltage ranges from 120 – 250 $V_{rms}$, output dc voltage is regulated at 390 *V*. The circuit components and specifications are listed in Table II. The inductor $L_1$ was built by using the PQ5050 core. The inductors $L_2$ and $L_3$ are integrated into a single coupled inductor $L_{23}$ and it also uses the same core. The algorithm for two control loops of the converter, PWM modulation, and data acquisition are implemented on a DSP using the development board LAUNCHXL-F280049C (Texas Instruments).

The experimental results are shown in Figs. 8 – 11 ($V_{in}$ = 220 $V_{rms}$/60 *Hz*, $V_o$ = 390 *V*, $P_o$ = 1.6 *kW*). Fig. 8 shows the performance of the proposed PFC with the waveforms

TABLE II
CIRCUIT PARAMETERS

| Symbol | Value | Symbol | Value |
|---|---|---|---|
| $V_{in}$ | 120~250 $V_{rms}$ | $C_1$, $C_2$ | 2 $\mu F$ |
| $f_{grid}$ | 60 $Hz$ | $L_1$, $L_2$, $L_3$ | 420, 240, 240 $\mu H$ |
| $V_o$ | 390 $V$ | $C_o$ | 990 $\mu F$ |
| $P_o$ | 1.6 $kW$ | $S_1$, $S_2$ | IPW60R040C7 |
| $f_{sw}$ | 50 $kHz$ | $D_1$, $D_2$ | RHRG3060 |

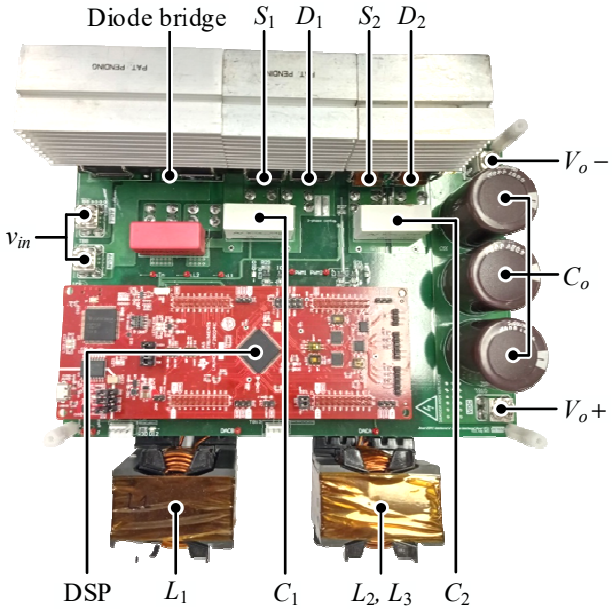


Fig. 7. Prototype photo of the proposed BSI-PFC converter.

of the input voltage $v_{in}$, input current $i_{in}$, and output voltage $V_o$. As can be seen, the input current of the BSI-PFC follows in phase and uniform with the sinusoidal grid voltage, thus making the power factor of the circuit near to unity. This shows that the current controller has a good performance even with only one current sensor. Similarly, the output voltage is well regulated at the fixed value of 390 $V$.

The current of the inductors ($i_{L1}$, $i_{L2}$, $i_{L3}$) are shown in Fig. 9. They follow the semi-sinusoidal waveform of the rectifier current $i_{rec}$. Although only the rectifier current $i_{rec}$ ($i_{rec} = i_{L1} + i_{L2}$) is sensed and controlled by the current controller, the relationship ($i_{L2} = Di_{L1}$) between inductor currents is still maintained. In other words, the ability of self balancing of inductor currents is guaranteed during a cycle of the grid.

The voltage stress on switches is given in Fig. 10. While the output voltage is fixed at 390 $V$, the stress on the switch is always less than the output voltage, and it is greatly reduced at the zero-crossing of grid voltage.

As shown in Fig. 11, the peak efficiency of the proposed PFC is 98 % at ($V_{in}$ = 220 $V_{rms}$, $P_o$ = 1400 $W$). When the proposed PFC operates with $V_{in}$ = 120 $V_{rms}$, the highest efficiency is about 96.8 % at $P_o$ = 1000 $W$. Compared to the IB-PFC, the efficiency of the proposed one is significantly improved at low-line input voltage.

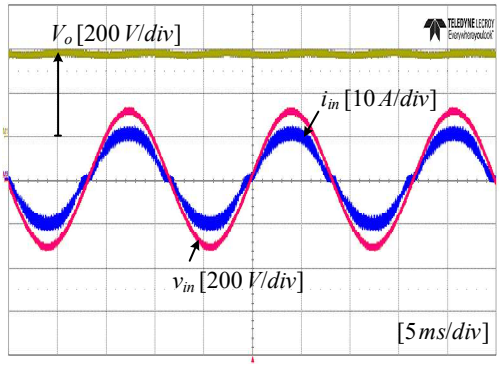


Fig. 8. Experimental waveforms ($V_o$, $v_{in}$, $i_{in}$).

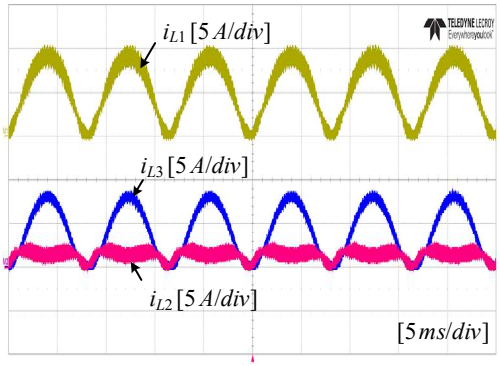


Fig. 9. Inductor currents ($i_{L1}$, $i_{L2}$, $i_{L3}$).

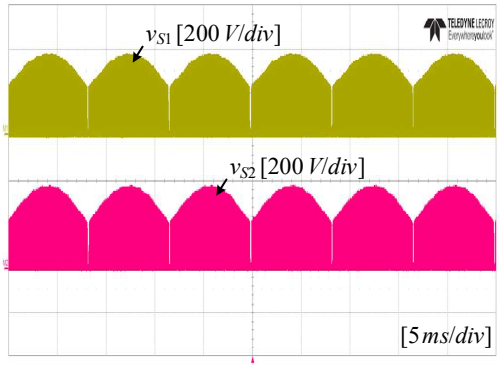


Fig. 10. Voltage stress on switches ($v_{S1}$, $v_{S2}$)

## IV. CONCLUSION

In this paper, a high power factor rectifier using the boost-SEPIC interleaved structure is presented. The operation and characteristics of the proposed BSI-PFC converter as well as the control aspect of the PFC application are discussed. The proposed solution offers:

1) Automatic balancing of inductor currents is achieved without any active current balancing mechanism.

2) Only one current sensor with one current control loop is used for regulating the input current.

3) Because of the high voltage gain and low voltage stress on switches, the efficiency of the proposed PFC is improved compared to IB-PFC.

Experimental results with the 1.6 $kW$ prototype verify the performance and above characteristics of the proposed

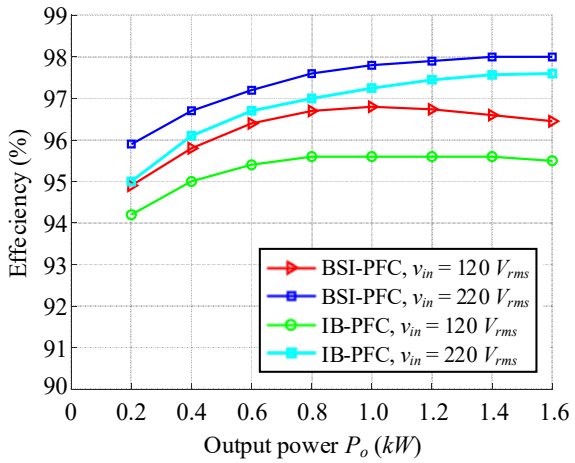


Fig. 11. Efficiency vs. output power of the IB-PFC and the proposed BSI-PFC converters.

BSI-PFC converter. These benefits show that the BSI-PFC is a potential candidate for practical PFC applications.

## ACKNOWLEDGMENT

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