

Boosting Pilot-Diode Reverse-Conducting IGBTs Turn-ON and Reverse-Recovery Losses with a Simple Gate-Control Technique

Daniel Lexow^{1,2}, Hans-Günter Eckel¹

¹UNIVERSITY OF ROSTOCK

Albert-Einstein Str. 2

18059 Rostock, Germany

Phone: +49 (0) 381-498 7112

Fax: +49 (0) 381-498 7102

Email: daniel.lexow@uni-rostock.de

URL: <http://www.iee.uni-rostock.de>

²NORDEX SE

Langenhorner Chaussee 600

22419 Hamburg, Germany

Phone: +49 (0) 40-300030-1000

Fax: +49 (0) 40-30030-1101

Email: dllexow@nordex-online.com

URL: <https://www.nordex-online.com/de/>

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Abstract

PD-RC-IGBTs reverse-recovery and turn-ON losses are significantly improvable by reducing the inverter interlock time in diode conduction mode. Device Measurements with 1200 V PD-RC-IGBTs reveal a loss reduction potential of up to 27,5 % for reverse-recovery and 26,2 % for turn-ON energy losses, compared to state-of-the-art inverter interlock times. A gate control realizing this selective inverter interlock time adaption for the diode mode, as well as the corresponding measurements and loss calculations, are presented.

Introduction

Today, the concept of RC-IGBTs has been widely known for well over two decades [1], [2]. But in 2004, Mitsubishi established a 1200 V RC-IGBT module [3] which can be seen as the initial starting point for consumer awareness and the introduction of the RC-IGBT into the field of high-power semiconductors. [4]. In order to achieve a reverse conducting functionality, the implementation of n-shorts into the IGBTs collector-sided p-layer was accomplished. In this way, the diode merged with the IGBT and an RC-IGBT, based on only one chip – the so-called: “*first-generation*” (1. Gen.) RC-IGBTs (see figure 1) was created. Related to a full 6.5 kV *High-Voltage (HV)* IGBT module, which usually consists of 24 IGBT and 12 diode chips, the same HV-RC-IGBT module could now be equipped with 36 RC-IGBT chips. This not only results in a significantly higher electrical power output but also increases the device lifetime due to the new chip properties. Since the current can now be conducted bidirectionally in one single chip, temperature ripple and resulting thermal-mechanical stress are significantly reduced [5], [6].

Despite all the positive features mentioned above, the 1. Gen. RC-IGBT comes with a challenging issue. Contrary to conventional IGBTs, the electron-hole plasma concentration in the RC-IGBT is highly dependent on the applied *gate-emitter voltage* (V_{GE}) as long as the current is driven in the diode direction. A positive V_{GE} ($V_{GE} > V_{THRESHOLD}$, e.g., $V_{GE} = +15$ V) creates an electron channel under the gate, allowing electrons to bypass and causing a unipolar current flow which drastically reduces the emitter efficiency in diode mode. Therefore, it is inevitable to turn OFF V_{GE} (e.g., $V_{GE} = -15$ V) in diode mode in order to ensure high emitter efficiency and low diode *forward losses* (V_F). To guarantee proper device behaviour, the control state, either the *Gate Drive Unit (GDU)* or a higher-level control unit, relies on some sort of current direction detection that utilizes a static MOS-Control as stated in [7].

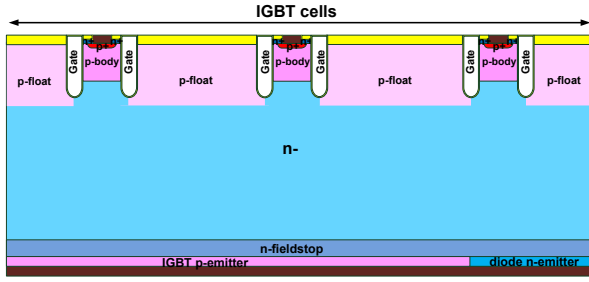


Fig. 1: Cross-section of a conventional RC-IGBT (1. Gen.) with homogeneous frontside and collector-sided n^+ -shorts

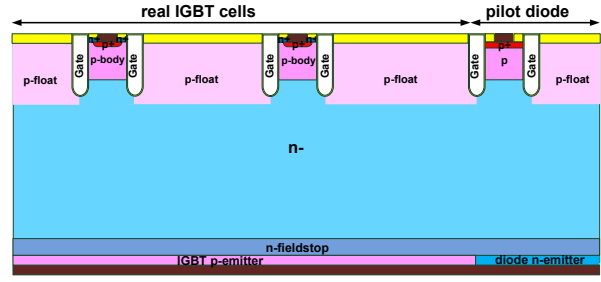


Fig. 2: Cross-section of a PD-RC-IGBT (2. Gen.) with inhomogeneous frontside due to pilot diode areas

Unfortunately, not only the need for a static MOS-Control is a disadvantage of the 1. Gen. RC-IGBT. The significantly increased diode area within an entire module (36 RC-IGBT chips) leads to a considerably higher reverse-recovery charge and, therefore, greater reverse-recovery as well as turn-ON losses. This issue needs to be addressed by implementing a Dynamic MOS-Control [7] into the gate control scheme. Herby, the emitter efficiency in diode mode is deliberately reduced by turning on V_{GE} for a short time ($t_{DESAT} \sim 5 \dots 20 \mu s$) right before reverse-recovery. It is possible to build a functional RC-IGBT control that is able to include both MOS-Control strategies, but it is complicated and demanding, as shown in [8], [9]. Furthermore, high-frequency parasitic oscillations on the load current need to be addressed to protect the GDU from overheating due to multi-switching, as explained in [10]. In this respect, customers are very cautious about using these components within their applications.

To minimize the effort of control and thus make the RC-IGBT more user-friendly, the *Pilot-Diode (PD)* RC-IGBT was developed. This “*second generation*” (2. Gen.) RC-IGBT is characterized by additionally implemented pilot diode areas guarantying low V_F in diode mode without the necessity of special gate control mechanisms [11]. The pilot diode areas ensure sufficient electron-hole plasma in the device even at $V_{GE} = +15 V$ in diode mode. Here, the electron channel reduces the electron-hole plasma concentration in all IGBT cells, but this does not affect the pilot diode areas. Due to the modified front side of the PD-RC-IGBT, no electron channel is created in PD areas, and therefore, sufficient electron-hole plasma to obtain low diode ON-state losses is supplied.

Hence, PD-RC-IGBT can be used with conventional IGBT GDUs. They simplify the applicability and allow easy access of the components into the commercial market. Nevertheless, producers are aware of the fact that they still have an adverse issue caused by the *inverter interlock time* (t_{INT}), leading to high reverse-recovery and turn-ON losses [11]. The problem itself and its proposed solution, supported by device measurements with real PD-RC-IGBTs, are described in the ongoing chapters of this paper.

The latest scientific research shows different forms of RC-IGBTs, which unit both exceptional electrical and thermal-mechanical performance as well as independence from special gate control mechanisms [12]. Those RC-IGBTs are not “hardware-based” at the moment. They are only available for device simulations and might be produced and used in the future. They are referred to as “*third-generation*” (3. Gen.) RC-IGBTs and mentioned here for the sake of completeness.

Inverter interlock time (t_{INT}) and its negative impact on PD-RC-IGBTs

In 2015 Rahimo et al. introduced a novel 6.5 kV/1000 A PD-RC-IGBT referred to as “6500 V Plug-In BIGT” [11]. In their publication, they not only described the internal structure of the component but also made detailed reflections on the switching losses. In this context, they choose an interlock time of $t_{INT} = 10 \mu s$, typical for the voltage class of 6500 V, to present their devices’ switching losses. The working group further shared a key finding: concerning interlock time reduction. They stated: “By reducing locking time moderately to 5 usec, a further 5 % reduction in turn-ON losses and a 10 % reduction in reverse recovery losses can be obtained”[11].

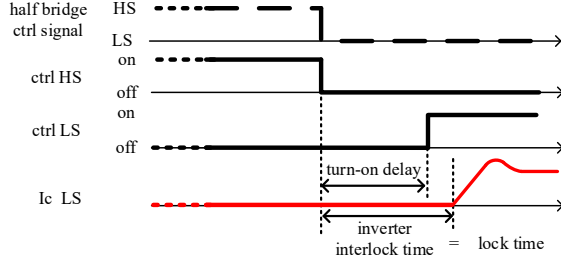


Fig. 3: Definition of the inverter interlock time (t_{INT}) [device point of view]

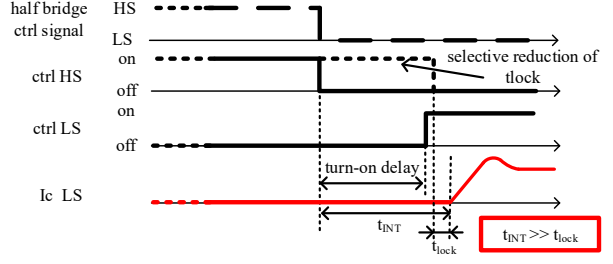


Fig. 4: Definition of the lock time (t_{LOCK})

The reason for this device behaviour is that the conventional RC-IGBT frontside (see figure 2) of the PD-RC-IGBT is still V_{GE} dependent in diode conduction mode. As long as the gate-emitter voltage is turned on to $V_{GE} = +15$ V, electron-hole plasma in those IGBT areas is reduced. The low-loss diode on-state properties (low V_F) are, in this case, ensured by the pilot diode regions, but at the same time, a minimum electron-hole plasma is present in the device. Therefore, it would be desirable to start the reverse-recovery process instantly as soon as the turn-OFF signal from the inverter control is received. Unfortunately, this is prohibited due to the inverter interlock time by several μ s (figure 3, HS RC-IGBT in diode mode). Within the t_{INT} , the PD-RC-IGBT keeps conducting current in diode direction. Still, V_{GE} is now turned OFF to $V_{GE} = -15$ V. This results in an electron-hole plasma increase in the conventional RC-IGBT areas, leading to unnecessarily high reverse-recovery and turn-ON losses at the time of the actual reverse-recovery process.

If it is assumed that the HS IGBT is in diode mode, then for the conventional diode turn-OFF process, the inverter interlock time (t_{INT}) is equal to the lock time (t_{LOCK}). Figure 4 shows the behaviour of t_{LOCK} for an applied selective lock time reduction method. In this case, the lock time (t_{LOCK}) becomes significantly smaller than the inverter interlock time (t_{INT}). Deriving from this, in diode conduction mode, it is preferable to minimize the inverter interlock time as much as possible (see figure 4) in order to achieve the lowest reverse-recovery losses. For IGBT conduction mode, this is not possible because t_{INT} prevents half-bridge short circuits. Therefore, there has to be some sort of distinguishing process which ensures that a reduction of t_{INT} is only applied while conducting current in diode direction.

Implementation of a selective lock time reduction in diode conduction mode for PD-RC-IGBTs GDU

As discussed and introduced in [13], realizing a selective lock time reduction for the PD-RC-IGBTs diode mode relies on a current direction detection method. Hereby, three different methods can be used:

Firstly, the direct current measurement via a current sensor (e.g., LEM-Converter). This method impresses with its accuracy and precision but is not recommended for the present application due to its high costs. In this respect, this variant will not be further considered.

Secondly, the indirect current measurement via high-voltage desaturation diodes. Here, V_{CE} is monitored by the HV desaturation diode circuit. The decision of whether a positive or negative current is conducted through the device is based on either the positive or negative decoupling voltage. This method impresses with its simplicity and cost-efficiency. Since the desaturation diodes need a specific creepage distance that must be obeyed if installed directly on the GDU, it is rather recommended for lower voltage classes ($< 1,7$ kV).

Lastly, another indirect current measurement method can be utilized as fully described in [12], [13]. The “gate observation method” distinguishes between IGBT and diode mode by keeping track of the miller plateau in the turn-OFF process. If a miller plateau is detected by a time-dependent gate voltage threshold, the GDU performs a conventional IGBT turn-OFF. If no miller plateau is detected by the time-dependent gate voltage threshold, a special diode mode turn-OFF is performed.

As a result, the gate voltage is instantly turned back ON again and remains “ON” until lock time is sufficiently reduced. This method is easy to implement into the GDU (see GDU in [14]) and very cost-efficient. Unfortunately, it is only suitable for higher voltage classes ($>1,7$ kV) since a pronounced miller plateau, especially at low currents, is needed to determine the correct turn-OFF mode. RC-IGBTs in voltage classes below 1,7 kV do not show a sufficiently pronounced miller plateau, as shown in figure 9.

Measurement Results

All measurement results were obtained using 1200 V; 1000 A PD-RC-IGBTs with nominal gate resistors @ a temperature of $T = 125$ °C. The used module is a half-bridge module, where each RC-IGBT (low side and high side switch) can be controlled individually by external GDUs. The GDU responsible for achieving the t_{LOCK} reduction utilizes HV desaturation diodes and an FPGA (see [14]).

Double pulse tests for measurements (A and B) were performed using a test bench (Fig. 5) equipped with a DC-link capacitor ($C = 2,82$ mF) and a load inductance ($L = 543$ μ H) to adjust the current. The parasitic stray inductance in the commutation path was $L\sigma = 39$ nH.

The oscillating load current measurements (C) were performed in a different test-bench (Fig. 6) with the following characteristics: DC-link capacitor ($C = 2,82$ mF), a load inductance ($L = 130$ μ H) and a load capacitor ($C = 175$ μ F). Due to different test-bench conditions and mechanical superstructures, parasitic stray inductance in the commutation path increased to $L\sigma = 44$ nH.

A) Reverse-recovery and turn-ON losses with successively reduced interlock time

Within the performed double pulse measurements, the inverter interlock time for the high-side PD-RC-IGBT was successively reduced. As shown in figures 7 and 8, the lock time reduction results in significantly decreased collector peak currents, turn-ON losses as well as reverse-recovery peak currents, and reverse-recovery losses. All results are shown in Table I. For the value of the "reduction" columns, the row value (e.g. $t_{\text{LOCK}} = 0,3$ μ s) is set in relation to the reference value ($t_{\text{INT}} = t_{\text{LOCK}} = 5$ μ s [state-of-the-art inverter interlock time], bold). The output value (in %) thus indicates how much the test value is below the reference value. Measurements were also accomplished with a maximal $t_{\text{LOCK}} = 10$ μ s (first row of Table I), showing that plasma barely increases with longer lock times.

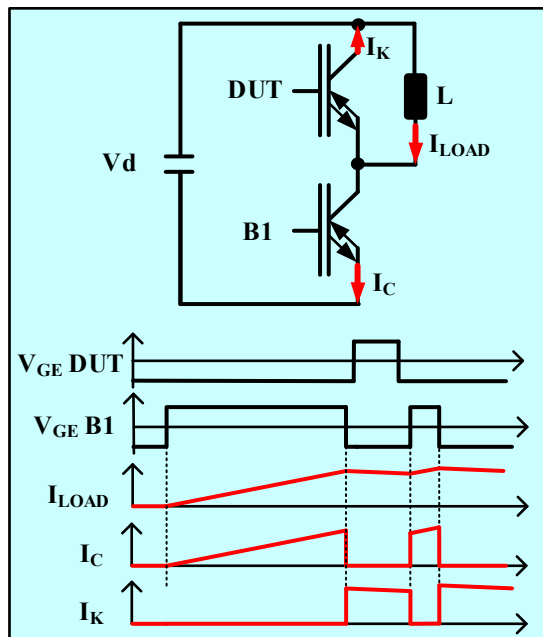


Fig. 5: Double pulse test with a corresponding pulse pattern

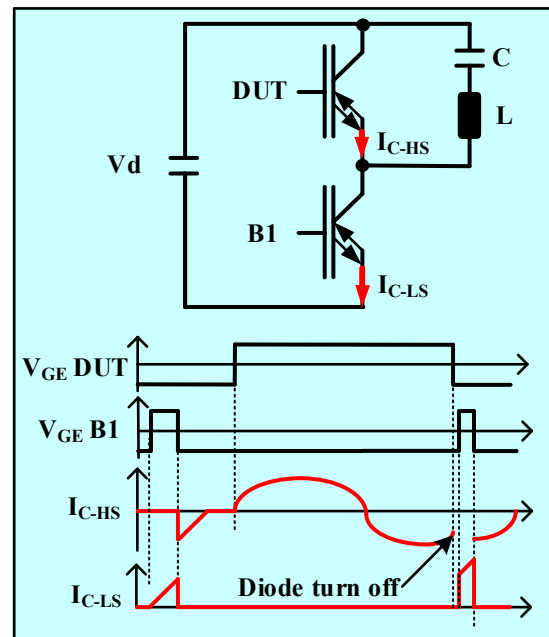


Fig. 6: Oscillating load current test with a corresponding pulse pattern

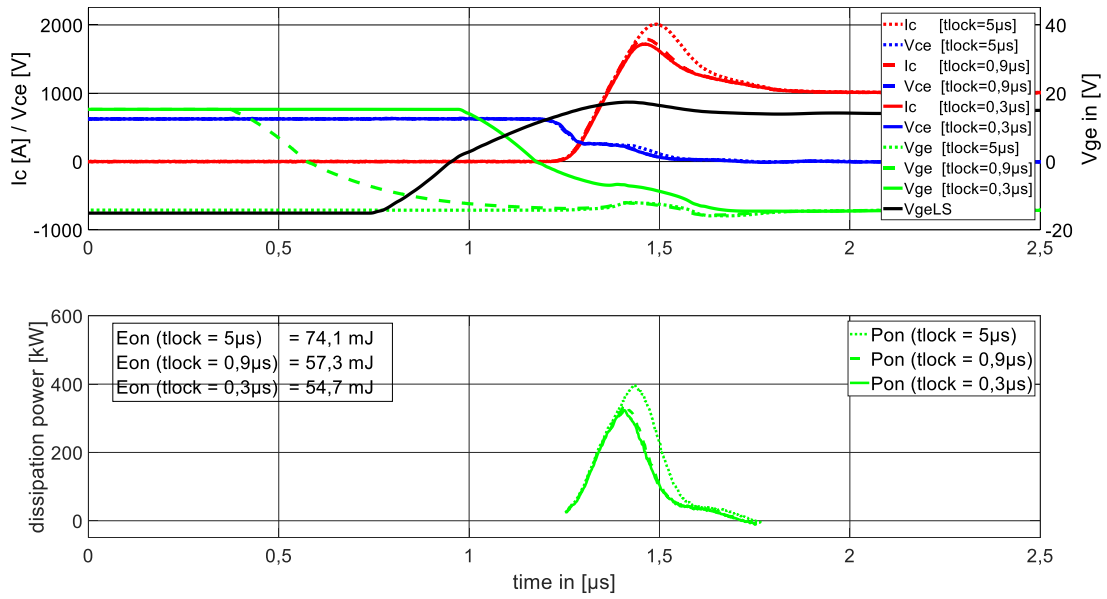


Fig. 7: Turn-ON curves and turn-ON losses for different t_{LOCK}

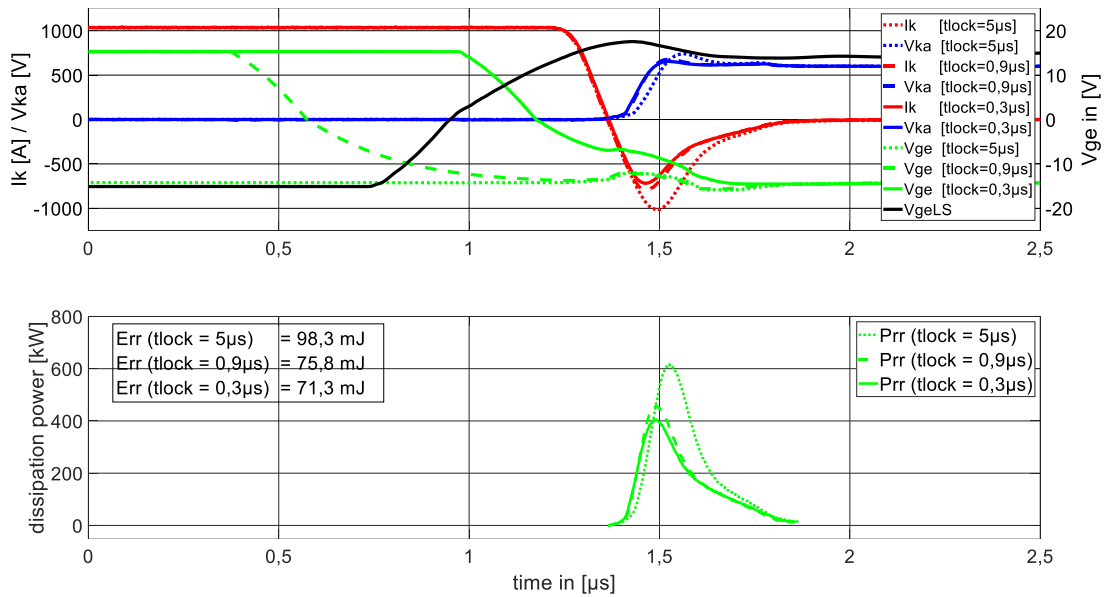


Fig. 8: Reverse-recovery curves and reverse-recovery losses for different t_{LOCK}

Table I: Overview of turn-ON and reverse-recovery losses as a function of t_{LOCK}

t_{LOCK} [μ s]	I_{C_max} [A]	reduction [%]	E_{ON} [mJ]	reduction [%]	E_{RR} [mJ]	reduction [%]	E_{TOTAL} [mJ]	reduction [%]
10	2038	+1,6	74,7	+0,8	102,0	+3,8	176,7	+2,5
5	2005	0	74,1	0	98,3	0	172,4	0
2,5	1910	-4,7	65,5	-11,6	87,8	-10,7	153,3	-11,1
1,5	1839	-8,3	61,1	-17,5	80,3	-18,3	141,4	-18,0
0,9	1787	-10,9	57,3	-22,7	75,8	-22,9	133,1	-22,8
0,6	1750	-12,7	55,6	25,0	73	-25,7	128,6	-25,4
0,4	1720	-14,2	55,1	-25,6	71,5	-27,3	126,6	-26,6
0,3	1716	-14,4	54,7	-26,2	71,3	-27,5	126	-26,9

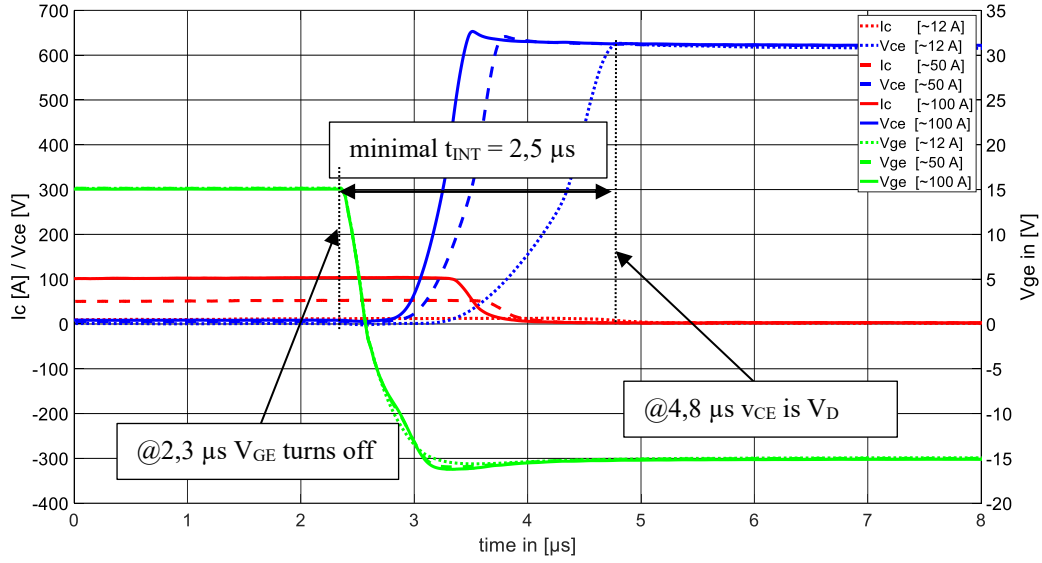


Fig. 9: Turn-OFF times dependent on the collector current

B) IGBT mode turn-OFF with the nominal turn-OFF gate resistor

This series of tests aims to determine the maximum IGBT mode turn-OFF times. Since the turn-OFF process is strongly dependent on the load current and takes longer with decreasing collector currents, an attempt was made to determine the maximum turn-OFF time by switching off a minimum current (see figure 9). Knowing the maximum turn-off time at minimum current makes it possible to define a fair and comparable inverter interlock time for the individual component (locking time = 5 μ s with safety margin). The results obtained from the previous tests can be related to this defined interlock time to specify the objectively achievable loss savings.

The obtained results allow two different procedures: Firstly, the locking time is adopted almost without a time safety buffer. This means that the obtained turn-OFF time of 2,5 μ s (figure 9) is rounded up to a 3 μ s inverter locking time. However, this would be relatively “tight” and would leave no room for any delays. Accordingly, the choice of the second method is recommended, which entails the introduction of a time safety buffer that can counteract possible delays. Here, the locking time could be increased “moderately” to 4 μ s or “conservatively” to 5 μ s. The results for those cases are shown in Table II.

Table II: Overview of turn-ON and reverse-recovery losses for three different t_{INT}

	inverter locking time [μ s]	$E_{RR} +$ E_{ON} [mJ]	reduced lock time [μ s]	$E_{RR} +$ E_{ON} [mJ]	reduction [%]	reduced lock time [μ s]	$E_{RR} +$ E_{ON} [mJ]	reduction [%]
“tight”	3	159,6	0,9	133,1	16,6	0,3	126	21,1
“moderate”	4	167,3	0,9	133,1	20,4	0,3	126	24,7
“conservative”	5	172,4	0,9	133,1	22,8	0,3	126	26,9

C) GDUs functionality validation with the help of an L-C oscillating circuit

This last series of tests aims to validate the GDUs functionality in a close to real application. Hereby, an oscillating (L-C) circuit was utilized to provide the DUT with a low-frequency oscillating load current (figure 6). Based on that provided current, the GDU needs to self-adapt its switching behaviour. Within the switching experiment, the resonant circuit capacitor is first charged by switching ON the lower RC-IGBT. Subsequently, the oscillation of the load current can start as soon as the DUT receives its turn-ON signal from the higher-level control. Hence, two experiments were performed:

1. The turn-OFF signal for the DUT was given within the positive load current half-wave

The GDU must recognize that a positive collector current is conducted and that an IGBT switch-OFF process has to be carried out accordingly. This must be initiated immediately in order to have reliably switched off the DUT before the opposite RC IGBT is switched on after the interlock time of $t_{INT} = 5 \mu s$. This behaviour can be traced in Figure 10. It is important to realise that the driver switches OFF correctly. The gate-emitter signal depicted in green shows that the CTRL signal from the higher-level controller, which is displayed in black, is followed directly. The time offset (~ 250 ns) between the two signals arises from the processing times during signal processing in the FPGA and during forwarding on the driver. These can vary depending on the driver (components) and FPGA (clock frequency) but can be regarded as constant variables and are therefore not critical in the design for timing aspects such as inverter locking times. For the PD-RC-IGBT GDU, the resulting $t_{LOCK} = 5 \mu s$ can be seen between the upper (green, solid) and lower (green, dashed) RC-IGBT.

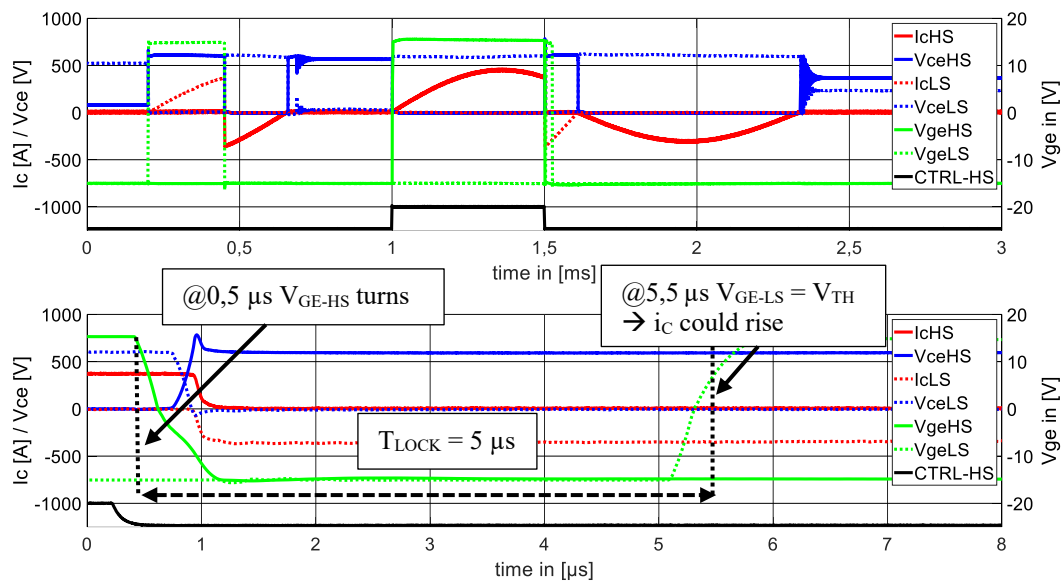


Fig. 10: Top (macroscopic view): IGBT turn-OFF in positive load current half-wave
Bottom (microscopic view): lock time determination based on V_{GE-HS} and V_{GE-LS}

2. The turn-OFF signal for the DUT was given within the negative load current half-wave

The driver must recognize that a negative collector current is conducted and that a modified diode turn-OFF process must be carried out accordingly. In contrast to a conventional IGBT driver, the higher-level turn-OFF signal is not to be followed directly. Instead, the driver must delay the turn-OFF. The delay time can be defined individually for each voltage class and application. In the present measurement example, it was set to $4 \mu s$ and thus led to a moderate lock time (t_{LOCK}) of $1 \mu s$.

Figure 11, like Figure 10 for the IGBT turn-OFF process, now shows the corresponding curve for the diode turn-OFF process. It can be seen that the interlock time of $t_{INT} = 5 \mu s$ (approx. CTRL_HS (black) "off" to Vge_LS "on" (dashed green)) specified by the higher-level controller is not executed. The driver detects the diode mode with the help of its current direction detection. Accordingly, the FPGA modifies the turn-OFF process, which results in a reduction of the effective lock time. The lock time set in the present example is a moderate $1 \mu s$ and is calculated as seen in the bottom part of figure 11. The gate driver's (hardware) functionality, combined with the proposed control principle (software), is thus proven. The effects of the presented control principle in terms of loss balance (switching losses) are considered below.

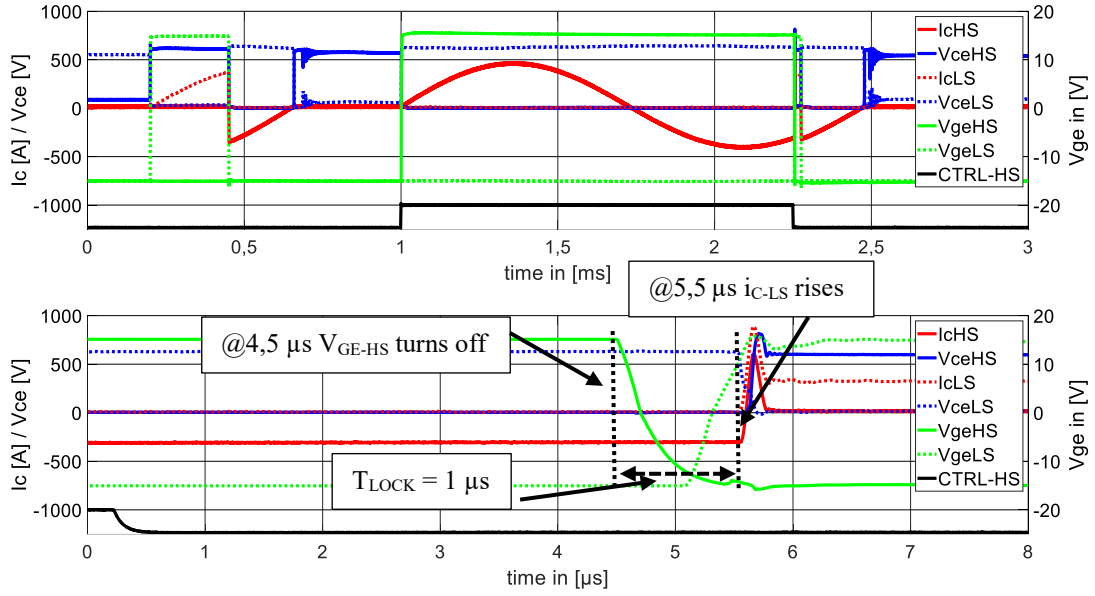


Fig. 11: Top (macroscopic view): Diode turn-OFF in negative load current half-wave
Bottom (microscopic view): lock time determination based on V_{GE-HS} and i_{C-LS}

Figure 12 shows the course of the diode turn-OFF, and Figure 13 shows the turn-ON of the opposite RC-IGBT. The gate emitter voltage (green, dotted) shows the influence of the driver on the turn-OFF process. To better illustrate the positive effect on the E_{RR} and E_{ON} , these were contrasted with the resulting reverse recovery and turn-ON processes with a conventional IGBT gate control ($t_{INT} = t_{LOCK} = 5 \mu s$) in a second measurement experiment. For this purpose, a blind gate driver (green, solid) was used, which exclusively follows the incoming signals of the higher-level control. Within the measurements, it was found that there is a significant reduction in switching losses, as already shown in Tables I and II. The introduced PD-control is able to reduce switching losses [mean reduction value = (reduction E_{on} + reduction E_{err})/2] for the given turn-ON current by 25,9 %. The comparison, especially with regard to current and voltage characteristics as well as the significant loss reduction between those two GDU variants, makes it evident that the use of the novel PD-RC-IGBT control is unrestrictedly recommended.

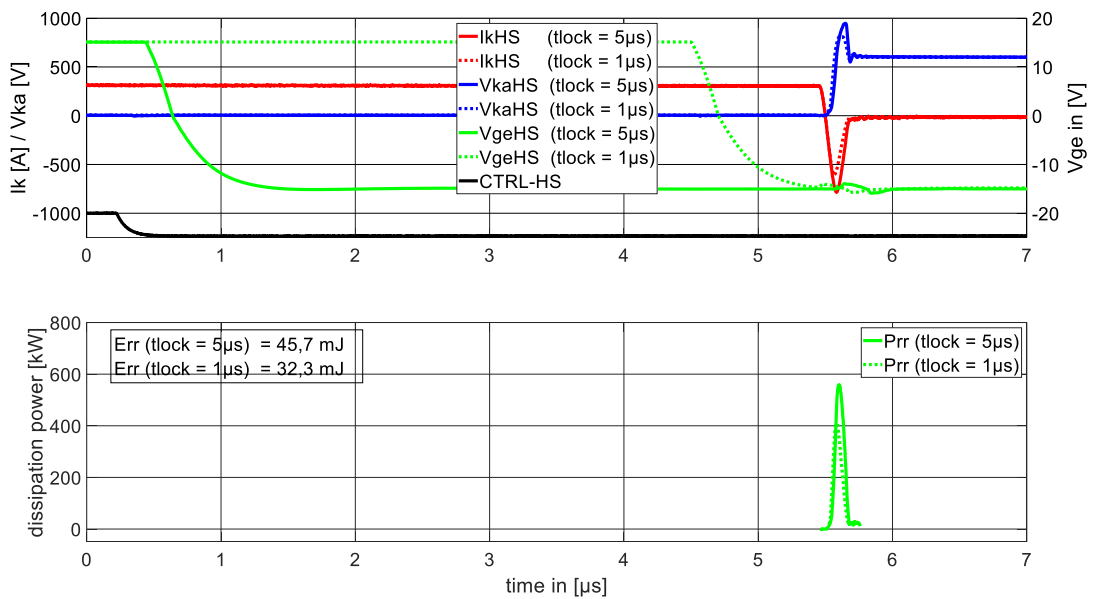


Fig. 12: Diode reverse-recovery behaviour with corresponding loss calculation

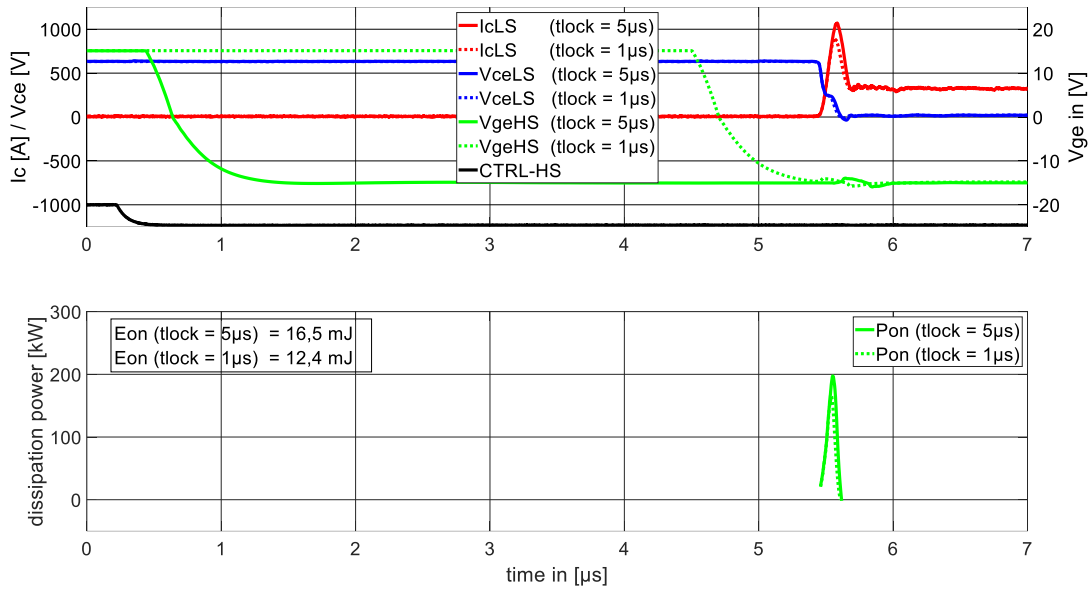


Fig. 13: IGBT turn-ON behaviour with corresponding loss calculation

Conclusion

The results of this paper are, due to the inclusion of high voltage measurements on real PD-RC-IGBTs, able to prove that an adapted gate control (selective locking time reduction) can significantly reduce the reverse-recovery and the turn-ON energy losses of PD-RC-IGBTs. To put the obtained results into a comparative perspective and guarantee an appropriate classification, Table III provides a comparison to a conventional IGBT module. Please note that the RC-IGBT switching losses are optimized to meet the results of the conventional module. Therefore, V_F is increased. The Fuji – 2MBI800XNE120-50 exhibits equivalent chip technology and blocking voltage and is scaled up to 1000 A to allow proper comparison with the Fuji 1200 V 1000 A PD-RC-IGBT (2MBI1000XRNE120-50). Latter is presented with data sheet values (column 2) and own measurements (columns 3 and 4). Results indicate a huge switching loss (E_{ON} and E_{RR}) advantage (18,1 %) over the conventional module while simultaneously introducing all positive features (higher current density, greater diode surge current capability and reduced thermo-mechanical stress and therefore longer life-time expectancy) of the RC-technology into the application.

Table III: Performance comparison of 1200 V (RC) IGBT [Fuji]

Product	<u>data sheet values</u>		<u>own measurements</u>	
	1200 V 800 A IGBT	1200 V 1000 A RC-IGBT	1200 V 1000 A RC-IGBT	1200 V 1000 A RC-IGBT
Product name	2MBI800 XNE120-50	2MBI1000 XRNE120-50	2MBI1000 XRNE120-50	2MBI1000 XRNE120-50
MOS-Control	no	no	no	t_{LOCK} reduction to 0,3 μs
V_F @ $V_{GE} = 0$ V	1,65	1,9	1,9	1,9
E_{RR} @ $T = 125$ °C in [mJ]	52,9	72,8	91	71,3
E_{ON} @ $T = 125$ °C in [mJ]	70,2	85,2	68,6	54,7
$E_{ON} + E_{RR}$ in [mJ]	123,1	158	159,6	126
$E_{ON} + E_{RR}$ scaled up to 1000 A in [mJ]	153,9	/	/	/
Losses ($E_{ON} + E_{RR}$) relatively to conventional IGBT	100%	102,70%	103,70%	<u>81,90%</u>

At this point, it should be emphasised once again that the general control effort is drastically reduced compared to the RC-IGBTs of the first generation. The PD-RC-IGBT does not require any current direction-dependent control for normal operation and can therefore be operated at $V_{GE} = +15$ V in diode mode. The implemented current direction detection ensures the selective determination of the operating mode exclusively when receiving the turn-off signal from the higher-level inverter control. In the case of a diode mode, this results in the desired lock time (t_{LOCK}) reduction. Further, the adaptation effort for the GDU is rather low or almost non-existent if the used GDU already provides an FPGA or V_{CE} monitoring.

Conclusively, it would be desirable that the results obtained in this paper contribute to making the PD-RC-IGBT more user-friendly and pushing it into technical high-power applications.

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