Optimal design of integrated motor drives - Comparison of topologies (2L/3L/modular), PWM variants, and switch technologies (Si/SiC/GaN)

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Abstract

In this paper, a new design procedure for the optimal design of an integrated motor drive is presented, including an extended iron loss model. The design procedure is based on a multi-objective optimization of power density, efficiency, and cost. In the optimization, a large design space is covered, including the inverter topology, the PWM scheme, the chip technology (Si/SiC/GaN), the winding scheme, the chip area/cost, and the switching frequency. In addition to power density/efficiency/cost, the system reliability is investigated. Considering a 1.5 kW IMD as example, the optimal design in terms of efficiency and cost is achieved using a modular topology, GaN HEMTs, and a 9-phase motor winding. This design enables an efficiency increase of +2.26 % at 36 % higher cost compared to the cost-optimal design that is achieved with the standard 2L-topology, Si IGBTs, and a 3-phase motor winding.

1 Introduction

Integrated motor drives (IMDs) combine an electric motor and its driving inverter in one mechanical unit [1]. A basic question during the design of such IMDs is what is the optimal inverter topology and what are the optimal topology-related design parameters such as the PWM scheme and the chip technology (Si/SiC/GaN) in terms of power density/efficiency/cost.

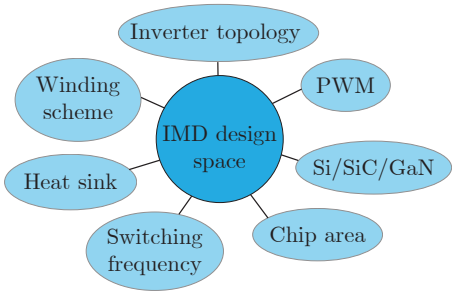

Figure 1: Design space considered for the optimal design of IMDs.

Existing literature already covers several topology comparisons for inverters in general [2–4], and for IMDs in particular [1, 5, 6]. According to [1], modular topologies are advantageous due to their potential for higher fault-tolerance, smaller size, and lower cost. In [5], the focus is on different topologies for the rectifier whereas for the inverter always the same 2L-topology is considered and the motor has a 3-phase winding. However, [5] considers neither different topologies for the inverter, nor multiphase motor windings. In addition, a comprehensive design procedure that enables a holistic comparison of modular inverter topologies and standard 2L- and 3L-topologies is missing. A limited approach of such a comparison is given by [6], wherein standard 2L- and 3L- inverter topologies are compared to different modular inverter topologies such as a *2L-2S-VSI* (series connection of two 2L-modules) or a *3L-2P-VSI* (parallel connection of two 3L-modules). However, the approach in [6] is limited because the chip area/size is not optimized and the analysis only focuses on efficiency, i.e. power density and cost are not included in the comparison.

To fill this gap, this paper presents a design procedure for a holistic comparison of modular converter topologies and standard 2L- and 3L-topologies. In this context, "holistic" means that multiple design goals (power density/efficiency/cost/reliability) and a relatively large set of topology-related design parameters is considered. An overview of the considered design parameters (i.e. the design space), is shown in Fig. 1. Therein, the variable *winding scheme* indicates that also multiphase motors are considered in this paper.

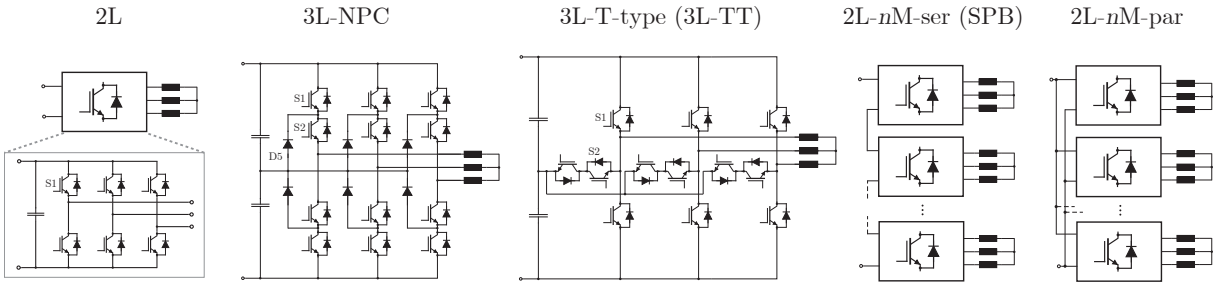

Figure 2: Inverter topologies considered for the IMDs. The topologies 2L, 3L-NPC, and 3L-TT are standard non-modular topologies that are connected to the 3-phase motor. The topologies 2L-*n*M-ser & 2L-*n*M-par are modular topologies that consist of $n \times$ 2L-modules connected in series (2L-*n*M-ser) or parallel (2L-*n*M-par) and that are connected to multiphase motors.

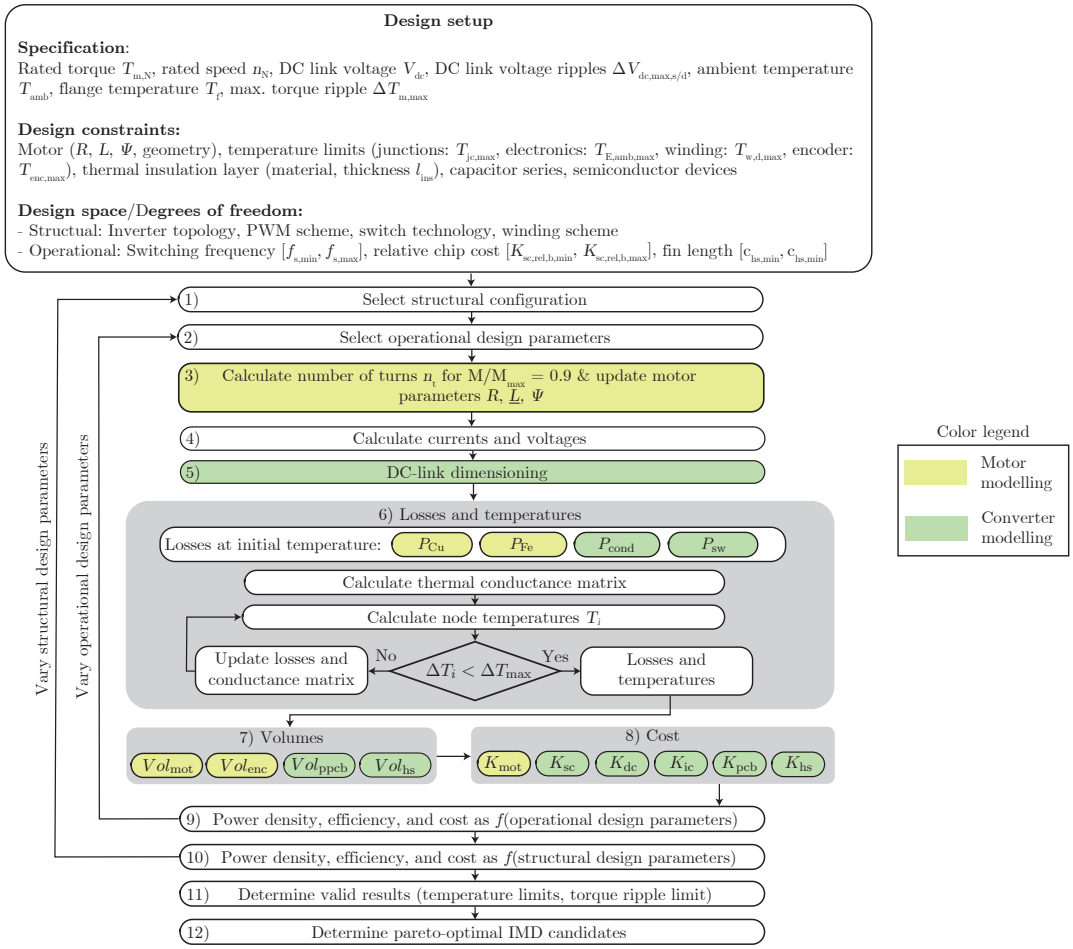

Figure 3: Procedure for the optimal design of an IMD in terms of power density, efficiency, and cost.

In the following, first the proposed design procedure is presented in section 2. The models used for the design procedure and for evaluating the system reliability are given in section 3. In section 4, the results of applying the design procedure to an exemplary system specification of a 1.5 kW high-torque, low-speed motor are presented and discussed. In section 5, the reliability of the considered converter topologies is analysed and compared.

2 Design procedure

Fig. 3 shows the proposed procedure for the IMD design for a fix DC link voltage and a given PMSM, where only the number of turns of the stator winding is varied. The considered integration concept is an axially integrated IMD, which is shown in Fig. 4 and explained in detail in [7]. In the following, the design setup and the different steps of the design procedure are explained.

2.1 Design setup - Specification, constraints, and design space

The start of the design procedure in Fig. 3 is to initialise the system specification, the design constraints, and the design space. The system specification comprises the DC link specification, the motor specification, and the ambient temperatures (air/flange). The design constraints for the different parameters are determined by the selected motor, the semiconductor devices, the capacitor series, the electronics temperature rating, and the thermal insulation layer.

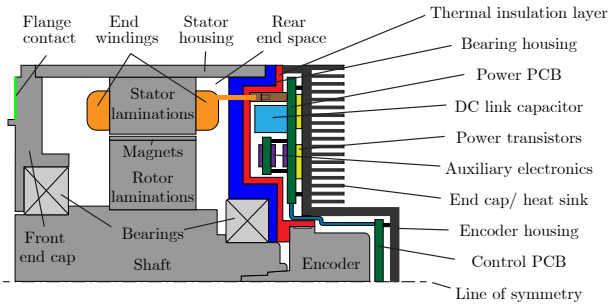

Figure 4: Inverter integration concept [7].

The overall design space is split into structural degrees of freedom and operational degrees of freedom (DOFs). The structural DOFs in Fig. 3 define the basic system configuration, i.e. they describe a combination of an inverter topology, a PWM scheme, a semiconductor technology, and a winding scheme. The considered system configurations are summarized in Tab. I. The procedure could be extended to other configurations as well.

Table I: Considered system configurations. In case a certain *PWM*-/*SC*-/*W*-variant is only combined with particular topologies, these topologies are indicated in parenthesis.

Topology Top	Modulation scheme PWM	Semiconductor technology SC	Winding scheme W
1: 2L	1: Sin-PWM	1: Si	1: 3-phase ($Top = 1/2/3$)
2: 3L-NPC	2: OC-PWM ($Top = 1/4/5$)	2: SiC	2: 9-phase ($Top = 4/5$)
3: 3L-TT	3: NPB-PWM ($Top = 2/3$)	3: GaN	
4: 2L-3M-ser			
5: 2L-3M-par			

The selected topologies are shown in Fig. 2. This selection of topologies is based on the motivation to compare standard non-modular topologies (2L, 3L-NPC, 3L-TT) to modular topologies (2L-3M-ser, 2L-3M-par), that are particularly developed/presented for IMDs in literature [6, 8]. As PWM schemes, standard Sinus-PWM (Sin) and advanced schemes such as Optimal Clamped-PWM (OC) and Neutral Point Balanced-PWM (NPB) are considered. Regarding semiconductor technologies, Si IGBTs, SiC MOSFETs, and GaN HEMTs are considered with an overall voltage blocking capability of 1200 V for DC link voltages up to 800 V. Concerning the winding scheme, non-modular topologies are combined with a standard 3-phase winding and modular topologies are combined with a non-phase-aligned 3x3-phase winding, called 9-phase in the following. This winding scheme is chosen, because for the same topology, it is already known to perform better than phase-aligned 3x3-phase windings due to a higher winding factor [9].
The operational DOFs in Fig. 3 are design parameters that are linked to the relevant trade-offs in the design goals (system power density ρ_{sys}, system efficiency η_{sys}, system cost K_{sys}). These trade-offs are:

1. With increasing switching frequency the switching losses increase, but harmonic motor losses and the torque ripple are decreased in the standard case of 3-phase motors. With multiphase-motors like 9-phase motors, the switching frequency also affects the harmonic motor losses and the torque ripple but the dependency is more complex due to the fact that multiphase motors have multiple inductances for different harmonic sequences.

2. Increasing the heat sink size decreases the power density, but increases efficiency due to the temperature dependence of the conduction losses ($R_{\mathrm{ds,on}}$) and the motor losses.

3. Increasing the chip area/chip cost decreases conduction losses, but increases the system cost. Depending on the $E_{\mathrm{on}}(I)/E_{\mathrm{off}}(I)$-curves, increasing the chip area/chip cost can furthermore increase switching losses due to the larger parasitic capacitances that have to be charged/discharged during switching.

The relative chip cost $K_{\mathrm{sc,rel,b}} := {}^{K_{\mathrm{sc}}}/_{K_{\mathrm{sc,b}}}$ is used as an indicator for the chip area, where $K_{\mathrm{sc,b}}$ is a chip cost budget that is constant for all system configurations to ensure a fair comparison.

2.2 Calculation steps of the design procedure

The procedure in Fig. 3 starts in step 1) with an outer loop (brute force) over the structural DOFs and continues, in step 2), with an inner loop over the operational DOFs. In each iteration, which starts in step 3), the number of turns n_{t} is adapted to a relative modulation index M/M_{max} of 90 % to achieve a good DC link utilization with 10 % margin for the control. In step 3) also the motor resistance R, the inductance matrix $\underline{L}$, and the PM flux linkage Ψ are calculated. In step 4)-5), these motor parameters and the modulation index are used to calculate the switched currents and voltages, and the required DC link capacitance. In step 6), the system losses and temperatures are calculated in an iterative routine. Therein, all considered loss components (copper, iron, conduction, switching) are calculated, which are the input values of a lumped parameter thermal network (LPTN) model. Then the LPTN is solved resulting in the node temperatures of the LPTN. For this resulting temperature distribution, the motor copper losses and the inverter conduction losses are recalculated and the LPTN is solved again. This process is repeated until the losses and the temperatures converge. Thereafter, the system volume and costs are calculated in step 7)-8). The results are used in step 9)-11), where the system power density, the system efficiency, and the system costs are calculated and the designs are identified, which meet the temperature limits and the torque ripple limit defined in the design setup. Finally, the pareto-optimal designs are determined from the set of valid designs in step 12). In the following, the models, that are used in the design procedure, are described.

3 Modelling of IMDs

In this section, the models used in the design procedure in Fig. 3 are presented, separately for the calculation of electrical quantities (steps 3-5 in Fig. 3), losses and temperatures (step 6), volumes (step 7), and costs (step 8). In addition, a model used for calculating the system reliability is given. Models taken from literature are mainly referenced, whereas new models (iron loss model & redundancy model) are explained in detail.

3.1 Electrical model

Step 3 of the design procedure in Fig. 3 uses basic motor design equations to adapt the number of turns of a given reference motor to the required DC link voltage and to calculate the motor parameters (R, L, Ψ) accordingly [10]. In step 4, the motor/converter voltages and currents are calculated based on known models for non-salient 3-phase PMSMs [11] (6.4) and for non-salient 9-phase PMSMs [12] (5.9). As part of step 4 in Fig. 3, the torque ripple $\Delta T_\mathrm{m} = \max(T_\mathrm{m}) - \min(T_\mathrm{m})$ is calculated based on the transient torque $T_\mathrm{m}(t)$ that is calculated with (1). In (1), N_mod is the number of three-phase modules, $T_{\mathrm{m},i}(t)$ is the transient torque, $v_{\mathrm{bemf,r/s/t},i}(t)$ are the motor back-emfs, and $i_{\mathrm{r/s/t},i}(t)$ are the currents flowing in the i-th 3-phase winding module.

$$T_\mathrm{m} = \sum_{i=1}^{N_\mathrm{mod}} T_{\mathrm{m},i(t)} = \frac{1}{\omega_\mathrm{mech}} \sum_{i=1}^{N_\mathrm{mod}} \left(v_{\mathrm{bemf,r},i} i_{\mathrm{r},i} + v_{\mathrm{bemf,s},i} i_{\mathrm{s},i} + v_{\mathrm{bemf,t},i} i_{\mathrm{t},i} \right) \tag{1}$$

The model for the DC link dimensioning in step 5 of the design procedure, as well as the analytical duty cycle formulas for different modulation schemes are taken from [13].

3.2 Loss model

The inverter losses comprise conduction and switching losses. Both loss types are calculated using the equations given in [14]. For the conduction losses, this includes a scaling of the $R_\mathrm{ds,on}$ of selected reference devices which could be based on the chip area. Instead of such chip area based scaling, $R_\mathrm{ds,on} \propto {}^1/_{I_\mathrm{r}}$ is assumed, where I_r is the rated current of the semiconductor device, and I_r is scaled with the relative semiconductor costs $K_\mathrm{sc,rel,b}$ in the considered model. For the switching losses, the loss energies $E_\mathrm{T,on}$, $E_\mathrm{T,off}$, and $E_\mathrm{D,off}$ of the reference devices at a reference operating point are taken from the datasheet/application note. For the 3LTT-topology, the switching energies are scaled with the same factors that are also used in [13] (Tab. 2.6) to account for the difference between the switching energies occurring in a 3LTT-converter and the loss energies given in the datasheets that are based on a 2L-topology.

In the motor losses, copper losses and iron losses are included. For the copper losses, a frequency and temperature dependent stator resistance $R_\mathrm{ac}(f,T)$ is used, taking the skin effect and the proximity effect into account based on [15] (6.43). For the iron losses, a new model for calculating the iron losses in laminated steel in the frequency domain is applied. The model is given by the following formulas for the iron loss density p_m.

$$p_\mathrm{m} = \bar{K}_\mathrm{h,dc} K_\mathrm{h,0}(f) \hat{B}^2 f + \bar{K}_\mathrm{c,dc} K_\mathrm{c,0}(f) (\hat{B} f)^2 + \bar{K}_\mathrm{e,dc} K_\mathrm{e,0}(f) (\hat{B} f)^{1.5} \tag{2}$$

$$\bar{K}_{h/c/e,\mathrm{dc}} = \{ \frac{1}{N} \sum_{k=1}^{N} K_{h/c/e,\mathrm{dc}}(H_\mathrm{dc}(t_k)), f > 10 f_1; 1, f < 10 f_1 \} \tag{3}$$

Therein, $\hat{B}$ is the peak flux density, f is the frequency, f_1 is the fundamental frequency, $K_\mathrm{h/c/e,0}(f)$ are frequency dependent weighting factors, and $\bar{K}_\mathrm{h/c/e,dc}$ are DC-bias dependent weighting factors. This approach is a variation of the classic Bertotti equation and combines the idea of fitting the Bertotti loss terms (hysteresis, eddy current, excess) to frequencies in the range of PWM harmonics ($\approx 10..100\,\mathrm{kHz}$) [16] (3.22) with the idea of fitting the loss terms to DC-biased excitation [17] (3.7.1). In electric motors the "DC-bias" is given by the fundamental wave excitation and hence (slowly) varies over time. This is taken into account with (3) by calculating the effective DC-bias weighting factors $\bar{K}_{h/c/e,\mathrm{dc}}$ from an averaging of the DC-bias weighting factors at the actual dc excitation $K_{h/c/e,\mathrm{dc}}(H_\mathrm{dc})$, where H_dc is the DC magnetic field strength. The parameter functions $K_\mathrm{h/c/e,0}(f)$ and $K_{h/c/e,\mathrm{dc}}(H_\mathrm{dc})$ are found from a curve fitting of measured iron loss curves where sinusoidal excitation is used.

3.3 Volume model

The considered system volume contributions are the motor volume Vol_motor, the volume of the PCB populated with the DC link capacitors Vol_ppcb, the inverter heat sink volume Vol_hs, and a constant volume of the encoder housing Vol_enc. For the DC link dimensioning, the model from [9] is used and the heat sink volume is obtained from an offline-optimization of a finned heat sink based on [7].

3.4 Cost model

For the inverter costs, the cost model from [18] is used that takes into account the chip cost, consisting of the power semiconductor cost K_sc and the cost of auxiliary ICs K_ic, the capacitor cost K_dc, the PCB cost K_pcb, and

Table II: Formulas for calculating the converter reliability for the converter topologies shown in Fig. 2. The used reliability functions of the power semiconductor devices S1/S2/D5 from Fig. 2 are given by $R_\mathrm{S1} = e^{-\lambda_\mathrm{S1} \cdot t}$, $R_\mathrm{S2} = e^{-\lambda_\mathrm{S2} \cdot t}$, and $R_\mathrm{D5} = e^{-\lambda_\mathrm{D5} \cdot t}$. The value pair $\{k,n\}$ defines the k-out-of-n redundancy for the modular topologies with $k \in [0, n-1]$.

Topology	2L	3L-NPC	3L-TT	2L-nM-ser-k / 2L-n-par-k
Reliability	$R_\mathrm{S1}^6 =: R_\mathrm{2L}$	$R_\mathrm{S1}^{12} \cdot R_\mathrm{D5}^6$	$R_\mathrm{S1}^6 \cdot R_\mathrm{S2}^6$	$\sum_{i=0}^{k} \binom{n}{i} (R_\mathrm{2L})^{(n-i)} (1-R_\mathrm{2L})^i$

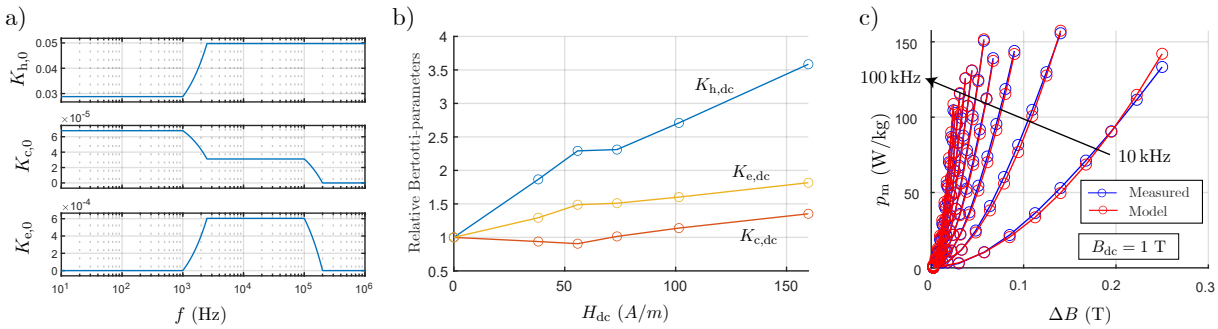

Figure 5: a) Frequency dependent loss parameters and b) DC-bias dependent loss parameters for the parametrization of the iron loss model. c) Measurement vs. model with DC-bias.

the heat sink cost K_{hs}. The motor costs K_{mot} are approximated based on the costs of the copper windings, the iron laminations, and the magnets. The motor costs are assumed to be constant (constant copper fill factor). Concerning the parametrization of the cost model, the specific prices from [18] are used for K_{dc}, K_{pcb}, and K_{hs}, whereas K_{sc} & K_{ic} are parametrized based on the cost study presented in section 4.1.

3.5 Thermal model

For the thermal model, a lumped parameter thermal network (LPTN) is used, where the motor part is based on [19] and the converter part is based on [7]. Solving the LPTN is an iterative process, as shown in Fig. 3, because the copper losses, the conduction losses, and the thermal resistance of the finned heat sink are temperature dependent.

3.6 Reliability model

2L-*n*M-ser- & 2L-*n*M-par-converters can be designed with a *k*-out-of-*n*-redundancy, which means that up to *k* 2L-modules can fail while the system can still operate (in part-load). On the one hand, such redundancy improves system reliability. On the other hand, the higher component count of the modular topologies compared to a 2L-converter degrades system reliability due to the higher risk of component failure. Given these contrary effects, the question is, if the modular topologies 2L-*n*M-ser & 2L-*n*M-par overall have an advantage over the 2L- and 3L-topologies in terms of reliability. To answer this question, a reliability model is built that is based on the following three definitions according to [20].

1. The *reliability* $R(t)$ of an item is defined as the probability that an item can perform a required function under given conditions for a given time interval $[0,t]$.
2. The *failure rate* $\lambda(t)$ of an item is defined as the average number of failing items per time unit normalized to the total number of still good/working items at the time instant t.
3. The *Mean-Time-To-Failure MTTF* is defined as $\int_0^\infty R(t)dt$.

To calculate the reliability of a system consisting of multiple items, the reliabilities of these items are combined in one of the following two ways depending on the type of redundancy: 1) If the items are non-redundant, their reliability functions (i.e. probabilities of working) are multiplied. 2) If the items are redundant, the overall reliability corresponds to the sum of the probabilities of all working combinations. This concept is applied to all considered

Table III: Design space limits for the operational DOFs in Fig. 3.

Switching frequency f_s	1 kHz…100 kHz
Relative semiconductor cost $K_{sc,rel,b}$	0…1
Heat sink fin length c_{hs}	0 mm…30 mm

Table IV: Benchmark system parameters.

System configuration {*Top-PWM-SC-W*}	2L-Sin-Si-3ph
Switching frequency f_s	26.28 kHz
Relative semiconductor cost $K_{sc,rel,b}$	0.0764
Heat sink fin length c_{hs}	1 mm
System power density $\rho_{sys,ref}$	0.1291 kW L^{-1}
System efficiency $\eta_{sys,ref}$	86.05 %
System cost $K_{sys,ref}$	190.45 CHF
Motor cost K_{mot}	138.18 CHF

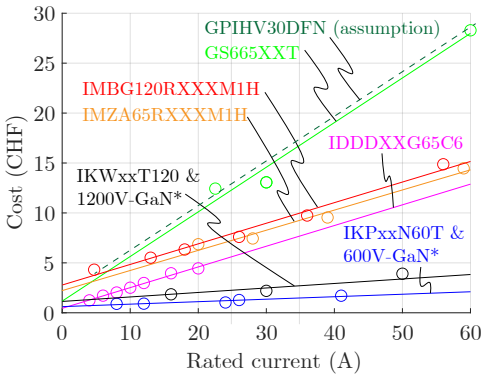

Figure 6: Chip cost as a function of rated current/chip size based on distributor prices for an order volume of 1000 pieces.

Table V: System specifications and design constraints of a general-purpose, high-torque, low-speed IMD.

Rated power P_N	1.5 kW	Max. junction temperature $T_{j,max}$	125 °C/150 °C
Rated torque $T_{m,N}$	48 Nm	Max. electronics ambient temperature $T_{e,amb,max}$	80 °C
Rated speed $n_{n,N}$	300 rpm	Max. winding temperature $T_{w,max}$	130 °C
DC link voltage V_{dc}	800 V	Max. encoder temperature $T_{enc,max}$	80 °C
Max. static DC link voltage ripple $\Delta V_{dc,max,s}$	$0.01 V_{dc}$	Max. torque ripple $\Delta T_{m,max}$	0.5 Nm
Max. dynamic DC link voltage ripple $\Delta V_{dc,max,d}$	$0.125 V_{dc}$	Min. PCB height $T_{pcb,min}$	15 mm
Max. load step $\Delta i_{dc,out}/I_{mod}$	1	Insulation layer thickness l_{ins}	0 mm
Ambient temperature T_{amb}	40 °C	Semiconductor cost budget $K_{sc,b}$	190.2 CHF
Flange temperature T_f	65 °C		

converter topologies (Fig. 2), where the items are given by the power semiconductor devices. Considering a constant failure rate over time for each device, the reliability of a single device, e.g. switch S1 of the 2L-topology, is given by $R_{S1} = e^{-\lambda_{S1} \cdot t}$ [20]. The resulting formulas for calculating the converter reliability are summarized in Tab. II. The reliability results for a specific number of modules and for a specific failure rate are given in section 5.

4 Application of the design procedure

The design procedure presented in Fig. 3 is applied to the optimization of a 1.5 kW IMD. In the following, first the design setup is given. Then, the optimization results are presented and discussed.

4.1 Design setup - Specifications, constraints, and design space

The considered system specification, design constraints, and the design space limits of the operational DOFs are summarized in Tab. V & III. The parameters of the benchmark system used for the definition of the relative system cost $K_{sys,rel} := K_{sys}/K_{sys,ref}$ are given in Tab. IV. Tab. VI shows the selected reference power semiconductor devices and the cost parameters obtained from a cost study of the corresponding device series. The results of this study are shown in Fig. 6, indicating that the considered WGB devices (SiC/GaN) are 5 to 10 times more expensive than conventional Si IGBTs of the same current rating. However, as the production of GaN devices is based on silicon substrate, the cost of GaN is expected to reach the level of Si devices in the long run. Therefore, GaN HEMTs are considered in two "cost versions": 1) Based on present costs, denoted as GaN, and 2) with future costs which are assumed to be equal to the costs of Si IGBTs as indicated in Fig. 6. These devices are denoted as GaN* in the following.

The parameters used in the iron loss model are given in Fig. 5a & b. These parameters are obtained from a curve fitting of the iron loss density curves shown in Fig. 5c, which originate from iron loss measurements performed with a BH-analyzer (IWATSU SY-8219) and a DC-bias tester (IWATSU SY-960).

The parameters used for the semiconductor loss model are shown in Fig. 7a-d. Fig. 7a & b show the switching energies of the reference devices which decrease from Si IGBTs to SiC MOSFETs to GaN/GaN* HEMTs, as expected. Compared to MOSFETs and HEMTs, IGBTs have an on-state resistance with a strong dependency on the current. Therefore, in order to compare the conduction loss behavior of MOSFETs, HEMTs, and IGBTs on the device level, an effective on-state resistance $R_{ds,on,eff}$ is defined as the on-state resistance at a typical operating current which is assumed to be equal to $1/3$ of the rated current. Fig. 7c & d show that, for the same cost per transistor, the static losses increase from GaN* HEMTs to Si IGBTs to SiC MOSFETs to GaN HEMTs. The fact that the effective on-state resistance of GaN* HEMTs (i.e. GaN HEMTs with future expected costs) is lower than the one of the considered Si IGBTs is due to the following two reasons: 1) As previously mentioned, it is assumed that, for the same cost per device, GaN* HEMTs have the same rated current as the considered Si IGBTs (Fig. 6). 2) Due to that assumption, the effective on-state resistance of the reference devices is scaled to the same rated current (using $R_{ds,on} \propto 1/I_r$), for which the considered GaN HEMTs have a lower $R_{ds,on,eff}$ than the Si IGBTs.

4.2 Optimization results

In this section, the pareto-optimal IMD designs resulting from the design procedure in Fig. 3 are analysed. Therefore, in a first part, the pareto-front is shown and an overall optimal system configuration is suggested. In a second

Table VI: Reference power semiconductor devices, selected as the devices with the largest current rating within each device series with the same package dimensions. Given parameters: Rated current $I_{r,25\,°C}$, cost parameters a_{sc} & b_{sc}, and maximum junction temperature $T_{j,max}$. As the switching energies $E_{on/off}$ of the 1200V GaN HEMT are not provided in literature, it is assumed that these scale with $V_{ds,max}$ like the switching energies of SiC MOSFETs, i.e. $E_{on/off,T6} = E_{on/off,T3} \cdot (E_{on/off,T5}/E_{on/off,T2})$.

ID	Device type	$I_{r,25\,°C}$ (A)	Name	a_{sc} (CHF/A)	b_{sc} (CHF)	$T_{j,max}$ (°C)	Source of $E_{on/off}$
T1	600 V Si IGBT	41	IKP20N60T	0.0443	1.097	175	Datasheet
T2	600 V SiC MOSFET	59	IMZA65R027M1H	0.2016	2.22	150	Application note [21]
T3	600 V GaN HEMT	30	GS66508T	0.7976	2.083	150	Datasheet
T4	1200 V Si IGBT	75	IKW40T120	0.0802	2 .026	150	Datasheet
T5	1200 V SiC MOSFET	56	IMBG120R030M1H	0.2063	2.778	175	Datasheet
T6	1200 V GaN HEMT	30	GPIHV30DFN	0.7976	3.083	150	Assumption
D1	600 V SiC Diode	51	IDDD20G65C6	0.2073	0.4457	175	-

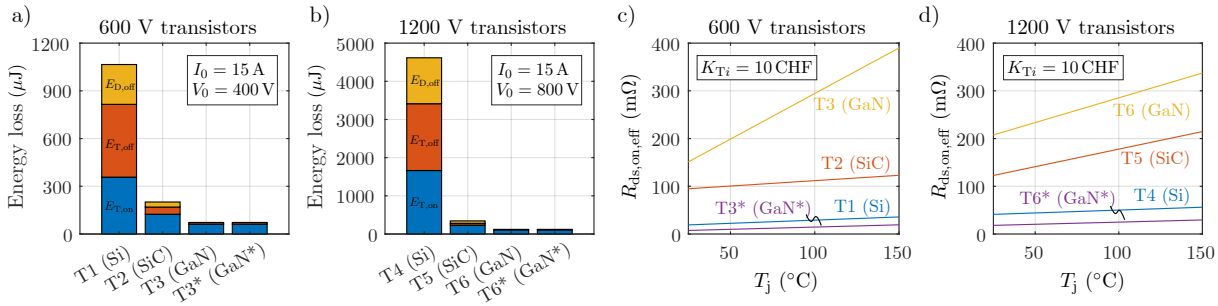

Figure 7: a) & b) Switching loss energies of the reference devices from Tab. VI, based on the scaling of one $E_x(I)$-value pair from the datasheet/application note which is scaled to the switched current I_0 and voltage V_0. c) & d) Effective on-state resistance of the reference devices over the junction temperature, scaled to the same cost per device $K_{T,i}$. The values in a)-d) are used to parametrize the semiconductor loss model described in section 3.2.

part, the considered semiconductor technologies, PWM schemes, and topologies are compared with regard to the maximum system efficiency at approximately equal system cost and volume.

4.2.1 Investigation of the pareto-optimal designs

Fig. 8a shows the pareto-front of the pareto-optimal IMD designs in the $(\rho_{sys}, \eta_{sys}, K_{sys,rel})$-space resulting from the design procedure in Fig. 3, where only the present costs of semiconductor technologies Si/SiC/GaN are considered, i.e. GaN* is not considered. Fig. 8a, shows six pareto-optimal {*Top-PWM-SC-W*}-configurations (i.e. system configurations in terms of the topology, the PWM scheme, the semiconductor technology, and the winding scheme). These configurations are color-coded by means of the colored configuration names in Fig. 8a & b. The overall optimal/best configuration depends on how the design objectives $(\rho_{sys}, \eta_{sys}, K_{sys,rel})$ are weighted. This is shown in Fig. 8b which displays the color of the configuration that minimizes the scalar cost function $f_s = w_\rho(-\rho_{sys}/\rho_{sys,ref}) + w_\eta(-\eta_{sys}/\eta_{sys,ref}) + w_K(K_{sys}/K_{sys,ref})$, as a function of the weighting factors w_ρ & w_η with the constraint $w_\rho + w_\eta + w_K = 1$. To illustrate how to read Fig. 8b, an exemplary point at $w_\rho = 0.1$, $w_\eta = 0.2$, and $w_K = 1-(w_\rho + w_\eta) = 0.7$ is indicated in Fig. 8b. The color at that point belongs to the configuration *2L-OC-Si-3ph*, indicating that this is the overall optimal configuration for the weighting factors at the considered exemplary point.

Fig. 8a & b show that the cost-optimal system configuration is *2L-OC-Si-3ph*, the most efficient configuration is *2L3Mpar-OC-GaN-9ph*, and the highest power density is reached by all configurations (in the case of no cooling fins). For a compromise between costs and efficiency, the least expensive IMD of the most efficient system configuration, i.e. of the configuration *2L3Mpar-OC-GaN-9ph*, is suggested as the overall optimal IMD (IMD_{sg} in Fig. 8a). Fig. 8a shows that the suggested IMD enables an efficiency increase of $+2.26\,\%$ (i.e. percentage points) at the expense of $36\,\%$ higher costs compared to the cost-optimal IMD (IMD_{co} in Fig. 8a).

The same analysis is performed now including the future expectation of GaN HEMT costs (GaN*). The result is shown in Fig. 8c & d, indicating that only two GaN*-based system configurations are on the pareto-front. Hence, for the considered specification, GaN HEMTs are expected to outperform Si IGBTs and SiC MOSFETs in the future. As shown in Fig. 8c & d, the cost-optimal configuration is now *2L-OC-GaN*-3ph* and the most efficient configuration is *2L3Mpar-OC-GaN*-9ph*. The suggested IMD (IMD^*_{sg} in Fig. 8c) now enables $0.65\,\%$ more efficiency for $23\,\%$ more costs, compared to the future expected cost-optimal IMD (IMD^*_{co} in Fig. 8c).

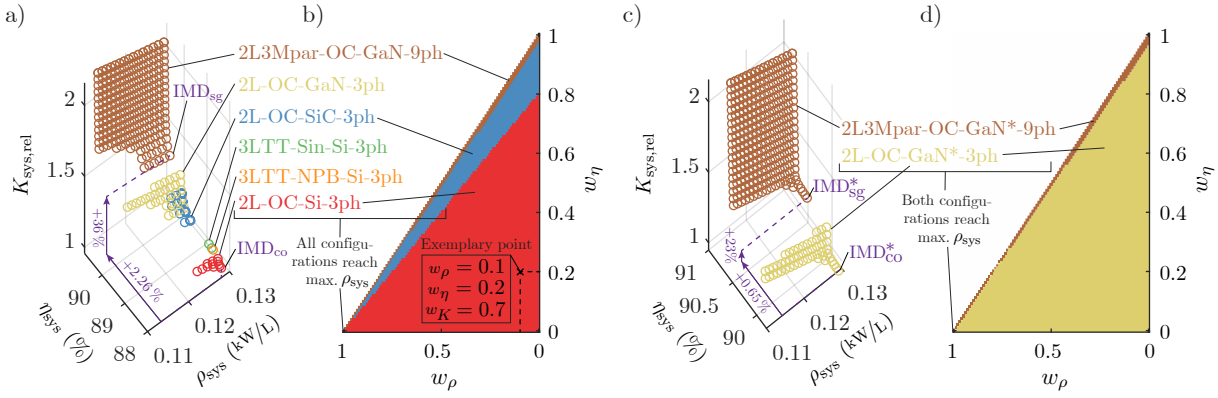

Figure 8: a) Pareto-front of the pareto-optimal IMD designs resulting from the design procedure in Fig. 3 and from the system specification in Tab. V, considering present semiconductor prices (i.e. Si/SiC/GaN). b) Overall optimal system configuration as a function of the weighting factors w_ρ & w_η of the cost-function $f_s = w_\rho(-\rho_{sys}/\rho_{sys,ref}) + w_\eta(-\eta_{sys}/\eta_{sys,ref}) + w_K(K_{sys}/K_{sys,ref})$ with $w_K = 1-(w_\rho + w_\eta)$. c) & d) Analog results to a) & b), considering expected future GaN prices (i.e. Si/SiC/GaN*).

4.2.2 Comparison at equal cost and volume

While the previous analysis revealed the best system configurations for the given system specification, in a next step, the impact of the different semiconductor technologies, PWM schemes, and topologies on the system performance is investigated. For that purpose, all system configurations defined in Tab. I are compared with regard to maximum system efficiency/minimum system losses $P_{\mathrm{sys,loss,opt}}$ at approximately equal system cost $K_{\mathrm{sys,rel}} = 1.8 \pm 0.03$ and approximately equal system volume $Vol_{\mathrm{sys}} = 12.89\,\mathrm{L} \pm 0.17\,\mathrm{L}$. These intervals for $K_{\mathrm{sys,rel}}$ & Vol_{sys} are chosen so that all considered system configurations can be compared. In other intervals some configurations might not have a solution because the ranges of $K_{\mathrm{sys,rel}}$ & Vol_{sys} are different for each configuration.
Fig. 9 shows the resulting cost distribution, volume distribution, and optimal power loss distribution as bar plots, as well as a table listing the corresponding optimal design parameters ($f_{\mathrm{sw,opt}}$, $K_{\mathrm{sc,rel,b,opt}}$, $c_{\mathrm{hs,opt}}$), the efficiency gain compared to the reference system (Tab. IV), and the optimum type (*opttype*). The optimum type indicates

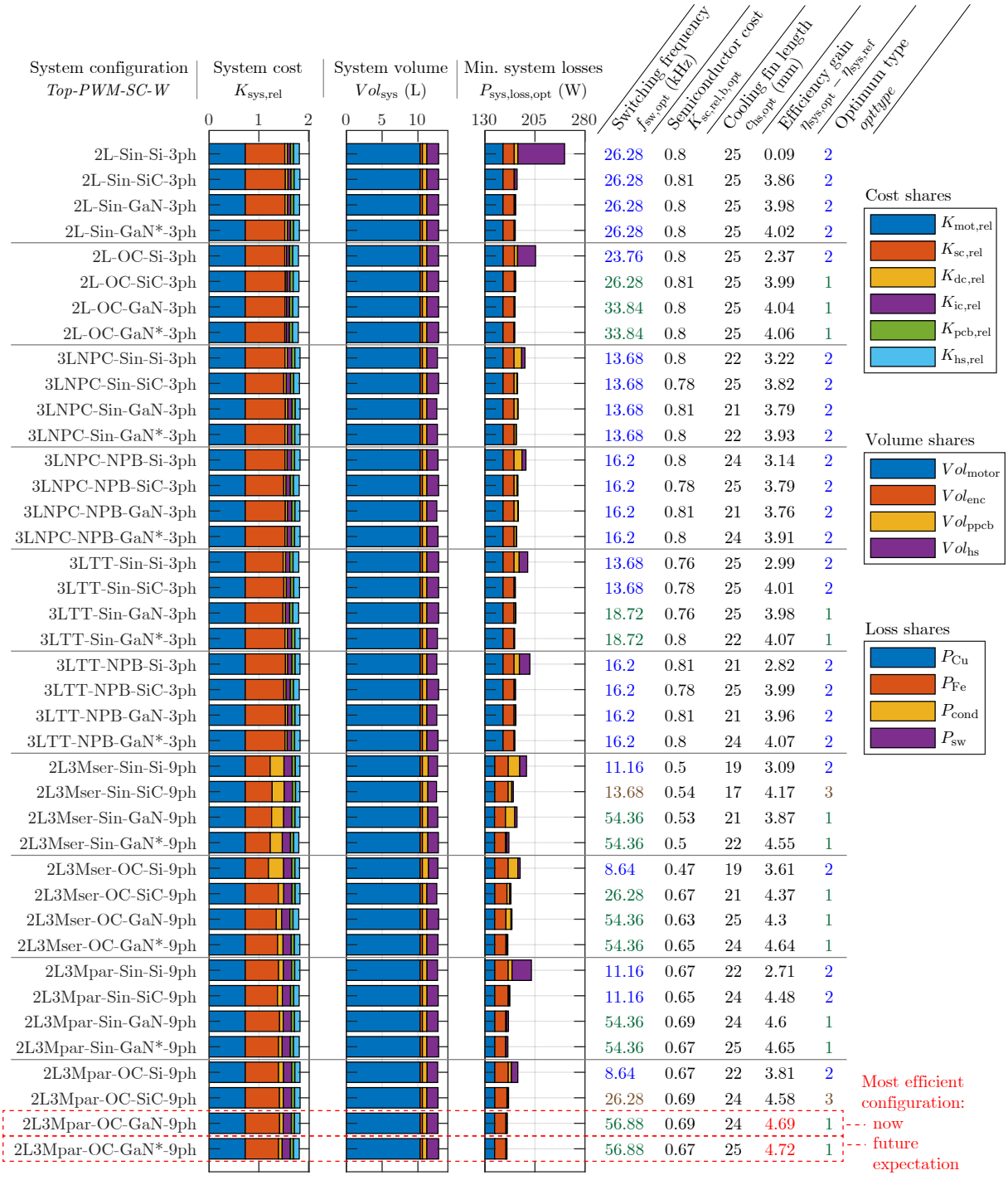

Figure 9: System performance resulting from the design procedure in Fig. 3 at approximately equal system cost $K_{\mathrm{sys,rel}}$, volume Vol_{sys}, and minimized losses $P_{\mathrm{sys,loss,opt}}$ for all system configurations defined in Tab. I. Bar plots: Distribution of system cost, volume, and losses. Table on the right: Optimal design parameters ($f_{\mathrm{sw,opt}}$, $K_{\mathrm{sc,rel,b,opt}}$, $c_{\mathrm{hs,opt}}$), efficiency gain with regard to the reference system (Tab. IV), and the optimum type that indicates what determines the optimum design parameters.

what determines the optimal design parameters as explained in the following. The optimal semiconductor costs $K_{\mathrm{sc,rel,b,opt}}$ and the optimal cooling fin length $c_{\mathrm{hs,opt}}$ are determined by the upper limits of the already mentioned cost and volume intervals for all considered system configurations. However, different cases are identified for the optimal switching frequency $f_{\mathrm{sw,opt}}$: For $opttype = 1$, $f_{\mathrm{sw,opt}}$ results from an optimal balance between the switching losses and the harmonic motor losses. That is, for switching frequencies lower than $f_{\mathrm{sw,opt}}$, the harmonic motor losses increase faster than the switching losses decrease, so that the system efficiency decreases. For $opttype = 2$, $f_{\mathrm{sw,opt}}$ lies on the boundary defined by the torque ripple constraint $\Delta T_{\mathrm{m}} < \Delta T_{\mathrm{m,max}}$. That is, for switching frequencies lower than $f_{\mathrm{sw,opt}}$, the torque ripple exceeds $T_{\mathrm{m,max}}$. For $opttype = 3$, $f_{\mathrm{sw,opt}}$ lies on the boundary defined by the upper cost limit of this analysis $K_{\mathrm{sys,rel}} < 1.83$. That is, for switching frequencies lower than $f_{\mathrm{sw,opt}}$, the cost exceeds its limit (as larger and hence more expensive capacitors are required to keep the DC link voltage ripple constant). In the following, the semiconductor technologies, modulation schemes, and topologies are compared, based on the results shown in Fig. 9.

Table VII: Comparison of semiconductor technologies. The most efficient variant is printed in bold.

Topology-PWM	$\eta_{\mathrm{sys,opt,ref}}$ Si	$\eta_{\mathrm{sys,opt}} - \eta_{\mathrm{sys,opt,ref}}$ SiC	GaN	GaN*
2L-Sin	86.14	3.77	3.89	**3.93**
2L-OC	88.41	1.63	1.68	**1.70**
3LNPC-Sin	89.26	0.61	0.57	**0.72**
3LNPC-NPB	89.19	0.65	0.62	**0.77**
3LTT-Sin	89.04	1.02	0.99	**1.08**
3LTT-NPB	88.86	1.18	1.15	**1.26**
2L3Mser-Sin	89.13	1.09	0.79	**1.46**
2L3Mser-OC	89.66	0.76	0.68	**1.03**
2L3Mpar-Sin	88.76	1.77	1.89	**1.94**
2L3Mpar-OC	89.86	0.77	0.88	**0.91**

Table VIII: Comparison of PWM schemes. The most efficient variant is printed in bold.

Topology (2L)	$\eta_{\mathrm{sys,opt,ref}}$ Sin-PWM	$\eta_{\mathrm{sys,opt}} - \eta_{\mathrm{sys,opt,ref}}$ OC-PWM
2L	90.07	**0.04**
2L3Mser	90.59	**0.10**
2L3Mpar	90.70	**0.07**
Topology (3L)	Sin-PWM	NPB-PWM
3LNPC	**89.98**	-0.02
3LTT	**90.12**	0.00

1) *Comparison of semiconductor technologies (Si/SiC/GaN/GaN*)*
Based on the efficiency gain given in Fig. 9, Tab. VII compares the maximum efficiency achieved with different semiconductor technologies (Si/SiC/GaN/GaN*) for each combination of topology and PWM scheme, where Si IGBTs are used as a reference. The following conclusions are drawn from Tab. VII: 1) For the considered specification, Si IGBTs are the least efficient, which is expected due to the high switching loss energies (Fig. 7a & b). 2) In general, GaN HEMTs are expected to be the most efficient technology in the future (at the same cost & volume). 3) In general, and in particular for SiC vs. GaN for the considered system specification, which semiconductor technology is more efficient cannot be determined just based on the device level characteristics. Instead, whether one technology is more efficient than the other depends on the device level characteristics (Fig. 7), the used combination of topology and PWM scheme (which influences the $P_{\mathrm{sw}}/P_{\mathrm{cond}}$-ratio), and the optimal switching frequency that depends on the design constraints such as the torque ripple constraint.

2) *Comparison of modulation schemes*
Based on the efficiency gain given in Fig. 9, Tab. VIII compares the maximum efficiency achieved with different PWM schemes for each topology (taking the maximum over Si/SiC/GaN/GaN*), where Sin-PWM is used as a reference. The following conclusions are drawn from Tab. VIII: 1) For the 2L-topologies (2L, 2L3Mser, 2L3Mpar) with the considered system specification, OC-PWM is more efficient than Sin-PWM, as expected, because OC-PWM avoids switching of the phase-leg with the largest current, thereby reducing switching losses. 2) For the 3LNPC-topology and the considered specification, NPB-PWM leads to slightly higher switching losses due to an additional space vector used in every switching period. 3) For the 3LTT-topology with the considered system specification, Sin-PWM & NPB-PWM reach approximately the same efficiency because the loss-related disadvantage of the additional space vector of NPB-PWM is compensated by a lower switching frequency of 3LTT-NPB-GaN*-3ph compared to 3LTT-Sin-GaN*-3ph in Fig. 9. 4) In general, the most efficient PWM scheme cannot be determined just based on a simple comparison at equal switching frequency but the most-efficient PWM scheme depends also on the optimum switching frequency and hence also on the design constraints.

3) *Comparison of topologies*
Based on the efficiency gain given in Fig. 9, Tab. IX compares the maximum efficiency achieved with different topologies (taking the maximum over all combinations of Si/SiC/GaN/GaN* and PWM schemes). The following conclusions are drawn from Tab. IX: 1) For the considered specification, the topology 2L3Mpar has the best efficiency with $+0.66\,\%$ higher efficiency than the 2L-topology. 2) For the considered specification, the modular topologies (2L3Mpar/2L3Mser) enable an efficiency increase of $+0.65\,\%$ compared

Table IX: Comparison of topologies. The most efficient variant is printed in bold.

$\eta_{\text{sys,opt,ref}}$	$\eta_{\text{sys,opt}} - \eta_{\text{sys,opt,ref}}$				$\eta_{\text{sys,opt,ref}}$	$\eta_{\text{sys,opt}} - \eta_{\text{sys,opt,ref}}$
2L	3LNPC	3LTT	2L3Mser	2L3Mpar	2L/3LNPC/3LTT	2L3Mser/2L3Mper
90.11	-0.13	0.01	0.58	**0.66**	90.12	**0.65**

to the non-modular topologies (2L/3LNPC/3LTT), which is due to the higher winding factor of the 9-phase winding that reduces the motor losses. Indeed, Fig. 9 shows lower copper losses P_{Cu} for all configurations with modular topologies compared to the configurations with standard/non-modular topologies. The fact that the modular topologies can be combined with 9-phase windings with a higher winding factor than 3-phase windings is a general advantage of these topologies.

5 Reliability analysis

The considered converter topologies are also compared with regard to the reliability based on the model given in section 3.6 for the reliability related system specification summarized in Tab. X. For simplicity, the same failure rate of $\lambda = 500$ fit is assumed (which is chosen based on Fig. 6 in [22]) for all power semiconductor devices, where 1 fit corresponds to 1 *failure in time* with a reference time interval of 10^9 hours. The 2L-*n*M-ser-topology is analyzed with 3 modules ($n = 3$) and for three different redundancy configurations (no redundancy ($k = 0$), 1-out-of-3-redundancy ($k = 1$), and 2-out-of-3-redundancy ($k = 2$)) to investigate the effect of redundancy on the reliability. The 2L-*n*M-par-topology is not separately listed, as the model equations in Tab. II already indicate that both modular topologies (2L-*n*M-ser & 2L-*n*M-par) have the same reliability.
Tab. X shows the results for the absolute mean time to failure *MTTF* and for the relative mean time to failure with regard to the 2L-topology, $MTTF_{\text{rel,2L}}$. Note that the *MTTF* depends on λ, whereas the $MTTF_{\text{rel,2L}}$ is independent of λ. The resulting values for the $MTTF/MTTF_{\text{rel,2L}}$ show that the modular topologies without any redundancy ($k = 0$) are as reliable as the 3L-NPC but less reliable than 2L and 3L-TT. With a 1-out-of-3-redundancy, the reliability of the modular topologies increases, as expected, but is still lower than the one of the 2L-topology. This shows that for a 1-out-of-3-redundancy, the higher risk of component failure due to more components of the modular topologies outweighs the redundancy effect on the reliability. Only for a 2-out-of-3-redundancy, the modular topologies are more reliable in terms of the *MTTF* than the 2L-topology. It should be noted that for 2L-*n*M-ser and for a given DC link voltage, a higher redundancy level implies a higher required voltage rating of the power semiconductor devices, whereas for 2L-*n*M-par there is no such additional design requirement.

Table X: Reliability related system specification and results of the reliability analysis.

Topology	Device failure rates (fit)	Redundancy	$MTTF$ (years)	$MTTF_{\text{rel,2L}}$
2L	$\lambda_{S1} = 500$	-	38.1	1
3L-NPC	$\lambda_{S1} = \lambda_{D5} = 500$	-	12.7	1/3
3L-TT	$\lambda_{S1} = \lambda_{S2} = 500$	-	19.0	1/2
2L-*n*M-ser	$\lambda_{S1} = 500$	$\{k,n\} = \{0,3\}$	12.7	1/3
2L-*n*M-ser	$\lambda_{S1} = 500$	$\{k,n\} = \{1,3\}$	31.7	5/6
2L-*n*M-ser	$\lambda_{S1} = 500$	$\{k,n\} = \{2,3\}$	69.8	11/6

6 Conclusion

The following conclusions are drawn:

- A procedure for the optimal design of IMDs in terms of ρ_{sys}, η_{sys}, and K_{sys} is presented. The design procedure incorporates a new iron loss model and enables the comparison of modular converter topologies (2L3Mser/2L3Mpar) to standard/non-modular topologies (2L/3LNPC/3LTT) covering a large design space including different PWM variants, semiconductor technologies (Si/SiC/GaN), and winding schemes.
- For a 1.5 kW IMD, the cost-optimal system configuration is 2L-OC-Si-3ph. Compared to this, the suggested design has the configuration 2L3Mpar-OC-GaN-9ph and enables an efficiency increase of $+2.26\,\%$ at $36\,\%$ higher cost. Assuming a utilization of $90\,\%$ and an energy price of $0.1\,\text{CHF/kWh}$, the higher costs are compensated by the lower energy consumption after approximately 2 years.
- For a 1.5 kW IMD, different topologies, PWM schemes, and semiconductor technologies are compared with regard to maximum efficiency at equal system cost and volume. Modular topologies reach higher efficiencies than the standard topologies due to the general advantage that modular topologies can be combined with multiphase windings. The optimal PWM scheme and the optimal semiconductor technology cannot be predicted in general, as they depend on the system specification, such as the torque ripple constraint.
- A model for comparing the system reliability of standard topologies and of modular topologies is presented. The modular topologies 2L3Mser and 2L3Mpar only have an advantage over the standard 2L- and 3L-topologies, if a 2-out-of-3-redundancy is achieved.

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