Boost/Buck-boost Based Grid Connected Solar PV Micro-inverter with Reduced Number of Switches and Having Power Decoupling Capability

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Keywords

≪DC-AC converter≫, ≪Grid-connected inverter≫, ≪Renewable energy systems≫, ≪Transformerless PV inverter≫, ≪Micro-inverter≫ ≪Power Decoupling≫.

Abstract

A boost/buck-boost based transformer-less micro-inverter suitable for interfacing a 35 V, 220 W PV module to a single phase 220 V ac grid is proposed in this paper. The intermediate capacitor between the the boost stage and the buck-boost stage helps in achieving power decoupling between the dc side and the ac side. Since the inverter is endowed with inherent power decoupling feature, it is more reliable compared to the inverters utilizing high value electrolytic capacitors. The micro-inverter utilizes six switches, two of them operating at high frequency, two at line frequency and the rest two switches operate at high frequency either during the positive half cycle or in the negative half cycle. Both the boost stage and buck-boost stage is operated in discontinuous conduction mode for all possible operating conditions in order to achieve higher voltage gain, and negligible turn on losses of the high frequency switches. The direct connection between the negative terminal of the PV module and the grid neutral ensures the leakage current flow to be zero. The analyses of the proposed micro-inverter is carried out. The viability if the proposed scheme is validated by detailed simulation studies in the MATLAB/Simulink platform.

Introduction

The renewable energy resources are becoming more popular in the whole world as they are environment-friendly and inexhaustible in nature. In countries like India, where the sunlight is abundant throughout the year, solar power generation is a viable alternative to the conventional fossil fuel based electricity generation. In order to integrate the solar photovoltaic (PV) systems to the existing ac grids the extracted power must be processed through an inverter. In case of grid connected rooftop solar PV inverters, micro-inverters are becoming more popular over central or string inverters as they offer modularity, plug and play feature and for their capability of extracting maximum available power from each PV module [1]. However due to smaller power rating and higher voltage gain requirement, the efficiency is poor compared to central or string inverters. In order to improve the efficiency of a micro-inverter, less number of power conversion stages are desired [2, 3]. Hence transformer-less single stage topologies are taken into consideration.

In most of the countries the distribution voltage level is 220-230 V. Interfacing a 35 V PV module to a 220 V ac grid without using a transformer is a major challenge. Further in case of a transformer-less micro-inverter topology, the leakage current issue also needs to be considered [4, 5]. The micro-inverter topologies reported in [6–16] are doubly grounded, i.e, the negative terminal of the PV module is directly connected to the grid neutral. Hence the leakage current flow is zero in the aforementioned micro-inverters. However, the micro-inverters reported in [6–12, 14, 15] are not suitable for interfacing a 35 V module to a 220 V ac grid as they offer lower voltage gain and suitable for interfacing to a 110 V ac grid. The micro-inverters reported in [13, 16, 17] are suitable for interfacing a 35 V PV module to 220 V ac grid. However, the leakage current issue has not been addressed in [17].

In case of single phase inverters, there is a mismatch in the instantaneous power between the dc side and the ac side, which leads to significant second order harmonic ripple in the dc bus voltage. However, such ripple in the voltage across PV terminals decreases the maximum power point tracking (MPPT) efficiency [18, 19]. The simplest and cheapest solution to this issue is to connect a high value capacitor across the PV module such that the voltage ripple across it becomes low. If the voltage ripple has to be less the 5%, the capacitance needs to be connected across a 35 V, 220 W PV module is more than 13 mF as per the design guidelines provided in [20]. However, the usage of electrolytic capacitor is not a reliable solution as their lifetime is very poor compared to a PV module. High value thin film capacitor is also not a practical solution for a micro-inverter as it would increase the volume and cost of the inverter significantly. It is to be noted that, the micro-inverters reported in [6, 8, 9, 11–15, 17] do not have the power decoupling capability and hence a large value capacitor needs to be connected across the PV terminals. A viable solution to this issue is to connect an additional active power decoupling circuit (APDC) across the PV module, wherein the value of capacitance required is significantly less and hence thin film capacitors can be utilized. A number of APDC are reported in [20–22]. However, APDC required two additional high frequency (HF) switches and an inductor, which add losses to the system. Hence attempts have been made to achieve the power decoupling inherently in the main micro-inverter circuit [7, 10, 16].

Among all the aforementioned micro-inverters, only the topology reported in [16] has all of the following features:

- It is suitable for interfacing a 35 V PV module to a 220 V ac grid.
- It is doubly grounded, and hence the leakage current flow is zero.
- It is having the inherent power decoupling capability.

However that micro-inverter utilizes seven switches. Further it is operated in continuous conduction mode (CCM) for all possible operating conditions. Hence the duty ratio of the boost stage is as high as 0.85. Also the volume of the inductors are significantly high. In order to overcome all the aforementioned drawbacks of micro-inverter reported in [16], a micro-inverter having only six switches are proposed in this paper. The micro-inverter is having inherent power decoupling capability and suitable for interfacing a 35 V PV module to a 220 V ac grid. The leakage current issue is also been addressed. The proposed micro-inverter is operated in discontinuous conduction mode (DCM) in order to achieve (i) same voltage gain at lower duty ratio, (ii) reduction in volume of the inductors and (iii) negligible turn on losses of the HF switches. A detailed simulation studies on the proposed micro-inverter is carried out to confirm its viability.

Principle of the Proposed Topology

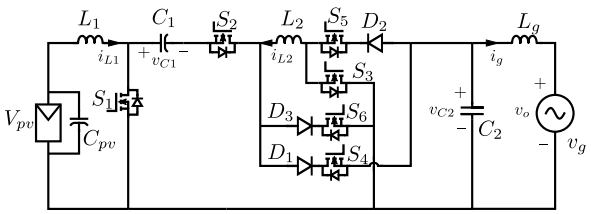

Fig. 1: Schematic diagram of the proposed micro-inverter

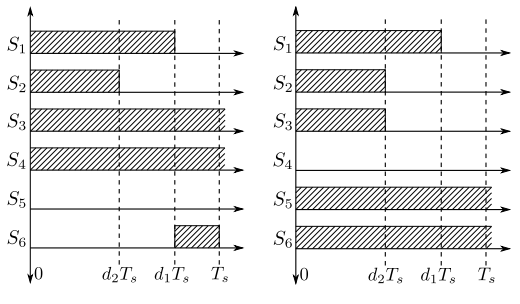

Fig. 2: Switching pulses: (a) positive half cycle and (b) negative half cycle

The schematic diagram of the proposed micro-inverter topology is shown in Fig. 1. This inverter topology is also realized by integrating a boost stage followed by a buck-boost stage as is the case in [16]. However, the topological configuration is modified and hence the number of switches is reduced to six. The intermediate capacitor, C_1 acts as a coupling element between the boost stage and the buck-boost stage, and it is also used for power decoupling. The duty ratio of the boost stage, d_1 is used to control the

current drawn from the PV module and maintain the converter operating at MPP. The duty ratio of the buck-boost stage, d_2 is used to maintain the voltage across C_1, and accordingly the power is fed to the grid. The gating pulses are given to the switches as shown in Fig. 2. It is to be noted that the switches, S_1 and S_2 operate HF, S_4 and S_5 ant line frequency (LF), and the remaining two switches, S_3 and S_6 operates at HF for either in positive half cycle (PHC) or in negative half cycle (NHC) of the grid voltage. The switching time period, T_s can be divided into three intervals. In case of this configuration of the inverter, the inductor, L_2 has to be designed in such a way that the current through it has to be become zero before $d_1 T_s$ for all operating conditions. The current through L_1 is also discontinuous.

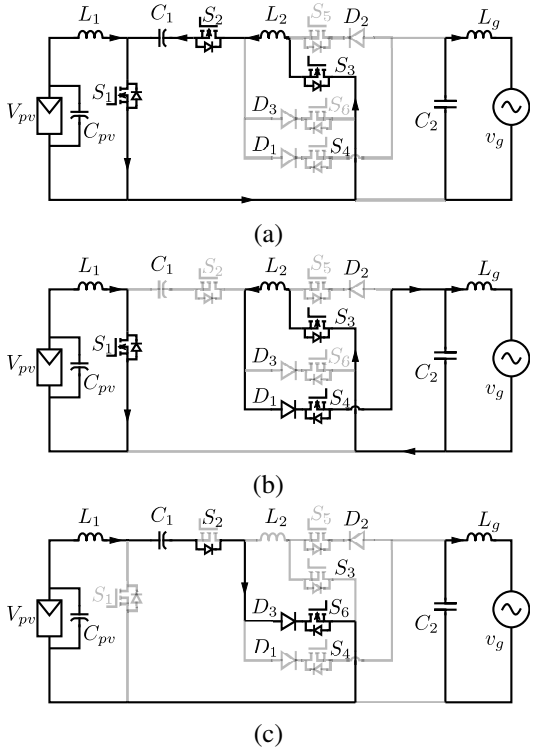

Fig. 3: Modes of operation for PHC: (a) Mode-I, (b) Mode-II, and (c) Mode-III

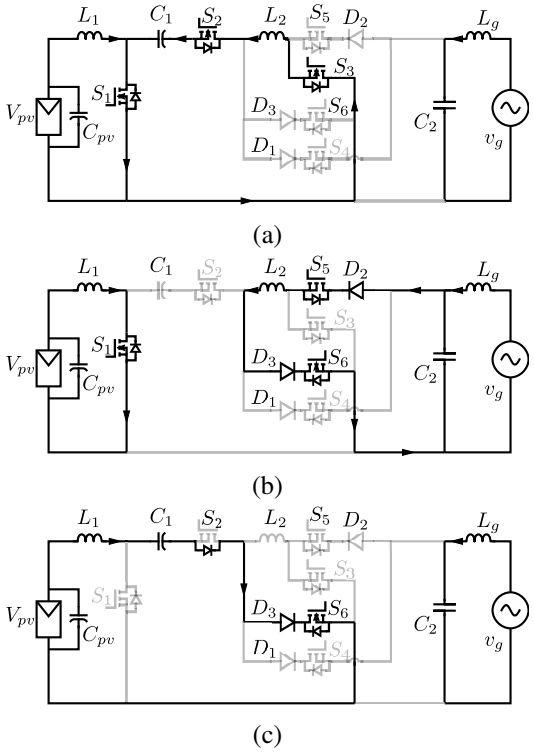

Fig. 4: Modes of operation for NHC: (a) Mode-I, (b) Mode-II, and (c) Mode-III

Positive Half Cycle

The modes of operation in PHC are shown in Fig. 3. The switches, S_3 and S_4 are turned on for the whole half cycle whereas S_5 is kept off.

Mode-I ($0 \leq t < d_2 T_s$): The switches, S_1 and S_2 are turned on while the S_6 is kept off. The currents through L_1 and L_2 start rising from zero. Both the capacitors, C_1 and C_2 gets discharged in this mode. The D_1 blocks the current through S_4.

Mode-II ($d_2 T_s \leq t < d_1 T_s$): In this interval, S_2 is turned off, while the states of the other switches remain the same as in mode-I. The current, i_{L1} flowing through L_1 continues to rise while the current, i_{L2} flowing through L_2 starts decreasing. Before the end of this mode i_{L2} becomes zero. The capacitor C_1 is in floating condition. The inductor L_2 supplies the power to the load.

Mode-III ($d_1 T_s \leq t < T_s$): At the start of this interval, S_1 is turned off and S_6 is turned on. The current, i_{L2} remains zero in this mode. The current, i_{L1} starts decreasing and becomes zero before or at the end of this mode depending on the loading condition. The capacitor C_1 gets charged in this interval. It is to be noted that, the body diode of S_2 conducts in this interval and hence no gate pulse is given to S_2.

Negative Half Cycle

The modes of operation in NHC are shown in Fig. 4. The switches, S_5 and S_6 are turned on for the whole half cycle whereas S_4 is kept off.

Mode-I ($0 \leq t < d_2T_s$): The switches, S_1, S_2 and S_3 are turned on. The currents through L_1 and L_2 start rising from zero. Both the capacitors, C_1 and C_2 gets discharged in this mode. The D_1 blocks the current through S_4.

Mode-II ($d_2T_s \leq t < d_1T_s$): In this interval, S_2 is turned off, while the states of the other switches remain the same as in mode-I. The current, i_{L1} flowing through L_1 continues to rise while the current, i_{L2} flowing through L_2 starts decreasing. Before the end of this mode i_{L2} becomes zero. The capacitor C_1 is in floating condition. The inductor L_2 supplies the power to the load.

Mode-III ($d_1T_s \leq t < T_s$): At the start of this interval, S_1 is turned off and S_6 is turned on. The current, i_{L2} remains zero in this mode. The current, i_{L1} starts decreasing and becomes zero before or at the end of this mode depending on the loading condition. The capacitor C_1 gets charged in this interval. It is to be noted that, the body diode of S_2 conducts in this interval and hence no gate pulse is given to S_2.

Combined Operation

The governing equations of the inductors, L_1 and L_2 for different modes are provided in Table I. It may be noted that, all these equations are valid in both PHC and NHC.

Table I: Governing equations of the inductors, L_1 and L_2

<table>
<tr><th>Mode-I</th><th>Mode-II</th><th colspan="2">Mode-III</th></tr>
<tr><td colspan="2">$0 < t < d_1T_s$</td><td>$d_1T_s < t < (1-\Delta_1)T_s$</td><td>$(1-\Delta_1)T_s < t < T_s$</td></tr>
<tr><td>$0 < t < d_2T_s$</td><td>$d_2T_s < t < (1-\Delta_2)T_s$</td><td colspan="2">$(1-\Delta_2)T_s < t < T_s$</td></tr>
<tr><td colspan="2">$L_1\frac{di_{L1}}{dt} = V_{pv}$ (1)</td><td>$L_1\frac{di_{L1}}{dt} = v_{C1}$ (2)</td><td>$L_1\frac{di_{L1}}{dt} = 0$ (3)</td></tr>
<tr><td>$L_2\frac{di_{L2}}{dt} = v_{C1}$ (4)</td><td>$L_2\frac{di_{L2}}{dt} = \lvert v_g \rvert$ (5)</td><td colspan="2">$L_2\frac{di_{L2}}{dt} = 0$ (6)</td></tr>
</table>

Δ_1T_s: interval for which i_{L1} remains zero Δ_2T_s: interval for which i_{L2} remains zero

Applying volt-second balance across L_1 and L_2 respectively, the voltage gain of the boost stage and the buck-boost stage are obtained as,

$$\frac{v_{C1}}{V_{pv}} = \frac{1-\Delta_1}{1-d_1-\Delta_1} \quad \text{and} \quad \frac{v_g}{v_{C1}} = \frac{\text{sgn}(v_g)d_2}{1-d_2-\Delta_2}. \tag{7}$$

Therefore, the voltage gain of the inverter can be obtained as,

$$\frac{v_g}{V_{pv}} = \frac{\text{sgn}(v_g)(1-\Delta_1)d_2}{(1-d_1-\Delta_1)(1-d_2-\Delta_2)}. \tag{8}$$

However, the output voltage is decided by the grid voltage whereas the input voltage is decided the MPP voltage at steady state. Further, the average voltage across C_1 is also maintained to a predefined value. Therefore the voltage gain is remains independent of the loading conditions. Since both the stages are operated in DCM, the duty ratios are related to the transferred power. Hence d_1 and d_2 need to be estimated to feed the desired power. The duty ratios of the boost stage and the buck-boost can be respectively estimated as,

$$d_{1_0} = \sqrt{\frac{2I_{L1}L_1(v_{C1}-V_{pv})}{v_{C1}V_{pv}T_s}} \quad \text{and} \quad d_{2_0} = \frac{2}{v_{C1}}\sqrt{\frac{V_gI_gL_2}{T_s}}|\sin\omega t|. \tag{9}$$

The current fed to the grid is controlled indirectly by controlling i_{L2}. Therefore, the reference, i^*_{L2} has to be estimated from I^*_{gm} and it is given by,

$$i^*_{L2} = I^*_{gm}(|\sin\omega t| + \frac{V_{gm}}{v_{C1}}\sin^2\omega t). \tag{10}$$

Configuration of Control

The main objective of the controller is to feed sinusoidal current with appropriate magnitude to the grid while operating at MPP. The configuration of control is shown in Fig. 5. The boost stage and the buck-boost stage of the proposed micro-inverter is separated by the intermediate capacitor, C_1. The voltage across C_1 is controlled by a controller having slower dynamics compared the current controller. Hence the two stages can be controlled individually.

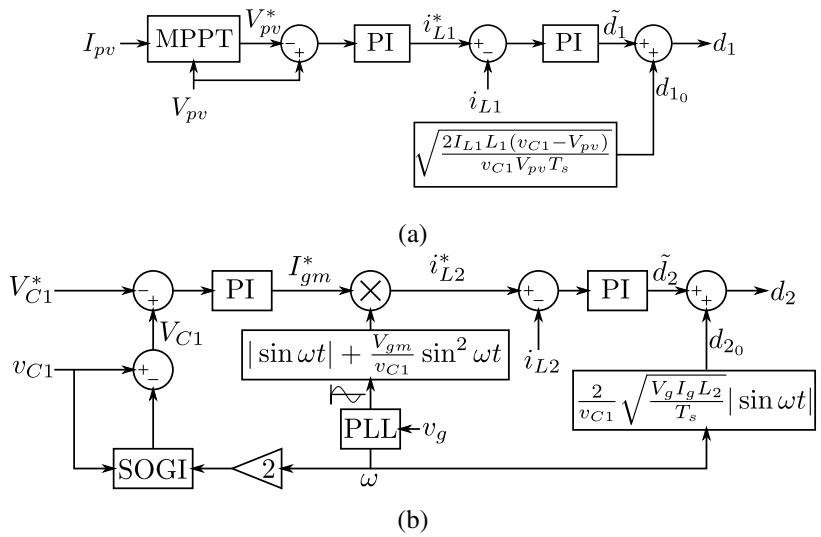

Fig. 5: Block diagram of the control configuration: (a) boost stage and (b) buck-boost stage

The controller dedicated for the boost stage is shown in Fig. 5(a), which can also be termed as a input controller. An incremental conductance based MPPT controller is utilized, which generates the reference voltage, V^*_{pv}. The error between the reference and the measured V_{pv} is passed through a PI based voltage controller to generate the reference current, i^*_{L1}. The duty ratio, d_1 is estimated using the expression provided in (9), which is the feed forward component of d_1. The measured i_{L1} is compared with i^*_{L1} and the generated error is passed through a PI controller the generate the feedback component, $\widetilde{d_1}$. Finally, $\widetilde{d_1}$ is added with the feed forward component to obtain the actual duty ratio d_1.

The controller for the buck-boost stage is depicted in Fig. 5(b), which can also be termed as a output controller. The power drawn from the PV module at the boost stage needs to be fed to the grid in order to maintain V_{C1} to a predefined reference, where V_{C1} is the average voltage across C_1. A second order generalized integrator (SOGI) filter tuned at twice the grid frequency is utilized to filter out the the second order harmonics in v_{C1}. The PI controller, which maintains V_{C1} at V^*_{C1}, generates the reference peak output current I^*_{gm}. The reference current, i^*_{L2} is obtained from I^*_{gm} using (10). The reference sinusoidal wave having unit magnitude is generated from the grid voltage using the single phase PLL. The feed forward component of d_2 is estimated using the expression provided in (9). The feedback component of d_2 is $\widetilde{d_2}$ is generated by a PI controller which maintains i_{L2} to its reference, i^*_{L2}. At the end, the feedback component is added with the feed forward component to obtain the actual duty ratio of the buck-boost stage, d_2.

Design Guidelines

Input Inductor, L_1

The input inductor, L_1 needs to be designed in such a way, so that the current through it remains discontinuous for all possible operating conditions. Hence the limiting condition for L_1 is obtained as,

$$L_1 \leq \frac{V_{pv}T_s(V_{C1}-V_{pv})}{2I_{pv}V_{C1}}. \tag{11}$$

Output Inductor, L_2

Since the current, i_{L2} must become zero before the end of mode-II, the limiting condition for L_2 can be obtained as,

$$L_2 \leq \frac{(V_{C1} - V_{PV})V_{C1}}{V_{PV}(V_{gm} + V_{C1})} \left(\frac{I_{L1}}{I_{gm}}\right) L_1. \tag{12}$$

Intermediate Capacitor, C_1

The intermediate capacitor, C_1 acts as a coupling between the dc side and the ac side by allowing second order harmonic ripple. Therefore

$$C_1 = \frac{P}{2\pi f_g V_{C1} \Delta v_{C1}}, \tag{13}$$

where P is the power being transferred, f_g is the frequency of the grid voltage, and Δv_{C1} is the maximum allowable voltage ripple across C_1.

Output Capacitor, C_2

The voltage ripple, Δv_{C2} is maximum at $\omega t = \pi/2$. Therefore

$$C_2 = \frac{I_{gm} d_2 T_s}{V_{gm} \frac{\Delta v_{C2}}{V_{C2}}}, \tag{14}$$

where the value of d_2 can be calculated from (9).

Simulated Performance of the Proposed Micro-inverter

Detailed simulation studies of the proposed micro-inverter is carried out on MATLAB/Simulink platform. The parameters chosen from the simulation are depicted in Table II.

Table II: Parameters for Simulation

System Parameters		**Inverter Parameters**	
Parameters	Values	Parameters	Values
V_{mpp} and V_{oc} at STC	34.7 V and 44 V	L_1	38 μH
I_{mpp} and I_{sc} at STC	6.35 A and 6.6 A	C_1	100 μF
MPP power, P_{mpp} at STC	220.34 W	L_2	200 μH
Grid voltage, V_g	220 V	C_2	0.47 μF
Grid frequency, f_g	50 Hz	L_g	1 mH
Switching frequency, f_s	50 kHz	C_{pv}	20 μF

V_{oc}: Open circuit voltage of the PV module V_{mpp}: Voltage of the PV module at MPP
I_{sc}: Short circuit current of the PV module I_{mpp}: Current from the PV module at MPP
STC: Standard test condition (Solar insolation=1 kW/m^2, Temp.=25°C)

The solar irradiance is varied over time as depicted in Fig. 6. The power drawn from the PV module is also shown in this figure. It can be inferred from the figure that MPP is tracked properly with variation of solar irradiance over time. The waveforms of the voltage across PV module and the current drawn from it are shown in Fig. 7. In Fig. 8, the grid voltage and the current fed to the grid are shown. From Fig. 7 and Fig. 8, it can be inferred that the micro-inverter is capable of interfacing a 35 V PV module to a 220 V ac grid. THD of the grid current is observed to be 4.09% while negotiating the solar irradiance of 1 kW/m^2.

The voltage across the capacitor, C_1 is depicted in Fig. 9. The average voltage is maintained at 250 V, and second order harmonic ripple is 27 V peak to peak when the irradiance is 1 kW/m^2. It can be observed from Fig. 10 that i_{L2} becomes zero before i_{L1} starts decreasing. The plots of duty ratios, d_1 and d_2 for

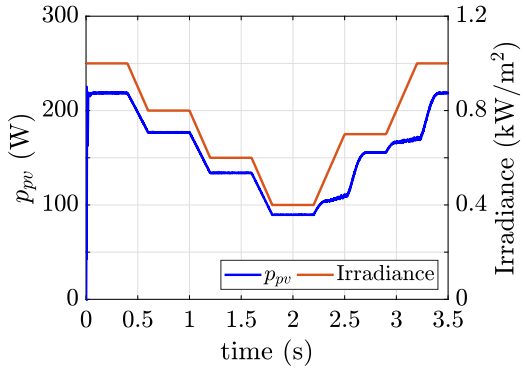

Fig. 6: Waveform of solar irradiance and the power drawn from the PV module

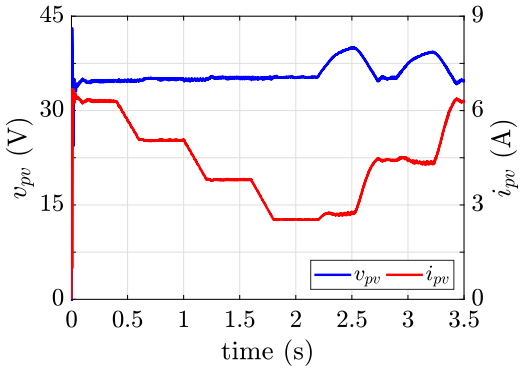

Fig. 7: PV module voltage and its current waveform

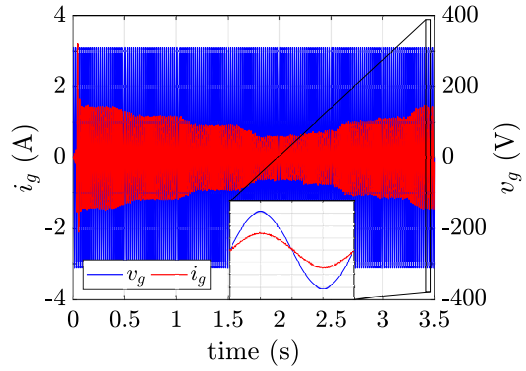

Fig. 8: Grid side voltage and current waveform, and magnified plot over 20 ms

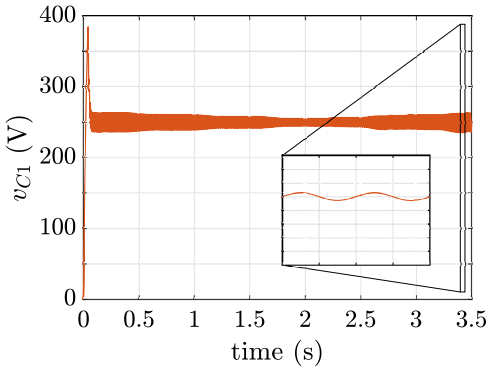

Fig. 9: Voltage waveform across C_1, and magnified plot over 20 ms

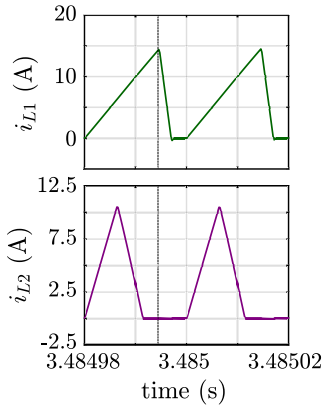

Fig. 10: Waveform of i_{L1} and i_{L2} magnified over 40 μs near $\omega t = \pi/2$

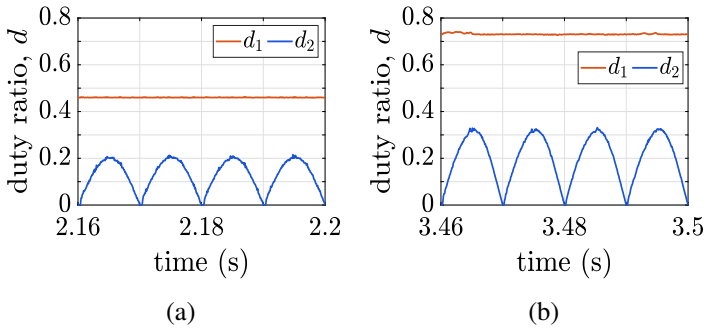

Fig. 11: Waveform of duty ratio over 40 ms for (a) 400 W/m^2, and (b) 1 kW/m^2

different solar irradiances are shown in Fig. 11. At rated power, the value of d_1 is 0.73, which is less compared to that reported in [16]. The waveform of d_2 is a rectified sine wave. Depending on the solar irradiance level, the duty ratios change as the inverter is operated in DCM.

The efficiency of the proposed micro-inverter at STC is estimated as 95%. The estimated maximum efficiency of the inverter is 95.8% when the irradiance level is 800 W/m^2.

Conclusion

A transformer-less solar PV micro-inverter topology is proposed in this paper. Due to the chosen modified operation, one switch is reduced compared to that in [16]. The volume of the inductor is also reduced significantly as the inverter is operated in DCM. Further, DCM operation ensures negligible turn on losses of the switches. This micro-inverter is suitable for interfacing a 35 V PV module to a 220 V grid and is having the feature of power decoupling. The negative terminal of the PV module is connected to the grid neutral, which ensures negligible leakage current flow.

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