Bus voltage regulation using sequentially switched ZVZCS converters for spacecraft power systems

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Abstract

This work proposes a regulation technique for photovoltaic sources power bus based on quasi resonant zero-voltage, zero-current power switching cells controlled in a sequential manner to provide tight bus voltage regulation, fast transient response, and simple control loop design. This method has been devised for high-power bus regulated satellites following European Space Agency standards.

Acronyms

BC(D)R – Battery Charge (Discharge) Regulator
DCX – DC Transformer
EMI – Electromagnetic Interference
EP – Electric Propulsion
ESA – European Space Agency
IPOS – Input Parallel Output Series
MEA – Main Error Amplifier
MPP – Maximum Power Point
PCU – Power Conditioning Unit
SAR – Solar Array Regulator
SAS – Solar Array Section
SMART – Standard Multiple Application Regulator Topology
S^3R – Sequential Switching Shunt Regulator
S^3MPR – Sequential Switching Shunt Maximum Power Regulator
S^3ZVZCS – Sequential Switching Shunt Zero Voltage Zero Current Switching
$S^3ZVZCSMPR$ – Sequential Switching Shunt Zero Voltage Zero Current Switching Maximum Power Regulator
S^4R – Sequential Switching Shunt Series Regulator
S^4MPR – Sequential Switching Shunt Series Maximum Power Regulator
S^4ZVZCS – Sequential Switching Shunt Series Zero Voltage Zero Current Switching
$S^4ZVZCSMPR$ – Sequential Switching Shunt Series Zero Voltage Zero Current Switching Maximum Power Regulator
TWTA – Travelling Wave Tube Amplifier
ZCS – Zero Current Switching
ZVS – Zero Voltage Switching
ZVZCS – Zero Voltage Zero Current Switching

Introduction

Today the typical bus voltage for high-power satellites is 100 V. As spacecraft power is scaled up to tens of kW, mainly due to electric propulsion and more demanding payload, a 100 V power bus leads to high mass and losses in the DC harness, connectors, and equipment components. An increase in bus voltage to 300 V or more would reduce power losses, mass and would increase the electrical efficiency.

Considering the ESA standard [1], a 25kW power conditioning unit (currently the highest bus power capability of the largest European telecommunications platforms) will impose the following design constraints in 100V and 300V bus voltage distribution, please refer to table 1. Clearly, 300V bus voltage distribution will bring multiple benefits.

Table I: Estimated values for bus regulated architecture, 25kW – ECSS-S-ST-20C

Parameter	Bus: 100V	Bus: 300V	Comments
Bus current	250A	83.3A	Harness, connectors, distribution and protection switches specifications relaxed for 300V.
Maximum output impedance (Z_{Omax}) - § 5.7.2.o	8mΩ	72mΩ	Z_O < 10mΩ imposes a difficult bus bar design for 100V.
Bus capacitance (C_{BUS}) - § 5.7.2.o	8mF	880uF	Bus capacitance improvement (mass and volume) around 30% for 300V.

The most common electrical architecture for large satellites is the one represented in figure 1 (left) and it is composed of a direct-energy transfer solar array regulator, known as Sequential Switching Shunt Regulator (S^3R), a Battery Discharge Regulator (BDR) and a Battery Charge Regulator (BCR), being all of them implemented by several modules. The main error amplifier (MEA) is used to control the three main regulators and provide bus voltage regulation [2]. The control of the S^3R to achieve bus voltage regulation, is the sequential activation and deactivation of individual solar array sections based on hysteretic control [3].

To achieve 300V bus regulation with an S^3R electrical architecture [4], 300V-S^3R, high-voltage photovoltaic strings are required which in turn represent many challenges in the solar array design:

- Solar array arcing due to differential charging of the different materials on the solar array surface.
- Slip rings, design for 300V requires sealed assembly and arc mitigation system.
- String voltage equalization of solar cells. The larger the number of solar cells in series the more complicated the voltage distribution between cells. This is aggravated if the solar array section is shunted.
- Parasitic elements, solar array section capacitance (C_{SAS}) has a critical effect in 300V S^3R regulator in terms of energy dissipation and bus voltage performance, both in static and transient response.
- Qualification and cost, the solar array is the most expensive part of the satellite platform.

The proposed electrical architecture, represented in figure 1 (right), only changes the Solar Array Regulator (SAR) of the original Power Conditioning Unit (PCU) concept. Obviously, an important number of benefits are derived from this approach:

- Solar array design is decoupled from bus voltage distribution, higher but also lower bus voltage might be realized from a standard solar array.
- PCU design could be optimized in terms of efficiency, mass and volume while keeping existing and well-established control techniques and power conversion topologies.

- Modularization is easily achieved, for instance, higher bus voltage distribution could be easily achieved connecting several ZVZCS converters in input-parallel and output-series (IPOS) connection.

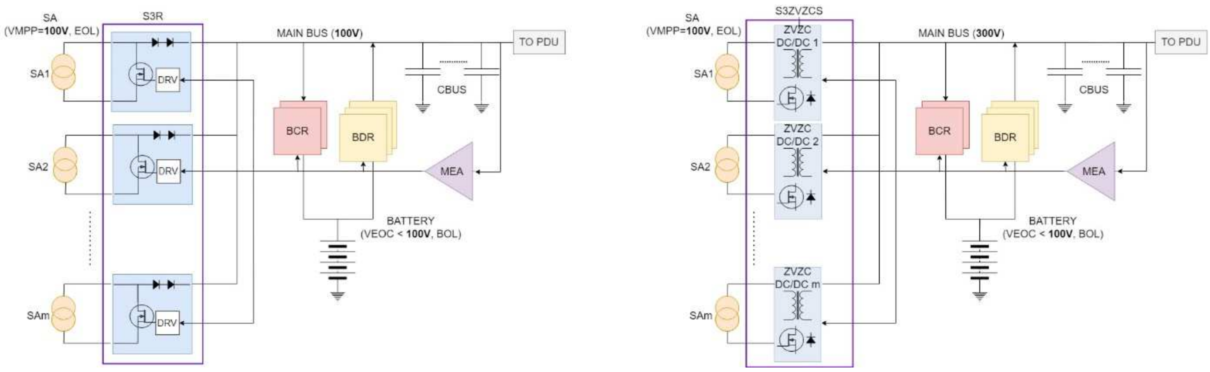

Fig. 1: Electrical Power Conditioning Unit architectures for large satellites. Left side: S^3R bus regulated - 100V. Right side: S^3ZVZCS – 300V.

In the space sector, high-voltage power supplies are common for Travelling Wave Tubes Amplifiers (TWTA's) and Electrical Propulsion (EP) systems, and therefore, there is always a special interest in reliable, high-efficiency, high-voltage conversion ratio converters. A widely spread ZVZCS technique for DCX applications, used by many European space manufacturers and ESA itself, is the one detailed in [5-7], which has been revisited recently [8, 9] applied to low-voltage, low-power, and high-voltage, high-power applications, respectively.

This ZVZCS switching technique, which can be applied to push-pull, half-bridge, full-bridge or any other dual-ended topology has the following benefits:

- all the parasitic elements are used in a resonant manner (efficiency > 97%).
- all power semiconductors are operated in ZVS and ZCS when turned on and off.
- ZVS and ZCS (neglecting magnetizing current) are load independent in a wide range.
- very simple low loss gate drive (especially in push-pull version).
- good power semiconductor utilization (with high duty cycles).
- operation at fixed frequency and duty cycle.
- reduced number of components.
- very low EMI.

Obviously, the main drawback is the absence of regulation capability, which has been also an important topic of research, and different approaches have been described in the literature to achieve output voltage regulation. Focusing on European space sector, a widely adopted solution by ESA and many manufacturers is the two-stage approach, typically a buck converter (pre-regulator) followed by a ZVZCS push-pull (DCX), known as SMART [10]. This approach, although it is widespread today, has an efficiency penalty due to the cascade connection. Other techniques, as parallel power processing and variable transformer turns ratio were introduced at that time [11,12] to alleviate that problem. This topic is still relevant and different approaches, like [13], are being proposed.

In the case of a segregated power source, such as it happens with the satellite solar array, another approach for output voltage regulation is possible. Essentially, some DCX converters are permanently providing power to the bus, while others DCX are disconnected. Only one DCX is turning on and off to eventually regulate the output voltage. This is the natural evolution of the sequential hysteretic control S^3R, and as consequence it has been named here, S^3ZVZCS.

The rest of the work is organized as follows. Section 2 describes the ZVZC conversion (focusing on the push-pull converter) and the output voltage regulation. Section 3 covers the design and simulation of 300V bus distribution and section 4 briefly discusses the results and issues related to space-grade implementation.

Photovoltaic power regulation using the S^3ZVZCS technique

In essence, a DCX is an unregulated DC-DC converter that converts voltage and current with a fixed ratio, n, (V_o=nV_{in} and I_{in}=nI_o). Typically, the DCX converter family considered in this work [5-7] can maintain ZVZC conditions in a wide load range. The S^3ZVZCS power cells using a push-pull and a half-bridge structure are represented in figure 2. The solar array section (SAS) is modelled by the equivalent single-diode model and the parasitic capacitance (C_{SAS}) and the harness inductance (L_h). The photovoltaic source has some interesting characteristics when used with a ZVZCS converter:

- The power source exhibits inherent current limited characteristics (I_{SAS}).
- The maximum input voltage is limited to the open-circuit solar array section voltage (V_{OC}).
- The converter is current fed, so the solar array harness inductance can be part of it.

The shunt section consists in a power transistor with a current limiting circuit. The main function is to short the solar array section when its energy is not required while provides controlled energy discharge of the parasitic elements. M_1 and M_2 could also be controlled to perform the same operation, however considering a separate circuit allows optimization of MOSFET selection for each function, low-frequency, <10kHz, and linear operation (shunt) and high-frequency operation (ZVZCS converter). Further, instead of shunting M_1 and M_2, these can be left open to disconnect the solar array section from the bus; however, this method has some drawbacks related to high voltage at very low temperatures, e.g. during eclipse exits. A key difference with the two-stage approach, S^3R cascaded by a ZVZCS converter, is that the S^3R diode function is performed by the DCX output diodes.

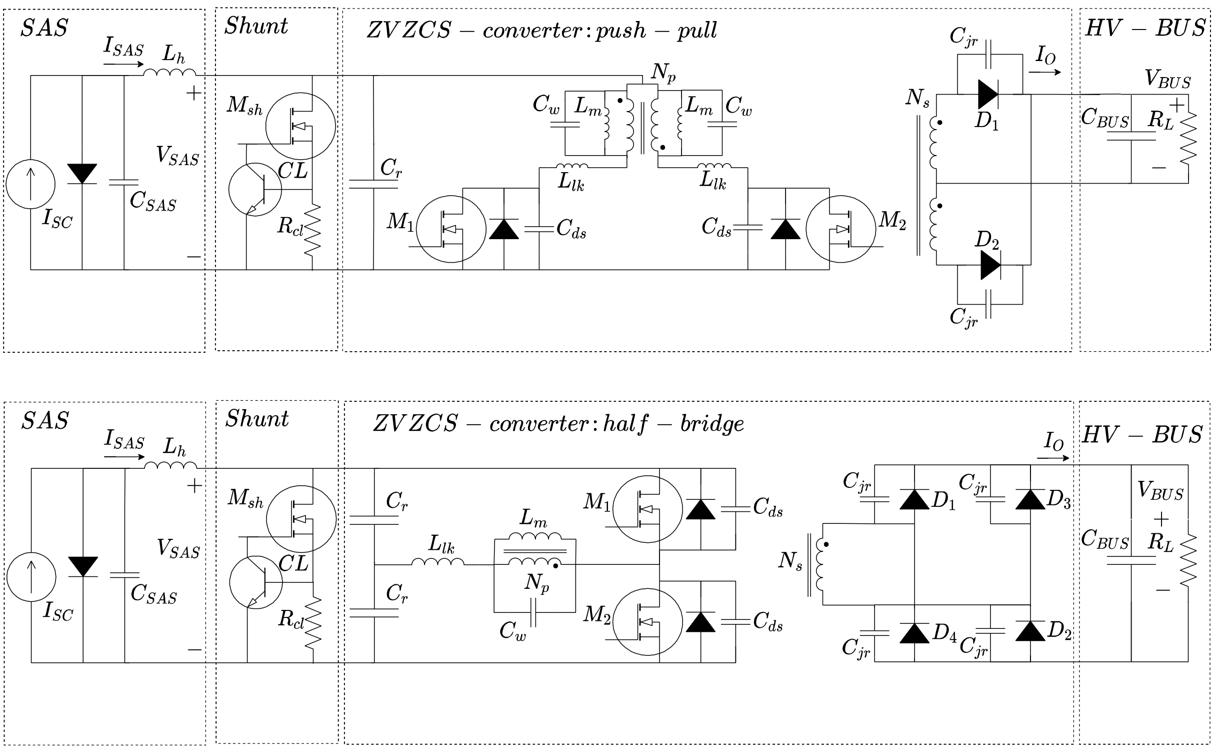

Fig. 2: S^3ZVZCS power cells. Top side: push-pull DCX. Bottom side: half-bridge DCX.

The ZVZCS converter operates at fixed switching frequency and duty cycle. It has two operating states, ON state (one of the power MOSFETs is turned-on) and GAP state (both power MOSFETs are turned-off), with equivalent circuits shown in figure 3. During the ON state, a resonant switch current appears due to the resonant tank formed by C_r (resonant capacitor) and L_{lk} (transformer leakage inductance). During the GAP state, the magnetizing current charges and discharges the equivalent capacitances. The idealized MOSFET waveforms are shown in figure 3 (right). For a detailed description of the converter operation and design equations, please refer to [7,8].

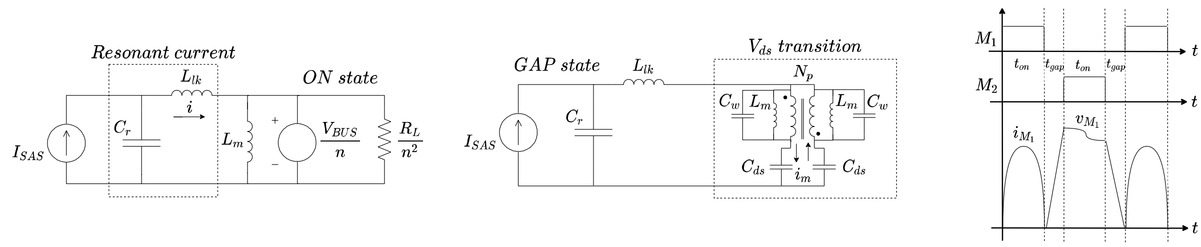

Fig. 3: ZVZCS-push-pull: equivalent circuits (ON and gap) and idealized waveforms.

When supplied from a photovoltaic source, as represented in figure 4, the converter can maintain ZVS and ZCS in a wide range of load variation (between operating points A and B), and it is not sensitive to irradiance deviations and temperature changes. For load lines exceeding the operating point B, the transferred power becomes negligible since the SAS current becomes magnetizing current and it is employed to charge and discharge parasitic capacitors on each cycle. On the other side, if the load line crosses below operating point A, the reflected input voltage becomes low enough that the voltage ripple in the resonant capacitor goes to zero. Between these two extremes, ZVZCS conditions are guaranteed, and for maximum power transfer, the load line should cross the Maximum Power Point (MPP).

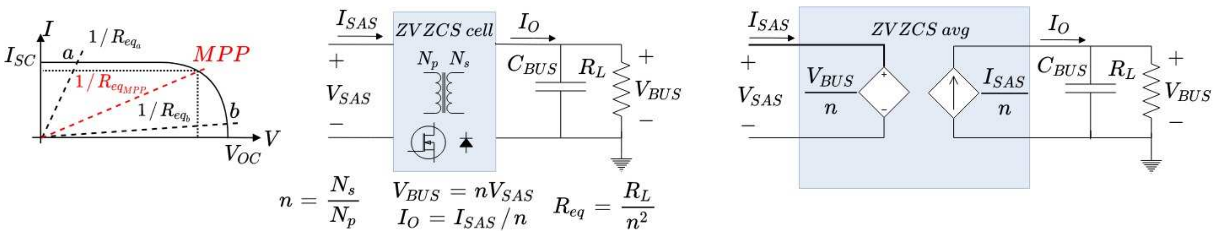

Fig. 4: ZVZCS-push-pull: connection to a photovoltaic source and equivalent DC circuit.

The DCX can be modelled as an output current source, whose value is the SAS current divided by the transformer turns ratio (n), that feeds the bus capacitance, see figure 4. At fixed duty cycle, the output current of a power cell is not controllable and mainly depends on irradiance, temperature and the load. However, in an arrangement of several power cells connected in parallel at the output, the average bus current (sum of all output currents) and, therefore the output voltage, can be controlled by connecting and disconnecting different power cells. In case of using a hysteretic-sequential control, in steady-state conditions, only one power cell will switch on and off while the others remain either fully-on or fully-off . An averaged linear model of the complete power regulator considers a voltage-controlled current-source, whose gain is simply the output current of a DCX divided by the hysteresis voltage [14]. Please refer to figure 5 for the S^3ZVZCS configuration, non-linear power stage model and its linearization.

As a result of using sequential-hysteresis control, a variable low frequency signal (in the kHz range) defines the bus voltage ripple between two limits. A much higher frequency component appears at the switching frequency (or multiple of switching frequency if DCX interleaving is considered), but its amplitude remains very small because is filtered by the bus capacitance. Since the power stage is conductance-modelled, a simple Proportional-Integral error amplifier (MEA) is sufficient to guarantee bus voltage regulation.

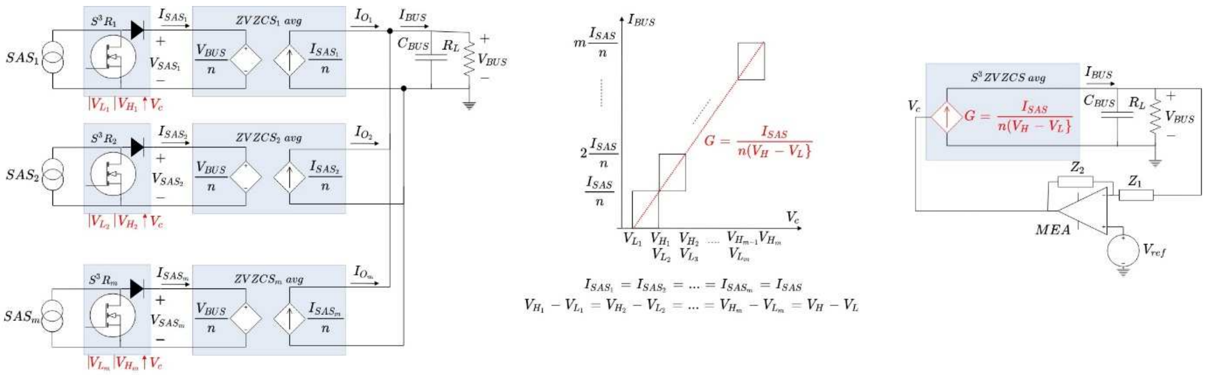

Fig. 5: S^{3}ZVZCS-regulator. Left side: Equivalent circuit S^{3}R and ZVZCS averaged model. Middle: Non-linear power regulator model. Right side: S^{3}ZVZCS linearized model.

An implementation of the S^{3}ZVZCS using a push-pull power cells is shown in figure 6.

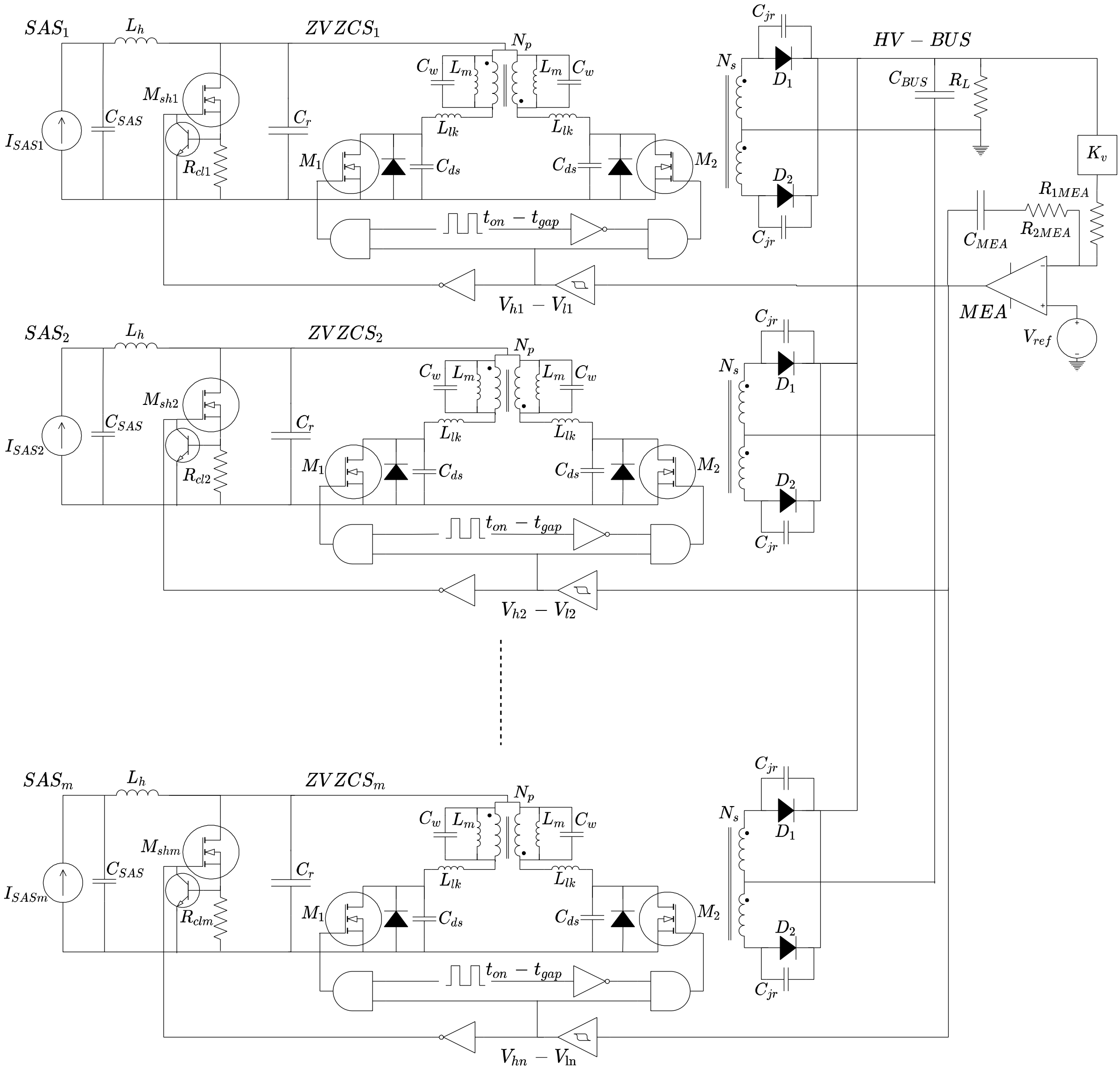

Fig. 6: S^{3}ZVZCS-regulator block diagram: push-pull implementation.

Design and simulation of a S^3ZVZCS for 300V satellite bus regulation

The design of a three-power cell S^3ZVCS push-pull regulator has been carried out (three is the minimum number of cells required to observe the static, dynamic and potential *double sectioning* issues) to validate the proposed power regulation technique. The main characteristics of the regulator have been gathered in table 2.

Table II: 300V S^3ZVZCS main parameters

Parameter	Value	Comment
Solar array section - SAS		
V_{SAS}	100V	Operating conditions (1367W/m2; T=60ºC)
V_{OC}	120V	Operating conditions (1367W/m2; T=60ºC)
I_{SAS}	5A	Operating conditions (1367W/m2; T=60ºC)
C_{SAS}	2uF	Estimated value
L_h	33uH	Estimated value. It also considers S^3R inductor used for current limitation.
Transformer ZVZCS		
Core	ETD49	Material 3C90
N_p	8	Magnetizing current approx. 15% of SAS current
N_s	24	V_{BUS} = 300V
L_m	307.5uH	Measured value
L_{lk}	1uH	Measured value
Resonant circuit ZVZCS		
C_r	500nF	ON state (L_{lk}-C_r resonant circuit)
C_{ds}	1.4nF	Estimated capacitance during GAP interval
f_s	104.5kHz	MOSFET Si (100kHz – 150kHz)
D	0.418	ON state power transfer optimization
Bus capacitance – ECSS-S-ST-20C		
C_{BUS}	250uF	Zo mask impedance (§ 5.7.2.o)
MEA - ECSS-S-ST-20C		
V_{ref}	6.4V	Temperature compensated voltage reference
K_v	0.0213	V_{BUS}=300V
R_{1MEA}	5kΩ	Zo mask (§ 5.7.2.o). A_{min}=20
R_{2MEA}	100kΩ	Zo mask (§ 5.7.2.o). A_{min}=20
C_{MEA}	6.8nF	Zo mask (§ 5.7.2.o). f_{zero}=234Hz
Hysteresis comparator - ECSS-S-ST-20C		
V_H-V_L	1V	Zo mask (§ 5.7.2.o).
Shunt current limitation		
R_{lim}	0.05Ω	I shunt max=14A

Figure 7 shows the bus steady-state voltage ripple and voltage response under a step load of 50% of the bus power. Before t=10ms, ZVZCS1 is maintaining the bus voltage regulation. After t=10ms, ZVZCS1 and ZVZCS2 are fully on to provide power to the bus and ZVZCS3 performs bus regulation by hysteresis control action. It is clearly observed that bus voltage ripple and bus voltage transient response only depend on the hysteresis-sequential control loop, while DCX high-frequency ripple (red trace) is filtered by the bus capacitance. Figure 8 is a zoomed view around t=13ms, where bus voltage, DCX-MOSFET voltage and DCX-MOSFET current are shown. Superimposed ripple on the bus voltage due to DCX and zero-voltage and zero-current switching of the power cell are clearly observed.

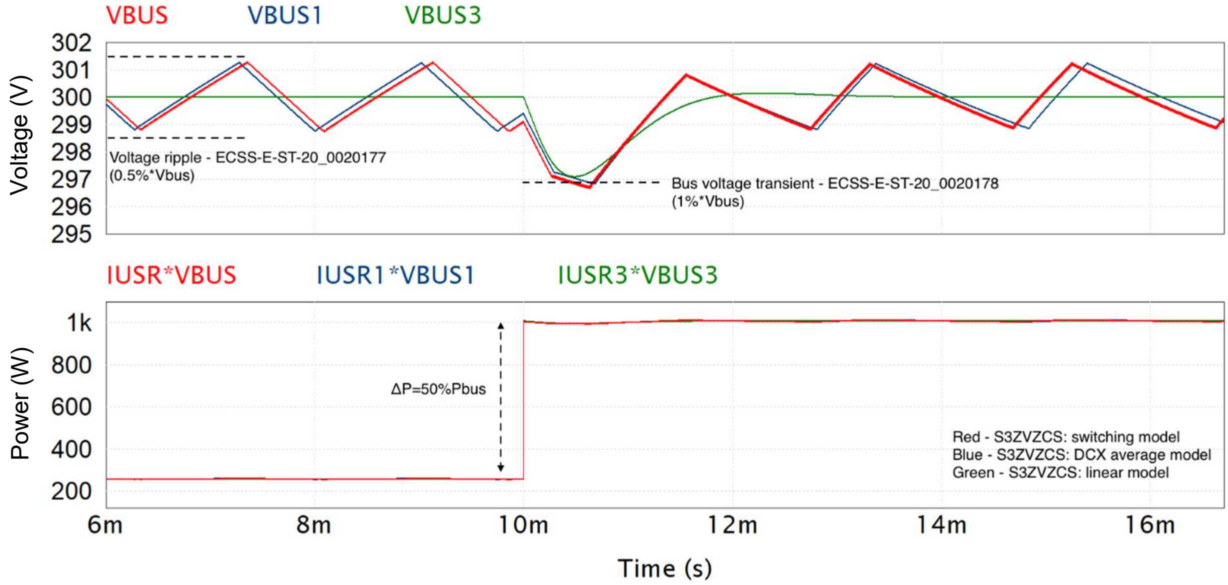

Fig. 7: S^{3}ZVZCS-regulator transient response. Top figure: bus voltage. Bottom figure: Power step load

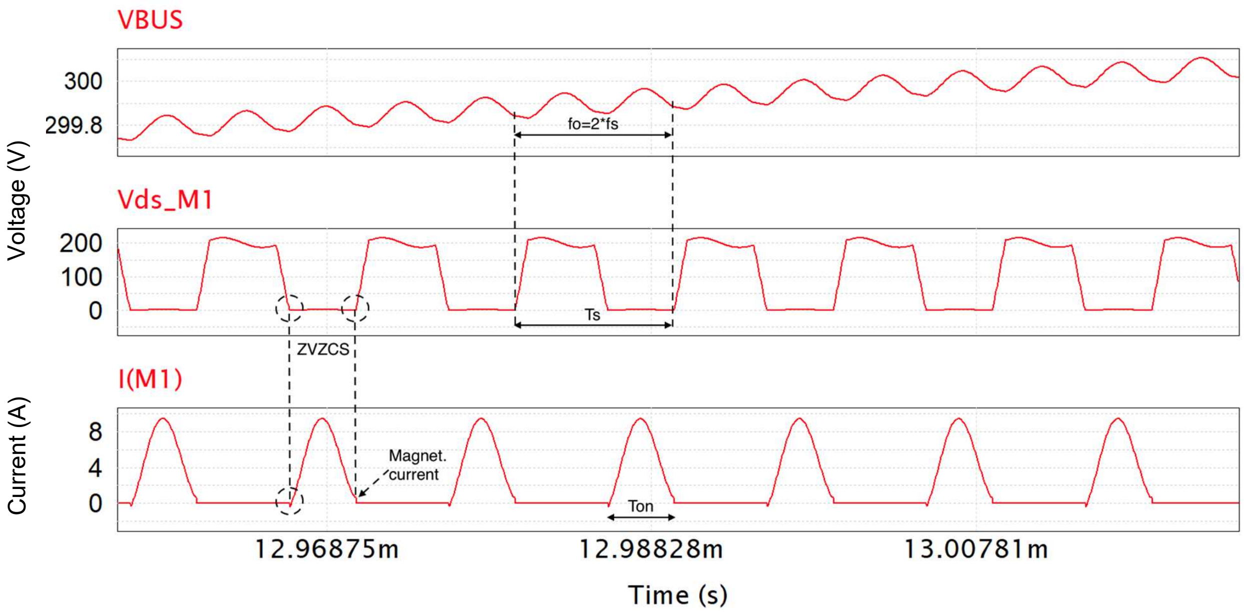

Fig. 8: S^{3}ZVZCS-switching frequency detail. Top figure: bus voltage. Middle figure: DCX-MOSFET drain-source voltage. Bottom figure: DCX-MOSFET current.

Results discussion

A space-qualified implementation of the proposed concept has different issues to be dealt with. Some of them are briefly discussed below.

a) Power semiconductors. A critical evaluation of available technologies and potential needs is required to assess the viability of the presented approach. The increase of voltage and switching frequency ask for, as many other power electronics applications, wide bandgap power devices. Today, up to 650V/60A E-mode GaN space-qualified power transistors and drivers are available for DCX primary switches, allowing the implementation of any kind of the available topologies, e.g. push-pull, half-bridge or full-bridge. 1.2kV - SiC space-qualified power diodes are also a good starting point for rectifiers, but their availability is limited. However, there is an interest for 1.2kV SiC power diodes in other space applications, like TWTAs, and technology is already mature in other high reliable terrestrial applications, like automotive or aeronautical. Finally, shunt transistor requirements are covered by current space-qualified Si MOSFET technology and no major issues are anticipated.

b) Passive components. WBG power devices will allow an increase of switching frequency up to MHz range, and recent studies have been demonstrated operation up to 1MHz in similar applications [13]. Soft ferrites and space-qualified polyester PET film capacitors are already available for energy storage and tuning purposes.

c) Analog vs. digital control. Fully analog control implementation appears to be the simplest approach since all the elements involved in the S^3ZVZCS have flown as separate subsystems. Dynamic interleaving between DCX converters will minimize RMS bus current and it could be implemented with analog space-qualified timing circuits. However, additional benefits would be derived from a digital implementation of the DCX control. Dynamic and real-time reconfiguration of t_{on} and t_{gap}, to compensate any variation of the resonant conditions, can be more easily achieved using a digital approach, as well as dynamic interleaving and other high-level monitoring and control options. Obviously, this is at the expense of additional complexity.

d) Electrical power architectures variations. The proposed concept could be easily adapted to other satellite electrical architectures, S^4R [14], S^3MPR [15] and S^4MPR. In particular, the evolution of the S^4R architecture, either the MPP version, S^4ZVZCSMPR or the full regulated, S^4ZVZCS, has the advantage of removing the double power processing step (SA Low Voltage – BUS High Voltage – BAT Low Voltage) as represented in figure 10.

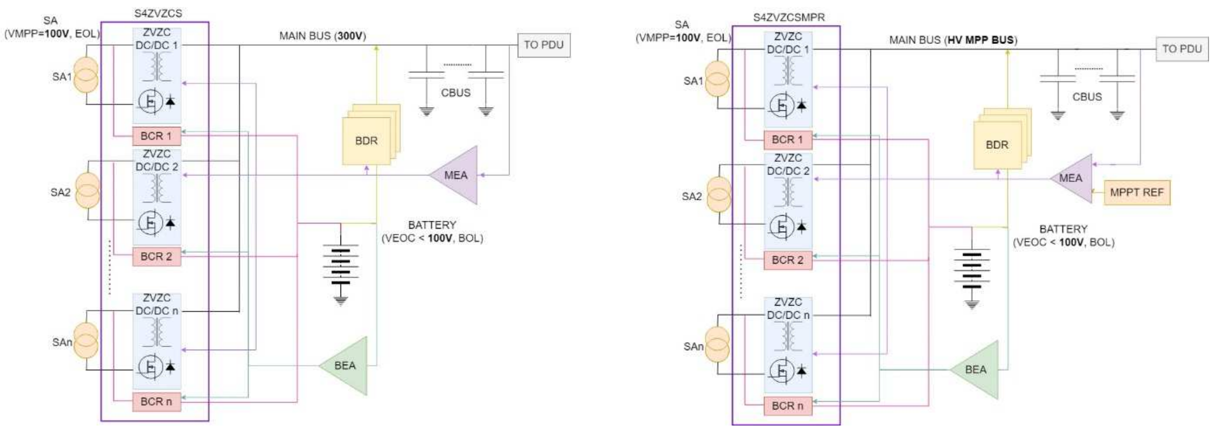

Fig. 9: S^4ZVZCS electrical architecture (left side). S^4ZVZCSMPR electrical architecture (right side).

e) Scalability. Another interesting point regards to DCX output serialization using a IPOS configuration (Input-Parallel Output-Series configuration). This would allow for a higher bus voltage, a reduction in the transformer turns ratio, and a voltage stress reduction in the secondary side power semiconductors. This also open new applications, like power conditioning for solar satellites, being in line with other recent studies [16].

Conclusion

Two well-known space power conversion techniques have been combined to propose a novel solar array regulation technique for high-voltage satellite power bus. Although, DC transformer function can adopt many forms, the proposed ZVZCS technique is well suited for a photovoltaic source since it operates as almost an ideal current source at the voltage regulation point. In addition, this method is applicable to push-pull, half-bridge, full-bridge or any dual-ended topology which provides a large degree of flexibility for designers. Design and simulation of the proposed method illustrate the benefits for a 300V bus voltage distribution in high-power satellites. The concept can be extrapolated to other bus regulated architectures, like S^4R, S^3MPR or S^4MPR.

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