Short Circuit Type II and III Behavior of 1.2 kV Power SiC-MOSFETs

Xing Liu[1], Xupeng Li[1], Thomas Basler[1]

[1]Chemnitz University of Technology, Chair of Power Electronics
Reichenhainer Str. 70, 09126, Chemnitz, Germany
Tel.: +49 371 531-30465
E-Mail: xing.liu@etit.tu-chemnitz.de

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Abstract

The application relevant short circuit (SC) behavior of 1.2 kV power SiC-MOSFETs during the forward conduction mode (type II) and the body-diode conduction (type III) is experimentally investigated in this paper. Compared with Si-IGBTs, the SC type II and III behavior are less critical from the perspective of short-circuit energy. The reason is due to the smaller ratio between the Miller-capacitance and gate-source capacitance and further the more significant short-channel effect or Drain Induced Barrier Lowering (DIBL) effect for SiC-MOSFETs. Moreover, the influence of the operation temperature and gate trapping effect on the SC behavior are discussed.

Introduction

Silicon-Carbide (SiC) MOSFETs have experienced significant development over the recent years, and their level of majority is now sufficient for product development of converters for various applications for medium-power classes [1]. It ranges from motor drives for different kinds of electron vehicles to various industrial applications. The major advantages of SiC devices are their lower on-state resistance, higher operating temperature capability, and faster-switching speed compared with Silicon (Si) IGBTs. However, due to the higher current density and the thinner base region, the thermal capacitance of the SiC-MOSFETs chip is considerably smaller compared with Si counterparts. Therefore, the behavior and robustness of SiC-MOSFETs under the short circuit (SC) condition have to be crucially considered and investigated. The first type of SC, also called Hard Switching Fault (HSF), has been studied in numerous publications [2]-[4]. For 1.2 kV voltage classes, there are two main failure modes that have been found: thermal runaway and failure in the gate oxide [3]. However, minor research is currently focused on the application relevant SC type II and III characteristics of SiC-MOSFETs, especially for the SC III, where the SC event occurs under the conduction of the body diode (BD) mode. Unlike Si-IGBT applications, where a separate free-wheeling diode chip has to be used for an inductive load. SiC-MOSFETs can conduct reversely because of the integrated body diode. To reduce the conduction losses during the BD conduction, a positive gate voltage can be applied to open the channel and make the MOSFET work in reverse conduction mode. During this time, if another blocked device on the same bridge arm losses the blocking capability or the load is shorted accidentally, the reverse-conducting MOSFET will directly enter the short circuit type III mode.

In this paper, the low-inductive SC type II and III behavior for 1.2 kV SiC-MOSFETs will be experimentally investigated. Different gate structures from three manufacturers will be compared. The effects of different negative gate voltages, gate resistances, conduction current and operating temperatures will be analyzed. For SC type III, the bipolar effect of the BD and the charge-carrier trapping at the SiO_2/SiC interface will be considered.

Test setup and conditions

Three different gate structures have been selected as Devices Under Test (DUTs) for this investigation. The general information is summarized in Table I. A half-bridge based test setup, and the used pulse pattern to trigger the different SC events have already been introduced in our previous studies [5]. The only difference is the utilized auxiliary switch (aux. switch): two 30 mΩ SiC-MOSFETs (IMZ120R030M1H) were used in parallel as the high side (HS), see also Fig. 6. The drive voltage for aux. switch was set to -5/18 V, and a 0 Ω external gate resistance was implemented to achieve a fast turn-ON. This can simulate the SC behavior in the laboratory environment as close as possible to the reality. The lumped parasitic inductance of the SC loop is around 50 nH.

Table I: DUT information

Abbreviation	Name	Manufacturer/Gate structure	$R_{DS,ON}$	$R_{G,int}$	Packaging
M1	IMZ120R060M1H	Infineon/Asymmetrical Trench	60 mΩ	6 Ω	TO-247-4
M2	SCT3080KR	ROHM/Double Trench	80 mΩ	12 Ω	
M3	NTH4L080N120SC1	ON Semiconductor/Planar	80 mΩ	1.7 Ω	

For the SC type III measurements, the pulse is described later in detail to consider the bipolar and trapping effects. The DC-link voltage was set to 800 V, the applied negative gate voltage $V_{GS,OFF}$ was changed between different levels to investigate the trapping effect causing the gate threshold voltage $V_{G,th}$ shift/hysteresis. The positive gate voltage $V_{GS,ON}$ was fixed to 15 V to guarantee a certain short circuit capability. All DUTs are packaged in a 4-pin TO-247 discrete housing, and the sense-source is used as the measurement reference point to minimize the measurement error caused by the packaging parasitic inductance due to the fast current commutation.

The Short Circuit Type II Behavior of SiC-MOSFETs

The SC type I and II waveforms for M1 are shown in Fig. 1 (a). The duration of the SC event is limited to 1 µs to avoid possible destruction. The OFF-state gate voltage was set to 0 V to prevent the negative $V_{G,th}$ shift. Before the SC II event, the MOSFET was carrying a 13 A load current, which is the application-near current according to the datasheet of M1. The most considerable difference compared with the SC I is the desaturation process of the drain-source voltage V_{DS}. Due to the desaturation process, a displacement current flows through the Miller-capacitance C_{GD} from drain to gate and further charges the gate-source capacitance C_{GS} [6]. Hence, a gate voltage overshoot can be observed in the SC II measurement just after around 0.1 µs. As a consequence of the V_{GS} overshoot, a higher current peak is recorded as well. After approximately 0.27 µs, the SC II behavior is analogous to the SC type I. Although the SC II current peak is higher, the short circuit energy E_{SC} for both SC types is still comparable.

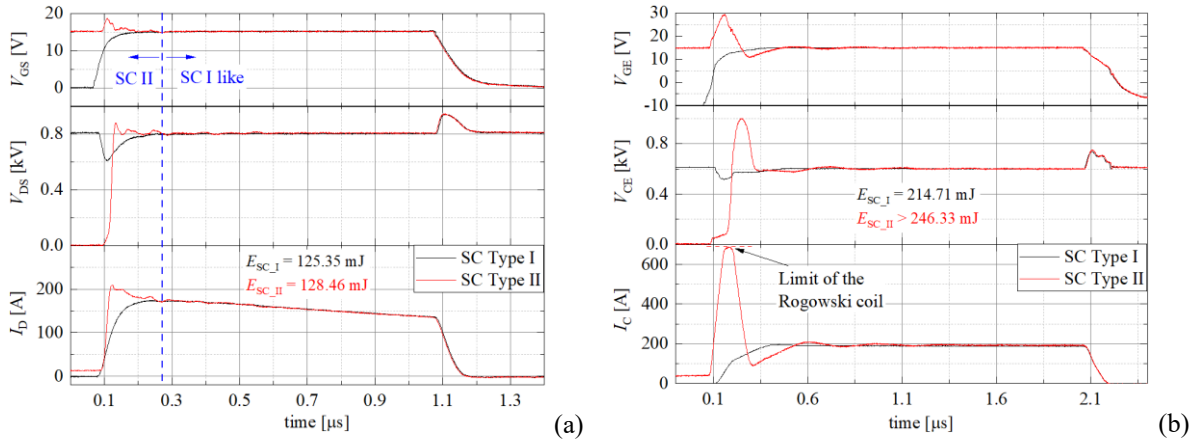


Fig. 1: (a) SC type I and II behavior comparison for M1, V_{DS} = 800 V, $R_{G,ON}$ = 7.5 Ω, $V_{GS,OFF}$ = 0 V, $V_{GS,ON}$ = 15 V, room temperature; (b) SC II for Si-IGBT, V_{CE} = 600 V, $R_{G,ON}$ = 7.5 Ω, $V_{GS,OFF}$ = -10 V, $V_{GS,ON}$ = 15 V

For comparison, the SC II behavior of a 1.2 kV, 40 A rated IGBT (IKY40N120CH3) is shown in Fig. 1 (b), a more significant Miller-capacitor feedback can be detected. For both measurements, no clamping circuit for gate voltage was utilized. The measured gate voltage overshoot of IGBT reaches 30 V, which leads to a current peak of more than 700 A. This current value already exceeds the measurement range of the used 600 A Rogowski coil. In addition to higher currents, the induced voltage peak from negative dI_C/dt is another possible cause of failure. Because the avalanche breakdown robustness of Si-IGBTs is weaker compared with SiC-MOSFETs. The reason for this less critical SC II behavior for SiC-MOSFET M1 should be the low ratio between the charge from the Miller-capacitance Q_{GD} and the gate-source capacitance C_{GS}. In Fig. 2, this ratio is expressed versus the drain-source voltage and is based on the static voltage-dependent capacitances (C-V) measurement. With the increased DC-link voltage (here expressed via V_{DS}), the Miller-effect becomes more and more pronounced. It can be seen from Fig. 2 that the ratio for SiC-MOSFETs is remarkably lower compared with IGBTs from the comparable

current/voltage class except for M2 from ROHM. At 800 V, the ratio for M1 and M3 is around 5.5 V and 4.5 V, respectively. For M2, the ratio is even higher than for a similar IGBT.

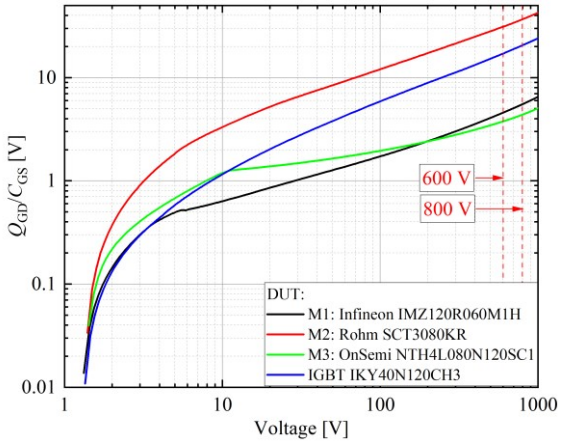
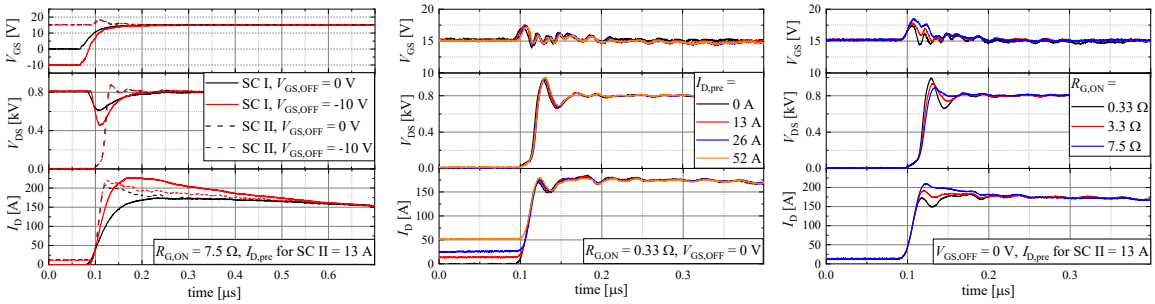


Fig. 2: Ratio between Q_{GD} and C_{GS} for SiC-MOSFETs and a comparable IGBT based on the static C-V measurement

However, it has to be emphasized that this ratio is just a rough estimation for the intensity of the Miller-effect under the SC II condition. Two essential factors are not considered for this estimation. The first is the gate-voltage-dependent gate capacitor (MOS-capacitor), and the second is the gate-drive loop impedance, which will be discussed in the following. Nevertheless, as a consequence of the much smaller C_{GD}, the Miller-feedback is in general weaker for SiC -MOSFETs under the SC II condition.

The effect of the OFF-state gate voltage $V_{GS,OFF}$, conduction current, and the turn-ON gate resistance $R_{G,ON}$ on the SC II behavior for M1 is shown in Fig. 3. Because the main consideration in SC II is in the desaturation stage, the subsequent SC characteristics are similar to SC I. Therefore, the following test results only exhibit the SC behavior around the desaturation stage.



(a) (b) (c)

Fig. 3: Short circuit behavior for M1 with the effect of (a) $V_{GS,OFF}$ for SC I and SC II; (b) conducting current $I_{D,pre}$; (c) $R_{G,ON}$

At lower $V_{GS,OFF}$ during OFF-state, more positive charges from the p-region can be trapped at the SiO_2/SiC interface, due to the significantly higher trap density compared to the Si/SiO_2 interface [1]. This positive trapped charge acts similar like a positive gate voltage and leads to a dynamically negative shift of $V_{G,th}$. Therefore, the SC current peak becomes higher with lower $V_{GS,OFF}$. However, this effect is less pronounced under the SC II condition. The difference of the current peak caused by the $V_{GS,OFF}$ is around 55 A and 13 A for SC I and SC II, respectively. Because during the conduction phase before SC II, a positive gate voltage has already been applied, which pushes away the trapped positive charges. Meanwhile, a neutralizing process between channel electron current (load current) and trapped charges takes place. Both effects simultaneously attenuate the negative shift of $V_{G,th}$. Therefore, the influence of $V_{GS,OFF}$ on the SC II current peak is not as significant as that of SC I. In general, this effect depends on the applied turn-ON gate voltage $V_{GS,ON}$, the conduction current, conduction duration, and the operating temperature.

The influence of the conduction current is given in Fig. 3 (b). The pre-conducted current $I_{D,pre}$ was increased from 0 A to 4 times application-near current (52 A), $V_{GS,OFF}$ was set to 0 V to prevent the influence of the trapping effect

for this measurement. There is almost no visible difference in the SC behavior that can be found. As a unipolar device, the channel current determines the total current flowing through the MOSFET, if the operating temperature is not extremely high, which could trigger the parasitic npn-transistor. With simplification that neglects the JEFET effect, different currents can be represented with different electron drift velocities in the channel:

$$J_D = J_n = n_{ch} \cdot q \cdot v_n = n_{ch} \cdot q \cdot \mu_n \cdot E_{ch} \tag{1}$$

where n_{ch} is the electron density in the channel, E_{ch} is the electrical field strength across the channel. As the conducting current increases, the device will move earlier from the ohmic-region into the current saturation region. But there is no plasma sweep-out process like in bipolar devices during desaturation, e.g. in IGBTs. Therefore, different currents hardly affect the short-circuit characteristics of the device, especially the current and voltage peaks. In Fig. 3 (c), the influence of $R_{G,ON}$ on the SC behavior is shown. The total capacitive charge from C_{GD} during the desaturation flows to the C_{GS} and is discharged by the gate loop simultaneously. The discharge process of overcharged C_{GS} depends on the output stage topology of the Gate Drive Unit (GDU) and mainly the gate resistance (internal and external) for a low inductive gate connection, which is described in [5]. Before SC II and III, C_{GS} is already fully charged to the static ON-state voltage and the GDU holds the turn-ON signal. Therefore, only $R_{G,ON}$ is involved in the gate loop for a source and sink separated GDU output stage. With increased $R_{G,ON}$, the GDU and MOSFET are more de-coupled, more capacitive charge flows into C_{GS} and leads to a higher V_{GS} overshoot and accordingly a higher current peak. Meanwhile, the induced voltage peak caused by the negative dI_D/dt becomes smaller. This can also be seen for M2 and M3 as shown in Fig. 4 [7].

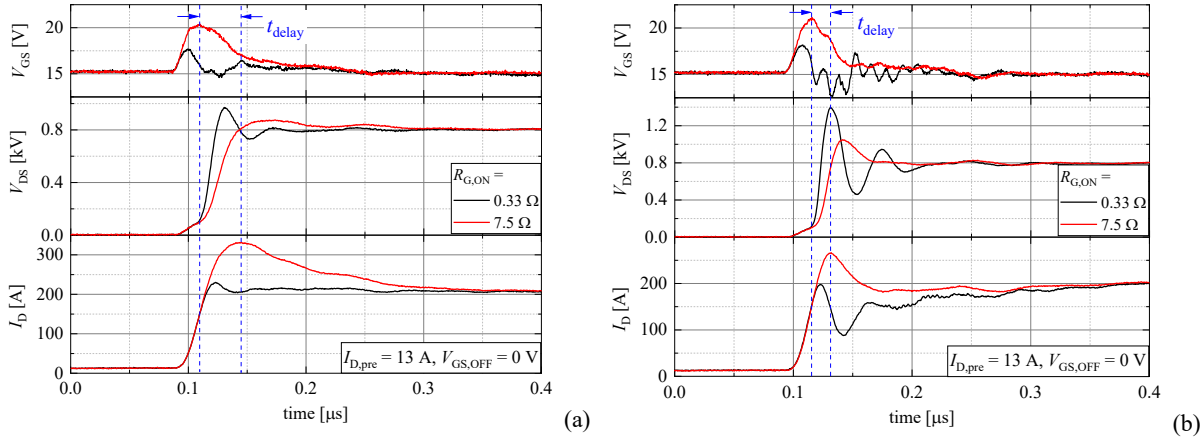


Fig. 4: SC II measurement with different $R_{G,ON}$, (a) M2 with double trench gate, (b) M3 with planar

As can be seen from Fig. 3 and 4, the gate impedance has the most impact on the SC II behavior. A trade-off between current peak and voltage peak has to be made. The relation between current peak and voltage peak according to the gate resistance is explained in [7]. Further, the different gate structures have a distinct response for varied $R_{G,ON}$. The SC II behavior of M2 with double trench gate is relatively soft even with very small (0.33 Ω) external $R_{G,ON}$. In contrast, M3 has an excessive voltage peak around 1.4 kV with the same condition due to the steep negative dI_D/dt. This voltage peak is close to the measured static avalanche breakdown voltage. Hence, such a voltage peak could force the DUT into avalanche mode and lead to potential destruction. The reason for this phenomenon may be due to different gate structures and their capacitive conditions. On the other hand, the integrated internal gate resistor $R_{G,int}$ (see Table I) on the chip, which is only 1.6 Ω for M3, while for M2 it is 12 Ω.

One interesting point that can be found in Fig. 4 is the time offset between the V_{GS} peak and the current peak for all three DUTs marked as t_{delay} for $R_{G,ON}$ = 7.5 Ω for M2 and M3. At the early phase of the SC II (from the starting of desaturation to SC I like operation), the increased chip temperature should not be high enough to trigger already the parasitic npn-transistor. Therefore, the total current is still the electron current across the channel, which is controlled by the applied V_{GS}. Hence, a higher gate voltage should cause a higher current peak according to the saturation current equation for MOSFETs:

$$I_{D,sat} = \frac{W \cdot \mu_n \cdot C_{OX}}{L} \cdot \left(V_{GS,ON} - V_{G,th}\right)^2 \tag{2}$$

where W and L are channel width and channel length, respectively. C_{OX} is the gate-oxide capacitance. Two main factors cause this time offset t_{delay}: first, a measurement error is caused by the chip integrated $R_{G,int}$ and the gate inductance from the internal gate bond wire. Hence, a precise gate voltage measurement is almost not possible at the outside of the device packaging. The measured value is lower than the real chip V_{GS} if the gate current flows

out of the gate. Besides this measurement error, the significant short-channel effect or Drain Induced Barrier Lowering (DIBL) effect plays a major role in this offset. The $V_{G,th}$ depends on the applied drain-source voltage V_{DS}. After the onset of the SC II, the current increases rapidly to the saturation value for the applied V_{GS}, V_{DS} rises slowly in this interval and holds on a low value. At the time point before fast desaturation, V_{GS} reaches the maximum, but the current does not. During the desaturation process (interval t_{delay} for $R_{G,ON}$ = 7.5 Ω), the increased V_{DS} leads to a continuously decreased $V_{G,th}$. Hence, the SC current further increases after the V_{GS} peak according to Eq. (2). In other words, although the V_{GS} reaches the maximum, the SC current value is limited due to the high $V_{G,th}$ at low V_{DS} condition. Therefore, SC II behavior of SiC-MOSFETs is relatively soft compared to IGBTs. In addition, the negative temperature-dependency/coefficient of $V_{G,th}$ is also more pronounced due to the higher temperature rise rate of SiC-MOSFETs in SC operation [8]. This could lead to a further increase in the current value. At the current peak, the dI_D/dt is equal to zero, and V_{DS} reaches to the DC-link voltage.

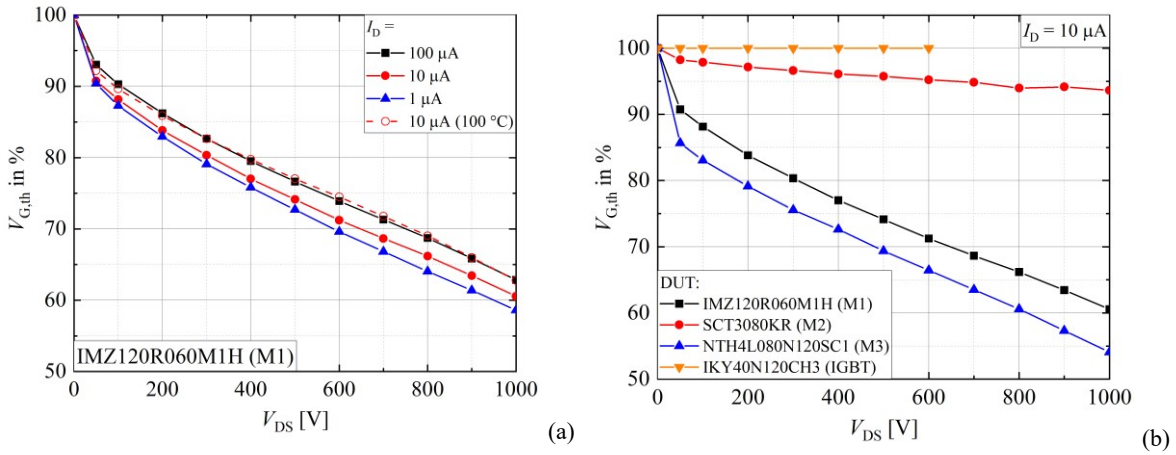


Fig. 5: (a) current and temperature dependency of the DIBL-effect for M1; (b) DIBL-effect for different DUTs

Fig. 5 shows the measurement of the DIBL effect. $V_{G,th}$ is extracted at I_D which is 10 µA to avoid self-heating. The current and temperature dependency of the DIBL effect for M1 is shown in Fig. 5 (a), the difference on the slope is negligible. It can be seen from Fig. 5 (b) that when the voltage increases to a specific value, (around 50 V), the threshold voltage shows a linear reduction with the increase of V_{DS}. This is valid for the asymmetric trench gate DUT (M1) and planar gate DUT (M3), where the DIBL effect is significant. $V_{G,th}$ is decreased about 34% and 40% at V_{DS} = 800 V, respectively. For the double trench gate structure (M2), the DIBL effect is weaker (5% at 800 V), and for the IGBT no DIBL-effect can be observed until 600 V. The reason for this phenomenon is on the one hand due to the lower electric field strength at the front-side p-region and n-base junction for IGBTs. On the other hand, it may be due to the particular electric field shielding structure, which reduces the influence of the electric field on the channel region, such as for the M2 double trench gate.

There are two concerns that cannot be explained with the performed measurements. First, for M2, although it has the biggest Q_{GD}/C_{GS} ratio, the corresponding SC II characteristic is not like that of IGBTs, which has a very high current peak. Moreover, attributed to its weak DIBL effect, $V_{G,th}$ should be hardly affected by V_{DS}. However, a large time shift between the V_{GS} and I_D (t_{delay}) peaks can still be observed in Fig. 4 (a). One possible reason for this behavior is the large internal gate resistance caused measurement error. The second point is that for the M3 device, as shown in Fig. 2, the Q_{GD}/C_{GS} ratio is the minimum, the V_{GS} overshoot due to the Miller-effect alone should not be higher than 5 V. However, the measured peak gate voltage is about 21 V under the condition of $R_{G,ON}$ = 7.5 Ω. Meanwhile, V_{DS} at this time is only around 100 V, see Fig. 4 (b). Considering the presence of $R_{G,int}$, the actual V_{GS} should be even higher than the measured value. Therefore, a hypothesis can be constructed here: the gate voltage overshoot in SC II should not only be generated by the Miller-effect but there should be other unrecognized effects that dynamically affect V_{GS} in the process of current rising. Furthermore, under SC II condition, the current could be limited by other factors besides the gate voltage, such as the low channel electron mobility and the electric field applied across the channel. These open questions will be further investigated with the help of semiconductor device simulation in the future.

Short Circuit Type III Behavior of SiC-MOSFETs

In this section, the SC type III behavior is discussed, the utilized pulse pattern is explained in Fig. 6. In time interval t_1, the high-side auxiliary switch is turned-ON, the load current flows through the HS-switch and the load inductor L_{load}. The freewheeling current through the body diode $I_{D,BD}$ can be adjusted by changing the time of this period. In t_2, the HS-switch is turned-OFF and the BD starts to carry the load current. Depending on the applied gate voltage, the Body Diode (BD) can be operated in bipolar mode or the current flows unipolar via the channel. When the applied $V_{GS,OFF}$ is low enough, the channel will be completely closed. In this case, the current flows entirely through the BD in bipolar mode. When $V_{GS,OFF}$ is not low enough or equals zero, the current will be shared by BD and the channel due to the body-effect [9]. In this circumstance, the injection of holes from p-region is small.

To demonstrate the effect of plasma on the SC III behavior, $V_{GS,OFF}$ = -10 V was selected for M1, and -5 V for M2 and M3 during t_2. The duration of t_2 is fixed to 5 µs, to ensure that the BD enters a stable working state and the plasma distribution is stable as well. In interval t_{detrap}, the gate voltage of the DUT shifts to +15 V, the channel is opened. After this time point, the MOSFET works in the reverse conduction mode. This time period is defined as t_{detrap}, because the negative shift of the $V_{G,th}$ in t_2 is gradually compensated during this time. $V_{G,th}$ gradually increases with the increase of t_{detrap}. After t_{detrap}, the auxiliary switch turns-ON again to trigger SC III. The reverse recovery process of the BD starts, the current commutates to the channel and continues to rise to the peak value. The voltage and current waveforms are similar to SC type II. The minimum value of t_{detrap} was set to 50 ns. Because if t_{detrap} is 0, the DUT is turned-ON at the same time as the auxiliary switch. The turn-ON process of the aux. switch will affect the SC III characteristics of the DUT.

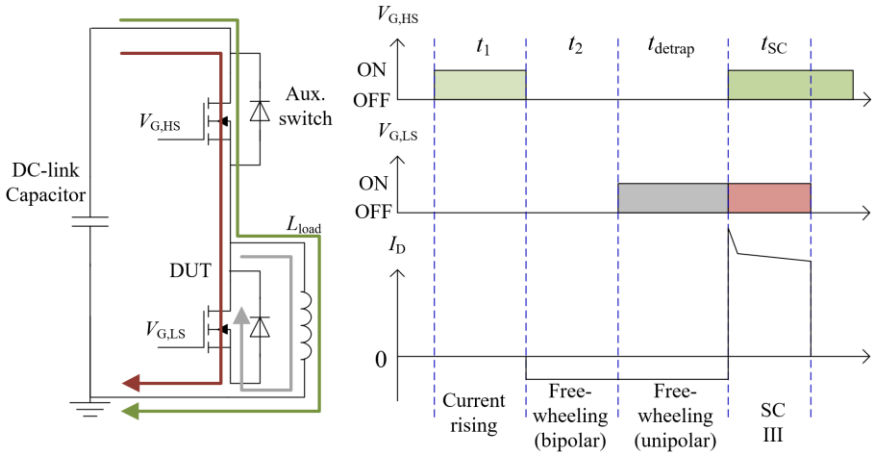


Fig. 6: SC type III test setup and pulse pattern

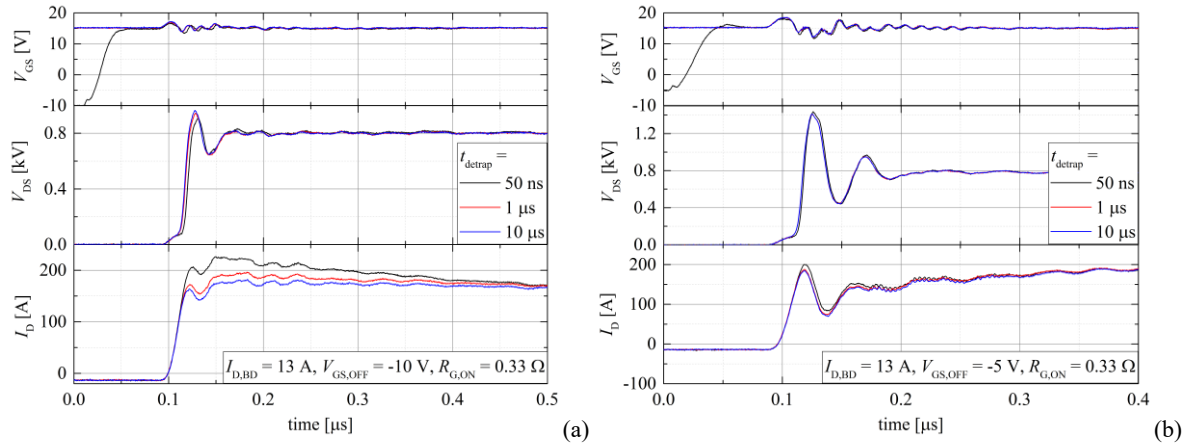


Fig. 7: SC type III behavior with different t_{detrap}: (a) M1, $V_{GS,OFF}$ = -10 V; (b) M3, $V_{GS,OFF}$ = -5 V

Fig. 7 (a) shows the effect of the de-trapping time t_{detrap} in the SC III behavior of M1. Since -10 V was applied to the DUT during t_2, therefore, the current flows entirely through the body-diode. When t_{detrap} is reduced to 50 ns, the dynamic $V_{G,th}$ of the DUT becomes the smallest, the hysteresis effect is most pronounced. Hence, the corresponding SC current peak value is the maximum. This current peak decreases with increasing t_{detrap}. The results for M2 are similar to M1, but a distinct result was measured for M3, as shown in Fig. 7 (b). The difference

of the current peak is smaller and the peak value remains the same for t_{detrap} = 1 µs and 10 µs. This should be firstly related to a smaller $V_{G,th}$ hysteresis due to the lowest interface trap density of M3, which can be confirmed with a sub-threshold sweep in Fig. 8. The second reason could be the applied negative gate voltage (-5 V), which is not fully close the channel due to the body-effect. Hence, a small electron current can already flow through the channel and neutralize the trapped positive charge during t_2. Nevertheless, with this test setup, the negative gate voltage during t_2 can be further decreased to close the channel completely. But the DC-link voltage has to be reduced to avoid the possible critical electrical field in the oxide layer. t_{detrap} can be freely adjusted until the current peak reaches a stable value, which means that the trapped positive charge is fully neutralized. With this method, the time constant of the de-trapping phase for specific current and temperature can be estimated. For instance, the time constant of the de-trapping phase for M3 under given conditions is smaller than 200 ns.

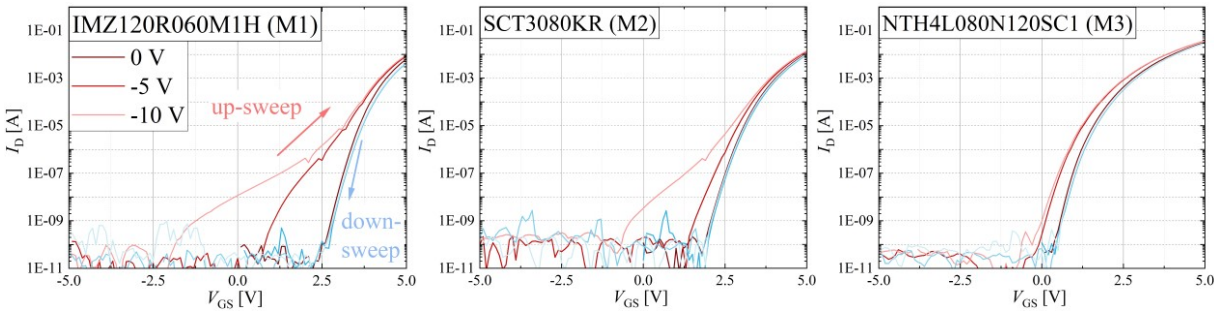


Fig. 8: Sub-threshold sweep from V_{GS} = -10, -5 and 0 V to V_{GS} = 15 V (up-sweep) and vice versa (down-sweep), V_{DS} = 0.1 V, I_D is limited to 500 mA

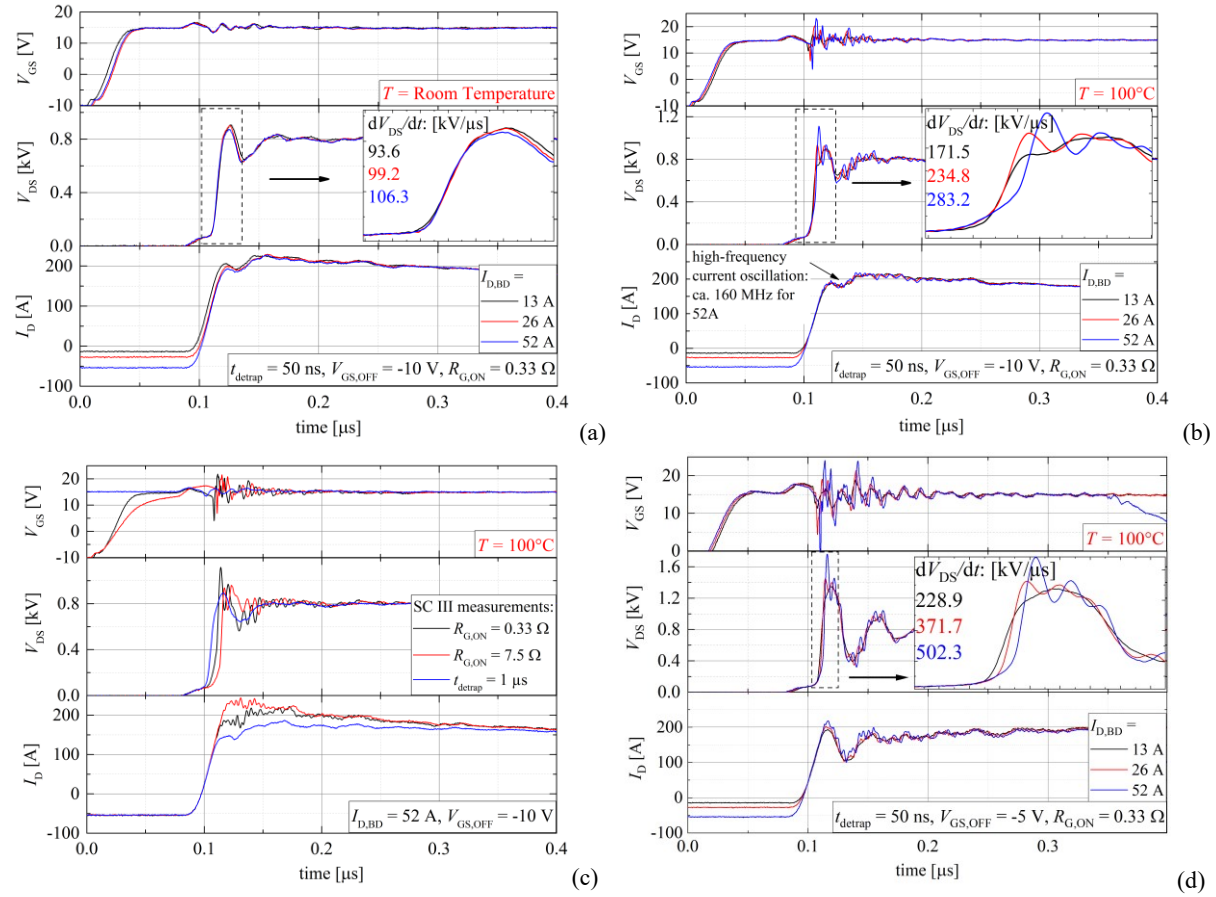


Fig. 9: (a) SC III behavior with different body diode current for M1 at room temperature; (b) at 100 °C. (c) Influence of the $R_{G,ON}$ and de-trapping time t_{detrap}, $I_{D,BD}$ = 52 A at 100 °C, t_{detrap} = 50 ns if not declared otherwise. (d) SC III behavior with different $I_{D,BD}$ for M3 at 100 °C, for $I_{D,BD}$ = 52 A, only 300 ns SC pulse was given to avoid a possible destruction.

The effect of different BD currents $I_{D,BD}$ on the SC III characteristics of M1 at room temperature is shown in Fig. 9 (a). The maximum dV_{DS}/dt during the desaturation is given in the figure as well. It can be seen that $I_{D,BD}$ value

is hardly affecting the SC III characteristics. On the one hand, due to the wide bandgap of SiC material, p-doping cannot be fully ionized at room temperature [1]. Consequently, the emitter efficiency of the BD is quite low, despite the fact that the BD is working in the bipolar mode during t_2, which causes a specific density of plasma inside the MOSFET. But the plasma density is extremely low; although the current value is high. On the other hand, the minority carrier lifetime of SiC devices is much lower compared to Si-counterparts at room temperature [1]. The stored charge carriers are probably fully recombining in the t_{detrap} stage before SC occurs. Therefore, basically no influence from $I_{D,BD}$ on the SC III characteristics can be observed at room temperature.

However, when the temperature of the device increases, the minority carrier lifetime and the p-emitter efficiency of the BD increase simultaneously. The plasma may not fully be recombined after t_{detrap} and needs to be swept out during the reverse recovery process in SC III. Therefore, the value of $I_{D,BD}$ will affect the SC III characteristics. As shown in Fig. 9 (b) at 100°C, the peak value of the SC current decreases slightly due to the decreased electron mobility. But the gate voltage and drain-source voltage oscillate strongly. The oscillations become more severe as the current increases. The maximum dV_{DS}/dt at $I_{D,BD}$ = 52 A increases strongly from 106.3 kV/µs to 283.2 kV/µs. The frequency of this oscillation is approximately 160 MHz. The oscillations and V_{DS} spikes can be damped with a larger gate resistor. Besides, if t_{detrap} extends, the plasma could already recombine completely before SC III, and will hence no longer affect the SC characteristics as shown in Fig. 9 (c) where the blue current peak with t_{detrap} = 1 µs is the smallest.

For M2 with a double trench gate, the effect of the temperature on the SC behavior is not apparent. This is firstly due to the large 12 Ω internal gate resistor, which damps the oscillations. On the other hand, the selected $V_{GS,OFF}$ was -5 V during the t_2 phase. This voltage is already lower than the V_{GS} surge value specified in the datasheet (-4 V), but it may still not totally close the channel due to the body-effect. Hence, a part of the current flows through the channel during t_2. The plasma density in the MOSFET could be negligibly low before the short circuit. For M3 with a planar gate in Fig. 9 (d), the effect of the temperature is analogous to M1. However, due to the smaller $R_{G,int}$, the V_{DS} oscillation and the maximum dV_{DS}/dt of the device are even more pronounced than that of M1. For $I_{D,BD}$ = 13 A, the induced voltage peak already reaches 1350 V, which is above the rated blocking voltage. At 26 A and 52 A, it reaches 1420 V and 1764 V, respectively. In this case, the device will inevitably enter the avalanche mode.

In practical applications, the current and temperature are determined by the MOSFETs operating conditions, and SC can occur at any time of t_{detrap}. Therefore, to realize a better short circuit robustness, the external gate resistance should be carefully considered.

Conclusion

In general, due to the smaller Miller-capacitance and the significant DIBL effect of SiC-MOSFETs, the current overshoot of SC II is much smaller than that of IGBTs. Therefore, from the perspective of short-circuit energy, the SC II behavior of SiC-MOSFETs is not more critical than SC type I. The choice of the gate resistor should be carefully considered because it affects the current peak and induced voltage peak, which is similar to IGBTs.

The SC type III characteristics at room temperature are similar to SC II. The low plasma density at room temperature hardly influences the reverse recovery of the body diode under SC condition. When the temperature increases, the plasma effect on the reverse recovery of the BD can be observed from high-frequency oscillation and high induced voltage peak. However, a destruction could not be observed during the reverse-recovery phase, even at very high dV/dt. With a small R_G in combination with a short de-trapping time (the time difference between the application of positive gate voltage after bipolar conduction and the occurrence of SC), the device could enter the avalanche mode after the onset of SC III.

The reasons for the oscillation in the SC type III and the reverse recovery process of the body diode under short circuit condition will be further studied with the help of semiconductor device simulation in the future.

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