Influence of DC Supply Voltage Unbalances on the Performance of ARCP Inverters

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Keywords

«DC-AC converter», «Voltage Source Inverter (VSI)», «Soft switching», «ZCZVS converters», «Calculation method»

Abstract

The auxiliary resonant commutated pole inverter (ARCPI) is an attractive soft switching topology due to its small Electromagnetic Interference (EMI), voltage and current stresses. This topology has previously been investigated for balanced DC input voltages, which not always occur in practical applications. This paper therefore presents an analysis of an ARCPI with unbalanced DC supply voltage to determine necessary conditions to also achieve soft switching for reduced losses in the load current switches under such conditions. First, the necessary timings of the switches are calculated and validated through simulation. Then, possibilities to optimize the behavior of this topology are discussed.

Introduction

Increasing the switching frequencies of power electronic converters is a proven technique to enable smaller passive components within converters and, consequently, to reach a higher power density. However, switching frequencies cannot be increased to arbitrarily high values due to the switching losses of power semiconductors and EMI radiation that occur in hard-switching topologies. One approach to handle these limitations for power electronic inverters is the Auxiliary Resonant Commutated Pole Inverter (ARCPI), introduced in [1, 2]. The ARCPI (Figure 1) permits zero voltage switching (ZVS) conditions and provides significantly reduced switching losses, dv/dt and di/dt for its main switches [3]. To ensure soft switching for real-world applications, the influence of unbalanced input dc voltage should be investigated carefully. In this paper, this effect on the ARCPI operation is analytically analyzed and confirmed through simulation.

For this investigation, the split dc input capacitors are modeled through voltage sources V_{S1} and V_{S2}, respectively (see Figure 1). Furthermore, we assume ideal properties for all sources, passive components and switches. A constant output load current I_{Load} is assumed over the investigated commutation cycle, flowing in the direction marked in Figure 1. The resonance frequency ω_r, the effective resonant

capacitance C_r, the characteristic impedance of the auxiliary resonant circuit $Z_{r,}$ and the input DC voltage V_{dc} are defined through (1) – (4).

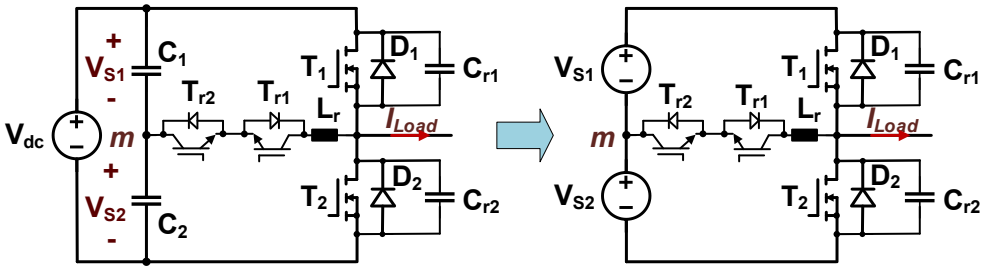

Figure 1: Circuit scheme and equivalent circuit of the auxiliary resonant commutated pole inverter.

$$C_r = 2\,C_{r1} = 2\,C_{r2} \tag{1}$$

$$\omega_r = \frac{1}{\sqrt{L_r\,C_r}} \tag{2}$$

$$Z_r = \sqrt{{L_r}/{C_r}} \tag{3}$$

$$V_{dc} = V_{S1} + V_{S2} \tag{4}$$

A variable timing method that ensures soft switching with minimized losses over a wide DC input voltage range has been presented in [3]. The timings of the gate-signals of the auxiliary switches $T_{r1}$and T_{r2} vary depending on the load current and dc-link voltage. The length of the overlap between the two gate signals of one of the main switches T_1 and T_2 and the corresponding auxiliary switch is called overlapping time. The overlapping time for a commutation from the high-side switch to the low-side switch is called t_{ovp1} while the overlapping time for the reverse commutation is called t_{ovp2}. This paper will focus on the commutation from D_2 through T_2 and T_{r2} to T_1, illustrated in separate phases of the commutation in Figure 2, and therefore the calculation of t_{ovp2}. The pulse width of the auxiliary switch has to be calculated and applied to variable timing control for each commutation process since the output current changes between each switching event, thus altering the necessary timing values [3].

Operational modes and calculation of the resonant current

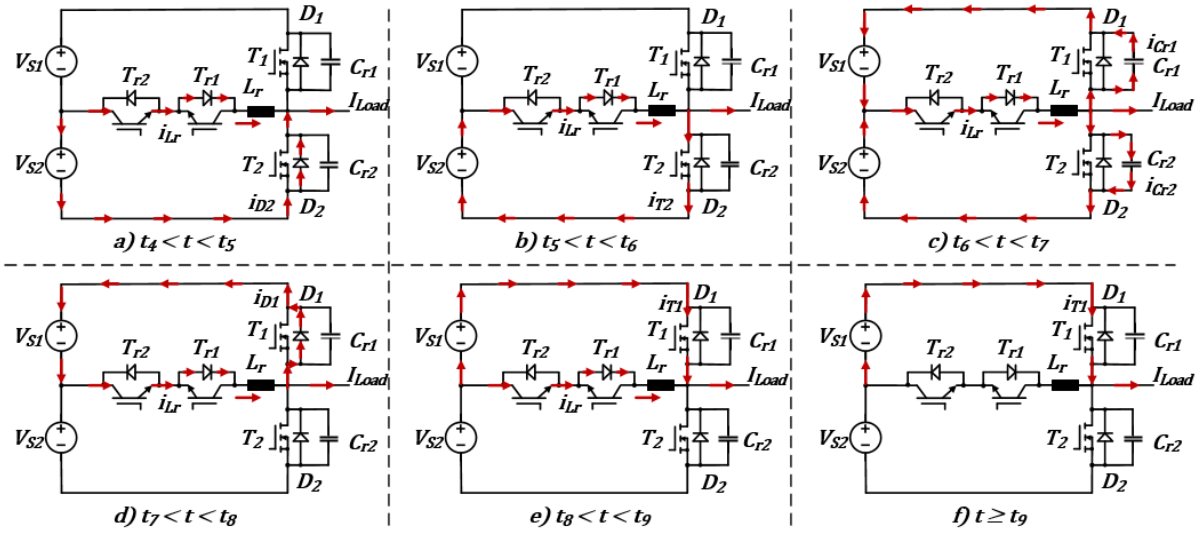

Figure 2: Transition states and time intervals of the commutation from a conducting lower diode D_2 to the upper main switch T_1.

The circuit can operate both with balanced or unbalanced dc input voltages, if the voltage imbalance is not too large. The following investigation is performed for a positive output current I_{Load}, starting with both main switches T_1 and T_2 turned off while D_2 conducts the load current (Fig. 2a) (5).

$$i_{D2}(t_0) = I_{Load} \tag{5}$$

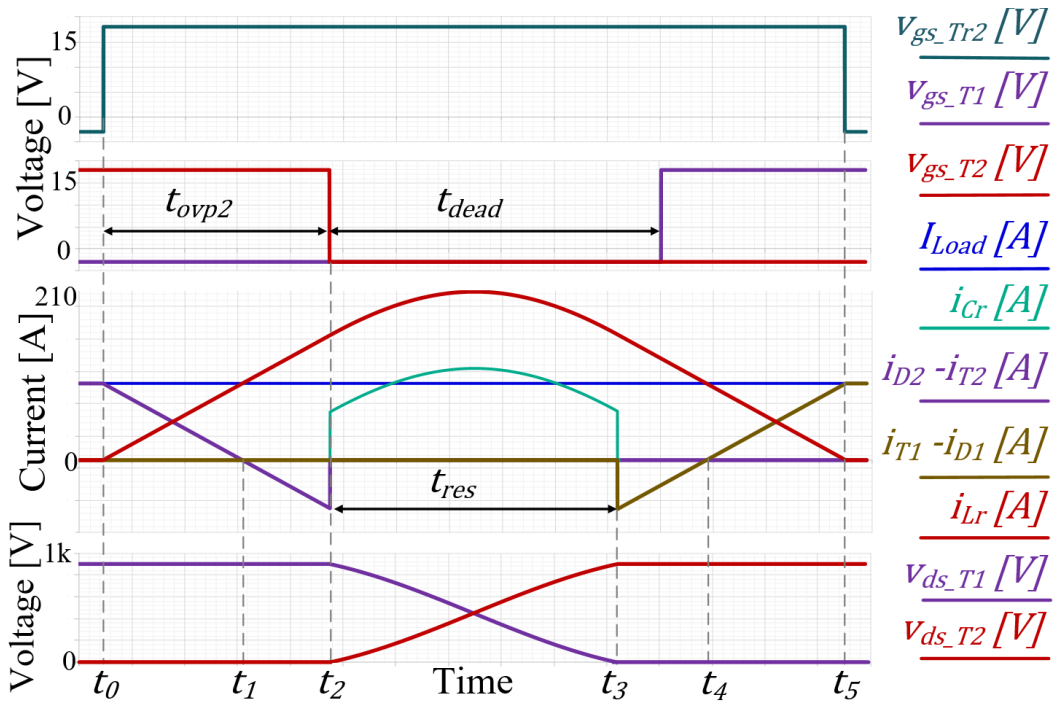

Figure 3: Voltage and current waveforms for commutation from D_2 to T_1 for $V_{S1} = V_{S2}$ and $I_{Load} > 0$.

A. Balanced operating mode: $V_{S1} = V_{S2} = V_{dc}/2$

The balanced operation of the ARCPI was previously analyzed in [3]. Figure 3 shows the ideal commutation from D_2 to T_1 and subsequently ZVS and ZCS operation of the main switch T_1. Referring to [3], the timing values for balanced dc voltages can be calculated as (6) – (8), where I_{off_T2} is the cutoff current of T_2 at $t = t_2$.

$$t_{ovp2} = t_2 - t_0 = t_5 - t_3 = \frac{2\,L_r}{V_{dc}}\left(I_{Load} + I_{off\_T2}\right) \tag{6}$$

$$t_{diode\_cond} = t_4 - t_3 = t_2 - t_1 = \frac{2\,L_r}{V_{dc}}\,I_{off\_T2} \tag{7}$$

$$t_{res} = 2\sqrt{L_r\,C_r}\,tan^{-1}\left(\frac{V_{dc}}{2\,Z_r\,I_{off\_T2}}\right) \tag{8}$$

These results will now be derived for and compared to the operation under unbalanced dc input voltages.

B. Unbalanced operating mode: $V_{S1} \neq V_{S2}$

The following calculations correspond to the commutation phases shown in Figure 2; the resulting calculated waveforms for unbalanced operation are shown in Figure 5.

Phase a and b: $t_0 \leq t \leq t_2$

T_{r2} is switched on and the current of the auxiliary inductance L_r rises linearly (9). Consequently, the diode current I_{D2} decreases and reaches zero at $t = t_1$ (10). The gate of T_2 is activated at or before $t = t_0$ and has to be kept active until $t = t_2$ so that T_2 starts conducting in the opposite direction as D_2 (11) and reaches I_{off_T2} (12).

$$i_{Lr}(t) = \frac{V_{S2}}{L_r}(t - t_0) \tag{9}$$

$$i_{D2}(t) = I_{Load} - \frac{V_{S2}}{L_r}(t - t_0) \tag{10}$$

$$i_{T2}(t) = \frac{V_{S2}}{L_r}\,(t - t_1) \tag{11}$$

$$I_{off\_T2} = i_{T2}(t = t_2) = \frac{V_{S2}}{L_r}\,t_{ovp2} - I_{Load} \tag{12}$$

The overlapping time t_{ovp2} can be expressed in terms of the cutoff current I_{off_T2} of T_2 (13) and the conduction time of T_2 can be calculated as (14) by inserting $t = t_2$ into (11).

$$t_{ovp2} = \frac{I_{Load} + I_{off\_T2}}{V_{S2}}\,L_r \tag{13}$$

$$t_2 - t_1 = \frac{I_{off\_T2}}{V_{S2}}\,L_r \tag{14}$$

Phase c: $t_2 < t \leq t_3$

T_{r2} is still on and T_2 is switched off, thus begins the resonant period. The time interval $[t_3 - t_2]$ is called resonance time t_{res}. During this period, the resonant capacitor C_{r1} will discharge from V_{dc} to almost zero, while C_{r2} will charge vice versa. The current of the resonant inductor i_{Lr} and the voltages of the resonant capacitors v_{Cr1} and v_{Cr2} can be obtained through (15) – (17).

$$i_{Lr}(t) = I_{Load} + I_{off\_T2}\cos\big(\omega_r(t - t_2)\big) + \frac{V_{S2}}{Z_r}\sin\big(\omega_r(t - t_2)\big) \tag{15}$$

$$v_{Cr1}(t) = V_{S1} + V_{S2}\cos\big(\omega_r(t - t_2)\big) - I_{off\_T2}\,Z_r\sin\big(\omega_r(t - t_2)\big) \tag{16}$$

$$v_{Cr2}(t) = V_{S2} - V_{S2}\cos\big(\omega_r(t - t_2)\big) + I_{off\_T2}\,Z_r\sin\big(\omega_r(t - t_2)\big) \tag{17}$$

At the end of the resonant period, i.e. at $t = t_3$, the resonant capacitor C_{r1} is almost discharged. Therefore, the resonant time can be calculated from the equations above, through evaluation at $t = t_3$, as (18).

$$t_{res} = t_3 - t_2 = 2\sqrt{L_r C_r}\;tan^{-1}\left(\frac{-I_{off\_T2}\,Z_r + \sqrt{\big(I_{off\_T2}\,Z_r\big)^2 + V_{S2}^2 - V_{S1}^2}}{V_{S2} - V_{S1}}\right) \tag{18}$$

To ensure resonant transition under the unbalanced operating conditions, the radical expression of (18) must be zero or positive. If $V_{S1} \leq V_{S2}$ this requirement is automatically fulfilled. However, if $V_{S1} > V_{S2}$, the necessary condition (19) can be obtained. Substituting (12) into (19), the requirement for the overlapping time can be given as (20).

$$I_{off\_T2} > \sqrt{\frac{C_r}{L_r}\,\frac{V_{dc}}{2}\,(V_{S1} - V_{S2})} \tag{19}$$

$$t_{ovp2} > \sqrt{L_r\,C_r}\sqrt{\left(\frac{V_{S1}}{V_{S2}}\right)^2 - 1} + \frac{I_{Load}}{V_{S2}}L_r \tag{20}$$

Equation (20) is a necessary requirement to achieve ZVS if the load current I_{Load} is positive and if $V_{S1} > V_{S2}$. Similarly, this requirement can be expressed for negative load currents and for $V_{S1} < V_{S2}$ as (21).

$$t_{ovp2} > \sqrt{L_r\,C_r}\sqrt{\left(\frac{V_{S2}}{V_{S1}}\right)^2 - 1} + \frac{|I_{Load}|}{V_{S1}}L_r \tag{21}$$

Phase d: $t_3 < t \leq t_4$

At $t = t_3$, the resonant period of the auxiliary circuit is finished. Substituting (18) into (15) yields (22) and the current of the resonant inductor for $t > t_3$ can be expressed as (23). At $t = t_3$, a negative linear ramp current starts to flow through D_1 at the same rate as i_{Lr} (24). After the gate of T_1 is activated, this current commutates to the channel of T_1. At $t = t_4$, the current of D_1 reaches zero, hence the diode conduction time can be calculated by rearranging (23) as (25).

$$I_{Lr}(t_{res}) = |i_{Lr}(t = t_3)| \tag{22}$$

$$i_{Lr}(t) = I_{Lr}(t_{res}) - \frac{V_{S1}}{L_r}(t - t_3) \tag{23}$$

$$i_{D1}(t) = I_{Lr}(t_{res}) - I_{Load} - \frac{V_{S1}}{L_r}(t - t_3) \tag{24}$$

$$t_{diode\_cond} = t_4 - t_3 = \frac{I_{Lr}(t_{res}) - I_{Load}}{V_{S1}} L_r \neq t_2 - t_1 \tag{25}$$

Comparing the result of the balanced operation (14) with the result of the unbalanced operation (25) reveals that the diode conduction times are not identical. To achieve ZVS turn-on, T_1 must be switched on during this time interval. In other words, the diode conduction time must be sufficiently long so that T_1 can be switched on.

Phase e: $t_4 < t \leq t_5$

When the gate signal of the upper switch T_1 is applied during the diode conduction time, T_1 starts conducting under ZVS conditions and a linear ramp current with a positive slope starts flowing through T_1 (26). At $t = t_5$, the resonant current i_{Lr} reaches zero and consequently, the current of the upper switch T_1 reaches the load current. Therefore, the commutation is completed and since the current slope in L_r is constant between not only t_4 and t_5, but also between t_3 and t_5, the time interval $[t_5 - t_3]$ can be derived as (27).

$$i_{T1}(t) = \frac{V_{S1}}{L_r}(t - t_4) \tag{26}$$

$$t_5 - t_3 = \frac{I_{Lr}(t_{res})}{V_{S1}} L_r \tag{27}$$

Again comparing the balanced operation result (13) to (27), it can be concluded that the length of the last linear ramp in the time interval $t_3 \leq t \leq t_5$ is not equal to the overlapping time (28). Through these equations, the waveforms for the possible voltage imbalances $V_{S1} < V_{S2}$ and $V_{S1} > V_{S2}$ can be illustrated as shown in Figure *5*.

$$t_{ovp2} = t_2 - t_0 \neq t_5 - t_3 \tag{28}$$

Simulation results

To check the accuracy of the presented equations, a single phase ARCPI model was created in Matlab/Simulink using the "Specialized Power Systems Blockset", investigating its operation at $I_{Load} = 95\ A$ and $V_{dc} = 900\ V$. In order to maintain a low current stress in the auxiliary circuit, the design strategy presented in [3] was adopted. The resonant tank parameters were then calculated to $L_r = 625\ nH$ and $C_r = 29\ nF$.

Figure 4 shows the schematic of the simulated circuit. This schematic is derived from the one shown in Fig. 1.

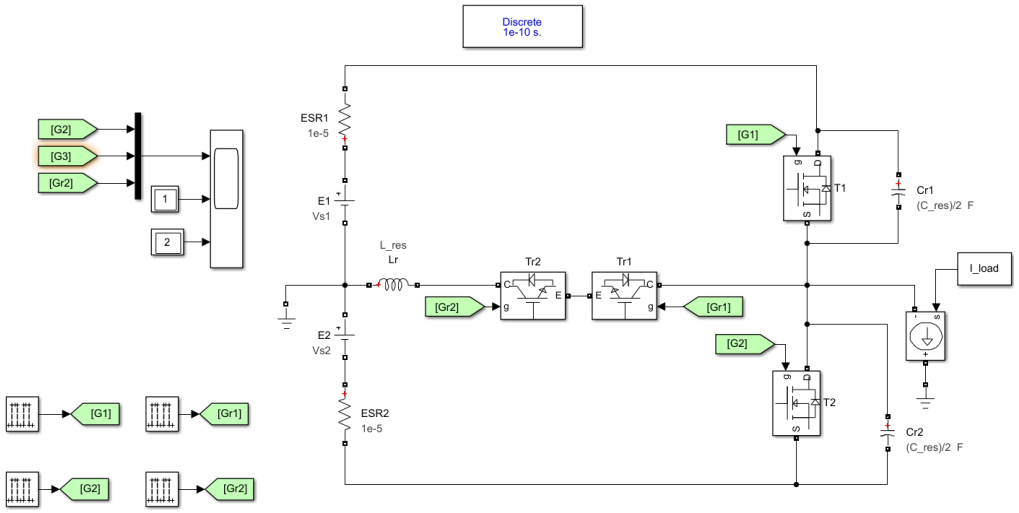

Figure 4: The simulated circuit

Simulink solver is able to work with a variable- or fixed-step sample time. Fixed-step discrete solver computes the time of the next simulation step by adding a fixed step size to the current time, and the accuracy of the resulting simulation depends on the size of the steps taken by the simulation. The smaller the step size, the more accurate the results are but the longer the simulation takes. To achieve a high accuracy, a fixed- step discrete solver with a step size of $\Delta t = 100\ ps$ was selected.
Three different simulations were conducted.

1. $V_{S1} = 300\ V$ and $V_{S2} = 600\ V$
2. $V_{S1} = 450\ V$ and $V_{S2} = 450\ V$
3. $V_{S1} = 600\ V$ and $V_{S2} = 300\ V$

The semiconductors and the passive components are modeled using the "Specialized Power Systems" device models. The two halves of the DC-link are modeled using ideal voltage sources and no parasitic properties are taken into consideration.

Table 1: Input parameters and the resulting calculated and simulated values.

Input Parameters				Results			
Case	V_{S1} [V]	V_{S2} [V]	t_{ovp2} [ns]		$\lvert\hat{I}_{Lr}\rvert$	t_{res2}	t_{diode_cond}
1	300	600	160	Calculated	236,91 A	217,82 ns	263,21 ns
				Simulated	236,52 A	217,3 ns	262,1 ns
				Difference	-0,1 %	-0,2 %	-0,4 %
2	450	450	215	Calculated	208,9 A	274,11 ns	83,06 ns
				Simulated	208,6 A	271,9 ns	84,2 ns
				Difference	-0,1 %	-0,8 %	+1,4 %
3	600	300	460	Calculated	236,43 A	219,07 ns	59,82 ns
				Simulated	236,36 A	217,8 ns	60,3 ns
				Difference	-0,03 %	- 0,06 %	+0,8 %

Table 1 summarizes important input parameters and the simulation results. Cases 1 and 3 represent extreme imbalances in the input voltages, while case 2 investigates the balanced operation. For the critical case 3 with $V_{S1} > V_{S2}$, the minimum value of t_{ovp2} can be obtained using (20):

$$t_{ovp2\_min} = 431\ ns \tag{29}$$

If this minimum time was selected, then the time interval to turn on T_2 under ZVS condition would be close to zero. Therefore, the overlapping time for the simulation is selected to $t_{ovp2} = 460\ ns$, which also provides a safety margin to account for component tolerances in physical setups. Table 1 indicates

a high precision for the proposed approach with less than 1.5 % deviation between the calculated and simulated data, confirming the derived formula.

Figures 5 und 6 shows the simulated voltage and current waveforms of the ARCP inverter under the unbalanced input voltage cases. Figure 6 shows the resonant currents $i_{Lr}(t)$ for these cases and compares them to the operation with balanced input voltage.

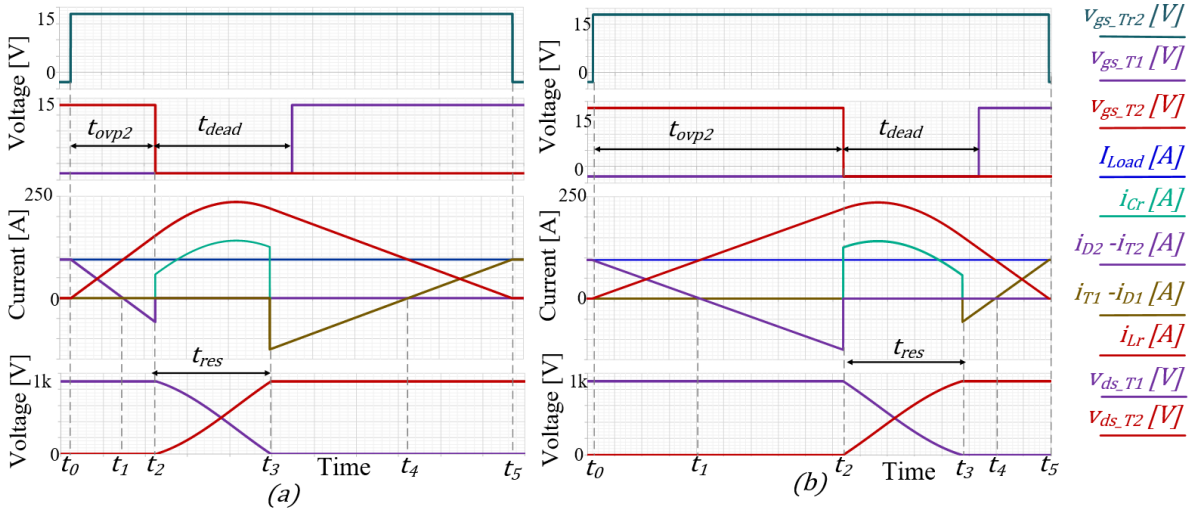

Figure 5: Voltage and current waveforms for positive load current commutation from D_2 to T_1 (a) for $V_{S1} < V_{S2}$, (b) for $V_{S1} > V_{S2}$.

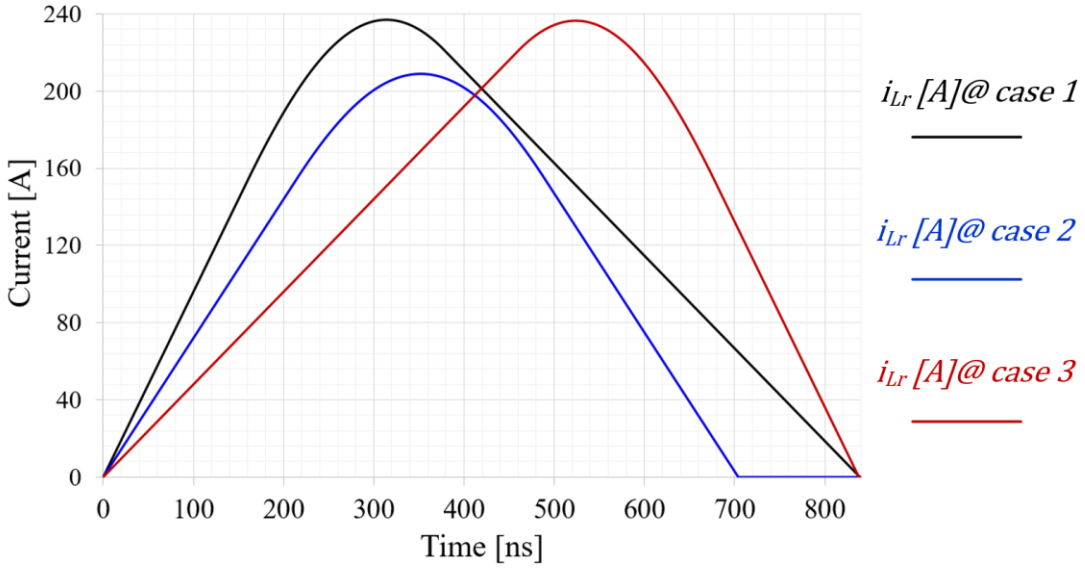

Figure 6: Comparison of the simulated resonant currents in the investigated input voltage scenarios for $L_r = 625\ nH,\ C_r = 29\ nF$ and $I_{Load} = 95\ A$.

As shown in Figure 6, the resonant currents differ considerably from each other. The minimum commutation time occurs under the balanced operating condition (blue curve). From Figures 5 and 6, it can be seen that wide variations of commutation time can be expected when input supply voltage unbalances occur.

Comparing results for different overlapping times

As previously mentioned, to achieve ZVS, the overlapping time must meet the requirement (20). If the selected overlapping time is less than the minimum value (20), then the resonant capacitor C_{r1} cannot fully discharge during the resonant period because the radical expression of (18) would be negative. Thus the diode D_1 cannot be biased in forward direction and when the main switch T_1 turns on, it quickly

discharges C_{r1}, i.e. the capacitor voltage is forced to zero. This leads to an inrush current through the main switch T_1 and subsequently causes additional switching losses in the switch T_1, since the voltage across T_1 has not yet fully dissipated at $t = t_3$, as shown in Figure 7 (b).

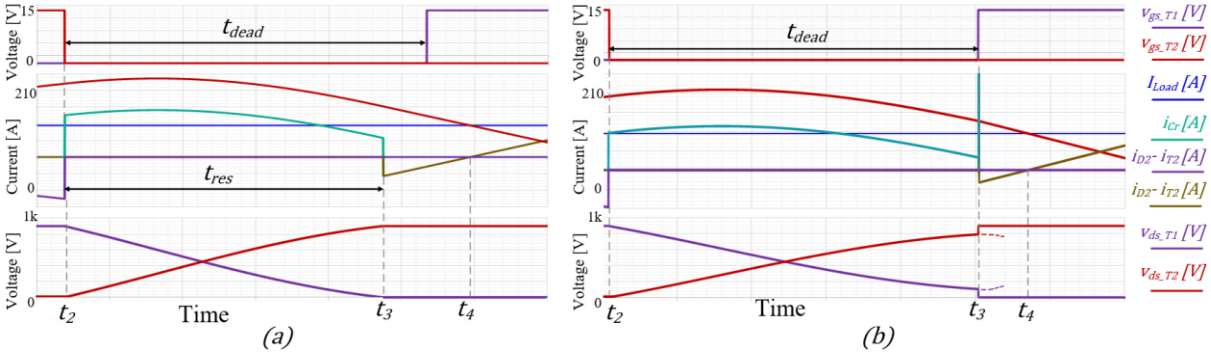

Figure 7 Extended waveforms for positive load current commutation and unbalanced input voltages $V_{S1} > V_{S2}$. (a) $t_{ovp2} = 460\ ns >\ t_{ovp2\_min}$, (b) $t_{ovp2} = 420\ ns < t_{ovp2\_min}$

From Figure 7 (b), it can be seen that no full ZVS is possible when the overlapping time is selected as $t_{ovp2} < t_{ovp2\_min}$. If the selected overlapping time remains below the minimum overlapping time (29), additional switching losses occur, which remarkably decrease the efficiency of the ARCP inverter and limit the applicable switching frequency. To prevent this from occurring, two other important design parameters can be considered:

(a) Increasing only the dead time t_{dead}

Looking at the voltage waveform of the main switches in Figure 7(b), it could be concluded that a longer dead time could further decrease the voltage across the main switch T_1. However, since L_r and C_r form a resonant network, this voltage would not further decrease, but continue to oscillate if the resonant period is not interrupted. Therefore, the resonant capacitor C_{r1} would begin to charge in the opposite direction (dashed line), leading to even higher switching losses than in the investigated case where the resonant period is interrupted at the minimum possible voltage at the end of the dead time. This approach therefore cannot overcome the incomplete ZVS problem.

(b) Decreasing the resonant inductance L_r

As previously analyzed in [3], choosing an appropriate value of L_r can minimize the total conduction losses of the auxiliary circuit. Equation (20) shows that a reduction in the resonant inductance causes the minimum allowed overlapping time to decrease further, but simultaneously increases conduction losses of the auxiliary circuit. Consequently, this requires more robust components for the auxiliary circuit, likely increasing their size.
In other words, the advantages of ZVS can only be fully realized for unbalanced input voltage operation when the resonant inductance properly decreases, at the cost of increased conduction losses.

From these investigations, it can be concluded that the best solution to achieve true ZVS commutation is to increase the overlapping time t_{ovp2} to values larger than t_{ovp2_min}, with a suitable safety margin to account for component tolerances etc.

In addition, it can be clearly seen that the imbalances in the input supply voltages have a significant influence on the commutation timing and consequently on the inverter performance in terms of efficiency. Therefore, both input supply voltages should be monitored for each switching cycle in addition to the load current. Depending on these acquired data, the timing of the output signals have to be calculated accordingly to achieve true ZVS commutation.

Conclusion

Effects of imbalances in the supply voltage of the ARCP inverter based on the variable timing control have been explored in this paper. The major conclusion is that the imbalances in the DC input voltage can significantly affect the performance of an ARCP inverter and have a large influence on the timing control of the ARCPI to achieve ZVS.

Therefore, the DC input voltage sources should be monitored, and applied to the variable timing control of the ARCPI on a cycle-by-cycle basis. Due to these imbalances, a minimum overlapping time must be observed to ensure soft switching. It was shown that simulation results have good agreement with the results of the theoretical analysis and they reconfirm the presented theoretical analysis.

An optimized design method of the ARCPI should be investigated in the future, which takes into account the imbalances in input supply voltage and its effect on the selection and dimensioning of the relevant component.

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