Experimental Comparison of FPGA-Implemented Model Predictive Voltage Control to Cascaded Proportional Resonant Control for a Three-Phase Four-Wire Three-Level Grid-Forming Inverter of 250 kVA

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Keywords

Abstract

Modern microgrid systems require inverters capable of forming an acceptable grid voltage, during islanded operation, both supplying and absorbing power, through unbalanced load conditions and transients. In order to address this concern, the steady state and transient performance of two control methods are compared which are both capable to supply unbalanced three-phase loads. The first method is a cascaded proportional resonant (PR) control, which is a state-of-the-art controller for single-phase-capable voltage-source inverters but suffers from lower performance in transient conditions. The second method is a new field-programmable gate array (FPGA)-implemented finite control set model-based predictive control (FCS-MPC) which shows high performance for transients as well as black-start capability. Experimental results show the model-based predictive controller (MPC) to have better steady-state performance, with an average total-harmonic-distortion (THD) over the entire steady-state operation range of 1.4 % vs. 2.2 % for the PR controller, and a voltage regulation error of 0.71 % for the MPC vs. 1.1 % for the PR controller over the entire operating range. The MPC also shows advantages over the PR controller during transient response conditions, enabling settling times within 600 µs vs. 100 ms of the PR controller.

1   Background

In the expansion of renewable electrical power systems with inverter-based generation systems, the ratio of inertia-based generation is decreasing. This places greater responsibility on the performance of both grid-supporting and grid-forming inverter control systems, especially in islanded conditions. Under islanded conditions, inverters are required to respond faster to maintain acceptable voltage conditions despite the presence of unbalanced loads or transient events.

As the technology of power electronic devices advances, the switching frequencies of inverters increases. This results in shorter control cycles for grid-connected inverters and, therefore, allowing better controller performance in grid-related applications. However, devices of power rating in the 100 kW range and above are still operating at switching frequencies of about 1 kHz or even at some 100 Hz. Hence, the control for these devices is limited in bandwidth [1]. This presents challenges for the modern power system, where increasing controller bandwidth is important to avoid controller-controller interactions. As computational performance increases, it does not necessarily benefit these larger power devices.

At the moment, a state-of-the-art industrial controller for the control of voltage sourcing inverters is the PR controller. This single-phase-capable controller allows for the control of voltage-source inverters in the presence of imbalances and other non-ideal conditions. However, the nature of PR control, to operate on the average-voltage model, means that the transient performance of control is limited. In practical applications the control can only act upon the analog-to-digital converter (ADC) sample representing the average value (say in the middle of sampling interval, which may be inconsistent with multi-level converters) and must calculate the appropriate action before the next pulse width modulation (PWM) update.

The MPC, presented in [2], however, is not dependent on any controller states and hence acts only upon the most recent sample of measured values and produces a reaction immediately. This places a greater emphasis on the processing requirements, described in [3], as a valid control decision should be computed as quickly as possible. The implementation of the finite control set model-based predictive control (FCS-MPC), however, lends itself to the parallel operation of modern FPGA processors.

Fig. 1: Test hardware: two back-to-back 250 kVA inverters

Max. power	250 kVA per device
Topology	3-level NPC
Filter inductance	70 μH
Filter capacitance	250 μF
Control hardware	dSPACE DS6001, DS6601

Table I: Technical specifications of test hardware

This investigation focuses on the control of a single custom 250 kVA voltage-source inverter shown in Fig. 1. It is controlled via a combination of FPGA and CPU dSPACE SCALEXIO rapid control prototyping system. One rack system consists of two back-to-back 250 kVA 3-level neutral-point-clamped (NPC) insulated gate bipolar transistor (IGBT) converters, where one is operated as the voltage forming inverter under test and one is operated as an AC-load. Each converter is equipped with a configurable filter, where the IGBT network output of the grid forming source connects to a LC filter and the load side to a L filter. An overview of the experimental setup is shown in Fig. 2.
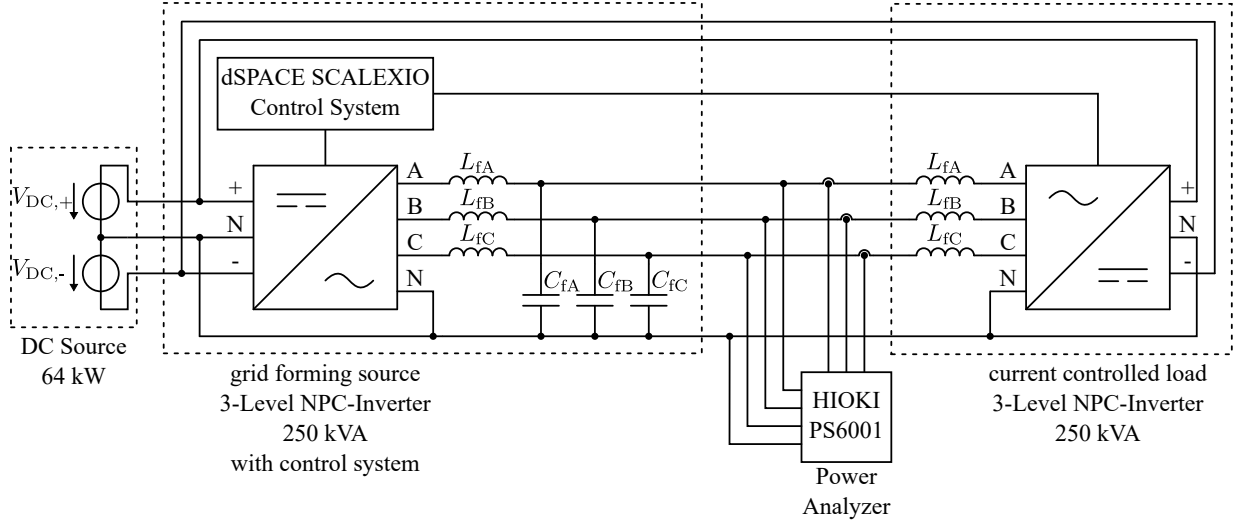
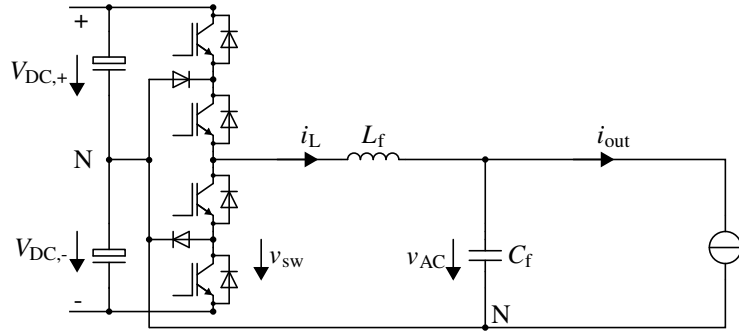Fig. 2: Experimental setup used for the performance evaluation

Fig. 3: Single-phase circuit diagram, indicating the used measurements and states

2 Plant model and control

The control objective for both considered controllers is the correct regulation of the symmetrical three phase, four wire (three phases and neutral) voltages, with minimal distortion, under a set of steady-state and transient conditions. Further constraints on the control is the limitation of the IGBT currents to protect the system, and avoid exceeding any protection limits. Since the LC filter is connected via the external neutral line, the analysis is performed in the per-phase representation. The LC network is shown in Fig. 3, where i_L is the inductor current and v_{AC} the capacitor voltage of the output filter. v_{SW} describes the output voltage of the IGBT network and i_{out} is the load current. The dynamics of the LC network are described as follows:

$$
\begin{aligned}
\frac{\mathrm{d}}{\mathrm{dt}} \begin{pmatrix} i_L \\ v_{AC} \end{pmatrix} &= \begin{pmatrix} 0 & -\frac{1}{L_f} \\ \frac{1}{C_f} & 0 \end{pmatrix} \begin{pmatrix} i_L \\ v_{AC} \end{pmatrix} + \begin{pmatrix} \frac{1}{L_f} \\ 0 \end{pmatrix} (v_{SW}) + \begin{pmatrix} 0 \\ -\frac{1}{C_f} \end{pmatrix} (i_{out}), \\
\frac{\mathrm{d}}{\mathrm{dt}} \boldsymbol{x} &= \boldsymbol{A}\boldsymbol{x} + \boldsymbol{B}\boldsymbol{u} + \boldsymbol{E}\boldsymbol{w}, \\
\boldsymbol{y} &= \boldsymbol{I}_2 \boldsymbol{x} = \boldsymbol{C}\boldsymbol{x},
\end{aligned}
\tag{1}
$$

where $\boldsymbol{I}_2$ is a 2x2 identity matrix.

2.1 Proportional resonant control

In this approach, a cascaded control modelling (Fig. 4) was implemented, with a voltage controller G_{PR}^v and a subordinated current controller G_{PR}^i. In comparison of control strategies for grid-connected converters, linear proportional-integral (PI) controllers in the stationary frame have the disadvantage of a remaining steady-state error. As the control has to cope not only with symmetrical three-phase loads, the common control in a rotating dq-frame is also not suitable. Instead, three single-phase controls are implemented, each with a resonant controller action in the voltage controller as well as the current controller with the base frequency ω_0 in order to be able to track a sinusoidal reference without a steady-state error [4].

	Current controller G_{PR}^i	Voltage controller G_{PR}^v
K	$0.001 \frac{1}{\mathrm{A}}$	$0.452 \frac{\mathrm{A}}{\mathrm{V}}$
K_{R0}	500000	500000
ω_0	$314.159 \frac{\mathrm{rad}}{\mathrm{s}}$	$314.159 \frac{\mathrm{rad}}{\mathrm{s}}$
d_0	$5 \cdot 10^{-6}$	$1 \cdot 10^{-6}$
K_{R1}	10000	15000
ω_1	$942.478 \frac{\mathrm{rad}}{\mathrm{s}}$	$942.478 \frac{\mathrm{rad}}{\mathrm{s}}$
d_1	$10 \cdot 10^{-6}$	$2 \cdot 10^{-6}$
ω_{I}	$62.832 \frac{\mathrm{rad}}{\mathrm{s}}$	0

Table II: Proportional resonant controller parameters

The measurements of the average inductor currents of the inverter by Regular Sampling approach delivered unconvincing results. The necessary interlock between the semiconductors combined with rather complex commutation processes of a 3-level neutral-point-clamped topology and a relatively small inductor led to high measurement errors. Instead, the currents were sampled 500 times per switching period and from the results, the average value of the previous switching period was calculated. That caused an additional delay in the current control loop which had to be compensated by a discrete-time prediction model based on (1) using the matrix-exponential method, in order to avoid stability problems.
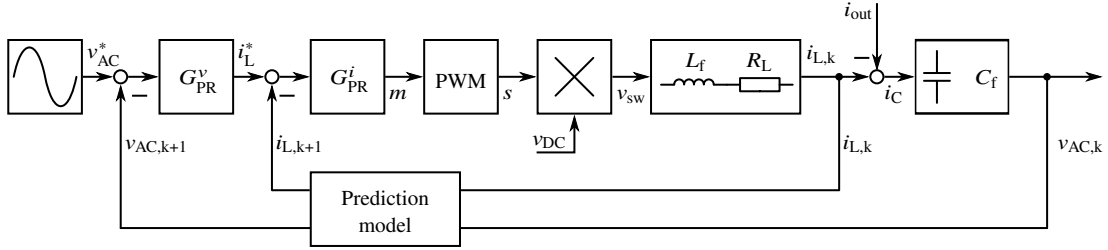

Fig. 4: Cascaded proportional resonant control modelling

It is shown in [5] that the PR controller in the stationary frame can be derived by transforming two separate PI-controllers from the positive and negative sequence frames. The infinite gain at the base frequency ω_0 can lead to stability problems in the practical implementation, because small control errors could cause saturation of the controller output. Therefore it is helpful to use a non-ideal integrator with the damping factor d. In a four-wire-system, 3rd harmonics can easily show up, therefore a second resonant term with three times the base frequency was added. Furthermore, to achieve better accuracy for controlling DC-offsets, an integral term was added to the controller, which is only active in the current controller. The plant transfer function of the current control loop does not show integrating behaviour over the complete frequency range. The corner frequency resulting from the gain factor K and the integral part, functionally similar to a PI-controller, was set to the corner frequency of the inductor with its series resistance to cancel out the pole of the low-pass and achieve setpoint tracking for low frequencies. The plant transfer function of the voltage control loop shows integrating behaviour for the full frequency range, hence an additional integrator is not needed. The resulting transfer function for the proposed proportional resonant controller is

$$G_{\mathrm{PR}}(s) = K \left(1 + \frac{2K_{\mathrm{R1}} d_0 \omega_0 s}{s^2 + 2d_0 \omega_0 s + \omega_0^2} + \frac{2K_{\mathrm{R2}} d_1 \omega_1 s}{s^2 + 2d_1 \omega_1 s + \omega_1^2} + \frac{\omega_{\mathrm{I}}}{s} \right) \tag{2}$$

under the condition $d_i \ll 1$ and combined with a gain factor $K_{\mathrm{R}i}$.

The discrete-time implementation of (2) similar to the described solution in [6] is

$$G_{\mathrm{PR}}(z) = K \left(1 + \frac{b_{2,0} z^2 + b_{1,0} z + b_{0,0}}{a_{2,0} z^2 + a_{1,0} z + a_{0,0}} + \frac{b_{2,1} z^2 + b_{1,1} z + b_{0,1}}{a_{2,1} z^2 + a_{1,1} z + a_{0,1}} + \frac{\omega_{\mathrm{I}} T_s z}{z - 1} \right) \tag{3}$$

with the coefficients of Tab. III.

	First resonance term	Second resonance term
	$\omega_0 = 2\pi\cdot 50\,\frac{\text{rad}}{\text{s}}$	$\omega_1 = 2\pi\cdot 150\,\frac{\text{rad}}{\text{s}}$
a_0	$T_s^2\omega_0^2 - 4\omega_0 d_0 T_s + 4$	$T_s^2\omega_1^2 - 4\omega_1 d_1 T_s + 4$
a_1	$2T_s^2\omega_0^2 - 8$	$2T_s^2\omega_1^2 - 8$
a_2	$T_s^2\omega_0^2 + 4\omega_0 d_0 T_s + 4$	$T_s^2\omega_1^2 + 4\omega_1 d_1 T_s + 4$
b_0	$-4K_{R0}T_s\omega_0 d_0$	$-4K_{R1}T_s\omega_1 d_1$
b_1	0	0
b_2	$-b_0$	$-b_0$

Table III: Proportional resonant controller coefficients
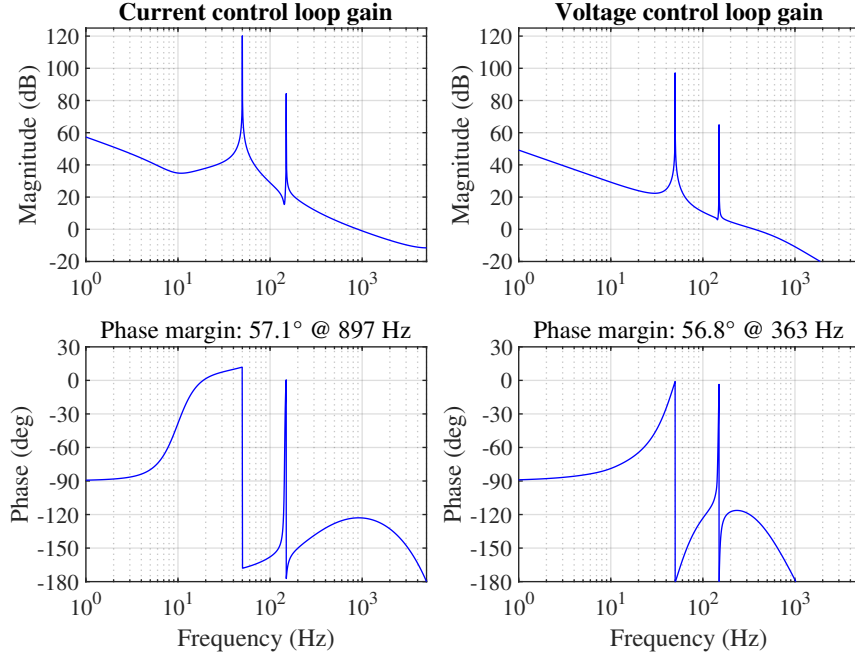

Fig. 5: Open-loop gain of the current- and voltage control loops for the PR approach

The Bode plots of the open-loop transfer functions for the discrete-time models are shown in Fig. 5 with the parameters listed in Tab. II. The control design objective is a gain for the first resonance term as high as possible with a phase margin of at least 50° for both voltage- and current-controllers. The specific controller parameters from Tab. II have been optimized by manual tuning.

2.2 MPC approach

The MPC used is an adaptation of the MPC introduced in [2], illustrated in Fig. 6. Here, the implemented MPC is geared towards the control of the capacitor voltage while limiting the IGBT current. The MPC uses the per-phase model of the LC filter to determine the predicted states. The model is discretized using the matrix-exponential method, and v_{sw} is evaluated for all 3 possible switch states $[V_{DC+}; 0; -V_{DC-}]$, providing 3 predictions per phase. The prediction is then repeated to obtain the x_{k+2} prediction, resulting in 9 predictions per phase. The error function is:

$$J\left(x_{k+1}\right) \quad = \quad \left(v_c^* - v_{c,k+1}\right)^2 + f_{oc}\left(i_{l,k+1}, i_{\lim}\right)$$

where,

$$f_{oc}\left(i_{l,k+1}, i_{\lim}\right) \quad = \quad \begin{cases} k_{i,\lim}\left(i_{l,k+1} - i_{\lim}\right)^2 & \text{if } \left|i_{l,k+1}\right| > i_{\lim} \\ 0 & \text{otherwise.} \end{cases}$$

(4)

and $i_{\lim}$ is the maximum allowed instantaneous current value. The weighting term for the over-current term, $k_{i,\lim}$ was arbitrarily set to a value of 10A^{-2}. The current limit is implemented as a soft-constraint, to enable continuous operation during over-current conditions, allowing the controller to choose an output state that minimises the
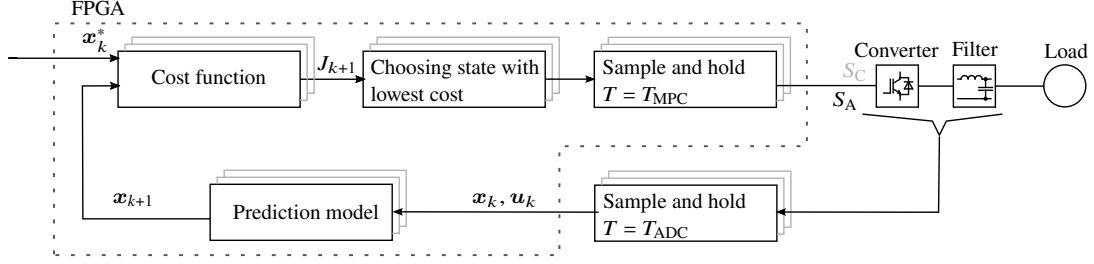
Fig. 6: Principle of FPGA implemented MPC operation

over-current condition.

The switch selection, which produces the lowest error function result, is then selected every T_{MPC}. This switch state is then applied until the next evaluation, T_{MPC} later. For an average effective switching frequency of approximately 10 kHz, T_{MPC} was set to 21 µs. This is significantly slower than the ADC sample time of $T_{\mathrm{ADC}} = 200$ ns.

The entirety of the control logic was implemented in the FPGA (dSPACE DS6601) interfaced with multi-I/O modules (dSPACE DS6651). The controller current limit, i_{lim}, was set to 600 A, to limit operation outside of the nominal operating region.

3 Experimental comparison results

The two controllers are compared for a limited number of steady-state and transient performance conditions. There are several similarities and differences in the operation principle, as well as the implementation of the two controller approaches shown in Tab. IV.

3.1 Metrics

The RMS and THD calculations are performed independantly of the control systems, by a HIOKI power analyzer. The RMS calculation is

$$V_{\mathrm{RMS}} = \sqrt{\frac{1}{M} \sum_{k=0}^{M-1} \left(v\left(k\right) \right)^2} \tag{5}$$

where M is the number of samples ($v(k)$) taken within a period of the voltage. Absolute voltage regulation error is calculated as

$$V_{\mathrm{RMS,Err}} = \left| \frac{V_{\mathrm{RMS}} - V_{\mathrm{nom}}}{V_{\mathrm{nom}}} \right| \tag{6}$$

where V_{nom} is the nominal voltage setpoint. The THD is calculated

$$THD_{v_{\mathrm{AC}}} = \frac{\sqrt{\sum_{k=2}^{K} \left(u_k \right)^2}}{u_1} * 100\%. \tag{7}$$

Here, K is the number of harmonics (u_k) used for the harmonic calculation. Harmonic orders are referenced from the fundamental component (u_1). For the measurements performed $K = 50$, with harmonic measurements complying to the IEC 61000-4-7:2002 standard.

3.2 Steady-state performance

One comparison of the two controller structures is their behaviour across a range of load conditions. To demonstrate this, the controllers were operated with constant set-point voltages (three-phase, 230 V RMS per phase) and loaded by a balanced current source across the operating range of the device (0 kVA to 250 kVA) for a full rotation of the phase angle. The results shown in Fig. 7 uses the data obtained from the HIOKI PW6001 power analyzer, connected as shown in Fig. 2.

Both controllers show acceptable steady-state performance, seen in Fig. 7 over the entire test region, with a maximum THD of 2.5% with a maximum voltage regulation error of 3%. This harmonic content performance

	PR control	FCS-MPC
Computing hardware	CPU	FPGA
Switching frequency	10 kHz (fixed)	Appr. 10 kHz (variable)
Control cycle time	100 µs	21 µs
Computation time	12 µs	320 ns
Sampling concept	Oversampling with averaging	Single measurement of most recent sample
Manipulated variable	Modulation index for PWM	Finite switching vector

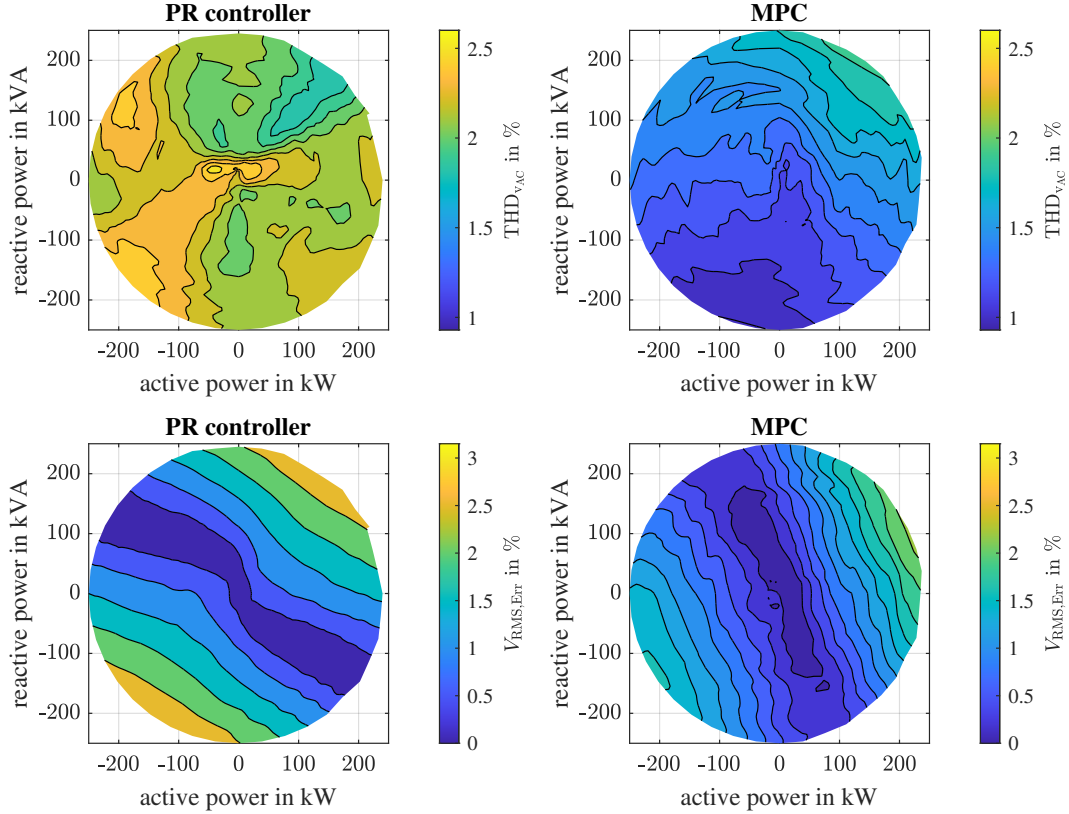Table IV: Comparison of the FCS-MPC and the PR control approach

Fig. 7: Three-phase load voltage total harmonic distortion and absolute RMS voltage error

is well below the IEEE STD 519-2014 requirements of a maximum 5% THD. Voltage regulation is also for both controllers within the ±10% requirements for most voltage source applications (IEC 64020-3 for example). The voltage regulation of both controllers is heavily dependant on the model parameters used (both controllers used the ideal parameters of Tab. I). However, when the average performance over the entire range is averaged and compared in Tab. V, it is clear, by the metrics provided that the FCS-MPC performs better under steady-state conditions.

3.3 Dynamic response

In order to compare the dynamic response of both controllers their performance is demonstrated through two different high dynamic test conditions; a black start condition (the establishment of the three-phase voltages after all three-phase voltages have reached 0 V) and a load step. These represent some of the more demanding test cases for a voltage forming inverter in the field. The results shown are from the measurements using the sensors and processing units on the device.

	PR control	FCS-MPC
mean $(\mathrm{THD}_{V_{AC}})$	2.2%	1.4%
mean $(V_{\mathrm{RMS,Err}})$	1.1%	0.71%

Table V: Steady-state performance result comparison

3.3.1 Black-start

In order to reduce the initial currents into the filter capacitors, the voltage per phase reference to the controllers was only initiated from the internal voltage reference zero crossing point. From there on the voltage reference, for both controllers, was set to the nominal 230 V at 50 Hz. The results of the test, both voltage and currents are shown in Fig. 8.

The results show, as expected the MPC has stabilized the voltage to the setpoint within a few microseconds of the setpoint being non-zero. The PR controller, due to the resonant term of the controller and the delays of the cascaded controller design, requires approximately 80 ms before settling to the steady-state condition. It is noted that the more rapid control of the voltage does result in higher inductor current ripple for the MPC approach, resulting in higher filter capacitor currents (approx. 30 % higher compared to the PR approach).
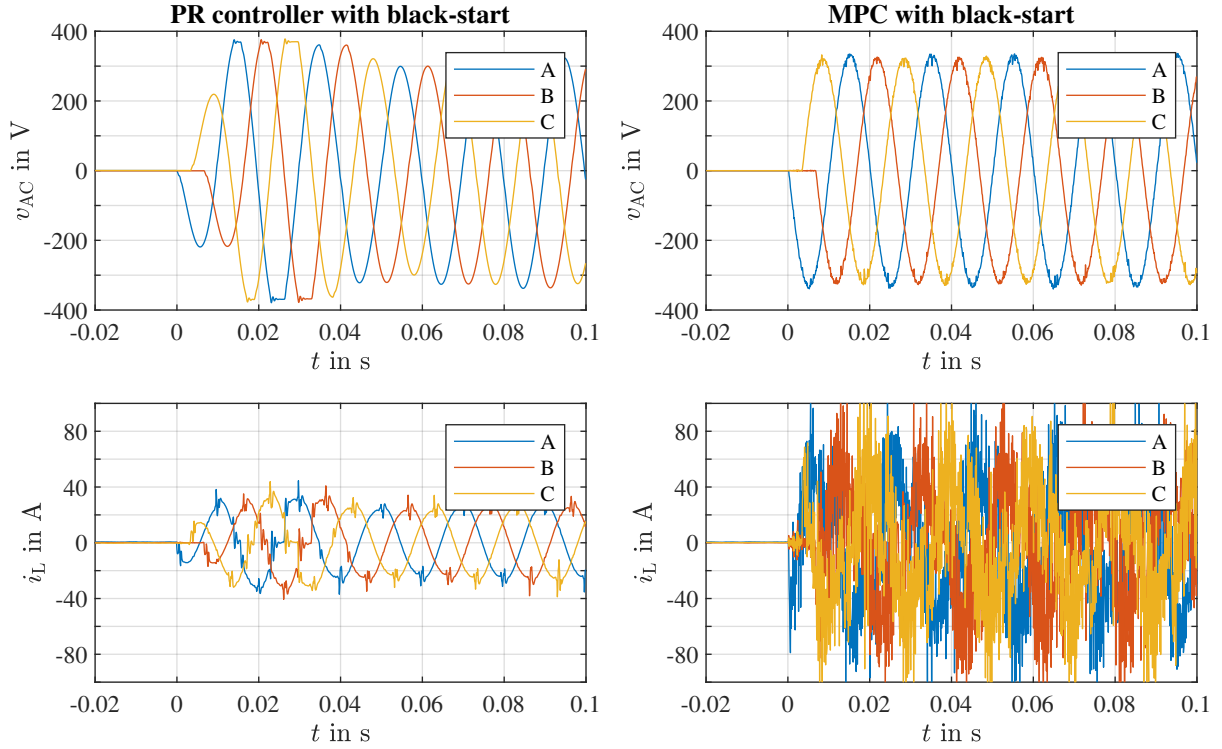

Fig. 8: Capacitor voltage v_{AC} and inductor currents i_{L} during black-start with no load connected

3.3.2 Load step

In order to demonstrate a load step, a load with a power factor of 1.0 was changed from a nominal load of 25 % (63 kW) to 75 % (188 kW). The load was provided with the phase angle information from the voltage controllers and approximates an ideal current source. The results of the load step test are shown in Fig. 9.

During the load step, the PR controller recovers from the load step within approximately 100 ms, including an overshoot of the output voltage, which was limited by the DC bus voltage of the converter during the experiment. In comparison the MPC shows a minor dip in the output voltage, lasting 600 µs. The duration of this dip was extended due to the inductor current limit (600 A). It is again noted that the MPC technique does result in higher inductor current ripple.

4 Conclusion and outlook

Experimental tests were conducted on an experimental three-phase four-wire three-level 250 kVA inverter to compare the behaviour of a voltage forming PR controller to a voltage forming FCS-MPC. The PR controller was designed and implemented with oversampling and averaging using fixed time windows of 100 µs fitting the PR controller cycle time to control a standard PWM modulation index. The FCS-MPC, however, utilized the FPGA to implement the algorithm which held a single switch state for a fixed period of time. The steady-state performance of the two controllers is similar with both controllers meeting standard performance metrics. However, the MPC provided a lower voltage THD and better voltage regulation across the entire tested operational range at the expense of higher capacitor currents. During transient tests, a black-start test and a load-step, the MPC reached
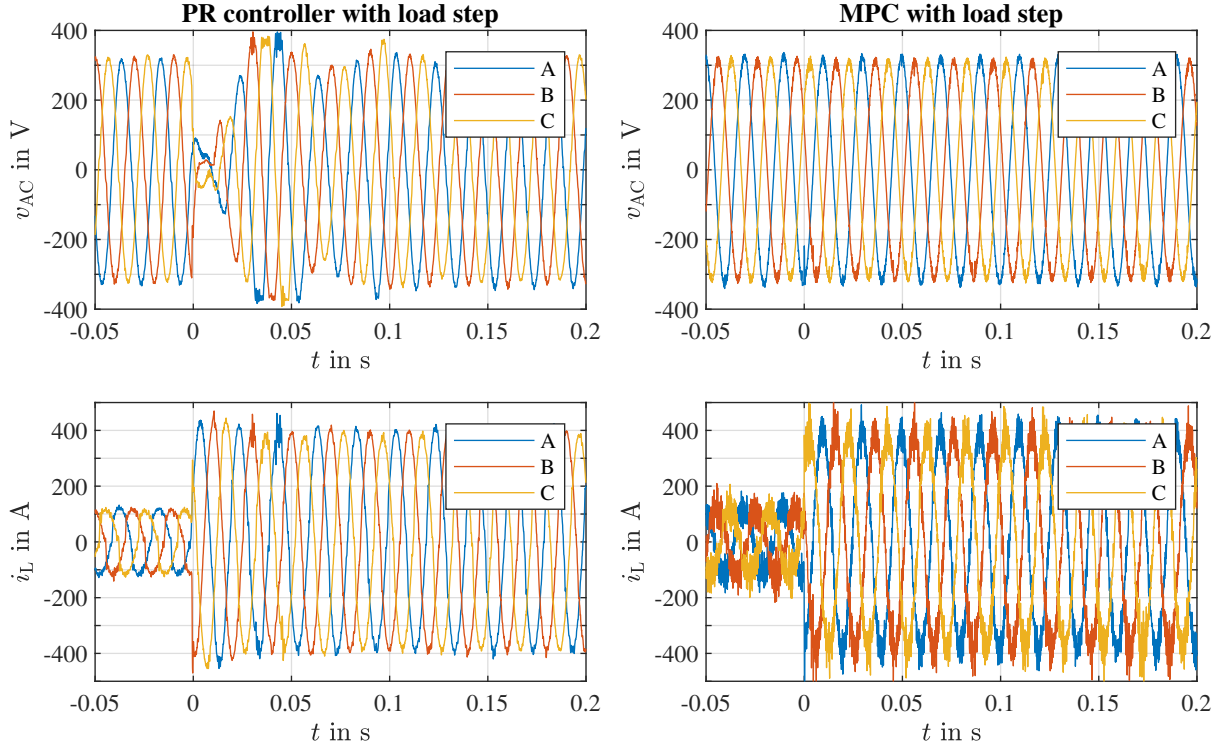
Fig. 9: Capacitor voltage v_{AC} and inductor currents i_L during load step of both controllers from 25 % to 75 % (of rated 360 A capacity, with a power factor of 1)

a stable steady-state condition within 600 µs compared to the 100 ms response time needed by the PR to stabilize. Further investigations into the MPC controller include removing the time gating logic (T_{MPC}) to utilize the available FPGA architecture with the intention of improving dynamic performance. Comparisons against other controller architectures are also required.

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