Implementation of onsite Junction Temperature Estimation for a SiC MOSFET Module for Condition Monitoring

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Keywords

«Junction Temperature Estimation», «Reliability», «Condition Monitoring», «SiC MOSFET, « $R_{ds,\mathrm{on}}$ ».

Abstract

This paper presents an advanced methodology for mapping junction temperature (T_j) based on the drain to source resistance ($R_{ds,\mathrm{on}}$) of a SiC MOSFET module to monitor the power electronics converter health condition. Capturing real-time measurement of on-state drain-source voltage ($V_{ds,on}$), drain-source current ($I_{ds,on}$) and baseplate temperature, and taking advantage of a fast edge computing device, a significant correlation can be established between T_j and $R_{ds,\mathrm{on}}$. Due to having a linear correlation and simple circuity in comparison to other junction temperature estimation methods, e.g., the internal gate resistance method (R_{Gint}), gate threshold voltage method ($V_{g,th}$) and short-circuit current method (I_{sc}), the output results of the proposed paper can be effortlessly implemented in a simple microcontroller that can monitor the health condition of a SiC MOSFET module in terms of bond wire fatigue and metallization reconstruction. To validate the proposed method, a synchronous boost converter is prototyped and tested. The experimental results depict the effectiveness of the proposed method.

Introduction

Nowadays, Power Electronic Converters (PECs) are utilized to efficiently convert electrical energy between power generators, storage systems, and power consumers. The power electronics industry comes across a growing appeal for cost reduction, increasing density, upgrading their products fast and continuously, and reducing time to market, which has brought severe reliability challenges that should be addressed. Field data shows that the PECs in some applications like renewable energy is considered one of the primary causes of malfunctions with the contribution of 13% to the overall failure rate, while in the PECs, semiconductor devices are the most failure-prone devices which are responsible for an overall 31% of failures in power electronics converters [1]-[2]. Thus, it is required to identify stress factors in power electronics devices. One of these factors is junction temperature (T_j) and junction temperature swing (ΔT_j), which are associated with wear-out and solder fatigue of the semiconductor module and can be measured onsite. Using real-time methods, junction temperature can be converted to the parameter that can predict the end of life (EOL) and also be the basis for derating estimation.

Regarding derating, it is worth mentioning that it will be fruitful to manage the processed power or speed up the cooling process if the module is experiencing abnormal temperature through a condition monitoring routine. Therefore, implementing condition monitoring systems via appropriate thermal management can enhance the lifetime of semiconductor modules [2].
In order to benefit from thermal management and condition monitoring, it is necessary to estimate onsite junction temperature. So far, several approaches have been proposed in the literature to estimate junction temperature [3]-[7]. The first one is implementing temperature sensors directly in module packages. In this method, a negative temperature coefficient sensor (NTC) or a p-n diode is implemented on the die or direct bonded copper (DBC) in the module and thus can estimate junction temperature [3]. The NTC temperature sensor can measure junction temperature several millimeters away from the die; thus, the thermal model is needed for junction temperature estimation. Also, junction temperature can be measured via a p-n diode built on the die which its instantaneous forward voltage changes according to temperature variations. On the other hand, temperature measurement by means of NTC and the p-n diode will not be highly accurate and fast. Also, most semiconductor modules lack integrated temperature sensors which worsens the situation.
Temperature-sensitive electrical parameters (TSEP) such as the internal gate resistance method (R_{Gint}), gate threshold voltage ($V_{g,th}$), short-circuit current (I_{sc}), turn-OFF transition time, and turn-ON delay are indirect temperature measurement methods with appropriate time resolution. Internal gate resistances in MOSFET and IGBT modules depend on junction temperature variations. A variation on this resistor can be calculated by applying test pulse currents with delay to switching pulses. However, a specially modified substrate is required to measure this resistance [4]-[5].
To benefit temperature estimation via measuring change in the gate threshold voltage, it is necessary to sense the $V_{g,th}$ in a short time interval, which requires high-speed data acquisition [6]. In the short circuit approach, the corresponding elements like auxiliary switches should be added to the converter for performing any short circuit tests for junction temperature estimation. It is necessary to ensure only considered device-under-test (i.e., MOSFET) are subjected to short circuit tests. Also, precise protection circuits are needed to guarantee that short circuit current will not pass safety limitations, limiting the applicability of this approach [7]. Turn-OFF transition time and turn-ON delay also are used for junction temperature estimation; however, it should be mentioned they need sensitive and accurate measurement circuits which cannot be easily implemented [8]. Also, system-level approaches like identification of change of low-order harmonics in the output of a voltage source inverter are used for junction temperature estimation, which is out of the scope of this paper [9]. The temperature within semiconductors can also be estimated using optical methods via measuring stimulated, naturally emitted, and reflected radiation, which has been explained in [10].
To fulfill the above-mentioned research gap, this paper focuses on an advanced method for junction temperature estimation and validates it experimentally. In this approach, as shown in Fig. 1, by heating up heatsink temperature and turning-ON semiconductor for a short duration and sensing drain-source voltage ($v_{ds,\mathrm{on}}$) and drain-source current ($i_{ds,\mathrm{on}}$), drain-source resistance ($R_{ds,\mathrm{on}}$) can be mapped onto junction temperature. The rest of the paper discusses the proposed test bench preparation, calibration approach, and characterizing tests of a SiC MOSFET module. Then, experimental results are presented, followed by the conclusion in the last section.

Measurement circuit (Sensorics)

The schematic of the analog circuit used for measuring $v_{ds,\mathrm{on}}$, $i_{ds,\mathrm{on}}$ and $R_{ds,\mathrm{on}}$ is shown in Fig. 2. The sensorics comprise a PTC sensor and its amplifier, Current Transducer (LA 55-P/SP23) and its amplifiers, and several op-amps in different combinations for sensing ON-state drain-source voltage and blocking OFF-state voltage. The outputs of the sensorics are connected to a Microcontroller with 12-bit ADC. The other topologies for sensing on-state voltage of semiconductor modules have been discussed in [11]-[14].

Test Bench Preparation and Calibration for Mapping Routine

A synchronous boost converter is prototyped to verify the proposed approach using a SiC half-bridge MOSFET module (CAS120M12BM2) mounted on a temperature-controlled heatsink. For heating up the heatsink, six parallel heating resistors (450Ω, 150 W) are connected to the heatsink, and one positive

temperature coefficient (PTC) sensor is pasted on the heatsink close to the module to measure baseplate temperature. The junction temperature of the MOSFET module is considered equal to the baseplate temperature measured by the PTC sensor because of generating a short ON time signal (i.e., 100 ms) from 2 A to 10A with 1 A slope and utilizes natural air circulation for cooling the MOSFET module. As Fig. 1 shows, to start calibration, first, the temperature of the baseplate is increased up to a higher temperature (i.e., 80 ºC), and then the control circuit pauses heating the heatsink and starts generating turn-ON pulses. There is a 200ms delay between each pulse to guarantee that any residual temperature perturbation has been eliminated [8].

Meanwhile, using current and voltage sensors and a 12-ADC unit, the microcontroller is able to measure $v_{ds,\text{on}}$ and $i_{ds,\text{on}}$ and thus can calculate $R_{ds,\text{on}}$. Also, using a PTC thermocouple, the microcontroller can measure baseplate temperature in each interval. It is worth mentioning that switching pulses are generated when baseplate temperature decreases by 5 ºC, and the process continues until the baseplate temperature becomes equal to room temperature (25ºC). Finally, a 3-D map to estimate $R_{ds,on}$ is generated based on extracted data.

Condition Monitoring

After completing the above-mentioned commissioning test, a 3-D $R_{ds,\text{on}}$ map is calculated, and thus it is programmed in edge, fog and cloud devices. In the actual operational condition, by sensing ON-state drain-source current and voltage and hence calculation of drain-source resistance of the MOSFET and also feeding edge/fog/cloud device on drain-source resistance and drain-source current and using implemented 3-D $R_{ds,\text{on}}$ map, the junction temperature is estimated. T_j data are valuable for thermal and lifetime control techniques like derating and increasing cooling effort.

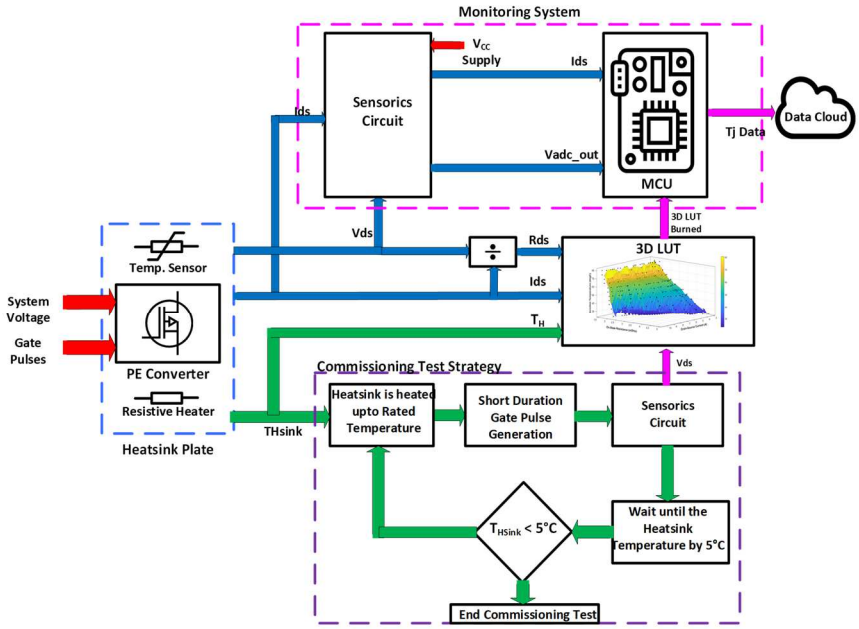


Fig. 1. Commissioning and junction temperature estimation algorithm.

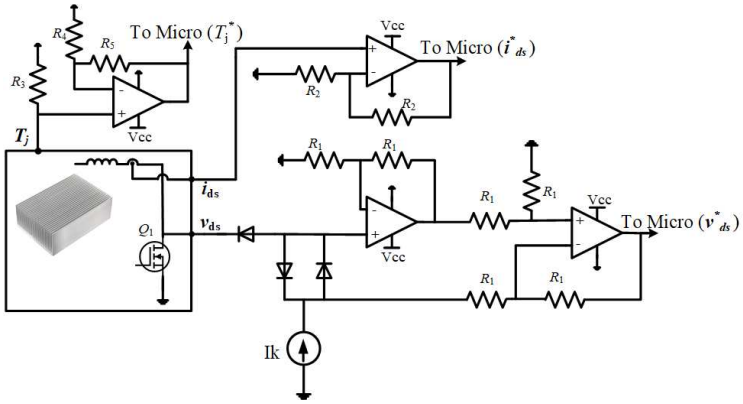


Fig. 2. Sensorics schematic of the T_j estimation.

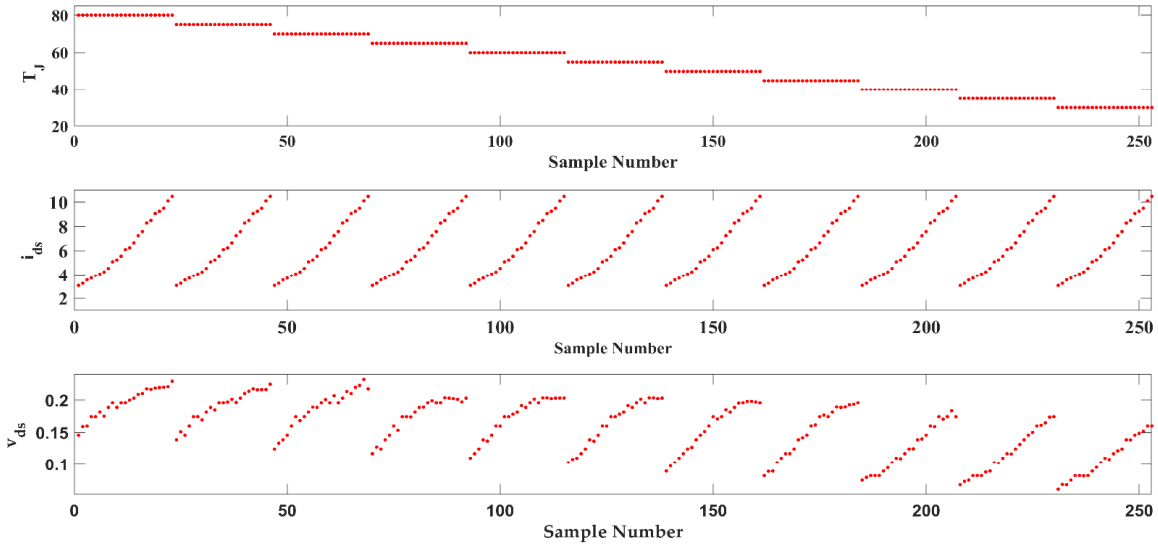
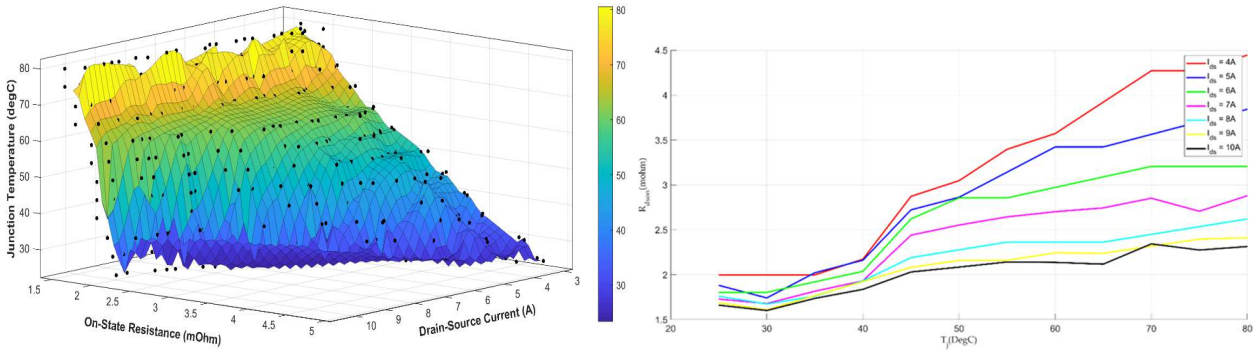


Fig. 3. Data collected during the commissioning test. From top to bottom: Junction temperature, drain-source current and drain-source voltage.



(a) (b)

Fig. 4. Look-up tables gained via commissioning test (a) 3-D Look-up table, (b) 2-D Look-up table

Results and Discussion

After conducting commissioning tests, the results are reported in the form of T_j, $R_{ds,\text{on}}$ and $v_{ds,\text{on}}$. As Fig. 3 shows, the results are collected whenever junction temperature decreases by 5 ºC until the temperature reaches 25 ºC. Also, Fig. 4 represents 3-D and 2-D look-up tables of a SiC MOSFET module from calibration tests for current below 10A, respectively. These look-up tables have the capability of being mapped to the microcontroller for use as a junction temperature estimation tool for condition monitoring purposes. In Fig. 4(a), the x-axis is T_j, while y-axis is $i_{ds,\text{on}}$ and z-axis is $R_{ds,\text{on}}$. Also, Fig. 5 illustrates the gate pulses (V_{gs}) generated by the dSPACE unit and drain-source current ($i_{ds,\text{on}}$) measured by Agilent current probe (1146B). During the test, the time interval between pulses is kept at about 200ms. The experimental test setup is illustrated in Fig. 6. In addition, the results are interpolated using the polynomial function, which is shown as Equation (1)

$$T_j(i_{ds}, R_{dson}) = p_{00} + p_{10}i_{ds} + p_{01}R_{dson} + p_{20}i_{ds}^2 + p_{11}i_{ds}R_{dson} + p_{02}R_{dson}^2 + p_{30}i_{ds}^3 + p_{21}R_{dson}i_{ds}^2 + p_{12}i_{ds}R_{dson}^2 \quad (1)$$

where, $p00 = 369,\ p10 = -98.56,\ p01 = -176.5,\ p20 = 8.603,\ p11 = 53.56,\ p02 = 20.36,\ p30 = -0.1636,\ p21 = -3.069,\ p12 = -5.436.$

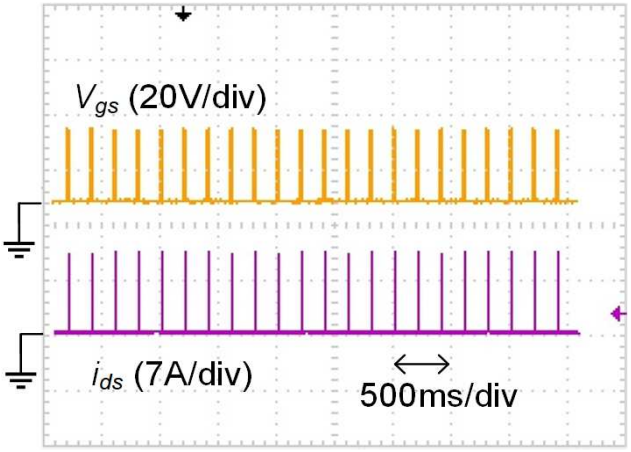


Fig. 5 Gate signals and drain-source current waveform

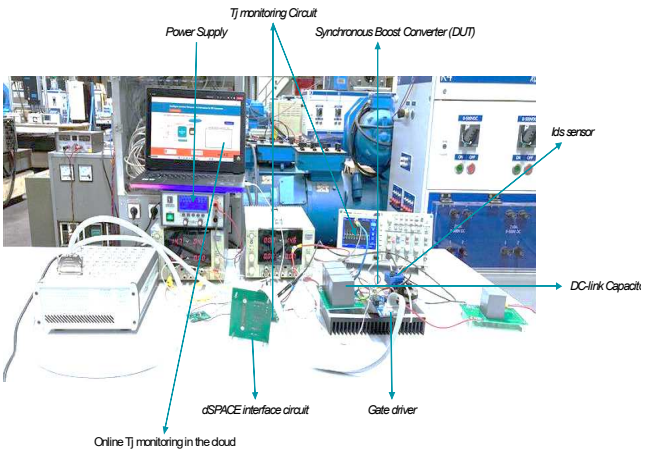


Fig. 6 Test set up

The proposed methods have some advantages and disadvantages as follows. Also, in Table 1, a comparison between some parameters used for junction temperature estimation is presented.

- This method does not require any especial equipment like a semiconductor parameter analyzer and can be performed on a power electronics converter, and implementation of the circuity is not costly in comparison with converter implementation. Also, discrepancies between modules manufactured by the same company will not affect the test process.
- There is no need for any thermocouple sensor inside the SiC MOSFET module.
- Temperature can be estimated very fast. Also, results can be easily implemented in a Microcontroller.
- The temperature estimation process does not influence the normal operation of the PECs.
- But due to semiconductor degradation, the test should be conducted for continuous accurate temperature estimation after receiving each level of degradation [11].
- Variation in gate threshold voltage might influence the test, which should be investigated [6],[11].
- Last but not least, this method gives information about average temperature and cannot identify hotspots on the chip [10].

Table 1. Comparison between different TSEPs [14]-[15]

TSEP	Online	Sensitivity	Effect On Converter	Linearity	Integrability	Complexity
$V_{ce,on}$	Yes	± (2-3) mV/°C	Yes	Good	Yes	Less
R_{Gint}	Yes	(1-3) mΩ/°C	No	Good	Yes	High
I_{sat}	Yes	-	No	Exponential	No	High
I_{sc}	Yes	17% of $I_{sc,max}$/°C	Yes	Good	No	High
$V_{g,th}$	No	-(2-10) mV/°C	-	Good	No	High
R_{ds}	Yes	(3-7) mΩ/°C	No	Good	Yes	Less

CONCLUSION

This paper has focused on the feasibility of using drain-source resistance as a TSEP for tracking the junction temperature of the SiC MOSFET module for onsite condition monitoring. During the calibration test, the heatsink is heated to around 80 ºC and left until its temperature reaches 25ºC. Meantime, baseplate temperature, drain-source voltage, and drain-source current are measured, and also by employing fast edge computing, 3-D and 2-D look-up tables are programmed. Since the heatsink is cooled naturally and the interval between two turn-ON pulses is short (i.e., 200 ms), it is estimated that the instantaneous baseplate temperature is equal to junction temperature precisely.

On the other hand, due to the aging process and thus an increase in drain-source resistance, the SiC module requires to be calibrated after a specific time. In future work, it will be worthwhile to investigate using accelerated aging tests, counting algorithms, and accumulative damage models to update drain-source resistance after a specific level of degradation.

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