

Advanced Low-Voltage System-in-Package Half-Bridge MOSFET with Added Protection Features

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Abstract:

This paper deals with a smart System in Package (SiP) synchronous MOSFET half-bridge with internal current and thermal sensing circuits devoted to low-voltage supplies for autonomous driving applications. This kind of advanced application requests that Buck, Boost, or Buck-Boost converters can supply and stabilize the voltage. Furthermore, the temperature and the load current must be continuously monitored and controlled to increase the system's reliability. The SiP half-bridge described is experimentally evaluated in a Buck converter operation. Finally, a Buck interleaved configuration to improve the output current ripple and increase the current fed is experimentally investigated. The experimental results investigation demonstrates the effectiveness of the proposed SiP integrated half-bridge solution for an enhanced and reliable low voltage power supply.

Introduction

In the field of point of load power supplies for low voltage critical load such as microprocessors for new frontiers of high performance and reliability CPU cores, and in the section DDR (Double Data Rate) of chipset in the Fully Autonomous Driving (FAD) vehicles, the smart integrated synchronous half-bridge converter is a very attractive solution [1]. In this kind of application, the auxiliary power supplies play a crucial role in the reliability of the electronic systems used [2], [3]. In particular, considering the advanced automotive applications such as FAD, power supplies are a critical circuit system to ensure the safety of autonomous driving. For these power supply applications is necessary to monitor the main quantities such as maximum current and temperature thus that the limitation and protection systems can act promptly to avoid damage and dangers to the user and the vehicle. To take full advantage of the use of different technologies for systems that integrate power and complex signal circuits, SiPs represent a very viable solution. The advantages of the System in Package (SiP) are well known [4]

- Increasing of the switching transients
- Parasitic components (inductances and capacitances) reduction
- System compactness
- High power density

From point of view of the technology solution, the new wide-bandgap devices such as GaN FETs allow very high performance, and the SiP or full monolithic integration of power devices and gate drivers are the promising approaches to obtain advanced both switching and thermal conductivity features for power converters at high temperatures over 200 °C such as requested in electrical vehicle application [5]. However, at low-voltage application under 30V the pure silicon, MOSFETs (beyond the strongly reduced costs) a SiP technology approach is still very competitive especially as regards the direct resistance (R_{DSon}) obtainable

compared with low-voltage GaNs available in the market [6]. In an integrated solution of a half-bridge and driver, GaN technology features a drain-source voltage of 80V [7]. For these motivations, a SiP device with low voltage MOSFETs is a very effective way to achieve low-cost and high-performance integrated power supply systems. Furthermore, the MOSFET technology allows obtaining a switch for converter system with a simply driver circuit and quite satisfactory thermal behaviour [8]. The half-bridge circuit is a flexible topology to obtain the basic converter circuit such as Buck, Boost useful in voltage regulator circuit for power supplies system. In the paper, an asymmetric low-voltage power MOSFET-based half-bridge with gate protection, and sensing circuits integrated device is investigated. The operative conditions of the proposed devices for power supplies in advanced applications are extended in the range of 600 to 2000 kHz. The main switching results are carried out to demonstrate the effectiveness of the SiP solution in protected half-bridge converter applications. The added temperature and current sensing performance are described and tested. Furthermore, the presented SiP solution in the interleaved configuration are evaluated.

Integrated MOSFET Based Synchronous Half-Bridge Converter

The SiP in half-bridge configuration is composed of a MOSFET power stage in the last generation of advanced trench-gate Strip-FET technology [9]. While the gate control and sensing circuits are developed in the latest Bipolar, CMOS, and DMOS (BCD9) technology arrangement [10]. The SiP simplified circuit schematic is depicted in Fig. 1a, beyond the classic gate drivers, protection, and control logic circuits, the device has temperature and current sensing circuits. These device features are essential for the reliability of FAD systems. In the paper, these added sensing circuits are investigated in terms of fidelity and accuracy of the electrical and thermal quantities measurement.

The devices are encapsulated in a standard three-island power Quad Flat No-lead (QFN) package. The power QFN package is designed for medium power applications. It integrates low on-resistance and high-speed switching MOSFETs. Furthermore, the power QFN is a flexible solution showing a highly efficient space-saving package and very low parasitic inductances. Nowadays QFN package is used in a wide range of power applications Integrated Circuits (IC), with power stage and signal circuits in the same package. The package Power QFN in this SiP configuration is depicted in Fig. 1b. The Figure of Merit (FOM) is the parameter to evaluate the benefit of the MOSFET power stage. The FOM are related to the mathematical multiplication of on-resistance (R_{DSon}) and total Gate Charge (Q_G). In Table 1 the FOM parameters for the high-side (HS) and the low-side (LS) devices are described. The R_{DSon} reported in Table I are relative to the maximum value.

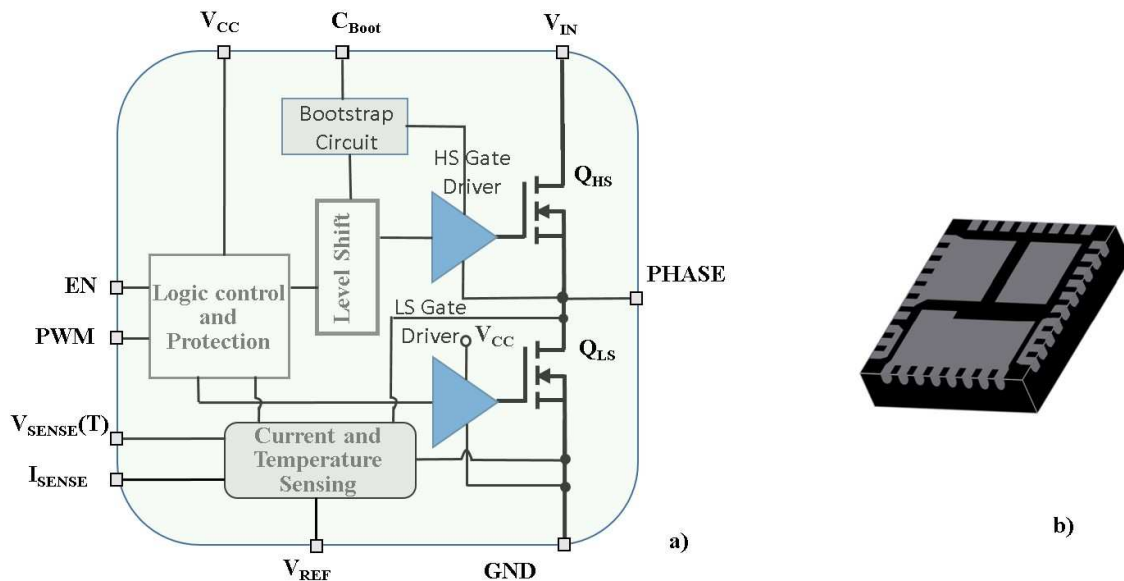


Fig. 1 a) Simplified schematic of half-bridge SiP power stage, gate control and sensing circuits. b) Power QFN package used.

The half-bridge integrated circuit can be used as Buck or Boost converter to supply a wide range of voltage load requests. To investigate the proposed SiP solution, a suitable evaluation board is developed. By the use of the experimental board, the sensing circuit behaviour is investigated. Furthermore, the converter switching performance and efficiency measurement at different switching frequencies are analyzed.

Current and Thermal Sensing Circuits

The thermal and current sensing circuits allow measuring the phase current by a dedicated circuit. The board design leads to an experimental relation to computing the actual current value by the following design equation.

$$I_{SENSE} = K_I \cdot (V_{ISENSE} - V_{REF}), K_I = \left(\frac{1000}{5} \cdot \frac{A}{V} \right) \quad (1)$$

An external current probe (based on the Hall effect) to measure the low side MOSFET average current (through the R_{DSon} and the phase node voltage processing) as the load varies is considered to compare the effectiveness of the proposed sensing approach.

The layout of the experimental board is reported in Fig. 2a. While the comparison between sensing current I_{SENSE} evaluated by (1) and the actual measured current I_{Lmean} . Is depicted in the graph in Fig.2b.

Table I Main MOSFETs Parameters

Parameters	HS MOSFET	LS MOSFET
$R_{DSon} @25^{\circ}C$ [m Ω]	4	1.2
$R_{DSon} @100^{\circ}C$ [m Ω]	6	1.8
Total gate charge: $Q_{G(max)} @10V$ [nC]	11	29.4

Thermal Sensor Arrangement and Operation

The temperature is measurement is obtained by a voltage signal proportional to the thermal variation. The voltage V_{TSENSE} linked with the device temperature is obtained by the equation

$$V_{TSENSE}(T) = V_{REF} + K_T \cdot T_{SENSE}, K_T = \left(8 \frac{mV}{^{\circ}C} \right) \quad (2)$$

The thermal sensor was placed inside the smart system in the package of the device. It was positioned in the bottom right corner of the driver, (see a green rectangle in Fig. 3a), to be as close as possible to both power switches. Therefore, the sensing placement choice allows a better thermal derating behavior. It is a Proportional to Absolute Temperature (PTAT) Bandgap Current sensor, a conventional architecture implemented in the IC to link the sensor current to the actual temperature of the chip. To check the fidelity and mismatch between the real MOSFET devices' junction temperatures and the one detected by the thermal sensor, a dedicated thermal measurement was run. The diode placed in the chip structure of the driver, used as a thermal sensor (reachable through two pins of the IC device), and the body-drain diodes of the high side/low side MOSFETs were pre-characterized to define their forward voltage drop dependence versus the temperature.

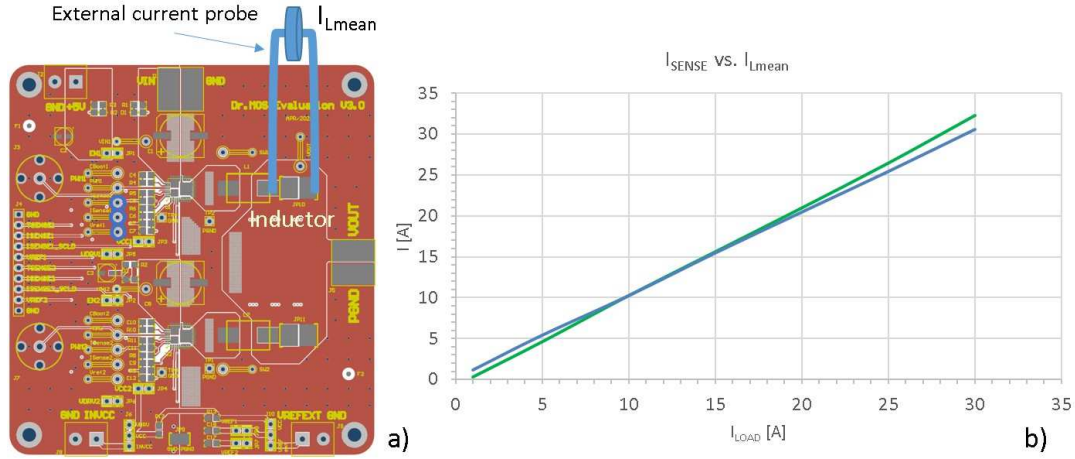


Fig. 2 a) Layout of half-bridge SiP evaluation board with external current probe. b) I_{SENSE} versus I_{Lmean} current comparison.

The two diodes on the power switches and the one on the driver were initially calibrated by heating them to a known temperature, their voltage drop V_F for MOSFET was measured at different temperatures and then their calibration was fixed. They were used as thermal sensors, according to this calibration methodology. It provides a fixed current, once the thermal steady state is achieved. The V_{FD} voltage (voltage variation on sensing driver diode) was measured, allowing to compute the temperature, through (2) of the chip tracking back their V_F versus, T_j characteristics considering the dependence previously set during the characterization itself. This method applied to the two power MOSFETs' diodes and the driver's one defined a measured mutual thermal impedance. This parameter allows us to sense the heat transferred by the power devices to the driver chip. Thus the temperature increase of every single die when others are managing power can be estimated. The temperatures were estimated following the above-reported methodology either on the driver or on the MOSFETs and so was defined the maximum temperature gap among the power devices and the driver itself that, by a simple matching through the copper frame and package construction features, is heated up indirectly. In Fig. 3b is reported a typical waveform to physically demonstrate the process previously described with the relevant current, voltage and energy loss values. Where V_{FD} is the voltage drop waveforms for driver diode, and V_{FS} is the voltage transient waveforms for Body diodes of the MOSFETs at the imposed current source-drain I_{FS} . In Fig. 3b, the diode placed in the driver circuit (Fig. 3a) is pre-turned on in forward bias with a small current of few mA, flowing through it, which is not able to raise its temperature. The waveform shows the V_F variation of both driver and body-drain diodes when a fixed current of 4.2 A flows through the body-drain diode of the power MOSFETs.

Temperature estimation and validation

To demonstrate the effectiveness of the thermal sensing approach a temperature estimation at different load current conditions I_{load} is carried out. The operative conditions are $V_{\text{in}}=12\text{V}$, $V_{\text{out}}=1\text{V}$, inductive load, $L=150\text{nH}$, at switching frequency $f_{\text{sw}}=600\text{kHz}$, and output current variation I_{LOAD} in the range 5 – 30 A. The temperatures evaluated by the thermal sensor housed in the SiP are compared with the measurements achieved with an infrared thermal camera on the top of the device. In Table II the main results of the sensing temperature and the measured one are reported. Considering the estimation and measurement results at 20 A, the difference between the temperature from the thermal sensing T_{SENSE} and the temperature detected by the infrared thermal camera T_{ITC} is around 10°C .

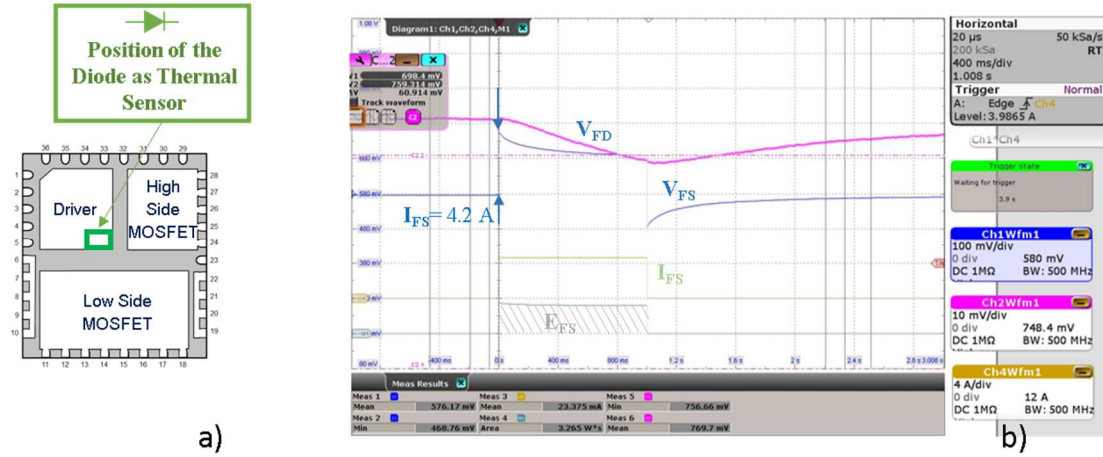


Fig. 3 a) Thermal sensor position in the SiP device. b) V_{FD} variation on driver diode due to thermal mutual coupling body diode heating, body-drain diode V_{FS} , I_{FS} body-drain diode current imposed and the energy losses calculated in the area defined by the current pulse shape, $E_{FS}=3.265\text{W}\cdot\text{s}$.

The graphics of Fig. 4 show the behavior of the temperature rising with the increase of the I_{LOAD} and the comparison with the measurements obtained with the infrared thermal camera on the top of the device. The differences in the two curves displayed are related to the equivalent thermal resistance between the package and the die R_{THeq} .

Table II. Voltage measured and Temperature Estimation with thermal sensor and infrared thermo camera versus load current

Parameters	I_{out} (A)	V_{TSense} (V)	T_{Sense} (°C)	T_{ITC} Thermo camera (°C)
Operative Condition $V_{in}=12\text{V}$, $V_{out}=1\text{V}$, $f_{sw}=600\text{kHz}$	5	0.895	36.88	43.3
	10	0.965	45.63	55.0
	15	1.031	53.88	62.8
	20	1.132	66.50	76.3
	25	1.267	83.38	96.5
	30	1.451	106.38	123.6

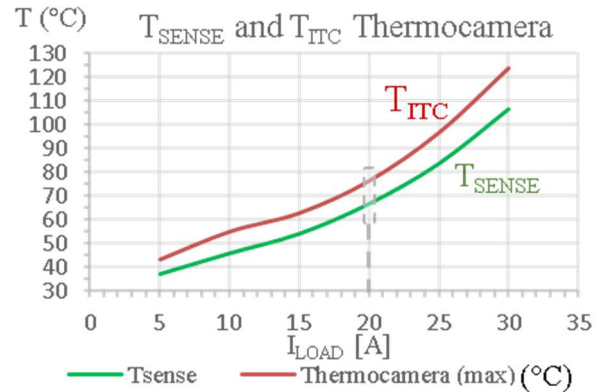


Fig. 4. Sensing temperature T_{SENSE} comparison with the temperature measured with the infrared thermal camera T_{ITC} at different load current I_{LOAD} .

In the same working condition at 20A the the power losses in the high and low side MOSFETs were estimated. In a single switch, both switching and conduction losses were considered. At $I_{LOAD}=20\text{A}$, in the low side (Q_{LS}) MOSFET the power losses are 1.06 W while in the high side (Q_{HS}) are 0.67 W. We used a 4layer board and the results of a pre-characterization show the high side, the low side and the mutual Z_{TH} curves reported in the picture of Fig. 5.

At steady state the R_{TH} are:

- $R_{TH\text{ LS-4layer}} = 24.6\text{ }^{\circ}\text{C/W}$
- $R_{TH\text{ HS-4layer}} = 29.6\text{ }^{\circ}\text{C/W}$
- $R_{TH\text{ HSLs-4layer}} = 16.8\text{ }^{\circ}\text{C/W}$ (mutual thermal resistance)

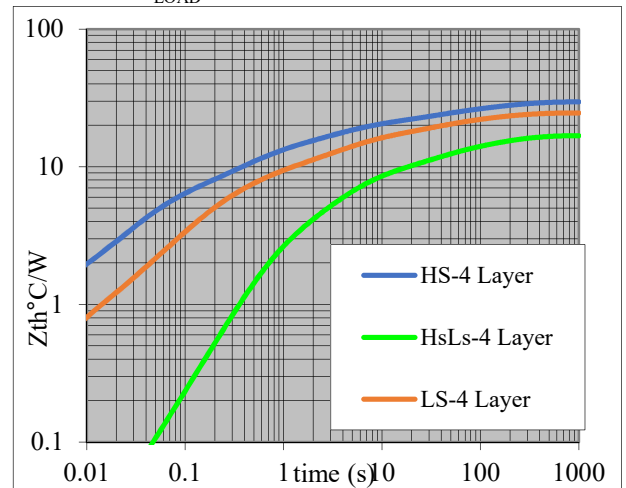


Fig. 5. Thermal impedance of the junction to 4 layer copper (Cu) board curves of the high side switch, the low side switch, and the mutual Z_{TH} .

Thus it is possible to calculate the single contribution to the junction temperature variation at $I_{LOAD}=20$ A in a single switch. The temperature difference ΔT_{JLS} due to the power losses (P_{LSTOT}) of the Q_{LS} switch is

$$\Delta T_{JLS} = R_{TH LS-4layer} \cdot P_{LSTOT} = 24.6 \cdot 1.06 = 26.1^{\circ}C \quad (3)$$

The ΔT_{JHS} due to the power losses (P_{HSTOT}) of the Q_{HS} switch is

$$\Delta T_{JHS} = R_{TH HS-4layer} \cdot P_{HSTOT} = 29.6 \cdot 0.67 = 19.8^{\circ}C \quad (4)$$

The $\Delta T_{j mutual}$ due to the power losses due to the mutual impedance is

$$\Delta T_{j mutual} = R_{TH HSLS-4layer} \cdot (P_{LSTOT} + P_{HSTOT}) = 16.8 \cdot (1.06 + 0.67) = 29^{\circ}C \quad (5)$$

The total temperature difference $\Delta T_{j TOT}$ is the sum of the every contribute.

$$\Delta T_{j TOT} = \Delta T_{JLS} + \Delta T_{JHS} + \Delta T_{j mutual} = 26.1 + 19.8 + 29 = 74.8^{\circ}C \quad (6)$$

The temperature evaluated by (6) is in agreement with the corresponding results obtained in Table II.

Furthermore, the validation of the thermal sensing features is carried out in comparison with both thermocouple and infrared thermal camera measurements with a different heating approach. An external thermal gun to heat up the component up to a fixed temperature is used, without imposing a current I_{LOAD} . This passive validation methodology allows for a more accurate temperature evaluation demonstrating the effectiveness of the thermal sensor solution proposed. At thermic steady-state, the heat propagation reaches the MOSFETs and driver circuit in the SiP. Thus, the V_{TSENSE} furnishes a temperature closer to the actual one set by the heat gun. The thermal sensor temperature T_{SENSE} is obtained by reading V_{TSENSE} and applying (2). The package temperatures set by the thermal gun have been measured both through the infrared thermal camera and the thermocouple (considering the thermocouple results as a reference for the thermal gun action). The T_{SENSE} is achieved by (2) detecting the corresponding V_{TSENSE} . The V_{TSENSE} and the temperatures achieved by thermal gun heating on the SiP device are reported in Table III. In Fig. 6 a graphic comparison of the three temperature measurements is reported with the voltage V_{TSENSE} detected at $70^{\circ}C$ highlighted.

As shown in Fig. 6, at $70^{\circ}C$ the V_{TSENSE} is 1.16V. This V_{TSENSE} value compared to the value achieved in the previous test at 20A (1.16 V) highlighted in Table II shows a discrepancy of 0.03V (around 2.6%) the $\Delta V = 1.16 - 1.13 = 0.03$ V matches with a $\Delta T = 3.75^{\circ}C$ mismatch.

TABLE III Results of V_{TSENSE} and the Temperatures Achieved by Thermal Gun Heating

V_{TSENSE} (V)	T_{SENSE} ($^{\circ}C$)	T_{ITC} Thermo camera ($^{\circ}C$)	T_{TC} Thermo couple ($^{\circ}C$)
1.030	53.75	50.6	50
1.290	86.25	84.7	80
1.485	110.63	103.4	100
1.640	130	132.8	130
1.778	147.25	150.2	150

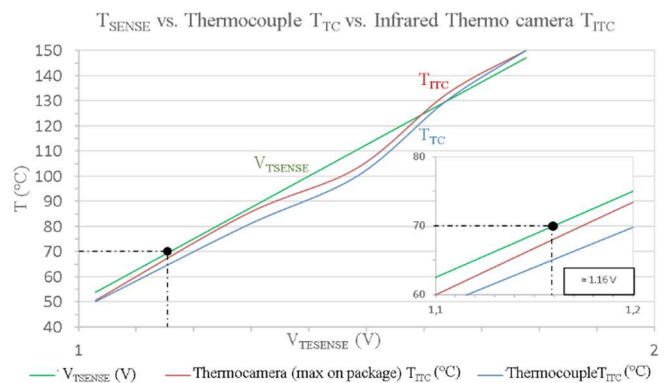


Fig. 6. Sensing temperature T_{SENSE} comparison with the temperature measured with the infrared thermal camera T_{ITC} and a thermocouple T_{TC} .

Experimental Buck Converter Evaluation

The switching behaviour analysis of a single-phase buck converter is based on the following test conditions reported in Table IV.

The switching waveforms of the synchronous switching leg in Buck configuration (see Fig. 7a) at 600kHz are reported in Fig. 7b. The current paths during the different stages of the transient behaviour are depicted in Fig. 7a. Furthermore, in Fig. 7b the devices' current path transients are also indicated. Moreover, the voltage trace related to the current sensing (V_{ISENSE}) are reported with the I_{out} and V_{in} .

Table IV. Buck Converter Test Conditions

V_{in} [V]	12-16
V_{out} [V]	1-1.1
I_{load} [A]	5-30
f_{sw} [kHz]	600-2000
L [H]	150n

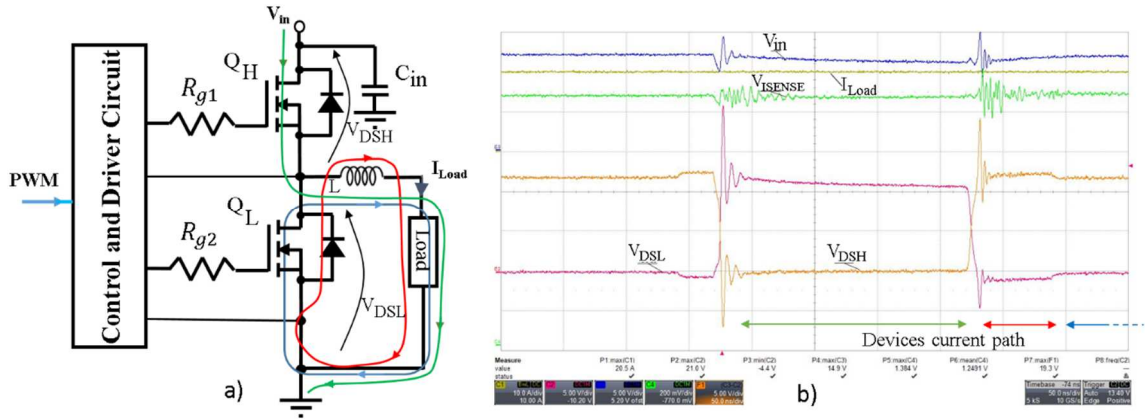


Fig. 7 a) Synchronous switching leg for Buck converter topology and current path during the switching transients. b) Switching waveforms of the Drain-Source of both low-side and high-side. The input voltage V_{in} with the output current (I_{out}) and the voltage trace related to the current sensing are reported too. $I_{LOAD}=10A/div$, $V_{DHS}=V_{DLS}=5V/div$, $V_{in}=5V/div$, $t=50ns/div$.

In the switching waveforms reported, the ringing voltage and the spike are due to high di/dt on the parasitic inductances in the switching power mesh of the evaluation board layout. The steady-state switching waveforms in the operative condition of Table IV considering a $I_{LOAD}=20A$ with the temperature sensing (T_{SENSE}) displayed are reported in Fig. 8a. In Fig. 8b a zoomed view during the switching transients is shown. The peak value appears during the switching transients of the low side switch and high side switch due to the parasitic inductances of the power loop lead a maximum voltage peak up to 20V on the low side MOSFET. T_{SENSE} waveform maintain a clean voltage information also during the transients switching conditions as shown in Fig. 8b.

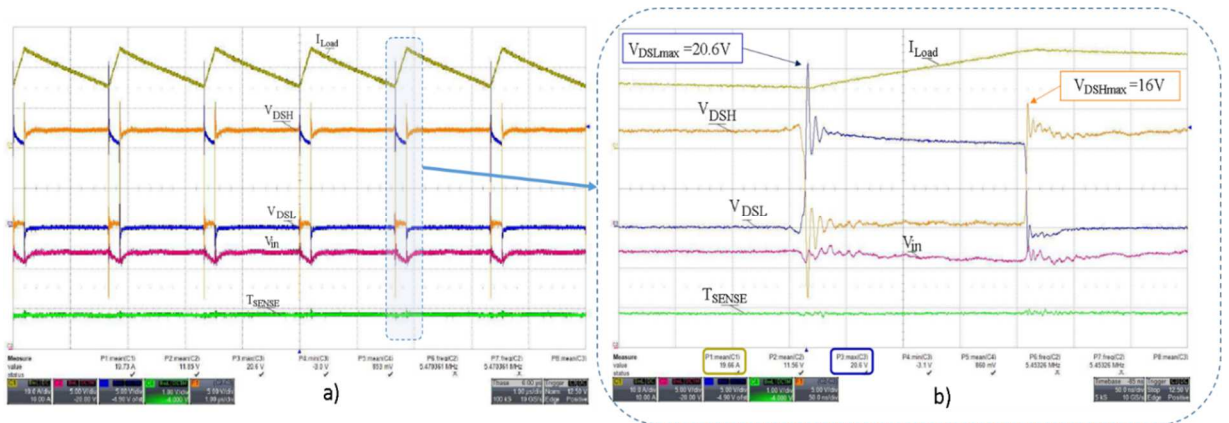


Fig. 8 a) Synchronous switching leg for Buck converter switching waveforms in steady-state. b) Zoomed view of the switching transient. $I_{LOAD}=10A/div$, $V_{DHS}=V_{DLS}=5V/div$, $V_{in}=5V/div$, $T_{SENSE}=1V/div$. a) $t=100\mu s/div$, b) $t=50ns/div$.

The over current protection action is described in Fig. 9. During normal working (at $I_{load}=20$ A, $V_{in}=12$ V and $f_{sw}=600$ kHz) the device was externally heated to bring it to an over temperature condition (OTP) as described in Fig. 9a. During the OTP the PWM stopped and it restarted once the OTP state was removed. The zoomed view of Fig. 9b details the return of standard PWM operating conditions when the over-temperature is removed.

The efficiency of the Buck converter developed on the SiP system is satisfactory and in line with the requirements of the applications considered. The device has the best performance at a switching frequency of 600 kHz. However, the efficiency is also remarkable at the frequency of 1.2 MHz and features lower efficiency at 2 MHz. In Fig. 10 the efficiency results versus the load current (I_{Load}) are reported at the three switching frequencies in the range reported in Table 4.

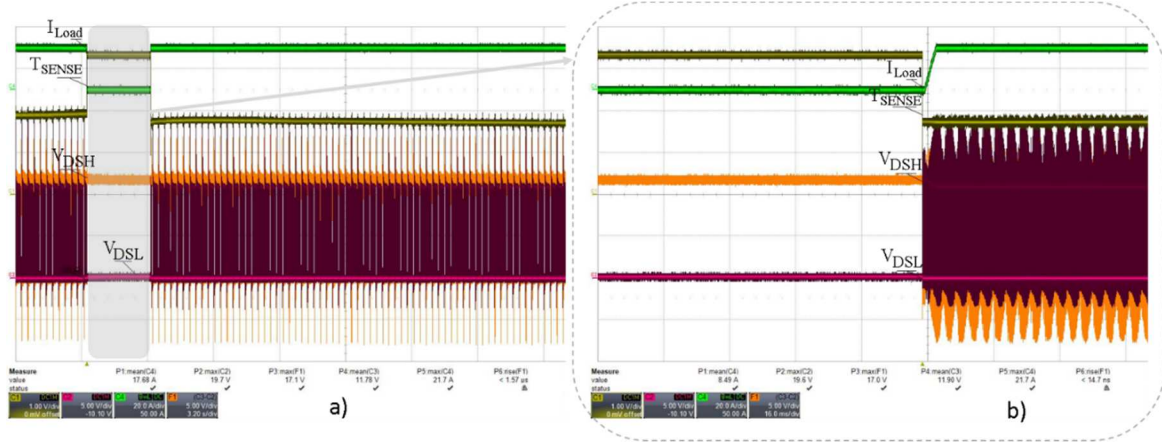


Fig. 9 a) Steady-state operating condition with an over-temperature condition caused through a time-limited externally heating. b) Zoomed view of the return of standard PWM operating conditions when the over-temperature is removed. $I_{LOAD}=10$ A/div, $V_{DHS}=V_{DLS}=5$ V/div, $T_{SENSE}=1$ V/div, $I_{LOAD}=20$ A/div a) $t=10$ ms/div, b) $t=1$ ms/div.

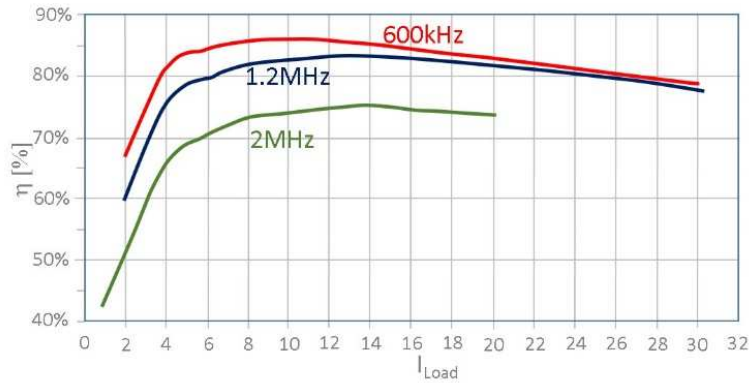


Fig. 10 Power converter efficiency versus the load current at different switching frequency

Interleaved Buck Converter Application

In FAD application the interleaved buck and boost configuration is a viable solution to improve the current output waveforms quality reducing the ripple. Furthermore, the output-filter sizes decrease in an interleaved implementation due to the lowered current in the power switching leg for each phase [11]. The number of the operating switching legs can be activated according to the load request optimizing the device's current share. Selecting the maximum number of the switching legs (generally 3 in this kind of application) the current in

the single device is reduced acting in the MOSFETs heating reduction. A simplified block scheme of SiP MOSFET in interleaved configuration implementing 3 switching legs is reported in Fig. 11.

Therefore, the interleaved solution features several advantages which can be summarized in

- Reduction of ripple on the output current;
- Reduced input capacitance;
- Reduced output capacitance;
- Better thermal performance and efficiency at high load currents.

The current ripple of the output current depends on the duty-cycle and the number of switching legs adopted in the interleaving technique [12]. Considering two phases of interleaved Buck converter with non-coupled inductors, the experimental operative waveforms at Continuous Current Mode (CCM) are reported in Fig. 12a.

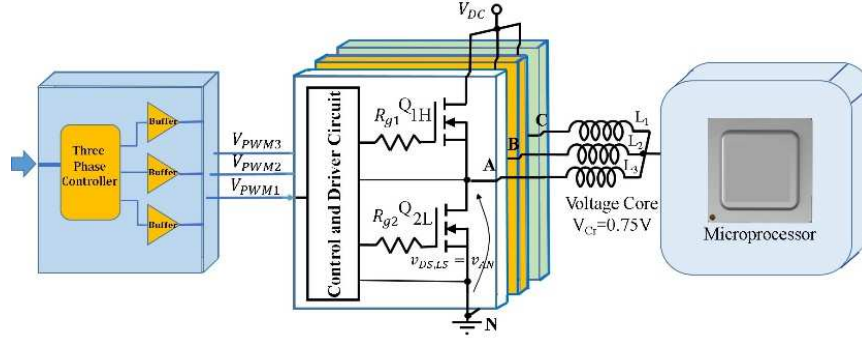


Fig.11 Power supply based on the SiP MOSFET half-bridge converter in interleaved configuration

The total output current $I_{Loadtot}$ is the sum of the single leg current I_{Load1} and I_{Load2} . In Fig 12b a single switching leg voltage are zoomed with the maximum peak voltage ($V_{DSL1, peak}$) of 17.8V. The reduction of the output load current ripple peak ($\Delta I_{Loadtot} = 0.5A$) is depicted in Fig.12b. Finally, the dead time imposed to avoid cross conduction is also highlighted. In the actual two phase interleaved converter design a dead time of 45ns was chosen.

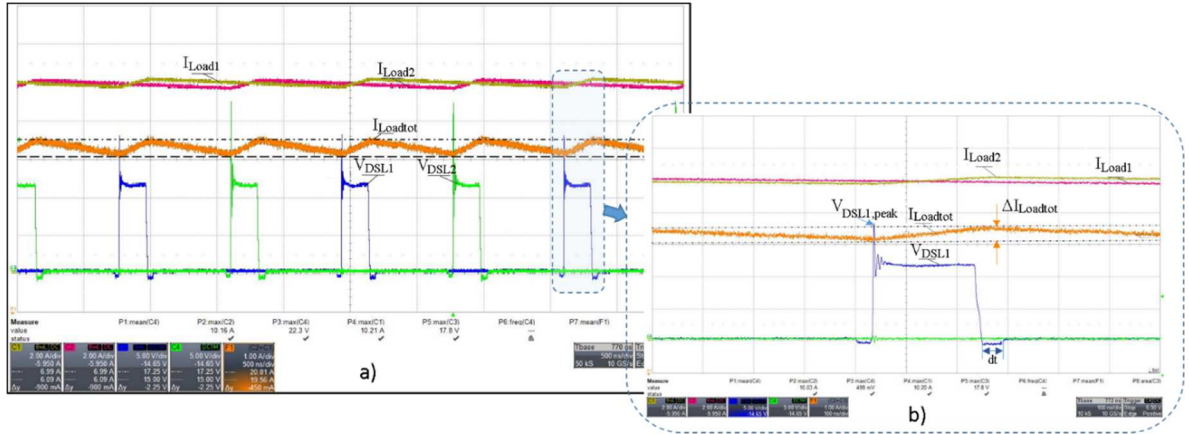


Fig.12. a) Low side voltages and currents switching waveforms of the two switching legs in interleaved configuration with the total load current. b) Single switching voltage V_{DSL1} with the total output current waveform $I_{Loadtot}$ and the underlined dead time chosen. $I_{Load1}=I_{Load2}=2A/div$, $V_{DSL1}=V_{DSL2}=5V/div$, $I_{Loadtot}=1A/div$, a) $t=500ns/div$, b) $t=100ns/div$

Conclusions

In the proposed paper an advanced cost-effective SiP half-bridge MOSFETs is presented. The integrated device is oriented to develop a flexible and reliable power supply to power the FAD IC system. The half-bridge SiP solution can be used to achieve Buck, Boost, or Buck-Boost converters. In the paper, a Buck converter switching evaluation is carried out to demonstrate the usefulness of the proposed hybrid integrated power switch and control gate circuits. The inner sensing circuits related to the leg current and the power device temperature are focused. In particular, the temperature sensing approach is tested and validated by several

measurement experimental tests and numerical analysis to demonstrate the effectiveness of the proposed sensing solution. Furthermore, a two-phase interleaved buck converter application is experimentally evaluated to demonstrate the effectiveness of the SiP solution. In the interleaved configuration, the control circuit allows activating the switching legs according to the load demand to modulate the IC supply current request. In this way, the achievable Buck, Boost or Buck-Boost converters are able to supply and stabilize the voltage at the value required by the active safety system in automotive application.

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