Investigation and Mitigation of Common-mode Voltage in Four-level NPC Converters Modulated by Redundant Level Modulation

Jun Wang*, Wei Xu, Xibo Yuan and Lihong Xie
Department of Electrical and Electronic Engineering, University of Bristol, Bristol, UK
*Email: jun.wang@bristol.ac.uk

Keywords

«DC-AC converter», «Multi-level inverters», «Modulation strategy», «Power quality», «Capacitor voltage balancing»

Abstract

Redundant level modulation (RLM) has emerged as a powerful modulation-based voltage balancing method for a range of multilevel converters. For four-level neutral point clamped (4L-NPC) topologies, utilizing redundant voltage levels is the mandatory solution in principle to enable the single-end 4L-NPC converters to keep a voltage balance under all operating conditions, without requiring auxiliary circuits. However, the side effects of RLM caused by the extra switching actions have not been fully studied, with the common-mode voltage in particular. Hence, this work investigates the worsened common-mode voltage problem induced by RLM through theoretical analysis and simulations, followed by a simple carrier-based mitigation method that is verified in experiments.

Introduction

Multilevel converters, e.g. neutral-point-clamped (NPC) converters, have been intensively researched as promising alternatives to conventional two-level converters, because they in general offer lower switching loss, lower blocking voltage requirement and lower output harmonics/EMI. For example, the three-level NPC topologies, such as diode-clamped [1], T-type [2] and active-clamped [3] NPC topologies, have been widely implemented in low/medium-voltage power conversion systems to improve the system efficiency and power density, such as in [2], [4]. As the derivation of three-level topologies, four-level topologies, such as π-type NPC [5], active-clamped NPC [6] and hybrid clamped [7] variations, offer further reduced switching voltage and more output voltage steps, for which a typical system and operation principle are illustrated in Fig. 1 and Fig. 2. However, due to the inherent lack of capacitor-self-balancing capability, the application of four-level NPC converters has been significantly hindered [8]. For example, the four-level converter implemented by Schneider Electric [9] requires auxiliary 'dc bus balancers' circuits to maintain the capacitor voltages, which introduces extra loss and additional hardware.

Fortunately, the recently proposed redundant level modulation (RLM) [10] has solved the voltage balancing issue completely, which is a modulation-based approach that relies on more switching events rather than requiring additional hardware. RLM shares the same principles as other existing approaches, such as the overlapped carrier [11] and virtual vector [12] approaches, in terms of utilizing the redundant voltage levels. RLM has been proven effective and implemented in [13], [14] with its most significant side effect, the extra switching loss, well evaluated and understood. However, there have been concerns raised about the common-mode (CM) voltage in RLM-modulated four-level converters since the additionally switching events can very likely lead to worsened CM voltage, which is reported to cause issues such as the reduced bearing lifetime, increased insulation stress and

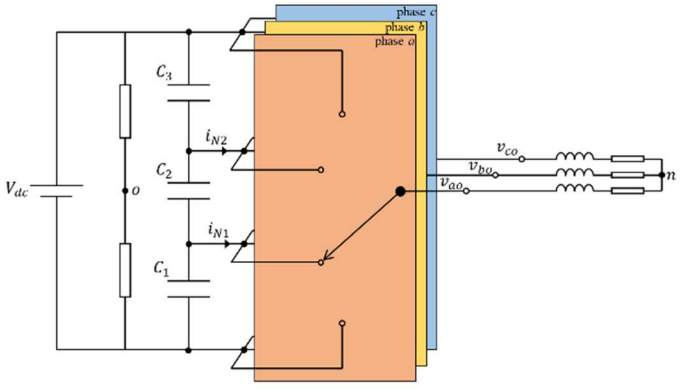

Fig. 1. A four-level NPC three-phase inverter-load system

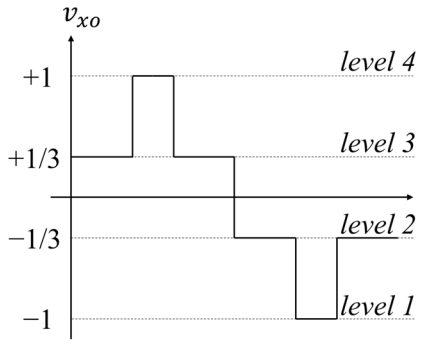

Fig. 2. Illustration of the four-level phase output voltage

electromagnetic interference (EMI) problems. While the RLM is deemed mandatory for four-level NPC converters to maintain their basic functionality without auxiliary circuits, this potential CM voltage issue need to be investigated and mitigated. Although there are previous studies conducted on the CM voltage of four-level NPC converters and the mitigation methods, e.g. [15], [16], they are all based on the assumption of having auxiliary voltage balancing circuits.

Hence, as the contribution, this work investigates the CM voltage in RLM-modulated four-level NPC converters for the first time and subsequently proposes a modulation-based simple solution to mitigate it. The investigation starts from the theoretical analysis of the generation principles of CM voltage comparing the regular modulation and RLM cases. This issue is then evaluated in simulation with a novel mitigation method implemented, which is later verified in an experimental setup.

Overview of Redundant Level Modulation in 4L-NPC converters

To start with, the principle of the RLM is explained as follows. In contrast to the regular modulation, RLM introduces one output voltage level in each carrier cycle as illustrated in Fig. 3 to gain extra control of capacitor voltages, while the volt-second product of this carrier cycle remains the same. This can be understood as altering the high-frequency behavior of the converter output by adding more switching actions. In four-level NPC converters, RLM can be easily realized through splitting and altering the modulating waves as demonstrated in [10], with regular level-shifted carriers in place as illustrated in Fig. 4 and the output states defined in Table I.

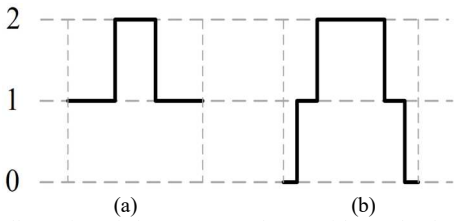

Fig. 3. Illustration of phase output voltages with equal volt-second product (a) regular modulation (b) redundant modulation

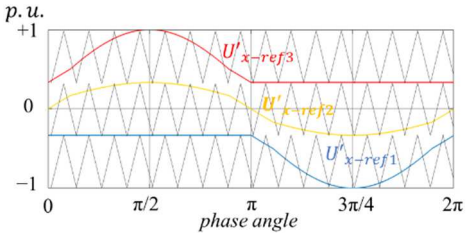

Fig. 4. Implementation of RLM with level-shifted carriers [10].

Table I Output states of a four-level NPC phase leg

Level *l*	Output states per unit	Output voltage v_{xo}
4	*+1*	$+V_{dc}/2$
3	*+1/3*	$+V_{dc}/6$
2	*−1/3*	$-V_{dc}/6$
1	*−1*	$-V_{dc}/2$

Fig. 5 further illustrates the principle of this carrier-based implementation of RLM in 4L-NPC converters. It can be seen that, with an offset value added to space away two adjacent split modulating waves, one extra voltage level can be added to the output voltage, which brings a new degree of freedom to manipulate the duty ratio of certain voltage levels to control the capacitor voltages. The closed-loop control based on this concept can be found in [10]. Note that the RLM pattern showing in Fig. 5 means that one phase leg compulsorily outputs three voltage levels in one carrier cycle, either *level 4/3/2* (when $V_{x\text{-ref}} \geq 0$) or *level 3/2/1* (when $V_{x\text{-ref}} < 0$).

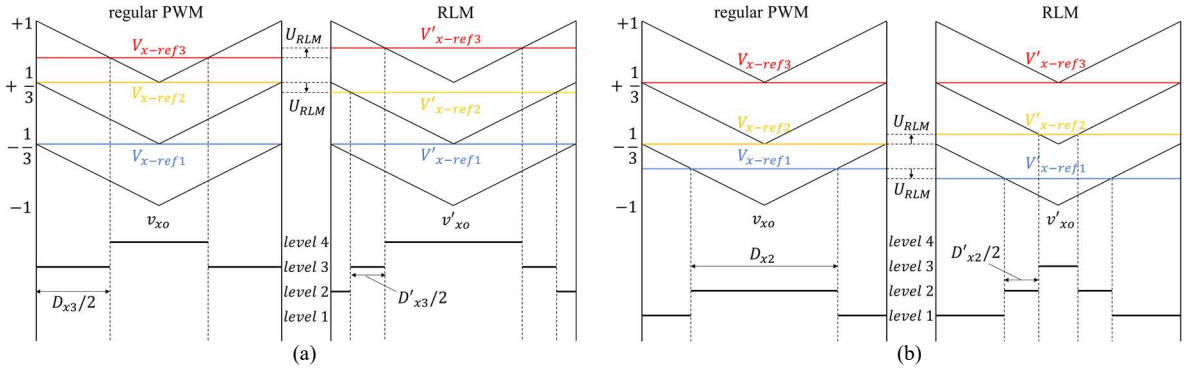

Fig. 5. Illustration of one carrier cycle under regular PWM and RLM when (a) $V_{x\text{-ref}} \geq 0$ (b) $V_{x\text{-ref}} < 0$

The drawback of RLM is the extra switching events, e.g. four switching transitions in one carrier cycle instead of two transitions in regular modulation. This drawback leads to extra switching losses as analyzed in [10]. Meanwhile, it also has impacts on the common-mode voltage which will be shown in the next section.

Common-mode voltage in RLM-modulated 4L-NPC converters

The common-mode (CM) voltage in a three-phase inverter-load system is expressed as

$$v_{no} = \frac{1}{3}(v_{ao} + v_{bo} + v_{co}) \tag{1}$$

Where n denotes the load neutral point; o is the dc-link neutral point (normally grounded); a, b, c represents the three phases. To investigate the CM voltage impacted by RLM, a simulation model has been built based on the following specifications in a 1200V, three-phase, four-level ANPC [13], [14] configuration. The switching frequency f_{sw} is lowered to 2 kHz to show the phenomenon more clearly.

TABLE II SYSTEM SPECIFICATIONS

DC-link voltage V_{dc}	1200 V
Nominal capacitor voltage E	400 V
Carrier frequency f_{sw}	2 kHz
Fundamental frequency f_0	50 Hz
C1 = C2 = C3	450 μF
Modulation index M	0.92
R	4.57 Ω per phase
L	3 mH per phase

Firstly, to theoretically analyze the CM voltage, the three phase output voltages (V_a, V_b, V_c) in one switching cycle are re-classified into a dominant voltage V_1 and two possible cancelling voltages V_2 and V_3. Starting from a four-level converter modulated by regular Sinusoidal Pulse Width Modulation (SPWM), the possible common mode voltages are listed in Table III, referring to the combinations of V_1, V_2 and V_3. All the cases are illustrated in Fig. 6 throughout one fundamental cycle. In the majority of the cases, V_2 and V_3 fully cancel each other, which leaves V_1 as the only term left in (1), such as Case A2, A3, A4, A5 in Table III, and yields possible CM voltage amplitude of 1/6 of V_{dc} and 1/12 of V_{dc}. In some cases, V_2 and V_3 can only partly cancel each other (e.g. *+1* and *−1/3*), which yields a higher CM voltage amplitude of 5/18 of V_{dc}, such as Case A1 and A6 in Table III. A typical switching window under regular SPWM is shown in Fig. 7(a), where the peak CM voltage is 333.3V (5/18 of 1200V).

Table III Common-mode voltage levels in 4L-NPC with regular SPWM

Case	Sum of voltage level l	V_1	V_2	V_3	V_{CM}
A1	10	*+1*	*+1*	*−1/3*	$5/18 \cdot V_{dc}$
A2	9	*+1*	*+1/3 (+1)*	*−1/3 (−1)*	$1/6 \cdot V_{dc}$
A3	8	*+1/3*	*+1*	*−1*	$1/12 \cdot V_{dc}$
A4	7	*−1/3*	*+1*	*−1*	$-1/12 \cdot V_{dc}$
A5	6	*−1*	*+1/3(+1)*	*−1/3(−1)*	$-1/6 \cdot V_{dc}$
A6	5	*−1*	*−1*	*+1/3*	$-5/18 \cdot V_{dc}$

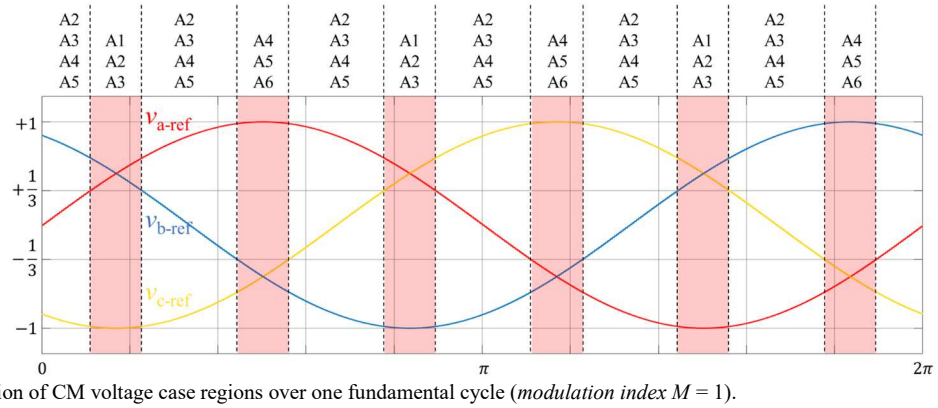

Fig. 6. Illustration of CM voltage case regions over one fundamental cycle (*modulation index* M = 1).

In the case of RLM, the converter phase leg mandatorily outputs three voltage levels in one switching cycle, rather than two levels, which leads to two more additional combinations of voltages as listed in Table IV. As can be seen, in Case B1 and Case B8, V_2 and V_3 have the same sign and therefore they reinforce rather than cancel each other. These two extra cases leads to a higher CM voltage amplitude of 7/18 of V_{dc} to appear in RLM four-level converters. This is illustrated in Fig. 7(b) where a peak CM voltage of 466V (7/18 of 1200V) can be observed. It can also be seen that the output phase voltage V_{xo} shows the RLM pattern as intended in Fig. 5. The cause of this is that the highest voltage levels of three phases all locate at the central of a switching cycle, showing a 'hill' shape.

Table IV Common-mode voltage levels in 4L-NPC with RLM

Case	Sum of voltage level *l*	V_1	V_2	V_3	V_{CM}
B1	11	*+1*	*+1*	*+1/3*	$7/18 \cdot V_{dc}$
B2	10	*+1*	*+1*	*−1/3*	$5/18 \cdot V_{dc}$
B3	9	*+1*	*+1/3 (+1)*	*−1/3 (−1)*	$1/6 \cdot V_{dc}$
B4	8	*+1/3*	*+1*	*−1*	$1/12 \cdot V_{dc}$
B5	7	*−1/3*	*+1*	*−1*	$-1/12 \cdot V_{dc}$
B6	6	*−1*	*+1/3(+1)*	*−1/3(−1)*	$-1/6 \cdot V_{dc}$
B7	5	*−1*	*−1*	*+1/3*	$-5/18 \cdot V_{dc}$
B8	4	*−1*	*−1*	*−1/3*	$-7/18 \cdot V_{dc}$

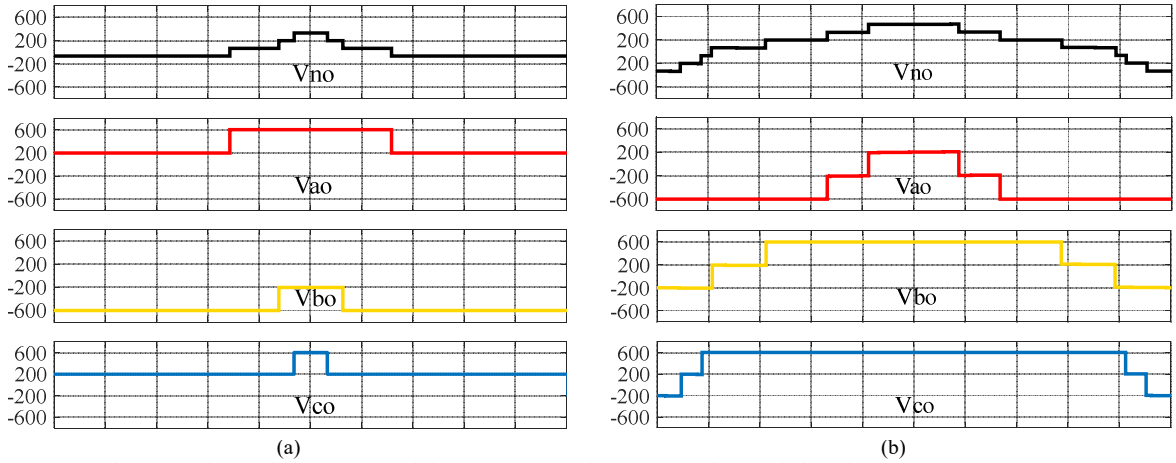

Fig. 7. Zoomed in view of the switching cycle with largest V_{no} (a) regular SPWM with ideal dc-link (b) RLM

Fig. 9 shows a comparison of common-mode voltage extracted from simulation between regular modulation and RLM cases. Note that the regular SPWM case assumes the dc-link is idea, i.e. the three capacitor voltages in Fig. 1 constantly stay at the nominal value - so there is no voltage balancing problem. This ideal case is not realistic without any external voltage balancing circuits or three isolated dc sources connected in series. Therefore, the regular modulation case here is just for the reference purpose.

It can be seen that the common-mode voltage in the RLM case is worse than the regular modulation case. In the regular modulation, the V_{no} shows six steps as analyzed in Table III, in which the peak value is ±333 V ($5/18 \cdot V_{dc}$). In contrast, in the RLM case, the V_{no} shows two more steps (one extra step towards each polarity), which brings the peak value to ± 466 V ($7/18 \cdot V_{dc}$ as analyzed in Table IV). The FFT analysis of the CM voltage is plotted in Fig. 9, which shows the amplitude of CM voltage harmonics has a spike of 300 V at the switching frequency. Note there is also a low-frequency CM voltage component at the 3rd order as can be observed in Fig. 9, which is caused by the zero-sequence voltage added for voltage balancing purpose [10]. This finding establishes that the RLM does worsen the CM voltage problem in a 4L-NPC converter.

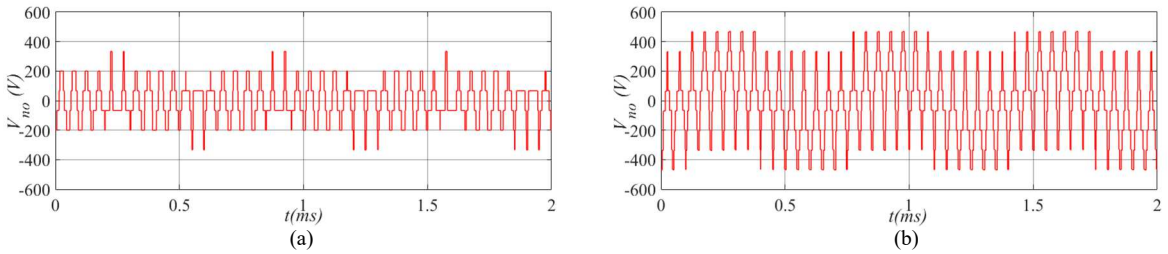

Fig. 8. Common-mode voltage V_{no}, (a) regular SPWM with ideal dc-link (b) RLM

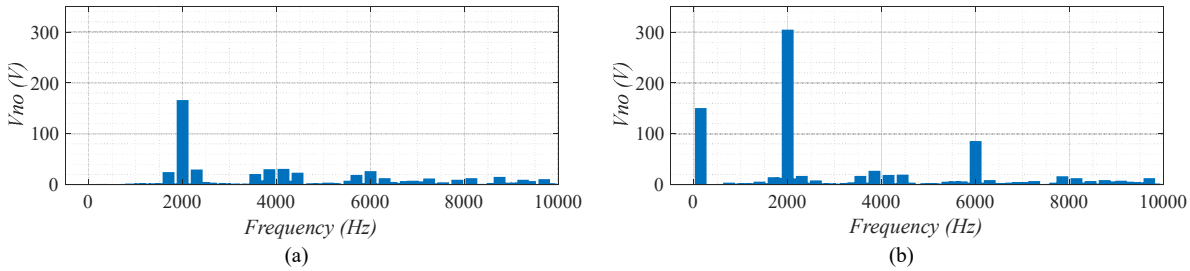

Fig. 9. FFT of common-mode voltage V_{no} (a) regular SPWM with ideal dc-link (b) RLM

A simple carrier-based mitigation method of common-mode voltage

To mitigate the CM voltage, this work proposes a simple carried-based approach as follows. To counter the worst-case scenario discovered in the last section, the proposed solution is to apply modified carriers with 180° phase shift (flipped vertically) when $V_{ref} \geq 0$, as shown in Fig. 10. When $V_{ref} < 0$, the carriers stay the same. This approach leads to a time-domain redistribution of voltage levels in one carrier cycle. As can be seen, this redistribution results in the output *level 4* pushed to the two sides of one carrier cycle when $V_{ref} \geq 0$, instead of the middle, which result in a 'valley' shape instead of a 'hill' shape. In this case, when $V_{ref} \geq 0$, the middle part of one switching cycle will be *level 2* instead of *level 4*, which can avoid the CM voltage to fall on the *level 4 + level 4 + level 2* case in Fig. 7. By applying approach, the output voltages v_{xo} (when $V_{ref} \geq 0$) and v_{xo} (when $V_{ref} < 0$) show a symmetric pattern with reference to the dc-link neutral point voltage v_o, in contrast to the regular case in Fig. 5. This approach is referred as the 'flipped carrier'.

Given sinusoidal reference voltages, there is always one phase having the opposite signum to the other two as illustrated in Fig. 6. In this case, the 'valley' shaped voltage with flipped carriers would show in at least one phase , which leads to V_2 and V_3 fully/partly cancelling each other at the center of one switching cycle, instead of reinforcing each other as in the case of Fig. 7(b). Therefore, the worst cases B1 and B8 are mitigated.

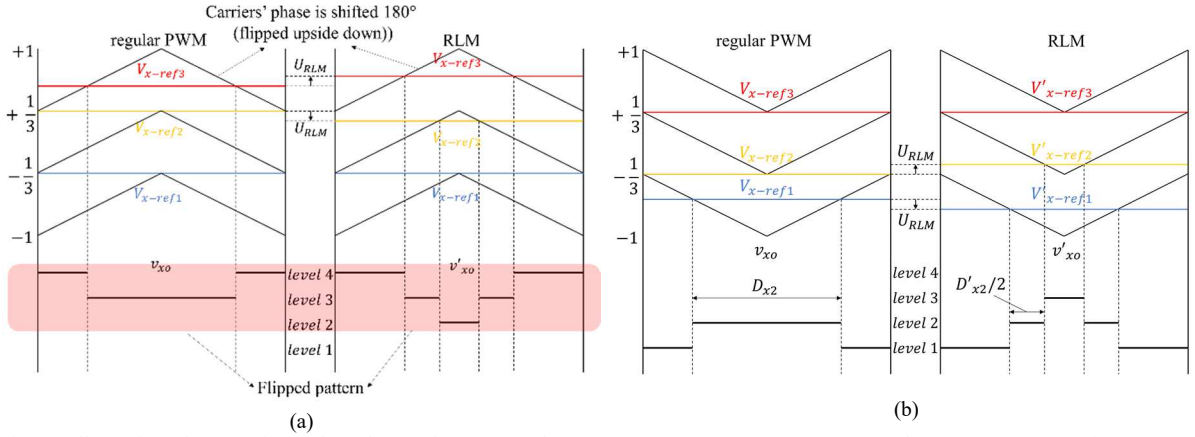

Fig. 10. Illustration of one carrier cycle under regular PWM and RLM (a)$V_{x\text{-}ref} \geq 0$ **with flipped carriers** (b)$V_{x\text{-}ref} < 0$ (same as Fig. 5)

The proposed flipped carrier approach is evaluated in simulation under the same conditions. Fig. 11 shows the CM voltages in this case, where a clear improvement can be observed in comparison to Fig. 8. In the RLM case, the largest amplitude is mitigated from 466V to 333V, which only appears four brief times in one fundamental cycle under this operating point. For most of the time, the CM voltage is only 1/6 or 1/12 of the dc-link voltage. The FFT analysis of the CM voltage is shown in Fig. 12(b). As can be seen, the amplitude of CM voltage at around the switching frequency is damped from 300V to <100V, which is a considerable improvement compared to Fig. 9(b). Note the flipped carrier is also effective for the SPWM case. The peak CM voltage is also improved to 1/6 of V_{dc}

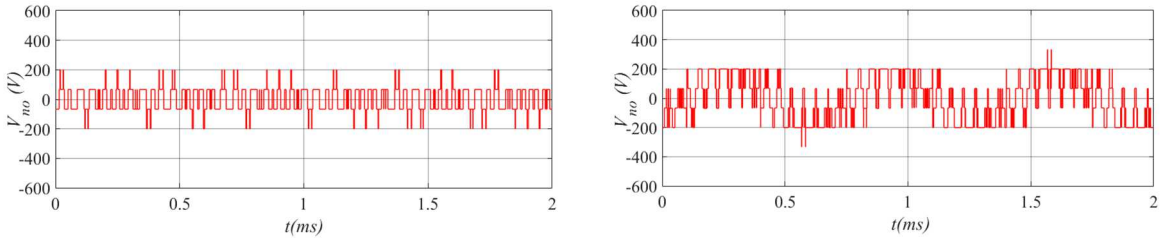

Fig. 11. Common-mode voltage V_{no} **with flipped carriers** (a) regular SPWM with ideal dc-link (b) RLM

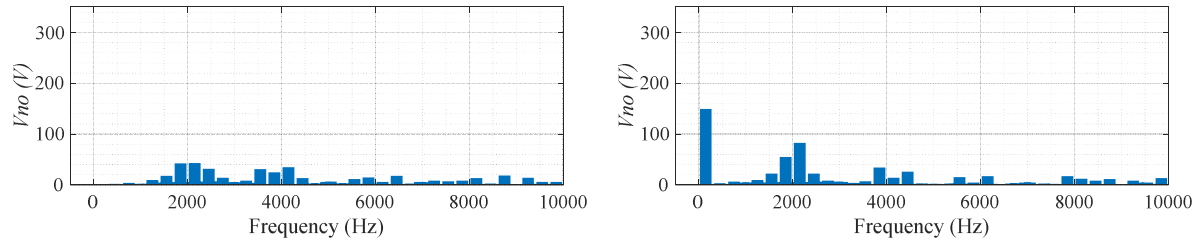

Fig. 12. FFT of common-mode voltage V_{no} **with flipped carriers** (a) regular SPWM with ideal dc-link (b) RLM

As plotted in Fig. 13(b), the worst-case center part in one switching cycle becomes *level 2* + *level 4* + *level 4*, which has an amplitude of 333V (5/18 V_{dc}) and shows much less frequently in contrast to Fig. 7. Note that the V_2 and V_3 (the top levels of V_{ao} and V_{bo} at the center in Fig. 13(b)) does not always completely cancel each other since the width of them does not always equal to each other. The widths of these levels depend on the voltage balancing algorithm which is corelated to the load current level, switching frequency and the capacitances as demonstrated in [10]. Therefore, there are still possible high CM voltage at 7/18 of V_{dc} that 'leaks out', i.e. the brief spikes reaching 466 V observed in Fig. 13(b). These spikes can also occur at the boundaries between switching cycles.

In other words, because this flipped carrier method is not an "active" CM voltage mitigation method (e.g. by actively selecting the appropriate voltage vectors as in [17]), it cannot completely and consistently suppress the peak CM voltage throughout fundamental cycles depending on the operating point, while it can effectively damp the CM voltage harmonics as demonstrated. Note that, with regular SPWM assuming auxiliary voltage balancers, the proposed flipped carrier also shows effective CM voltage suppressing effect comparing Fig. 8(a)/Fig. 9(a) against Fig. 11(a)/Fig. 12(a).

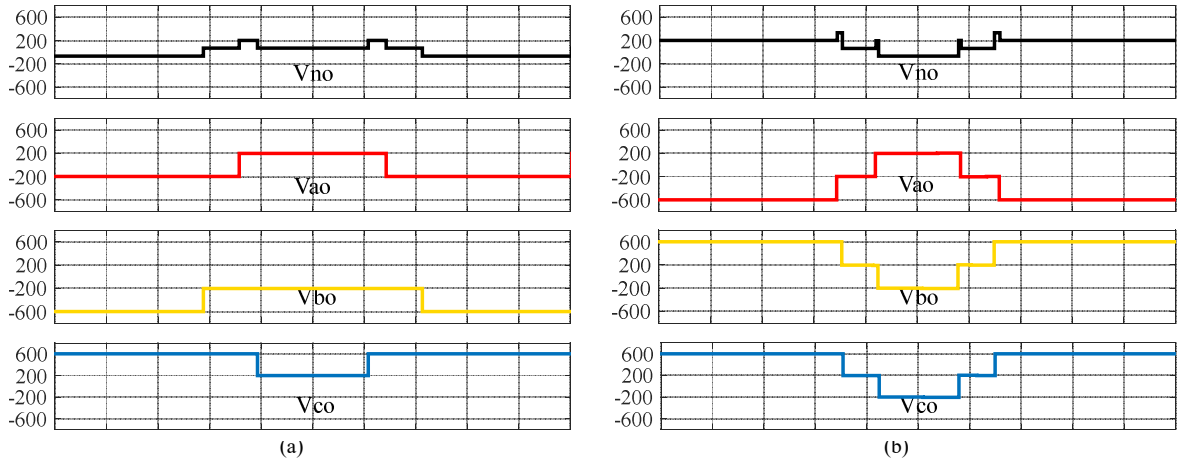

Fig. 13. Zoomed in view of the switching cycle showing largest V_{no} **with flipped carriers** (a) regular SPWM with ideal dc-link (b) RLM

This flipped carrier approach can be straightforwardly implemented through the process illustrated in Fig. 14, with the polarity of the reference voltage $V_{x\text{-ref}}$ (before introducing RLM) as the criteria to determine the phase angle of the carriers in each switch period T_{sw}. This approach can also be referred as the symmetrical modulation since the output voltage pattern in the positive and negative cycle of $V_{x\text{-ref}}$ is symmetrical with respect to the *x* axis.

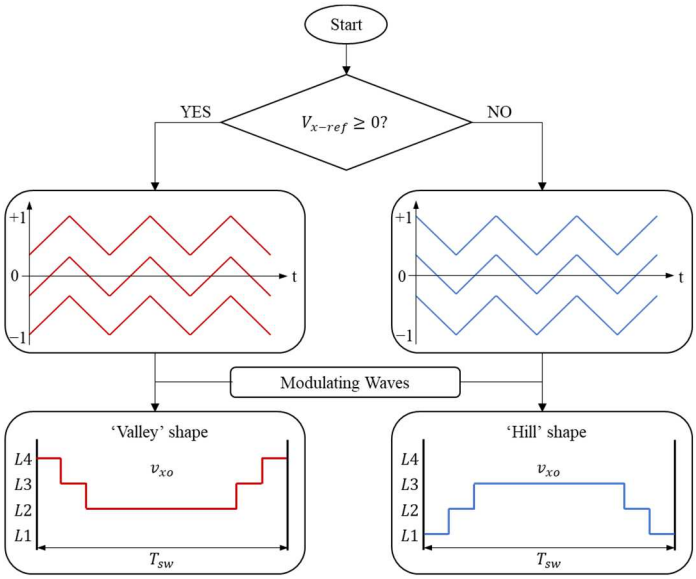

Fig. 14. Flow chart of the proposed 'flipped carrier' approach

However, the flipped carrier approach is found to trade off the quality of differential-mode (DM) line-to-line voltage while mitigating the common-mode voltage, which is a common trade-off as reported in [17]. This trade-off is reflected in Fig. 15, where it can be seen that the THD and harmonic at f_{sw} is worse in the case of the flipped carriers. Meanwhile, it does not impact the phase voltage quality as noticeably. Therefore, this trade-off between CM voltage and DM line voltage quality needs to be considered when the flipped carrier approach is applied.

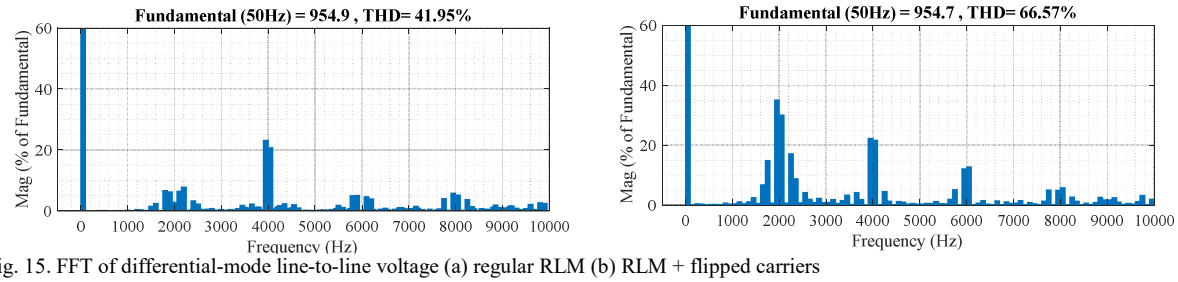

Fig. 15. FFT of differential-mode line-to-line voltage (a) regular RLM (b) RLM + flipped carriers

Experimental Evaluation

The presented CM voltage analysis and the proposed mitigation method are evaluated in an experimental prototype consisting of Silicon Carbide (SiC) modules and four-level active NPC topology as presented in [14], of which a photo is shown in Fig. 16. The functionality of the original RLM has been proven as shown in Fig. 17 in a single-end inverter operating at a high modulation index and near-unity power factor, which shows well-balanced capacitor voltages given the four visible straight-line output voltage levels in the phase voltage. The converter operates at a dc-link voltage V_{dc} of 1000V, a switching frequency f_{sw} of 5 kHz, a modulation index M of 0.9 and a power factor $cos\ \varphi$ of 0.99 in this case as a proof of concept.

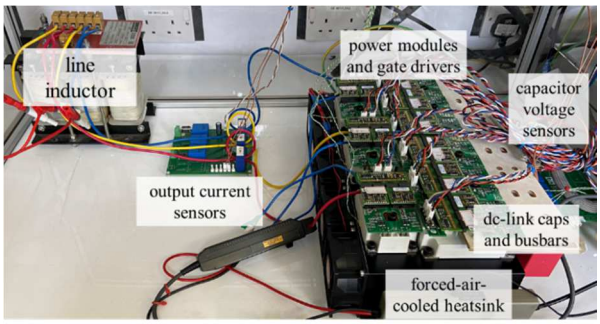

Fig. 16. Photo of a three-phase four-level inverter prototype

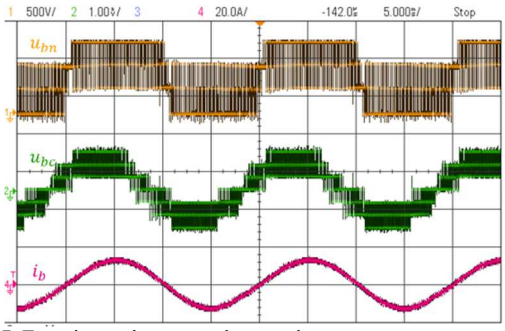

Fig. 17. Experimental output voltage and current

With the dc-link voltage reduced to 300 V, the waveforms are captured and shown below, with FFT performed on the measured CM voltage. The RLM-based voltage balancing algorithm and the flipped carrier approach are programmed in a DSP (TMS320F28335) based controller.

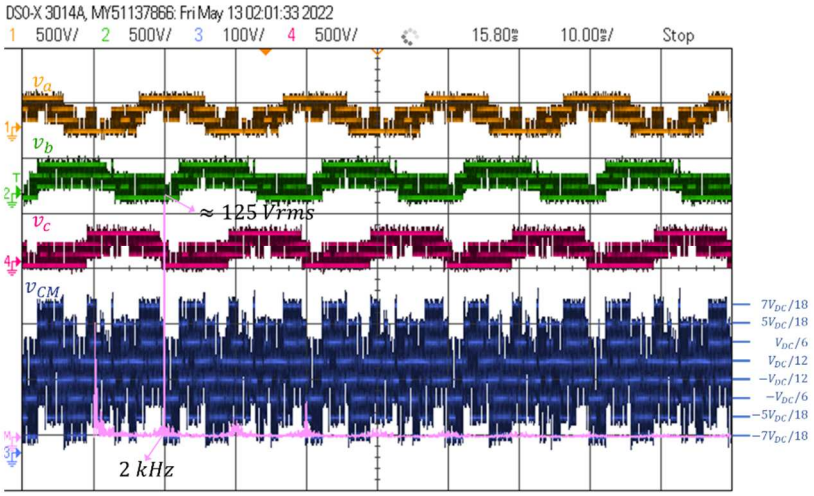

Fig. 18. Experimental waveforms with RLM and regular carriers (f_{SW} = 2 kHz, M = 0.8, V_{DC} = 300 V)

In the case with RLM and regular carriers in Fig. 18, it can be seen that the CM voltage often reaches the $7V_{dc}/18$ level, and the largest harmonic around the switching frequency reaches around 125 V. With the flipped carriers implemented, the improved waveforms are shown in Fig. 19. Although there are still spikes reaching $7V_{DC}/18$, it is visible that the CM voltage is improved overall. This is proved by the FFT results showing that the largest harmonic around the switching frequency is significantly reduced to 33 V from 125 V. In summary, this comparison verifies the effectiveness of the proposed flipper carrier as a CM voltage mitigation method.

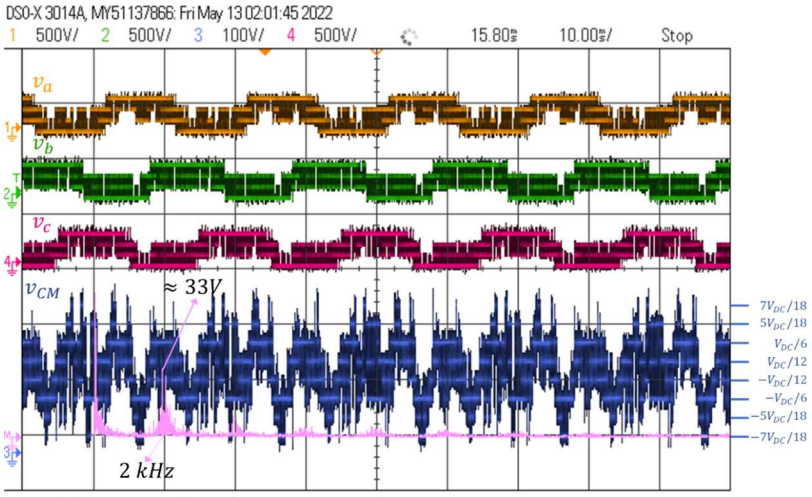

Fig. 19. Experimental waveforms with RLM and flipped carriers (f_{SW} = 2 kHz, M = 0.8, V_{DC} = 300 V)

Fig. 20 shows a zoom-in view of the waveforms. In the highlighted switching cycle, it can be seen that v_b and v_c show a 'valley' shape while v_a shows a 'hill' shape as intended in Fig. 10. This results in the CM voltage mostly ranging between $+V_{dc}/6$ and $-5V_{dc}/18$, with a narrow spike reaching $-7V_{dc}/18$, which is explained by Fig. 13(b).

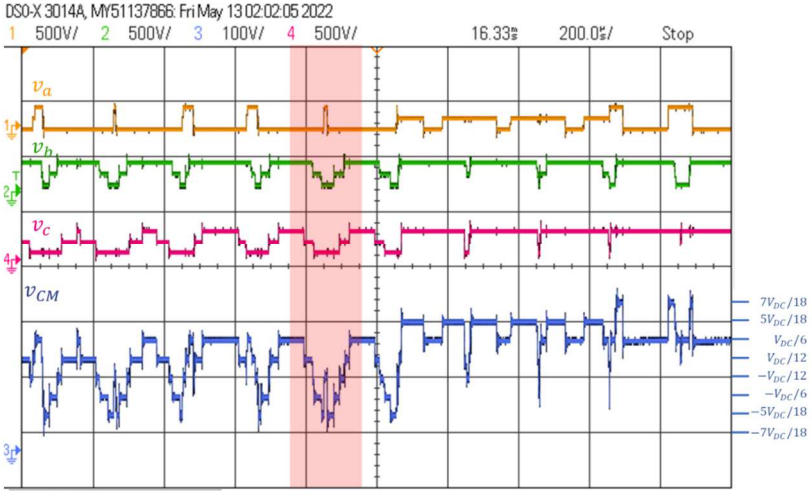

Fig. 20. Zoomed-in experimental waveforms with RLM and flipped carriers (f_{SW} = 2 kHz, M = 0.8, V_{DC} = 300 V)

Conclusion

This paper studied the common-mode voltage issue in the RLM-modulated four-level NPC converters. While the RLM is mandatory for the voltage balancing purpose, its negative impact on the CM voltage has been confirmed by theoretical analysis and simulation, which shows a considerable increase of switching-frequency harmonics and peak amplitude (from $5V_{DC}/18$ to $7V_{DC}/18$). To address this issue, this work proposes a simple carrier-based method with flipped carriers to mitigate the CM voltage, which has proven to be effective in the simulation and experiments.

References

[1] A. Nabae, I. Takahashi, and H. Akagi, “A new neutral-point-clamped PWM inverter,” *IEEE Trans. Ind. Appl.*, vol. 1A-17, no. 5, pp. 518–523, 1981.

[2] M. Schweizer and J. W. Kolar, “Design and implementation of a highly efficient three-level T-type converter for low-voltage applications,” *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 899–907, 2013.

[3] P. Barbosa, P. Steimer, J. Steinke, M. Winkelnkemper, and N. Celanovic, “Active-Neutral-Point-Clamped (ANPC) multilevel converter technology,” in *European Conference on Power Electronics and Applications*, 2005.

[4] D. Zhang, J. He, and D. Pan, “A megawatt-scale medium-voltage high-efficiency high power density ‘ SiC + Si ’ hybrid three-level propulsion systems,” *IEEE Trans. Ind. Appl.*, vol. 55, no. 6, pp. 5971–5980, 2019.

[5] X. Yuan, “A four-level π-type converter for low-voltage applications,” in *IEEE Proc. European Conference on Power Electronics and Applications*, 2015.

[6] B. Wang, “Four-level neutral point clamped converter with reduced switch count,” in *IEEE Annual Power Electronics Specialists Conference*, 2008, pp. 2626–2632.

[7] K. Wang, Z. Zheng, L. Xu, and Y. Li, “A four-level hybrid-clamped converter with natural capacitor voltage balancing ability,” *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1152–1162, Mar. 2014.

[8] J. Pou, R. Pindado, and D. Boroyevich, “Voltage-balance limits in four-level diode-clamped converters with passive front ends,” *IEEE Trans. Ind. Electron.*, vol. 52, no. 1, pp. 190–196, Feb. 2005.

[9] H. R. Nielsen, “3-phase high-power UPS,” US8385091B2, 2013.

[10] J. Wang, X. Yuan, and B. Jin, “Carrier-based closed-loop dc-link voltage balancing algorithm for four level NPC converters based on redundant level modulation,” *IEEE Trans. Ind. Electron.*, vol. 68, no. 12, pp. 11707–11718, 2021.

[11] K. Wang, Z. Zheng, and Y. Li, “A novel carrier-overlapped PWM method for four-level neutral-point clamped converters,” *IEEE Trans. Power Electron.*, vol. 34, no. 1, pp. 7–11, Jan. 2019.

[12] S. Busquets-Monge, J. Bordonau, and J. Rocabert, “A virtual-vector pulsewidth modulation for the four-level diode-clamped DC–AC converter,” *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1964–1972, Jul. 2008.

[13] X. Yuan, J. Wang, I. Laird, and W. Zhou, “Wide-bandgap device enabled multilevel converters with simplified structures and capacitor voltage balancing capability,” *IEEE Open J. Power Electron.*, vol. 2, no. May, pp. 401–410, 2021.

[14] J. Wang, I. Laird, X. Yuan, and W. Zhou, “A 1.2 kV 100 kW four-level ANPC inverter with SiC power modules and capacitor voltage balance for EV traction applications,” in *IEEE Proc. Energy Conversion Congress and Exposition (ECCE)*, 2021.

[15] J. Pribadi, B. Park, and D. C. Lee, “Operation of four-Level ANPC inverter based on space-vector modulation for common-mode voltage reduction,” in *IEEE Proc. International Symposium on Electrical and Electronics Engineering (ISEE)*, 2019, pp. 281–285.

[16] J. Pribadi, D. C. Lee, and B. M. Han, “Suppression of common-mode voltage based on space-vector modulation for four-level hybrid inverters,” in *IEEE Proc. International Future Energy Electronics Conference (IFEEC)*, 2019.

[17] X. Yuan, Y. Li, and C. Wang, “Objective optimisation for multilevel neutral-point-clamped converters with zero-sequence signal control,” *IET Power Electron.*, vol. 3, no. 5, pp. 755–763, 2010.