On the Limit Cycle Caused by Controller Saturation in Synchronous Buck Converter

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***Abstract*-- In the reported instability incidents of power converter-based systems, a constant-amplitude oscillation instead of divergence was often observed, which is the so-called limit cycle phenomenon. This does not agree with theoretical analysis based on classical linear control theory. Taking a synchronous buck converter as an example, this paper aims to investigate the underlying mechanism of the limit cycle phenomenon. It finds that this phenomenon results from the nonlinear controller saturation. To clarify the underlying mechanism, the controller saturation is linearized through the describing function method, then the generalized Nyquist stability criterion is applied. It reveals that the system operation point dynamically drifts and ultimately stays at the critically stable point, featuring the constant-amplitude oscillation. Moreover, the occurrence condition and the calculation of the oscillating amplitude and frequency are also explored. Simulations and experiments verify the correctness of the analysis.**

***Index Terms*—Power converter, nonlinear, controller saturation, limit cycle, stability, oscillation.**

I. Introduction

Power converters have been widely used in various fields, such as aerospace [1], marine [2], renewable energy generation [3], etc. Their typical characteristics are commonly elaborated by means of the small-signal average modeling [4]. As a rule of thumb, the dynamic behavior of a stable system is convergent, and that of an unstable system should feature divergence [5]. In practice, the former always coincides well with the theoretical expectation, whereas the latter does not always. For instance, a resonance of 1270 Hz rather than divergent was reported at Luxi high voltage direct current (HVDC) project in Yunnan, China [6]. In fact, the oscillation with constant amplitude and frequency can be categorized as the limit cycle.

Up to now, many efforts have been made to explain the limit cycle phenomenon under instability. It is found that this phenomenon is far related to the nonlinear factors in the system [7], [8]. For instance, the controller saturation is usually employed at the output of the regulator to prevent the modulation signal from exceeding the range of the sawtooth signal, which has already been proven to affect the dynamic behavior of the system through the Lyapunov method [9], [10] or phase portrait [11]. However, to the author's best knowledge, the condition for the occurrence of the limit cycle remains open. Besides, the prediction of the associated oscillating frequency and amplitude is also unclear. To clarify these issues are helpful for risk assessment of such phenomena in the engineering project. In view of this, a synchronous buck converter is taken as an example in this paper to explore the limit cycle phenomenon caused by the nonlinear controller saturation.

The rest of this paper is organized as follows. In Section II, taking the nonlinear controller saturation into account, an accurate model of the synchronous buck converter is established. In Section III, the nonlinear controller saturation is linearized through the describing function method [12], and then the generalized Nyquist stability criterion (GNC) [13] is applied to reveal the underlying mechanism of the limit cycle. Besides, the occurrence condition and the calculation of the limit cycle are elaborated. In Section IV, simulations and experiments are conducted to verify the theoretical analysis. Section V concludes this paper.

II. System Description and Accurate Model

A. System Description

Fig. 1 shows the topology of the synchronous buck converter. It consists of an LC filter, a load R_{Ld}, and two power switches Q and Q_r applied with complementary control signals. To regulate the output voltage v_o tracking its reference V_{ref}, the error signal v_e is processed by a voltage regulator $G_c(s)$. The obtained modulation signal v_{M} is compared with the sawtooth signal v_{saw} through a pulse-width modulator (PWM), generating the gate signals of Q and Q_r with the duty cycle of d. From Fig. 1, the traditional linear block diagram of the synchronous buck converter can be derived, as shown in Fig. 2(a). Therein, V_{M} and $G_{vd}(s)$ are the amplitude of v_{saw} and the control-to-output transfer function, respectively. The loop gain $T_{\mathrm{p}}(s)$ can be expressed as

$$T_{\mathrm{p}}(s)=\frac{1}{V_{\mathrm{M}}}G_c(s)G_{vd}(s)=\frac{V_{\mathrm{in}}}{V_{\mathrm{M}}}\frac{G_c(s)}{s^2LC+sL/R_{\mathrm{Ld}}+1} \quad (1)$$

where a proportional-integral (PI) regulator is adopted as $G_c(s)$, expressed as

$$G_c(s)=K_{\mathrm{P}}+K_{\mathrm{I}}/s \quad (2)$$

where K_{P} and K_{I} are the proportional and integral gains, respectively.

The associated characteristic equation of the system is expressed as

$$1+T_{\mathrm{p}}(s)=0. \quad (3)$$

According to the classic linear control theory, the

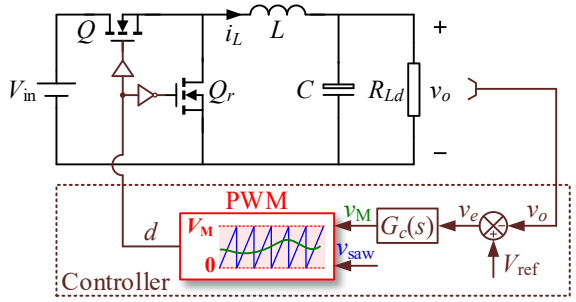

Fig. 1 Topology of the synchronous buck converter.

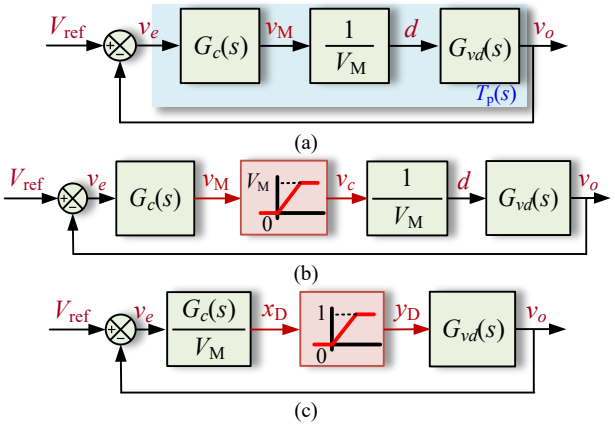

Fig. 2 Block diagram. (a) Traditional model. (b) Accurate model. (c) Equivalence form of the accurate model.

system will be stable if none of the eigenvalues in (3) locate in the right-half plane (RHP), otherwise, instability occurs and v_o will unboundedly diverge as shown in Fig. 3(a). However, the output of the circuit topology behaves as a constant-amplitude oscillation as shown in Fig. 3(b). Thus, a more accurate model is needed.

B. Accurate Model

In fact, a controller saturation is configured at the output of $G_c(s)$ to prevent v_M from exceeding the range of v_{saw}, the corresponding model is shown in Fig.2 (b). If the system is stable, v_M is always within the linear modulation range, the controller saturation does not work, and Fig. 2(b) can be simplified to Fig. 2(a). Once instability occurs, v_M inevitably increases, resulting in the occurrence of controller saturation. Moving the PWM gain $1/V_M$ from the output of the saturation to its input, as shown in Fig. 2(c), the controller saturation is equivalent to limiting the duty cycle within [0, 1], where its input and output signals are denoted as x_D and y_D, respectively. Fig. 4 shows the relation between x_D and y_D, where the saturation function with upper and lower limits of 1 and 0 is denoted as sat(·), yields

$$y_D = \mathrm{sat}(x_D) = \begin{cases} 0 & x_D \le 0 \\ x_D & 0 < x_D < 1. \\ 1 & x_D \ge 1 \end{cases} \tag{4}$$

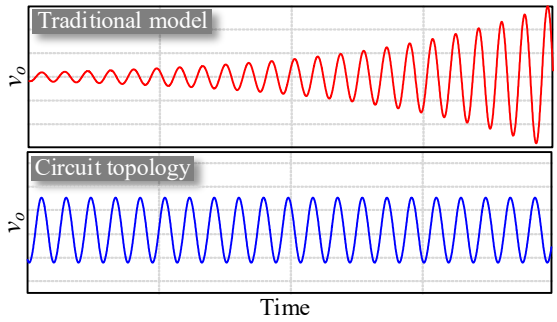

Fig. 3 The instability behaviors of the traditional model and circuit topology.

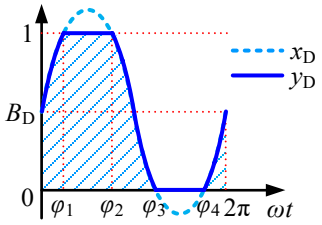

Fig. 4 Input-output relation of the controller saturation.

III. Exploration of the Limit Cycle Phenomenon by Describing Function Method

A. Describing Function Method

To unfold the features of the limit cycle, the forms of x_D and y_D should be examined in advance. Due to the presence of the output LC filter, the ac component of x_D can be approximated as the first-order harmonic. Thus, x_D is expressed as

$$x_D = B_D + A_D \sin \omega_1 t \tag{5}$$

where ω_1 is the oscillating frequency; B_D and A_D are the dc bias and the first-order harmonic amplitude of x_D, respectively.

To linearize sat(·) shown in (4), y_D is approximated by means of the describing function method. As shown in Fig. 5, this method divides the saturation function into two parts, denoted as $S_B(A_D, B_D)$ and $S_A(A_D, B_D)$, responsible for the transmission of dc and ac components, respectively. Thus, the approximation of y_D is expressed as

$$y_D \approx \underbrace{B_D \cdot S_B(A_D, B_D)}_{Y_B} + \underbrace{A_D \cdot S_A(A_D, B_D)}_{Y_A} \sin \omega_1 t \tag{6}$$

where Y_B and Y_A are the dc bias and the first-order harmonic amplitude of the approximated y_D, respectively; the expressions of $S_B(A_D, B_D)$ and $S_A(A_D, B_D)$ are given as (7) at the bottom of this page.

B. Underlying Mechanism of the Limit Cycle

Note that A_D will increase as instability occurs, only $S_A(A_D, B_D)$ is concerned to unfold the generation of the

$$S_B(A_D, B_D) = \frac{1}{2\pi B_D}\int_0^{2\pi} \mathrm{sat}(x_D)\, d\omega t = \frac{1}{\pi}\left[\frac{\pi}{2B_D} + \arcsin\frac{B_D}{A_D} - \frac{1-B_D}{B_D}\arcsin\frac{1-B_D}{A_D} + \frac{A_D}{B_D}\left(\sqrt{1-\left(\frac{B_D}{A_D}\right)^2} - \sqrt{1-\left(\frac{1-B_D}{A_D}\right)^2}\right)\right] \tag{7a}$$

$$S_A(A_D, B_D) = \frac{1}{\pi A_D}\int_0^{2\pi} \mathrm{sat}(x_D)\sin\omega_1 t\, d\omega t = \frac{1}{\pi}\left[\arcsin\frac{B_D}{A_D} + \frac{B_D}{A_D}\sqrt{1-\left(\frac{B_D}{A_D}\right)^2} + \arcsin\frac{1-B_D}{A_D} + \frac{1-B_D}{A_D}\sqrt{1-\left(\frac{1-B_D}{A_D}\right)^2}\right]. \tag{7b}$$

limit cycle. Recalling Fig. 5(b), intentionally separating the $T_p(s)|_{s=j\omega}$ and $S_A(A_D, B_D)$, the system characteristic equation is expressed as

$$1+T_p(j\omega)\cdot S_A(A_D,B_D)=0 \Rightarrow T_p(j\omega)=-1/S_A(A_D,B_D). \quad (8)$$

Comparing (3) with (8), the critically stable condition is no longer determined by the fixed critically stable point $(-1, j0)$, but by a trajectory $-1/S_A(A_D, B_D)$ varying with A_D and B_D, which is called the GNC.

As GNC claimed, a stable system should ensure the number of its closed-loop RHP pole $Z = N + P = 0$, where N and P are the numbers of the Nyquist contour of $T_p(j\omega)$ clockwise encircling $-1/S_A(A_D, B_D)$ and the open-loop RHP pole, respectively. Recalling (1), $P = 0$ is always satisfied. Fig. 6 shows the possible positions of $-1/S_A(A_D, B_D)$ relative to $T_p(j\omega)$, where the arrow of $-1/S_A(A_D, B_D)$ indicates its motion direction as A_D increases. The system dynamic behaviors are analyzed as follows.

1) Encircled [see Fig. 6(a)]

$T_p(j\omega)$ is always clockwise encircling $-1/S_A(A_D, B_D)$, i.e, $Z = N = 1$. The system is unstable and its output will diverge unboundedly.

2) Encircled [see Fig. 6(b)]

There is no encirclement of $-1/S_A(A_D, B_D)$, i.e., $Z = N = 0$. The system operates stably.

3) Partly Encircled [see Fig. 6(c)]

As shown, $T_p(j\omega)$ and $-1/S_A(A_D, B_D)$ intersect at S_0. Initially, suppose the operation point locates at S_1, resulting in $Z = N = 1$. Accordingly, instability will occur, and the first-order harmonic amplitude A_D will continuously increase, leading the operation point to depart from S_1 toward the intersection point S_0. Once it passes S_0, the operation point is no longer encircled by $T_p(j\omega)$, resulting in $Z = N = 0$. The system regains stability, leading the operating point to move toward S_0.

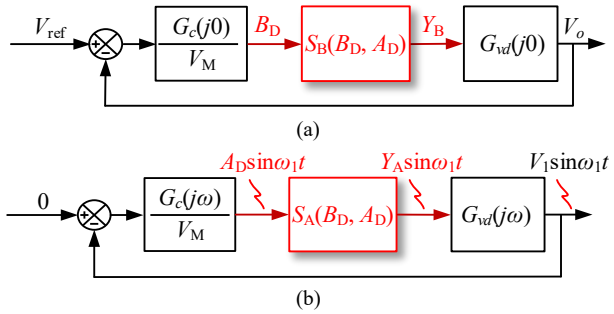

Fig. 5 Linearized block diagrams for describing function. method. (a) Dc component. (b) Ac component.

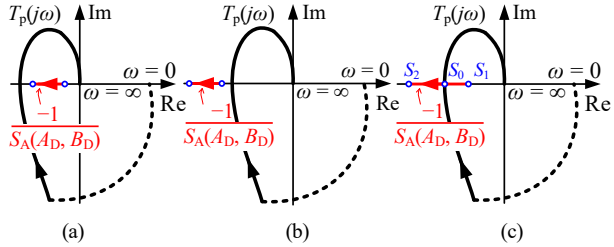

Fig. 6 Different positions of $-1/S_A(A_D, B_D)$ relative to $T_p(j\omega)$. (a) Encircled. (b) Not encircled. (c) Partly encircled.

Iteratively, it will finally stay at S_0 and behaves as an oscillation with constant amplitude and frequency, that is, the limit cycle.

C. Calculation of the Oscillating Frequency and Amplitude

The above discussion reveals the property of the limit cycle. Next, the oscillating frequency and amplitude of the output voltage, i.e., ω_1 and V_1 will be calculated.

Recalling Fig. 6(c), the operation point will eventually stay at the intersection S_0, where the coordinate of S_0 is denoted as $(-1/S_{A0}(A_{D0}, B_{D0}), j0)$. Substituting $s = j\omega_1$ into (1) and combining with the coordinate of S_0, yields

$$\omega_1 = 2\pi f_1 = \sqrt{\frac{1}{L\left[C - K_P/(K_I R_{Ld})\right]}} \quad (9a)$$

$$S_{A0}(A_{D0}, B_{D0}) = \frac{V_M}{V_{in}(K_I R_{Ld} C - K_P)}. \quad (9b)$$

Note that the limit cycle occurs when there exists a numerical solution to Eq. (8a). Meanwhile, recall that the controller saturation limit y_D within [0, 1], that is, $S_{A0}(A_{D0}, B_{D0})$ in (9b) should always be less than 1. Thus, the condition for the limit cycle should satisfy

$$\begin{cases} C - K_P/(K_I R_{Ld}) > 0 \\ V_M < V_{in}(K_I R_{Ld} C - K_P) \end{cases} \Rightarrow R_{Ld} > (V_M/V_{in} + K_P)/(K_I C) \quad (10)$$

Eq. (10) points out that the limit cycle phenomenon tends to occur under light load conditions.

From (9a), the oscillating frequency f_1 can be calculated. Next, how to derive the oscillating amplitude of the output voltage, V_1, will be presented.

Recalling Fig. 5, v_o can be expressed as

$$v_o = V_o + V_1 \cdot \sin\omega_1 t \quad (11)$$

where

$$V_o = \underbrace{B_{D0}\cdot S_{B0}(A_{D0}, B_{D0})}_{Y_{B0}} \cdot |G_{vd}(j0)| \quad (12a)$$

$$V_1 = \underbrace{A_{D0}\cdot S_{A0}(A_{D0}, B_{D0})}_{Y_{A0}} \cdot |G_{vd}(j\omega_1)| \quad (12b)$$

where V_o is the steady-state value of v_o; Y_{B0} and Y_{A0} are the quantitative values of Y_B and Y_A at S_0, respectively.

Recalling (1), Substituting $s = j\omega$ into (1), yields

$$|G_{vd}(j\omega)| = V_{in}/\sqrt{(1-LC\omega^2)^2 + (\omega L/R_{Ld})^2}. \quad (13)$$

Considering the gain of the PI regulator at 0 Hz is infinity, V_o should always track its reference, i.e., $V_o = V_{ref}$. Substituting $s = j0$ into (13) and combining with (12), yields

$$Y_{B0} = B_{D0}\cdot S_{B0}(A_{D0}, B_{D0}) = V_{ref}/G_{vd}(j0) = V_{ref}/V_{in}. \quad (14)$$

According to (12b), V_1 is determined by $|G_{vd}(j\omega_1)|$ and Y_{A0}. Based on the above formulas, they can be calculated by following the flowchart in Fig. 7. As shown, $|G_{vd}(j\omega_1)|$ can be easily obtained by substituting the given prototype parameters into (9a) and (13) in sequence. According to (7b) and (12b), to calculate Y_{A0}, the quantitative values of A_{D0} and B_{D0} should be determined in advance. For this purpose, substituting the given prototype parameters into (9b) and (14), the quantitative values of $S_{A0}(A_{D0}, B_{D0})$ and Y_{B0} can be calculated. Substituting $A_D = A_{D0}$, $B_D = B_{D0}$

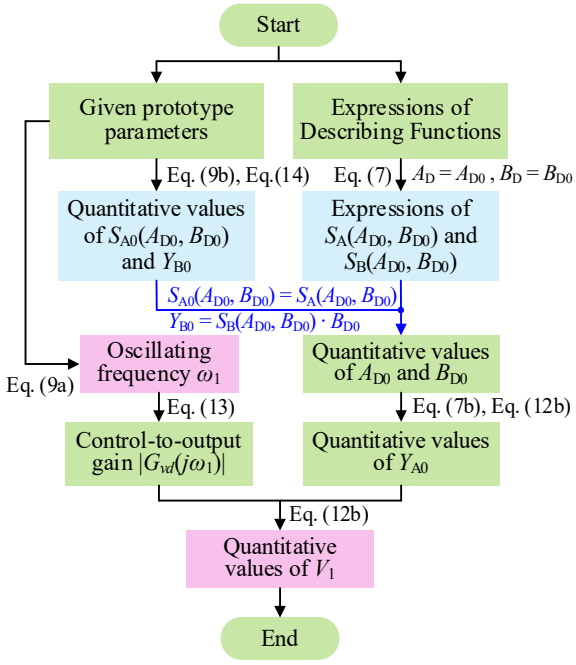

Fig. 7 Flowchart of the calculation process.

into (7) and (14) in sequence, then combining them with the obtained $S_{A0}(A_{D0}, B_{D0})$ and Y_{B0}, the quantitative values of A_{D0} and B_{D0} can be determined.

IV. Verification

A. Simulation Results

The synchronous buck converter model was established in MATLAB/Simulink with the main parameters given in Table I to verify the condition for the generation of the limit cycle and the related calculation accuracy of the oscillation.

Firstly, the occurrence condition of the limit cycle is examined. Substituting the parameters as listed in Table I into (10), the limit cycle will occur when $R_{Ld} > 4.9\ \Omega$. In view of this, R_{Ld} is set to 3 Ω and 6 Ω for verification. Fig. 8 depicts the Nyquist diagram of $T_p(j\omega)$ and the trajectory of $-1/S_A(A_D, B_D)$ under the load variation. As shown, there is no intersection between $T_p(j\omega)$ and $-1/S_A(A_D, B_D)$ when $R_{Ld} = 3\ \Omega$, whereas an intersection with the coordinate of $(-1.27, j0)$ exists when $R_{Ld} = 6\ \Omega$. Theoretically, the stable state and the limit cycle should occur, respectively. As shown in Fig. 9(a), when R_{Ld} is set to 3 Ω, the system is stable, and the output voltage v_o tracks its reference of 12 V. As shown in Fig. 9(b), when R_{Ld} is set to 6 Ω, limit cycle phenomenon occurs, where the output voltage v_o and the inductive current i_L oscillate with constant frequency and amplitude. Clearly, the simulation results match well with the theoretical expectations.

Secondly, the correctness of the calculation for the oscillating frequency f_1 and amplitude V_1 is verified. For the limit cycle, according to the flowchart as shown in Fig, 7, the oscillating frequency and amplitude can be calculated as 2088 Hz and 28.05 V, respectively. Based on the Fast Fourier Transform (FFT) result in Fig. 9(c), the simulation results of f_1 and V_1 are measured as 2088 Hz and 28.10 V, respectively. Accordingly, the simulation results are in agreement with the theoretical calculation results.

TABLE I
Main Parameters

Parameter	Symbol	Value
Input voltage	V_{in}	24 V
Amplitude of sawtooth signal	V_M	3.9 V
Reference voltage	V_{ref}	12 V
Inductor	L	220 μH
Capacitor	C	30 μF
PI regulator	$G_c(s)$	0.028+1300/s
Switching frequency	f_s	100 kHz

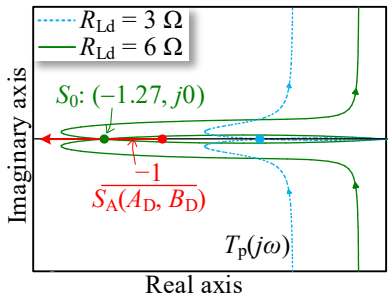

Fig. 8 Nyquist diagram under load variation.

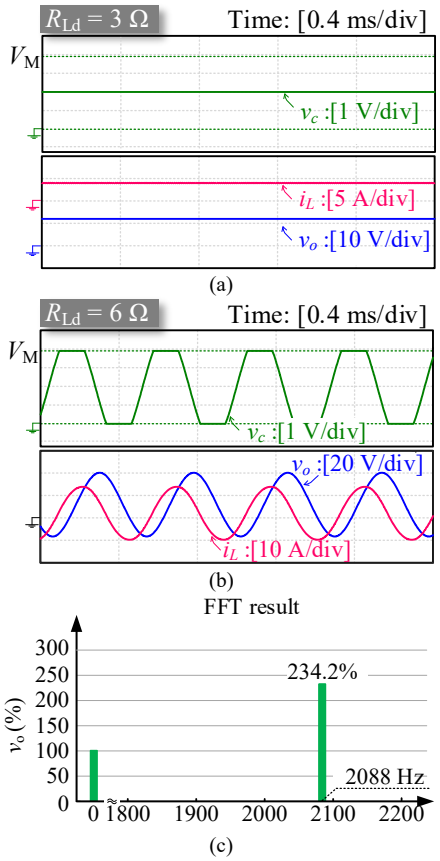

Fig. 9 simulation results. (a) Waveforms under R_{Ld} = 3 Ω. (b) Waveforms under R_{Ld} = 6 Ω. (c) FFT result of v_o under R_{Ld} = 6 Ω.

B. Experimental Results

According to the parameters listed in Table I, the experimental setup as shown in Fig. 10(a) was constructed to verify the correctness of the above theoretical analysis. The synchronous buck converter

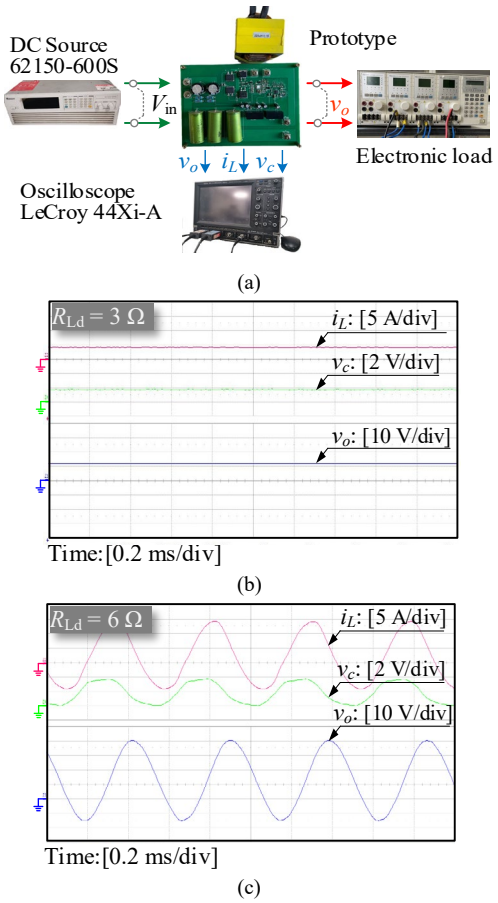

Fig. 10 Experimental setup and the recorded results. (a) Configuration. (b) Waveforms under R_{Ld} = 3 Ω. (c) Waveforms under R_{Ld} = 6 Ω.

prototype was implemented with a P-Channel MOSFET (SQM40P10-40L), an N-Channel MOSFET (SQR40N10 -25), and three film capacitors (MKP1839) in parallel. The control algorithm was implemented in a TI integrated circuit (TPS40061). The experimental results as shown in Fig. 10 are recorded by the oscilloscope (LeCroy 44Xi-A).

To verify the occurrence condition of the limit cycle, Fig. 10(b) and (c) show the waveforms of v_o and i_L when R_{Ld} is set to 3 Ω and 6 Ω, respectively. As shown, the former operates stably, whereas the latter presents as a limit cycle. Besides, the experimental results of f_1 and V_1 are measured as 2090 Hz and 28.01 V under R_{Ld} = 6 Ω. Clearly, the above experimental results are also consistent with the theoretical results.

V. Conclusions

In this paper, an accurate model with nonlinear controller saturation is established to explore the limit cycle phenomenon in synchronous buck converters. The underlying mechanism and the occurrence condition of the limit cycle are revealed, and the prediction of the oscillating frequency and amplitude is also presented. The simulation and the experimental results are in agreement with the theoretical expectations. This work can be further extended to other complex systems, such as the cascade converters, and their limit cycle phenomena can also be investigated.

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