Experimental Demonstration of a 2.2kW Active-Clamp Converter for High-Current Wide-Voltage-Transfer Ratio Applications

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Keywords

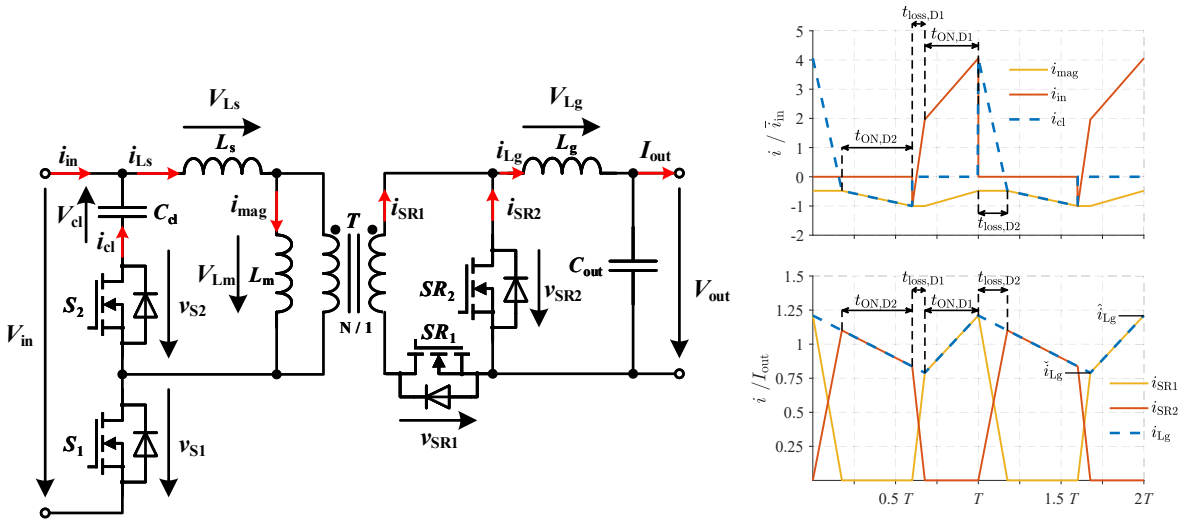
≪High frequency power converter≫, ≪Switched-mode power supply≫, ≪DC-DC converter≫, ≪Battery charger≫, ≪Cooling≫.

Abstract

Active-clamp forward converters are typically not applied for converters with power ratings larger than 500 W as power as the power transfer between primary and secondary is discontinuous leading to large magnetic components. This paper, however, proves that silicon carbide (SiC) devices enable this topology as a well-suitable topology for a wide voltage-transfer ratio due to the low switching losses allowing high switching frequencies reducing the size of the magnetic components. A laboratory prototype is designed using a very precise model. It employs SiC MOSFETs of 900 V for the primary and Si synchronous rectifiers of 100 V. The semiconductors are cooled with cost-efficient copper inlays, which effectiveness is demonstrated through a thermal FEM simulation. The developed prototype achieves a maximum efficiency of 95% while maintaining an efficiency above 92% for almost the entire operating region. The high efficiency and the power density of approximately 2 kW/l confirm the proposed concept. Finally, the converter is benchmarked to two LLC resonant converters (Si, SiC) and the prototype is used to verify a highly accurate steady-state model showing errors below 1 %.

1 Introduction

Automotive on-board DC-DC converters are the connecting link between the traction battery with a nominal voltage of around 400 V and the auxiliary battery with a nominal voltage of 12 V. The actual voltages, however, largely depend on the state-of-charge of the batteries. The voltages may vary by a factor of two or even more (200-420 V, 8-16 V) such that the connecting converter needs to cover a very wide voltage-transfer ratio. Earlier publications showed that traditional topologies (LLC, phase-shifted full bridge) suffer from the wide-voltage transfer ratio and pointed out that the active-clamp forward converter (ACFC) and the LLC with operating mode variations are suitable topologies for this application [1, 2]. In contrast to the LLC resonant converter, the ACFC only employs two primary switches making it a cost-effective solution. Typically, however, the ACFC is not used for such large output powers as energy is only transferred once per period to the secondary side making it a single-pulse topology. This results in a larger transformer and a large output inductor L_g compared to other topologies.



(a) Circuit diagram (b) Current shapes

Fig. 1: Circuit diagram and current shapes of the active-clamp forward converter (ACFC)

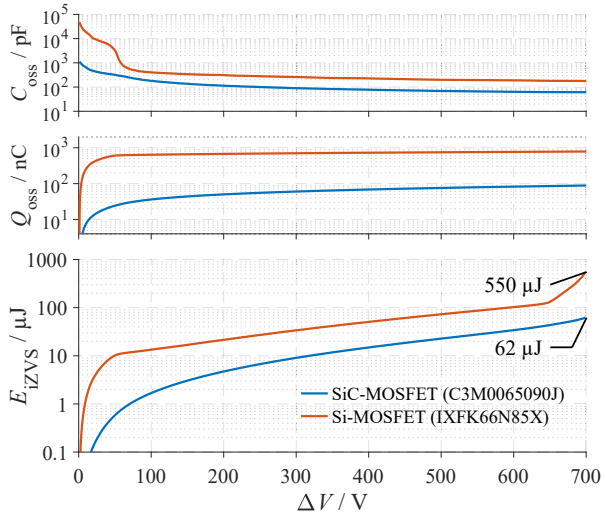


Fig. 2: Advantage of SiC semiconductors over Si semiconductors. The output capacitance C_{oss}, output charge Q_{oss} and incomplete ZVS lossses E_{iZVS} are significantly smaller.

The topology of the ACFC offers the potential of zero-voltage switching (ZVS) for both switches as the turn-off current of both switches is positive (cf. Figure 1b). The large transferred current results in a large turn-off current for the main switch S_1 easily enabling ZVS for the auxiliary switch S_2. The lower turn-off current of the auxiliary switch can be utilized to achieve ZVS for main switch S_1. Due to the significantly smaller current, only a small energy is available to achieve ZVS. However, due to the outstanding performance of wide-bandgap semiconductors, only a small energy is necessary to achieve ZVS and the losses associated with the turn-on at a residual voltage [3] are much smaller (cf. Figure 2). In preceding work [2], the ACFC was analytically benchmarked vs. the LLC resonant converter and phase-shifted full bridge showing that the topology is an attractive alternative as it yields in low transformer currents and low primary switch currents. This paper, consequently, presents the design of an active-clamp forward converter as an on-board DC-DC converter. The analysis and parameter selection of the converter is presented in Section II, the evaluation is described in Section III before the paper is concluded.

2 Converter Design

When designing the ACFC, the system is conventionally modeled without the series inductance L_s and with large output and magnetizing inductances (L_g and L_m respectively). This yields block-shaped currents and a neglection of the duty-cycle loss intervals $t_{\text{loss,D1}}$ and $t_{\text{loss,D2}}$ [4–7]. This overestimates the length of the demagnetizing interval $t_{\text{ON,D2}}$. With this assumption, the clamp capacitor voltage $V_{\text{cl,com}}$ is commonly calculated as

$$V_{\text{cl,com}} = V_{\text{in}} \frac{D}{1-D} \tag{1}$$

where $D = \frac{NV_{\text{out}}}{V_{\text{in}}}$. However, as the demagnetizing interval $t_{\text{ON,D2}}$ is shortened by the duty-cycle loss intervals $t_{\text{loss,D1}}$ and $t_{\text{loss,D2}}$ the clamp capacitor voltage V_{cl} becomes much larger resulting in errors of more than 60 % [1, 8]. Consequently, [1, 8] described the detailed and accurate modeling procedure of an ACFC operating in continuous conduction mode (CCM). While this model was only verified with simulation results, this work will also demonstrate its accuracy by verifying it with experimental results. Consequently, this model will be used during the following design procedure. However, since this model only described the analytical derivation yielding a complex analytical expression, the next section shortly describes the analytical derivation and expression of a simplified calculation of the clamp capacitor voltage, which still gives good results.

2.1 A simplified model of the clamp-capacitor voltage V_{cl}

The preceding simplified modeling methods [4–7] assumed an ideal transformer such that the transformed input voltage appears at the secondary side of the transformer during the energy-transfer interval $t_{\text{ON,D1}}$ (cf. Figure 1b). However, this is not the case since a significant portion of the input voltage may be applied to the series inductance L_s. Thus, the output inductor voltage is reduced and $V_{\text{Lg,D1}}$ must be accurately calculated by solving the following four equations [1, 8].

$$\begin{aligned} V_{\text{in}} &= V_{\text{Ls,D1}} + V_{\text{Lm,D1}} \\ V_{\text{Lm,D1}} &= V'_{\text{Lg,D1}} + V'_{\text{out}} + V'_{\text{D}} \\ \Delta i_{\text{Ls}} &= \Delta i_{\text{Lm}} + \Delta i'_{\text{Lg}} \\ \frac{V_{\text{Ls,D1}}}{L_s} &= \frac{V_{\text{Lm,D1}}}{L_m} + \frac{V'_{\text{Lg,D1}}}{L'_g} \end{aligned} \tag{2}$$

For $V_{\text{Lg,D1}}$ and $\widetilde{V}_{\text{out}} = V_{\text{out}} + V_{\text{D}} = V_{\text{out}} + V_{\text{d}} + R_{\text{d}} I_{\text{out}}$ (V_{d} is the forward voltage of the rectifier, R_{d} is the resistance of the rectifier), this yields

$$V_{\text{Lg,D1}} = -\frac{L_g N \left(-L_m V_{\text{in}} + N\widetilde{V}_{\text{out}}(L_s + L_m)\right)}{N^2 L_g (L_m + L_s) + L_m L_s} \tag{3}$$

Thus, the duty cycle $\widetilde{D}$ can be calculated as $\widetilde{D} = \frac{\widetilde{V}_{\text{out}}}{V_{\text{Lg,D1}} + \widetilde{V}_{\text{out}}}$. The duty-cycle loss intervals $t_{\text{loss,D1}}$ and $t_{\text{loss,D2}}$ (cf. Figure 1b) can be estimated as $t_{\text{loss,D1}} = \frac{I_{\text{out}} L_s}{N V_{\text{in}}}$ and $t_{\text{loss,D2}} = \frac{I_{\text{out}} L_s}{N V_{\text{cl}}}$. The voltage-time area of the voltage applied to the magnetizing inductance L_m during $t_{\text{ON,D1}}$ and $t_{\text{ON,D2}}$ must be equal:

$$V_{\text{cl}}(T - t_{\text{loss,D1}} - t_{\text{loss,D2}} - \widetilde{D}T) = V_{\text{in}} \widetilde{D} T. \tag{4}$$

In this equation, the voltage V_{in} is used for the magnetizing voltage V_{Lm} during $t_{\text{ON,D1}}$, even though the real voltage $V_{\text{Lm,D1}}$ can be accurately calculated by solving (2). This was done as it yields a slightly higher approximation of the clamp capacitor voltage to simplify the lengthy accurate calculation of the clamp capacitor voltage as it was done in the preceding work of [1, 8]. Equation (4) can be solved for the clamp capacitor voltage V_{cl} yielding

$$V_{\text{cl}} = -\frac{V_{\text{in}} (\sigma + NTV_{\text{in}} V_{\text{out}})}{\sigma - NTV_{\text{Lg,D1}} V_{\text{in}}} \tag{5}$$

with (3) and

$$\sigma = I_{\text{out}} L_s \left(V_{\text{Lg,D1}} + V_{\text{out}}\right) \tag{6}$$

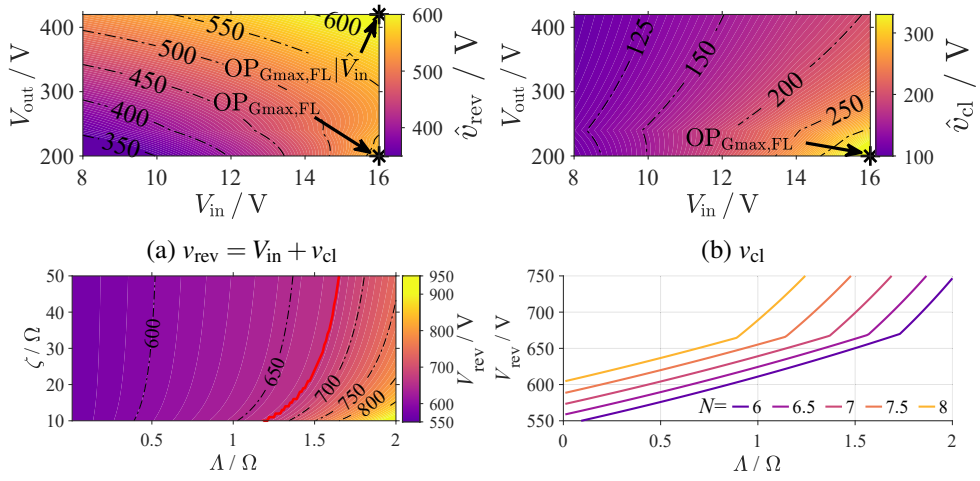
Table I: Operating points with the maximum component stress

Abbreviation	OP (V_{in} ,V_{out} ,I_{out})	component
$OP_{Gmax,FL}$	240 V, 14 V, 160 A	SR_1, S_1
$OP_{Gmax,FL}\|\hat{V}_{in}$	420 V, 16 V, 140 A	T, L_g, V_{rev}, V_{SR2}
$OP_{Gmin,FL}$	420 V, 8 V, 160 A	SR_2, S_2
$OP_{Gmax,DL}$	200 V, 16 V, 100 A	C_{cl}, V_{SR1}
OP_{Gnom}	345 V, 14 V, 64 A	SR_1, S_1

This calculation is much simpler than the calculation developed in [1]. The simplified model and the complex model of [1] are benchmarked in 3.3.

2.2 Definition of characteristic design operating points

The circuit is designed to run with an input voltage $V_{in} \in [200\,V, 420\,V]$ and an output voltage of $V_{out} \in [8\,V, 16\,V]$ at a maximum power of $P_{out} = 2.24\,kW$ and a maximum output current of $I_{out} = 160\,A$. For an input voltage smaller than $V_{in} = 240\,V$, the maximum output current is proportionally reduced from its maximum current at the operating output voltage to $I_{out} = 100\,A$ at $V_{in} = 200\,V$. This is the derated operating region. The maximum current stress of the primary and secondary semiconductors is fairly obvious. The forward synchronous rectifier SR_1 is most stressed at the operating point of $V_{in} = 240\,V$, $V_{out} = 14\,V$ as this is the operating point with the maximum current and duty cycle. The same also applies for S_1. For output voltages larger 14 V, the current is reduced due to the maximum power rating. For freewheeling synchronous rectifier SR_2 and the auxiliary switch, the operating point with the maximum stress is $V_{in} = 420\,V$, $V_{out} = 8\,V$ as this is the operating point with the smallest duty cycle. For the maximum reverse voltage of the primary semiconductors ($\hat{v}_{rev} = \hat{v}_{cl} + V_{in}$), two operating points need to be considered as depicted in Figure 3a. While the clamp capacitor voltage increases with increasing duty cycle (cf. Figure 3b) such that $OP_{Gmax,DL}$ is the operating point with the largest clamp capacitor voltage $\hat{v}_{cl}$, the increasing input voltage provokes a larger blocking voltages.



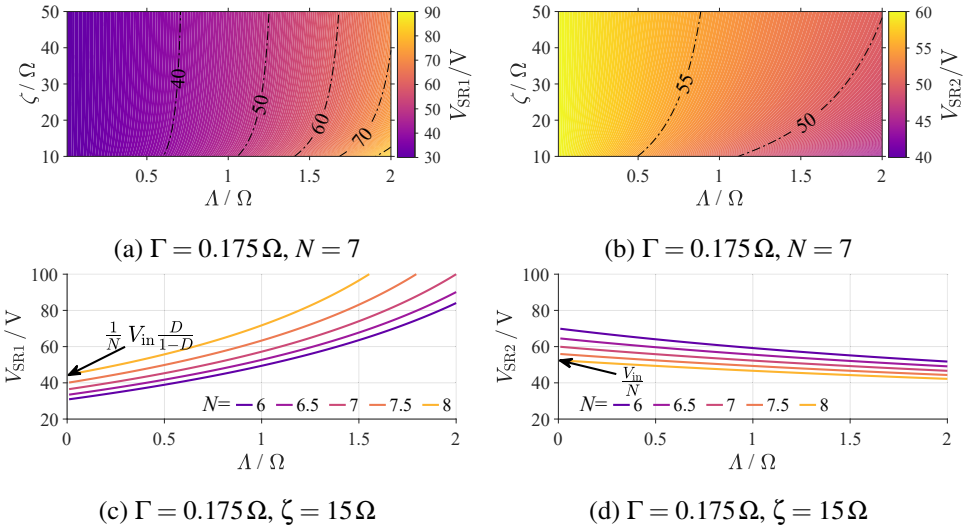
(a) $v_{rev} = V_{in} + v_{cl}$ (b) v_{cl}

(c) $\Gamma = 0.175\,\Omega$, $N = 7$ (d) $\Gamma = 0.175\,\Omega$, $\zeta = 15\,\Omega$

Fig. 3: Operating point dependent reverse voltage v_{rev} (a) and clamp capacitor voltage v_{cl} (b) for a sample set of parameters. Parameter-dependent reverse voltage v_{rev} for the dependency on Λ and ζ (c) and Λ and n (d). Depicted is the maximum for $OP_{Gmax,FL}|\hat{V}_{in}$ and $OP_{Gmax,DL}$.

2.3 Circuit parameter selection

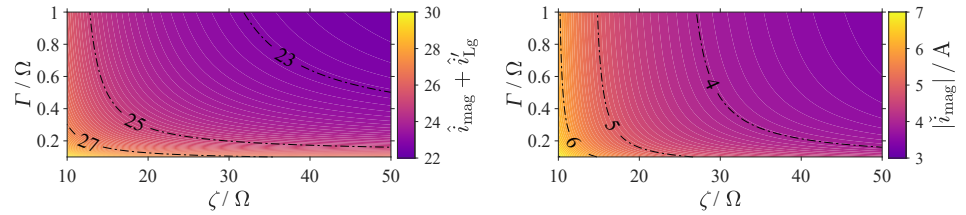
The definition of a suitable switching frequency is one of the most crucial steps in the design of a power electronic circuit. However, when comparing a set of designs, the calculated stress values only apply for a single switching frequency since the inductances scale anti-proportionally with the switching frequency [2, 9]. Thus, the following analysis normalizes the system parameters with the switching frequency such



(a) $\Gamma = 0.175\,\Omega$, $N = 7$ (b) $\Gamma = 0.175\,\Omega$, $N = 7$

(c) $\Gamma = 0.175\,\Omega$, $\zeta = 15\,\Omega$ (d) $\Gamma = 0.175\,\Omega$, $\zeta = 15\,\Omega$

Fig. 4: Parameter-dependent synchronous rectifier reverse voltage v_{SR1}, v_{SR2} for the dependency on Λ and ζ (a,b) and Λ and n (c,d). For (a,c), the operating point is Depiction as the maximum for $OP_{Gmax,DL}$ and $OP_{Gmax,DL}$; for (b,d), the operating point is $OP_{Gmax,FL}|\hat{V}_{in}$.



(a) (b)

Fig. 5: Parameter dependent turn-off current for the main switch S_1 (a) and auxiliary switch S_2 (b). For (a), the operating point is $OP_{Gmax,FL}$; for (b), it is $OP_{Gmin,FL}$.

that the frequency can be selected in a later step. To define switching frequency-independent system parameters, the following three variables are defined:

$$\begin{aligned} \zeta &= L_m f_{sw} \\ \Lambda &= L_s f_{sw} \\ \Gamma &= L_g f_{sw}. \end{aligned} \tag{7}$$

where ζ is a measure for the magnetizing inductance L_m, Λ for the series inductance L_s and Γ for the output inductance L_g. Through this normalization, current and voltage values can directly be analyzed. Figure 3c shows an analysis of the maximum reverse voltage in relation to the normalized system parameters. For system parameters in the upper left of the red line, the operating point with the maximum reverse voltage is $OP_{Gmax,FL}|\hat{V}_{in,max}$, for system parameters in the lower right, it is $OP_{Gmax,DL}$. The reverse voltage increases significantly with a larger series inductance L_s (Λ). The maximum reverse voltage can be reduced by a definition of a suitable transformation ratio N (cf. Figure 3d). To limit the reverse voltage of the primary semiconductors, N and L_s must be chosen carefully. As the clamp capacitor voltage also influences the blocking voltage of the secondary semiconductors, this choice also influences the design of the secondary semiconductors. Figure 4a and Figure 4c show the blocking voltage of the synchronous rectifier SR_1. For $\Lambda \to 0$, the blocking voltage can be calculated through (1). However, similar to the calculation of the clamp capacitor voltage, the series inductance has a severe impact on the blocking voltage and may lead to a significant increase whereas an increased series inductance, in turn, results in a reduced blocking voltage for the freewheeling synchronous rectifier SR_2 (cf. Figure 4a, Figure 4c).

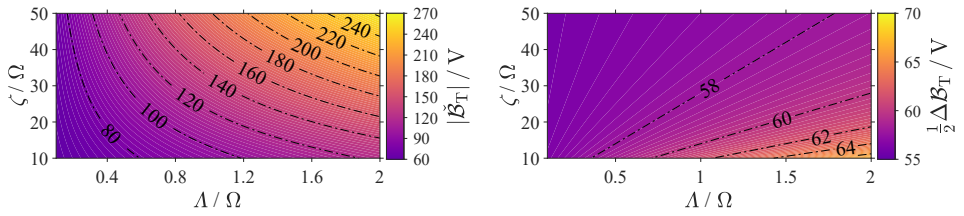
To accurately design the transformer, the influence of the magnetizing current must be considered. For this analysis, it is considered that the series inductance L_s is integrated in the transformer such that the flux density can be calculated as [10]

$$b(t) = \frac{(L_\mathrm{m} + L_\mathrm{s}) i_\mathrm{mag}}{N_\mathrm{prim} A_\mathrm{eff}}. \tag{8}$$

To keep the analysis frequency-independent, the stress value $\mathcal{B}_\mathrm{T}$ is introduced, which is of the unit *volts*.

$$b(t) = \frac{\overbrace{(\zeta + \Lambda) i_\mathrm{mag}}^{\mathcal{B}_\mathrm{T}(t)}}{f_\mathrm{sw} N_\mathrm{prim} A_\mathrm{eff}}. \tag{9}$$

The stress variable $\mathcal{B}_\mathrm{T}$ is analyzed to investigate the flux ripple of the transformer. Of special interest is the minimum transformer flux $\check{b}_\mathrm{min}$ to avoid saturation, which is influenced by the system parameters through the minimum magnetizing current. To investigate the minimum flux, the normalized stress value $\check{\mathcal{B}}_\mathrm{T}$ is displayed in Figure 6a whereas the flux ripple is investigated through $\frac{1}{2}\Delta\mathcal{B}_\mathrm{T}$ in Figure 6b. The analysis shows that while the flux ripple is barely influenced through the design of the inductances, the minimum magnetizing current may significantly influence the minimum transformer flux. For a large magnetizing inductance L_m (corresponding with a large ζ), and a large series inductance L_s (corresponding with a large Λ), the minimum magnetizing current and thus the minimum transformer flux becomes very large. Eventually it is about four times half the magnetizing current or flux ripple ($\check{\mathcal{B}}_\mathrm{T} \approx 4 \cdot \frac{1}{2}\Delta\mathcal{B}_\mathrm{T}$) such that for those designs, the transformer cross section A_eff must be designed for significantly larger surface areas.



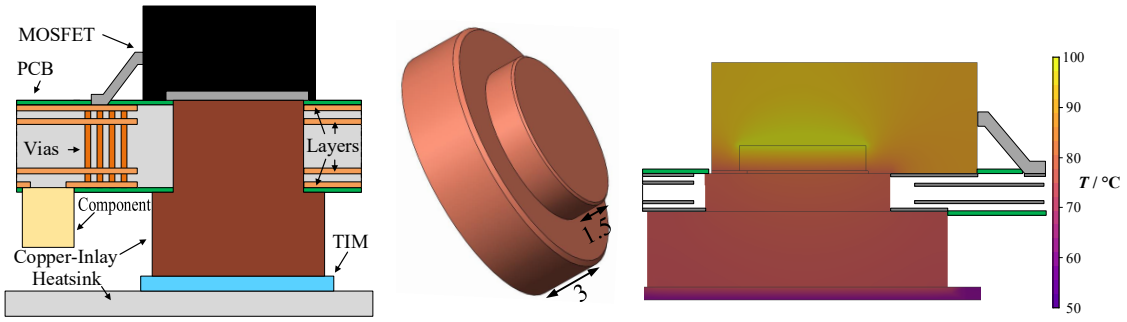
(a) (b)

Fig. 6: Parameter dependent minimum magnetizing flux $\check{\mathcal{B}}_\mathrm{T}$ (a) and flux ripple $\frac{1}{2}\Delta\mathcal{B}_\mathrm{T}$ (b) with its dependency on Λ and ζ. The operating point is $\mathrm{OP}_\mathrm{Gmax,FL}|\hat{V}_\mathrm{in}$.

2.4 ZVS consideration

The conventional ACFC operation can be used to achieve ZVS for both MOSFETs. The main switch S_1 is turned off at a large positive transformer current value i_Ls. During the turn-on of the auxiliary switch S_2, the current reverses (cf. Figure 1b) such that at the turn-off of this semiconductor, the transformer current is negative. With a proper design of the magnetizing inductance and the series inductance, both switches can be switched at zero voltage (ZVS). For reasons of brevity, only the switching transition of the main switch S_1 will be considered since the absolute value of the turn-off current of the auxiliary switch $|\check{i}_\mathrm{mag}|$ is much lower compared to the turn-off value of the main switch $|\hat{i}_\mathrm{mag} + \hat{i}'_\mathrm{Lg}|$. Furthermore, it is assumed that $\check{i}_\mathrm{mag} + \frac{\check{i}_\mathrm{Lg}}{N} \geq 0$. If this condition is not fulfilled, i_Ls is negative at the end of $t_\mathrm{loss,D1}$ (cf. Figure 1b) such that ZVS can be achieved more easily.

When the auxiliary switch is turned-off, the output capacitance of S_1 is discharged while the one of S_2 is charged. The magnetizing inductance L_m does not participate in the transition as it is clamped to the transformed secondary-side blocking voltage v'_SR1. At the beginning of the transition, the energy available for ZVS is $E_\mathrm{Ls} = \frac{1}{2} L_\mathrm{s} \check{i}^2_\mathrm{mag}$. The energy can, therefore, be influenced by the minimum magnetizing current value through the design of L_m and the series inductance L_s. While for other topologies, the ZVS condition can directly be calculated [3], this is not possible for the ACFC since three semiconductors (S_1, S_2 and SR_1) are involved during this condition. While preceding work [1] neglected the influence of the



(a) Thermal concept (b) CAD drawing of inlay (in mm) (c) Thermal FEM simulation (heatsink at 60 °C)

Fig. 7: Employed cooling concept (a) for the primary and secondary semiconductors. A copper inlay is soldered into the PCB. Construction drawing of the inlay (b) and FEM thermal simulation of the inlay (c).

output capacitance of the synchronous rectifier, this results in large errors. Thus, computer simulations that considered the nonlinear output capacitance of the primary and secondary semiconductors were used to design the circuit for ZVS in this work.

2.5 Definition of the system parameters

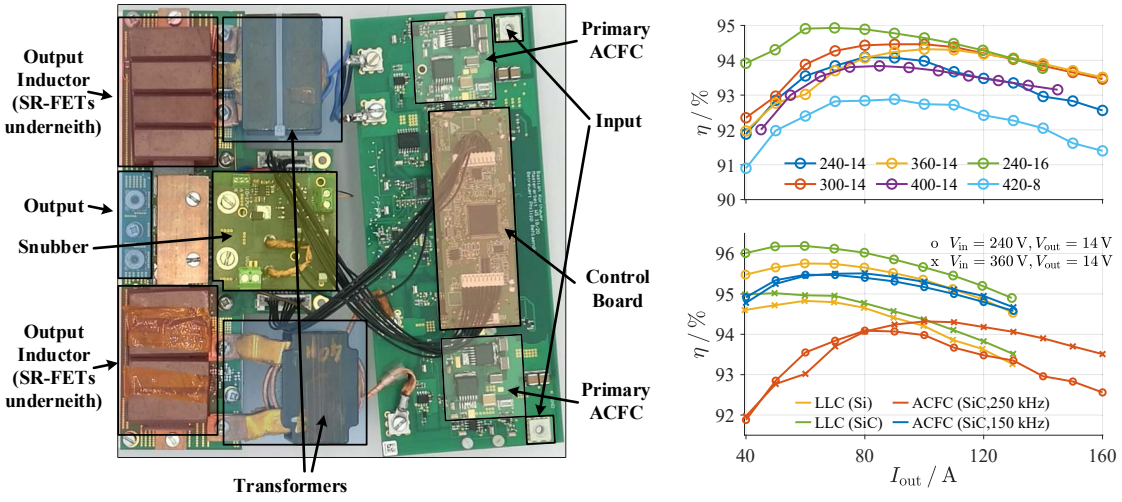
From the above analysis, the inductance values were defined as follows: $\Lambda = 0.75\,\Omega$, $\Gamma = 0.175\,\Omega$ and $\zeta = 11.25\,\Omega$. While this does result in increased turn-off currents, the influence on the design of the transformer and reverse voltage are kept low. For the main switch S_1, the semiconductor *C3M0065090J* (Cree 900 V, 65 mΩ) was selected, for the auxiliary MOSFET, the switch *C3M0120090J* (Cree 900 V, 120 mΩ) was chosen. Both are bottom-cooled SMD components. The cooling concept will be discussed in Section 2.6. The secondary semiconductors are two parallel MOSFETs of type *IAUT300N10S5N015* (Infineon Optimos 100 V, 1.5 mΩ) for SR_1 and SR_2. The switching frequency was set to 250 kHz to achieve a balance of small magnetic components and switching losses. With the definition of the switching frequency, the transformer was build up with a 7:1 turns ratio consisting of seven primary litz wire windings, three parallel copper sheet windings of 500 µm thickness and the transformer core ER54/38/20.

2.6 Cooling concept

To dissipate the heat of SMD semiconductors, a number of different methods has been used in the past [11]. By introducing thermal vias, the heat can be dissipated through the PCB vias connecting the top and bottom layer [12–15]. However, the possible heat dissipation is low resulting in a large thermal resistance. A better heat dissipation can be achieved through pedestals, where a piece of copper is placed between the top and bottom layer [11, 16, 17]. Similarly, it is also possible to insert a piece of ceramic (AIN) between the top and bottom layer for a reduced thermal resistance [15]. While these methods allow the application of a multi-layer PCB, the insertion of copper or a piece of ceramic is costly. Another possibility is the use of an insulated metal substrate [18–21] where the heat dissipation is very good but the layer number is limited to two. However, the heat dissipation is very good. In this work, the heat dissipation is achieved through a thermal inlay, which can be placed as an SMD component. Figure 7a shows the setup. The inlay is placed into the PCB and connected by solder to the sides. The component is placed on the other side on the top layer. A thermal interface material (TIM) is placed between the copper inlay and the heatsink to achieve the required isolation. A construction drawing of the inlay is depicted in Figure 7b. A FEM simulation is depicted in Figure 7c for a power dissipation of 20 W and a heatsink temperature of 60 °C.

3 Evaluation

The developed dual-rail prototype is depicted in Figure 8a. The dimensions of the prototype for two parallel ACFCs are (width×length×height) 193 mm × 28 mm × 210 mm without the aluminum chassis



(a) Prototype

(b) Efficiencies

Fig. 8: (a) Developed dual rail 4.48 kW (2×2.24 kW) ACFC prototype and (b) measured efficiencies.

and the transformer as the largest component. With the designed chassis the dimensions are 220 mm × 43 mm × 235 mm yielding in a power density of about 2 kW/l considering the maximum transferred power of 2×160 A·14 V = 4.48 kW.

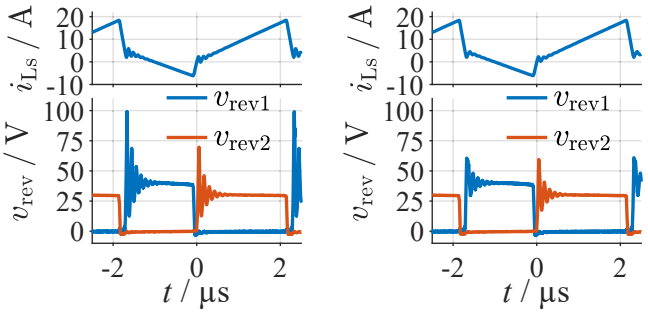
The right side of the prototype shows the primary PCB with the two times two primary semiconductors and the control board in the center. The transformers are depicted in the center with the 7 : 1 transformer on the bottom and the 15 : 2 transformer on the top. Between the transformers is the snubber circuit, which will be addressed in section 3.1. The left side shows the secondary PCB with the output inductor, which is assembled as a ferrite around a busbar. The synchronous rectifiers are placed below this ferrite.

3.1 Secondary semiconductor overshoot reduction

While the primary SiC MOSFETs are characterized by their small die area with a small output capacitance, the secondary rectifier MOSFETs are made of silicon, which results in a large output capacitance. In operation, this capacitance resonates with the series inductance of the transformer. Since the output capacitance is highly non-linear, the resulting overshoot may surpass twice the blocking voltage [22]. An exemplary shape of the secondary reverse voltages is depicted in Figure 9a. In preceding works, it was shown that the high energy of the oscillation prevents the application of a traditional *RC*(*D*) snubber and that a regenerative snubber must be employed. The analysis and design of this snubber is covered in [22]. The employed solution uses a buck converter that controls the clamping voltage of the snubber, which is connected to the output. An exemplary operation with the employed snubber is depicted in Figure 9b. The overvoltages are clamped by the snubber voltage, which is controlled to about 60 V. A nominal operation could not be achieved without the developed snubber. Only by employing the clamping snubber, an operation at higher input voltages and output loads is possible.

3.2 Stationary results

The developed converter achieves a top efficiency of about 95 %. Figure 8b (top) shows the measured efficiencies for different operating points over the output current. Since the high core losses are almost load independent, the top efficiency is limited. However, for increased output currents, the efficiency drop is quite limited and the converter achieves similar efficiencies for different operating points. To address the high core losses, the converter was modified to a 15:1 transformer (depicted in Figure 8a, top) with a magnetizing inductance of 105 µH and an increased output inductance of 1.5 µH, which was operated at 150 kHz (the converter is operated up to an output current of 130 A). The efficiencies are compared with the previous described ACFC and an LLC converter (with Si and SiC MOSFETs) for the same application in Figure 8b. The design of the resonant tank of the LLC converter with Si semiconductors has previously been covered in [23, 24]; the LLC converter with SiC semiconductors

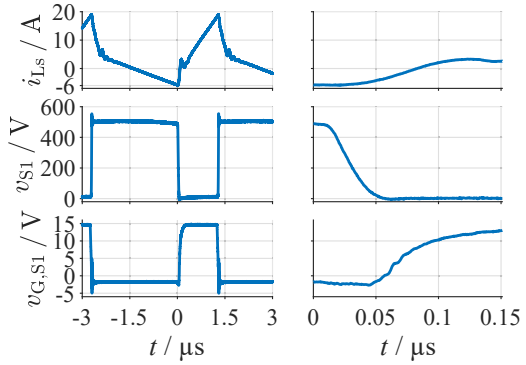


(a) Without snubber (b) With snubber

Fig. 9: Synchronous rectifier reverse voltages; (a) operation without snubber, (b) operation with employed snubber (snubber voltage at 60 V).

C3M0060065J (Cree 650 V, 60 mΩ) employs the same resonant tank compared to the LLC converter with Si MOSFETs *IPW65R080CFDA* (Infineon super junction 650 V, 80 mΩ). The development of the SiC converter was described in [25]. Both LLC resonant converters are operated in a number of different operating modes to cover the wide voltage-transfer ratio, whereas the operating concept of the ACFC is much simpler. By considering the efficiency comparison of Figure 8b (bottom), it is evident that the efficiency of the LLC resonant converters reduces significantly for smaller voltage-transfer ratios (360 V to 14 V) whereas for an operation near resonance (240 V to 14 V), the efficiency is very high. Compared to the LLC resonant converter, the ACFC offers relatively stable efficiencies, independently from the operating point, which are also relatively stable over the output load.

It has also been tested whether the converter achieves ZVS for the nominal operating point at ($V_{in} = 345\,V, V_{out} = 14\,V, I_{out} = 64\,A$). Figure 10a shows the nominal operation with the drain-source v_{S1} and gate voltage $v_{G,S1}$ of the main switch S_1 and the primary transformer current i_{Ls}. Figure 10b shows a zoom to the switching transient. It is evident that ZVS was achieved and that the transformer current is still negative when the drain-source voltage v_{S1} reaches zero.

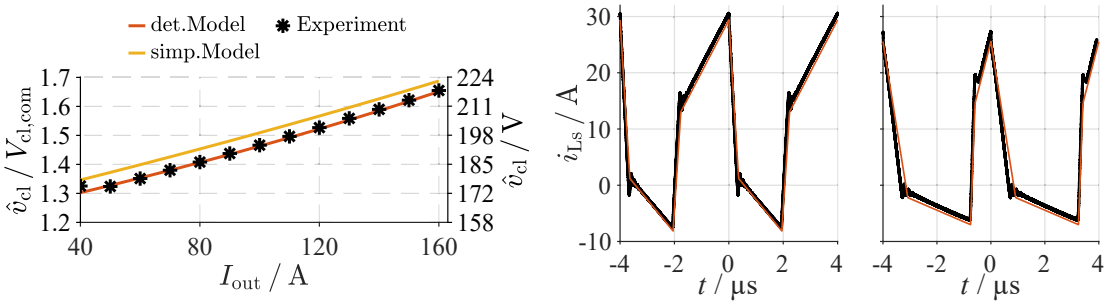


(a) (b)

Fig. 10: ZVS analysis for the nominal operating point. (a) Measured operation and (b) zoom to the switching transient.

3.3 Model evaluation

The values of the transformer were measured with a Wayne Kerr 6500B to $L_{11} = 43\,\mu H$, $M_{12} = 6.32\,\mu H$ and $L_{22} = 902\,nH$. If the connectors and the PCB tracks are estimated with a stray inductance of $L_{con} = 45\,nH$, the equivalent inductances are $L_s = 3.27\,\mu H$, $L_m = 37.8\,\mu H$ and $n = 6.48$. These values were used for the calculation of the clamp-capacitor voltage in Figure 11a and the depiction of the calculated and measured primary transformer currents in Figure 11b and Figure 11c. The prediction of the detailed model fits very well. The maximum error is below 1 %. The simplified model, which was developed in



(a) Load-dependent clamp voltage

(b) Large-gain operation

(c) Low-gain operation

Fig. 11: (a) Validation of the clamp capacitor voltage model (detailed and simplified for the operating point $V_{in} = 290\text{V}$, $V_{out} = 14\,\text{V}$, $I_{out} = 130\,\text{A}$ (a). Modeled and measured primary transformer currents for the operating point (b) $V_{in} = 240\,\text{V}$, $V_{out} = 14\,\text{V}$, $I_{out} = 130\,\text{A}$ and (c) $V_{in} = 420\text{V}$, $V_{out} = 8\,\text{V}$, $I_{out} = 130\,\text{A}$.

2.1 also shows accurate results with errors below 3 %. The voltage is, however, slightly overestimated. Considering the measured and calculated current shape displayed in Figure 11b and Figure 11c, it is evident that the current slope of the model in the $t_{loss,D1}$ interval fits the measured current slope. Hence, this assumption of a connection stray inductance of $L_{con} = 45\,\text{nH}$ can be considered valid.

4 Conclusion

Silicon-carbide semiconductors enable the active-clamp forward converter as an attractive topology for applications with a wide voltage-transfer ratio. This paper presented the design and the experimental evaluation of an active-clamp forward converter applied as a single-stage onboard DC-DC converter of 2.24 kW. An experimental prototype revealed a maximum efficiency of 95 % while maintaining an efficiency larger than 90 % over almost the entire operating region. The achieved power density is 2 kW/l. Copper inlays that can be assembled as SMD components proved to be an effective cooling method achieving a maximum thermal resistance from junction to heatsink of $R_{th} = 2\,\text{K/W}$. Moreover, a developed high-accuracy steady-state model was validated on the prototype showing a maximum deviation of below 1 % compared to the conventional modeling approach that shows an error of about 70 %. An additional presented simplified model can be used for easy and accurate prediction of the clamp-capacitor voltage.

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