

Optimization of the hybrid-switch inverter by decoupling SiC and Si

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Abstract- - The main objective of this paper is to optimize the overall power losses of a traction inverter operating at a DC-link voltage of 400V by using a discrete 650V Si-IGBT and freewheeling diode and a 650V SiC-MOSFET in parallel. The study proposes a new approach to decouple the SiC-MOSFET half bridge and the IGBT/Si-Diode half bridge from each other using a small additional inductance. This approach reduces the turn-on losses of the SiC-MOSFET and turn-off losses of the Si-Diode, resulting in lower overall losses in the hybrid-switch inverter compared to a non-decoupled configuration. The system losses of the hybrid-switch inverter are simulated and validated through both a double pulse test setup and an inverter test rig.

Index Terms- - electric-vehicle, hybrid-switch, Si-IGBT, SiC-MOSFET

I. INTRODUCTION

Efforts are currently underway to reduce the costs of e-mobility traction systems. One method to achieve this objective is to use low-cost IGBTs (full-Si-inverter), accepting higher inverter losses that cause a higher battery capacity for a given vehicle range. On the other hand, the inverter can also use SiC-MOSFET semiconductors, which result in higher semiconductor costs but better efficiency compared to a full-Si inverter [1]–[3]. To combine the benefits of Si-IGBT (low costs and better conduction characteristics at high load currents) and SiC-MOSFET (lower switching losses and better conduction behavior at low load currents), a new approach to reducing overall system costs of a powertrain is using a hybrid-switch topology inverter. Previously, attempts were made in hybrid-switch topology to drive IGBT and SiC-MOSFET in parallel with delayed switching [4]–[8]. The most investigated control strategy in literature involves delaying the switching process between the IGBT and SiC-MOSFET. With the approach in this paper, the MOSFET and IGBT are controlled separately, and the active semiconductor half bridge is selected based on the load current. This allows the benefits of the different output characteristics to be used to increase the efficiency of the hybrid-switch inverter [9]. However, the hybrid-switch inverter has the disadvantage that the active MOSFET switches against the Si-Diode with respect to the interlock time of the inverter, leading to higher turn-on losses of the MOSFET and turn-off losses of the Si-Diode due to bipolar charge carriers. To decouple the SiC-MOSFET

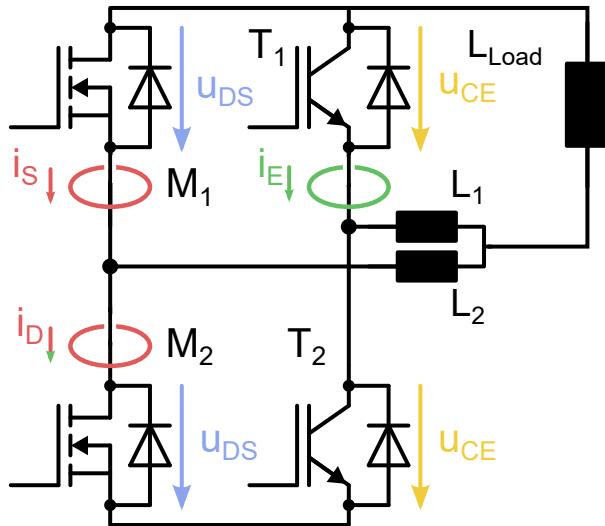


Fig. 1. Simplified electrical schematic of the inductive decoupled hybrid-switch inverter double pulse setup.

half bridge from the IGBT/Si-Diode half bridge, an additional inductance can be used to reduce switching losses of the SiC-MOSFET and Si-Diode. Figure 1 shows a simplified electrical schematic of an inductive decoupled hybrid-switch half bridge. This paper focuses solely on investigating the MOSFET operation mode, as it is currently the leading control strategy for reducing overall system losses during a typical driving cycle.

II. SWITCHING PROCESS

To investigate the performance of a hybrid-switch inverter for e-mobility applications, scaled single-chip double-pulse measurements were conducted to extract switching losses at different temperatures. The reference inverter has a nominal current of 450 A and a DC-link voltage of 400 V, with a stray inductance of 20 nH. For the SiC-MOSFET measurements, a Wolfspeed C3M0120065K was used, while the IGBT used was the STGW40H65DFB-4 from STMicroelectronics, which has a freewheeling diode in the same package.

Figure 2 illustrates a typical turn-on process of the MOSFET M2 in the hybrid-switch half bridge. The left-hand side of the figure displays the switching behavior at a decoupling inductance of 2 μ H, while the right-hand side shows the behavior at several nH. The measurement was performed at a temperature of 25°C, and the colors

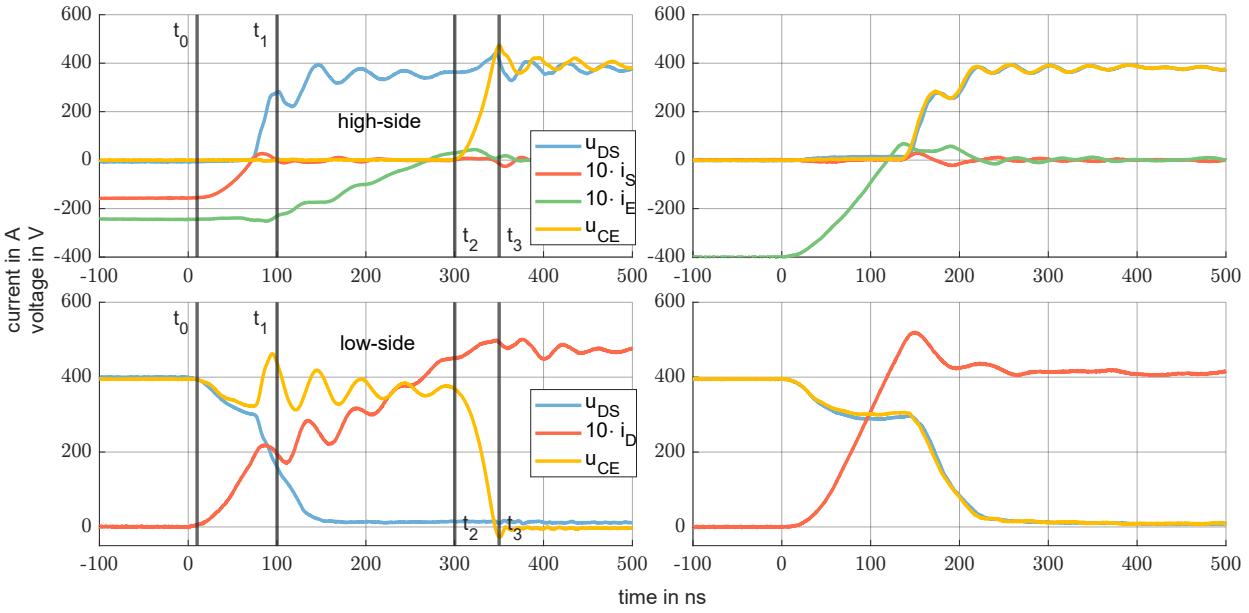


Fig. 2. (left) Typical turn-on process of the decoupled hybrid-switch half bridge at a load current of 40 A and a decoupling inductance of $2\mu\text{H}$. (right) Turn-on process at several nH decoupling inductance. t_1 conducts the whole current before turn-on process because of the interlock time. The graphs in this picture are measured with an oscilloscope. The colour of the transients refers to the colour in Fig. 1

of the graphs correspond to the colors in Fig. 1. The load current in both scenarios was 40 A. The figure shows the high-side signals at the top and the low-side signals at the bottom. In the case of switching at $2\mu\text{H}$, after turning off MOSFET M2, the load current is distributed between MOSFET M1 and the Si-diode T1. M1 conducts 15 A, and T1 conducts 25 A right before the turn-on process. The current share between M1 and T1 depends on the decoupling inductance and the pulse pause of the double pulse test. The current distribution can be observed in Fig. 3, where at approximately -1300 ns, the MOSFET channel M1 closes and the MOSFET current starts to flow through the SiC-MOSFET diode. This results in a higher conduction voltage at M1, leading to a new steady current distribution. When the decoupling inductance is several nH , the time constant is small enough to reach a steady state current distribution before the turn-on process of MOSFET M2. However, with a decoupling inductance of $2\mu\text{H}$, the time constant is too high, and the current share does not reach a steady state before the turn-on of M2. Nevertheless, this effect is useful since it lowers the MOSFET M2 turn-on current from 40 A to 15 A.

Returning to Figure 2, it can observe the turn-on process of MOSFET M2. At time t_0 , the process starts and the current from SiC-diode M1 commutes to MOSFET M2. Between t_0 and t_1 , MOSFET M1 eliminates all the bipolar charge carriers, and the $\frac{du}{dt}$ phase of MOSFET M2 begins. The voltage from MOSFET M2 transfers to MOSFET M1. Due to the current distribution between M1 and T1 before $t = 0$ s, MOSFET M2 experiences only the turn-on losses that correspond to the current of M1. At t_1 , once the bipolar charge carriers of M1 are cleared out, a potential difference between M1 and T1 arises, resulting in a voltage at the inductances L1 and L2 (see Fig. 1). The current from T1 then commutes across the

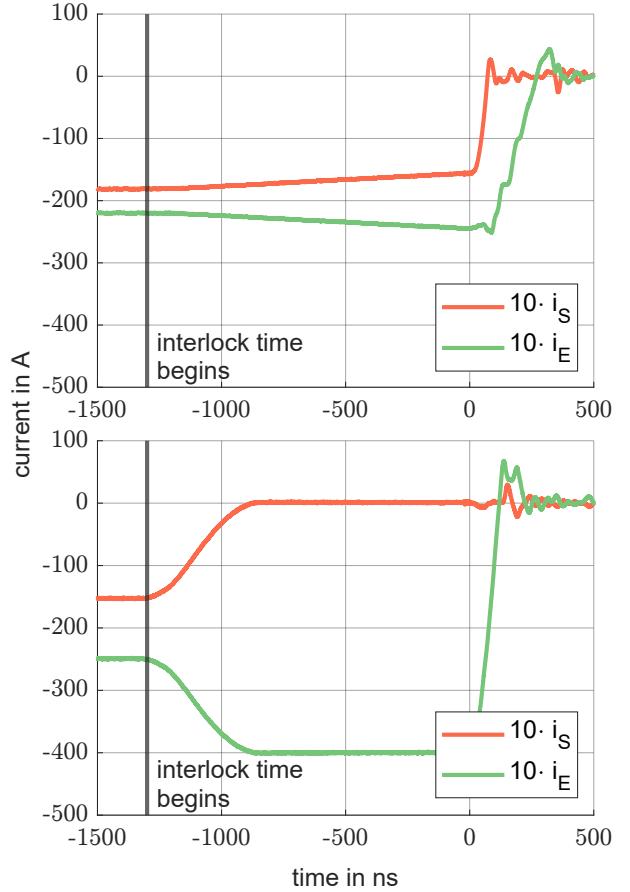


Fig. 3. Current share of MOSFET M1 and Si-Diode T1 before the turn-on process at t_0 . This figure corresponds to fig. 2 before time t_0 . (Top) Inductive decoupling with $2\mu\text{H}$. (Bottom) Inductive decoupling with several nH .

decoupling inductances to M2, as shown by the current i_E high-side and i_D low-side in the figure. At t_2 , the bipolar charge carriers from T2 begin to clear out and the voltage commutes from T2 to T1. However, between t_2 and t_3 , the reverse recovery peak current results in an overcurrent at M2. This reverse recovery current peak also causes a magnetisation of inductance L1. At t_3 , all bipolar charge carriers of the diode T1 have been cleared out, but the inductance L1 is still magnetized. The current flowing through L1 will now drain off over the free-wheeling loop consisting of L1, L2, M2, and T2. This can be observed in the low-side current i_D , which slightly decreases after the reverse recovery of T1 and returns to the load current of 40 A after t_3 .

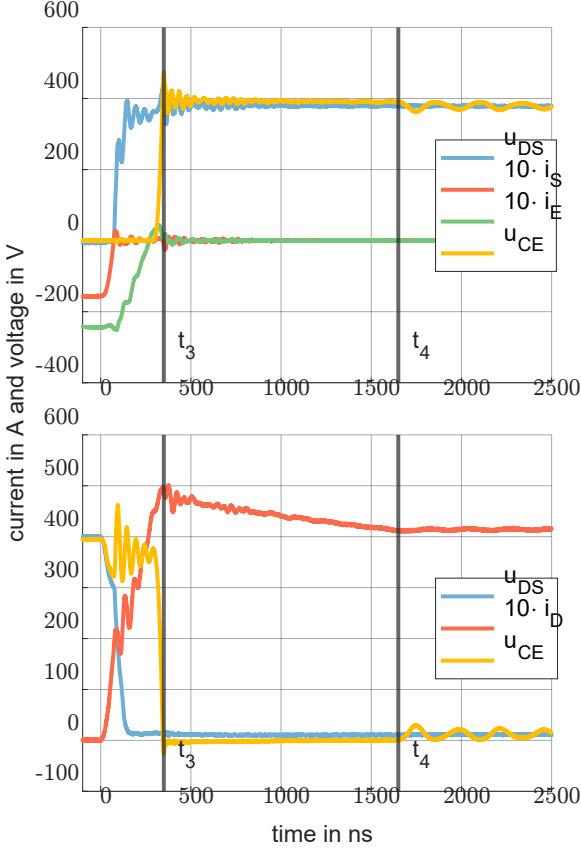


Fig. 4. Turn-on switching process of MOSFET M2 at a wider time range is shown (see Fig. 2 right). The overcurrent of M2 drain off over the freewheeling loop L1, L2, M2, and T2.

Figure 4 illustrates the process of current drain off through MOSFET M2 between t_3 and t_4 . At t_3 , the reverse recovery peak of T1 causes an overcurrent at MOSFET M1, as discussed earlier. Si-Diode T1 enters the blocking state and can no longer maintain the current flow through L1. However, inductance L1 remains magnetized and drives the current. The only path for the current to continue is through the freewheeling loop L1, L2, M2, and T2. This leads to additional conduction losses and demagnetizes the inductance L1. Once L1 is demagnetized, MOSFET M2 carries the load current of 40 A. At t_4 , the diode T2 begins to block, and the capacitance of T2 forms a series resonant circuit with L1, L2, and the

on-state resistance of M2. This results in low-frequency oscillations at T1 and T2. The decoupled hybrid-switch topology reduces the turn-on losses of the active switch M2 but increases the conduction losses. Therefore, an optimal decoupling inductance value must be determined to minimize the overall losses of the inverter.

III. MEASUREMENT

To determine the ideal decoupling inductance, double-pulse measurements were conducted to measure the switching losses with various decoupling inductances. The inductances were tested within a range of 1 μ H to 21 μ H.

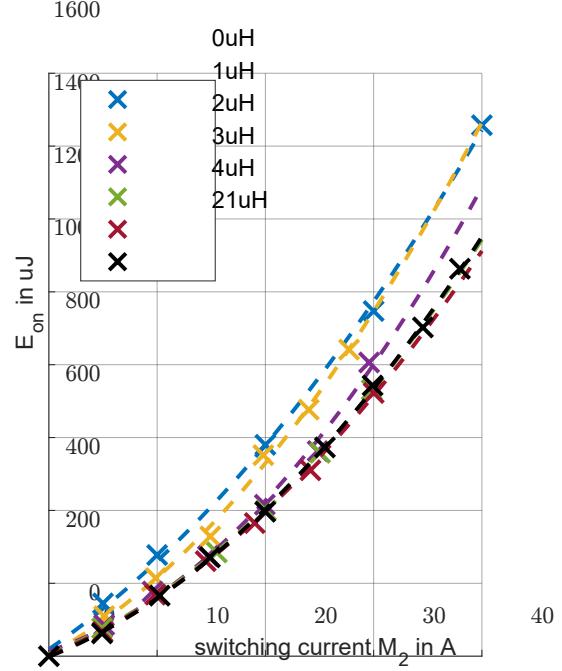


Fig. 5. This graph shows the turn-on switching losses of MOSFET M2 at a temperature of 25°C. The decoupling inductance is varied from 1 μ H up to 21 μ H.

Figure 5 illustrates the turn-on losses of MOSFET M2 at 25°C, obtained from double pulse measurements with varying decoupling inductances. The inductances were tested in a range from 1 μ H to 21 μ H. Results show, that the turn-on losses of MOSFET M2 are almost identical for decoupling inductances of 21 μ H, 4 μ H, and 3 μ H. However, when using an inductance of 2 μ H, the turn-on losses deviate at higher currents. Moreover, as the decoupling inductance is further decreased, the turn-on losses deviation shifts to lower switching current. The highest turn-on losses occur with an inductance of several nH, which is attributed to MOSFET M2 shifting against the Si-Diode, leading to higher turn-on losses. At higher decoupling inductances, this effect becomes smaller. At decoupling inductances of around 2 μ H, this effect is almost gone, and the MOSFET switches entirely against the SiC-MOSFET body diode. It can be seen that further increasing the decoupling inductance does not have

a positive effect on the switching losses any more. It should be mentioned that the turn-on gate resistance is optimized for a decoupling inductance of several nH. By increasing the inductance, the gate resistance remains the same. The dashed lines show fit functions to model the turn-on losses in the upcoming simulation. The turn-off losses of the MOSFET are not affected by the decoupling inductance, so no switching losses are shown.

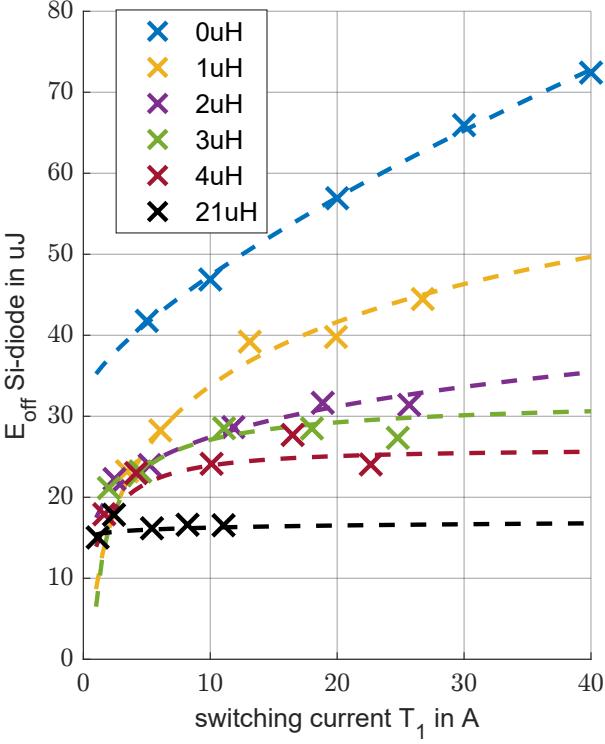


Fig. 6. Turn-off switching losses of Si-diode T1 at 25°C are shown in the figure below. The decoupling inductance is varied from 1 μ H up to 21 μ H.

Beside considering the turn-on losses of the MOSFET, the turn-off losses of the Si-diode also need to be investigated. Figure 6 shows the turn-off switching losses of the Si-diode T1 at a temperature of 25°C. It can be seen that the switching losses decrease by increasing the decoupling inductance. The highest losses are shown at an inductance of several nH, and the lowest losses appear at 21 μ H. This is due to the slower $\frac{di}{dt}$ at the turn-off process of the Si-diode caused by the decoupling inductance. The dashed lines show fit functions to model the turn-off losses for the upcoming simulation. Figure 7 depicts the current transients during the turn-off process of the Si-diode. Due to the decoupling inductance, the rate of change of current ($\frac{di}{dt}$) changes, which leads to a lower reverse recovery peak current. Additionally, this results in less reverse recovery charge and, therefore, lower turn-off losses of the Si-diode.

IV. SIMULATION MODEL

To evaluate the decoupled hybrid switch inverter, a simulation model was built to investigate whether the decoupling strategy confers any overall advantage to the system's losses.

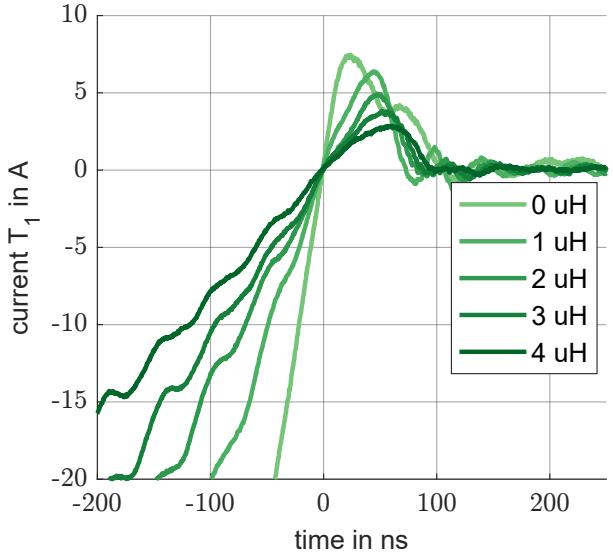


Fig. 7. Current transients of Si-diode with different decoupling inductances.

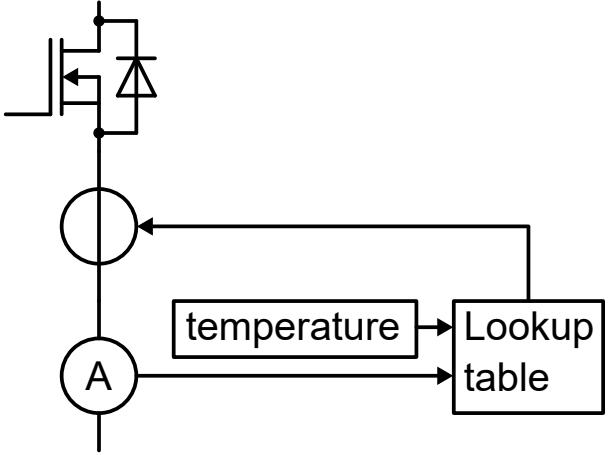


Fig. 8. Fundamental scheme to model the conduction behaviour of a semiconductor

A. Conduction losses

The simulation of the hybrid switch inverter is performed using the simulation software Plecs from Plexim due to the complex communication process between the SiC-MOSFET half bridge and the Si half bridge. Unfortunately, with Plecs, the conduction behavior of the implemented semiconductor cannot be modeled out of the box. Only a fixed on-state resistance can be implemented for the semiconductor. To model the electric conduction characteristic, some tweaks are done. First, every semiconductor shown in Fig. 1 is modeled according to Fig. 8. It consists of an ideal MOSFET with an on-state resistance of 0 Ω . The MOSFET works only as an ideal switch to replicate the switching. To model the conduction behavior, a voltage source and a current meter are used. The current flowing through the semiconductor is measured with the current meter, and this current is fed to a lookup table. Additionally, the present temperature of the semiconductor is taken into the lookup table. The lookup table contains the output characteristics of the different

semiconductors that are deposited. Based on the input parameters, the conduction voltage is fed to the voltage source as shown in Fig.8. However, in reality, the application is more complex than shown. To model the different conduction behaviors of the MOSFET channel and body diode, another lookup table is used. Depending on the interlock time, there is a transition between the characteristics of the channel and the body diode. Although this transition is not shown in Fig.8, it is accounted in the simulation model. For every operational parameter, the steady-state losses and temperature are calculated, and the simulation is run multiple times. After each iteration, the average losses and temperature are calculated and used as input for the next iteration. This is repeated until the steady-state operation losses and temperature are reached. The conduction losses are calculated by measuring the current through the semiconductor and using the output voltage of the lookup table.

B. Switching losses

The switching losses can be calculated using the intrinsic semiconductor model in Plecs, but due to the conduction behavior model shown in Fig. 8, an algebraic loop arises, causing difficulty in calculating the correct switching current. Therefore, switching losses are modeled using another lookup table. This table contains the switching loss characteristic, and the right switching current (see Fig. 2) is used as input. The output values from the lookup table are used to calculate the average switching losses.

C. Modelling the reverse recovery behaviour of the Si-diode

As previously mentioned, the reverse recovery peak current has a significant impact on the communication process of the hybrid switch inverter. This peak current affects the overcurrent of the active MOSFET M2, leading to additional conduction losses in the free wheeling loop. An important goal is to model the reverse recovery peak current of the simulated hybrid switch inverter. To achieve this, the reverse recovery behavior of the simulation is done with the intrinsic reverse recovery diode of Plecs. Essential parameters are extracted from turn-off diode measurements to parametrize the diode behavior, requiring four parameters. The first is the continuous forward current at a specific operational point, and the second is the current slope during the turn-off process of the Si-diode. The current slope depends on the decoupling inductance and can be extracted from Fig.7. The third parameter needed is the reverse recovery time, which can also be determined by the turn-off switching transients of the double pulse test measurement. The last parameter is the reverse recovery charge under the test conditions. With these parameter set, the reverse recovery peak of the Si-diode can be calculated according to [10].

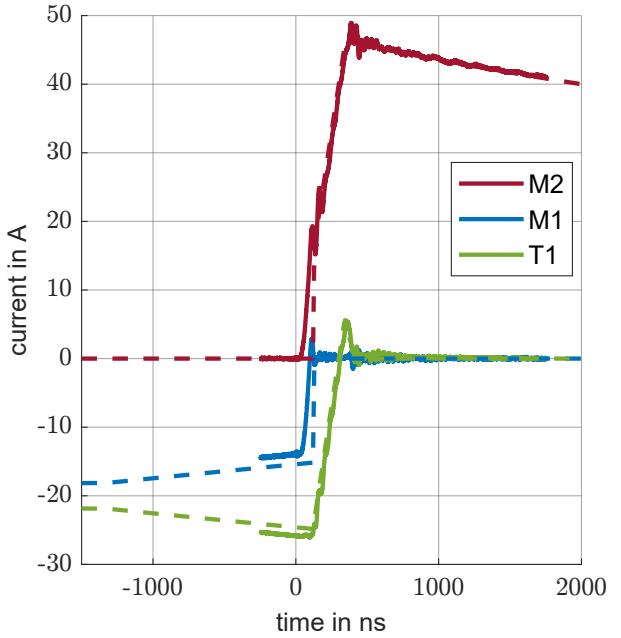


Fig. 9. Comparison between simulation and double pulse measurement of the hybrid switch at a load current of 40A. The solid line represents the measurement results, while the dashed line represents the simulation results.

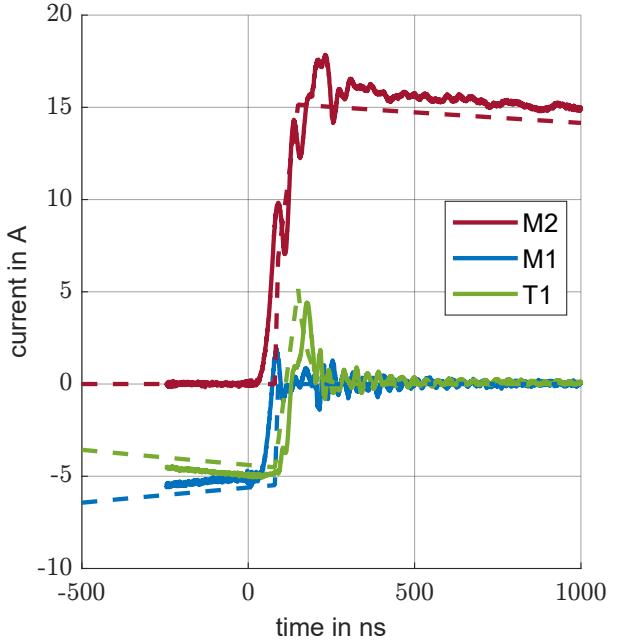


Fig. 10. Comparison between simulation and double pulse measurement of the hybrid switch at a load current of 10A. The solid line represents the measurement results, while the dashed line represents the simulation results.

Figure 9 illustrates the transient comparison of the double pulse measurements at a load current of 40A and a temperature of 25°C. The pulse pause time was maintained at 40μs. It can be observed that there is a slight difference in current share between the simulation and the measurement. However, the current slope of the Si-diode matches perfectly. Furthermore, the reverse recovery current peak is also in perfect agreement. Additionally, the drain off of the overcurrent at MOSFET M2 is

consistent between the simulation and measurement.

Figure 10 shows a comparison of the transient responses from the double pulse test measurements and simulation at a load current of 10A and a temperature of 25°C, with a pulse pause time of 40μs. Although there is a small difference in current share between the simulation and measurement, the current slope of the Si-diode matches perfectly. The reverse recovery current peak matches well, but it can be observed that the current transient of M1 (measurement) is superimposed with oscillations, leading to a deviation at the overcurrent. However, the drain-off slope of the overcurrent at MOSFET M2 matches well between simulation and measurement. Overall, the simulation results show a very good agreement with the double pulse test measurements.

V. CONTINUOUS OPERATION TO VALIDATE SIMULATION

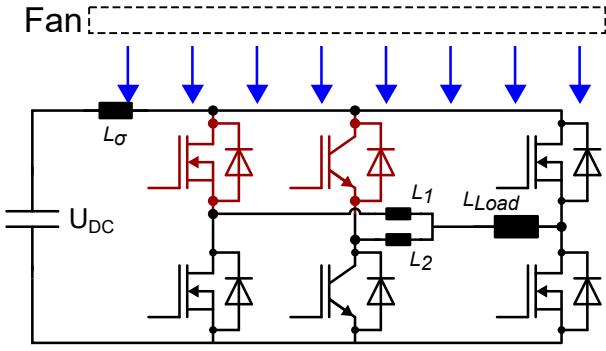


Fig. 11. Electrical schematic of the hybrid switch inverter, which was used to validate the simulation.

To validate the simulation results, an H-bridge hybrid-switch inverter was constructed. The electrical schematic of the hybrid inverter is shown in Fig.11. The inverter is composed of a hybrid switch half bridge and a SiC-MOSFET half bridge. The pure SiC-MOSFET half bridge has a much higher nominal current rating than the hybrid switch half bridge. The inverter losses are

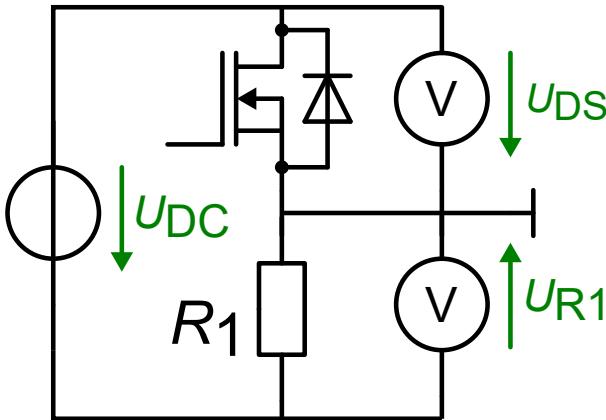


Fig. 12. Electrical schematic for measuring DC power loss to calibrate the thermal resistance of the semiconductors.

measured through a calorimetric method that measures the temperature rise of the semiconductors at specific

DC power losses. A 4-wire DC calibration measurement (shown in Fig. 12) is used to calculate the thermal resistance (as shown in Fig. 13). With the thermal resistance and measured temperature rise, the power losses of the different semiconductors can be calculated during inverter operation. The packaging is opened using laser methods to remove the molding, enabling precise temperature measurements of the chip. The temperature measurements are performed using pyrometers of the Optris CT 4ML type, and the temperature rise of the semiconductors marked in red in Fig. 11 are measured.

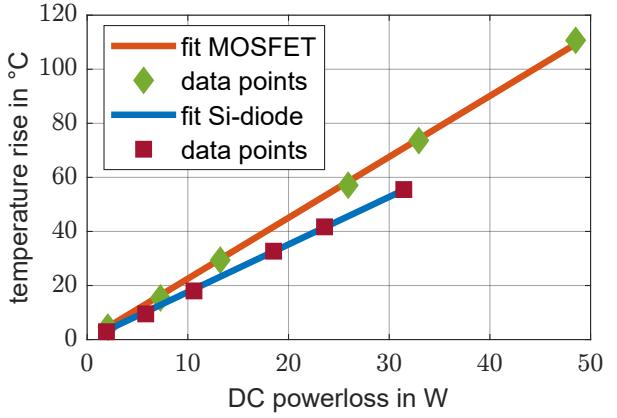


Fig. 13. Calibration of the thermal resistance of the SiC-MOSFET and Si-diode.

Figure 14 depicts the experimental setup used to validate the hybrid switch inverter. The thermal resistance of SiC-MOSFET and Si-Diode is first measured, after the inverter operates continuously at different operational points with different decoupling inductances. The steady-state temperature rise is measured at each point, with the degree of modulation set to 0.1, 0.15, and 0.2. A load current amplitude of 12 A, 20 A, and 27 A is generated by changing the degree of modulation. To keep things simple, the degree of modulation is set to the same value for both the hybrid-switch half bridge and SiC-MOSFET half bridge. Additionally, the power factor of all operational points is zero. The switching frequency remains 10kHz and the base frequency is 200Hz. The simulation is carried out with the same parameters to facilitate comparison between the measurements and the simulation.

The figure labeled as 15 illustrates the comparison of absolute power losses in continuous operation mode between the simulation and the experiment. To ensure the reliability of the measurements, the experiment was conducted twice. The results indicate a deviation between the measurements obtained from the experiment and the simulation. These discrepancies can be attributed to the differences in the current share and the imperfectly modeled reverse recovery current peak in the simulation. Additionally, capacitive effects were not taken into consideration in the simulation. Despite these differences, the trend observed in the results obtained from the simulation and the experiment matches perfectly. In all of the tested cases, the minimum power losses were observed

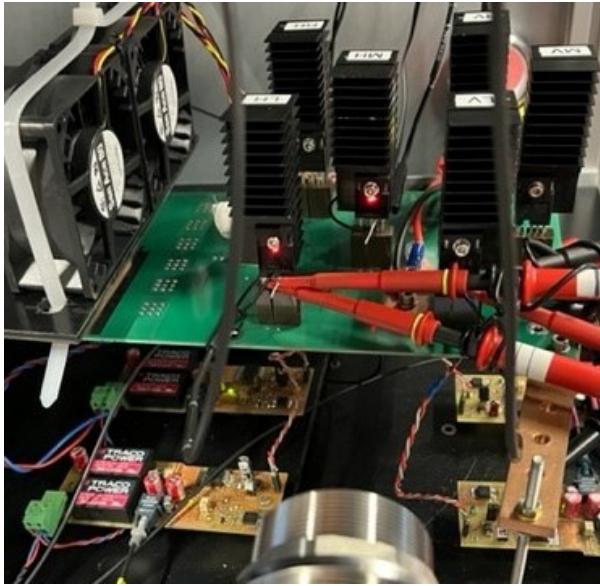


Fig. 14. Experimental setup of the hybrid-switch inverter.

at a decoupling inductance of $1\ \mu\text{H}$.

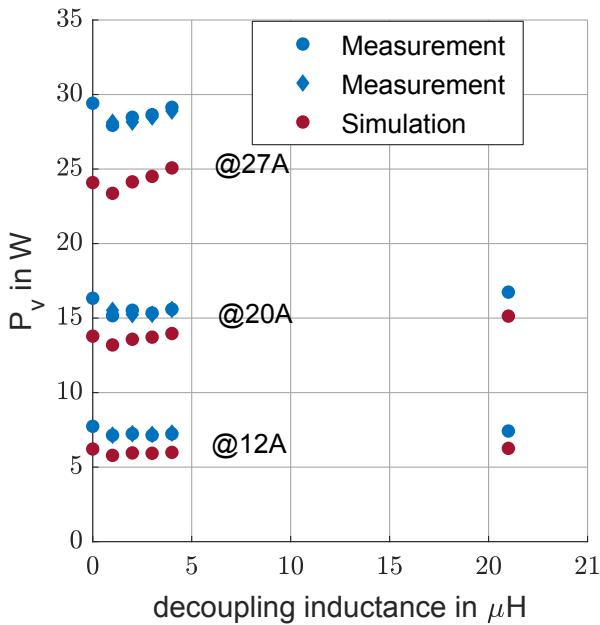


Fig. 15. Absolute power loss comparison of continuous operation mode between simulation and experiment. Several nH decoupling inductance $\approx 0\ \mu\text{H}$

Figure 16 shows the power loss comparison of continuous operation mode between simulation and experiment relative to several nH decoupling inductance. The trend between simulation and measurement matches well at all operational points. Therefore, the use of decoupling inductance in the hybrid switch inverter is a promising approach to reduce the overall current losses of the inverter. Furthermore, the validated simulation can be used to calculate the power losses during typical driving cycles such as the Worldwide harmonized Light vehicles Test Procedure (WLTP). To simulate all operational points of the WLTP would require too much computing time even

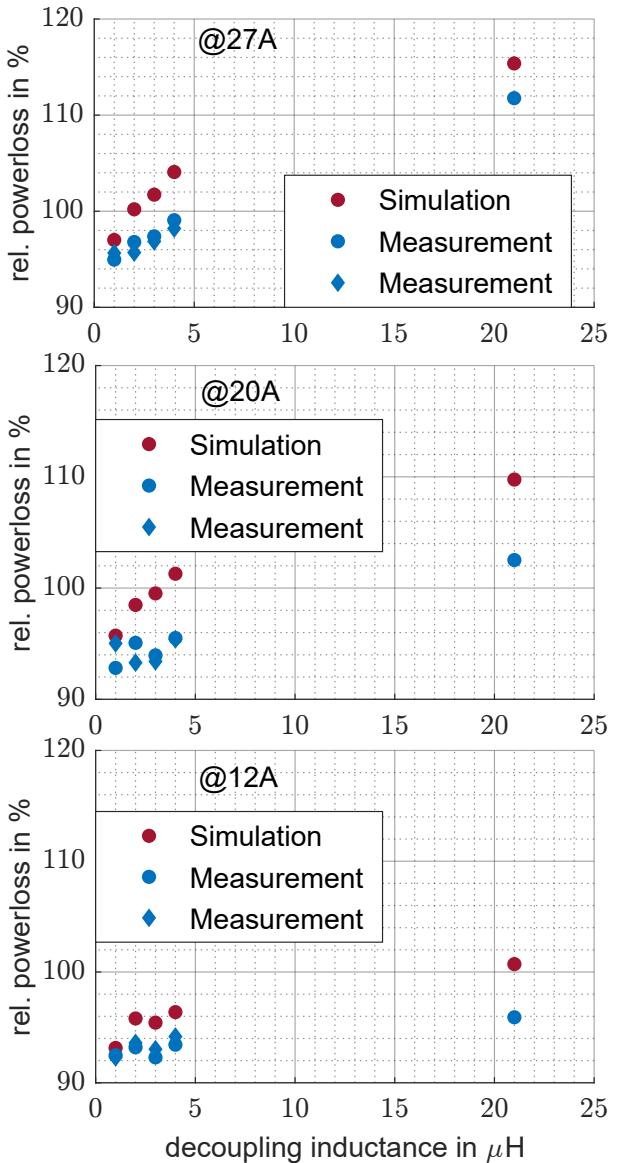


Fig. 16. Relative power loss comparison of continuous operation mode between simulation and experiment relative to several nH decoupling inductance $\approx 0\ \mu\text{H}$.

though the Plecs simulation is parallelized. To reduce the simulation time, the important parameters of the driving cycle, such as the current, power factor, and degree of modulation, are discretized. For example, the current is denominated in steps of 1 A. The power factor is only for the values 1 and -1 taken into account, while the degree of modulation is incremented in steps of 0.1. This significantly reduces the number of operational points. The specific thermal resistance is set to $r_{SiC} = 20\ \text{Kmm}^2/\text{W}$ for the SiC MOSFET and to $r_{SiC} = 30\ \text{Kmm}^2/\text{W}$ for the Si-diode, which is closer to real-world applications. Thermal capacitances are neglected.

The maximum RMS current of the driving cycle is scaled to ensure that the MOSFET does not surpass a temperature limit of 125°C at several nH decoupling inductance. This scaled driving cycle is used for all decoupling inductances to ensure comparability. As a result, the MOSFET is used as the active switch throughout

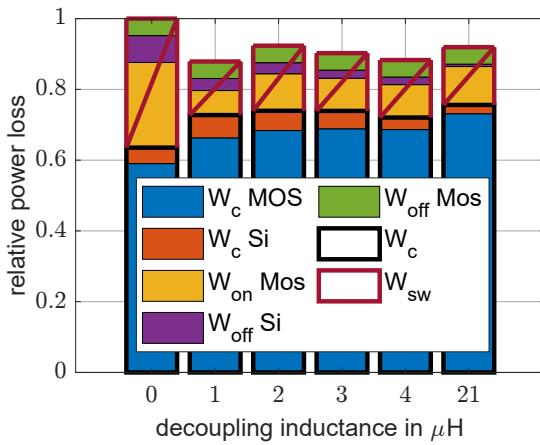


Fig. 17. relative power loss at WLTC driving cycle

the entire driving cycle, while the IGBT remains passive [9]. Figure 17 illustrates the relative power loss at the WLTP driving cycle. It can be observed that the minimum power losses occur at a decoupling inductance of $1\mu\text{H}$. The results show that increasing the decoupling inductance from several nH to $1\mu\text{H}$ leads to a decrease in turn-on switching losses of the MOSFET and an increase in its conduction losses. Surprisingly, the conduction losses of the Si-diode also increase, which can be attributed to the time constant of the decoupling inductance in relation to the interlock time of the MOSFET. This causes a higher current time area at the Si-diode, resulting in higher conduction losses (as shown in Fig. 18). However, increasing the decoupling inductance further leads to a decrease in conduction losses of the Si-diode.

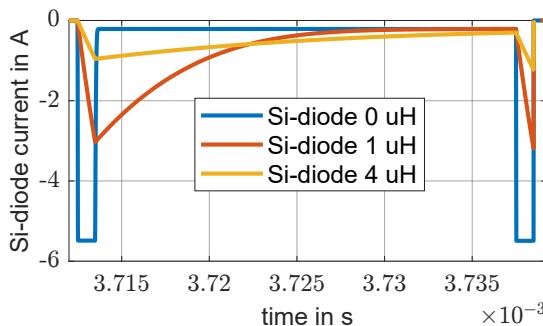


Fig. 18. Current of Si-diode

VI. CONCLUSIONS

By implementing inductive decoupling in the hybrid-switch inverter, the power loss can be significantly reduced, and the level of reduction depends on the decoupling inductance. The simulation results were validated by experimental measurements of an H-bridge hybrid-switch inverter. To assess the performance of the decoupled hybrid switch inverter, a typical driving cycle was simulated, and the results indicated a reduction of over 12% in overall power loss, depending on the decoupling inductance. The gate resistance of the hybrid switch was kept constant for several nH inductance values and used for all other inductances. Preliminary results suggest that

the power losses can further be lowered by optimizing the gate resistance for each decoupling inductance, resulting in a turn-on loss reduction of up to 60% depending on the decoupling inductance. This will further enhance the performance of the inductive decoupled hybrid switch inverter.

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