Dynamic Load Emulation for Automotive Power IC Robustness Validation

Alexander Ulbing[1,2], Daniel Kostynski[1], Markus Sievers[1,2]
[1]KAI Kompetenzzentrum fuer Industrie- und Automobilelektronik
[2]Technical University of Graz - Institute of Electronics
[1]Europastr. 8, [2]Infeldgasse 12
[1]9524 Villach, Austria, [2]8010 Graz, Austria
Phone: +43 (51777) 19968
Email: alexander.ulbing@k-ai.at
URL: [1]http://www.k-ai.at, [2]https://www.tugraz.at/institutes/ife/home

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Keywords

≪Automotive Application≫, ≪Machine Emulation≫, ≪Test Bench≫, ≪Integrated Circuit (IC)≫, ≪Power Hardware-in-the-loop≫.

Abstract

This paper addresses the gap in application related stress testing for automotive power IC qualifications as well as for development-related testing to make ICs more robust. To make test systems more efficient and reduce the cost per test slot the concept of dynamic load emulation has been evaluated. An approach taken by industrial power converters has been adapted to fit the needs of the low power automotive drive domain. To prove the concept and show how application relevant stress could be applied to the device under test simulations are done. In a further step a dedicated hardware test bench has been created and the applicability of the concept within the automotive domain was verified. Several measurements are shown to demonstrate the functionality as well as possible improvements and next steps are discussed.

Introduction

Since the early beginnings of the automotive industry electrical engineers have been in the pursuit of making cars more convenient, performant, efficient and more environmentally friendly. Above all though, the need for reliability has been a define factor in this global industry, especially with the increasing electrification. The semiconductor industry is a key enabler for many reasons and in many areas. While the focus in the last years has been on the replacement of fuses and relays, nowadays, motor control topics become more and more important. For example, driven by the above mentioned credo to make cars more reliable, brushed Direct Current (DC) motors are increasingly replaced by Brushless Direct Current (BLDC) motors. In addition to the reduced mechanical wear and tear of the missing brushes welcome side effects such as electromagnetic interference normally caused by the brushes are reduced as well. Other advantages are higher efficiency (15 % to 20 %), higher torque and a higher dynamic response. Additional diagnostic features and Field Oriented Control (FOC) make BLDC motors the best fit for the use in Advanced Driver Assistance Systems (ADAS), Heating, Ventilation, Air Conditioning (HVAC) air flaps, x-by-wire applications and various other automation topics within cars [1, 2]. These applications are more and more controlled by dedicated automotive power Integrated Circuits (ICs) with a high level of integration. For example, a power IC can encompass not only the power stage but also the

driver and sometimes even the controller itself. This trend will certainly continue such that power ICs will incorporate more and more functionality as well as complex power electronic circuitry.

Throughout the operative lifetime of automotive power ICs the loads connected to them and the resulting load profiles have a tremendous impact on the IC's lifetime. Therefore, it is necessary to start robustness validations and reliability investigations according to application related load profiles at an early stage of chip development. Due to the high amount of test throughput there is a need for a concept that emulates such load profiles without having to use the many specific loads. To handle this issue it is necessary to address the topic of *load emulation*. One of the strategies that can be used is hardware-in-the-loop (HIL) testing. While this takes already place for converter topologies described by Zade *et al.* in [3] and Kadam *et al.* in [4], module testing as described by Ibrahim *et al.* in [5] or for high power electric motor applications as described by Oliveira *et al.* in [6] has not been applied to the characterization and qualification of automotive power ICs.

Before any Automotive Power IC, that drive and control the aforementioned electronic applications, can go to the market rigorous stress tests have to be conducted. Besides the usual standards such as the *AEC-Q100* it is necessary to validate the parts' robustness and reliability under application relevant stress condition with a suitable test bench. Economic and ecological aspects are some of the main consideration points when designing such a test setup. First of all, it is necessary to reduce the complexity of the system development through modularization. Steinwender *et al.* have introduced such a modular test system in [7]. This brings about a significant cost reduction during the design phase of the system in addition to the re-usability of many system components. Since a change of the Device Under Test (DUT) requires only the directly associated printed circuit board (PCB) to be re-designed and changed. The remaining system can stay untouched.

The system presented in this work represents a feasibility study to investigate the aforementioned impact of load profiles with a rapid controller platform. For the design of a test system that needs to stress many devices in parallel the mentioned modular system approach will be used. The following sections show how a setup has been developed to first simulate relevant but simple load profiles and then validate them with a hardware setup. The final sections will discuss the results and offer an outlook on the next steps.

Simulation Model Derivation

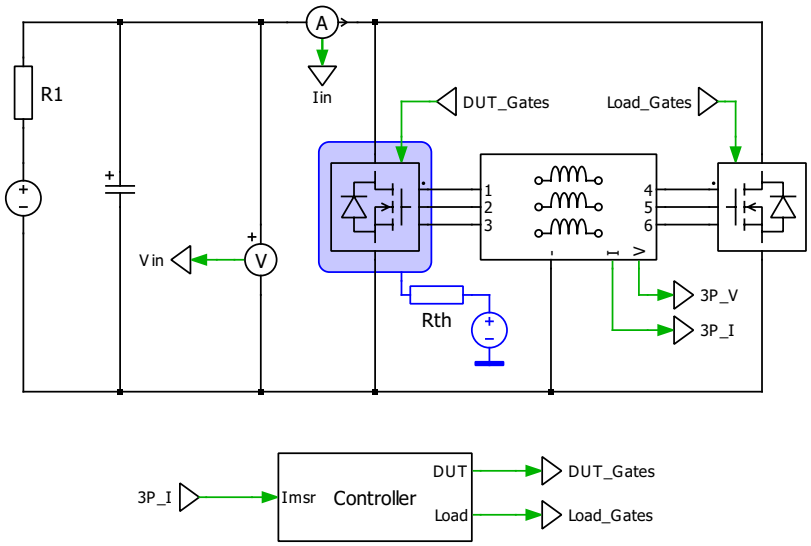


Fig. 1: Overview of the simulation

As described in the previous section the aim is to develop a modular platform that allows various application relevant stress scenarios to be applied to integrated power semiconductor products at various stages of their development cycles. Such integrated power semiconductor products can embody many different

topologies. Nevertheless, a B6 configuration is a commonly implemented solution and will be the focus of the herein presented investigation. In order to investigate a variety of test scenarios a commercially available Rapid Control Prototyping (RCP) platform (here PLECS®) is used to first create a model of the system and then apply the operating points of interest to the DUTs.

Similar to the approach described by Choi *et al.* in [8] two B6 bridges are connected to the same DC link at their DC+ and DC- terminals. The phase terminals are interconnected through inductors. Thereby, one of the converters will act as the DUT and the other as the controllable load that provides the application relevant stress pulses. An overview of this setup is depicted in Figure 1.

The setup has the unique advantage that the load current is circulated within the test system, such that the power supply will only have to supply the energy that is dissipated within the test system. Since [8, 9] already provide a thorough discussion on controller concepts, especially with respect to the simulation of motors characteristic the focus herein is to demonstrate the ability to generate and apply a variety of stress pulses. Since these pulses are intended to investigate the ability of the developed system some of them may be uncharacteristic to motor application. This approach is of special interest when the final application profile of the investigated product is not yet set in stone or the robustness and reliability of the device needs to be investigated during the development process. To accomplish such stress pulses one of the requirements is that each leg of the load module must have a current measurement.

Next to the electrical performance of the system the thermal behavior of the DUT module and load module is of interest. The thermal characteristics of the power semiconductor are taken into account by the use of a thermal model of the power semiconductor provided by the manufacturer, which will require additional tuning with the implemented demonstrator hardware. As shown in Figure 1 additional components, such as the heat sink, are modeled with the appropriate thermal simulation library elements.

Each controller uses a reference current signal (I_{ref}), which is located within the controller block to streamline the code generation for the RCP system. As shown in Figure 2 the input and output blocks of the controller are special functional blocks to implement the hardware functionality of the RCP hardware. During the simulation stage these blocks enable the later used hardware to be simulated. Therefore, besides the reference current the measured inductor currents (I_{msr}) are fed to the controller. Based on these inputs, the controller block generates the PWM control signals for all twelve power semiconductors. While the DUT module is operated with a fixed duty cycle, D, of 50 % for most scenarios the load module uses individual current controllers to generate the desired load profiles for each phase.

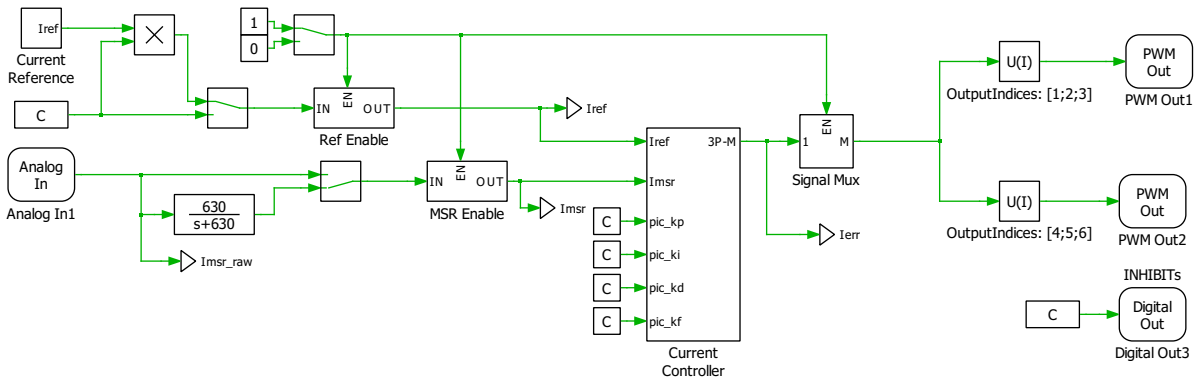


Fig. 2: Overview of the controller implementation

At the heart of the current controller is a PID controller that controls the duty cycle of each half-bridge in the load module. The PID controller uses commonly known anti-windup and saturation features to improve the controller response. Besides it being a well known controller concept the simulation results presented in the next section show that the dynamic requirements of the targeted application profiles can be covered with such a PID controller. Therefore, no further discussion on the controller implementation is provided at this point.

Simulation Results

To verify the concept within the simulation environment, two scenarios are used. The goal of the first scenario is to simulate the stress exerted on the DUT during the start of a motor application. This start-up behavior is simulated by applying a constant value for I_{ref}. Besides simulating the abrupt load change this scenario also helps to analyze the controller response and stability after a step change at the input. The second current profile presented below is a repetitive load change the DUTs may experience throughout its lifetime.

Start-up of the System

As a first step a static operating point is applied to the system at rest. The controller is then forced to perform a step response to reach the static working point. This commonly used approach shows the theoretic functionality of the implemented controller. In Figure 3 the controller behavior for each Half-Bridge is shown.

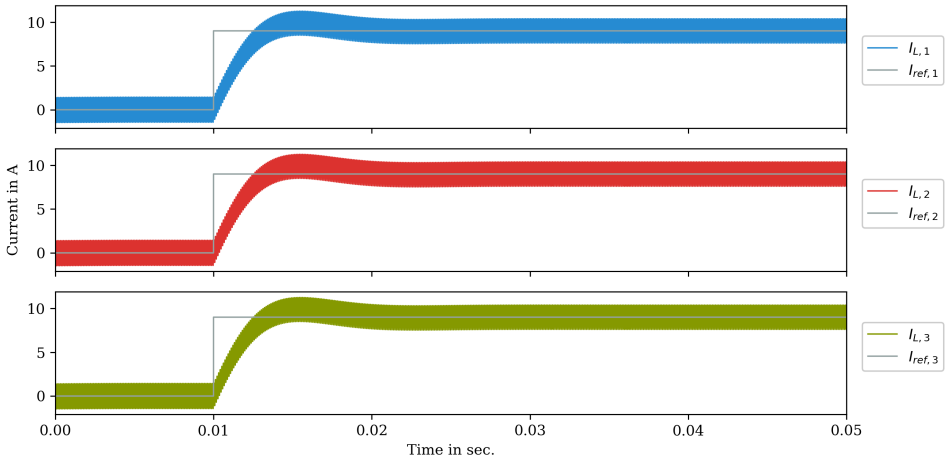


Fig. 3: Overview of the main system parameters at startup

The static working point is defined by a unit step of the output current from 0 A to 9 A as it is shown in Figure 3. Furthermore, the curves demonstrate the controller behavior and the dynamic of the system very well. After 10 ms and a small overshoot, the input parameters have already settled and the power losses in the system remain constant.

Repetitive load change

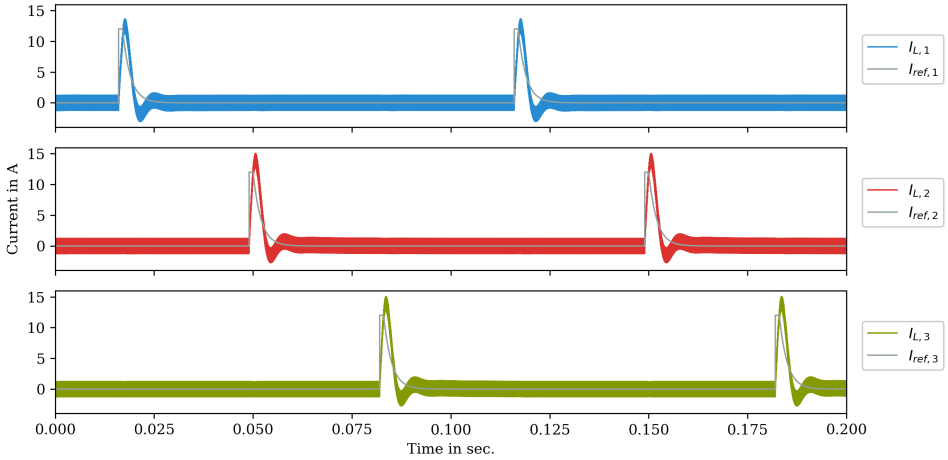
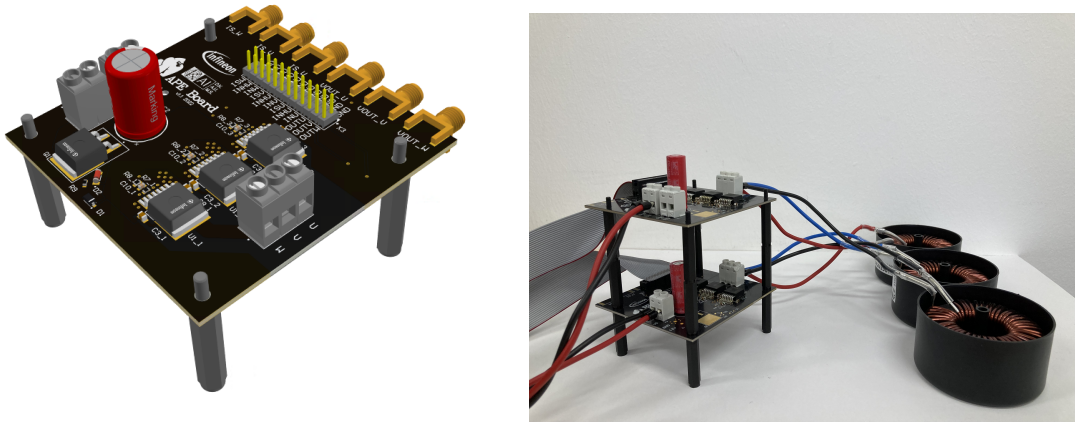


Fig. 4: Overview of the main system parameters during repeated load change

After verifying the basic functionality, an arbitrary reference is added. The aim is to check the performance of the controller and the system when repetitively changing the reference current. The arbitrary reference current is applied alternatingly to all three phases. With this kind of input the half bridge ICs undergo a repetitive stress which can be clearly seen by the currents depicted in Figure 4.

Hardware Prototype

To apply the proposed concept to a real DUT, a hardware (HW) prototype has been developed and is shown in Figure 5a. On the prototype board the DUT is a fully integrated Half-Bridge IC with integrated current sense structures and driver stages. Thereby it is possible to connect to the devices directly with the RCP system. The selected IC is placed three times on the prototype board in a B6 bridge configuration. Due to the fact that the HW setup is intended verify the concept at this stage it serves as a first experimental platform to investigate necessary adaptations and performance limitations. Therefore, the same type of board has been used here for the DUT side and the load side. As a result two of the shown prototype boards in Figure 5a have been connected via inductors at the midpoint of each half-bridge share the same input power supply. This HW setup is shown in Figure 5b.



(a) CAD model of the prototype board

(b) Lab Setup with stacked prototype boards and loads

Fig. 5: Overview of the used hardware

Measurement Results

In a first step it was intended to show that the setup is able to reach a stable steady state after a load change has been applied. Therefore, a static reference current of 9 A was applied to the controller after it had been running with approximately 0 A. Since the DUT board was operated with a fixed duty cycle there is already a current ripple visible before the applied step input. As shown in Figure 6 the controller performs well when applying a load step. Similar to the simulation, the controller shows a small overshoot at the beginning but the steady state is reached fairly quickly. Due to the very low switching frequency of 10 kHz and interferences on the measurement signal, that can be mainly attributed to ground bouncing of the system, small control deviations are noticeable.

As a next step it was necessary to show that the system is able to handle repetitive load pulses. Figure 7 shows the measured phase currents of such an operating point. The figure also includes the simulation results showing that for this operating point the performance is very similar. Since the selected DUTs have a much higher rating that the pulses that are of interest for future DUTs the case temperature was measured but revealed only a negligible increase. Therefore, a more detailed investigation of the thermal behavior will be addressed once the DUTs have been determined.

Although the here presented results show a very stable operation the investigations conducted up to this point show that the signal integrity is strongly affected by the fact that everything is referenced to the

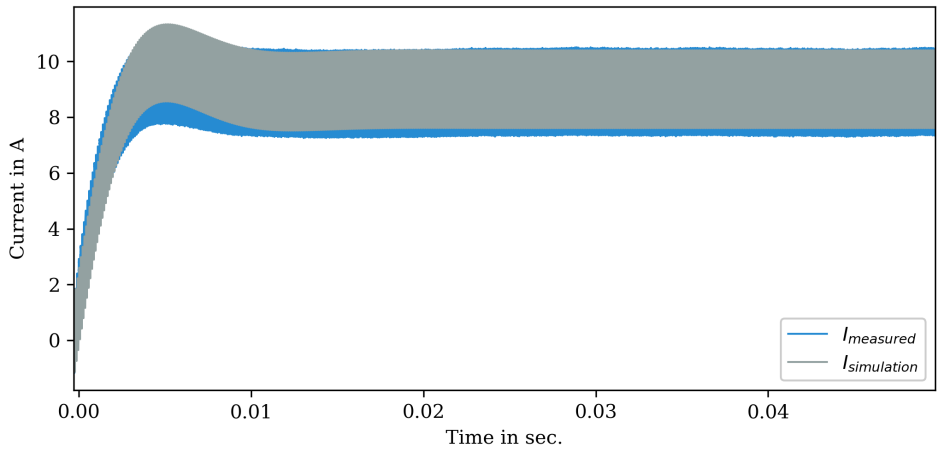


Fig. 6: Recorded oscilloscope measurement results compared to the simulated step response of the system for a single phase.

same ground potential in the automotive power ICs. While the reference to the same ground potential simplifies the HW setup and the connections to the RCP system the controllability of the system is strongly affected by the noise introduced by the switching of the power transistors. Higher ground bouncing due to higher switching currents also contribute to higher interferences on the measurement signals which require additional filtering. The gained insights will serve for a revision of the HW in the near future with the intention to establish a platform suitable for investigation throughout the development process of new power semiconductor technologies and products.

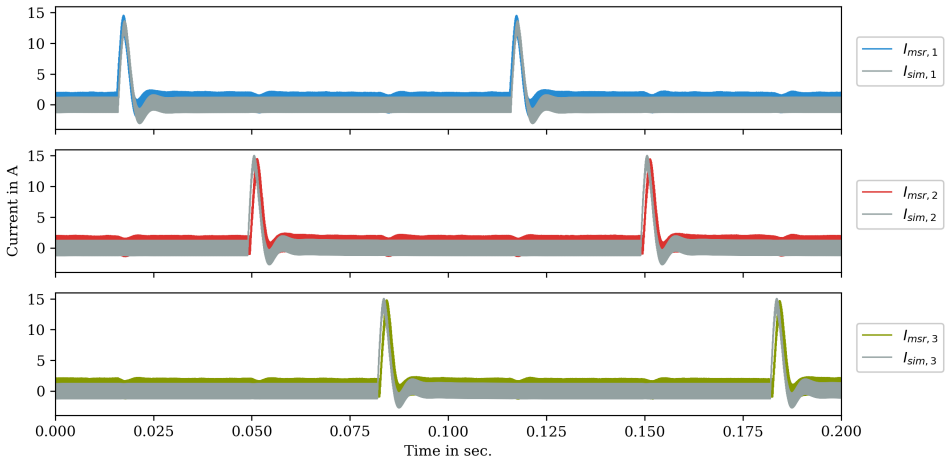


Fig. 7: Recorded oscilloscope measurement results compared to the simulated profiles of a repetitive load pulses.

Conclusion

In conclusion the concept of having a modular platform to perform application related stress to automotive power ICs has been presented and verified in this paper. While this concept is known in the industrial sector it is necessary to start a discussion for automotive reliability and robustness investigations that go beyond the tests required by the known standards. Within the simulation chapter, the approach of running two B6 bridges back-to-back was verified using discrete power semiconductor models since no suitable models were readily available of the later on used automotive power ICs. Using the developed modular HW platform connected to the RCP software the functionality of the controller has been verified for two scenarios. With the help of the RCP system and the HW platform two operating points have been presented to demonstrate the functionality of the system. The first operating point presented was

a single load step to demonstrate the system's response. The second presented operating point showed the dynamic performance and stability of the system under repetitive pulses. Overall it is shown that the developed HW platform is ready to use for further investigations, especially taken various load mission profiles under consideration. Future work will focus on improving the setup with respect to signal integrity and space as well as investigations and test runs on new control concepts. Additional investigations will apply different load profiles and stress levels to the DUTs and monitor the resulting stress at the power ICs. Last but not least, additional measurements will be implemented to acquire more diagnostic data of each stressed device to verify which factors impacts the most.

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