Partial Discharges of Insulated Wires under Impulses from Wide Bandgap Power Electronics

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Keywords

≪Partial discharge≫, ≪Insulation≫, ≪Filtering≫, ≪Pulse Width Modulation (PWM)≫, ≪Wide bandgap devices≫.

Abstract

Due to the high voltage slopes from the wide bandgap (WBG) power electronics, which generate high frequency (HF) electromagnetic noises, the identification of partial discharges (PD) becomes very cumbersome. In this paper, a validated PD detection system is utilized to decouple PD signals from those HF noises. In addition, the influences of different insulation systems, grade of insulated wires, steepness of the voltage slope as well as voltage overshoot because of various cable length on the PD events are also presented.

1. Introduction

PD detection is essential to the evaluation and qualification of insulation systems in electrical machines, especially for those which are restrained by the norm DIN EN 60034-18-41 (Partial discharge free electrical insulation systems) [1]. However, due to the steep-edged voltage impulses from the new generation of WBG power electronics, the identification of PD is more cumbersome [2], as the impulse contains HF components and generates electromagnetic noises, which share a similar frequency spectrum like the PD signals [3, 4]. In this paper, a PD detection system, which is validated through two different measurement setups, is illustrated to decouple the PD signals from HF noises, effectively. In addition, influences of the rise-time, the DC-link voltage and the peak value of the voltage impulses on PD events are also studied and presented by different samples of insulated wires.

2. PD Detection System Validation

A schematic description of the developed PD detection system is presented in Fig. 1. The function of a PD Ring-Sensor is to receive all electromagnetic signals, for example, from the transmission cables (noises from switching operations and PD events) as well as the background noises (for example, from radios, mobile phones). In order to ensure, that measurement results are reproducible, the transmission cables are located in defined position through the Ring-Sensor.

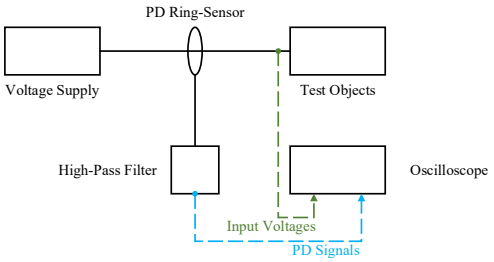


Fig. 1: Schematic description of the PD detection system

Afterwards, all the captured signals are passed through a High-Pass (HP) filter, which has a high corner frequency at about 730 MHz, as illustrated in Fig. 2. This high corner frequency enable a selective filtering between PD signals and switching noises.

The validation of this PD detection system is conducted through the following measurements.

(a) (b)

Fig. 2: HP Filter: (a) Circuit board of HP filter, (b) Frequency spectrum

2.1 Validation with Twisted Pair

The first validation measurement is conducted with a silicon carbide (SiC)-based inverter (CREE C2M004-5170D transistors) as a voltage supplier, a twisted pair with 0.75 mm copper diameter, grade 2 as test objects, a camera as a real-time monitoring system and a PD detection system, which was designed for insulated gate bi-polar transistors (IGBT)-based inverters [5], as a reference object (see Fig. 3).

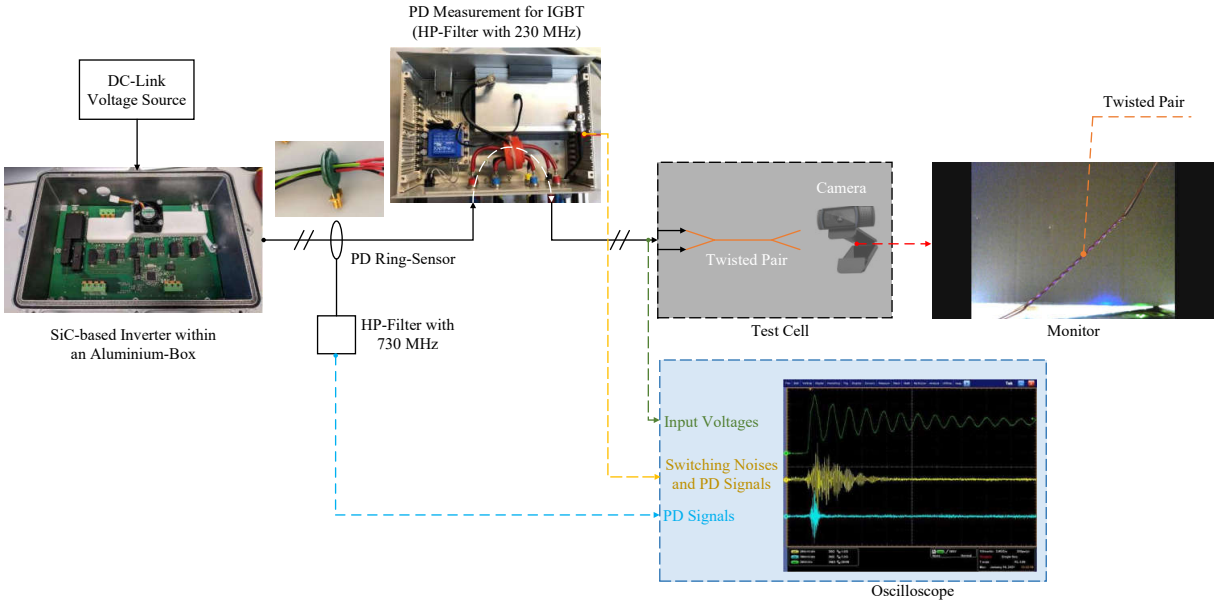
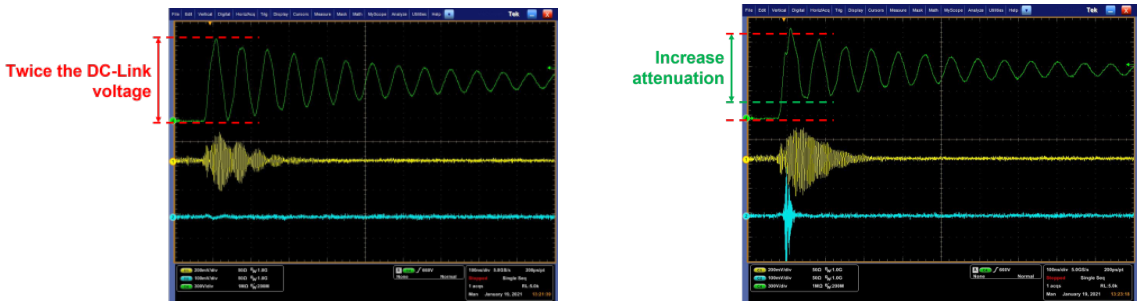


Fig. 3: Schematic circuit diagram for the validation measurement with twisted pair

The purpose and intention of this validation measurement are:

1. With twisted pair as test objects, the detection of PD events is much easier, as it can be directly observed in real-time through the camera.
2. The ability of this new PD detection system, especially the corner frequency, in terms of decoupling PD signals from switching noises of the SiC-based inverter can be examined.

The results of both with and without PD events are illustrated in Fig. 4. The evidence, that there are PD events in Fig. 4 (b) is, that, firstly, the PD lights are observed from the display monitor; secondly, the oscillation of the input voltage converge faster than the 'healthy' voltage curve (Fig. 4 (a)). In other words, the voltage vibration under PD condition cannot reach the double DC-link voltage, which means that there are extra energy losses during this period of time and it is caused by the PD events. It can be noticed, that a corner frequency of 230 MHz is no longer sufficient for the PD detection with SiC-based inverter, as the switching noises contain higher spectrum of frequency noises and cannot be filtered out. Therefore, the corner frequency needs to be increased and the experiments with twisted pair demonstrate, that the chosen of 730 MHz is efficient to filter the noises from the SiC-inverter.



(a) without PD (b) with PD

Fig. 4: Signal records from the oscilloscope: input voltage of the twisted pair (green line); output signal from the PD detection system for IGBT (yellow line); output signal from the new PD detection system (blue line)

2.2 Validation through a Commercial Surge Voltage Tester

Based on the validation measurement with twisted pair, it is proved, that this PD detection system is able to detect PD signals in a SiC-based application environment. The next step is to verify the PD-sensitivity of this system with a qualified commercial surge voltage tester (see Fig. 5).

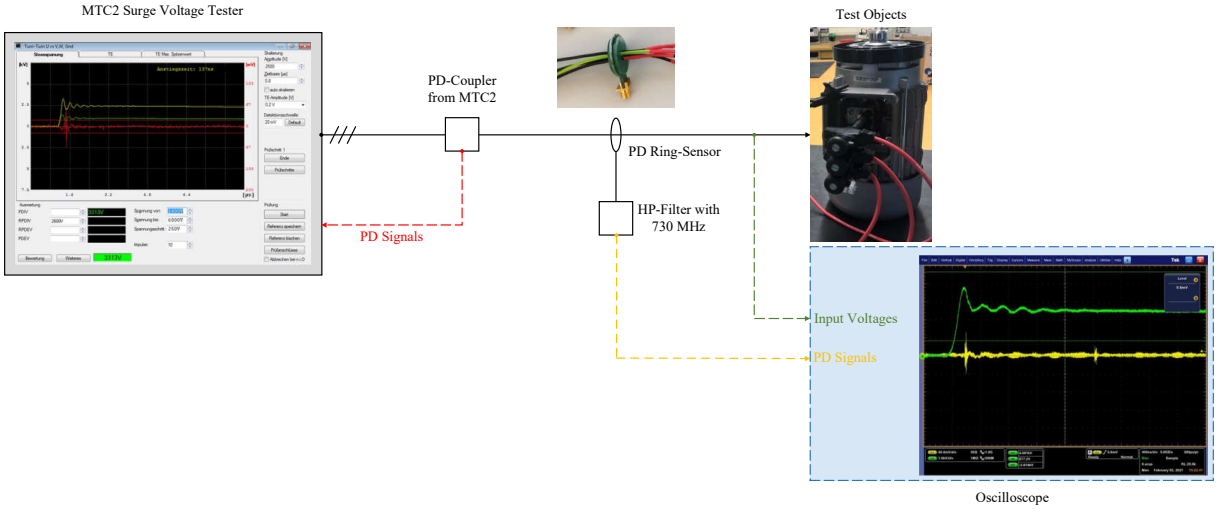
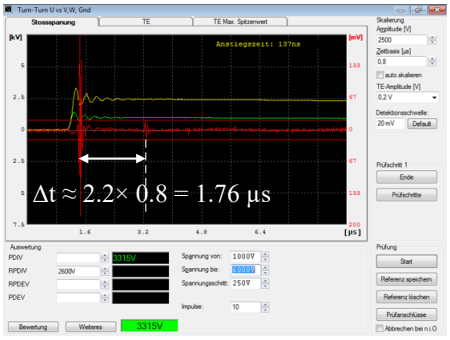


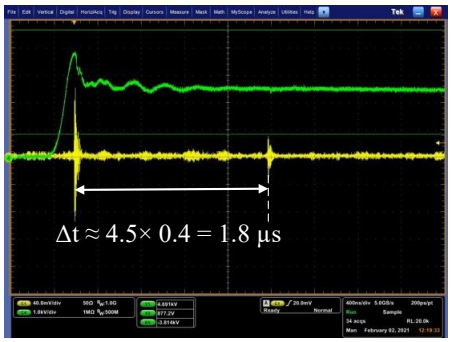
Fig. 5: Schematic circuit diagram for the validation measurement with the surge voltage tester

The surge tester produces surge voltages and using its own PD-coupler to detect the PD signals. Meanwhile, the developed PD detection system with PD Ring-Sensor and HP-Filter is also integrated into

the measurement system to detect the same PD signals. The test object is a three-phase asynchronous machine. The surge voltage and recorded PD signals are illustrated on the monitor of the surge tester and the oscilloscope (see Fig. 6).



(a) display interface of the surge tester



(b) display interface of the oscilloscope

Fig. 6: Recorded surge voltages and PD signals from (a) the surge tester and (b) the oscilloscope: (a) PD signals (red line), surge voltage (yellow line), the reference surge curve (green line); (b) PD signals (yellow line), surge voltage (green line)

The surge tester is programmed to stop, after the PD inception voltage (PDIV) is detected and at the mean time, the oscilloscope shows only the triggered event. In this way, both systems detect the same signal (the first PD event). It can be seen, that both systems show the same number of recorded PD signals and the time intervals between adjacent PD illustrate also a high agreement. This process is repeated several times with similar results.

3. PD Measurements

The ability of decoupling WBG-related HF noises and PD-sensitivity of the developed PD detection system are validated through SiC-based inverter and surge voltage tester, respectively. The following PD measurements utilize this verified detection system to investigate the influences of the DC-link voltage, cable length, rise times, impregnation on the repetitive PDIV (RPDIV) and PD pattern of enameled wires.

3.1 Specimens

The test objects are three different types of enameled wires with the same copper diameter of 0.85 mm and are of the same manufacturer. Two of them are of insulation grade 2 (A and B) where one of them features a PD-resistant additive (B). The third type (C) is of insulation grade 3. All specimens are twisted according to the standard DIN IEC 60851-5 [6] with eight twists. The standardized twisted pair specimens, as well as the twisted pair specimens with impregnated insulation resin are both considered, as proposed in [2]. The respective designations of the specimens are listed in Table I. Hence, overall, there are six variants and each of them has five samples: without impregnation (A1, B1 and C1); with impregnation (A2, B2 and C2). In this way, the effects of insulation film thickness, corona-resistant insulation film and the impregnation process can be investigated.

Fig. 7: In insulation resin impregnated twisted pair of enameled wire

For impregnation, the test specimens are first immersed in a coating resin. To extract air voids from

the resin coating, the specimens are placed in a vacuum chamber for 20 min. Subsequently, the resin is precured for 10 min at 50°C before being fully cured for 60 min under UV irradiation. Figure 7 shows a section of an impregnated twisted pair specimen.

Table I: Parameters of enameled wires

Specimen	Type of Wire	Resin Impregnation
A1	grade 2	no
A2	grade 2	yes
B1	grade 2 PD resistant	no
B2	grade 2 PD resistant	yes
C1	grade 3	no
C2	grade 3	yes

3.2 Test Circuits

The PD measurements are conducted with the surge tester and SiC-based inverter, respectively.

3.2.1 Surge Tester

The applied test voltage of the surge tester with Step-by-Step (SBS) methods [7] starts from 400 V and stops automatically, when the peak-to-peak RPDIV is detected. The voltage rises 100 V on each step and each step contains 10 impulses. The threshold of PD detection is defined at 60 mV according to the system and background noises. Figure 8 shows the peak-to-peak RPDIV of each specimen.

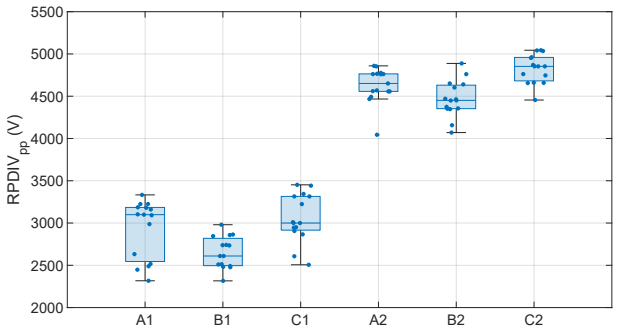


Fig. 8: RPDIV of each specimen under surge tests

It is shown, that peak-to-peak RPDIV of impregnated specimens are almost twice as high as the specimens without impregnation. As a results of that, the maximum allowed DC-link voltage of the SiC-based inverter (950 V_{DC}) cannot reach the PDIV of impregnated twisted pair. Hence, for the test with SiC-based inverter only A1, B1 and C1 are used as test objects.

3.2.2 SiC-Based Inverter

Similarly, the test voltage of SiC-based inverter is, as well, produced in terms of SBS method. It starts also at 400 V and rises step by step (100 V each step) until RPDIV is detected. The measurement setup is demonstrated in Fig. 9.

In this paper, due to the limitation of memory space and the storage dead-time of the oscilloscope (Tektronix MSO5104B) the meaning of RPDIV [8] needs to be redefined. The oscilloscope is triggered through an external equipment (Keysight 33500B), which produces a train of square impulse with a frequency of 0.5 Hz, 50 % duty cycle and 15 cycles. In other words, during each voltage step, the oscilloscope will save the input voltage and PD signals 15 times, which means that each voltage level lasts 30 s. The time period of each saved file is 1 ms. At the meantime, the inverter produce Phase-to-Phase voltage impulses at a frequency of 16 kHz. Hence, each storage contains 32 bipolar-impulses. The definition of $RPDIV_{DC}$ is the minimum DC-link voltage, at which the sum number of recorded PD events is greater than one half of the sum number of the recorded voltage impulses within one voltage step:

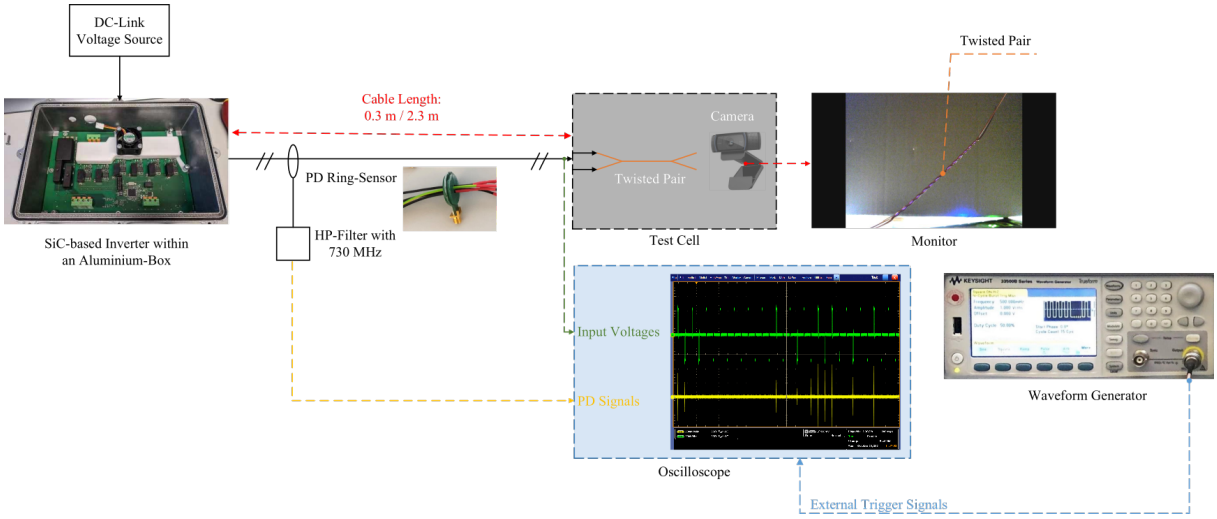


Fig. 9: Measurement setup with SiC-based inverter

$$\mathrm{RPDIV_{DC}}(\mathrm{PD_{sum}}, \mathrm{Imp_{sum}}) = U_{\mathrm{DC,\,min}} \tag{1}$$

subject to $\mathrm{PD_{sum}} > 0.5 \cdot \mathrm{Imp_{sum}}$ and $\mathrm{Imp_{sum}} = 32 \cdot 15 = 480$, where 15 is the number of trigger as well as storage times within one voltage step.

In order to study the effects of peak voltage and the slew rate (dU/dt) the cable between the specimen and the SiC-inverter is varied between 0.3 and 2.3 m (see Fig. 9) and two different gate resistances (20 Ω, 0.5 Ω) are utilized. The rise time t_r is defined as the time for the voltage rise from $0.1U_\mathrm{p}$ to $0.9U_\mathrm{p}$, where U_p is the maximum voltage overshoot [9]

$$dU/dt = \frac{0.9U_\mathrm{p} - 0.1U_\mathrm{p}}{t_\mathrm{r}} \tag{2}$$

After the measurements, the slew rates under different gate resistance and cable length can be summarized as: 20 Ω with 55 V/ns; 0.5 Ω with 120 V/ns.

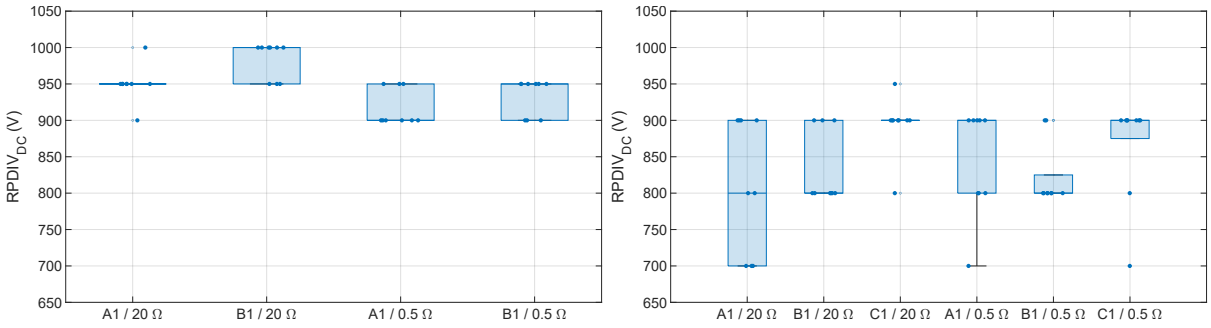
3.3 Measurement Results with SiC-Based Inverter

The measurement results are analyzed from the aspects of $\mathrm{RPDIV_{DC}}$, the time lag between adjacent PD signals and 2D-density plots presenting the pattern of PD events during transient oscillation phases. Each type of enameled wires has five samples and each sample is tested three times.

3.3.1 $\mathrm{RPDIV_{DC}}$

The $\mathrm{RPDIV_{DC}}$ is measured with different cable lengths and gate resistances (see Fig. 10). As mentioned, the maximum DC-link voltage is $950\,\mathrm{V_{DC}}$. However, some tests unsatisfied the condition of $\mathrm{RPDIV_{DC}}$ (defined in 3.2.2), which means that for these tests their $\mathrm{RPDIV_{DC}}$ are higher than $950\,\mathrm{V_{DC}}$. In order to present this undetected $\mathrm{RPDIV_{DC}}$, the voltage is set to be $1000\,\mathrm{V_{DC}}$ (for example, $\mathrm{RPDIV_{DC}}$ at 20 Ω with 0.3 m cable length).

It can be seen, that, in general, the $\mathrm{RPDIV_{DC}}$ with shorter cable length is higher than those with 2.3 m cable length. Similarly, this tendency can also be observed under larger gate resistance. However, a long cable length weaken the influence of gate resistance, as the peak value of the transient oscillation plays a more dominant role for $\mathrm{RPDIV_{DC}}$ than the voltage slew rate. In addition, the $\mathrm{RPDIV_{DC}}$ of C1 in Fig. 10 (a) is not illustrated, as all fave samples of C1 present a higher dielectric strength, which can resist the steep voltage impulse under 0.3 m connection cable. On the other hand, with long cable length



(a) cable with 0.3 m length

(b) cable with 2.3 m length

Fig. 10: RPDIV$_{DC}$ (a) with 0.3 m connection cable and (b) with 2.3 m connection cable

it is capable to reach the RPDIV$_{DC}$ of C1 due to the much higher peak voltage amplitude (see Fig. 10 (b)).

3.3.2 Time Lag between Adjacent PD Signals

The influence of voltage slew rate and cable length on the time interval Δt between adjacent PD events are demonstrated in Fig. 11. The maximum DC-link voltage with 0.3 m cable length is capable to reach 950 V$_{DC}$ (see Fig. 11 (a)(b)), on the other side, with 2.3 m cable length the maximum value is set to be 800 V$_{DC}$ (see Fig. 11 (c)(d)) due to the much higher voltage overshoot.

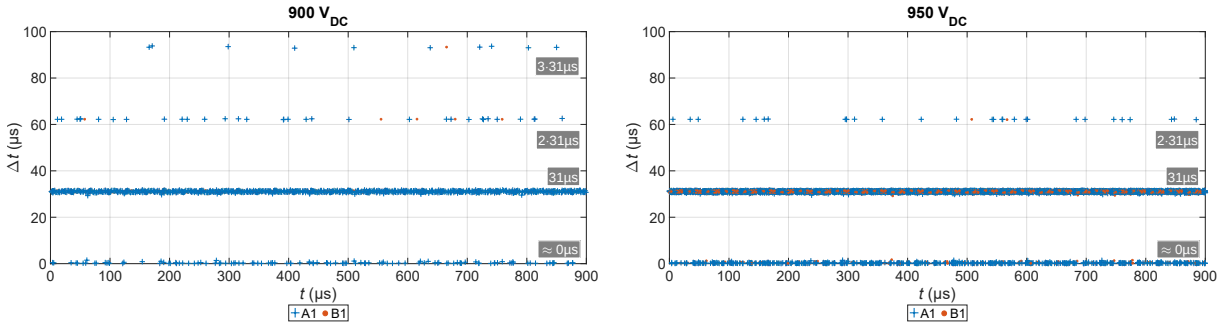
As is shown, the time interval Δt is impacted markedly by the voltage slew rate, DC-link voltage and cable length. The values are mostly concentrated at 3 µs, 28 µs, 31 µs and multiples of 31 µs, which correspond to the time intervals between the four edges of the applied test voltage (see Fig. 12):

1. 31 µs: PD appears in the early stage only at positive and negative rise edges. This phenomenon is explained in [9] in terms of the charge accumulation.
2. 3 µs and 28 µs: PD appears no longer only at positive and negative rise edges, but all four edges due to higher electrical field strength caused by higher voltage slew rate or longer cable length.
3. Multiples of 31 µs: After the first PD event, the successive discharge appears not immediately at the next rise edge, but after some periods.
4. $\approx$ 0 µs: In contrast, this pattern shows, after the first PD event, the successive discharge appears immediately afterwards.

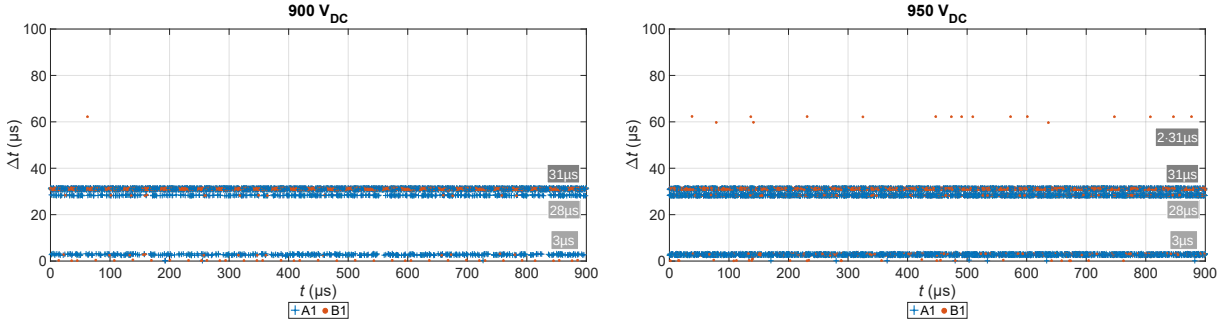
Overall, in terms of the PD event distribution, the influences of voltage slew rate and overshoot on all three types of wires are similar. At 20 Ω, the occurrence of PD events is mostly triggered at rise edges (except Fig. 11 (c) at 800 V$_{DC}$, as the electrical field strength is high enough to trigger the PD under each voltage edge) and after the first PD often follows another PD event, immediately. With the increase of DC-link voltage, the shortly followed successive discharge happens more frequently. On the contrary, with smaller gate resistance (0.5 Ω), the PD distribution is changed and PD events appear now at all edges, as illustrated in Fig. 11 (b)(d). Besides, with the increase of cable length, the most successive PD occur rather after some periods than shortly afterwards.

3.3.3 2D-Density Plot

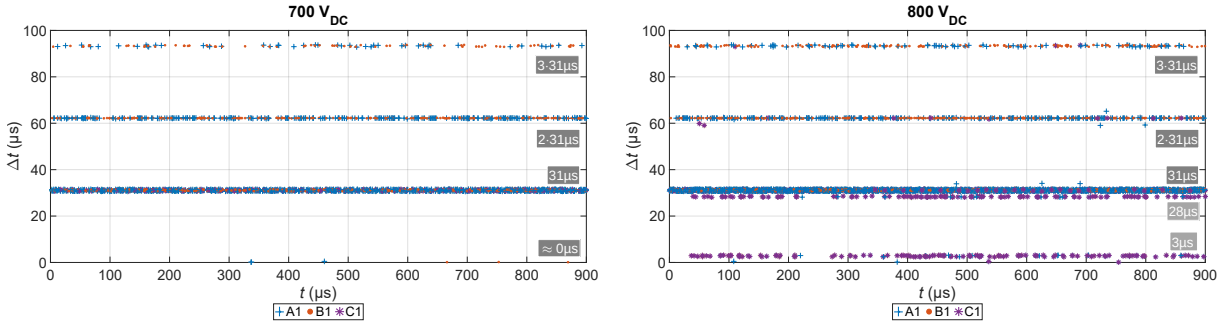
From the analysis of section 2.3.2, it is clearly demonstrated, that the PD often occurs at the impulse voltage edges. Hence, in order to study the PD pattern during these transient oscillation periods, a 2D-density plot presentation is introduced (see Fig. 13 and Fig. 14). As the pattern with longer cable (2.3 m) is similar to that with 0.3 m and it is almost independent of wire types, the recorded data of wire A1, number 5, is used to represent the discharge distribution as a function of the voltage slew rate and DC-link voltage. The orange dot representing the recorded discharges during the repeated measurements, indicates the normalized magnitude, the point of time of each PD event and are overlapped in the plots with different test voltages (the blue line). All voltages are normalized by the maximum magnitude of the voltage at 0.5 Ω, 950 V$_{DC}$.



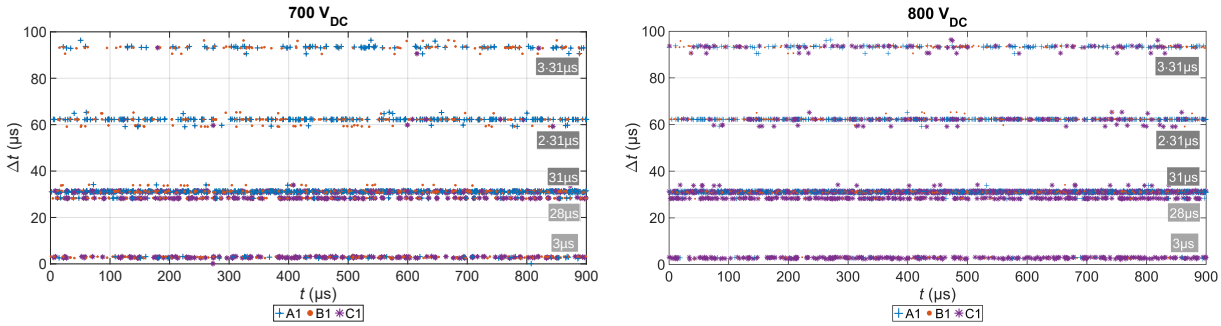
(a) 20 Ω, 0.3 m cable length



(b) 0.5 Ω, 0.3 m cable length



(c) 20 Ω, 2.3 m cable length



(d) 0.5 Ω, 2.3 m cable length

Fig. 11: Time interval Δt between two adjacent PD events under different slew rate (20 Ω: 55 V/ns, 0.5 Ω: 120 V/ns) and peak voltage amplitude in terms of cable length (0.3 m, 2.3 m)

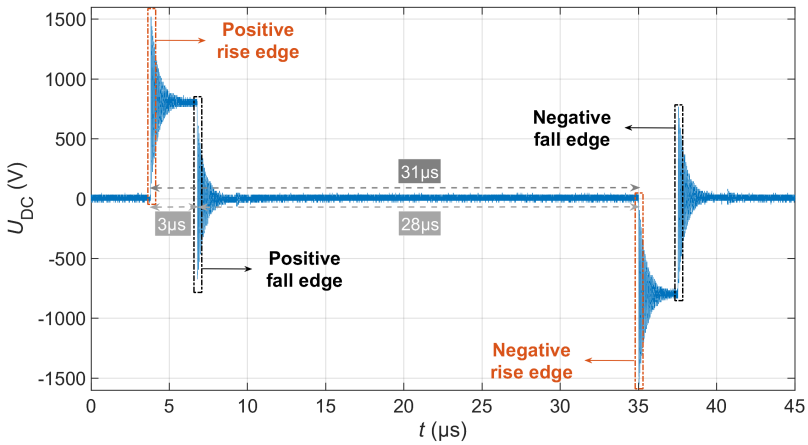
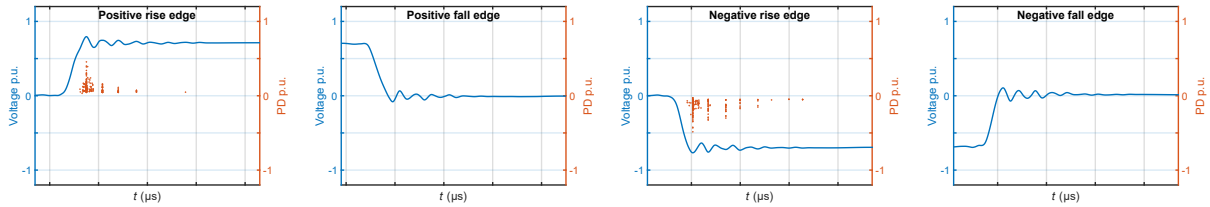
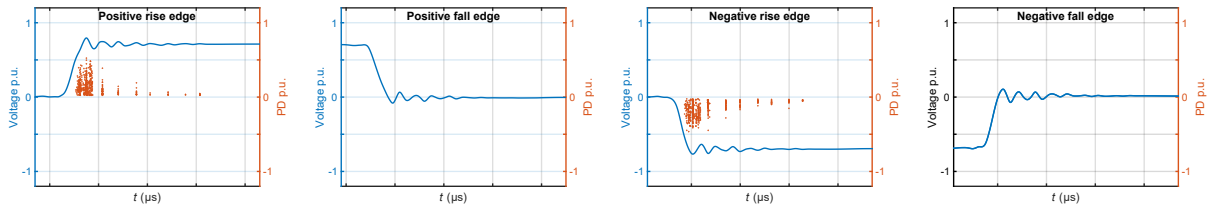


Fig. 12: Four edges: positive and negative rise as well as fall edges

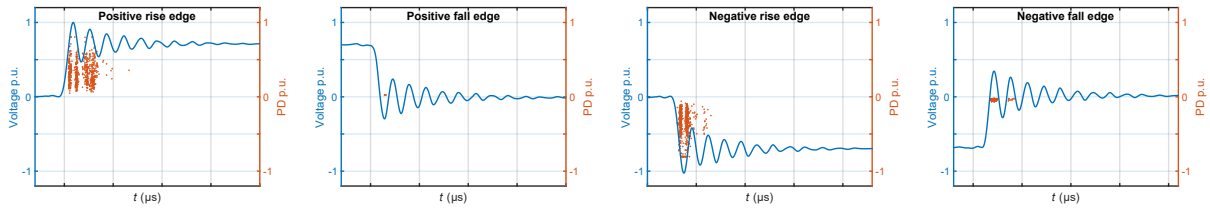


(a) 20 Ω, 0.3 m cable length, 900 V_{DC}, the time period of each subplot: 0.23 µs

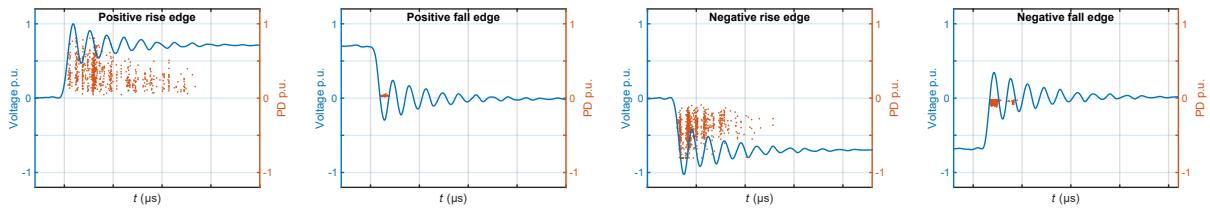


(b) 20 Ω, 0.3 m cable length, 950 V_{DC}, the time period of each subplot: 0.23 µs

Fig. 13: 2D-density plot: illustrating PD patterns during transient voltage oscillations by 20 Ω



(a) 0.5 Ω, 0.3 m cable length, 900 V_{DC}, the time period of each subplot: 0.23 µs



(b) 0.5 Ω, 0.3 m cable length, 950 V_{DC}, the time period of each subplot: 0.23 µs

Fig. 14: 2D-density plot: illustrating PD patterns during transient voltage oscillations by 0.5 Ω

Combining with the previous results from the time lag between adjacent PD signals, the same conclusions could be drawn from the 2D-density plot. At 20 Ω, PD occur only at both rise edges. With the increase of voltage slew rate (at 0.5 Ω), there are a few PD appeared at the fall edges, however, with much smaller discharge magnitude and PD counts compared to the PD at rise edges. Along with the rising of DC-link voltage, the PD counts enhance markedly. Moreover, it is obvious, that:

1. At 20 Ω, the PD concentrate under every maximums with declined magnitude and intensity along the oscillation period.
2. On the other hand, at 0.5 Ω, the PD pattern is changed. Instead of concentrating under the maximums, the discharges locate at the left and right sides of the peaks, separately. And the occurrence of PD is more scattering distributed along the whole vibration zone than at 20 Ω.
3. The magnitude of PD at 20 Ω is generally lower than those at 0.5 Ω.

4. Conclusion

In this paper, a cable-connected PD-detection system is introduced and validated through both PD tests with SiC-based inverter as well as the commercial surge tester considering the ability of HF Electro-Magnetic Interference rejection and PD-sensitivity. In addition, this system is utilized to investigate the influences of steep-edged voltage impulses on different insulated wires with or without impregnation. The recorded PD events are analyzed through the aspects of $\mathrm{RPDIV_{DC}}$, the time lag between adjacent PD signals and the 2D-density plot.

The results show, in general, with impregnation the $\mathrm{RPDIV_{DC}}$ of wires is much higher than that without impregnation. Similarly, the wire samples with thicker isolation film (type C) also have considerable improved dielectric strength. Secondly, the overshoot of the test voltage plays a more dominant role than the voltage slew rate in terms of $\mathrm{RPDIV_{DC}}$.

With regard to the time lag, a significant effects of voltage slew rate and voltage overshoot on the time interval Δt between adjacent PD events can be observed. Normally, the PD events occur only at rise edges, which corresponds to the value of 31 µs. With the enhancement of the electrical field strength, via gate resistance, DC-link voltage or cable length, more discharges are triggered at the fall edges (3 µs and 28 µs), which demonstrate an increasement of the PD counts and an acceleration of the altering process.

Additionally, these patterns are also validated in the 2D-density plot. Furthermore, from the density plot, it can also be noticed, that the PD concentrate firstly under each maximum during the vibration phase. With the rising voltage overshoot, the location of discharges is divided into right and left parts around the maximum and no longer directly under the peaks, which is similar to the PD pattern under AC voltage [10]. This PD pattern and the influence of voltage slew rate as well as the voltage overshoot on the $\mathrm{RPDIV_{DC}}$ should be further studied with actual stators.

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