Optimization and Scaling of a Compact High-Power IGCT Capacitor Charger Based on Simulation and Measurements with a 300 kW/3.3 kV Demonstrator

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Keywords

≪IGCT≫, ≪Pulsed power converter≫, ≪Capacitors≫, ≪DC-DC power converter≫, ≪Optimization≫

Abstract

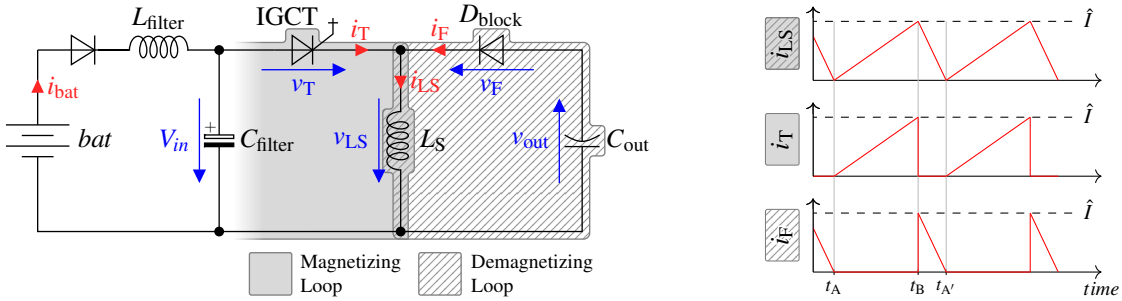
This paper presents the efficiency and charging power optimization of a high pulsed-power inverting buck-boost converter used as a capacitor charger. The influence of converter parameters is investigated with a measurement-based semi-analytical model of the proposed topology. Additionally, the power scaling of such a pulsed power charging system is analyzed.

I Introduction

Pulsed power sources are used for the generation of short (ns-ms) very high power (MW-TW) pulses which are conventionally generated by high voltage capacitors [1]. Industrial applications like electromagnetic forming or heat treating use pulsed power. It is also needed in research for particle physics, electromagnetic acceleration or high power microwave generation. To charge the necessary energy buffers, e.g. high voltage capacitors, compact pulsed power chargers are required. A high efficiency is of special interest in order to reduce losses, as they increase the size of the cooling system.

Brommer et al. [2] analyzed a compact capacitor charger which is used as a basis for these investigations. It utilizes an inverting buck-boost topology in contrast to the H-bridge inverter which is commonly used in such charging systems [3], [4]. Albrecht et al. [5] discussed the different operation principles and showed that operation in Boundary Conduction Mode (BCM) is clearly superior for this specific setup.

The schematic of the charger which uses an IGCT switch and a Brooks-like storage inductor can be seen in Fig. 1 (a). Furthermore, a series diode and an input filter are connected to the input of the converter to protect the battery from high current pulses and negative current. In Fig. 1 (b) the three fundamental currents of BCM operation can be seen. The inductor current i_{LS} is the sum of the magnetizing loop (i_T) and demagnetizing loop (i_F) current.



(a) Schematic with marked magnetizing and demagnetizing loop **(b)** Fundamental converter currents

Fig. 1: Schematic of the capacitor charger and corresponding currents in the inverting buck-boost topology

The parameters of the converter's main components are given in Tab. I. A picture of the experimental setup is shown in Fig. 2. For an input voltage of 200 V its average charging power is > 300 kW with a power density of $4.07\,\mathrm{kW/dm^3}$ [5].

Tab. I: Component list of the converter with references to schematic in Fig. 1a and Fig. 2

	Symbol	Component	Information
①	L_S	Brooks-Like Coil	$L_S \approx 107\,\mu\mathrm{H}$, $R_{LS,DC} = 3.15\,\mathrm{m\Omega}$
②	C_{out}	Film Capacitor	$C_{out} \approx 872\,\mu\mathrm{F}$
③	IGCT	ABB 5SHY 55L4500 [6]	$V_{DRM} = 4500\,\mathrm{V}$, $I_{TGQM} = 5000\,\mathrm{A}$
④	D_{block}	Fast Recovery Diode ABB 5SDF 05D2505 [7]	Two series connected diodes $V_{RRM} = 2500\,\mathrm{V}$
⑤	L_{filter}	Core-Less Inductor	$L_{filter} = 30\,\mu\mathrm{H}$
⑥	C_{filter}	Electrolytic Capacitor	$C_{filter} = 75\,\mathrm{mF}$
⑦		IGCT Gate-Unit Power Supply	$V_{supply} = 38\,\mathrm{V}$
	V_{in}	Lithium Battery Bank [8]	$V_{in} = 200\,\mathrm{V}$

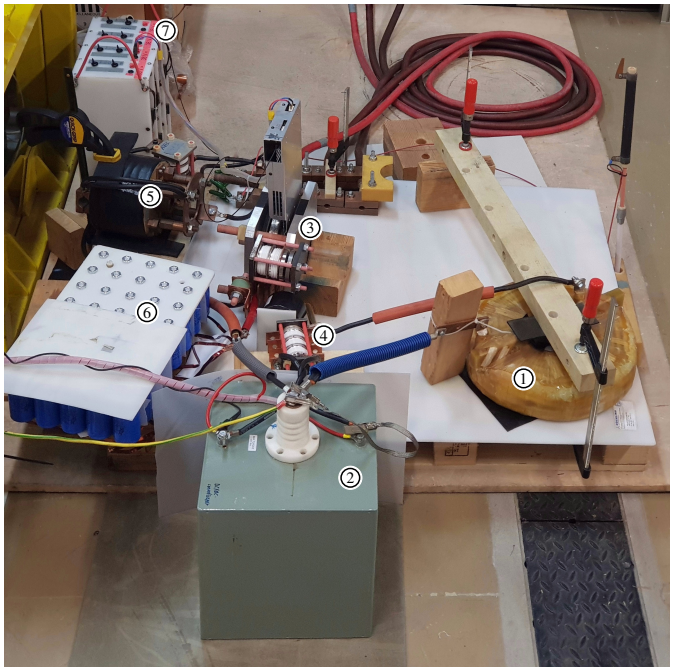


Fig. 2: Picture of the laboratory setup of the power converter

II Converter Simulation Model

In order to identify possible improvements to the proposed converter system without changes to the experimental setup, a simulation model is implemented using Python. This model is based on measurements and an analytical description of currents. With a deviation of the simulated losses of < 10 %, the simulated efficiency deviates less than two percentage points from measurement derived values. More information about the accuracy of the simulation can be found in the following section *Verification*.

Conduction Losses

The conduction losses are calculated based on an analytical description of the currents i_T (magnetizing loop) and i_F (demagnetizing loop). Equation (1) shows the definition of i_{LS} which is the sum of i_T and i_F (see Fig. 1 (b)). The total parasitic resistance in the magnetizing loop is defined as $R_{tot,m}$ and V_{in} defines the input voltage. Due to the input filter, V_{in} is not constant during one pulse. However, to simplify the mathematical model it is considered to be constant. The equation for the demagnetizing loop is obtained by solving the differential equation of a series resonant circuit with L_S as well as C_{out} and the corresponding initial conditions $i_{LS}(t_B) = \hat{I}$ and $v_{out}(t_A) = v_{out}(t_B) = V_{out,t_B}$. The voltage V_{out,t_B} describes the output voltage at the beginning of each demagnetizing cycle. The angular frequency ω is defined as $\omega = \left(\sqrt{L_S C_{out}}\right)^{-1}$. In contrary to magnetizing, the voltage drop across the parasitic loop resistance during demagnetizing is only a small fraction of the voltage v_{LS}. Therefore, it does not alter the waveform significantly and can be neglected.

$$i_{LS}(t) = \begin{cases} \frac{V_{in}}{R_{tot,m}} \left(1 - \exp\left[-(t\text{-}t_A) \cdot \frac{R_{tot,m}}{L_S}\right]\right) & t_A \leq t < t_B \quad \text{(magnetizing loop)} \\ \hat{I} \cdot \cos(\omega[t\text{-}t_B]) - V_{out,t_B} \sqrt{\frac{C_{out}}{L_S}} \cdot \sin(\omega[t\text{-}t_B]) & t_B \leq t < t_{A'} \quad \text{(demagnetizing loop)} \end{cases} \tag{1}$$

The total conduction losses are the sum of conduction losses in the magnetizing loop and the demagnetizing loop ($E_{loss,m}$ and $E_{loss,d}$). They are obtained by integrating the coil current i_{LS} combined with the loop resistances and threshold voltages of the respective loop (see Eq. (2)). The resistances of each loop are summarized in $R_{tot,m}$ and $R_{tot,d}$ - all threshold voltages in $V_{tot,m}$ and $V_{tot,d}$.

$$E_{cond} = E_{loss,m} + E_{loss,d} = \underbrace{\int_{t_A}^{t_B} \left(V_{tot,m} \cdot i_{LS} + R_{tot,m} \cdot i_{LS}^2\right) \mathrm{d}t}_{E_{loss,m}} + \underbrace{\int_{t_B}^{t_{A'}} \left(V_{tot,d} \cdot i_{LS} + R_{tot,d} \cdot i_{LS}^2\right) \mathrm{d}t}_{E_{loss,d}} \tag{2}$$

Each pulse is defined by a desired maximum inductor current $\hat{I}$ and a starting time t_A. The corresponding integration limits t_B and $t_{A'}$ can be obtained by solving (1) for the corresponding parameter t.

The storage inductor L_S is affected by skin and proximity effects. Therefore, its actual resistance is significantly higher than the DC value. In this simulation model, the actual resistance is calculated based on the measurement of $R_{LS}(\omega)$ and an FFT of the occurring current waveform, as proposed in [9]). Other solutions, like the ladder-model presented in [10], [11] are not accurate for all operation points.

Switching Losses

The total switching losses of the converter consist of the turn-on and turn-off losses of the switching semiconductor as well as the forward and reverse recovery losses of the blocking diodes (a series connection of two diodes is needed, as seen in Fig. 2). A previous paper has shown that operation in BCM results in a significant efficiency increase over Continuous Conduction Mode (CCM) [5].

The turn-on losses of the IGCT as well as forward and reverse recovery losses of the blocking diodes were measured and can be considered as neglectable. A series of measurements provided the turn-off losses of the IGCT for selected operating points. Linear interpolation is then used to approximate the turn-off energies between the individual measured points. Since the turn-off losses change when an *RC*-snubber is connected in parallel to the IGCT, the measurement series was conducted with and without a snubber circuit.

The turn-on losses increase with a snubber because the energy of the snubber capacitor is dissipated as heat in the snubber resistor and the IGCT. At turn-on, the stored energy of the snubber capacitor is

minuscule (< 50 mJ) because the voltage at it is equal to V_{in}. Despite of the additional energy lost due to the snubber, the total turn-on losses can still be neglected.

Efficiency
Since all the major loss components are known, the energy related efficiency (per pulse) can be calculated with Eq. (3). The parameter $E_{\text{LS}} = \frac{1}{2} L_{\text{S}} \hat{I}^2$ is the energy in the storage inductor and $E_{\text{loss,sw}}$ is the switching loss.

$$\eta_{\text{pulse}} = \frac{E_{\text{LS}} - E_{\text{loss,d}}}{E_{\text{LS}} + E_{\text{loss,sw}} + E_{\text{loss,m}}} \tag{3}$$

III Analysis of the Converter Setup

Unless otherwise noted, following values for power or efficiency refer to average values for a complete capacitor charging cycle up to 3.3 kV. The setup used is the one shown in Fig. 2, with a battery input voltage of 200 V. Measurements have been conducted with a combination of Rogowski coils and coaxial shunts as well as active and passive high-voltage probes (see Tab. IV for more information). Please take into account that especially losses derived from measurements in the mJ range (IGCT turn-on, reverse recovery, forward recovery) have associated inaccuracies.

Commutation Loop Inductance
The commutation loop inductance is the sum of parasitic inductances which hinder the commutation of the current from magnetizing loop to demagnetizing loop and vice versa. Typically, it is a result of the connections between components. A more extensive explanation can be found in [12]. The simplified commutation cell of the converter is shown in Fig. 3.

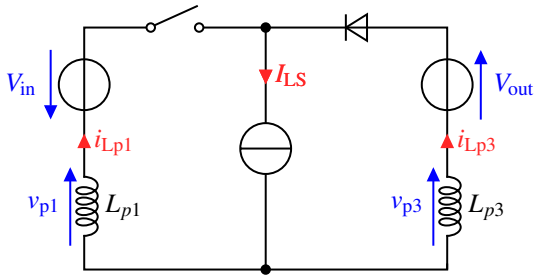


Fig. 3: Commutation cell of an inverting buck-boost converter

Since the commutation process is sufficiently fast, the current I_{LS} does not change throughout it. Therefore, the inductor L_{S} is represented by a constant current source. The Kirchhoff loop with V_{in} and V_{out} shows that the total commutation loop inductance is $L_{\text{com}} = L_{\text{p1}} + L_{\text{p3}}$. Since I_{LS} is constant, any parasitic series-connected inductance does not influence the commutation process. Therefore, only the Kirchhoff loop with V_{in} and V_{out} benefits from connections with lower self-inductance and reduced length. Methods to achieve this have been proposed in [13]. By rearranging the components as well as shortening and rerouting the connections, the commutation loop inductance was reduced from more than 1900 nH to approximately 730 nH. These values are determined based on IGCT turn-off measurements without a snubber circuit or a clamping network.

Switching Losses
The most dominant switching losses are the turn-off losses of the IGCT. Therefore, they are characterized for different turn-off voltages and currents i_{TGQ} of the IGCT. The following measurements were conducted with neither a snubber circuit nor a clamping network. Fig. 4 illustrates a typical turn-off measurement for 2500 V and 2500 A. The turn-off energies of multiple operation points are visualized in Fig. 5. Contrary to [14] the turn-off energy does not scale linearly with current and blocking voltage.

For the used input voltage of 200 V, the turn-on losses of the IGCT are less than 1 mJ. Forward recovery losses of the blocking diodes are below 500 mJ for this application. The blocking diodes' reverse recovery charge causes a slight discharge of the output capacitor, resulting in an energy loss of approximately

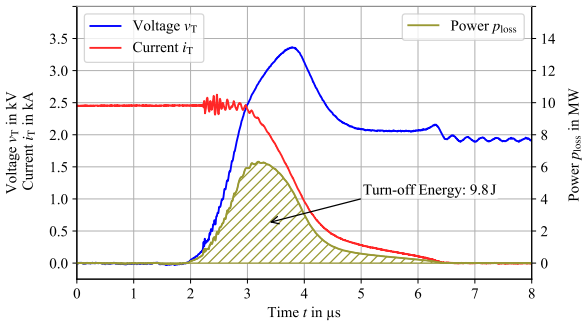


Fig. 4: IGCT turn-off measurement

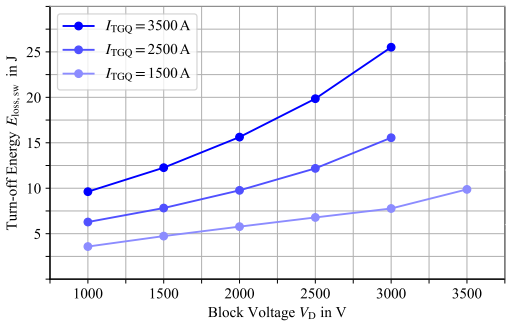


Fig. 5: Measured turn-off losses of the IGCT

5 J throughout one charging cycle up to 3.3 kV. The reverse recovery charge Q_{RR} increases with the parameter $-\frac{di_F}{dt}$. The measured maximum of 710 µC therefore occurs with the highest output voltage at the last pulse of a charging cycle. The relationship between the reverse recovery charge and the lost energy in the output capacitor is further explained in [5].

All small energy losses ($\leq$ 5 mJ) listed above result in a less than 0.2 % of the total transferred energy over one capacitor charging cycle. Additionally, they are complicated to implement into the simulation model. Therefore, the only switching losses included in the model are the turn-off losses of the IGCT.

Conduction Losses

The values of threshold voltages and resistances of the components are given in Tab. I. Parasitic resistances of the connection cables are 1556 µΩ and 808 µΩ for the magnetizing and demagnetizing loop, respectively. The resulting conduction losses are dominated by the energy dissipation in the storage inductor. Its DC and AC resistance was measured via a micro-ohmmeter and an *LCR* meter. Moreover, a FEM simulation is used to verify these results. Parameters for the IGCT and diodes were obtained from the devices' datasheets.

Efficiency and Distribution of Losses

The simulation model combined with the obtained information of the experimental setup can be used to determine the efficiency for each possible pulse in the BCM operation. Additionally, the distribution of losses can be investigated. The former is of special interest because the converter does not operate in steady state. Therefore, every pulse during one charging cycle is unique and has to be calculated individually (based on the output voltage and desired $\hat{I}$). Information on the distribution of losses is of high interest since it reveals the components with the highest potential of optimization.

The following Fig. 6 shows the efficiency of pulses for different maximum conduction currents $\hat{I}$ and output voltages v_{out}. The dashed line crossing all peaks indicates the pulses of maximum efficiency for every output voltage. The influence of different input voltages is not considered, since it is fixed (see Tab. I).

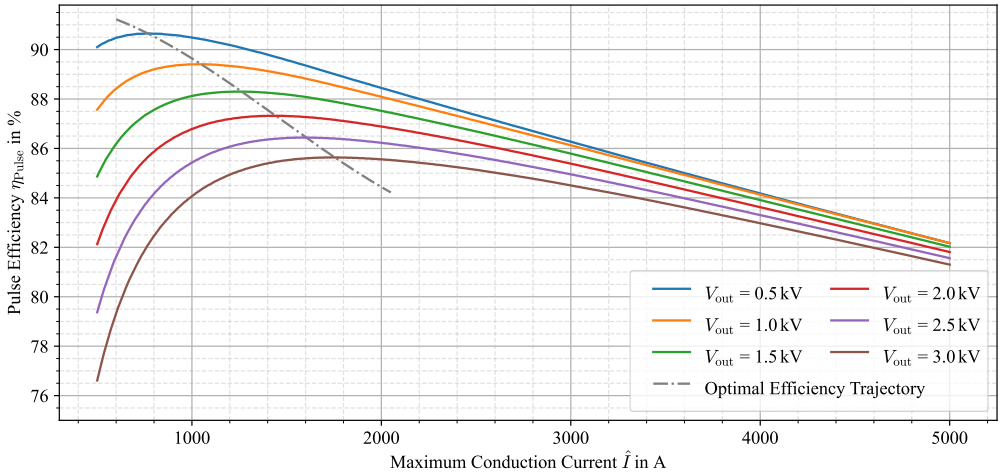


Fig. 6: Efficiency of the converter for different operation points

Fig. 6 illustrates that the pulse efficiency decreases with an increasing output voltage. This is due to the higher switching and reverse recovery losses of the corresponding semiconductors. Hence, the first pulse during a capacitor charging cycle has the highest efficiency. Towards higher maximum conduction currents the influence of V_{out} on the efficiency decreases. The maximum pulse efficiencies exceed 90 %. Pulses with higher maximum conduction current still have pulse efficiencies over 80 %. As shown in [5], power transfer rises approximately quadratically with $\hat{I}$. Therefore, operation along the optimal efficient trajectory drastically limits the power transfer of the converter.

Fig. 7 presents the simulated distribution of losses for the fastest possible charging cycle. The figure is a summary of multiple unique pulses needed to charge the output capacitor up to 3.3 kV. The power maximized control scheme used to achieve this is explained in the following section *Power Transfer*. A nested pie chart visualizes the distribution of losses. Its inner circle differentiates between the **type of loss** (switching and conduction). The conduction losses are furthermore split into losses occurring during the magnetizing ($t_{\text{A}} \leq t < t_{\text{B}}$) and demagnetizing phase ($t_{\text{B}} \leq t < t_{\text{A}'}$). The outer circle indicates in which component the losses are generated. Key parameters of the used setup and charging cycle are presented in the lower right.

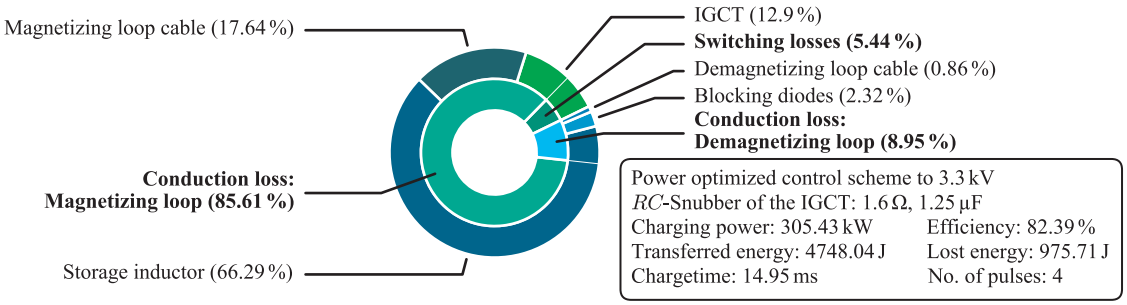


Fig. 7: Simulated distribution of losses during one charging cycle up to 3.3 kV; categorized by type of loss (**inner circle**) and by component (outer circle)

The following conclusion can be drawn from the simulation results summarized in Fig. 7: The total efficiency of the charging cycle is 82.39 %. Its average charging power is 305.43 kW. In total, four pulses are needed to charge the capacitor to 3.3 kV.
Note, that the switching losses of 5.4 % contribute the least to the overall losses. Even the losses generated in the IGCT turn out to be less than 50 % switching losses. The most optimization potential clearly lies in the reduction of the conduction losses. Since the output voltage is typically higher than

the input voltage, the magnetizing phase is significantly longer than the demagnetizing phase. Therefore, the conduction losses during the magnetizing phase are higher than the losses during the demagnetizing phase.

IV Verification

In order to verify the simulation model, a series of measurements were conducted.
According to Eq. (4), the output energy is determined by the difference in output voltage before and after a pulse in combination with the output capacitance.

$$E_{\text{Pulse,out}} = \frac{1}{2} C_{\text{out}} \left(V^2_{\text{out,t}_{A'}} - V^2_{\text{out,t}_B} \right) \tag{4}$$

A Fluke 233 multimeter in combination with a passive high-voltage probe is used to measure the output voltage.
The input energy is determined by integrating the input power over a given time interval. The input power is the mathematical product of the voltage v_{in} and the current i_{bat} marked in Fig. 1. An alternative approach would be to integrate the product of v_{in} and i_{T}. However, the first approach has the advantage that the amplitude of the measured current is significantly lower and also not as steep. This makes measurements easier and thus, improves accuracy.
A passive oscilloscope voltage probe is used to measure v_{in}, while the current is measured with a 1 mΩ coaxial shunt. Refer to Tab. IV for more information about the used metrology.
This means that the losses of the input filter are not resembled in the obtained measurements. The filter decreases the efficiency by approximately one percentage point. The efficiency is defined as the ratio between the output energy and the input energy for each pulse. It is presented in the following Fig. 8 for different output voltages and $\hat{I} = 2500\,\text{A}$. Measurements at other turn-off currents have a similar deviation.

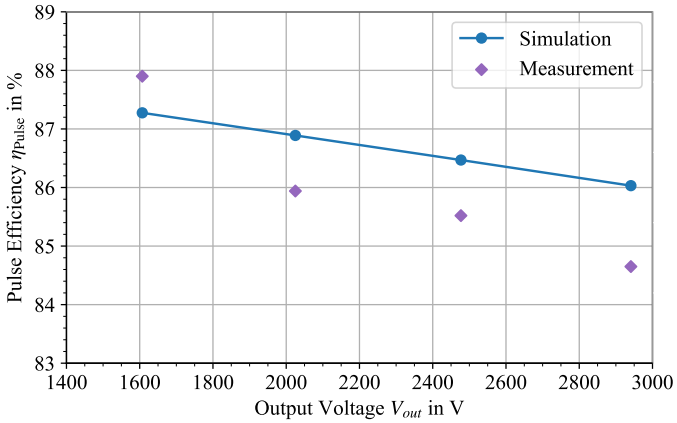


Fig. 8: Comparison between the simulation and measurements for 2500 A

It can be seen, that the simulated values match the measured values. The highest deviation in the simulated efficiency is ≈ 1.4 percentage points for a current of 2.5 kA and an output voltage of 2.9 kV. Simulated values for the efficiency are typically higher than the values derived from measurements. The value at 1.6 kV and 2.5 kA is the only exception for all 20 compared operation points. Note, that the measured values also have inaccuracies due to integration and measurement errors.

V Optimization

In order to increase the efficiency or power transfer of the converter, one can either change the experimental setup or alter the control strategy of the switching semiconductor. For the hardware changes the following factors are analyzed: Input voltage, storage coil inductance, commutation loop inductance (L_S), parasitic resistances. Additionally, optimal control strategies (Dynamic Pulse-Current Control in short DPCC) for both maximized power transfer and maximized efficiency are investigated.

Efficiency

As mentioned earlier, the majority of the converter's losses are dissipated in the magnetizing loop. The magnetizing losses $E_{\mathrm{loss,m}}$ are approximately inversely proportional to the input voltage. Therefore, the best option to decrease them is an increase of V_{in}. This however is only practical up to a certain point, since a high ratio between the output and input voltage is the main reason a boost converter is used to charge the capacitor. A decrease of the total parasitic resistance through shorter interconnections or by redesigning the storage inductor using high-frequency litz-wire or foil conductors would further reduce the losses [15].

The commutation loop inductance also affects the efficiency of the converter. For each turn-off process, its total stored energy is dissipated. Since $L_S \gg L_{\mathrm{com}}$, the transferred energy is significantly higher than the energy lost due to L_{com}. As mentioned in the subsection *Commutation Loop Inductance*, a noteworthy reduction of the commutation loop inductance was achieved by rearranging the components of the converter. The reduction from 1900 nH to 730 nH decreased the switching losses at $I_{\mathrm{TGQ}} = 1.5\,\mathrm{kA}$ and $v_{\mathrm{T}} = 1\,\mathrm{kV}$ by 20 % (from 4.4 J to 3.5 J). Since the switching losses are only a small fraction of the total losses, the increase in efficiency is only marginal.

Additionally, one can change the control strategy of the switching semiconductor to maximize efficiency. The maximal efficiency is achieved by adjusting the length of each pulse in accordance to the dashed line in Fig. 6. One full capacitor charging cycle with this efficiency optimized DPCC has an efficiency of 88.7 % and takes 41.6 ms (simulated), while the fastest possible charging cycle requires 14.95 ms and has an average efficiency of 82.39 %. However, for the efficiency optimized DPCC, $\hat{I}$ of each pulse is below 2000 A. The power transfer is therefore drastically reduced and the charging time inevitably increased.

Power Transfer

The power transfer of the converter increases approximately linear with the input voltage V_{in} and maximum conduction current $\hat{I}$ [5]. A higher input voltage results in a higher $\frac{\mathrm{d}i_{\mathrm{LS}}}{\mathrm{d}t}$ during the magnetizing phase and thus, a shorter pulse duration. Since the energy in the storage inductor rises quadratically with its current and the current increases linearly with time, a higher maximum conduction current also increases the power transfer. However, a higher $\hat{I}$ also results in a higher overvoltage generated by the commutation loop inductance during turn-off. Since this overvoltage has to be blocked by the IGCT, the current has to be limited if a certain output voltage is reached. Reducing this overvoltage is therefore a key element in order to increase the power transfer. Possible solutions for this are now presented in more detail.

The mentioned reduction of the commutation loop inductance (1900 nH to 730 nH) has reduced the overvoltage by up to 53 % (from 3650 V to 1725 V at $\hat{I}$=3000 A). This enables higher current pulses, especially at the end of each charging cycle. Increasing the power transfer from 83.1 kW to 166.3 kW.

A further power increase is possible by dynamically changing $\hat{I}$ throughout the charging cycle. There are two phases during one charging cycle. For the first pulses, the peak current $\hat{I}$ is equal to the maximum rating of the IGCT ($I_{\mathrm{TGQM}} = 5\,\mathrm{kA}$). Here, the specified maximum blocking voltage of the IGCT is higher than the sum of the input, output and overvoltage ($v_{\mathrm{DRM}} > V_{\mathrm{in}} + v_{\mathrm{out}} + v_{\mathrm{Lcom}}(\hat{I})$). If the charging state of the capacitor is increasing, the current $\hat{I}$ must be decreased in order to stay in the SOA of the IGCT. In this second phase, the voltage limit of the IGCT limits the maximum possible conduction current $\hat{I}$. Without the proposed regulation of $\hat{I}$ the maximum possible current of the last pulse has to be used throughout the whole charging cycle, thus reducing the power transfer drastically.

With the implementation of the presented power-optimized DPCC the average power transfer increases from 166.3 kW to 251.88 kW.

The implementation of an *RC*-snubber circuit (1.6 Ω, 1.25 µF) increases the possible power transfer from 251.88 kW to 305.43 kW by allowing higher currents without exceeding the IGCT's maximum voltage. Furthermore, the turn-off losses of the IGCT itself decrease by ≈ 20 %. However, the total switching losses are typically not reduced if a snubber is implemented. Instead, the turn-on losses increase and the snubber's components also generate losses.

Summary
Table II presents the summary of the optimization possibilities. They are rated and sorted after relevance.

Tab. II: Rated overview of possible improvements

Relevance	Improvement	Power Transfer	Efficiency	Effort
1st	Power-Optimized DPCC	+++	−	−
2nd	Commutation Loop Inductance	++++	+	−−−
3rd	Input Voltage	+++	+++	−−−
4th	Parasitic Cable Resistance	+	+	−−
5th	Storage Coil Inductance and Resistance	0	+++	−−−−
6th	Efficiency-Optimized DPCC	−−−	+	−

VI Scaling of the Charging System

The benefit of a converter utilizing a ferrite-less storage inductor becomes apparent when the charger system is scaled towards a higher power. This can be realized by parallel converters or by a single, higher current converter that utilizes multiple semiconductors connected in parallel. For the latter, the coil's inductance is adapted so that the IGCT currents and switching frequency remain the same. Additionally, $\frac{L_S}{R_{DC}}$ is held constant so that the sum over all resistive inductor losses remains constant compared to the parallel converter system. This is possible by adjusting both the number of coils and the winding cross-section. The following Table III presents how the two approaches scale. The advantage of the high current converter lies in the inductive storage. If scaled appropriately, its volume stays constant while the overall losses increase by factor N in both cases [16]). In the approach of parallel converters, the size increases with N.

Tab. III: Scaling laws for parallel converters and a higher current converter. N resembles the power scaling factor

	Power Transfer	Semiconductors	Inductor Volume	Inductor Losses
Parallel Converters	N	N	N	N
High Current Converter	N	N	**1**	N

VII Conclusion

In this paper, the power transfer and the efficiency optimization of a high pulsed-power capacitor charger are investigated. A simple yet accurate simulation was set up and validated by experimental measurements. Consequently, the influence of parameters like the input voltage, commutation loop inductance and storage coil inductance on the performance were investigated. Simulation results show that conduction losses are significantly higher than switching losses and that most of the conduction losses are generated in the main inductor. Therefore, an improvement of the coil's L/R ratio and a higher input voltage are the most promising optimization approaches in terms of efficiency. The rated maximum blocking voltage of the IGCT switch was identified as "the" parameter which limits the power transfer rate. Methods to increase the power and simultaneously stay below the devices' voltage limitations are the decrease of the commutation loop inductance, the use of a snubber circuit or an improved control scheme with dynamically adjusted maximal pulse currents adapted to the charging state of the output capacitor. The power transfer could be increased from 80 kW to 300 kW without significant changes to the experimental setup.

In the case of scaling the charger system, the approach of operating a single coil at a higher current is more promising than multiple converters in parallel.

VIII Appendix

Tab. IV: Measurement Metrology

Name	Range	Bandwidth
Rogowski Coil [17]	± 3 kA	16 MHz
Differential Voltage Probe [18]	± 7 kV	70 MHz
1 mΩ Coaxial Shunt (Zirrgiebel)	–	170 MHz

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