Influence of Different PWM Methods on Thermal Loadings of Power Devices and DC-link Capacitors of Single-Phase Five-Level T-type NPC Inverter

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***Abstract*-- The pulse width modulation (PWM) method significantly affects the performance of inverters such as efficiency, power quality, and reliability. In previous research, the efficiency and power quality are typically considered when Discontinuous PWM methods are applied, whereas study about the reliability of the power devices and DC-link capacitors is insufficient. In this paper, the impact of PWM methods on the reliability of power devices and DC-link capacitors of a single-phase five-level T-type NPC inverter is investigated by considering their power losses and thermal loadings based on simulations and experiments.**

***Index Terms*—DC-link capacitor, Power device, Reliability, Thermal loading.**

I. INTRODUCTION

The pulse width modulation (PWM) method plays a crucial role to ensure the high efficiency, power quality, and reliability of a single-phase five-level T-type NPC inverter. The Discontinuous PWM methods reduce the number of switching transitions within a switching cycle to decrease the switching loss of the power devices. Hence, the efficiency of the inverter increases. However, the application of the DPWM leads to an increase in the total harmonic distortion (THD) of outputs.

Several Discontinuous PWM methods have been proposed to improve the efficiency of the T-type inverter. In [1], the DPWM method called One Pole Clamping PWM (OPC-PWM) has been proposed, where one leg is fixed to the switching state [P] or [N] depending on the polarity of the reference voltage during its fundamental period. Therefore, the power loss of the inverter is reduced because nearly no switching occurs in the clamped leg. This method is called OPC-PWM (PN) in this paper. A similar DPWM method denoted by OPC-PWM (PON) has also been introduced, where the clamped leg also has a switching state [O] for a certain period depending on the magnitude of the reference voltage [2], [3]. The last one is equally distributed DPWM called ED^{2}PWM in this paper, where two legs have equal clamping periods for switching state [P] and [N] during the fundamental period [4]. This method has been proposed not only for power loss reduction but also for junction temperature reduction to improve the reliability of the power devices [5].

The previous research typically focuses on the analysis of the efficiency and power quality when DPWM methods are applied whereas the study about the impact of the DPWM on the reliability of the power device and DC-link capacitor is insufficient even though the different PWM methods lead to the variation of power losses and thus their thermal loadings. Consequently, it has a significant impact on the lifetime of power devices and DC-link capacitors since thermal stress is one of the main causes of wear-out failure of them [6]-[8]. Furthermore, their comparison regarding the efficiency, THD, and reliability has not been performed yet, which needs to be considered to ensure the required performance of the system by analyzing the trade-off between efficiency, power quality, and reliability.

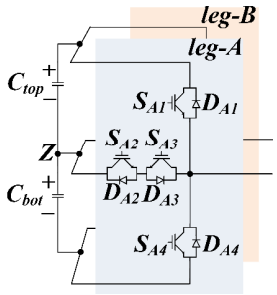

Fig. 1. Single-phase five-level T-type NPC inverter

In this paper, the impact of different PWM methods on reliability of power devices and DC-link capacitors of a single-phase five-level T-type NPC inverter is investigated by considering their power losses and thermal loadings. The analysis is carried out through simulations and experiments.

II. UNIPOLAR PWM AND DISCONTINUOUS PWM METHODS

A. Unipolar PWM (UP-PWM)

The single-phase five-level T-type NPC inverter is shown in Fig. 1, where each leg has three switching states of [P], [O], and [N]. The status of switches and corresponding output pole voltage depending on the switching states are given in Table I.

The reference voltages (V_{ref_A} and V_{ref_B}) of the single-phase five-level T-type NPC inverter, when the UP-PWM is applied, are shown in Fig. 2 (a) and defined as

$$V_{ref\_A} = V_{mag}\sin(2\pi f_g t),\ V_{ref\_B} = -V_{ref\_A} \quad (1)$$

where V_{mag} is the magnitude of the reference voltage and f_g stands for the fundamental frequency of the grid.

B. Discontinuous PWM (DPWM) methods

For applying DPWM, The reference voltages are modified depending on the magnitude of V_{ref_A}.

TABLE I
SWITCHING STATUS AND POLE VOLTAGE DEPENDING ON SWITCHING STATES

Switching state	Status of switches	Pole voltage
[P]	S_{x1}, S_{x2} : ON, S_{x3}, S_{x4} : OFF	$V_{DC}/2$
[O]	S_{x2}, S_{x3} : ON, S_{x1}, S_{x4} : OFF	0
[N]	S_{x1}, S_{x2} : OFF, S_{x3}, S_{x4} : ON	$-V_{DC}/2$

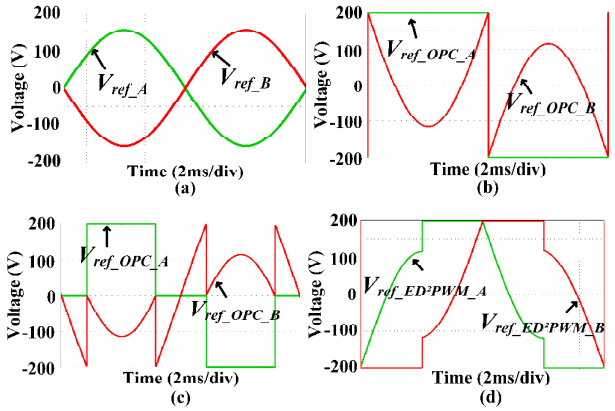

Fig. 2. Reference voltages of two legs under (a) UP-PWM, (b) OPC-DPWM (PN), (c) OPC-PWM (PON), and (d) ED²PWM.

This explanation is under the assumption that leg-A is clamped. For the OPC-PWM (PN), leg-A is fixed to [P] or [N]. If $V_{ref\ A}$ / (V_{DC}/2) is above 0, the reference voltage of leg-A ($V_{ref\ OPC\ A}$) is modified to V_{DC}/2 so that its switching state is clamped to [P]. Then, the reference voltage of leg-B ($V_{ref\ OPC\ B}$) is modified to $V_{ref\ B}$ + (V_{DC}/2-$V_{ref\ A}$) to keep the difference between the two reference voltages. In the other case when the $V_{ref\ A}$ / (V_{DC}/2) is less than 0, $V_{ref\ OPC\ A}$ is changed to -V_{DC}/2 to fix the switching state of leg-A to [N], and $V_{ref\ OPC\ B}$ becomes $V_{ref\ B}$ – (V_{DC}/2 + $V_{ref\ A}$). The modified reference voltages for the OPC-PWM (PN) are given below

$$
\begin{aligned}
&(\text{if } V_{ref\_A}/(V_{DC}/2) \geq 0)\\
&\quad [\text{for [P] Clamping of Leg-A}]\\
&\quad V_{ref\_OPC\_A} = V_{DC}/2\\
&\quad V_{ref\_OPC\_B} = V_{DC}/2 - V_{ref\_A} + V_{ref\_B}\\
&(\text{if } V_{ref\_A}/(V_{DC}/2) < 0)\\
&\quad [\text{for [N] Clamping of Leg-A}]\\
&\quad V_{ref\_OPC\_A} = -V_{DC}/2\\
&\quad V_{ref\_OPC\_B} = -V_{DC}/2 - V_{ref\_A} + V_{ref\_B}
\end{aligned}
\tag{3}
$$

In the OPC-PWM (PON), the clamped leg also has the switching state [O] depending on the magnitude of the reference voltage. When the $V_{ref\ A}$ / (V_{DC}/2) is between 0.5 and -0.5, the $V_{ref\ OPC\ A}$ becomes 0 to make the switching state of leg-A [O] for this period and the $V_{ref\ OPC\ B}$ is modified to $V_{ref\ B}$ - $V_{ref\ A}$. When, $V_{ref\ A}$ / (V_{DC}/2) is above 0.5, the leg-A is clamped to [P] and it is fixed to [N] when $V_{ref\ A}$ / (V_{DC}/2) is below -0.5 as OPC-PWM (PN). Consequently, the reference voltages are modified for the OPC-PWM (PON) as

$$
\begin{aligned}
&(\text{if } V_{ref\_A}/(V_{DC}/2) \geq 0.5)\\
&\quad [\text{for [P] Clamping of Leg-A}]\\
&\quad V_{ref\_OPC\_A} = V_{DC}/2\\
&\quad V_{ref\_OPC\_B} = V_{DC}/2 - V_{ref\_A} + V_{ref\_B}\\
&(\text{if } -0.5 \leq V_{ref\_A}/(V_{DC}/2) < 0.5)\\
&\quad [\text{for [O] Clamping of Leg-A}]\\
&\quad V_{ref\_OPC\_A} = 0\\
&\quad V_{ref\_OPC\_A} = -V_{ref\_A} + V_{ref\_B}\\
&(\text{if } V_{ref\_A}/(V_{DC}/2) < -0.5)\\
&\quad [\text{for [N] Clamping of Leg-A}]\\
&\quad V_{ref\_OPC\_A} = -V_{DC}/2\\
&\quad V_{ref\_OPC\_B} = -V_{DC}/2 - V_{ref\_A} + V_{ref\_B}
\end{aligned}
\tag{2}
$$

The reference voltages under OPC-PWM (PN) and OPC-PWM (PON) are shown in Fig. 2 (b) and (c), respectively.

In the case of ED²PWM, two legs are alternately fixed to [P] or [N] for 90 ° depending on the polarity of the reference voltages. For example, during the period where $V_{ref\ A}$ is positive, $V_{ref\ A}$ is modified so that leg-A is clamped to [P] or leg-B is fixed to [N], where the clamping periods for each switching state are equally distributed during the fundamental period as shown in Fig. 2 (d). A more detailed explanation of ED²PWM can be found in [3]. Finally, the modified reference voltages for ED²PWM are expressed as

$$
\begin{aligned}
&(\text{if } V_{ref\_A} \geq 0)\\
&\quad [\text{for [P] Clamping of Leg-A}]\\
&\quad V_{ref\_ED^2PWM\_A} = V_{DC}/2\\
&\quad V_{ref\_ED^2PWM\_B} = V_{DC}/2 - V_{ref\_A} + V_{ref\_B}\\
&\quad [\text{for [N] Clamping of Leg-B}]\\
&\quad V_{ref\_ED^2PWM\_A} = -V_{DC}/2 + V_{ref\_A} - V_{ref\_B}\\
&\quad V_{ref\_ED^2PWM\_B} = -V_{DC}/2\\
&(\text{if } V_{ref\_A} < 0)\\
&\quad [\text{for [N] Clamping of Leg-A}]\\
&\quad V_{ref\_ED^2PWM\_A} = -V_{DC}/2\\
&\quad V_{ref\_ED^2PWM\_B} = -V_{DC}/2 - V_{ref\_A} + V_{ref\_B}\\
&\quad [\text{for [P] Clamping of Leg-B}]\\
&\quad V_{ref\_ED^2PWM\_A} = V_{DC}/2 + V_{ref\_A} - V_{ref\_B}\\
&\quad V_{ref\_ED^2PWM\_B} = V_{DC}/2
\end{aligned}
\tag{4}
$$

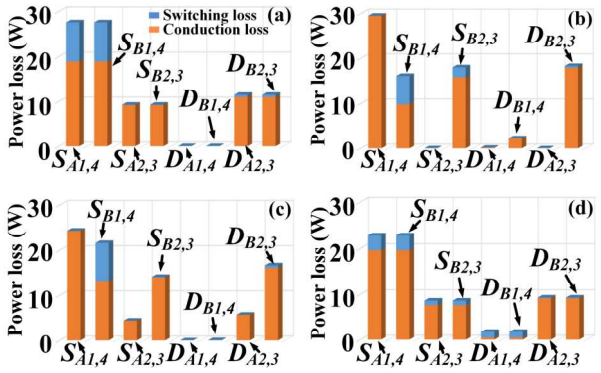

Fig. 3. Power loss distributions of T-type inverter at 7 kW with PWM methods: (a) UP-PWM, (b) OPC-DPWM (PN), (c) OPC-PWM (PON) and (d) ED²PWM

III. Analysis of Thermal Loadings of Power Devices and DC-Link Capacitors

The thermal loadings of the power devices and DC-link capacitors are comparatively evaluated with different PWM methods through the simulations under the following conditions: DC-link voltage (V_{DC}): 400 V, switching frequency (f_{sw}): 20 kH, DC-link capacitance (C_{DC}): 2200 μF, grid voltage (V_g): 220 V_{rms}, grid frequency (f_g): 60 Hz, filter inductor: 2 mH, rated output power (P_{out}): 7 kW, IGBT module: 10-12NMA040SH-M267F, DC-link capacitor: E93E451VN T222MCA5U.

A. Thermal loading of the power devices under different PWM methods

The junction temperatures (T_j) of the power devices is obtained as

$$T_j(t) = P_d(t) \cdot Z_{th(j-h)}(t) + P_m(t) \cdot Z_{th(h-a)}(t) + T_a$$
$$Z_{th(j-h)}(t) = \sum_{i=1}^{n} R_i (1 - e^{-t/\tau_i}) \quad (5)$$

where P_d = power loss of device, P_m = power loss of IGBT module, $Z_{th(h-a)}$ = heatsink to ambient thermal impedance, T_a = ambient temperature, $Z_{th(j-h)}$ = junction to heatsink thermal impedance, $\tau_i = R_i C_i$, R is the thermal resistance and C is the thermal capacitance at the number (i) of RC combinations for the Foster model [9]. The parameters of the thermal model can be obtained from the datasheet. $R_{th(h-a)}$ is set 0.18 K/W in order that T_j is about 70 % of the rated junction temperature at the rated power [10].

Under the UP-PWM, the power devices of two legs have symmetric power loss distributions, and $S_{A1,4}$ and $S_{B1,4}$ have higher power losses than the other devices as shown in Fig. 3 (a), and thus have the highest T_j of 104 °C as shown in Fig. 4 (a).

The power loss distribution under the OPC-PWM (PN) is shown in Fig. 3 (b), where it is assumed that the leg-A is clamped. Since the leg-A is clamped to [P] or [N] for the fundamental period, S_{A1} and S_{A4} have only conduction loss and their total power loss slightly increases. However, the power losses of the $S_{A2,3}$ and $D_{A2,3}$ notably decrease since no current flows through them. The T_j of the power devices of leg-A is illustrated in Fig. 4 (b). Because of the reduced total power loss of the IGBT

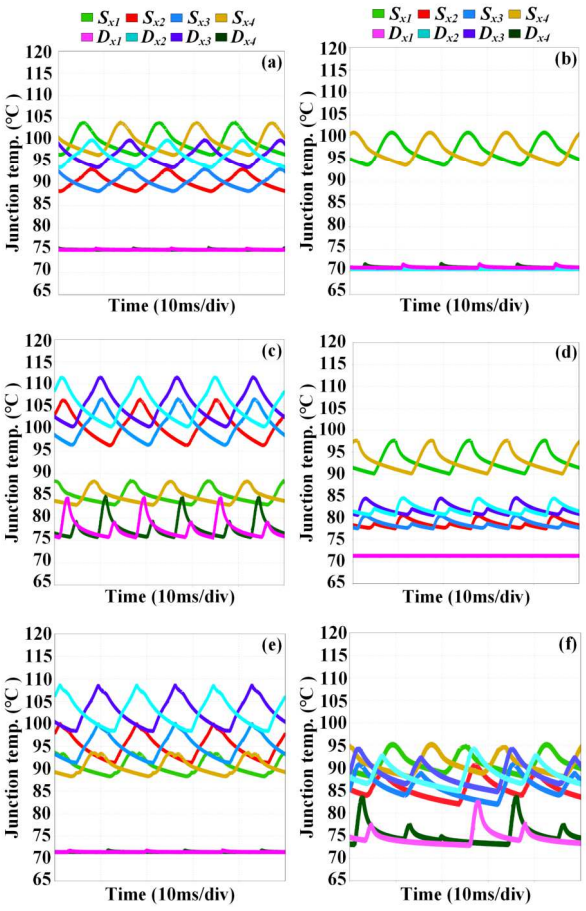

Fig. 4. Junction temperature of power devices of the T-type inverter at 7 kW with different PWM methods: (a) UP-PWM, (b) Leg-A with OPC-PWM (PN), (c) Leg-B with OPC-PWM (PN) (d) Leg-A with OPC-PWM (PON) (e) Leg-B with OPC-PWM (PON) (f) ED²PWM.

module, the T_j of all power devices is fallen compared with those under UP-PWM. Especially, there are large T_j drops in $S_{A2,3}$ and $D_{A2,3}$. In the case of leg-B, the period for the [O] increases since the modulation index of leg-B is reduced due to clamped leg-A. Therefore, the power losses of $S_{B2,3}$ and $D_{B2,3}$ increase but the power losses of $S_{B1,4}$ decrease. Consequently, the T_j of $S_{B2,3}$ and $D_{B2,3}$ increase, but the T_j of $S_{B1,4}$ decreases as shown in Fig. 4 (c), where $D_{B2,3}$ has the highest T_j of 111.2 °C.

Applying OPC-PWM (PON) results in similar power loss and T_j distributions with OPC-PWM (PN). However, since leg-A is fixed to not only [P] and [N], but also [O] for a certain period, the power loss of $S_{A1,4}$ a bit decreases, but the power loss of $S_{A2,3}$ and $D_{A2,3}$ increases as shown in Fig 3 (c). Therefore, a similar T_j distribution of leg-A is obtained as given in Fig. 4 (d). In the case of leg-B, the power loss of $S_{B2,3}$ and $D_{B2,3}$ is reduced, but the power loss of $S_{B1,4}$ increases, which leads to a decrease in the highest T_j of $D_{B2,3}$ from 111.2 °C to 108.8 °C as illustrated in Fig. 4 (e).

From the above results, it can be concluded that the application of two OPC-PWM methods causes asymmetric thermal loadings of power devices between two legs. It also increases the highest T_j compared with that under UP-PWM and the highest T_j under OPC-PWM (PN) is higher than that under OPC-PWM (PON).

The power loss and T_j distributions under ED²PWM are shown in Fig. 3 (d) and 4 (f), respectively. Since the clamping period is equally applied between two legs, they have balanced power loss distribution and thus T_j distribution between two legs. Furthermore, the highest T_j of $S_{A1,4}$ and $S_{B1,4}$ is reduced from 104 °C to 97.7 °C due to reduced switching loss.

The total power loss due to power devices under UP-PWM is 193.8 W and it is reduced to 170.1 W, 173.7 W, and 170.7 W, when OPC-PWM (PN), OPC-PWM (PON), and ED²PWM are applied, respectively.

B. Thermal loading of the capacitors with PWM methods

The hot-spot temperature (T_{hot}) of capacitors is associated with the power loss of capacitor (P_{cap}), ambient temperature (T_a) and thermal impedance as

$$T_{hot} = Z_{th} \cdot P_{cap} + T_a$$
$$P_{cap} = \sum_{h=1}^{n} \left(I_{C(RMS)}(f_h) \right)^2 \times R_{ESR}(f_h) \quad (6)$$

where Z_{th} is the thermal impedance from the hot-spot to the ambient environment, $I_{c(RMS)}(f_h)$ and $R_{ESR}(f_h)$ are the ripple current and the equivalent series resistance of the capacitor at a certain frequency (f_h), respectively. At the low frequency, the $R_{ESR}(f_h)$ is relatively higher than that at the high frequency [11]. Therefore, the magnitude and frequency of the ripple current play a major role in P_{cap} and thus T_{hot}. The related parameters to analyze the thermal loading of the capacitors are given in [11], [12].

Fig. 5 shows the operations of the T-type NPC inverter with different voltage vectors and their influence on the capacitor ripple current. Fig. 5 (a) and (b) show the inverter operation with a large voltage vector [PN] and zero voltage vector [OO], respectively. Under the [PN], the outputs are unconnected to neutral-point Z, and thus the current does not flow through Z. In the case of [OO], since two outputs are connected to Z, the current does not flow through Z. Under the P-type switching states of small voltage vectors such as [PO] as illustrated in Fig. 5 (c), the current flows into Z. Therefore, the lower capacitor voltage (V_{DC2}) is raised, but the upper capacitor voltage (V_{DC1}) is reduced. The N-type switching states such as [ON] make V_{DC1} increases, but V_{DC2} decreases because the current flows out from Z as shown in Fig. 5 (d). Consequently, the small voltage vectors affect the ripple current of the DC-link capacitors but the impact of the large and zero vectors is inconsiderable on the ripple current of the DC-link capacitors.

Fig. 6 shows the reference voltages and switching states of small voltage vectors which exist for the corresponding period under different PWM methods. The UP-PWM method has both P-type and N-type switching states of small vectors in a switching cycle for all periods as shown in Fig. 6 (a), and thus the polarity of the capacitor current is changed in a switching cycle. However, under the DPWM methods, there is only one type of the switching state of the small vector in a switching cycle and its type is maintained during a certain

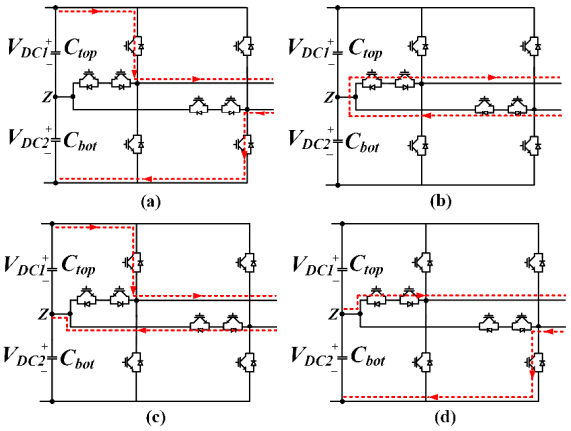

Fig. 5. The operation of voltage vectors in the T-type NPC inverter (a) large voltage vector [PN], (b) zero voltage vector [OO], (c) P-type switching state of small voltage vector [PO] (d) N-type switching state of small voltage vector [ON].

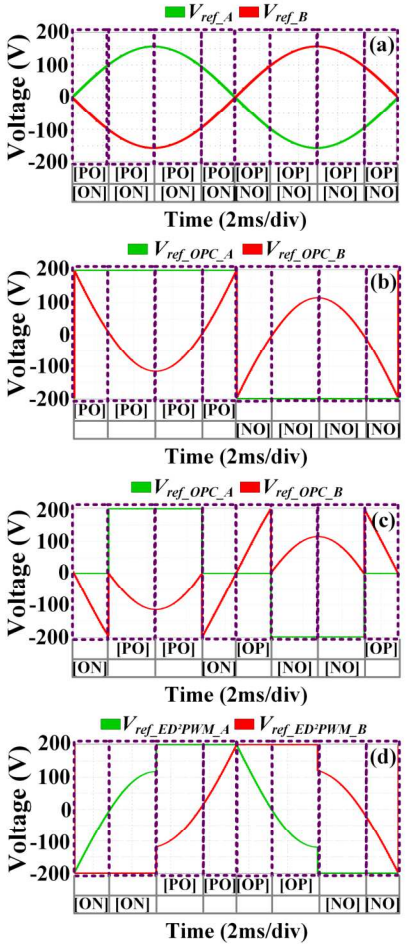

Fig. 6: The reference voltages and corresponding switching state of small voltage vectors in one switching cycle with different PWM methods (a) UP-PWM, (b) OPC-PWM (PN), (c) OPC-PWM (PON), and (d) ED²PWM.

clamping period as shown in Fig. 6 (b), (c), and (d), respectively. It means that the polarity of the capacitor current is not changed in a switching cycle. Consequently, the DC-link capacitors under the DPWM methods have higher ripple currents at low-frequency regions compared with those under the UP-PWM.

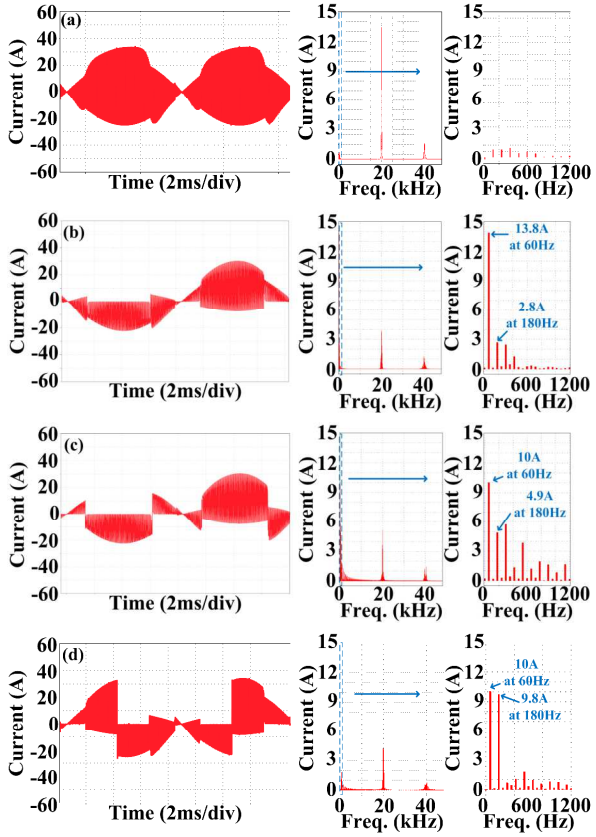

Fig. 7: The DC-link capacitor current and FFT analysis at 7 kW with different PWM methods (a) UP-PWM, (b) OPC-PWM (PN), (c) OPC-PWM (PON) and (d) ED²PWM.

When the OPC-PWM (PN) is applied, the type of the switching state of the small voltage vector is kept during half of the fundamental period as presented in Fig. 6 (b). It means that the polarity of the capacitor current is changed one time during the fundamental period. Under the OPC-PWM (PON), as shown in Fig. 6 (c), the type of the switching state of the small voltage vector is changed five times in the fundamental period. Therefore, it makes the polarity of the capacitor current change five times. It is varied twice under the ED²PWM as illustrated in Fig. 6 (d). Therefore, it can be expected that the OPC-PWM (PN) produces the highest low-frequency ripple components in the DC-link capacitor current, followed by ED²PWM and OPC-PWM (PON).

The currents of the upper DC-link capacitor and their FFT analysis results under considered four PWM methods are shown in Fig. 7, respectively. As expected, the DC-link capacitor has higher ripple currents at low-frequency regions when the DPWM methods are applied. The DC-link capacitor mainly has a ripple current at 20 kHz when UP-PWM is applied, where P_{cap} is 3.86 W. Under OPC-PWM (PN) as shown in Fig. 7 (b), the capacitor has ripple currents at low-frequency regions. It has the highest ripple current of 13.8 A at 60 Hz, which is the dominant current to P_{cap} since R_{ESR} has a relatively higher value and tends to decrease as the frequency increases. Therefore, P_{cap} increases by 7.16 W. It is seen that under OPC-PWM (PON), the ripple current at 60 Hz is reduced from 13.8 A to 10 A.

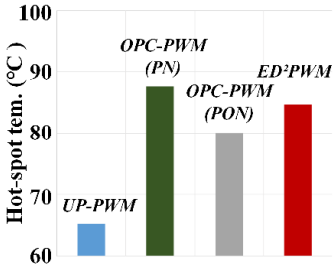

Fig. 8: Hot-spot temperature at 7 kW under different PWM methods.

Even though the ripple currents at other frequencies such as 180 Hz and 240 Hz are increased, the effect of the reduction in the ripple current at 60 Hz on P_{cap} is more significant. Therefore, it has a lower P_{cap} of 6.02 W compared with that under OPC-PWM (PN). In the case of ED²PWM, compared with OPC-PWM (PON), it has the same ripple current at 60 Hz but an increased ripple current at 180 Hz. Therefore, P_{cap} is 6.72 W, which is higher than that under OPC-PWM (PON) but lower than that under OPC-PWM (PN).

The corresponding T_{hot} is given in Fig. 8 under four PWM methods. The capacitor under UP-PWM has the lowest T_{hot} of 65.2 °C. It has the highest T_{hot} of 87.7 °C under OPC-PWM (PN) as analyzed and followed by T_{hot} of 84.7 °C under ED²PWM and T_{hot} of 80.1 °C under OPC-PWM (PON).

It is seen that the application of DPWM reduces the reliability of the DC-link capacitor due to increased T_{hot}.

IV. Experiments

To verify the analyzed results, the experiments are carried out under the following conditions: DC-link voltage (V_{DC}): 400 V, DC-link capacitors (C_{DC}): 2200 µF, Load (R-L): 40 Ω, 1.5 mH, and switching frequency (f_{sw}): 20 kHz.

Fig. 9 (a) shows the pole voltages (V_A and V_B), output voltage (V_{out}), output current (I_{out}) in the time domain and the capacitor current (I_c) in the frequency domain when UP-PWM is applied. The pole voltage of each leg, and output voltage have three levels and five levels, respectively, and the sinusoidal output current is generated. It is seen that the capacitor has a ripple current mainly at 120 Hz.

Under the OPC-PWM (PN), the pole voltage of leg-A is clamped to $V_{DC}/2$ or $-V_{DC}/2$ as shown in Fig. 9 (b). In the case of the OPC-PWM (PON), leg-A has not only $V_{DC}/2$ or $-V_{DC}/2$ but also 0 for a certain period as shown in Fig. 9 (c). Therefore, reduced switching loss can be expected under both OPC-PWM methods. The output voltage has five levels but it is seen that the output currents have more ripple components compared with UP-PWM because the switching frequency of the output voltage is reduced by half due to the clamping leg-A. The DC-link capacitor has additional ripple currents at 60 Hz and 180 Hz. Thus, it verifies that the DPWM methods lead to higher P_{cap} and thus higher T_{hot} due to higher ripple currents at lower frequency regions. Furthermore, under OPC-PWM (OPN), the capacitor has a smaller ripple current at 60 Hz compared with that under

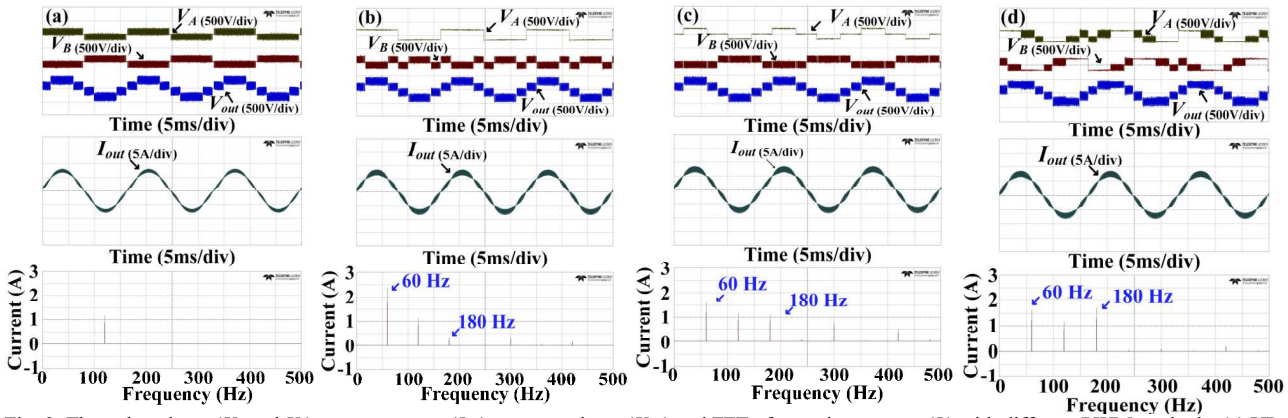

Fig. 9: The pole voltage (V_A and V_B), output current (I_{out}), output voltage (V_{out}) and FFT of capacitor current (I_c) with different PWM methods: (a) UP-PWM, (b) OPC-PWM (PN), (c) OPC-PWM (PON) (d) ED²PWM.

OPC-PWM (PN). Therefore, even though it has a higher ripple current at 180 Hz, the smaller P_{cap}, which means the lower T_{hot} can be expected as analyzed in the previous section since R_{ESR} has a higher value at 60 Hz than that at 180 Hz.

As illustrated in Fig. 9 (d), two legs are alternately clamped to [P] or [N] per 90 °, and thus they have the corresponding pole voltage of $V_{DC}/2$ or $-V_{DC}/2$ when ED²PWM is applied. Therefore, improved efficiency is also expected due to reduced switching loss. The output voltage also has five levels and the output current similar to that under OPC-PWM is obtained. In this case, the DC-link capacitor also has ripple currents at 60 Hz and 180 Hz. The magnitude of the ripple current at 60 Hz is almost the same, but the magnitude of the ripple current at 180 Hz is higher than those under OPC-PWM (PON). However, compared with those under OPC-PWM (PN), the ripple current at 60 Hz is smaller, but the ripple current at 180 Hz is higher. It results in higher power loss and thus higher T_{hot} compared with that under OPC-PWM (PN) but lower T_{hot} in comparison with that under OPC-PWM (PON) as analyzed in the previous section.

V. Conclusions

This paper investigates the influence of PWM methods on the thermal loadings of power devices and DC-link capacitors of a single-phase five-level T-type NPC inverter by considering the UP-PWM, and three different DPWM methods. The application of DPWM methods decreases the power loss of the power devices. OPC-PWM (PN) and ED²PWM have the best performance to reduce total power loss. However, OPC-PWM (PN) and OPC-PWM (PON) cause asymmetric T_j distribution between the two legs. Furthermore, the highest T_j among the power devices increases compared with that under UP-PWM. On the other hand, under ED²PWM, the highest T_j is reduced compared with the highest T_j under UP-PWM, and the T_j distributions between the two legs are also identical. Therefore, ED²PWM is the most effective to improve the reliability of power devices through T_j reduction. The DPWM methods introduce a significant power loss in the DC-link capacitor due to the high amplitude of low-frequency ripple current which leads to an increase in T_{hot}. Therefore, they reduce the lifetime of the DC-link capacitor. OPC-PWM (PON) is the most effective DPWM method among the three DPWM methods when the reliability of the DC-link capacitor is considered since the increase in T_{hot} is the smallest.

Applying DPWM methods has different effects on the thermal loadings of power devices and DC-link capacitors. Therefore, their reliability needs to be considered in addition to other performance metrics such as power loss and power quality when selecting the PWM methods.

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