Turn-on Losses Optimization for Medium Power SiC MOSFET

Half-bridge Module

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Abstract

This paper explains the mechanism of the parasitic turn-on (PTO) effect in a medium power SiC MOSFET half-bridge module and the relation between it and the reverse-recovery process of MOSFET's body diode. Based on that knowledge, a detail practical turn-on losses optimization process for medium power SiC MOSFET modules using PTO is presented. To quantify the stability of this method, some quantitative metrics are suggested to measure the critical values' sensitivity. The experimental measurements show that turn-on losses can be reduced 50% lower than conventional R_{gon} tuning method.

Introduction

The turn-on speed of a SiC MOSFET half-bridge module is limited by the overvoltage of its body diode during reverse-recovery which is the consequence of the commutation's loop stray inductance and the reverse-recovery current speed. In a conventional approach, a higher gate resistance is used to reduce the turn-on speed and hence protect the device from overvoltage [11]. The price for this protection is the higher turn-on losses on the MOSFET due to slower turn-on speed. This paper shows an effective process to achieve lower turn-on losses for a MOSFET half-bridge module which takes advantage of parasitic turn-on effect. The method was introduced in [1] for discrete chips with scale inductance but there was no explanation about the mechanism behind the method which is very important to understand the boundary conditions and also pros and cons of using parasitic turn-on effect.

Parasitic turn-on (PTO) is a complex effect which depends on many different parameters. To control PTO safely without destructing the module, it is necessary to have some metrics to quantify the risk of the module's destruction. There are two main destruction mechanisms: overvoltage of the MOSFET and the shoot-through which is presented by critical reverse-recovery losses. The overvoltage and the reverse-recovery energy are called critical parameters and their relationship with the PTO's control parameters are quantified by sensitivity factors. The optimization process is secured by selecting the lower sensitivity factor zones and proper safety margins for the overvoltage and threshold voltage. The experimental demonstration of the optimization process is also presented in this paper.

1. PTO in SiC MOSFET half-bridge modules

The double pulse test setup is shown in Fig. 1 with more detail of T31 parasitic elements. These capacitors C_{gd}, C_{gs}, C_{ds} are MOSFET T31's internal capacitors. L_{sin}, L_{sext} are the internal, external stray inductance of the source terminal of T31. L_{gin} and R_{gin} are T31's internal gate inductance and resistance. Lp is stray inductance between DC link voltage source and the MOSFET modules. According to [2], there is a magnetic coupling Mg in the SiC MOSFET module between T31's gate network circuit and $\frac{di_{ds}}{dt}$ of T32. The voltage induced by the magnetic coupling can be added or subtracted to T31's gate voltage depends on the internal structure of the device and is different from manufacturers to manufacturers. Double pulse test (DPT) is applied on the lower MOSFET T32, the upper MOSFET T31 is off at adjustable gate voltage v_{gsoff}. The voltage and current across T31 (v_r, i_r) were measured to calculate reverse-recovery energy E_{rr}. The voltage and current across T32 (v_{ds}, i_{ds}) were measured to calculate turn-on energy E_{on} of T32. The parasitic turn-on happens at T31 when its body diode is turned off by turning on T32. When the load current i_L is taken over by T32, the voltage across T31 is raising at speed $\frac{dv_r}{dt}$. The displacement current i_{gd} of C_{gd} then flows through the gate i_g and also C_{gs}, pulling up T31's gate voltage. T31's gate voltage at this time can be modeled by the equation (1):

$$v_{gsoff} = -(R_{goff} + R_{gin})i_g - (L_g + L_{gin})\frac{di_g}{dt} + v_{gs} - L_{sin}\frac{di_r}{dt} + M_g\frac{di_{ds}}{dt} \quad (1)$$

$$i_{gd} = i_g + i_{gs} \leftrightarrow i_g = C_{gd}\frac{dv_r}{dt} - (C_{gs} + C_{gd})\frac{dv_{gs}}{dt} = C_{gd}\frac{dv_r}{dt} - C_{iss}\frac{dv_{gs}}{dt} \quad (2)$$

In case of having low gate inductance and low internal gate resistance, equation (1) can be approximated:

$$v_{gs} = v_{gsoff} + R_{goff} \cdot \left(C_{gd}\frac{dv_r}{dt} - C_{iss}\frac{dv_{gs}}{dt}\right) - (M_g + L_{sin}) \cdot \frac{di_{ds}}{dt} \quad (3)$$

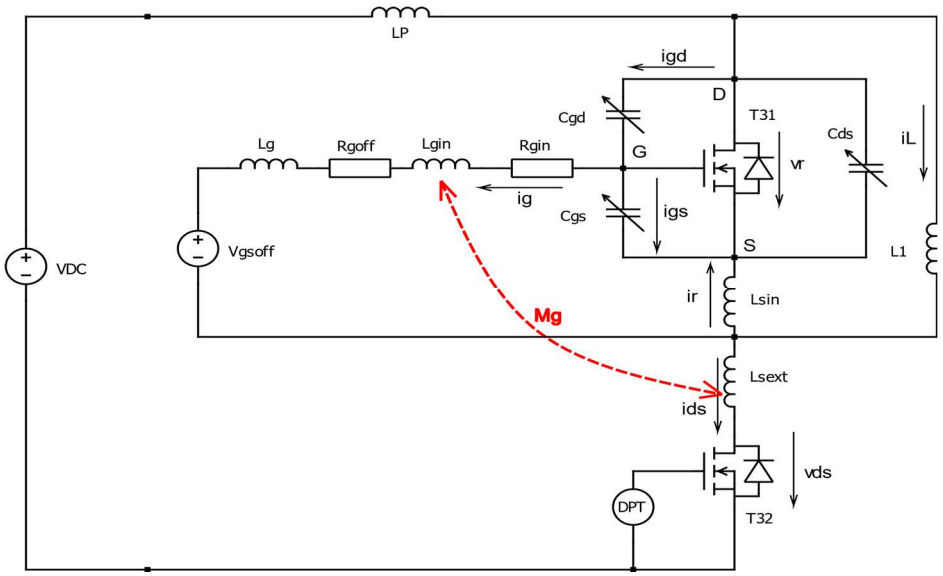

Fig 1: Medium power SiC MOSFET half-bridge double pule test set-up with detail T31 parasitic elements and magnetic coupling Mg between T31's gate circuit network and $\frac{di_{ds}}{dt}$ of T32

When the induced gate voltage of T31 is larger than the threshold voltage $v_{gs} > v_{th}$, PTO happens. Equation (3) is a combination of 3 components: v_{gsoff} is the static component, the voltage dynamic component: $R_{goff}\left(C_{gd}\frac{dv_r}{dt} - C_{iss}\frac{dv_{gs}}{dt}\right)$ and the current dynamic component: $-\left(M_g + L_{sin}\right)\frac{di_{ds}}{dt}$.
If we look at the current dynamic part of equation (3), some interesting effect can be seen. When T32 is turned on, the current go through it always has $\frac{di_{ds}}{dt} > 0$. If the module has a positive magnetic coupling M_g, the current dynamic component of (3) is larger at faster turn-on speed (smaller R_{gon}) and hence reduce the parasitic turn on effect on T31. There is also the case when the module has a negative magnetic coupling [2], it will increase the T31's parasitic turn-on. The parasitic inductance on the source terminal L_{sin} also helps to reduce parasitic turn-on of T31. Hence the module without Kelvin connector has a positive effect on preventing parasitic turn-on. The voltage dynamic component depends on R_{goff} , C_{gd}, C_{iss}. Small R_{goff} , C_{gd} reduce the effect of dynamic voltage component. The static and current dynamic component are user controllable by changing v_{gsoff} and R_{gon} .The voltage dynamic component is a user uncontrollable part. This means the setup which has low R_{goff} , C_{gd} and high C_{iss}, $M_g + L_{sin}$ has more user control ability or user can control PTO more easily.

2. Reverse-recovery of SiC MOSFET's intrinsic body diode

There are three stages in the reverse-recovery of SiC MOSFET's body diode that can be seen in Fig 2. At the first stage, when T32 is turned on, the T31's body diode forward current starts decreasing until zero. At the second stage, the diode enters the reverse-biased state, its current continues flowing in reverse direction at the speed di_{rf}/dt because there are still a lot of carriers in the n- drift layer need to be swept out. When the reverse current reaches its peak value Irr, the depletion layer starts to form, the diode enters its third stage. When the depletion starts to expend, the drain-source voltage vr increases to the blocking voltage, the amount of carrier needing to be swept out of the depletion region also reduces and hence the reverse current also reduces at the speed di_{rr}/dt. In this stage, high dvr/dt can cause parasitic turn-on. Depending on the stray inductance of the external circuit (LP), the peak voltage over T31 at this stage is:

$$v_r = VDC - LP \cdot \frac{di_{ds}}{dt} = VDC + LP \cdot \frac{di_{rr}}{dt} \quad (4)$$

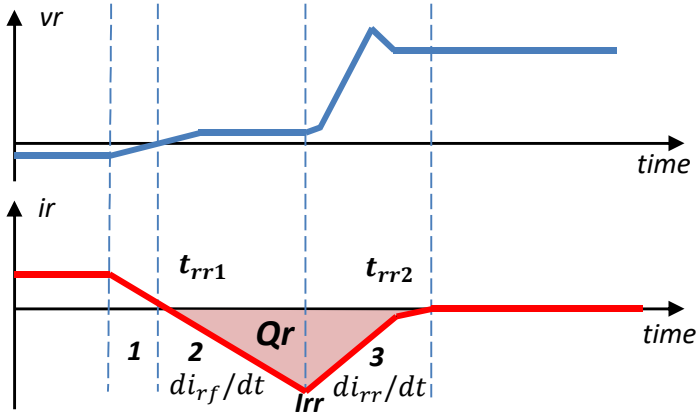

Fig 2: Reverse-recovery waveform of SiC MOSFET intrinsic body diode.

Apart from the overvoltage cause by di_{rr}/dt, T31 also encounters the oscillation from the combination of external stray inductance LP and the output capacitor C_{oss} of T31 (Fig 3.), the total voltage on T31 is:

$$v_r = VDC + LP \cdot \frac{di_{rr}}{dt} + \sqrt{\frac{LP}{C_{oss}}} \cdot I_L \cdot \sin(\omega t + \theta) \cdot e^{-\omega \tau t} \quad (5)$$

With IL is the load current at the turn-on moment. $\omega \approx \frac{1}{\sqrt{LP.C_{oss}}}$ is the angle frequency of the oscillation, τ is the oscillation damping factor. R_P is the parasitic resistance of the external circuit. R_{bd} is the series resitance of the body diode in the drift region which can be seen in Fig 3.

$$\tau = \frac{R_P + R_{bd}}{2} \sqrt{\frac{C_{oss}}{LP}} \quad (6)$$

At high junction temperature, the life time of the minority carriers in the drift region is longer [6,7,8] and hence the intrinsic carrier concentration in drift region is higher. That means the body diode's series resistance R_{bd} is lower at higher temperature [6]. Consequently, the turn-on oscillation is poorly damped and hence more overvoltage on the body diode has. For many medium power module applications, the modules are connected by a busbar which has a long commutation loop and a large parasitic inductance. The reverse-recovery oscillation becomes more severe in this scenario, especially at high current and high junction's temperature.

3. Parasitic turn-on and the reverse-recovery oscillation damping

From the damping factor of the reverse-recovery oscillation which is described in equation (6), to damp the oscillation, R_{bd} should be increased to have bigger damping factor. Since R_{bd} depends on the concentration of intrinsic carriers in the drift layer [6], R_{bd} can be increased by reducing the concentration of the intrinsic carriers in the drift layer. According to [9] this can be done by increasing the off-state gate voltage of T31. At higher gate voltage, the channel's resistance gets lower, a portion of charges in the drift region will be attracted to the channel area and hence temporarily reduces the charge concentration near by the body diode (Fig 3.). The same experiment result can be found in [10].

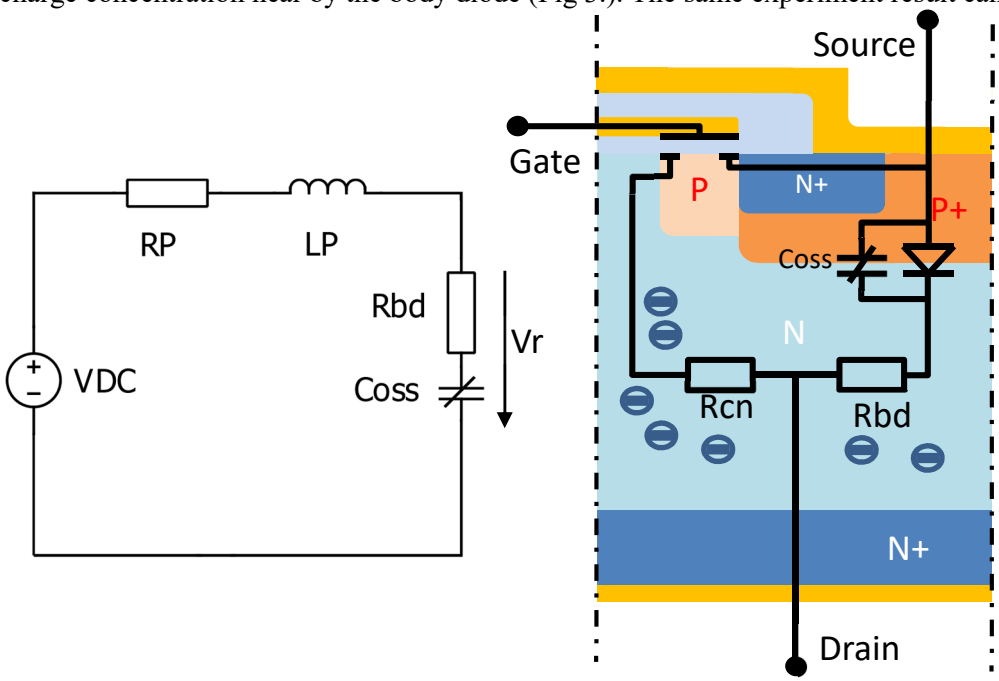

Fig 3: Cross section of power MOSFET with its intrinsic body diode, internal resistance and the oscillation circuit formed together with the external stray inductance LP.

In literature [9,10], the gate voltage is increased but not excess the threshold voltage. Hence, there were no parasitic turn-on. With parasitic turn-on, when the gate voltage excesses the threshold voltage for a short time only in the third stage of the reverse-recovery, the channel is partially opened and its

resistance is decreased more than without PTO. This leads to further increase the body diode's series resistor R_{bd}, it consequently increases the damping factor and hence reduces further the overvoltage on T31. Too much parasitic turn-on (when the channel is completely opened or goes into the low ohmic region) can lead to huge reverse-recovery losses and may destroy the device. But if PTO is used in a controlled way such as adjusting the R_{bd} just enough to damp the oscillation to reduce the overvoltage, The R_{gon} of T31 can be lowered .This leads to a faster turn-on with much less turn-on losses and only slightly higher reverse-recovery losses. Fig 4. shows the voltage and current across the body diode during reverse-recovery process at 900VDC, 400A load current, 150°C junction temperature with different turn-off gate voltage v_{gsoff} = [-7, -3, -2, -1] V. It can be seen that during the third stage of the recovery process, when the depletion layer starts to form, the voltage vr fast increases at speed $\frac{dv_r}{dt}$ and starts oscillating. Because of high $\frac{dv_r}{dt}$, the gate voltage of T31 is parasitically turned on and hence reduces MOSFET T31's channel resistance. The charge carriers in drift region are now attracted to the area near to the channel and then temporarily reduce the charge concentration in the drift region near to the body diode. Because of less charge carrier concentration, the series resistor of the body diode is temporarily increased and damps the oscillation, the higher v_{gsoff} is, the better vr is damped. The overvoltage on T31 is further reduced when increase v_{gsoff}.

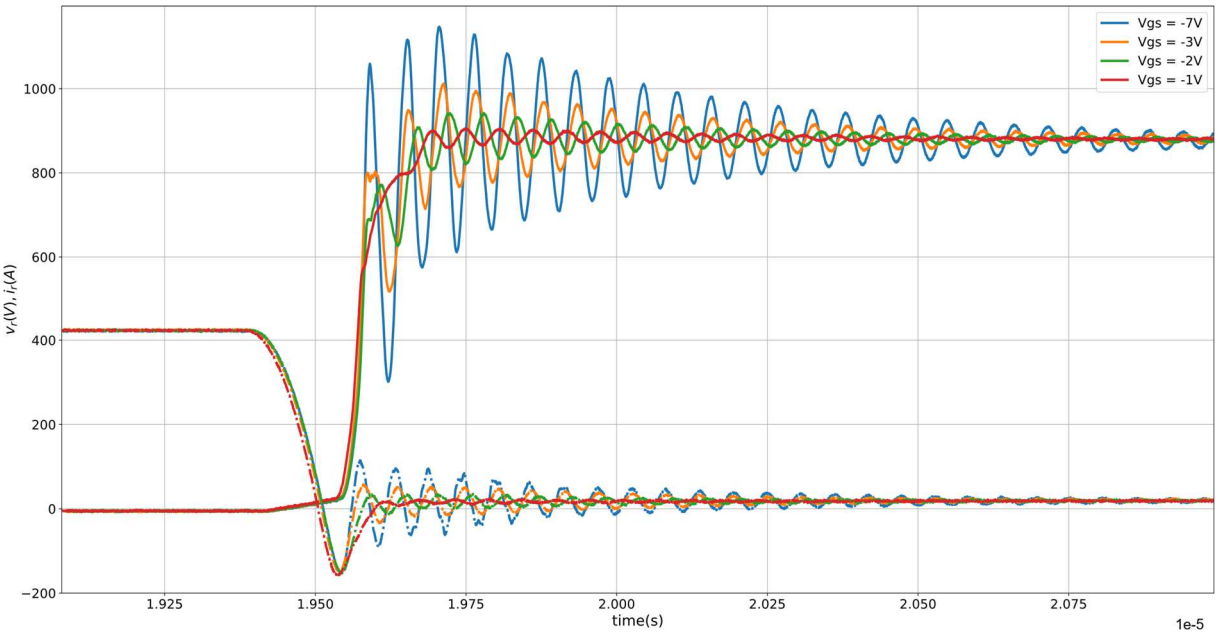

Fig 4: The reverse-recovery oscillation's damping effect of the body diode's series resistance R_{bd} at different v_{gsoff} which were measured at 150°C.

4. Turn-on losses optimization process

As mentioned in section 2 and 3, when there is a large external parasitic inductance and high load current, the oscillation amplitude becomes the major part of the overvoltage of the body diode during reverse-recovery. This oscillation can be damped by increasing the body diode's series resistance R_{bd} using the parasitic turn-on effect. In other cases, when there is a low external stray inductance and low load current, the parasitic turn-on has no positive effect on optimizing turn-on losses because the overvoltage is dominated by reverser-recovery current speed $\frac{di_{rr}}{dt}$. This is also the limitation for this optimization method.

Section 1 shows how the user can control the PTO by changing v_{gsoff} and R_{gon} . To increase the user's PTO control ability, R_{goff} should be small enough to have more independence from the voltage

dynamic component. If the stray inductance LP is too large, active clamping or a decoupling capacitor may be used to further reduce R_{goff} .

The first step in the optimization process is finding the range of the controllable variable v_{gsoff} and R_{gon} . To do this, a double pulse test is set up. To find the controllable range of R_{gon} ,first the v_{gsoff} should be set low enough to ensure that there is no parasitic turn-on. The user should keep the tolerance of the gate's oxide in mind while reducing v_{gsoff}. A conventional R_{gon} tuning process should be carried out to get the minimum value of $R_{gon} = Rn_{gon}$, which ensures the over voltage on T31 $Vrmax$ stay inside the safe operating area (SOA) of the MOSFET. The total turn-on energy and reverse-recovery energy $E_{summax} = E_{rr} + E_{on}$ should be recorded to have a threshold for the optimization process. The optimization process is only meaningful when the total turn-on losses is smaller than the conventional R_{gon} tuning. when using PTO to optimize losses, R_{gon} can be further reduced. So Rn_{gon} is the maximum value of R_{gon} . The minimum value R_{gonmin} is limited by the application's maximum turn-on speed. After this step, the user should have $R_{gon} \in [R_{gonmin}, Rn_{gon}]$.

To find the v_{gsoff} control range, the gate's voltage of T31 should be measured and recorded during double pulse test with different v_{gsoff} voltages. The double pulse test in this case has to be done at the maximum junction temperature of the device since the overvoltage gets worst at high temperature. The lowest value $v_{gsoffmin}$ is the value, at which, the induced gate's voltage of T31 is equal to the threshold voltage of the MOSFET when turning on T32 at $R_{gon} = Rn_{gon}$. The maximum $v_{gsoffmax}$ should be closed to the threshold voltage of the MOSFET, but the user should have some safety margin for this value to avoid shoot-through. The control range of v_{gsoff} is now defined in the range $[v_{gsoffmin}, v_{gsoffmax}]$.

At the second step, the user should discretize the control parameters range into $R_{gon} \in [R_{gonmin}, R_{gon1}, R_{gon2}, \dots Rn_{gon}]$ and $v_{gsoff} \in [v_{gsoffmin}, v_{gsoff1}, v_{gsoff2}, \dots v_{gsoffmax}]$. The number of points depend on the user's choice. A large number of points may create more measurements but give more accurate result.

As the third step, double pulse testes in worst case scenario of the operation (maximum junction temperature, maximum DC link voltage and maximum load current) are made for each combination of v_{gsoff}, R_{gon} and the total turn-on energy and reverse-recovery energy $E_{sum} = E_{rr} + E_{on}$should be recorded to compare with the threshold E_{summax} that has been measured in the first step.

At the last step, the parameter's sensitivity should be calculated to identify the stable zone of the method. The sensitivity factors are defined in the next section.

5. Parameters' sensitivity factors

During the turn-on process with parasitic turn-on effect, the overvoltage of T31 Vrmax and the reverse-recovery energy E_{rr} are the critical values, which are directly related to the module's destruction. These values should not be too sensitive with the control parameters. This means some small changes in the application's parameters, because of temperature or components' tolerance…, should not change much the critical values to assure a stable operation. To quantify this stability, four sensitivity factors are introduced:

$$S_{EV} = \frac{\partial E_{rr}}{\partial v_{gsoff}} \; for\ discrete\ value\ is\ \frac{\Delta E_{rr}}{\Delta v_{gsoff}} \tag{7}$$

$$S_{ER} = \frac{\partial E_{rr}}{\partial R_{gon}} for\ discrete\ value\ is\ \frac{\Delta E_{rr}}{\Delta R_{gon}} \tag{8}$$

$$S_{VV} = \frac{\partial V_{rmax}}{\partial v_{gsoff}} for\ discrete\ value\ is\ \frac{\Delta V_{rmax}}{\Delta v_{gsoff}} \tag{9}$$

$$S_{VR} = \frac{\partial V_{rmax}}{\partial R_{gon}} for\ discrete\ value\ is\ \frac{\Delta V_{rmax}}{\Delta R_{gon}} \tag{10}$$

S_{EV}, S_{ER} measure how sensitive the reverse-recovery energy E_{rr} to v_{gsoff} and R_{gon} respectively.

S_{VV}, S_{VR} measure how sensitive the body diode's overvoltage Vrmax to v_{gsoff} and R_{gon} respectively.

6. Experimental result

To demonstrate the optimization process, an experimental testbench is set up like in Fig 1. The device under test is a 1200V-375A, 62mm SiC MOSFET module. The module has no Kelvin connector, so there is a slop on vr's measurement during ir falling. The double pulse test setup (Fig 1.) has 26nH external inductance together with 20nH internal module's stray inductance. The worst case scenario is defined at 900VDC link voltage, 600A load current and 150°C junction temperature. All the differential voltage probes and Rogowski coil current probes are properly calibrated and de-skewed. At the first and second step of the optimization process, the conventional R_{gon} tuning process was done with $v_{gsoff} = -5V$ and having no parasitic turn-on involved. The smallest Rn_{gon} = 4.7 Ω, at maximum overvoltage on T31 is $Vrmax$ = 1175V (safety margin is 25V below 1200V), $R_{goff} = 2\Omega$. The total energy losses in this case was $E_{summax} = E_{rr} + E_{on}$ = 37 mJ. R_{gon} range chosen for the optimization is $R_{gon} \in [0, 1, 2, 2.9]$. When turning on T32 with R_{gon} = 4.7 Ω and adjusted $v_{gsoff} = -4.4V$, the parasitic turn-on gate voltage measured on T31 was equal to the MOSFET threshold voltage $v_{th} = 4.5V$. The $v_{gsoffmax}$ was chosen to -1V with a safety margin of 5.5 V below the threshold voltage v_{th}. v_{gsoff} was discretized into 8 points:
$v_{gsoff} \epsilon [-4.4, -4, -3.5, -3, -2.5, -2, -1.5, -1](V)$.
At the third step, the double pulse measurements at worst case scenario for 32 combinations of v_{gsoff} and R_{gon} were made. The total energy $E_{sum} = E_{rr} + E_{on}$ and T31's overvoltage $Vrmax$ were recorded and compared to the conventional R_{gon} tuning. The result is displayed in Fig 5.

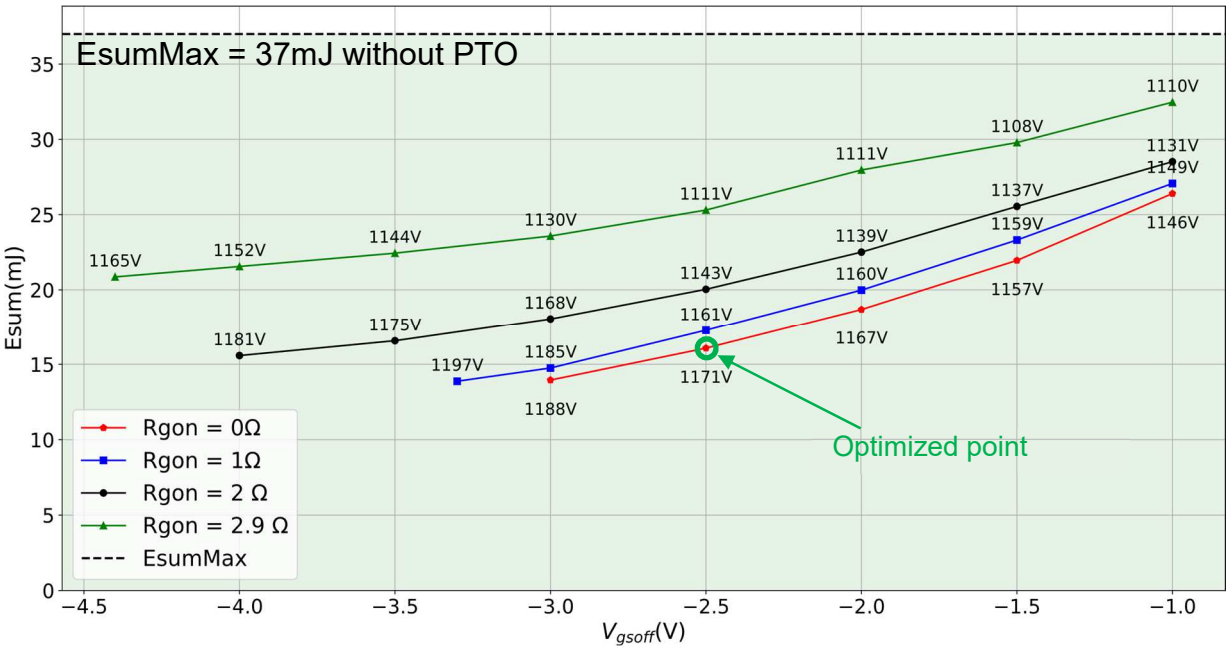

Fig 5: Total turn-on energy E_{sum} with different combination of v_{gsoff},R_{gon}. The body diode's overvoltage Vrmax is marked at each measurement point. The green area depicts the total turn-on losses E_{sum}that can be further optimized compare to $E_{summax} = 37$ mJ conventional turn-on.

The optimal turn-on energy $E_{sum} = 16\ mJ$ was found at $R_{gon} = 0\Omega$ and $v_{gsoff} = -2.5V$ where the overvoltage of T31 $Vrmax$ = 1171V is still below the safety margin.

At the last step, the discrete sensitivity factors $S_{EV}, S_{ER}, S_{VV}, S_{VR}$ are calculated. The example calculation for discrete S_{EV} is showed in table I. The same manner is applied for the other sensitive factors.

Table I: Example of calculating discrete sensitivity $S_{EV}(\frac{mJ}{V})$ factor.

$v_{gsoff}(V)$	Err(mJ)	$S_{EV}(mJ/V)$
-3	12.45	$S_{EV} = \frac{14.5 - 12.45}{-2.5 - (-3)} = 4.1$
-2.5	14.5	
-2	17.2	$S_{EV} = \frac{20.4 - 17.2}{-1.5 - (-2)} = 6.4$
-1.5	20.4	

The results of the calculation are displayed in Fig 6.,7.,8.and 9. It can be seen in Fig 6. That the reverse-recovery energy E_{rr} is less sensitive at lower v_{gsoff} values. At higher v_{gsoff}, the parasitic turn-on gets worse and hence increases the E_{rr} faster than at lower v_{gsoff}.

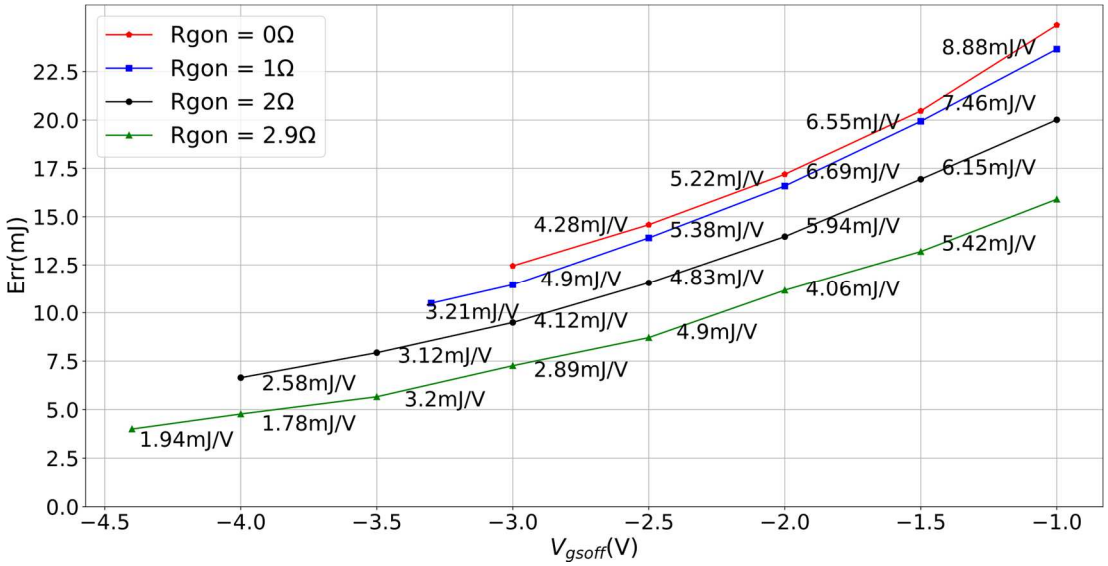

Fig 6: Reverse-recovery energy E_{rr} is less sensitive at lower v_{gsoff} range. The sensitivity factor S_{EV} is also marked on the graph.

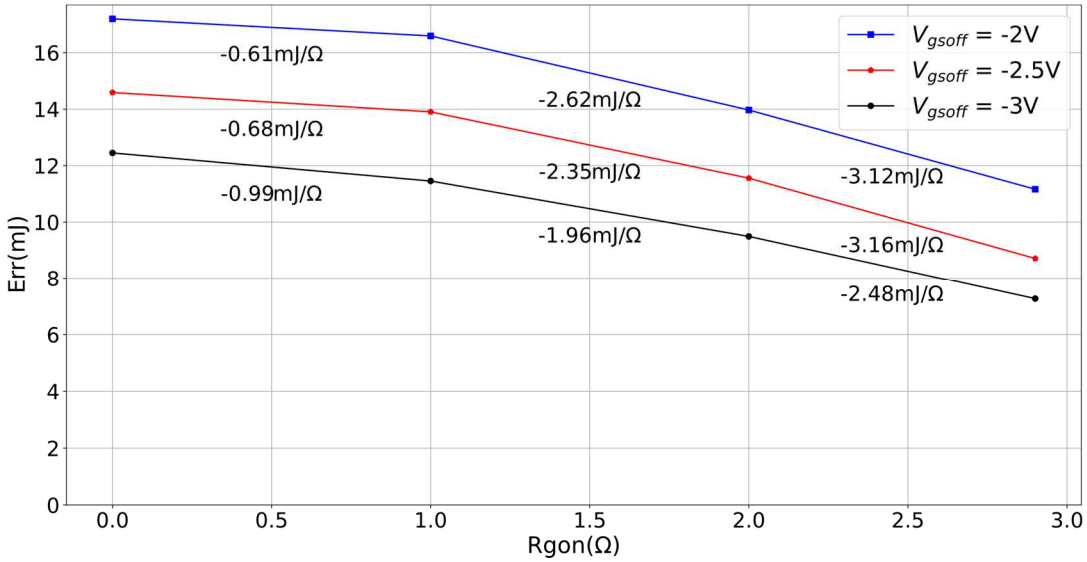

Fig 7: Reverse-recovery energy E_{rr} is less sensitive at lower R_{gon} range. The sensitivity factor S_{ER} mJ/Ω is marked on the graph.

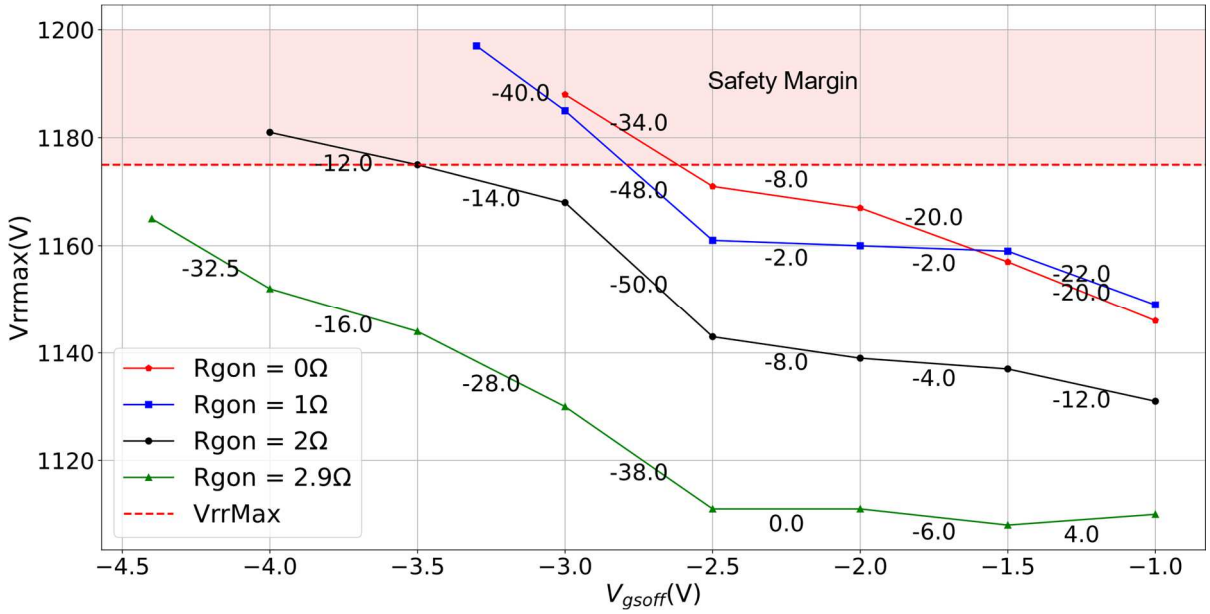

Fig 8: Body diode's overvoltage Vrmax is less sensitive at higher v_{gsoff} range. The sensitivity factor S_{VV} is also marked on the graph

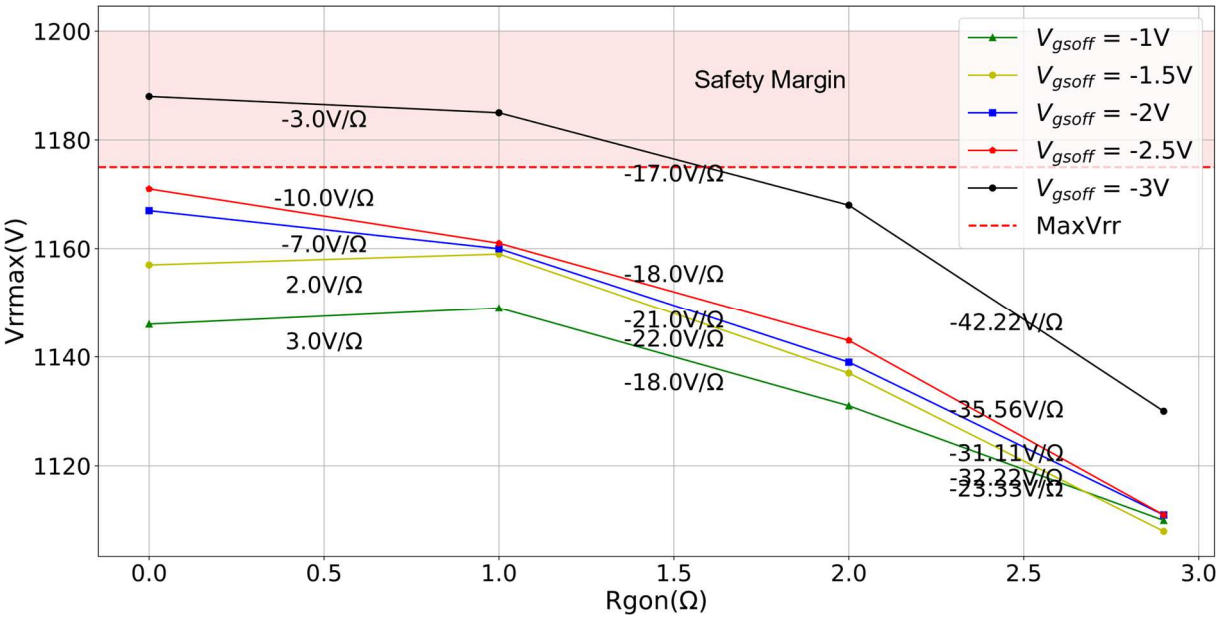

Fig 9: Body diode's overvoltage Vrmax is less sensitive to lower R_{gon} range. The sensitivity factor S_{VR} V/Ω is also marked on the graph.

In Fig 7, the reverse-recovery energy E_{rr} is less sensitive at lower R_{gon} range because in equation (3), when the dynamic current component has a positive $M_g + L_{sin}$, at high turn-on speed (lower R_{gon}), T31 has less parasitic turn-on so E_{rr} less sensitive at lower R_{gon} range. In Fig 8, the body diode's overvoltage $Vrmax$ is less sensitive at higher v_{gsoff} range, because the oscillation is suppressed by high resistance of R_{bd}. In Fig 9, the body diode's overvoltage $Vrmax$ is less sensitive to lower R_{gon} range because at the same v_{gsoff}, the R_{bd} value does not change much, the over voltage of the body diode is dominated by $LP \cdot \frac{di_{rr}}{dt}$ from equation (5). At low switching speed, a certain number of

charges in the drift region are recombined before they are swept out [9]. This phenomenon makes the $\frac{di_{rr}}{dt}$ more sensitive at slow turn-on speed than at fast turn-on speed, hence the $Vrmax$ is less sensitive in the lower R_{gon} range (Fig 10.).

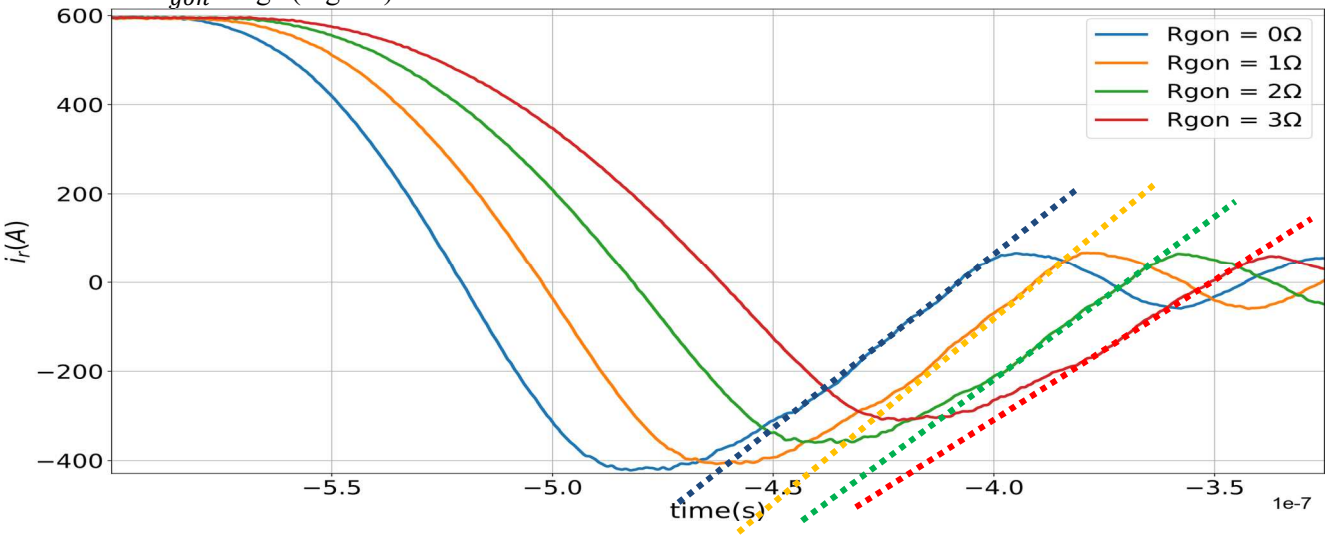

Fig 10: Reverse-recovery current speed $\frac{di_{rr}}{dt}$ is more sensitive at slow turn-on speed (red and green lines) than high turn-on speed (blue and orange lines) at the same v_{gsoff}

From the calculated sensitivities above there is a trade off between low and high v_{gsoff}. Low v_{gsoff} gives a stable E_{rr} but high-sensitive $Vrmax$. v_{gsoff} should be chosen with high priority to have a stable $Vrmax$ and less E_{rr}. After considering all the quantitative stability above, the lowest and stable turn-on losses can be optimized with the PTO method is 16mJ at $R_{gon} = 0\Omega$, $v_{gsoff} = -2.5V$, more than 50% lower than the case without parasitic turn-on effect. Fig 11. shows the low total turn-on losses and the reverse-recovery losses of the proposed optimization method versus the losses of a conventional R_{gon} tuning at different operating points.

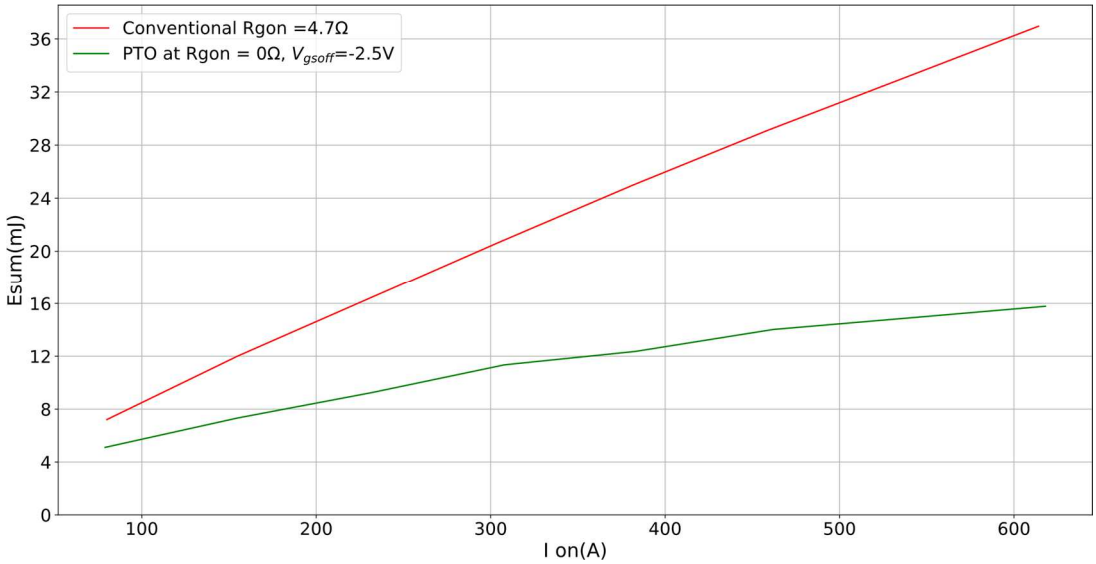

Fig 11. Comparison of total turn-on losses Esum = Err + Eon of the proposed method and the conventional R_{gon} tuning method at different operation points

Conclusion

The paper has shown the principle mechanism behind the parasitic turn-on effect and its relation with the reverse-recovery of the intrinsic body diode of SiC MOSFET in the half-bridge module. Also a step by step process to optimize turn-on losses using parasitic turn-on effect was introduced and demonstrated with experimental measurement. The results show, that the turn-on losses can be reduced by more than 50% compare to the conventional tuning method. The optimization point was selected at the less sensitive zone of the control parameters to ensure a safe turn-on.

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