Analysis and Discussion of Different Three-Phase dv/dt Filter Topologies and the Influences of Their Filter Parameters on Losses and EMC

[1]Eric Fritze, [1]Michael Meissner, [1]Klaus F. Hoffmann,
[1]Kai-Uwe Rathjen, [1]Stefan Dickmann, [2]Oliver Woywode
[1]HELMUT SCHMIDT UNIVERSITY
[2] PHILIPS MEDICAL SYSTEMS DMC GMBH
[1]Holstenhofweg 85
[1]Hamburg, Germany
Phone: +49 (0) 40 6541 2713
Fax: +49 (0) 040 6541 2018
Email: eric.fritze@hsu-hh.de
URL: https://www.hsu-hh.de/lek/en/

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Keywords

≪Passive filter≫, ≪EMC/EMI≫, ≪Wide bandgap devices≫, ≪Reliability≫, ≪Efficiency≫, ≪Electrical machine≫, ≪Automotive application≫, ≪Converter machine interactions≫.

Abstract

In this paper two modified three-phase dv/dt filter networks are analysed. They're investigated in a fast switching SiC-MOSFET inverter system with the primary purpose of reducing the steep voltage slopes caused by the wide bandgap semiconductor devices at the output of the inverter. This should preserve the insulation system of a connected electrical load machine from partial discharges and deterioration. The necessity of damping down the voltage slopes outside of the inverter can arise from the possibility of lower switching losses and more favourable temperatures within the inverter. An additional filter of course will cause power losses depending on it's parameters. Hence, the influence of the passive filter parameters on those losses are an integral part of the analysis. In addition to the slope-damping of the inverter output voltage, the two discussed filter topologies should also challenge the conducted EMI of the system. Therefore, both of the circuits use special modifications to reduce the interference levels introduced by the fast switching inverter. Furthermore, a diode clamping of the filter output voltage to the DC-link potentials is implemented and it's impact on the dv/dt reduction, filter losses and EMI is discussed. Generally, a higher filter inductance, meaning a lower necessary capacitance, will reduce the extra filter losses at the expense of a higher filter volume as well as additional oscillations of the output voltage. The diode clamping leads to a significantly less overshoot and ringing of the resulting voltages, but to an increase of the measured losses. Finally, examining the influences of the different filter topologies, their parameters and the diode clamping on the conducted EMC behaviour, it will be shown that both of the modified topologies have the ability to reduce EMI levels in certain areas.

Introduction

The development and commercial availability of wide bandgap devices based on e. g. silicon carbide (SiC) and gallium nitride (GaN) enhances the possibilities of designing more efficient, compact and

high-performance systems. Due to higher switching speeds, lower switching losses combined with low on-resistance and higher thermal conductivity, both high-temperature applications and high switching frequencies can be addressed as well [1, 2]. The wide field of applications empowers their usage in DC-DC converters and DC-AC traction inverters, for example in the automotive industry.

However, the combination of modern fast switching inverter topologies and electric machines recently causes several technical challenges, such as cable reflection phenomena due to long stator cables and problems concerning EMI, shaft voltages and bearing currents [3, 4]. But also using short cable lengths, the permitted rise times of the inverter output voltages have to be limited to prevent partial discharges and premature insulation failure of the electric machines' stator windings [5]. One way to face those problems while maintaining high switching speeds of the used semiconductors and favoring lower power loss-based heating are $\mathrm{d}v/\mathrm{d}t$ filter networks in order to damp the voltage gradients to a value which is non-critical for the machine insulation system and to reduce EMI. Although losses are induced by the usage of $\mathrm{d}v/\mathrm{d}t$ damping networks as well, the benefit of lower semiconductor temperatures at comparable efficiencies is remarkable concerning the durability and reliability of the devices [6].

In this paper two $\mathrm{d}v/\mathrm{d}t$ filter topologies are evaluated. For this, a fast switching, three-phase 600 V SiC-MOSFET inverter is used, which generates voltage slopes of up to $50\,\mathrm{V/ns}$. The filters are designed to damp the voltage transients at the filter output to a maximum of 10 -15 $\mathrm{V/ns}$. Therefore, different *LCR*-parameter-combinations are analysed. Besides their effectiveness in reducing high voltage transients, the influence of parameters like the size of the filter inductance on occuring filter losses and the efficiency of the system is examined. To prevent overvoltages a diode clamping of the filter output voltage to the DC-link potentials is implemented. Finally, the impact of various filter topology setups and extensions as well as the influence of the diode clamping on the conducted EMC behaviour is presented.

Measurement setups

In previous publications, passive filter topologies have already been discussed concerning their advantages in both differential mode $\mathrm{d}v/\mathrm{d}t$ reduction and common mode (CM) voltage suppression [7, 8, 9]. Lots of them have used conventional IGBT inverter technology with medium to low voltage transients compared to the dynamic switching abilities of modern wide bandgap devices such as SiC MOSFETs. In this paper, those filter topologies will be investigated in a wide bandgap setup using a fast switching three-phase SiC inverter.

Figure 1 shows the standard *LCR*-filter topology connected between a three-phase SiC MOSFET inverter and a machine load. The used additional diode clamping of the filter output voltage to the DC-link voltage (marked in grey) should prevent a high voltage overshoot. In figure 2 the above mentioned extensions of the standard topology are presented to challenge both common and differential mode EMI by using a simple $\mathrm{d}v/\mathrm{d}t$ filter network. The filter structure in figure 2a uses an accessible midpoint of the DC-

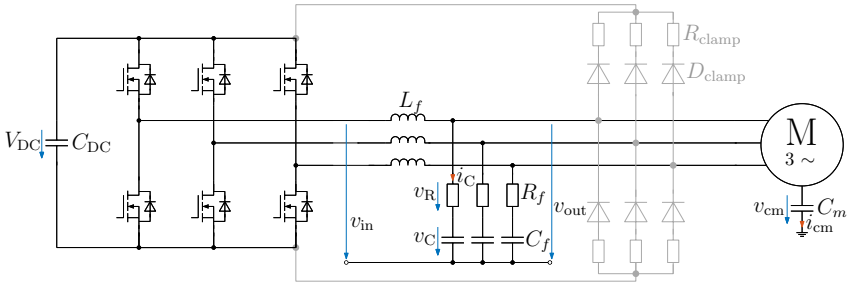
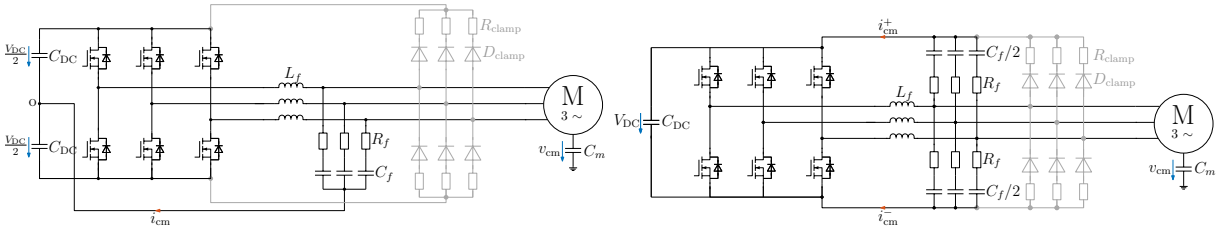


Fig. 1: Standard three-phase *LCR* $\mathrm{d}v/\mathrm{d}t$ filter topology

link (marked as O), which is connected to the neutral point of the three *RC*-legs of the filter to create a common mode path for high-frequency noise caused by the SiC inverter [8]. This is implemented to additionally reduce the amount of common mode noise leaving the drive system for example through a parasitic capacitance C_m from the machine load to ground. For the same purpose, the filter topology

shown in figure 2b uses a symmetrical connection of two three-phase *RC*-legs to both of the DC-link potentials to reduce the $\mathrm{d}v/\mathrm{d}t$ at each switching operation [9]. An advantage of this topology, despite the higher amount of filter components needed, is that the DC-link positive and negative potentials are generally more easily accessible than a DC-link midpoint of an inverter.



(a) Topology 1 with access to the DC-link midpoint

(b) Topology 2 with symmetrical connection to both DC-link potentials

Fig. 2: Filter topologies to challenge common and differential mode EMI

Dimensioning and filter design

The *LCR*-parameter-combinations were chosen in order to meet the $\mathrm{d}v/\mathrm{d}t$-damping requirements of reducing a voltage slope of $50\,\mathrm{V/ns}$ down to a maximum of $10\text{-}15\,\mathrm{V/ns}$ and to keep the filter losses manageable. According to [10], the losses dissipated by the damping resistors of one phase can be estimated by the equation

$$P_{\mathrm{loss}} = f_{\mathrm{load}} \cdot C_f \cdot \Delta V_C^2, \tag{1}$$

which means that they are proportional to the size of the filter capacitor. It should be considered that ΔV_C is the phase-to-neutral voltage of the inverter in this three-phase filter topology. Another analytical approach to calculate the losses of a three-phase filter is given in [4]. The correlation between L_f and C_f in order to achieve the required resonance frequency for the $\mathrm{d}v/\mathrm{d}t$ low-pass filter ($\omega_0 = 1/\sqrt{L_f C_f}$) describes that by reducing C_f to minimize the filter losses, L_f has to be increased. This would lead to higher space requirements of the filter as well as a higher voltage drop across the inductor, reducing the effective exploitation of the DC-link voltage transferred to the load [4]. Hence, a compromise between capacitance and inductance has to be found. For the filter dimensioning in this paper, at first the desired inductance value L_f was selected, mainly by availability and size. Afterwards, the values of C_f and R_f were determined by an optimising algorithm following the Nelder–Mead method in order to meet the slope-damping criterion. To configure the filter parameters analytically, an alternative approach is also given e. g. in [5]. The chosen dimensioning can be checked previous to measurement by solving the differential equations of a one-phase *LCR*-circuit, which are excited by an equivalent ramp function. The following equations

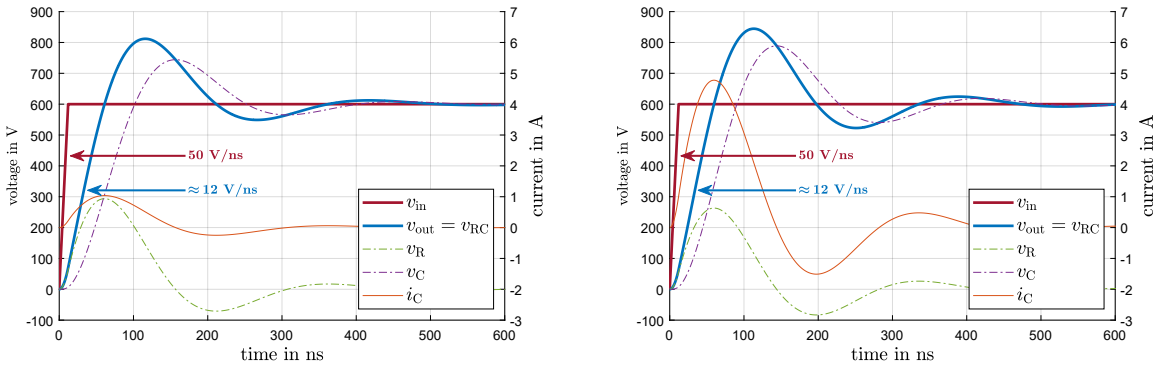
$$\frac{\Delta V_{\mathrm{in}}}{\Delta T} \cdot t = L_f \cdot \frac{\mathrm{d}i(t)}{\mathrm{d}t} + R_f \cdot i(t) + \frac{1}{C_f} \int i(t)\mathrm{d}t + K_1 \qquad \Delta V_{\mathrm{in}} = 600\,\mathrm{V} \qquad \Delta T = 12\,\mathrm{ns} \tag{2}$$

and

$$V_{\mathrm{in}} = L_f \cdot \frac{\mathrm{d}i(t)}{\mathrm{d}t} + R_f \cdot i(t) + \frac{1}{C_f} \int i(t)\mathrm{d}t + K_2 \qquad V_{\mathrm{in}} = 600\,\mathrm{V} \tag{3}$$

therefore consider a linear part and a constant part of an excitatory ramp function, respectively. The voltage and current curves resulting from this are exemplarily depicted in figure 3. The characteristics of the filter output voltage were calculated according to the case of a damped harmonic oscillator. Due to more parasitic passive elements in the real setup, increased ringing and a higher overshoot of the voltage can be expected. Furthermore, the real inverter output voltage will not occur as a perfect ramp with constantly high slope, but the presented method is still suitable for the parameter dimensioning. Another aspect to mention is that this approach doesn't include the diode clamping. The mathematical behaviour

of the diodes would introduce non-linearity to the differential equations presented in equation (2) and (3). Therefore, the behaviour of the filter constellations utilizing a diode clamping was checked with an appropriate simulation model in Simulink / PLECS Blockset. Both of the discussed filter topologies were analysed using four parameter combinations with different inductances, see table I. For the clamping, SiC Schottky diodes are used with a resistance of $R_{\text{clamp}} = 7.5\,\Omega$ in series (see figure 2).

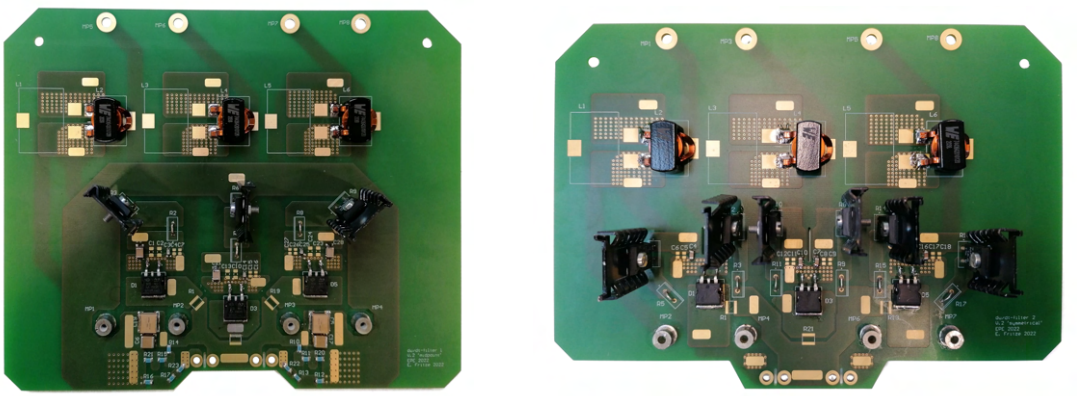


(a) $L_f = 10\,\mu\text{H}$, $C_f = 168\,\text{pF}$, $R_f = 175\,\Omega$ (constellation (IV))

(b) $L_f = 2.2\,\mu\text{H}$, $C_f = 1.36\,\text{nF}$, $R_f = 75\,\Omega$ (constellation (II))

Fig. 3: Voltage and current curves of the standard *LCR*-circuits based on analytical solutions of the differential equations excited by a $50\,{}^{\text{V}}/_{\text{ns}}$ ramp function (see figure 1)

The dv/dt-filter PCB layouts are given in figure 4. In order to investigate different *LCR*-combinations with the same circuit board, various components and packages were included on the PCBs, dependent on the desired constellation. They were designed as symmetrical as possible to achieve similar behaviours on all three phases.



(a) PCB-layout of filter topology 1

(b) PCB-layout of filter topology 2

Fig. 4: Designed dv/dt-filter PCBs for investigation of the different topologies and *LCR*-combinations

Table I: L, C, R parameters used for the measurements

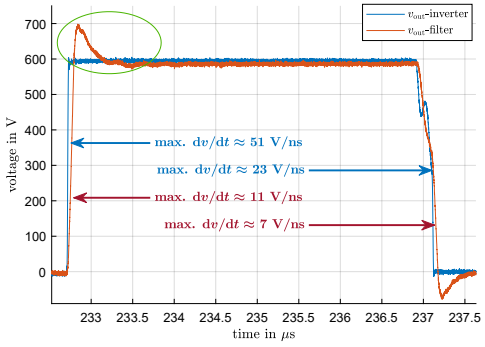
	Filter topology 1			Filter topology 2		
Constellation	L_f	C_f	R_f	L_f	$C_f/2$	R_f
(I)	1.2 µH	1.33 nF	15 Ω	1.2 µH	680 pF	15 Ω
(II)	2.2 µH	780 pF	33 Ω	2.2 µH	470 pF	33 Ω
(III)	4.2 µH	470 pF	75 Ω	4.2 µH	200 pF	75 Ω
(IV)	10 µH	168 pF	175 Ω	10 µH	100 pF	175 Ω

Measurement results

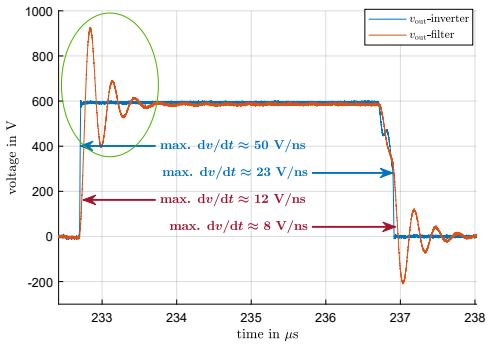
For the performance analysis of the filter setups as well as for the EMC measurements, a DC-link voltage of 600 V and a switching frequency of 30 kHz were defined. The fundamental output frequency of the inverter was set to 1.5 kHz. The electrical machine was replaced by an equivalent *RL*-load to achieve a RMS load current of about 11.7 A at steady-state. To prevent overheating, the inverter baseplate was cooled down to 20 °C using a water-cooled heat sink and external fans were used to cool the damping resistors and components of the filter. In addition to the modified output $\mathrm{d}v/\mathrm{d}t$-filters, an input common mode filter was used. It consisted of a 5 mH and a 0.9 mH common mode choke in series as well as a 47 nF parallel capacitance, resulting in a resonance frequency of the filter of about 9.56 kHz.

Performance analysis and losses

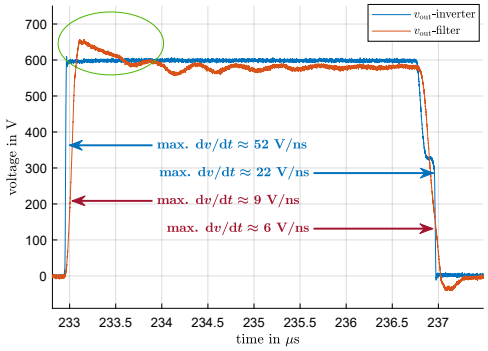
Measurement results that confirm the functionality of the $\mathrm{d}v/\mathrm{d}t$-filters in terms of slope reduction are given in figure 5, for constellation (I) of filter topology 1 and constellation (III) of filter topology 2, respectively. To analyse the maximum $\mathrm{d}v/\mathrm{d}t$ of all the constellations accordingly, the observed timespan ΔT was set fix to 30 timesteps of the discretely sampled signal, meaning 4.8 ns. The $\mathrm{d}v/\mathrm{d}t$ values were then calculated as $\Delta V/\Delta T$. In general, the voltage slopes and curves show a good fit compared to the parameter layout and preliminary expectations. The highest $\mathrm{d}v/\mathrm{d}t$ values reached by the inverter of about $52\,\mathrm{V/ns}$ are damped down to a maximum of about $12\,\mathrm{V/ns}$ at the output of the filter networks. The shown pulses are representative for the remaining constellations, which all showed a similar $\mathrm{d}v/\mathrm{d}t$ reduction in the desired area. However, it has to be mentioned that the diode clamping has a big influence concerning the occuring overvoltages and ringing of the filter output. The overshoot (marked in green) compared to the measurements without clamping is remarkably lower. Omitting the diode clamping results in overvoltages of up to 1 kV. This value is expected to be problematic for the insulation system of a prospective electrical machine connected to the filter network [11]. The high amount of voltage ringing can furthermore contribute to higher amounts of EMI caused by the inverter system.



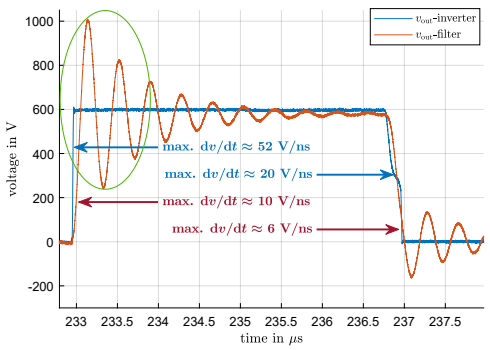
(a) Constellation (I) of filter topology 1 with clamping



(b) Constellation (I) of filter topology 1 without clamping



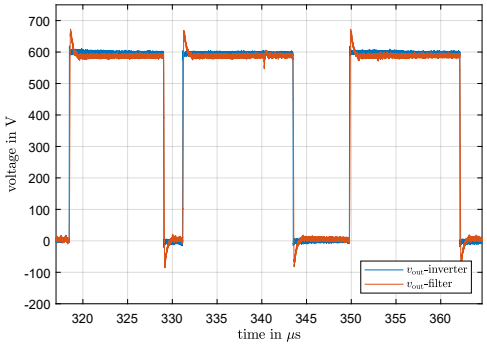
(c) Constellation (III) of filter topology 2 with clamping



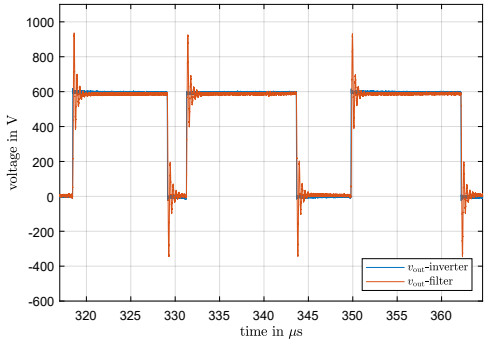
(d) Constellation (III) of filter topology 2 without clamping

Fig. 5: Measurement results of inverter and $\mathrm{d}v/\mathrm{d}t$-filter output voltages regarding representative phase-to-phase voltage pulses

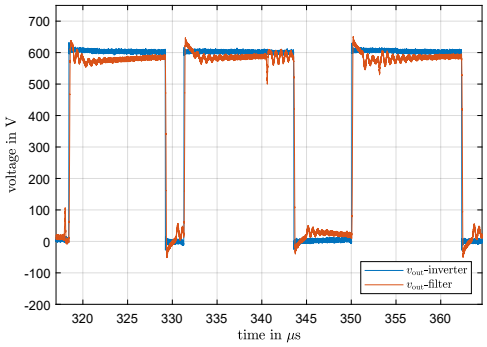
In figure 6, each oscillogram presents three representative output voltage pulses to further investigate the impact of the diode clamping as well as the filter parameters in terms of ringing. It is clearly observable that an increase of the filter inductance L_f, meaning also a decrease of capacitance C_f, leads to higher ringing of the filter output voltage in both setups with and without diode clamping. For the constellation shown in figure 6d, regarding the first falling slope, this means that the oscillation is not decayed until the next positive voltage pulse. This behaviour can be referred to a higher parasitic capacitance of the larger coil as well as the lower voltage-stabilizing capacitance and was also observed for filter topology 2. Moreover, a higher steady-state voltage difference from inverter output voltage to filter output voltage is noticeable with increasing filter inductance due to a higher voltage drop across L_f. Referring to



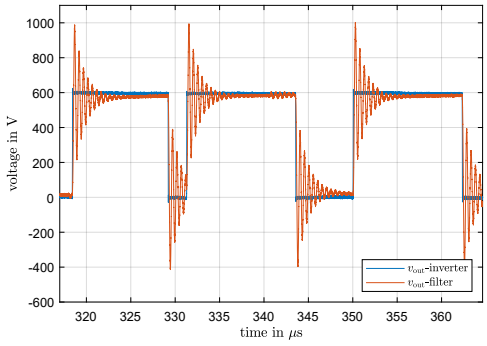
(a) Constellation (II) of filter topology 1 with clamping



(b) Constellation (II) of filter topology 1 without clamping



(c) Constellation (IV) of filter topology 1 with clamping



(d) Constellation (IV) of filter topology 1 without clamping

Fig. 6: Measurement results showing three pulses of inverter and filter output voltages

the filter constellations of table I and the previously mentioned performance settings of the inverter, also the power losses P_{loss} of the different filter circuits were analysed. They are specified in table II. For reference, the inverter PCB, including the input CM-filter, was also tested without any $\mathrm{d}v/\mathrm{d}t$-filter leading to power losses of 86 W at an efficiency of 98.75 %. Those losses are implied in table II and III. It can be seen clearly that the size of the inductance behaves inversely proportional to the capacitance value and therefore to the occuring losses that are dissipated mainly by the damping resistors. The increase of inductance from constellation (I) to (IV) of 8.8 µH comes along with a decrease of capacitance by almost 90 % and reduces the system losses significantly by 29 W for topology 1. Regarding topology 2, the filter capacitance decreases by 85 % and the losses by 23 W.

Table II: Filter power losses and total system efficiencies of the filter circuits with diode clamping

	Filter topology 1		Filter topology 2	
Constellation	P_{loss}	η	P_{loss}	η
(I)	136 W	97.96 %	131 W	98.12 %
(II)	128 W	98.07 %	121 W	98.25 %
(III)	117 W	98.22 %	111 W	98.40 %
(IV)	107 W	98.35 %	108 W	98.43 %

Concerning the impact of the diode clamping on arising losses, table III shows the measurement results of all previously mentioned constellations without clamping of the output voltage. Here, a noticeable reduction of power losses is observable regarding every setup. This can be referred to the omitted losses dissipated by the clamping diodes and resistors. However, considering the measurements in figure 6, this reduction of losses comes along with rising oscillations of the filter output voltage.

Table III: Filter power losses and total system efficiencies of the filter circuits without diode clamping

	Filter topology 1		Filter topology 2	
Constellation	P_{loss}	η	P_{loss}	η
(I)	129 W	98.07 %	129 W	98.15 %
(II)	117 W	98.23 %	108 W	98.44 %
(III)	105 W	98.40 %	87 W	98.74 %
(IV)	93 W	98.57 %	90 W	98.69 %

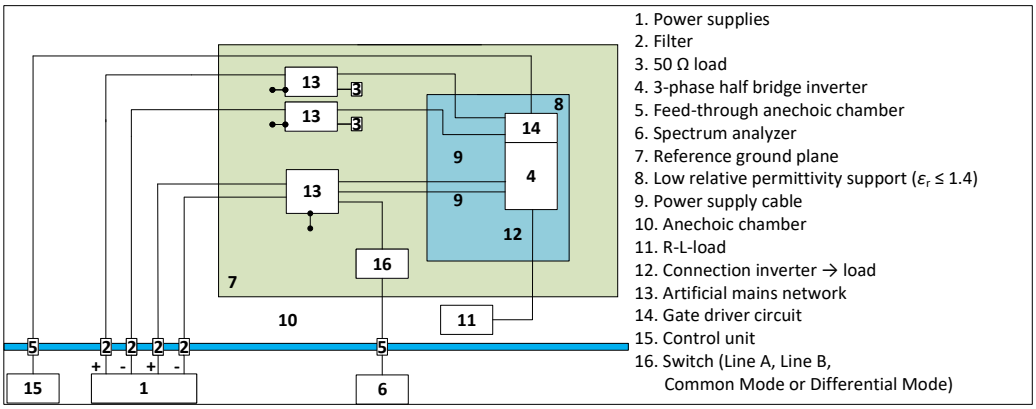
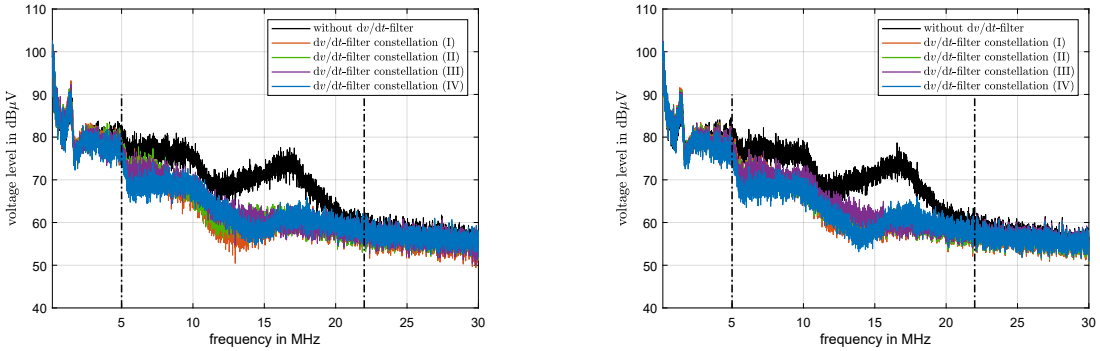


Fig. 7: Measurement setup for the common mode EMI measurements

EMC measurement

The measurement setup for the common mode EMI measurements is depicted in figure 7. As frame condition and in order to investigate the EMC effects under a standard-conditioned environment, the standard *CISPR25* was the used basis [12]. In the measurements the inverter, the driver circuit board as well as the input and output filter constellations were included. The results are presented in figure 8 and 9. To compare the impact of the modified $\mathrm{d}v/\mathrm{d}t$-filters on the common mode interference levels, the measurement of the inverter and input filter without any output filter is depicted in black in each figure.

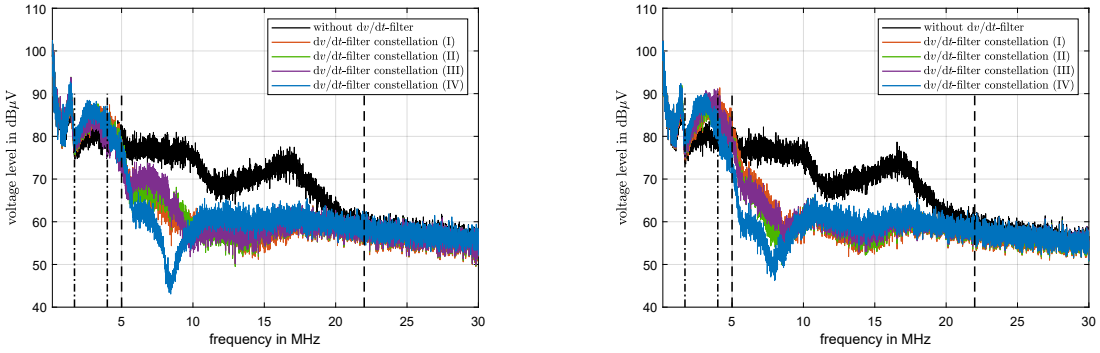


(a) filter topology 1

(b) filter topology 2

Fig. 8: Common mode EMI measurement results of the modified $\mathrm{d}v/\mathrm{d}t$-filter circuits with diode clamping of the output voltage

At lower frequencies of up to 2 MHz the voltage curves don't show noticeable differences, which is the reason why a linear display of the frequency domain was chosen instead of a logarithmic display. Despite that, in general the measurement without output filter shows remarkably higher voltage levels than the measurements with the modified dv/dt-filter networks, meaning that the modifications for a better common mode behaviour indeed show a positive impact. This applies for both presented filter topologies, especially in the wide interval of 5 MHz to 22 MHz. All four *LCR*-constellations are characterised by an overall similar behaviour for filter topology 1. Constellation (IV) shows a more advantageous behaviour regarding filter topology 2, in the area around 14 MHz, compared to other constellations.



(a) filter topology 1 (b) filter topology 2

Fig. 9: Common mode EMI measurement results of the modified dv/dt-filter circuits without diode clamping of the output voltage

Regarding figure 9, remarkable differences between the measurements with and without diode clamping are observable. In the interval of 1.7 to 4 MHz, the interference levels of the setups without diode clamping are even higher than in the measurement without any dv/dt-filter. This is a clear disadvantage of those constellations and can be referred to the high-frequency ringing of the filter output voltage, as seen e. g. in figure 5d. Another perceivable difference can be seen in both figures 9a and 9b concerning filter constellation (IV). With a negative peak in the interval around 8 MHz the common mode voltage level drops below 50 dBµV, which is a significant difference compared to any other measurement setup. This effect is a little more considerable for filter topology 1. However, the filter constellations with the additional diode clamping lead to more favourable conditions and a better overall dv/dt-filter performance.

Conclusion

In this paper two different three-phase dv/dt-filter topologies, which have been previously presented in other publications, are investigated and discussed in a fast switching, wide bandgap inverter environment. Besides a dv/dt damping of the steep inverter output voltage pulses, they should also challenge the common mode interference behaviour of the system. The slope reduction of the inverter output voltage in the desired area was verified successfully with both topologies and all four *LCR*-combinations. Furthermore, the influence of the inductor size on occuring losses was clearly observable. Increasing the inductance leads to a reduction of the required filter capacitance and therefore to lower system power losses. Although, this also introduces higher oscillations of the filter output voltage and a higher filter volume due to larger coils. Regarding the utilization of an additional diode clamping of the filter output voltage to the DC-link potentials, positive effects on the investigated objectives of this paper were detectable. While preserving the requested damping of the inverter's voltage slopes, the overshoot of the filter output voltage is reduced drastically. Moreover, it leads to a less oscillating voltage. Nevertheless, it induces some additional losses due to the power dissipation of the diodes and clamping resistors. An analysis of the conducted EMI levels shows an advantageous behaviour of the dv/dt filter topologies concerning the common mode interference, as it was desired by their modifications. In a wide frequency range, the common mode voltage levels are considerably lower than in the measurement without the output dv/dt-filters. Omitting the diode clamping increases the amount of CM noise in certain areas, which can be referred to the higher amount of oscillation of the filter output voltage in this frequency domain.

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