Systematic analysis of oscillations in DC-links of fast switching power electronics

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Keywords

≪Capacitors≫, ≪DC-link≫, ≪Design optimization≫, ≪Hardware≫, ≪Harmonics≫, ≪High frequency power converter≫, ≪Impedance analysis≫, ≪Impedance measurement≫, ≪MOSFET≫, ≪Parasitic elements≫, ≪Passive component≫, ≪Test bench≫

Abstract

Increasingly faster switching and higher switching frequencies amplify the impact of parasitics of the DC-link causing higher voltage overshoots, oscillations, losses and also EMI. Higher-frequency resonances due to polarization effects of dielectrica and oscillations between either different capacitors or capacitors and switches (or even other components) due to a mismatch of pcb parasitics and component impedances are just some of the possible causes. This paper marks the beginning of a series of studies with the aim of a set of design rules for DC-links of high switching frequency power electronics. Therefore circuit simulations, impedance measurements (of capacitors and pcb's) and experiments using an evaluation platform are carried out. Some of the results are presented in this paper.

I Introduction

The increase of switching speeds and frequencies caused by the evolution of wide-bandgap-semiconductors like Siliconcarbide (SiC) and Galliumnitride (GaN) also leads to an increase of the influence of parasitics. First of all the assembly technologies and pcb layouts represented a first hurdle. Decreasing the stray inductances of both in the power loop was a necessary step towards the utilization of the new semiconductors properties, since it limits the $\frac{di}{dt}$ and causes voltage overshoots and oscillations [1]. But due to the higher switching frequencies of SiC and GaN the requirements for magnetic elements like chokes and transformers also increased, which brought them more into focus again [2]. New core materials, winding configurations, braids and even design methods were and are still investigated [3]. In addition the influence of capacitors and DC-links on voltage overshoots and oscillations emerges more and more often [4]. One reason for this is as well the stray inductance, but in this case the ones of capacitors and the DC-link-assembly including the pcb. For this reason the parasitic elements of the DC-link are currently in the focus. Optimizing single capacitor types seems to bee a promising option [5][6]. But also the investigation of pcb layouts and interconnections are being discussed more and more often [7][8]. Finally, the stray inductance is not the only important parameter that can cause the problems mentioned above. Oscillations between capacitors and switches or even between different capacitors are possible.

Many of this investigations regard a specific application and not the DC-link in general (related to high switching frequency applications). The presented paper therefore forms the beginning of a series of studies which will help to understand the influence of capacitors, their combinations, circuit topologies and their interaction on voltage overshoots, oscillations, losses and EMI. Based on this findings design rules are to be created, which will support during the design process of DC-links for fast switching power electronics. Therefore this paper will present three parts of this studies. Impedance measurements of different electrolytic and ceramic capacitors regarding the DC-bias, the realization of a GaN-based test platform for evaluation purposes and simulations of fundamental correlations, which will be described first.

II Simulations

The dc-link's behaviour (more precisely: its impedance) mainly depends on the characteristics of three parts of the system. The capacitors, the switches and the PCB layout. The combination of these parts defines the DC-link's behaviour, with the parasitics playing an important role since they are responsible for the most unintended oscillations. They can cause oscillations between capacitors and switches or even between different capacitors. This interactions can become complex which is why they will be subject of more detailed studies in the future. Nevertheless there are a few general questions that often come up when discussing about capacitors and DC-links:

1. Which effect has the DC-links main resonance frequency f_{link} (e.g. the resonance of C_{link} and L_{link} defined in Fig. 1)?
2. Where should the switching frequency be in relation to this resonance frequency?
3. Is it better to have some ESR (R_{link} in Fig. 1) e.g. for dampening in terms of EMI?

This questions are suitable for gaining some fundamental knowledge and testing the simulation models described next. The simulation model implemented a single-phase synchronous buck-converter using LTspice. All parameters were adopted from the DC-link evaluation platform described in Section IV. To start with, the DC-link was modeled by using a simple capacitor-model which consists of R_{link}, L_{link} and C_{link} (see Fig. 1).

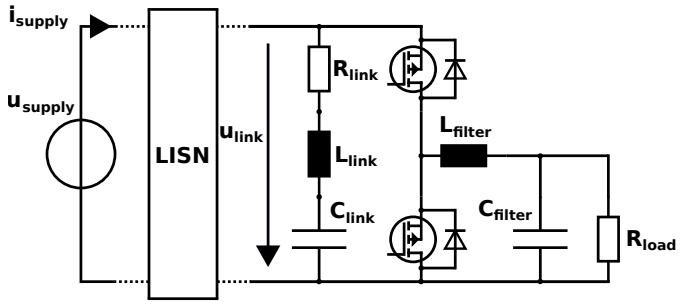


Fig. 1: Schematic representation of the implemented simulation model

The simulations neglected the influences of the pcb layout and the switches (ideal switches were used) to keep the number of parameters low. The key parameters are:

- Switching frequency $f_{\text{sw}} = 1\,\text{MHz}$
- DC-link supply voltage $u_{\text{supply}} = 150\,\text{V}$
- Duty cycle 50 %
- Load resistance $R_{\text{link}} = 5\,\Omega$
- DC-link capacity $C_{\text{link}} = 10\,\mu\text{F}$

To replicate real conditions the line was implemented as HV-LISN (Line Impedance Stabilization Network, also known as Artificial Mains Network or AMN) with values according to CISPR 25 [9]. This ensures comparable conditions. To receive significant data a specifically implemented Python-based simulation-controller automatically varied the main resonance frequency f_{link} of the DC-link (by modifying L_{link}) and the ESR (here: R_{link}). This leads to a result matrix that allows for a separate analysis

of the impacts of f_{link} and R_{link} on characteristic values like the DC-link voltage and the supply current, which will be described next.

A DC link voltage

Since the DC-link itself was the subject of the investigations the influences of the switches and their parasitics were consciously neglected. This was realized by the usage of ideal switches (except for resistances).

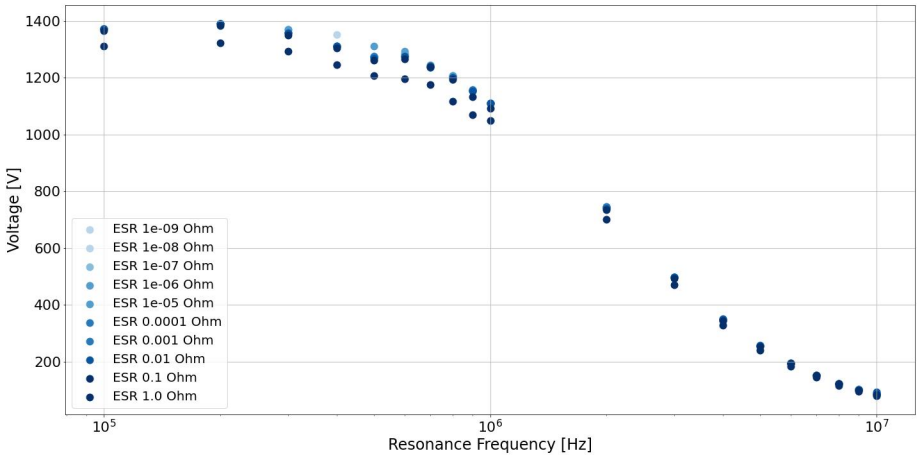


Fig. 2: Max. positive voltage overshoot related to the mean value of u_{link} during variation of f_{link} and R_{link}

Fig. 2 shows the maximum positive voltage overshoot of the DC-link voltage u_{link}. Several dots at the same frequency mark the values of different R_{link} settings while the dot's course along the x-axis shows the behaviour of the voltage overshoots during variation of f_{link}. The voltage overshoot starts to drop the closer f_{link} gets to the switching frequency of 1 MHz. The inflection point of the curve lies slightly higher than f_{sw}. Finally at $f_{\text{link}} \approx 10 \cdot f_{\text{sw}}$ the gradient of the curve becomes small and the region of the lowest voltage overshoot is reached.

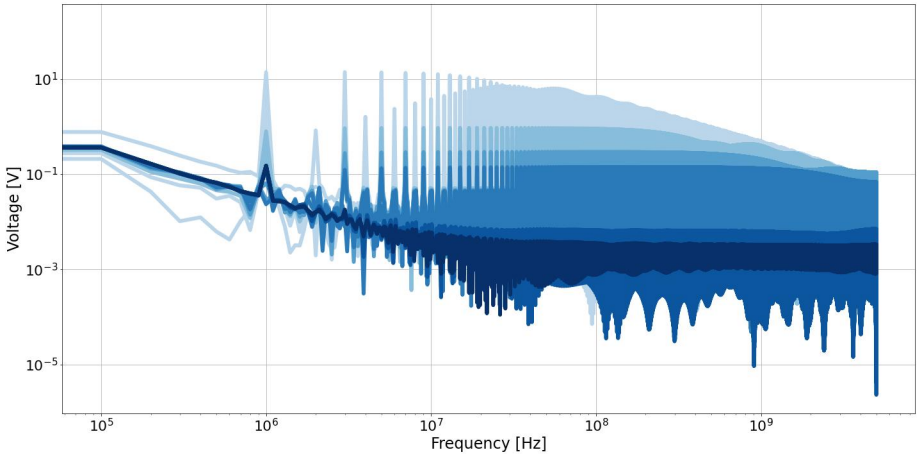


Fig. 3: Spectra of u_{link} during variation of f_{link} (darkest color marks highest f_{link}) and a fixed R_{link} at 1 nΩ

In Fig. 3 the resistance R_{link} stays fixed at 1 nΩ. By doing so, the impact of f_{link} on the harmonics of u_{link} can be evaluated. This comparison shows significantly lower amplitudes the higher the resonance frequency of the DC-link gets (Note that the resonance frequency f_{link} is marked by the colors with the darkest blue marking the highest frequency while the x-axis shows the frequency of the spectra). This behaviour correlates with the course of the voltage overshoot analyzed before. In sum this results showed that a main resonance frequency of the DC-link above the switching frequency decreases the harmonics

and the voltage overshoot significantly. A good indicative value seems to be $f_{\text{link}} \geq 10 \cdot f_{\text{sw}}$. Since the switching frequencies of SiC and GaN can be up to several MHz this might be a tough requirement.

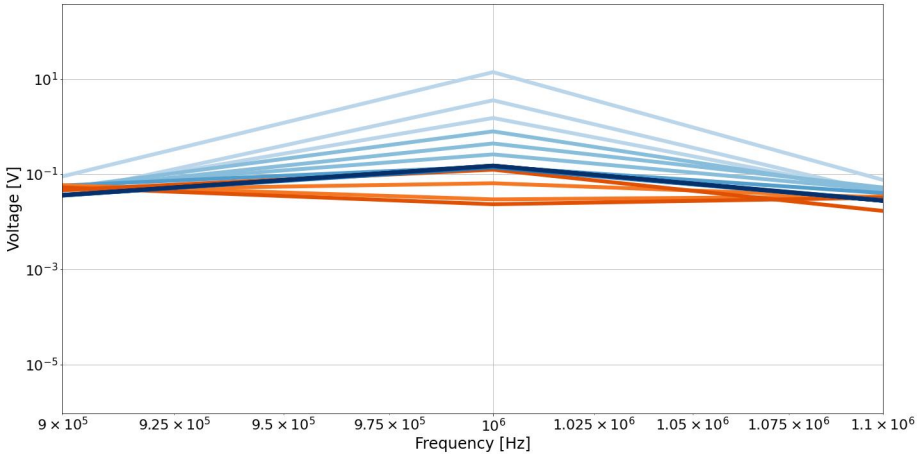


Fig. 4: Spectra of u_{link} during variation of f_{link} (darkest blue marks highest f_{link}) and a fixed R_{link} at 1 nΩ, orange marks resonance frequencies close to f_{sw}

Another striking aspect of the spectra is the behaviour around the switching frequency (see Fig. 4). If the main resonance of the DC-link lies close to the switching frequency the two impedances $\underline{X}_{\text{C,link}}$ and $\underline{X}_{\text{L,link}}$ become almost equal and cancel each other out. In consequence only R_{link} is effective. If this resistance is low enough, the resulting harmonic of u_{link} will be lower than one of a DC-link with an even higher main resonance frequency. To highlight this, frequencies close to f_{sw} are marked in orange (see Fig. 4). The significance of this effect (e.g. regarding the capacitors losses) will be subject of further studies.

B Supply Current

The current i_{supply} sourced by the supplying voltage source shows a different characteristic than the DC-link voltage analyzed above. Fig. 5 shows the RMS-value of the AC-part of the current i_{supply} for different combinations of f_{link} and R_{link} (the plot configuration is identical to the one of Fig. 2).

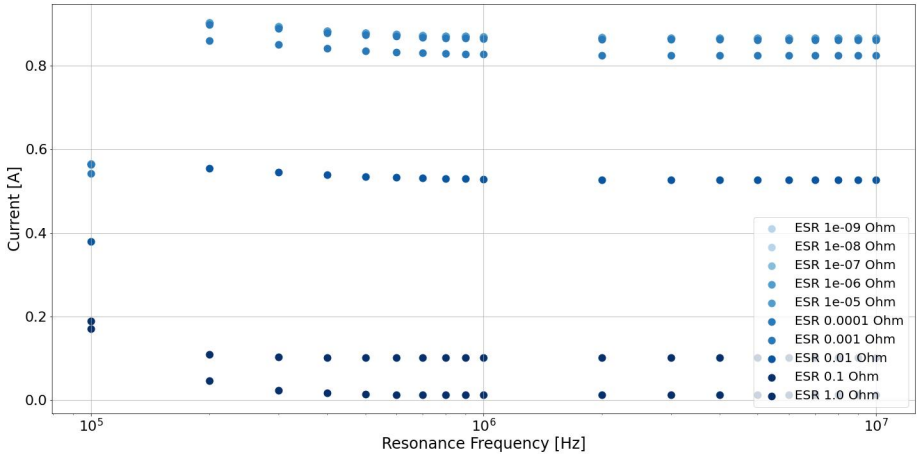


Fig. 5: RMS-value of the AC-part of the supply current i_{supply} during variation of f_{link} and R_{link}

In contrast to the DC-link voltage the main resonance frequency f_{link} has only an effect at very low frequencies, approximately below $0.1 \cdot f_{\text{sw}}$. Above this frequency the impact of f_{link} can be neglected. The situation is different for the impact of the resistance R_{link} as it shows a greater impact on the supply current than it did on the DC-link voltage. A higher resistance leads to a lower AC-RMS-value of i_{supply}.

C Summary

In sum the simulations lead to the following observations:

- f_{link} has great impact on the overshoot and the harmonics of u_{link}. Higher frequencies lead to lower overshoot and amplitudes of the harmonics
- R_{link} has small impact on the overshoot and the harmonics of u_{link}. The higher f_{link} the lower the impact of the resistance
- f_{link} has small impact on the AC-RMS of the supply current i_{supply}. The impact above $0.1 \cdot f_{\text{sw}}$ is neglectable
- R_{link} has significant impact on the AC-RMS of the supply current i_{supply}. The higher the resistance the lower the AC-RMS

Whether this observations are generally valid or not, what might be possible restrictions to them and how they have to be customized for specific applications will be subject of further studies. Nevertheless this results showed that the characteristics of the DC-links capacitor can have major impact on voltage overshoot and harmonics. This motivates the investigation of different capacitors described next.

III Capacitors

The simulations described in II used a fairly simple capacitor model consisting of only one resonance circuit. Nevertheless they showed a major impact of the capacitors impedance (resonance frequency and ESR) on important characteristics like voltage overshoots and EMI. To evaluate the influence of real capacitors more complex models are needed, some are already available [11]. The complexity of these models is needed because of the highly non-ideal characteristics of most capacitor types. The following are only the most significant reasons for those non-idealities [10]:

- different behaviour of the dielectric materials (like frequency- and temperature-dependencies of the permittivity ε_r)
- different polarization mechanisms (e.g. electron polarization, ionic polarization and oriental polarization)
- differences between polar and non-polar materials
- hysteresis effects like they appear in ferroelectric materials (for example Barium Titanate $BaTiO_3$)
- piezoelectric effects (ceramic capacitors)

To evaluate these models and to be able to simulate the behavior of real capacitors impedance measurements are needed. In terms of comparability among each other and the usage in the evaluation platform described in IV the voltage rating of most capacitors was set to 250 V.

A Electrolytic capacitors

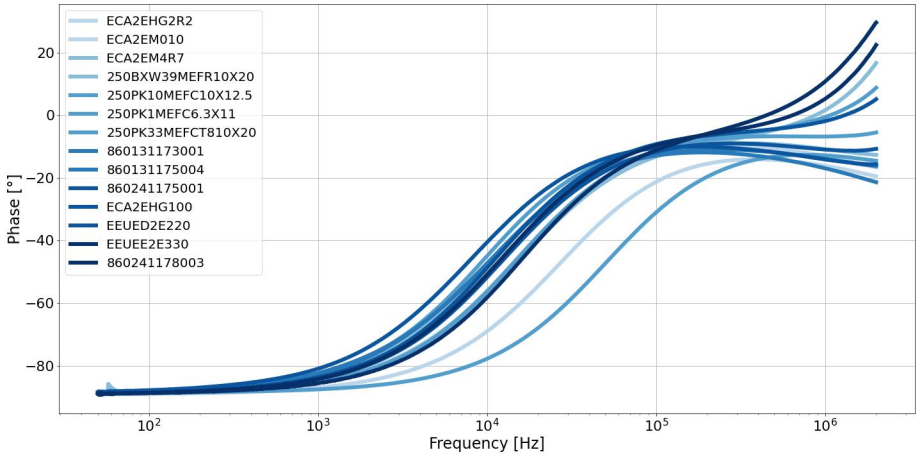


Fig. 6: Impedances of different electrolytic capacitors, all 250 V rated, applied DC-bias 150 V, measured with Keysight E4990A and 16065A DC bias fixture

Due to their high capacitance density electrolytic capacitors (especially Aluminium-electrolytic capacitors, Al_2O_3) are often the first choice for many applications in power electronics. However, since these capacitors typically show a comparatively high ESR and low resonance frequencies their usage is at least questionable in applications with high switching frequencies and fast switching times. Measurements were taken from several different capacitors (all 250 V rated) within the range of 0.68 μF to 33 μF. The results of the impedance measurements are shown in Fig. 6. Characteristic is the early (at comparatively low frequencies) beginning of the capacitors main resonances at frequencies between 1 kHz and 10 kHz. Compared to the known resonance of a simple capacitor model like the one used in II the impedances courses are very wide (referred to the frequency axis) and show an extensive flat region around 0°. Some of them even turn around to a negativ gradient before they get up towards 90°. In addition the impedances show no relevant voltage dependency, which was the expected behaviour. It can be noted that the wide course and the flat region of the impedance seems to be characteristic for electrolytic capacitors.

B Multi-Layer ceramic capacitors

Multi-layer ceramic capacitors (MLCC's) are often used in modern power electronics with higher switching frequencies since they show comparatively low ESR and ESL. The partially very high capacitance densities are another reason for their usage especially in volume critical applications.

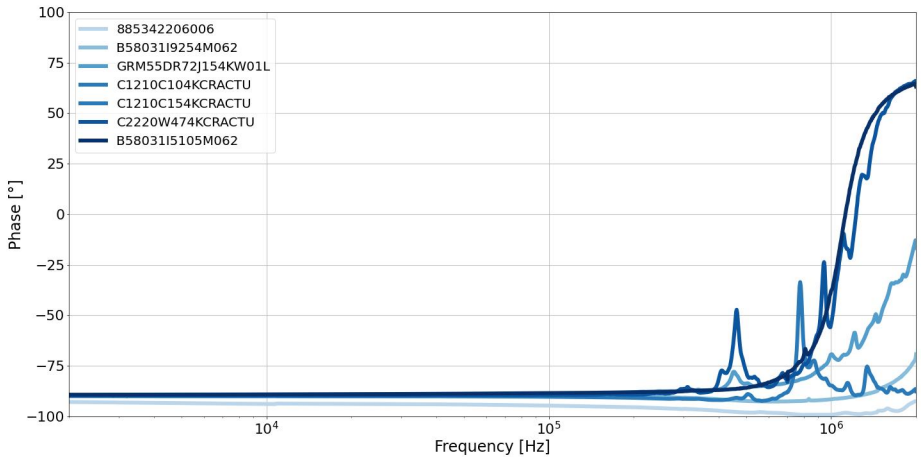


Fig. 7: Impedances of different ceramic capacitors, applied DC-bias 150 V, measured with Keysight E4990A and 16065A DC bias fixture

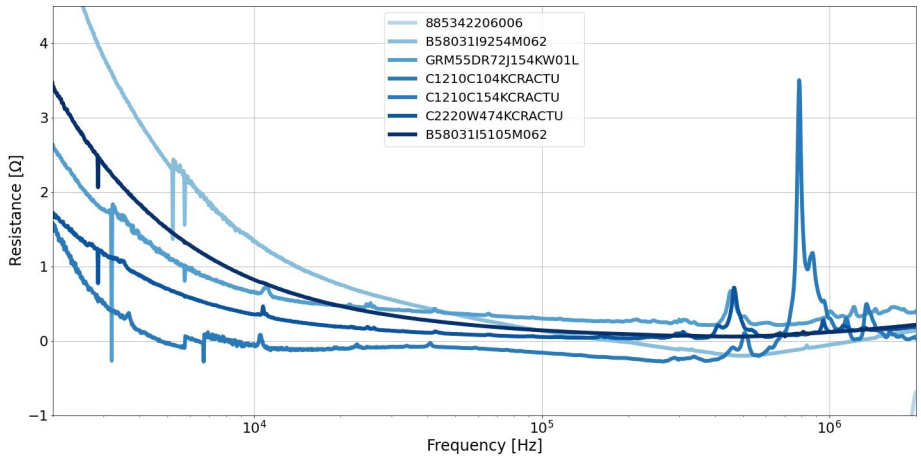


Fig. 8: ESR of different ceramic capacitors, applied DC-bias 150 V, measured with Keysight E4990A and 16065A DC bias fixture

Fig. 7 shows the impedances of different ceramic capacitors. Not all of them are, like the electrolytics, 250 V rated (e.g. the B58031I9254M062 and B58031I5105M062 which are due to their PZLT-ceramic

not available with 250 V rating). The highest capacity of all MLC-capacitors was 2.2 μF, which is lower than those of the electrolytic ones. Nevertheless there are some 1.0 μF capacitors in both measurements (compare ECA2EM010 in Fig. 6 and B58031I5105M062 in Fig. 7) which shows, that the MLC's main resonance frequency lies much higher than those of the electrolytic ones. Thinking of the simple capacitor model used in II the ESL of the ceramic capacitors has to be much smaller (as long as the capacities are equal).

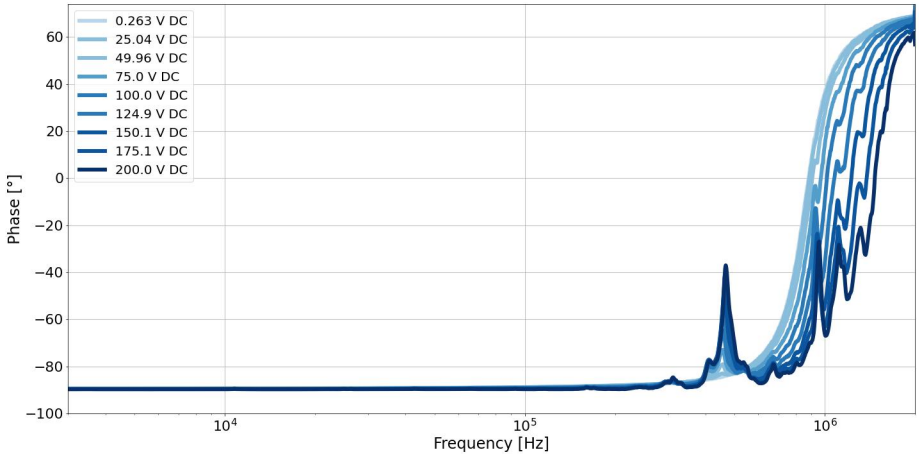


Fig. 9: Impedance of KEMET C2220W474KCRACTU 500 V 0.47 μF X7R, measured with different DC-bias voltages using the Keysight E4990A and 16065A DC bias fixture

Unfortunately these type of capacitors also suffers from disadvantages like a high dependency of the capacity from the electric field strength and therefore the voltage. Fig. 9 shows this behaviour using the KEMET C2220W474KCRACTU X7R-capacitor as an example. The higher the DC-bias voltage the higher the main resonance frequency. In addition the course of the impedance gets rougher the higher the DC-bias gets, which is a sign of additional resonances that get stronger with the increase of the DC-bias. What strikes in this plot is a phase peak before the main frequency that also increases with the DC-bias.

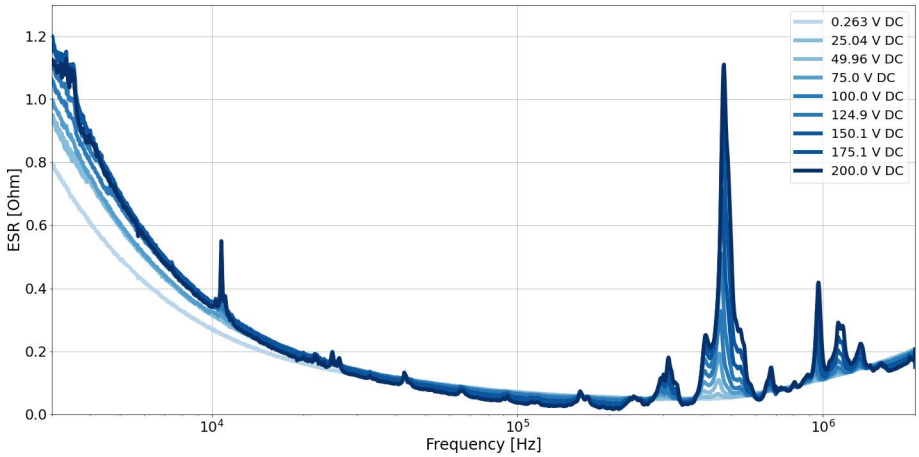
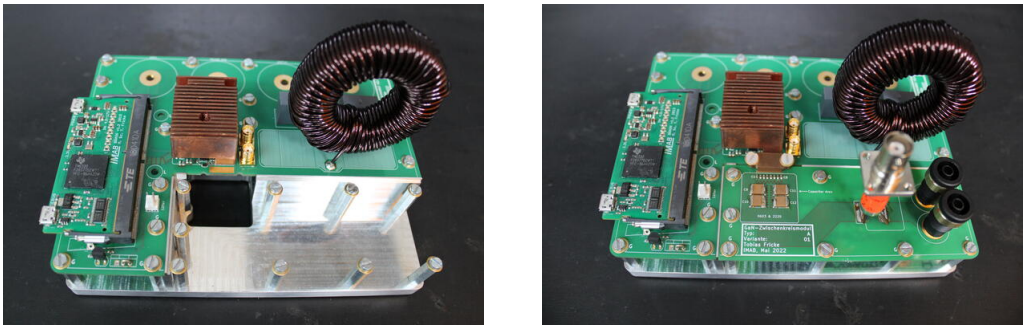


Fig. 10: ESR of KEMET C2220W474KCRACTU 500 V 0.47 μF X7R, measured with different DC-bias voltages using the Keysight E4990A and 16065A DC bias fixture

This peak causes a temporary increase of the ESR, which can be seen in Fig. 10. This peak can cause a significant increase in losses when current harmonics match it's area. Even oscillations between capacitors due to a mismatch of their impedances in combination with those of the pcb are possible. Since all other ceramic capacitors showed this spikes it seems to be characteristic (see Fig. 8). Whether these behaviour of the capacitors is significant or not will be subject of future studies. One opportunity to evaluate all described effects is the DC-link evaluation platform described in the next section.

IV DC-link evaluation platform

The evaluation platform is based on a synchronous buck converter using EPC2034C® eGaN-FET's. The system covers a frequency range from 50 kHz to 1 MHz at a maximum $i_{\text{load}} = 15\,\text{A}$ and a maximum DC-link voltage of 200 V (see Fig. 11). The special feature is the easy interchangeability of the DC-link.



(a) (b)

Fig. 11: (a) GaN-converter-module mounted on the milled baseplate without a DC-link-pcb connected, (b) module with a connected DC-link-pcb and a special copper clamp between the two pcb's

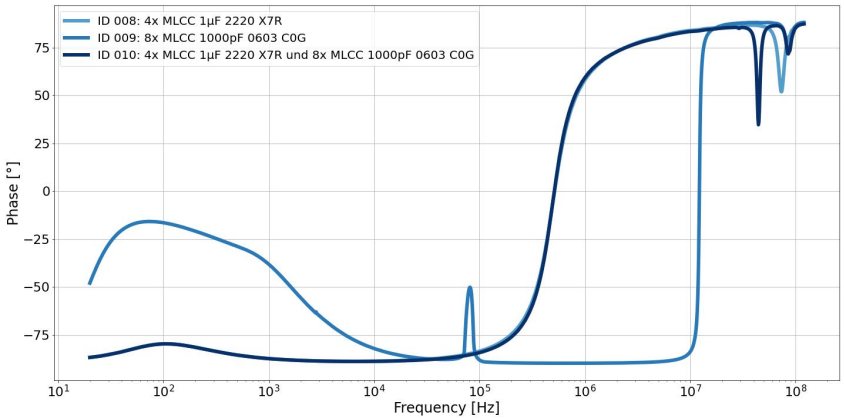


Fig. 12: DC-link impedance of evaluation platform using different ceramic capacitor combinations

Impedances of different capacitor combinations are shown in Fig. 12. The results are a combination of the capacitors impedances and those of the setup. While the bigger capacitors ($4\,\text{x}\,1\,\mu\text{F}$) define the main resonance frequency the smaller ones add higher resonances, further correlations are being investigated.

V Conclusion

Section I described the increasing influence of parasitics in DC-links when using high switching frequencies and fast switching times. The emergence of oscillations and overshoots of the DC-link voltage was mentioned as well as the impact on harmonics of the supply currents and therefore the increase of EMI. To investigate this systematically, a series of sudies was announced whose inception is marked by the sections II, III and IV. This began with the description of simulations which investigated fundamental correlations in DC-links. They lead to observations regarding the impact of the DC-links main frequency and the ESR on voltage overshoots, harmonics and RMS-values (see section II C for details). This section clarified the impact of the capacitors impedance, which is why they were thematized in section III. It pointed out the reasons for the capacitors non-ideal behaviour before impedance measurements were analyzed. This showed some specific characteristics of different capacitor types as well as the impact of the DC-bias voltage. In addition, the emergence of ESR-spikes of ceramic capacitors was discussed. Finally section IV described a DC-link evaluation platform and some first results regarding the combination of different sized MLC-capacitors, switching tests to study oscillations will be carried out.

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