Class-E Push-Pull Resonance Converter with Load Variation Robustness for Industrial Induction Heating

Janus Dybdahl Meinert, Benjamin Futtrup Kjærsgaard, Thore Stig Aunsborg
Asger Bjørn Jørgensen, Stig Munk-Nielsen
Department of Energy, Aalborg University
Pontoppidanstræde 111
9220 Aalborg Øst, Denmark
Email: {jdm, bfk, tsu, abj, smn}@energy.aau.dk
URL: https://www.energy.aau.dk

Sune Bro Duun
Topsil GlobalWafers A/S
Siliciumvej 1
3600 Frederikssund, Denmark
Email: sdu@gw-topsil.com
URL: http://www.topsil.com

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Keywords

≪Resonant converter≫, ≪Zero-voltage switching≫, ≪Wide bandgap devices≫,
≪Radio frequency (RF)≫ , ≪Current Source Inverter (CSI)≫, ≪Simulation≫

Abstract

Emerging wide bandgap devices are extending the operating frequency range and power handling capability of solid state based resonant power converter solutions. Presently, resonant power converters for industrial induction heating are using vacuum-tubes, achieving efficiencies of 50-60 %. By replacing the prevalent vacuum tube technology with a solid state based solution, the efficiency of the industrial induction heating processes is expected to be increased. A design of a Class-E Push-Pull resonance converter using silicon carbide MOSFETs is proposed. A prototype, operating at 2.5 MHz, has been built showing a proof-of-concept of the topology at 4 kVA, achieving an efficiency of 91.8 % with a representative industrial induction heating load.

Introduction

Resonant converters operating in a high frequency high power range are used in a wide range of industrial applications including dielectric and inductive heating. Dielectric heating includes various drying processes, whereas inductive heating is used for e.g. sawblade hardening and float zone processes [1–4]. The float zone processing industry currently uses vacuum-tube technology for the resonance converters with efficiencies ranging from 50-65 % [5, 6]. However, with the higher breakdown voltage, lower

on-resistance, higher thermal conductivity and lower gate charge of the silicon carbide (SiC) MOSFETs compared to their silicon counterparts [7,8], high power radio frequency (RF) applications based on solid state technology is enabled [9–13]. Thus, by using wide bandgap (WBG) devices as a replacement for the vacuum-tubes, the efficiency of the float zone process is expected to be increased significantly.

In this paper, a proposed prototype resonance converter using SiC MOSFETs will be built and demonstrated for 2.5 MHz induction heating applications. The next section will present the intended converter design, its functionalities and design considerations. An experimental demonstration is given and a comparison between experiments and digital twin simulations is presented in the following two sections. Lastly the most relevant findings of this paper are summarized.

Proposed Topology

The chosen converter topology for the proposed design is a Class-E Push-Pull resonance current source converter, illustrated in Fig. 1a. Recent research utilizing the Class-E Push-Pull converter for inductive power transfer applications has shown high frequency oscillations and voltage spikes during switching instances, which is found to be caused by the stray inductance as presented in [13, 14].
The proposed design intends to utilize the stray inductance by having two distinct resonance loops; (*1*) The drain-source resonance loop, consisting of the stray inductance L_{stray} and the respective drain-source capacitance C_{ds} visualized by the red and green colored areas in Fig. 1a. (*2*) The load resonance tank, illustrated by the blue colored area, consisting of the resonance capacitor C_r and the single turn resonance induction coil L_r which through inductive power transfer will dissipate power in the form of iron losses heating the load object represented by R_{iron}. A sketch of the used single turn coil is shown in Fig. 1b.

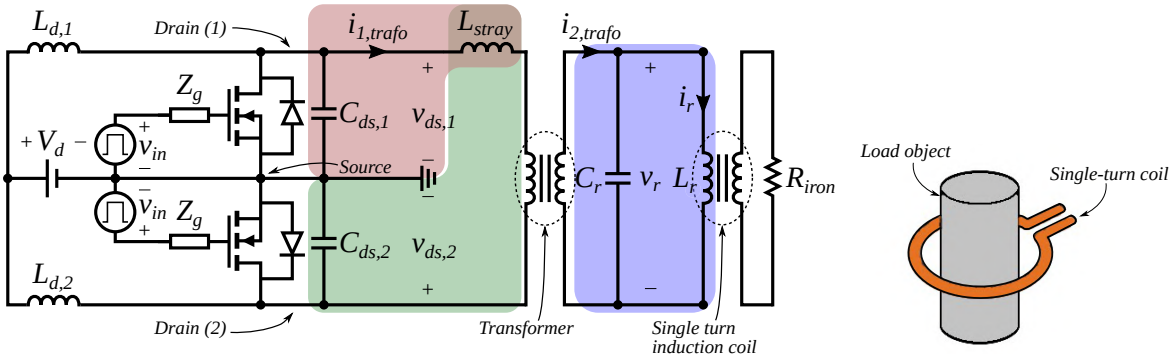


Fig. 1: (a) Circuit schematic of proposed topology with colored areas illustrating different resonance loops. (b) Sketch of a single turn induction coil.

The concept of the design is to ensure zero-voltage switching (ZVS) over a wide range of load resonance frequencies f_r by controlling the drain-source resonance frequency f_{ds}. This is obtained with the following two design considerations; (*1*) Utilizing the leakage inductance of the transformer $L_{lk,trafo}$ the trace/wire inductance from the converter to the resonance load $L_{trace,\sigma}$ is dominated. (*2*) Inserting sufficiently large drain-source capacitors $C_{ds,ext}$ in parallel with the MOSFETs, reduces the influence of the voltage dependent intrinsic output capacitance $C_{ds,\sigma}$ of the MOSFETs.
The two design considerations are summarized in (1) and (2).

$$L_{stray} = L_{lk,trafo} + L_{trace,\sigma} \simeq L_{lk,trafo}, \qquad L_{lk,trafo} \gg L_{trace,\sigma} \tag{1}$$

$$C_{ds} = C_{ds,ext} + C_{ds,\sigma} \simeq C_{ds,ext}, \qquad C_{ds,ext} \gg C_{ds,\sigma} \tag{2}$$

By the designers choice the drain-source resonance frequency f_{ds} can be varied by controlling the size

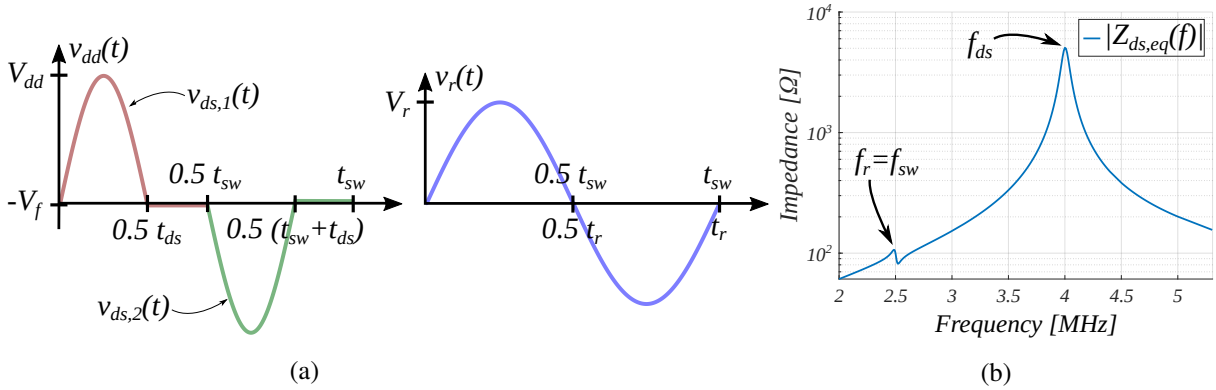
of the transformer leakage inductance and the inserted drain-source capacitance.

$$f_{ds} = \frac{1}{2\pi \cdot \sqrt{L_{stray} \cdot C_{ds}}} \simeq \frac{1}{2\pi \cdot \sqrt{L_{lk,trafo} \cdot C_{ds,ext}}} \tag{3}$$

By choosing the drain-source resonance frequency f_{ds} higher than the switching frequency f_{sw}, ZVS of the MOSFETs are ensured for a wide range of load variations if the constraint in (4) is satisfied.

$$f_{sw} = f_r < f_{ds} \tag{4}$$

The mode of operation of the proposed topology is similar to a single-ended Class-E where the turn-OFF of a MOSFET triggers the drain-source resonance circuit and a half sine-wave voltage is generated across the drain-source terminals of the MOSFET [15]. Since the drain-source resonance frequency is higher than the switching frequency, the drain-source capacitor will discharge to 0 V before the MOSFET turns ON, leading to a time period where the body diode is conducting. In Fig. 2a the expected waveforms for the topology are seen, where the drain-drain voltage is defined as $v_{dd} = v_{ds,1} - v_{ds,2}$.



(a) (b)

Fig. 2: (a) Class-E Push-Pull expected voltage waveforms and (b) The absolute value of the equivalent drain-source impedance illustrating the two resonance frequencies of the converter, f_r and f_{ds}.

As seen from Fig. 2a two time periods are defined; t_{ds} and t_{sw} which represent the drain-source resonance period and switching period respectively, with the switching period being equal to the load resonance period. The two different resonance frequencies of the converter are illustrated as an impedance curve in Fig. 2b. The analytical expressions for the voltage waveforms in Fig. 2a are shown in (5) and (6).

$$v_{dd}(t) = \begin{cases} V_{ds} \cdot \sin(2\pi f_{ds} \cdot t), & 0 < t \leq 0.5\ t_{ds} \\ -V_f, & 0.5\ t_{ds} < t \leq 0.5\ t_{sw} \\ -V_{ds} \cdot \sin(2\pi f_{ds} \cdot t), & 0.5\ t_{sw} < t \leq 0.5\ (t_{sw} + t_{ds}) \\ V_f, & 0.5\ (t_{sw} + t_{ds}) < t \leq t_{sw} \end{cases} \tag{5}$$

$$v_r(t) = V_r \cdot \sin(2\pi f_r \cdot t + \theta) \tag{6}$$

Using the analytical expressions in (5) and (6), the proposed topology shown in Fig. 1a can be reduced to the equivalent circuit diagram in Fig. 3, where $L_{eq,dd}$ is the total equivalent inductance between the drain-terminals and resonance load.

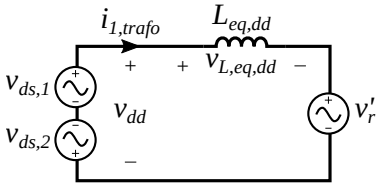


Fig. 3: Equivalent Class-E Push-Pull circuit diagram.

As depicted in Fig. 3, the current injected to the load resonance circuit is dependent on the voltage drop across the equivalent inductance. This can be utilized for controlling the output power of the converter by controlling the phase of this current, similar to a current controlled voltage source converter.

Experimental Verification

The functionality of the proposed topology is confirmed through experimental verification. A prototype converter is built as shown in Fig. 4.

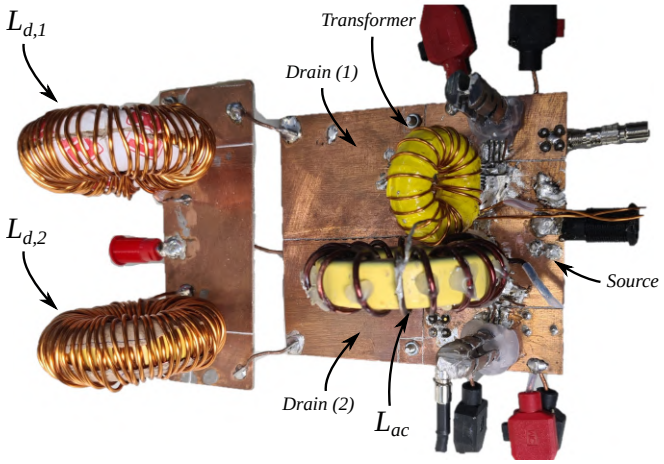


Fig. 4: Built Class-E Push-Pull prototype converter with a transformer between the converter and load.

As observed an AC-inductance L_{ac} is introduced in series with the transformer leakage inductance, thus the stray inductance will be given as $L_{stray} = L_{ac} + L_{lk,trafo} + L_{trace}$. The AC-inductance is needed to obtain the desired drain-source resonance frequency, without exceeding the 12 A current limit of the chosen Wolfspeed C3M0160120J SiC MOSFETs [16]. The commutation loops of the two MOSFETs are designed with a focus on symmetry to achieve similar impact from parasitic inductance and capacitance on the drain-source voltage waveforms $v_{ds,1}$ and $v_{ds,2}$. All magnetic components are designed using core materials with approximately constant permeability in the 2.5 MHz range. The DC-inductors are designed to achieve near constant DC-supply current. Due to the inductors being self-wound a slight deviation in DC inductance is observed. Using the IXDN614YI [17] gate driver, a low inductive hard switched gate driver design has been achieved through symmetrical layout, allowing for fast switching performance without gate-source voltage oscillations while having no external gate resistance. Circuit parameters are given in Table I.

Table I: The circuit parameters used in the built Class-E Push-Pull resonance converter.

Converter side

Components	V_d	$L_{d,1}$	$ESR_{Ld,1}$	$L_{d,2}$	$ESR_{Ld,2}$	L_{ac}	$C_{ds,ext}$
Value	30 V	145 µH	1 Ω	144 µH	1.4 Ω	1.6 µH	440 pF

Load side

Components	$L_{lk,trafo}$	$L_{m,trafo}$	$R_{c,trafo}$	n_{trafo}	L_r	C_r	Q_r
Value	442 nH	4.2 µH	30 kΩ	0.353	93 nH	46 nF	61

The performance of the converter is tested by connecting the secondary side of the transformer to the external resonance tank with a representative single turn induction coil for induction heating purposes designed in [13]. The driver signals for the two MOSFETs are supplied complimentary with a 50% duty cycle. The switching frequency is adjusted until the resonance frequency of the load is met at 2.45 MHz. The resulting experimental results are shown in Fig. 5.

As observed ZVS is achieved with a drain-source resonance frequency of 3.9 MHz ($T_{ds} = 256$ ns). This leaves a tolerable margin of load resonance frequency variations greater than 1 MHz for which ZVS can be ensured. The drain-source voltage amplitude of 163 V yields a significantly higher voltage gain than the usual Class-E voltage gain of approx. 3.6, which is due to the volt-second balance of the DC-inductor yielding a voltage gain dependent on the ratio of the switching and drain-source resonance frequencies as shown in (7) [15, 18].

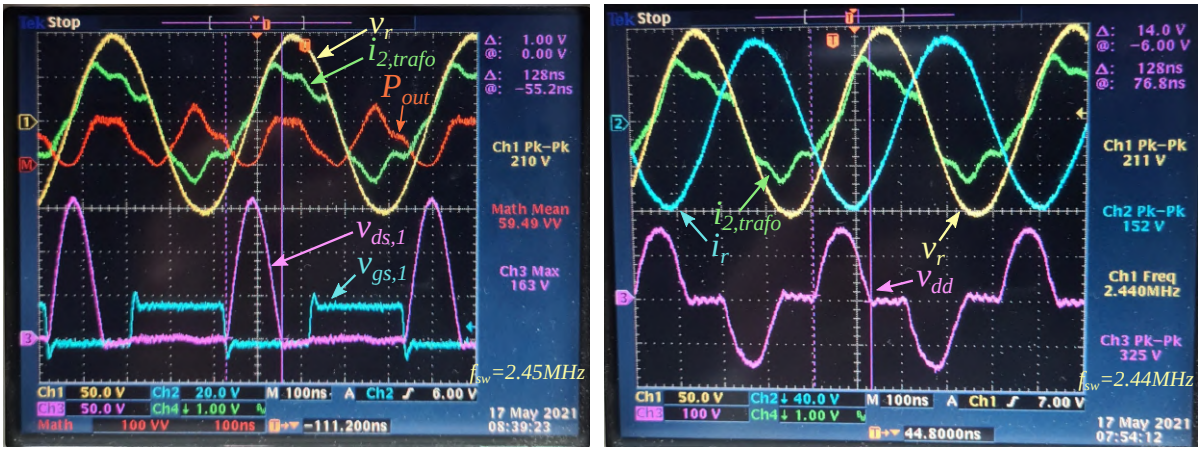


Fig. 5: Experimental results demonstrating the performance of the built prototype converter, with the drain-source resonance frequency being higher than the switching frequency, thus achieving ZVS. The MOSFETs are operated at the resonance frequency of the load, seen from v_r and $i_{2,trafo}$ being in phase. The drain-drain voltage v_{dd} is following the expected trend derived in (5).

$$V_{ds} = (V_d - V_{ESR,Ld}) \cdot 3.562 \cdot \frac{T_{sw}}{T_{ds}} = \left(30\,\text{V} - (1.08\,\text{A} \cdot 1\,\Omega)\right) \cdot 3.562 \cdot \frac{408\,\text{ns}}{256\,\text{ns}} = 164\,\text{V} \tag{7}$$

Where the term $V_{ESR,Ld}$ takes into account the DC-voltage drop across the ESR of the DC-inductor, with an observed DC-current of 1.08 A read from the DC-supply.

The current i_r in the single turn induction coil and the voltage v_r of the resonance capacitor are observed to be approx. 90° phase-shifted due to the reactive nature of the resonance tank. An apparent power of 4 kVA is observed in the resonance tank, which with a supply input power of only 64.8 W implies a reactive power of approx. 4 kVAr.
From Fig. 5 it is observed that the secondary side transformer current $i_{2,trafo}$ is in phase with the resonance voltage v_r, due to switching at the load resonance frequency. By multiplying these two signals the instantaneous output power is obtained, for which the mean active power transferred to the load object through the single turn induction coil is calculated to 59.49 W with an input DC-voltage of 30 V. Thus, the efficiency of the built prototype converter is 91.8 %.

Analysis of Design Robustness

A SPICE model of the proposed design is developed to analyze whether the design has obtained the desired robustness and drain-source resonance frequency predictability in regards to the influence of parasitic inductance and capacitance on the drain-source resonance circuit. Three different SPICE model levels are created with increasing complexity; (*Model 1*) an ideal circuit model, (*Model 2*) a model including the parasitic inductance between the circuit elements and (*Model 3*) a model including the parasitic inductance and capacitance between the circuit elements. A 3D model of the circuit board is shown in Fig. 6 and imported into ANSYS Q3D Extractor to extract the mentioned parasitics. This method has in previous studies proven valuable in determining the parasitic influence on the performance for a given circuit design [19].

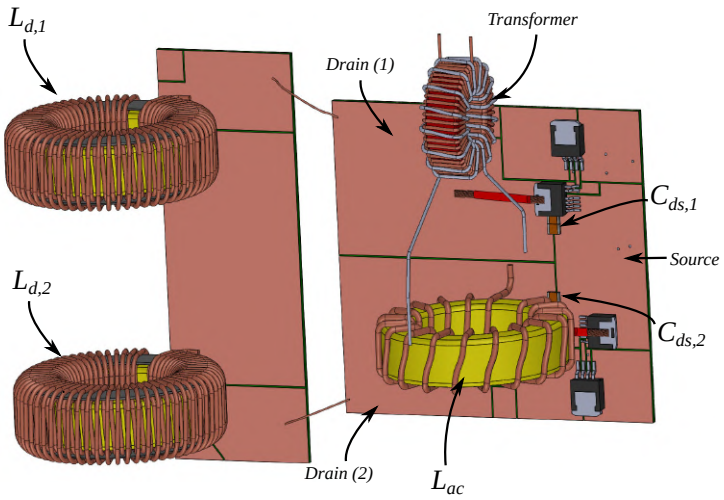
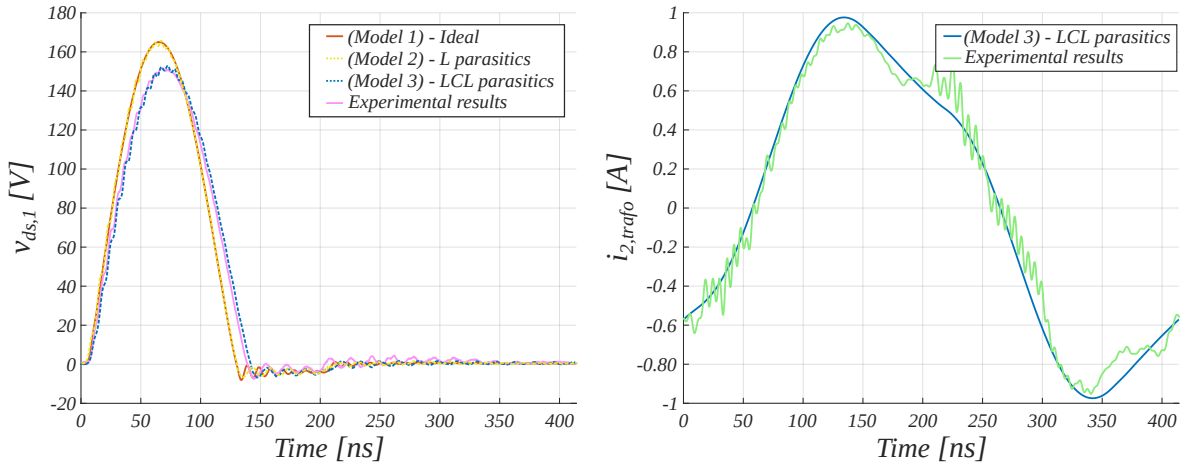


Fig. 6: 3D model of the built Class-E Push-Pull prototype converter.

The three SPICE models are simulated at an input voltage of 30 V and compared to experimental measurements as shown in Fig. 7.



(a) (b)

Fig. 7: Experimental and simulated waveforms with an input voltage of 30 V and a switching frequency of 2.415 MHz. (a) shows the drain-source voltage and (b) shows the secondary side transformer current.

It is observed that the drain-source voltage is similar for both SPICE model 1 and 2. This implies that the drain-source resonance loop in the present design is not influenced by the parasitic inductance between the circuit elements, implying that the first design consideration seen in (1) is satisfied. This outcome is expected as the extracted parasitic inductances between the circuit elements are between 10-30 nH which is 2 orders of magnitude smaller than the inserted stray inductance.
However, the two drain-source voltages from SPICE model 1 and 2 do not match the experimental drain-source voltage. A good similarity is obtained between SPICE model 3 and the experimental measurements, implying that the drain-source capacitance of the present design is influenced by the physical circuit board parasitic capacitance. The parasitic drain-source capacitance is mainly contributed from the capacitance to the bottom side of the PCB, as this is connected to the source plane. The size of the extracted equivalent parasitic drain-source capacitance is read to approximately 80 pF, which is in the same order of magnitude as the external drain-source capacitance of 440 pF. Thus, the constraint in (2) is not satisfied leading to a decrease in design robustness in regards to drain-source capacitance, which is also observed from the deviation between the drain-source voltage waveforms in Fig. 7.

Investigating the secondary side transformer current shown in Fig. 7 it is seen that a great resemblance between SPICE model 3 and the experimental measurements is obtained. This indicates that the impedance of both the transformer and the single turn induction coil is modelled adequately which together with the matching drain-source voltage waveforms enables the use of SPICE model 3 for performance predictability of future designs.

Concerning the design considerations in (1) and (2), the present design has only achieved complete robustness in regards to the parasitic inductance. Ideally the inserted inductance and capacitance should both have been order of magnitudes higher than the parasitic impedances for a fully robust design. Due to the size difference between the stray inductance and the parasitic inductance, it is a possibility for future designs to reduce the inserted stray inductance while increasing the external drain-source capacitance in order to achieve the desired drain-source capacitance robustness. Simultaneously the design constraint from (4) has to be considered in order to maintain a drain-source resonance frequency higher than the switching frequency to ensure ZVS. For the present design the current limitation of the MOSFET's has been a constraint which lead to a minimum allowable stray inductance. Due to this minimum allowable inductance it has not been possible to insert a sufficiently large drain-source capacitor while still satisfying the design constraint in (4) to ensure ZVS. Ultimately, for future designs a trade-off between robustness in terms of capacitance and inductance has to be made, while ensuring ZVS by satisfying the design constrain in (4). Additionally the current limitation of the MOSFET's has to be addressed, which will also aid in the scalability of the proposed design.

Conclusion

In this paper a proof-of-concept of a 4 kVA, 2.5 MHz prototype Class-E Push-Pull resonance converter for industrial induction heating has been demonstrated with an efficiency of 91.8 %. It is shown how the addition of a transformer and an external drain-source capacitor can provide load variation robustness and ZVS capability over a wide range of load resonance frequencies. A digital twin simulation based on parasitic extractions is showing a good agreement between experiment and simulation, which for future designs allows for predictability of the converter performance in new design domains.

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