High-bandwidth Control Structure for Solid-State-Transformers with EtherCAT Protocol

DongUk Kim[1], Jaehong Lee[2], Seung-Hwan Lee[2], and Sungmin Kim[1]
[1] Department of Electrical and Electronic Engineering, Hanyang University, ERICA Campus, Ansan, S. Korea
[2] School of Electrical and Computer Engineering, University of Seoul, Seoul, S. Korea

***Abstract*—This paper proposes a high-bandwidth control structure for solid-state-transformers (SSTs). To fabricate a medium-voltage (MV, 25 kV_{rms}) SST, a 42-level AC/DC rectifier and forty-two dual-active-bridge (DAB) converters are required. However, it is challenging to simultaneously control these converters due to synchronization, propagation delay, and complexity. In this paper, an optimized structure for MV high-level SST controller is proposed. An industrial EtherCAT master PC and state-of-the-art micro-control-units (MCUs) TMS320F28388D are employed to fabricate the control environment. Using the serial-peripheral-interface (SPI) and EtherCAT protocols, a 10 kHz bandwidth data communication between controllers was achieved within a 100 μs delay. Based on the fast communication environment, a partially decentralized voltage balance control scheme, which reduces communication data size, is presented. The proposed controller is evaluated with a PLECS simulation model of the 42-level SST system.**

Keywords—solid state transformer, EtherCAT, high-voltage isolation, controller

I. INTRODUCTION

Conventional medium-voltage (MV, 25 kV_{rms} in S. Korea) grid-tied power electronics use line frequency (LF, 60 Hz) transformers to step down the MV to low voltages (LV, 1~3 kV), which are compatible with semiconductor switching devices. However, LF transformers are bulky and heavy, increasing installation costs in urban areas or trains [1]. Instead of LF transformers, solid-state-transformers (SSTs) have attracted much attention due to their high efficiency, high power density, easy maintenance, and additional functionalities [2]–[4].

The SST consists of cascaded AC/DC rectifiers and DAB converters, as shown in Fig. 1. The DAB converter with the primary and secondary full-bridge converters and a high-frequency (HF) transformer is the key component of the SST system that provides galvanic isolation between MV primary-side and LV secondary-side. To realize an MV SST system, high-voltage isolation of the DAB converter should be solved. Many researchers make efforts to develop MV isolation HF transformers [5]–[7]. In addition to the power bridges, auxiliary power sources for MV-side gate-driving-units (GDUs) require the same isolation strength as the HF transformer. Wireless power transfer (WPT) coils were implemented for the auxiliary sources to meet the high-voltage isolation and high dv/dt immunity requirements [8]–[10].

The input-series and output-parallel (ISOP) configuration alleviates the voltage and current stresses of power transistors. In 2023, state-of-the-art high-voltage transistors in the market have blocking voltages of 1.2, 1.7, or 3.3 kV. Since the 3.3 kV switches are costly and limited in supply, 1.7 kV SiC MOSFET and IGBT are employed in this study. To convert the 25 kV/60 Hz grid to LV using 1.7 kV transistors, the selected dc-link cell voltage is 1 kV, and the net DC voltage of the entire system reaches 42 kV. Consequently, the target SST system requires a 42-level AC/DC rectifier and forty-two DAB converters. The target application of the proposed SST is a power electronic traction transformer (PETT).

From the point of control, it is very challenging to control the many converters consisting of SST simultaneously. Multiple micro-control-units (MCUs) are necessary to generate gating signals, diagnose fault conditions, process sensor signals, and calculate algorithms. In addition, these MCUs should have synchronized clocks owing to the current sharing characteristic of the cascaded AC/DC rectifiers [11], [12]. To complete the requirements, master-slave type control structures are adopted [13]–[15]. Although the master-slave controllers are more stable than decentralized controllers, controller bandwidth and the number of slaves is restricted by communication speed. Generally, the data exchange between master-slave controllers should be finished within one sampling period. Control-area-network (CAN) and serial-communication-interface (SCI) protocols-based SST controllers were reported in [15], [16]. However, the above two protocols have slow communication speeds and are not suitable for a 42-level SST system. Serial-peripheral-interface (SPI) has sufficiently fast communication speed, but it can handle only three or fewer slave controllers.

Instead, the EtherCAT protocol, a well-known communication method in many industrial fields such as robotics, can simultaneously command up to 100 servo motors [17]. The EtherCAT has extraordinary performances in high-speed communication (100 Mbps) and scalability. Due to the demand for high power and modularization of converters for reliability in power electronics systems, the EtherCAT protocol has been adopted in power converters. Jeong *et al.* developed a 13.2 kV 3-phase SST with the EtherCAT protocol [18]. In this study, one EtherCAT master PC and seven MCUs TMS320F28395 were employed to fabricate the control structure. Although the TMS320F28395 requires extra media converters to connect the EtherCAT network, the achieved data transmission interval from master to slaves was 100 μs, which was sufficiently fast for fault protection and control bandwidth. The study used a single MCU per power module to command both primary- and secondary-side converters. However, the

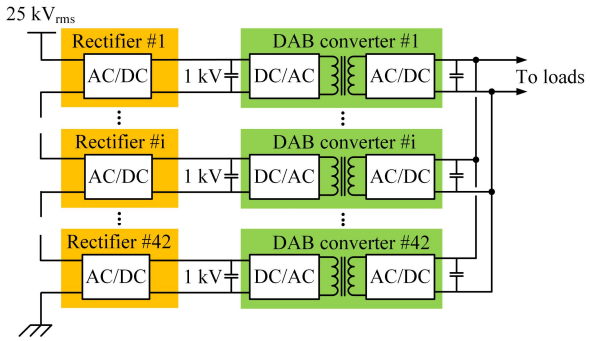


Fig. 1. Block diagram of a medium-voltage solid-state-transformer.

proposed control structure was difficult to apply for the 25 kV SST system because of the high-voltage isolation. Since the primary-side converters have floating potential, their power bridges, sensors, auxiliary sources, and GDUs should be isolated from the ground and require a high-voltage insulation package. It is safe that the MCUs are included in the high-voltage isolation package together. To do so, each power module of SST requires two MCUs, one for AC/DC rectifier and DAB's primary-side and the other for DAB's secondary-side. Then, the high- and low-voltage sides MCUs should be connected by an optic cable to withstand the high potential difference.

In this study, an optimized control structure for high-voltage, high-level SSTs is proposed based on the SPI and EtherCAT protocols. The requirements are generating gating signals, processing sensor signals, monitoring fault protection, and synchronization. To configure the optimal communication environment with the high-speed EtherCAT, a state-of-the-art TMS320F28388D is employed for the EtherCAT slave, and a high-performance embedded PC is used for the EtherCAT master. The 10 kHz bandwidth data transmission with one sample (100 μ s) delay is achieved. Based on the fast communication link, a partially decentralized voltage balance scheme for a modular high-voltage, high-level SST system is presented. Cascaded voltage and current controllers in the synchronous *dq* reference frame regulate the average voltage and the grid current. Meanwhile, partially decentralized voltage balance controllers achieve the cell-balancing of power modules with reduced communication burden. A 25 kV, 42-level, 4.6 MW SST system was built in the PLECS power electronic simulation software. This paper is organized as follows. In Section II, the proposed control structure is described in detail. In Section III, simulation results of a 42-level SST system are presented. Finally, this article is concluded in Section IV.

II. Proposed Control Structure for MV SST

Fig. 2 shows the equivalent circuit of the power module, which is the building block of the 25 kV SST system. The power module consists of three cascaded AC/DC rectifiers and three DAB converters. The DABP and DABS denote DAB converters' primary- and secondary- sides, respectively. The C_{DCP} and C_{DCS} are the dc-link capacitances of the DABP and DABS, respectively. The HF transformer with a turn ratio of 1:1 is employed to isolate the DAB converter. The L_{lk} is the

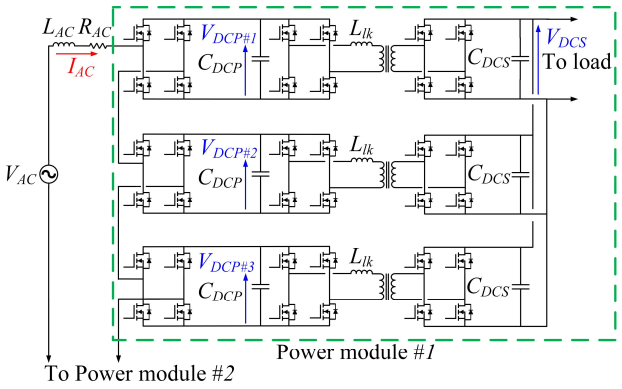
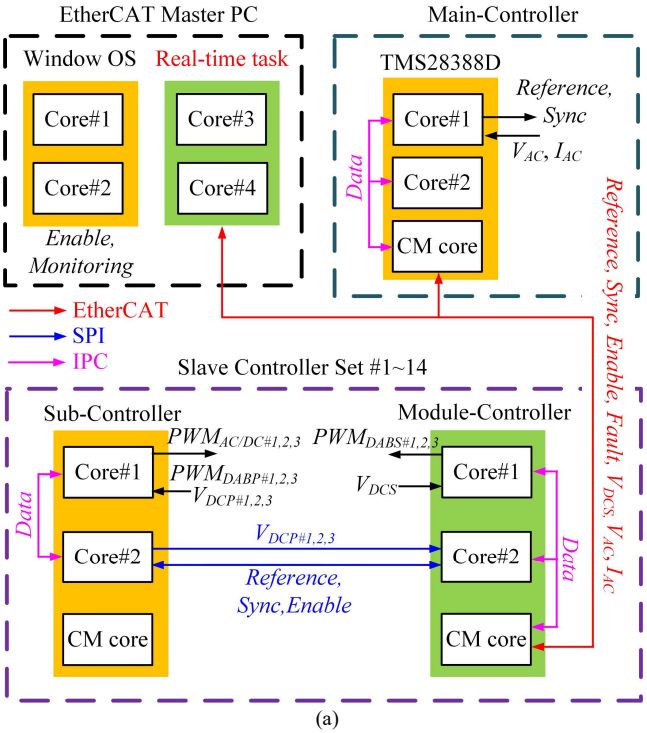


Fig. 2. Equivalent circuit of one of power modules consisting of the SST.

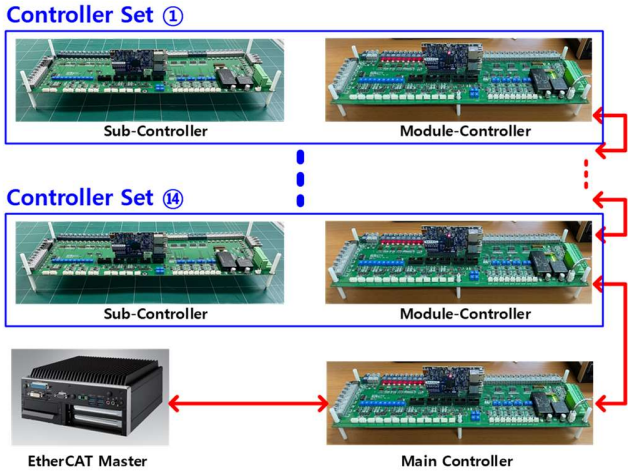
leakage inductance seen from primary-side of the HF transformer. The dc-link voltages of DABP ($V_{DCP\#1,2,3}$) and DABS (V_{DCS}) are regulated to be 1 kV, respectively. The cascaded primary-side voltage of the power module is 3 kV, while the parallel connected output voltage is 1 kV. The V_{AC} and I_{AC} are the grid voltage and current, respectively. The L_{AC} and R_{AC} are the grid filter inductance and resistance, respectively.

A. High-bandwidth communication environment

The target 25 kV, 42-level SST system requires fourteen power modules. To manage the high number of converters, the proposed high-bandwidth control structure is shown in Fig. 3 (a). The control structure consists of three blocks: 1) EtherCAT master PC, 2) Main-controller, and 3) Slave-controller sets. The industrial-embedded PC is employed for the EtherCAT master PC (ARK-3520P [19]), which handles the EtherCAT communication between the devices. The master PC has four cores, two of which operates the Window OS. Meanwhile, the other two cores are exceptionally assigned for the real-time task of the EtherCAT protocol to minimize the latency and suppress the jitter of communication. Users can command the enable signals and monitor the system through the master PC. The state-of-the-art MCU TMS320F28388D is employed for the main-controller and slave controller sets. The TMS320F28388D offers two cores for computation and one connectivity-manager (CM) core that is specialized in EtherCAT communication. The CM core enables EtherCAT communication without the usage of a media converter, which also causes the communication delay. The EtherCAT communication between devices can be accessed through the CM core, as shown in the red arrows in Fig. 3(a). Since the EtherCAT protocol has superior scalability, it is suitable for controllers of high-level SST systems. The signals can be transmitted to the entire device within a 100 μs delay. The main-controller consists of one MCU, which generates a synchronization signal and controls the grid voltage and current (V_{AC} and I_{AC}). The fourteen slave-controller sets consist of two MCUs, module- and sub-controllers. Each module-controller generates gating signals for three DABS converters $PWM_{DABS\#1,2,3}$. The sub-controller generates gating signals for three AC/DC rectifiers $PWM_{AC/DC\#1,2,3}$ and three DABP converters $PWM_{DABP\#1,2,3}$.



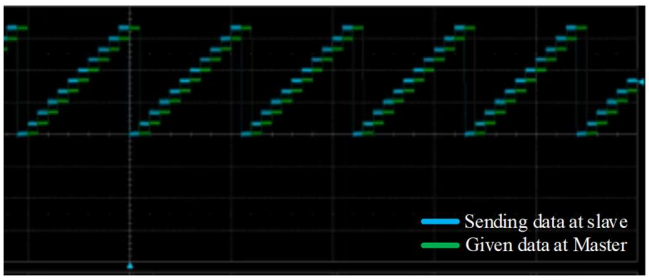
(a)



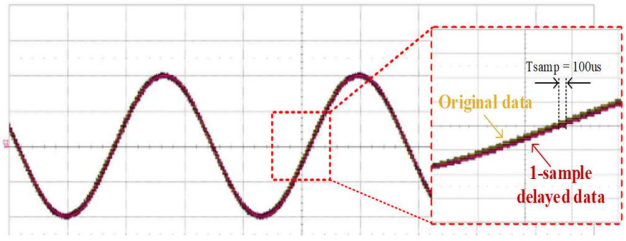
(b)

Fig. 3(a) Proposed control structure. (b) Photo of control structure.

The data exchange among three cores (Core#1, 2, and CM core) are accessed through the Inter-Processor Communication (IPC) and memory-sharing functionalities of the MCU. Between module- and sub-controllers, the data can be exchanged through the SPI port, as shown in the blue arrows in Fig. 3(a). In this study, core#2 of each MCU is assigned for the SPI communication. In contrast, core#1 accepts the sensor signals, computes the algorithm, and generates the PWM signals. Fig. 3(b) shows the photo of the proposed control structure. The EtherCAT master PC, main-controller, and slave module-controllers are connected in series using the LAN cables. The module- and sub-controller pairs are connected by optic cables, which can provide a high-voltage isolation.



(a)



(b)

Fig. 4. The time-delay of configured 10 kHz bandwidth data transmission with EtherCAT protocol. (a) bounding data (10 kHz). (b) AC voltage reference (60 Hz).

Using the communication environment in Fig. 3(b), 10 kHz bandwidth data transmission was evaluated. Although the number of slaves in this experiment was one, the slave sets can be easily expanded without the latency because the EtherCAT has sufficient data capacity. Fig. 4(a) shows the time delay of configured EtherCAT system. The original data is sent from the module-controller to the EtherCAT master PC via the main-controller. Then, it is returned to the module-controller. The sending data increases every 100 μs. It should be noted that the data was transmitted within 100 μs, which is one sampling time of the 10 kHz bandwidth controller. Fig. 4(b) shows the transmitted and received data of 60 Hz voltage references. Since the propagation delay (100 μs) is much smaller than the period of the reference (16.6 ms), stable operation of the current sharing AC/DC rectifiers is achievable.

B. Partially decentralized control scheme

Based on the high-speed communication environment, the control scheme for the MV high-level SST is presented in this section. The key roles of the SST controller are 1) balancing voltages of the cascaded primary-side cells, 2) regulating the output voltage of the secondary-side, and 3) power factor correction of the grid current. Fig. 5 shows the block diagram of the proposed control scheme. The controller consists of three parts: 1) Entire energy controller, 2) Current controller, and 3) Voltage balance controller. The red arrow shows the data transmission through the EtherCAT protocol. In this study, a partially decentralized voltage balance control scheme is adopted to minimize the communication data size [20]. The partially decentralized control scheme does not have a voltage balancing loop. Because the individual DAB converter of cell controls their own DABP dc-link voltage V_{DCP}.

The entire energy of the SST can be calculated as (1) from the output capacitors.

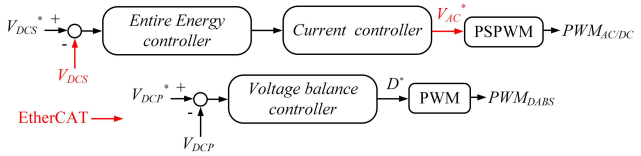


Fig. 5. Proposed control scheme.

$$E_{tot} = \frac{1}{2} N C_{DCS} {V_{DCS}}^2 \tag{1}$$

where N is the number of cascaded cells. Since the output dc-link capacitors are connected in parallel, their equivalent capacitance is NC_{DCS}. If the losses of the system are ignored, d-axis grid current reference in the synchronous reference frame can be derived as (2).

$$ {I_d}^{e*} = \frac{2}{V_{ACpeak}} \cdot \left(\frac{1}{2} N C_{DCS} {V_{DCS}}^{*2} - \frac{1}{2} N C_{DCS} {V_{DCS}}^2 \right) \cdot \frac{{\omega_{ne}}^2}{s^2 + 2\zeta\omega_{ne} s + {\omega_{ne}}^2} \tag{2}$$

where V_{ACpeak} is the peak voltage of the grid, ${V_{DCS}}^*$ is the voltage reference of the DABS, ω_{ne} is the natural angular frequency of the entire energy controller, and ζ is the damping ratio. The open-loop transfer function of the entire energy controller is regarded as a second-order low-pass-filter (LPF). It should be noted that the primary-side grid current reference ${I_d}^{e*}$ is calculated from the energy error of the DABS dc-link capacitors (NC_{DCS}). This is the main difference of the partially decentralized controller, which requires only one of the V_{DCS} for feedback signal. On the other hand, conventional centralized control methods require the whole dc-link voltages of the primary-side ($V_{DCP\#1\sim42}$) to generate the current reference. The proportional and integral (PI) gains of the entire energy controller follow (3) and (4), respectively.

$$k_{pe} = 2\zeta\omega_{ne} \tag{3}$$

$$k_{ie} = {\omega_{ne}}^2 \tag{4}$$

The PI gains make the entire energy controller as the LPF described in (2).

The current controller can be designed from the grid filter inductor loop equation. The d- and q-axis components of the voltage across the grid filter inductor follow (5) and (6), respectively.

$${V_d}^e = I_d^e R_{AC} + \frac{dI_d^e}{dt} L_{AC} - \omega_{AC} L_{AC} I_q^e \tag{5}$$

$${V_q}^e = I_q^e R_{AC} + \frac{dI_q^e}{dt} L_{AC} + \omega_{AC} L_{AC} I_d^e \tag{6}$$

where the I_d^e and I_q^e are the d- and q-axis components of the grid current, and ω_{AC} is the angular grid frequency. To utilize the pole-zero cancellation property, the PI gains of the current controller follow (7) and (8), respectively.

$$K_{pc} = \omega_{nc} L_{AC} \tag{7}$$

$$K_{ic} = \omega_{nc} R_{AC} \tag{8}$$

where ω_{nc} is the natural angular frequency of the current controller.

The voltage balance of the cascaded cells is achieved by the DAB converters. If the output voltage V_{DCS} is regulated very well, the primary-side cell voltage V_{DCP} can be controlled by the phase-shift angle reference D^* of the DAB converter. The V_{DCP} is only transferred between the module- and sub-controller pairs to decide the phase-shift angle. The energy error of the primary-side dc-link cell follows (11).

$$E_{err} = \frac{1}{2} C_{DCP} {V_{DCP}}^{*2} - \frac{1}{2} C_{DCP} {V_{DCP}}^2 \tag{9}$$

where ${V_{DCP}}^*$ is the voltage reference of the DABP. The phase-shift angle can be decided by the power equation of the DAB converter, which follows (10).

$$E_{err} = {P_{DAB}}^* \approx \frac{8 V_{DCP} V_{DCS} D^*}{\pi^2 \omega_{DAB} L_{lk} n} \tag{10}$$

where ω_{DAB} is the angular switching frequency of the DAB converter, L_{lk} is the leakage inductance of the HF transformer seen from the primary-side, and n is the turn ratio of the HF transformer. The PI gains of the voltage balance controller can be decided similarly to the entire energy controller. The PI gains follow (11) and (12), respectively.

$$k_{pb} = 2\zeta\omega_{nb} \tag{11}$$

$$k_{ib} = {\omega_{nb}}^2 \tag{12}$$

where ω_{nb} is the angular natural frequency of the voltage balance controller.

In general, cascaded controllers' natural frequencies are different from each other to avoid cross-couplings between them. The proposed controller has three natural frequencies that should be carefully designed for stability. For stable operation of the proposed controller, the following condition should be satisfied.

$$\omega_{ne} \ll \omega_{nb} \ll \omega_{nc} \tag{13}$$

Since the current controller is located in the inner loop, its natural angular frequency (ω_{nc}) should be much higher than that of the entire energy controller (ω_{ne}). As mentioned earlier, the voltage balance of the V_{DCP} is achieved by the DAB converter, which has a higher switching frequency than that of the AC/DC rectifier. This indicates that the voltage balance controller can achieve a faster dynamic response than the entire energy controller. Therefore, the ω_{nb} should be located at a higher frequency than the ω_{ne}. In this study, the switching frequencies of the AC/DC rectifier and DAB converters are 2 kHz and 30 kHz, respectively. To satisfy the condition in (13),

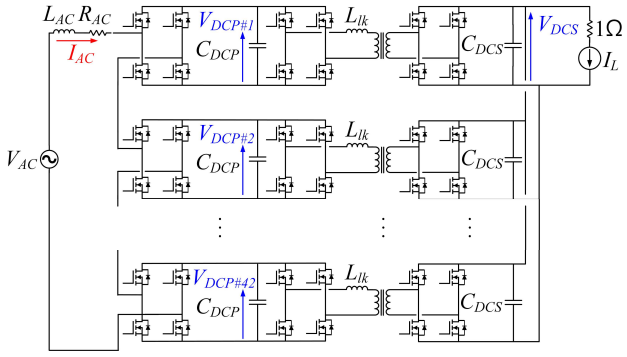


Fig. 6. Simulation model of the 25 kV, 42-level SST system.

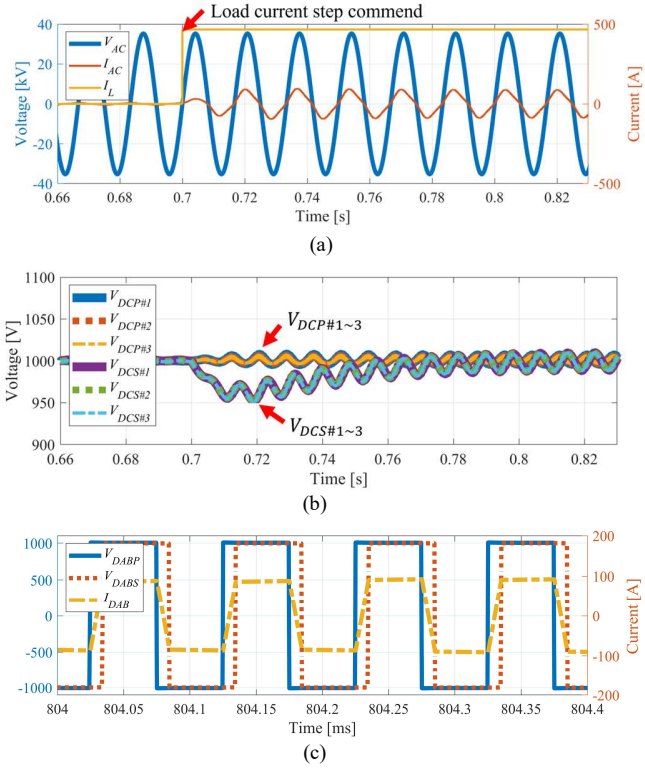


Fig. 7. Simulation waveforms of the 42-level SST system. (a) Grid voltage, grid current, and load current. (b) Three DAB converters' primary and secondary dc-link voltages. (c) Primary and secondary voltages and current of one of the DAB converters.

the selected angular natural frequencies of ω_{ne}, ω_{nb}, ω_{nc} are 31.4 rad/s, 125.6 rad/s, and 3768 rad/s, respectively.

III. Evaluations

To evaluate the proposed controller, a 4.6 MW, 25 kV, 42-level SST system is designed and evaluated using the PLECS [22]. Fig. 6 shows the simulation model of the SST system. The SST consists of 42-level AC/DC rectifiers and forty-two DAB converters. The load resistance of 1 Ω and the current source represent a power electronic traction system. Fig. 7(a) shows the simulation waveforms of the grid voltage (V_{AC}), grid current (I_{AC}), and load current (I_L). The load current was changed from 0 A to 466 A at 0.7 s. The grid current was regulated well. The output power of the entire system was 4.6 MW. Fig. 7(b) shows the three DABP and DABS dc-link voltages. It was assumed that the leakage inductances of the three DAB converters had parameter deviations of 10%. For example, $L_{lk\#1}$, $L_{lk\#2}$ and $L_{lk\#3}$ had 90%, 100%, and 110% values compared to the nominal value. It is notable that the dc-link voltages of the primary and secondary sides achieved the cell balancing. As depicted in (13), the natural frequency of the V_{DCP} was faster than that of the V_{DCS}, the settling times of the DABP and DABS dc-link voltage were different, as shown in the figure. Fig. 7(c) shows one of the DAB converters' primary and secondary voltages and current. The switching frequency of the DAB converter was 30 kHz, and the leakage inductance was designed to 17 μH. At the rated operation, the phase-shift angle between primary and secondary voltage was 20.37°.

IV. Conclusion

In this paper, a high-bandwidth control structure using the EtherCAT protocol for solid-state-transformer (SST) is proposed. The medium-voltage (25 kV_{rms}) SST consists of a 42-level AC/DC rectifier and forty-two DAB converter. To control the SST, the EtherCAT protocol-based control environment was developed. Based on the EtherCAT communication, several controllers can share the data and achieve synchronization between the controllers. The achieved bandwidth of the control environment was 10 kHz with a 1-sample delay. Based on the fast communication, the partially decentralized voltage balance control scheme was proposed. The proposed control scheme were validated with the simulation results.

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