Novel modulation method for common-mode noise reduction in Solid-State Transformer based on ISOP configuration

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Keywords

«Solid-State Transformer», «Converter control», «Power factor correction», «Resonant converter», «EMC/EMI»

Abstract

This paper proposes a modulation method for the reduction of the common-mode noise in Solid-State Transformer (SST) with the ISOP connection. Modular multilevel configurations based on the ISOP connection increase the common-mode noise path because of increasing the switching components. Moreover, the cancellation of the common-mode noise using active common-mode canceler is not able to be applied because of complex common-mode noise path in SST with the ISOP connection. In the proposed method, one of the cells is driven by PWM in order to compensate for the harmonic component. The other cells are driven by square-wave operation in order to share the load. Therefore, the common-mode voltage is suppressed by the switching state of PFC. The advantage of the proposed method is that the additional EMC filter is not necessary for the reduction of the common-mode noise. The operation waveform with the proposed method is shown in the experimental results. The conducted emission is reduced by 11 dB and 7 dB in 200 kHz-band and 1 MHz-band, respectively.

Introduction

Recently, the DC microgrid has been attracted in terms of widespread use of the renewable energies. Solid-State Transformer (SST) is the one of the key components of the distributed system proposed by the Future Renewable Electric Energy Delivery and Management Systems Center [1-3]. SSTs are a power electronic interface between a medium voltage system and a low voltage system, which provides galvanic isolation with medium-frequency transformer [4]. The role of the power converter is the power flow control and the compensation for the reactive power. The medium frequency transformer enables to increase in the power density of the converter. Focusing on improvement of efficiency and power density, various circuit topologies of SST have been proposed in this decade [1-10]. Modular multilevel configurations in based on input series and output parallel (ISOP) have been widely used. The advantage of the ISOP connection is that low on-resister and low-switching loss devices are available because the applied voltage on each cell is divided by the number of cells. For these topologies, SiC-MOSFETs have been widely used because of their fast switching and low on-resistance. However, these wide-bandgap devices increase the common-mode noise due to the rapid switching behavior [11]. The emission limit for information technology equipment is defined in the International Special Committee on Radio Interference (CISPR) 11. Therefore, the EMC filter is designed for compliance with CISPR 11/EN55011 standard [12]. The active common-mode canceler (ACC) based on the voltage cancellation method or the current cancellation has been proposed in [13-20]. These filters have the advantage of suppressing sufficiently the common-mode noise with a push-pull emitter follower amplifier. However, the additional ACC is limited by the rated voltage of the amplifier. Therefore, It is not able to apply the additional ACC to the medium-voltage system such as SST.

In this paper, a novel modulation method is proposed in order to reduce the common-mode noise in SST with the ISOP connection. The advantage of the proposed method is that the additional EMC

filter is not necessary for the reduction of the common-mode noise. The originality of this paper is that the modulation method uses the deference driving frequency in order to suppress the common-mode voltage. Owing to the propose modulation, the leakage current is suppressed in comparison with the conventional modulation. Moreover, the new contribution of this paper is that the reduction of the common-mode noise by replacing high-frequency SiC devices to low frequency Si devices.

This paper is organized as follows: firstly, the system configuration of SST with the conventional method and the proposed method is described. Secondly, the principle of the proposed method for the reduction of the common mode noise is explained with the common-mode equivalent circuit of SST. Finally, the conducted emission is compared between the conventional method and the proposed method in the experiment.

System Configuration

Circuit configuration

Fig. 1 shows the circuit configuration of the single-phase SST when the number of cell is three. Note that the number of cell is decided by the grid voltage and voltage rating of the power devices. Each cell has a PFC stage and an isolated resonant DC/DC converter. The input of the PFC stage in the cells is connected in series. The outputs of the isolated resonant DC/DC converters, which ensure the galvanic isolation, are connected in parallel. The input diode rectifier is common for all cells in order to reduce the number of components. The high-frequency operation contributes to minimizing the isolation transformer. The transformer of the isolated resonant DC/DC converter is smaller than the commercial frequency transformer because the switching frequency is higher than the grid frequency. Besides, the resonant capacitor C_r is connected to the primary side of the isolated transformer in series. The DC/DC converter is controlled with open-loop control due to the constant voltage transfer ratio. The switching frequency is a little higher than the resonant frequency for zero-voltage switching (ZVS) operation.

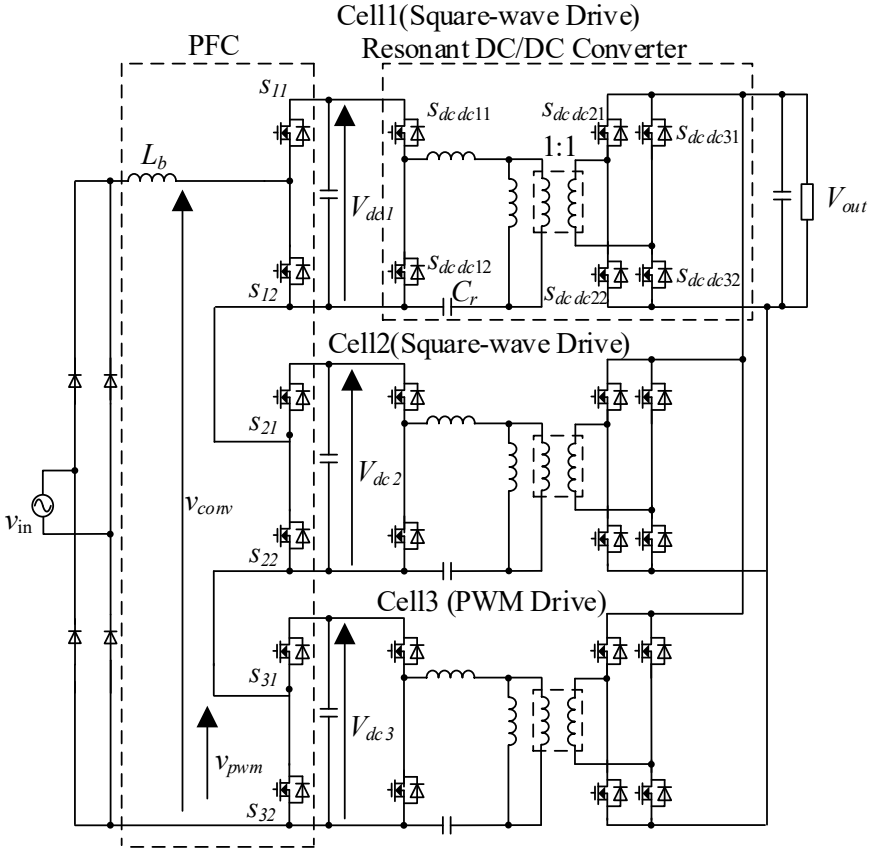


Fig. 1. Circuit configuration of the single-phase SST.
The proposed modulation method is applied into the PFC stage.

Conventional method

Fig. 2 shows the block diagram of the conventional control method of the PFC stages. The conventional method controls the inductor current with PWM in all cells. The overall PFC circuits controls phase and amplitude of the input current to correct the input power factor. Then, reference of the input current is given by

$$i_L^* = I_{amp}\left|\sin(\omega t)\right| \tag{1}$$

where I_{amp} is amplitude of the input current command. The phase of the input current is generated by PLL from the phase of the grid voltage. Note that the ripple current is reduced by operating phase shifted carrier in the PFC converter. Thus, the input voltage is equally divided because the switching timing is equally shifted.

Fig. 3 shows the switching pulse generation of the secondary side rectifier. The full-bridge converter on the secondary side operates as a synchronous rectifier. The switching pulse is the same as the pulse of the primary side. In the primary side, the resonant current i_{re} is positive when S_{dcdc11} , S_{dcdc21}, S_{dcdc32} are turn-on. Note that the phase of the primly side resonant current is a little different in order to design resonant DC/DC converter. Similarly, S_{dcdc12}, S_{dcdc22}, S_{dcdc31} are turn-on when the resonant current is negative.

Proposed modulation method

Fig. 4 shows the relationship between the input voltage and the output voltage of the cell. The switching state of the cell3 is followed by the boost mode. The cell3 is driven by the PWM operation in order to compensate for the harmonic component of the other cells. The cell1 and cell2 are driven by square-wave operation. The output voltage of the cell operated with square-wave is determined by the comparison with the voltage command of the PFC stage and the DC-link voltage of each cell. The switching device on the upper arm of the cell1 turns on when the output voltage command v_{conv} is higher than DC-link voltage of the cell1. Similarly, the switching device on the upper arm of the cell2 turns on

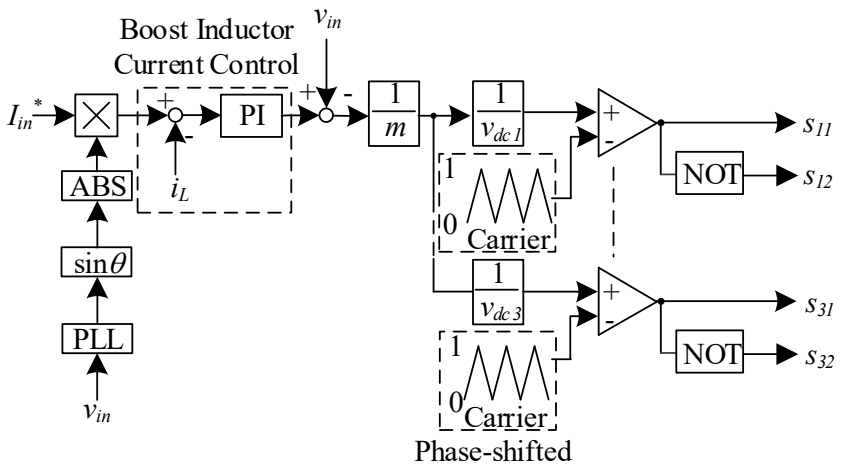


Fig. 2. Control block diagram of the PFC with the conventional method.
The conventional modulation of the PFC is driven by PWM.

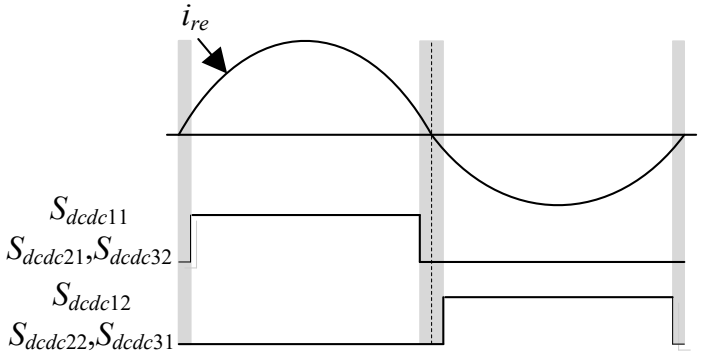


Fig. 3. Pulse generation for secondly side rectifier in DC/DC converter.

when the output voltage command is higher than the sum of the DC link voltages of the cell1 and the cell2. Thus, the output voltage of the cell1 and the cell2 is double of the grid frequency.

Fig. 5 shows the block diagram for the control of the input current with the proposed method. The output voltage of the square-wave cells behave to the current controller as the disturbance because the output value of the PI controller is the total output voltage of all the cell converters. Thus, the input voltage of the cell3 v_{in3} is given by

$$v_{in3} = |v_{in}| - v_{dc1}s_{sqr11} - v_{dc2}s_{sqr21} \quad (2)$$

where v_{dc1} and v_{dc2} are the DC-link voltage of cell1 and cell2, respectively. Moreover, s_{sqrn1} is the switching function of the square-wave cell in the PFC stage. When the upper switch s_{n1} is on-state, s_{sqrn1} equals 1. When the upper switch s_{n1} is off-state, s_{sqrn1} equals 0. As shown in (2), the current controller compensates the output voltage of the square-wave cells with the feed-forward control. Then, the output voltage compensated is the output voltage of the cell3, the gate signal of the PFC circuit is determined with standardizing and comparing triangle carrier. Note that the output power of each square-wave cell is balanced by the sorting the switching state in SST [21].

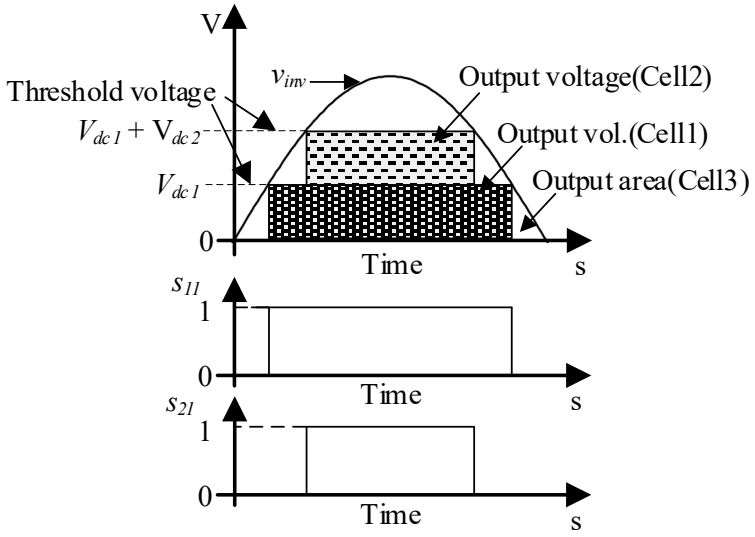


Fig. 4. Operation principle of the proposed method.
The relationship between the input voltage and the output voltage of cell #1 and #2, #3. (m = 3).

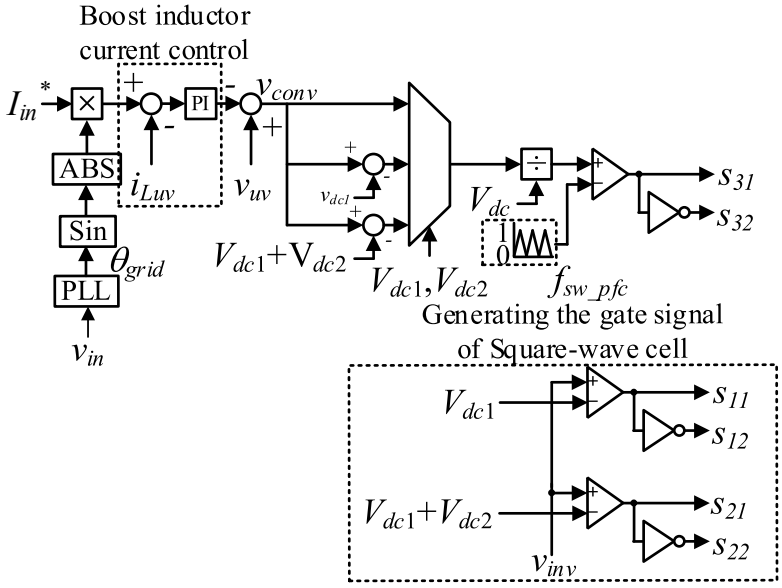


Fig. 5. Control block diagram with the proposed method (m = 3).

Common-mode equivalent Circuit

Equivalent circuit model of PFC

Fig. 6 shows the PFC circuit based on the input series connection with the parasitic components. This model consists two cell converters for the simplification of the following analysis. Note that this model does not consider the different values for the parasitic capacitance, the parasitic inductance and the parasitic resistance. The circuit model considers the parasitic capacitance between the switching component and the heatsink in order to simulate the leakage current generated by the switching operation of the PFC stage. Moreover, the circuit model is symmetric in order to design the equivalent model of the PFC stage.

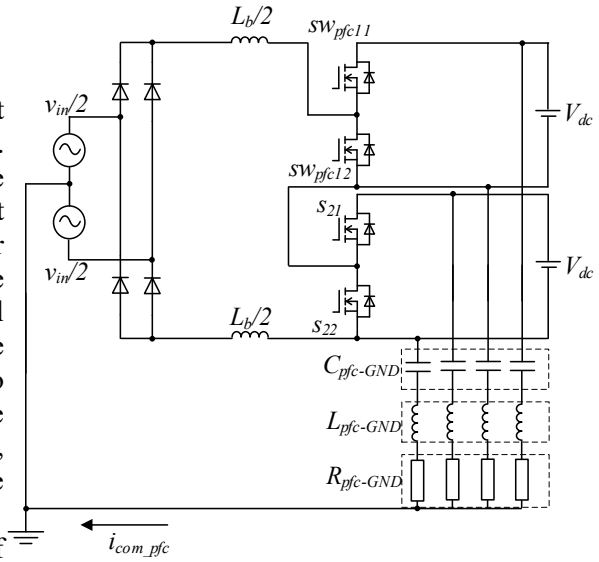


Fig. 6. Circuit configuration of the PFC stage with the parasitic components.

Fig. 7 shows the equivalent circuit model of PFC. C_{pfc_gnd} is the parasitic capacitance. L_{pfc_gnd} is the parasitic inductance. R_{pfc_gnd} is the parasitic resistance. L_b is boost inductance. The common-mode voltage-source v_{com_pfc1}, v_{com_pfc2} are given by

$$v_{com\_pfc1} = sw_{pfc11}V_{dc1}/2 + sw_{pfc21}V_{dc2}/2 \quad (3)$$

$$v_{com\_pfc2} = -sw_{pfc11}V_{dc1}/2 + sw_{pfc21}V_{dc2}/2 \quad (4)$$

where V_{dc1} and V_{dc2} are DC-link voltage of each cell, sw_{pfcn1} is the switching state of the upper arm device, sw_{pfcn2} is the switching state of the lower arm device. Hence, the common-mode voltage is changed by the switching state of each cell. As the shown in Fig. 7, the leakage current of the PFC is given by

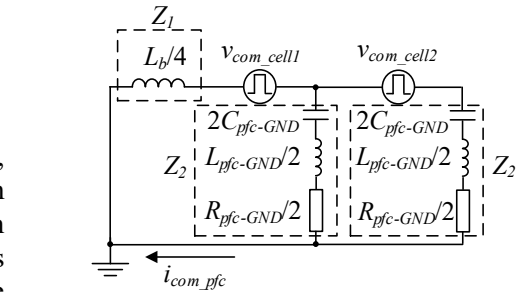


Fig. 7. Common-mode equivalent model of the PFC stage.

$$i_{com\_pfc} = (2v_{com\_pfc1} + v_{com\_pfc2})/(2Z_1 + Z_2) \quad (5)$$

where Z_1 is the impedance of the boost inductor L_b. Z_2 is the combined impedance of the parasitic capacitor C_{pfc_gnd}, the parasitic inductor L_{pfc_gnd} and the parasitic resistance R_{pfc_gnd}. Here, the common-mode voltage v_{com_pfc1} is twice impact of the common-mode voltage v_{com_pfc2} as shown in (5). This means that suppressing the common-mode voltage v_{com_pfc1} is effective in order to attenuate the leakage current in PFC. In the conventional method, the switching operation of the cell1 is caused by PWM. On the other hand, in the proposed method, the switching operation of the cell1 is double of the grid frequency in order to be driven by square-wave. Thus, the common-mode voltage v_{com_pfc1} is suppressed by the proposed method.

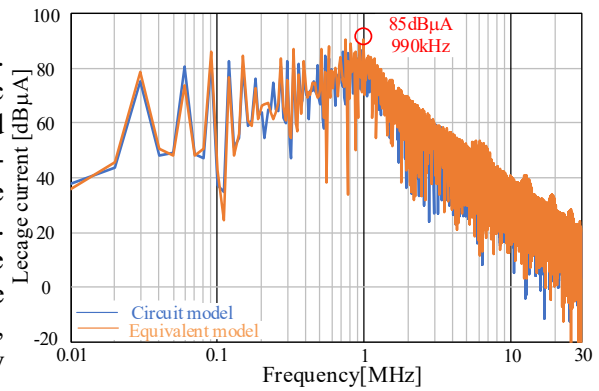


Fig. 8. Comparison of the leakage current between the circuit model and the equivalent model in the PFC stage.

Fig. 8 shows the comparison of the leakage current with the circuit model and the equivalent model in the PFC stage with the switching frequency of 30 kHz. The envelope of the leakage current in the circuit model almost agrees with the equivalent model. Each model has the spectrum of maximum value 85 dBμA at the 990 kHz. This means that the frequency is the resonant frequency between the parasitic capacitor and the boost inductor.

Equivalent circuit model of resonant DC/DC converter

Fig. 9 shows the circuit model of the resonant DC/DC converter with the parasitic components. This model consists one cell converter because the gate signal of each cell is same with the open-loop control. The circuit model considers the parasitic components between the switching component and the heatsink in order to simulate the leakage current generated by the switching operation of the DC/DC converter. Moreover, the circuit model is symmetric in order to design the equivalent model of DC/DC converter.

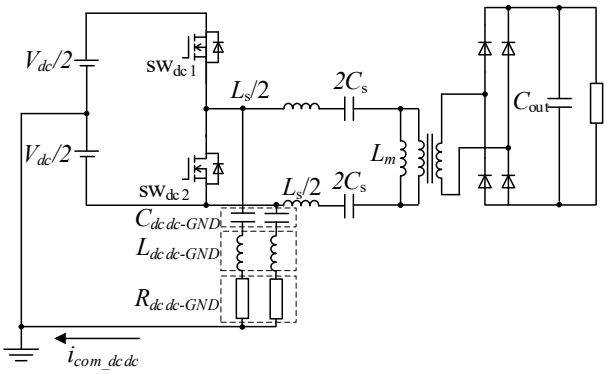


Fig. 9. Circuit configuration of resonant DC/DC converter with the parasitic components.

Fig. 10 shows the common-mode equivalent model of DC/DC converter. Here, C_{dcdc_gnd} is the parasitic capacitance. L_{dcdc_gnd} is the parasitic inductance. R_{dcdc_gnd} is the parasitic resistance. Note that the magnetizing inductance L_m does not consider because the indicator is shorted in the equivalent model. The common-mode voltage-source v_{com_dcdc}, is given by

$$v_{com\_dcdc} = sw_{dc1}V_{dc1}/2 - sw_{dc2}V_{dc1}/2 \quad (6)$$

where V_{dc1} and V_{dc2} are the DC-link voltage of each cell, sw_{dc1} is the switching state of the upper arm device and sw_{dc2} is the switching state of the lower arm device. Hence, the common-mode voltage is changed by the switching state of each cell.

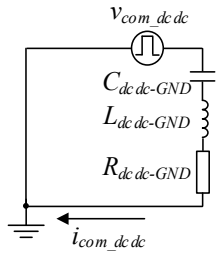


Fig. 10. Common-mode equivalent model of resonant DC/DC converter.

Fig. 11 shows the comparison of the leakage current with the circuit model and the equivalent model in the resonant DC/DC converter with the switching frequency of 50 kHz. The envelope of the leakage current in the circuit model almost agrees with the equivalent model. Each model has the spectrum of the maximum value 101 dBμA at the 2.3 MHz. This means that the frequency is the resonant frequency between the parasitic capacitor and the parasitic inductance.

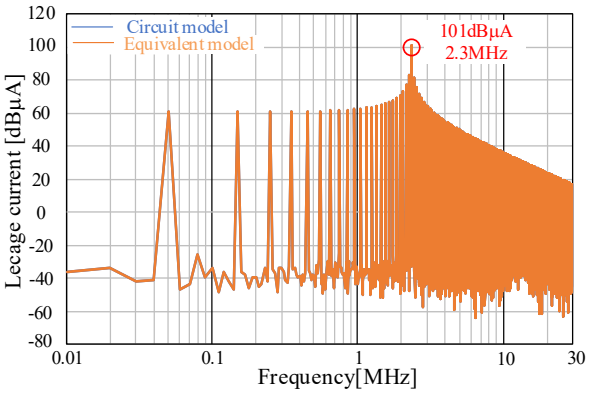


Fig. 11. Comparison of the leakage current with the circuit model and the equivalent model in resonant DC/DC converter.

Equivalent circuit model of SST

Fig. 12 shows the SST circuit model based on the ISOP connection with the parasitic components. This model uses three cell converters for the comparison with experimental model. Note that this model does not consider the different values for the parasitic capacitance, the parasitic inductance and the parasitic resistance.

Fig. 13 shows the common-mode equivalent model of SST. This model considers the parasitic component between the switching devices and the heatsink in PFC and the DC/DC converter. Note that the parasitic component of the secondly side rectifier does not consider because the conventional method and the proposed method are driven by the same operation with open-loop control.

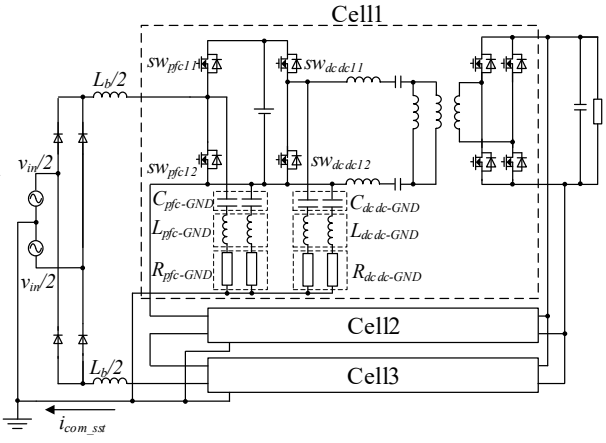


Fig. 12. Circuit configuration of SST with the parasitic components.

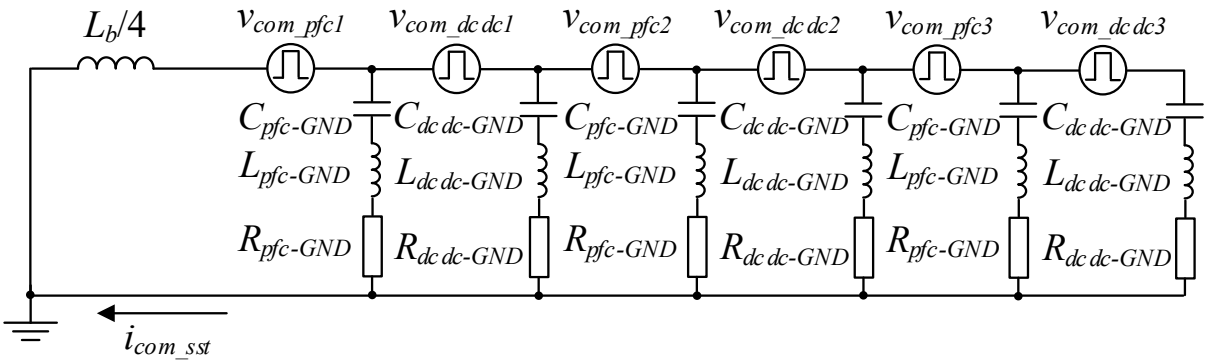


Fig. 13. Common-mode equivalent model of SST.

Fig. 14 shows the comparison of the leakage current between the circuit model and the equivalent model in SST with the switching frequency of 30 kHz in the PFC part using the conventional method. The switching frequency of DC/DC converter is 50 kHz with open-loop control. The envelope of the leakage current in the circuit model almost agrees with the equivalent model. Each model has the spectrum of the maximum value 103 dBμA at the 2.3 MHz.

Fig. 15 shows the comparison of the leakage current between the simulation model and the experimental model. The leakage current has 74.4 dBμA in 120 kHz-band and 87.6 dBμA in 180 kHz-band. Thus, the switching frequency components of PFC is large impact in SST. Moreover, the simulation model is the appropriate model because of almost the agreement with the experimental result.

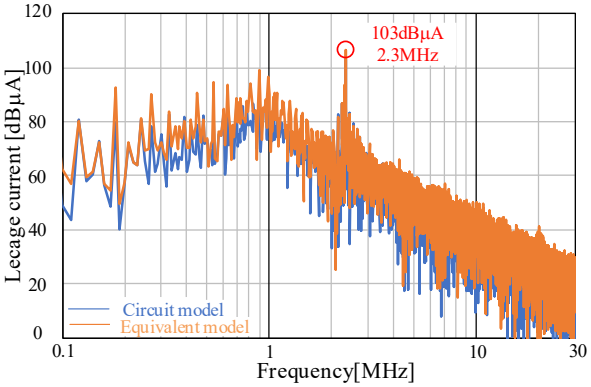


Fig. 14. Comparison of the leakage current with the circuit model and the equivalent model in SST.

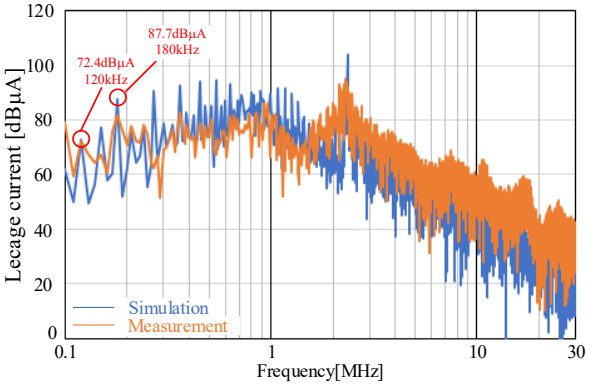


Fig. 15. Comparison of the leakage current with simulation and experiment in SST.

Experimental results

Experimental result with the conventional method

Table I shows the experimental parameters. The input voltage is 200 V, the rated power is 1.0 kW, and the number of cells is three. Moreover, the prototype is operated with the conventional control block diagram, as shown in Fig. 3, and the proposed control, as shown in Fig. 5.

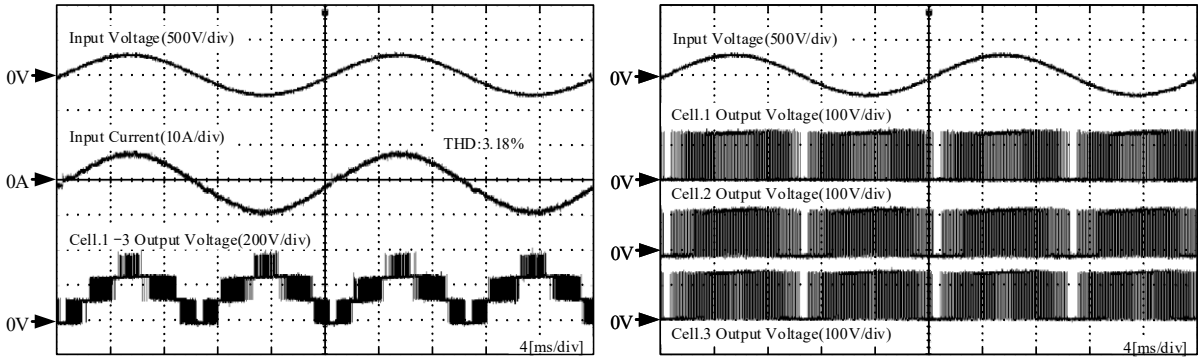
Fig. 16 shows the operation waveforms of the conventional method. Fig. 16(a) shows that the input current THD is 3.18%, and the input power factor is 0.99. Fig. 16(b) shows that each cell is driven by PWM against grid voltage.

Experimental result with the proposed modulation

Fig. 17 shows the operation waveforms of the proposed method. In the proposed method, the switching frequency of the PFC circuits is 30 kHz. Fig. 17(a) shows that the input current THD is 2.91%, and the input power factor is 0.99. In

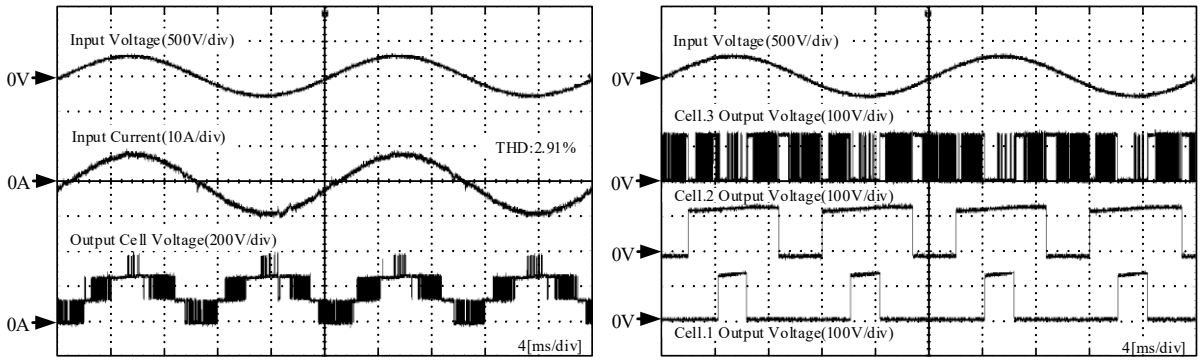
Table I. Experimental parameters.

Input voltage	V_{in}	200 V_{rms}
Rated output power	P_{out}	1.0 kW
Rated output voltage	V_{out}	50 V
Switching Device		SCT2080KE
Grid Freqency	f_s	50 Hz
Primary side capacitor	C_1	1500 μF
Resonant capacitor	C_r	204 nF
Leakage inductor	L_r	50 μH
Secondary side capacitor	C_2	3600 μF
Trans turns ration	N_1:N_2	1 : 1
Number of cells	m	3
Switching frequency of PFC	f_{sw_pfc}	30 kHz
Switching frequency of LLC	f_{sw_llc}	50 kHz



(a) Operation waveform. (b) Output voltage of each cell.

Fig. 16. Operation waveform with the conventional method.



(a) Operation waveform. (b) Output voltage of each cell.

Fig. 17. Operation waveform with the proposed method.

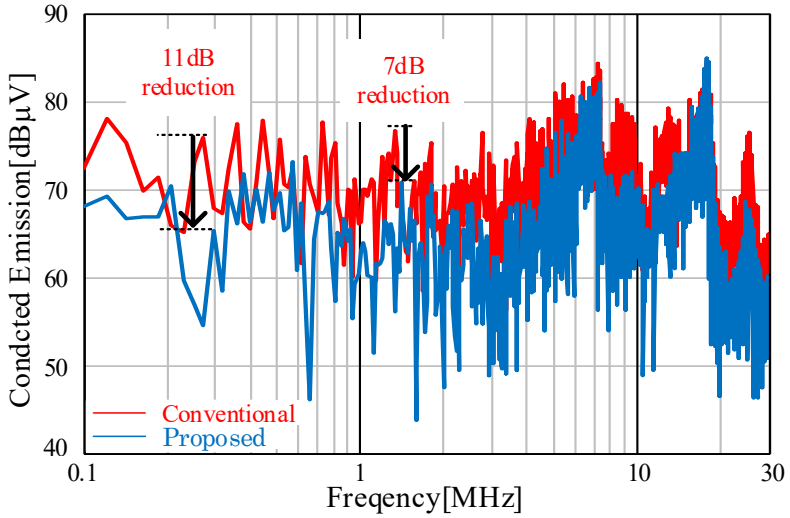


Fig. 18. Frequency spectrum of the Conducted emission with the conventional or the proposed method.

addition, Fig. 17(b) shows the output voltage of the square-wave cells in double of the grid frequency. The PWM cell compensates the harmonic components of the square-wave cell.

Comparison of the conducted emission with the conventional and the proposed method.

Fig. 18 shows the analysis of the conducted emission with the conventional and the proposed method. The proposed method reduces the carrier frequency component produced by PWM. Moreover, the attenuation of almost 11dB and 7dB in 200 kHz-band and 1.2 MHz-band are achieved, respectively.

Fig. 19 shows the comparison of the frequency spectrum with applying PWM to PFC of each cell using the proposed method. Focusing on the frequency spectrum of Cell1 and Cell3, the attenuation of almost 13 dB and 7 dB in 200 kHz-band and 2 MHz-band are achieved, respectively. Thus, the proposed method is effective in order to reduce the conducted emission by applying PWM to the lower cell.

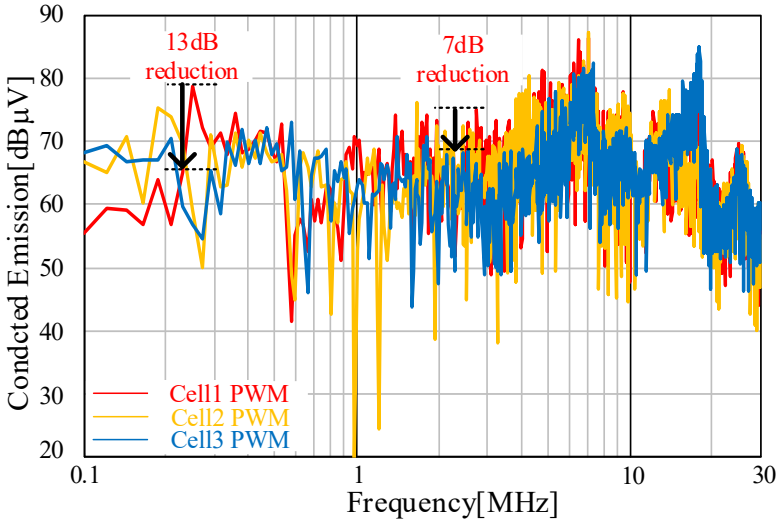


Fig. 19. The comparison of the frequency spectrum with applying PWM to each cell with the proposed method.

Conclusion

This paper had proposed a novel modulation method in order to reduce the common-mode noise in SST based on the ISOP connection. In the proposed method, one of the cells is driven by PWM in order to compensate for the harmonic component. This paper showed the reduction of the common-mode voltage with the proposed method at the switching frequency. The principle of the proposed method was shown by the equivalent circuit of SST. As the experimental result, the conducted emission was reduced by 11 dB at 200 kHz-band, 7 dB at 1 MHz-band with the proposed method. Moreover, the proposed method is effective in order to reduce the conducted emission by applying PWM to the lower cell.

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