# Insulation Design and Analysis of a Medium Voltage Planar PCB-based Power Bus Considering Interconnects and Ancillary Circuit Integration

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## Keywords

«Bus bar», «High power density systems», «Medium voltage converter», «Modular Multilevel Converters (MMC) », «Partial discharge»

## Abstract

This paper presents a design method for a medium voltage (MV) PCB-based bus, focusing on interconnects and considerations for the integration of converter level ancillary circuits. A 6 kV power electronics building block (PEBB) is used as a case study to analyze the design of its PCB bus. Surface mounted balancing resistors and interconnects for power terminals are integrated to further increase the PEBB's power density. PCB-embedded structures, referred herein as shield pads, are introduced as a method to control the peak electric field (E-field) intensity in air near critical terminals and other devices. Additional features to relax the requirements for insulation design within the converter were also incorporated to fully leverage the design flexibility offered from a PCB bus. The final bus demonstrated a partial discharge inception voltage (PDIV) of 11.04 kV.

## Introduction

The introduction of wide bandgap (WBG) power semiconductors devices, such as silicon carbide (SiC) and gallium nitride (GaN), have presented new opportunities in power electronic converter design. These WBG devices offer faster turn-on and turn-off times, higher blocking voltage, and operate at higher junction temperature allowing reductions in passive components and ease cooling requirements [1]. It is essential to consider power loop inductance to ensure components are not subject to an overvoltage as the device turns off. To achieve low inductance, it is common to place parallel conductors serving as a power bus in close proximity to achieve mutual inductance cancellation. Not considering apertures, inductance of a planar bus is directly proportional to conductor length and width and is inversely proportional to the conductor spacing [2]. However, as the conductor spacing is reduced, electric field intensity (E-Field) is increased. Low inductance planar busses have been designed to reduce impedance [2], [3] but did not address high voltage concerns. A medium voltage planar bus was designed for operation in a 6 kV converter but failed to meet partial discharge (PD) requirements [4]. Dielectric thickness is commonly selected considering average E-field intensity and with an added safety factor. However, finite element analysis (FEA) simulations performed in COMSOL Multiphysics indicate a peak E-field intensity more than an order of magnitude larger where the conductor edges interface the dielectric, also known as the triple point. A design method was introduced in [5] which

uses geometric techniques to reduce the peak E-field intensity and optimize insulation thickness to avoid overdesign. In this work, a multilayer PCB is designed using geometric techniques for E-field control to optimize conductor clearances on a layer-by-layer basis to ensure insulation reliability while achieving a low inductance design for operation in a 6 kV 500 kW modular converter utilizing Wolfspeed 10 kV XHV-6 or XHV-9 MOSFET modules with the overall target of >10 kW/l power density. In addition to the bus insulation design, full system integration of the power cell will be considered as the larger purpose is to improve total power density by integrating all necessary power stage components into a highly modular power electronics building block (PEBB). Power levels can be customized by assembling individual PEBBs various series or parallel configurations to achieve higher voltage or current levels respectively, depending on end use requirements. This work is a continuation of [5] which eliminates bulky decoupling capacitors and considers integration of PEBB level ancillary circuitry such as the voltage sensor, temperature sensor, controller, and power supplies for these circuits [6]-[8].

In this paper, Section 1 describes the PEBB-level system architecture. Section 2 describes the method for electric field control used for the overall bus and terminals. The insulation design strategy for terminals, pads, and ancillary components is presented in Section 3. Finally, testing results are provided in Section 4.

## 1. Power Cell Architecture

Each PEBB includes all components necessary for the power cell to operate independently, or as part of a larger converter assembly. In a modular multilevel converter- (MMC) type assembly, PEBBs can be stacked in series to get a higher voltage. To achieve true modularity, each PEBB must be designed to meet the maximum voltage requirement while operating in the MMC. Each PEBB is cooled by a set of push-pull fans powered from an earth-grounded power supply. Since the heatsink is connected to the midpoint (MID) of each power cell, the maximum common mode voltage for the MMC assembly is the MMC bus voltage plus half of the cell voltage (since the heatsink is connected to MID). In this application, the target MMC bus voltage is 24 kV leading to an insulation system designed for 27 kV. The insulation system is divided into two primary zones: PEBB-level and converter-level (referring to the MMC). Components included in the converter-level insulation zone are the heatsink, fans and wireless auxiliary power converter (WPT). Other components have a maximum differential voltage of 6 kV and are included in the PEBB-level insulation design. All ancillary circuits are referenced to MID making this a local ground. The 6 kV 500 kW half-bridge PEBB is shown in Fig. 1 with key components

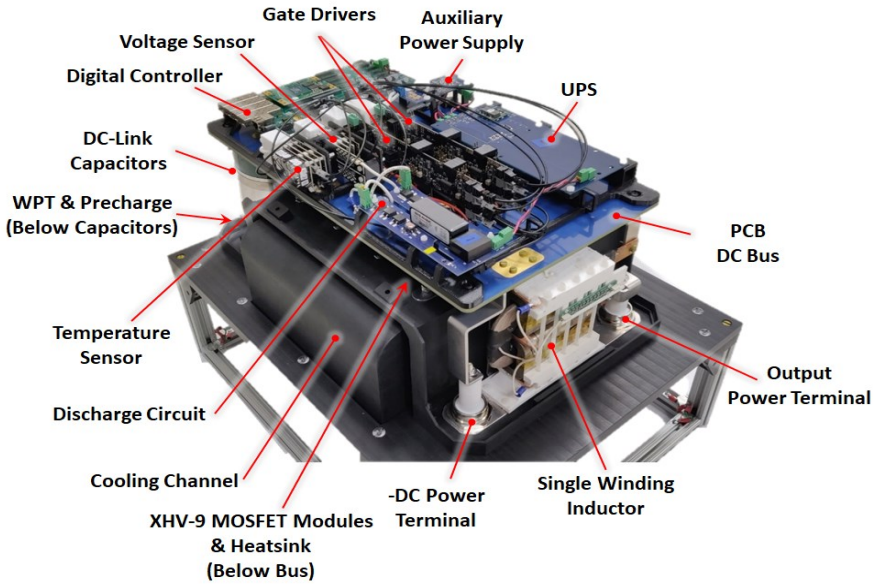


Fig. 1: 6 kV, 500 kW SiC MOSFET-based PEBB with key components indicated; 12 kW/l

indicated. A simplified circuit schematic is shown in Fig. 2. All ancillary circuits are powered from the WPT directly or indirectly. First, the dc-link capacitors are charged from a precharge circuit. Both of these circuits are located under the capacitors for improved power density. The precharge circuit is able to connect across the positive (+DC) and negative (-DC) dc-link capacitor terminals from below the bus. All other powered ancillary circuits are located above the bus which requires a power wire routed from below the bus to above it. Power from the WPT is then split and fed to a current-transform (CT)-based auxiliary power supply (GDPS) and a UPS. The gate drivers, voltage sensor, and temperature sensor are powered from the GDPS. Power to the controller and discharge circuit is passed through the UPS. Three parallel XHV-9 power modules are located below the bus and mounted to a single heatsink. Output from the modules connect to a differential mode (DM) inductor. PEBB power terminals connect to the -DC and the output of the DM inductor.

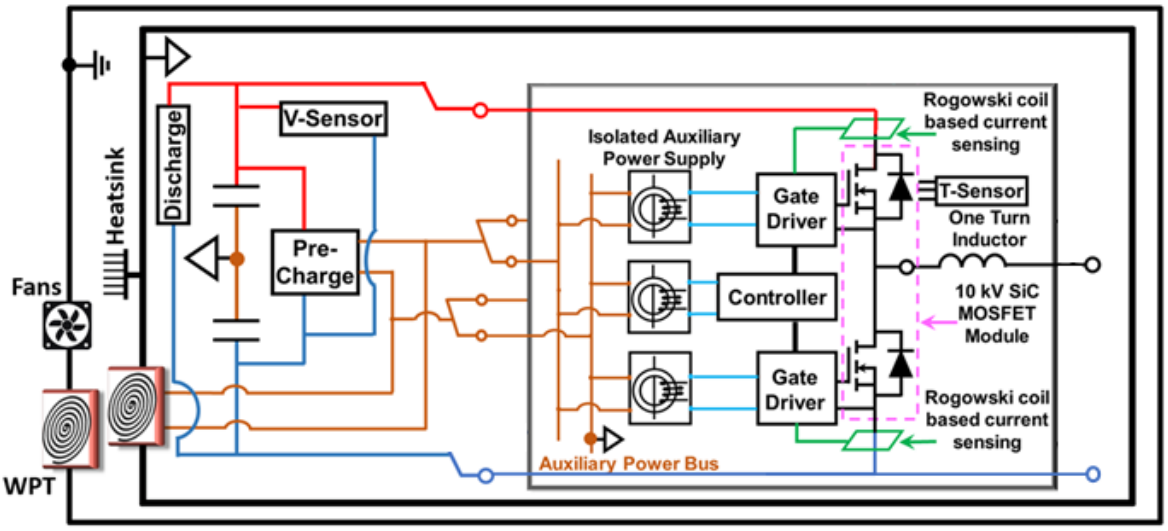


Fig. 2: Simplified schematic of full-bridge PEBB with voltages indicated w.r.t local ground. Dark blue) -3 kV V; Brown) 0 V; Red) +3 kV

## 2. High Voltage PCB Insulation Design

The design flow shown in Fig. 3 was implemented to optimize conductor clearance requirements near component terminals to ensure E-field intensity was within the design target throughout the PCB as well as in air. It should be noted that the terminal modeled in this section can be used for components that have enough space from the edge of the pad, so they do not influence the E-field around this section of the board. A method to account for surface mount components, larger boards with higher voltage, or to simply add an additional safety margin is presented in Section 2. As a continuation from [5], the layer stackup is such that a MID layer is placed as the outermost conductor layer on both sides of the bus followed by +DC and -DC. The +DC and -DC are separated by another MID layer centered between them. In the final stackup, +DC and -DC consisted of multiple parallel layers to increase the current carrying

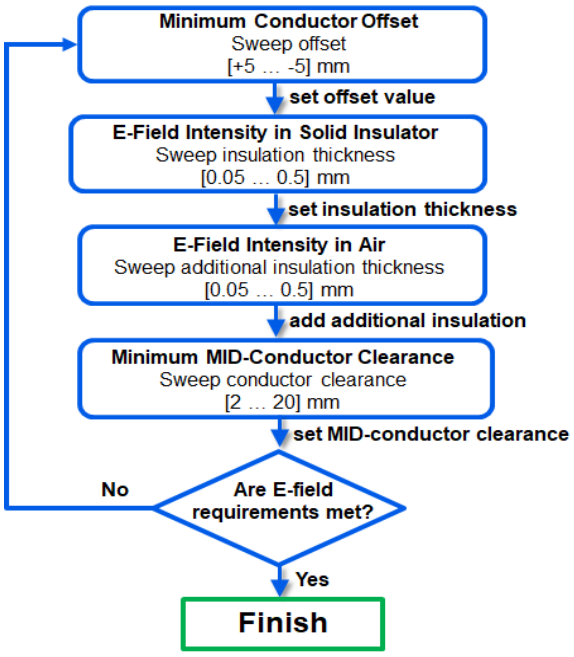


Fig. 3: Design flow for E-field constrained PCB design

capability. The 2D model used for E-field analysis at a terminal connected to the -DC layer is shown in Fig. 4. The material selected was Isola 370HR for its high electrical strength of 54 kV/mm (1350 V/mil) and glass transition temperature of 180 °C. To account for aging [9], a derating factor for FR4 is applied so that the maximum allowable field strength inside of the PCB will be derated. A common value for air breakdown is 3 kV/mm. The actual value at which air begins to ionize may be lower as air conditions vary. The limit for this design is 2 kV/mm in air to ensure its usefulness in applications without corona or surface discharge. Before the design flow was initiated, the +DC and all MID conductor edges were isolated from the -DC terminal to ensure the only factors influencing the results were the actual conductor offset and insulation thickness. The minimum conductor offset determined from Step 1 indicates the importance of incorporating an offset between layer edges as the highest field strength occurred with the case where no offset was applied. Introducing a 1 mm offset reduced the peak field intensity by 13%. After setting the offset, insulation thickness was increased, and the clearance was set to meet the field intensity requirement within the PCB.

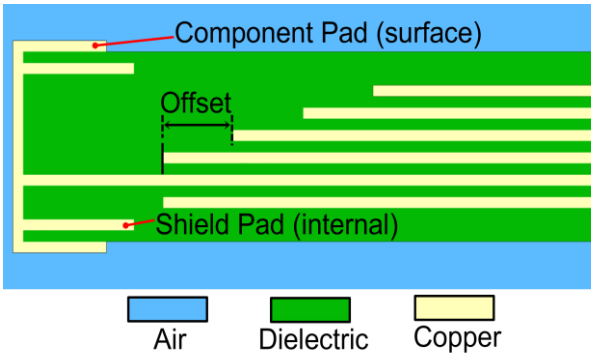


Fig. 4: Example of PCB cross section at component terminal.

To meet field intensity requirements in air, three options were investigated. These included adding dielectric 1) to all layers 2) between the two outer MID and +/-DC layers and 3) adding an additional core between the outer MID layers and air. Adding the additional core between the outer MID and air proved to be the most effective option as this forced the high fields into the dielectric instead of air.

## 3. Ancillary Circuits and Power Terminals

To achieve a highly modular design, ancillary circuits necessary for the power converter operation should be included in a single PEBB enclosure. The target power density is >10 kV/l power density, which requires components to be placed in close proximity to each other. With the bus structure implemented, the outer most bus layers are at the MID and serve as local ground. This allows the local controller, power module temperature sensors, voltage sensor, and their power supplies to be referenced to the same local ground and placed in close proximity to the bus with low E-field between. Shared terminals for the voltage sensor measurement and bus discharge were created using the standard approach presented in Section 2. E-field simulations were performed in ANSYS Maxwell 3D to determine spacing for components with high differential voltage such as the power terminals. Interconnects were designed to keep the peak E-field below 2 kV/mm.

For cold start operation, the PEBB is designed with a 10 kV 12 W custom pre-charge circuit. To charge the 32.5 µF capacitors, power dissipated through balancing resistors should be limited. Twelve surface mount device (SMD) resistors rated at 1 MΩ/1 W were placed in series between the dc-link capacitor terminals to provide voltage balancing while dissipating 3 W at full voltage. A small radius on SMD pads causes a high E-field intensity in that region. To alleviate this issue, shielding pads were placed on layers below the SMD pads to concentrate fields inside of the PCB dielectric rather than air; see Fig. 5.

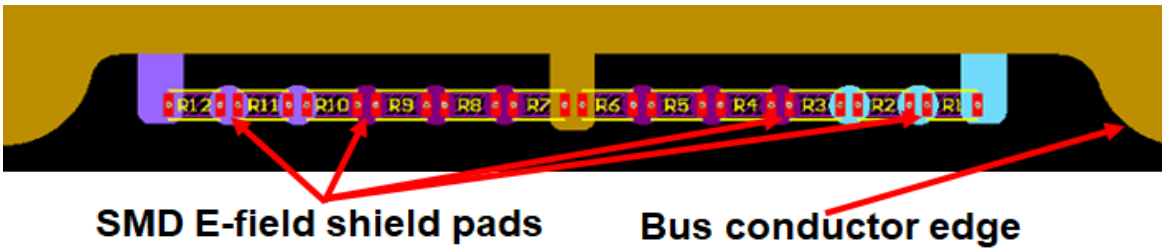


Fig. 5: PCB embedded pads for SMD component electric field control

For thicker boards, optimizing the height and width of this shield pad can reduce the peak field intensity in air by an order of magnitude while preserving overall insulation reliability [10]. Although they can be placed at any height that meets the maximum field strength requirements, placing them on existing layers used for one of the other bus conductors can reduce the final board cost due to a lower layer count.

Power from the WPT must be routed from below the bus to the top. Although the wire is approximately 48 V w.r.t. local ground, placing it near the board edges can still cause field enhancements due to the embedded +DC and -DC layers. Additionally, thermocouples referenced to MID must connect from the temperature sensor above the bus to the heatsink below. These wires have very small radii and present challenges like the WPT power wire. Leveraging the flexibility offered from a PCB, plated-through-holes (PTH) connected to MID can be used as shielded feedthroughs for wires and cables that need to pass from one side of the bus to the other. The hole diameter is dependent on the size and number of wires passing through any one PTH. Although this method can be used to pass wires at any voltage common to one of the bus plan voltages, there is no requirement to size the PTH outer annular ring since the outermost conductor layers are also MID. A 3D rendering of the PCB bus is shown in Fig. 6.

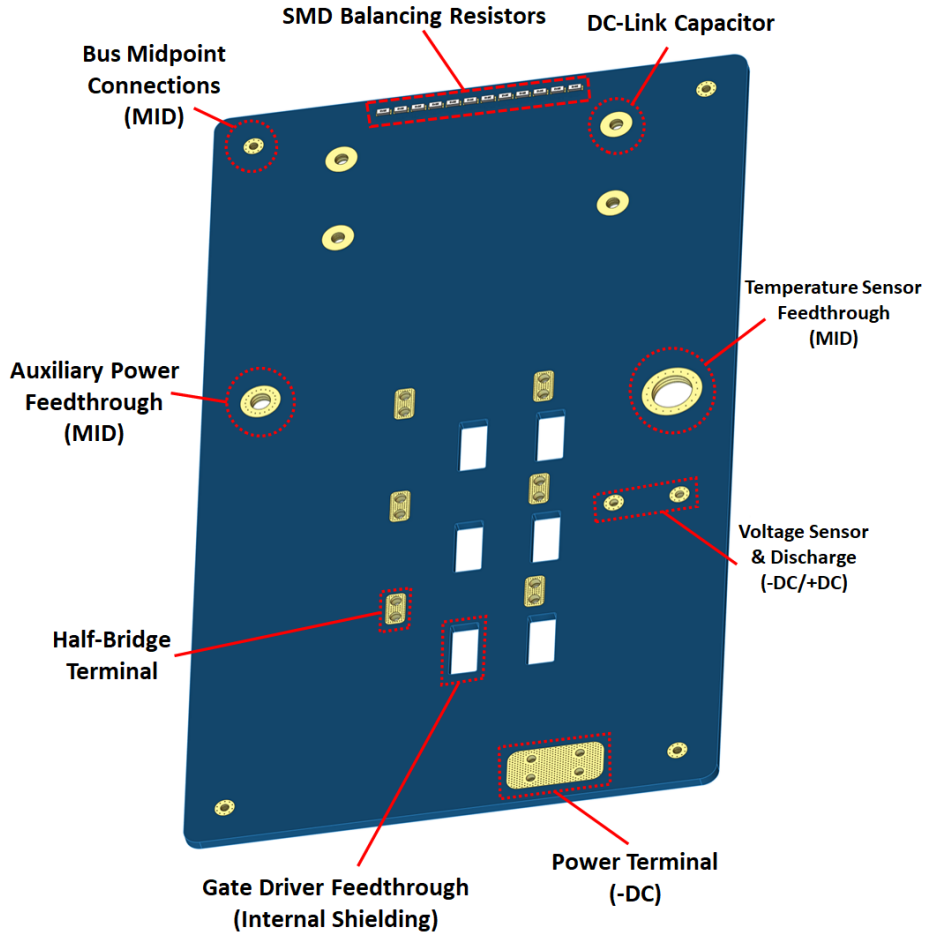


Fig. 6: 3D rendering of 6 kV PCB bus with terminals and feedthroughs labeled

## 4. Experimental Results

The bus insulation quality was tested using an MPD 600, 1 nF 100 kV coupling capacitor, and a measurement impedance for PD measurement and analysis. A 60 Hz sinusoidal excitation was applied using a Phenix 6CP100/50-7.5. High voltage (HV) and reference (REF) were connected across +DC, -DC, and MID in various combinations to test the insulation across each adjacent layer and well as +DC and-DC. Individual discharge events are plotted as a function of magnitude and time, then superimposed on top of the voltage excitation signal. The pattern created is the phase resolved partial discharge (PRPD)

diagram. The PRPD pattern can help determine the type of discharge events that are likely occurring, e.g., PD or corona discharge. Corona discharge occurs in air near the insulator due to a metal part ionizing the air. PD occurs of the insulation. This can near the triple point or anywhere within the insulation due to defects such as voids, delamination, or contaminants.

The PDIV for each layer combination is shown in Table I. All combinations were required to ensure that each insulation layer was tested adequately. Due to the varying nature of PD measurements, six measurements were taken for each connection and averaged. Although the PDIV for Connection 6 much higher than the other measurements, this is expected since the total insulation between +DC and -DC is much thicker than any of the other layer combinations (MID is left floating). In the final application, the maximum voltage between any two adjacent layers is 3 kV. The minimum measured PDIV is about twice the operating voltage. Fig. 7 shows the PRPD for Connection 6. Here, the tested insulation is inside of the PCB between +DC and MID layers as well as the air insulation primarily at +DC and MID terminals. The voltage was kept at the PDIV for 3 minutes to record the PRPD pattern. This pattern indicates discharge occurs first in air which is consistent with what is expected based on simulation results.

**Table I: Bus PDIV for various layer combinations**

| **Connection** | High Voltage | Reference (GND) | Floating | PDIV (kV) |
|---|---|---|---|---|
| 1 | -DC | MID | +DC | 7.96 |
| 2 | +DC | MID | -DC | 6.31 |
| 3 | +DC | -DC | MID | 11.04 |
| 4 | +DC & -DC | MID | - | 6.03 |
| 5 | +DC & MID | -DC | - | 6.42 |
| 6 | -DC & MID | +DC | - | 5.77 |

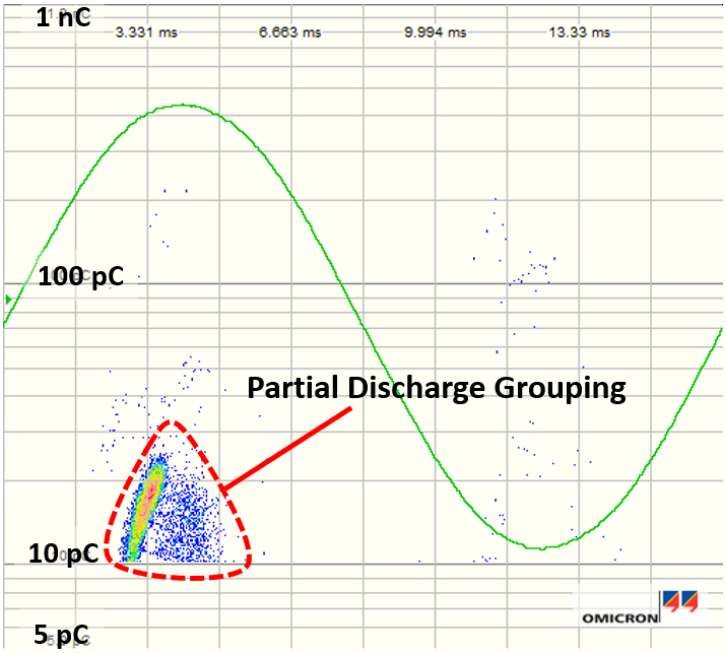


Fig. 7: PRPD pattern for insulation test between layers +DC and MID.

## Conclusion

In this work, an MV PCB-based dc bus is presented, demonstrating PD free operation up to 11.04 kV. As the PCB fabrication process is mature, insulation quality is superior due to lower defects when compared to a conventional planar laminated bus. Due to the inherently low inductance, overall system weight and cost can be reduced by eliminating decoupling capacitors and placing the dc-link capacitors directly on the bus. The converters power density can be increased by placing ancillary circuitry, such as discharge and measurement circuits, in the area previously occupied by decoupling capacitors. To fully utilize the customizability offered by a PCB bus and eliminate long wire runs with a high potential, terminals should be added near circuitry that would otherwise need to connect to the dc capacitor terminals via long traces for power or measurement purposes. Additionally, shield feedthroughs connected to any potential can be placed where necessary for cables to pass from above to below the bus without creating field enhancements near the board edges.

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