Investigation of the short-circuit type II safe operating area of IGBTs

[1]Madhu Lakshman Mysore, [1]Mohamed Alaluss, [1]Abhishek Maitra, [1]Thomas Basler,
[2]Roman Baburske, [2]Franz-Josef Niedernostheide, [2]Hans-Joachim Schulze

[1]Chemnitz University of Technology, Chair of Power Electronics, Chemnitz, Germany.
Tel.: +49 371/531-36091.
Fax: +49 371/531-836091.
[2]Infineon Technologies AG, Neubiberg, Germany
E-Mail: madhu-lakshman.mysore@etit.tu-chemnitz.de
URL: https://www.tu-chemnitz.de/etit/le/ and https://www.infineon.com/

Acknowledgements

This investigation was funded by the Power2Power project. Power2Power is a European, co-funded innovation project involving the semiconductor industry. The project receives grants from the European H2020 research and innovation program, ECSEL Joint Undertaking, National Funding Authorities, and from eight countries involved in the project including the German Federal Ministry of Education and Research (BMBF) under grant agreement No. 826417. The authors would like to thank Karen Hanson for critically reading the manuscript. Additionally, the authors would like to thank Sven Mauerberger from the faculty of mechanical engineering for his help with the sample preparation for failure analysis.

Keywords

«IGBT», «Short circuit», «Current filaments», «Device simulation», «Ruggedness».

Abstract

This study focuses on the short-circuit type II safe operating area (SC-II SOA) with and without gate-emitter voltage clamping. The SC-II measurements without gate-emitter voltage (V_{GE}) clamping show a reduced SC-II SOA at higher DC-link voltages induced by transient gate-emitter voltages that are far beyond the allowed level. These high transient gate voltages result in correspondingly high peak currents. As a consequence, they cause device failure during the negative $\mathrm{d}i_C/\mathrm{d}t$ phase, which is induced by the inductive overvoltage. However, the SC-II SOA can be completely recovered to the level of the SC-I SOA by applying an appropriate V_{GE} clamping circuit, although the IGBT will be subjected to harsher conditions in the SC-II event compared to the SC-I event. To understand the failure types observed in SC-II measurements with and without V_{GE} clamping, computer-aided TCAD simulations were performed using a real front-side, trench-gate IGBT structure.

Introduction

The insulated gate bipolar transistor (IGBT) is one of the most frequently used power semiconductor devices in the field of power electronics. A very important property for many applications is short-circuit (SC) ruggedness. However, IGBTs can be exposed to different short-circuit types (SC-I, SC-II, SC-III or more) in the application described in [1-6]. SC type I (SC-I), or hard switching faults (HSF), occur if the IGBT turns on into an existing short-circuit [4]. The short-circuit type I safe operating area (SC-I SOA) for different voltage classes ranging from 600 V to 6500 V were investigated in [7-14]. The results shown in [10, 11] indicate that an IGBT SC failure can be due to the formation of current filaments occurring at the collector side. Typically, these current failures occur far beyond the safe operating area (SOA) of the IGBT [10, 11].

Short-circuit type II (SC-II), or fault under load (FUL), occur during the conduction phase of the IGBT [2, 3]. In real applications, it is more likely for the IGBT to experience SC-II than SC-I. Hence, it is important to study the ruggedness of the IGBT under SC-II conditions and to understand the root cause of the limitation in the SC-II SOA of the IGBT.

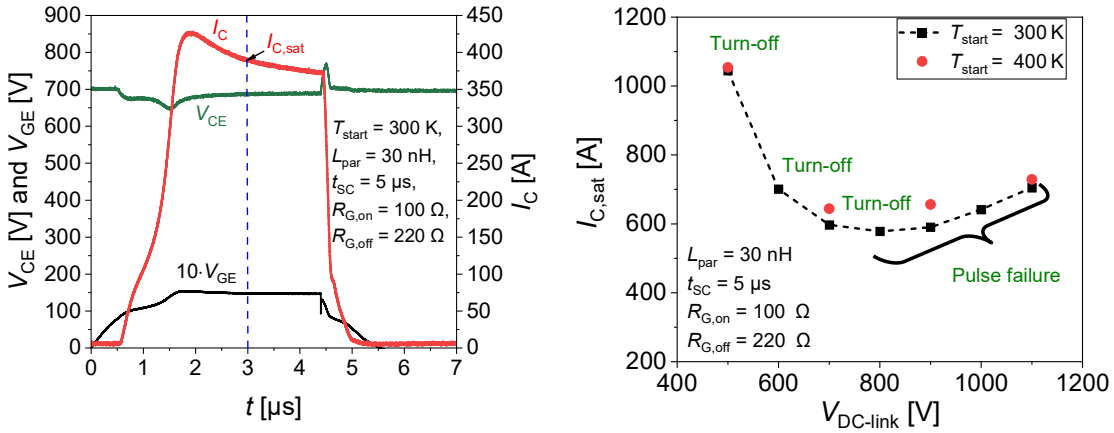
In the present work, SC-I measurements were initially performed on single-chip, 1700 V IGBTs with trench technology, using chips soldered on a direct copper bonded (DCB) substrate. The measured SC-I results show a U-shaped destructive boundary line in the $I_C - V_{DC\text{-}link}$ phase space, where I_C and $V_{DC\text{-}link}$ denote the collector current of the IGBT and the applied DC-link voltage. To study the SC-II ruggedness of the 1700 V single chip, SC-II measurements were carried out initially without gate-emitter voltage (V_{GE}) clamping and without common-emitter

inductance (L_{CE}). The influence of the L_{CE} without V_{GE} clamping was also taken into account in the SC-II measurements. Furthermore, V_{GE} clamping was applied in SC-II measurements. Using a technology computer-aided design (TCAD) tool, 2D electro-thermal SC simulations were performed for a 1.7 kV IGBT trench-gate cell structure to study the internal behavior of the IGBT during SC-II events.

Simulation model

The measurements performed in this work cannot provide an explanation for the internal behavior of the IGBT. However, the electro-thermal simulation results will help to understand the different failure modes that occur during SC-I and SC-II. The following device simulation using the *Synopsys TCAD* tool was carried out to study the SC turn-off failure, the pulse failure and the negative $\mathrm{d}i_C/\mathrm{d}t$ failure [15]. A multi-cell, trench-gate 1.7 kV IGBT was designed and used to investigate the current filament behavior under different $V_{DC\text{-}link}$ and collector current (I_C) conditions. Also, simulations were carried out with and without V_{GE} clamping. The simulated IGBT structure was 192 µm wide. A time-dependent, electro-thermal SC-II pulse was simulated with a starting temperature (T_{start}) of 300 K, parasitic inductance (L_{par}) of 30 nH, for a fixed gate-emitter voltage (V_{GE}) and with an applied DC-link voltage. The University of Bologna mobility model, together with the carrier-carrier scattering model were utilized as well as the University of Bologna avalanche model and the Shockley-Read-Hall (SRH) and Auger recombination models, and the Slotboom model for effective intrinsic density. For the SC simulation, self-heating was considered with a thermal boundary condition at the collector contact and a thermal resistance of 0.505 K/W. The SC pulse width was set to 5 µs.

SC-I SOA of the IGBT



(a) SC-I at $V_{DC\text{-}link}$ = 700 V, V_{GE} = 15 V

(b) SC-I measured destruction limit

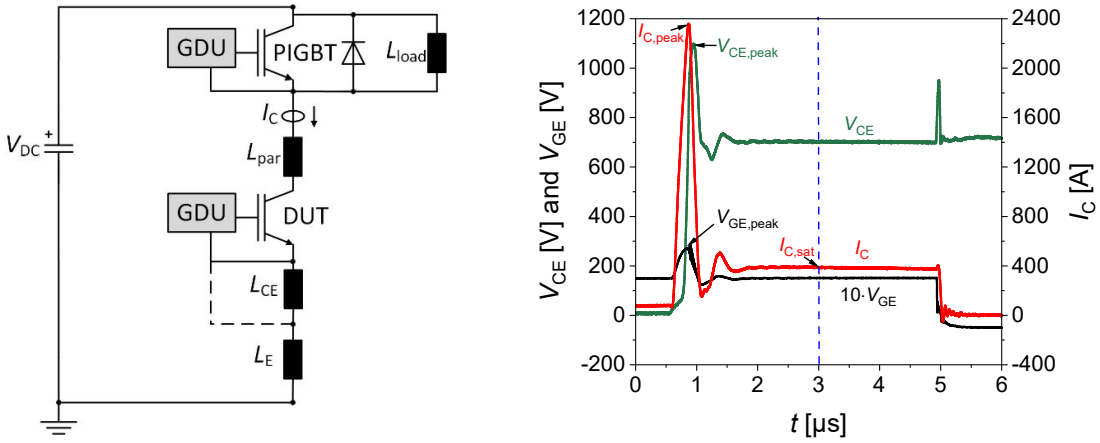
Fig. 1: (a) A typical measured SC I waveform for a non-destructive pulse and (b) measured destruction limit far above the SC-I SOA in I_C-$V_{DC\text{-}link}$ phase space for 1.7 kV single-chip IGBT at different temperatures. The text indicated at the different points describes the failure modes.

For comparison with the following SC-II investigations, a typical SC-I waveform is shown in Fig. 1(a). The black and red points show the critical saturation collector current ($I_{C,sat}$) as a function of the DC-link voltage ($V_{DC\text{-}link}$) of the last non-destructive SC-I pulse at two different temperatures in Fig. 1(b). For a fixed V_{CE}, the destruction current limit was measured by increasing the gate voltage in increments of 0.25 V. A short-circuit pulse width of 5 µs was set for all measurements. The minimum destruction indicated occurs at 800 V for the 1.7 kV IGBT during a SC-I occurrence. For both temperatures, as shown in Fig. 1(b), the decrease in SC ruggedness from 500 V to 800 V is due to the formation of destructive current filaments [10, 11]. It is important to note that the respective applied gate voltage for this experiment was clearly above the datasheet limits. Above 800 V, the SC capability increases again due to the recovered homogenous current distribution in the IGBT, as the space-charge region covers the entire drift region at a higher applied DC voltage and higher collector current [11]. For DC-link voltages from 500 V to 700 V, the destruction of the IGBT occurred during the SC turn-off and for DC-link voltages from 800 V to 1100 V during the SC pulse. A similar type of failure occurred at higher temperatures with a slightly higher last-pass saturation collector current.

SC-II SOA of the IGBT without V_{GE} clamping

SC-II measurement setup

The schematic measurement setup used to measure the SC-II of an IGBT is shown in Fig. 2(a). The protection IGBT (PIGBT) and the device under test (DUT) are connected in series close to the DC-link capacitors to reduce the parasitic inductance (L_{par}) of the SC path. A parasitic inductance of the entire SC loop is 30 nH. The PIGBT was used to limit the failure current in the event of DUT failure to the level of its own SC current of the PIGBT. Two gate drive units (GDU) were used to control the gate voltages of the DUT and the PIGBT.



(a) (b)

Fig. 2: (a) Schematic diagram of a SC-II measurement setup without V_{GE} clamping, and (b) measured SC-II pulse without V_{GE} clamping and without L_{CE} influence at given conditions T_{start} = 300 K, L_{par} = 30 nH, L_{load} = 82 µH, R_G = 10 Ω, t_{SC} = 5 µs, $V_{DC\text{-}link}$ = 700 V, V_{GE} = 15 V.

The measurements were carried out without gate-emitter voltage (V_{GE}) clamping. If the gate driver unit (GDU) is connected across the gate and sense emitter of the IGBT as displayed in Fig. 2(a), then measurements were performed without common-emitter inductance (L_{CE}) influence. On the other hand, if the GDU is connected across the gate and load emitter of the IGBT, then the measurements are influenced by L_{CE}. The measured SC-II pulses without V_{GE} clamping and without L_{CE} influence are displayed in Fig. 2(b). Due to the missing V_{GE} clamping, a high current peak is reached in the range of 6 times the nominal SC current, at V_{GE} = 15 V. This is due to the feedback effect across the Miller capacitance (C_{GC}) during voltage desaturation and the removal of remaining plasma from the prior on-phase.

SC-II measurements without V_{GE} clamping and without L_{CE} influence

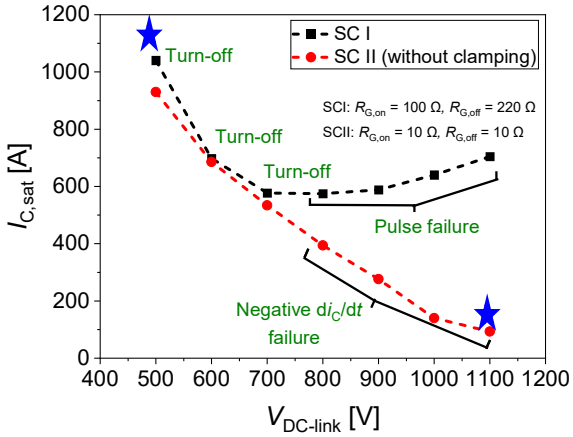
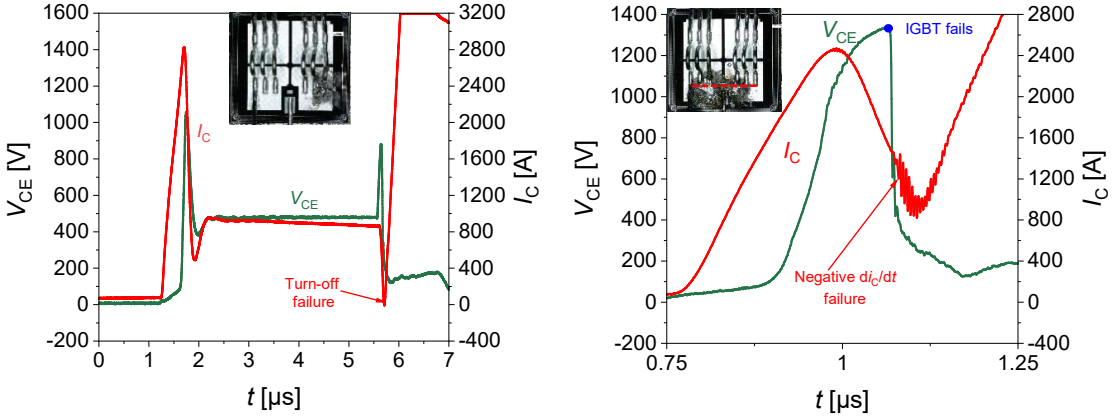


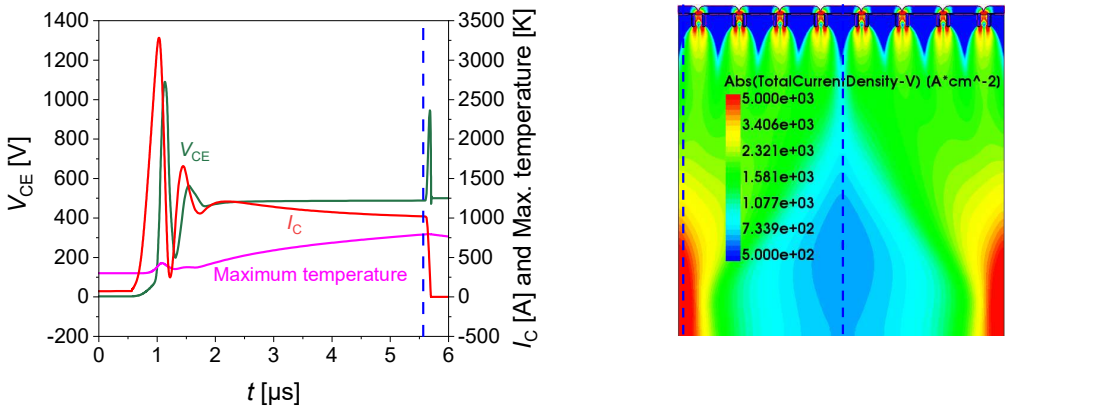
Fig. 3: Measured destruction limit for SC-I and SC-II in the I_C-$V_{DC\text{-}link}$ phase space for 1.7kV single chip at given conditions T_{start} = 300 K, L_{par} = 30 nH, L_{load} = 82 µH, t_{SC} = 5 µs.

To investigate the SC-II ruggedness of the 1700 V IGBT chip at a given DC-link voltage, the gate-emitter voltage was increased in increments of 0.2 V in a very low inductive setup with L_{par} = 30 nH. The measured SC-II destruction limits without V_{GE} clamping are compared with the SC-I destruction boundary (Fig. 3). For the SC- II measurements without V_{GE} clamping and without L_{CE}, the SC-II critical current level $I_{C,sat}$ continuously decreases with increasing DC-link voltage. For DC-link voltages from 500 V to 700 V, the destruction boundary line is approximately the same for both SC-I and SC-II measurements. Furthermore, the failure mode (turn-off failure) is the same for all conditions up to 700 V. The turn-off failure at 500 V is shown in Fig. 4(a). However, SC-II measurements without V_{GE} clamping show a further decrease of critical $I_{C,sat}$ for DC-link voltages above 800 V compared to SC-I. In this voltage range, negative $\mathrm{d}i_C/\mathrm{d}t$ failures were observed after reaching $I_{C,peak}$ [Fig. 4(b)]. The negative $\mathrm{d}i_C/\mathrm{d}t$ failure occurs after the SC-II turn-on collector current peak, when the collector-emitter voltage reaches a maximum peak value. Contrary to the SC-II behavior without clamping, the SC-I measurements show pulse failures above 800 V DC-link voltage. To study the internal mechanisms for the different failure types, SC-II simulations were performed at DC-link voltages of 500 V and 1100 V, as marked with blue stars in Fig. 3.



(a) Turn-off failure at 500 V (b) negative $\mathrm{d}i_C/\mathrm{d}t$ failure at 900 V

Fig. 4: Measured SC-II failure types at given conditions T_{start} = 300 K, L_{par} = 30 nH, L_{load} = 82 µH, R_G = 10 Ω, t_{SC} = 5 µs. Inset: destruction picture of the chip.



(a) (b)

Fig. 5: (a) Simulated SC-II at V_{CE} = 500 V with conditions: T_{start} = 300 K, L_{par} = 30 nH, L_{load} = 82 µH, R_G = 10 Ω, t_{SC} = 5 µs (b) current-density distribution at the beginning of the SC-II turn-off for a 1700 V IGBT.

Fig. 5(a) shows the transients of the current, voltage and maximum temperature at $V_{DC-link}$ = 500 V, $I_{C,sat}$ = 1135 A. Fig. 5(b) shows the distribution of the absolute total current density in the IGBT shortly before the SC-II turn-off. The current flow in the IGBT becomes inhomogeneous. The maximum temperature in the current filaments in the IGBT reaches a value of 795 K. For the simulated structure width, there are two half current filaments at the edges of the IGBT. The edge-to-edge lateral distance between the current filaments is 160 µm. The formation of current filaments depends on the width of the structure, with more current filaments expected in wider structures, as explained in [13].

Fig. 6 shows the vertical cross-section of the absolute value of the electric-field strength, electron density and hole density in the IGBT structure at the time 5.6 µs for the given SC-II conditions. The positions of the vertical cross-sections are marked inside and outside the current filament in Fig. 5(b). The electric-field peak shifts from the emitter side to the collector side [7]. As the current constricts in the current filament, the electron and hole densities are 1.5 orders of magnitude higher in comparison to the outside filament cut. The simulation shows a correlation between the lateral distance between the filaments and the width of the quasi-plasma region. The width of the high-field region defines the diameter of the current filament [13, 14], see Fig. 5(b).

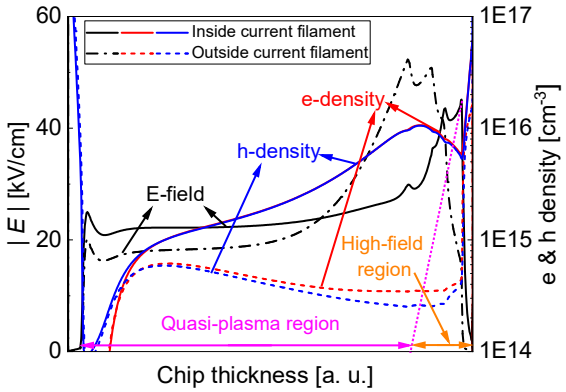
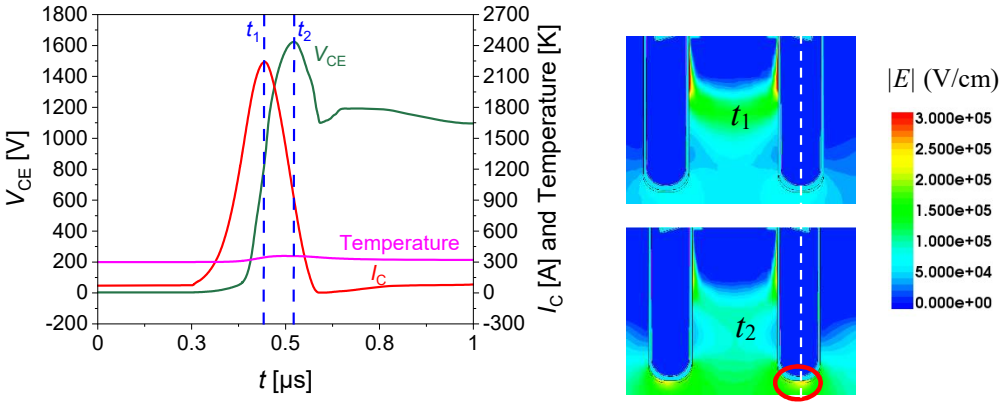
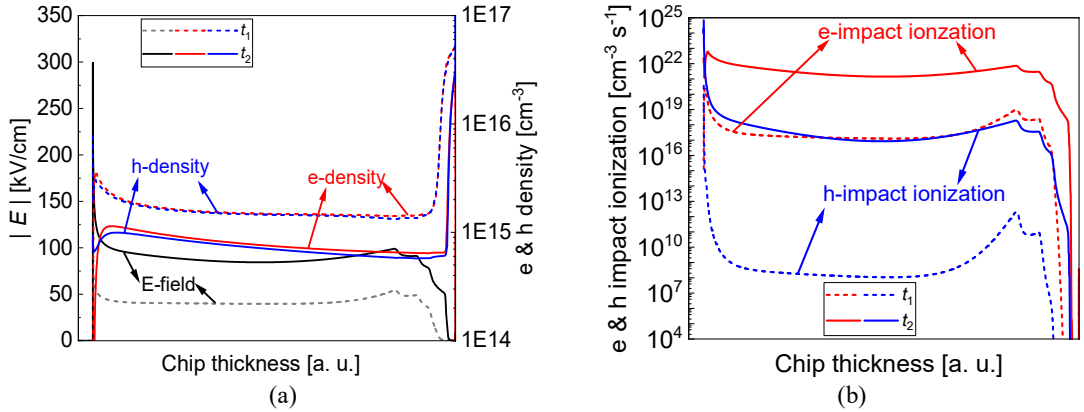


Fig. 6: Absolute value of the electric-field strength, electron and hole density distribution in the IGBT during SC-II simulation at $V_{DC\text{-}link}$ = 500 V, $I_{C,sat}$ = 1135 A, T_{start} = 300 K at 5.6 µs; vertical cuts are marked in Fig. 5(b).



(a) (b)

Fig. 7: (a) Simulated SC-II pulse at $V_{DC\text{-}link}$ = 1100 V, $I_{C,peak}$ = 2235 A, T_{start} = 300 K, L_{par} = 30 nH, L_{load} = 82 µH, R_G = 10 Ω, t_{SC} = 5 µs. (b) Absolute electric-field strength at time t_1 ($I_{C,peak}$) and t_2 ($V_{CE,peak}$).



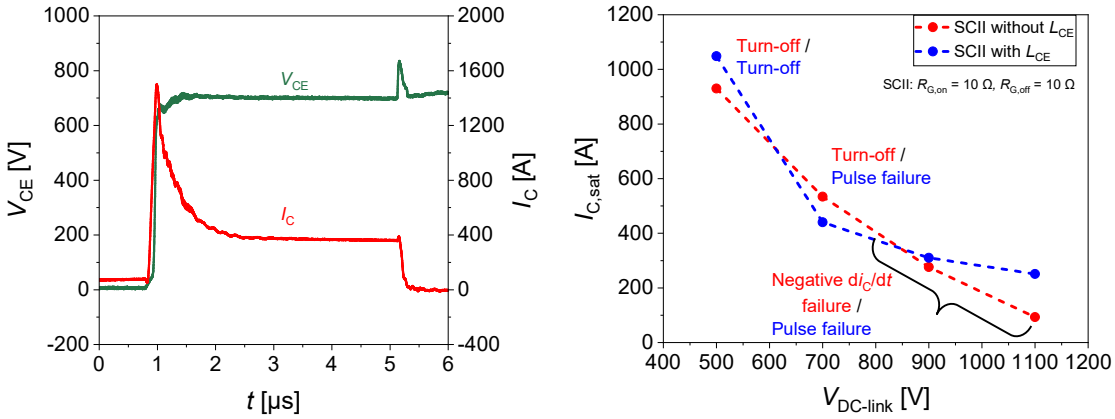
(a) (b)

Fig. 8: Absolute value of the electric-field strength, electron and hole density distribution in IGBTs obtained by an SC-II simulation at $V_{DC\text{-}link}$ = 1100 V, T_{start} = 300 K at time point t_1 and t_2, (b) Electron and hole impact ionization rates at time point t_1 and t_2; vertical cuts are marked in Fig. 7(b).

The simulated SC-II transients for $V_{DC\text{-}link}$ = 1100 V, $I_{C,peak}$ = 2235 A, are shown in Fig. 7(a). At time t_1 during the $I_{C,peak}$, the maximum electric field can be found in the channel region, with a value of about 0.3 MV/cm. The vertical distributions of the absolute value of the electric-field strength, electron density and hole density in the IGBT structure at the time t_1 and t_2 for the given SC-II conditions are shown in Fig. 8(a) and the corresponding impact ionization rates of electrons and holes are plotted in Fig 8(b). The positions of the vertical cross-sections through the gate trench are marked in Fig. 7(b). During the time t_1, the IGBT undergoes only a very weak dynamic avalanche.

At time t_2 with $V_{CE} = V_{CE,peak}$, the plasma is reduced, and the electric field expands further into the drift region. The charge carrier concentration in the space-charge region decreases accordingly, as shown in Fig. 8(a). Strong dynamic avalanche occurs, and the maximum electric field now moves below the gate trench, showing a value of approximately 0.3 MV/cm. This exceeds the critical electric field value for impact ionization [Fig. 8(b)] as a consequence of the higher current and voltage stress, resulting eventually in s failure during the negative $\mathrm{d}i_C/\mathrm{d}t$ phase. Furthermore, the appearance of emitter-side filaments is expected during the negative $\mathrm{d}i_C/\mathrm{d}t$ phase, as explained in [16].

SC-II measurements without V_{GE} clamping and with L_{CE} influence



(a) $V_{DC\text{-}link}$ = 700 V, V_{GE} = 15 V (b)

Fig. 9: (a) Measured SC-II pulse without V_{GE} clamping and with L_{CE} influence and (b) comparison of the SC-II capability as a function of V_{CE} with and without L_{CE} at the following measurement conditions: T_{start} = 300 K, L_{par} = 30 nH, L_{load} = 82 µH, R_G = 10 Ω, t_{SC} = 5 µs.

Typical SC-II transients measured with L_{CE} influence and without V_{GE} clamping are shown in Fig. 9(a). During SC-II turn-on, the $V_{CE,peak}$ and $I_{C,peak}$ are significantly reduced by utilizing the negative feedback of the common-emitter inductance. The peak current is just 4 times the SC current at V_{GE} = 15 V (compare with Fig. 2b). The last-pass SC-II $I_{C,sat}$ values, with and without L_{CE}, are plotted as a function of $V_{DC\text{-}link}$ in Fig. 9(b). Even though the current peaks and voltage peaks are notably lower with L_{CE} influence, there is only a slightly increased SC-II ruggedness for DC-link voltages 900 V and 1100 V with L_{CE} influence. Further, the failure type for 900 V and 1100 V has changed from negative $\mathrm{d}i_C/\mathrm{d}t$ failure to pulse failure. At V_{CE} = 700 V, SC-II capability is reduced slightly for L_{CE}, and the failure type has changed from a turn-off failure to a pulse failure for L_{CE}.

Overall, under the SC II conditions without V_{GE} clamping and with common-emitter inductance influence, there is no significant improvement regarding the SC-II SOA. Therefore, in the next step, we consider an approach for reducing the current and gate-voltage peak by means of a suitable clamping circuit.

SC-II SOA of the IGBT with V_{GE} clamping

Clamping circuit in the gate driver unit

The clamping circuit provides a solution by utilizing the negative feedback generated from the load emitter inductance, which is the result of the high $\mathrm{d}i_C/\mathrm{d}t$ of the short-circuit current. The clamping circuit used in this work was adapted from [17]. The clamping circuit connected between the gate and load emitter is shown in Fig. 10(a). The circuit consists of two fast Schottky diodes (D_1 and D_2) placed in opposite directions. A clamping capacitor

(C_{Clamp}) and a discharge resistor (R_2) in parallel are connected between the two Schottky diodes. Once the driver is powered, the clamping capacitor is charged to a voltage V_{Clamp}, that is approximately equal to the applied gate-emitter voltage. In normal operation, V_{Clamp} does not influence the output voltage V_{GE} due to the Schottky diode D_1.

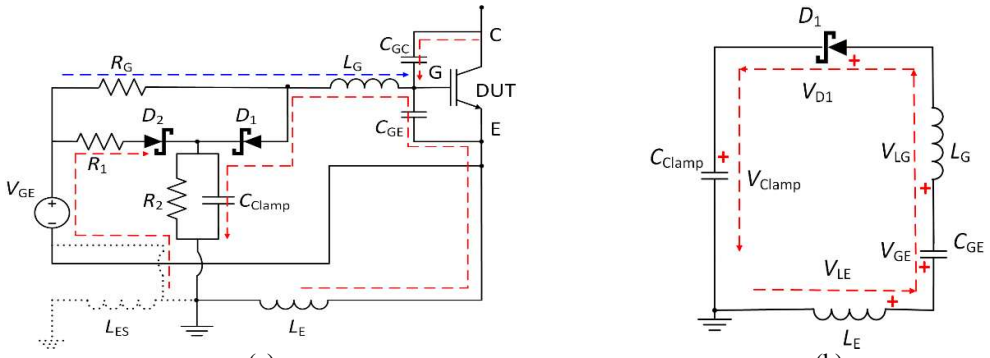


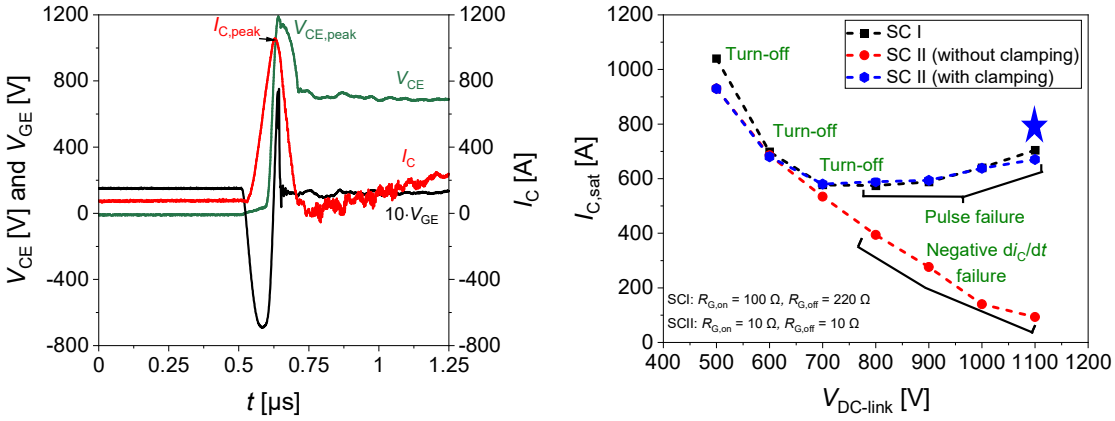
Fig. 10: (a) Schematic diagram of a clamping circuit used in the GDU for SC-II measurements and (b) schematic diagram of a gate-emitter loop during the onset of a short-circuit II event.

The voltage drop across all the components in the gate-emitter loop during the SC-II event is displayed in Fig. 10(b). The voltage drop V_{LE} across the load emitter inductance L_E acts as negative feedback on the gate voltage, and is responsible for the clamping effect. The resistance R_1 limits the current from the output of the voltage regulator. The D_1 diode blocks any current, which is caused by the emitter stray inductance L_{ES} (for packaged modules), from flowing back to the gate driver unit (GDU). Due to the induced voltage, current passes through the D_1 into the clamping capacitor (C_{Clamp}). The D_2 diode blocks any from current flowing back into the voltage regulator [17].

$$V_{GE} = V_{Clamp} + V_{LG} + V_{D1} - V_{LE} \tag{1}$$

The relationship between V_{GE} and the voltage drops across the components in the gate-emitter loop, including the clamping components, as seen in Fig. 10(b), is described in Eq. 1. The voltage across the clamping capacitor V_{Clamp} is constant, and is very small across the Schottky diode V_{D1}, since it is in the conducting state. Hence, the voltage drop across the load-emitter inductance (V_{LE}) pulls the gate-emitter voltage V_{GE} down, resulting in a clamping effect. The voltage drop across the V_{LE} is a function of the value of L_E and di_C/dt [17].

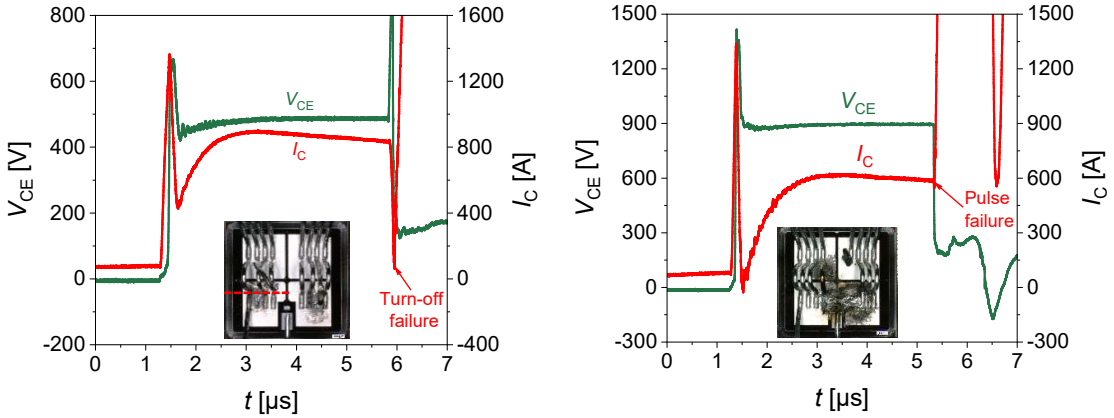
SC-II measurements with V_{GE} clamping



(a) With clamping at V_{GE} = 15 V and V_{CE} = 700 V (b) Measured destruction limit

Fig. 11: (a) A typical SC-II measurement with clamping and (b) measured destruction limit in I_C-$V_{DC-link}$ phase space for SC-II measurements with and without V_{GE} clamping for a 1.7 kV single chip IGBT under the following test conditions: T_{start} = 300 K, L_{par} = 30 nH, L_{load} = 82 µH, R_G = 10 Ω, t_{SC} = 5 µs.

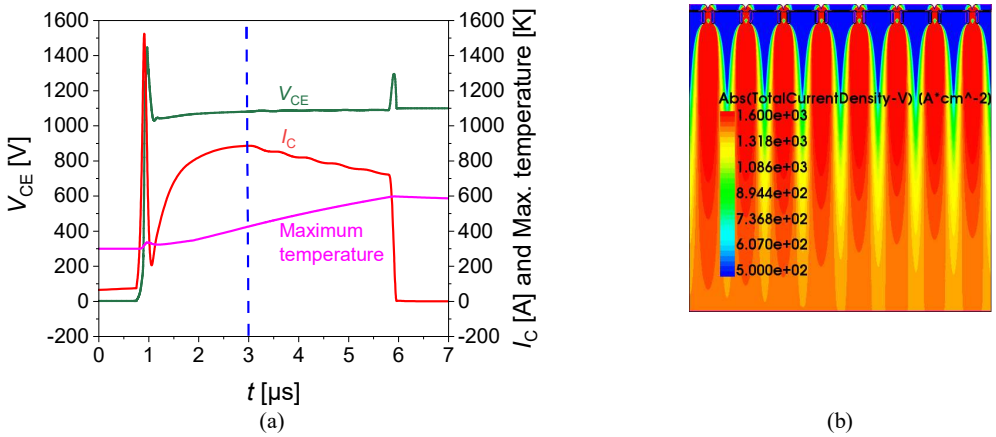
In Fig. 11(a), a typical SC-II measurement with V_{GE} clamping is plotted for V_{GE} = 15 V and V_{CE} = 700 V. The SC- II measurement with V_{GE} clamping [Fig. 11(a)] shows a significantly reduced collector-current peak ($I_{C,peak}$) during turn-on, with a magnitude of ~2.7 times lower compared to the SC-II measurements without V_{GE} clamping [Fig. 2(b)] under the same test conditions. The clamping is not perfect, as some parasitics are still present between the clamping capacitor and the chip gate (usually internal gate resistor, gate inductance). The $V_{CE,peak}$ is higher with V_{GE} clamping due to the steeper negative di_C/dt but still acceptable. Additionally, the SC-II measurement with V_{GE} clamping shows a self-turn-off of the IGBT after the negative di_C/dt [18]. It should be noted that the plotted V_{GE} is the measured signal of the outer gate terminal, and does not correspond to the internal gate-emitter voltage. Therefore, the current peak value $I_{C,peak}$ is the better characteristic value to assess the effectiveness of the clamping circuit.



(a) SC-II turn-off failure at 500 V (b) SC-II pulse failure at 900 V

Fig. 12: Measured SC-II failure types with V_{GE} clamping at given conditions T_{start} = 300 K, L_{par} = 30 nH, L_{load} = 82 µH, R_G = 10 Ω, t_{SC} = 5 µs. Inset: microscopic image of the destroyed chip.

The SC-II SOA measurements with and without V_{GE} clamping are compared in Fig. 11(b). There is a significant improvement in the SC-II ruggedness of the IGBT when the clamping circuit is used at the GDU, especially at DC-link voltages exceeding 700 V. The destructive boundary line for the SC-II with V_{GE} clamping is almost identical to that of SC-I SOA. The minima can be seen at a V_{CE} of 700 V with a corresponding last-pass saturation current of 589 A for the 1700 V IGBT used. For a DC-link voltage range from 500 V to 700 V, the IGBT fails during the SC-II turn-off. However, instead of a negative di_C/dt failure, a pulse failure is observed for a V_{CE} range of 800 V to 1100 V with V_{GE} clamping in SC-II measurements. The two insets in Fig. 12(a) and (b) show the corresponding chip microscopic images after the SC-II failure.



(a) (b)

Fig. 13: (a) Simulated SC-II at V_{CE} = 1100 V with simulated conditions: T_{start} = 300 K, L_{par} = 30 nH, L_{load} = 82 µH, R_G = 10 Ω, t_{SC} = 5 µs (b) current density distribution at 3 µs for a 1700 V IGBT.

For DC-link voltages from 500 V to 700 V, the IGBT fails during the SC-II turn-off due to the formation of destructive current filaments. At a V_{CE} range from 900 V to 1100 V, the clamped SC-II measurements show pulse failures in contrast to a failure during the negative di_C/dt in SC-II without V_{GE} clamping. The pulse failures above

DC-link voltages of 800 V [Fig. 11(b)] are consistent with the failure signature of the SC-I tests. The change in failure type can be due to the reduced magnitude of the collector current peak and the self-turn-off in the IGBT. Additionally, the duration of very high V_{CE} across the IGBT shortly after the $I_{C,peak}$ is reduced to 140 ns for clamped V_{GE} measurements compared to the 500 ns for the SC-II measurements without V_{GE} clamping (see Fig. 2b).

To gain a better understanding of the observed pulse failure, an SC II simulation with V_{GE} clamping was performed at a $V_{DC-\,link}$ = 1100 V, $I_{C,sat}$ = 800 A; the position is marked with the blue star in Fig. 11(b). The simulated V_{CE}, I_C and maximum temperature transients are shown in Fig. 13(a). Fig. 13(b) shows the absolute total current density in the IGBT during the SC-II pulse at 3 µs. As the space-charge region at higher V_{CE} voltages expands further towards the collector-side, the current distribution becomes more uniform in the IGBT compared to the conditions with lower DC-link voltages. Hence, a higher current is necessary to generate a plasma in the drift region. Consequently, the short-circuit ruggedness increases above 800 V as shown in Fig. 11(b) [7]. For the SC II simulated condition at $I_{C,sat}$ = 800 A, which is above the measured destructive boundary, $I_{C,sat}$ shows only a slight inhomogeneous current flow at the anode side in the IGBT, as shown in Fig. 13(b).

Failure analysis

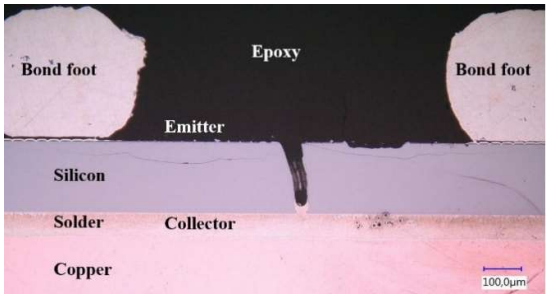


Fig. 14: IGBT cross-section during destructive SC-II turn-off event at V_{CE} = 500 V, T_{start} = 300 K, L_{par} = 30 nH, L_{load} = 82 µH, R_G = 10 Ω, t_{SC} = 5 µs [cut position: as shown in inset Fig. 12(a)].

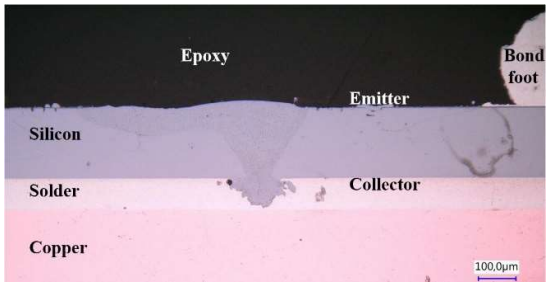


Fig. 15: IGBT cross-section during destructive SC-II negative di_C/dt events at V_{CE} = 900 V, T_{start} = 300 K, L_{par} = 30 nH, L_{load} = 82 µH, R_G = 10 Ω, t_{SC} = 5 µs [cut position: as shown in inset Fig. 4(b)].

In order to analyze the failures due to turn-off and negative di_C/dt, two of the damaged IGBT devices were cut at the precise position where they were destroyed. Fig. 14 and Fig. 15 show the cross-section of the devices after a single destructive SC-II pulse at 500 V and 900 V, respectively. The cross-section in Fig. 14 corresponds to the destroyed chip and plot shown in Fig. 12(a). The IGBT was cut at the position marked by red dashed-line. Similarly, the IGBT cross-section illustrated in Fig. 15, cut at the position where the destructive SC-II negative di_C/dt event occurred corresponds to the destroyed chip and plot shown in Fig. 4(b). The figures displayed in Fig. 14 and Fig. 15 correspond to the filamentation process failures at the collector side and at the emitter side respectively. Also, the destruction on the chip depends on how fast the protection IGBT (PIGBT) reacts after the device under test fails during short-circuit.

Conclusion

The measured SC-II SOA with and without V_{GE} clamping was compared to that of the SC-I SOA. For the SC-II measurements without V_{GE} clamping, the critical saturation collector current decreases continuously with increased

DC-link voltage. For a V_{CE} ranging from 500 V to 700 V, the destruction of the IGBT occurs during the SC turn-off, which is the same as for SC-I. Here, the formation of collector-side current filaments triggers the failures. For DC-link voltages above 700 V, the IGBTs fail during the negative di_C/dt phase. In these cases, the IGBTs undergo strong dynamic avalanche due to the high $V_{CE,peak}$ and $I_{C,peak}$ values occurring during SC-II. Furthermore, it could be shown that the SC-II SOA could be significantly improved by using V_{GE} clamping. As a result of V_{GE} clamping, the SC-II SOA is approximately same as the SC-I SOA.

References

1] J. Lutz, H. Schlangenotto, U. Scheuermann, and R. De Doncker, "Semiconductor Power Devices: Physics, Characteristics, Semiconductor Power Devices: Physics, Characteristics, Reliability," 2nd ed. Berlin, Germany: Springer-Verlag, 2018.

[2] H.-G. Eckel, L. Sack, "Experimental Investigation on the Behaviour of IGBT at Short-Circuit during the On-State," 20th International Conference on Industrial Electronics, Control and Instrumentation, IECON, pp. 118-123, 1994.

[3] J. Lutz, T. Basler, "Short-Circuit Ruggedness of the High-Voltage IGBTs" in Proc. 28th International Conference on Microelectronics (MIEL), pp. 243-250, May, 2012.

[4] R. Letor, C.G. Aniceto, "Short circuit behaviour of IGBTs correlated to the intrinsic device structure and on the application circuit," IEEE Industry Applications Society Annual Meeting, 1992.

[5] D. Hammes, et al. "High-inductive short-circuit Type IV in multi-level converter protection schemes," 42nd Annual Conference of the IEEE Industrial Electronics Society, IECON 2016.

[6] J. Fuhrmann, S. Klauke, H.G. Eckel, "Passive IGBT turn-off during short-circuit type V" in Proc. Conf. International Exhibition and Conference for Power Electronics Intelligent Motion, Power Quality, Nuremberg, 2016.

[7] A. Kopta, M. Rahimo, U. Schlapbach, et al., "Limitation of the Short-Circuit Ruggedness of High Voltage IGBTs," in Proc. ISPSD, 2008, pp. 33-36.

[8] R. Baburske, V. Treek, F. Pfirsch, F. J. Niedernostheide, et al., "Comparison of Critical Current Filaments in IGBT Short Circuit and during Diode Turn-off," in Proc. ISPSD, 2014, pp. 47-50.

[9] M. Tanaka, A. Nakagawa, "Simulation studies for Avalanche induced short-circuit current crowding of MOSFET-Mode IGBT," in Proc. ISPSD, 2015, pp. 121-124.

[10] R. Bhojani, J. Kowalsky, J. Lutz, et al., "Observation of Current Filaments in IGBTs with Thermo-Reflectance Microscopy," in Proc. ISPSD, May 2018, pp. 164-167.

[11] R. Baburske, F. J. Niedernostheide, H.-J. Schulze, et al., "Unified view on energy and electrical failure of the short-circuit operation of IGBTs," Microelectronics Reliability, 2018, Vol. 88-90, pp. 236-241.

[12] M. L. Mysore, R. Bhojani, J. Kowalsky, et al., "Al Modification as Indicator of Current Filaments in IGBTs under repetitive SC operation," Transactions on IET power electronics, ISSN 1755-4535, pp. 1-10, 2019.

[13] R. Bhojani, M. L. Mysore, R. Raihan et al, "Current Filament Behavior in Different Voltage Class IGBTs using Measurements and Simulations," in Proc. ISPSD, Sep. 2020, pp. 446-449.

[14] M. L. Mysore, T. Basler, J. Lutz et al., "Aluminum Modification as Indicator for Current Filaments under Repetitive Short-Circuit in 650V IGBTs," in Proc. of 15th ISPS, pp. 21-29, 2021.

[15] SYNOPSYS, *Sentaurus Device User Guide*, 2020.

[16] T. Basler, "Ruggedness of high-voltage IGBTs and protection solutions," PhD thesis, Technische Universität Chemnitz, 2014, page 94.

[17] X. Liu, J. Kowalsky, C. Herrmann, et al., "Influence of the gate driver and common-source inductance on the SC behavior of IGBT modules," IEEE transactions on power electronics, vol. 35, no. 10, October 2020.

[18] T. Basler, J. Lutz, T. Brückner, et al., "IGBT Self-Turn-Off Under Short-Circuit Condition," in Proc. Int. Conf. 10th International Seminar on Power Semiconductors (ISPS), Prague, 2010.