Characterization of Si-IGBT Crosstalk with a Concentration on Power Circuit Parasitic Elements and the Device Operation Point

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Keywords

«IGBT», «Parasitic elements», «Thermal stress», «Short circuit».

Abstract

Crosstalk is a serious issue in power electronics converters having a phase-leg in their structure. The crosstalk destructive effect can lead to failure of the device. Hence, several models are presented in the literature to analyze the crosstalk and prevent the undesired failures. However, these models need to be enhanced so as to be characterized in different aspects. In this paper, a new comprehensive model based on the last models in state-of-art has been presented. This model includes the parasitic elements of the power circuit and parasitic capacitances of Si-IGBT. Thus, the effect of variable elements can be investigated. In this paper, the effect of the high-side switch specifications such as off-sate voltage, conducting current, and turning-on time on the crosstalk has been figured out. It is found that the most critical condition in terms of the crosstalk is when the converter operates on the high voltage levels of DC-bus and light-load conditions. Moreover, the different values of parasitic inductance are considered in the model, and their effect on the crosstalk is evaluated. Furthermore, the experimental setup has been introduced in order to check the model accuracy. In order to study the effect of Si-IGBT parasitic capacitances, the ratio of C_{GC}/C_{GE} has been changed, and results have been presented. The case study device for the investigation of the crosstalk and experimental tests is IXGH60N60.

Introduction

Applications of high voltage/power insulated gate bipolar transistors (IGBTs) are very widespread in power converters. They are widely employed in traction systems [1], high-voltage DC/DC converters [2], pulsed power supplies [3], HVDC circuit breakers [4]-[5]-[6], and solid-state transformers [7]-[8]. The reliability of the power converters is very important since they play an important role in the industry. Prior studies indicate that 34 % of failures in power converters are related to IGBTs [9]. However, the power IGBTs are more rugged than their other counterparts in severe conditions such as short circuit faults [10], but there are many reliability issues threatening IGBTs during the operation. Hence, as an important topic, enhancing IGBTs' reliability and comprehension of the root of the failure in normal and harsh conditions have been the target of recent research.

When the IGBTs are used in a phase-leg structure, the shoot-through currents due to short-circuiting the DC-link can be fatal for the IGBTs. The phase-leg exists in many power converter topologies such as single/multi-phase inverters and DC/DC resonant converters. It should be carefully considered that even using intentional dead-time between the operation of IGBTs in the phase-leg, the risk of shoot-through currents is high. The origin of these shoot-through currents is crosstalk or parasitic turn-on. In crosstalk, the turning on of the upper device parasitically turns on the lower side device as depicted in Fig. 1. Consequently, for a while, both devices are conducting and the shoot-through current flows among the phase-leg. Crosstalk occurs due to the voltage change of the Miller capacitance of the low-side device in transition of the high-side device from the off-state to the on-state and vice-versa. Accordingly, when the high-side device changes state from the off to on, a positive voltage jump occurs

for the low-side device gate-emitter voltage as shown in Fig. 1. When the peak value of the gate-emitter voltage ($V_{GE1\text{-}P}$ in Fig. 1) exceeds the device gate threshold voltage (V_{TH}), it can operate in the active region, and saturated current can flow through the IGBTs in the phase-leg structure. The extra power loss due to crosstalk can increase the device's junction temperature. In some conditions, the value of the short circuit current can be several times the device's nominal current. This condition can potentially lead to device failure.

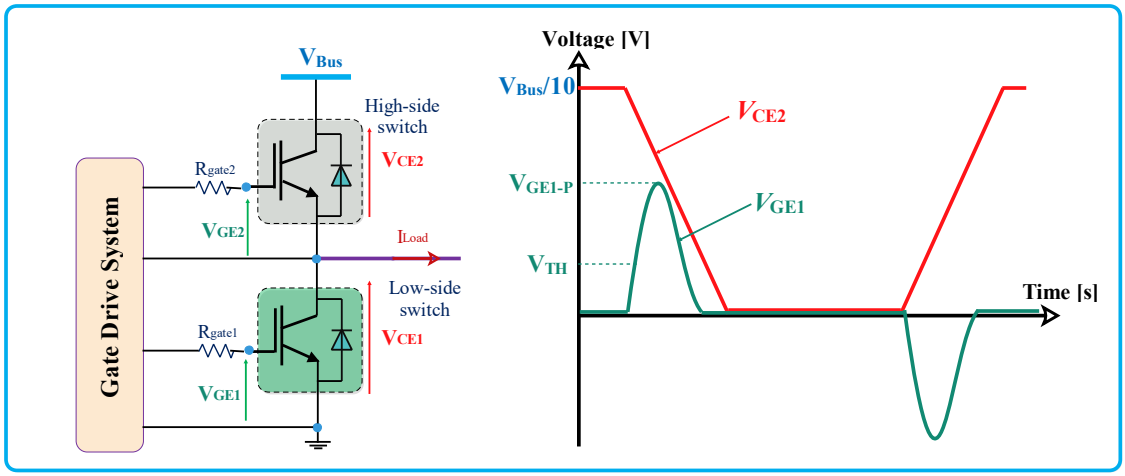


Fig. 1. The schematic of a phase leg and occurrence of a parasitic turn-on for the low-side switch.

To cease crosstalk and parasitic turn-on, several solutions have been reported in the prior research. Applying a negative bias in the off-state at gate-emitter terminals of the devices is proposed in [11] to alleviate the gate-emitter peak voltage in crosstalk. This method is promising but the cost added to the system for an isolated DC power supply is not acceptable in many applications. Moreover, this method cannot be served in boot-strap gate drive systems. In addition, negative bias solely cannot be effective in avoiding parasitic turn-on in many cases. Gate impedance regulation (GIR) is investigated in [12], [13], and [14]. These papers aim is to optimize the gate impedance to minimize the effect of Miller capacitance on the gate side in the crosstalk. These solutions are practical but the improvement is limited to the cases with specific conditions. Several novel gate drive systems also are proposed in [15], [16], and [17]. The focus of the mentioned solutions is on the gate side. The effect of the power path on the crosstalk has not been deeply investigated yet. More importantly, the behavior of the crosstalk strictly depends on the converter power rating and power path elements. Thus, before devising a crosstalk suppression scheme, a predictive approach for the determination of $V_{GE1\text{-}P}$ in crosstalk seems to be mandatory.

This paper aims to characterize the crosstalk by considering power path parasitic elements and the converter operating point. It will be revealed that the power path elements have a dominant effect on the crosstalk. The results show a considerable dependency of the crosstalk of power path parasitic inductance. An optimum region for the power path parasitic inductance is obtained to minimize the effect of the crosstalk. This parasitic inductance depends on the PCB trace length and ESL of the DC-link capacitors. Hence, in the design phase, the practitioner has a practical guideline to design the power circuit for minimum crosstalk. In addition, the effects of the converter operating point as well as the high-side switch turning on speed on parasitic turn on are investigated. The theoretical discussions are validated using experiments. The case study device is IXGH60N60C a 600 V and 60 A discrete IGBT.

Characterization of the IGBT crosstalk

A. Existing approaches

There are several studies devoted efforts to characterizing the crosstalk using equivalent circuits. [18] provides (1) as a simple crosstalk model

$$V_{GE1} = R_G C_{GC} \frac{dV_{CE}}{dt}\left(1 - e^{\frac{-t}{R_G(C_{GC}+C_{GE})}}\right) \quad (1)$$

where R_G is the gate equivalent resistance, C_{GC} and C_{GE} are the junction capacitances of the device between gate-collector and gate-emitter terminals. Expression (1) also demonstrates the effect of the switch transient speed (dV/dt) and gate resistance (R_G) in order to investigate the crosstalk and the gate emitter voltage of the low-side switch (V_{GE1}). In addition, the parasitic capacitances of IGBT are considered. However, this model simplifies the power circuit and cannot study its effect.

The second model which can be considered as the most comprehensive one in the literature is discussed in [19] and is presented in Fig. 2. This model includes the power parasitic components. The shortcomings of this model are: 1- It does not consider the transient speed of the high-side device in the turning-on process. 2-It does not consider the mutual inductances between the gate circuit and power circuit.

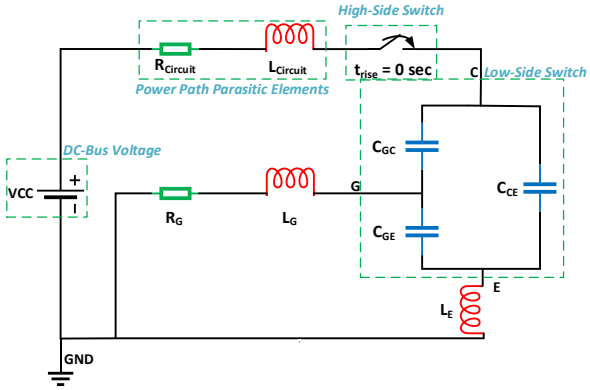


Fig. 2. The crosstalk model proposed in [19]

B. Proposed Model

Keeping in mind the shortcomings of the present crosstalk models, this paper tries to modify the model of [19]. These modifications are:

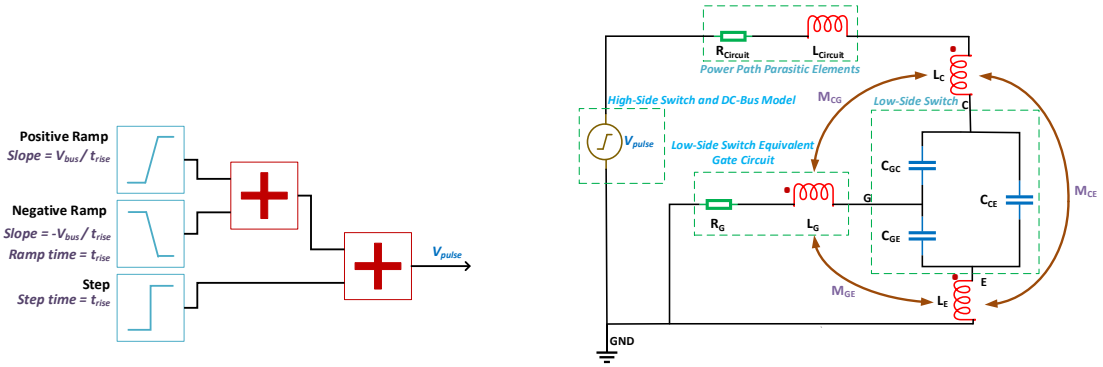
a) Considering the high-side switch turning-on transient time. Since this time depends on the device current and voltage, the analysis of the device operating point and its effect on the crosstalk can be carried out using the proposed model. In addition, the effect of the high-side switch gate drive system on the crosstalk can be well-studied.

b) The proposed model considers the mutual inductances of the power circuit and gate side circuit. Hence, the parasitic elements effect on the crosstalk can be studied more accurately.

The process of consideration of high-side device turning-on time is presented in Fig. 3-(a) and the proposed model schematic is presented in Fig. 3-(b). According to Fig. 3-(a), the time-domain equation of $V_{pulse}(t)$ can be written as

$$V_{pulse}(t) = \frac{V_{bus}}{t_{rise}} t\big(u(t) - u(t - t_{rise})\big) + V_{bus} u(t - t_{rise}) \quad (2)$$

Where V_{bus} is the DC-link voltage of the phase-leg, t_{rise} is the turning-on time of the high-side switch, and $u(t)$ is the Heaviside step function.



(a) (b)

Fig. 3. The process of applying high-side device speed (a), and the full schematic of the proposed model (b).

In addition, considering Fig. 3-(b), the Laplace forms of the model equations can be written as

$$\frac{V_G}{R_G + sL_{GG}} + (V_G - V_E)sC_{GE} + (V_G - V_C)sC_{GC} = 0 \tag{3}$$

$$(V_E - V_G)sC_{GE} + \frac{V_E}{sL_{EE}} + (V_E - V_C)sC_{CE} = 0 \tag{4}$$

$$(V_C - V_G)sC_{GC} + (V_C - V_E)sC_{CE} + \frac{V_C - V_{pulse}}{R_{Circuit} + sL_{Circuit} + L_{CC}} = 0 \tag{5}$$

where V_C, V_G, and V_E are the collector, gate and emitter voltages of the device. In addition, regarding the investigations of [20], the mutual inductances of the model can be considered as

$$\begin{aligned} L_{GG} &= L_G + M_{CG} + M_{GE} - M_{CE} \\ L_{CC} &= L_C + M_{GC} + M_{CE} - M_{GE} \\ L_{EE} &= L_E + M_{CE} + M_{GE} - M_{GC} \end{aligned} \tag{6}$$

Regarding expressions (3) to (6), the equation of low-side switch in Laplace form can be expressed as

$$V_{GE1} = \frac{C_{GC}V_{Bus}e^{-s\times t_{rise}} \times (e^{s\times t_{rise}} - 1) \times (R_G + L_{GG}s)}{st_{rise} \times (D_4s^4 + D_3s^3 + D_2s^2 + D_1s + 1)} \tag{7}$$

The denominators of equation (7) are

$$\begin{aligned} D_4 &= (L_{Circuit} + L_{CC})\big((L_{EE} + L_{GG})(C_{CE}C_{GE} + C_{GC}C_{GE}) + C_{CE}C_{GC} \times L_{GG}\big) \\ &\quad + C_{GC}C_{GE} \times L_{EE}L_{GG} \\ D_3 &= C_{CE}C_{GE}(L_{EE}R_{Circuit} + L_{CC}R_G + L_{Circuit}R_G + L_{GG}R_{Circuit}) \\ &\quad + C_{CE}C_{GC}(L_{CC}R_G + L_{Circuit}R_G + L_{GG}R_{Circuit} + L_{EE}R_{Circuit}) \\ &\quad + C_{GC}C_{GE}(L_{CC}R_G + L_{Circuit}R_G + L_{EE}R_G + L_{GG}R_{Circuit}) \\ D_2 &= (L_{CC} + L_{Circuit})(C_{CE} + C_{GC}) + C_{GE}(L_{EE} + L_{GG}) + C_{GC}L_{GG} \\ D_1 &= R_{Circuit}(C_{CE} + C_{GC}) + R_G(C_{GC} + C_{GE}) \end{aligned} \tag{8}$$

According to (8), the time-domain of shoot-through current can be measured analytically, hence the effect of various elements can be investigated in the model.

C. Determination of the high-side switch turning-on time (t_{rise})

The turning-on time of the device depends on the device blocking voltage (V_{bus}) and conducting current (I_{Load}). According to investigations of [21] and [22], the turning-on time of the high-side switch can be written as

$$t_{rise} = C_{GC}R_G \frac{V_{bus}}{(V_{CC} - V_{GP})}; \tag{9}$$

, where V_{CC} is the applied on-state voltage of the gate driver, and V_{GP} is the Miller plateau voltage which can be expressed as

$$V_{GP} = V_{TH} + I_{Load}/gfs \tag{10}$$

, where V_{TH} is the gate threshold voltage. The parameter g_{fs} is the device transconductance and can be written as [23]

$$g_{fs} = \frac{\partial I_{CH}}{\partial V_{GE}} = \frac{1}{1-\alpha_{PNP}} \frac{\mu_{ns} C_{ox} Z}{L_{CH}} (V_{GE} - V_{TH}) \tag{11}$$

, where μ_{ns} is the average electron mobility in the channel, C_{ox} is oxide capacitance per unit area, Z is the channel width, L_{CH} is the channel length.

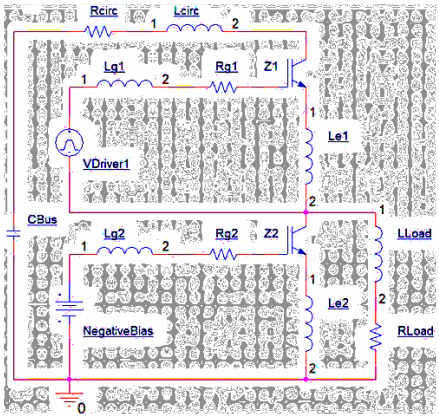
C_{GC} is a nonlinear capacitance and depends on the device voltage in the transient time interval. [24] and [14] provide algorithms for consideration of this nonlinear capacitor. In this paper, we used the same method and consider the average value for the nonlinear gate-collector capacitance for the calculation of t_{rise}. According to (9) -(11), the turning-on time of the high-side device depends on the device operating point. On the other hand, t_{rise} is an important parameter in the gate-emitter voltage on the low-side device in crosstalk. Thus, the device operation point is very important to be considered in analyzing the crosstalk in the design phase and is feasible by the proposed approach.

D. Accuracy check

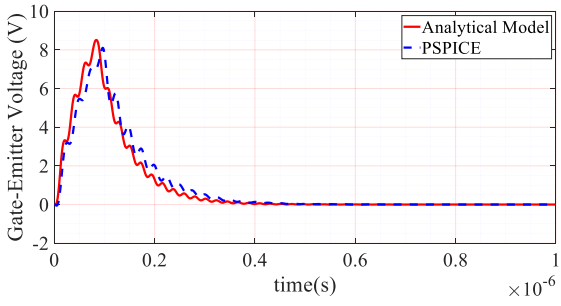
To check the accuracy of the proposed model, the output of the model is compared with a PSPICE simulation for a case study with the parameters of TABLE I.

TABLE I. MODEL PARAMETERS AND VALUES

C_{GC}	53.75 pF
C_{GE}	3614 pF
C_{CE}	204 pF
L_C	0.9 nH
L_G	3 nH
L_E	10 nH
M_{GC}	-5.71 nH
M_{GE}	-5.47 nH
M_{CE}	-10.3 nH
I_{Load}	20 A
$R_{Circuit}$	1 Ω
$L_{Circuit}$	50 nH
V_{bus}	400 V
Calculated t_{rise}	90 ns



(a)



(b)

Fig. 4. The simulation circuit (a), and output waveforms (b).

The circuit used for the simulation of the crosstalk is presented in Fig. 4-(a) and the resultant waveforms are presented in Fig. 4-(b). According to Fig. 4-(b), the accuracy of the proposed model is acceptable and it can be employed to characterize the crosstalk.

Effect of the high-side switch operating point on Crosstalk

A. The high-side switch current effect on Crosstalk

To figure out the effect of high-side device current on the peak voltage of the gate-emitter, a variety of loads should be applied to the output. Moreover, in practice, there is always an inductance in the output. Thus, in the simulation of the case study, the load should be an RL type. The value of load inductance is, however, so less than its resistance 100 nH. In this study, the load resistance is changed to vary the load current. The dependency of the crosstalk voltage from the device current is presented in Fig. 5-(a). Fig. 5-(a) indicates that by increasing the load current, the peak of gate-emitter voltage decreases. This can be explained by the fact that the increment in the device current slows down the high-side device according to (9) to (11). Hence, the crosstalk effects are more dominant when the converter works under low power mode.

B. The high-side switch off-state voltage effect on Crosstalk

So as to investigate the other aspects of crosstalk, the effect of high-side off-state voltage should be investigated. The off-state voltage of the case study is 400 V. Thus, by decreasing the off-state voltage its effect can be studied. Fig. 5-(b) indicates the consequence of the off-state voltage of the high-side device on crosstalk. By increasing the off-state voltage, the crosstalk effect is dominant. This behavior is in accordance with (2) while the V_{bus} directly determines the input of the model. Thus the negative bias is necessary in order to prevent crosstalk in such conditions.

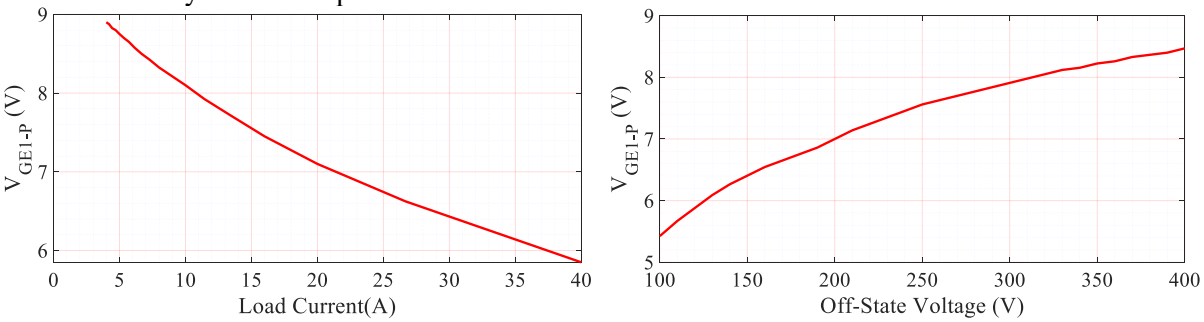


Fig. 5. The effect of the load current(a), and the effect of off-state voltage (b).

Effect of the power circuit parasitic inductance on crosstalk

In this paper, the concentration is on the parasitic elements of the power circuit. The PCB length and width are dominant factors for the circuit inductance. Fig. 6 presents the effect of the circuit inductance on the obtained crosstalk. There are some optimum regions where the obtained peak value of the V_{GE1} is less. On this basis, the PCB designer must take care of the length and width of the PCB track to minimize the effect of crosstalk. Moreover, in lower values of inductance, the maximum value of the curve is lower, and the distance between the DC-link and Si-IGBTs should be limited.

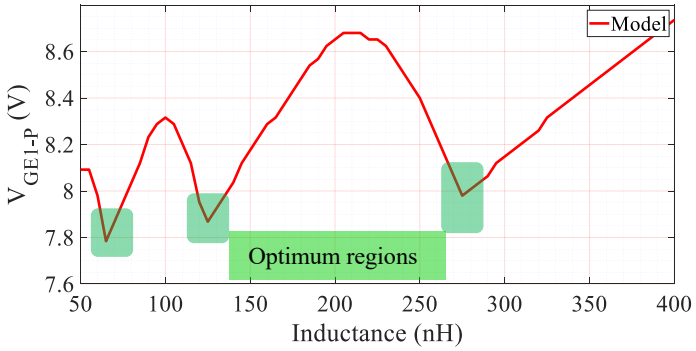


Fig. 6. The effect of the power circuit inductance on crosstalk.

Parasitic Capacitance Ratio C_{GC}/C_{GE} Effect

The values of the device parasitic capacitances are determined by the manufacturer and could be found in the device datasheet. Their values can affect the crosstalk, and hence, the change of C_{GC}/C_{GE} is studied. In the case study of this paper, the ratio is 0.014872. The value of this ratio is increased and decreased by 30%. Fig. 7 shows the effect of parasitic capacitances on crosstalk. By increasing this ratio, the gate-emitter voltage increases and may destroy the IGBT of the phase-leg. Moreover, the parasitic capacitance ratio does not have a tangible effect on the crosstalk time interval.

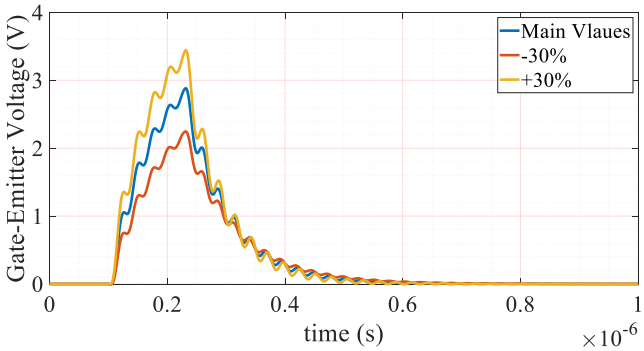
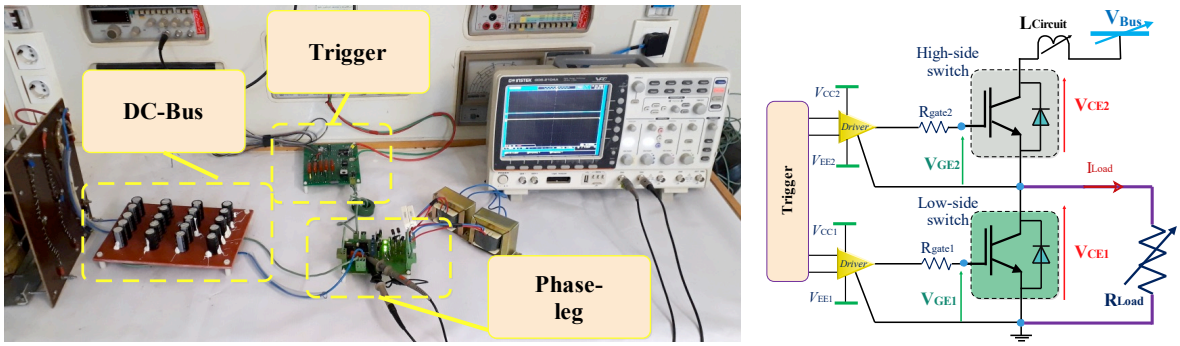


Fig. 7. The effect of C_{GC}/C_{GE} ratio on the crosstalk.

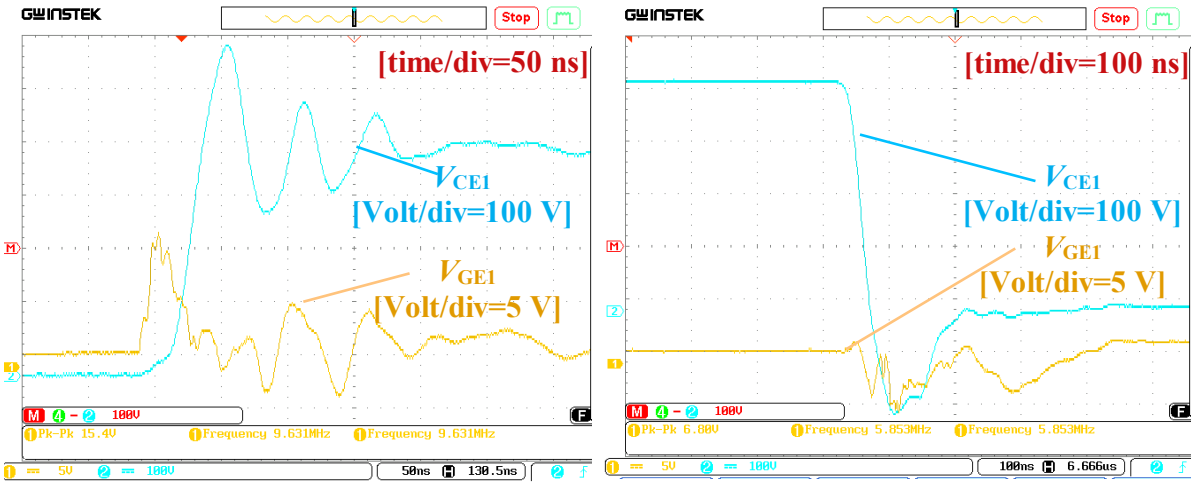
Experimental results

In order to verify the proposed crosstalk model, a phase-leg structure is implemented and experiments are conducted. The overview and block diagrams of the test setup are provided in Fig. 8-(a) and (b) respectively. The specifications of the experimental case are the same as the case used for simulation. The procedure of the test is as follows. The trigger unit provides a low-level signal for the input of the low-side device driver. Thus, the low-side device is in the off-state in the experiments. The trigger signal generates a 10 µs pulse width high-level signal for the high-side device. Before the arrival of this high-level signal, both switches are in the off-state. Since the resistance of R_{Load} is much less than the off-state impedance of the high-side switch, the voltage across the low-side switch is almost zero when both devices are in the off-state. After receiving the turning-on command, the high-side device voltage decays from V_{bus} to zero. At the same time, the collector-emitter voltage of the low-side device (V_{CE1}) raises from zero to V_{bus}. As deeply discussed in the paper, this voltage change causes a positive voltage jump at gate-emitter terminals of the low-side device (V_{GE1}). Fig. 9-(a), represents the experimental waveforms of this event in the high-side switch turning-on process. In the turning-off process of the high-side switch, V_{CE1} decays from V_{bus} to zero. Thus, V_{GE1} experiences a negative voltage change as occurred in Fig. 9-(b).



(a) (b)

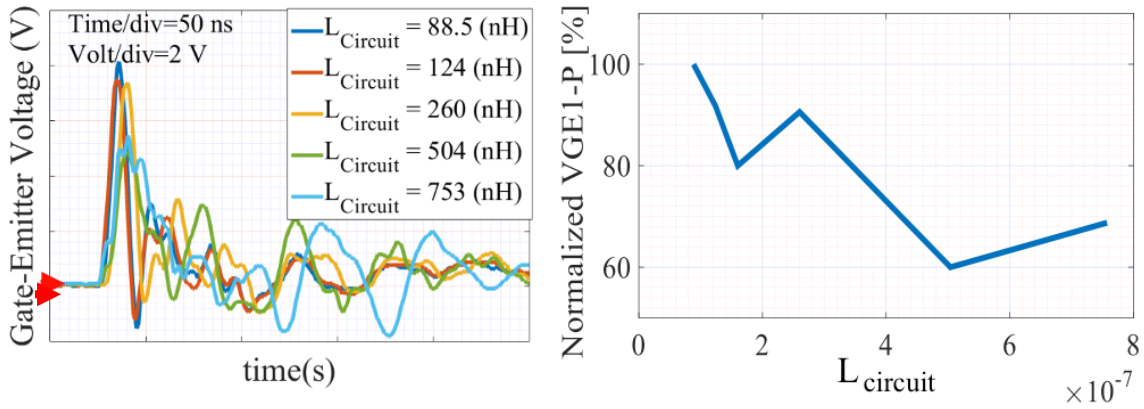
Fig. 8. The photo of the test bench (a), and the experimental setup block diagram (b).



(a) (b)

Fig. 9. The low-side switch waveforms in the high-side switch turning-on process (a), and in the high-side switch turning-off process (b).

In the experiments, the value of the power circuit inductance ($L_{circuit}$) is changed by adding external inductance. The value of the original circuit inductance is the sum of PCB traces inductance and the DC-link ESL. The inductance of PCB tracks is calculated based on the guidelines of [25] and [26] as 50 nH. In addition, the ESL of the DC-Link is 35 nH according to the component datasheet. Fig. 10-(a) presents the waveforms of V_{GE1} when the value of $L_{circuit}$ is changed. Fig. 10-(b) shows the normalized values of the low-side switch gate-emitter peak value ($V_{GE1\text{-}P}$) based on the existing maximum value. Considering Fig. 10, the optimum regions for $L_{circuit}$ values are also detectable in practice. This outcome is in accordance with the results achieved by the analytic model.



(a) (b)

Fig. 10. The experimental gate-emitter voltage waveforms of the low-side switch when the $L_{circuit}$ varies.

In order to investigate the converter/device operating point on the crosstalk experimentally, several experiments are carried out. Firstly, the load current is changed and the $V_{GE1\text{-}P}$ is measured. Fig. 11-(a) presents the obtained experimental results when the load current is varied. These results are in accordance with the results achieved from the crosstalk model. As can be seen, the $V_{GE1\text{-}P}$ has higher values when the load current decreases. Thus, the effect of the crosstalk is more dominant in the light load conditions of the converter. As another important parameter, the off-state voltage of the device is changed in the experiments. The results of these experiments are provided in Fig. 11-(b). Regarding Fig. 11-(b), by increasing the off-state voltage of the device, the $V_{GE1\text{-}P}$ value is increased. A saturated region is detectable in Fig. 11-(b) which can be explained by the non-linear behavior of C_{GC} which exhibits very low values when its voltage grows. Considering Fig. 11, the most dangerous condition for the converter in terms of crosstalk is when the converter is operating under high input voltage levels and light-load.

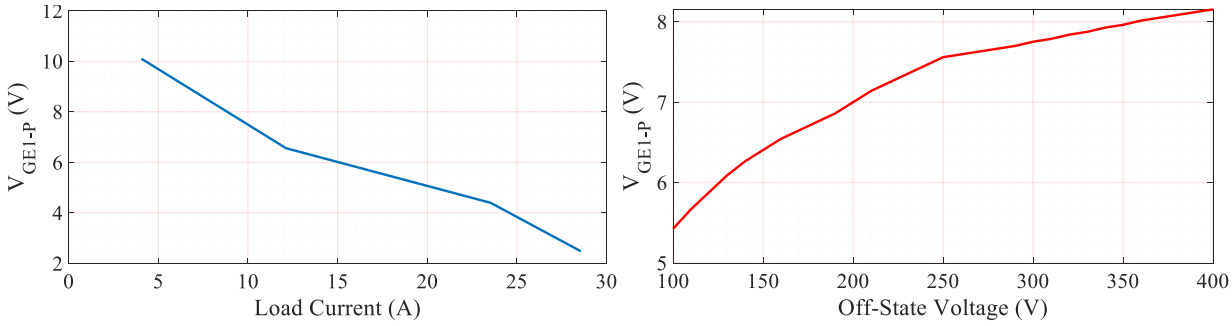


Fig. 11. The experimental results obtained by changing the operating point of the device. (a)-the change in the load current, and (b)- the change in the device off-state voltage.

Conclusion

Crosstalk remains a big challenge in power electronics converters including a phase-leg in their structure. Traditional models face problems in representing and analyzing the power path parasitic elements accurately. Thus, a new general model was introduced in this paper. The concentration is on the power path parasitic inductance and high-side switch current and off-state voltage. The crosstalk occurring in a converter arm is sensitive to the values of parasitic parameters. Hence, by changing the parasitic elements, their effect of them on crosstalk was analyzed. The considered switch nominal values are 600 V and 75 A. Therefore, the DC-link voltage in the case study is 400 V and the device current is 20 A. By increasing the output current, the peak value of the gate-emitter voltage decreases, which means crosstalk mostly has its highest values when there is a low power load in the output. The power path parasitic inductance is a significant element in crosstalk. Furthermore, there are several optimum regions in the curve due to the device model. Hence, the PCB designer must take ultra care of the power path inductance in order to mitigate the crosstalk effect on the arm. In addition, the parasitic capacitance ratio of IXGH60N60 is investigated. As a result, based on the application, the designer should opt for a device with a low parasitic capacitance ratio. Finally, the experimental results present so as to verify the proposed model and simulation results.

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