Climatically Induced Insulation Degradation in Power Semiconductor Modules of Wind Turbines

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Keywords

≪Lifetime≫, ≪Condition Monitoring≫, ≪Degradation≫, ≪Humidity≫, ≪Wind energy≫

Abstract

Power converters are among the most frequently failing subsystems in wind turbines. Humidity-induced degradation plays a key role, especially in locations with geographically high absolute humidity. In a laboratory experiment, a failure of a power module induced by humidity and condensation could be replicated under extreme climatic conditions.

Introduction

Power converters in wind turbines (WT) stand out with high failure rates [1]. The SPARTA initiative reported an average of 1.32 repairs per turbine and year from the converter subsystems of 1045 offshore wind turbines in the waters of the UK [2]. A study of Fraunhofer IWES based on a worldwide fleet of 2734 onshore and offshore turbines revealed an annual average of 0.48 converter system failures per turbine, with a third of it associated with the core components including the IGBT semiconductor modules, their gate-driver units, DC link capacitors, and busbars [3]. In view of the fact that the frequent and typically unexpected failures cause substantial repair costs and downtime-related revenue losses, enhancing converter reliability is an important task to further reduce the cost of wind energy.

Previous research has shown that environmental influences, in particular humidity, play a key role in the emergence of converter failures while well-understood thermo-mechanical fatigue is relegated to the background as a life-limiting mechanism in wind turbines [4, 5]. Failures are not limited to power semiconductors but spread over the whole converter subsystem. Among the issues reported from the field, degradation of the insulation foils between the DC terminals of power modules as well as in the area of DC busbars or laminates under the influence of moisture or condensation is a repeatedly observed phenomenon: The insulating materials degrade until the insulation strength drops below a critical limit and short-circuit failure occurs between DC+ and DC− [4]. In addition to improvements in the

design and protection of the converter hardware, condition monitoring is an important measure to prevent impending failures and reduce downtime. In order to be effective, it must cover the failure modes and mechanisms prevailing in the field. As a consequence, condition monitoring approaches should be capable of detecting not only faults developing at the semiconductor chip or packaging level, but also insulation degradation in the converter system.

The investigations of this paper serve as a first step toward potential monitoring approaches of these insulation properties. A power module from a wind turbine is examined in a simplified electrical load setup in a climatic chamber: The test specimen is subjected to a typical DC link voltage level used in low-voltage converters in the field but without a continuous pulse width modulation (PWM). The applied climate profile is based on field-measurement data from India and replicates the highly fluctuating climatic conditions to which power converters in wind turbines are exposed [5].

Measurement Configuration

The following chapter describes the experimental configuration and discusses the selection of the operating parameters. Important aspects of the test setup are detailed here and the operational control is presented.

Experimental Setup

The test setup as shown in Fig. 1 consists of two devices under test (DUT). The first module is a Semikron SKiiP 513GB 172CT (DUT 1) consisting of a total of four individual half-bridges of which three are connected on the AC side in this test setup. The module has an integrated gate driver unit and a heat sink for liquid cooling that was not used during the test. Snubber capacitors are mounted directly to the DC terminals. The second DUT is a submodule (DUT 2) from a Semikron SKiiP 603GB 123CT but without the DCB (direct copper bond) substrate and, thus, without power semiconductor components. Also, the gate driver unit is removed and no snubber capacitors are mounted in this case. As the two DUTs are from different module generations, the materials of their insulation foils used at the DC terminals differ. Though the material thickness is identical with both types measuring 0.25 mm, differences can be identified mainly in color: the foil of DUT 2 is transparent, whereas on DUT 1 it has an additional orange tint.

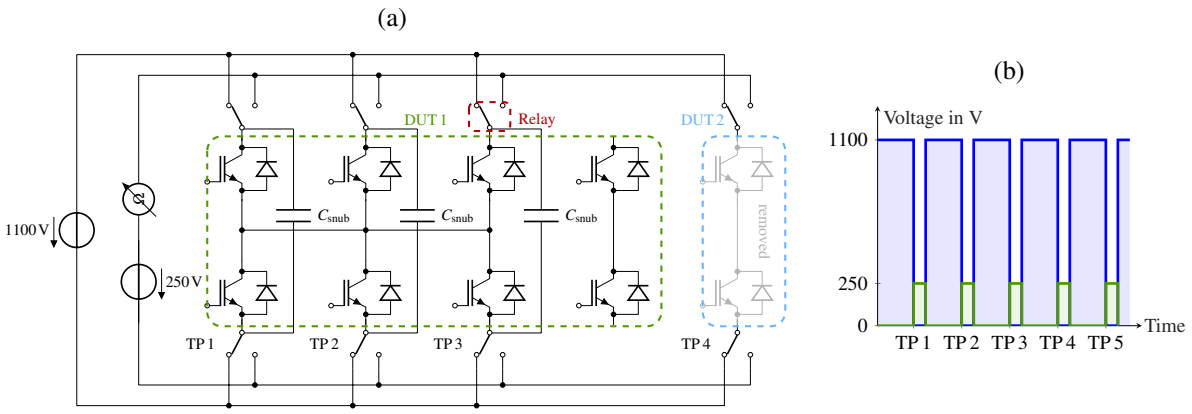

Fig. 1: Schematics of the experimental setup: Simplified circuit diagram of the test setup consisting of a high-voltage source (a): an insulation resistance meter with a laboratory source for the offset voltage, the two DUTs, and the relays for switching the test configuration (TP 1 to TP 4). Schematic of the applied voltage, with cycling between static load states and the individual test points (b): Here, TP 5 is a parallel connection of TP 1-3.

A high voltage source is used to apply a voltage of 1.1 kV to the DUTs, which corresponds to the DC link voltage commonly used in low voltage wind turbine converters. The switch-on time of the high voltage is about 150 ms, which means that a significant influence of overvoltage peaks due to parasitic inductances in the setup can be excluded here. After 15 min in load state, the setup automatically switches to

measurement state and measures one of the test points (TP) for 6 min after which it returns to load state, see the right part of Fig. 1 for a schematic. To be able to carry out the corresponding insulation resistance measurements, the DC link voltage is switched off during the measuring process and the voltage source is disconnected by contactors. The individual measuring sections are switched to the measuring circuit via relays. TP 1 to TP 3 are associated with the respective half-bridges in DUT 1, see Fig. 1, TP 4 is the submodule without semiconductors (DUT 2), and TP 5 switches to a parallel connection of the three half-bridges TP 1-3 (DUT 1). During measurement, the insulation resistance meter is connected in series with a 250 V voltage source to force the diodes into a reverse-biased operating point. This is necessary to match the measurement procedure of the insulation resistance meter to the requirements of the experiment. The IGBTs remain switched off throughout the whole experiment.

Climatic Conditions during the Experiment

With the aim of exposing the power modules to extreme climatic stress, we have chosen parameters based on field data from India [5]. Fig. 2 shows the temperature and humidity conditions measured inside the cabinet air of the power converter with a temporal resolution of 1 min. The 10-day excerpt of the time series in the left part of the figure illustrates the pronounced day-night cycles to which power converters in wind turbines are typically exposed, cf. [5]. The climatogram in the right part of the figure summarizes the climatic conditions encountered during the 2-year measurement campaign and indicates the climatic conditions selected for the present experiment.

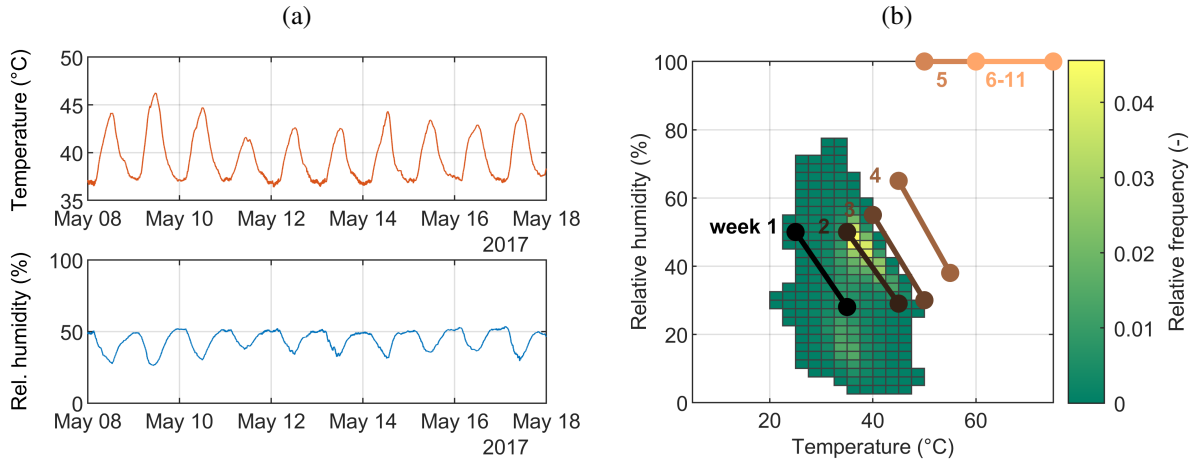

Fig. 2: Climatic conditions measured inside the converter cabinet of a WT in India; time series excerpt with typical day-night cycles of temperature and relative humidity (a), climatogram based on the entire 2-year measurement campaign with climatic conditions chosen for the experiment (b).

The test can be divided into two parts: During the so-called pre-stress phase of the first four weeks, a weekly increase of humidity and temperature is carried out. Within each week, day-night cycles occurring in the field are replicated in a simplified manner by toggling every 12 h between a state with higher temperature and lower relative humidity and a state with lower temperature and higher humidity. As Fig. 2 indicates, the climatic conditions applied during the first three weeks of the experiment correspond to conditions that are representative of those inside the considered wind turbine: The profile applied in week 1 replicates a level of absolute humidity encountered during spring and autumn; week 2 is typical of the Indian summer, while week 3 represents the strongest climatic stress exposure of converter components possible during summer. From week 4, the climatic stress is increased beyond conditions measured in the field. At the end of each week, an additional 12 h cycle with a temperature of 35 °C and 20 % relative humidity is conducted to allow for drying of the DUTs. After four weeks, i.e. 28 days, the stress phase begins: The DUT is subjected to extreme climatic stress by setting the humidity to 100 % and further increasing the level of the temperature cycles. First, the temperature is toggled between 50 and 60 °C, thereafter between 60 and 75 °C. The drying cycles at the end of every week are also implemented in the stress phase.

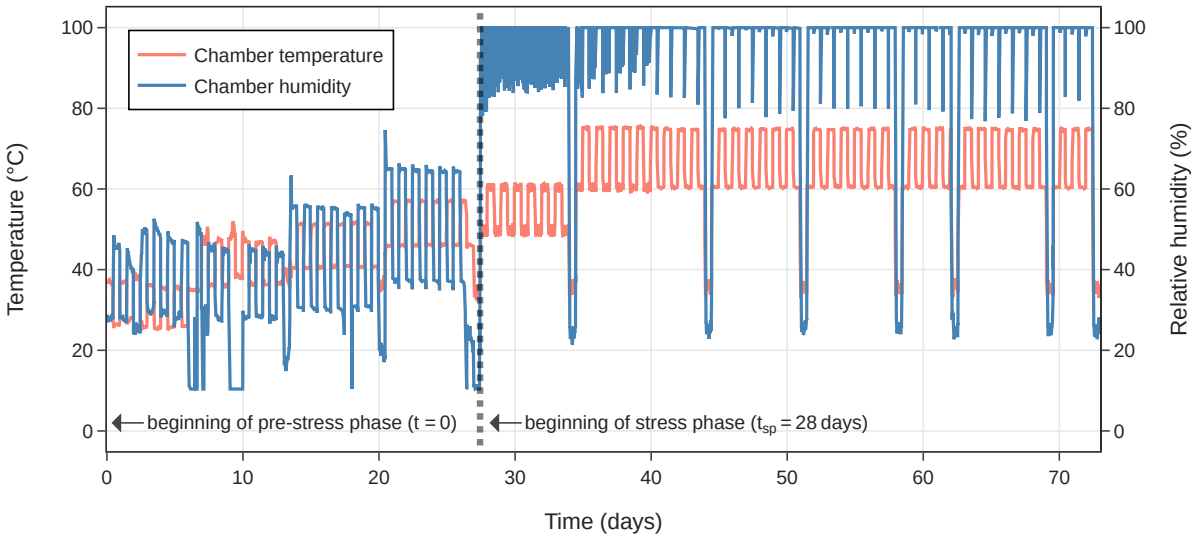

Fig. 3: Measured temperature and humidity inside the climate chamber over time. The dotted line indicates the transition between the two phases of the experiment.

It is important to note that the climatic conditions of the stress phase in the second part of the experiment include condensation. These conditions are far outside the specification of the power modules. While the level of absolute humidity used to enforce the precipitation of liquid water is excessive, the occurrence of condensation in converters of wind turbines in the field is a matter of fact. As the DUTs are subjected to voltage only and no continuous PWM operation with load currents is carried out, there are only negligible leakage currents through the semiconductors such that the modules experience no considerable self-heating. Therefore, the temperatures of the modules follow the climatic conditions inside the chamber with a time delay caused by their thermal capacity. The climatic conditions inside the test chamber during our experiment are shown in Fig. 3.

While the levels of the applied climatic cycles are intended to remain identical during each week of the test period, Fig. 3 shows that the climatic conditions recorded inside the chamber during the experiment deviate from the intended time series to some extent: During the pre-stress phase, the humidity control failed several times, causing an unplanned reduction to 10 % relative humidity. Furthermore, at the beginning of the stress phase, the climate chamber had issues regulating to 100 % relative humidity, identifiable by the noisy data between days 28 and 35. Additionally, due to a failure incident—see results—on TP 4 after 61 days we had to stop the chamber and restart it, beginning with a drying cycle. For that reason, there is a period shorter than 7 days between two drying cycles between days 58 and 62.

Results and Discussion

In the following chapter, we present and discuss the measured resistances, a post-mortem analysis of a failed module, and an investigation of parasitic conductive paths at the power modules.

Measurement Results

The recorded resistance data for the four test points (TP 1, TP 2, TP 3, and TP 4) and the parallel connection of TP 1-3 (TP 5) over the course of the experiment are displayed in Fig. 4.

During the pre-stress phase, a 12 h toggle of the resistance can be observed for TP 1-3. The mean value of this toggle decreases from 300 MΩ to 70 MΩ with increasing temperature. Due to the parallel connection of TP 1-3, a lower resistance value of $\approx \frac{1}{3}$ of that of the single TPs is expected for TP 5. The measured resistance time series decreasing from 100 MΩ to 25 MΩ agrees with this expectation. All variations observed in this phase show a typical strong temperature dependence of the semiconductor components

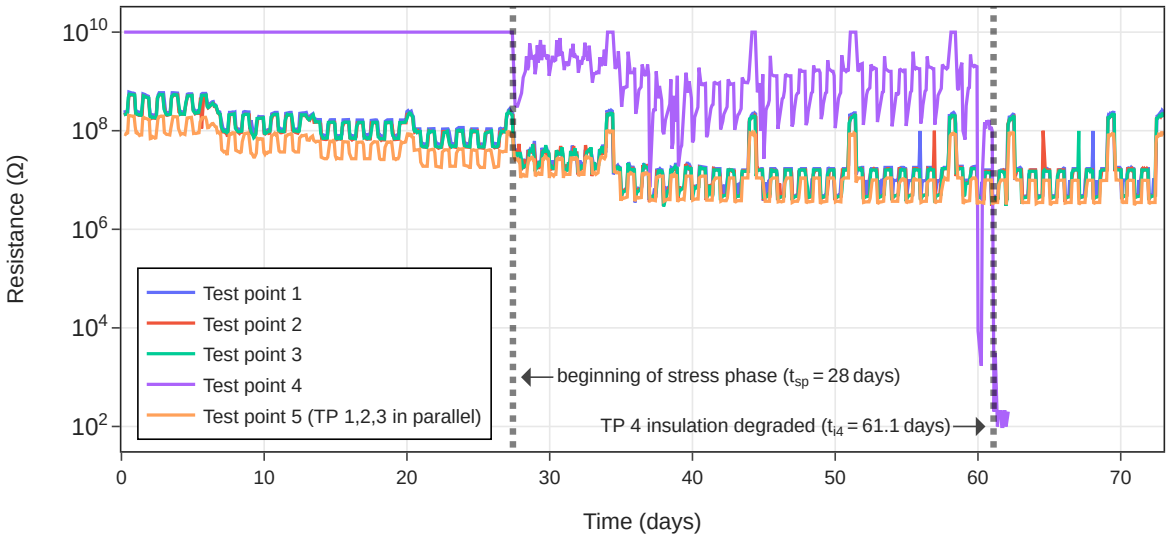

Fig. 4: Raw measured resistances from the resistance meter for each test point.

and are, therefore, attributed to this behavior, see also Eq. (1) in the chapter after next. Furthermore, during the drying cycles the resistance always stays at 250 MΩ (90 MΩ for TP 5), thus, we see no signs of irreversible degradation in the pre-stress phase. No change in the resistance is observed for TP 4 as its insulation resistance remains above the detection limit of 10 GΩ.

With the beginning of the climatic stress phase at $t_{sp} = 28\,\mathrm{d}$ and its harsh ambient conditions, a further decrease of the toggling behavior of the resistances at TP 1-3 and a significant drop in the insulation resistance of TP 4 is observed. After this initial drop, a 12 h toggle of the resistance is also visible for TP 4, although not as regular as for TP 1-3 or TP 5. Since the humidity is constant at $\approx 100\,\%$ in this phase, changes in the insulation resistance are mainly attributed to a temperature dependence of the power semiconductor path, dominating at TP 1-3 and 5, as well as condensation, dominating at TP 4.

Compared to the pre-stress phase, the slopes of the resistances of TP 1-3 keep their regular toggle also in the stress phase, as expected by a semiconductor's temperature dependence. We observe values of around 100 MΩ in the first week and 10 MΩ thereafter. During the drying cycles, the resistances at TP 1-3 always recover to values around 250 MΩ, i.e. no evidence of an irreversible degradation of the insulation in DUT 1 during the time of the experiment is found in the data.

On TP 4 during the first week of the stress test, i.e. $t < 35\,\mathrm{d}$, the mean value remains around 2.5 GΩ, after half of the second week it reaches approximately 350 MΩ. The drying periods also show a recovery of the previously reduced insulation resistance. As the recorded data exceeds the measuring range of the insulation resistance meter, it remains unclear if during these periods the insulation recovers to its original value at the start of the measurement campaign.

After 60 days, during ambient conditions of a temperature of 75 °C and 100 % relative humidity, the resistance at TP 4 suddenly drops to a value of merely 1.7 kΩ. It recovers to 150 MΩ during the subsequent cycle with a lower temperature of 60 °C, but breaks down completely to the measuring range limit of 100 Ω during the next cycle on day 61 showing the collapse of the insulation of TP 4. This event is highlighted by a dashed line in Fig. 4. The incident's timestamp is denoted by t_{i4}. At this point in our experiment, a low resistance path has formed triggering one of the protection measures of the setup: The overcurrent protection (OCP) of the voltage source intervenes, not allowing to apply high voltages during the load part. Due to this feature, the affected insulating area at the DC terminals is not completely destroyed yet at t_{i4}. This also means that the plotted data does not show the final resistance.

To investigate the condition of the insulation, we reduced the target voltage to determine the residual voltage strength of the section. After approximately 200 V of residual voltage strength, the OCP shut

down the power supply. This value could not be clearly reproduced after a recurrent break-in. Another attempt to set the voltage source back into operation was made by resetting the OCP and subsequently ramping up the DC link voltage, albeit, without success. A fault in the measuring system could be ruled out. After several endeavors we recognized the complete destruction of the insulating foil, also displayed in Fig. 6 (b), that we wanted to enforce within the experiment with its harsh climatic condition. After this discovery, the connections to TP 4 were detached from the setup to be able to continue the experiment under voltage load at the remaining test points.

Post-Mortem Analysis

After the removal of the damaged submodule from the test bench, significant, visually recognizable damage can be observed, see also Fig. 5 and Fig. 6. Residues from repetitive water condensation are found on the surface of the entire submodule. Metallic surfaces have undergone corrosive processes, particularly visible on screw connections and load terminals. The insulation foil which is folded between the DC terminals of the module has lost its insulation properties due to partial disintegration, see Fig. 6 (b). It is likely that the presence of condensed water in combination with the voltage between the terminals has driven the degradation process. We suspect that the low resistance path that formed due to the degradation of the film resulted in an increased temperature at the spot and that the temperature impact finally became severe enough for carbonization to occur.

Fig. 5: Close-up image of the damaged insulation foil between the DC contacts.

The disintegrated area on the foil is located at the folding zone of the foil between the two busbars. There is also massive damage to the housing of the power module in the form of melted plastic and black stain at this point, see Fig. 6 (a).

Apart from the mentioned damage in the vicinity of the DC connectors and stain on the housing, the tin-plated busbars inside the module remain in relatively speckless condition. Humidity-induced degradation due to moisture penetration into the silicone of the module is discussed in the literature [6, 7]. In the present case, however, also no change in structure or color of the insulating foil are visible on the inside of the submodule. Thus, we assume that there has only been faint, if any, condensation or capillary motion of water to this part of the module.

Apart from traces of corrosion and deposits, the other four half-bridge modules—with different insulating foil—show no externally visible damage, which is consistent with the measurement results.

Investigation of Parasitic Conductivity

As shown in the post-mortem analysis, the insulation foil at TP 4 has been destroyed during the experiment. As the module DUT 2 at TP 4 contains no DCB with semiconductors, its changes in resistance must be solely attributed to the insulation foil between the DC contacts. Consequently, we also analyzed the changes in the resistances at TP 1-3 as well as TP 5 (the parallel connection of TP 1-3) for a

(a) (b)

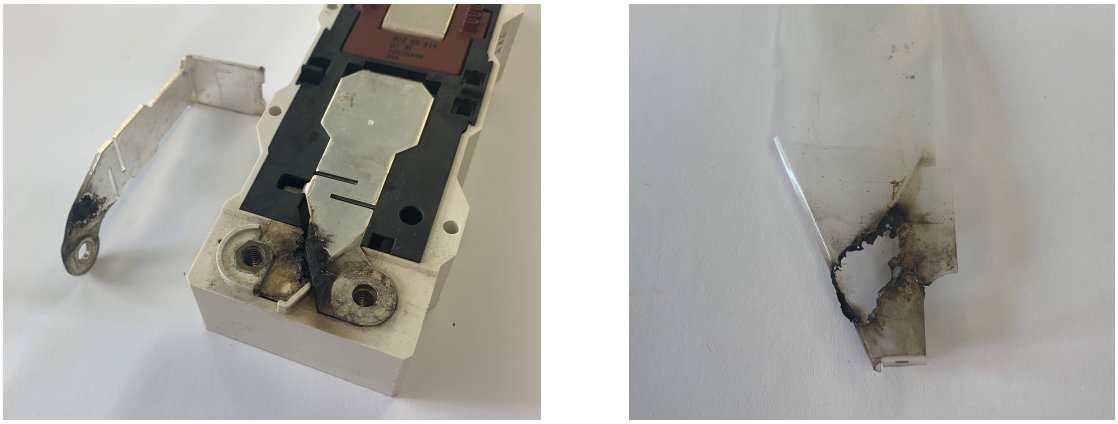

Fig. 6: Close-up image of the defective area with the insulation foil removed and the upper part of the housing disassembled (a). Damaged insulation foil (b).

possible emerging parasitic conductive path. Due to the nature of semiconductors, the resistance in the blocking state of the DUT itself is highly dependent on the semiconductor temperature. In the present case without a load, the DCB temperature signal available from the gate driver unit recorded during the experiment provides a good approximation of the semiconductor temperature and is, therefore, used for the following analysis.

Assuming only minor changes in resistance caused by parasitic paths during the pre-stress phase, data recorded within the first 28 days of our experiment are used to fit an empirical semiconductor resistance model:

$$R(T) = R_0 \cdot \exp\left(\frac{E}{2k_\mathrm{B}T}\right) \tag{1}$$

This model comprises only two fit parameters R_0 and E, whereas k_B is the Boltzmann constant. This simple model is used under the assumption that all conductive paths of the DUT that are connected in parallel to our measurement device undergo a similar temperature dependence, i.e. their band gaps and induced charge carrier densities closely resemble each other. As the main resistance should be dominated by the properties of the IGBTs in their blocking state, we see this as a valid approach. Furthermore, it provides a straightforward solution to model an otherwise complex system.

The parameters are estimated separately for each test point based on the corresponding data set using a Levenberg-Marquardt algorithm. The resulting regression functions are shown as dotted curves on top of the underlying data in Fig. 7 (a), the corresponding parameter values are listed in Table I.

Table I: Resulting optimized fit parameters of the empiric semiconductor resistance model (1) with standard deviation directly obtained from the optimizer used as uncertainty.

Test point	R_0 (mΩ)	E (eV)
1	$0.67 \pm 14\,\%$	$1.40 \pm 0.5\,\%$
2	$0.28 \pm 7\,\%$	$1.44 \pm 0.25\,\%$
3	$0.38 \pm 7\,\%$	$1.43 \pm 0.27\,\%$
5	$0.20 \pm 12\,\%$	$1.41 \pm 0.5\,\%$

Fig. 7 (b) exemplarily summarizes the procedure for TP 1 on a logarithmic scale with both the underlying data of the pre-stress phase $t < t_\mathrm{sp}$ as purple circles as well as the data of the stress phase $t \geq t_\mathrm{sp}$ as red crosses. The regression function is depicted by the dashed black line accompanied by thin purple dashed lines that show the extent of the algorithm's uncertainty region. Although this uncertainty region is slightly smaller for the data of the other test points, the overall behaviors strongly resemble each other.

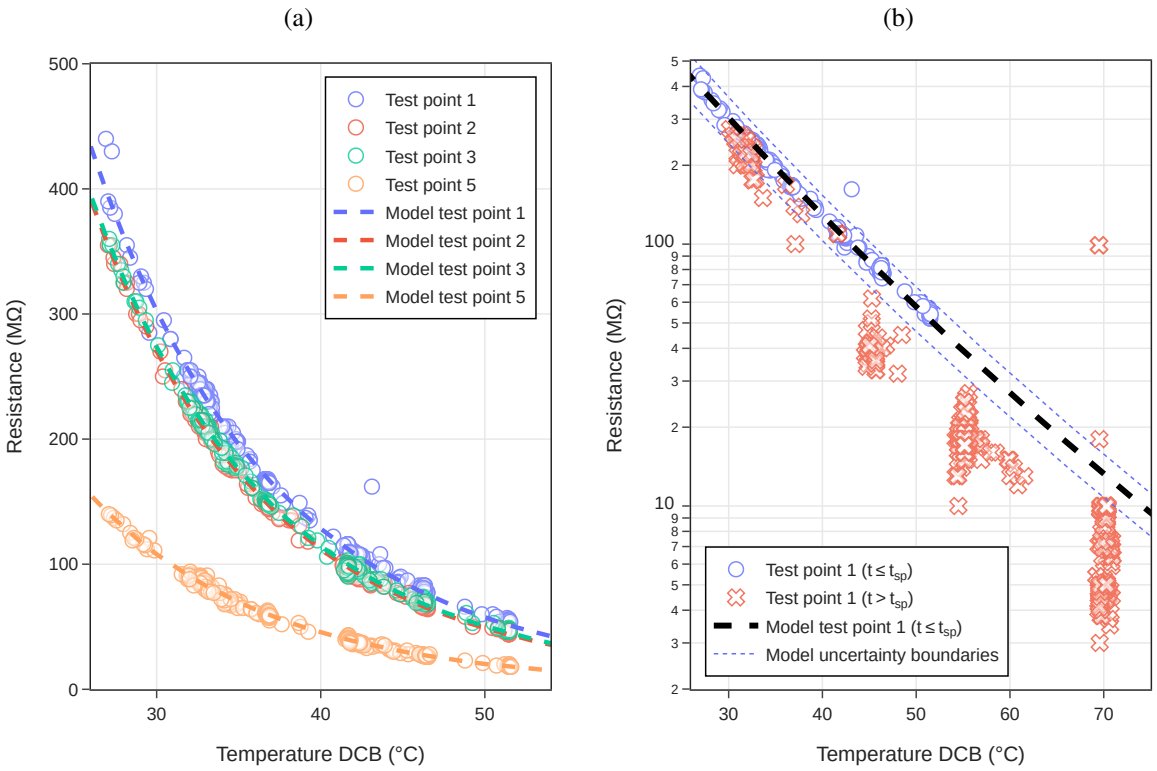

Fig. 7: Visualizations of model (1) to the data of $t < t_{sp}$ (a). Detailed logarithmic plot of the regression function with uncertainty region resulting from the standard deviations of the parameters and corresponding data $t < t_{sp}$ in purple circles as well as data of stress phase $t \geq t_{sp}$ for the calculation of the parasitic resistance in (2) in red crosses (b).

As the next step, all measured resistance data is subtracted from the model. Under the assumption that the temperature dependence of the semiconductor part of the total resistance does not change during the stress phase, i.e. the resulting parameters of (1) are also valid for $t > t_{sp}$, the main reason for any deviation must be a parasitic conductive path parallel to the DC connectors. The resistance of this parasite is described by

$$R_{\text{parasitic}} = \frac{R_{\text{model}} \cdot R_{\text{measure}}}{R_{\text{model}} - R_{\text{measure}}}. \tag{2}$$

As the deviation from the model $R_{\text{deviation}} = R_{\text{model}} - R_{\text{measure}}$ can become very small or even negative due to scattering of data around the model, the resulting parasitic resistances are capped at a maximum of 50 GΩ and also set to 50 GΩ for negative values. The latter results when the scatter of data is above the regression function, cf. Fig. 7. The resulting data is displayed in Fig. 8 for each test point: TP 1, 2, and 3 depicted by purple, red, and green circles in the top pane, TP 5 by yellow circles in the bottom pane. To show a general trend, rolling mean values with a time window of 24 h over the data for TP 1-3 in semi-opaque black and for TP 5 in semi-opaque brown are added to the plot.

During the first phase of the measurement, most data of TP 1-3 up to t_{sp} remains above 10 GΩ. Nevertheless, the scattering goes down to values as low as 1 GΩ. Only one outlier reaches 170 MΩ. With the beginning of the stress phase at $t > t_{sp}$ with its 100 % relative humidity, the parasitic resistances drop to a mean of 50 GΩ, decreasing to a mean of 28 MΩ when the temperature is further increased during the stress test. This value keeps decreasing to values of 18 to 20 MΩ at the end of the experiment. During the drying phases, the resistance recovers to higher values of 1 to 10 GΩ. Albeit, the values do not reach the pre-stress phase values but remain two orders of magnitude lower. After the first drying phase of the stress phase, two domains of parasitic resistances can be observed in the raw data of TP 1-3: One around

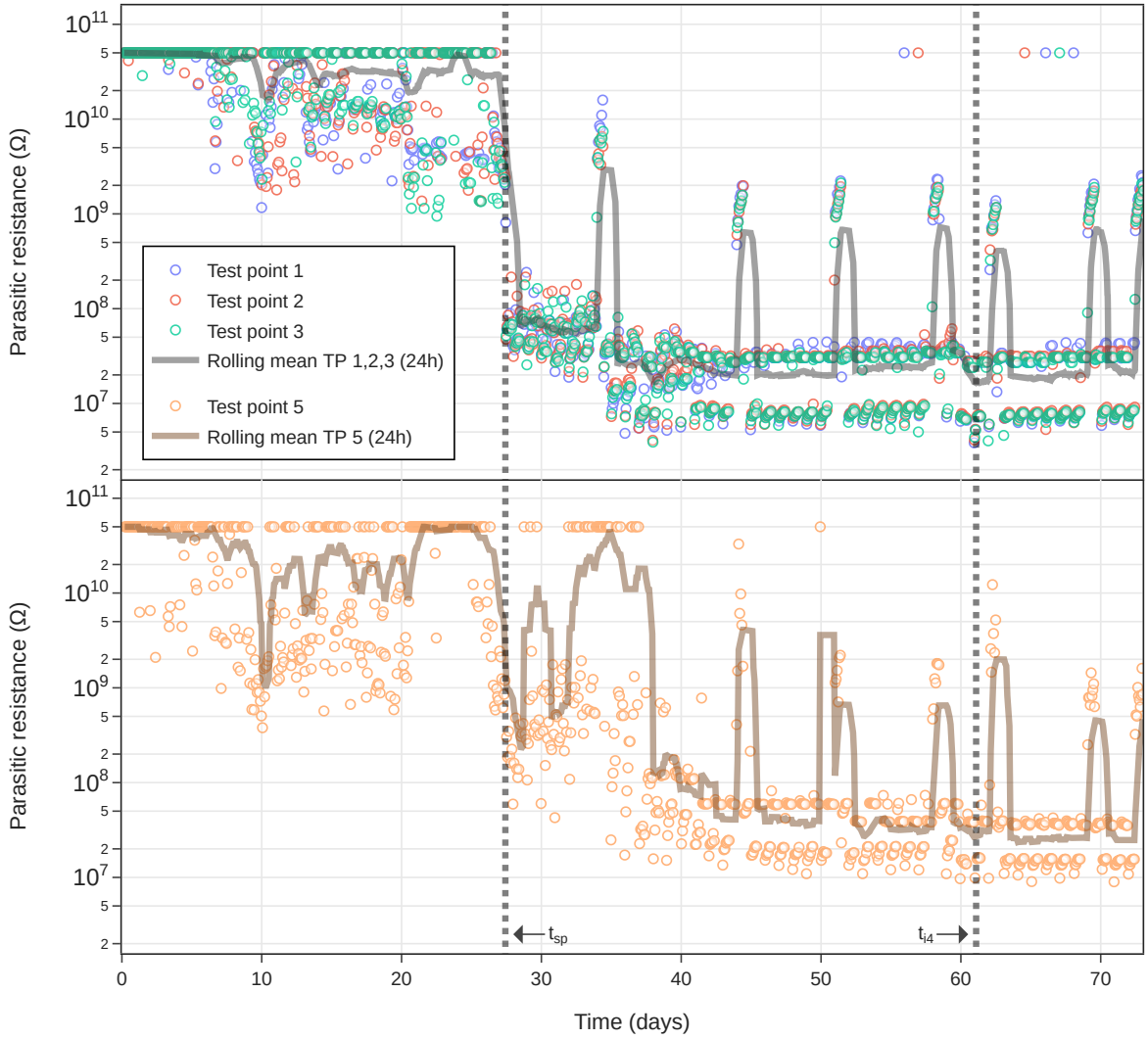

Fig. 8: Deduced parasitic resistances parallel to the DC connector of each test point and a 24 h rolling mean over all data points highlighting the general trend.

30 and the other one around 8 MΩ. They are directly related to the toggle between the two temperatures in this phase. Nevertheless, these temperatures are outside the scope of the training data for the model (1). Therefore, the uncertainty of the model might also play a role here.

When considering the data at TP 5, the general trend is similar. For $t < t_{sp}$ also most data is above 50 GΩ, although the scattering is stronger leading to values as low as 200 MΩ. After the beginning of the stress phase, the decrease in parasitic resistance is not as strong as for TP 1-3 although a parasitic resistance of $\approx \frac{1}{3}$ of the parasitic resistances of TP 1-3 due to their parallel connection might be expected. However, the value range of the recorded data of TP 5 is much lower, leading to an already higher uncertainty that might be amplified in the calculation of the parasitic resistance. The values further decrease during the run time of the experiment, also undergoing recovery to former values when drying phases take place. After the fifth drying phase in the stress phase on day 63, the values of the parasitic resistance show a similar range of values as for TP 1-3.

Conclusion

Using a climate chamber, we exposed IGBT power modules of type SKiiP3 under voltage load to increasingly harsh climatic conditions in a laboratory experiment. We have been able to reproduce the

failure of an insulating foil as previously observed in the field in the form of partial disintegration. The failure pattern on the empty module can clearly be attributed to climatic and electrical stress. Nevertheless, some uncertainties in clarifying the actual failure mechanism remain. One important question is how exactly the conductive path is formed. Due to the very harsh climate in the chamber, condensation has taken place on the devices under test, forming a water film on the whole surface of the housing. This has also led to various residual depositions on the housing of the modules and visible corrosion on all metallic connections.

Besides the observation of a complete disintegration of an insulating foil on a power module with removed semiconductors, an increasing parasitic conductive path in parallel to the DC connectors could also be observed on an unmodified power module in the presence of condensed water during the measurement's stress phase. Although the calculated resistances do not qualify for quantitative analysis, a general trend of an increasing parasitic conductivity with increasing temperature and humidity can be seen. These resistances recover during drying cycles, but only occasionally reach their original values after prolonged exposure to 100 % relative humidity at high temperatures. One reason might be an insufficient drying time, leaving residual humidity or even liquid water on or inside the foil. Furthermore, this observation is solely attributed to water condensation: An optical inspection during the post-mortem analysis showed no signs of irreversible degradation and the resistances returned to their original values on the unmodified power modules after the experiment.

While some questions remain unanswered at this stage, a key result of the present work is the successful identification of a precursor of insulation failure in IGBT power modules. In view of the urgent need for condition monitoring methods capable of detecting also humidity-induced degradation and faults in power converters, future work will be dedicated to adapting and testing the insulation-monitoring approach on larger units such as power stacks including DC link components in order to assess the suitability for application in the field.

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