Design For Enhanced Noise Immunity of PCB Coils used for Sensing Current through Power Devices

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Keywords

≪Current Sensor≫, ≪Silicon Carbide (SiC)≫, ≪Half bridge≫, ≪High frequency power converter≫, ≪Measurements≫.

Abstract

PCB coil, when placed near a current carrying trace, senses the rate of change of current by virtue of its flux linkages through the coil. Thereafter, the coil output is integrated to obtain the sensor output which is proportional to the trace current. Proximity of the PCB coil to external current carrying conductors can make the coil susceptible to undesired flux linkages which can interfere with the operation of the sensor. Furthermore, presence of a switching node near the coil, with high dv/dt, can influence the sensor output through parasitic coupling with the coil. This paper investigates the influence of external magnetic fields as well as on-board dv/dt on the performance of PCB coil based current sensors. Based on theoretical analysis followed by experimental investigations on two PCB coil prototypes on a half-bridge board, design guidelines for enhancing noise immunity of PCB coils are presented.

Introduction

Current sensing in power electronic devices requires high sensing bandwidth owing to the wide frequency spectrum of the pulsed switching current. Moreover, the sensor should introduce very low inductance inside the power-loop to minimize peak voltage overshoot in the drain-source voltage of the power device. For that purpose, the sensing element should posses a small size. Commonly available high bandwidth sensors like CTs are bulky and are difficult to integrate inside switching power-loops. Rogowksi coils have been demonstrated to be effective for sensing the current in power modules with high bandwidth [1]. Rogowksi coils are simple air cored coils which pickup the rate of change of flux linkage through the coil. The flux linkage through the coil is due to the magnetic field generated by the device current under measurement.

Similar to Rogowksi coils, PCB pick-up coils have been effectively utilized for sensing current on PCB traces with a high bandwidth [2–5]. Unlike circular Rogowski coils, these PCB coils are not fabricated with a symmetrical distribution of its turns around the current carrying conductor at the center of the coil. Consequently, the PCB coils lack the external magnetic field rejection capability which is inherent with circular Rogowski coils. The factors which influence the noise immunity of PCB coils towards external magnetic fields are identified in this paper. Further, based on these factors, methodology for the design of PCB coils with enhanced noise immunity is presented.

In addition to noise coupled by external magnetic fields, another source of noise which gets coupled to the PCB coil output is through the high dv/dt switching node, which is inherent with the power electronic circuit. While faster switching wide-bandgap (WBG) devices like silicon carbide (SiC) MOSFETs and gallium nitride (GaN) HEMTs are helpful for improving the efficiency of power converter, the high switching node slew rate (dv/dt) is responsible for higher noise being coupled to sensitive control and sensor circuitry. When this voltage node with high dv/dt gets coupled with the PCB coil through parasitic capacitances, a displacement current flows through the PCB coil which produces noise in the sensor output. An experimental scheme is presented to investigate the influence of dv/dt induced noise due to the structure of the PCB coil as well as the power-board layout.

PCB Coil Based Current Sensing

Fig. 1(a) shows a half-bridge circuit schematic. The hardware implementation of this circuit featuring embedded PCB coils is shown in Fig. 1(b). The PCB coil is fabricated around the trace which connects the power MOSFET to the DC busbars. The trace (T_2) is shown zoomed in Fig. 1(b), and it serves to connect source of M_2 with the negative DC bus. PCB layout of T_2 along with the PCB coil is depicted in Fig. 2. T_2 is routed on the bottom copper layer as shown in Fig. 2(a). Placement of the PCB coil above T_2 is shown in Fig. 2(b). Further, on a four-layered PCB, the PCB coil can be fabricated either between layer 2 and the top copper layer (Coil A) or between layer 1 and layer 2 (Coil B). For both these coil structures, the output voltage of the coil (V_C) is expressed as

$$V_C(t) = M\frac{dI_M(t)}{dt} \tag{1}$$

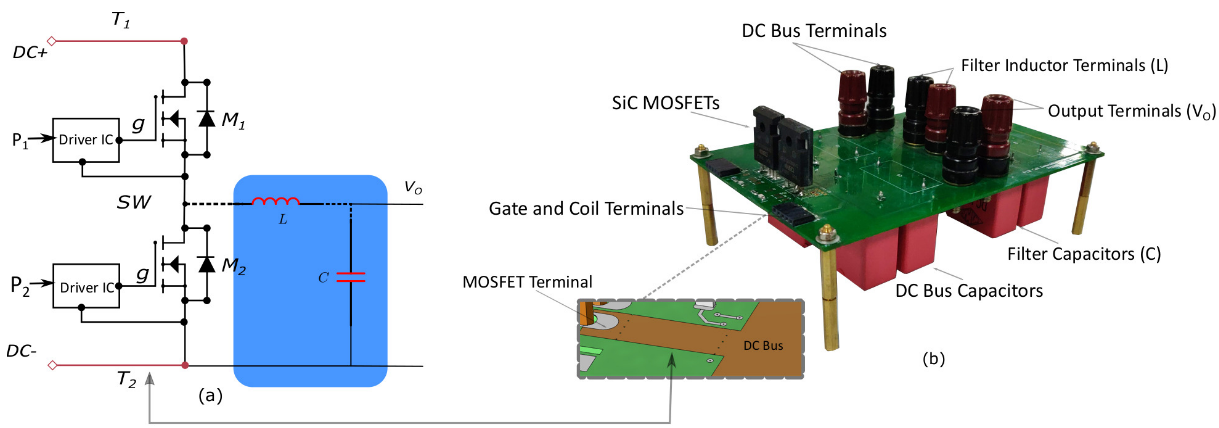

Fig. 1: (a) Half-bridge circuit. (b) PCB design of the half-bridge circuit with embedded PCB coils for trace T_1 and T_2.

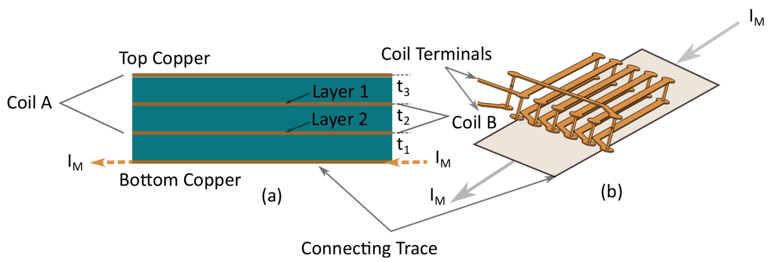

Fig. 2: (a) Possible coil designs on a four-layered PCB. (b) Embedded PCB coil above the trace.

where M is the mutual inductance between the power trace and the PCB coil. The coil voltage is then integrated using an analog integrator circuit with an ideal gain of $1/R_iC_i$ to produce the sensor output voltage (V_S), expressed as

$$V_S(t) = \frac{MI_M(t)}{R_iC_i}. \tag{2}$$

M is influenced by the size of the PCB coil as well as its proximity (t_1) with the power-loop trace. Both the coils, A and B, are fabricated and tested separately and the sensor voltage (V_S) is measured for both the coils as shown in Fig. 3(a) and Fig. 3(b), respectively. Current measurements are also compared with measurements from a commercial Tektronix current probe (TRCP0300), indicated as I_M. The drain-source voltage (V_{DS}) and the gate-source voltage (V_{GS}) of the MOSFETs are shown for both the tests. With the same integrator circuit gain ($R_i = 470\,\Omega$ and $C_i = 0.1$ nF) current measurement with coil A exhibits a sensitivity of 80 mV/A while the measurement with coil B exhibits a sensitivity of 65 mV/A.

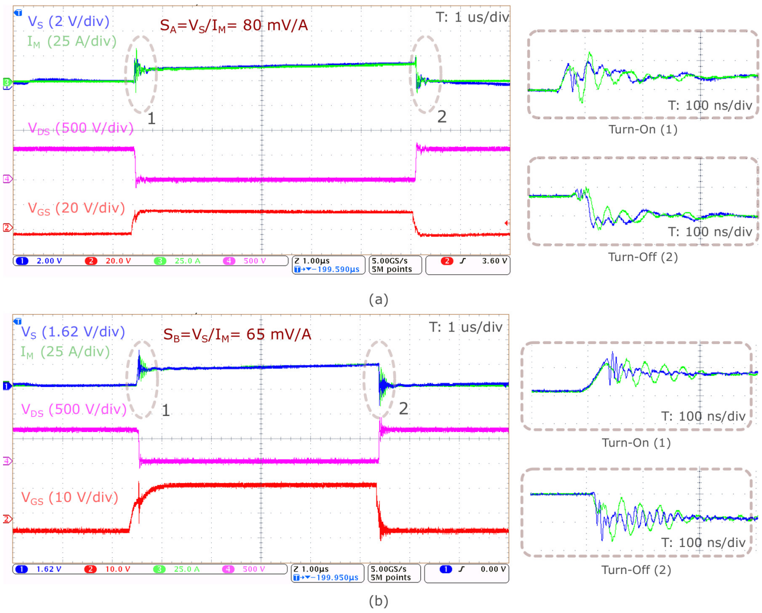

Fig. 3: (a) Pulse test results with coil A. (b) Pulse test results with coil B.

Therefore, coil A exhibits a higher mutual inductance than coil B with the power trace, owing to its larger size. Higher mutual inductance between the PCB coil and the power trace enhances the sensitivity of the sensor and helps reduce error in the sensor output due to op-amp input offset voltage [6]. However, a larger coil size can also make it susceptible to external magnetic fields. For both the coil A and coil B, an external current carrying conductor is placed 1.5 mm above the center of the PCB coil and the output voltage of the coil is measured, as shown in Fig. 4. Coil A shows a higher induced voltage due to the time-varying external current (I_L) on account of the larger coil size. An alternate approach to enhance M is by reducing the separation between the coil with the power trace. The separation (t_1) of both these coil designs to the current carrying trace is fixed by the number of layers in the PCB and the total finished PCB thickness. To quantify these factors, an analytical approach towards determining the influence of external magnetic fields on the performance of PCB coil based current sensor is now given.

Noise Due to External Magnetic Fields

Consider that the PCB coil lies in a region where an external magnetic field (B) is present. Let α denote the angle with which B penetrates the PCB coil, as shown in Fig. 5(a). Due to this magnetic field, the flux linking the PCB coil is expressed as

$$\lambda = (NA)B\sin\alpha = kB\sin\alpha \tag{3}$$

where N is the number of turns of the PCB coil and A is the cross-sectional area of each turn. The factor

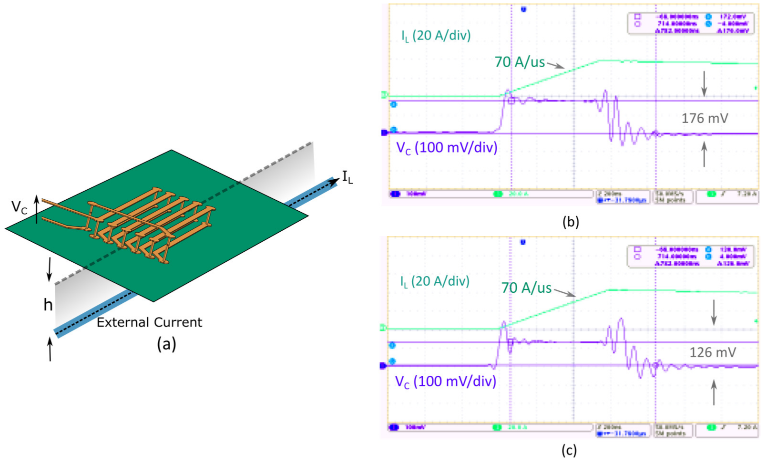

Fig. 4: (a) PCB coil in the presence of an external conductor carrying a current I_L. (b) Output voltage of coil A due to I_L. (b) Output voltage of coil B due to I_L.

$k = NA$ is, therefore, determined by the dimensions of the PCB coil. If B is time-varying, the voltage induced across the PCB coil is expressed as

$$V_c(t) = k \sin\alpha (dB/dt). \tag{4}$$

Therefore, this induced coil voltage can be a source of error in the sensor output. To estimate the error, B, as an illustration, can be considered as a homogeneous sinusoidal varying field as

$$B = B_m \sin \omega t. \tag{5}$$

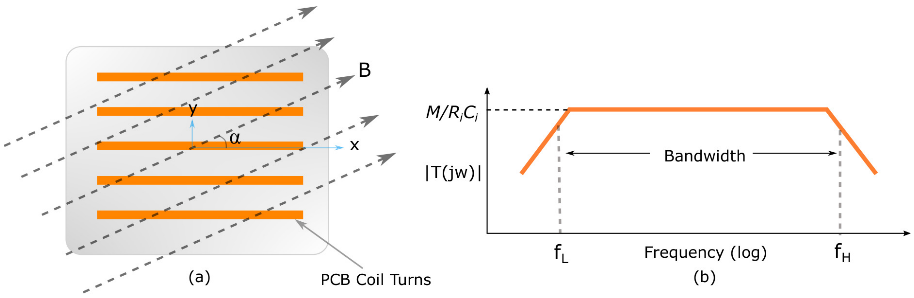

Fig. 5: (a) PCB coil in the presence of a penetrating magnetic field (B). (b) Frequency response of the PCB coil based current sensor.

If the frequency (ω) of the externally varying field (B) lies within the bandwidth of the sensor, as depicted in Fig. 5(b), the sensor output when measuring a current $I_M(t)$ is expressed as

$$V_s(t) = \frac{MI_M(t)}{R_iC_i} + \frac{kB_m \sin \omega t \sin\alpha}{R_iC_i}. \tag{6}$$

To analyze the noise immunity performance of the PCB coil based current sensor, an error can be defined in terms of the peak value of interference in the sensor output and the sensor output corresponding to the steady state value of device current ($I_{M_{SS}}$) as

$$E = \frac{kB_m / R_i C_i}{MI_{M_{SS}} / R_i C_i} = \frac{kB_m}{MI_{M_{SS}}}. \tag{7}$$

Therefore, immunity of the coil towards external fields can be enhanced by increasing M. However, increasing M by increasing the coil size will also lead to an increased k, and therefore not enhance the immunity of the coil towards external magnetic fields. Consequently, the factor k/M needs to be reduced for enhancing the noise-immunity of coils towards external magnetic fields. One approach to reduce k/M is by reducing the separation (t_1) between the PCB coil and the power trace. While t_1 can be reduced by employing a PCB with higher number of layers, clearances needed for track isolation at high voltages need to be respected. An illustration to demonstrate this concept is provided below.

Consider the case of two PCB stack-ups with four (A) and eight (B) PCB layers with different thickness, specified in Table 1 and Table 2, as provided by a PCB manufacturer. As shown in Fig. 6, if similar sized PCB coils are designed for both these stack-ups, stack-up B results in a coil with a mutual inductance of 3.5 nH between the coil and the power-trace and stack-up A results in a coil with a mutual inductance of 2.9 nH between the coil and the power-trace. Therefore, noise immunity can be enhanced by 20% with a different stack-up configuration. Therefore, depending on the intended application, PCB stack-up can play an important factor in determining the noise immunity of PCB coils against external magnetic fields.

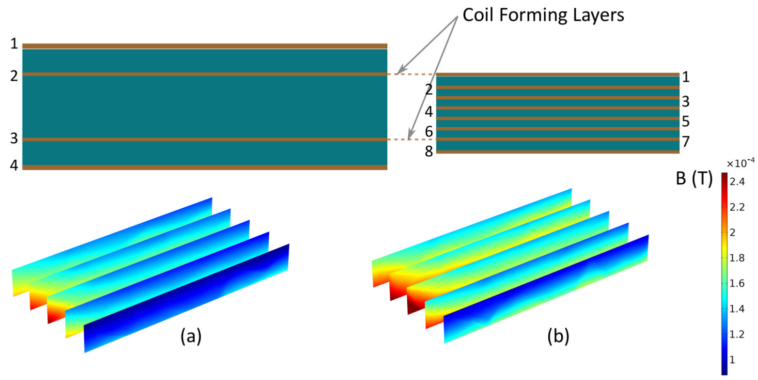

Fig. 6: PCB coil design and the magnetic field distribution through the coil due to a 1 A current flow through the power-loop for (a) PCB coil designed for a four-layered PCB of 1.6 mm thickness (Stack A) (b) PCB coil designed for an eight-layered PCB of 1.2 mm thickness (Stack B).

Finished Thickness	Tolerance	Prepreg 1-2	Core 2-3	Prepreg 3-4
1.6	±10%	0.31	0.73	0.31

Table I: Stackup thickness of a 4-Layer PCB (mm).

Finished Thickness	Tolerance	Prepreg 1-2	Core 2-3	Prepreg 3-4
1.2	±10%	0.08	0.13	0.14
	Core 4-5	Prepreg 5-6	Core 6-7	Prepreg 7-8
	0.13	0.14	0.13	0.08

Table II: Stackup thickness of an 8-Layer PCB (mm).

dv/dt coupled noise

Fig. 7 shows the lumped model of the PCB coil interfaced with a non-inverting integrator circuit [6]. Noise is injected from the switching node of the power device to the PCB coil through parasitic capacitance (C_P). Even though this capacitive coupling is distributed over the entire length of the PCB coil, the coupling is depicted with a lumped capacitance (C_P) in Fig. 7(a) for simplicity.

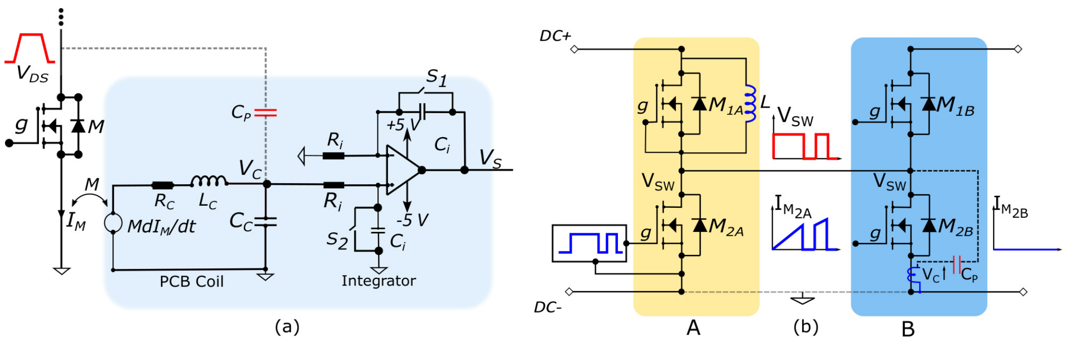

Fig. 7: (a) Coupling of the switch node with the PCB coil through a lumped parasitic capacitance C_P. (b) An experimental scheme to investigate the noise in the coil output due to parasitic coupling with the switch node.

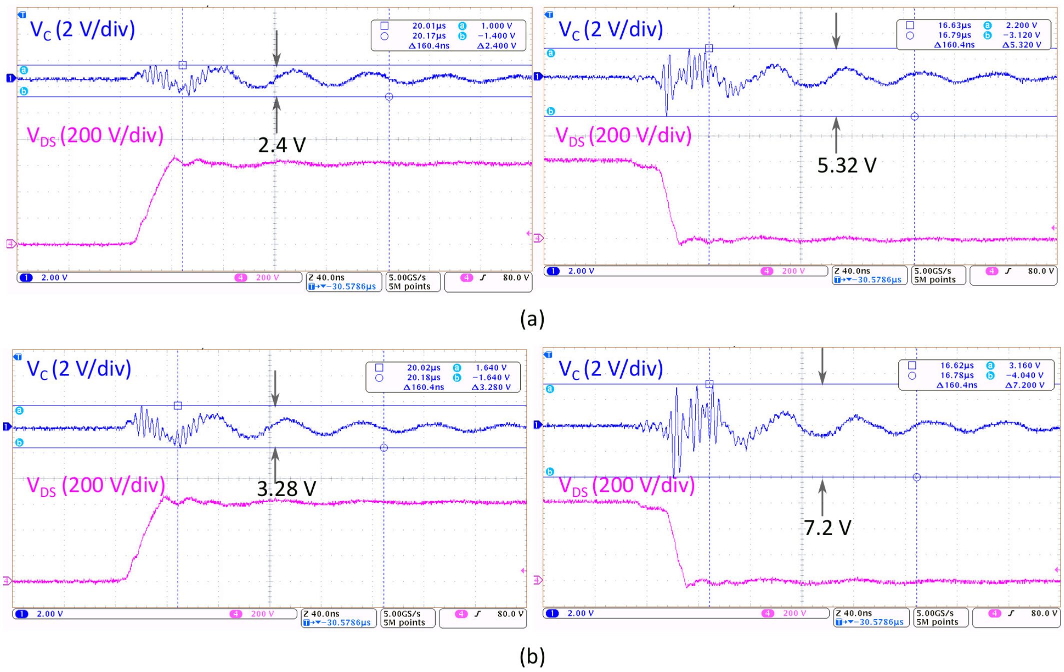

Fig. 8: Coil voltage due to signal injected by the switch node due to parasitic capacitive coupling with the PCB coil for (a) Coil B and (b) Coil A.

Due to to complexity of the parasitic capacitance owing to its distributed nature, dv/dt induced noise on the sensor output is difficult to model analytically [7]. To show the influence of coil structure on the dv/dt noise immunity of the PCB coils, an experimental scheme is shown in Fig. 7(b). The setup consists of two half bridge boards A and B. A pulse test is carried with M_{2A} on board A which causes causes high dv/dt on the switching node of the bridge. Further, the node is connected to the switching node of bare half-bridge board B. Consequently, board B only has a high dv/dt on its switching node and without any switching current through the devices. Since the only coupling the switching node will have with the PCB coils on board B are due to parasitic capacitance between the switching node and the coil, the output voltage of the PCB coil will be due to dv/dt induced noise.

The coil output voltage is measured for both the A and B coil configurations demonstrated earlier in Fig. 2. The experimental results are shown in Fig. 8. Coil A exhibits a higher coupling of the coil with the switch node traces owing to its larger size than coil B. Therefore, not only does a larger coil size increase susceptibility towards external magnetic fields, there is also an increase in the amount of noise coupled on account of parasitic coupling with the switch node traces on the PCB.

Conclusion

Noise immunity of PCB coils used for measuring fast transitioning switch current was investigated in this paper. Based on the theoretical analysis and the experimental investigations, it is inferred that the noise immunity of the coil is dependent on the coil size as well as the proximity of the coil with the current carrying power-trace. Consequently, layout of the coil on the power-board PCB is especially critical towards determining the noise immunity of the PCB pickup coils. Therefore, a proper PCB stack-up specification can be selected for adjusting the proximity of the coils with the power-trace, based on the desired noise immunity of the PCB coil. Moreover, coils with small size and high mutual inductance have better immunity to dv/dt generated noise due to lesser parasitic coupling between the switching node and the PCB coil.

References

[1] D. Gerber, T. Guillod, R. Leutwyler, and J. Biela, "Gate unit with improved short-circuit detection and turn-off capability for 4.5-kv press-pack IGBTs operated at 4-ka pulse current," *IEEE Trans. Plasma Sci.*, vol. 41, no. 10, pp. 2641–2648, Oct 2013.

[2] Y. Kuwabara, K. Wada, J. Guichon, J. Schanen, and J. Roudet, "Implementation and performance of a current sensor for a laminated bus bar," *IEEE Trans. Ind. Appl.*, vol. 54, no. 3, pp. 2579–2587, May 2018.

[3] U.-J. Kim, "Design of a rectangular pickup coil fabricated on a pcb using wbg power semiconductor in discrete package," *Applied Sciences*, vol. 11, no. 5, 2021.

[4] K. Wang, X. Yang, H. Li, L. Wang, and P. Jain, "A high-bandwidth integrated current measurement for detecting switching current of fast GaN devices," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 6199–6210, July 2018.

[5] A. Rafiq, S. Pramanick, and R. Maheshwari, "Design of pcb coil based high bandwidth current sensor with power-loop stray inductance characterization," *IEEE Trans. Ind. Electron.*, pp. 1–1, 2020.

[6] A. Radun, "An alternative low-cost current-sensing scheme for high-current power electronics circuits," *IEEE Trans. Ind. Electron.*, vol. 42, no. 1, pp. 78–84, Feb 1995.

[7] C. Hewson and W. Ray, "The effect of electrostatic screening of rogowski coils designed for wide-bandwidth current measurement in power electronic applications," in *2004 IEEE 35th Annual Power Electronics Specialists Conference (IEEE Cat. No.04CH37551)*, vol. 2, 2004, pp. 1143–1148 Vol.2.