

Dynamic Control of the Switching Behavior of SiC MOSFETs in Converter Operation

Jochen Henn, Laurids Schmitz and Rik W. De Doncker

RWTH Aachen University, Institute for Power Electronics and Electrical Drives (ISEA)

Jaegerstrasse 17-19

Aachen, Germany

Phone: +49 241 80 96920

Fax: +49 241 80 92203

Email: post@isea.rwth-aachen.de

URL: <https://www.isea.rwth-aachen.de>

Acknowledgments

The project on which this report is based was funded by the Federal Ministry of Education and Research under the funding code 16EMO0375. The author is responsible for the content of this publication.

Keywords

«Intelligent gate driver», «EMI/EMC», «Smart Gate Drivers», «Wide Bandgap».

Abstract

This paper presents a control approach to regulate voltage slope and oscillation amplitude in a silicon carbide inverter during operation. Based on sensor measurements, the control adapts the switching characteristics using an adaptive gate driver and thus adjusts the level of voltage slopes, oscillation amplitude and consequently, electromagnetic emissions to a target level.

1 Introduction

In recent years the advantages of wide bandgap (WBG) semiconductor devices became accessible and led to their widespread adaption [1]. Future power electronic converters using WBG semiconductors can use advanced gate driving technologies to mitigate the drawbacks of faster switching devices such as electromagnetic interference (EMI) [2].

Adaptive gate drivers are the basis for dynamic control of the switching behavior. All of the following examples either use a fixed voltage source and adapt the gate resistance or apply a controlled gate current. An array of segmented current sources is fabricated into an application-specific integrated circuit (ASIC) to form an adaptive gate driver in [3]. Instead of current sources, an array of transistors with different $R_{DS,ON}$ can be used as presented in [4] and [5]. For this paper a discrete adaptive current driver as introduced in [6] is used. The results in the literature [7–9] regarding the optimization of the next switching event promise an enhanced operating behavior under the usage of adaptive gate drivers, because they extend the safe operating area (SOA) at equal or less losses.

When adaptive gate drivers are equipped with feedback circuits, they can adapt their gate driving characteristics in order to optimize the operating behavior. Closing the feedback loop while the switching event is still in progress is a challenge for WBG converters and has so far only been achieved for IGBTs [10–12]. In addition to the relatively low bandwidth feedback needed for IGBT based converters, research has shown highly dynamic feedback loops based on current mirrors [13], RC based voltage sensors [14] and load current based adaption [3].

Similar to the goal of this paper, the following publications use feedback loops and adaptive gate drivers to optimize the operating behavior in regard to switching characteristics. In [15] the authors use a dedicated ASIC to drive gallium nitride (GaN) devices at 650 V and adapt a single parameter in between switching events. With a focus on crosstalk suppression, the authors of [9] and [16] use a direct feedback of the active switching event on the gate voltage. These approaches limit the overall flexibility of the gate driver but could be combined with an adaptive driver. Finally, [5] and [17] optimize the switching behavior during converter operation but either lack interpretation of the overshoot amplitude or use external equipment to measure the switching characteristics.

In contrast to the aforementioned work, this paper presents an enhanced PI based control algorithm which allows a dynamic control of different switching characteristics by using discrete on-board sensors and an adaptive gate driver. Thus, first, the setup of the dynamic control loop is presented by giving a description of the utilized sensors and summarizing the applied algorithm. After this the hardware used to validate the dynamic control is introduced. The validation of the algorithm is conducted based on the measurement results presented in the second to last section. Finally, the paper is concluded by summarizing the contributions to dynamic control algorithms.

2 Dynamic Control Loop

To adjust the switching characteristics and therefore the electromagnetic emissions (EME) to a predefined level, the feedback loop depicted in Fig. 1 is introduced.

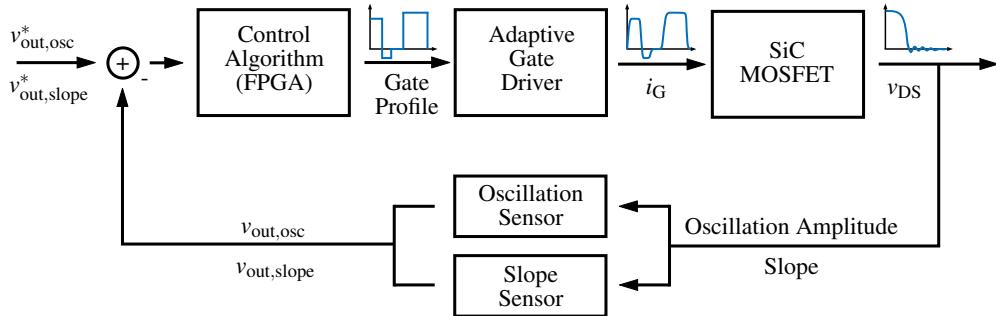


Fig. 1: Structure of the proposed dynamic feedback loop.

It consists of two sensors which measure the slope and the oscillation amplitude of each v_{DS} transition following a switching event. Additionally, the control algorithm runs on the field-programmable gate array (FPGA), which determines the adaptions to the gate profiles based on the sensor measurements. Finally, this results in a change of the switching characteristics of the silicon carbide (SiC) MOSFETs which in turn will be measured by the sensors and used as feedback for the next switching cycle.

The v_{DS} measurement after the activation of the control algorithm, depicted in Fig. 2, illustrates the effect of the control presented in this paper. The algorithm is activated after the fourth falling edge at $t = 150\mu\text{s}$. Consequently, the negative overshoot drops from 121 V to 51 V and the voltage slope decreases from 33.7 V/ns to 28 V/ns according to the preset slope target value. In Fig. 2 the reduction of the negative overshoot is a result of the adapted voltage slope. The effect of the control on the voltage slope is visible in Fig. 6. As a result, the electromagnetic emissions are adapted as well.

Evaluation and Control Algorithm

After each switching event, an adaption of the gate profile is determined by the control algorithm. The adaption of gate profiles is possible in several ways. A gate profile itself is divided into n different states. They are comprised of a reference gate current amplitude a_i and a state duration d_i , where i marks the position in the gate profile, which is depicted in Fig. 3a. The reference gate current amplitude can be positive or negative, depending on the sign of the targeted current value. An amplitude between -31 and +31, which is set by two 5 bit R-2R-ladders within the adaptive gate driver, is related to the desired

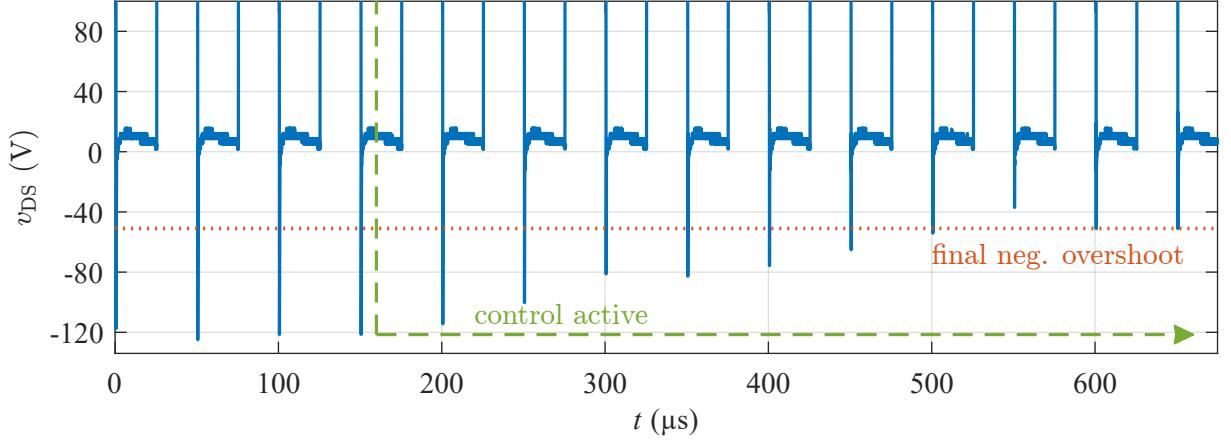
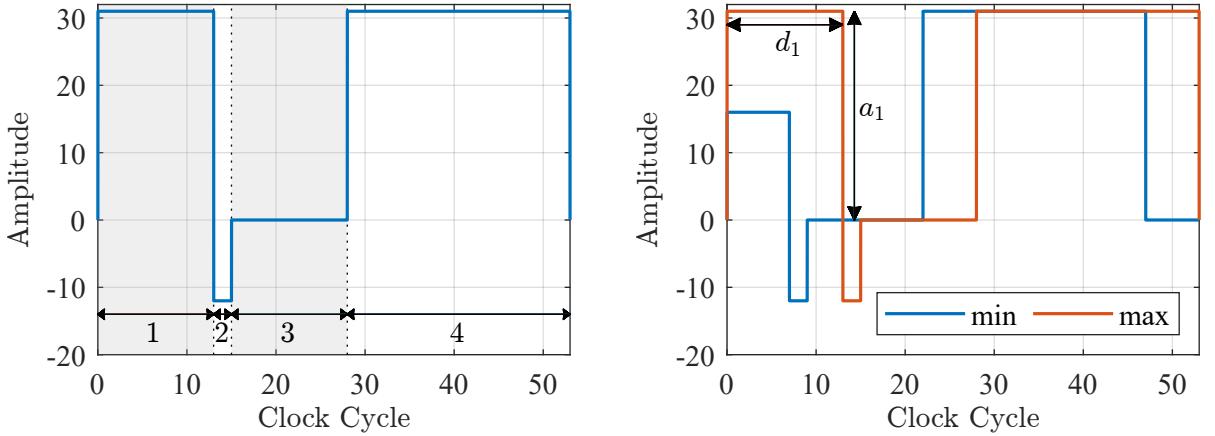


Fig. 2: Negative overshoot of v_{DS} for the first iterations of the control.

maximum turn-off and turn-on gate currents. The resolution of the duration is limited by the length of an FPGA clock cycle of 2.5 ns.

In the standard gate profile in Fig. 3a, the first state with a positive amplitude increases v_{GS} above the threshold voltage. The short second state with a negative amplitude and the longer third state with an amplitude of 0 A are used to maintain a constant level of v_{GS} after the initial charging. Finally, the fourth state is used to guarantee the increase of v_{GS} to its maximum of 15 V at the end of the transition to reduce conduction losses.



(a) Standard turn-on reference current profile used as the default profile when the control is not active.

(b) Minimum and maximum allowed reference current profiles that still ensure proper switching behavior.

Fig. 3: Profile set used for the measurements presented.

Within the set of gate profiles shown in Fig. 3, several parameters are controlled consecutively. For the control presented in this paper, the duration and the amplitude of state 1, d_1 and a_1 , are selected as control parameters. These two parameters allow for fast adaptions of slope and oscillation amplitude of v_{DS} . Adaptions to d_1 lead to quick and coarse changes, while changes of a_1 allow finer adjustments and are used as the secondary parameter. All parameters are limited to a defined range, which is visualized by the minimum and maximum profile in Fig. 3b. The reason for these limitations is that parameter values outside of a certain range may disturb the v_{DS} transition too much or stop it entirely. Furthermore, the synergy between the two consecutively controlled parameters can only be guaranteed within a certain range. The standard reference profile depicted in Fig. 3a is used as the starting point of the algorithm.

The control algorithm on the FPGA compares the sensor analog digital converter (ADC) readout with a provided target value that represents the desired emission level after each v_{DS} transition. The resulting error is processed by a PI element with the resulting PI output value being the main input for the control

algorithm. It is compared to thresholds as visualized in Fig. 4 and as a result, the direction as well as the step size of the adaption are determined.

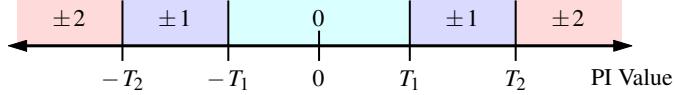


Fig. 4: Control threshold levels used to determine the adaption step size and sign.

If the absolute PI output value is higher than T_1 , the currently controlled parameter is adapted by a step of 1 while it is adapted by 2 if the absolute value is higher than the second threshold level, T_2 . The sign of the adaption step depends on the sign of the PI output value and the configuration for the control parameter.

A parameter is adjusted until one of the following two conditions is met: a) the valid range defined by minimum and maximum profile would be violated by the calculated adaption step, b) the previous adaption step led to an increased error, indicating the local optimum for this parameter is reached. In those cases, the control algorithm continues with adaptions to the following parameter.

Using the proportional and integral gain of the PI element, the characteristics of the control can be adapted to various requirements allowing for a trade-off between speed and accuracy. If there is a need for the adaption of additional control parameters or control thresholds and thus higher adaption step sizes, they can be added to the control algorithm.

Sensor Implementation

Two sensors are designed to measure the slope of the voltage transitions and as the magnitude of the oscillations on v_{DS} to be able to develop an algorithm that can control and limit both emission causes. Both sensors comprise a probe, a filter and a sample & hold element (S&H element) as introduced in [14]. The probe derives a high pass filtered version of v_{DS} , the subsequent filter selects the frequencies needed for the determination of slope and oscillation amplitude, respectively, while the concluding S&H element allows for analog-to-digital conversions by the FPGA. For the slope sensor, a low pass filter with a bandwidth of 65 MHz is selected while the cut-off frequencies of the oscillations sensor's band pass filter are 60 MHz and 100 MHz. These filter bands are designed to offer optimal separation for the used power module at a dc-link voltage of 800 V while allowing detection of all expected slope and oscillation amplitude levels. Nevertheless, due to the proximity of slope- and oscillation-induced spectral components in the frequency domain, a full separation cannot be accomplished. For a dc-link voltage of 400 V used for the measurement presented in this paper, the separation between slope and oscillation amplitude is impaired due to a decrease in the resonant frequency of the switching cell. This results in an increased cross correlation between the two measurement values. Therefore, both sensor measurements can be used interchangeably in this case.

3 Hardware Setup

The hardware used to develop and evaluate the presented control algorithm is depicted in Fig. 5. In the upper right corner in Fig. 5, which depicts the top side of the driver module, the discrete slope sensor elements are located. The oscillation sensor is placed on the bottom side of the gate driver module. Next to the sensor, the current gate driver as introduced in [6] is positioned. The turn-on part of the gate driver is on the top side, while the turn-off part is on the bottom side. The FPGA that evaluates the sensor readouts and controls the adaptive gate driver is situated in the center. As basis for the control algorithm the ADCs integrated into the FPGA are used. They can be sampled at a resolution of 12 bit and a sample rate of 1 MHz. With a base clock frequency of 100 MHz, the FPGA can complete the feedback evaluation and adaption of the profiles in roughly 500 ns. Thus, the evaluation and control algorithm needs at least 1.5 μ s between two switching events.

Six of these driver modules are connected between a low-voltage controller Board and a high-voltage

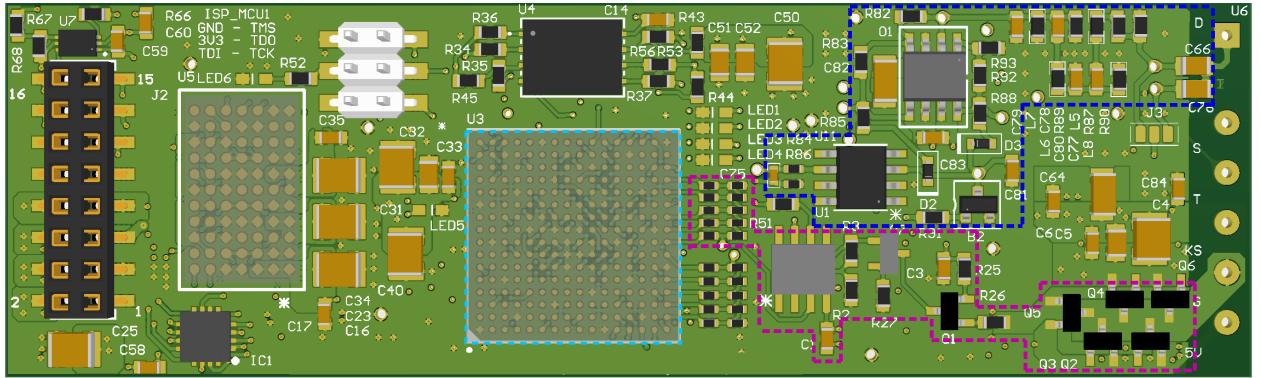


Fig. 5: Top view of a driver module printed circuit board (PCB). It contains an FPGA (marked with light blue), an adaptive current gate driver (marked with purple) and the slope sensor above the driver (blue).

PCB containing the switching cell and the dc-link. Together they operate as a three phase inverter using the 21 mΩ variant of the 1200 V SiC MOSFETs manufactured by Wolfspeed (C3M0021120K).

4 Measurement Results

Measurements are taken at 400 V without any load connected to the inverter. In this synthetic operating point, the switching slopes are fast and consistent over time, which allows better analysis of the effects of the control algorithm on the switching behavior. The goal for the control algorithm in this scenario was to reach and hold a target value of 90 for the slope sensor's feedback. The 8 MSB of the sensor ADC readouts are evaluated resulting in a range from 0 to 255.

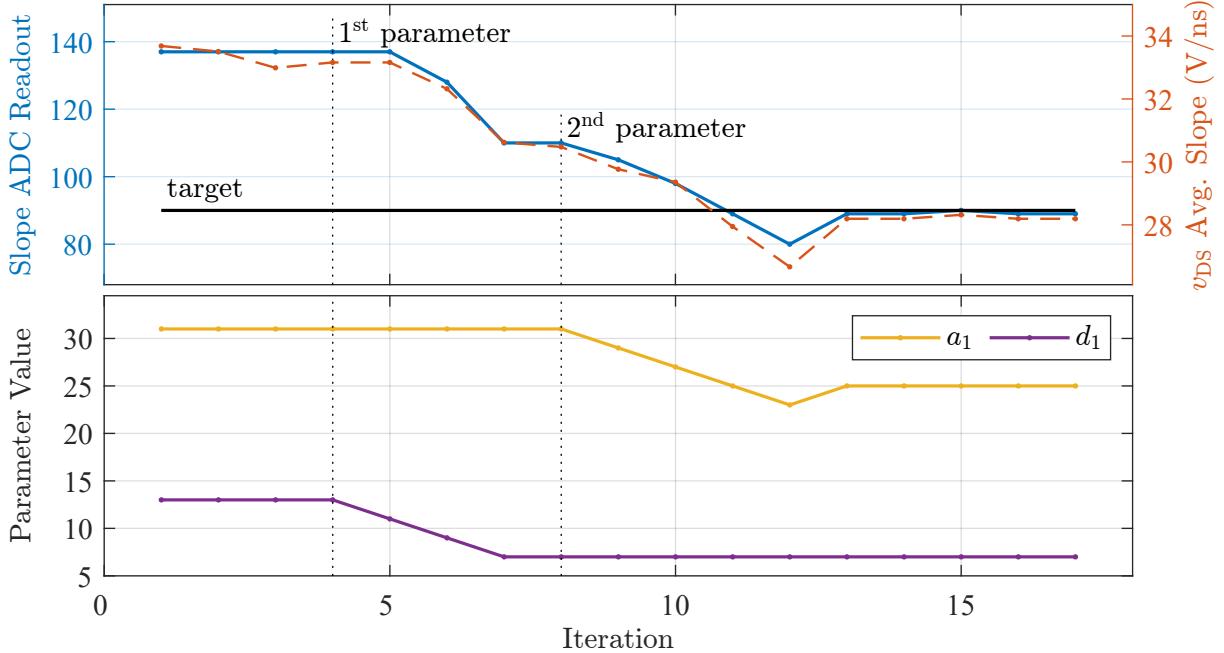
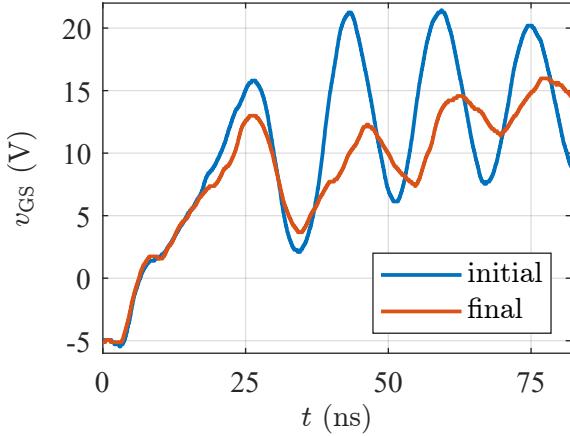
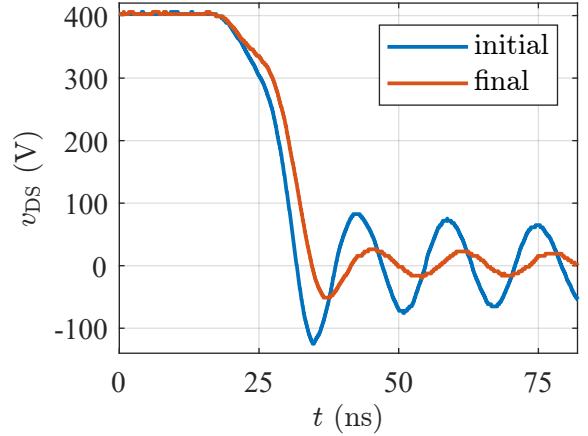


Fig. 6: Control sequence to reduce the voltage slope using two parameters.

Figure 6 visualizes the slope sensor's ADC readout and the change in the control parameter values as a reaction of the control algorithm. Additionally, the average slope values as they can be calculated from an oscilloscope measurement are plotted into the top graph. They show a very similar behavior and were exclusively used to validate the sensors. The control algorithm relies only on the sensor values gathered on the PCB itself. The control is initiated at iteration 4 and the first parameter is decreased because the



(a) v_{GS} for initial and final iteration.



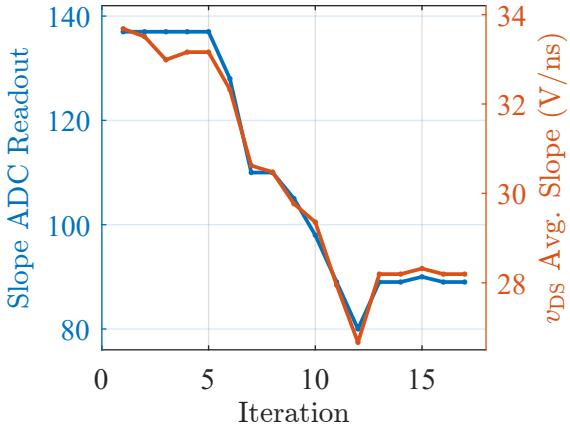
(b) v_{DS} for initial and final iteration.

Fig. 7: Comparison of v_{GS} and v_{DS} waveforms of initial and final control iteration.

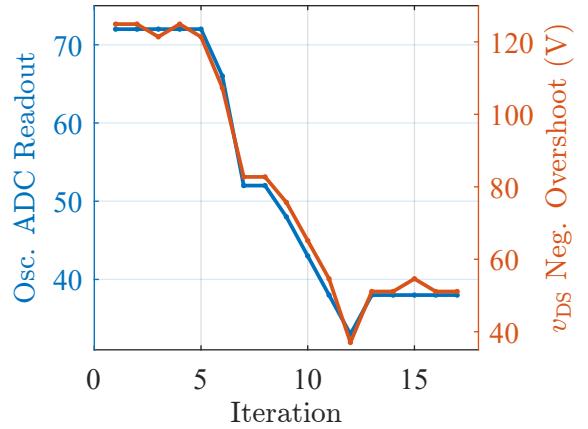
target value is lower than the input from the ADC. After three iterations the target value is not reached, but the duration parameter hit its lower limit and the secondary parameter is chosen to be adapted next. At iteration 12 the control causes a negative overshoot below the target value, which is detected and reversed in the next iteration. One way of reducing this negative overshoot in the control would be to decrease the integral gain at the cost of a slower approach to the target value.

The effect of using coarse changes on the primary parameter is visible in Fig. 6. According to the internal thresholds and Fig. 1 parameter d_1 is decreased by two counts at iterations five and six, because the sensor feedback is still far from the target. For these two steps the error is reduced by 57 %. Decreasing a_1 as the second parameter results in finer adjustments, because the amplitude's influence on the switching event is not as severe. The three adaptions at iteration eight to ten reduce the error by the remaining 43 % relative to the initial error.

Figure 7 depicts the initial and final voltage waveforms for v_{GS} and v_{DS} . The v_{DS} measurements for the initial and final iteration are also visible in Fig. 2 at $t = 150\mu s$ and $t = 650\mu s$. At $t = 20\text{ ns}$ in Fig. 7a the difference in the gate profiles is visible. After reaching the threshold voltage the gate charges slower, which results in a decreased slope and overshoot on v_{DS} .



(a) Slope ADC readouts in comparison to average 90 % to 10 % slope during control.



(b) Oscillation ADC readouts in comparison to maximum negative overshoot during control.

Fig. 8: ADC readouts in direct comparison with oscilloscope measurements.

The direct comparison between the sensor readings and the data gathered from oscilloscope measurements in Fig. 8 indicates very similar behavior for both sensors but also shows differences, which will be addressed here. The biggest difference between the sensors readings and measurements is the relative

Table I: Comparison of relative changes in slope and overshoot characteristics between sensor readings and oscilloscope measurements.

	Slope	Overshoot Amplitude
Change in Oscilloscope Measurement	17 %	57 %
Change in Sensor Reading	35 %	47 %

scaling of the results. Table I contains the relative changes between the initial and final switching characteristics. Although there is a substantial relative difference between the slope sensor and the external measurement, they show a linear dependency as shown by the matching waveforms in Fig. 8a. Additionally, the oscilloscope measurements of both characteristics, the slope and the overshoot amplitude, show more noise during the first four switching iterations. This is caused by resolution limitations in the oscilloscope and the influence of disturbances onto the measurement probe. As mentioned above, during these first iterations the control is inactive and the gate driver applies the standard gate profile. The constant sensor readout during these switching instances underlines the advantage of placing the sensors and their ADCs on the same reference potential and close to the semiconductor devices. Furthermore, the control algorithm benefits from the robust and clean input.

5 Conclusion

In this paper, a feedback loop that allows the control of switching characteristics in a SiC inverter has been successfully developed. The control is based on two sensors, a slope and an oscillation sensor, that allow the independent evaluation of slope and oscillation amplitude of the drain-source voltage in an inverter. In order to adjust the level of the electromagnetic emissions, the control algorithm that runs on an FPGA is able to incrementally adapt different parameters of the gate profile of the SiC-MOSFETs based on the feedback of the sensors. An enhanced PI-based control algorithm allows closing the feedback loop and controlling the emission level during the operation of the inverter solely based on the feedback from the onboard sensors. Hence, it can operate autonomously and does not need additional information. Moreover, this approach offers the advantage that it can counteract external error sources such as temperature changes and aging effects, which cannot be covered by a feed-forward control. Measurement results at 400 V validate the algorithm's ability to iteratively adjust parameters within the gate profiles to decrease both causes of emissions, slope and oscillation amplitude, from switching event to switching event.

References

- [1] A. Elasser and T. Chow, “Silicon carbide benefits and advantages for power electronics circuits and systems,” *Proceedings of the IEEE*, vol. 90, pp. 969–986, 2002.
- [2] J. Henn, C. Lüdecke, M. Laumen, S. Beushausen, S. Kalker, C. H. van der Broeck, G. Engelmann, and R. W. de Doncker, “Intelligent gate drivers for future power converters,” *IEEE Transactions on Power Electronics*, vol. 37, no. 3, pp. 3484–3503, Mar. 2022.
- [3] S. Kawai, T. Ueno, H. Ishihara, S. Takaya, K. Miyazaki, and K. Onizuka, “A 1ns-resolution load adaptive digital gate driver ic with integrated 500ksps adc for drive pattern selection and functional safety targeting dependable sic application.” Vancouver, BC, Canada: IEEE, 2021, pp. 5417–5421.
- [4] Y. S. Cheng, D. Yamaguchi, T. Mannen, K. Wada, T. Sai, K. Miyazaki, M. Takamiya, and T. Sakurai, “Digital active gate drive with optimal switching patterns to adapt to sinusoidal output current in a full bridge inverter circuit,” in *Proc. IECON 2019 - 45th Annual Conf. of the IEEE Industrial Electronics Society*, vol. 1, Oct. 2019, pp. 1684–1689.
- [5] D. Yamaguchi, Y. S. Cheng, T. Mannen, H. Obara, K. Wada, T. Sai, M. Takamiya, and T. Sakurai, “An optimization method of a digital active gate driver under continuous switching operation being

capable of suppressing surge voltage and power loss in pwm inverters,” *IEEE Transactions on Industry Applications*, vol. PP, pp. 1–1, 2021.

- [6] J. Henn, L. Heine, and R. W. De Doncker, “A high bandwidth active sic gate driver for dynamic adjustment of electromagnetic emissions in electric vehicles,” in *PCIM Europe digital days 2020; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*. VDE, 2020, pp. 1–7.
- [7] Z. Li, R. W. Maier, and M.-M. Bakran, “Mitigating drain source voltage oscillation with low switching losses for SiC power MOSFETs using FPGA-controlled active gate driver,” in *2020 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe)*. IEEE, sep 2020.
- [8] E. Raviola and F. Fiori, “Experimental investigations on the tuning of active gate drivers under load current variations,” in *2021 International Conference on Applied Electronics (AE)*, 2021, pp. 1–4.
- [9] T. Shao, T. Q. Zheng, H. Li, J. Liu, Z. Li, B. Huang, and Z. Qiu, “The active gate drive based on negative feedback mechanism for fast switching and crosstalk suppression of sic devices,” *IEEE Transactions on Power Electronics*, vol. PP, pp. 1–1, 2021.
- [10] Y. Lobsiger and J. W. Kolar, “Closed-loop di/dt and dv/dt igit gate driver,” *IEEE Transactions on Power Electronics*, vol. 30, no. 6, pp. 3402–3417, 2014.
- [11] L. Chen and F. Z. Peng, “Closed-loop gate drive for high power igitbs,” in *2009 Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition*. IEEE, 2009, pp. 1331–1337.
- [12] S. Beushausen, F. Herzog, and R. W. De Doncker, “Gan-based active gate-drive unit with closed-loop du/dt -control for igitbs in medium-voltage applications,” in *PCIM Europe digital days 2020; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, July 2020, pp. 1–8.
- [13] P. Bau, M. Cousineau, B. Cougo, F. Richardeau, and N. Rouger, “Modeling and design of high bandwidth feedback loop for dv/dt control in cmos agd for gan,” in *2020 32nd International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, Sep. 2020, pp. 106–109.
- [14] J. Henn, C. Fronczeck, and R. W. De Doncker, “Design of sensors for real-time active electromagnetic-emission control in sic traction inverters,” in *International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM Europe)*. VDE, 5 2021.
- [15] P. Bau, M. Cousineau, B. Cougo, F. Richardeau, and N. Rouger, “Cmos active gate driver for closed-loop dv/dt control of gan transistors,” *IEEE Transactions on Power Electronics*, vol. 35, no. 12, pp. 13 322–13 332, Dec 2020.
- [16] H. Li, Z. Qiu, T. Shao, Y. Zeng, H. Du, and C. Yin, “A low level-clamped active gate driver for crosstalk suppression of sic mosfet based on dv/dt detection.” Vancouver, BC, Canada: IEEE, 2021, pp. 5348–5353.
- [17] Z. Wu, H. Jiang, Z. Zheng, X. Qi, H. Mao, L. Liu, and L. Ran, “Dynamic dv/dt control strategy of sic mosfet for switching loss reduction in the operational power range,” *IEEE Transactions on Power Electronics*, vol. PP, pp. 1–1, 2021.