EMI Mitigation Induced by An IGBT Driver Based on A Controlled Gate Current Profile

Daniel S. Martinez-Padron[1], Nicolas Patin[1], Eric Monmasson[2]
[1] Université de technologie de Compiègne,
Roberval (Mechanics, energy and electricity)
Centre de recherche Royallieu CS 60319-60203
Compiègne Cedex - France
[2]SATIE laboratory, CY Cergy Paris Université
Cergy-Pontoise, France
Phone: +33 (0)-3 234727
Email: dmartine@utc.fr; nicolas.patin@utc.fr; eric.monmasson@cyu.fr

Acknowledgments

The authors would like to thank The National Council of Science and Technology of Mexico (CONACyT) for the academic scholarship under the grant number 705759.

Keywords

≪Gate driver≫, ≪IGBT≫, ≪Electromagnetic interference (EMI)≫, ≪Switching losses≫, ≪EMI/EMC≫.

Abstract

The transistors used in power electronics applications are source of electromagnetic interference(EMI) during switching process. In this work a gate current profile to reduce conducted EMI is proposed. It is based on the gate charge curve and it allows to control the conducted EMI generation with two degrees of freedom. In order to evaluate the performance of proposed method, it is compared with a validated method in the literature, namely, CATS method. It is shown that, for the same level of power switching losses, the conducted EMI generation is less with the proposed method.

1 Introduction

In last decades, power transistors such as field-effect transistor (MOSFET) and insulated gate bipolar transistor (IGBT) have been widely used in industrial and consumer electronics applications. They are suitable devices due to their capability to handle high currents at high switching frequencies. However, they are source of electromagnetic interference(EMI) during switching since the high levels of dI/dt and dV/dt are sources of radiated and conducted EMI, which affects normal operation of surrounding equipment [1]. The EMI generation and power losses are strongly related, since the switching losses occur during the overlap of non-zero voltage and current. Low switching losses implies short switching time but at the same time it increases the EMI levels. For this reason, a suitable transistor driver has to guarantee an adequate trade-off between power losses and EMI. In order to address this problem, several driving methods have been proposed in the literature. For instance, control the voltage fall injecting gate current during turn-on transistor and during turn-off, changing the gate resistance value to satisfy the EMI requirements is proposed in [3] and [2] to obtain an acceptable trade-off between switching speed and EMI. This driving method is improved in [4] in turn-off process to avoid spurious turn-on on IGBT by applying a negative bias. A driving method based on a closed-loop approach is presented in [6][7]. In [7], a closed loop gate driver is reported that feedbacks the voltage, and as consequence

its slope measure, and controls the voltage and current transients by the gate current. In the same way, in [6] a closed loop IGBT driver is proposed. It feedbacks the voltage and current transient to shape them into smoothest waveforms with a PI controller. Driving method called CATS is proposed in [10] to reduce the EMI generation smoothing dV/dt and dI/dt waveform applying an intermediate gate voltage level. (In french: *Commande Autour de la Tension de Seuil*, that could be translated by "Control around the Threshold Voltage"). In this sense, an active voltage control is reported in [12] to shape the dV/dt of an IGBT. The EMI reduction is achieved with an "S"-shaped waveform that has smooth corners. It is reported that the high order time derivatives of dV/dt and dI/dt waveform can reduce the EMI generation [13] and it is theoretically proved in [14] that a Gaussian shape switching pattern ensure the optimal trade-off between power losses and EMI generation. Most of the proposed methods are based on gate charge approach reported in[19]. However they don't consider the non-linear behaviour during the Miller's Plateau 'knee', which occurs during the interval between the end of the dI/dt and the beginning of dV/dt. Recently, in [15, 16, 17, 18] drivers based on gate current with a fine resolution haven been proposed. They allow to shape the transient waveform injecting steps of current during gate charge. However, there is not a systematic method to choose the level and the duration of the steps. For these reasons, a driving method based on a gate current profile is proposed. It consists on applying a gate current profile formed by steps that is based on the gate charge curve [19] and it allows to shape the voltage and its derivative to reduce the conducted EMI. In order to evaluate its performance, the proposed method is compared with a previously evoked methodology, namely, CATS because it is an effective strategy validated in practice that can serve as reference. Additionally, a benchmark which considers the switching power losses and the frequency response as two performance criteria is also proposed. The article is organized as follows: Section 2 describes the proposed methodology and the proposed gate profile. In section 3, the benchmark and the comparison between CATS and the proposed method are described. Finally in Section 4 conclusions are drawn.

2 Proposed methodology

In power electronics, the high levels of dV/dt and dI/dt during switching are sources of conducted and radiated EMI. Slowing down the switching duration can reduce the EMI generation but it tends to increase the power losses. As mentioned previously, smoothing the transients waveform can improve the trade-off between EMI and switching losses. For insulated gate transistors, such as MOSFET and IGBT, switching transient waveforms are strongly related to the charge supplied to gate input capacitance and the switching behaviour can obtained from gate charge curve. In order to shape the voltage/current transient waveform and reduce the EMI generation, a driving method based on a gate current profile is proposed. The method consists of injecting different current levels during gate charging. In order to describe the proposed method, the transistor gate charge is detailed in the following paragraph.

Transistor gate charge

The gate charging behaviour of insulated gate power transistors, as IGBT and MOSFET, determines the shape and duration of dV/dt and dI/dt and consequently the EMI generation. This behaviour is caused by transistor internal structure, the internal capacitances, the wiring resistance and inductance, the gate resistor, the collector voltage and current, load current, among others. The internal capacitances are the main elements involved in this process and the complexity of this mechanism is due to their non linear behaviour. The gate charging dynamics can be simplified considering that it is conformed by different values during gate charging shown in Fig. 1. The V_{ge} vs charge curve is obtained by injecting a constant current into the gate and it can be split in several stages. In Fig. 2 (a) a typical test circuit with an IGBT and their internal capacitances is presented. Injecting a constant current in the gate it is possible to obtain the dynamic curve shown in Fig. 2 (b) which presents the turn-on behaviour by gate charge. This dynamic curve can be divided in 5 stages, influenced by the different gate charge values, that are described below

- **Stage 1**. Before the gate voltage V_g reaches the threshold voltage V_{th} the collector current I_c is strongly limited (only few μA). The slope of V_g is fixed by the gate-emitter capacitance C_{ge}.

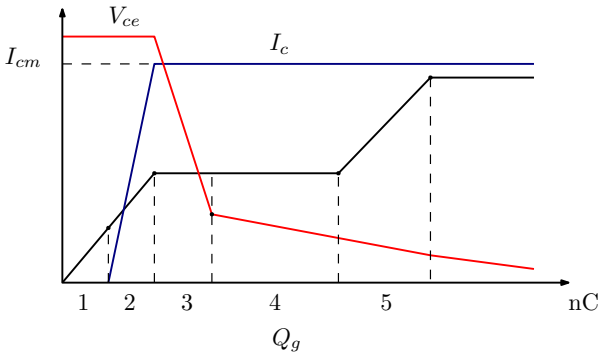

Fig. 1: Gate charge curve.

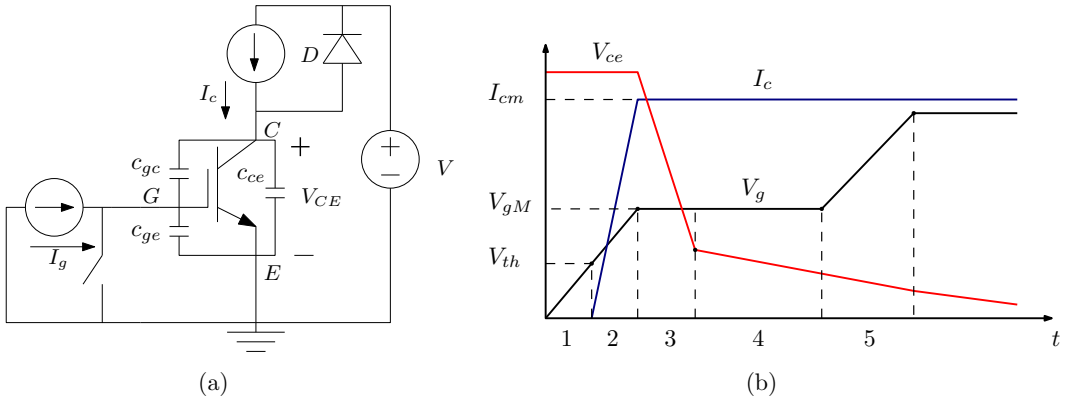

Fig. 2: (a) Test circuit and (b) dynamic charge during a turn-on transient.

- **Stage 2.** Once V_{gth} is reached, the device is turned-on and the collector current flows reaching its maximum value I_{cm}, while the collector voltage V_{ce} remains unchanged at its maximum value. V_g reaches the Miller's plateau voltage V_{gM}.
- **Stage 3 and 4.** During this stage the Miller effects starts, the input appears to be infinite since the V_g remains equal to V_{gM} even though the gate circuit is supplying current to the gate. V_{ce} starts dropping with different slopes determined by the charges of Miller's capacitance [19]. During the Miller's plateau, remains due the non linear gate-collector capacitance C_{gc} (Miller's capacitance).
- **Stage 5.** As soon as the Miller's effect ends, V_g starts to increase again towards its final value.

Proposed gate current profile

As presented before, the switching transient behaviour of insulated gate transistors is determined by the gate charge supplied. The total charge is the same during switching and it can be controlled by the gate current amplitude and duration. These parameters allow to control the duration and waveform of the transient, and at the same time the EMI generation and power switching losses. In this sense, a driving method to reduce the EMI generation based on the gate charge curve is proposed in this article. The proposed method consists of injecting a current step profile (CSP) to control the voltage transient switching and, consequently, to reduce the conducted EMI. The proposed CSP is shown in Fig. 3 and it is formed by 4 steps I_j with $1 \leq j \leq 4$. Notice that this kind of profile can be implemented using the drivers presented in [15, 16, 17, 18]. Each step of CSP allows to control the behaviour of switching transient by their amplitude and duration. In this article the duration is fixed and the amplitude step is calculated with the correspondent equations of each stages from the dynamic curve presented in Fig. 2. The procedure to calculate the amplitude of each step of CSP is described as follows.

- **Step 1**. This step is a mixture of stage 1 and 2 in gate charge curve. During stage 1, the V_{th} is reached. The gate current is determined by the charge for C_{ge} then

$$I_{g1} = C_{ge}\frac{dV_{ge}}{dt} \approx C_{ge}\frac{V_{th}}{\Delta t_{s1}}, \tag{1}$$

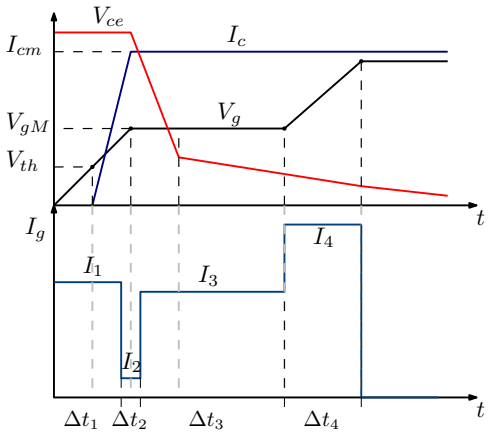

Fig. 3: Current step profile proposed.

where I_{g1} is the gate current for Stage 1, Δt_{s1} is the time that V_{ge} takes to reach V_{gth}. During stage 2, I_c increases until I_{cm} during Δt_{s2} and C_{gc} is charged by the current

$$I = C_{gc}\frac{dV_{gc}}{dt}. \tag{2}$$

Considering that $V_{ge} = V_{ge} - V_{ce}$, V_{ce} remains constant and the transconductance of the IGBT is $g_m = \Delta I_c/\Delta V_{ge}$, the gate current can be calculated by

$$I_{g2} = \frac{C_{ies}}{g_m}\frac{dI_c}{dt} \approx \frac{C_{ies}}{g_m}\frac{\Delta I_c}{\Delta t_{s2}}, \tag{3}$$

where I_{g2} is the gate current for Stage 2. Taking $I_1 = I_{g1} = I_{g2}$, then step 1 duration can be calculated from equations (1) and (6) and $\Delta t_1 = \Delta t_{s1} + \Delta t_{s2}$.

- **Step 2**. This step considers the end of stage 2 and the beginning of stage 3, during V_{ce} and I_c intersection and the 'knee' of Miller's Plateau [19]. Due to the non linear behaviour of the input capacitance [19] and the effect of the diode recovery, a low step I_2 amplitude is proposed.
- **Step 3**. During this step, the dV/dt is controlled. From stage 3, the gate current can be estimated by

$$I_3 = C_{gc}\frac{dV_{ce}}{dt} \approx C_{gc}\frac{\Delta V_{ce}}{\Delta t_3}. \tag{4}$$

Then, fixing Δt_3, which corresponds to the step I_3 duration, the dV/dt can be controlled by step I_3 amplitude. The duration of step current I_3 is selected by trial and error test.

- **Step 4**. In order to finish the gate charge, the amplitude of the step I_4 is calculated using (1) considering the equivalent capacitance during this time.

Proposed method evaluation

In order to verify the effectiveness of CSP, it is evaluated in the test circuit shown in Fig. 4. The evaluation is performed by simulation using Ltspice software and the IGBT IKW40N65ET7 SPICE model [21]. The evaluation consists on injecting the CSP and varying the amplitude of I_3, which shape the voltage waveform, to evaluate the impact of amplitude value on conducted EMI generation and power losses. The I_3 amplitude values chosen in this evaluation are: $I_3 = 10mA$, $I_3 = 20mA$, $I_3 = 30mA$, $I_3 = 40mA$ and $I_3 = 50mA$. The simulations are performed with a minimal step simulation of 100 ps and the parameters in Tab. I. The selection of the steps of the proposed profile is described as follows.

- **Step 1**. First, considering the value of V_{th} and C_{ies} shown in Tab.Iand proposing $t_{s1} = 1\mu s$, the

Table I: Simulation Parameters

Parameter	Value
Input capacitance (C_{ies})	2.475 nF
Reverse transfer capacitance (C_{res})	25pF
Switching period (T)	50ns
Transconductance (g_m)	10.25 S
Threshold voltage (V_{th})	5.8 V
Collector voltage (V)	130 V
Collector current (I_c)	40 A

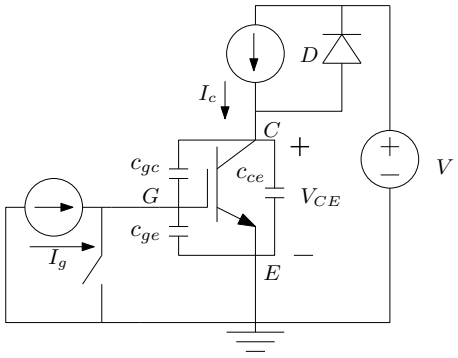

Fig. 4: Test circuit for the CSP evaluation.

current gate to reach the V_{th} can be calculated by

$$I_1 = C_{ies}\frac{V_{th}}{\Delta t_{s1}} = 14.32mA. \tag{5}$$

For the second part, the maximum collector current I_{cm}=40 A. In order to slowdown the current slope during Miller plateau, it is proposed reach 80% of I_{cm} during this step. Since $I_1 = 14.32mA$, the duration of this part is given by

$$\Delta t_{s2} = \frac{C_{ies}}{g_m}\frac{\Delta I_c}{I_1} = 538.49ns. \tag{6}$$

In this sense, the step 1 amplitude is $I_1 = 14.32mA$ with a time duration of $\Delta t_1 = 1.538\mu s$.

- **Step 2**. For this step, in order to finish the current slope and start the 'knee' of Miller's Plateau, a low step I_2 amplitude is proposed. In this case $I_2 = 1.5mA$ is selected and the value of C_{ies} estimated is $250pF$, then the time duration is calculated by

$$\Delta t_2 = \frac{C_{ies}}{g_m}\frac{\Delta I_c}{I_2} = 200ns. \tag{7}$$

The step 2 amplitude is $I_2 = 1.5mA$ with a time duration of $\Delta t_2 = 200ns$.

- **Step 3**. For this step, five different values are selected: $I_3 = 10mA$, $I_3 = 20mA$, $I_3 = 30mA$, $I_3 = 40mA$ and $I_3 = 50mA$. The time duration is set to $\Delta t_3 = 500ns$ for all cases.
- **Step 4**. In order to finish the gate charge, the time duration $\Delta t_4 = 500ns$ is proposed, the capacitance estimated from datasheet gate charge curve is $C = 18nF$ and the amplitude of the step 4 is calculated by

$$I_4 = C\frac{\Delta V}{\Delta t_4} = 0.204A. \tag{8}$$

Then, the step 4 amplitude is $I_4 = 0.204mA$ with a time duration of $\Delta t_4 = 500ns$.
The obtained results, shown in Fig. 5 and Fig. 6, present the V_{ce} waveform during falling and rising edge at different amplitude of I_3 respectively. Additionally, the frequency spectra of each test are presented in Fig. 7 that shows their EMI generation can be reduced by reducing the amplitude of I_3 that can be used as degree of freedom to improve the conducted EMI requirements. However, as shown in Tab.II the power losses increase when the EMI generation is reduced.

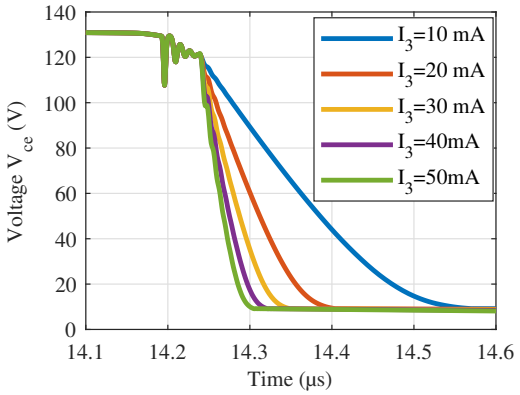

Fig. 5: Simulation results for falling edge.

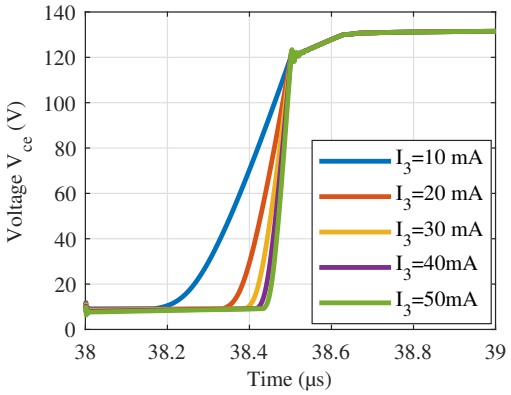

Fig. 6: Simulation results for rising edge.

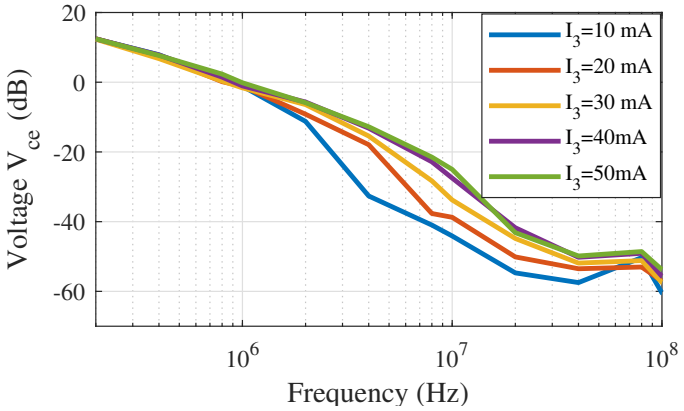

Fig. 7: Frequency spectra at different levels of I_3.

Table II: Power losses for different level of I_3

I_3 **amplitude**	**Power losses** P_{sw}
10 mA	114.37 W
20 mA	103.14 W
30 mA	99.10 W
40 mA	96.87 W
50 mA	95.37 W

3 Comparison

The performance of the CSP is evaluated by a comparison with an effective method reported in the literature. For this purpose, CATS methodology is chosen as a reference and it is described as follows.

CATS methodology

CATS methodology is proposed in [10] and it consists in reducing the dI/dt and dV/dt by introducing an intermediate gate voltage level close to the threshold voltage V_{th}. During turn-on, an intermediate voltage $V_{th} < V_{int} < V_g$ is injected during T_{int} unlike classical driving as shown in Fig. 8(a). During turn-

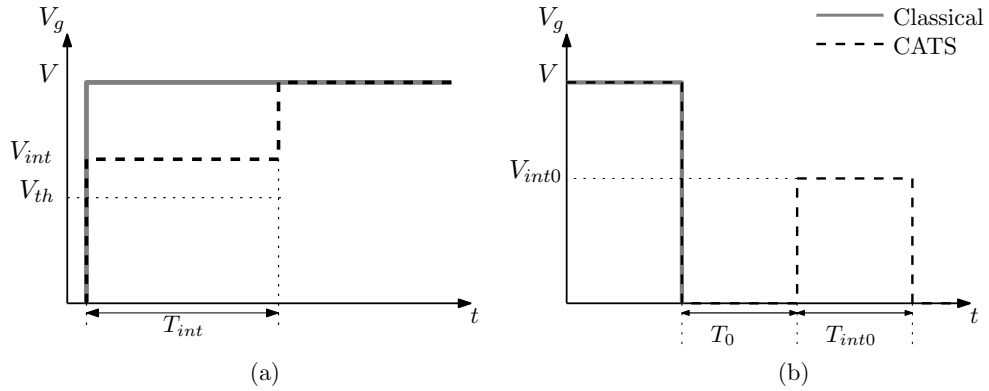

Fig. 8: Operating principle of CATS: (a) Turn-on and (b)Turn-off.

off, a zero or negative voltage is forced to evacuate the excess of charges, which maintain the transistor in conduction during a time interval T_o. Then a second level $V_{int0} < V_{int}$ is injected during T_{int0} [11] as shown in Fig. 8(b).

Benchmark

In order to perform an adequate comparison between the CSP and CATS methods, an appropriate benchmark has to be established. Since, the relationship between the power losses and EMI is an important issue, a benchmark test is proposed with the following considerations:

- The analysis frequency bandwidth considered is 200 kHz to 20 MHz because it is the typical range of propagation of conducted EMI [20].
- The switching power losses are fixed to the same value for both strategies and they are calculated as reported in the transistor datasheet [21] as:

    1. For turn-on, the switching power losses are measured during the time interval between 10 % of V_{ge} and 2% of V_{ce}.
    2. For turn-off, the switching power losses are measured during the time interval between 90 % of V_{ge} and 2% of I_c.

- The switching duration is proposed to achieve V_{ge}=15V and ensure the IGBT saturation.

Results

The comparison is performed using the proposed benchmark and the test circuit shown in Fig. 9 with the IGBT IKW40N65ET7 [21]. The transistor parameters are

- C_{ies}=2.475 nF,
- C_{res} = 25pF,
- g_m= 10.25 S,

and the following parameters are taken into account

- V=130 V,
- f_{sw}=20 kHz,
- I_c=40 A.

The comparison consists of determine the EMI generation performance of CSP and CATS methodology at the same level of switching power losses. Three different levels of power losses are chosen: $P_{sw} = 90W$, $P_{sw} = 93W$ and $P_{sw} = 99W$. The comparison is performed with Ltspice software considering a maximum simulation step of 100 ps. For CATS methodology the parameters T_{int}, V_{int0}, T_0 are fixed and V_{int} is chosen as degree of freedom with the following values

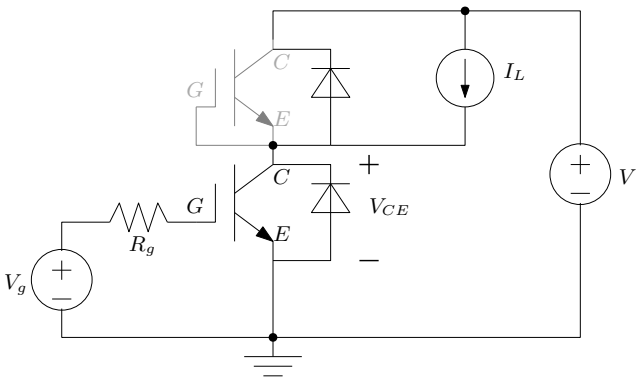

Fig. 9: Test circuit for the comparison.

- $T_{int} = 2\mu$ ns,
- $V_{int0} = 625$ns,
- $T_0 = 1.875\mu s$,
- $V_{int} = 7.5V$ for $P_{sw} = 90W$,
- $V_{int} = 7.53V$ for $P_{sw} = 93W$,
- $V_{int} = 7.605V$ for $P_{sw} = 99W$.

For the CSP, the source V_g in Fig. 9 is replaced by a current source $I_g(t)$ and the step I_3 becomes the degree of freedom to vary the switching power losses. The CSP is formed by

- $I_1 = 14.32$ mA and $\Delta t_1 = 1.538\mu s$,
- $I_2 = 1.5$ mA and $\Delta t_2 = 200ns$,
- $I_3 = 60$ mA and $\Delta t_3 = 150ns$ for $P_{sw} = 90W$,
- $I_3 = 40$ mA and $\Delta t_3 = 76ns$ for $P_{sw} = 93W$,
- $I_3 = 20$ mA and $\Delta t_3 = 50.85ns$ for $P_{sw} = 99W$,
- $I_4 = 0.204$ mA and $\Delta t_4 = 650ns$.

For both methods the gate voltage is V_{ge}=15V which implies a gate charge of $Q_G = 228$ nC. The comparison results are presented in Fig. 10, Fig. 11 and Fig. 12. They show the frequency spectra envelope of CSP and CATS for the different level of switching power losses. The CSP has the lowest response after 10 MHz for the three cases. The average difference between the two methodologies in the frequency band of 10 MHz to 20 MHz is 7.51 dBV for $P_{sw} = 90W$, 12.02 dBV for $P_{sw} = 93W$ and 23.32 dBV for $P_{sw} = 99W$. It implies an interesting reduction of conducted EMI at the same level of power losses.

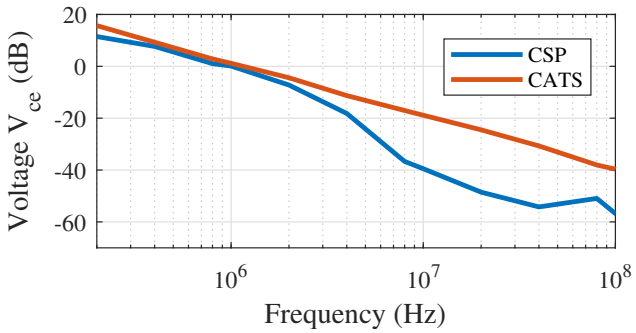

Fig. 10: Result of the comparison at $P_{sw} = 99W$.

4 Conclusion

In this paper, an IGBT driving technique based on a gate current profile is presented. Its aim is the mitigation of conducted EMI under switching losses constraints. the proposed CSP allows us to control the dV_{ce}/dt by a step current amplitude and its time duration. The CSP performance is evaluated by

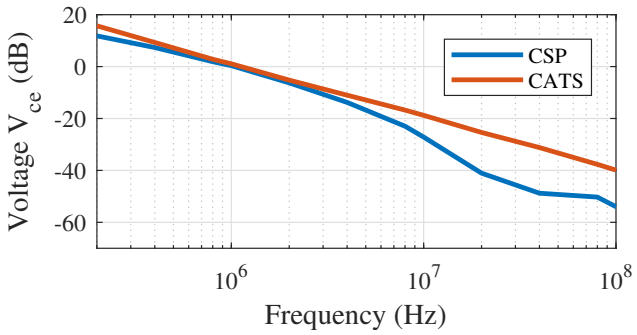

Fig. 11: Result of the comparison at $P_{sw} = 93W$.

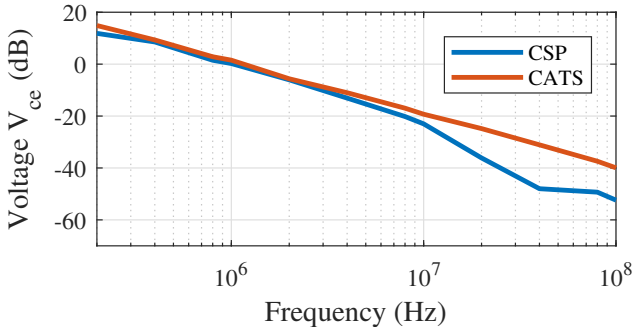

Fig. 12: Result of the comparison at $P_{sw} = 90W$.

simulation with different levels of I_3 that shows the feasibility of the method of reducing the generation of EMI. This method is compared with a reference control scheme (CATS) and simulation results show that for the same switching losses, in three different cases, the CSP exhibits the lowest level in the frequency domain which implies that is generates less conducted EMI. A disadvantage of proposed method with respect to methods such as CATS, is that it is necessary to know some transistor parameters which made more complicated its implementation. An advantage is that the CSP is a systematic method that allows control the conducted EMI generation with two different degrees of freedom. This leads to the possibility of split the step 3 into several levels to shape voltage transient to get a more sophisticated waveform, for instance, Gaussian waveform to ensure the optimal trade-off between EMI and power losses.

References

[1] F. Costa and D. Magnon.: Graphical analysis of the spectra of EMI sources in power electronics, in IEEE Transactions on Power Electronics, vol. 20, no. 6, pp. 1491-1498.

[2] A. Galluzzo, M. Melito, G. Belverde, S. Musumeci, A. Raciti and A. Testa.: Switching characteristic improvement of modern gate controlled devices, 1993 Fifth European Conference on Power Electronics and Applications, vol.2, pp. 374-379, 1993.

[3] A. Consoli, S. Musumeci, G. Oriti and A. Testa.: An innovative EMI reduction design technique in power converters, in IEEE Transactions on Electromagnetic Compatibility, vol. 38, no. 4, pp. 567-575, Nov. 1996.

[4] S. Musumeci, A. Raciti, A. Testa, A. Galluzzo and M. Melito.: Switching-behavior improvement of insulated gate-controlled devices, in IEEE Transactions on Power Electronics, vol. 12, no. 4, pp. 645-653, July 1997.

[5] Shihong Park and T. M. Jahns.: Flexible dv/dt and di/dt control method for insulated gate power switches, in IEEE Transactions on Industry Applications, vol. 39, no. 3, pp. 657-664, May-June 2003.

[6] Y. Lobsiger and J. W. Kolar.: Closed-Loop di/d t and dv/dt IGBT Gate Driver, in IEEE Transactions on Power Electronics, vol. 30, no. 6, pp. 3402-3417, June 2015.

[7] H. Riazmontazer, A. Rahnamaee, A. Mojab, S. Mehrnami, S. K. Mazumder and M. Zefran.: Closed-loop control of switching transition of SiC MOSFETs, 2015 IEEE Applied Power Electronics Conference and Exposition (APEC), 2015, pp. 782-788.

[8] P. R. Palmer and H. S. Rajamani.: Active Voltage control of IGBTs for high power applications, in IEEE Transactions on Power Electronics, vol. 19, no. 4, pp. 894-901, July 2004.

[9] I. Baraia, J. A. Barrena, G. Abad, J. M. Canales Segade and U. Iraola.: An Experimentally Verified Active Gate Control Method for the Series Connection of IGBT/Diodes, in IEEE Transactions on Power Electronics, vol. 27, no. 2, pp. 1025-1038, Feb. 2012.
[10] H. Sawezyn.: Etude de la commande autour de la tension de seuil (CATS) des transistors de puissance à grille isolée et de ses applications, Université des Sciences et technologies de Lille, PhD Thesis, 2003.
[11] N. Idir, R. Bausière, J.J. Franchaud, H. Sawezyn.: Contrôle des commutations des transistors à grille isolée : commande CATS, Revue internationale de génie électrique 2004,49-74.
[12] X. Yang, Y. Yuan, X. Zhang and P. R. Palmer.: Shaping High-Power IGBT Switching Transitions by Active Voltage Control for Reduced EMI Generation, in IEEE Transactions on Industry Applications, vol. 51, no. 2, pp. 1669-1677.
[13] N. Oswald, B. H. Stark, D. Holliday, C. Hargis and B. Drury.: Analysis of Shaped Pulse Transitions in Power Electronic Switching Waveforms for Reduced EMI Generation, in IEEE Transactions on Industry Applications, vol. 47, no. 5, pp. 2154-2165, Sept.-Oct. 2011.
[14] N. Patin and M. L. Viñals.: Toward an optimal Heisenberg's closed-loop gate drive for Power MOSFETs, IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society, 2012, pp. 828-833.
[15] S. Fukunaga, H. Takayama and T. Hikihara.: A Study on Switching Surge Voltage Suppression of SiC MOSFET by Digital Active Gate Drive, 2021 IEEE 12th Energy Conversion Congress and Exposition - Asia (ECCE-Asia), 2021, pp. 1325-1330.
[16] H. Takayama, T. Okuda and T. Hikihara.: A Study on Suppressing Surge Voltage of SiC MOSFET Using Digital Active Gate Driver, 2020 IEEE Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia), 2020, pp. 1-5.
[17] R. Morikawa, T. Sai, K. Hata and M. Takamiya.: New Gate Driving Technique Using Digital Gate Driver IC to Reduce Both EMI in Specific Frequency Band and Switching Loss in IGBTs, 2020 IEEE 9th International Power Electronics and Motion Control Conference (IPEMC2020-ECCE Asia), 2020, pp. 644-651.
[18] K. Miyazaki et al.: General-purpose clocked gate driver (CGD) IC with programmable 63-level drivability to reduce Ic overshoot and switching loss of various power transistors, 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), 2016.
[19] F. Portuese and M. Melito.: Gate charge leads to easy drive design for Power Mosfet circuits, PCIM '90 Proceedings of the 18th International Intelligent Motion Conference, 1990, pp. 237-243.
[20] C. R. Paul.: Introduction to Electromagnetic Compatibility, 2nd ed. Hoboken, NJ: Wiley, 2006.
[21] Infineon.: Low Loss Duopack: IGBT with Trench and Fieldstop technology IKW40N65ET7, TRENCHSTOP™, 2020,Datasheet version 2.2.