Sub-Modules Switching Algorithms for Dual Active Bridge Modular Multilevel Converters to Optimize Capacitor Voltage Deviation versus Power Efficiency

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Keywords

≪Dual Active Bridge (DAB) DC-DC converters≫, ≪Electromagnetic Interference (EMI)≫, ≪Modular Multilevel Converter (MMC)≫, ≪Soft switching≫, ≪Switching losses≫.

Abstract

This article firstly presents a detailed analysis and improvement for the dual active bridge employing MMC cells (MMC-DAB converter). The presence of MMC cells can effectively address the concern that medium or high voltage level is beyond voltage rating of semi-conductor devices in conventional DAB converter. However, the introduction of MMC cells results in significant losses originated from resonance between line inductor and sub-module capacitor. Besides, the non-negligible switching loss is another factor of efficiency drop. In order to solve the additional losses and improve the overall conversion efficiency, this article proposes three innovative switching algorithms, where manipulating cell states to stop current oscillation and enable zero voltage switching (ZVS). Simulated results for a medium voltage level MMC-DAB converter is provided to verify the efficiency gain under optimal switching algorithms. Moreover, a 2-level MMC-DAB converter is implemented and the experimental result shows the proficiency of the converter.

Introduction

Isolated Bi-directional DC-DC converters (IBDC) are a key building block for DC power systems, due to their advantages of easy power flow regulation and reduced power conversion stages [1]. Various topologies of IBDC converters have been discussed in recent researches, such as dual-flyback converter [2], flyback-forward converter [3], dual-half-bridge converter [4], and Dual-Active-Bridge (DAB) converter. Among all these topologies, DAB-IBDC has the advantages of high power capacity, bi-directional energy flow, simple control strategy, and inherent soft switching [5]. These merits make DAB converter a preferred IBDC topology in many applications such as solid-state transformer [6], micro-grid [7], and electric vehicle [8].

DAB Converter Employing Modular Multilevel Converter (MMC) Cells

Utility scale DC power networks will require DC-DC converters capable of operating beyond the ratings of available power semiconductor devices. In order to address these concerns, DAB converters based around Modular Multi-Level topologies are introduced [9]-[10]. As shown in Fig. 1, By replacing the power devices of a single phase DAB converter with series-connected sub-modules. The harmful dv/dt

stress is reduced by introducing intermediate voltage steps, where the output voltage of one bridge can be modulated as a trapezoidal waveform. The analysed MMC converter has a capacitor connected in series with an IGBT, which can act as a soft-voltage clamps for the converter. When the MMC cells are employed into DAB converter, all cells in upper or lower arm are utilizing half-bridge module, denoted as "quasi two-level converter" (Q2LC) [11].

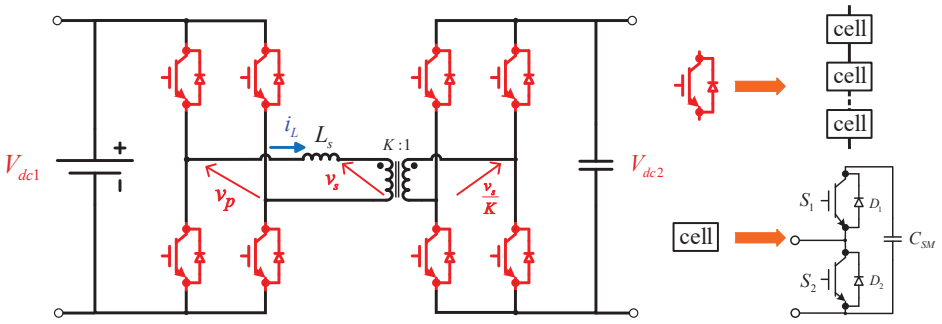


Fig. 1: The schematic of conventional DAB converter which applies MMC cells.

Fig. 2 depicts the schematic of MMC-DAB converter which is used in this article. The conventional H-Bridge connection of DAB is replaced by one bridge leg with centralized ground for simplifying set-up. Meanwhile, voltages across the leakage inductance L_s of AC transformer are denoted as v_p and v_s respectively, where trapezoidal modulation is used to create quasi two-level voltage waveform. The phase shift between v_p and v_s can be controlled to achieve output regulation, where controlling strategies such as linear quadratic regulator (LQR) can be added [12]. Moreover, N represents the number of cells within one arm, and there will be $N+1$ levels on aggregate for stack voltage generation. T_w indicates the transition dwell time which can be short enough compared to the main switching period T_s.

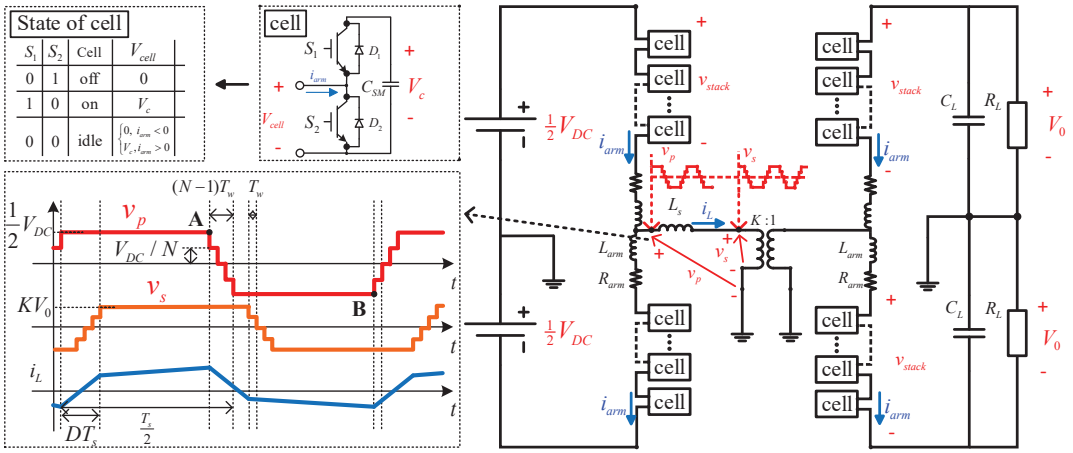


Fig. 2: Schematic of single phase MMC-DAB converter.

Loss Classification in MMC-DAB Converter

However, the introduction of MMC can result in extra losses, which can be classified as conduction losses and switching losses. The energy trapped in LC resonance is a dominant factor in efficiency reduction. Each time when a new cell being switched in, the sinusoidal charging current will cause oscillation in capacitor voltage which will draw more energy from sources. Subsequently, this extra energy will be transferred and trapped between cell capacitor and line inductor, and finally cause power dissipation on line resistance. This resonance can also result in electromagnetic interference (EMI) [13]-[14], which could have negative effect on the performances of semiconductor devices and also be harmful to circuits. In this article, an alternative switching algorithm is proposed (Algorithm 1) to control oscillation and reduce losses associated with quasi-two level switching of MMC stacks.

Additionally, during each switching transient, there will be a significant overlap between switch current and voltage due to the high-stand voltage of sub-module capacitor [15]. The switching losses can be

relatively large under high load current and high switching frequency. In order to address this problem, the second algorithm (Algorithm 2), is proposed which exploit zero voltage switch (ZVS) to reduce switching losses. Moreover, Algorithm 3 is proposed by combining Algorithm 1& 2.

Operating principle of MMC-DAB

As T_d is small enough and negligible compared to switching period, quasi two-level voltage waveforms are generated across AC transformer. Thus, the DAB characteristics of MMC-DAB converter, such as output voltage and leakage inductor current, can be derived directly using DAB analysis. In a typical DAB converter, if the duty ratio D is conventionally constrained between 0 and 0.5, the power will be transmitted from primary to secondary side. Two conditions of AC current have been depicted as shown in Fig. 3. This article will analyse forward power flow. Moreover, the polarity of I_1 determines whether the cells in the upper arm of secondary bridge will experience positive (inductive loading) or negative (capacitive loading) current. The inductor current is analysed in DAB converter [12],

$$\begin{aligned} I_1 &= \frac{v_p - v_s - 2Dv_p}{4Lf_s} - \frac{N-1}{2L_s}(v_p + v_s)T_w \qquad I_2 = -\frac{2v_sD - v_s + v_p}{4Lf_s} + \frac{N-1}{2L_s}(v_p + v_s)T_w \\ I_3 &= \frac{2Dv_p + v_s - v_p}{4Lf_s} + \frac{N-1}{2L_s}(-v_p + v_s)T_w \qquad I_4 = \frac{2v_sD - v_s + v_p}{4Lf_s} - \frac{N-1}{2L_s}(v_p - v_s)T_w \end{aligned} \tag{1}$$

where $v_p = V_{dc}/2$ and $v_s = KV_0$ are the voltages across leakage inductance L_s, K is the turns ratio of AC transformer, D represents the duty ratio. The power and the output voltage will be,

$$\begin{cases} P_{sec} = P_{pri} = \dfrac{KV_{DC}V_0D(1-D)}{4L_sf_s} \\ V_0 = \dfrac{KV_{DC}D(1-D)R_L}{L_sf_sC_LR_L + 2L_sf_s} \end{cases} \tag{2}$$

From (2), we can see that the output voltage can be regulated by controlling phase shift D.

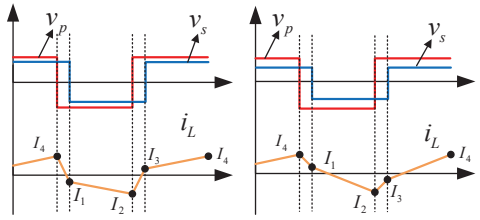


Fig. 3: AC current waveform under high (left) and low (right) modulation index.

Voltage balancing

Achieve sub-module capacitor voltage V_c balance is a premise of MMC successful operation [14]. As the cell which turns on under positive current first sees the greatest charge, the cells with lower voltage should be turned on before those with higher voltage in order to achieve voltage balancing. Thus, each individual cell voltage can be balanced by firstly applying conventional sorting algorithms, where sub-module capacitor voltage V_c are sorted in ascending or descending order based on arm current polarity. Then the cell capacitor is brought into conduction following the order [11]. Other advanced balancing techniques are researched such as rotating gate signals in turn [16] and in [14] which solves the challenge that current polarity may reverse.

In this article, conventional balancing control is sufficient enough as medium voltage level and small quantity of sub-modules are mainly considered. Suppose $D \in [0, 0.5]$ which indicates forward power flow, the switched-in arm of primary bridge would always meet positive current as $I_4 > 0$. Positive (charging) arm current illustrates that for primary bridge, V_c should be sorted in the ascending order, where cell with the lowest V_c will be firstly switched in, and cell with the highest V_c will be the last one.

However, for secondary bridge, it depends on polarity of I_1. When $I_1 < 0$, cells should still be switched in from low V_c to high V_c. For negative (discharging) current where $I_1 > 0$, cells will be sorted in the descending order. The cell capacitor with the highest V_c will be firstly brought into conduction while the cell with the lowest V_c will be lastly switched in. This article mainly analyse the condition of $I_1 < 0$, where

$$I_1 < 0 \rightarrow \frac{v_p - v_s - 2Dv_p}{4Lf_s} - \frac{N-1}{2L_s}(v_p + v_s)\,T_w < 0 \tag{3}$$

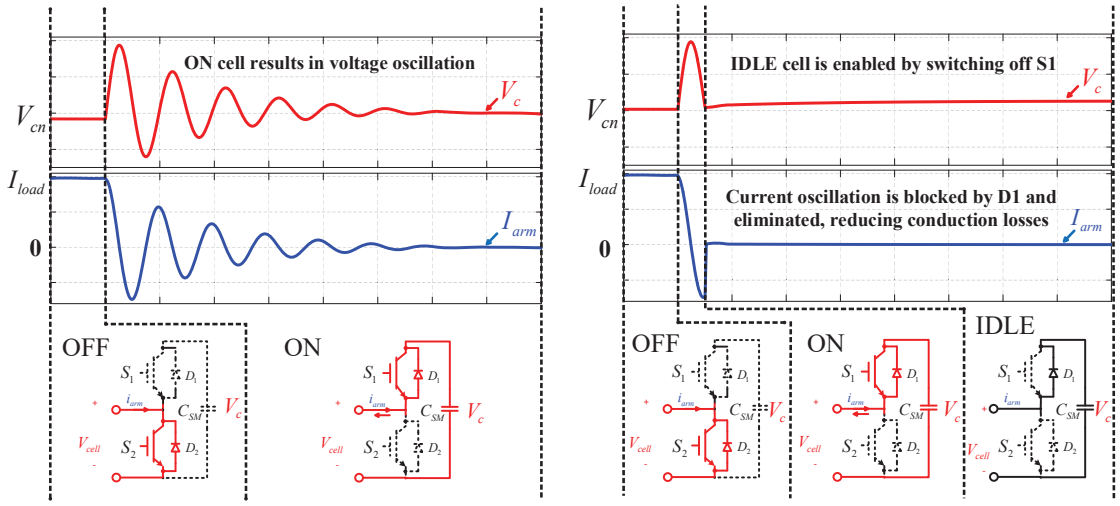
Component sizing

The choice of sub-module capacitance C_{PM} is of great importance in MMC-DAB converter, since it determines the voltage overshoot which could be potentially harmful for semiconductor devices [17]. Thus, we consider the worst case for voltage overshoot, where phase shift reaches maximum, $D = 0.5$, exhibiting the highest current. Meanwhile, the capacitor voltage rise is closely related to the energy released from leakage inductor L_s. Thus, we have,

$$C_{PM} = \frac{2N}{\ell V_{DC}} \int_0^{(N-1)T_w} \left(I_4 + \frac{1}{L_s} \int_0^t (v_p - v_s) dt \right) dt \tag{4}$$

where $\ell = \delta V / V_{cn}$, δV is the voltage overshoot, and V_{cn} is the nominal cell voltage. As shown in Fig 2, according to the values of v_p, v_s, we can derive the designed equation for C_{PM},

$$C_{PM} \geq \begin{cases} \dfrac{N(N-1)T_w}{12\ell L_s}\left(3DT_s - \dfrac{3T_s}{2} + \dfrac{3v_sT_s}{2v_p} - \dfrac{2v_s}{v_p}(N-1)T_w\right) & ,v_p \leq v_s \\ \dfrac{N(N-1)T_w}{12\ell L_s}\left(3DT_s - 2(N-1)T_w\right) & ,v_p = v_s \\ \dfrac{N(N-1)T_w}{12\ell L_s}\left(\dfrac{T_s}{2} - \dfrac{T_sv_s}{2v_p} - (N-1)T_w + \dfrac{Dv_sT_s}{v_p} - \dfrac{v_s}{v_p}(N-1)T_w\right) & ,v_p > v_s \end{cases} \tag{5}$$



(a) (b)

Fig. 4: The capacitor voltage V_c and arm current i_{arm} of MMC-DAB converter regarding different cell states under (a)Normal operation, (b)Algorithm 1.

Optimal Switching Algorithms for Gating Signals

In regular MMC, the cell output voltage can be regulated to V_{cn} or 0 by adjusting states of two devices. During "ON" state, S_1 turns on while S_2 turns off, leading to $V_{cell} = V_{cn}$. While during "OFF" state, the

S_1 turns off and S_2 turns on result in $V_{cell} = 0$. Conventionally the gating signals of two IGBT devices will be complementary, always keeping the aggregate number of "ON" cells and "OFF" cells to be N, where $N_{\text{on}} + N_{\text{off}} = N$.

MMC Mode (Algorithm 1)

Based on regular MMC, "Idle" state is enabled, where both of S_1 and S_2 are switched off, and the discharging current of submodule capacitor C_{PM} can be blocked by the diode D_1. As a result, LC resonance is forced to stop, and cell capacitor voltage V_c will remain constant. The switch off operation for S_1 should only happen during discharging process, otherwise the current could still charge the capacitor through diode D_1. Fig. 4 demonstrates the corresponding cell states for one switching instance under normal operation and Algorithm 1. There will be voltage oscillation caused by LC resonance under normal operation, where cell state is always "ON". When Algorithm 1 is applied, S_1 will be switched off when V_c oscillates back to nominal voltage V_{cn} after the first oscillation cycle. The energy stored in the inductance is returned to the DC supply when S_1 is turned off.

DAB Mode (Algorithm 2)

In order to achieve ZVS in MMC-DAB, S_1 can be turned on during all operating time, allowing C_{PM} to be fully charged and discharged. In this mode, C_{PM} is equivalent to the snubber capacitance in conventional DAB converter. Fig. 5(a) illustrates the power flow within the stack. For turn off transient, as $V_c = 0$ there will be no overlap between device voltage and current. For turn on transient, the S_{2L} of complementary arm will be switched off first, which results in power transfer between two sub-module capacitors. Thus the cell capacitor will be fully discharged, and anti-parallel diode conducting, resulting in zero voltage switching. Based on different delay time T_d between S_{2U} and S_{2L}, there will be a minimum load current for C_{PM} to be fast charged and discharged. According to Fig. 5(a),

$$V_1 + V_2 + L_{arm}\frac{dI_1}{dt} - L_{arm}\frac{dI_2}{dt} = V_{DC};\ I_1 + I_2 = I_{load};\ C_{equi}\frac{dV_1}{dt} = I_1;\ C_{equi}\frac{dV_2}{dt} = -I_2 \tag{6}$$

where $C_{equi} = C_{PM}/N$, and $\omega_d = 1/\sqrt{L_{arm}C_{equi}}$. Then the discharging equation would be

$$V_2 = \frac{I_{load}}{2\omega_d C_{equi}}\sin(\omega_d t) - \frac{I_{load}t}{2C_{equi}} + V_{cn} \tag{7}$$

The derivation of required minimum load current, or duty ratio $D_{\min}$, would be

$$\begin{cases} D_{\min} = \dfrac{-4C_{equi}V_{cn}}{v_p\left(\omega_d \sin\left(\frac{T_d}{\omega_d}\right) - T_d\right)} + \dfrac{-v_p + v_s}{2v_p} & \text{For primary bridge} \\ D_{\min} = \dfrac{-4C_{equi}V_{cn}}{v_p\left(\omega_d \sin\left(\frac{T_d}{\omega_d}\right) - T_d\right)} + \dfrac{v_p - v_s}{2v_p} & \text{For secondary bridge} \end{cases} \tag{8}$$

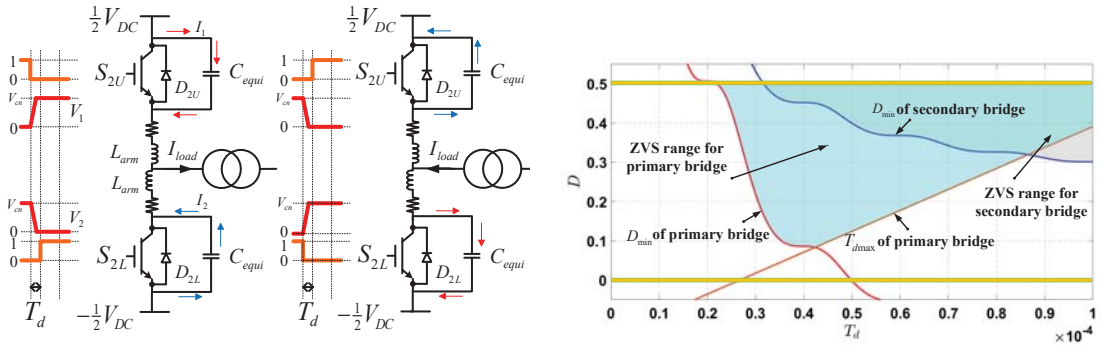
Additionally, there should be constraint on T_d for certain load current, to avoid reverse current, where C_{PM} could be charged again. Based on (1), the value of $T_{d\max}$ can be derived by letting $i_L = 0$,

$$\begin{aligned} i_L &= \frac{2Dv_s + v_p - v_s}{4L_s f_s} - \frac{(N-1)T_w}{2L_s}(v_p + v_s) - \frac{v_p + v_s}{L_s}T_d = 0 \\ T_{d\max} &= -\frac{(N-1)T_w}{2} + \frac{2Dv_s + v_p - v_s}{4f_s(v_p + v_s)} \end{aligned} \tag{9}$$

Based on (8) and (9), Fig. 5(b) shows the ZVS range for varying chosen delay time T_d.

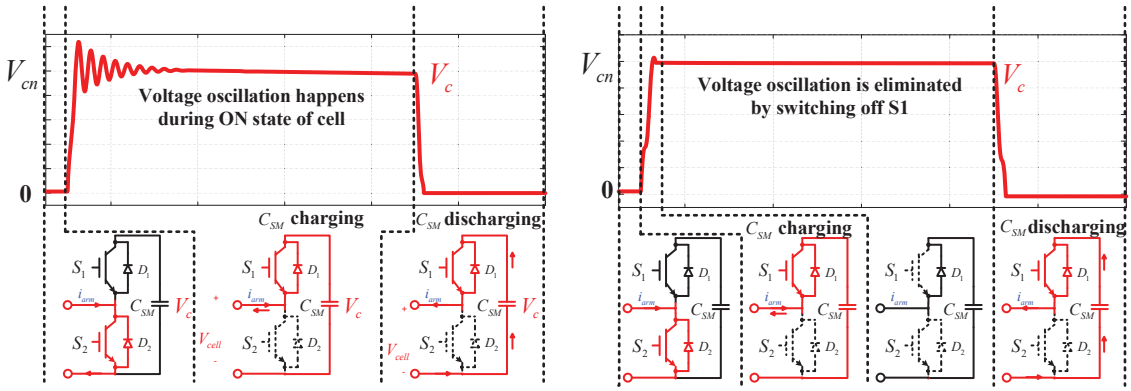
Algorithm 3

By combining Algorithm 1& 2, the improved optimal gating signals in DAB mode (Algorithm 3) will switch off S_1 when capacitor voltage returns to V_{cn}. Fig 6 contrasts the current flow (red arrow) of cells



(a) (b)

Fig. 5: When Algorithm 2 is enabled, the power flow diagram during dead-band between upper S_{2U} and lower S_{2L}, with charging current (red solid line) and discharging current (blue solid line). (b)ZVS range of primary (blue area) and secondary bridge (grey area) under varying T_d.



(a) (b)

Fig. 6: The capacitor voltage V_c of MMC-DAB converter regarding different cell states under (a)Algorithm 2, (b)Algorithm 3.

under Algorithm 2 and 3. As noted from Fig. 6(b), the switching off of S_1 can block discharging current, and thus the voltage variation caused by LC resonance will be eliminated. Voltage balancing algorithm becomes unnecessary under Algorithm 2& 3, as V_c will be fully discharged at the end of each switching cycle. Fig. 7 gives specific flowchart of applying each optimal switching algorithms.

Simulated Results

To begin with, a DAB converter employing MMC cells has been set up in Simulink, which operates under the voltage range of -2 kV to 2 kV. Based on (4) and (5), the value of C_{PM} can be determined, where the detailed parameters are shown in Table I.

Table I: Designed circuit parameters of MMC-DAB converter and optimal algorithms.

Power rating	Values	Circuit parameter	Values
DC source voltage (V_{dc})	4kV	Number of cells per arm (N)	4
Output voltage (V_0)	2kV	Submodule capacitance (C_{SM})	60 μF
Sub-module nominal voltage (V_{cn})	1kV	Arm impedance (R_{arm})	10 mΩ
Duty ratio D	0.4	Arm inductance (L_{arm})	2 μH
Dwell time (T_w)	5 μs	Leakage inductance L_s	1mH
Operating frequency (f_s)	1 kHz		

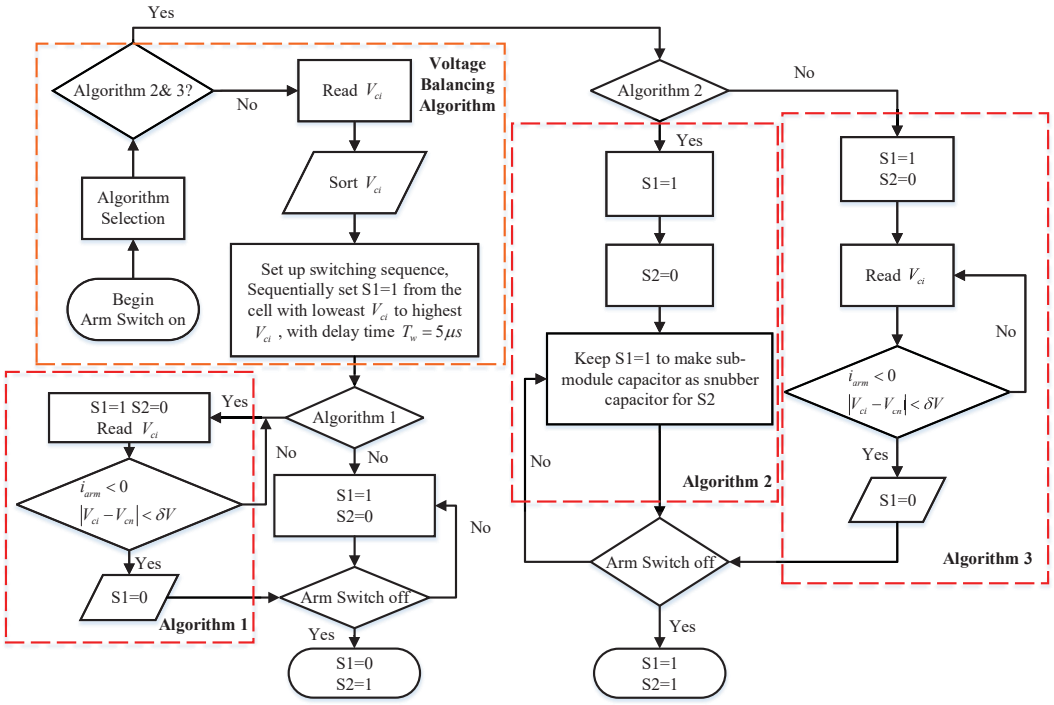
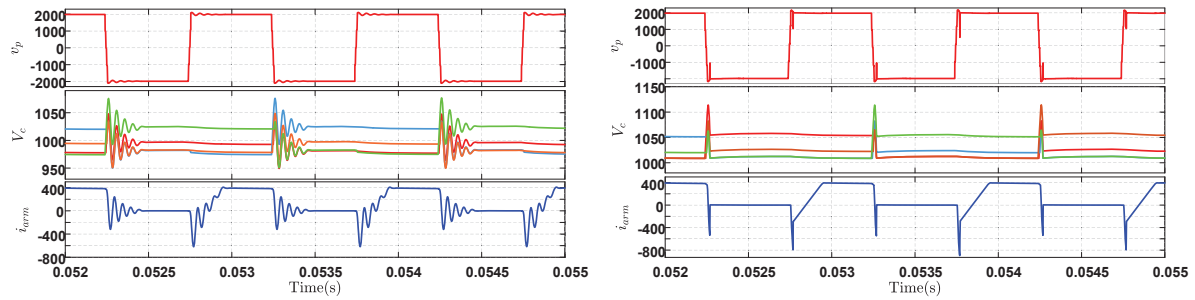


Fig. 7: The flowchart of applying proposed optimal switching algorithms in MMC-DAB converter.

Output Characteristics under Optimal Gating Signals

Fig. 8 contrasts the output and cell capacitor voltage under trapezoidal modulated MMC complementary gating signals and optimal gating signals in MMC mode (Algorithm 1). It indicates that there will be no more voltage oscillation in output waveform after one cycle of resonance. One thing has to be noticed is that not all capacitor voltage is returning to the voltage level within the statutory limit. This is because if one cell is switched to Idle, negative charging current for all cells will be blocked since they are connected in series. Although some cell capacitor voltages are not returned to the statutory limit, voltage balancing control can guarantee the stability of cell capacitor voltage.

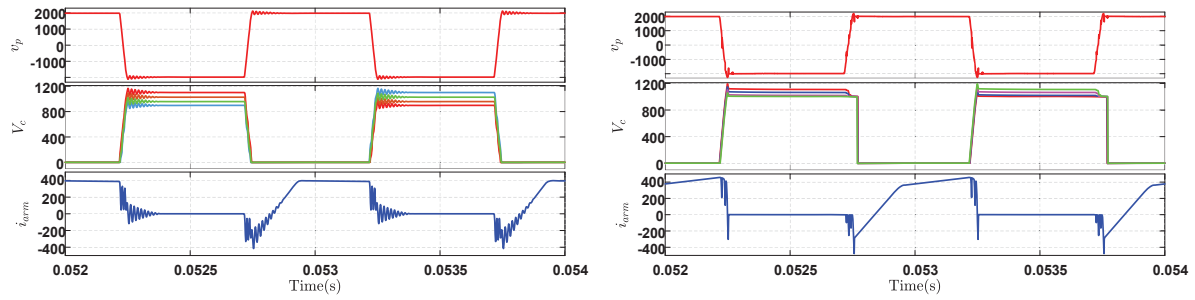
From Fig. 8(b), we can notice that there will be a spike in v_p. When S_1 is turned off, the negative current can conduct D_2 then result in $V_{cell} = 0$. The overall conversion efficiency will not be affected, where the efficiency gain is still achieved by applying Algorithm 1 as it has eliminated the power loss from resonance.



(a) (b)

Fig. 8: Submodule capacitor voltage and arm current of MMC-DAB converter under (a)normal operation, (b)optimal switching Algorithm 1.

Fig. 9 contrasts the output and cell capacitor voltage operated under Algorithm 2 and 3, which is under DAB mode. The cell capacitor will be charged and fully discharged every switching cycle. The sub-module voltage can sill be stabilized although there is no voltage balancing control. Under Algorithm 3, the LC damping has been eliminated by switching off S_1 as V_c approaches V_{cn}.



(a) (b)

Fig. 9: Submodule capacitor voltage and arm current of MMC-DAB converter under (a)Algorithm 2, (b)Algorithm 3.

Switching loss analysis

A simulink-simscape model was set up to calculate the switching losses of semiconductor devices. Fig. 10 gives simulated result of the switching transient under normal operation and Algorithm 2. For normal operation, during one switching cycle, there will be two hard switches, especially the turn off transient of S_2 would result in 95.72mJ losses. Under Algorithm 2, C_{PM} is utilized as snubber capacitor for the turning off transient of S_2, and switching losses have been significantly reduced as ZVS is achieved. The total switching loss of the converter under Algorithm 1 will be similar to that of normal operation, but the turn off process of S_1 causes more energy consumption as there is negative current flowing through the device during switching off. The turn off switching losses of S_1 increase from 11.78mJ to 101.37mJ. Nevertheless, the application of Algorithm 1 would not contribute to significant switching losses since only 1 S_1 needs to be switched off among the whole arm under Algorithm 1.

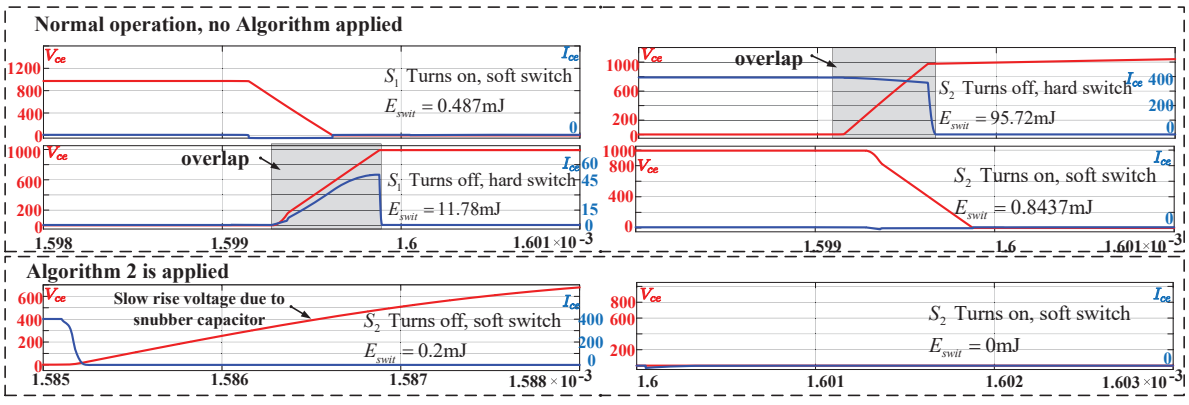


Fig. 10: The switching characteristics of S_1 and S_2 under normal operation and switching algorithm 2.

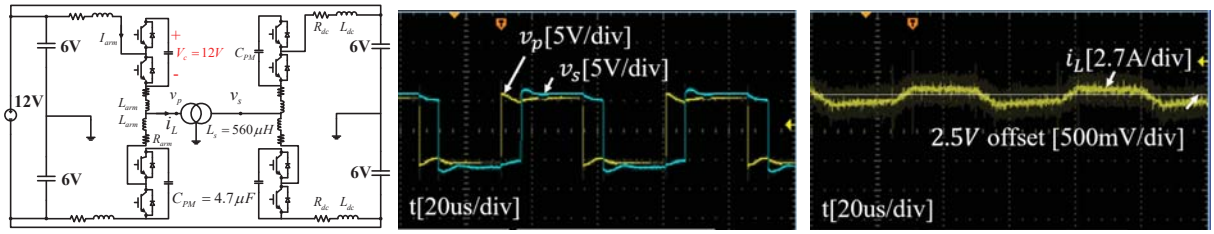
Table II gives detailed power flow and losses during one entire switching cycle for MMC-DAB converter. Under the proposed switching algorithms, the overall conversion efficiency has been improved. Although efficiency is improved under Algorithm 1, the output spike may potentially affect output stability. The effect could be mitigated when more cells are applied. More efficiency gain can be achieved for Algorithm 1 when intense resonance occurs, such as with higher L_{arm}. The system under Algorithm 2& 3 have higher conversion efficiency. However, there is limited operating range for adopting these two algorithms as they both require high load current and careful design of delay time T_d, to achieve rapid charging and discharging, subsequently ZVS. The employment of Algorithm 3 does not achieve efficiency gain as expected, since it has additional switching on and off transients for S_1.

Table II: Power losses of MMC-DAB converter under different operating switching algorithms.

Algorithms	Input power P_{in}	Conduction losses P_{cond}	Switching losses P_{swit}	Total losses P_{tot}	Efficiency η
Normal Operation	478kW	23.11kW	3.47kW	26.58kW	94.4%
Algorithm 1	477kW	17.7kW	3.83kW	21.53kW	95.5%
Algorithm 2	477kW	19.14kW	8W	19.15kW	95.9%
Algorithm 3	498kW	18.5kW	4.3kW	22.8kW	95.4%

Experimental Test

In order to verify the simulated result, a DAB converter employing MMC cells needs to be built. It remains impractical to build an MMC-DAB converter in industrial level, which typically rates at hundreds of Megawatts within a traditional laboratory. Thus, a scaled-down version of MMC-DAB converter was set up, where the proposed algorithms can be tested. The designed sub-module is in half-bridge operation, and rated at 12V. When 4 series-connected sub-modules of each stack are enabled, $\pm$ 24V square wave will be generated. C_{PM} is chosen as 4.7μF and L_{arm} is relatively large at 27μH to create enough oscillation which can be later tested and eliminated. f_s is chosen at 2kHz and L_s is set to 560μH. The allowed maximum i_L is 3A. Fig. 11(a) shows the circuit diagram of the experimental test, where only 1 cell is enabled in each arm. Thus, 2-level voltage waveforms with phase shift as shown in Fig. 11(b) across leakage inductance L_s are generated under normal operation. As only one cell of the arm is enabled, the v_p and v_s depict at $\pm 24/4 = \pm 6$V, with phase shift $D = 0.25$. The voltage oscillation is not obvious in this test indicates that mosfets with superior performance (specifically lower $R_{ds(on)}$) are required.



(a) (b) (c)

Fig. 11: (a)The circuit diagram of experimental test for 2-level MMC-DAB converter. Under normal operation, (b)the voltages across L_s, and (c)the current flowing through L_s, which is i_L.

The quasi 2-level voltages contribute to the typical current waveform of DAB, as shown in Fig. 11(c). The highest inductor current from the diagram is 670mA, which matches the derivation of (1). Besides, the current shows symmetrical characteristics which verifies that the MMC-DAB converter is under stable operation, and with power transfer from primary to secondary bridge. Generally, the result verifies the fundamental operation of DAB converter employing MMC cells. The later work will be focusing on the experiment of converters with full cells and optimal algorithms enabled.

Conclusion

This article firstly reviews the analysis and design of DAB converter employing MMC cells. Then, three advanced gating signals are proposed in order to mitigate the significant losses caused by LC resonance, and the switching losses. The overall conversion efficiency under these optimal gating signals are tested in Simulink, verifying the efficiency improvement brought by these algorithms. As for experiment, a scaled down MMC-DAB converter was established, DAB converter with 2 voltage levels has been tested, which can confirm the correct operation of DAB converter employing MMC structures. The future work will enable full MMC cells to generate trapezoidal waveform, and verify the efficiency improvement when optimal algorithms are applied.

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