Oscillation Damping in a 500kW Hybrid Si/SiC Three-Level ANPC Inverter with Decoupling Capacitor

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Keywords

«Voltage Source Inverter (VSI) », « Hybrid », « Converter control », « Silicon Carbide (SiC) »

Abstract

This paper presents a high-power hybrid Si/SiC 3L ANPC using only two SiC MOSFET. The high parasitic inductive commutation loop is decoupled by adding a decoupling capacitor near to the SiC MOSFET modules. Because of the decoupling capacitor, there are two main oscillation circuits are formed. These oscillations can lead to serious EMI issues and need to be damped. The damping schemes for the switching oscillation were experimental investigated and a special switching strategy was also developed to actively cut off the decoupling oscillation.

Introduction

The active neutral point clamped (ANPC) was famous for having flexible switching states and hence losses can be flexibly distributed among the power switches [4]. Silicon carbine (SiC) MOSFET has much lower switching losses compare to Si IGBT, but it is still not a good option for mass production because of its high cost. With 3 level output voltage and high switching frequency, the filter inductor's volume can be significantly reduced. In order to take advantages of both ANPC three level topology and SiC MOSFET at lower cost, many studies have proposed the hybrid ANPC (HANPC) topology, which uses both silicon IGBT and SiC MOSFET as power switches [5-12]. The main principle of the HANPC is using the flexible switching states to relocate the high switching frequency on SiC MOSFETs to reduce the switching losses. Those publications can be divided into two main streams: one is replacing 4 Si IGBT with 4 SiC MOSFET [5,6,10] (Fig 1.a), the other is replacing two Si IGBT with two SiC MOSFET [6,7,8,9,11,12] (Fig 1.b). Most of the publications concentrated on low power applications which can be done with discrete SiC chip on PCB or all switches are integrated in one module [11] which have low parasitic inductance commutation loop. For high power applications, the separated SiC MOSFET, IGBT modules are connected by busbar to form HANPC topology. In this scenario, the large stray inductance commutation loop becomes the major issue which increases the switching losses of the high power HANPC (Fig 1.b). In [5], a HANPC with four SiC MOSFET in megawatt scaled was introduced, which took the advantage of the small commutation loop (Fig.1a). On the other hand, four SiC MOSFET were used which again increased the cost of the inverter.

This paper proposes a high power HANPC which uses only two SiC MOSFET together with a decoupling capacitor (C_f) placed near to SiC MOSFET to decouple the high parasitic commutation loop (Fig.1c). This configuration can reduce the cost of the inverter and decouple the large inductive commutation loop from the SiC MOSFET module. During switching the SiC MOSFET, the oscillation circuit is created from the stray inductance of the commutation loop and the output capacitor (C_{oss}) of the MOSFET. Because of C_f, this oscillation circuit is divided into two loops. The low frequency (LF)

oscillation loop or can also be called decoupling oscillation loop (Fig.2 blue dash line) and the high frequency (HF) oscillation loop (Fig.2 a green dash line). The theoretical model of the oscillation circuit was studied in [13]. These oscillations pose a threat to electromagnetic interference (EMI) compliance both in conducted emission and magnetic field radiated emission over regulatory frequency range from 150kHz to 30MHz [14,15]. The main challenge of this 2SiC hybrid ANPC concept is how to damp these oscillations. Ferrite core (FC) is proposed to damp the high frequency loop and high-power film capacitor C_f with external stainless-steel connections is proposed to damp both of the oscillations. A special switching scheme is also designed to actively cut off the low frequency oscillation path. The experimental 500kW 2SiC hybrid ANPC testbench is setup to verify the concept can be seen in Fig.8.

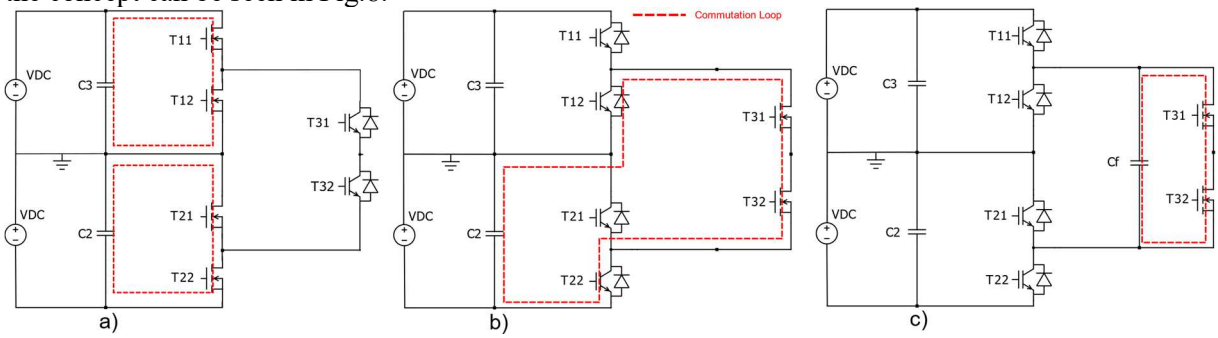


Fig. 1: HANPC topology, a) 4SiC with short commutation loop proposed in [5], b) 2SiC with long commutation loop, c) 2SiC with decoupling capacitor C_f is proposed in this paper.

1. Switching oscillation in HANPC

2SiC hybrid ANPC has 3 levels output: positive (P), zero (ZN, ZP) and negative(N) output voltage. The conventional switching combination is shown as the table I.a. When the switch is on, it is marked with 1 and off with 0. It can be seen that the IGBT switch (T11, T12, T21, T22) are switched at fundamental frequency and SiC MOSFET (T31, T32) are switched at carrier frequency when the switching states change between $P \leftrightarrow ZP$ or $N \leftrightarrow ZN$.

Table I. HANPC switching states

	a) Conventional switching states							b) Proposed switching states						
	T11	T12	T21	T22	T31	T32		T11	T12	T21	T22	T31	T32	Vout
P	**1**	0	**1**	0	**1**	0		**1**	0	0	0	**1**	0	VDC
ZP	**1**	0	**1**	0	0	**1**		0	0	**1**	0	0	**1**	0
ZN	0	**1**	0	**1**	**1**	0		0	**1**	0	0	**1**	0	0
N	0	**1**	0	**1**	0	**1**		0	0	0	**1**	0	**1**	-VDC

Let's take a look at the transition from $P \rightarrow ZP$ when the negative current IL direction is going into the inverter (Fig 2.a), the switches T11, T21 are on, T32 is off, T31 is turned from on (P) to off (deadtime) before turning on T32(ZP). With the assumption that DC link capacitors C2, C3 are very big and can be considered as voltage source VDC, the equivalent circuit in this case can be seen in Fig. 2b with L_{s1}, R_{s1} are stray inductance and resistance between DC link capacitor and decoupling capacitor C_f. L_{s2}, R_{s2} are stray inductance and resistance between C_f and T31's output capacitor C_{oss}, R_f is external resistance of C_f. According to [13], when $C_f \gg C_{oss}$ and $L_{s1} >> L_{s2}$ (the conditions are normally archived with decoupling capacitor is put near to the MOSFET module), the loop's stray inductance will be fully decoupled and the oscillations can be studied separately for each individual loop. The oscillation voltage v_{ds} over T31 can be modeled with the equation:

$$v_{ds} = VDC + \widehat{V_L}.\sin(\omega_L t + \emptyset_L).e^{-\omega_L t.\tau_L} + \widehat{V_H}.\sin(\omega_H t + \emptyset_H).e^{-\omega_H t.\tau_H} \qquad (1)$$

With the angular frequency of LF and HF loop: $\omega_L \approx \frac{1}{\sqrt{L_{s1}.C_f}}$, $\omega_H \approx \frac{1}{\sqrt{L_{s2}.C_{oss}}}$,

the initial phase of LF, HFoscillations: $\emptyset_L, \emptyset_H$

oscillation amplitude of LF and HF loop:

$$\widehat{V_L} = \sqrt{\frac{L_{s1}}{C_f}} I_L, \widehat{V_H} = \sqrt{\frac{L_{s2}}{C_{oss}}} I_L \quad (1.a)$$

With IL is load current at the turn off moment
Damping factor of LF and HF loop:

$$\tau_L = \frac{R_{s1}+R_f}{2}\sqrt{\frac{C_f}{L_{s1}}}, \tau_H = \frac{R_{s2}+R_f}{2}\sqrt{\frac{C_{oss}}{L_{s2}}} \quad (1.b)$$

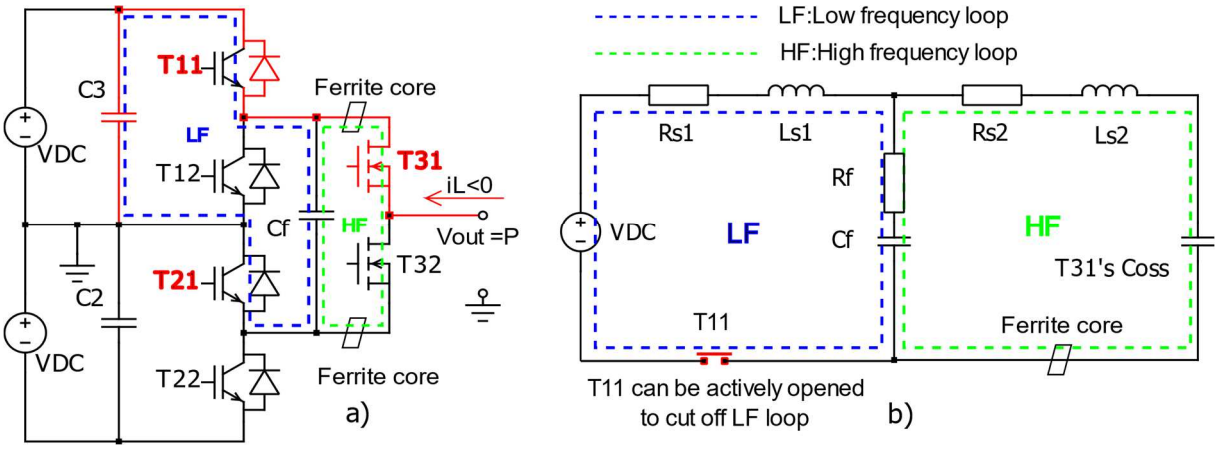


Fig. 2: a) Two oscillation circuits are formed by decoupling capacitor C_f, b) LF, HF's equivalent circuits, R_f is C_f's external resistance it can increase the damping ratio of both LF, HFloop. MnZn Ferrite core damp HF loop. T11 can be turned off to actively cut off the LF oscillation.

From equation (1.b), the resistance of the loop (R_{s1}, R_{s2}) can be increased in order to damp the oscillation for HF and LF loop. But increasing the resistance of the busbar or terminals will lead to high conduction losses due to DC current. By using capacitors which have external parasitic resistance R_f either than only the conventional film snubber capacitor, the resistance of both HF and LF loop can be increased without losses cause by DC current. The HF loop also can be damped effectively with ferrite core (FC) because the HF's frequency range of the switching is in the damping frequency range of the common ferrite cores on the market (from 1MHz to 50 MHz). Another way to damp the LF loop is actively cut off the oscillation loop by turning off one of the IGBT (for example T11 or T21). The details of these damping methods are explained in the next section of this paper.

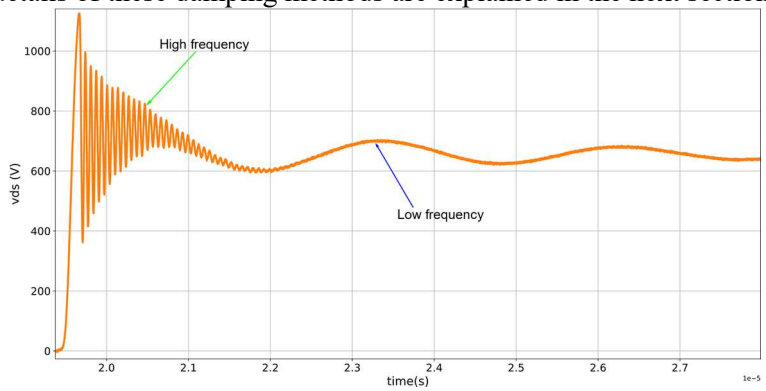


Fig. 3: Low and high frequency (LF, HF) oscillations on T31's voltage during turn-off

2. High Frequency oscillation damping

Damping switching oscillation with snubber RC circuit or ferrite cores are preferred than conventional reducing switching speed technique because of lower switching losses [15-18]. According to the snubber design guideline in [16], the RC snubber circuit values can be estimated in equations (2), (3): with C_{sn}, R_{sn}, PR_{sn} are snubber capacitor, snubber resistor, power losses on snubber resistor values.

IL_{max} is the maximum load current, Vds_{peak} is the peak voltage under safe operation area (SOA) of the SiC MOSFET module, f_{sw} is the switching frequency, t_r is the turn-on current rise time.

$$C_{sn} = \frac{(L_{s1} + L_{s2})IL_{max}^2}{\left(Vds_{peak} - VDC\right)^2} \quad (2)$$

$$R_{sn} = \frac{1}{6 \cdot C_{sn} \cdot f_{sw}} \quad (3)$$

$$PR_{sn} = \frac{1}{2} \cdot C_{sn} \cdot f_{sw} \cdot \left(V^2 ds_{peak} - VDC^2\right) + 1.125 \cdot f_{sw} \cdot \frac{(L_{s1} + L_{s2})^2 IL_{max}^2}{t_r \cdot R_{sn}} \quad (4)$$

In this 500kW 2SiC hybrid ANPC experimental setup, the stray inductance loop is quite large, around 115nH, $IL_{max} = 450$A, VDC = 750V, $Vds_{peak} = 1200\,V$,switching frequency $f_{sw} = 10\,kHz$. From equation (4), it can be seen that due to high load current, high switching speed and large parasitic inductance, the power losses on the snubber resistor is huge. This make the damping method using RC snubber is not practical in this scenario. In contract to RC snubber, some ferrite core materials can provide high equivalent resistance at high frequency range (>1MHz) and low equivalent resistance at low frequency range which can increase the damping ratio at high frequency and lower losses at low frequency range (< 1MHz) [19], those special properties of ferrite cores best fit for high power, high frequency oscillation damping. In the experiment, MnZn ferrite cores were placed on the high frequency loop of the oscillation circuit (Fig 2.a). Voltage vds across T31 was measured during turning off. The result shows in Fig 4.b, the high frequency oscillation was totally removed. Ferrite cores also introduced more stray inductance to the commutation loop that increased the over voltage more than the case without ferrite cores.

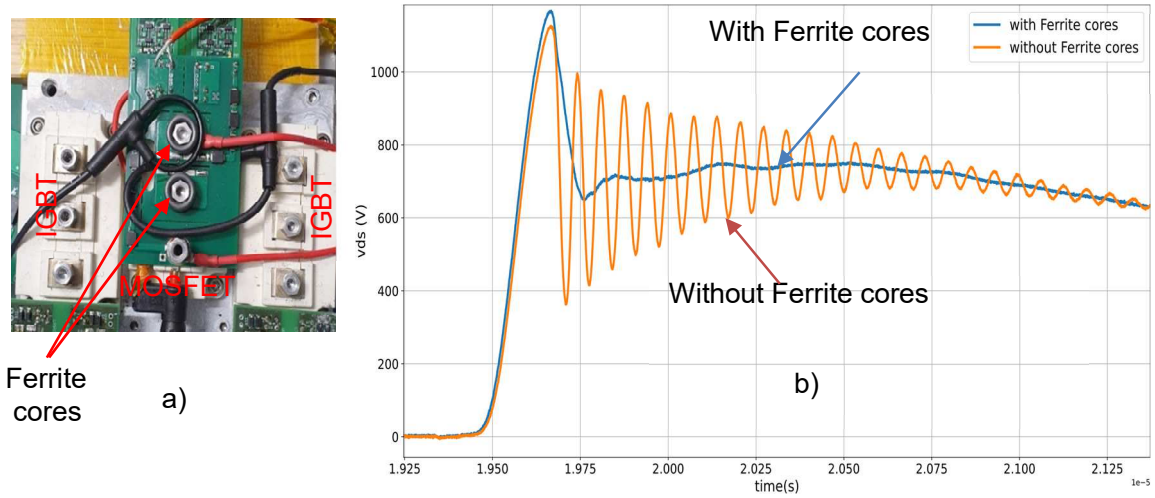


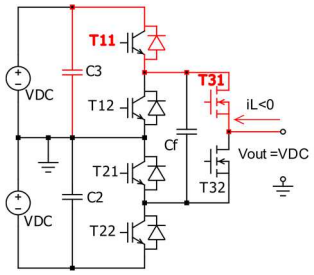
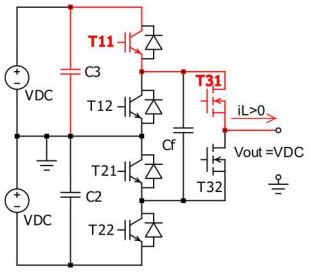
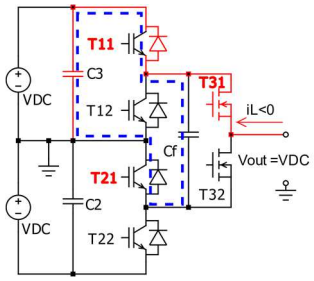
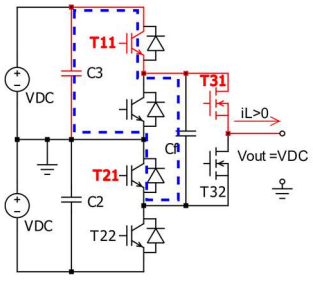
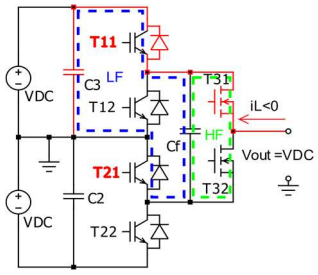
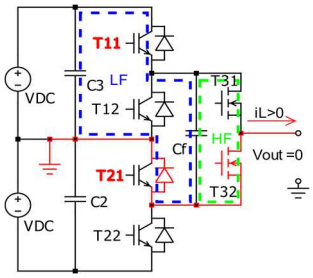
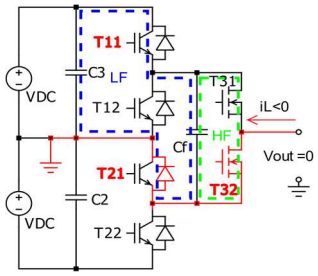
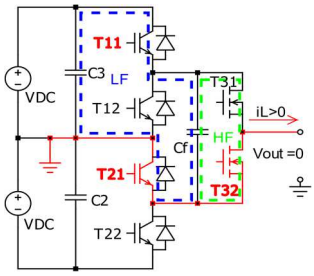
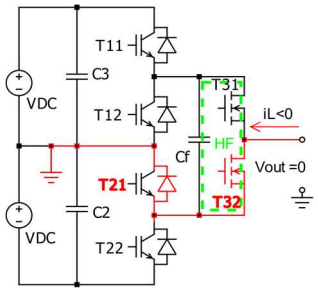
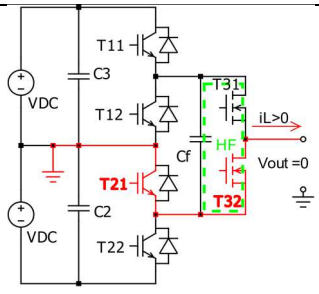
Fig. 4: High frequency (HF) damping effect of MnZn Ferrite cores. a) real implementation in 2SiC ANPC layout. b) voltage of T31 during turn-off with and without ferrite cores.

3. Low frequency oscillation active cut-off switching scheme

From Fig.2a, the oscillation circuit of LF makes a closed loop when both T11, T21 are on. The low frequency oscillation or the decoupling oscillation can be actively cut off by turning off either T11 or T21 if one of them does not carry the load current. In this paper, the switching states in table I.b is proposed based on that principle. The important thing is how to transit between the switching states safely with lowest switching losses and independent of the load current direction. One example for the transition from state P to ZP as describe in table II. is analyzed.

In the proposed switching scheme, the IGBTs are switched at the switching frequency but there are no switching losses because the switching is done at no load current. Moreover, the switching scheme is independent from the load current's direction because the current's location (upper or lower side of HANPC) is always defined when T31(upper side) or T32 (lower side) is on. These other transition $ZN \leftrightarrow N, N \leftrightarrow Z, ZN \leftrightarrow ZP$ use similar approach with the above example.

Table II: Transition from P to ZP

Step	Current direction IL < 0	Current direction IL > 0	Note
1			- State P: T11, T31: on. - Vout = VDC (P). - Load current is the red line of the circuit. The red color switches' names are the on state switches.When T31 is on, load current is always located on the upper side of ANPC with all its direction.
2			- T11, T31: on, T21 complemented to T11 is turned on, Vout = VDC. - LF loop is closed, LF starts oscillating - Load current is located on upper side of ANPC. T21(lower side of ANPC) is always turned on at no load current independent from IL's direction => no switching losses.
3			- Dead time: T11, T21: on, T31 is turned off - The oscillation in HF and LF are triggered when T31 is off. Load current is on T11 (upper side) if IL<0 and on T21 (lower side) if IL >0. - The switching state is independent from IL's direction.
4			-T11, T21: on, T32 is turned on -Vout = 0 (ZP) -When T32 is on, the load current is always relocated to the lower side of ANPC, no longer go through T11 with all IL directions. The switching state is independent from IL's direction.
5			- State ZP, T21, T32: on, T11 is turned off. - T11 is actively turned off to cut off the LF oscillation loop. - load current is located at lower side of ANPC. So T11 is always turned off at no load, no turn off losses. The switching state is independent from IL's direction.

The switching scheme is implemented in a FPGA and DSP controller board and do the experiment with the 2SiC hybrid ANPC. The result was measured at IL = 550A, VDC = 650V with ferrite cores the result showed that the low frequency oscillation or the decoupling oscillation is actively cut off at the time T11 is off when the inverter state transferred from P to ZP (Fig. 5).

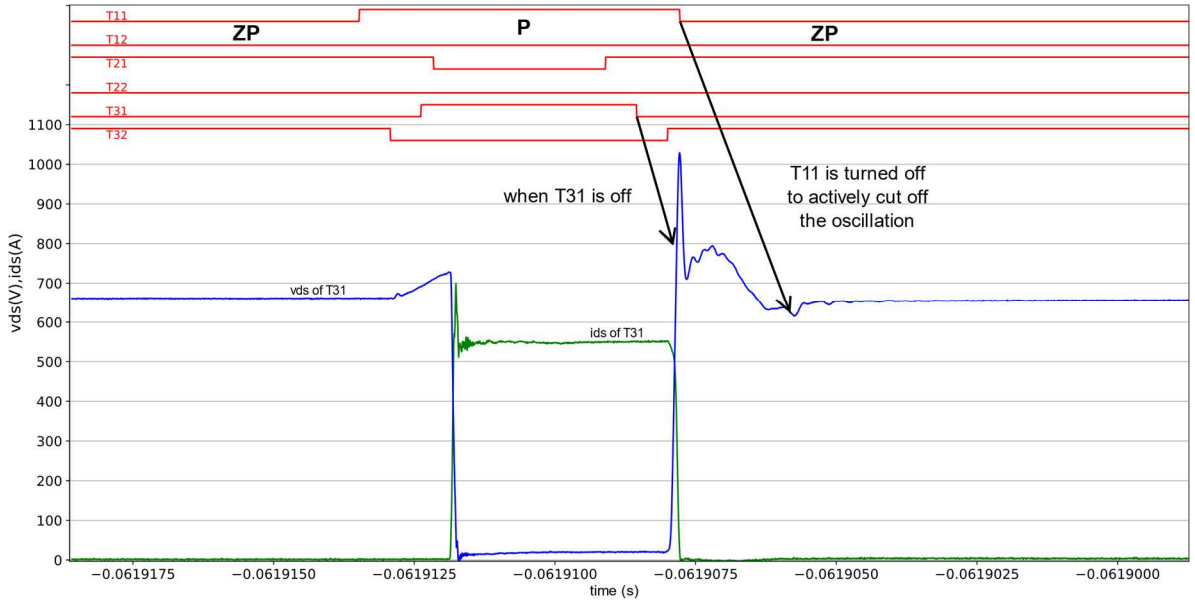


Fig 5: The decoupling oscillation (LF) on T31 is actively cut off during the transition from P to ZP.

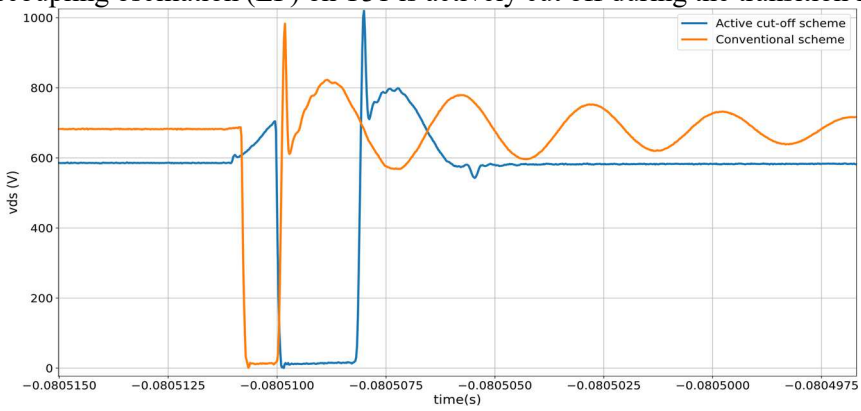


Fig 6: Compare conventional switching scheme and active cut-off scheme effect on the T31'svoltage oscillation when ANPC changed from state P to ZP (measured at different VDC)

Fig.6 shows the voltage of T31 during transition from state P to ZP with conventional switching scheme (measured at VDC = 750V) and with active cut-off scheme (measured at VDC = 600V). The decoupling oscillation or LF is cut off successfully right after the inverter reaching its new state ZP.

4. Decoupling capacitor

The decoupling capacitor C_f plays an important role in 2SiC hybrid ANPC topology. The value of C_f has to be large enough to decouple the large commutation loop and lower the oscillations' amplitude so that it is smaller than the overvoltage of the SiC MOSFET during turn-on and turn-off transient. During switching, there is current that charges and discharges C_f and causes losses on the internal capacitor's parasitic resistance (ESR) which can be heated up and destroy the capacitor. Those charging and discharging current are proportional to the capacitor value and hence set the upper limit value of the decoupling capacitor. The decoupling capacitor value can be estimated:
From equation (1), the maximum oscillation amplitude of the voltage across SiC MOSFET can be:

$$v_{dsmax} = VDC + I_L\left(\sqrt{\frac{L_{s1}}{C_f}} + \sqrt{\frac{L_{s2}}{C_{oss}}}\right) \quad (5)$$

If we assume that the voltage on the decoupling capacitor C_f is constant and equal to VDC during the switching transient. The voltage across the SiC MOSFET during turn-off after fully decoupled is:

$$v_{ds} = VDC - L_{s2}\frac{di_{ds}}{dt} \tag{6}$$

The value of C_f should be chosen so the maximum oscillation amplitude is smaller than the overvoltage of SiC MOSFET after decoupling. From (5), (6)

$$C_f \geq \frac{I_L^2 L_{s1}}{\left(I_L \cdot \sqrt{\frac{L_{s2}}{C_{oss}}} + L_{s2} \cdot \frac{di_{ds}}{dt}\right)^2} \tag{7}$$

During turn-on, the overvoltage on SiC MOSFET in the half-bridge depends on the reverse recovery current speed $\frac{di_{rr}}{dt}$. For SiC MOSFET the reverse recovery current speed is significantly fast at high temperature [22]. The overvoltage on SiC MOSFET during turn-on can be calculated:

$$v_{ds} = VDC + L_{s2}\frac{di_{rr}}{dt} \tag{8}$$

In the same manner like turn-off case. The value of C_f for turn-on

$$C_f \geq \frac{I_L^2 L_{s1}}{\left(-I_L \cdot \sqrt{\frac{L_{s2}}{C_{oss}}} + L_{s2} \cdot \frac{di_{rr}}{dt}\right)^2} \tag{9}$$

To protect the SiC MOSFET module during switching, the value of the decoupling capacitor should be satisfied both turn-on and turn-off cases.

$$C_f \geq Max\left[\frac{I_L^2 L_{s1}}{\left(I_L \cdot \sqrt{\frac{L_{s2}}{C_{oss}}} + L_{s2} \cdot \frac{di_{ds}}{dt}\right)^2}, \frac{I_L^2 L_{s1}}{\left(-I_L \cdot \sqrt{\frac{L_{s2}}{C_{oss}}} + L_{s2} \cdot \frac{di_{rr}}{dt}\right)^2}\right] \tag{10}$$

According to [20] the RMS current goes through the decoupling capacitor can be estimated

$$I_{cRMS} = I_L \sqrt{f_{sw}\left(\frac{L_{s1}}{R_{s1} + ESR} + \frac{1}{4}C_f(R_{s1} + ESR)\right)} \tag{11}$$

The power losses on decoupling capacitor is

$$P_c = ESR \cdot I_{cRMS}^2 = ESR \cdot I_L^2 \cdot f_{sw} \cdot \left(\frac{L_{s1}}{R_{s1} + ESR} + \frac{1}{4}C_f(R_{s1} + ESR)\right) \tag{12}$$

With ESR is the internal parasitic resistance of decoupling capacitor C_f.

(10) shows the minimum value of the decoupling capacitor to protect the SiC MOSFET module from overvoltage. From (1.a), the larger C_f value is, the smaller amplitude of low frequency oscillation. But the upper limit value of C_f is limited by its internal parasitic resistance ESR can be seen from equation (12) and the cooling conditions.

From equation (1.b), there is another option to increase the damping factor of both low and high frequency loop is increasing the external resistor R_f of C_f. This external resistor can be physically installed by using stainless steels plates as can be seen in Fig.7. Because stainless steel has resistivity 40 times higher than copper, this material increases R_f value enough to damp the oscillation without increasing internal temperature of the capacitor.

Fig 7. shows a capacitor assembly with 1.3 µF high power film capacitor with ESR = 0.3 mΩ, max Irms = 850A, 900 Vrms rated voltage. The capacitor is connected to the SiC MOSFET module using 2 stainless steel plates. The voltage measured on T31 during turning off in case of using 1.5 µF normal film snubber capacitor and in case of using this special capacitor assembly. The stainless steel plates showed a clearly damping effect on both 2 oscillation circuits.

During continuous running the inverter at full load current 300Arms for two hours, the capacitor's temperature reached maximum only 28°C at 20°C ambient temperature.

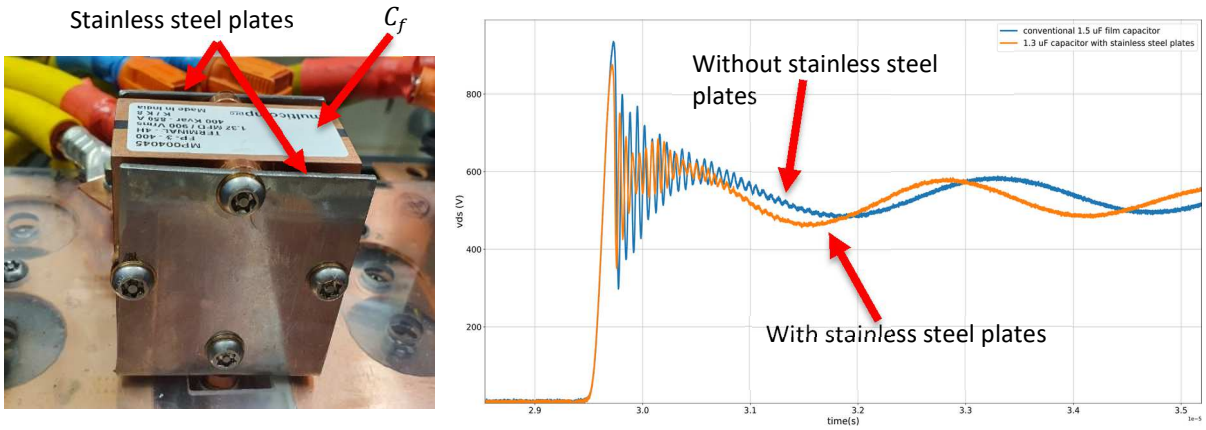


Fig 7: Decoupling capacitor with stainless steel plates assembly and the damping effect on both low and high frequency oscillation.

5. 500 kW 2SiC hybrid ANPC experiment.

The 500kW 2SiC ANPC (Fig. 8) was built to verify the damping concept. The inverter specification shows in table III.

Table III: 500kW 2SiC hybrid ANPC specification

Parameters	**Value**
Output power	520 kVA/500kW
DC link voltage	1500V
Output voltage	3Phases, 50Hz, VLL = 1000V
Output current	300Arms
Switching frequency	10kHz
Cooling method	Forced-air cooling

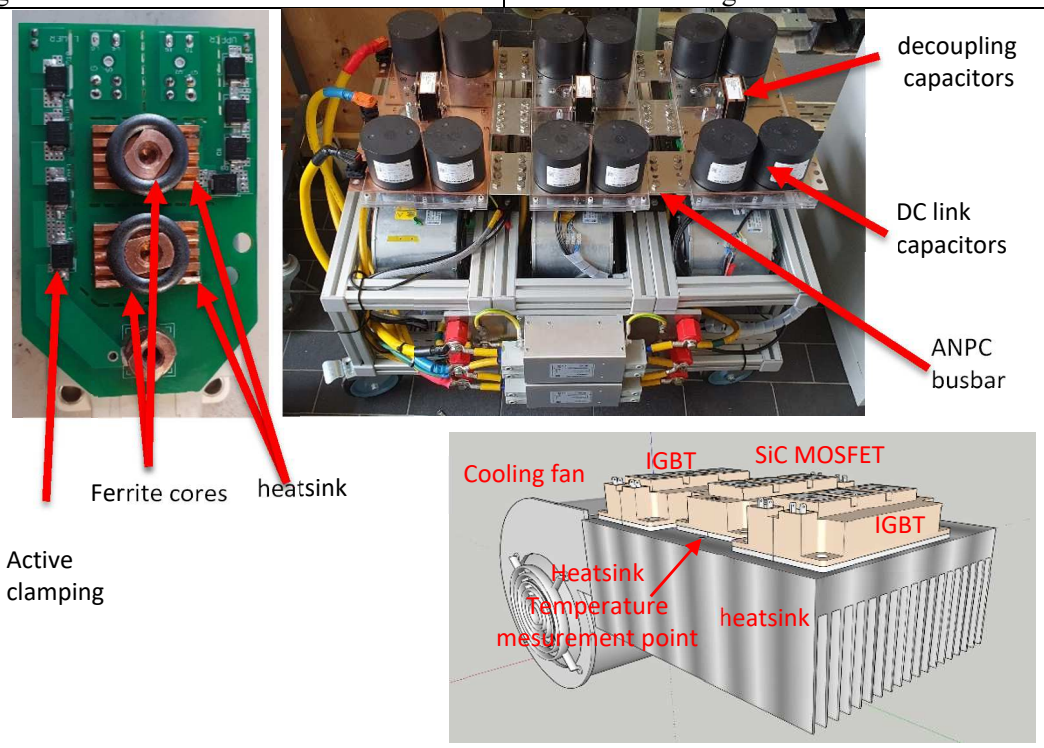


Fig 8: 500 kW 2SiC ANPC experiment inverter with forced-air cooling setup

To verify the damping effect of the damping scheme and check the temperature of critical components of the 2SiC ANPC during continuous running, one phase of the inverter was setup like in Fig 9. The

inverter was run continuously for 2 hours at 305 Arms load current without any problem. The temperatures of the critical components were also marked on Fig 9.

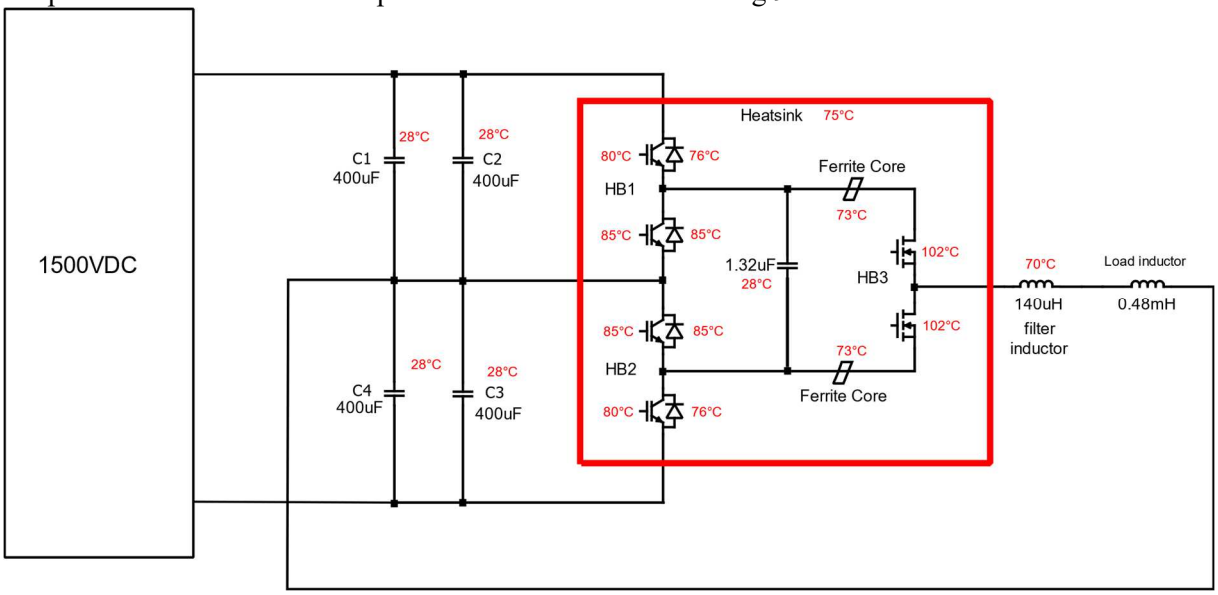


Fig 9: One phase 2SiC ANPC continuous test setup and its critical components' temperature at 305Arms for 2hours continuous running

The losses of all switches were simulated in Plecs at 305 Arms are shown in Table 4. And their junctions's temperature were also calculated in Table IV.

Table IV: Semiconductors' power losses and their junction temperature at 305 Arms load current.

	T11	T12	T21	T22	T31	T32	D11	D12	D21	D22	∑P
Ploss(W)	92	183	183	92	228	228	14	102	102	14	1238
Tj(°C)	80	85	85	80	102	102	76	85	85	76	

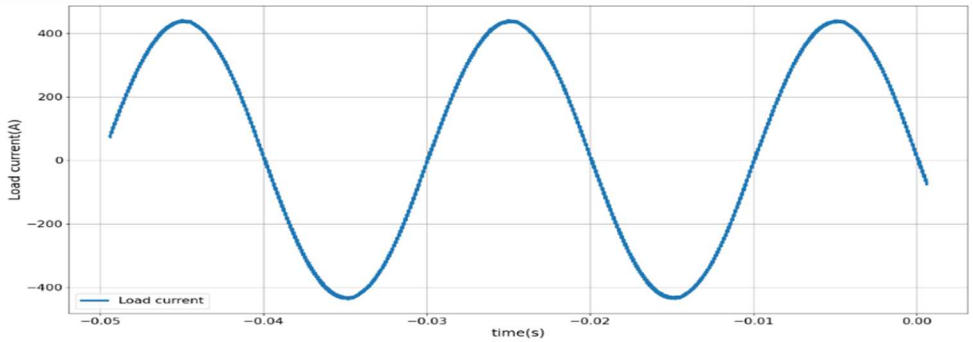


Fig 10: One phase load current waveform at 305 Arms

The experiment successfully archived the target designed at full load current 300Arms and had efficiency 99.25% (only semiconductors' losses) without overheating components. The switching oscillations are well damped by the special active cut-off switching scheme and ferrite cores. SiC MOSFET's junction temperature were still in the safe operating range.

Conclusions

In this paper, an experimental 500 kW 2SiC hybrid ANPC was presented and the switching oscillations of the SiC MOSFET module were successfully damped by using ferrite cores and a special active cut-off switching scheme. The paper also shows the method to choose the value of the decoupling capacitor and the possibility to damp the switching oscillations with stainless steel external resistance. The inverter was run at full load current for two hours without overheating its critical components. And the efficiency can reach 99.25% at rated current output.

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