Characterization of Online Junction Temperature of the SiC power MOSFET by Combination of Four TSEPs using Neural Network

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Keywords

«Condition monitoring», «Device characterization», «TSEP», «Silicon carbide», «Machine learning», «Neural network», «Wide bandgap»

Abstract

This paper presents an approach to combine multiple temperature-sensitive electrical parameters to improve the accuracy and precision of the junction temperature estimation of power transistors using the example of a silicon-carbide power MOSFET. Switching delays and the threshold voltage of the power transistor during turn-on and -off of a silicon-carbide power transistor are used as temperature-sensitive electrical parameters for the online junction temperature measurements. In order to improve the accuracy, a shallow fully-connected neural network is used as the means to combine the four measurements in one switching cycle of the transistor. The maximum measurement error of the junction temperature of the power transistor is reduced approximately 10-fold from 8.98 K to 0.92 K.

Introduction

The robustness and reliability of the power semiconductor devices in an application are critically affected by the junction temperature of wide-bandgap power transistors. The temperature swings and maximum temperature is the main cause of the failure in power electronics [1] which makes the knowledge of the operating temperature of the power transistor paramount. There are different methods depending on the usage and application that can be used to measure or estimate the junction temperature of the transistor. Some of them are physical contact where thermistors or thermocouples are positioned directly on or near the active chip area in order to get the temperature information on the junction of the power transistor. However, the issues like EMI and voltage isolation while implementing this method should be considered. There are also optical methods to measure the junction temperature of the transistor such as infrared sensor (IR). The exposure of a non-reflecting chip surface is required to have the two-dimensional temperature map of the transistor in order to use an optical method for the online junction temperature estimation [2]. Moreover, the optical measurements can lead to a bulky measurement setup and are difficult to implement in application. One of the most important methods to monitor the junction temperature of the power transistors is by measuring the change in the electrical characteristics of the transistor with temperature. These electrical parameters are called temperature-sensitive electrical parameters (TSEP) and have been widely used especially in the applications like the end of life estimation, condition monitoring, power cycling [3], and temperature control [2]. Some of the TSEPs and their dependencies are shown in Table 1.
The choice of the TSEP is highly dependent on the intended application usage. Some of the criteria to select a particular TSEP are temperature sensitivity, linearity, accuracy, invasiveness, complexity, and calibration need [4]. Most of the selection criteria are dependent on each other. For example, the non-linear behavior of the TSEP leads to high calibration needs in terms of measurement points. The

accuracy of a TSEP measurement decreases with the decrease in temperature sensitivity of the electrical parameter and makes the circuit more complex. Similarly, the invasive TSEPs which affect the normal operation of the transistor are complex and require more attention during calibration.

Table I: TSEPs and their dependencies [5, 6]

TSEPs	Threshold voltage	Transient delay	Drain-source voltage	Internal gate resistance	On-resistance
Dependencies	T_J	T_J, V_{DS}, I_D, R_G	T_j, I_D	T_J	T_J, V_{DS}, I_D

In this paper, the transient delays and quasi threshold voltage, both of them during turn-on and -off, so altogether four TSEPs, are used as the means of monitoring the online junction temperature of the power device, and an improved circuit is proposed to measure the same which is independent of the DC-link voltage. Then the results are used to train a shallow fully connected neural network to improve the accuracy of the temperature measurements in an online application.

Measurement concept

The quasi-threshold voltage $V_{th,q}$ and transient delays during turn-on and off of the SiC power transistors as TSEPs are measured to extract the information on the junction temperature of the transistor. The measurement circuits for quasi-threshold voltage and transient delays are adapted from [5] and [7] respectively. The block diagrams of the measurement circuit are shown in Fig. 1 and 2. Whenever there is a change in current flowing through the transistor during turn-on and -off switching transient, there is a voltage drop ($V_{SS'}$) across the parasitic inductance between power and Kelvin source of the transistor. For the measurement of quasi-threshold voltage, the $V_{SS'}$ is used as a trigger during turn-on and turn-off transient of the transistor. To generate these triggers, a comparator is connected across the power and Kelvin source terminal of the transistor which generates an output as soon as the $V_{SS'}$ goes higher than a certain reference voltage. This comparator is designed in a way that the trigger is generated before the transistor reaches the Miller plateau region. The dependencies from other electrical parameters are introduced in the Miller plateau region, therefore, the trigger generation in or after the Miller plateau is avoided. The output of the comparator is connected to a D flip-flop. The D flip-flop is used so that the measurement circuit is triggered only once in one switching cycle to avoid the false triggering due to the ringing in $V_{SS'}$ [5]. The two different circuits are used to measure the quasi-threshold voltage during turn-on and off transient. The only difference between the two circuits is the polarity of the comparator connected between the power and Kelvin source.

A commercially available time-to-digital converter (TDC) is used to measure the turn-on delay ($t_{d,on}$) and turn-off delay ($t_{d,off}$). A TDC requires two signals: first to start and second to stop its internal clock. The pulse-width modulated (PWM) signal from a function generator, which is temperature-independent,

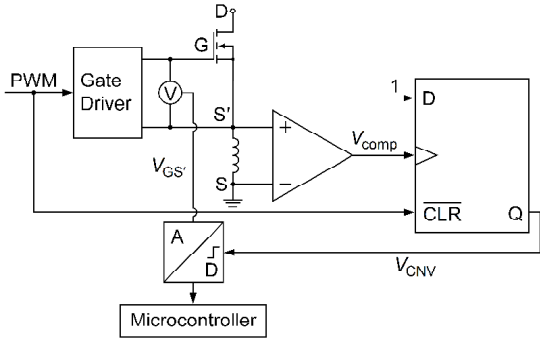

Fig. 1: Block diagram for quasi-threshold voltage measurements [5]

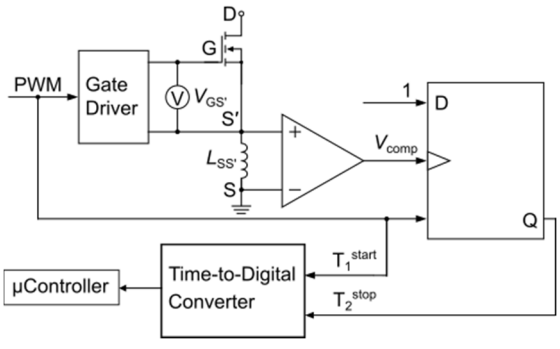

Fig. 2: Block diagram for quasi-threshold voltage measurements [7]

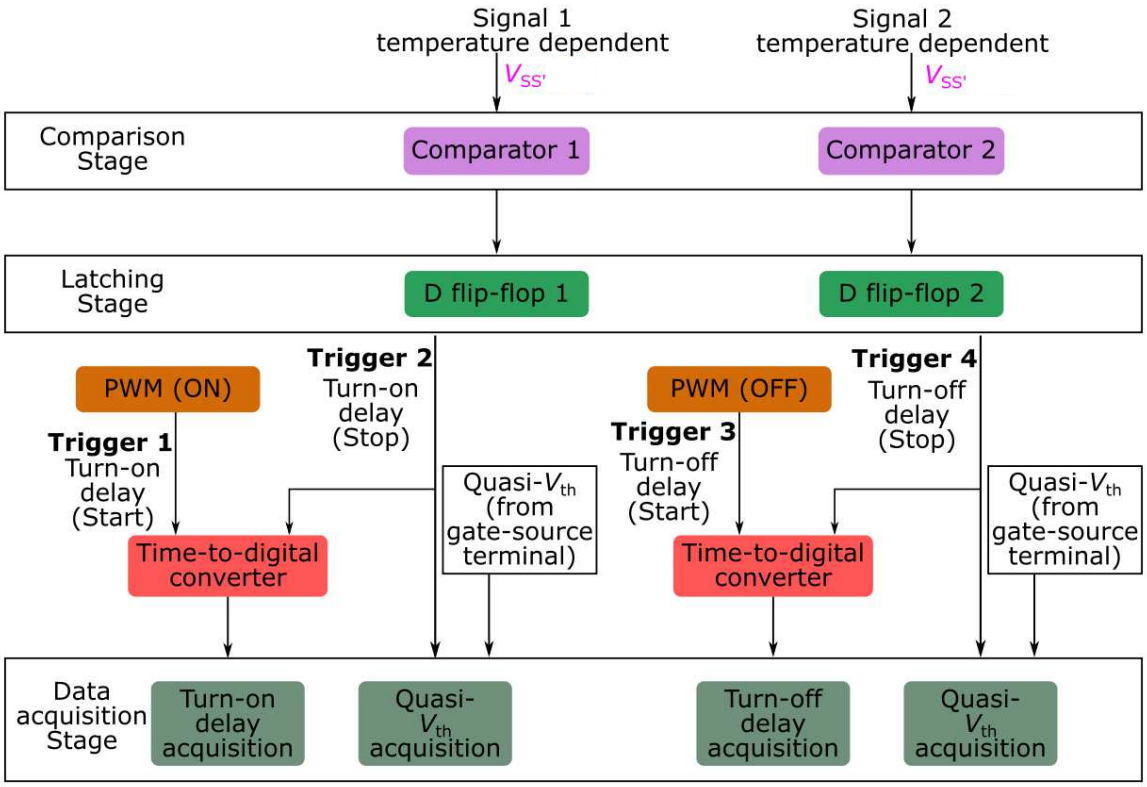

Fig. 3: Flow chart of all four TSEPs acquisition

is used as the first trigger to start the internal clock of the TDC. For the second trigger, which stops the TDC internal clock, the voltage drop across the parasitic inductance between Kelvin and the power source when the current flow changes in the transistor are used which is temperature-dependent [7]. The second trigger is the same which is used for $V_{\mathrm{th,q}}$ acquisition. A flow chart is shown in Fig. 3 to explain the trigger generation and the acquisition of all four TSEPs.

Although measured TSEPs have very little dependencies on other electrical parameters, the novelty of this paper lies in the combination of TSEPs using machine learning (ML) algorithms to further improve the accuracy of the measurements. This method eliminates the influence of the load conditions on junction temperature measurements of the power transistor because the data acquisition takes place before the Miller plateau, moreover, the shallow fully connected neural network takes these conditions into account.

Online Measurements

The proposed measurement circuit is implemented on a commercially available SiC power module. The device under test used in this research is BSM120D12P2C005 from ROHM [8]. The gate driver circuits in a half-bridge configuration are designed and implemented in buck converter topology. The proposed junction temperature measurement method is applied on the low-side of the half-bridge while keeping the high-side off. An inductive load of 150 µH is used as an inductive load. The temperature is varied from 25 ºC to 125 ºC. The measurements are performed on SiC power MOSFET for quasi-threshold voltage and transient delay with varying DC-link voltage from 100 V to 400 V in 100 V step and load current of 5 A and 10 A during turn-on and -off transition of the silicon carbide power module. The 10 Ω external gate resistor in a double pulse test setup and the data is generated to train the ML model. During turn-on transition, the results show that the $t_{\mathrm{d,on}}$decreases linearly with the increase in temperature with the temperature sensitivity of around -275 ps/K. This negative temperature coefficient is due to its relation with the threshold voltage. As the DC-link voltage is increased from 100 V to 400 V, the change in temperature sensitivity has a negligible change of around -30 ps/K. The linearization of

the raw data shows a root mean square error (RMSE) of 2.2 ns. Whereas for the threshold voltage during turn-on transition ($V_{\mathrm{th,q}}^{\mathrm{on}}$), the RMSE is 4 mV. The $V_{\mathrm{th,q}}^{\mathrm{on}}$ has a linear relationship with the temperature with a temperature sensitivity of around -7 mV/K. The negative temperature coefficient of $V_{\mathrm{th,q}}^{\mathrm{on}}$ is due to the increase in the carrier concentration and decrease in the bandgap. The measured value of the $V_{\mathrm{th,q}}^{\mathrm{on}}$ is decreased by 176 mV with the change in DC-link voltage from 100 V to 400 V whereas the change in temperature sensitivity is negligible. However, with the change in load current from 5 A to 10 A, the temperature sensitivity is increased to -11 mV/K and the threshold voltage is decreased by 667 mV. During the turn-off transition, the $t_{\mathrm{d,off}}$ also shows a linear relationship with the temperature sensitivity of 350 ps/K. When the load current is increased from 5 A to 10 A, the $t_{\mathrm{d,off}}$ is decreased by 25 ns but the temperature sensitivity remains similar. However, with the increase in DC-link voltage from 100 V to 400 V, the $t_{\mathrm{d,off}}$ is increased by 13.6 ns. The quasi-threshold voltage during turn-off ($V_{\mathrm{th,q}}^{\mathrm{off}}$) also has a linear relationship with the temperature. It has a temperature sensitivity of -1.1 mV/K. The RMSE between the raw and the linearized data is around 20 mV. With the increase in load current from 5 A to 10 A, the acquired $V_{\mathrm{th,q}}^{\mathrm{off}}$ increases by around 50 mV with a little increase in temperature sensitivity to -1.5 mV/K whereas with the increase in DC-link voltage from 100 V to 400 V, the $V_{\mathrm{th,q}}^{\mathrm{off}}$ decreases by 41.7 mV. The results are summarized in Table II.

Table II: TSEPs and their temperature sensitivities

TSEPs	Temperature sensitivity	Root mean square error (RMSE)	Temperature error (in K)
Turn-on delay	-275 ps/K	2.2 ns	5.71
Threshold voltage during turn-on	-7 mV/K	4 mV	1.98
Turn-off delay	370 ps/K	1.85 ns	3.08
Threshold voltage during turn-off	-1.1 mV/K	20 mV	8.98

The error and variation in the measured value of all TSEPs are due to the parasitics introduced by the measurement circuit. A machine learning model can be useful to improve the overall error by combining multiple TSEPs.

Combination of TSEPs

ML algorithms are in general capable of learning complex input (TSEPs) to output (temperature) mappings. For the training procedure, training samples are needed, where the input-output relationship is included. For supervised learning, labels are needed which determine the target output. Since the relations between the TSEPs and temperature exist but are hard to combine which can lead to better accuracy, ML algorithms can be a promising approach to estimate the temperature based on the obtained TSEPs. For the first investigation, the correlation between the parameters and temperature is determined by the calculation of Pearson's linear correlation coefficient between all pairs of variables as shown in Fig. 4.

The figure shows a high correlation between the individual TSEPs as well as between the TSEPs and the temperature. Just $V_{\mathrm{th,q}}^{\mathrm{on}}$ shows a slightly lower correlation (-0.96) with the temperature compared to the other three TSEPs (-1, 1, -0.99). Two assumptions can be made based on this evaluation.

- The junction temperature of the power transistor can be estimated based on the given TSEPs data

- Individual TSEPs should also be used to estimate the junction temperature of the power transistor because of the high correlation between e.g. $V_{\mathrm{th,q}}^{\mathrm{on}}$, $t_{\mathrm{d,on}}$, $t_{\mathrm{d,off}}$ and the temperature

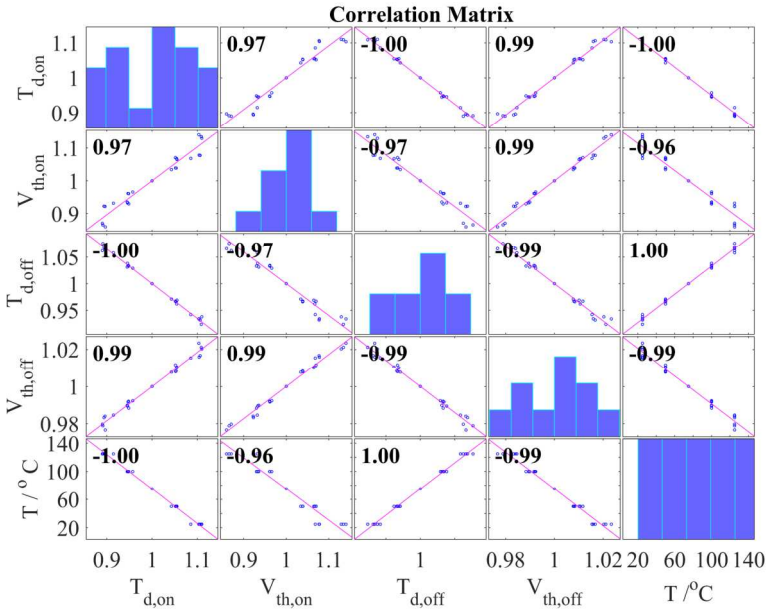

Fig. 4: Correlation coefficients between all TSEPs and temperature

A simple shallow fully connected neural network is used for estimating the junction temperature of the power transistor. In a fully connected layer, all neurons are connected to the outputs of the previous layer. Each connection has a weight parameter w_{i}, which is adjusted during training. Per neuron, one bias parameter b exists. The final output y_{i} of the neuron i in a fully connected neural network is given by equation 1 with the (non-linear) activation function σ.

$$y_{\mathrm{i}} = \sigma(w_1 x_1 + \cdots + w_{\mathrm{m}} x_{\mathrm{m}} + b) \tag{1}$$

The network contains four layers, an input layer where the number of neurons is equal to the number of input parameters, two hidden layers with 10 and 5 neurons, and an output layer with one neuron for the junction temperature. The hidden layers use rectified linear unit (ReLU) activation function and the output layer uses a linear activation function. The basic architecture is shown in Fig. 5.

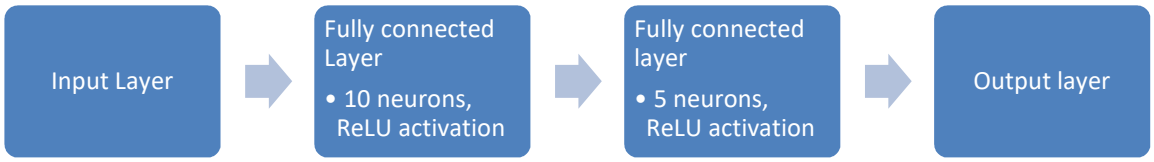

Fig. 5: Architecture of the shallow fully connected neural network

The network is trained for 100 epochs and the dataset is split randomly into 80% training data (32 measurements) and 20% test data (8 measurements). First, the neural network is trained with all four investigated TSEPs. Fig. 6 shows the prediction of the trained network on unseen test data. For each obtained parameter vector, estimation is performed. Therefore, the network can predict the temperature each time the TSEPs are sampled. The model shows promising results with a mean absolute temperature deviation of 0.92 K on the test data. The neural network is also trained with each TSEP as an input

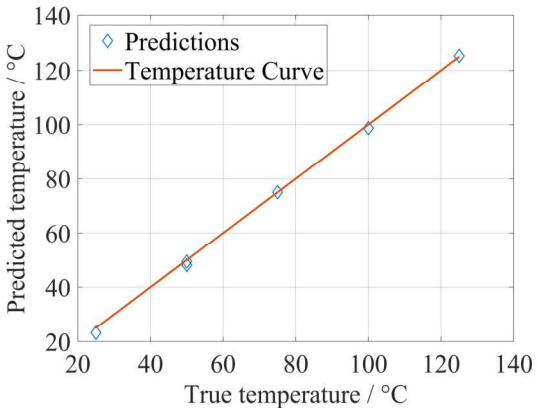

Fig. 6: Temperature predictions of the neural network (all TSEPs) on unseen test data

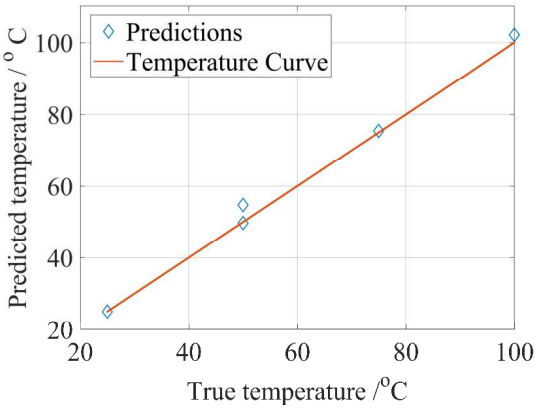

Fig. 7: Temperature predictions of the neural network ($t_{\mathrm{d,on}}$) on unseen test data

before combining them. The network which is trained with $t_{\mathrm{d,on}}$ as an input parameter shows best temperature prediction among models with other individual TSEP as input. Therefore, the prediction on unseen test data of $t_{\mathrm{d,on}}$ is shown in Fig. 7. The model is also able to estimate the temperature well with a mean absolute temperature deviation of 1.05 K on the test data. Table III shows the improvement in the accuracy of measured TSEPs after processing with the ML algorithm.

Table III: TSEPs and their mean temperature deviation

Transition	TSEP	Mean absolute temperature deviation (in K)
Turn-on	Delay time	5.71
	Quasi-threshold voltage	1.98
Turn-off	Delay time	3.08
	Quasi-threshold voltage	8.98
Combined TSEPs		**0.92**

For further evaluation of the model learning behavior, the model for the combined TSEPs is trained with 20 to 100 epochs with a step size of 20. The obtained mean temperature deviation (in K) is shown in Table IV, with the mean results over five independent runs.

Table IV: Performance for different number of epochs with combined TSEPs

Number of Epochs	Mean absolute temperature deviation (in K)
20	3.05
40	2.39
60	1.43
80	**1.37**
100	1.57

The results of the table show, that already from 60 epochs on, good results can be obtained, while with 80 epochs the best mean performance over five independent runs are achieved. Therefore, 80 epochs are further used for model training. Until now, the data was split randomly into 80% training data (32 measurements) and 20% test data (8 measurements). As the next step, the model's capability of learning with a limited amount of training data shall be proved. Therefore, the ratio of training and test data will be changed from 20% training data to 80 % training in steps of 15%. The mean results of five independent runs for each split are shown in the following Table V.

The best results are obtained with the highest number of training data. However, already with 20 measurements as training data, better results are obtained than with the best single TSEP model (see Table III). From 20 measurements on, the performance of the model just slightly improves, so it can

also be used with less training data than the previously selected 32. However, a decrease in performance has to be considered for this.

Table V: Performance for different amounts of training data with combined TSEPs

Number of measurements in training data	Mean absolute temperature deviation (in K)
8	5.72
14	2.84
20	1.88
26	1.59
32	**1.37**

For TSEPs noise and measurement, inaccuracy is always a big factor and one of the main reasons adoption of that measurement principle is difficult in the application. A small change in the measured parameter usually causes a huge estimation error. Therefore, the effect of adding noise to the measurement data is investigated in this paper. White Gaussian noise with mean zero and different values for the variance is added to the normalized signal (normalized to [0, 1]) and the final estimation performance of the model on test data over five independent runs is shown in Table VI. The variance was set to the values of 0.001, 0.005, 0.01, and 0.05.

Table VI: Performance for different variance values

Variance for noise generation	Mean absolute temperature deviation (in K)
0	**1.37**
0.001	2.66
0.005	3.51
0.01	4.96
0.05	18.82

The performance is drastically decreasing with added noise. With small variances (e.g. 0.005) the performance is in a similar range, but above 0.01 variance, the deviation of the estimation to the original value is becoming worse. Therefore, the model needs to be further adjusted for added noise in the measurements to become robust against measurement inaccuracies and noise.

It is assumed, that the accuracy of the temperature estimation can further be improved by using the additional temperature-sensitive parameter as an additional input. However, the results with the combined TSEPs are already promising and serve as a strong baseline for further work.

The temperature sensitivity after combining the TSEPs using neural networks cannot be determined because the neural network works as a black box with many non-linear behaviors. Each neuron in the model adds a non-linearity. However, the capability of the neural network as a universal function approximator offers the possibility to model arbitrary complex relationships and establish correlations between individual and combined TSEPs.

Conclusion

The junction temperature of the power transistor is measured via temperature-sensitive electrical parameters. Four TSEPs are considered here, namely the quasi-threshold voltage and the delay times during turn-on and turn-off. The data generated from the measurements are used to improve the accuracy of the measurement by training a shallow fully connected neural network. The maximum error in the measurement is reduced from 8.98 K to 0.92 K. The temperature sensitivities after combining the TSEPs are not possible to calculate since the used machine learning algorithm works as a black-box. However, there is a possibility to calculate second or third-order polynomial approximation using a symbolic regression algorithm in the machine learning model.

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