Difference in the design process of LCL filters for grid connected VSI when using SiC/GaN instead of Si semiconductors

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Abstract

Although the design of LCL filters has been discussed extensively in recent years, the different requirements for the design process when using SiC/GaN semiconductors instead of classical Si semiconductors have not been presented in detail. Due to the higher switching frequency, new EMI limits in lower frequency range and other influencing factors, there are some differences, which must be taken into account in the design process. This enables a more resource-saving use of materials as well as a faster development time.

Introduction

LCL filters are used to reduce voltage and current harmonics of grid-connected inverters (VSI) to an acceptable level. A good design of the values of the three elements L_1, L_2 and C is crucial to keep the harmonics on the one hand and the costs, losses and size low enough on the other hand.

Classical LCL filter design process and evaluation when using SiC/GaN semiconductors

In this section, the classical design process of LCL filters in the literature is presented and discussed in terms of usability in SiC/GaN VSI.

Equivalent circuit assumed for the design

Typically, the equivalent circuit in Fig. 1 (left) is assumed when designing LCL filters [1]. The line impedance is neglected because the filter inductance values are significantly higher than the line impedances.
→When using SiC/GaN semiconductors, a much higher switching frequency is often used. As a result, the inductance values related to the inverter power are significantly lower and the line impedances should no longer be neglected in the filter design. In addition, the switching frequency with SiC/GaN mostly lays within EMI limits, especially since standards were extended down to 9kHz, i.e. [19].

Therefore, a line stabilization network (LISN, [18]) should be considered at least for designing the filter attenuation, Fig. 1 (right).

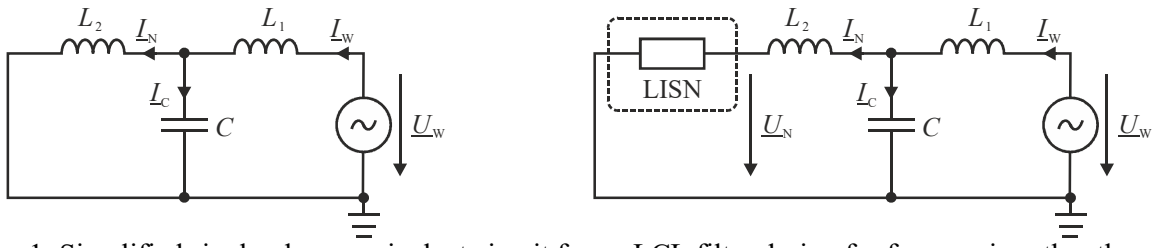

Fig. 1: Simplified single-phase equivalent circuit for an LCL filter design for frequencies other than the grid frequency most used in literature (left) and minimum required equivalent circuit (right) if switching frequency is in the frequency range of EMI-limits.
U_W = inverter output voltage, I_W = inverter output current, U_N = grid voltage, I_N = grid current.

Determination of a maximum total inductance

The maximum total inductance L_1+L_2=L is defined by the permissible voltage drop across the filter at grid frequency ω_g. In [10] the maximal inductance is limited by the control dynamics. The inductance is often defined <5% [1] up to <10% [3] of the phase voltage of the network. The higher the inductance, the higher the required DC link voltage of the converter to be able to feed energy into the grid against the grid voltage.

$$L_{max} = \frac{(0{,}05 \dots 0{,}15) \cdot U_N}{\omega_g \cdot I_N} \tag{1}$$

→Due to the often higher switching frequency when using SiC/GaN, the inductance required for the filter effect is so low that the maximum voltage drop is mostly not a design criterion anymore.

Determination of the minimum inverter side inductance L_1

In practice, the dominant approach is to define a maximum current ripple through the inverter-side inductance and calculate the inductance required to achieve it. The "x" depends on the converter topology, modulation method and modulation factor.

$$L_{1,min} = x \cdot \frac{U_{ZK}}{f_s \cdot \Delta I_{Pk-Pk}} \tag{2}$$

Where U_{ZK} = DC link voltage ΔI_{Pk-Pk} = peak-peak current ripple f_s = switching frequency

The current ripple is usually limited by the RMS value to max. 10% of the rated current RMS [1], [2], [4]. Only few papers suggest higher ripple values like 20% [5], [6], 30% [7] or even 40% [8].

The reason for limiting the current ripple to low values is, on the one hand, to limit the core losses as well as the additional copper losses of the inverter-side inductance L_1. This is very relevant for IGBT inverters, since the switching frequencies are so low that the inverter-side inductance is often designed with a core made of electrical steel and a solid copper conductor. Eddy current core and conductor skin- and proximity losses might become critical.

→ For SiC/GaN converters, however, the switching frequency is normally so high that the inductance on the converter side is designed with ferrite, powder or nanocrystalline core material and HF stranded wire. These inductors could carry significantly higher ripple currents.

Second, for at least older IGBT semiconductors, turn-off switching losses are higher than turn-on switching losses.

→ For SiC/GaN semiconductors turn-off losses are lower than turn-on losses. Thus, with increasing ripple, switching losses tend to increase for IGBTs while for SiC/GaN switching losses tend to decrease with increasing ripple [cmp. 9]. This can be seen, looking at the datasheet values of an older IGBT and a SiC MOSFET. Therefore, more ripple current can be accepted with SiC/GaN in comparison to IGBT.

Table I: Comparison of the relation between turn-on and turn-off energy of SIC MOSFET [11] and IGBT [12]

Type	Turn-on energy E_{on}	Turn-off energy E_{off}
IMZ120R045M1 CoolSiC 1200V SiC Trench MOSFET	280µJ	70µJ
IGW15T120 TrenchStop IGBT	1300µJ	1400µJ

Third, the ripple current has also an effect on the capacitor design, as it increases the RMS value of the capacitor current and therefore the size and costs of the capacitor.
→ Because the equivalent series resistance ESR of a foil capacitor is decreasing with frequency, higher ripple currents can be tolerated for high switching frequencies with SiC/GaN semiconductors in comparison to IGBT converters.

Determination of the grid side inductance L_2

For a given capacitance and total inductance L, the optimum filter effect can be achieved if L_1=L_2, since the resonance point is then at the lowest frequency and the filter therefore has higher attenuation at higher frequencies [3]. However, due to a high load on the converter and the inductance on the converter side caused by high ripple currents, a different ratio is often selected in practice. The ratio is often set to $a = 2$ according to the authors experience.

$$L_1 = a \cdot L_2 \tag{3}$$

→As shown above, when SiC/GaN semiconductors are used, higher ripple currents and thus a smaller inverter-side inductance L_1 can be used. This means that the optimum ratio $a = 1$ regarding the filter effect can be used in the design.

Checking the filter resonance point range

The resonance frequency f_r should be placed with a suitable distance between the grid frequency f_g and the switching frequency f_s. A usual placement of the resonance point in practice is [1], [3], [13]:

$$5 \ldots 10 \cdot f_g < f_r < \frac{f_s}{2}. \tag{4}$$

→This design rule is just as valid when using SiC/GaN semiconductors as it is for IGBTs, but with larger design space.

Choice of capacitor value

In [1], [2], [3], [4], [5] and [6], the capacitor C is first specified by the maximum permissible reactive power in order not to generate too high additional load for the inverter. Values between 5% and 15% [6] of the inverter rated power P_N are mentioned.

$$C_{max} = \frac{(0{,}05 \ldots 0{,}15) \cdot P_N}{3 \cdot \omega_g \cdot U_N^2} \tag{5}$$

Where ω_g= fundamental grid frequency U_N= grid voltage

Especially for high power IGBT converters with correspondingly low switching frequency, this limit is very relevant and important for the design process.
→However, when using SiC/GaN semiconductors and a much higher switching frequency, the resonant frequency of the LCL filter is accordingly much higher. Therefore, the design criterion is irrelevant here, because a maximum limit of the capacitor is never reached in these applications.

Filter effect: Checking the attenuation of switching-frequency components

Typically, the gain of the inverter-side current ripple to the line-side current ripple is calculated as follows [1]:

$$\frac{\underline{I}_N(h)}{\underline{I}_W(h)} = \frac{1}{|1 + r \cdot (1 + \alpha \cdot x)|} \tag{6}$$

Where

$$\alpha = \frac{L_1 \cdot \omega_s^2}{\omega_g \cdot \frac{U_N^2}{P_N}} \qquad r = \frac{L_2}{L_1} \qquad x = 0{,}05 \ldots 0{,}15 \ (\%\ of\ P_N) \tag{7}$$

Here, a damping of 20% [1] is often proposed. Hamonic limits, i.e. from IEEE519 are considered in some papers [1], [4] or [14] to set the attenuation.

→A fundamental problem with this approach is that limits of EMI standards >2kHz are not taken into account in the design. Today, there are EMI limits at least for the frequency range 9kHz-150kHz [19], [21] and up to 30MHz [20]. Examples are given in Fig.2.

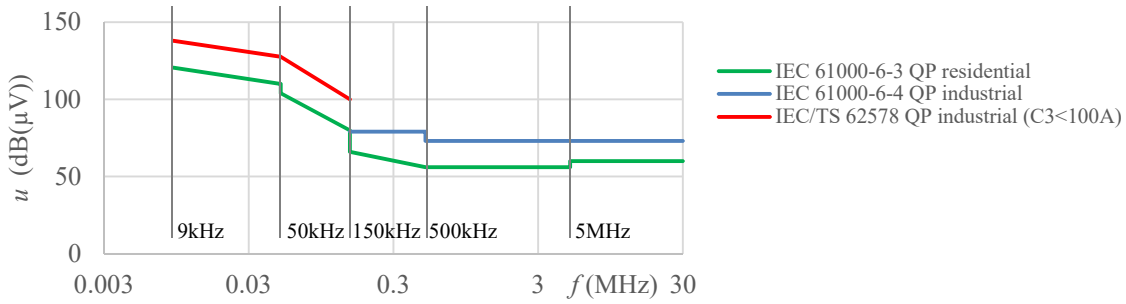

Fig. 2: Example limit values QP for interference voltages.

Typical switching frequencies of SiC/GaN usually lie exactly in this frequency range. Ignoring these limits in the design process, the filter values must be adjusted again and again in practice.
Here, it is now proposed to keep at least the switching frequency component of the grid voltage compared to the standard limit value at switching frequency $\underline{U}_{N,limit}$. To calculate the corresponding max. grid ripple current, formula (8) can be used.

$$\underline{I}_{N,max}(\omega_s) = \frac{\underline{U}_{N,limit}(\omega_s)}{\underline{Z}_{LSIN}(\omega_s)} \tag{8}$$

The necessary current attenuation is calculated by

$$\frac{\underline{I}_{N,max}(\omega_s)}{\underline{I}_W(\omega_s)} = \frac{1}{X_C(\omega_s) \cdot (X_C(\omega_s) + X_{L2}(\omega_s) + Z_{LSIN}(\omega_s))} \tag{9}$$

The minimum required capacitor value can be found by resolving equation (9) to *C*.

→ Although this dimensioning of the capacitor value is much better than previous rules of thumb in the literature, it only provides a good starting value for the filter design. Especially due to the higher switching frequency when using SiC/GaN, parasitic effects of real components like inductors, capacitors, semiconductors, layout, cables etc. are all the more influential in the actual EMI emission. In addition, the component values of LCL filters and additional required components for higher frequency EMC compliance such as Y-capacitors and common-mode chokes are closer to each other, so they actually need to be considered together when designing LCL filters.

Control consideration and Damping

Passive or active damping for LCL filter is widely discussed, i.e. in [1],[3], [15], [16] or [17]. The current control closed loop might be unstable because of the filter resonance frequency. This is especially important for the design of LCL filters for high power IGBT inverters with low switching frequencies and therefore low filter resonance frequencies near to the bandwidth of the controller dynamics.

→If it is again assumed that the switching frequencies are significantly higher when using SiC/GaN instead of IGBT, the stability considerations concerning current control become less relevant. The filter resonance point lies in a significantly higher frequency range and thus at a far distance from the control bandwidth, if huge invests in control components should be avoided.

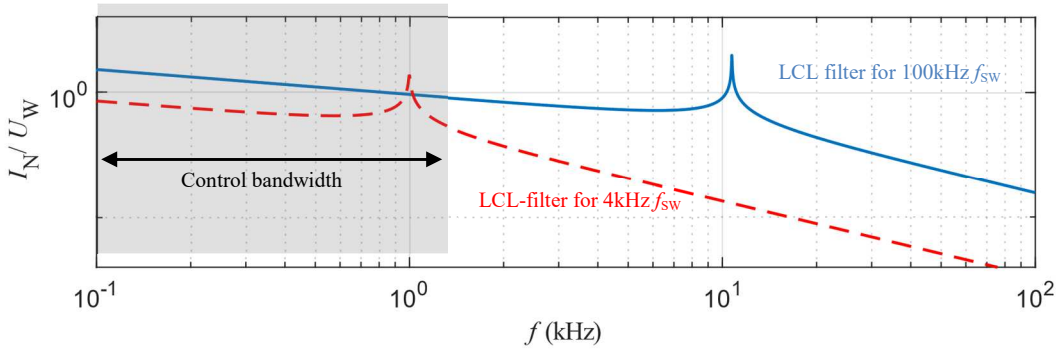

Fig. 3: Resonant frequency of the LCL filter for 4kHz and 100kHz switching frequency compared to the control bandwidth.

However, the range around the resonant frequency must be damped to prevent excessive excitation by the output voltage of the VSI or other voltage sources from the mains. But in contrast to the literature on the design of damping at low switching frequencies, at high switching frequencies with SiC/GaN, significant damping can already be accounted for and utilized by the parasitic properties of the inductors, see [22] and [13], as well as the cables, terminals and other system components. Only the still missing damping must then be supplemented by additional passive damping resistors.

Conclusion

In this paper, the classical design of LCL filters is critically discussed with respect to applicability to SiC/GaN inverters. It turns out that some steps of the classical design are no longer as relevant as for IGBT converters due to the usually higher switching frequency. There are also new design criteria. For example, the influence of the grid impedance due to smaller component values as well as new EMI limits in the frequency range down to 9kHz. The parasitic behavior of the components is very important and the design of the LCL filter should be made considering also the high frequency EMI-filter components. The evaluation shown here allows LCL filters for SiC/GaN converters to be designed with more background knowledge and gives opportunity for a faster design with less material invest.

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