Utilizing the Reactive Current Control Capability of an MMC-Fed AC/DC Converter for Volt-Second Balancing in Medium Frequency Transformers

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Keywords

≪Charging infrastructure for EVs≫, ≪Grid-connected converter≫, ≪Modular Multilevel Converters (MMC)≫, ≪AC-DC ≫, ≪Transformer ≫.

Abstract

The non-ideal behavior of power switches and/or circuit asymmetries in transformer-isolated converters can result in nonzero average voltage across the transformer terminals, which, in turn, can saturate the transformer. In this paper, a volt-second balancing scheme is developed for a Modular-Multilevel-Converter (MMC)-fed AC/DC converter to avoid transformer saturation.

Introduction

Rising adoption of Electric Vehicles (EV) and introduction of EVs with large battery capacities, such as electric trucks, demand Medium-Voltage (MV) connected ultra-fast charging stations [1, 2]. Here, a transformer is needed to provide the galvanic isolation and step down the MV grid voltage to a level that is suitable for EV battery charging. Typically, an MV-connected 50 Hz transformer at the required power level has a large volume, which can be reduced considerably by using a transformer that operates in the Medium-Frequency (MF) range. In this regard, MMC-based chargers are getting more popular [3]. Fig. 1 shows a typical structure of an MMC-based ultra-fast charger, where the MMC, followed by an MF transformer and a zero-voltage switched AC/DC converter, converts the grid voltage to an MF voltage wave [4].

The MMC-based charger comprises a transformer-isolated converter. In such a converter, preventing DC bias in the transformer magnetizing flux is critical, as it can take the transformer core outside its linear operation region. This bias can result from any mismatch in the applied volt-seconds to the transformer primary and secondary windings [5, 6]. Since the primary winding average current is often closed-loop controlled by the MMC, the applied voltage to the primary winding is free of a DC component [3]. On the other hand, the secondary winding is likely to be excited with a DC biased voltage through the Low-Voltage AC/DC converter (LVC). As a remedy, the average current of the secondary side can also be controlled to avoid DC bias, but this demands additional sensing circuity and control complexity. Passive methods are also used to avoid transformer saturation, such as the introduction of a DC-blocking capacitor, inclusion of an air gap in the transformer core, and overdimensioning the flux density, which

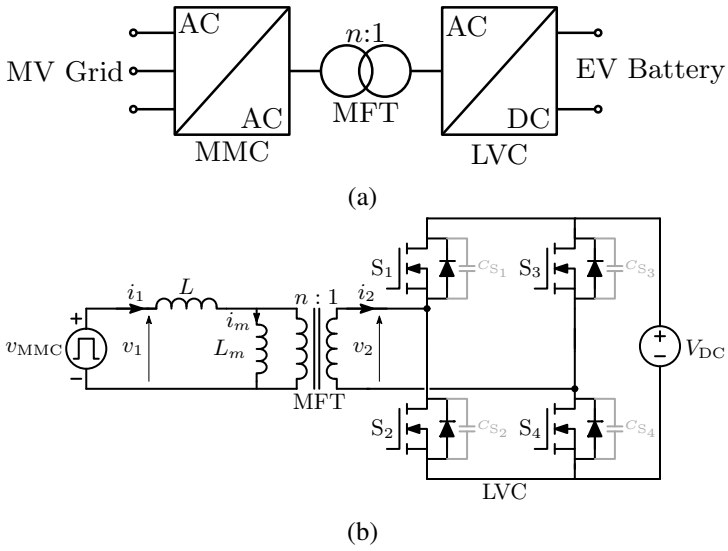


Fig. 1: (a) Block diagram of an MMC-based ultra-fast charger, (b) AC/DC converter with equivalent circuit model of the MMC and the MFT.

result in additional volume and/or power losses [5]. In [7], it is shown that a zero-voltage switched active bridge can compensate a small part of the net volt-seconds it undesirably applies to the transformer. The resulting DC component in the bridge current positively modifies the voltage waveform of the bridge within the switching transitions. This compensating effect becomes more pronounced when decreasing the switching current. This effect was exploited in [8] in a modified modulation strategy for a dual-active bridge (DAB) to restrict the switching current and enhance the inherent volt-second balancing effect of the bridge. This modulation strategy uses inner phase shift angles within each H-bridge in addition to the outer phase shift angle between primary and secondary bridges, thereby bringing about additional control effort.

In the MMC-fed LVC, the switching current of power devices can be easily modified by adjusting the reactive current drawn from the MMC [4, 9]. Here, the MMC acts like a controlled voltage source, which can be used to control the active and reactive terms of its terminal current separately. The objective of this paper is to employ the reactive term to control the switching current of the LVC, thereby minimizing the steady state volt-second imbalance. An analytical relationship between the transformer reactive current and resulting offset current through the transformer is derived, and the analysis is verified with simulations.

Volt-second balancing

The inherent volt-second balancing of the LVC can be analytically quantified. This in turn allows it to be enhanced by changing the available free parameters.

Inherent volt-second balancing

Fig. 2 shows the voltage and current waveforms of the LVC and magnetizing current of the transformer under both normal operation and in the presence of an offset current due to a timing error t_{err} in the switching cycle. During normal operation, the LVC switches with a constant duty cycle of 50% in a ZVS manner. In a zero-voltage switched bridge, the transitions of the AC-terminal voltage from $+V_{\text{DC}}$ to $-V_{\text{DC}}$ (or vice versa) are not instantaneous, and the transition time is determined by the commutation process of the power switches [8], which is governed by the charging and discharging of the output capacitances of the power switches in the bridge legs. If the switching current I_{sw} remains relatively constant during the switching transition, the commutation time is given to a good approximation by

$$t_{\text{cmt}} = \frac{C V_{\text{DC}}}{I_{\text{sw}}}, \tag{1}$$

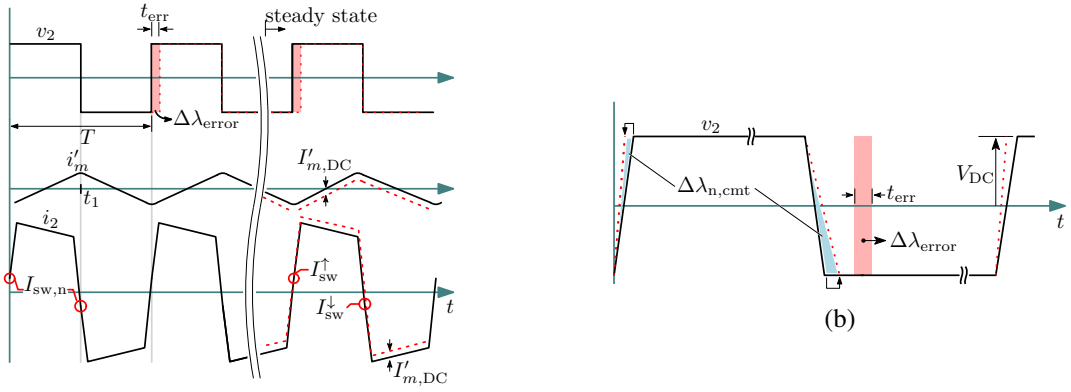


Fig. 2: (a) Nominal and DC-biased waveforms of the converter, where the solid lines and red-dotted lines indicate normal operation and operation under a DC bias, respectively, (b) the enlarged secondary voltage during switching transitions.

where C denotes the switch-node capacitance, the equivalent capacitance of the parallel connection of high- and low-side switch output capacitances (see Fig. 1b). As shown in Fig. 2b, during normal operation, the switching currents and therefore commutation times are the same for both rising and falling edges of the secondary voltage $v_2(t)$. Hence, given the half-cycle symmetry, the net volt-second area is zero in each switching cycle (see Fig. 2b). In case of a timing error t_{err} in the LVC due to the deviation of duty cycle from 50%, $v_2(t)$ will have an undesired net volt-second component $\Delta\lambda_{\text{error}}$ equal to $2t_{\text{err}}V_{\text{DC}}$. Subsequently, a finite DC current component will flow through the LVC and magnetizing path of the transformer, providing that there is a nonzero resistance in the DC current path. As can be seen from Fig. 2b, in this case, the switching currents are no longer the same for the rising and falling edges of $v_2(t)$ and–providing the fact that the LVC still switches in a ZVS manner–they are, respectively,

$$\begin{cases} I^{\uparrow}_{\text{sw}} = I_{\text{sw,n}} - I'_{m,\text{DC}} \\ I^{\downarrow}_{\text{sw}} = I_{\text{sw,n}} + I'_{m,\text{DC}} \end{cases}, \tag{2}$$

where $I_{\text{sw,n}}$ and $I'_{m,\text{DC}}$ represent the switching current during normal operation and the secondary referred DC component of magnetizing current under DC-biased operation, respectively. Hereafter in this paper, the prime notation indicates secondary-referred primary quantities. According to (2), the commutation times will differ, or equivalently the switching transitions will be faster in one edge compared to the other edge of $v_2(t)$. As can be seen from Fig. 2b, this will create a net volt-second contribution $\Delta\lambda_{\text{n,cmt}}$ (blue-shaded area) partially compensating the original undesired net volt-second component $\Delta\lambda_{\text{error}}$ (red-shaded area). Using (1), the compensating net volt-second component is found to be

$$\Delta\lambda_{\text{n,cmt}} = \left(\frac{CV^2_{\text{DC}}}{I_{\text{sw,n}}} - \frac{CV^2_{\text{DC}}}{I^{\uparrow}_{\text{sw}}}\right) - \left(\frac{CV^2_{\text{DC}}}{I_{\text{sw,n}}} - \frac{CV^2_{\text{DC}}}{I^{\downarrow}_{\text{sw}}}\right). \tag{3}$$

Substitution of (2) into (3) yields

$$\Delta\lambda_{\text{n,cmt}} = -\frac{2I'_{m,\text{DC}}CV^2_{\text{DC}}}{I^2_{\text{sw,n}} - I'_{m,\text{DC}}}. \tag{4}$$

The other counteracting effect against the imbalanced net volt-second is the DC voltage drop over the resistance of the DC current path which is

$$R_{\text{DC}} = 2R_{\text{DS-on}} + R_{\text{s,w}} + R_b, \tag{5}$$

where $R_{\mathrm{DS-on}}$, $R_{\mathrm{s,w}}$, and R_b represent the drain-source on resistance of the MOSFETs in the LVC, the secondary winding resistance, and the internal resistance of the EV battery pack, respectively. This resistance compensates for the volt-second imbalance by

$$\begin{aligned}\Delta\lambda_{\mathrm{n,R}} &= -V_R\,T \\ &= -R_{\mathrm{DC}}\,I'_{m,\mathrm{DC}}\,T,\end{aligned} \tag{6}$$

with T the switching period. Considering the (typically) low value of R_{DC}, the resulting offset current is so large that the transformer core can be driven into saturation.

At steady state, the volt-second balance of the circuit can be expressed as

$$\Delta\lambda_{\mathrm{error}} + \Delta\lambda_{\mathrm{n,R}} + \Delta\lambda_{\mathrm{n,cmt}} = 0. \tag{7}$$

Substitution of (4) and (6) into (7) gives

$$2\,t_{\mathrm{err}}\,V_{DC} = -R_{DC}\,I'_{m,\mathrm{DC}}\,T - \frac{2\,I'_{m,\mathrm{DC}}\,C\,V_{\mathrm{DC}}^2}{I_{\mathrm{sw,n}}^2 - {I'_{m,\mathrm{DC}}}^2}. \tag{8}$$

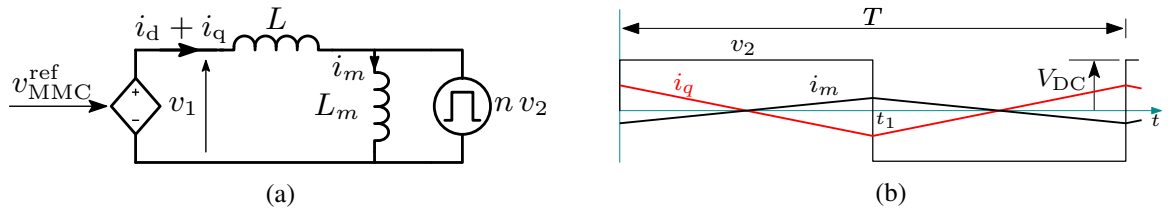
Then, the offset current can be determined as a function of the normal switching current $I_{\mathrm{sw,n}}$ and circuit parameters. Given (8), the compensating effect becomes more pronounced when decreasing the switching current during normal operation.

Switching current control

To ensure ZVS transitions in the LVC, the minimum commutation current of switching devices should be provided. The commutation current is equal to the sum of the inductive reactive currents given to the converter by the MMC and the magnetizing inductance of the transformer. Fig. 3a shows the simplified representation of the MMC-fed AC/DC converter, where the MMC is modeled as a controlled voltage source and linked to the LVC by the inductor L. Here, L represents the sum of the MFT's leakage inductance and arm inductance of the MMC. The terminal current of the MMC comprises an active term $i_d(t)$ and a reactive term $i_q(t)$ (see Fig. 3b). These terms can be controlled through $v_{\mathrm{MMC}}^{\mathrm{ref}}$, denoting the reference of the MMC terminal voltage. As a result, the reactive current of the MMC side $i_q(t)$ is adjustable [4, 9]. Apart from the MMC, the magnetizing inductance of the MFT contributes to the required commutation current in the LVC. Considering a negligible MFT leakage inductance compared to the arm inductance of the MMC, as can be seen from Fig. 3b, the secondary referred magnetizing current will have a triangular waveform with peak amplitude equal to

$$\hat{I}'_m = i'_m(t_1) = \frac{V_{\mathrm{DC}}\,T}{4\,L'_m} \tag{9}$$

where L'_m represents the secondary-referred magnetizing inductance of the MFT. As shown in Fig. 3b, the switching current of the LVC during normal operation is equal to the total reactive current delivered



(a) (b)

Fig. 3: (a) The simplified representation of the MMC-fed AC/DC converter, (b) the reactive currents through the LVC.

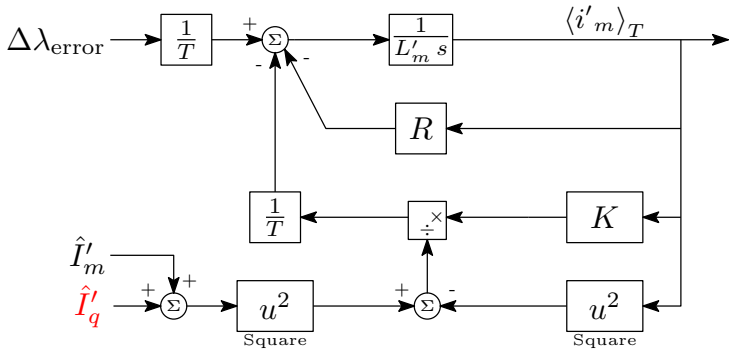


Fig. 4: Average dynamic representation of the LVC with control input $\hat{I}'_q$ for compensating the imbalance in the applied volt-seconds.

to the converter by the MMC and the MFT and given by

$$I_{\text{sw,n}} = |i'_q(t_1) - i'_m(t_1)| = \hat{I}'_q + \frac{V_{\text{DC}}\, T}{4\, L'_m}. \tag{10}$$

The first term of (10) is adjustable by the MMC to change the normal switching current $I_{\text{sw,n}}$ of the LVC. Substitution of (10) into (8) yields

$$2\, t_{\text{err}}\, V_{DC} = -R_{DC}\, I'_{m,\text{DC}}\, T - \frac{I'_{m,\text{DC}} \overbrace{2CV_{\text{DC}}^2}^{K}}{(\hat{I}'_q + \frac{V_{\text{DC}}\, T}{4\, L'_m})^2 - {I'_{m,\text{DC}}}^2}. \tag{11}$$

As a result, the normal switching current can be modified through controlling i_q to enhance inherent volt-second balancing of the LVC. This also can be represented by the average dynamic model of the system drawn in Fig. 4, where $\langle i'_m \rangle_T$ represents the average of the secondary referred magnetizing current over one switching period. As can be seen, both R_{DC} and $\Delta\lambda_{\text{n,cmt}}$ act as a negative feedback to limit the offset current.

Simulation results

To verify the theoretical analysis, simulations were conducted using PLECS with the circuit parameters given in Table I. Quite a large timing error $t_{\text{err}} = 50\,\text{ns}$ is considered in the LVC. In order to find the attenuation of the offset current with the proposed method, first, the offset current without inherent volt-second balancing is obtained by setting $\Delta\lambda_{\text{n,cmt}}$ to zero in (7,8), which yields an offset current equal to $\Delta\lambda_{\text{error}}/R_{\text{DC}}\, T$. Afterwards, using (8) the resulting offset current with the inherent volt-second balancing is derived versus the normal switching current. Subsequently, the attenuation of the offset current, with regard to $\Delta\lambda_{\text{error}}/R_{\text{DC}}\, T$, is plotted in Fig. 5. As can be seen, the higher the normal switching current, the

Table I: Circuit parameters

Description	Parameter	Value
Power rating	P	1 MW
Output DC voltage	V_{DC}	800 V
Operating frequency	f	1 kHz
Switch-node capacitance	C	13.2 nF
Dead time	t_d	500 ns
Magnetizing inductance	L_m	200 mH
Path resistance	R_{DC}	5.5 mΩ
Transformer turn ratio	$n:1$	10 : 1

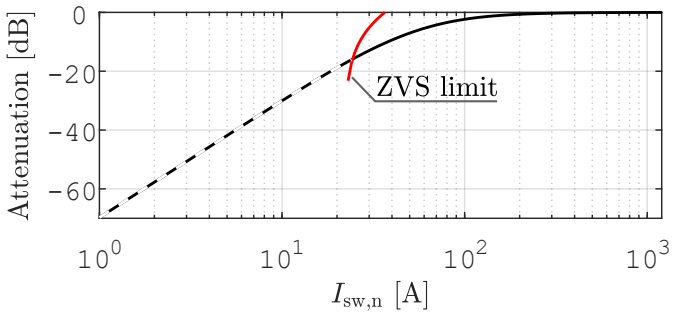
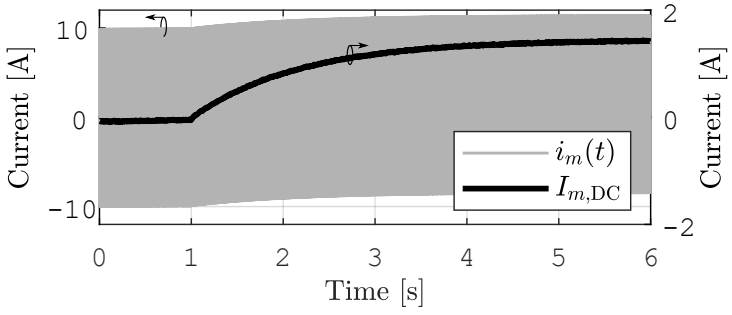
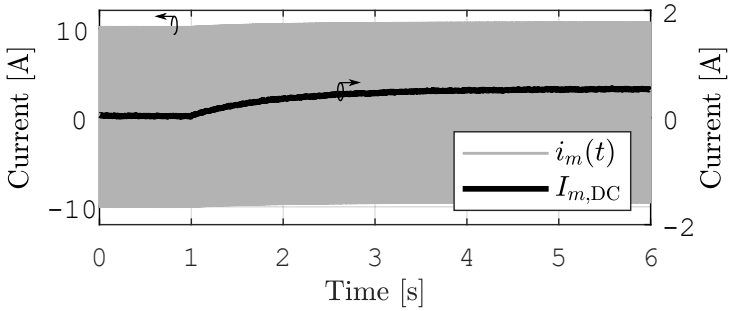


Fig. 5: The attenuation of the offset current versus the normal switching current.



(a)



(b)

Fig. 6: Simulated magnetizing current i_m and its DC component $I_{m,\mathrm{DC}}$ for (a) phase shift control and (b) the proposed method.

smaller the balancing effect of the bridge. Especially at elevated switching currents (which is a typical situation for phase shift control [4]), the inherent volt-second balancing effect of the bridge is negligible. In addition, the minimum desired offset current is determined by ZVS limit of power switches. Although this limit can be relaxed by increasing the dead time in the legs of the LVC, a very large dead time can bring about performance deterioration of the converter such as the duty cycle loss.

Fig. 6 depicts simulation results of the instantaneous transformer magnetizing current as well as its DC component, both with and without reactive current control. By means of the reactive current control, the switching current is set to be $I_{\mathrm{sw,n}} = 40\,\mathrm{A}$, which is around two times the minimum required commutation current of power devices in the LVC. Initially, the LVC works ideally without a timing mismatch, so that there is no DC current through the transformer. At $t = 1\,\mathrm{s}$ the timing error $t_{\mathrm{err}} = 50\,\mathrm{ns}$ is applied to the LVC. As can be seen from Fig. 6a, for large switching currents (phase shift control), the imbalance causes a large DC component in the transformer magnetizing current, which can take the transformer core into saturation. On the other hand, when the switching current during normal operation is limited by means of reactive current control, the resulting DC component of the magnetizing current is decreased by a factor of about 3, as shown in Fig. 6b. The further decrease in the offset current is achievable by reducing the

normal switching current as shown in Fig. 5.

Conclusion

A volt-second balancing method is presented for an AC-DC converter interconnected to an (AC-AC) MMC by means of an MFT. This method utilizes the reactive current control capability of the MMC-connected AC/DC converter to boost the inherent volt-second balancing of the zero-voltage switched bridge and therefore mitigate the offset current through the transformer. The inherent volt-second balancing of the LVC is analytically quantified, which yields analytical relationship between the transformer reactive current, the parameters of the converter circuit, and the resulting offset current. In simulations, a large timing error is imposed on the LVC, and the resulting offset current is significantly reduced by the proposed method.

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