Compensation of Non-Ideal Characteristics of Switch Elements in Voltage Source Inverter

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Abstract-- A voltage source inverter (VSI) inserts dead-time in switching signals to prevent shoot-through in its legs. However, voltage errors from this dead time cause output voltage and current distortion, which can degrade the control performance of AC induction motors. Previous papers corrected this distortion by analyzing additional circuit configurations or load characteristics. This paper proposes a new method to compensate for non-ideal switch characteristics that causes the output voltage distortion and compensates through control code. Firstly, the equation mathematically expresses the effects of switch devices' non-ideal characteristics on switch waveforms and pole voltages to enable compensation. Secondly, through experimentation, it confirms the effects of non-ideal switch characteristics on output voltage distortion. Finally, the compensation values for non-ideal characteristics propose compensating for output voltage distortion in the control code. By applying this method to a general-purpose inverter system, a more accurate output voltage waveform is obtained with a simple numerical method. The experimental results demonstrate the validity of the analysis and the usefulness of the compensation method.

Index Terms-- voltage source inverter, VSI, IGBT, non-ideal characteristic, three-phase inverter, dead-time

I. INTRODUCTION

Voltage source inverters (VSIs) are widely used in electrical control systems due to their ability to operate at high frequencies. However, when both switches operating complementarily are turned on in a VSI, a shoot-through in one leg can occur, causing circuit shorts, overcurrent flows, and switch damage. Fig. 1 shows a typical configuration of a three-phase VSI. With advancements in power semiconductor devices such as GaN, SiC, and other materials, pulse width modulation (PWM) techniques and VSIs have become increasingly popular for high-frequency operations. To prevent shoot-through, a short delay, known as "dead time," must be inserted between turning off one device on a leg and turning on the other. However, dead time insertion causes phase voltage distortion and reduces the fundamental voltage when the inverter works at a low output voltage [1]-[10].

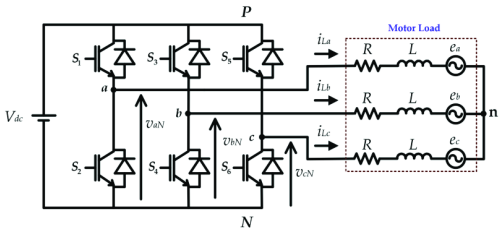


Fig. 1. 3 phase voltage source inverters with motor load.

Several compensation methods have been proposed to eliminate dead-time effects and distortions, including non-linear characteristics of the inverter, voltage drop across the switch, on/off delay, and parasitic capacitance [2]-[6]. Inverter non-linear characteristics can cause phase voltage distortion, which can impact control performance and reduce efficiency [2]-[7]. To compensate for these effects, many strategies have been proposed, including those focused on transmission delay. One approach presented in [2] involves using an algorithm to sortie the PI integrator as an input signal for dead-time compensation. In the paper [3] and [5], the output voltage distortion was suppressed by constructing an additional circuit that improves the accuracy of current direction measurement. The paper [4] reduced distortion by compensating for switch-on delay according to on-resistance, while [6] applied the motor's back EMF as the load to the dead-time compensation. However, these papers only dealt with output voltage distortion and did not address other non-ideal switch characteristics. In [7], the analysis focused on the parasitic capacitance of the IGBT as a source of output voltage distortion, and the distortion was compensated by adding parallel capacitance to the switch device.

In the case of an inverter system, there are many factors that distort the output voltage including non-ideal characteristics of switching devices, such as voltage drop across the switch, on/off delay, and parasitic capacitance, in addition to the dead time effect. Although one of these factors may appear insignificant, it can affect the switching waveform and result in voltage distortion respectively. This paper focuses on compensating for all these non-ideal characteristics of switching devices to address these issues in 3-phase DC/AC inverters. Specifically, the paper analyzes these three non-ideal characteristics of switching devices such as the difference of voltage drop across the switch, the delay time of turn-on/turn-off, and the parasitic capacitance of the switch devices. The voltage error compensation values are derived using the parameters of the device which can be obtained from the datasheets. The compensation method is implemented in the control program which is a part of induction motor V/f control, and the effectiveness of the proposed compensation method is validated through experimental results.

II. Effect of Non-Ideal Characteristics

The commonly used three-phase PWM inverter is shown in Fig. 1 when the induction machine is modeled as an R-L network and a back-EMF. It represents the VSI with ideal switching device IGBTs, but real devices have non-ideal characteristics such as turn-on/off delay, voltage drops across, and parasitic capacitance. These are the reason for the output voltage distortion of VSIs. To accurately compensate for the voltage distortion, these influencing factors should be compensated.

A. Turn-on/off delay

The on/off delay is caused by the on-resistance of the switch gate stage and the signal delay of the gate driver. The switching waveform is delayed by the delay time between the on-time input to the controller and the on-time when the switch accepts it. Therefore, the actual output voltage is distorted by this delay time. Fig. 2 shows the effect of the on/off delay on the output voltage.

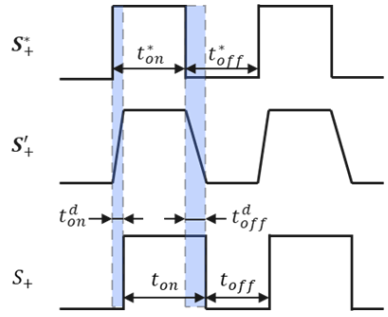


Fig. 2. Turn-on/off delay switching waveform.

When S_+^* denotes the reference of the switching waveform and t_{on}^*, t_{off}^* denote the duration of the turn on/off time. S_+' denotes the actual output waveform of the gate driver. S_+ denotes the waveform when switch device operates on/off signal and t_{on}^d, t_{off}^d are the duration of turn on and off delay time. And V_o denotes the equivalent output voltage. From Fig. 2, the effective turn-on and turn-off duration of S_+ is given by [3]

$$t_{on} = t_{on}^* + t_{off}^d - t_{on}^d \quad (1)$$

$$t_{off} = t_{off}^* + t_{on}^d - t_{off}^d \quad (2)$$

It should be noted that the resulting output voltage differs from the ideal waveform in both pulse width and phase due to the device's on/off delay. Distortion of the output voltage waveform occurs during the dead time when both switches of a single arm are turned off. Therefore, compensation for the device's on/off time delay must consider the rising time (t_{rise}) and falling time (t_{fall}) of the gate driver and IGBT. Applying the values of the rising and falling time of the IGBT and the rise and fall time of the gate driver is as [3]

$$t_{on}^d = t_{Ion} + t_{Ir} + t_{Gr} \quad (3)$$

$$t_{off}^d = t_{If} + t_{If} + t_{Gf} \quad (4)$$

The t_{Ir} and t_{If} denote rising and falling time in the IGBT and t_{Ion}, t_{Ioff} denotes turn on and turn off delay in the gate driver's output switching waveform. And t_{Gr}, t_{Gf} denotes rising and falling time of are gate driver. To compensate the turn-on/off delay time apply the t_{on}^d and t_{off}^d parameter value of dead band rising and falling edge variables in the switches control code.

B. Voltage Drops across the Switches

Voltage distortion in the output voltage of the 3-phase inverter can be caused by the voltage drop of the power devices at low voltage. When the main switch is in the on state, the voltage drops of the switch devices include the voltage drop and the voltage drop when the freewheeling diode is conducting. Therefore, depending on the direction of the load current, the high side and low side IGBT operation and following voltage drop of the pole voltage can be analyze as follows.

In the a-phase, if the phase current $i_{as} > 0$, the actual pole voltage can be shown as [6]

$$S_1\ ON: \quad V_{ao} = \frac{V_{dc}}{2} - V_{ce} \quad (5)$$

$$S_1\ OFF: \quad V_{ao} = -\frac{V_{dc}}{2} - V_d \quad (6)$$

The V_{ce} denotes the voltage drop of the active switch and V_d denotes the voltage drop of the freewheeling diode.

If the phase current $i_{as} < 0$, the actual pole voltage can be shown as [6]

$$S_4\ ON: \quad V_{ao} = -\frac{V_{dc}}{2} + V_{ce} \quad (7)$$

$$S_4\ OFF: \quad V_{ao} = \frac{V_{dc}}{2} + V_d \quad (8)$$

From this equation the actual pole voltage with voltage drop depends on the direction of the current and the on/off state of the switch. Therefore, the compensation of the voltage drop is based on current direction, according to the pole voltage is smaller or larger than zero. And it declared the voltage drop variables in the control code.

C. Output Parasitic Capacitance

Parasitic capacitances in switch devices considerably influence the output pulse durations. One of the switch elements, the IGBTs, is associated with several types of parasitic capacitances [9]. The Fig. 3 shows the parasitic capacitance of IGBT.

The collector emitter capacitance C_{CE} is consist of the output capacitance C_{oes} and reverse transfer capacitance C_{res}. The equation shows how the parasitic capacitance C_{oes}, C_{CE}& C_{res} effect to switch on/off delay is given by [9].

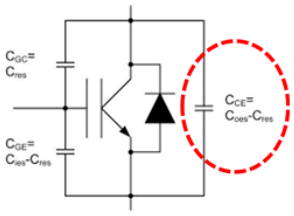


Fig. 3. IGBT parasitic capacitance.

$$C_{oes} = C_{CE} + C_{\text{res}} \tag{9}$$

Recently, this parasitic capacitance has been minimized but it is not perfectly eliminated. The parasitic capacitance still effects the distortion of the phase current during the dead-time. The current flow path of the parasitic capacitance can be represented in Fig. 4.

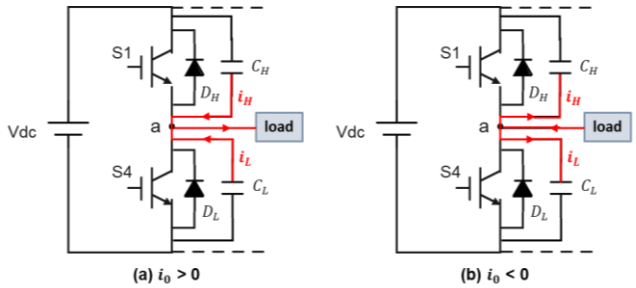


Fig. 4. The current loop with the parasitic capacitance.; (a) $i_o > 0$, (b) $i_o < 0$

The current i_L denotes the current when the lower parasitic capacitor discharges and the current i_H denotes when the upper parasitic capacitor is on charge. If the current is considered constant for the so short dead time. Then, the phase current during dead time can express [7]

$$i_{as} = i_L + i_H \tag{10}$$

If the voltage changes in the same way for the upper and lower parasitic capacitor, the current is also the same by charging and discharging capacitance have the same amount. So, when the ΔV_{an} means the decreased pole voltage and the Δt means the falling time of the pole voltage, the relationship between i_L and i_H is [7]

$$i_L = i_H = C_{oes} \times \frac{\Delta V_{an}}{\Delta t} = \frac{i_a}{2} \tag{11}$$

From this equation, the duration time of pole voltage falling to zero can be given by[6]

$$\Delta t = 2C \times \frac{V_{DC}}{i_a} \tag{12}$$

The equation (12) represents the time at which the voltage error occurs during the dead time between the complementary switching waveforms S+ and S- and the on/off switching waveform of the two switches. The error voltage waveform by the parasitic capacitor at the dead time can be represented as shown in Fig. 5.

The Fig. 5 shows the pole voltage waveform in a PWM period at a certain current. The green and orange areas are the pole voltage errors by each current direction which can be given by the equation. The orange area represents the error voltage when the duration time is longer than the dead-time. And the green area represents the error voltage when the duration time is smaller than the dead-time.

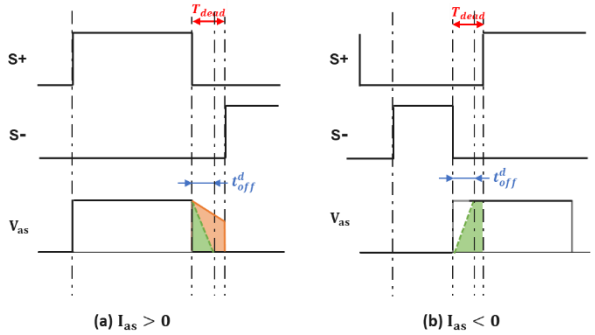


Fig. 5. The effect of the parasitic capacitance in waveform.; (a) $I_{as} > 0$, (b) $I_{as} < 0$

When the phase current is bigger than 0 and the duration time Δt is smaller than the dead time T_{dead}, the pole voltage error an express as [7]

$i)\ \Delta t \le T_{dead}$,

$$V_{err} = \frac{T_{dead} \times V_{dc} - \frac{1}{2} V_{dc} \times \Delta t}{T_{sw}}$$

$$= \frac{T_{dead} \times V_{dc} - \frac{1}{2} V_{dc} \times (2C_{oes} \times \frac{V_{dc}}{i_{as}})}{T_{sw}} \tag{13}$$

From the Fig. 5(a) which is painted in green is the case of the equation (13), the voltage error represents the subtract duration time voltage from dead time voltage.

If the duration time is longer than dead time, the voltage error which painted in orange can calculate by multiply the dead time with decrease pole voltage [7].

$ii)\ \Delta t \ge T_{dead}$,

$$V_{err} = \frac{T_{dead} \times \Delta V_{an}}{2T_{sw}}$$

$$= \frac{T_{dead} \times (\frac{1}{2C_{oes}} \times i_{as} \times \Delta t)}{T_{sw}} \tag{14}$$

When the phase current is smaller than 0, the pole voltage error V_{err} is same when the dead-time is smaller than voltage falling duration [7].

$iii)\ \Delta t \le T_{dead}$,

$$V_{err} = \frac{-T_{dead} \times V_{dc} - \frac{1}{2} V_{dc} \times \Delta t}{T_{sw}}$$

$$= \frac{-T_{dead} \times V_{dc} - \frac{1}{2} V_{dc} \times (2C_{oes} \times \frac{V_{dc}}{i_{as}})}{T_{sw}} \quad (15)$$

Fig. 5(b) in green illustrates the scenario for Equation (15), where the voltage error is the difference between the voltage during the subtract duration time and the voltage during the dead time. The equations (13) to (15) provide an equation expression for the parasitic capacitance. By using these equations, voltage distortion can be corrected through parasitic capacitance compensation.

The compensation for parasitic capacitance in IGBT is determined by considering the current direction and the voltage drop time relative to the dead time period. The parasitic capacitor variable is in the control code, and the compensation formula for parasitic capacitance is applied after converting the phase voltage from d-q axis voltage to a three-phase voltage waveform.

III. Experiment Results and Discussions

The input DC link voltage is supplied by transformer, the switch is controlled through the DSP28335 board, and the voltage source inverter works with the load induction motor. TMS320F28335 is the digital signal processor (DSP) used in the experiment. To compensate for the non-ideal characteristics of the switch device, it is important to consider the values presented in the data sheet and interpret the graph. However, the switch element can also be affected by the driving current and ambient temperature during operation, which must be considered when selecting the value to be applied to the compensation formula. In this study, non-ideal device values were selected based on the datasheet and the operating conditions of the load induction motor during the experiment. Table 1 shows the feature of the IGBT, including switch turn-on/off delay time, switch saturation voltage, and parasitic capacitance. The parameter values are retrieved from the datasheet of the IGBT (A1P25S12M3-F) and the gate driver (FOD3150) manufacturers.

TABLE I
Non-Ideal Characteristic Parameters

Parameters	Symbols	Values
Turn-on delay time	t_{on}^{d}	$0.64\mu s$
Turn-off delay time	t_{off}^{d}	$0.83\mu s$
Switch saturation voltage	V_{CE}	$1.2V$
Forward voltage	V_{d}	$1.7V$
Parasitic capacitance	C_{oes}	$130pF$

TABLE II
Induction Motor Parameters

Parameters	Symbols	Values
Rated power	C_{rated}	$3kW$
Rated voltage	V_{rated}	$220V$
Rated current	I_{rated}	$14.7A$
Frequency	f	$60Hz$
Pole	P	4

The power device is an IGBT module whose current rating is 25[A] and the voltage rating is 1200[V]. The dc-link voltage is about 220V and switching frequency is 10[kHz], the dead-time is 2.984usec, and the output frequency. The parameters of the induction motor used as the load are shown in Table II.

The experiment was conducted so that the output voltage was 10Hz with V/f control. The experimental results show the effectiveness of the proposed distorted voltage compensation strategy in the zero current clamping region. From these basic settings, the phase current waveform was measured with the oscilloscope as follows. The dq-axis current waveform output of the DSP D/A converter is shown in Fig. 6. In this experiment, the peak phase current is 5[A] and 10[Hz]. From the Fig. 6, the tree-phase current waveforms are very distorted.

The first compensation is for the switch turn-on/off delay. The parameters of the switch turn on/off delay time are in Table I. The result of compensating switch turn-on/ /off delay time are shown by dq-axis current waveform in Fig. 7. The distortion at zero current and peak current is reduced, and the value of the peak current is increased. From this result, it can be concluded that the compensation of switch turn-on/off delay is effective in compensating for the distorted voltage output.

The second compensation is for the switch voltage drop. The result of compensating for switching saturation voltage is shown by dq-axis current waveform in Fig. 8. There is no significant difference between the non-compensation case, Fig. 6, and voltage drop compensation, Fig. 8. Since the voltage drop 1.7V or 1.2V is too small compared to the input voltage 220V, it can be confirmed that the degree of compensation is very small.

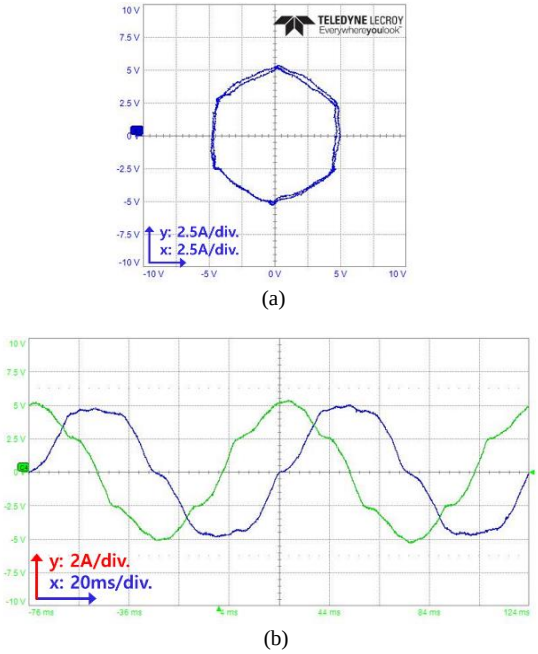
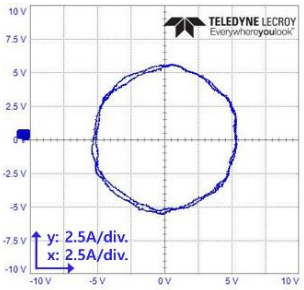


Fig. 6. non-compensation current waveform.; (a) x-y plot of dq-axis phase current, (b) dq-axis phase current



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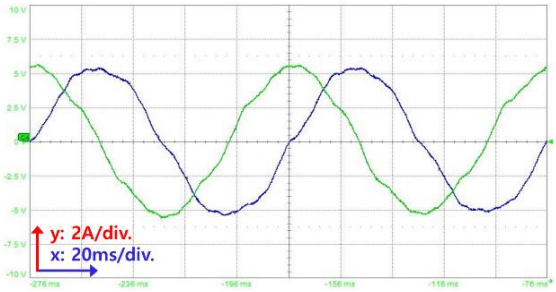

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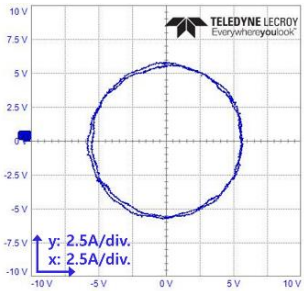
Fig. 7. Turn on/off delay compensation current waveform.; (a) x-y plot of dq-axis phase current, (b) dq-axis phase current.



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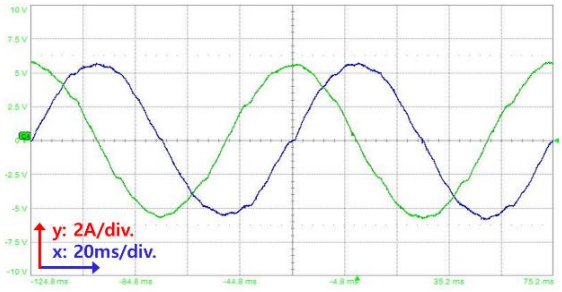

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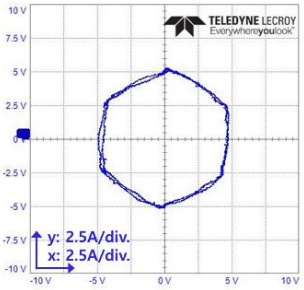
Fig. 9. Parasitic capacitance compensation current waveform.; (a) x-y plot of dq-axis phase current, (b) dq-axis phase current



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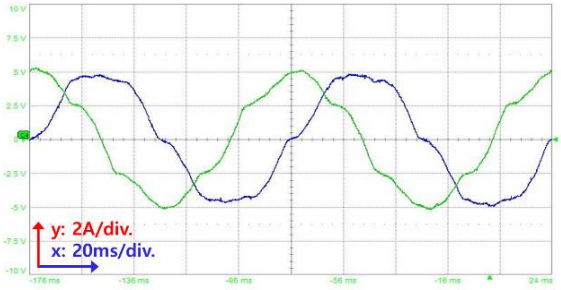

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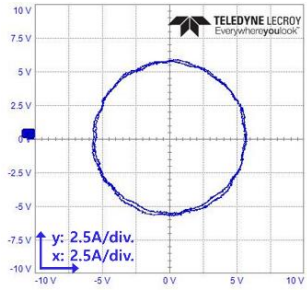
Fig. 8. Voltage drop compensation current waveform.; (a) x-y plot of dq-axis phase current, (b) dq-axis phase current



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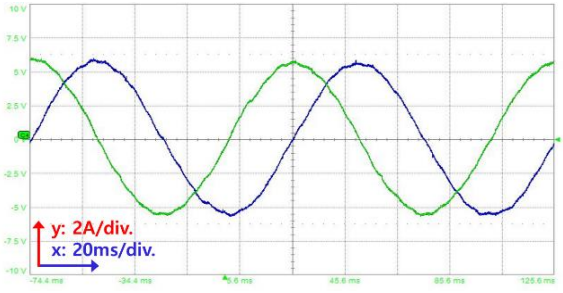
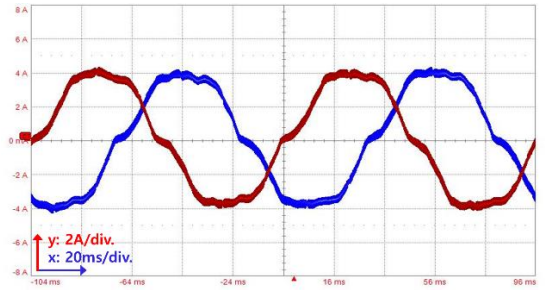


(b)

Fig. 10. Applied all compensations current waveform.; (a) x-y plot of dq-axis phase current, (b) dq-axis phase current.

The last compensation is about the parasitic capacitance. The way of compensating parasitic capacitance is different with the paper [7]. The paper [7] compensate the parasitic capacitance with adding another parallel capacitance but in this paper the parasitic capacitor is compensated with adjusting equation in control code mathematically. The value of the parasitic capacitor parameter is 130pF which is appeared in datasheet. Comparing Fig. 9 to Fig. 6, the result shows the parasitic capacitance compensation is effective. But it is still distorted at the zero and peak current.

Fig. 10 shows the dq-axis current waveform output with the three options of dead time compensation applied, indicating that it is almost a sine wave. When all compensation strategies are adopted, the phase current waveform becomes like Fig. 11. And the waveform of the output 3-phase current measured with the current probe before compensation is shown in Fig. 11(a), and the current waveform measured after compensation is shown in Fig. 11(b). In Fig.11(a), the current waveform is distorted in zero and peak.



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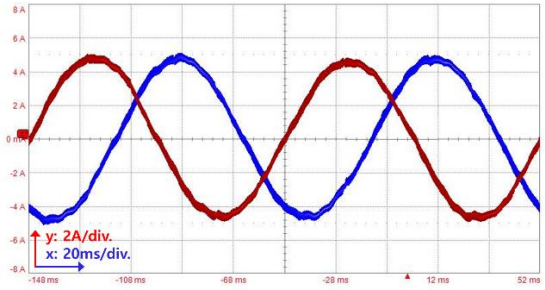

(b)

Fig. 11. Phase A and B current all compensation waveform.; (a) non-compensated, (b) all compensated.

Assuming that the main factors of non-ideal device characteristics affecting output, voltage distortion are switching on/off delay time, voltage drop, and parasitic capacitance, output voltage compensation was applied and confirmed.

IV. Conclusions

The effectiveness of the compensation strategies for non-ideal characteristics, such as switch turn-on/off delay time, voltage drop, and parasitic capacitance, were analyzed and confirmed through experiments. The experiment results showed that the compensation for the parasitic capacitance was the most effective and the switch turn-on/off delay time is also effective, as indicated by the reduced distortion in the output waveform. Although voltage drop compensation had a relatively smaller effect in this study due to the high DC-link voltage, it becomes important in low-voltage DC systems, such as 24V and/or 48V. When all compensation strategies are adopted, the waveforms of the output 3-phase currents show significantly reduced distortion as confirmed not only in the sampled dq-currents but also in the measurements by high bandwidth current probes. It was confirmed that the compensation strategy proposed in this study can effectively compensate for the distorted output voltage in a system using a voltage source inverter by considering only the datasheet values of the switching device. The study also emphasized the importance of compensating for non-ideal characteristics in achieving accurate and undistorted output voltage in a voltage source inverter, which can lead to improved efficiency and reduced losses.

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