Automated gate impedance network design for SiC MOSFETs using SPICE solver interfaced with MATLAB environment

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Keywords

≪Design optimization≫, ≪MOSFET≫, ≪Parasitic elements≫ ≪Silicon Carbide (SiC)≫ ≪Virtual prototyping≫

Abstract

In order to ensure proper switching of SiC devices gate impedance has to be carefully selected. Chosen topology and parameter values allow for damping the oscillations in poorly designed layouts, as well as adjusting dV/dt levels in cases where layout allows for too fast switching. Due to a wide choice of gate impedance topologies, some with multiple tunable parameters, experimental fine-tuning is a time-consuming process and analytical predictions do not take full effect of the parasitic elements into account. For this reason, an automated design process is developed using Matlab and LTSpice and the results are verified experimentally in a Double Pulse Test(DPT) setup, for the prediction accuracy assessment.

Introduction

Recently, wide band-gap (WBG) devices have been a subject of widespread integration in power converter design due to the significant improvement offered in the terms of switching speed, thermal performance and breakdown voltage in comparison with silicon devices [1]. However, the aforementioned improvements result in new design challenges due to high levels of voltage and current derivatives present [2]. High dV/dt and dI/dt tends to excite parasitic circuit elements, and degrades performance. Poorly designed layout results in an increased voltage overshoot, electromagnetic interference (EMI), gate loop stability issues and decreased reliability due to negative gate voltage spikes [3]. Those issues can be addressed in the early design phases by either designing the layout to mitigate the parasitics, or by proper choice of gate impedance network. The latter approach is investigated in this paper, as it can prove beneficial for both good and poor layouts.

Oftentimes gate impedance selection is performed manually and in the prototyping phase. Such a process is time-consuming and tends to omit the investigation of more advanced impedance networks than simple resistance, even though passive gate voltage waveform profiling has been presented in literature [4]. Additionally, manual selection rarely provides optimal performance and may not offer any compensation of layout shortcomings if different impedance network topologies are not considered. Due to aforementioned reasons, automation of gate impedance selection is desired as it is able to consider a higher variation of topologies, and improve parameter selection by applying optimisation algorithms.

In this paper, MATLAB environment has been interfaced with LTSpice circuit simulator, taking advantage of possibility to use manufacturer-provided device models and LTSpice accuracy combined with the extensive MATLAB function library. The possibility to freely manipulate SPICE netlists has been used for direct comparison of different gate impedance network topologies over a wide parameter range,

and selection of optimal network using simple graphical optimisation. For accurate parasitic elements model, ANSYS Q3D has been used to extract full parasitics matrix as a SPICE subcircuit. Additionally, accuracy of simulation results has been verified experimentally.

Switching waveform prediction

The circuit considered is a standard double pulse test (DPT) setup, presented in Fig. 1. As it is a common practice to verify the switching performance using the DPT setup, it can be considered a good example for demonstrating the design methodology and interface proposed.

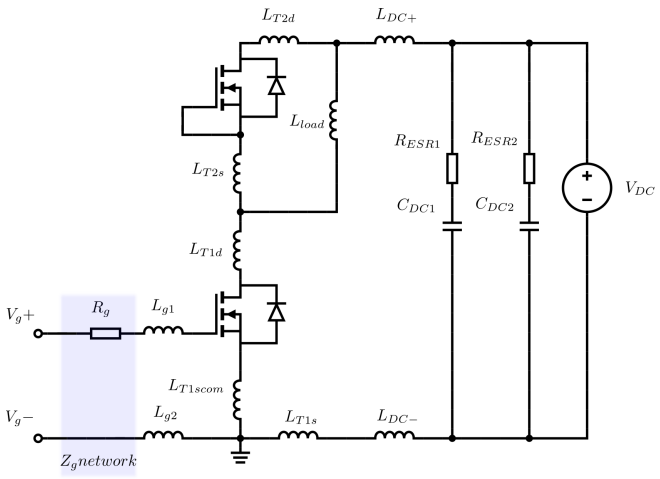

Fig. 1: Simplified Double Pulse Test circuit diagram.

The selected switches are CREE C3M0030090K. As an important mention, one of the SiC MOSFET selection criterion's was low internal gate resistance. This allows designer to have a better control over the switching waveform, as otherwise the gate loop would be over-damped and less responsive to the gate impedance modifications. Table I contains key circuit parameters and component types known at the start of design process. The rest of parameters is estimated using ANSYS Q3D or contained within manufacturer SPICE models.

Table I: Key circuit parameters

Parameter name	Symbol	Value
DC link bulk capacitance	C_{DC2}	4,7μF
DC link bypass capacitance	C_{DC1}	100nF
SiC MOSFET type	-	CREE C3M0030090K
DC link voltage	V_{DC}	400V
Gate voltage amplitude	$\lvert V_{gd}\rvert$	15V
Equivalent series resistance of C_{DC1}	R_{ESR1}	50mΩ
Equivalent series resistance of C_{DC2}	R_{ESR2}	7mΩ
Load inductance	L_{load}	107μH

Modelling and simulation

The modelling approach chosen assumes full digital design approach, and no experimental information available aside from the device models and datasheets provided by manufacturers. The reasoning for this assumption is, that a knowledge of digital design process accuracy without any case-specific modifications based on experimental work has not been extensively investigated in the literature, and is desirable for further design automation development in this area.

Therefore, additional emphasis has been put on circuit simulation accuracy and led to selection of LTSpice. In the literature, this simulator has proven to be able to achieve closest match with experimental

results [5]. However, a major drawback of Spice simulators are numerical stability issues, especially when the trapezoidal integration method is used [6]. Some of the physically viable circuits might consume too much computational power, return no or incorrect results, due to e.g. wrong solver settings, improper initial condition definition or an unfortunate combination of parameters. This is traditionally mitigated by manual fine-tuning, but in the case of investigating large variation of parameters and different topologies it can become a highly time-consuming process by itself, especially for sensitive circuits.

The above mentioned drawbacks have been mitigated by deploying the MATLAB-LTSpice interface. The possibility of monitoring the simulation progress has been used to stop and automatically correct the solver parameters whenever an excessive time consumption is detected. In case of problem persisting, parameter step size is adjusted in order to find a stable point in a close proximity. Operating directly on a netlist, new possibilities for analysis definitions are available. An example of this would investigating the modular structure for optimal number of modules, performing sweeps with a specified ratio of parameters or applying optimisation algorithms using the extensive MATLAB function libraries. Finally, connecting with multi-physics analysis tools is enabled.

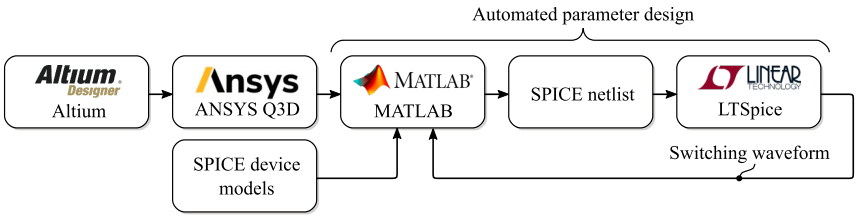

Fig. 2: Automated design flowchart

Fig. 2 depicts a workflow used for design automation. The geometry generated is exported from Altium Designer to Ansys Q3D, where parasitic element network is extracted. Then the network is used in MATLAB together with SPICE models in order to assemble a SPICE netlist for a given problem. The netlist is then simulated, and switching waveforms are fed back to MATLAB, where parameters or a structure of the netlist can be modified.

Extraction frequency selection

The choice of extraction frequency for lumped models of parasitic elements has been sparsely debated in the literature, due to broadband s-parameter based models being a default choice in electronics. Unfortunately, those models are not sufficient for power electronics, as frequency domain simulations are not an adequate mean of analysing the heavily non-linear behaviours. Even though attempts has been made in order to include non-linearities [7], time domain remain a standard. As the actual frequency present in the circuit is both a local and time dependent parameter in case of double pulse test, this selection is a non-trivial matter. There are three approaches used in practice.

Firstly, the highest frequency present can be used. While this can improve the model matching for the high frequencies, the response tends to get over-damped. Another approach may use the switching frequency, however this is hardly feasibly in the case of DPT circuit example with no particular switching frequency chosen. In this case, there is a risk of simulated response being under-damped, compared to the experiment. Last approach uses the rise time in order to approximate the signal bandwidth, using basic equation for the first-order step response. Once again, the response tends to be over-damped.
With those methods not being sufficient, the extraction frequency was selected by trial and error. The parasitic network values have been extracted at the frequency of 800kHz. A full RLGC model has been exported as a SPICE circuit and included in LTSpice circuit accordingly.

Gate impedance network design

The following gate impedance networks have been considered.

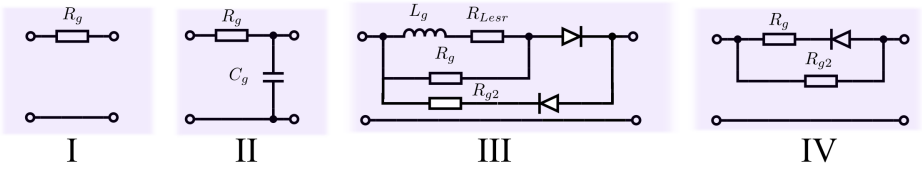

Fig. 3: Gate impedance networks considered

Networks I,II and IV are commonly used, while III is an alternative topology proposed in order to provide tunable frequency-varying gate impedance.

The optimisation criterion chosen is a sum voltage rise time(t_r) and fall time (t_f) further referred to as t_{tot}. The motivation behind this choice is simplifying the experimental verification, as switching energy measurement require meticulous adjustments in order to ensure current and voltage measurement to be synchronised in time. Additional constraint set is drain-source voltage overshoot lower than 10% of DC link voltage. The constraint value was set arbitrarily, as in practice it can vary with application. Standard definitions of t_r and t_f were used.

Simulation results

The impedance network topologies performance limitations have been investigated in simulations, with results present below. Firstly, the impedance network I has been investigated in the gate resistance range between 1 and 160Ω.

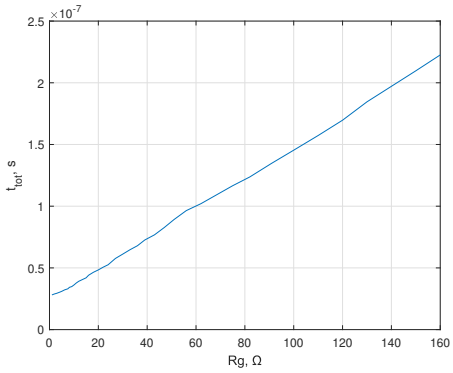

Fig. 4: Sum of drain-source voltage rise and fall times variation with gate resistance for topology I.

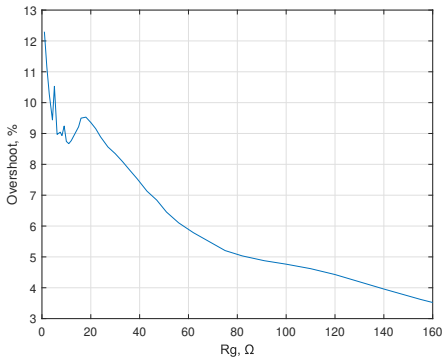

Fig. 5: Drain-source voltage percentage overshoot variation with gate resistance for topology I.

As expected, a linear increase of rise and fall time with increasing Rg is observed in Fig. 4. Slight deviations can be contributed to the oscillation presence for low values of gate resistance. The significant non-linearity present in Fig. 5 also originates from the drain-source voltage oscillations varying with gate resistance increase, until the response stops being heavily oscillatory.

The topology II is investigated next, within same Rg range and Cg ranging between 1 and 100nF.

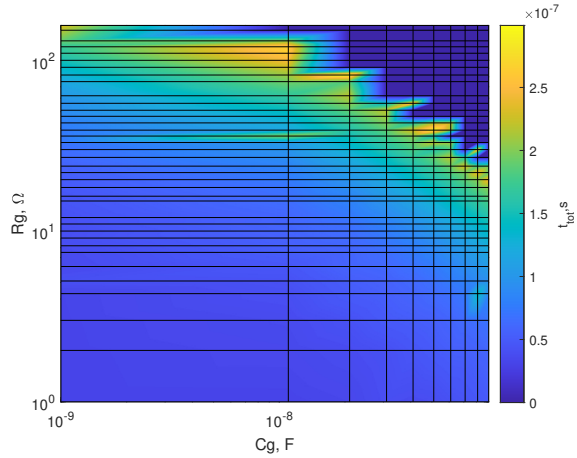

Fig. 6: Sum of rise and fall time variation with gate resistance (Rg) and capacitance (Cg) change for topology II.

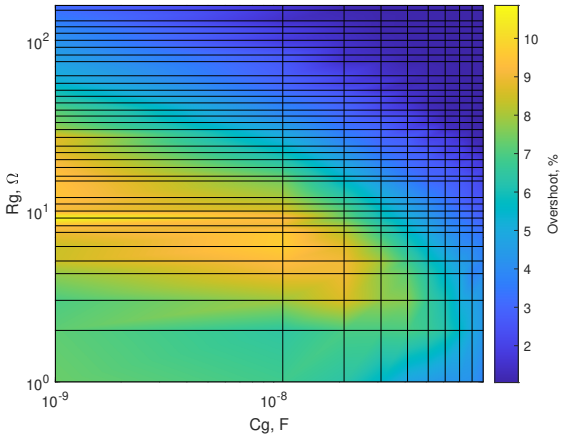

Fig. 7: Overshoot variation with gate resistance (Rg) and capacitance (Cg) change for topology II.

In the Fig. 6, two regions divided with high t_{tot} region are visible. This is due to the high parameter range used, as both rise and fall time increase with gate resistance and capacitance. At some point, the switching process is slow enough for no switching to happen. Fig. 7 describes the overshoot variation with Rg and Cg. The overshoot does not seem to be linearly dependent on the design parameters, as high overshoot can be avoided by either keeping the Rg and Cg high enough, above the high overshoot zone, or by keeping Rg low and varying the Cg for fine-tuning.

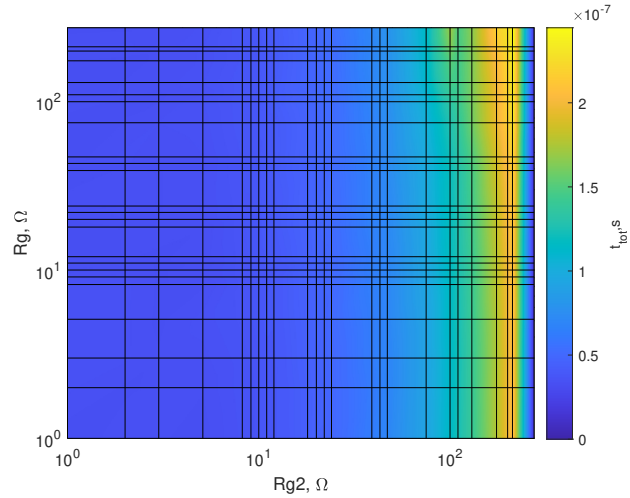

Fig. 8: The t_{tot} variation with two gate resistances (Rg and Rg2) change for topology IV.

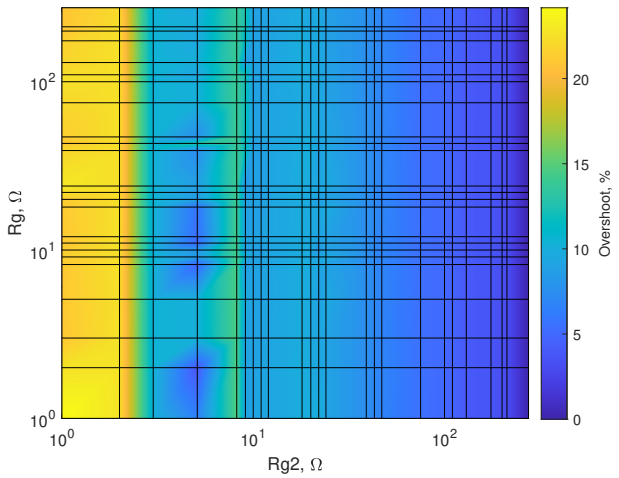

Fig. 9: Overshoot variation with two gate resistances (Rg and Rg2) change for topology IV.

The topology IV behaves in a predictable, though not necessarily linear manner. The t_{tot} variation in Fig. 8 is dominated by Rg2. This leads to Rg2 being the main design parameter in terms of switching speed. Similar behaviour can be seen in the Fig. 9, however in this case oscillatory behaviour for the low values of Rg2 causes some non-linear dependencies.

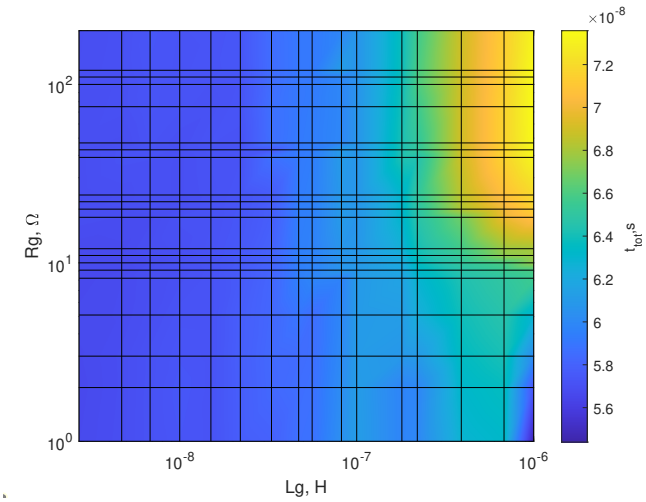

Fig. 10: Sum of rise and fall time variation with gate resistance (Rg) and gate inductance (Lg) change for topology III.

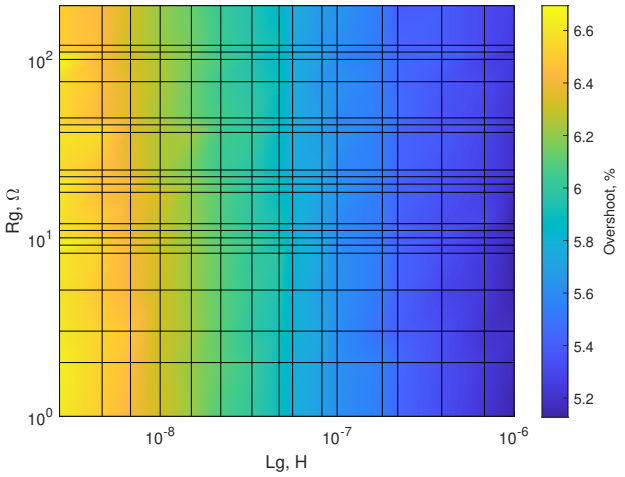

Fig. 11: Overshoot variation with gate resistance (Rg) and gate inductance (Lg) change for topology III.

Similarly to the topology IV, the behaviour is mainly controlled by one parameter, in this case L_g. The gate resitance sizing influence is visible mainly for very small values, due to the parallel connection. Surprisingly, there is a slight influence on the overshoot, even though the the main purpose of this topology is accelerating the turn-on. This is probably due to the oscillations originating from the turn-on undershoot.

Gate impedance network topology comparison

Finally, all of the topologies considered are compared in terms of the overshoot and sum of the rise and fall time.

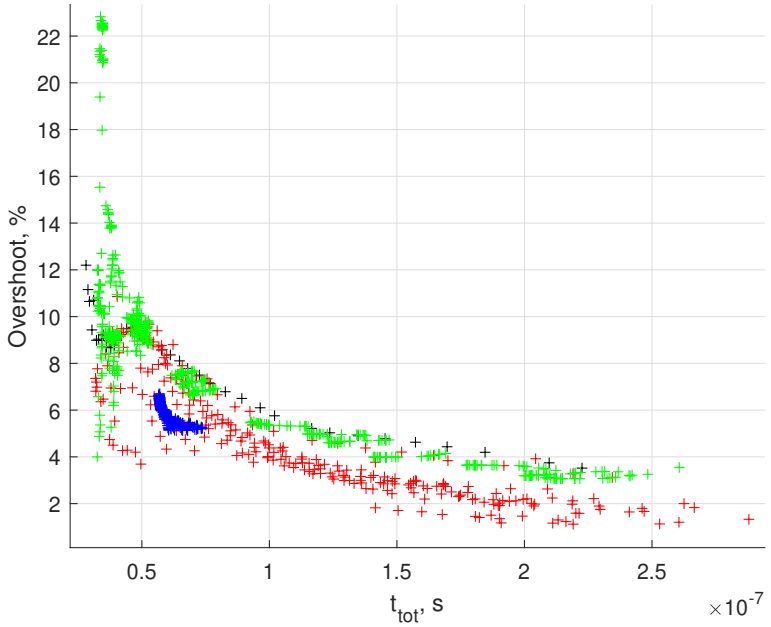

Fig. 12: Results of graphical optimisation for topologies I (black), II (red), III (blue), IV (green).

Fig. 12 shows the results of automated gate impedance design deploying graphical optimisation. Each of the points represents estimated voltage overshoot and a sum of rise and fall time for a single design variable point. The design variable combinations resulting in no switching, previously described in the

II topology simulation results, are removed from graphical optimisation. Finally, the minimal t_{tot} when subject to above mentioned overshoot limitation has been found to be 8 Ω gate resistance in topology I, closely followed by the topologies II and IV. This shows the importance of digital design for gate impedance network, as the topology IV would be a go-to in order to meet the overshoot requirements. However, in this case arresting the overshoot with special topology is not necessary, and topology I offers slightly better perfermonce in terms of t_{tot}. Topology III provides worse performance compared the other topologies investigated, which is most likely due to low impact of decreased turn-on fall time on t_{tot}.

Experimental validation

In order to validate the accuracy of switching waveform simulation and the automated design process results, the DPT board has been manufactured and tested in the setup presented in Fig. 14. Additionally, board layout exported from Altium Designer was depicted in Fig. 13.

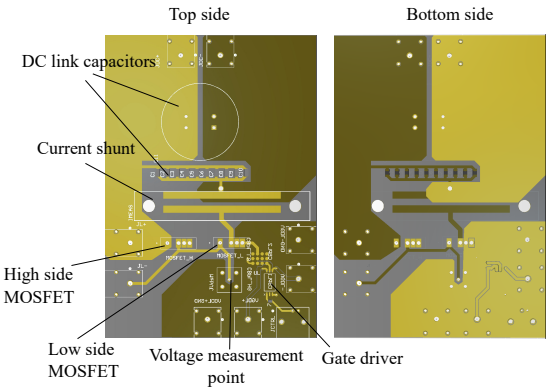

Fig. 13: DPT board layout.

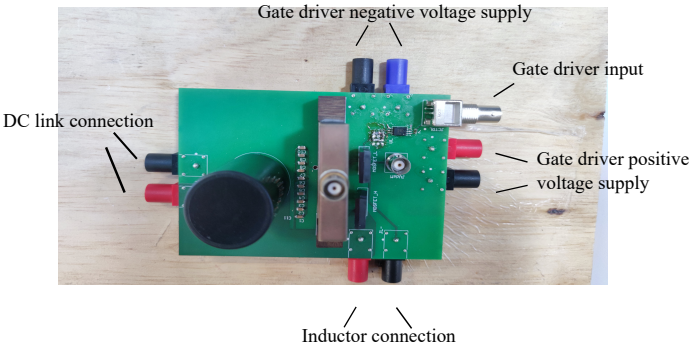

Fig. 14: Experimental DPT setup.

The experimental test results for topology I have been presented in Fig. 15 and Fig. 16. Two data points with a significant parameter distance between them were chosen from previous chapter and verified experimentally. The verification was performed for all of the topologies aside from topology III, due to subpar performance.

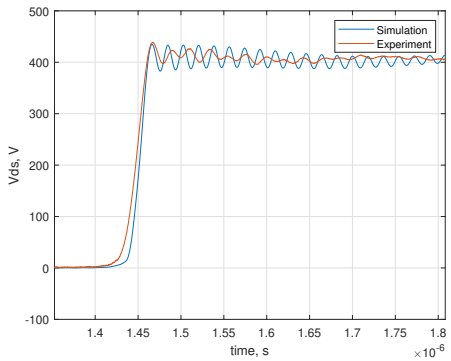

Fig. 15: Switching voltage waveforms for gate impedance I, at 10A load current and 10 Rg.

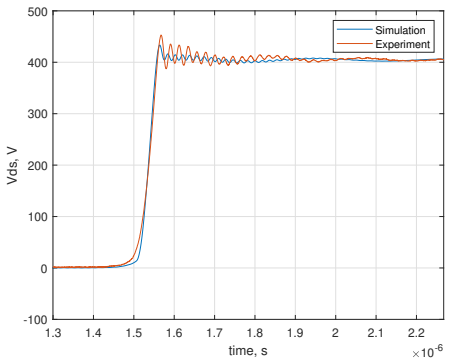

Fig. 16: Switching voltage waveforms for gate impedance I, at 10A load current and 30 Rg.

Firstly, the topology I has has been verified experimentally for the gate resistance values of 10 and 30 Ω, depicted in Fig. 15 and Fig. 16 respectively. A good matching in terms of rise time has been observed in both figures, as well as a very good match in terms of the overshoot in Fig. 15. In case of the second figure, overshoot predicted is lower than experimentally measured and this might be due to the too high extraction frequency. The extraction frequency issues are also visible in Fig. 15, as there is a lower damping in the simulation compared to the experimental results.

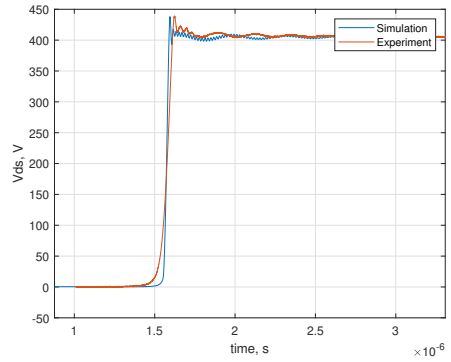

Fig. 17: Switching voltage waveforms for gate impedance II, at 10A load current, 3Ω Rg and 100nF Cg.

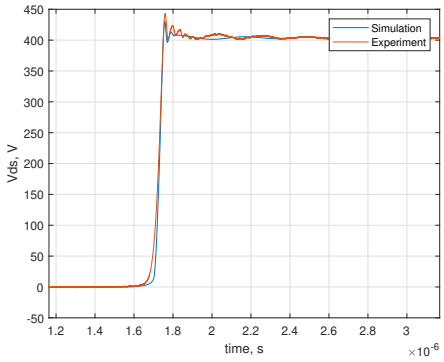

Fig. 18: Switching voltage waveforms for gate impedance II, at 10A load current, 10Ω Rg and 10nF Cg.

In the case of topology II, an overall good match between experimental and simulated waveforms can be observed in Fig. 17 and Fig. 18. In both case, oscillations and rise time is a close match, however in the Fig. 18 simulated overshoot is slightly lower than in the experimental waveform.

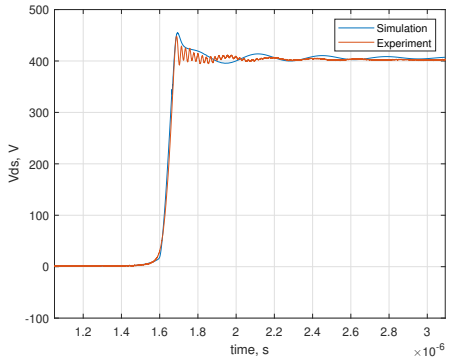

Fig. 19: Switching voltage waveforms for gate impedance IV, at 10A load current at 130Ω Rg and 75Ω Rg2

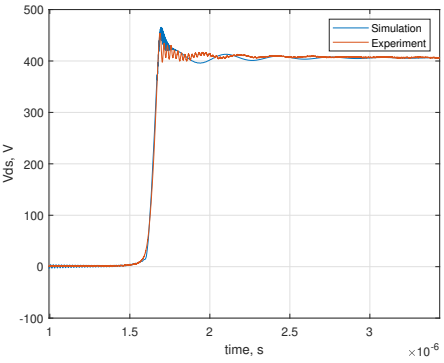

Fig. 20: Switching voltage waveforms for gate impedance IV, at 10A load current 75Ω Rg and 12Ω Rg2.

The last topology verfied experimentally was topology IV, once again with a good match between simulation and experimental results. Contrary to other topologies, the overshoot in Fig. 19 and Fig. 20 is slightly higher than in the experimental results.

Some of the simulation results were found to be mismatched with the experimental results. The main potential cause suspected is the limitation of frequency-dependent parameters used. Both capacitor ESR and parasitic network parameters used were chosen/extracted at one frequency. This assumes that the chosen frequency is valid for the whole sweep, which might not be the case.

Conclusion

The design framework based on LTSpice-Matlab interface and ANSYS Q3D extractor has been presented, along with the approach to automating the design of SiC MOSFET gate impedance design. Careful selection of SiC MOSFET gate impedance can increase the efficiency and reliability. Automation of this process allows to fully exploit its benefits and evaluate multiple impedance networks over a wide range of parameters. In future works, the passive gate voltage shaping circuits can be designed this way, further improving the performance.

The graphical optimisation has been used in order to determine the optimal gate impedance in analysed set, due to low number of optimisation parameters and possibility of easy visualisation. For cases

requiring higher number of optimisation parameters, more advanced algorithms such as e.g. differential evolution should be used. The optimisation parameter definition is crucial to obtaining valid results. Therefore, a further investigation of available and more objective parameter definitions is needed in order to achieve fine-tuned gate impedances for specific applications.

Experimental setup for result verification has been developed and presented, showing a decent matching between simulations and experimental results. The model validity can possibly be improved by either adapting the frequency dependent parameters along the wide parameter sweeps or usage of broadband models, and should be investigated in the future works.

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