Investigations on the Active Reduction of Common Mode Noise with Opposing Noise Sources

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Keywords

«Active filter», «EMC/EMI», «impedance analysis», «filtering», «frequency domain analysis»

Abstract

Conventional filters needed for the electromagnetic compatibility lower the system power density by consuming additional space in power electronic setups. To increase the power density, alternatives for these filters are needed. If the power electronic setup offers the possibility to synchronize two opposing switching transitions, the common mode noise can be reduced without additional filters. In this case two opposing noise currents reduce one another by superimposition. For power electronic setups which do not offer the possibility to synchronize switching transitions, this paper presents an approach which uses additional half bridges as opposing noise sources connected to a replicated grounding impedance to create the opposing common mode noise. The main goal of the opposing noise source is to create similar potential changes as the power electronic setup over the replicated grounding impedance. The replicated grounding impedance emulates the grounding impedance of an ohmic inductive load with discrete elements. The achieved reduction of the common mode noise with this approach is evaluated with measurements.

Introduction

The usage of wide band gap transistors in industrial and automotive applications is increasing. Their characteristics such as higher blocking voltages and increasing switching transitions slopes compared to conventional silicon transistors promise advantages in efficiency and power density. On the other hand, increasing switching slopes and smaller power electronic designs lead to increasing challenges regarding electromagnetic interference (EMI). The components used in conventional passive EMI filters get bigger and heavier so that they lower the gained benefits. Hence, active EMI filters to omit the conventional EMI filters are examined.

Basic idea of active EMI filters is to inject an inverted noise signal to suppress the disturbances by superimposition. Therefore, the noise is measured with a sensing system, inverted and adapted by an analog or digital system and injected in a feedback or feedforward loop into the circuit [1–4]. Because the signals have to be adapted and inverted with an analog or digital system which has a limited bandwidth, the bandwidth of the injected signal is also limited. In addition, the sensing and injection circuits need space, especially if transformers are used.

To overcome these drawbacks an alternative way to damp the noise is to synchronize the timing of two opposing switching transitions [5–11]. Because the noise is generated by the same noise source, there are theoretically no limits regarding the bandwidth. For this purpose, it is mandatory for the power electronic setup to offer the possibility to synchronize switching transitions and identical disturbance

propagation paths. If these requirements are met, the disturbances can be damped without any additional components. However, in various power electronic topologies, the adaption of the timing of the switching transitions is not possible, the propagation paths differ from each other or only one transistor is used. In these cases, the damping of the generated noise is not possible with this attempt.

To generate inverted noise signals, in [12] additional half bridges are used to generate switching transitions. The half bridges are connected with capacitances to ground. In this paper, different realization options to generate the switching transitions for such an approach are investigated. The designs attempt to save costs and space in comparison to the use of the same design as the load system. Moreover, the grounding impedances are investigated to provide an accurate emulation of the parasitic propagation path of the noise. A replication with discrete elements as a grounding impedance is built with the knowledge of the parasitic impedances. Furthermore, a possibility to adapt the timing of the generated switching transitions is presented. The potential of the approach is presented with measurements on a test setup. The different designs are compared to each other in terms of cost, space and reduction of the disturbances. Furthermore, the discrete elements of the replication are varied to show the influence of tolerances on the approach.

Approach

The origins of common mode noise are changing electrical potentials due to switching transitions in power electronic systems. The changing potential φ_1 across the parasitic impedances of the load to the ground potential result in the common mode current i_1. The magnitude and frequency components of the common mode currents are dependent on the derivative of the potential change and the parasitic grounding impedance.

It is possible to reduce the common mode disturbances of the load system, if a second potential change φ_2 with an opposing direction across a similar grounding impedance occurs at the same time. The second potential change generates an opposing common mode current i_2, which reduces the other common mode current by superimposition. The sum of both currents is theoretically zero. This principle is depicted in Fig. 1.

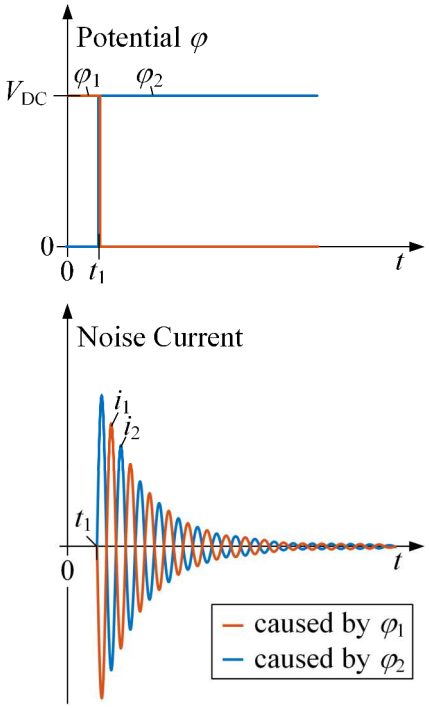

Fig. 1: Principle of the common mode reduction

In this approach, the second potential change is generated by an additional opposing noise source which is exclusively used for the active common mode reduction, so that it conducts no load current. The opposing noise source is connected to an impedance network of discrete elements, which is connected to the ground potential. The system components of the approach are depicted in Fig. 2. The impedance network emulates the parasitic impedances of the load to form the

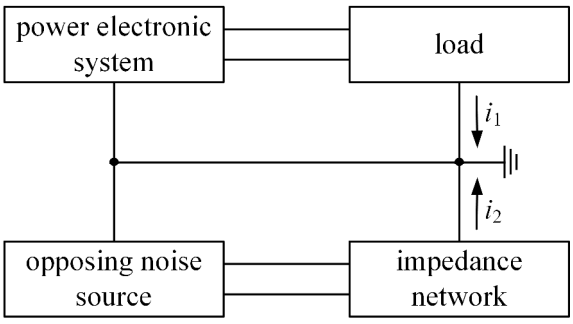

Fig. 2: System components of the approach

inverse temporal course of the common mode current i_1. Therefore, the impedance network should have the same impedance than the original parasitic common mode propagation path of the load connected to the power electronic system. To build up an accurate impedance network, the setup and its common mode propagation paths are evaluated. Based on this evaluation, the opposing noise source and the impedance network are designed to create an opposing noise current i_2.

Overall structure

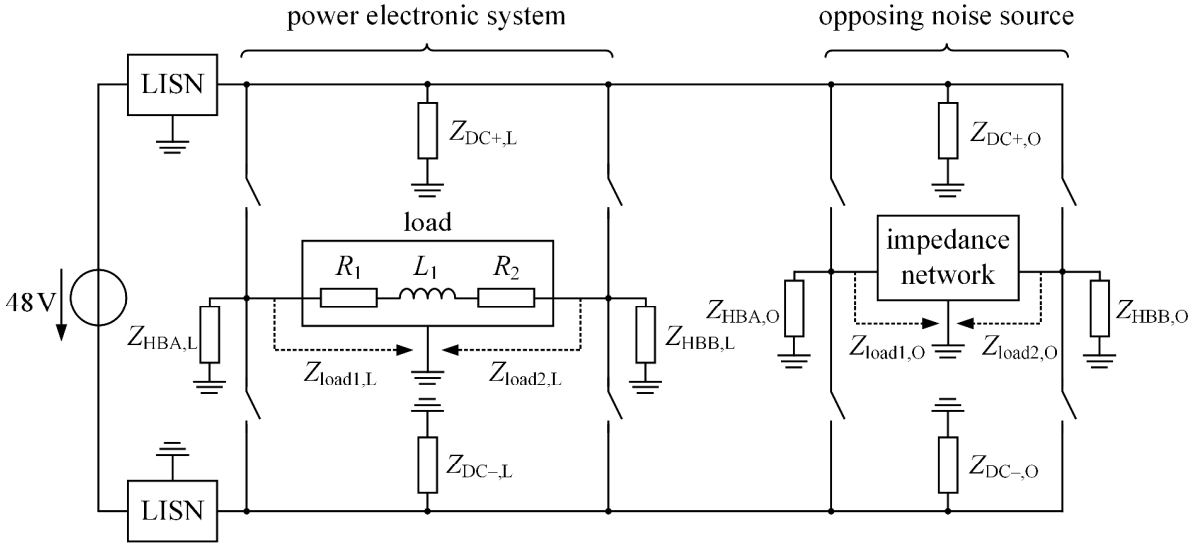

Fig. 3: Overall structure

The overall structure of the approach is depicted in Fig. 3. As the power electronic system, a full bridge converter connected to an ohmic inductive load is used. The design of the full bridge converter of the power electronic system is shown in Fig. 4. The full bridge converter consists of four transistors which are located in a TO263 package. The gate signals of the transistors are generated on another PCB which can be attached by connectors. The transistors are cooled through the PCB which is mounted with an isolation pad on a grounded heat sink. All electrically conductive areas of the full bridge converter form a parasitic impedance to the grounded heat sink. In detail, the impedance between the dc link terminals to ground $Z_{DC+,L}$ and $Z_{DC-,L}$, as well as the grounding impedances at both load terminals $Z_{HBA,L}$ and $Z_{HBB,L}$ are evaluated.

A conceivable field of application of the approach are power electronic converters for electrical machines. Hence, the inductor L_1 of the load is located in a machine housing to ensure realistic parasitic impedances. The resistors R_1 and R_2 are used to emulate the induced voltage of an electrical machine. They are placed at the two inductor terminals to create symmetrical parasitic impedances at both inductor terminals. $Z_{load1,L}$ and $Z_{load2,L}$ represent the grounding impedances of the load.

To create the same switching pattern as the power electronic system, also a full bridge converter is used as the opposing noise source. The opposing noise source itself forms parasitic grounding impedances $Z_{HBA,O}$, $Z_{HBB,O}$, $Z_{DC+,O}$, $Z_{DC-,O}$. The opposing noise source is connected to an impedance network. The grounding impedances $Z_{load1,O}$ and $Z_{load2,O}$ are formed with discrete elements by using the impedance network.

Opposing Noise Source

The main goal of the opposing noise source is to generate an inverse changing potential over the impedance network. Furthermore, the design of the opposing noise source attempts to form the same parasitic impedances to ground as the power electronic system. Therefore, three different designs are realized and evaluated.

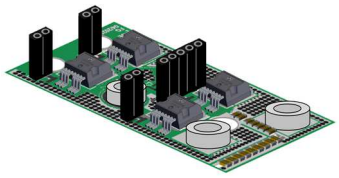

Fig. 4: Design of the full bridge converter (design 1)

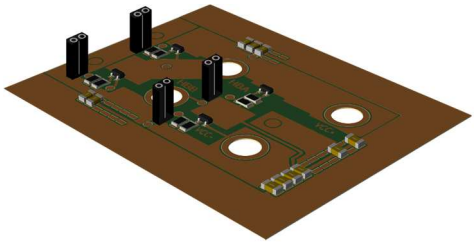

Fig. 5: Design 2

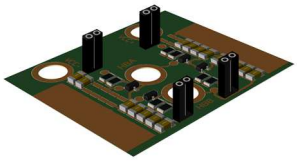

Fig. 6: Design 3

Design 1 uses the same power electronic setup for the opposing noise source as the load setup in Fig. 4. In that case, the copper areas are the same and therefore, the same parasitic impedances are formed. Although the switching transition slopes are dependent on the load current, with the use of same transistors, the derivative of the potential change is more similar as with different transistors.

Design 2 in Fig. 5 tries to omit the expensive power transistors and uses cheap signal transistors instead. This is possible as the filter full bridge converter only needs to carry the disturbance current. On the other hand, the use of different transistors influences the switching transition slope. The copper areas on the additional power electronic setup have the same size as the load power electronic. Additional discrete capacitances can be placed on the ground plate to adjust the parasitic impedance. By using the same copper area, the size of the additional noise source is equal to the power electronic setup and therefore not minimal.

In design 3, shown in Fig. 6, the goal is to minimize the opposing noise source. Therefore, the parasitic impedance is emulated only with discrete elements. Similar to design 2, cheap signal transistors are used to generate a changing potential. With this design the size of the opposing noise source is the smallest, but the emulated impedance has to be accurate.

To design the right discrete elements of design 2 and 3, the grounding impedances $Z_{\mathrm{DC+,L}}$, $Z_{\mathrm{DC-,L}}$, $Z_{\mathrm{HBA,L}}$ and $Z_{\mathrm{HBB,L}}$ of the power electronic system are measured with an impedance analyzer (Omicron Lab. Bode 100). The measurements are depicted in Fig. 7. The impedance courses of all impedances of the power electronic system show capacitive behavior in the considered frequency range. For this reason, only capacitors are used to adapt the grounding impedances $Z_{\mathrm{DC+,O}}$, $Z_{\mathrm{DC-,O}}$, $Z_{\mathrm{HBA,O}}$ and $Z_{\mathrm{HBB,O}}$ with discrete elements. With an iterative process the values of the required capacitances $C_{\mathrm{DC-}}$, $C_{\mathrm{DC+}}$, C_{HBA} and C_{HBB}, depicted in Tab. I, are found. Using these values, the impedance courses of design 2 and 3 indicated with O2 and O3, match with the impedance courses of the full bridge converter.

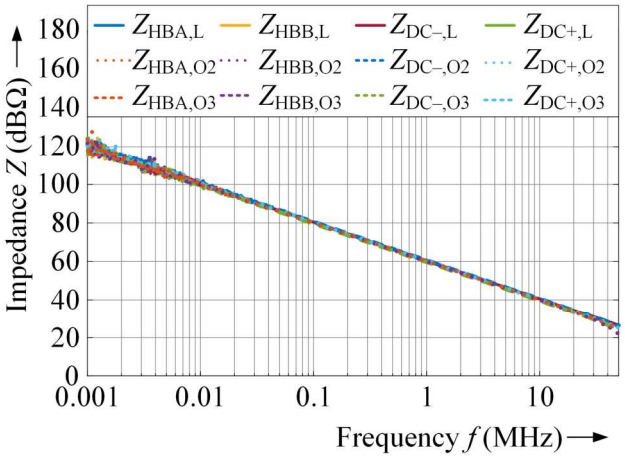

Fig. 7: Grounding impedances of the full bridge converter

Table I: Values of the used capacitances

	C_{DC+}	C_{DC-}	C_{HBA}	C_{HBB}
Design 2	66 pF	68 pF	55 pF	61 pF
Design 3	90 pF	95 pF	100 pF	96 pF

Design of the Impedance Network

To find a matching replication, the ohmic inductive load connected to the full bridge converter is evaluated. The connected ohmic inductive load can be described with the impedance circuit in Fig. 8 [10]. Two resistors are connected symmetrically to both terminals of the inductor. The two resistors are considered with its resistive part $R_{add,1}$ and $R_{add,2}$, and its parasitic inductive part $L_{add,1}$ and $L_{add,2}$. The inductor is located in a grounded machine housing. In particular the copper wires of the inductor are coiled around a stator tooth to ensure realistic parasitic impedances.

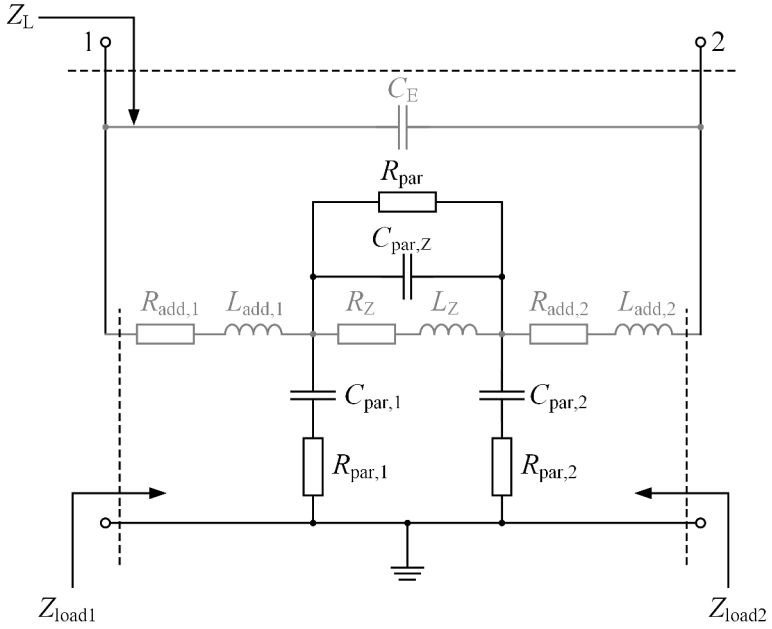

Fig. 8: Impedance circuit of the load

The impedance between the terminals of the inductor is modelled with R_Z and L_Z for frequencies below the resonance frequency and R_{par} and $C_{par,Z}$ are needed to describe the impedance in the frequency range above the resonance frequency. Between the windings of the inductor and the grounded machine housing a parasitic impedance is formed. Because the windings are coiled in several layers, the distance and therefore the effective parasitic impedance between the windings at both inductor terminals differ from each other. These grounding impedances are considered with $C_{par,1}$ and $R_{par,1}$ at one inductor terminal as well as with $C_{par,2}$ and $R_{par,2}$ at the other inductor terminal.

To generate the opposing common mode noise, which is propagating through the grounding impedances, an impedance network with discrete elements is designed. Therefore, the impedance courses of the parasitic impedances $Z_{load1,L}$ and $Z_{load2,L}$ of the load system need to be replicated as well as possible. The main focus is the frequency range close to the resonance frequency at around 6 MHz because in this frequency range the impedance is the lowest and vice versa the disturbance current is the biggest.
The resonance frequencies f_1 for Z_{load1} and f_2 for Z_{load2} can be calculated with:

$$f_1 = \frac{1}{2\pi}\sqrt{\frac{1}{(L_{\text{add1}} + L_{\text{add2}})\cdot\left(C_{\text{par,1}} + \frac{C_{\text{par,Z}}\cdot C_{\text{par,2}}}{C_{\text{par,Z}} + C_{\text{par,2}}}\right)}} \tag{1}$$

$$f_2 = \frac{1}{2\pi}\sqrt{\frac{1}{(L_{\text{add1}} + L_{\text{add2}})\cdot\left(C_{\text{par,2}} + \frac{C_{\text{par,Z}}\cdot C_{\text{par,1}}}{C_{\text{par,Z}} + C_{\text{par,1}}}\right)}} \tag{2}$$

Both grounding paths are linked with the parasitic capacitance $C_{\text{par,Z}}$ in the considered frequency range, also seen in (1) and (2). The inductance L_Z and the resistance R_Z have a negligibly small impact on the grounding impedances Z_{load1} and Z_{load2}. Because the impedance Z_L between the inductors terminals is insignificant for the approach, those two elements are neglected in the discrete impedance network to save space. Furthermore, the impedance network is connected to the same resistors as the load. Hence, the elements $R_{\text{add,1}}$, $R_{\text{add,2}}$, $L_{\text{add,1}}$, $L_{\text{add,2}}$ and C_E are already existing and are not replicated with the impedance network. The impedance network is built up with the values in Tab. II and measured with an impedance analyzer. The measurements of the impedance Z_L, depicted in Fig. 9, show big differences between the parasitic and replicated course. Due to the missing elements L_Z and R_Z the differences are as expected, but as mentioned not important for the approach.

Table II: Values of the impedance network

$C_{\text{par,Z}}$	$R_{\text{par,Z}}$	$R_{\text{par,1}}$	$R_{\text{par,2}}$	$C_{\text{par,1}}$	$C_{\text{par,2}}$
45 pF	2.8 kΩ	0 Ω	0 Ω	52 pF	51 pF

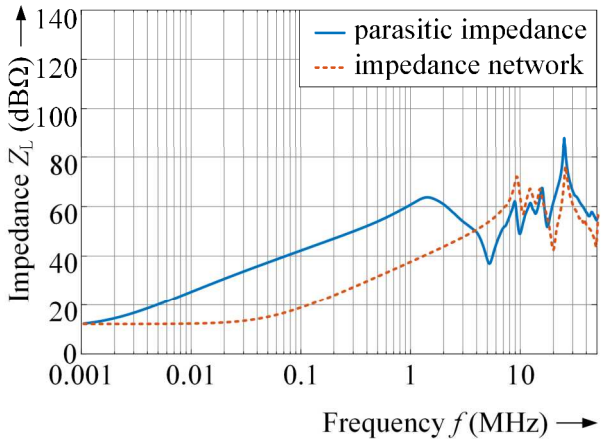

Fig. 9: Impedance between the inductor terminals

The measured impedance courses of $Z_{\text{load1,O}}$ and $Z_{\text{load2,O}}$ are shown in Fig. 10. Despite the missing elements L_Z and R_Z both impedance courses show a good replication of the original impedance course in the expanded view. Between 400 kHz and 1.5 MHz the courses slightly differ, due to an extra resonance. Also in the high frequency range, the replication is not accurate. The detailed view shows a good replication of $Z_{\text{load1,L}}$ with $Z_{\text{load1,O}}$ at the resonance frequency, but the replicated impedance $Z_{\text{load2,O}}$ differs slightly from the measured parasitic impedance $Z_{\text{load2,L}}$.

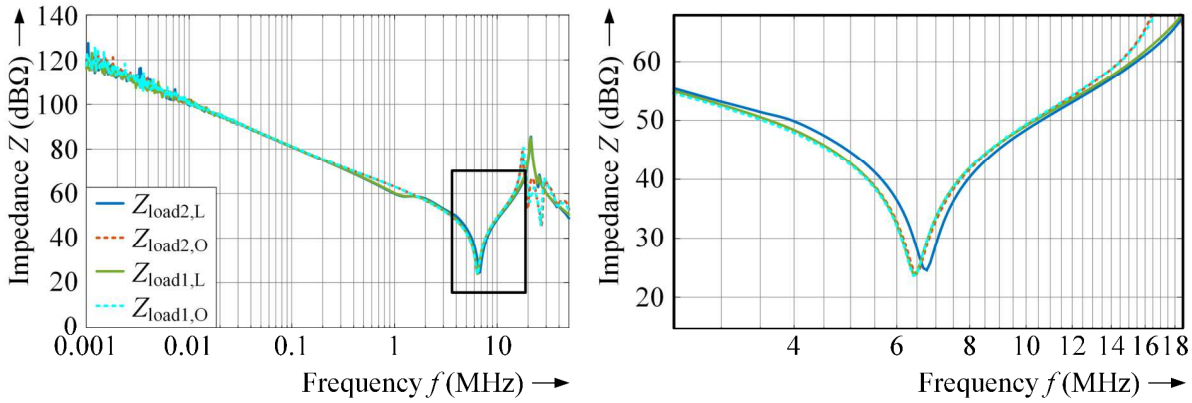

Fig. 10: Grounding impedances – expanded view (left) and detailed view (right)

Timing

For the best reduction of the disturbance currents, the changing potentials in both systems have to occur at the same time. In the opposing noise source the current direction in the power electronic system has to be considered. Depending on the current direction, the commutation type at the half bridges is either hard or soft. If the commutation type is hard, the potential change occurs before the dead time. If the commutation type is soft, the changing potential occurs after the dead time. Hence, the gate signals of the opposing noise source have to be shifted by the dead time dependent on the load current direction. Furthermore, to improve the reduction of the common mode noise, differences in the propagation delay of the gate signals should be adjusted. The gate signals are generated with a rapid prototyping system and afterwards processed with a FPGA. For large time shifts in terms of the dead time, delay chains are used to shift the gate signal in multiples of the FPGA clock. For small time shifts, a phase locked loop is used, which provides a precise timing in steps down to 120 ps. With the combination of both options the timing can be adjusted in a wide time range in a fine resolution. In this approach, the best timing is set manual.

Measurements and Results

The overall structure in Fig. 3 is built up on an electrically conductive ground plane. To provide a defined input impedance, two line stabilization networks (LISN) are connected to every DC-link terminal. The noise current generates the disturbance voltages v_{DC+} and v_{DC-} at both 50 Ω termination resistors of the LISNs. With a power splitter, the common mode voltage v_{CM} which is measured with a spectrum analyzer (Tektronix RSA306B), can be extracted. The measurements are performed at a DC-link voltage of 48 V at a load current of 5 A. The PWM frequency is set to 20 kHz with a duty cycle of 0.5, so the time between the switching transitions of the full bridge converter is at its maximum. In this case, the affection of two consecutive noise signals is at its minimum.

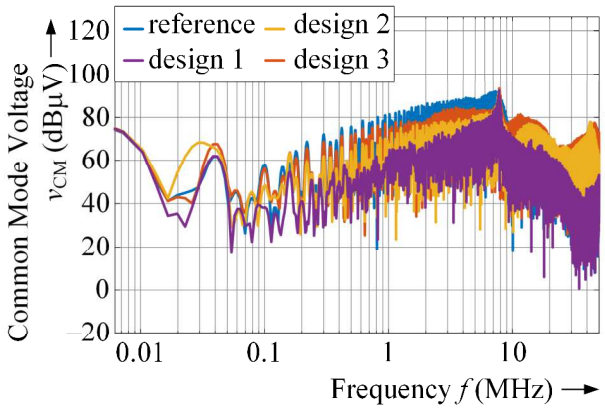

Fig. 11: Common mode voltage with different designs

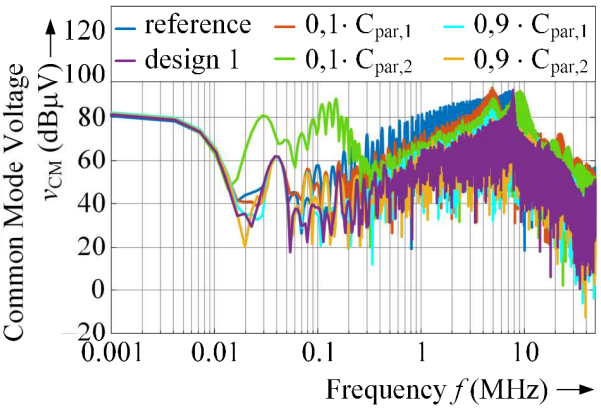

Fig 12: Common mode voltage with different values of the impedance network

The measurement results of the common mode voltage v_{CM} for the different designs of the opposing noise source and of a reference system are shown in Fig. 11. As a reference system, only the noise source connected to the load is operated. So the course depicted in blue shows the common mode voltage v_{CM} without any filtering. In all other colors the power electronic system and the opposing noise source are operated. In purple, the opposing noise source consists of the same power electronic design as the power electronic system but is connected to the discrete impedance network. In this case, the common mode voltage can be reduced over a wide frequency range. From 50 kHz to 5 MHz the reduction is more than 10 dB, at some frequencies the reduction is even higher than 20 dB. At around 8 MHz the common mode voltage peaks and no reduction to the reference system is measured. This shows that with the impedance network an opposing noise current with the same frequency spectrum can be shaped. The small differences of the impedance courses around the resonance frequency, where the noise current is the highest, have a big impact on the common mode voltage.
For the measurement results in yellow, design 2, which uses signal transistors and the same PCB areas as the load power electronic setup, is used. The reduction int the entire frequency range is lower than in the first setup. In the frequency area at the resonance frequencies the course is similar. Still, the reduction of the common mode voltage is more than 5 dB over a large frequency range. On the other hand, the common mode voltage rises at frequencies higher than 10 MHz.
With the use of design 3 as the opposing noise source, shown in red, the course of the common mode voltage is similar, but the reduction is even lower than with the second setup.
The lowered reduction of the common mode voltage with design 2 and 3 show that the signal transistors have an impact on the approach. Reasons can be differences in the grounding impedances and differences in the switching transitions slopes.

To evaluate how accurate the discrete elements have to be, the values of the discrete elements are changed. Design 1 is used as the opposing noise source due to the best results. The grounding capacitances $C_{par,1}$ and $C_{par,2}$ are reduced with 10% and 90% of its value. The measurements are shown in Fig. 12. If the differences are small the course of the common mode voltage is almost the same. With large differences, the reduction of the common mode voltage decreases. Furthermore, new resonance frequencies are formed which leads to higher common mode voltages at these frequencies. This shows that small differences due to construction tolerances in the impedance network are tolerable. Large differences reduce the effectiveness of the common mode reduction. In some frequencies the common mode is even reduced. Furthermore, this evaluation shows that the values of the impedance network were suitable in the first place.

Conclusion

With an additional noise source connected to an impedance network, it is possible to reduce the common mode noise in power electronic setups which do not offer the possibility to synchronize switching transitions. Three different designs are evaluated as an opposing noise source which provide changing potentials. The parasitic impedances of the designs are adapted to the load power electronic setup. Using the same design as the power electronic system provides the best results. By using cheaper signal transistors, the common mode noise can still be reduced, but the reduction is smaller due to differences in the grounding impedances and in the switching transition slopes. A space-reduced design, which emulates the grounding impedances with capacitances, lowers the reduction of the common mode noise. Future work will investigate adjustments of the switching transition slopes to improve the results.

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