Common-Mode EMI Noise Modeling of Three-Level T-Type Inverter for Adjustable Speed Drive Systems

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Keywords

≪Adjustable speed drive≫, ≪Electromagnetic Interference (EMI)≫, ≪EMC/EMI ≫, ≪MOSFET≫, ≪T-type inverter≫

Abstract

This article studies the EMI noise modeling of a three-level T-type inverter (3LT^{2}I) for adjustable speed drive (ASD) systems. A methodology to generate the common-mode (CM) voltages in the time-domain is proposed based on SiC MOSFETs switching behavior, such as the variable rise and fall times. The frequency spectrums of the time-domain voltages are used with the CM noise paths to predict the CM current of the 3LT^{2}I. The CM noise model of the 3LT^{2}I consists mainly of two CM noise sources. The effect of these noise sources on the CM current is investigated. The proposed EMI noise prediction method is validated by the comparison between the simulation and experimental results of the CM voltage and CM current spectrums.

Introduction

The 3LT^{2}I is becoming a popular topology because of its advantages, such as low total harmonic distortion (THD) and switching losses compared to a two-level voltage source inverter (2L-VSI) [1]. It also provides a better EMI behavior in the medium and low power ranges [2]. Wide-bandgap semiconductors, such as silicon carbide (SiC) MOSFETs, are increasingly used within 3LT^{2}I since they have significant operational advantages, in particular switching at higher current and voltage, with low switching losses and higher operating temperatures. However, the fast switching speed of SiC MOSFETs results in high-voltage slew rates ($\mathrm{d}v/\mathrm{d}t$), which leads to increasing EMI challenges, higher bearing currents in motors and deterioration in the insulation of motor windings [3–5]. Standards such as EN 50121 and IEC 61800 set the limits of EMI emissions to ensure that the system is electromagnetically compatible with its environment. An accurate EMI prediction model must be developed in order to evaluate the EMI performance of the 3LT^{2}I with parasitic capacitances. The prediction model will help designers to take early precautions in the design phase against the EMI noises.

The EMI noise modeling of the 2L-VSI has been widely conducted in the literature [6–9]. While each phase of a 2L-VSI has only one voltage varying node, the three-level neutral point clamped (3L-NPC) has rather three and the 3LT^{2}I has two voltage varying nodes. The increase in voltage-varying nodes complicates the EMI modeling of three-level inverter topologies. Most EMI models of the 3-level inverter

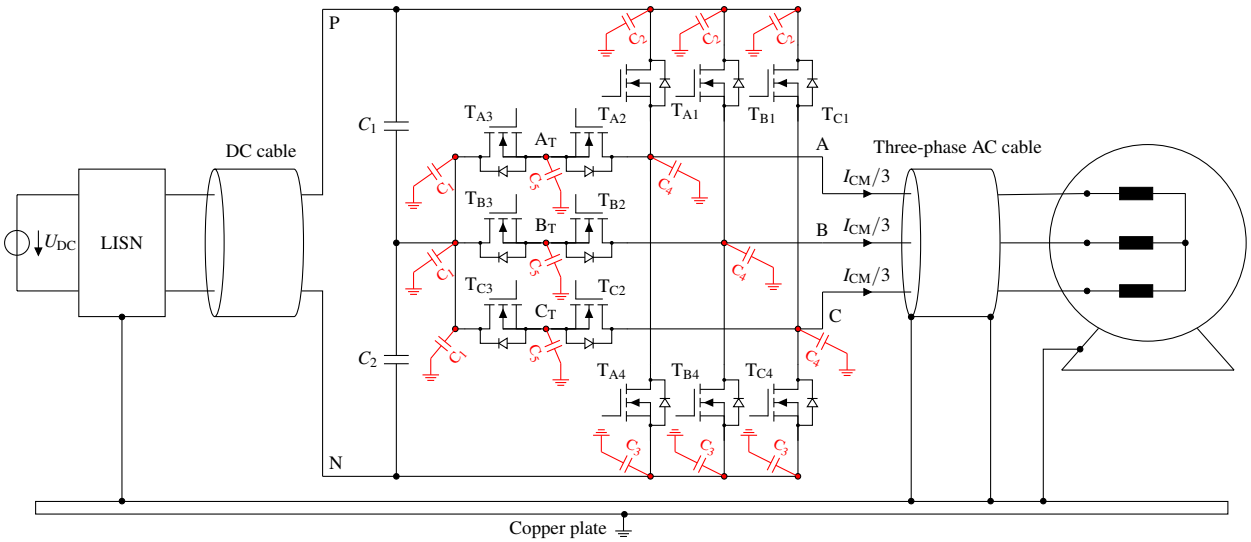


Fig. 1: Topology of a 3LT^{2}I for an ASD system with line impedance stabilization network (LISN) and parasitic capacitances.

– mainly the 3L-NPC – are focused on photovoltaic or grid applications [10–14]. However, no study has been conducted on the EMI modeling of the 3LT^{2}I for an ASD system, which is shown in Fig. 1.

The voltage spectrum used in the frequency-domain model can be obtained from the simulated or measured time-domain voltage waveforms using Fourier transform. In some papers, the switching waveforms are modeled as trapezoidal waves [9, 15]. In [13, 16], the switching waveform accuracy is improved by adding the ringing effect of the switching devices. Although the real switching waveform has variable commutation times, these models proposed to rather use fixed commutation times, which reduces the accuracy of the frequency-domain simulations. Furthermore, the model in [17] proposes an approach based on the switching behavior of SiC MOSFET, such as the variable rise and fall times. Nevertheless, the ringing effect is not considered in [17].

In this paper, a frequency-domain CM noise model is proposed for a 3LT^{2}I used in ASD systems. First, the CM noise sources for the 3LT^{2}I are derived, and a methodology to generate time-domain CM voltages is proposed based on SiC MOSFETs switching behavior. Then, the CM noise propagation paths of the ASD system are presented. Finally, the simulation and experimental results are provided to validate the proposed EMI modeling for the 3LT^{2}I.

Common-Mode Model for Three-Level T-Type Converter

The EMI noises can be simulated either in time-domain or in frequency-domain [9]. Frequency domain models are often used to simulate the EMI noise due to their simplicity and reduced computational effort [6]. Therefore, the frequency-domain EMI approach will be used in this article. Moreover, it should be noted that the asymmetry due to an unbalanced impedance in the three-phase system and the nonlinear operation of the inverter leads to a coupling between CM and differential-mode (DM) noises [18–20]. This type of noise is called the mixed-mode effect. For the sake of simplicity, the decoupled CM noise model in the frequency-domain is used in the proposed method, as it has also been considered in [6, 7, 10, 11].

Common-Mode Voltage Source Modeling

The CM model of three-phase 3LT^{2}I begins from analyzing a single-phase leg with parasitic capacitances, as shown in Fig. 2(a). The parasitic capacitance between the single-phase leg circuit and the grounded heatsink are presented by C_1– C_5. Discrete SiC MOSFETs are used in the 3LT^{2}I circuit. The parasitic capacitances of the drain of SiC MOSFETs to the heatsink (C_{MH}) and the parasitic capacitances of the printed circuit board (PCB) traces to the heatsink ($C_{PCB,H}$) have an important effect on the EMI

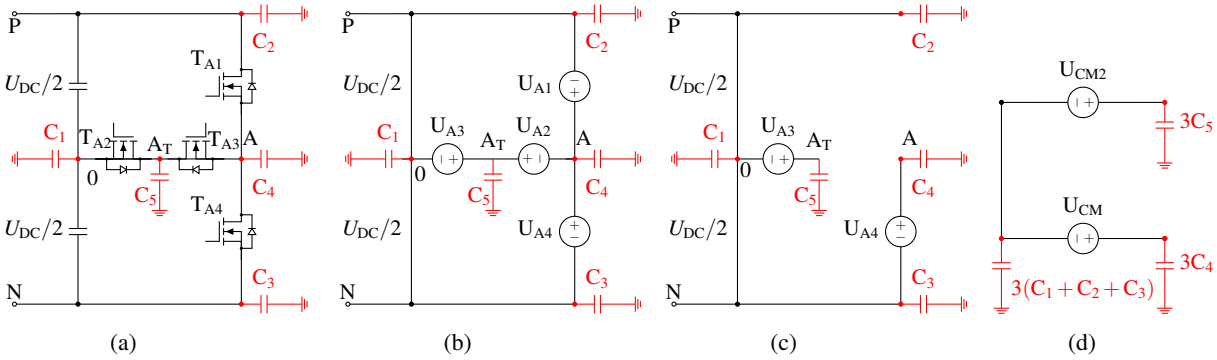


Fig. 2: Extraction of 3LT^{2}I CM model. (a) A phase of the 3LT^{2}I with parasitic capacitances. (b) Replacement of the switching devices by voltage sources. (c) Elimination of U_{A1} and U_{A2}. (d) The 3-phase CM model.

modeling of 3LT^{2}I. C_1 represents the parasitic capacitance between the midpoint of dc-link capacitors and the ground. C_2 is the combined parasitic capacitances of the drain of T_{A1} to the heatsink and the node P to the heatsink. C_3 is the node N to the heatsink parasitic capacitance. Furthermore, the parasitic capacitance of phase A and C_{MH} are summed up and presented as C_4. Since the bidirectional switches located at the midpoint leg has the common drain configuration, the parasitic capacitance of the common drain is determined by

$$C_5 = 2C_{MH} + C_{PCB,A_T}. \tag{1}$$

In general, semiconductors are replaced either by voltage or current sources within EMI prediction models, with the so-called substitution theorem [10, 11]. The switching devices are substituted with voltage sources to reflect the CM voltage behavior appropriately, as shown in Fig. 2(b). It is important to understand that these noise sources have the same time-domain waveform of the switching devices. The dc capacitors are short-circuited in Fig. 2(b) due to their small ac impedances. It must be ensured that the voltage sources are not placed in parallel to avoid a closed loop of the voltage sources [11, 14]. Thus, the voltage source of the switch T_{A1} and T_{A2} are eliminated, as shown in Fig. 2(c). The switching voltages U_{A3} and U_{A4} equal U_{A_T0} and U_{A0}, respectively. Finally, the CM EMI model of the 3LT^{2}I is obtained by extending the single-phase model in Fig. 2(c) to Fig. 2(d), where the CM voltages can be expressed as follow:

$$U_{CM} = \frac{U_{A0} + U_{B0} + U_{C0}}{3}, \tag{2}$$

$$U_{CM2} = \frac{U_{A_T0} + U_{B_T0} + U_{C_T0}}{3}. \tag{3}$$

The voltage source model in [17], which is for a 2L-VSI, will be modified for the 3LT^{2}I, and the ringing effect will be added. Fig. 3 shows the proposed algorithm for the generation of time-domain voltage sources. The gate signals of the 3LT^{2}I are generated based on the pulse-width modulation (PWM) technique. The PWM technique in [21], which proposes a modulation method for the 3LT^{2}I based on two-level space vector PWM (SVPWM), is implemented. The fundamental frequency of reference voltage (f_{fund}), the switching frequency (f_{sw}), the sampling frequency (f_{samp}), the dead time (t_{dt}) and the modulation index (m) are the input parameters of the SVPWM technique. It is worth mentioning that other PWM techniques can also be used. The generated PWM signals are implemented to the 3LT^{2}I circuit in which the ideal switching devices are used to obtain the output pulse voltages. On the output of the 3LT^{2}I, a three-phase star or delta RL load is connected, through which the values depend on the reactive and active power of the motor. The ideal source voltages U_{A0}, U_{B0} and U_{C0} in (2) together with U_{A_T0}, U_{B_T0} and U_{C_T0} in (3) are extracted as the output voltages ($U_{out,ideal}$) in the diagram.

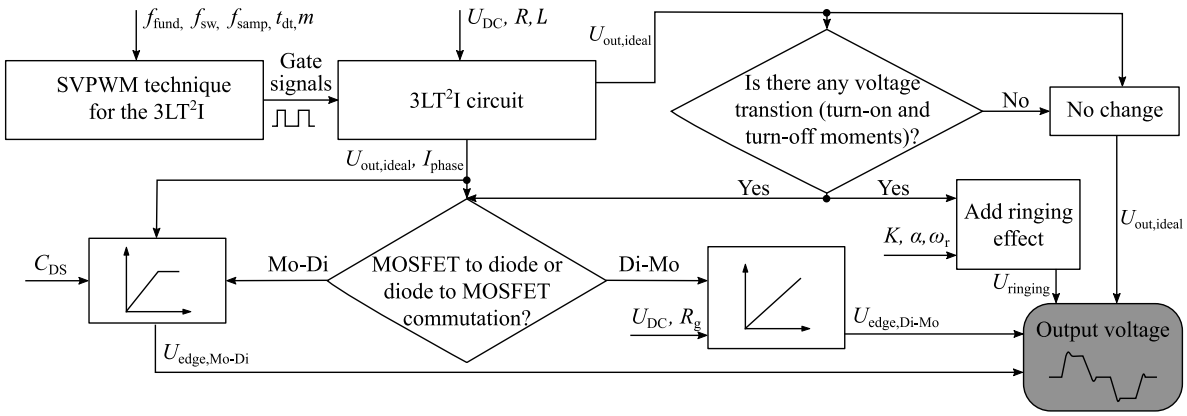


Fig. 3: The diagram for the generation of time-domain voltages of the 3LT^{2}I.

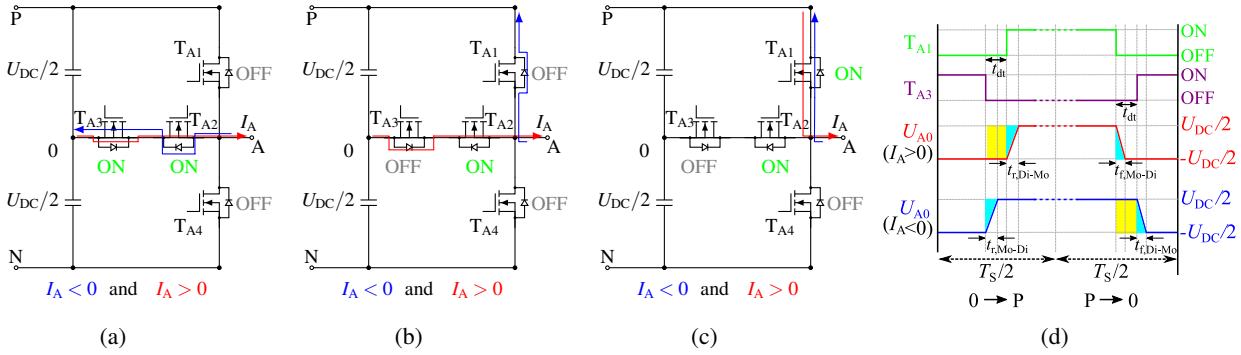


Fig. 4: 0→P transition of a single-phase leg of the 3LT^{2}I. (a) Steady-state before 0→P transition. (b) During the dead-time period. (c) Steady-state after 0→P transition. (d) Gate signals (T_{A1} and T_{A3}) and output voltage waveform (U_{A0}).

According to applied PWM signals and output phase currents, two commutation types occur: 1) MOSFET to diode commutation and 2) diode to MOSFET commutation. There are four possible output voltage state transitions of the 3LT^{2}I: P→0, 0→P, 0→N, and N→0. The semiconductors' rise and fall times during these transitions must be considered to model the voltage sources accurately. In Fig. 4, the switching behavior of a single-phase leg of the 3LT^{2}I during 0→P transition is analyzed under different current directions. A dead-time is set between the switch T_{A1} and T_{A3} gate signals in order to avoid shoot-through fault, as illustrated in Fig. 4(d). When the phase current is negative ($I_A < 0$), the MOSFET to diode commutation takes place during the dead-time period, as can be seen in Fig. 4(a) and 4(b). First, I_A charges the drain-source capacitance of T_{A3}, and the drain-source voltage of T_{A3} starts to increase while the current flows through the midpoint leg remains almost constant [17]. The internal diode of T_{A1} becomes forward biased after U_{A0} reaching $\frac{U_{DC}}{2}$. A similar MOSFET to diode commutation is observed in P→0 transition in the case of the positive phase current ($I_A > 0$), as shown in Fig. 4(d). The voltage rise time (t_r) and fall time (t_f) of the MOSFET to diode commutation are defined by the MOSFET drain-source capacitance (C_{DS}) as:

$$t_{edge,Mo-Di} = \frac{C_{DS}\frac{U_{DC}}{2}}{I_A} = \frac{Q_{DS}}{I_A} \tag{4}$$

where Q_{DS} is the MOSFET charge [17]. A linear model for the capacitance is assumed in (4). Thus, the edges with variable duration occur because of the MOSFET to diode commutation in the 3LT^{2}I. On the other hand, the diode to MOSFET commutation occurs after the dead-time period in 0→P transition when the phase current is positive, as given in Fig. 4(b) and 4(c). The t_r and t_f of the diode to MOSFET commutation mainly depend on the gate resistance (R_g) and U_{DC}, also the plateau voltage (U_P) and the reverse transfer capacitance (C_{rss}) [22]. In the measurement results, it is observed that t_r and t_f are

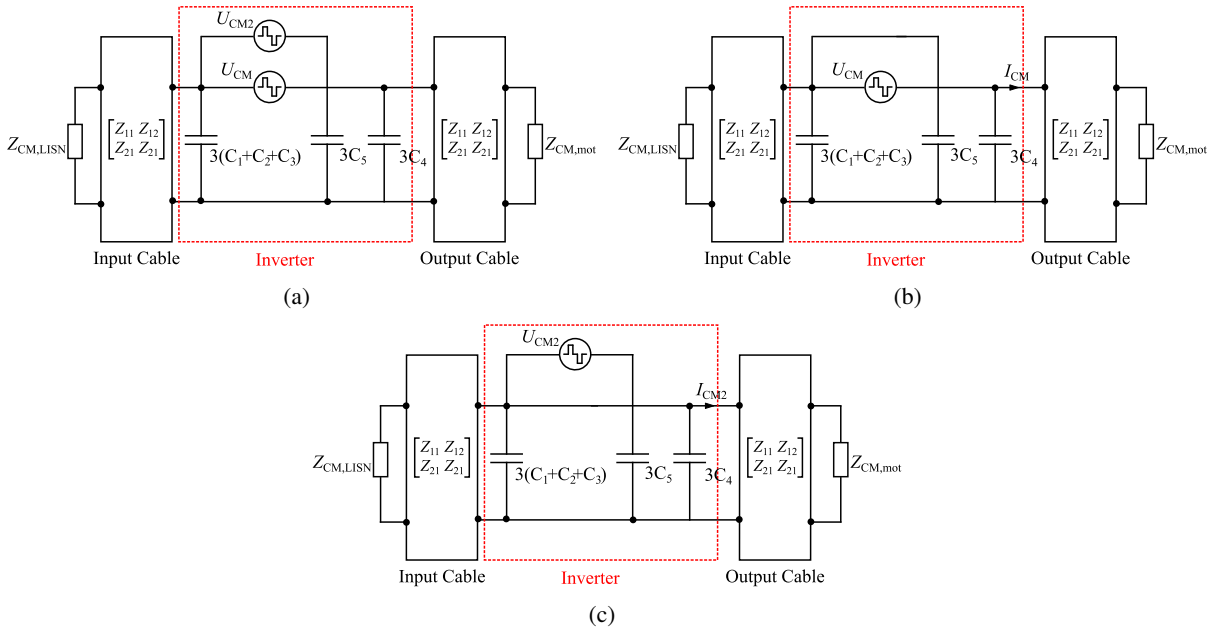


Fig. 5: The CM prediction model of an ASD system. (a) Extracted CM noise model. (b) Separate analysis of U_{CM}. (c) Separate analysis of U_{CM2}.

almost constant during the diode to MOSFET commutation. In the simulation of time-domain voltage, a constant value, which is determined from measurement results, is used for t_r and t_f of the diode to MOSFET commutation.

Finally, a damped exponential sinusoidal wave is added to the trapezoidal output voltage based on the following mathematical function:

$$U_{\text{ringing}} = K \exp(-\alpha t) \sin(\omega_r t) \tag{5}$$

where K is the magnitude of the ringing, α is the damping coefficient, and ω_r is the ringing frequency [13].

Final Common-Mode Model

The extracted CM model of the 3LT^{2}I in Fig. 2(d) is connected to the other noise paths of the ASD system, as shown in Fig. 5(a). The two-port impedance matrices of input and output cables are used to ensure that the model accurately characterizes the cable properties. CM impedance of the ADS system components and the parasitic capacitances of the 3LT^{2}I can be determined by direct measurements or simulation models. In the presented model, the measurement of CM impedance of the ADS system components and the parasitic capacitances of the drain of SiC MOSFETs to the heatsink are used. Furthermore, a finite element method (FEM) tool is used to find the parasitic capacitances between PCB and the heatsink.

There are two voltage sources in Fig. 5(a) and their spectrum forms are acquired from the time-domain voltages, which are generated based on the diagram in Fig. 3. It should be noted that the response of a linear circuit having two independent sources can be obtained by applying superposition principle. Thus, the contributions of CM current generated due to U_{CM} and U_{CM2} can be dissected, as shown in Fig. 5(b) and Fig. 5(c). The CM current at the input of the inverter (I_{CM} and/or I_{CM2}) is then analyzed in the ASD systems.

Simulation and Measurement Results

A 20-kW 3LT^{2}I is used to validate the proposed CM voltage and current models for the ASD system in Fig. 1. The input voltage is set at 300 V, the switching frequency is 24 kHz and the modulation index is

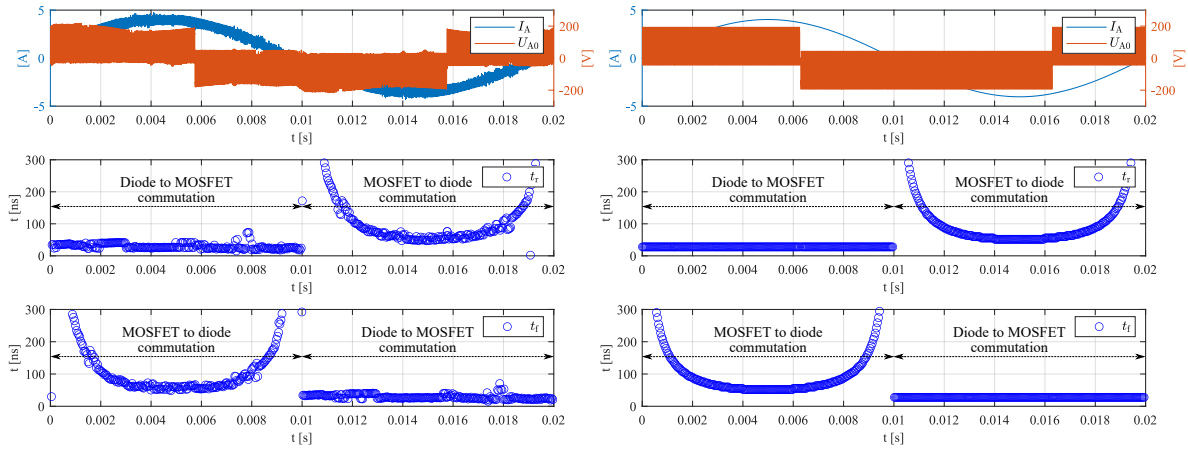


Fig. 6: (a) Measured and (b) simulated phase current (I_{A}), phase voltage (U_{A0}), the rise time (t_{r}) and fall time (t_{f}).

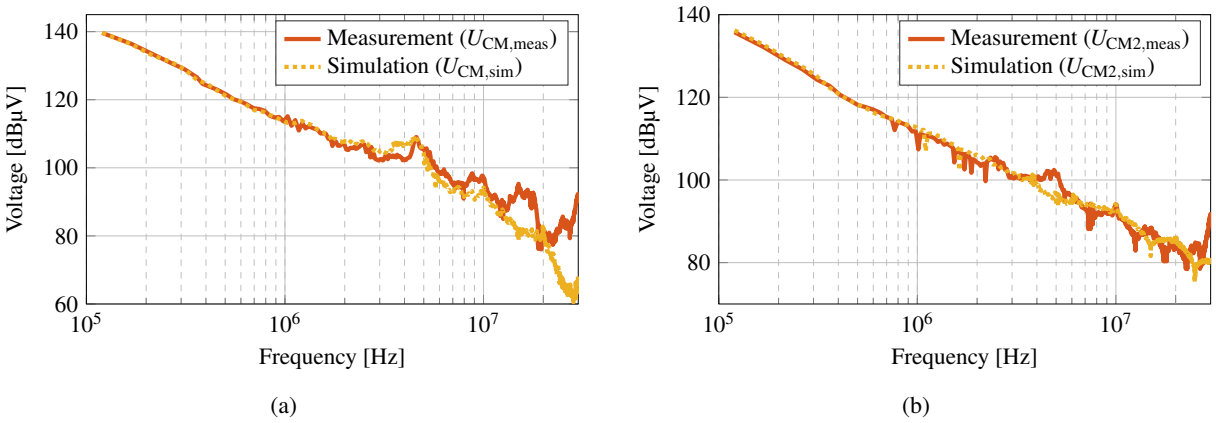


Fig. 7: Comparison between measured and simulated CM voltage sources. (a) U_{CM}. (b) U_{CM2}.

0.8. A Keysight E5061B vector network analyzer (VNA) with a test fixture 16047E is used to measure the SiC MOSFETs drain to the heatsink parasitic capacitances, the motor CM impedance and 2-port cable impedances in Fig. 5(a).

Fig. 6 shows the measured and simulated phase A current and voltage with respective commutation times (t_{r} and t_{f}). For each switching even, the value of the corresponding commutation time is displayed as a single circle in the graph. Fig. 6(a) shows that the duration of the measured diode to MOSFET commutation are concentrated around 30 ns. However, the MOSFET to diode commutations in the corresponding figure have variable t_{r} and t_{f}, which is from 50 ns to the dead time. The variable phase current is the main reason for the variable commutation times, as it was defined in (4). Furthermore, the measured and simulated results in Fig. 6 show that the proposed time-domain voltage model replicates the SiC MOSFETs switching behaviors, such as t_{r} and t_{f} of both commutation types.

The short window discrete Fourier transform (SWDFT) is applied to get the frequency domain peak value of the voltage and current spectrums, as described in [17]. Fig. 7 shows that the prediction of CM voltage has good agreement with the measured CM voltage. In the high-frequency range (10-30 MHz), there are 5-20 dBµV mismatches, and it can be explained by the non-linear switching behavior of SiC MOSFET, which was ignored in the proposed model.

Next, the CM current contributions generated due to U_{CM} and U_{CM2} will be investigated. The measured voltage spectrums in Fig. 7 are used to maximize the accuracy of the CM current in the simulation. The proposed CM current prediction model in Fig. 5(b) and Fig. 5(c) are simulated in the frequency-domain.

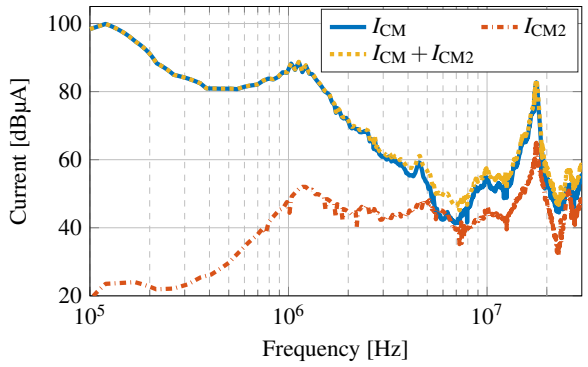


Fig. 8: Comparison between simulated I_{CM} and I_{CM2}.

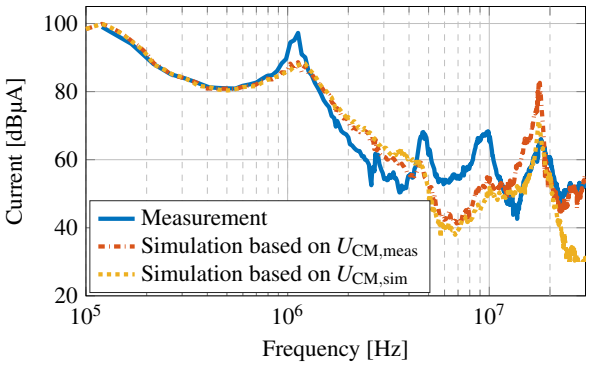
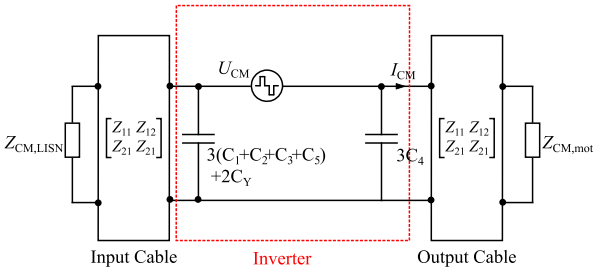
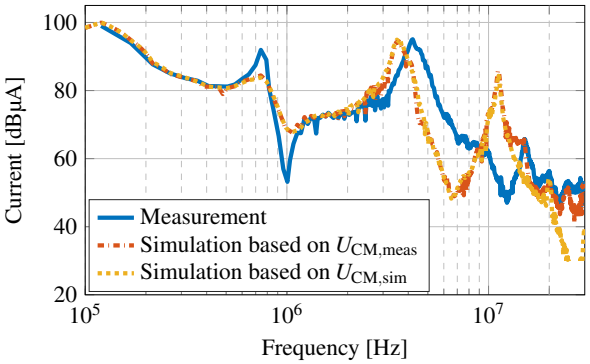


Fig. 9: Comparison between measured and simulated CM currents.



(a)



(b)

Fig. 10: (a) CM noise model after adding Y-capacitors between dc-link capacitor points and the heatsink. (b) Comparison between measured and simulated CM currents after adding Y-capacitors.

Fig. 8 shows separately calculated CM currents (I_{CM} and I_{CM2}) along with the overall CM current ($I_{CM} + I_{CM2}$) which is calculated based on the superposition principle. It can be observed that there is almost no effect of I_{CM2} on the overall CM current until 5 MHz. Although I_{CM2} relatively increases the overall CM current at high frequencies, I_{CM} is still the dominant CM current. Therefore, the CM current generated as a consequence of U_{CM2} can be ignored, and the model in Fig. 5(b) can be used as the final CM EMI noise model.

Fig. 9 shows the comparison between the measured and the simulated CM current results. First, the measured voltage spectrum of Fig. 7(a) ($U_{CM,meas}$) is used in the CM noise model. Even though some differences are observed in the high-frequency range, simulation and measurement results are in good agreement. The high-frequency mismatches between the measurement and simulation based on $U_{CM,meas}$ are due to the neglected stray inductance of the dc capacitors, the measured impedance errors and the mixed mode noise effect. Second, the simulated voltage spectrum in Fig. 7(a) ($U_{CM,sim}$) is used to find the CM current. The results in Fig. 9 show that the proposed CM current model is capable of sufficient accuracy when the simulated CM voltage based on SiC MOSFETs switching behavior is used. Furthermore, two Y-capacitors (C_Y) are connected between dc-link capacitors points (P and N) and the heatsink in order to analyze the proposed method under different situations. The CM noise model with the added Y-capacitors is given in Fig. 10(a), and the measured CM current is compared with the simulation results in Fig. 10(b). The change of the CM current is adequately covered in the new situation.

Conclusion

This article studied the CM voltage and current modeling of a 3LT^{2}I. First, the noise sources and propagation paths of the 3LT^{2}I were extracted. Then, a circuit model was developed by connecting the inverter

model to the other noise propagation paths of the ASD system. The simulation result of the CM voltage and current of the model showed a good agreement with measurements, although some differences were observed in the high-frequency range due to the simplifications.

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