A new power MOSFET technology achieves a further milestone in efficiency

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Abstract

This work introduces the characteristics and properties of the latest trench MOSFET technology released to the market. Based on the advantages of a revolutionary new cell design combined with the benefits of an advanced manufacturing technology, this new device family brings together the benefits of exceptionally low conduction losses, superior switching performances, improved SOA and good ruggedness. These features make it the best fit for high switching frequency applications, supporting the trend towards significantly higher efficiency while enabling designs for higher power densities and cost effectiveness. Typical applications for these MOSFETs include telecom, server, datacom as well as solar applications, drones, e-bikes, power tools and many other battery-powered applications (BPA). Results presented in this work focus on the 100 V voltage class intended for use in fast switching DC/DC telecom switch-mode power supplies (SMPS), and compares the new technology with its predecessor generation.

1. Introduction

Since their introduction, MOSFET technologies have been noted as excellent candidates to be used as switches in power management circuits. Vertical diffused MOSFET (VDMOS) structures, commercially available since the late seventies, first addressed the needs of a power switch [1]. The superior switching performance and the high input impedance placed the MOSFET as an appealing alternative to bipolar technologies. Still, the high on-state resistance limited the current-handling capabilities of the VDMOS and its applications in the power electronics industry. In a medium-voltage VDMOS, the major contributors to the total on-state resistance between drain and source are represented by the intrinsic channel resistance and by the JFET region limiting the channel current flow into the epitaxially-grown drift region (Fig. 1a). Overcoming this limitation required more than a decade of development in device design and process engineering, which culminated in the late 1980s with the commercialization of the first trench gate MOSFETs. The development of trench power MOSFETs was a milestone for the broad adoption of the field-effect transistors in the power electronics industry [1-3]. By moving the channel to the vertical direction, this device concept allowed a reduction in cell pitch without adversely affecting the current spreading by virtually removing the JFET region, hence dramatically reducing the on-state resistance (Fig. 1b). The achieved ultralow specific channel resistance no longer prevented low on-state resistances, although as a result the substrate and package resistances became significant contributors. However, the remarkable increase in cell density, besides finally establishing the trench MOSFET as a competitive alternative to the planar technology, has also brought to light significant disadvantages. The gate-drain capacitance (related to trench gate penetration in the epi drift region) and gate-source capacitance (overall capacitance between trench gate and source diffusion) increase linearly with the number of trenches, i.e. with the cell density. Together with a sublinear scaling in the on-resistance $R_{DS(on)}$, this significantly impacts the technology figure-of-merit $FOM_g = R_{DS(on)} \times Q_g$. Since the MOSFET is uniquely controlled through its gate terminal, the gate driver circuitry has to provide the total gate charge Q_g required to turn on the transistor. In the case of high switching frequency applications, like SMPS, the lowest gate charge is desirable since it proportionally affects the driving losses. A part of the total gate charge is associated with the gate-to-drain charge Q_{gd}, which governs the drain voltage

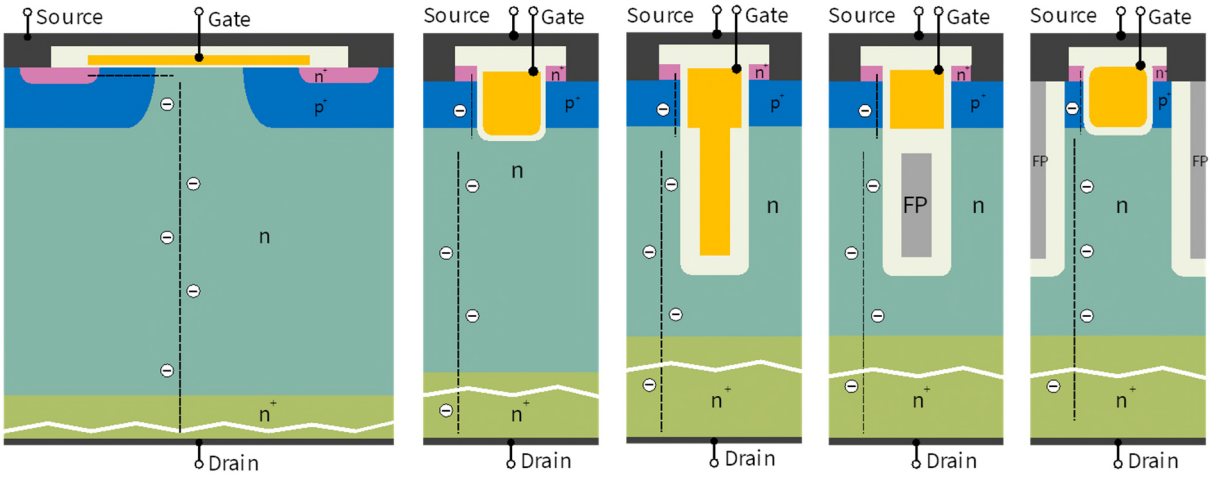

Fig. 1a-e: Exemplary device structures depicting the evolution of power MOSFET:
a) VDMOS structure with lateral channel and planar gate
b) Trench MOSFET structure with vertical channel
c) Trench MOSFET with lateral charge-compensation by a gate-connected field-plate
d) Trench MOSFET with lateral charge-compensation by an insulated field-plate connected to source
e) Trench MOSFET with lateral charge-compensation by an insulated field-plate and separated gate trench

transient. A higher Q_{gd} impacts the transient speed, increases the switching losses, and forces the use of longer dead-times. It became evident that specific measures were needed to reduce the overall gate and gate-drain charge. Additionally, another constraint is imposed by the Miller charge ratio: $Q_{gd}/Q_{gs(th)}$ must be lower than one if the intrinsic robustness against parasitic turn-on of the MOSFET under fast drain voltage transients is to be guaranteed [4].

A new era started with the introduction of charge-compensated structures, exploiting the same principle as super junction devices. The introduction of devices which use an insulated deep field-plate as an extension of the gate electrode enabled the lateral depletion of the drift region in the off state (Fig. 1c) [5]. The lateral depletion alters the electric field distribution throughout the structure, allowing the same voltage to be blocked within a shorter length. Since the electric field can be supported by a thinner and more heavily doped drift region, a substantial reduction in the on-state resistance can be achieved. It is worth noticing that the field-plate (as an extension of the gate electrode) leads to both a significant increase of the reverse-transfer capacitance C_{gd} (hence also Q_{gd} and Q_g) and a nonlinear dependence on the drain voltage. In fact, the transfer capacitance drops abruptly as soon as the mesa region completely depletes. These disadvantages were soon overcome by the use of a field-plate, which was isolated from the gate electrode and instead electrically connected to the source potential (Fig. 1d). While the charge compensation principle operates as before, the buried field-plate does not introduce any additional contributions to the gate-drain capacitance. Instead, the field plate shields the gate electrode from the drain potential, which reduces the gate-drain capacitance C_{gd} and related charges. These devices, at the time of their introduction to the market, showed best-in-class performance with low gate-charge and gate-drain charge characteristics, high switching speeds and good avalanche ruggedness [6]. Still, the presence of the field plate comes with the disadvantage of an increased output capacitance C_{oss} and output charge Q_{oss} - a consequence of the lateral charge-compensation. However, careful device optimization enabled field-plate based power technologies with FOM_{oss} comparable to those of the standard trench MOSFET [7]. These attributes made them even more suitable for a wide variety of switched-mode power supply (SMPS) applications.

2. Features and advantages of the new device technology

2.1 Novel cell design approach

In the development of a new silicon technology, special care must be taken in the definition of its specifications, in order to bring significant system-level advantages and to add value for the customer. The new device was required to provide improvements across all figures of merit, as this is needed to enable high-frequency SMPS operation where losses are associated both with charges (switching) and on-state resistance (conduction).

To meet these more demanding requirements, a novel cell-design approach, which explores a true three-dimensional charge compensation, has been developed and implemented. To follow this path, one first needs to enable a direct connection to the field-plate electrodes from above as illustrated in Fig. 1e. Second, the device layout must move away from the stripe layout, which is commonly used with charge-compensated MOSFETs

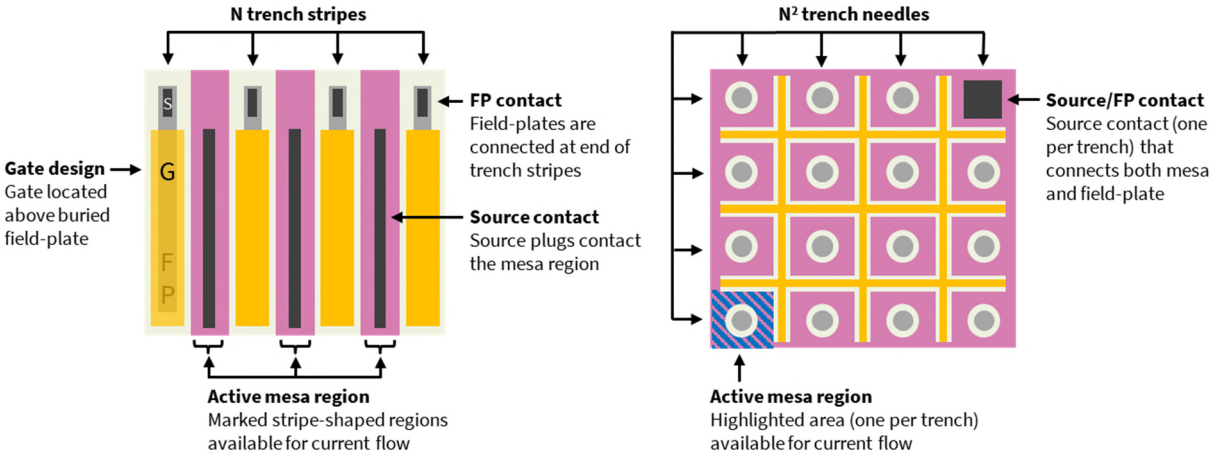

Fig. 2: Comparison of the commonly used stripe layout with the new grid-like layout approach (top-view)

employing a field plate, to a grid-like layout structure as depicted in Fig. 2. In this way the silicon area for current conduction is increased compared to a structure with stripes, allowing a further reduction of the overall on-resistance. In order to not only maintain but also further reduce the $FOM_g = R_{DS(on)} \times Q_g$ and $FOM_{gd} = R_{DS(on)} \times Q_{gd}$ values, the gate trench underwent a complete redesign to minimize its lateral extension.

2.2 Introduction of a metal gate for the trench power MOSFET

A drawback of the design measure to minimize the lateral extension of the gate trench is given by the dramatically reduced conduction area of the gate electrode itself. The use of a common polysilicon gate material results in an unacceptably large gate sheet resistance, linked to a clear increase of the internal gate resistance R_G. Large values for the gate resistance lead to a slowed-down switching behavior and increased switching losses, hence it is mandatory to avoid such an increase.

The introduction of gate fingers represents a common way to reduce the chip's internal gate resistance. The disadvantage of this measure is the reduction of the available active area due the space consumed. This results in an increase of the product on-resistance, especially in cases of smaller dies and the use of several gate fingers. Fig. 3 illustrates this correlation between gate resistance and active area loss for a best-in-class chip in an S3O8 package. The introduction of a metal gate system solves this problem, thanks to the much lower metal sheet resistance, as also indicated in Fig. 3.

Moreover, the use of a metal gate also enables a so-far unmatched switching uniformity over the die area. Simulations of the distributed local gate resistance impressively illustrate the much-improved gate resistance uniformity across the chip compared to the common use of polysilicon gates, see Fig. 4. Together with a direct connection of the field plates to the source metal, a device set-up is realized that not only ensures a very fast and homogeneous transition at turn-on and turn-off that minimizes switching losses, but also reduces the risk of an unwanted, dv/dt induced parasitic turn-on of the MOSFET.

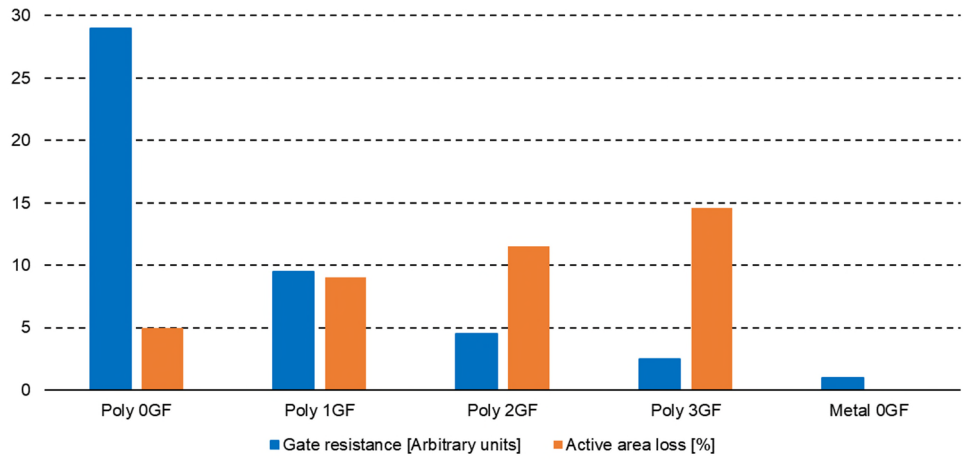

Fig. 3: Reduction of gate resistance depending on the number of gate fingers (GF) and active area loss for a best-in-class chip in an S3O8 package with the use of polysilicon and metal gate

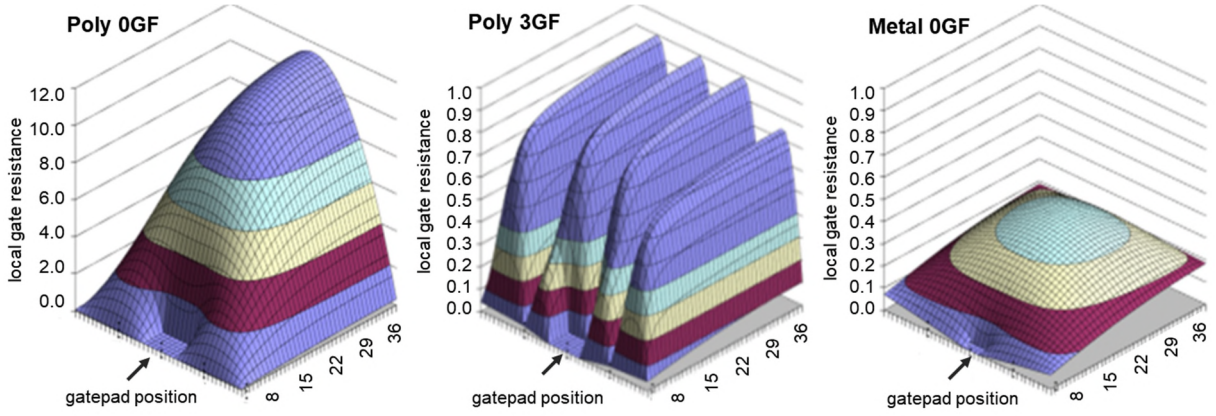

Fig. 4: Comparison of gate resistance uniformity for a best-in-class chip in an S3O8 package using different gate set-ups

3. Device properties

Fig. 5 summarizes the main device parameters of this technology with respect to its predecessor, indicating impressive improvements in all of the relevant parameters. The innovative gate trench engineering of the new device technology results in a remarkable reduction of both gate-source and gate-drain specific capacitances, which is reflected in the respective figures-of-merit FOM_g and FOM_{gd}.

These improvements are also clearly visible in the comparison of gate charge characteristics shown in Fig. 6. The devices have a comparable on-resistance $R_{DS(on)} \sim 3\ m\Omega$ in an SSO8 package. The Q_g reduction helps to achieve better efficiencies especially at light load conditions, due to the much reduced driving losses $P_{AUX} = Q_g \times V_{GS} \times f_{sw}$. This is of even higher importance for SMPS operated at high switching frequencies, as well as in applications where a larger number of MOSFETs are paralleled. In this case, the low gate charge also relaxes the requirements towards the gate driver's current capability. On the other hand, the low Q_{gd} enables fast switching transients, lowering the switching losses.

Fig. 7 compares the typical capacitance characteristics for both technologies. The output capacitance of the MOSFET is charged in every switching cycle. In hard-switched topologies, the energy that is stored in the output capacitance cannot be recovered and contributes significantly to the turn-on losses, as it is dissipated across the channel during the turn-on of the device. Losses associated with the output charge Q_{oss} are increasingly important at higher drain voltages, and scale linearly with the switching frequency. In general, in hard-switched SMPS operated at high switching frequencies, it is desirable to have a low value for the output charge in order to improve the efficiency. The previous technology generation was optimized with a strong focus on achieving an outstanding output charge figure-of-merit [8]. As can be concluded from Fig. 7, the new technology delivers only a minor improvement in this parameter, having opted instead for a compromise with the ease of use of the device. Besides, the clear reduction of the input and reverse transfer capacitance of the newly introduced technology reflect the improvements in the gate charge as just discussed.

The new cell design does influence the transfer characteristics that are important when the MOSFET operates in the linear region, e.g. when the MOSFET operates as a voltage controlled current source. This is a consequence of

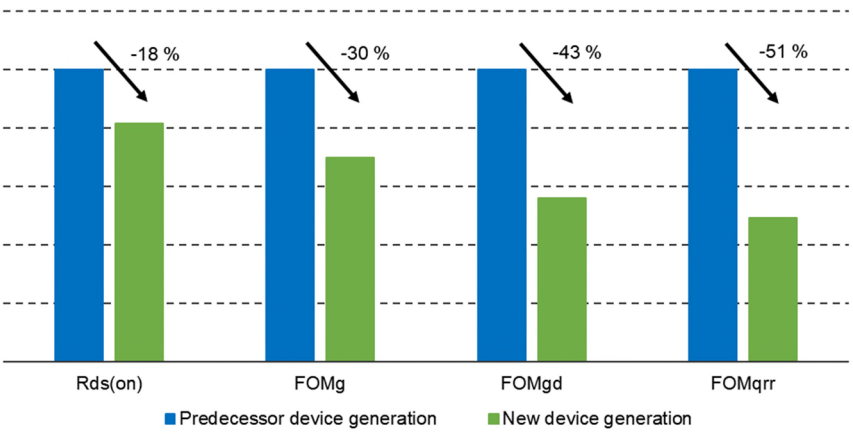

Fig. 5: Gained improvements in device performance for a best-in-class 100 V device in SSO8 package

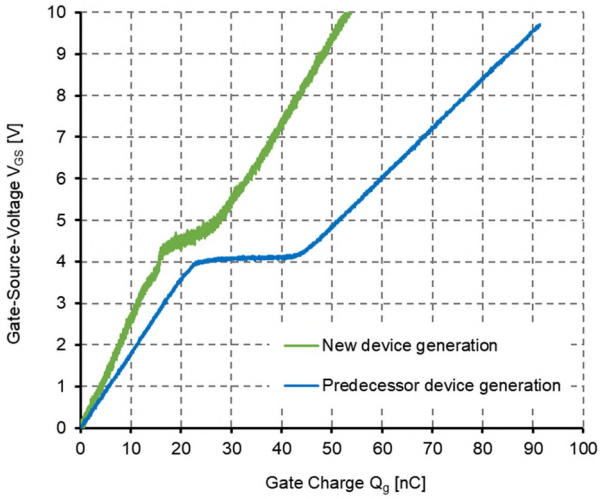

Fig. 6: Comparison of gate charge

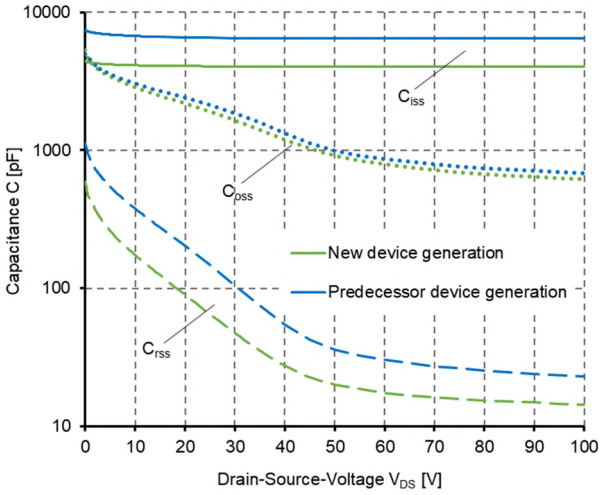

Fig. 7: Comparison of capacitance

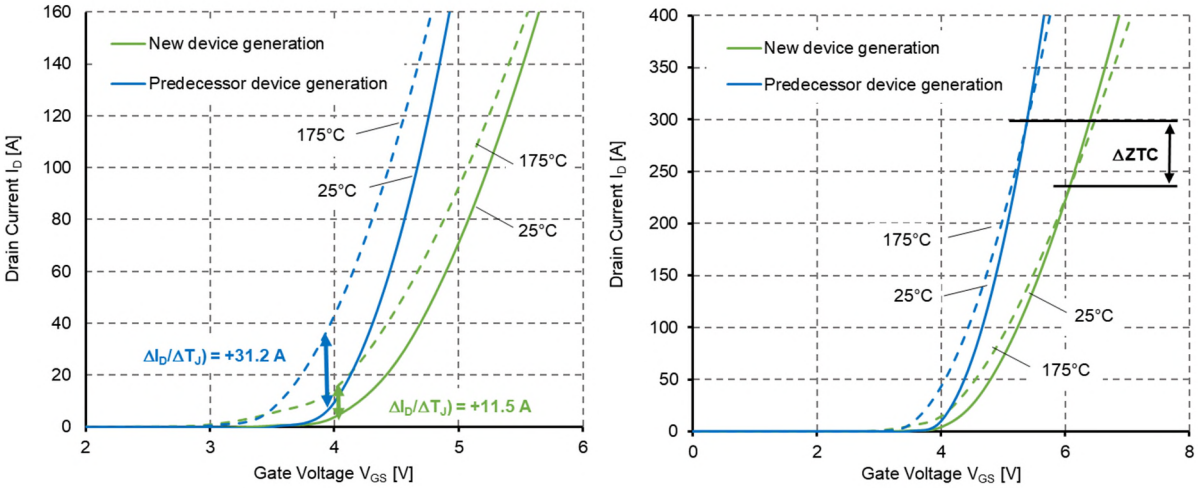

Fig. 8: Transfer characteristics of the new and predecessor technology for best-in-class devices in SSO8

the reduction in threshold voltage with rising temperature which is not completely compensated by a reducing bulk mobility, as current densities are still comparatively low [9]. The hottest part of the chip will draw more and more current, hence increasing again the temperature of the already hot spot (thermal runaway). At higher current densities, the effect of bulk mobility reduction starts to dominate the device behavior. At the zero-temperature-coefficient (ZTC) point, both effects balance out and the drain current is independent of temperature. Above the ZTC point, the drain current reduces with temperature and the device stabilizes itself.

Shifting the ZTC point to lower drain currents leaves the device less susceptible to thermal runway. Unfortunately, the strong increase of the channel density in low-voltage trench MOSFETs required to minimize on-resistance has shifted the ZTC point towards higher current densities, which has limited the device capabilities in linear mode operation. Fig. 8 compares the transfer characteristics of the new technology with the preceding one, revealing a more gradual turn-on behavior of the new device and consequently a move of the ZTC point towards lower currents. This means that the new technology comes with a lower transconductance in the linear region of operation, improving its robustness against thermal runaway. Along with an excellent thermal resistance from junction to case, the new device technology delivers a significant SOA improvement, as depicted in Fig 9. Such a behavior is very beneficial for applications besides SMPS, such as in hot-swap protection circuits, and widens the range of applications that this new technology generation is capable of addressing.

Hot swap is the procedure of replacing a faulty DC/DC converter by a good one, in a system that is up and running. This operation ought to be carried out without disturbing neighboring loads and without damaging the converter power connector contacts. The hot swap circuitry charges the new converter input capacitors with a charging current that has its peak value limited, avoiding big disturbances in the system bus voltage. MOSFETs employed in such applications must withstand the full system bus voltage and the bulk capacitors' charging current during its charging time: they need a wide SOA area in the region of the charging time pulse.

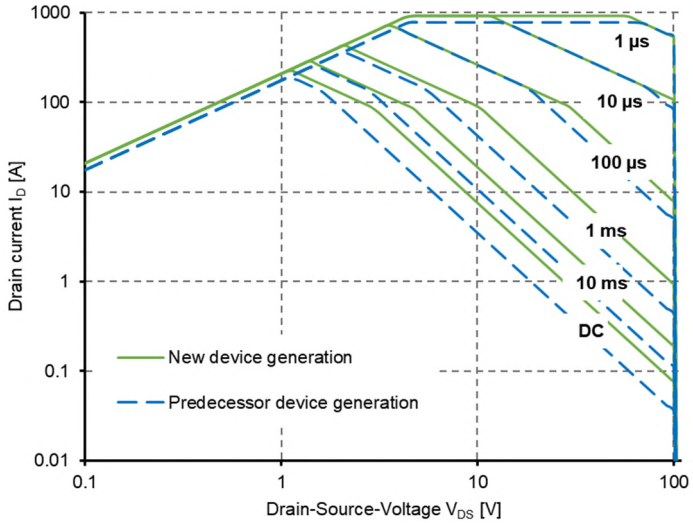

Fig. 9: SOA comparison of the introduced device technology with the predecessor device technology (best-in-class devices in SSO8 package)

4. Performance in target applications

4.1 Device operation in a DC/DC Intermediate Bus Converter for telecom applications

A telecom DC/DC converter serves as a test vehicle to compare the performance of the new-technology device with that of the predecessor technology. Such units are widely used in telecom and datacom power systems, typically as isolated DC/DC Intermediate Bus Converters (IBC) in the overall conversion chain with a nominal 48 V input and a 12 V output voltage bus for the downstream point-of-load converters [10]. The continuous improvement in MOSFET technology has allowed for a power density increase that enables the realization of the IBC in a standard quarter-brick form factor to typically deliver 600 W and more. Fig. 10 shows views of the realized board. For the measurement of the efficiency with the tested devices on the primary side, the test board developed employs a full-bridge topology on both the primary and secondary side, as depicted in Fig. 11. The full-bridge configuration on the secondary side is the topology of choice if the converter power increases, as the utilization of the transformer winding on the secondary side is better in this case. Although this configuration causes the use of two devices in series on the secondary side, the topology achieves a higher efficiency overall. This higher efficiency is also supported by the lower blocking voltage required of the MOSFET (due to the series connection), which is linked to a lower on-resistance. Typically, 40 V devices are used along with a full-bridge topology on the secondary side. To enable an assessment of the efficiency when the 100 V devices are used as synchronous rectifiers on the secondary side, a center-tapped topology needs to be used as shown in Fig. 12. This center-tapped configuration requires devices with a higher blocking voltage of 80 V … 100 V, and as such, it is the topology of choice in this part of the performance evaluation.

The board operates with a switching frequency of 250 kHz, the operating input voltage is allowed to vary between 36 V and 75 V. Due to the relatively large range of the allowed input voltage, voltage regulation is required [11].

Fig. 13 shows the comparison of the converter efficiencies achieved using the devices to be tested on the primary side with respect to the two technology generations. Here the synchronous rectifier on the secondary side is

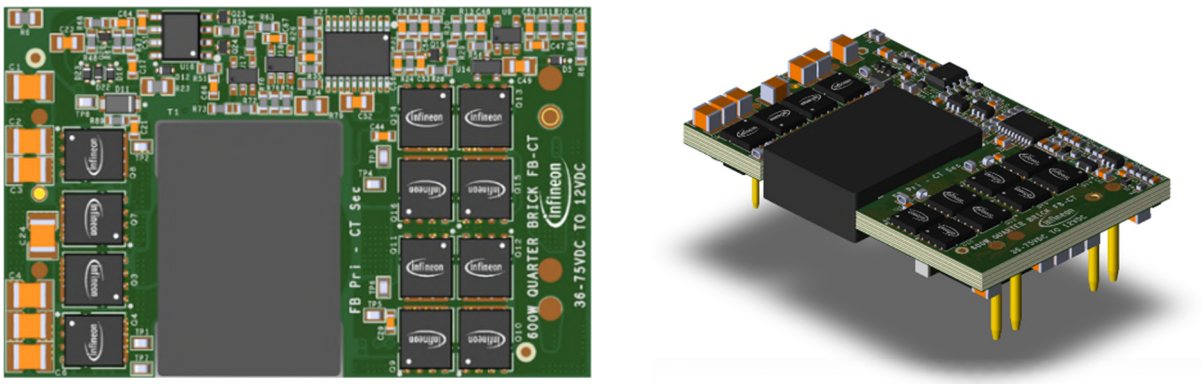

Fig. 10: Views of the 600 W isolated DC/DC IBC test board

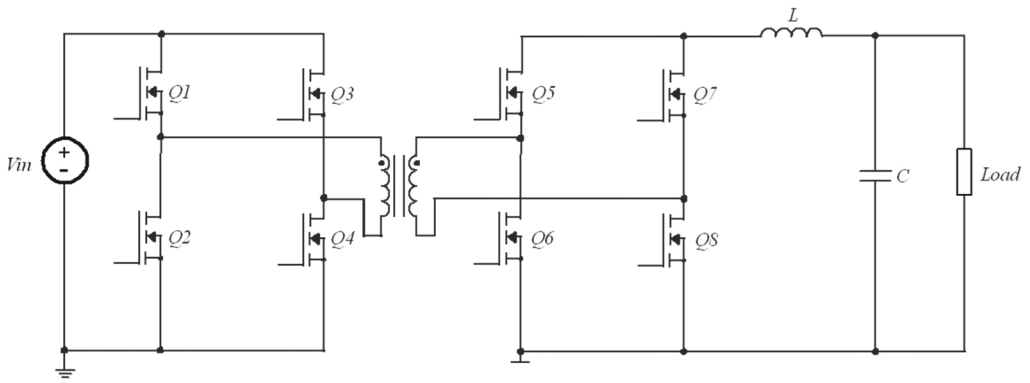

Fig. 11: Basic schematic of the 600 W isolated DC/DC IBC test board in FB-FB configuration

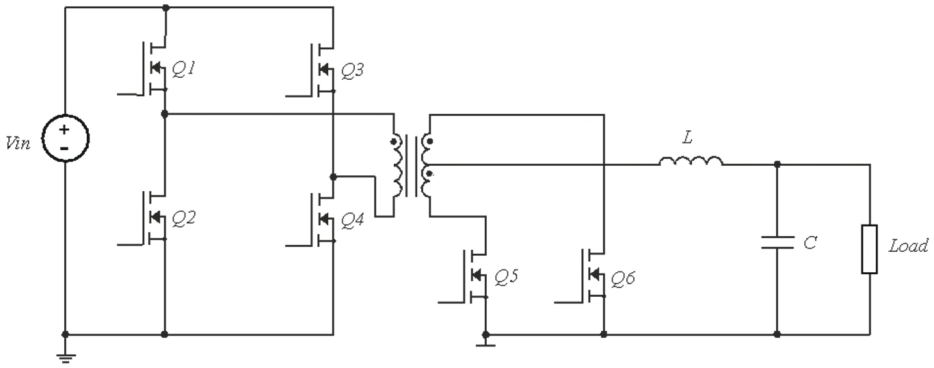

Fig. 12: Basic schematic of the 600 W isolated DC/DC IBC test board in FB-CT configuration

equipped with a fixed set of devices from the previous generation. The on-resistance of both devices was matched as closely as possible, using 6 mΩ devices of the new and 5 mΩ devices of the older technology. Compared to the predecessor solution, a valuable gain of up to 0.7 % is recorded at light-load conditions, which is a direct consequence of the improved switching performance of the new devices. The clearly reduced gate charge lowers the power consumption from the auxiliary bias supply, whereas the gate-drain charge which is less than half of the value of the predecessor technology enables ultra-fast switching, resulting in lowered turn-off losses. This high efficiency gain that is found at light load progressively reduces to a remarkable 0.2 % improvement at half load, where the IBC converter spends most of its operating time, and reaches 0.14 % at full load, despite the increased on-resistance. The reduction in the charges of the new generation device enables the improvements in efficiency even with the higher on-resistance. In the low load range, the reduction of the drain-to-source charge has more impact on the efficiency, whereas from half to full load the reduction of the gate-to-drain capacitance has a higher impact.

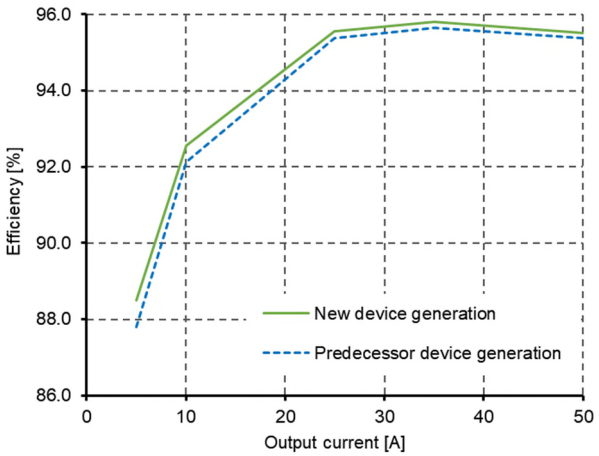

Fig. 13: Converter efficiency comparison of the devices tested in the primary side full-bridge stage of the IBC shown in Fig. 11

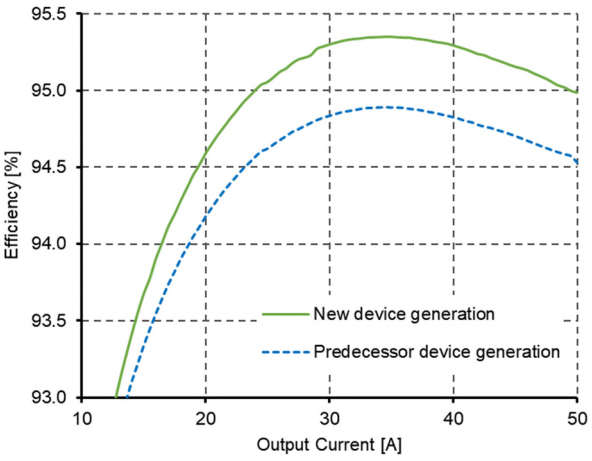

Fig. 14: Converter efficiency comparison of the devices tested on the secondary side synchronous rectifier stage of the IBC shown in Fig. 12

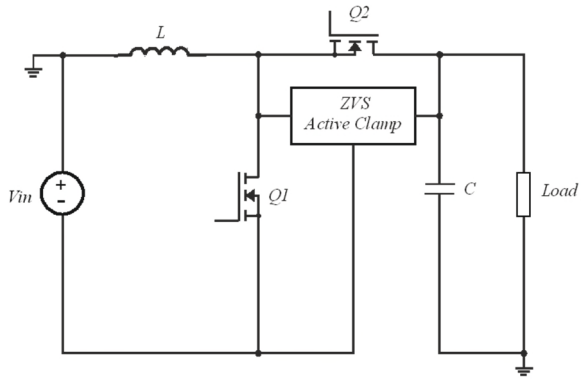

Fig. 15: Basic schematic of one phase of the inverting buck-boost DC/DC converter

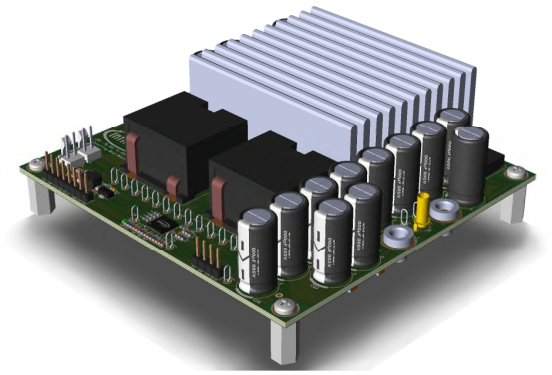

Fig. 16: 3D view of the realized evaluation board

For the efficiency investigation on the secondary side, the primary side was equipped with a fixed set of devices from the predecessor technology. Fig. 14 shows the measured efficiency values, again using devices of comparable on-resistance. Here, the efficiency improves by 0.46 % over the entire range from half to full load. This remarkable improvement is mainly attributed to the lower reverse-recovery charge and the lower gate charge. As can be seen in Fig. 2, the new device structure inherently offers a larger area for the current flow when compared to the predecessor device structure. As a consequence, the body diode current density reduces for the same current level in the application, and with it the reverse-recovery charge.

4.2 Device operation in an inverting buck-boost DC/DC ZVS converter for telecom applications

This example covers the efficiency of a telecom DC/DC converter based on a zero-voltage switching (ZVS) inverting buck-boost topology. Ordinary inverting buck-boost topologies find interest in telecom power systems as DC-DC converters that supply the RF power amplifiers (RFPAs). These amplifiers require the highest possible efficiencies for supply voltages ranging from +28 V (for use in LDMOS RFPAs) up to +50 V (for use in GaN RFPAs). The use of a novel active clamp auxiliary circuitry enables the transfer of the reverse recovery charge Q_{rr} from the Synchronous Rectifier MOSFET Q2 toward the output in a non-dissipative way, practically achieving ZVS turn-on for the control switch Q1. As such, the active clamp circuit effectively drives down the overall switching losses in the unit. This enables the use of best-in-class devices with lowest on-resistance, supporting a dramatic increase in the power density [12].

The evaluation board used in this investigation has been adapted to use an output voltage of only 12 V instead of the usually required 28 V, which is suitable for telecom equipment other than RFPA that does not require functional isolation. This configuration enables the use of MOSFETs with a blocking voltage of 100 V, which makes it an excellent platform to study the performance of the discussed devices in a soft-switching topology. The board, based on an interleaved (two-phase) inverting buck-boost, can deliver up to 600 W from an input voltage range of -36 V... -60 V. The basic schematic for one phase of the topology is given in Fig. 15, while the realized demonstrator board is shown in Fig. 16.

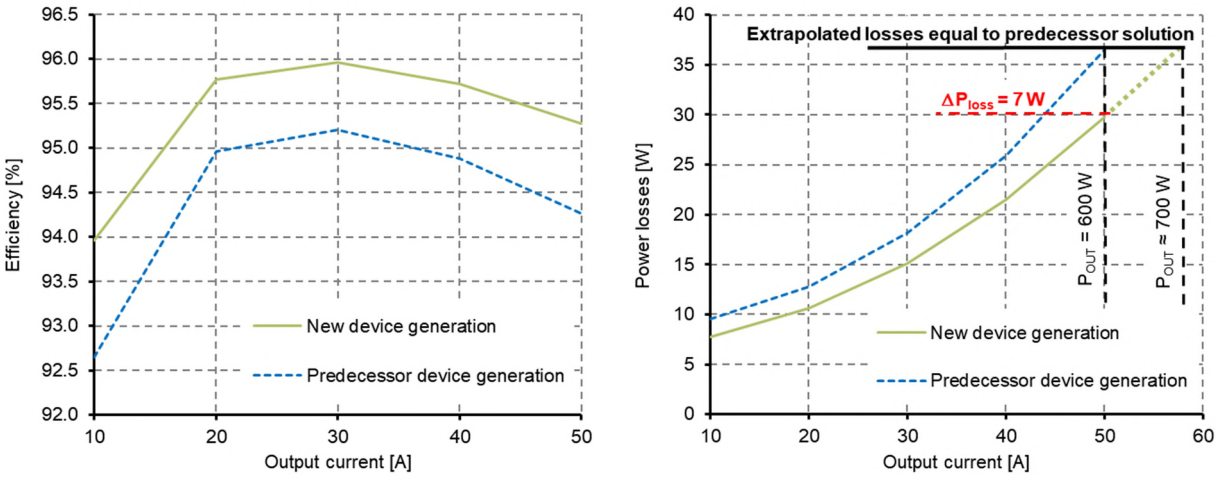

Fig. 17: Efficiency and extrapolated losses for the 600 W ZVS Inverting Buck-Boost Evaluation Board (V_{IN} = -48 V, V_{OUT} = 12 V, f_{sw} = 200 kHz)

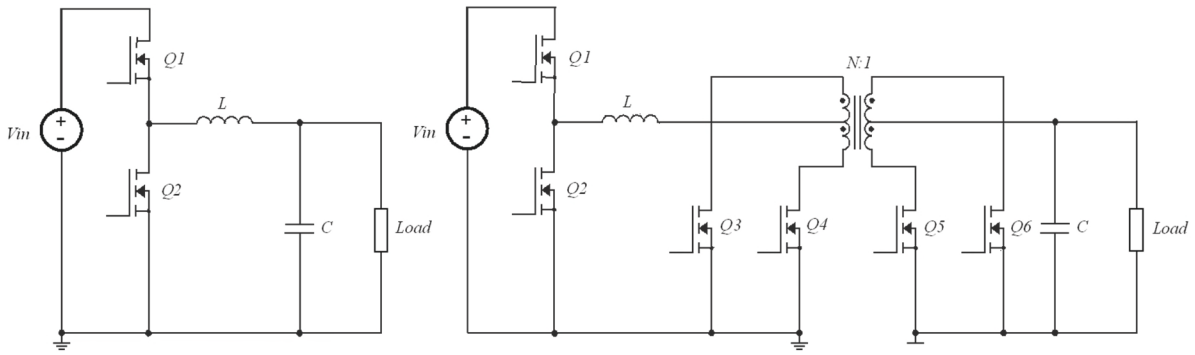

Fig. 18: Basic schematic of the buck converter (left) and the buck current-fed push-pull cascaded converter (right)

Fig. 17 shows the measured efficiencies for the new and predecessor device technology. The results clearly illustrate the huge impact of the effort invested in the device and technology development with an impressive efficiency gain of ~ 1 %. The higher efficiency results in lower losses of 7 W, which enables a power density increase of up to 15 % (see Fig. 17). This reduction in losses is mainly achieved due to the reductions in the on-resistance, the gate charge and the reverse-recovery charge that is transferred to the output by the active ZVS clamp circuit.

4.3 Device operation in a buck converter

The second application example examines the efficiency of operating the devices in a buck converter. This topology, among others, is often used as a front-end stage of current-fed cascaded push-pull converters (see Fig. 18). However, only the buck stage is covered in this investigation. The converter is operated at a switching frequency of 300 kHz, with a 60 V input, a 26 V output voltage, and an output power equal to 450 W. The selected input voltage represents the high voltage level in a 48 V telecom system and the output voltage is the same as the one used as the input for the push-pull stage in the cascaded converter. Devices realized in the new technology are compared with devices based on the previous technology. All devices have identical on-resistance and employ the chip layout without gate fingers; see also Fig. 4 (new technology: Metal 0 GF; previous technology: Poly 0 GF). Fig. 19 gives views of the board design.

Fig. 20 shows a comparison of the drain-source voltages for the devices of the two technologies at turn-off: the new generation device shows a clean drain-source voltage waveform, whereas the device from the previous generation shows a kink in the drain-source voltage at a value of about 15 V. This kink is related to the high dv/dt of the drain-source voltage, which induces a displacement current into the gate through the gate-drain capacitance C_{gd}. As a consequence the MOSFET turns-on despite the external gate driver circuit trying to pull-down the gate of the device. Such a parasitic turn-on occurs for the predecessor technology device, although both MOSFETs come with a similar value of internal gate resistance. The reason is the much less homogeneous distribution of the internal gate resistance. As can be seen from Fig. 4, the effective gate resistance in the region opposite to the gate pad is several times larger than for the area close to the gate pad. Due to this locally increased gate resistance, this part of the MOSFET chip is prone to suffering from an induced turn-on. Further comparing the drain-source voltage waveforms for the two devices it can be seen that the new technology device shows less damping of the

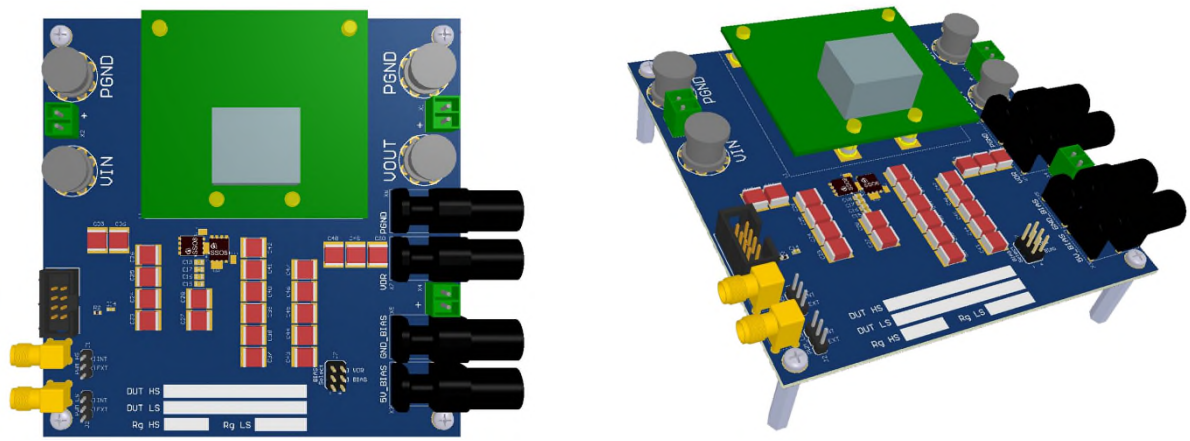

Fig. 19: Views of the buck converter test board

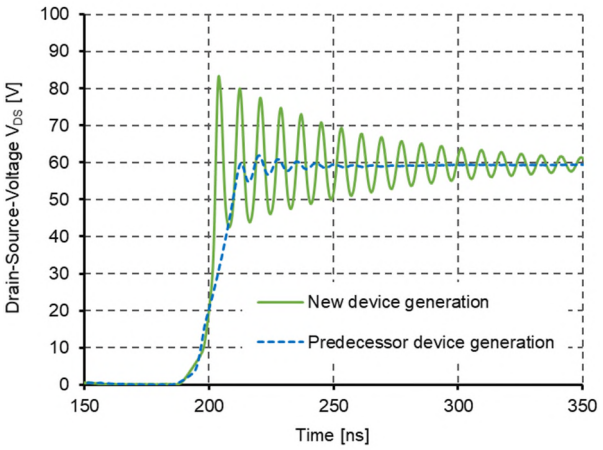

Fig. 20: Comparison of the drain-source-voltages for the two device generations in the buck converter

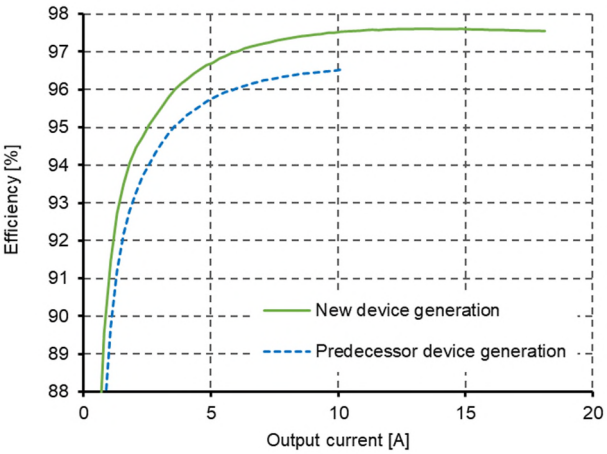

Fig. 21: Comparison of the efficiency for devices of both technologies in the buck converter

ringing. This effect is due to the low equivalent resistance of the field-plate for the new technology, a consequence of the high density of trenches per area.

In order to enable a valid efficiency comparison, avalanche on the low-side MOSFET needs to be avoided during the buck converter operation. Therefore, the high-side MOSFET needs to be slowed-down to limit the dv/dt over the low-side device, which required the use of a four times larger value for the external gate resistor for the previous technology device compared to the new technology generation.

Fig. 21 compares the achieved efficiencies for the two device generations. The device of the new technology delivers the full power providing a high efficiency, whereas the predecessor device can only deliver half of the required power. The experimental results show that gate fingers ought to be used in the previous-technology device chip layout in order to reduce the peak value of the internal gate resistance to acceptable values and avoid the MOSFET induced turn on. However, the insertion of such gate fingers in the MOSFET chip consumes chip area that would otherwise be used for current conduction and, therefore, a bigger chip ought to be used for the same MOSFET channel on-resistance, which increases the device cost. On the other hand, the use of a metal gate within the introduced new technology, with its more homogeneous distribution of internal gate resistance, provides a good immunity against parasitic induced turn-on without the need for gate fingers.

5. Conclusion

The new power MOSFET technology introduced in this work shows improvements in all important device parameters and combines the benefits of low on-state resistance with a superior switching performance. The new technology is specifically optimized for high switching frequency applications such as telecom SMPS and solar.

The remarkable jump in the overall device performance is enabled by substantial improvements at the device technology level. This has culminated in a unique device structure, which is the first to employ a three-dimensional charge compensation combined with the first-time use of a metal gate in a trench power MOSFET.

The reduction achieved in the on-resistance, the dramatically-lowered gate charge and gate-drain charge, together with the low output charge and improved switching homogeneity across the device area, enhance the system efficiency in the application across all load conditions. Additionally, the new technology offers an optimized transfer characteristic with a low temperature coefficient. This feature enables a safe operating area (SOA) that is significantly enhanced with respect to the predecessor technology, leaving this latest trench power MOSFET technology also as an ideal candidate for battery disconnect switches in battery-powered applications, battery management systems, and further enabling its use with motor drives.

The new device structure is also beneficial for the internal body diode of the MOSFET. While the silicon area conducting current is increased, the body diode current density is decreased which, for the same current level, decreases the reverse recovery charge.

Efficiency measurements in targeted SMPS applications confirm the findings at the semiconductor device level and yield efficiency improvements of up to 1 %, depending on the topology and load condition. These improvements provide a significant margin to meet the demanding requirements of the telecom power arena and other application fields.

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