

# **Experimental Evaluation of Battery Impedance and Submodule Loss Distribution for Battery Integrated Modular Multilevel Converters**

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## **Abstract**

Greenhouse gas emissions and the increase in average global temperature are growing concerns now more so than ever. Therefore it is of importance to increase the use of alternative energy sources, especially in the automotive industry. Battery electric vehicles (BEV) have gained popularity over the past several years. However, the performance of a BEV is limited by the battery pack, in particular, the weakest cell in the pack. Therefore, improved cell controllability and high efficiency are seen as important directions for research and development and one direction where it can be achieved is through using battery-integrated modular multilevel converters (BI-MMC). The battery current in BI-MMCs contains additional harmonics and the frequency dependent losses of these harmonics are determined by the resonance between the battery and the DC-link capacitor bank. The paper presents an experimental validation of previously published theoretical results for both harmonic allocations and loss distribution at the switching frequency within the BI-MMC submodule. Furthermore, a methodology for measuring the battery impedance using the full-load converter switching currents is presented.

## **Keywords**

«Modular Multilevel Converters (MMC)», «Power converters for EV», «Batteries», «DC-AC converters», «Automotive application».

## **Introduction**

The average global temperature has risen considerably due to greenhouse gas emissions and the automotive sector is responsible for about 15% of the greenhouse gas emissions [1, 2]. Therefore, it is of importance to increase the utilization of alternative energy carriers, that can replace fossil fuels, especially in this aforementioned automotive applications. Automotive battery packs are generally made up of several modules where each module consists of a number of parallel and/or series connected cells [3]. Differences in leakage currents and cell inhomogeneities cause individual cell voltage and state-of-charge (SOC) distribution among the cells to become non-homogeneous [4]. Therefore, the available energy and power is determined not only by the cell type and size, but to a large extent also by the configuration and battery management system (BMS) [5, 6]. By restructuring the cell interconnections and introducing more electronics in the pack, more precise control and better utilization of the energy in the individual modules can increase the available energy and provide additional benefits such as improved battery life and increased usable capacity of the battery pack [7, 8].

Modular multilevel converters (MMC), have proven to be highly reliable in power grids with HVDC system because of their modularity and improved EMC [9, 10]. Over the past several years, battery-integrated modular multilevel converters (BI-MMC) have gained popularity for EV powertrains because

of their added benefits such as high efficiency, greater cell-level control, and better fault isolation capabilities [11, 12]. Several pieces of research also indicate that there is a great benefit in terms of battery life-time and battery utilization by increasing the controllability of the cells [13, 14]. Some articles also suggested that pulsed current charging improves the lifetime of Li-ion batteries [15, 16]. Furthermore, [17] reported that pulsed charging ( $\approx 2$  kHz pulse current) significantly improved the battery life-time when compared to a constant current charging. These articles suggests that frequency of the battery current is an important factor that influences the battery lifetime. The battery current in BI-MMCs are inherently pulsating thus resulting in higher battery losses than a 2-level inverter [18–20].

This paper extends the results in [21] where the potential benefit of introducing MMCs into hybrid and electric vehicles was presented clarifying the advantages and disadvantages of different MMC topologies for a 400 kW 40 ton commercial vehicle. Furthermore, [21] presented the principle optimization of the submodule DC-link capacitor and MOSFET switching frequency, minimizing the total power losses. It was found that the the resonance between the battery and the DC-link capacitors determined the allocation of harmonics and in its turn the loss distribution between the battery and the DC-link capacitors. The article also showed that a crucial parameter was the battery impedance. Electrochemical impedance spectroscopy (EIS) is a method used to characterize the properties of electrochemical devices like batteries and capacitors. The EIS signature is often determined using low-amplitude perturbations [22, 23]. However, the EIS and impedance characterizations using pulse tests are not identical [24, 25].

The first contribution in this paper is a methodology to characterize the battery impedance utilizing the full load converter switching currents (switched pulse-test). The second contribution is the experimental validation of the DC-current harmonics allocation and the loss distribution at the switching frequency between the battery and DC-link capacitors on a single-phase half-bridge converter.

## Topology overview

A BI-MMC topology consists of either one or two arms per phase and each arm is made up of a number of cascaded stages of DC/AC converters that are commonly referred to as submodules (SM). Fig. 1, presents the schematics of 3-phase single-star half-bridge (SSHB) (Fig. 1(a)) and single-star full-bridge (SSFB) (Fig. 1(b)) topologies with  $N_{s(cells)}$  series and  $N_{p(cells)}$  parallel cells per SM. Each SM consists of  $N_{p(mos)}$  parallel MOSFETs and a DC-link capacitor bank consisting of  $N_{p(cap)}$  parallel capacitors, here represented by its ideal capacitance  $C$ , ESR, and ESL. Fig. 1(a) and Fig. 1(b) also show the half-bridge (HB) and full-bridge (FB) submodules, respectively. A single HB-SM connected to an RL load is used for experimental validations and is referred to as an HB-converter.

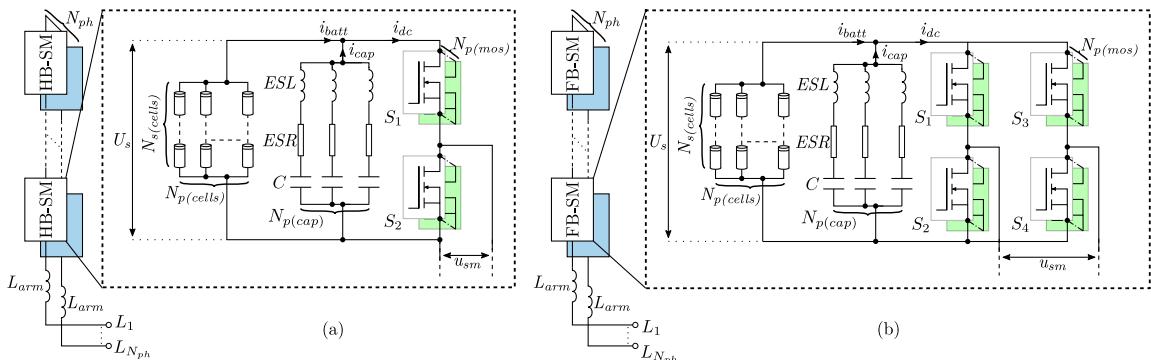


Fig. 1: Battery-integrated modular multilevel inverter topologies. (a) single-star half-bridge and (b) single-star full-bridge topologies.

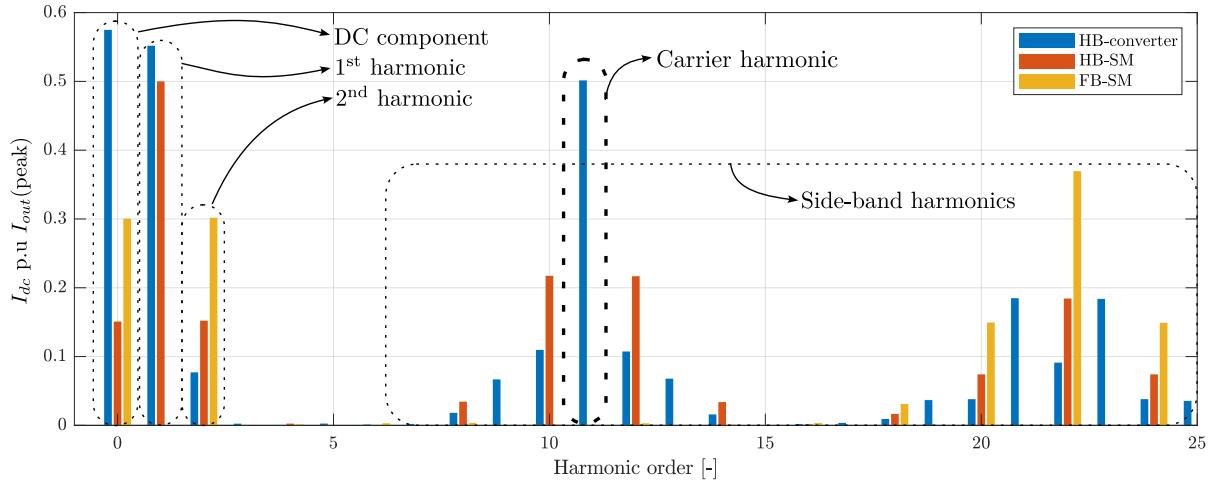


Fig. 2: The DC-side currents per unit output current for HB and FB submodules, and HB-converter considering a sinusoidal carrier based modulation scheme with  $f_{sw} = 11 f_1$  with a modulation index of 0.6 and  $\cos\phi = 0.9$ .

### Submodule DC-current

The instantaneous DC-side SM current ( $i_{dc}(t)$ ) is calculated as follows:

$$i_{dc}(t) = S_{conv}(t) i_{arm}(t), \quad i_{dc(HBc)}(t) = S_{conv}(t) i_{out}(t), \quad (1)$$

where,  $i_{arm}(t)$  represents the instantaneous arm current of the BI-MMC,  $S_{conv}(t)$  is the converter/SM switching function,  $i_{dc(HBc)}$  is the DC-side current of the HB-converter, and  $i_{out}$  is the output current of the HB-converter. In order to capture the high frequency characteristics of the battery, a sinusoidal carrier based modulation is selected. Fig. 2 shows the DC-side currents for the HB and FB SMs, and the HB-converter with a switching frequency,  $f_{sw} = 11 f_1$  (where  $f_1$  is the fundamental frequency) considering a modulation index of 0.6 and power factor of 0.9. The modulation index and power factor values correspond to those used in the battery impedance characterization and the validation of the distribution of harmonics between the battery and the DC-link capacitor bank. From the figure it is clear that the DC-side currents for the HB-SM contains DC, 1<sup>st</sup>, 2<sup>nd</sup>, and all the side-band harmonic components. However, the DC-side currents for the FB-SM consists of DC, 2<sup>nd</sup>, and only the even carrier multiples as the side-band harmonic components. However, the HB-converter DC-side current contains not only DC, 1<sup>st</sup>, 2<sup>nd</sup>, and side-band harmonics but also the carrier harmonic, i.e, the switching frequency component. The battery current and voltage components at the switching frequency are used to characterize the battery impedance through a set of measurements by varying the switching frequency.

### Loss-distribution

The principle distribution of harmonics and losses between the DC-link capacitor bank and the battery is presented in this section.

[21] presented a detailed calculation of the battery and the DC-link capacitor currents, and losses. Two key parameters pointed out in [21] that determine the loss distribution between the battery and the DC-link capacitor bank are the capacitor energy rating and the converter switching frequency. There exists a resonance, at the frequency  $f_{res}$ , between the battery and the DC-link capacitor given by the following:

$$f_{res} = \frac{1}{2\pi \sqrt{L_{dc} C_{cap}}}, \quad L_{dc} = L_s + L_p, \quad (2)$$

where  $L_{dc}$  is the total DC-side inductance,  $L_s$  is the inductance of the battery cell,  $L_p$  is the total parasitic inductance of the cables connecting the battery and the converter, and  $C_{cap}$  is the capacitance of the DC-

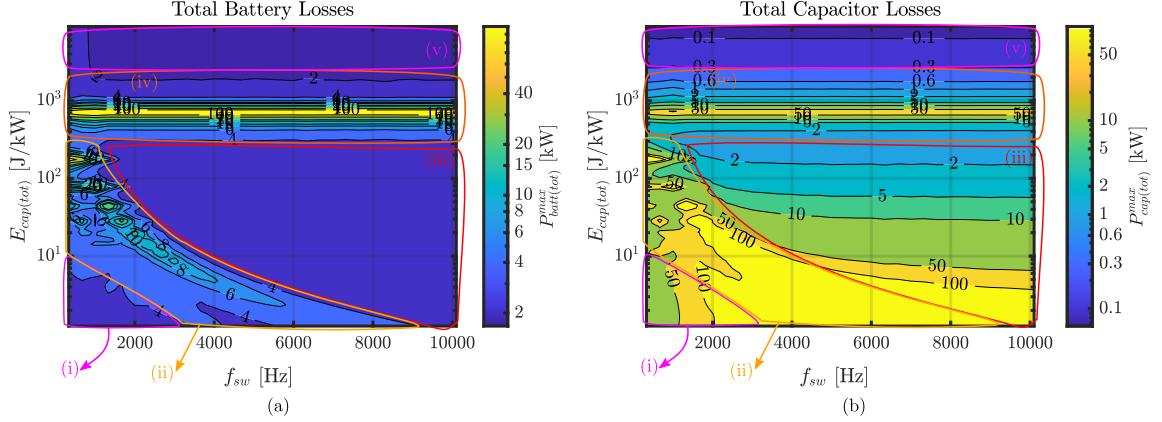


Fig. 3: Power losses as a function of the normalized total energy stored in the capacitors ( $E_{cap(tot)}$ ), and MOSFET switching frequency ( $f_{sw}$ ) for 3-phase  $1-N_{s(cells)}$  SSFB BI-MMC topology at rated power ( $P_{tot}^{max}$ ) of 400 kW. (a) total battery losses ( $P_{batt(tot)}^{max}$ ) and (b) total capacitor losses ( $P_{cap(tot)}^{max}$ ).

link capacitor bank.  $f_{res}$  defines the allocation of harmonics between the battery and the DC-link capacitor bank. An example of a 3-phase SSFB topology with 1 series battery cell per converter sub-module is presented to illustrate these principles. Fig. 3 shows the calculated total battery losses ( $P_{batt(tot)}^{max}$ ) and capacitor losses ( $P_{cap(tot)}^{max}$ ) as a function of total energy stored in the DC-link capacitor bank normalized to 1 C discharge power of the battery ( $E_{cap(tot)}$ ), and MOSFET switching frequency ( $f_{sw}$ ) for the converter operating at rated power of 400 kW. The loss distribution can be divided into five regions as shown in the figure. In region (i),  $f_{sw} < f_{res}$ , as a result, the switching harmonic components of  $I_{dc}$  flows through the battery, therefore  $P_{batt(tot)}^{max}$  is high. In region (ii),  $f_{sw} \approx f_{res}$ , i.e., a parallel resonance resulting in low impedance in the loop between  $L_{dc}$  and  $C_{cap}$  resulting in high circulating currents increases the total losses. In region (iii),  $f_{sw} > f_{res}$  and the battery current only consists of the DC-component and the 2<sup>nd</sup> harmonic (1<sup>st</sup> harmonic also for HB-SM). As a result, the battery losses are low. Although the capacitor current consists of all the switching frequency components, ESR is low due to large capacitor energy rating, thus resulting in lower capacitor losses. A detailed description of regions (iv) and (v) is presented in [21].

## Experimental determination of battery and DC-link capacitor bank impedances

This section describes in detail the battery and DC-link capacitor bank impedance characterization procedure and results. Furthermore, the experimental validation of the principle harmonic allocation and the loss distribution between the battery and the DC-link capacitor bank are presented.

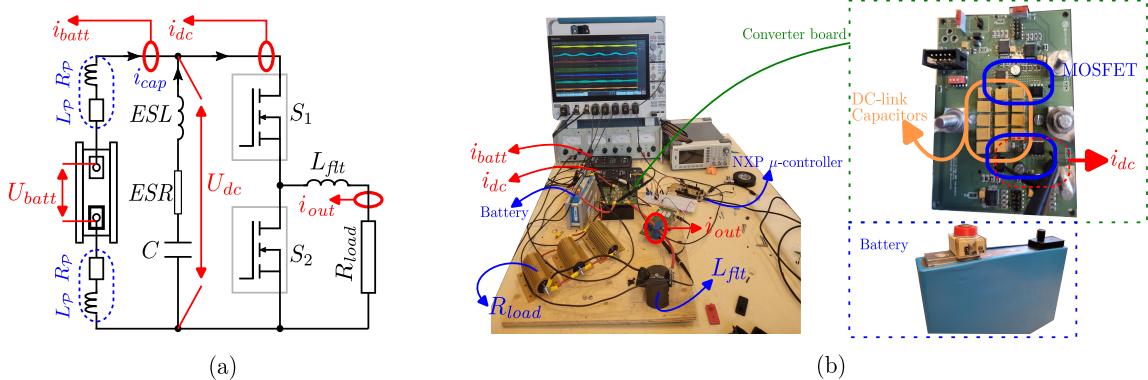


Fig. 4: Battery and DC-link capacitor impedance measurement setup.

## Experimental setup

Fig. 4 presents the experimental setup developed and used to determine both the battery and the DC-link capacitor impedances. Fig. 4(a) shows the schematic of the experimental setup to characterize the battery and the DC-link capacitor bank impedances. In the figure,  $i_{batt}$ ,  $i_{dc}$ , and  $i_{out}$  are the battery, DC, and output currents measurements, respectively.  $i_{cap}$  is the calculated capacitor current (in blue). In order to minimize the drain-source voltage step corresponding to the rate of change of drain current (i.e. minimize ESL in Fig. 4(a)), the trace lengths between the DC-link capacitors and the MOSFETs are short. As a result,  $i_{cap}$  cannot be measured using neither the Rogowski transducers nor the LEM transducers.  $U_{batt}$  is the battery voltage measurement and  $U_{dc}$  is the the DC-link capacitor voltage measurement,  $L_{flt}$  is the output filter,  $R_{load}$  is the output load resistor,  $L_P$  and  $R_P$  are the parasitic inductance and resistance of the cables connecting the battery and the converter board, respectively. In order to accurately determine  $i_{cap}$ ,  $i_{batt}$  and  $i_{dc}$  are measured using the same type of current sensor. This is done to ensure that both current transducers have identical phase and magnitude.  $i_{dc}$  and  $i_{batt}$  are measured using T3RC0300-UM Rogowski current waveform transducers [26]. With the use of Rogowski transducers, the DC current measurement is sacrificed. However, a more accurate measurement of the switching currents is achieved. This is an advantage when characterizing the high frequency battery impedance.  $i_{out}$  was measured using HAIS 100-P LEM current transducer and the voltage measurements were measured using TPP0500B passive voltage probes with a bandwidth of 500 MHz [27, 28].  $U_{batt}$  measurement is the calculated differential voltage using two passive probes. The measurements were recorded using a Tektronix MSO58, 500 MHz oscilloscope [29]. Fig. 4(b) shows the experimental setup. The figure also shows the Samsung 24 Ah Li-ion NMC battery cell connected to a converter board with 14 parallel units of 1 mF, 6.3 V TPSV108M006V0050 AVX Tantalum capacitors [30]. These capacitor units each have an internal resistance (ESR) of 50 mΩ and a maximum current ripple of 2.2 A RMS at 25 °C and 100 kHz. The total energy stored in the DC-link capacitor bank on the converter board normalized to 1 C discharge power of the battery is about 1.2 J kW<sup>-1</sup>. The converter board is a FB inverter with 4 SQJQ142E Vishay MOSFETs. The converter board is operated as an HB-converter and connected to three parallel load resistors of 100 mΩ each ( $R_{load}$ ) and a filter inductor ( $L_{flt}$ ) of 48 μH.

The battery discharge rate was set to 1 C and the half bridge converter with a sinusoidal carrier based modulation scheme is utilized to determine the impedances.  $i_{dc}$  contains the DC, 1<sup>st</sup>, 2<sup>nd</sup>, side-band, and carrier harmonics, and  $i_{batt}$  and  $i_{cap}$  harmonics depend on the battery, DC-link capacitor bank and cable-parasitic impedances. The current and voltage at the carrier harmonic (i.e. switching frequency component) is used to determine the impedances. By varying  $f_{sw}$ , the switching frequency component (or carrier harmonic) is varied and  $i_{batt}$ ,  $U_{batt}$ ,  $i_{dc}$ , and  $U_{dc}$  are measured for every  $f_{sw}$ . An impedance spectra is thus obtained. Only the switching frequency components (or carrier harmonics) are used to determine the battery impedance because the amplitude of this component is approximately equal to the 1<sup>st</sup> harmonic component. The side-band harmonics are not utilized to determine the battery impedance because the amplitude of these harmonics are significantly lower. The fundamental frequency of the output voltage and current is 50 Hz, thus the 1<sup>st</sup> and 2<sup>nd</sup> harmonic components, although high in amplitude, are close to the lower bandwidth of the current transducers, thus also not used to determine the impedances.

The battery, DC link capacitor bank, and the parasitic impedances are determined using the following relation:

$$\begin{aligned} Z_{batt}(\omega_{sw}) &= \frac{U_{batt}(\omega_{sw})}{I_{batt}(\omega_{sw})}, & Z_{cap}(\omega_{sw}) &= \frac{U_{dc}(\omega_{sw})}{I_{cap}(\omega_{sw})}, \\ Z_{dc}(\omega_{sw}) &= \frac{U_{dc}(\omega_{sw})}{I_{batt}(\omega_{sw})}, & Z_P(\omega_{sw}) &= Z_{dc}(\omega_{sw}) - Z_{batt}(\omega_{sw}), \end{aligned} \quad (3)$$

where  $Z_{batt}$  and  $Z_{cap}$  are the battery and the DC-link capacitor bank complex impedances, respectively,  $U_{batt}$  and  $U_{dc}$  are the measured complex battery and DC-link capacitor bank voltages, respectively.  $I_{batt}$  is the measured complex battery current,  $I_{cap}$  is the calculated complex capacitor current, and  $\omega_{sw}$  is the angular switching frequency ( $\omega_{sw} = 2\pi f_{sw}$ ).  $Z_{dc}$  is the total DC-side impedance and  $Z_P$  is the parasitic impedance of the cables connecting the converter board and the battery. It is important to mention that

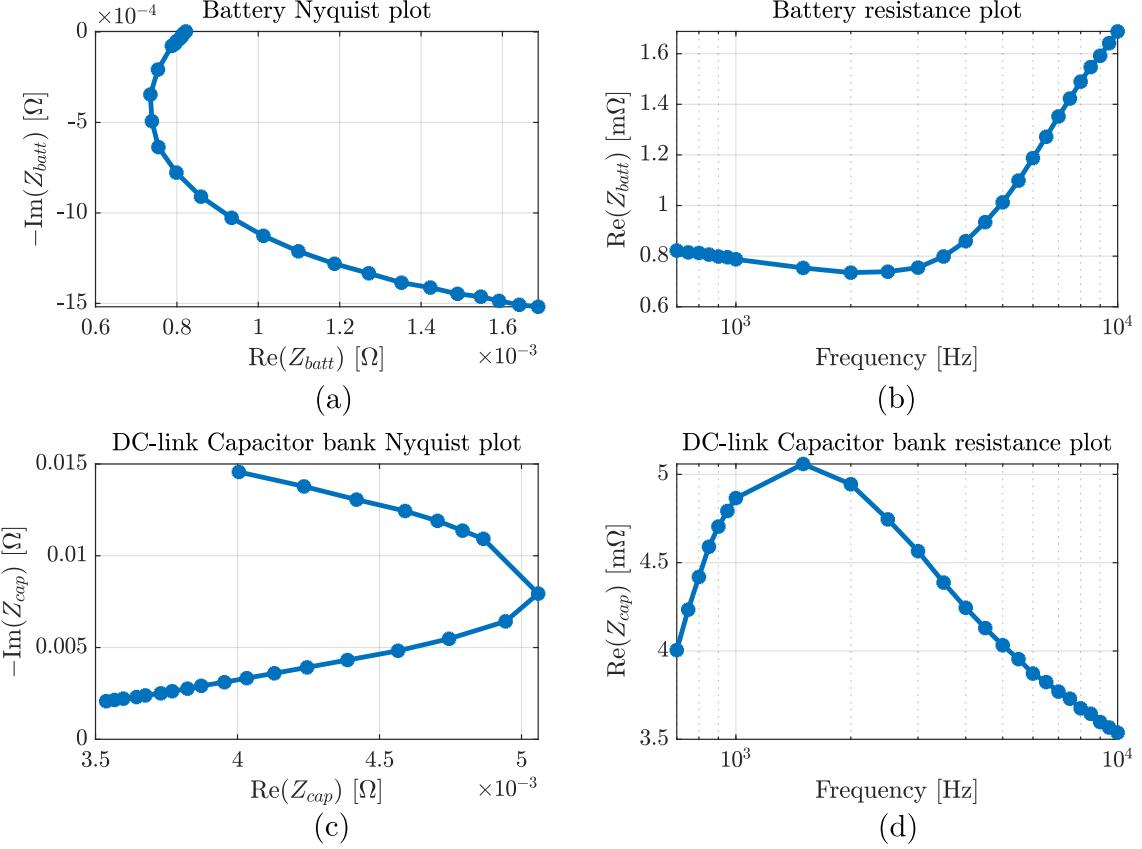


Fig. 5: Experimentally determined battery and DC-link capacitor bank impedances. (a) battery impedance Nyquist plot and (b) resistance plot, and (c) Nyquist plot of the DC-link capacitor bank impedance and (d) resistance plot.

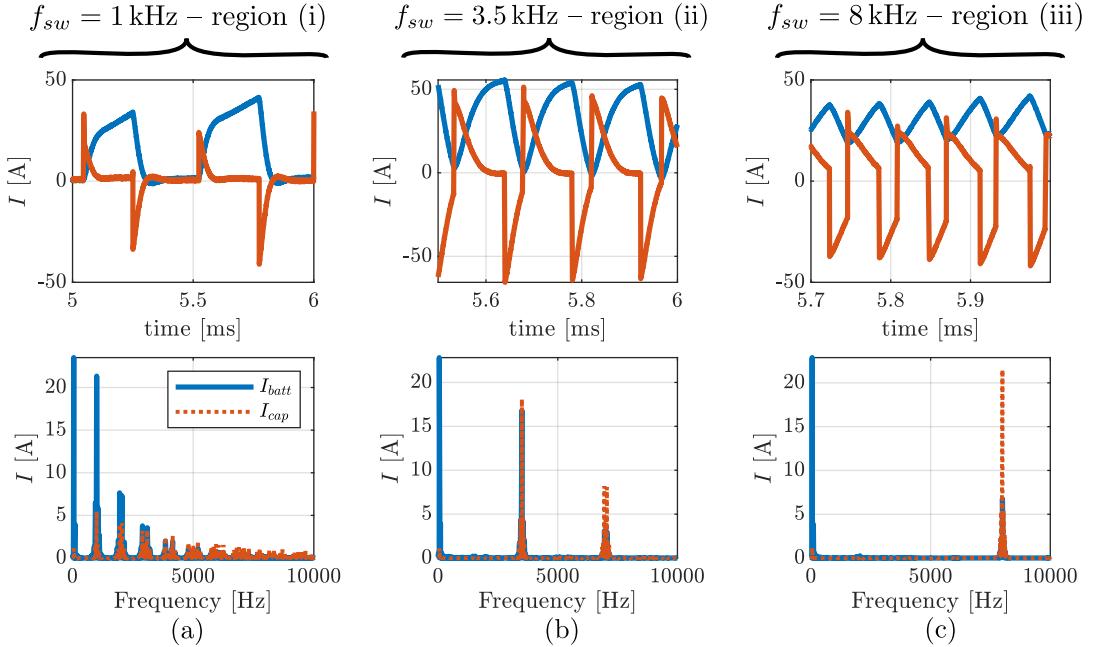


Fig. 6: Measured battery and capacitor currents different converter switching frequencies ( $f_{sw}$ ). (a) Battery and capacitor current time plot and frequency spectra with  $f_{sw} = 1$  kHz, in region (i), (b)  $f_{sw} = 3.5$  kHz, in region (ii), and (c)  $f_{sw} = 8$  kHz, in region (iii).

the battery state of charge during the measurement period is fairly constant. This is because during the measurement interval, the battery was discharged with 24 A for only a few seconds.

The HB-converter switching frequency was varied from 700 Hz to 10 kHz and  $Z_{batt}$ ,  $Z_{cap}$ , and  $Z_{dc}$  were determined at these frequencies. The recording time for each frequency was about 100 ms with a sample rate of 12.25 MS/s. Fig. 5 presents the battery and the DC-link capacitor bank impedances for different  $f_{sw}$ . Fig. 5(a) presents the battery impedance Nyquist plot and Fig. 5(b) shows the resistance plot. Fig. 5(c) and Fig. 5(d) shows the DC-link capacitor bank Nyquist and resistance plots, respectively.

### Loss Distribution

Fig. 6 shows the measured battery and capacitor current, time and frequency domain plots at three different switching frequencies illustrating the three different regions of harmonic allocations. In the figure,  $I_{batt}$  is the measured battery current and  $I_{cap}$  is the calculated DC-link capacitor bank current. Fig. 6(a) presents the HB-converter operating in region (i) (see Fig. 3) and it is clear that  $I_{batt}$  contains majority of the switching frequency components. Fig. 6(b) presents the HB-converter operating in region (ii) and it is clear that the magnitude of  $I_{batt}$  and  $I_{cap}$  components at  $f_{sw}$  are similar, indicating a resonance between the DC-link capacitor bank and the battery. Fig. 6(c) presents the HB-converter operating in region (iii) and it is clear that  $I_{cap}$  contains the majority of the switching frequency components. In all the three cases presented in the figure, it is clear that the resonance defines not only the allocation of the switching frequency component but also all the side bands and the low-frequency harmonic components. Therefore, it is sufficient to concentrate on the switching frequency component to illustrate the distribution of losses between the battery and the DC-link capacitor bank.

Fig. 7 shows the loss distribution between the battery and the DC-link capacitors at different  $f_{sw}$ . The figure shows the total DC-side impedance ( $Z_{dc} = Z_{batt} + Z_P$ , where  $Z_P$  is the cable impedance) and the DC-link capacitor bank impedance ( $Z_{cap}$ ). These impedances determine the allocation of harmonics between the battery the DC-link capacitor bank and is divided into three different regions. The area shaded in blue corresponds to region (i) and here  $Z_{dc} > Z_{cap}$ . The area shaded in orange represents the region (ii) and here  $Z_{dc} \approx Z_{cap}$ , indicating the resonance. The resonance frequency was found to be about 3.3 kHz. Finally, the shaded area in yellow represents region (iii), where  $Z_{dc} < Z_{cap}$ . It is important to mention that the losses presented in the figure are the losses determined at  $f_{sw}$ , i.e.:

$$\begin{aligned} P_{batt}(\omega_{sw}) &= (I_{batt}(\omega_{sw}))^2 \operatorname{Re}(Z_{batt}(\omega_{sw})), & P_P(\omega_{sw}) &= (I_{batt}(\omega_{sw}))^2 \operatorname{Re}(Z_P(\omega_{sw})), \\ P_{cap}(\omega_{sw}) &= (I_{cap}(\omega_{sw}))^2 \operatorname{Re}(Z_{cap}(\omega_{sw})), & \omega_{sw} &\in [1400\pi, 20000\pi]. \end{aligned} \quad (4)$$

As mentioned previously, the magnitudes of the side-band harmonics are significantly lower. Due to the amplitude and bandwidth limitations of the current transducers and the voltage probes, only the switching frequency components are used determine the loss distribution between the battery and DC-link capacitance. Fig. 7(a) shows the battery losses ( $P_{batt}$ ) at different  $f_{sw}$  and it is evident that  $P_{batt}$  has its maximum at region (i), this is due to the fact that the battery current contains majority of the switching-frequency harmonic components. As  $f_{sw}$  increases,  $Z_{batt}$  increases and  $Z_{cap}$  decreases. As a result, the switching harmonics are bypassed through the DC-link capacitor bank. Thus,  $P_{batt}$  is low. Fig. 7(b) shows the losses in the cables ( $P_P$ ) between the battery and the converter board and it follows  $P_{batt}$  for the same reasons as mentioned earlier. Fig. 7(c) shows the DC-link capacitor bank losses ( $P_{cap}$ ) and it is clear that it has its minimum in region (i). This is due to the fact that  $I_{cap}$  has little to no harmonic components. With an increased  $f_{sw}$ , i.e., moving towards region (iii),  $P_{cap}$  increases because  $I_{cap}$  now contains all the high-frequency harmonic components. In region (ii),  $P_{cap}$  has its maximum because of the resonance. It is clear that  $P_{cap}$  is subjected to the capacitor design, the ESR related to capacitor type and number of parallel units. An improved capacitor design with lower ESR will reduce  $P_{cap}$ . Fig. 7(d) and Fig. 7(e) presents  $I_{batt}$  and  $I_{cap}$  switching frequency components at different  $f_{sw}$ , respectively. From the figure it is clear that in region (i)  $I_{batt} > I_{cap}$ , region (ii)  $I_{batt} \approx I_{cap}$ , and in region (iii)  $I_{batt} < I_{cap}$ . From the figure, it is also clear that the DC-link capacitor bank current is lower than the ripple current limit from the capacitor data-sheet, i.e.  $I_{cap} < 18.5$  A at 700 Hz and  $I_{cap} < 25$  A at 10 kHz [30, 31].

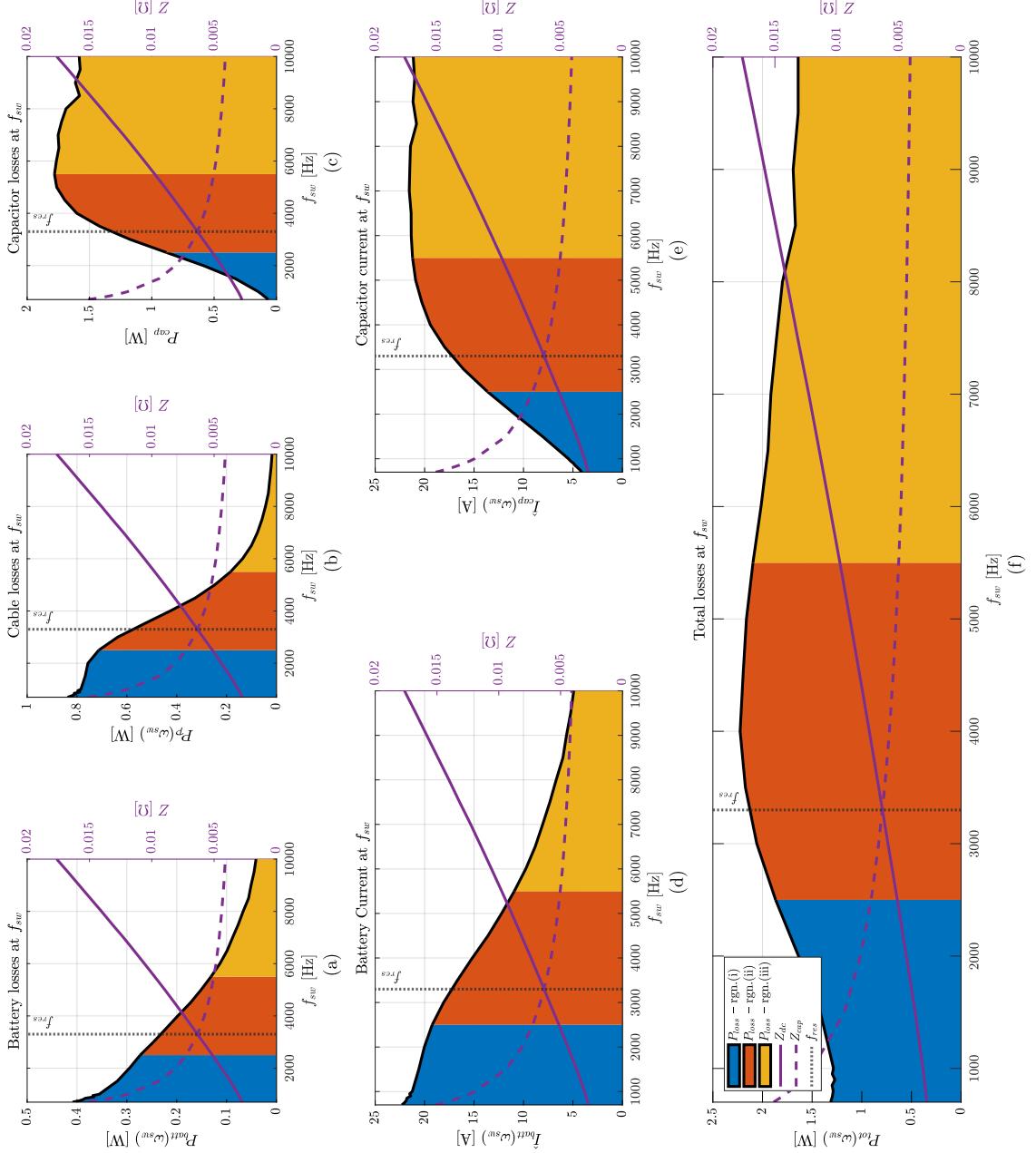


Fig. 7: Loss distribution between the battery and DC-link capacitor bank at different converter switching frequencies ( $f_{sw}$ ). (a) battery loses ( $P_{batt}$ ), (b) cable losses, (c) DC-link capacitor bank losses ( $P_{cap}$ ), (d) battery current ( $I_{batt}$ ) component at  $f_{sw}$ , (e) DC-link capacitor bank current ( $I_{cap}$ ) component at  $f_{sw}$ , and (f) total losses ( $P_{tot}$ ).

Fig. 7(f) presents the total losses ( $P_{tot} = P_{batt} + P_{cap} + P_{\varphi}$ ) at different  $f_{sw}$ . From the figure it is clear that  $P_{tot}$  has its minimum in region (i), the maximum losses occurs in region (ii), and  $P_{tot}$  gradually reduces in region (iii).

## Conclusion

A methodology to characterize the battery impedance at high frequencies using the full-load converter current is presented. The effect of battery and capacitor impedances on the battery and the DC-link capacitor bank currents' harmonics are experimentally validated. The allocation of harmonics can be divided into three regions given by the selection of switching frequency in relation to the resonance between battery inductance, cable inductance and DC-link capacitance. In region (i), the switching frequency ( $f_{sw}$ ) is below the resonance ( $f_{res}$ ), the battery current contains the major share of the switching frequency component and therefore increasing the battery losses. The total losses at the switching frequency are lowest in this region. The total losses peak in region (ii) because of the resonance between the battery and DC-link capacitor bank. Finally, in region (iii),  $f_{sw}$  is above the resonance, the battery current has little to no switching frequency harmonics and therefore reducing the battery losses. Although the capacitor currents are high in this region, the low resistance of the capacitors results in lower total losses in region (iii) when compared to region (ii).

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