

A General Method to Measure Parasitic Capacitance of Transformer Using Guarding Technique

Shaokang Luan¹, Stig Munk-Nielsen¹, Bruce Wakelin², Magnus Hortans², Jan Schupp²,
Hongbo Zhao¹

¹DEPARTMENT OF ENERGY, AALBORG UNIVERSITY

Pontoppidanstræde 111, Aalborg, Denmark

²DANFOSS A/S

Nordborgvej 81, Nordborg, Denmark

slu@energy.aau.dk

Acknowledgements

The authors would like to acknowledge the financial support from Innovation Fund Denmark and thank the editors and reviewers for providing valuable comments and suggestions.

Keywords

«Parasitic elements», «Measurement», «Transformer»

Abstract

Precise, simple, and general measurement methods are essential for parasitic capacitance of transformer. Conventional two-terminal method has some limitations on the measurement of multi-winding transformer, like complex measurement processes. This paper introduces guarding technique into a new method to measure parasitic capacitance of multi-winding transformer. The principle and measurement processes of proposed three-terminal guarding method are introduced in detail. Comprehensive comparisons between two-terminal method and guarding method are made based on circuit verification and three case studies. Guarding method has high accuracy, but simpler measurement processes, and higher feasibility for multi-winding transformer compared to the conventional two-terminal method.

I. Introduction

Due to the rapid development of wide-bandgap (WBG) semiconductors with higher switching speed and blocking voltage, the frequency and voltage level of DC/DC converters are on the increase in a wide range of applications. But much higher dv/dt during switching transient in WBG semiconductors is a potential source of electromagnetic interference (EMI) [1-4]. In the meanwhile, the sizes of passive components, e.g., transformers, can be significantly reduced at higher operation frequency [5]. More compact structure of transformer can result in larger parasitic capacitances because of smaller distances between turn to turn and turn to core [6, 7]. Large parasitic capacitances will offer paths for common mode (CM) noise and, together with high dv/dt , lead to severe EMI issues in converters [8]. Accordingly, parasitic capacitances are drawing more and more attention in transformer design [9, 10].

Proper measurement methods are crucial to evaluate the parasitic capacitance of transformer, which can provide verifications and guidelines for the transformer design. Six-lumped-capacitance equivalent circuit shown in Fig. 1 is precise and widely used in measurement and modelling of parasitic capacitance in two-winding transformer, which is derived based on the conservation of energy [11]. [12] introduced a conventional two-terminal measurement method, which is normally used in the measurement of two-terminal circuit, like inductor [13], to two-winding transformer based on six-capacitance equivalent circuit. In this method, at least six different measurement setups shorting the transformer into six different two-terminal circuits are needed. Then six two-terminal measurements are carried out by impedance analyzer to obtain equivalent capacitances of six two-terminal circuits. The values of six parasitic capacitances were calculated by matrix operations based on measurement results. Proper

selection of measurement setups is essential to simplify the measurement processes and matrix operations. Pre-analyses and data post-processing complicated the measurements and, together with the propagation of errors, became the obstacles to generalizing this method to the measurements for parasitic capacitances of multi-winding transformer.

Guarding technique is a three-terminal measurement function provided by impedance analyzer E4990A together with adaptor 16047E from Keysight [14], which is initially used in in-circuit-test (ICT) to detect the component and manufacture flaws of printed circuit board assemblies (PCBA) [15]. This method has been used to measure the parasitic capacitances of three-terminal inductors with grounded cores in [16, 17]. In this paper, guarding technique will be applied in a more general measurement method for parasitic capacitance of multi-winding transformer. Through proper uniform measurement setup, each individual parasitic capacitance of multi-winding transformer can be accurately measured in simple processes.

This paper is organized as follows: In Section II, conventional two-terminal method is reviewed together with its limitations. In Section III, the principle of proposed guarding method is introduced in detail, taking two-winding transformer as an example. In Section IV, the proposed guarding method is generalized to multi-winding transformer. In Section V, circuit verification and three case studies are conducted to compare guarding method with conventional two-terminal method on the accuracy, measurement simplicity, and feasibility for multi-winding transformer.

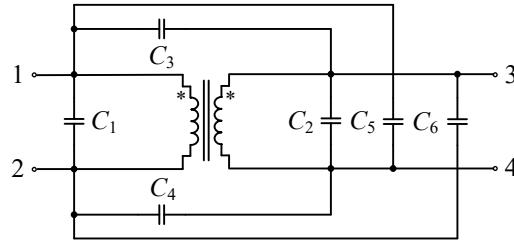
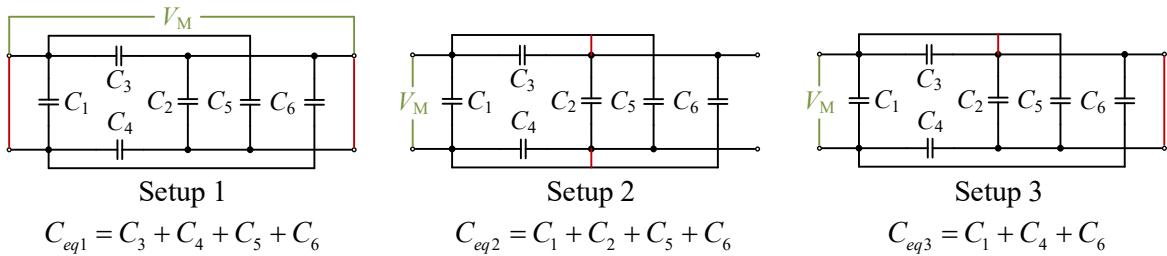


Fig. 1 Six-lumped-capacitance equivalent circuit for two-winding transformer

II. Review of conventional two-terminal method and its limitations

Conventional two-terminal method introduced in [11] only focused on two-winding transformer with four terminals, which is based on a six-lumped-capacitance equivalent circuit, shown in Fig. 1. C_1 and C_2 are intra-winding parasitic capacitances of primary and secondary sides. C_3 , C_4 , C_5 and C_6 are interwinding parasitic capacitances between primary and secondary sides. 1 ~ 4 are four terminals of two-winding transformer. The component under test (CUT), taking C_1 as an example, cannot be directly measured, because there are some shunt paths around CUT, like $C_2 \sim C_6$ connected to the two terminals of C_1 . So, there was an essential precondition in conventional two-terminal method: two-winding transformer can be seen as a linear system under small test signal from impedance analyzer, whether it be air-core transformers, ferromagnetic-core transformers, or ferrimagnetic-core transformers. In this condition, six parasitic capacitances in Fig. 1 can be treated as six variables, which can be deduced by six independent linear equations.



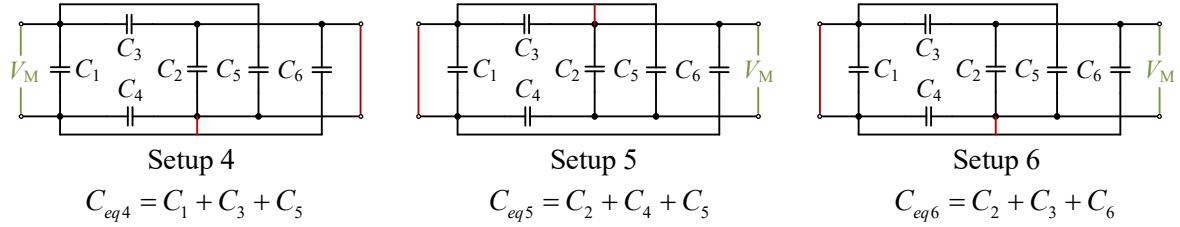


Fig. 2 Six independent measurement setups

Fig. 2 shows six independent measurement setups and six independent linear equations generated by two-terminal method. Red lines represent the short-circuit lines simplifying the four-terminal circuits of two-winding transformer to two-terminal circuits, V_M is the two-terminal source of impedance analyzer, $C_{eq1} \sim C_{eq6}$ are equivalent capacitances of six two-terminal circuits. The results obtained by impedance analyzer are frequency responses of six two-terminal circuits, from which $C_{eq1} \sim C_{eq6}$ are derived. All parasitic capacitance $C_1 \sim C_6$ can be deduced through matrix operations as (1).

$$\begin{bmatrix} C_1 \\ C_2 \\ C_3 \\ C_4 \\ C_5 \\ C_6 \end{bmatrix} = \frac{1}{2} \cdot \begin{bmatrix} -1 & 0 & 1 & 1 & 0 & 0 \\ -1 & 0 & 0 & 0 & 1 & 1 \\ 0 & -1 & 0 & 1 & 0 & 1 \\ 0 & -1 & 1 & 0 & 1 & 0 \\ 1 & 1 & -1 & 0 & 0 & -1 \\ 1 & 1 & 0 & -1 & -1 & 0 \end{bmatrix} \cdot \begin{bmatrix} C_{eq1} \\ C_{eq2} \\ C_{eq3} \\ C_{eq4} \\ C_{eq5} \\ C_{eq6} \end{bmatrix} \quad (1)$$

It should be noticed that proper selections of measurement setup are crucial for two-terminal method, which need thorough analyses before setting up the measurements. The reasons are as follows:

1. The measurement results of some setups, like Setup 7 shown in Fig. 3, can significantly increase the complexity of data post-processing. To simplify data post-processing, it requires that two-winding transformers need to be simplified by short-circuiting lines into two-terminal circuits with all parasitic capacitances paralleled to each other in all measurement setups. In other words, there should be only two nodes left in every simplified two-terminal circuits.
2. The measurement results of different setups can be same to each other, like Setup 8 shown in Fig. 3 and Setup 3 shown in Fig. 2, which are called dependent setups. There will be invalid measurements if dependent setups are chosen.

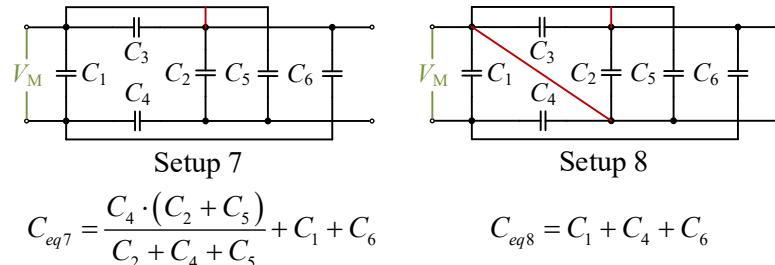


Fig. 3 Other two measurement setups

Through analysis, the limitations of conventional two-terminal method can be summarized as follows:

1. Pre-analyses for the proper selection of measurement setups is needed. Otherwise, large amounts of invalid measurements and unnecessary data post-processing will significantly complicate the measurement processes.

2. Data post-processing is always needed. All measurement results in this method are equivalent capacitances of different simplified two-terminal circuits. Additional matrix operations are needed to obtain the parasitic capacitances.
3. Low feasibility for multi-winding transformers. In the n -terminal equivalent circuit for multi-winding transformer, there will be $n(n-1)/2$ parasitic capacitances to be measured. At least $n(n-1)/2$ independent linear equations generated by $n(n-1)/2$ different measurement setups are needed. Limitation 1) and 2) will be more severe in parasitic capacitance measurement of multi-winding transformer if n is much larger.

III. Proposed guarding method for two-winding transformer

Guarding technique can eliminate the mentioned influences from shunt paths around CUT in Section II, which means that CUT can be directly measured. The schematic diagram of guarding technique, provided by impedance analyzer E4990A together with adaptor 16047E from Keysight, is shown in Fig. 4. There are three terminals in adaptor 16047E: S for source terminal, M for measurement terminal, G for guard terminal. V_s for source voltage, V_m for measurement voltage. I_1 , the current of Z_1 , which flows between S and G , does not flow to the auto-balancing bridge. Thus, I_1 has nearly no effect on the measurements of CUT. Because the equivalent input impedance of auto-balancing bridge is negligible, the voltage potential of M is nearly to zero (virtual ground due to auto-balancing), which basically shorts Z_2 . I_2 , which flows between M and G , is much smaller and negligible compared to I_x , current of CUT. Hence $I_x \approx I_m$, current of auto-balancing resistance R_m . CUT can be derived as (2). The measurement result of guarding technique is the frequency response of CUT. Therefore, direct measurement of CUT is achieved.

$$I_x \approx I_m \quad \frac{V_s}{\text{CUT}} \approx \frac{V_m}{R_m} \quad \text{CUT} \approx \frac{V_s \cdot R_m}{V_m} \quad (2)$$

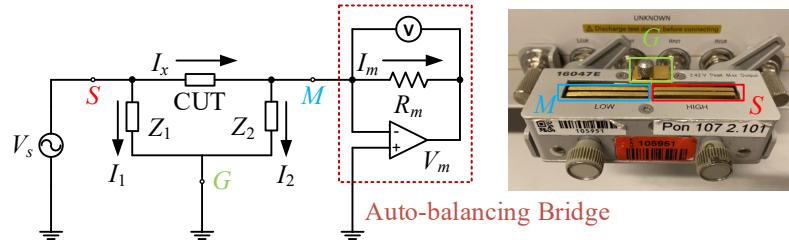
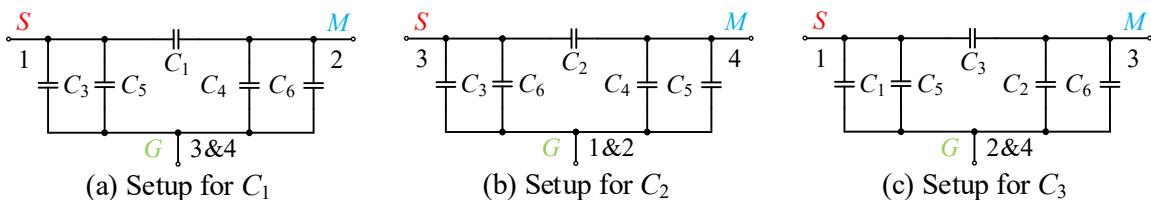


Fig. 4 Schematic diagram of guarding technique

Since guarding technique is provided for three-terminal circuit measurements, proper connections between two-winding transformers, which have four terminals, and adaptor 16047E are crucial to the feasibility of guarding method. The proposed guarding method to measure parasitic capacitance of two-winding transformer is shown in Fig. 5 (also based on the six-lumped-capacitance equivalent circuit in Fig. 1). Taking the measurement of C_1 as an example, S and G should be connected to the two terminals directly connected to C_1 , 1 and 2. The rest of two terminals, 3 and 4, should be connected to G . As shown in Fig. 5 (a), C_2 is shorted. Four-terminal circuit of two-winding transformer can be reduced to three-terminal circuit suitable for guarding technique. Based on former analyses in Fig. 4, C_1 can be directly measured through impedance analyzer E4990A together with adaptor 16047E. The other parasitic capacitances $C_2 \sim C_6$ can be measured in similar way with guarding technique shown in Fig. 5 (b) – (f).



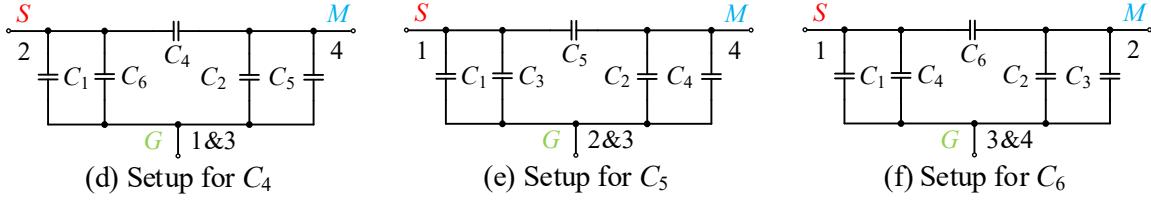


Fig. 5 Proposed guarding method to measure parasitic capacitance of two-winding transformer

IV. Proposed guarding method for multi-winding transformer

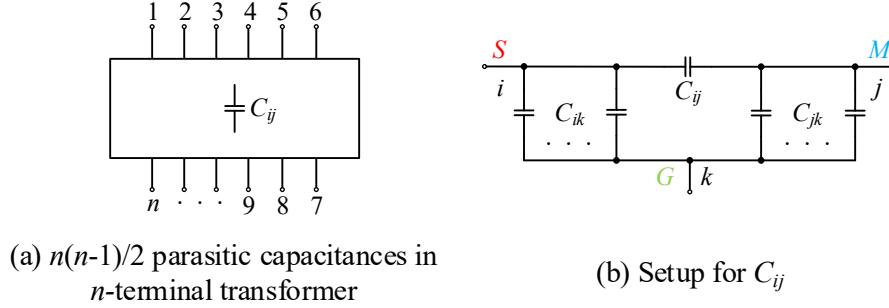


Fig. 6 Proposed guarding method to measure parasitic capacitance of multi-winding transformer

Guarding method can be extended to general multi-winding transformers (number of windings ≥ 2), there will be n terminals ($n \geq 4$) and $n(n-1)/2$ parasitic capacitances to be measured, shown in Fig. 6 (a). Randomly choose one parasitic capacitance C_{ij} ($i, j \in \{1, 2, \dots, n\}$) as CUT, S and G should be connected to two terminals directly connected to C_{ij} , i and j . The rest of $(n-2)$ terminals k ($k \in \{1, 2, \dots, n\} - \{i, j\}$) should be connected to G . As shown in Fig. 6 (b), all parasitic capacitances which are not directly connected to i or j are shorted and therefore only C_{ik} and C_{jk} are left. N -terminal circuit of multi-winding transformer is reduced to three-terminal circuit suitable for guarding technique. Based on former analyses in Fig. 4, C_{ij} can be directly measured through impedance analyzer E4990A together with adaptor 16047E.

Through analysis, guarding method shows several advantages compared to conventional two-terminal method, shown as follows:

1. Streamlined measurement processes. There is only one measurement setup for any parasitic capacitance. And all parasitic capacitances can be directly measured based on guarding technique. There are no needs for pre-analyses and data post-processing.
2. Higher feasibility for general multi-winding transformers. Uniform measurement setups and direct measurements will always valid no matter how many parasitic capacitances in all for general multi-winding transformers.

V. Experimental verifications

The experimental verifications will include two parts:

1. Circuit verification. The reason why circuit verification is needed is that standard values are always necessary no matter what comparison will be conducted. The comparison between two-terminal method and guarding method cannot be only based on transformer samples, in which all components are unknown and not satisfied for comparison standards. Inspired by ICT, circuit verification can be set as standards for measurements, which is based on a PCB assembled by passive components with known values.
2. Case studies based on three different two-winding transformers.

Through the circuit verification and three case studies, advantages, and limitations of both two measurement methods can be shown. All these verifications are conducted by impedance analyzer 4990A and adaptor 16047E, which are well calibrated. The values of capacitance are calculated based on measured frequency response.

For circuit verification, Fig. 7 (a) and (b) show the PCB assembled by passive components with known values and its schematic diagram. All values in schematic diagram are obtained by measurement results of six different branches shown in Fig. 7 (c) to eliminate the errors caused by tracks and components themselves. And all values of capacitance in every single branch will be set as standard values. Fig. 8 shows the measurement setups of two-terminal method and guarding method. Two-terminal method is based on six setups in Fig. 2, in which sixth order matrix operation shown in (1) is needed to obtain all values of capacitance in every single branch. Guarding method are based on six setups in Fig. 5, in which every single capacitance is directly measured. Table I shows the comparison of standard values, results of two-terminal method, and results of guarding method for all capacitances.

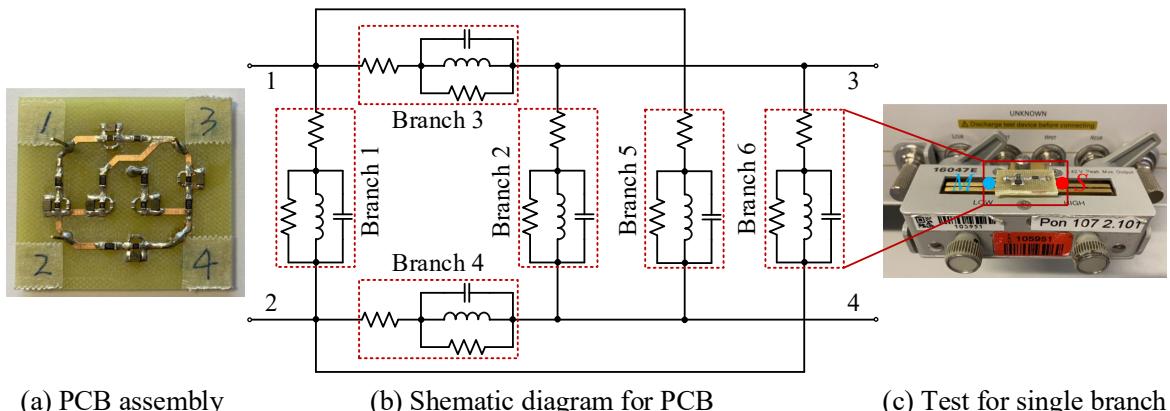


Fig. 7 Circuit verification

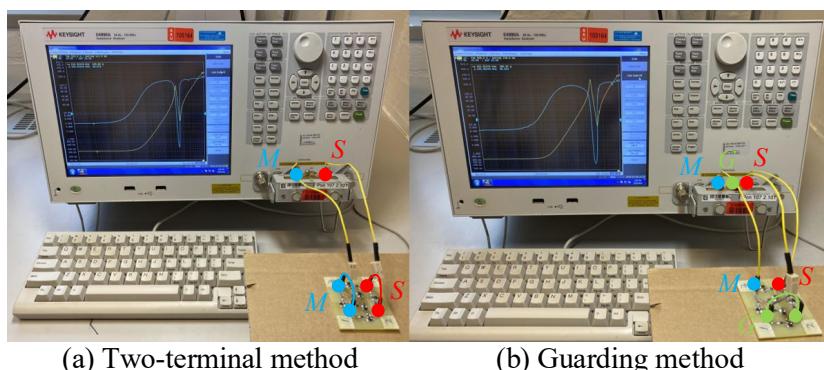


Fig. 8 Measurement setups of circuit verification

Table I: Comparison of standard values, two-terminal method results, and guarding method results in circuit verification

(pF)	Standard	Two-terminal	Errors of Two-terminal	Guarding	Errors of Guarding
C_1	1060	1134	6.98%	982	7.36%
C_2	1190	1046	12.10%	1088	8.57%
C_3	326	308	5.52%	312	4.29%
C_4	326	324	0.61%	330	1.22%
C_5	450	408	9.33%	424	5.78%
C_6	450	440	2.22%	436	3.11%

For two-terminal method, the calculated capacitances have $0.61\% \sim 12.10\%$ absolute values of error compared to standard values. For guarding method, the directly measured capacitances have $1.22\% \sim 8.57\%$ absolute values of error compared to standard values. Both two-terminal method and guarding method are capable to obtain all values of capacitance in every single branch with acceptable errors. Errors are caused by:

1. Extra cables connecting PCB to adaptor.
2. Discrepancies between selected frequencies and real frequencies of first resonant peak.
3. Couplings between different branches.
4. Propagation of errors through matrix operations. This will only occur in two-terminal method, which might have the potential to enlarge errors.

For case studies, Table II shows the comparisons between two-terminal method results and guarding method results for all parasitic capacitances. The test setups for case studies are same to circuit verification shown in Fig. 8. Because there are no accurate values of the parasitic capacitances as the references for the errors, no accuracy comparisons are shown in these samples. The mean values of results obtained by two different methods are set as the references for absolute values of discrepancy between two methods $|\Delta|$. Maximum discrepancy is 14.81% , which is still acceptable.

Table II: Comparison between two-terminal method results and guarding method results in case studies

	Case 1			Case 2			Case 3		
(pF)	Two-terminal	Guarding	$ \Delta $	Two-terminal	Guarding	$ \Delta $	Two-terminal	Guarding	$ \Delta $
C_1	684	752	9.47%	61	60	1.65%	238	247	3.71%
C_2	1100	1210	9.52%	62	62	0.00%	210	209	0.48%
C_3	354	343	3.16%	22	21	4.65%	1390	1260	9.81%
C_4	321	344	6.92%	29	25	14.81%	1440	1260	13.33%
C_5	647	678	4.68%	43	48	10.99%	962	1010	4.87%
C_6	698	693	0.72%	41	40	2.47%	998	1030	3.16%

After circuit verification and case studies, guarding method can be selected as the better measurement method based on followed advantages and limitations shown in Table III.

Table III: Advantages and limitations of two-terminal method and guarding method

	Two-terminal method	Guarding method
1. Accuracy	High	High
2. Measurement processes	Complex	Simple
3. Applicability	Narrow	Broad
4. Instrument Requirement	Low	High

1. Both two-terminal method and guarding method are feasible to obtain parasitic capacitances in two-winding transformers with similar and acceptable errors. Propagation of errors through matrix operations should be noticed in two-terminal method.
2. To obtain all parasitic capacitances in two-winding transformers, both methods need six tests. But there are pre-analyses for the proper selection of measurement setups and data post-

- processing in two-terminal method. Guarding method can directly measure each individual parasitic capacitance.
3. Measurement processes of two-terminal method will be much more complex for multi-winding transformer with more terminals. Meanwhile, it will keep simple in guarding method due to uniform measurement setups and direct measurements.
 4. Any impedance analyzer with any two-terminal adaptor is sufficient for two-terminal method. But guarding method can only be conducted using impedance analyzers and adaptors with guarding function.

Error analyses of both two methods are complex but important for more accurate results, especially the propagation of errors in two-terminal method. Therefore, error analyses will be discussed in future work.

VI. Conclusion

A more general method for parasitic capacitance measurement of transformer is proposed in this paper, which is based on three-terminal guarding technique. Without pre-analyses, data post-processing, and propagation of errors, guarding method can directly measure each individual parasitic capacitance, which is crucial for multi-winding transformer. Circuit verification based on a PCB with known components and three case studies of two-winding transformers was conducted for the comparisons between conventional two-terminal method and guarding method. With high accuracy, simpler measurement processes, guarding method is a better measurement method for parasitic capacitance in multi-winding transformer. Error analyses, especially propagation of errors in two-terminal method, will be priorities in future research.

References

- [1] Zhang, B. and Wang, S.: A survey of EMI research in power electronics systems with wide-bandgap semiconductor devices, *IEEE Journal of Emerging and Selected Topics in Power Electronics* 8.1 (2019), pp.626-643.
- [2] Dalal, D.N., Zhao, H., Jørgensen, J.K., Christensen, N., Jørgensen, A.B., Bęczkowski, S., Uhrenfeldt, C. and Munk-Nielsen, S.: Demonstration of a 10 kV SiC MOSFET based medium voltage power stack, *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 2751-2757.
- [3] Thummala, P., Schneider, H., Zhang, Z. and Andersen, M.A.: Investigation of transformer winding architectures for high-voltage (2.5 kV) capacitor charging and discharging applications, *IEEE Transactions on Power Electronics* 31.8 (2015), pp.5786-5796.
- [4] Nguyen-Duy, K., Ouyang, Z., Petersen, L.P., Knott, A., Thomsen, O.C. and Andersen, M.A.: Design of a 300-W isolated power supply for ultrafast tracking converters, *IEEE Transactions on Power Electronics* 30.6 (2014), pp.3319-3333.
- [5] Bahmani, M.A., Thiringer, T., Rabiei, A. and Abdulahovic, T.: Comparative study of a multi-MW high-power density DC transformer with an optimized high-frequency magnetics in all-DC offshore wind farm, *IEEE Transactions on power delivery* 31.2 (2015), pp.857-866.
- [6] Biela, J. and Kolar, J.W.: Using transformer parasitics for resonant converters-a review of the calculation of the stray capacitance of transformers, *IEEE Transactions on Industry Applications*, Vol. 44, No. 1 (2008), pp. 223-233.
- [7] Liu, X., Wang, Y., Zhu, J., Guo, Y., Lei, G. and Liu, C.: Calculation of capacitance in high-frequency transformer windings, *IEEE Transactions on Magnetics* 52.7 (2016), pp.1-4.
- [8] Zhang, H., Wang, S., Li, Y., Wang, Q. and Fu, D.: Two-capacitor transformer winding capacitance models for common-mode EMI noise analysis in isolated DC-DC converters, *IEEE Transactions on Power Electronics* 32.11 (2017), pp.8458-8469.
- [9] Dalessandro, L., da Silveira Cavalcante, F. and Kolar, J.W.: Self-capacitance of high-voltage transformers, *IEEE Transactions on power electronics* 22.5 (2007), pp.2081-2092.
- [10] Fei, C., Yang, Y., Li, Q. and Lee, F.C.: Shielding technique for planar matrix transformers to suppress common-mode EMI noise and improve efficiency, *IEEE Transactions on Industrial Electronics* 65.2 (2018), pp.1263-1272.

- [11] Blache, F., Keradec, J.P. and Cogitore, B.: Stray capacitances of two winding transformers: equivalent circuit, measurements, calculation and lowering, 1994 IEEE Industry Applications Society Annual Meeting Vol. 2, pp. 1211-1217.
- [12] Biela, J., Bortis, D. and Kolar, J.W.: Modeling of pulse transformers with parallel-and non-parallel-plate windings for power modulators, IEEE Transactions on Dielectrics and Electrical Insulation 14.4 (2007), pp.1016-1024.
- [13] Zhao, H., Luan, S., J Hanson, A., Gao, Y., Dalal, D.N., Wang, R., Zhou, S. and Munk-Nielsen, S.: Rethinking Basic Assumptions for Modeling Parasitic Capacitance in Inductors, IEEE Transactions on Power Electronics, Early Access Article.
- [14] Impedance Measurement Handbook, Keysight Technologies.
- [15] Hults, C., Schwedner, F. and Grossman, S.: In-Circuit Test Systems-An Evolution, IEEE Transactions on Manufacturing Technology 4.2 (1975), pp.42-48.
- [16] Zhao, H., Dalal, D.N., Jørgensen, A.B., Jørgensen, J.K., Wang, X., Bęczkowski, S., Munk-Nielsen, S. and Uhrenfeldt, C.: Physics-based modeling of parasitic capacitance in medium-voltage filter inductors, IEEE Transactions on Power Electronics 36.1(2021), pp.829-843.
- [17] Zhao, H., Shen, Z., Dalal, D.N., Jørgensen, A.B., Wang, X., Munk-Nielsen, S. and Uhrenfeldt, C.: Parasitic Capacitance Modeling of Inductors Without Using the Floating Voltage Potential of Core. IEEE Transactions on Industrial Electronics 69.3 (2021), pp.3214-3222.