Operating Test Circuit for Valves in MMC Based HVDC Power Conversion System

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***Abstract*-- This paper deals with a new valve test circuit for MMC based HVDC power system. IEC-62501 requires some clauses for the valve operating test to guarantee the reliability of the HVDC power conversion station. Therefore, the valve test circuit should satisfy the requirement of IEC-62501 standard. The proposed test circuit provides a test current contains 2^{nd} harmonic and dc offset components as well as the fundamental component which is very similar to the real operating arm current in HVDC system. The auxiliary valve and double two-phase inverters in the proposed scheme can reduce the power rating of the test circuit power supply and switching stress of the inverter dramatically compared to the conventional test circuits. Simulation and experimental results show the usefulness of the proposed circuit.**

***Index Terms*-- HVDC, MMC, Valve**

I. Introduction

VSC(voltage source converter)-HVDC(high voltage direct current) system has good features such as significantly reduced filter size, fast response time, and low construction cost compared to the LCC(line-commutated current source converter)-HVDC system. MMC(modular multilevel converter) is widely used for the power conversion topology of the VSC-HVDC system [1-2]. An MMC based HVDC power conversion station has six arms, and each arm has hundreds of submodules connected in series. It is important to guarantee the reliability of the power stations of the HVDC system. To obtain the reliability each arm should be tested under the worst operating condition, however, the test is very difficult because of too many submodules connected in series. Therefore, IEC-62501 (International standard for VSC valves for HVDC power transmission-electrical testing) proposes clauses about performance test of valves having several submodules connected in series for ensuring system reliability. In order to test the valve a test circuit is necessary to provide the test current similar to the real HVDC arm current in normal operation. Therefore, the test current should contain fundamental ac component, 2^{nd} harmonic component, and dc offset.

Few test circuits for the valve of MMC based HVDC system have been proposed. The test circuit in [3] is simple, however, it has some problems of high input dc voltage for the test and pure sinusoidal arm current without 2^{nd} harmonic and dc offset components. The voltage magnitude of the power supply for the test circuit should be almost equal to the sum of each submodule capacitor voltage, therefore, the power supply voltage magnitude is proportional to the number of submodules. The arm current in literature [4] satisfies the requirement of IEC-62501, however, huge capacitor and isolated dc-to-dc converter are necessary to reduce the ripple components caused by the circulating dc current between rectifier and inverter mode operations. The test circuit in [5] overcomes abovementioned problems, however, the inverter for the test current control has high switching stress.

This paper proposes a new valve test circuit with simple structure without circulating dc current, considerably reduced power supply voltage magnitude compared to the conventional test circuit, and reasonable switching stress.

II. Proposed Circuit and Operating Principle

A. Proposed circuit

Fig. 1 shows the proposed test circuit for a valve in MMC based HVDC power system. The circuit consists of a main valve, an auxiliary valve, two full bridge inverters connected in parallel and dc power source. A reactor is connected to the output of each arm in the inverter, and the other sides of the reactors are connected each other, therefore, the test current is the sum of the reactor currents. The main valve corresponds to the valve to be tested. An auxiliary valve is connected to the main valve, and the structure and the number of submodules in each valve are the same. IEC-62501 suggests the number of the submodules should be at least five. The topology of each

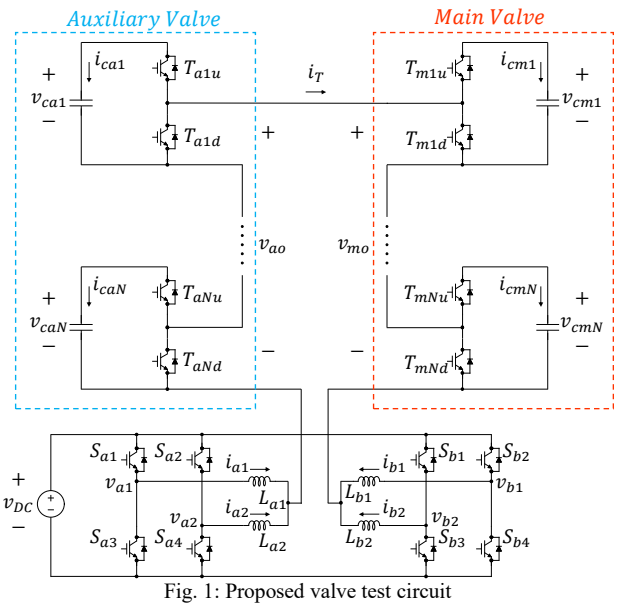

Fig. 1: Proposed valve test circuit

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submodule can be full-bridge type or half-bridge type, by the way, half-bridge type submodule is used in this paper.

B. Operating Principle

The IGBTs in the main valve are turned on and turned off according to the operating condition. The major role of the auxiliary valve is the compensation of the main valve output voltage of v_{mo}. The compensation is carried out by making the number of turned on submodules in the main and auxiliary valves the same, then the average values of v_{mo} and v_{ao} become the same. Therefore, it is easy to generate the test current i_T by inverter output current control. There is no need of the consideration of valve operating status. Furthermore, the magnitude of the dc power source voltage for the inverter can be minimized regardless of the number of submodules in the main and auxiliary valves. The two inverters operate in two-phase mode, therefore, the phase difference between v_{a1} and v_{a2} is $180°$. Fig. 2 shows an example of inverter switching to generate test current i_T.

The required test current contains fundamental, 2^{nd} harmonic, and dc components as shown in (1).

$$i_T(t) = \frac{\sqrt{2}}{2} I_1 \sin(\omega t + \emptyset) + I_d + I_z \sin(2\omega t + \theta) \quad (1)$$

Where, I_d is the dc component of the arm current, I_1 is the rms value of grid current, and I_z is the peak value of 2^{nd} harmonic component of the circulating current between arms as shown in Fig. 3.

The switching function for upper and lower arm are

$$S_{ap(t)} = \frac{1}{2}(1 - m\sin(\omega t)) \quad (2)$$

$$S_{an(t)} = \frac{1}{2}(1 + m\sin(\omega t)) \quad (3)$$

Where, m is modulation index. Therefore, the upper and lower arm submodule capacitor currents are

$$i_{cp}(t) = S_{ap}(t) \cdot i_{ap}(t) = i_{c0} + i_{c1} + i_{c2} + i_{c3} \quad (4)$$

$$i_{cn}(t) = S_{an}(t) \cdot i_{an}(t) = i_{c0} - i_{c1} + i_{c2} - i_{c3} \quad (5)$$

Where, i_{c0}, i_{c1}, i_{c2}, and i_{c3} are dc, fundamental, 2^{nd} harmonic, and 3^{rd} harmonic components, respectively, and expressed as follows.

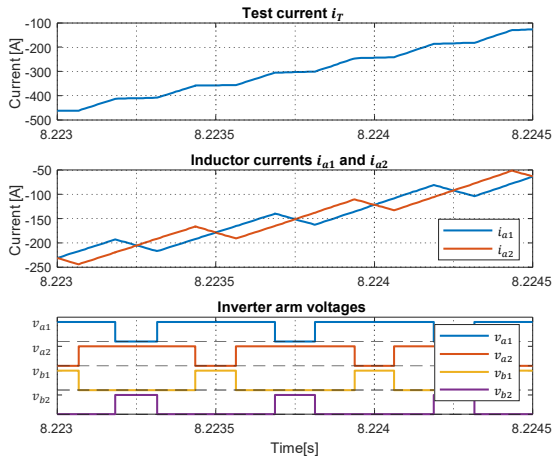


Fig. 2: Inverter arm voltages and currents in test current increasing mode

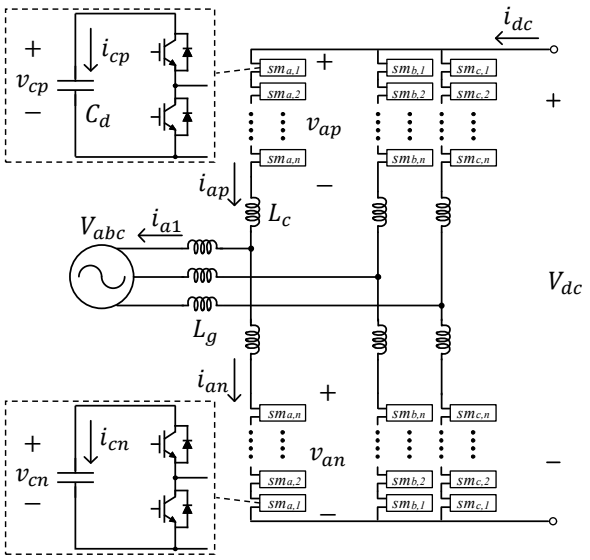


Fig. 3: MMC-based HVDC power station

$$i_{c0} = \frac{1}{2} I_d - \frac{\sqrt{2}}{8} m I_1 \cos\phi \quad (6)$$

$$i_{c1} = -\frac{1}{2} m I_d \sin(\omega t) + \frac{\sqrt{2}}{4} I_1 \sin(\omega t + \phi) - \frac{1}{4} m I_z \cos(\omega t + \theta) \quad (7)$$

$$i_{c2} = \frac{\sqrt{2}}{8} m I_1 \cos(2\omega t + \phi) + \frac{1}{2} I_z \sin(2\omega t + \theta) \quad (8)$$

$$i_{c3} = \frac{1}{4} m I_z \cos(3\omega t + \theta) \quad (9)$$

Submodule capacitor voltages are calculated from equations (4) and (5).

$$v_{cp}(t) = v_{c0} + \frac{1}{jn\omega C} i_{cp}(t) = v_{c0} + \Delta v_{c1} + \Delta v_{c2} + \Delta v_{c3} \quad (10)$$

$$v_{cn}(t) = v_{c0} + \frac{1}{jn\omega C} i_{cn}(t) = v_{c0} - \Delta v_{c1} + \Delta v_{c2} - \Delta v_{c3} \quad (11)$$

Where, v_{c0}, Δv_{c1}, Δv_{c2}, and Δv_{c3} are capacitor average voltage, fundamental, 2^{nd} harmonic, 3^{rd} harmonic component of the capacitor voltages, respectively, as follows

$$\Delta v_{c1} = \frac{m I_d}{2\omega C_d} \cos(\omega t) - \frac{\sqrt{2} I_1}{4\omega C_d} \cos(\omega t + \phi) - \frac{m I_z}{4\omega C_d} \cos(\omega t + \theta) \quad (12)$$

$$\Delta v_{c2} = \frac{\sqrt{2} m I_1}{16\omega C_d} \sin(2\omega t + \phi) - \frac{I_z}{4\omega C_d} \cos(2\omega t + \theta) \quad (13)$$

$$\Delta v_{c3} = \frac{m I_z}{12\omega C_d} \sin(3\omega t + \theta) \quad (14)$$

So, the upper and lower arm voltages are

$$v_{ap}(t) = N_{sm} \cdot S_{ap}(t) \cdot v_{cp}(t) = \frac{V_{DC}}{2} - \frac{V_{DC}}{2} m \sin(\omega t) + \Delta v_0 + \Delta v_1 + \Delta v_2 + \Delta v_3 + \Delta v_4 \quad (15)$$

$$v_{an}(t) = N_{sm} \cdot S_{an}(t) \cdot v_{cn}(t)$$
$$= \frac{V_{DC}}{2} + \frac{V_{DC}}{2} m \sin(\omega t)$$
$$+\Delta v_0 - \Delta v_1 + \Delta v_2 - \Delta v_3 + \Delta v_4 \quad (16)$$

Where, N_{sm} is the number of submodules in each arm. From (15) and (16) common mode leg output voltage $v_{com}(t)$ is

$$v_{com}(t) = \frac{v_{ap}(t)+v_{an}(t)}{2}$$
$$= \frac{v_{DC}}{2} + \Delta v_0 + \Delta v_2 + \Delta v_4 \quad (17)$$

Where, Δv_2 is 2^{nd} harmonic ripple component as follows.

$$\Delta v_2 = N_{sm}\left[-\frac{m^2 I_d}{8\omega C_d}\sin(2\omega t) + \frac{3\sqrt{2} m I_1}{32\omega C_d}\sin(2\omega t + \phi)\right)$$
$$-\left(\frac{I_z}{8\omega C_d} + \frac{m^2 I_z}{12\omega C_d}\right)\cos(2\omega t + \theta)] \quad (18)$$

Finally, the circulating 2^{nd} harmonic component current I_z is calculated as follows [6]

$$I_z = \frac{\sqrt{(A\cos\phi + B)^2 + (A\sin\phi)^2}}{1 - \frac{N_{sm}}{16\omega^2 C_d L_c} - \frac{m^2 N_{sm}}{24\omega^2 C_d L_c}} \quad (19)$$

$$\theta = \tan\left(\frac{A\cos\phi + B}{A\sin\phi}\right) \quad (20)$$

$$A = \frac{3\sqrt{2}}{64}\frac{m N_{sm} I_1}{\omega^2 C_d L_c} \qquad B = -\frac{N_{sm}}{16}\frac{m^2 I_d}{\omega^2 C_d L_c}$$

The test current $i_T(t)$ of (1) is generated with proper PI and PR controller of the full-bridge inverter. The inverter output current contains both common and differential components, and expressed as follows for i_{a1} and i_{a2}.

$$i_{a1} = i_{com,a} + i_{diff,a} \quad (21)$$

$$i_{a2} = i_{com,a} - i_{diff,a} \quad (22)$$

The differential component current should be zero. Fig. 4 shows the block diagram for the generation of each arm output voltage of the inverters. The number of phases in the inverter, of course, can be increased to three or four according to the current level.

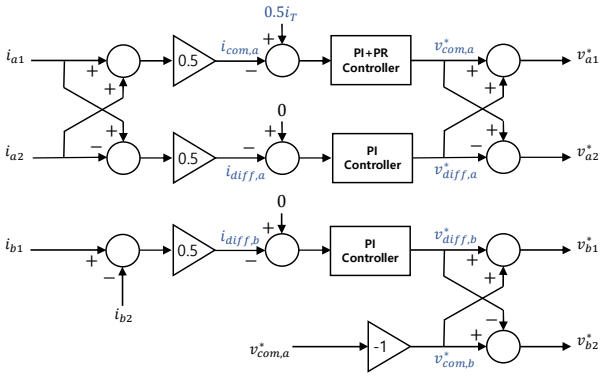


Fig. 4: Inverter arm voltage reference signal generation

III. Simulation Result

Simulations are carried out with the parameters in Table 1, and the number of submodules in each valve is four.

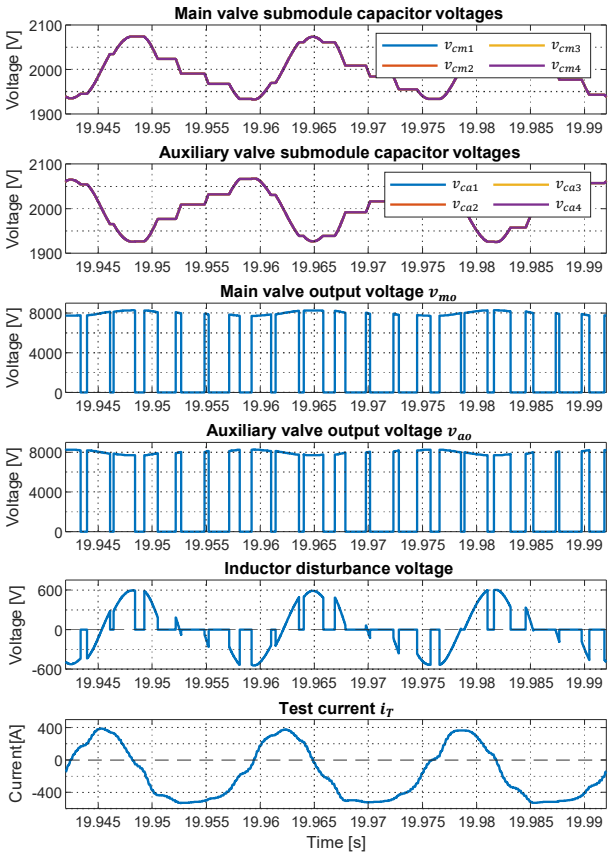
Fig. 5 shows the waveforms of voltages and currents in each component with the variation of carrier phase shift. Fig. 5(a) shows main valve submodule capacitor voltages, auxiliary valve submodule capacitor voltages, main valve output voltage v_{mo}, auxiliary valve output voltage of v_{ao}, the difference voltage of v_{mo} and v_{ao}, and test current of i_T, in case of carrier phase shift is $0°$. In this case all the carrier signals for each submodule are the same, therefore, each main valve submodule capacitor voltage is the same, and the waveforms of auxiliary valve submodule capacitors are also the same. Since all the submodules are turned on and off at the same time the magnitudes of main and auxiliary valve output voltage are zero or the sum of the 4 submodule capacitor voltages in each valve. Although the switching time of the IGBTs in each valve is the same the phase difference between the main and auxiliary valve output voltages results in a disturbance voltage to the inductor. It is found that the test current i_T has 2^{nd} harmonic component and dc offset as well as the fundamental component.

Fig. 5(b) shows each voltage and current waveform in case of carrier phase shift is $180°$. The valve output voltages have 3 levels due to the phase shift of $180°$, therefore, the voltage applied to the inductor has reduced harmonic components, which results in test current with reduced distortion. The test current also has 2^{nd} harmonic component and dc offset as well as the fundamental component. Fig. 5(c) shows each voltage and current waveform in case of phase shift of $90°$ between the carrier signals for the 4 submodules in the main and auxiliary valves. It is found that each submodule voltage is phase shifted each other by $90°$, and each valve output voltage has 5 levels. Therefore, the harmonic components of the inductor voltage are considerably reduced, and the test current has significantly reduced harmonic components except 2^{nd} harmonic component.

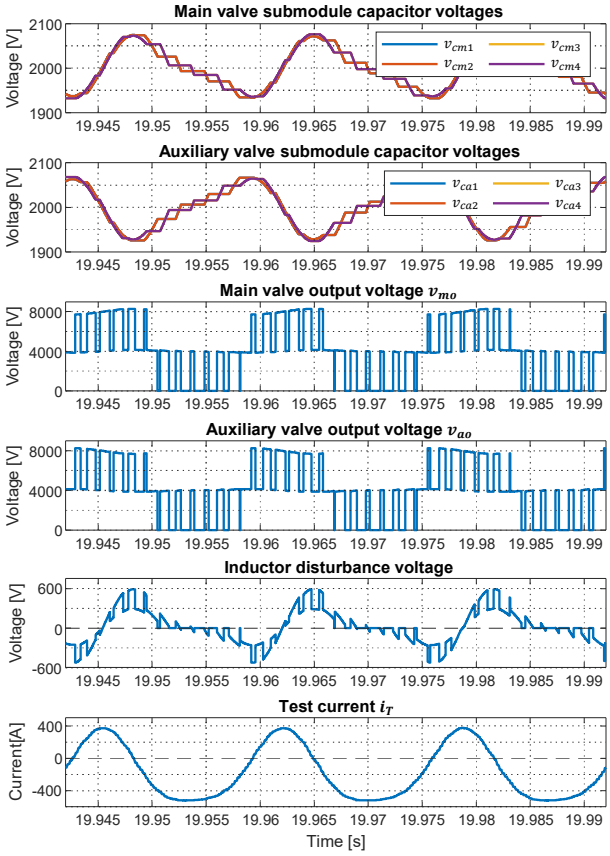
Fig. 6 shows the fourier spectrum of the inductor voltage and test current. It is found that the magnitude of the spectrum in case of $90°$ phase shift is dramatically reduced below 1 [kHz] compared to those in case of $0°$ and $180°$ phase shift.

TABLE I
Simulation Parameters

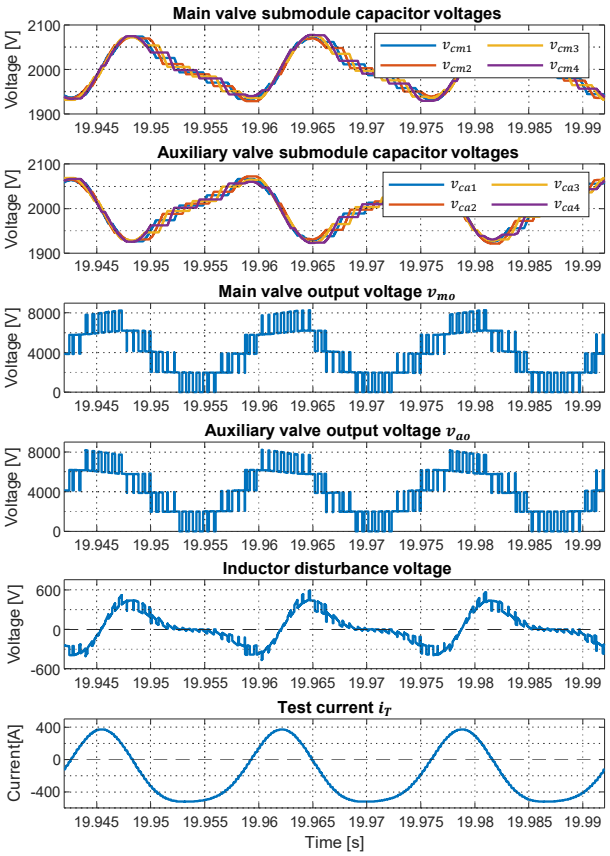
Parameter	Value
Submodule cap. voltage	2 [kV]
Submodule capacitor	8 [mF]
Inductor (L_{a1}~L_{b2})	5 [mH]
Inverter f_s	2 [kHz]
$i_{T,rms}$	360 [A]
$i_{T,peak-to-peak}$	975 [A]
$i_{T,dc}$	-167 [A]
Submodule f_s	400 [Hz]



(a) In case of carrier phase shift is 0°



(b) In case of carrier phase shift is 180°



(c) In case of carrier phase shift is 90°

Fig. 5: Voltages and currents in each component

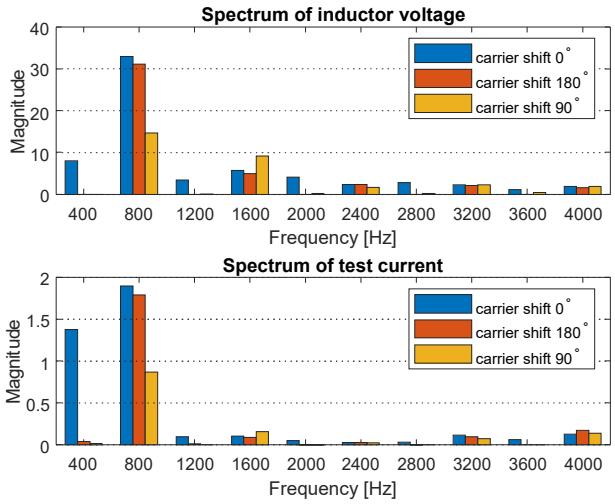
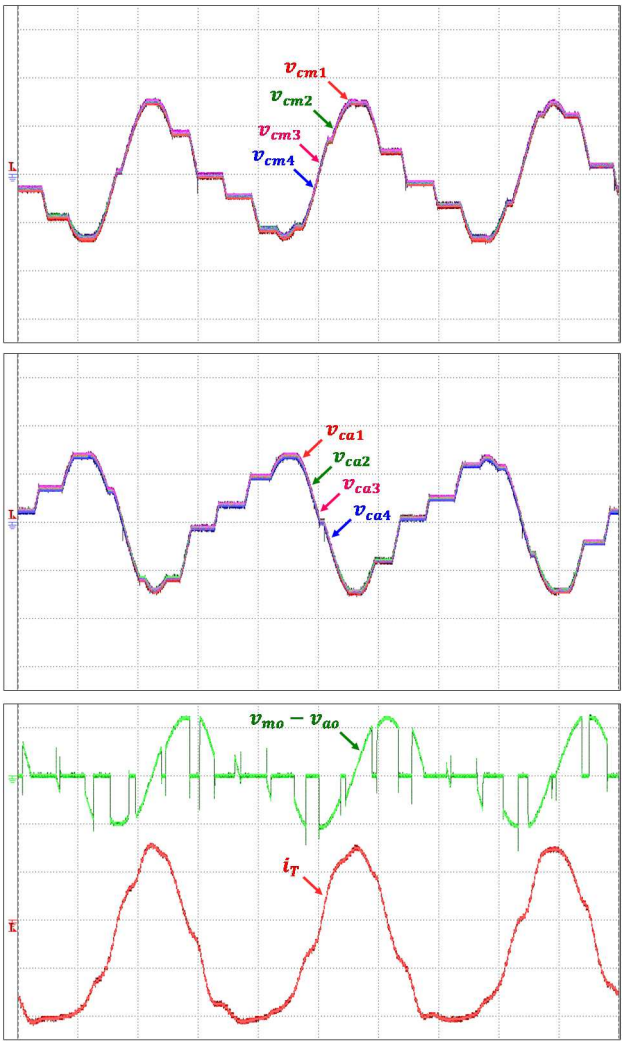


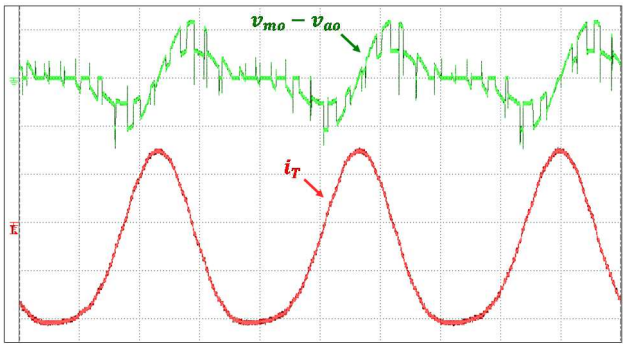
Fig. 6: Fourier spectrum of inductor voltage and test current

IV. Experimental Result

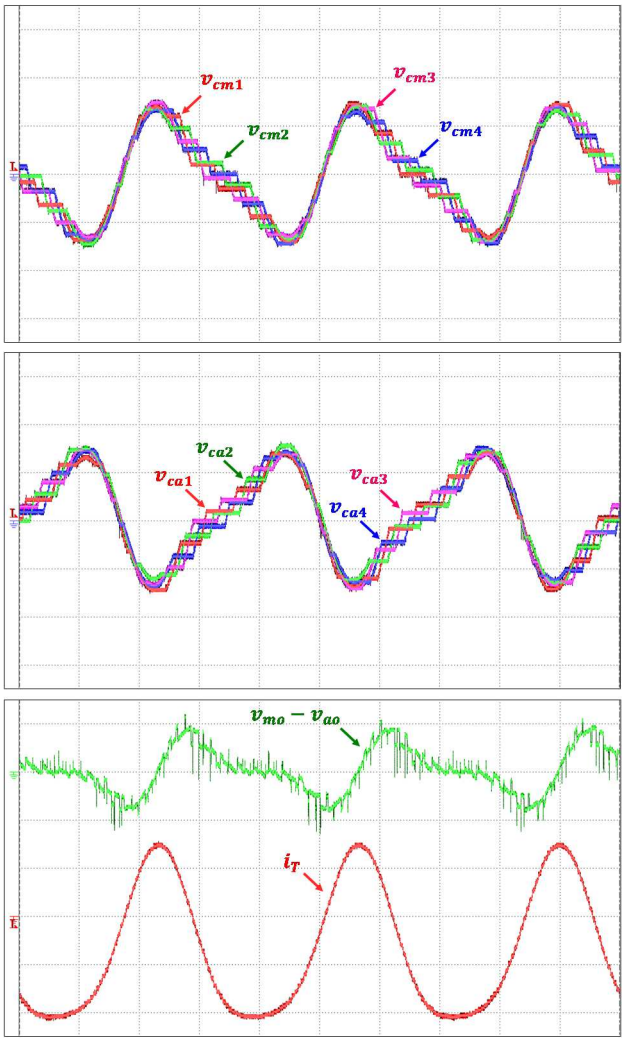
The hardware corresponds in Fig. 1 is implemented in a hardware in the loop of Typhoon HIL-402. The parameters used in the experiment are the same to those of the simulation. Fig. 7 shows each submodule voltage of main and auxiliary valves, inductor voltage, and test current in case of carrier phase shift of 0°, 180°, and 90°. Each waveform is similar to that of the simulation results.



(a) In case of 0° carrier phase shift



(b) In case of 180° carrier phase shift



(c) In case of 90° carrier phase shift

Fig. 7: Each submodule voltage, inductor voltage, and test current ($v_{cm1}, v_{cm2}, v_{cm3}, v_{cm4}$: 50 [V/div], −2 [kV] offset, $v_{ca1}, v_{ca2}, v_{ca3}, v_{ca4}$: 50 [V/div], −2 [kV] offset, $v_{mo} - v_{ao}$: 500 [V/div], i_T : 250 [A/div], 5 [ms/div])

V. Conclusions

This paper proposes a new valve test circuit for MMC based HVDC power conversion system. The proposed circuit can generate the test current having 2^{nd} harmonic and dc components as well as the fundamental component which satisfies the required clauses from IEC-62501. The

power rating of the dc power source for the test circuit can be dramatically reduced compared to that of the conventional test circuit providing fundamental test current component only because the voltage magnitude of the power supply of the proposed scheme can be reduced as small as 20% of the conventional test circuit in case of five submodules in a test valve.

The inverter switching stress also can be significantly reduced compared with the conventional test circuit having single phase inverter. The two phase inverter can be replaced with three phase or four phase inverter depending on the current level. The validity of the proposed scheme was verified through simulations and experimental results. It is expected that the proposed test circuit can be widely applied to the valve test with minimized power supply rating and reasonable switching stress in the field of high voltage application including HVDC and MVDC power system.

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