Determination of Optimal Associated Discrete Circuit Switch Model Parameters for Real-Time Simulation of Dual-Active Bridge Converters

Marija Stevic and Ravinder Venugopal
OPAL-RT Germany GmbH
Bucher Str. 100
90408 Nuremberg, Germany
Phone: +49 (0)911 38-44-52-02
Email: marija.stevic@opal-rt.com
URL: https://www.opal-rt.com/de/

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Keywords

≪Real-time simulation≫, ≪Dual Active Bridge Converter≫, ≪Discrete-time≫, ≪Field Programmable Gate Array (FPGA)≫, ≪DC-DC power converter≫.

Abstract

Real-time simulation of a Dual-Active Bridge (DAB) converter based on the Associated Discrete Circuit (ADC) switch model is considered in this work. The ADC switch model allows for efficient simulation as its topology is fixed regardless of the switch state. The main disadvantages of the ADC-based simulation of power electronics converters are virtual power losses and artificial oscillations following switching events, which might significantly deteriorate simulation fidelity. A suitable parameter for constant conductance of the ADC switch model should be selected to minimize virtual power losses and artificial oscillations. However, a constant conductance parameter that minimizes virtual power losses might result in a low degree of simulation fidelity in terms of transformer current for the case of the DAB converter. This paper demonstrates with a numerical example the inconsistency of the objectives when selecting an optimal constant conductance parameter for simulation of the DAB converter. To address the challenge, a Loss Compensation Algorithm (LCA) is utilized to minimize virtual power losses, while a method to determine a suitable ADC switch model parameter that ensures specified accuracy of the transformer current is derived analytically. Time-domain simulation results of DAB converter are provided for validation of the proposed method.

Introduction

Hardware-in-the-Loop (HiL) concept is widely used for testing and validation of devices in the context of research and innovation activities. Ongoing developments of novel control concepts for power electronics converters increasingly rely on the HiL testing to bridge the gap between simulations and the real-world conditions. The HiL testing of controllers allows for significantly wider range of testing conditions compared to hardware prototypes and simplifies testing procedures as safety measures are relaxed. Typically, in addition to the simulation of a power electronics converter that is controlled by an external controller, a RTS simulates the system surrounding the power electronics converter, that often represents a multi-converter system. High degree of fidelity of real-time simulation is of critical importance to ensure valid HiL testing. Applications of real-time simulation of Dual-Active Bridge (DAB) converters are in the context of multi-converter systems, such as Multi-Terminal Direct-Current (MTDC) grids [1] or Solid-State Transformers (SST) [2]. Real-time simulations are based on fixed-step solvers and the simulation time-step is determined considering the fastest system dynamics, including switching dynamics. To meet these timing requirements Field Programmable Gate Array (FPGA) platform is mostly required. One possible approach is to derive a mathematical model of a power electronics converter of interest and determine the custom implementation for FPGA platform while focusing on efficiency and system specifics of interest [3, 4]. The approach considered in this paper is a generic solver with the objective to provide the tradeoff between the simulation efficiency and model flexibility.

Suitable switch model is one of the key factors to enable model flexibility in terms of converter topologies, as well as model scalability in terms of number of converters to be simulated within the defined simulation time-step and with feasible memory requirements. Associated Discrete-Circuit (ADC) switch model [5] is proposed as a solution enabling fixed system matrix regardless of states of the switches and thus reducing memory and online computation demands. The equivalent circuit of the ADC switch model consists of a conductance and a current source connected in parallel, that represent an inductance for a switch in closed state and a capacitance for a switch in open state. If parameters are selected to obtain equal conductance parameter values for both switch states, the system matrix is constant for all combinations of switch states regardless of converter topologies. However, the ADC switch model introduces simulation inaccuracies in terms of virtual power losses and artificial oscillations following switching events. The degree of these inaccuracies depends on the conductance parameter of the ADC switch model that should be selected with respect to a specific application and simulation scenarios to ensure required simulation fidelity.

Several methods for selecting a suitable constant conductance parameter of ADC switch model to meet simulation fidelity requirements have been proposed in literature. This paper provides analysis of the ADC-based simulation of DAB converter topologies and discusses its simulation fidelity specific the the DAB topology. In this context, a suitable procedure to determine optimal conductance parameter is derived specifically for ADC-based real-time simulations of DAB converters. Validation is carried out and simulation fidelity is quantified based on a reference model with ideal switch model representation.

The paper is organized as follows. First, ADC switch model and the role of conductance parameter are introduced. Next, a single-phase DAB converter is introduced as a case study. Challenges specific to simulation of DAB converter topologies based on ADC switch model are described. Following this, a procedure for determination of optimal constant conductance parameter for simulation of DAB converters is derived. Validation and assessment are provided based on time-domain simulations of the described case study.

Associated discrete circuit switch model

The ADC switch model is proposed in the context of Fixed Admittance Matrix Nodal Method (FAMNM) for simulation of power electronics converters. If an ideal switch model is utilized, the admittance matrix varies depending on the states of the switches. The objective is to enable efficient simulation for a relatively large number of switches and independently of power electronics converter topologies. The ADC switch model allows for fixed admittance matrix, regardless of the switch states.

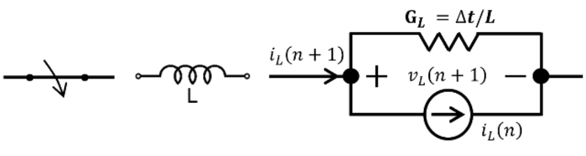

Fig. 1: ADC model of a switch in on-state

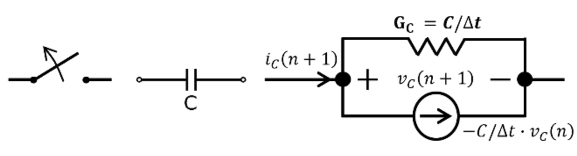

Fig. 2: ADC model of a switch in off-state

A switch is represented by an inductance in on-state and a capacitance in off-state [5]. The associated discrete circuits for an inductance and capacitance are illustrated in Fig. 1 and Fig. 2. For both states of the switch, an associated discrete circuit consists of a current source, connected in parallel to a conductance. Following the Euler Backward numerical integration method, the values of the conductance can be calculated based on the simulation time-step T_s and values of inductance or capacitance, while the value for current source is calculated based on the current or voltage quantity from the previous simulation time-step and thus represents the history of the element.

Fixed admittance matrix regardless of the states of the switches can be ensured if the value of the conductance in the ADC model of the switch is the same for both states of the switch. Namely, if conductance L_{sw} of the switch model in on-state and capacitance C_{sw} of the switch model in off-state are selected in a way that holds $G_s = T_s/L = C/T_s$, then the conductance has a constant value despite switching events and is known as a constant conductance parameter. The constant conductance parameter plays an important role in the overall power electronics converter model and might therefore significantly impact the simulation fidelity.

If a power electronics converter model with an ideal switch representation is considered as a reference benchmark, there are two effects of an ADC switch model that impact the simulation fidelity. First, the ADC switch model introduces virtual power losses. Namely, following a switching event, a capacitance (or an inductance) is removed from the circuit and replaced by an inductance (or a capacitance). In a standard FAMNM solvers the energy stored in a capacitance (or an inductance) disappears upon removing the element. As a result, power losses can be observed in the circuit and these losses are known as virtual because they are not related to actual power electronics converter behavior. The virtual power losses depend on the constant conductance parameter and the simulation time-step. Second, the ADC switch model introduces a parasitic inductance element of the value $L_{sw} = T_s/G_s$ when the switch is in the on-state and a parasitic capacitance element of the value $C_{sw} = T_s \cdot G_s$ when the switch is in off-state. As a result, artificial oscillations occur following the switching events and inaccurate dynamics of voltages and currents might be observed. In addition, if these parasitic elements are not sufficiently small compared to elements of the rest of the circuit, the dynamics of the overall circuit might be affected. The described behavior of the ADC switch model should be considered when selecting the constant conductance parameter value to ensure the simulation fidelity. In the following section a brief literature overview of methods and considerations for selecting suitable constant conductance parameter of ADC switch model is provided.

Constant conductance parameter of the ADC switch model

The ADC switch model provides substantial advantage for real-time simulation of power electronics converters; however, it potentially introduces simulation inaccuracies. The degree of the simulation inaccuracy depends on constant conductance parameter and the simulation time-step. The initial measure to ensure the simulation fidelity is to reduce the simulation time-step to the lowest value feasible for real-time execution of the system to be simulated. The size of the simulation time-step required to meet system and switching frequency dynamics is typically in the sub-microsecond range. Determination of the suitable size of the simulation time-step for real-time simulation of a single-phase DAB converters is described in [6] and it is out of the scope of this work. Here, the focus is on determining the suitable constant conductance parameter for a defined simulation time-step.

One approach to determining the constant conductance parameter value is to select parasitic inductance L_{sw} and parasitic capacitance C_{sw} of the ADC switch model based on the parameters of the physical switch [5]. Nevertheless, the actual parameters would typically require an extremely small simulation time-step, in the range of a few nanoseconds to several tens of nanoseconds, which is typically not suitable for a real-time execution of a moderate size of the system, even when a Field-Programmable Gate Array (FPGA) hardware is utilized.

Inaccuracies introduced by the ADC switch model can be determined by comparing the voltage and current quantities of the circuit simulated by employing the ADC switch model and the corresponding voltage and current quantities obtained from the simulation based on the ideal switch model. This allows the selection of constant conductance parameter values based on a trial-and-error approach, where multiple simulation runs are carried out for various values of the constant conductance parameter. In case of a multi-converter systems, different values of the constant conductance parameter should be considered for each of the converters. This approach provides reliable results as the reference model is utilized, however, it is time consuming.

One systematic approach for selecting the constant conductance parameter value is to minimize the virtual power losses. To do so, the power electronics converter topology and switching operation must be analyzed to derive the total energy loss depending on the switch parameters and current and voltage values of inductance and capacitance prior to switching events. Considering an arm of a two-level inverter, the optimal constant conductance parameter is equal to $G_{\mathrm{s}} = I_{\mathrm{rms}}/V_{\mathrm{dc}}$, where I_{rms} is the effective value of the load current and V_{dc} represents the dc-link voltage level [7]. However, selection of a constant conductance parameter that minimizes virtual power losses does not guarantee high degree of simulation fidelity of all converter quantities. Typical parameters of a DAB converter often result in the described inconsistency, which is shown in this work.

A method to select optimal constant conductance parameter based on the eigenvalues of the admittance matrix of the simulated system is proposed in [8]. The constant conductance parameters are determined based on an optimization algorithm with an objective to minimize the Euclidean distance between the eigenvalues of an admittance matrix obtained with ideal switch models and the eigenvalues of an admittance matrix obtained with ADC switch models. More precisely, a sum of Euclidean distances between the corresponding eigenvalues for all combination of switch states is considered as the objective function.

While the described method provides a holistic approach to selecting constant conductance parameter of an arbitrary converter topologies, this work focuses specifically on the DAB converter topology. In the context of DAB converters, a simple rule for determining optimal constant conductance parameter is derived and a high degree of simulation fidelity is achieved.

Simulation case study

The challenges of ADC-based simulations of DAB converter topologies are introduced based on a single-phase DAB converter topology illustrated in Fig. 3. The converter consists of two single-phase H-bridges, a bridge 1 with a dc-link voltage V_1 and a bridge 2 with a dc-link voltage V_2, interconnected by a single-phase two-winding power transformer with a total inductance L_{tot} and transformation ratio of $1:n$. Utilization of ADC-based switch model for real-time simulations of DAB power converters introduces several challenges that must be addressed to achieve high degree of simulation fidelity. To demonstrate the degree of impact of constant conductance parameter on the simulation fidelity, time-domain simulations of the DAB converter are conducted.

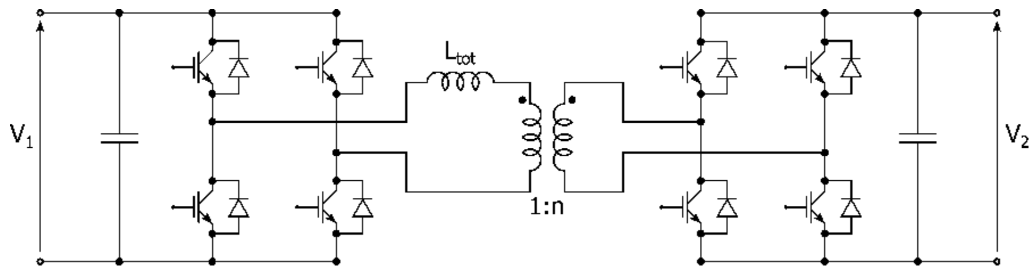

Fig. 3: Schematic of the single-phase dual-active bridge converter

Three simulation environments are utilized for simulation fidelity assessment and validation of the method for selecting a suitable constant conductance parameter. All simulation environments utilize fixed-step solver with Euler Backward numerical integration method. First, time-domain simulations of a DAB converter are conducted in an offline simulation environment to generate reference simulation results. Offline simulation environment utilized in this work is based on SimPowerSystems library in MATLAB/Simulink. Switching model of a DAB converter is based on the Resistive Switch Model (RSM), where a switch is represented with a two-valued resistance, $R_{\mathrm{on}} \approx 0$ when the switch is in on-state and $R_{\mathrm{off}} \gg 0$ when the switch is in off-state [9]. The parameters of the RSM are selected to ensure simulation results of negligible difference compared to the simulation with ideal switch model. Second, time-domain simulations in a simulation environment based on ADC switch model are conducted with various values of constant conductance parameter G_{s}. The ADC-based simulation environment that is utilized is electrical Hardware Solver (eHS) from OPAL-RT, that is a generic FPGA-based electromagnetic transient solver [10]. The eHS solver is accompanied with the LCA algorithm [11] that minimizes virtual power losses and artificial oscillations in ADC-based simulations. Two simulation environments are used, that are the eHS solver without the LCA algorithm and the eHS solver with LCA algorithm.

The parameters of a single-phase DAB converter used as a case study are listed in the Table I. The DAB converter is operated in open loop based on single-phase shift modulation [12], where the input and output bridges operate at a duty cycle of 50% and the converter is controlled through the phase-shift angle. The reference for the phase-shift angle used in the simulation is $\varphi = 18°$. The simulation time-step of $T_{\mathrm{s}} = 500\,\mathrm{ns}$ is selected as suitable for high-fidelity simulation the DAB converter [6].

Table I: Parameters of DAB converter

Parameter	Value
dc-link capacitance of primary side bridge	$C_1 = 2\,\mathrm{mF}$
dc-link voltage of primary side bridge	$V_1 = 5\,\mathrm{kV}$
dc-link capacitance of secondary side bridge	$C_2 = 2.5\,\mathrm{mF}$
dc-link voltage of secondary side bridge	$V_2 = 5\,\mathrm{kV}$
Transformer leakage inductance	$L_{\mathrm{tot}} = 750\,\mu\mathrm{H}$
Transformer winding resistance	$50\,\mathrm{m}\Omega$
Switching frequency	$2\,\mathrm{kHz}$

ADC-based simulation of a DAB converter

Time-domain simulation results for the parameters given in the previous section in offline simulation environment and in eHS simulation without LCA are illustrated in Fig. 4 and Fig. 5.

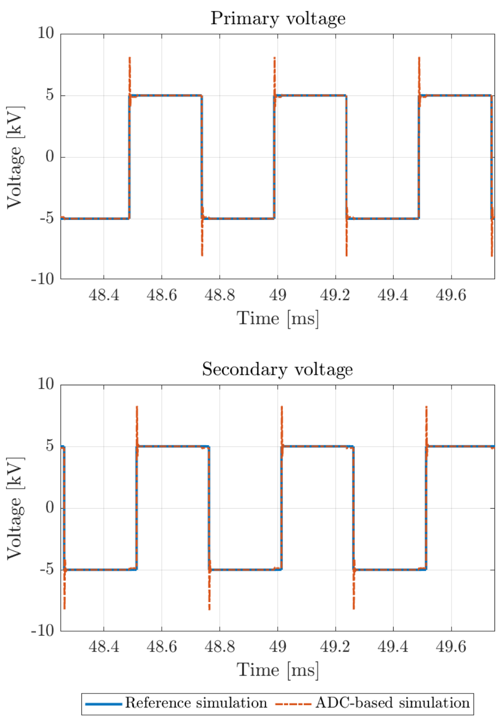

Fig. 4: Primary and secondary voltage in offline simulation and eHS simulation without LCA.

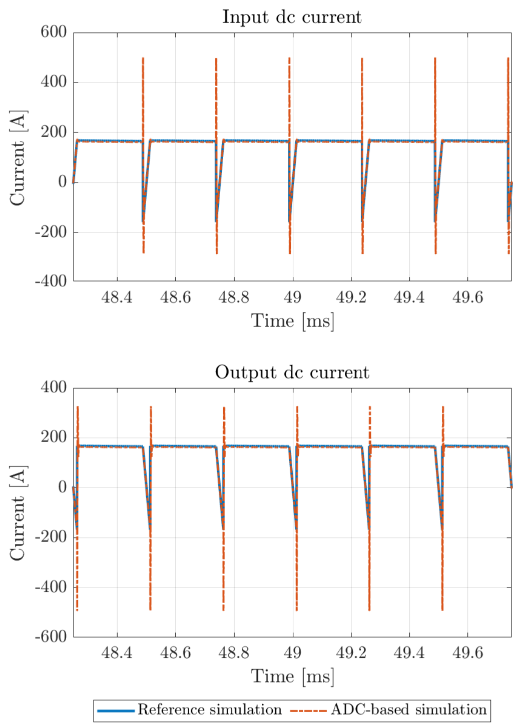

Fig. 5: Input and output dc current in offline simulation and eHS simulation without LCA.

The constant conductance parameter value of $G_s = 0.1\,\mathrm{S}$ is selected. Fig. 4 shows primary and secondary voltages of the DAB converter and indicates that voltage overshoots and artificial oscillations due to the ADC switch model are relatively large. Input and output dc currents shown in Fig. 5 demonstrate the same effect.

Another consequence of the ADC switch model are virtual power losses due to removal of the parasitic inductance or capacitance following the switching event. Table II gives values of power at the input and output of the DAB converters, as well as relative power losses. The difference between the power losses in the reference simulation and in the ADC-based simulation represents virtual power losses caused by the ADC switch model and it does not represent the actual converter behaviour. Therefore, these results might be misleading.

Table II: Power losses in eHS simulation without LCA

Parameter	P_{in}	P_{out}	P_{loss}
Reference simulation	752.8 kW	747.6 kW	0.69%
eHS without LCA	744.2 kW	716.8 kW	3.68%

In addition to the simulation fidelity issues related to virtual power losses and artificial oscillations, fidelity of the primary and secondary currents is affected by the parasitic inductances L_{sw} of the switches in on-state. Namely, the apparent inductance in the converter model in the ADC-based simulation is equal to the transformer leakage inductance L_{tot} increased by the parasitic inductances L_{sw} of all switches in on-state that are on the same current path. For the case of a single-phase DAB converter, the number of switches in on-state that should be considered when calculating the apparent inductance in the circuit is four.

Since the parasitic inductance is defined with $L_{\mathrm{sw}} = T_s/G_s$, the degree of the simulation fidelity depends on the constant conductance parameter G_s for the given simulation time-step. Fig. 6 shows primary currents in offline simulation and eHS simulation without LCA for the constant conductance parameter values of $G_s = 0.01\,\mathrm{S}$, $G_s = 0.03\,\mathrm{S}$ and $G_s = 0.1\,\mathrm{S}$. The simulation results show that the impact of the parasitic inductances on simulation fidelity in terms of the transformer current significantly depends on the constant conductance parameter.

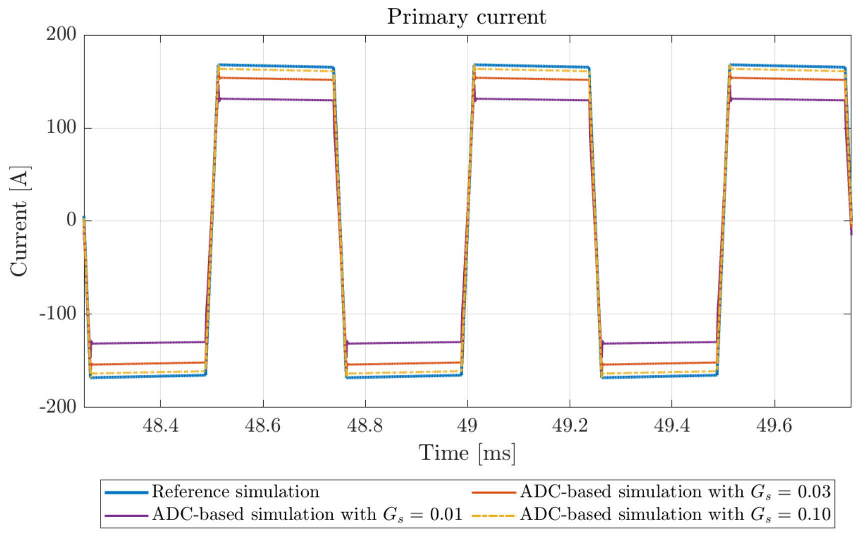

Fig. 6: Primary current in offline simulation and eHS simulation without LCA for Gs values of $G_s = 0.01\,\mathrm{S}$, $G_s = 0.03\,\mathrm{S}$ and $G_s = 0.1\,\mathrm{S}$.

To summarize, there are multiple objectives to be met when selecting a constant conductance parameter for ADC-based simulation of DAB converters. Virtual power losses, artificial oscillations and degree of simulation fidelity of transformer current depend on the constant conductance parameter. To characterize the dependency of virtual power losses and degree of simulation fidelity in terms of transformer current, time-domain simulations in eHS environment without LCA are conducted for the conductance parameter G_s in the range of values from $0.1\,\mathrm{S}$ to $0.4\,\mathrm{S}$. Simulation results are compared to the reference simulation in offline simulation environment and relative power losses and relative error of the primary Root Mean Square (RMS) current are calculated and illustrated in Fig. 7.

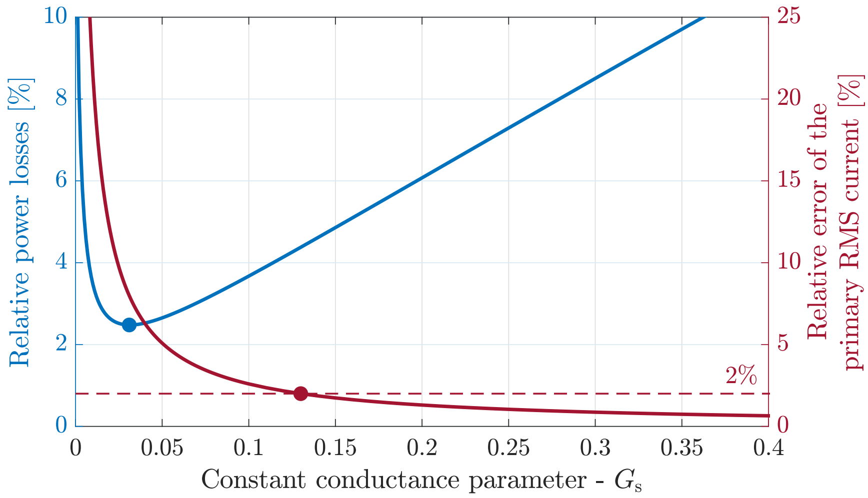

Fig. 7: Relative power losses and error of the primary RMS current.

The characteristic of relative power losses depending on the constant conductance parameter of the ADC switch model, in Fig. 7 shown in blue, is of typical shape for a converter topology consisting of 2-level arms. To determine the conductance parameter that minimizes virtual power losses, an approach derived in [7] for a two-level inverter can be followed. Following this method, ADC switch models are configured with constant conductance parameter values of $G_s = I_{rms}/V_1 = 0.03\,\mathrm{S}$. This result is consistent with the optimum obtained based on time-domain simulations and indicated with blue dot in Fig. 7.

However, the conductance parameter that minimizes the virtual power losses results in the relative error of primary RMS current above 5% as it is shown in Fig. 7 in red. Primary currents shown in Fig. 6 indicate significant difference of the current obtained in reference simulation and in eHS simulation with the conductance parameter of $G_s = 0.03\,\mathrm{S}$, that is calculated to minimize virtual power losses. This is the consequence of a relatively high ratio between the parasitic inductance of the ADC switch and the transformer leakage inductance. As it can be observed in Fig. 6 and Fig. 7, to achieve higher degree of simulation fidelity in terms of the transformer currents, a higher value of constant conductance parameter should be selected. For example, to achieve a relative error of the primary RMS current of 2%, the constant conductance parameter should fulfill the condition $G_s \geq 0.13\,\mathrm{S}$. However, this in turn results in relative power losses above 4%. The following section addresses the challenge of selecting optimal conductance parameter for ADC-based simulation of DAB converters in the context of conflicting objectives as described above.

ADC-based simulation with Loss Compensation Algorithm

Loss Compensation Algorithm (LCA) [11] is developed to minimize virtual power losses and artificial oscillations in ADC-based simulation of power electronics converters. The idea behind LCA is to properly initialize current and voltage values of the inductance and capacitance of the ADC switch model following switching events. Therefore, energy stored in the capacitance or inductance of the ADC switch model does not disappear and voltage and current states are not initialized with zero values each time the switch state is changed. The LCA is fully embedded in the eHS [10] and implemented for FPGA-based real-time simulation.

Assessment of the LCA in the context of simulation of DAB converters is illustrated in Fig. 8. First, relative power losses are significantly reduced and the values range between 0.75% and 0.95%. Note that relative power losses in the reference simulation are $P_{\mathrm{loss}} = 0.69\%$, as given in Table II. Therefore, LCA ensures high degree of simulation fidelity in terms of relative power losses almost independently from conductance parameter values.

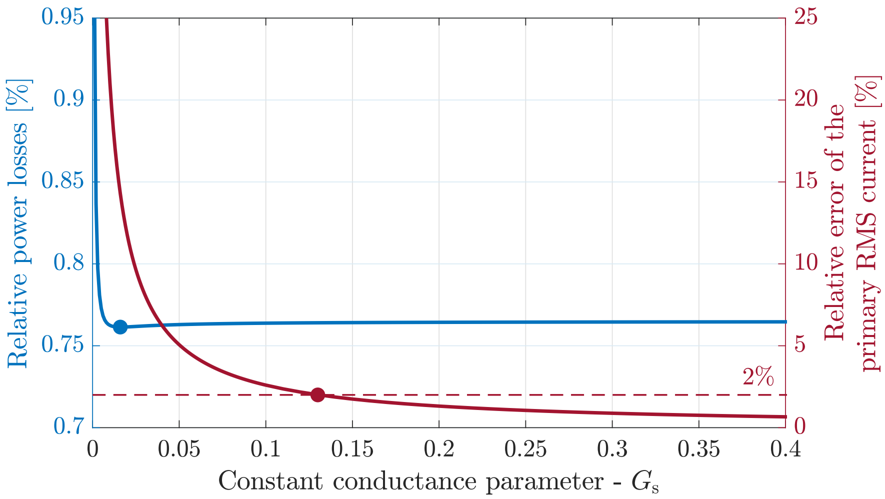

Fig. 8: Relative power losses and error of the primary RMS current with LCA.

Relative error of the primary RMS current is shown in red in Fig. 8. As expected, LCA does not improve this error, since this is the consequence of the parasitic inductance of the ADC switch model, which is the same regardless of the LCA. However, since relative power losses significantly reduced across the entire range of constant conductance parameter, the parameter can be selected to met the requirement for the relative error of the primary RMS current. The following subsection provides a simple rule to determine a suitable ADC switch model conductance parameter that meets a maximum error constraint of the transformer current.

Determination of the ADC switch model parameter

The current in a single-phase DAB converter with the same input V_{in} and output voltage output V_{out} levels is defined by Eq. 1.

$$I = \frac{V_{\mathrm{in}}\left(1 - \frac{\varphi}{\pi}\right)\frac{\varphi}{\pi}}{2 f_{\mathrm{sw}} L} \tag{1}$$

where φ denotes the phase-shift angle expressed in radians, L represents the total leakage inductance and f_{sw} refers to the switching frequency. As already described, the main source of fidelity degradation in terms of relative error of primary RMS current originates from the parasitic inductance of the ADC switch model. To characterize the degree of fidelity degradation in this context, the derivative of the converter current given by Eq. 1 with respect to the inductance value is derived as given in Eq. 2.

$$\frac{\mathrm{d}I}{\mathrm{d}L} = -\frac{V_{\mathrm{in}}\left(1 - \frac{\varphi}{\pi}\right)\frac{\varphi}{\pi}}{2 f_{\mathrm{sw}}} \cdot \frac{1}{L^2} \tag{2}$$

Next, the relative error of the DAB converter current $I_{\mathrm{err}}^{\mathrm{rel}} = |\Delta I / I|$ can be expressed by Eq. 3.

$$\left|\frac{\Delta I}{I}\right| = \left|-\frac{\Delta L}{L}\right| \tag{3}$$

The absolute error of the apparent inductance is equal to the total inductance of four parasitic inductances of ADC switches connected in series and is given by Eq. 4.

$$\Delta L = 4 \cdot L_{\text{sw}} = 4 \cdot \frac{T_{\text{s}}}{G_{\text{s}}} \tag{4}$$

If a constraint for maximum of the relative error of RMS current is defined $I_{\text{err,max}}^{\text{rel}} = 2\%$, the condition for parameters to satisfy this constrainet is given by Eq. 5.

$$\frac{1}{L} \cdot 4 \cdot \frac{T_{\text{s}}}{G_{\text{s}}} \cdot 100\% \leq I_{\text{err,max}}^{\text{rel}} \tag{5}$$

Finally, for a defined simulation time-step, the condition for constant conductance parameter is expressed with Eq. 6.

$$G_{\text{s}} \geq \frac{4T_{\text{s}}}{L} \cdot \frac{100\%}{I_{\text{err,max}}^{\text{rel}}} \tag{6}$$

In this context, the smallest value of G_{s} that satisfies the constraint for the relative error of the current should be selected. The reason is to minimize the size of the capacitor in off-state and therefore minimize its impact on the rest of the system.

Simulation results

Conductance parameter that satisfies the constraint given by Eq. 6 is equal to $G_{\text{s}} \geq 0.13\,\text{S}$, which is consistent with the fidelity assessment provided in Fig. 8. Simulation results in eHS environment and LCA with the specified value of the conductance parameter are provided in Fig. 9 and Fig. 10. Voltages and currents indicate high degree of simulation fidelity.

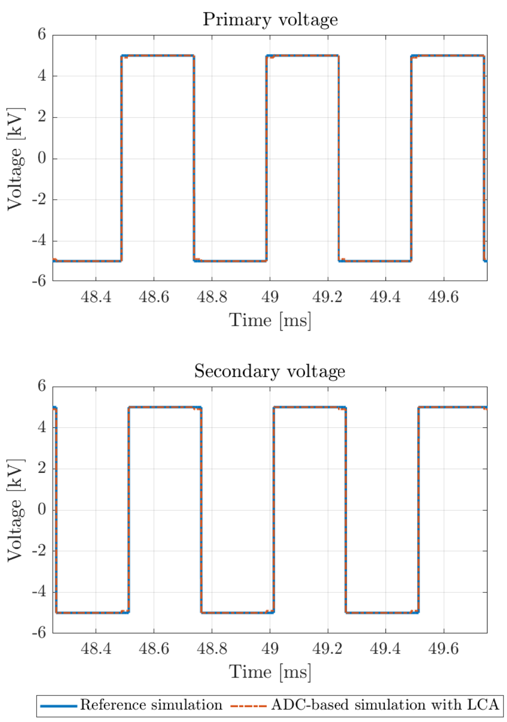

Fig. 9: Primary and secondary voltage in offline simulation and eHS simulation with LCA.

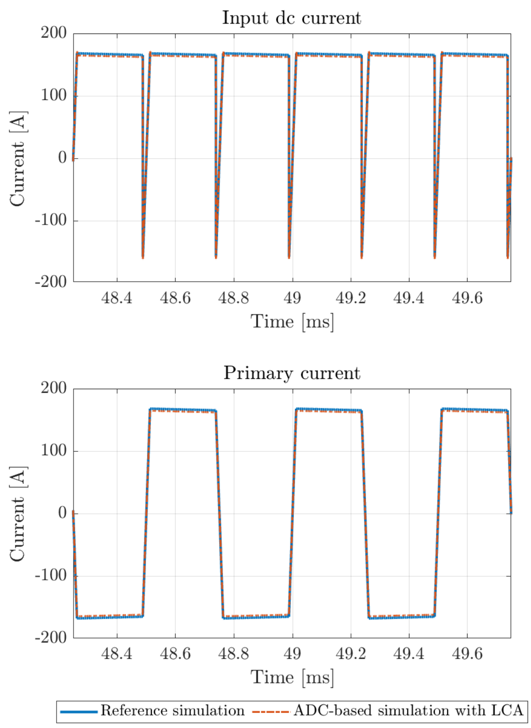

Fig. 10: Input and output dc current in offline simulation and eHS simulation with LCA.

Conclusion and outlook

The ADC switch model has been introduced and its advantages for FPGA-based real-time simulation due to its simplicity and computation efficiency have been outlined. The importance of constant conductance parameter value for simulation fidelity has been described. Moreover, the challenges specific to simulation of DAB converter topologies based on ADC switch model have been discussed. In this context, the specific characteristics of the DAB converter must be accounted for when determining the suitable constant conductance parameters.

As demonstrated based on the numerical example, the method to select constant conductance parameter values based on the minimization of the virtual power losses of each of the H-bridges might result in parasitic inductance values that are relatively large compared to the transformer leakage inductance. To address this challenge, a Loss Compensation Algorithm (LCA) is utilized to minimize virtual power losses, while a method to determine a suitable ADC switch model conductance parameter that meets a maximum error constraint of the transformer current is derived analytically. Finally, the procedure for determination of optimal conductance parameter values of ADC switch models for the case of DAB converters is validated based on the concrete example and time-domain simulations.

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