Real-time Temperature Estimation of SiC MOSFETs Using Gate Voltage at Zero-current Switching for Inverter Applications

Raul R. Rodriguez G., Mahfuzul Islam, Takashi Hisakado, and Osami Wada
Department of Electrical Engineering, Graduate School of Engineering, Kyoto University, Japan

***Abstract*—Nowadays, temperature monitoring has gained great focus to improve their reliability. For SiC MOSFETs, thermal sensitive electrical parameters (TSEP) are being widely investigated because of their ease of measurement and implementation. However, implementing such methods faces several critical problems, such as the ringing noise in the gate voltage waveform due to parasitic inductances and large output currents. This work proposes a gate voltage measurement method for inverter applications utilizing a zero-current switching (ZCS) period. We also propose slowing the gate switching speed during zero-current switching to obtain a stable gate voltage waveform for accurate estimation. We validate our proposed method by measuring the gate voltage waveforms of three commercial SiC devices through the double pulse test. Utilizing the plateau voltage, we demonstrate that temperature sensing can be performed within 5 % of error up to 100 °C temperature.**

***Index Terms*— Gate Resistance, Reliability, SiC MOSFET, TSEP,**

I. Introduction

With the recent attention to renewable resources, the presence of distributed power generation and electric vehicles have widely increased [1], causing an increase in research on reliability management for these systems. Single-phase full bridge inverters are proven to be one of the main components of these systems [2]. However, previous researches show that power device failure is the main cause of the failure of such systems, therefore increasing reliability issues [3]. One of the main factors affecting reliability is the fluctuation of junction temperature in the switching devices. This fluctuation slowly damages the device's junction, causing it to fail in the long run. [4]. Hence, temperature monitoring is necessary to manage the reliability of power devices [5]. Moreover, power inverters in power generation systems undergo a continuous operation regime, requiring real-time temperature monitoring [6].

On the other hand, the development of semiconductors has increased the usage of SiC MOSFETs in many high-power applications. SiC MOSFET's advantages over the typical Si MOSFET and Si IGBT reside in its high switching rate, smaller size, lower power loss, and wide bandgap, which allows the devices to work at higher temperatures [7]. This has caused high attention to temperature monitoring methods in SiC power devices [8]. Temperature monitoring methods can be classified into four categories: conduction contact-based, electro-thermal model-based, optical methods, and temperature-sensitive electrical parameter-based methods (TSEP) [9]. Conduction contact-based methods are invasive and slow in response, making them inappropriate for real time monitoring. Optical methods require unpacking the device, the implementation of thermal cameras, and the device to be painted in black. This results in an expensive method with a limited applicability. Electro-thermal models have low accuracy in aging devices and is difficult to update. TSEP method estimate temperature through measurement of parameters affected by the temperature. [10] Among these methods, TSEPs have proven to be less disruptive and more appropriate for real-time temperature estimation. However, the implementation of TSEPs faces accuracy problems because of the high ringing noise caused by parasitic inductances. As parasitic inductances are an inherent parameter of the power MOSFET packages, they cannot be eliminated. However, it is possible to mitigate their effect by reducing the switching speed, which can be achieved by increasing the device gate resistance. Fig. 1 shows the

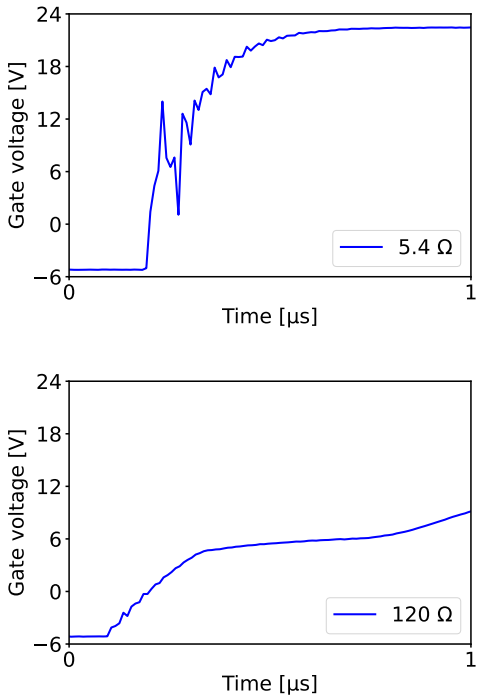
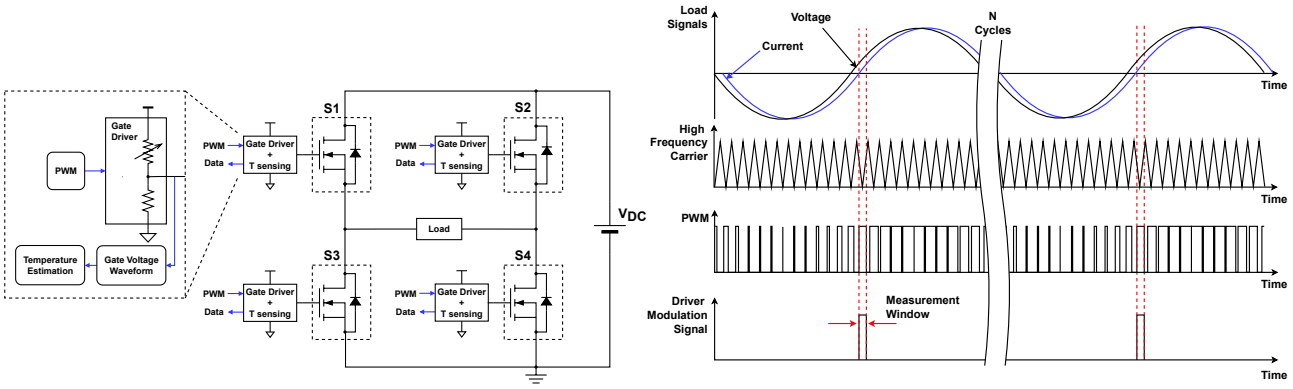


Fig. 1: Measured turn-on gate voltage waveform for a load Current of 0 A and supply voltage of 330 V.



(a) Gate-driving scheme **(b)** Zero-current switching

Fig. 2: Proposed gate-driving scheme for real-time temperature estimation.

turn-on gate-voltage at external gate resistance of 5.4 Ω and 120 Ω, for a supply voltage of 330 V, load current of 0 A, at 20 °C. When the driver resistance is 5.4 Ω, the effect of the parasitic inductance causes a large ringing in the plateau voltage. Moreover, this ringing increases at high switching frequencies and high load currents. On the other hand, a large driver resistance mitigates the effect of the parasitic inductance, allowing us to measure the gate voltage accurately. However, the application of a high gate resistance results in higher switching losses, compromising the design of converters in terms of efficiency and reliability. Among other TSEPs there are the switching rate and gate current peak. [10] The extraction of these parameters do not require a high gate resistance. However, the implementation of these measurements requires the application of high isolation to handle the high power side current, or additional measurement circuits.

II. Proposed Estimation Method

The proposed method utilizes the gate voltage plateau to estimate the junction temperature. Fig. 2 shows the gate-driving scheme, where a variable driver resistance slows down the switching speed during the measurement. The controller sets the driver resistance to a low value during normal operation and a high value during the measurement. In addition, we apply zero-current switching (ZCS) to avoid ringing caused by high load currents.

A. Miller Plateau Characteristics

This work focuses on the gate voltage Miller plateau during turn-on. Compared with other TSEPs, the gate voltage has the advantage of being measured on the gate driver, therefore requiring less isolation for measurement. Moreover, as demonstrated in [11], the plateau level has a negative dependency on the junction temperature, making it suitable for temperature estimation. This fact is confirmed in Fig. 3, where the gate voltage waveform is observed under zero current, for a supply voltage of 330 V at temperatures from 20 °C to 100 °C. Besides the plateau level, other TSEPs can be extracted from the Miller plateau is the plateau length. The general equation for the plateau length can be obtained by integrating Eq. (1), which is written considering the parasitic currents and the MOSFET working on the saturation region.

$$\int^{\mathrm{P}} \left(\frac{k}{2}(V - V_{\mathrm{T}})^2 - I\right) dt = (\mathrm{C_G} + \mathrm{C_S})\mathrm{V} + \mathrm{C_G} \int \mathrm{dV} \tag{1}$$

$$k = \frac{\mathrm{W}\mu\mathrm{C_{OX}}}{\mathrm{L}} \tag{2}$$

In Eq. (1) L is the plateau length, $\mathrm{C_G} + \mathrm{C_S}$ are the drain-gate and drain-source capacitances respectively. I is the load current, V_p is the plateau voltage, V_T is the threshold voltage, V is the supply voltage, and $\int \mathrm{dV}$ is the difference of the gate voltage between the end and the beginning of the plateau. The parameter k depends on geometry of the device and is expression is shown in Eq. (2), where μ is the electron mobility, $\mathrm{C_{OX}}$ is the oxide capacitance, W is the width and L is the length if the channel. Solving Eq. (1) is not easy because of the nonlinear relation of the plateau voltage, however, we can observe that there is influence from threshold voltage and electron mobility, and as observed in Fig. 3 it also decreases when the temperature increases.

The plateau slope is also a TSEP that can be extracted from the gate voltage. Contrary to Si MOSFETs, SiC MOSFETs plateau has a non-flat characteristic that has not been deeply studied. Assuming a linear behaviour of the slope and analysing Eq. (1), we observe a relationship between the slope, the threshold voltage, and the electron mobility. Moreover, as observed in Fig. 3, the slope also decreases with the temperature, making it a possible parameter for temperature estimation.

B. Driver Resistance Modulation

To properly observe the gate plateau, it is necessary to reduce the switching speed by increasing the driver resistance. High driver resistance compromises the efficiency of the converter. Therefore, a driver resistor modulation is required.

To implement this concept, the gate driver resistor is replaced by a variable resistor, as shown in Fig. 2. Then

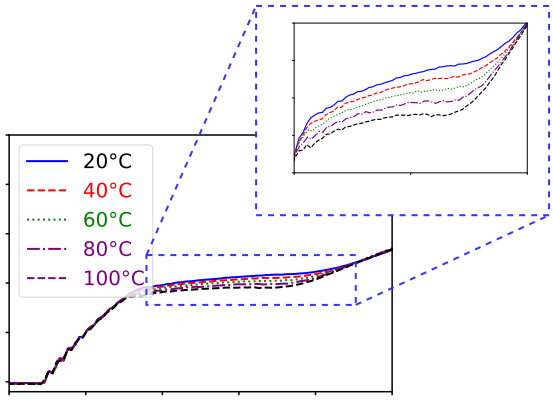


Fig. 3: Measured turn-on gate voltage waveform through double pulse test. at 20 °C and 100 °C for a load current of 0 A and supply voltage of 330 V.

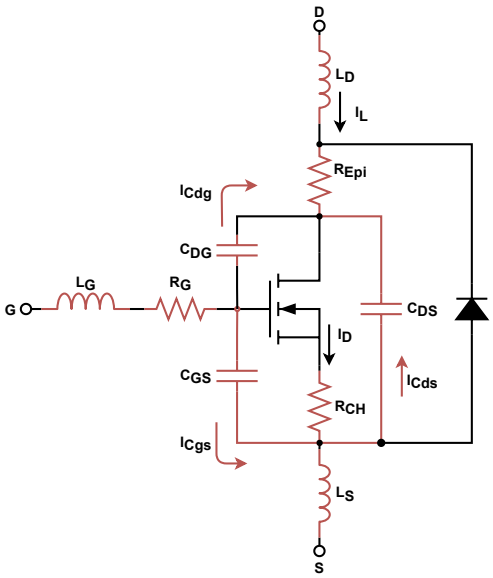


Fig. 4: MOSFET model including parasitic parameters.

the variable resistor is set to a large value during the gate voltage measurement, and to a low value during normal operation. We apply the resistance modulation for a period of only 1 μs every several minutes to minimize the switching loss. As observed in Fig. 1, 1 μs is enough to extract the plateau characteristics.

C. Zero-current Switching

Load current have a direct effect on the gate voltage. This relationship is commonly present through Eq. (3).

$$V = V_{\mathrm{T}} + \sqrt{\frac{2}{k} I} \tag{3}$$

However, to appreciate the relationship with the load current we must consider the parasitic parameters. Fig. 4 shows the MOSFET diagram including the parasitic parameters, along with the parasitic currents. By considering these currents we rewrite Eq. (3) into Eq. (4).

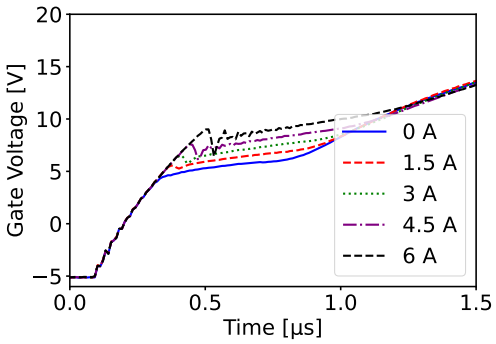


Fig. 5: Experimental turn-on gate voltage waveform at a supply voltage of 330V and 20 ∘C, under different load currents.

$$V = V_{\mathrm{T}} + \sqrt{\frac{2}{k}\left(I + I \left(1 + \frac{C_{\mathrm{S}}}{C_{\mathrm{G}}}\right)\right)} \tag{4}$$

This way is easier to notice the relationship between the load current and the plateau voltage. Since the output in inverters have a sine wave characteristic, the load current is constantly fluctuating. This fluctuation affects the plateau voltage, therefore requiring calibration. Moreover, a higher load current also causes a higher ringing on the gate voltage. When the load current is high, the drain current increases trying to reach the load current. This sudden current increase causes a high voltage drop in the parasitic source inductance L_S, generating ringing in the gate voltage. High gate resistance mitigates the effect of the ringing, however, it does not totally eliminates the ringing. This can be confirmed through Fig. 5, which shows the gate voltage at 330 V and 20 °C under different load currents. Same as the plateau level, the ringing increases with the load current reducing the accuracy of the temperature estimation, moreover, typical load in power applications are in the range of several amperes, causing a ringing large enough that the plateau can not be observed. Therefore, we propose zero-current switching (ZCS) method. The method consist in calculating the zero-cross of the load current and applying the driver resistance modulation at this point. To implement ZCS, the load characteristics must be known. For induction motors and distributed generation systems, the power factor is a known value used to calculate the phase difference between the reference signal and the load current. We use the phase difference in synchronization with the PWM to adjust the driver resistance to a high value for measuring the gate voltage. This concept is shown in Fig. 2b, where the modulation signal is send during the zero current.

III. Simulation Results

We test the driver modulation scheme and ZCS through simulation using HSpice. The simulation circuit is a single phase inverter as shown in Fig. 2a. We implement the gate resistance simulation through the circuit shown in Fig. 6, where the red inductance represents the parasitic

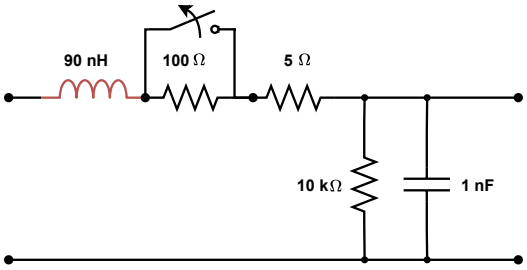


Fig. 6: Gate driver with resistance modulation model.

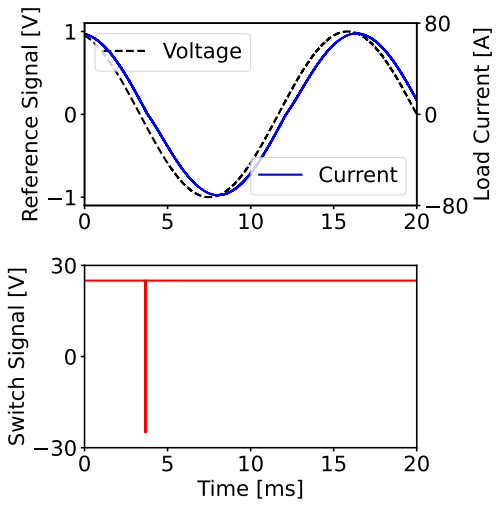
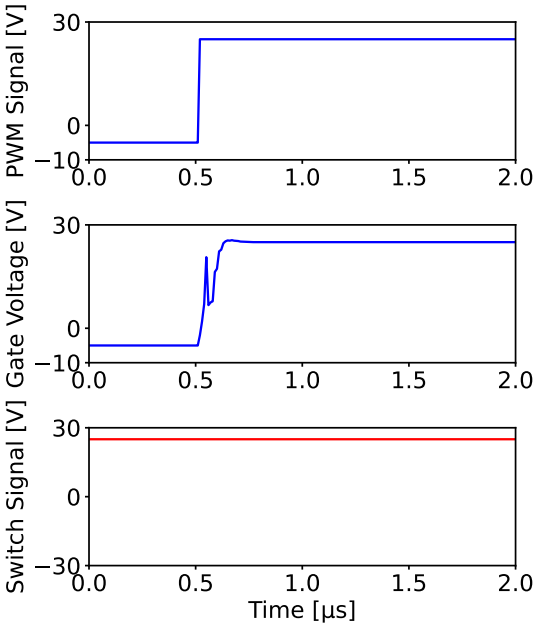


Fig. 7: Reference voltage, load current, and switch signal in a power inverter applying ZCS.

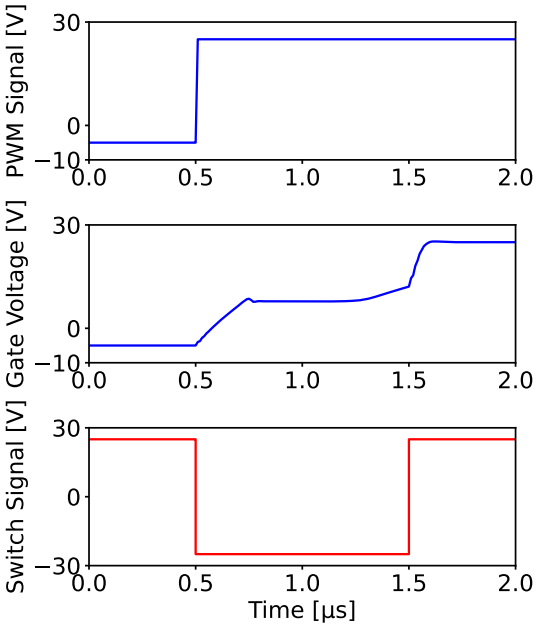
inductance of the driver. The parameters used in the gate driver were extracted from the model of a commercial gate driver, and the load parameters are based on a mid-voltage induction motor. The switch on the driver is normally on, causing a low gate resistance during normal operation. During temperature estimation, the controller calculates the zero current using the load power factor. Then, when the load current is zero, the switch opens, increasing the gate resistance to acquire the voltage waveform. The gate driver is supplied with a PWM signal, and the simulation parameters are shown in Table I. We implemented the switch signal by arbitrary behavioral voltage source, which is synchronized with the PWM.

Fig. 7 shows the simulation results of the ZCS. Fig. 7 shows the reference signal, the load current and the signal send to the switch for resistance modulation. As the load is based on a mid-voltage induction motor, the power factor is high, and the phase difference between the reference voltage, and the load current is small. We observe that when the current crosses the zero point the switch voltage drops, opening the circuit and increasing the driver resistance.

Fig. 8 shows the PWM signal, the gate voltage, and the switch signal during normal operation and during ZCS. Fig. 8(a) shows the gate voltage on S1 during normal operation when the load current crosses the zero amperes. We observe the ringing caused by the parasitic parameters



(a) Signals during normal operation.

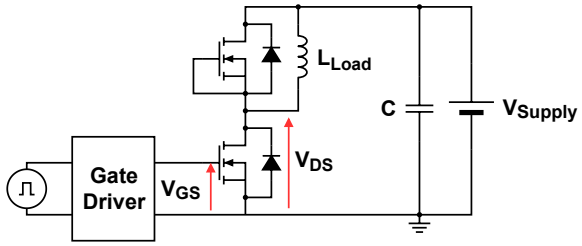


(b) Signals during temperature estimation.

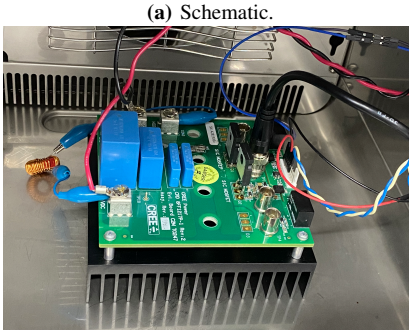
Fig. 8: PWM signal, gate voltage, and and switch signal waveforms at zero current during normal operation and temperature estimation.

TABLE I: Simulation parameters.

$V_{\text{Supply}}[V]$	I_{Load} [A]	L_{Load} [mH]	R_{Load} [Ω]	Carrier Frequency [kHz]	Reference Frequency [Hz]	MOSFET Model
500	70	3.7	6.6	100	60	SCT3022KL Rohm [12]



(a) Schematic.



(b) Measurement setup in a temperature chamber.

Fig. 9: Measurement setup for double pulse test under different temperatures.

during the high-speed turn-on, and a high-peak on the gate voltage caused by the parasitic parameters. Fig. 8(b) shows the gate voltage on S1 during ZCS. We confirm the resistance modulation through the signal input on the switch, and observe the voltage plateau caused by the slow switching. Simulation results show that is possible to achieve the gate the gate driving scheme to reduce the switching speed while applying ZCS. However, it is necessary to apply the resistance modulation twice in a cycle to extract the data of the four MOSFETs.

IV. Experimental Results

We use the double pulse test (DPT) to test the temperature estimation method. Fig. 9(a) and Fig. 9(b) show the experiment layout and the DPT schematic respectively. The experiment parameters are shown in Table II.The first pulse is used to emulate the zero current, and three devices were measured. The device temperature is set by placing the evaluation board inside a temperature chamber and adjusting the temperature from 20 °C to 100 °C. We acquire the gate voltage waveform from the devices and through a fitting of the waveform we extract the plateau level, length, and slope. Fig. 10 shows the measured data of the plateau level, length, and slope at 20, 40, 60, 80, and 100 °C, for the devices. In Fig. 10(a) we observe a linear relationship between the plateau level and the temperature, we also observe some different among the three devices caused by the variation in the mobility and the threshold voltage. Fig. 10(b) on the other hand, show a linear characteristic on DUT 1, but have some dispersion in other devices, however, as observed in Fig. 3, we can confirm that plateau length decreases when the temperature increases. Finally, Fig. 10(c) shows the relationship between the plateau slope and the temperature. This characteristic was extracted assuming a linear plateau slope, and we can confirm that characteristic also decreases with the temperature, but not in a linear way. Among the three measured quantities, the linear characteristic of the plateau level along with it low dispersion, makes it the best candidate for temperature estimation. Therefore, only the plateau level was used for temperature estimation. Fig. 11 shows the sensing error for the plateau level after a two-point calibration at 20 and 100 °C. The maximum error of 5%. Aging and damage in power devices result on higher operation temperatures, therefore the temperature estimation at high temperatures must be minimum. The proposed method uses the maximum temperature as calibration point the minimum and maximum temperature, reducing the estimation error around the temperature of interest. In addition, a maximum error of 5% is small enough to avoid misinterpretation on the device status .

V. Conclusion

This work proposed a temperature estimation method using the gate voltage plateau level during turn-on in power inverters. To assure a high estimation accuracy and low switching losses, a driver resistance modulation was implemented together with ZCS. The gate voltage is acquired during a measuring window of 1 μs, minimizing the switching loss. We tested the driver resistance scheme and the ZCS through simulation, confirming the effects of the resistance modulation on the gate voltage. We also tested the proposed estimation method experimentally using the double pulse test. We extracted the plateau level, length, and slope from the gate voltage assuming a lineal model. Among the three parameters, the lineal relation between the plateau level and the temperature, and its low dispersion in the results makes it the best candidate for temperature estimation. We estimated the temperature using 2-point calibration, achieving a maximum error of 5 %. Further work must include experimental results on the implementation of the driver modulation and ZCS in inverter applications.

References

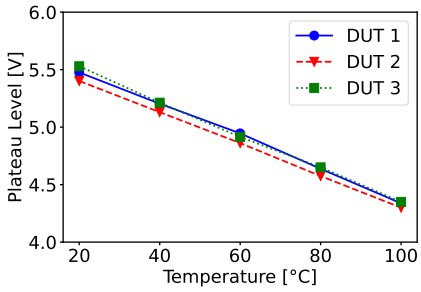
[1] X. Zhang and H. Liao, "Reliability assessment of power converters with partial redundancy and variable power distribution," in *Asian Conference on Energy, Power and Transportation Electrification (ACEPT)*, 2018, pp. 1–5.

[2] B. Backlund, M. Rahimo, S. Klaka, and J. Siefken, "Topologies, voltage ratings and state of the art high power semiconductor devices for medium voltage wind energy conversion," in *IEEE Power Electronics and Machines in Wind Applications*, 2009, pp. 1–6.

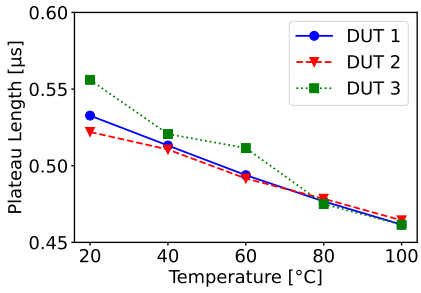
[3] S. Jaiswal and G. Pahuja, "Effect of reliability of wind power converters in productivity of wind turbine," in *IEEE India International Conference on Power Electronics (IICPE)*, 2014, pp. 1–6.

TABLE II: Experiment parameters.

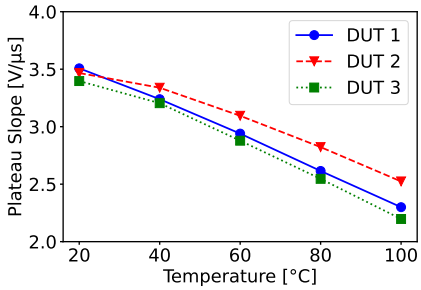
$V_{\text{Supply}}[V]$	I_{Load} [A]	L_{Load} [μH]	R_{Driver} [Ω]	T [°C]	MOSFET Model
330	0, 1.5, 3, 4.5, 6	220	120	20/40/60/80/100	SCT3022KL Rohm [12]
330	0	220	5.4	20	SCT3022KL Rohm [12]



(a) Plateau level.



(b) Plateau length.



(c) Plateau slope.

Fig. 10: Relation between measured TSEPs and temperature.

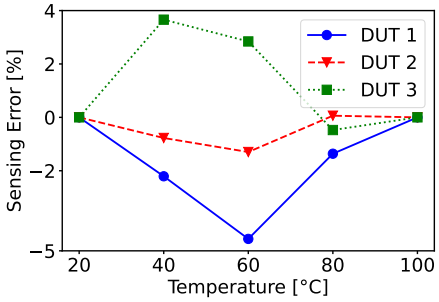


Fig. 11: Measured sensing error after a two-point calibration at 20 °C and 100 °C.

[4] A. V. Katore and A. P. Munshi, "Reliability evaluation of multi-level boost converter," in *International Conference on Smart Electric Drives and Power System (ICSEDPS)*, 2018, pp. 317–322.

[5] S. Peyghami, H. Wang, P. Davari, and F. Blaabjerg, "Mission profile based power converter reliability analysis in a DC power electronic based power system," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2018, pp. 4122–4128.

[6] Q. Niu and L. Wang, "Real-time inverter semiconductor die temperature estimation using inverter operating condition-based gate recurrent unit," in *IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2018, pp. 1–6.

[7] S. Sabri, E. Van Brunt, A. Barkley, B. Hull, M. O'Loughlin, A. Burk, S. Allen, and J. Palmour, "New generation 6.5 kV SiC power MOSFET," in *IEEE Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2017, pp. 246–250.

[8] H. Niu and R. D. Lorenz, "Evaluating different implementations of online junction temperature sensing for switching power semiconductors," *IEEE Transactions on Industry Applications*, vol. 53, no. 1, pp. 391–401, 2017.

[9] D. Zheng, Y. Kang, H. Cao, X. Chai, T. Fan, and P. Ning, "Monitoring of SiC MOSFET junction temperature with on-state voltage at high currents," *Chinese Journal of Electrical Engineering*, vol. 6, no. 3, pp. 1–7, 2020.

[10] Q. Zhang and P. Zhang, "An online junction temperature monitoring method for sic mosfets based on a novel gate conduction model," *IEEE Transactions on Power Electronics*, vol. 36, no. 10, pp. 11 087–11 096, 2021.

[11] J. O. Gonzalez, O. Alatise, J. Hu, L. Ran, and P. A. Mawby, "An investigation of temperature-sensitive electrical parameters for SiC power MOSFETs," *IEEE Transactions on Power Electronics*, vol. 32, no. 10, pp. 7954–7966, 2017.

[12] *N-channel SiC power MOSFET*, ROHM Semiconductors, 6 2018, Rev.005.