PCB Layer Optimization of Planar Medium Frequency Transformer for On-Board EV Chargers

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Keywords

« Planar magnetics», «Transformer», «Power density optimization», «Efficiency», «Power converters for EV»

Abstract

Planar medium frequency transformer (MFT) is a promising solution for on-board electric vehicle (EV) chargers, to achieve high power density and high efficiency. The trend towards higher power densities and higher efficiencies exposes a number of limitations on conventional litz wire transformers, especially for increasing the current density. Litz wire current density is limited by the temperature, due to poor thermal management capabilities. PCBs, however, have better thermal management capabilities, which allows for higher current densities. This paper optimizes planar MFT windings focusing on maximizing current density and the simplicity of the implementation. The losses, power density and thermal constraints are investigated and a pareto-front is created based on optimal solutions. High efficiency and power densities are achieved from 2D/3D FEM simulations. A solution within thermal constraints is selected and a prototype is built based on similar ratings. Tests with different current densities are carried out on the prototype and the temperatures are compared. The results verify that planar MFT with high current densities are feasible solutions for high efficiency and high power density MFTs.

Introduction

Compact and efficient power electronic converters are a prerequisite for E-mobility and particularly for on-board electric vehicle (EV) chargers [1], [2]. IEC60950 recommends that the off-grid power electronics converters might provide galvanic isolation in grid-connected mode operation for providing the required level of safety. Even though there are multiple ways for achieving galvanic isolation [3], magnetic transformer based isolation is much more popular owing to its reliable and low-loss operation. Isolated DC-DC converters with planar transformer are interesting solutions to satisfy the safety requirements as well as high efficiency and power density for on-board EV chargers [4]. A unique feature of the PCB windings is their ability to carry high current densities [5]. While, conventional litz wires suffer from poor thermal management capabilities. Litz strands insulator breakdown could easily propagate inside the entire winding and consequently it leads to medium frequency transformer (MFT) failure [6].

Planar transformers are used in a wide range of applications such as data centers [7] and on-board EV chargers where the power ratings are normally higher than 1 kW [8]. The existing trade-off between core losses and planar winding losses at different frequencies is addressed in [9] where the influence of the number of turns per PCB layer on the transformer total losses is also evaluated. Figure-of-merit method has been employed in [5] to achieve an integrated design of planar transformer and inductor in a DAB converter. However, the design variables are limited to magnetic field density B_m and current density J for a fixed integrated geometry of cores and windings. Moreover, low-power MHz range frequency planar transformers, in which volume is reduced effectively [10], are not suitable for high-power applications. Generally, the motivation to increase the frequency of the transformers is to reduce the volume according to the Faraday's Law of induction where the core volume reduces proportional to the inverse of frequency, i.e. $A_C \propto 1/f$. Increasing the switching frequency results in the higher parasitic capacities which might lead to lose of soft-switching and therefore impacts on the optimum design of the transformer [11]. Therefore, the correlation between current density and copper area, i.e. $A_{Cu} \propto 1/J$ is a motivation to increase the current density to reduce the copper volume. Nevertheless, thermal constraints severely restrict the increase of J and a careful design is demanded. Therefore, optimizing the current density is considered as an objective in this paper.
This paper presents an $\eta\rho$-brute-force optimization for planar transformer focusing on maximizing the current density which results in the reduced required copper area and therefore weight and volume of the used copper can be saved which is desirable for EV on-board charging. Analytical analysis is carried out to correlate the transformer parameter and thermal limitation to the Pareto fronts in the $\eta\rho$-plane. Considering level 1 on-board chargers, a 10 kW 400:400 V planar MFT is designed at 50 kHz for all simulation as well as experiment scenarios. Comprehensive analytical, 2D/3D FEM simulations, and experimental results show that high efficiency and power densities can be achieved at current densities up to 6 times of a conventional wounded MFTs. This paper is organized as follows. Section II explains the theoretical design approach. Loss equations and thermal equations are given to design the transformer. Section III described the optimization control variables and the creation of the $\eta\rho$-plane. Analysis for different numbers of layers per track, PCBs and a final pareto front with all solutions are given. The results of the pareto front are experimentally validated in section IV, where different currents and voltages are applied for thermal measurement at different current densities. Finally, Section V concludes this paper.

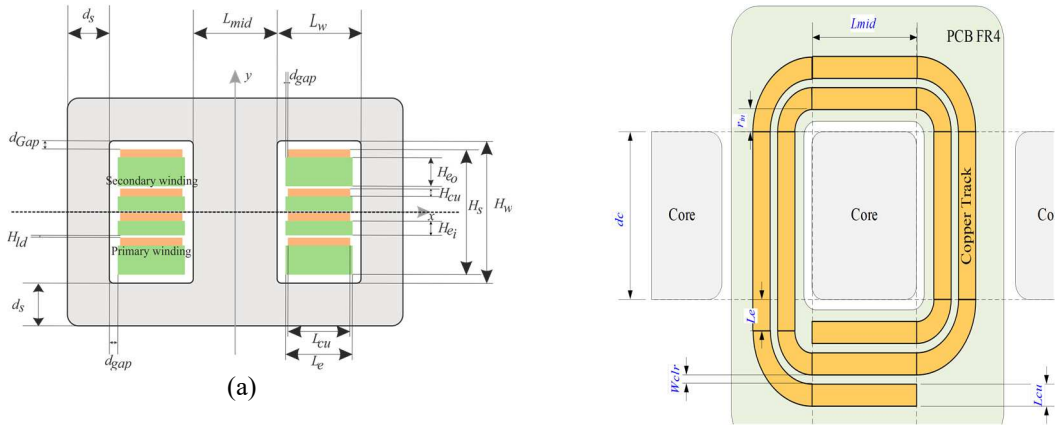


Fig. 1: Geometry of the MFT planar transformer: (a) core front view, and (b) one-layer PCB construction.

Theoretical Explanation of the Design

Fig. 1 shows the core and winding geometry of the planar MFT. Windings are constructed using PCB boards. Therefore, the number of turns can be identified by using the PCBs. The number of PCBs and the number of tracks per PCB determine the number of turns which must satisfy the Faradays law of the induction [12]. Theoretical basis to achieve a compact and thermally stable design of planar MFT are developed in the following. Power density (ρ) and efficiency (η) are defined as follows:

$$\rho = \frac{P_N}{V_T} \xrightarrow{(V_T = V_w + V_c)} \rho = \frac{P_N}{V_w + V_c} \quad \text{and} \quad \eta = \frac{P_N - P_{Cu} - P_{fr}}{P_N} \tag{1}$$

where P_N is the nominal output power, P_{Cu} is the winding losses and P_{fr} represents the core losses of the planar MFT. V_T, V_w and V_c are respectively total, winding and core volumes. Winding and core losses are analytically described by the following equation in [13]:

$$P_{Cu} = \rho_W V_W k_u J^2 \quad \text{and} \quad P_{fr} = V_C k_c f^{\alpha} B_{max}^{\beta} \tag{2}$$

Where ρ_W and k_u are the electrical resistivity of the conductor and the utilization factor of the window. P_{Cu} is explicitly given as a function of current density J. Steinmetz equation is used to analytically describe the core losses in equation (2), where k_c, α and β are constant given by the core manufacture. The power rating of the MFT planar transformer is related to the current density and geometrical dimensions of the winding as well as magnetic properties and magnetic core geometry by equation (3):

$$\frac{2P_N}{k_P} = k_V f B_{max} J k_f k_u A_c A_W \tag{3}$$

Where A_c and A_W are the magnetic core cross-section and core window area.

Thermal constraints

Temperature rise of the transformer, i.e. the difference between the hot spot and the ambient temperature can be estimated from the dissipated heat from the total surface area (A_T) of the transformer as in [14]. Therefore, thermal limits are also related to the $\eta\rho$ -plane as follows:

$$P_{Cu} + P_{fr} = h_t A_t \Delta T \tag{4}$$

Where ΔT and h_t are respectively the thermal transfer of the planar transformer. Then equation (4) can be inserted into equation (1):

$$\eta = \frac{\rho - h_t \frac{A_T}{V_T} \Delta T}{\rho} \tag{5}$$

To relate everything to the $\eta\rho$-plane the right side is divided by the transformer volume V_T. For further simplifications the thermal limit can be described with the thermal resistance R_θ.

$$h_t A_t \Delta T = \frac{\Delta T}{R_\theta} \xrightarrow{(1)} \eta = \frac{\rho - \frac{1}{R_\theta V_T} \Delta T}{\rho} = \frac{P_N - \frac{\Delta T}{R_\theta}}{P_N} \tag{6}$$

The thermal resistance for natural convection can be estimated with the core volume (V_C) [13]:

$$R_\theta = \frac{0.06}{\sqrt{V_c}} \xrightarrow{(1)} \eta = \frac{P_N - \frac{\Delta T \sqrt{V_c}}{0.06}}{P_N} \tag{7}$$

Winding losses

To optimize current density the winding losses needs to be considered. In planar MFT the winding losses can be estimated with the relation of AC resistance to DC resistance [15]:

$$\frac{R_{ac}}{R_{dc}} = \frac{\zeta}{2}\left[\frac{\sinh(\zeta)+\sin(\zeta)}{\cosh(\zeta)-\cos(\zeta)} + (2m-1)\frac{\sinh(\zeta)-\sin(\zeta)}{\cosh(\zeta)+\cos(\zeta)}\right] \quad (8)$$

Where $\zeta = H_{Cu}/\delta$ is the relation of copper thickness H_{Cu} and skin depth δ and m is the magnetomotive force (MMF) ratio at the layer.
For planar transformer the DC resistance can be assumed with the mean length of the track (MLT):

$$R_{dc} = \rho_{Cu}\frac{MLT}{H_{Cu} * L_{Cu}} \quad (9)$$

The MLT can be estimated with the following equation:

$$MLT = 2(d_C + 3L_{Cu} + L_{Cu}(N_{Tracks} - 1)) + L_{mid} \quad (10)$$

Where N_{Tracks} is the number of tracks per layer. The equation for MLT estimation is only a rough estimation and the accuracy of the equation depends on the design of the track. The total winding losses then results of the sum of the AC resistance of all n layers multiplied by current through the winding:

$$P_{Cu,} = \sum_{i=1}^{n} R_{ac,i} I_{rms}^2 \quad (11)$$

Where I_{rms} is the rms current through the winding, which is for a 400:400 V transformer the same in both windings.

$\eta\rho$-Brute-Force Optimization and Results

Comprehensive $\eta\rho$-brute-force optimization is carried out for the specifications mentioned in the introduction section. The simplest possible winding non-interleaved topology is considered. For the simulation different design scenarios are selected. Optimization control variables are copper thickness, current density, magnetic flux, number of PCB layers and number of tracks (turns) per PCB. Moreover, magnetic core geometry is freely swept according to the minimum and maximum planar core dimensions available in the market. The current density varied from 3 to 16 A/mm^2 in steps of 1 A/mm^2, the copper thickness from 0.105 mm to 0.28 mm in steps of 0.035 mm and the magnetic flux density from 0.1 to 0.3 T in steps of $(2^k/4) \times 0.1$ T with k from 0 to 3. Fig. 1 shows geometry of core and winding and their positions respective to each other.
To simply show the impact of optimization control variables on the objectives, i.e. η and ρ, a series of 2D-FEM simulations using Ansys Electronics is carried out for different number of PCBs and also tracks at different current densities. Fig. 2 (a), (b) and (c) show the impact of the number of PCB layers and tracks for J=16 A/mm^2. In this design, only the top layer is considered for copper tracks for maximizing the simplicity of implementation. As it can be seen maximum efficiency can be achieved for a specific number of tracks per layer and also there is a trade-off between efficiency and power density versus the number of PCBs. The overall results with variation of J, B_m and core and winding geometries for a fixed number of PCBs (i.e. 4) and tracks (i.e. 2) is shown in Fig. 2 (d).
Fig. 3 (a) illustrates the overall Pareto front obtained from the $\eta\rho$-brute-force optimization. Thermal limitations which are explained theoretically in $\eta\rho$-plane by equation (4) – (7). The Pareto front with thermal limitation is illustrated in Fig. 3 (b). Only the remaining solutions within thermal limitation are shown. Considering a minimum acceptable 99.5% for efficiency, a power density beyond 30 kW/l can be achieved. Utilizing a cooling system capable for removing larger amount of heat, lower efficiencies with higher power densities and higher current densities can be employed. Two solutions in the Pareto front are selected and the power losses distribution in the core and their current density are shown in Fig. 3 (c) and (d). For the same selections, detailed design parameters are presented in table I. As can be seen from this table both the designs are achieved at high current densities. These current densities are 3 times higher than a typical value for litz wires as in [16].

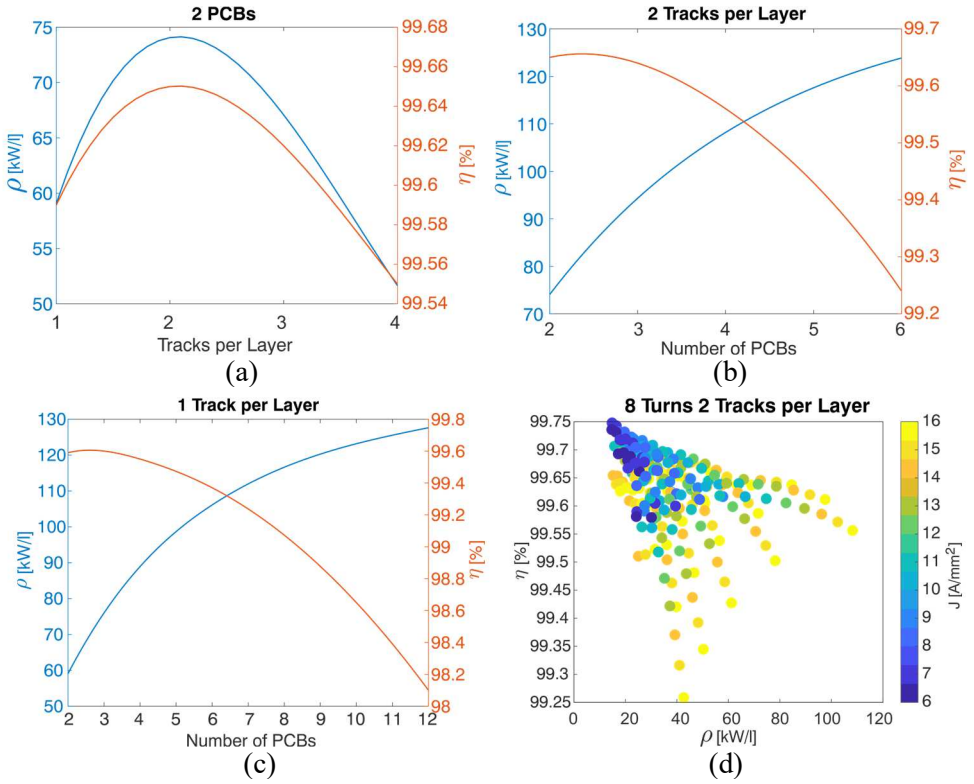


Fig. 2: Analysis for different number of tracks and PCBs at J=16 A/mm^2: (a) variation of efficiency and power density versus the number of tracks per layer, (b) variation of efficiency and power density with 2 tracks per layer versus the number of PCBs, and (c) variation of efficiency and power density with 1 track per layer versus the number of PCBs and (d) variation of copper thickness H_{Cu}, B_m and J.

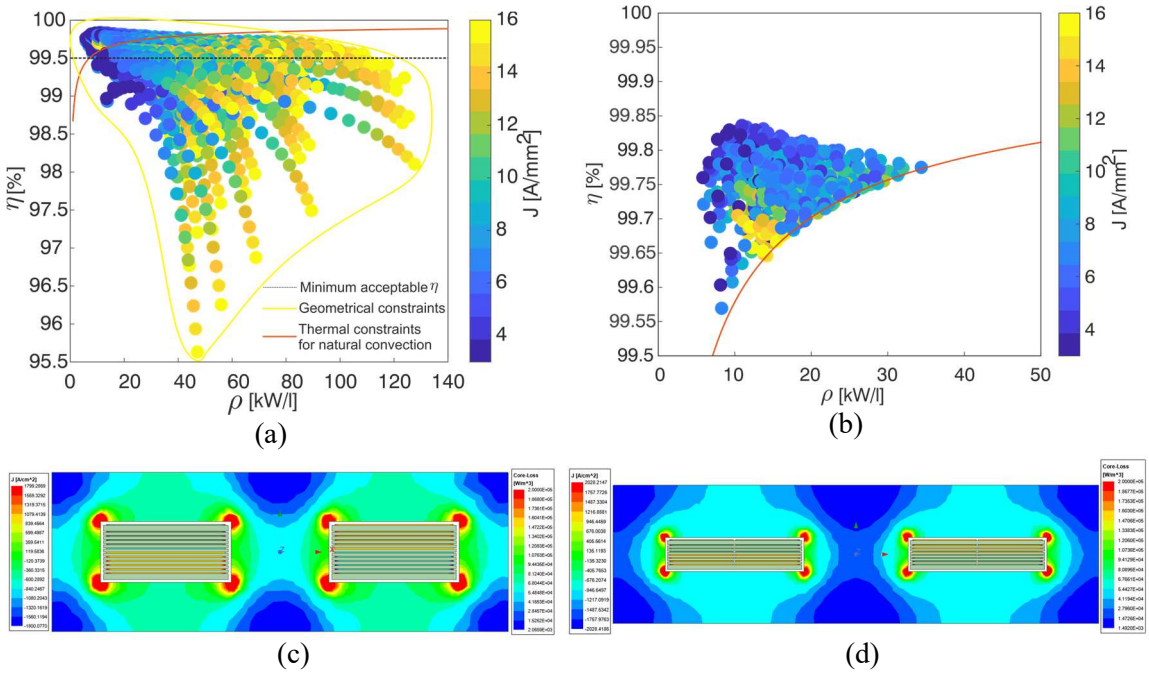


Fig. 3: Analysis for different number of tracks and PCBs: (a) comprehensive $\eta\rho$-brute-force optimization to form the Pareto front, (b) remaining Pareto front within thermal constraints, (c) selected 2D FEM design for 6 PCB layer per winding and 1 track per layer, (d) selected 2D FEM design for 4 PCB layer per winding and 2 tracks per layer.

Table I: Optimization results for 2 selected solution respect to $\eta\rho$ trade-off

Parameters	Variable	6 PCBs 1 Tracks	4 PCBs 2 Tracks
Volume [dm³]	V_T	0.2909	0.4484
Power density [kW/l]	ρ	34.38	22.30
Current density [A/mm²]	J	**7**	**8**
Efficiency [%]	η	99.77	99.72
Number of turns	T	6	8
Core width [mm]	d_C	135.9	123.62
Core length [mm]	L_C	78.43	112.92
Core height [mm]	H_C	27.29	32.12
Core window length [mm]	L_W	22.41	32.26
Core window height [mm]	H_W	10.49	7.93
Winding length [mm]	L_{Wi}	20.41	31.26
Winding height [mm]	H_{Wi}	4.425	3.47
Copper thickness [mm]	H_{Cu}	0.175	0.21
Copper width per track [mm]	L_{Cu}	20.41	14.88

Interleaving

For further current density optimization interleaving is considered. Interleaving the windings lowers the winding losses. The ratio of AC to DC resistance is shown in Fig. 4 (a). The ratio increases with increase of ζ, which with a constant δ is an increase of the copper thickness H_{Cu}. The higher the MMF the higher the ratio of resistance. The ratio of the AC to DC resistance can be interpreted as the losses in the windings. This is due to the fact, that the change of dc-resistance with the length L_{Cu} or the thickness H_{Cu} of the copper is lower than the change in the ratio due to the MMF. In Fig. 4 (b) the distribution of the MMF is shown for an example of 4 turns. When the windings are non-interleaved the MMF increases up to 4. Interleaving every layer will result in a constant MMF of 1.

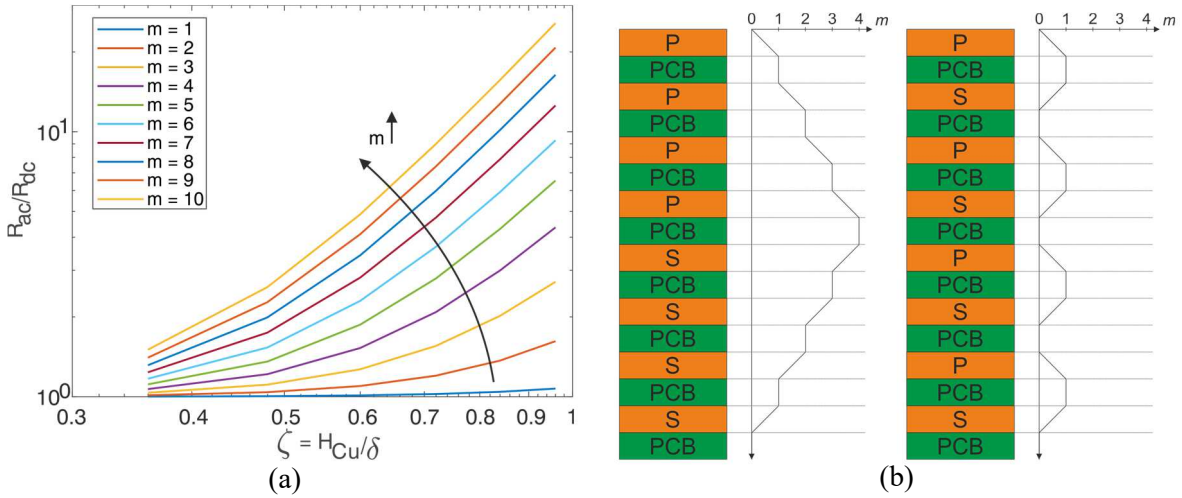
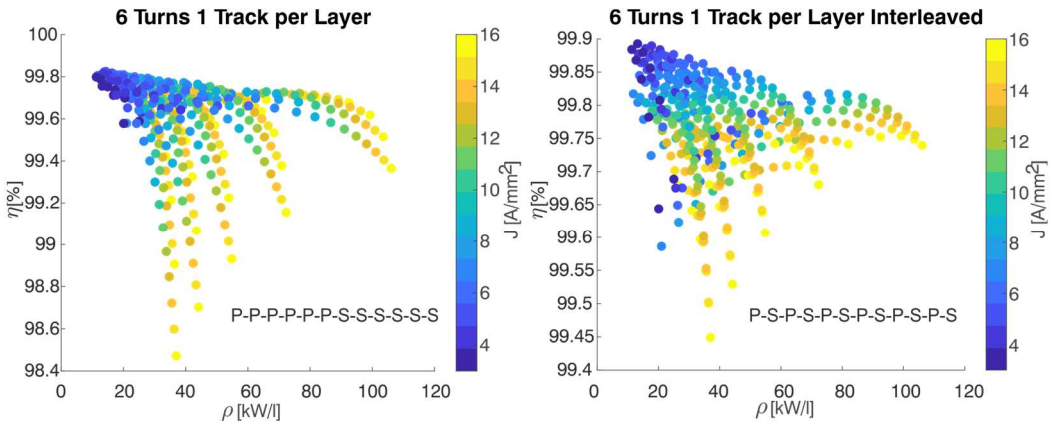


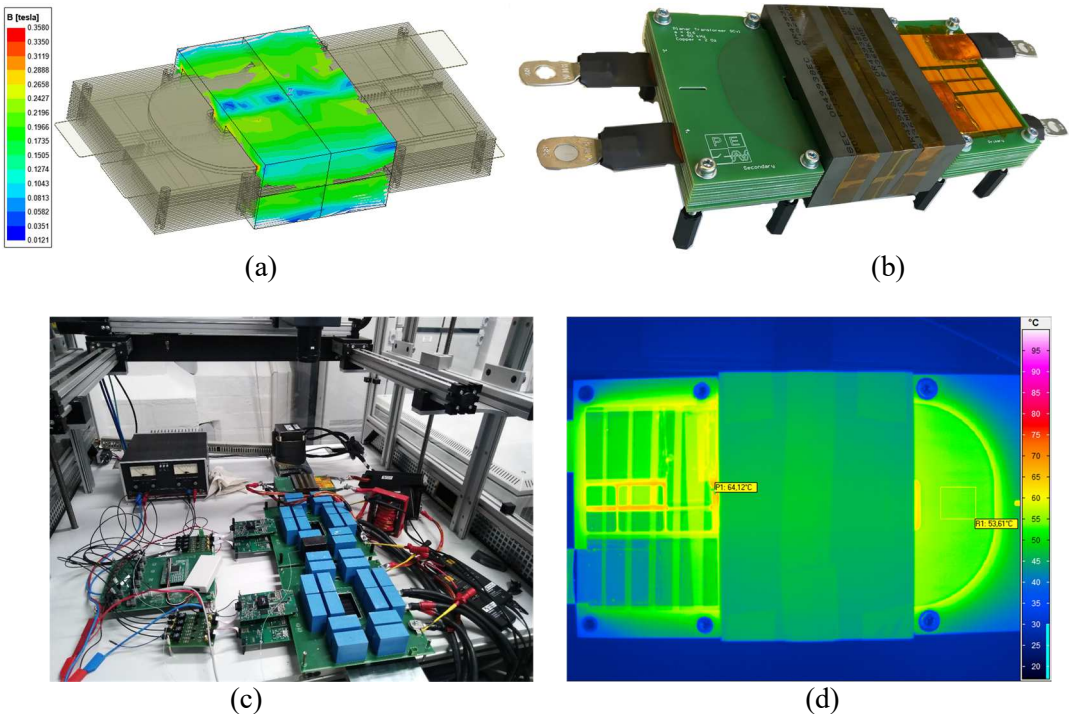
Fig. 4: (a) Ratio of AC to DC resistance as a function of ζ with the swept copper thickness H_{Cu} and (b) example of distribution of the MMF for 4 turns.

The effect of interleaving is shown for the example of 6 turns and 1 track per Layer in Fig 5. Fig. 5 (a) shows the pareto front of the non-interleaved structure and Fig. 5 (b) shows the pareto front of every layer interleaved structure (P-S-P-S-P-S-P-S). It is visible that the overall efficiency increases with interleaving the windings. The higher the copper thickness H_{Cu} the higher the increase of efficiency. This leads to an overall availability of higher current densities within thermal constraints.



(a) (b)

Fig. 5: Analysis of the effect of interleaving on the losses on the example of a 6 turn 1 track per layer transformer (a) non-interleaved and (b) interleaved P-S-P-S-P-S-P-S.



(a) (b)

(c) (d)

Fig. 6: Experimental results: (a) 3D FEM analysis of an example design to verify the performance, (b) developed hardware, (c) DAB converter prototype operated at 50 kHz and (d) Planar transformer at nominal current density in short circuit test.

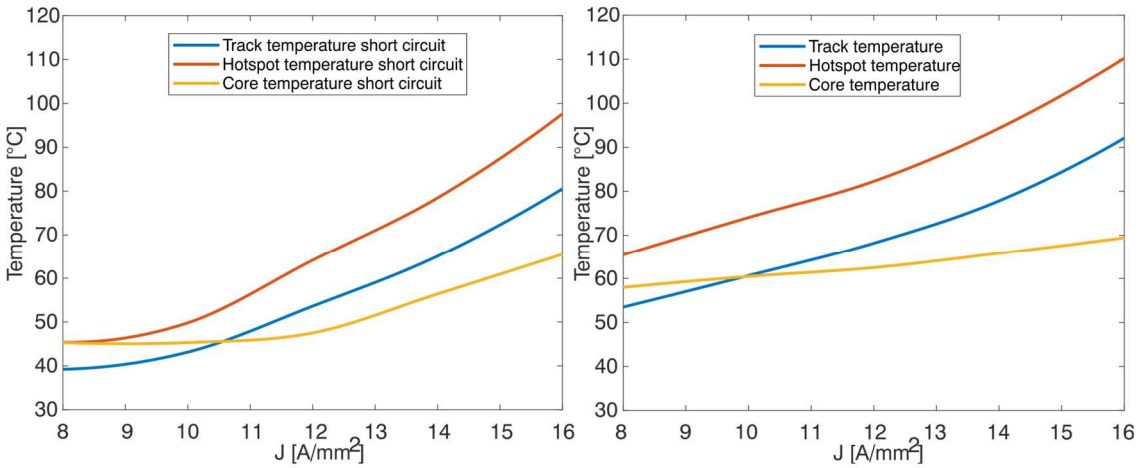
Experimental validation

Current density optimization is a trade-off between core losses and copper losses. In the following work different current densities are analyzed and compared to show the impact of current density in planar MFT. Fig. 6 includes the planar MFT prototype and the DAB converter setup for operating at 50 kHz. Fig. 6 (a) shows the 3D Ansys simulation of a simple planar MFT design with 1 track per layer and total of 6 turns where the magnetic field density is at linear range when excited with nominal quantities and approximately distributed uniformly. Fig. 6 (b) shows the built prototype with similar ratings as in table I and Fig. 6 (c) shows the planar MFT connected to the DAB converter. The ratings of the build prototype are given in table II. The design given in table II was selected, because lower copper thickness results in higher current density, to prove that high current densities are feasible for planar transformers. The winding structure of the build prototype is P-P-P-S-S-S-S-S-P-P-P. The temperature of the copper tracks at nominal current density is shown in Fig. 6 (d).

Table II: Parameters of the designed planar MFT

Parameters	Variable	6 PCBs 1 Track
Volume [dm³]	V_T	0.796
Power density [kW/l]	ρ	12.56
Current density [A/mm²]	J	**12**
Number of turns	T	6
Core width [mm]	d_C	75
Core length [mm]	L_C	102
Core height [mm]	H_C	40.6
Core window length [mm]	L_W	36
Core window height [mm]	H_W	26.6
PCB width [mm]	d_{PCB}	192.1
Copper thickness [mm]	H_{Cu}	0.07
Copper width per track [mm]	L_{Cu}	29.8

Fig. 7 shows the recorded temperature at different current densities in short circuit test (a) and with applied voltage (b). In the short circuit test the core temperature is due to the heat of the windings. At the nominal current density, the hotspot temperature reaches 64 °C. The temperature is increasing with the square of the current. In Fig. 7 (b) the temperatures are given with applied voltage, where the phase shift of the converter is hold constant. The current is increased through applying higher voltages. The temperatures at load is higher than in short circuit test, due to higher temperature in the core. It is visible, that in short circuit test and test at load that the temperature curves are very similar and the temperature difference between the track and hotspot to the core are in both case close together. This means, that with lower temperature in the core, higher current density within acceptable temperatures can be achieved. The build prototype achieves a current density of 5 times of litz wires and can achieve a current density up to 6 times of litz wire with lower applied voltage.



(a) (b)

Fig. 7: Experimental results of temperature measurement on different current densities: (a) temperature during short circuit test and (b) temperature with increasing voltage at higher current densities.

Conclusion

This paper presents a comprehensive optimization of planar MFT windings to achieve high efficiency and power density for on-board EV chargers. The behavior of the planar MFT design in $\eta\rho$-plane is evaluated theoretically and analytical equations for explaining the variation of efficiency versus power density as well as thermal constraints. Extensive $\eta\rho$-brute-force optimization is carried out for ratings of 50 kHz 400 V 10 kW based on 2D-FEM. Simulation results show the feasibility of designs with efficiencies and power densities beyond 99.5% and 30 kW/l, respectively. Moreover, a high level of

current density, up to 4 times of a conventional litz wire, can be applied to the planar MFT windings without significantly increasing the temperature rise. Interleaving the windings at higher copper thickness can increase the current density further. Simulation results show that at 50 kHz, 400 V and 10 kW current densities up to 10 A/mm² are feasible at natural convection. For solutions with forced convection higher current densities up to 16 A/mm² results in the best trade-off between power density and efficiency. The experiments show that high current densities within acceptable temperatures are feasible and that with a trade-off between current density and applied voltage, the current density can be increased further.

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