Modeling Method for Conducted Noise from Power Converter for Power Line Communication

Naoki Kojima, Takato Hattori, Wataru Kitagawa and Takaharu Takeshita
Nagoya Institute of Technology Gokiso, Showa, Nagoya, Japan

***Abstract*—This paper describes a method for modeling the leakage current from a DC/DC converter to a power line and selecting an EMI filter that suppresses the effect on power line communications. The relationship between the leakage current flowing in the power line and the error rate of power line communication is measured, and the limit value of the leakage current that does not affect power line communication is determined. Since the leakage current flowing in the power line is an attenuated waveform, it is modeled in RLC series circuits, and an equivalent circuit is created. EMI filter is inserted in the simulation, and filter is designed to keep the leakage current within the limit value. The results were compared with experimental results to confirm the reliability of this method.**

***Index Terms*-- Power Line Communication, Conducted Noise, DC/DC Converter, Modeling, Simulation**

I. INTRODUCTION

In recent years, the IoT has connected many objects to the Internet. As a result, wireless communications have become increasingly congested, adversely affecting communications. [1]-[2]Therefore, wired communications, especially power line communications, are attracting attention. [3]-[5] However, power line communication is characterized by its susceptibility to conducted noise. Therefore, noise suppression is an important issue for the widespread use of power line communications. In this paper, we propose a modeling method for conducted noise flowing from DC/DC converters to power lines. Since conducted noise is an attenuated waveform, an equivalent circuit is created using an RLC series circuit. [6]-[12] This equivalent circuit is used to evaluate the noise. Furthermore, CMCC and Y capacitor are inserted into the equivalent circuit as an EMI filter. The experimental and simulation results are compared in terms of current and communication error rate to demonstrate the usefulness of the proposed method.

II. EVALUATION METHOD AND EXPERIMENTAL RESULT

A. Experimental System

Fig.1 shows the circuit configuration of the DC/DC converter using the Sic device, and Table 1 shows the experimental conditions of the DC/DC converter. As shown in Fig 1, the DC power supply, LISN, DC/DC converter, and sliding resistor are connected, the DC/DC converter's substrate surface layer and the power line are connected with lead wires, and the conducted noise flowing into the power line is measured.

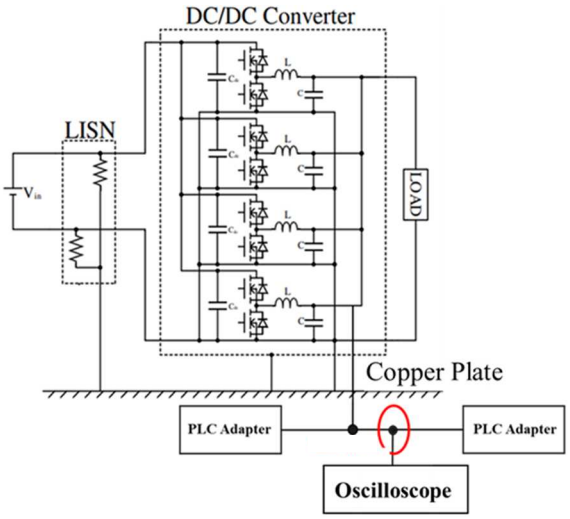

Fig. 1: Experimental system

Table 1: Experimental conditions

Input Voltage V_{in}	0~60V
Input Current I_{in}	2.06A
Output Voltage V_{out}	12.0V
Output Current I_{out}	2.4A
Output Power	72.0V
LOAD	5.00Ω

B. Experimental Results

i. Leakage Current in Power Line

Vary the input voltage of the DC/DC converter from 0V to 60V in 5V intervals and find the value of the leakage current flowing into the power line at each time. Fig. 2 shows the results of FFT analysis of the leakage current flowing from the DC/DC converter to the power line when the input voltage is 30V and 60V. As the input voltage increases, the value of the peak frequency does not change, but the value of the leakage current increases.

ii. Relationship between Leakage Current and Error Rate

For each leakage current that measures the effect of conducted noise flowing into the power line on communication, the error rate of power line communication that occurs at that time is measured. The error rate of communication is obtained by the following equation.

$$E_{rr}[\%] = \frac{N_{rcv}}{N_{snd}} \times 100 \qquad (1)$$

E_{rr} indicates error rate, N_{rcv} indicates the number of data sent, N_{rsv} indicates the number of data received in error. Based on IEEE802.3j, the leakage current value at which the communication error rate becomes 0.10% is defined as the limit value at which communication is normal. Fig.3 shows that the higher the frequency, the lower the limit value of noise and the more susceptible to noise.

III. SIMULATION

Fig.4 shows the leakage current flowing into the power line when the input voltage of the DC/DC converter is 60 V. The FFT result of the leakage current is shown in Fig.5.This leakage current is simulated on the equivalent circuit. From Fig.4, it can be seen that the leakage current flowing through the power line is damped and oscillating. Therefore, a high-frequency equivalent circuit of the leakage current is approximated by an RLC series circuit and simulated. The damped oscillating current flowing immediately after the application of a step voltage of width E_c is expressed by the following equation.

$$i(t) \cong \frac{E_C}{Z_0} e^{-\zeta\omega_n t} \sin \omega_n t \qquad (2)$$

The parameters are natural frequency, resonant frequency, characteristic impedance, maximum value of leakage current, and damping coefficient. They are read from experimental values. are calculated by FFT analysis. Parameters L and C are determined by the following equations. Parameter R is determined from the damping situation.[13]-[15]

$$\omega_n = 2\pi f = \frac{1}{\sqrt{LC}},\ Z_0 = \frac{E_C}{i_{peak}} = \sqrt{\frac{L}{C}},\ \zeta = \frac{R}{2Z_0} \qquad (3)$$

$$L = \frac{Z_0}{\omega_n},\ C = \frac{1}{\omega_n Z_0} \qquad (4)$$

For the leakage currents shown in Fig. 4, a high-frequency equivalent circuit was created using the method described above. The parameters of the derived equivalent circuit are shown in Table 2. The derived equivalent circuit is shown in Fig. 7. The waveforms of the leakage currents simulated by the equivalent circuit and the FFT results are shown in Figs. 4 and 5. The equivalent circuit takes into account the parasitic capacitance in the leads from the substrate surface to the power line.

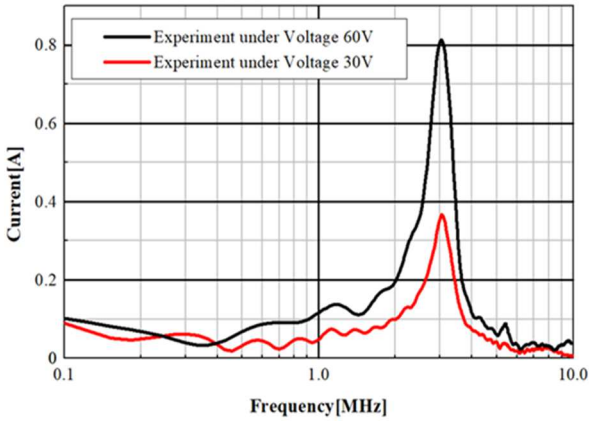

Fig.2: FFT analysis result of Experimental (Input Voltage 30V, 60V)

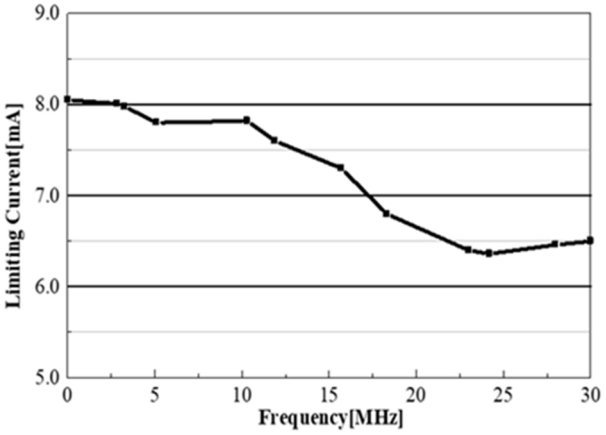

Fig.3: Frequency Characteristics of Error Rate in Power Line Communication

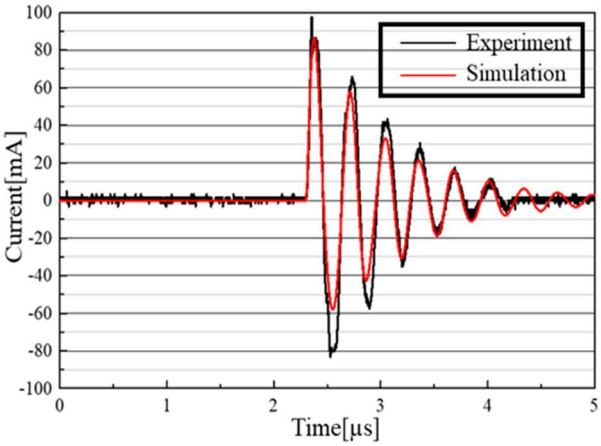

Fig.4: Experimental and simulation result of current on the power line (Input Voltage 60V)

A. Simulation of Current on The Power Line

Fig.4 and Fig.5 show the experimental and simulated currents in the power lines, as well as the FFT results. The attenuation and peak frequency noise levels are in good agreement, indicating that the leakage current can be simulated.

B. Simulation of Current on the Power Line with CMCC

This section describes EMI filters that keep leakage current flowing in power lines within limits. There are two types of conducted noise: normal mode noise and common mode noise. By inserting a separator between the EUT and the spectrum analyzer, normal mode noise and common mode noise can be separated. The measurement results of common mode noise and common mode noise are shown in Fig. 7 and Fig. 8, respectively. The figures show that

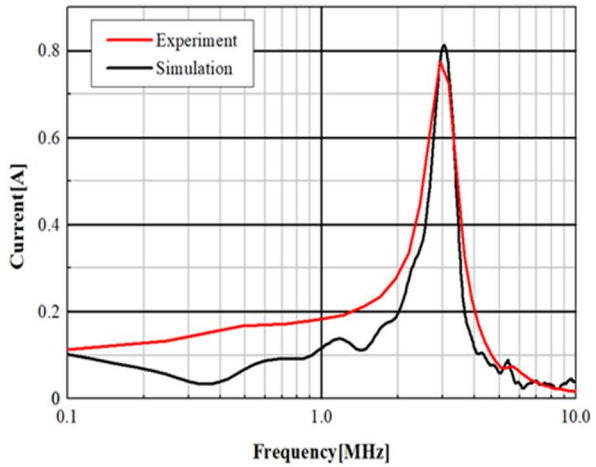

Fig.5: Experimental and simulation FFT analysis of current on the power line (Input Voltage 60V)

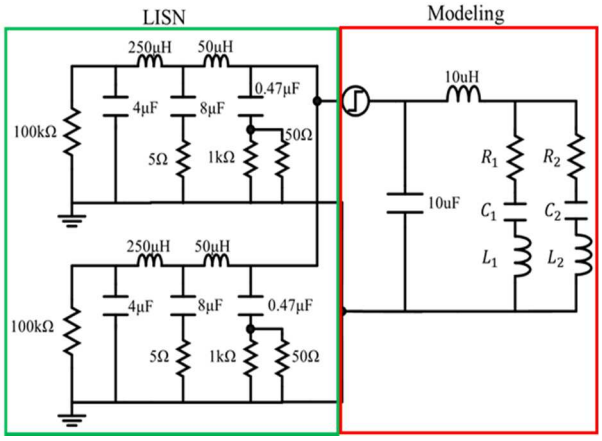

Fig.6: High frequency equivalent circuit

Table2: Parameters of equivalent circuit

$f_1, f_2[\Omega]$	3.24	8.06
$R_1, R_2[\Omega]$	73	200
$L_1, L_2[\mu H]$	21.7	135.4
C_1, C_2[nF]	120.5	2.87

common mode noise is dominant compared to normal mode noise. Therefore, common-mode noise countermeasures are important. In addition, Fig. 5 shows that the leakage current is dominated by 3.24 MHz. For the purpose of common mode noise at 3.24 MHz, a CMCC is used, and an EMI filter modeled by the high-frequency equivalent circuit in Fig. 6 is inserted to confirm its effectiveness.

i. CMCC Selection

Design the CMCC by simulation so that the leakage current flowing through the power supply line is within the specified value. The value of the leakage current is to be suppressed to 7.98 mA or less. Since the peak frequency of the target noise is 3.24 MHz, select a CMCC with the maximum impedance at that frequency. The impedance characteristics of the selected CMCC are shown in Fig. 9, and the CMCC inserted into the derived equivalent circuit is shown in Fig. 10, which is inserted on the input side of the DC/DC converter. The FFT results for that case are shown in Fig. 11, showing a decrease from 9.08 mA to 1.02 mA at a peak frequency of 3.24 MHz Furthermore, Fig. 10 shows the experimental results when the designed CMCC was installed in the actual device, which shows a decrease from 9.08 mA to 2.05 mA at the peak frequency of 3.24 MHz Although there are some errors, the reduction of noise at 3.24 MHz is generally consistent. Thus, the modeling method is validated.

ii. CMCC Insertion on Power Line Communication Quality

Fig. 12 shows the relationship between the leakage current flowing into the power line and the error rate of power line communication at 3.24 MHz This is the same as the error rate when actually inserted into the actual device. This is in general agreement with the experimental result of 0.040% when actually inserted into the actual device. This indicates that the relationship between the leakage current flowing into the power line at 3.24 MHz and the error rate of power line communication is reasonable, and that this method can also be used for the error rate.

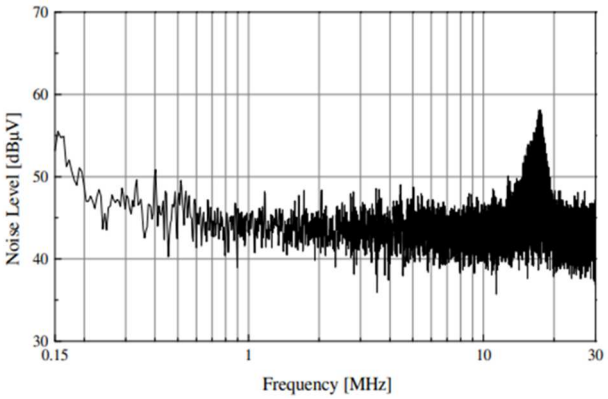

Fig.7: Noise terminal voltage of normal mode noise

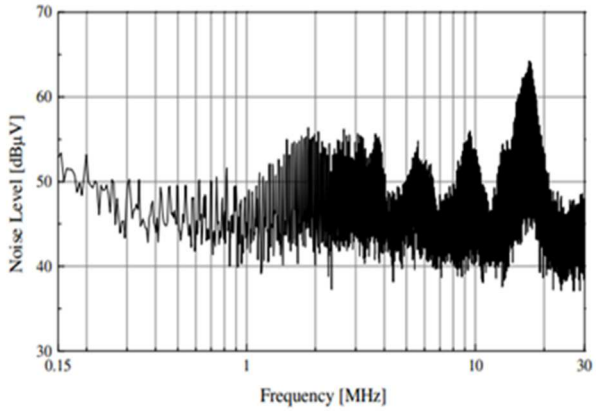

Fig.8: Noise terminal voltage of common mode noise

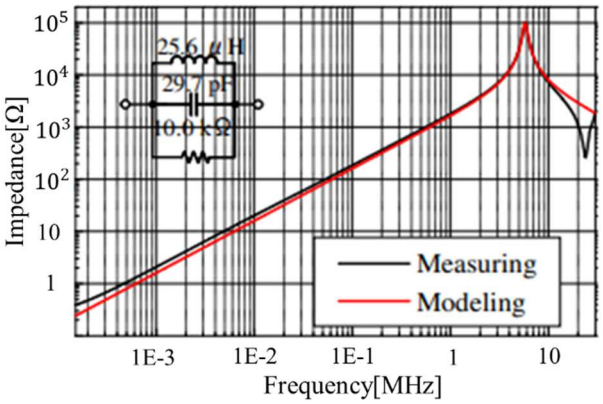

Fig.9: Impedance characteristics of CMCC

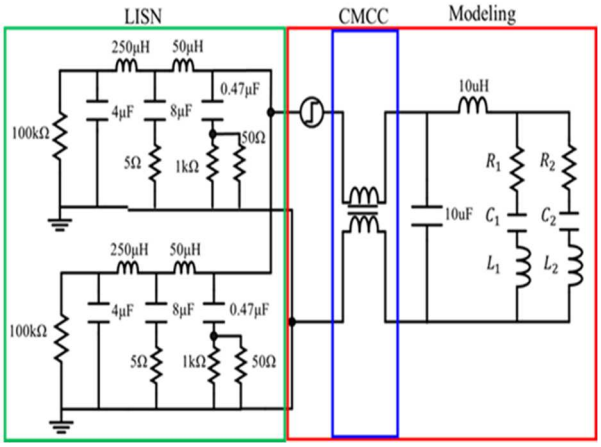

Fig.10: High frequency equivalent circuit with CMCC

C. *Simulation of Current on the Power Line with Y-capacitor*

Describes an EMI filter to keep leakage currents through power lines within limits. There are two types of conducted noise, normal mode noise and common mode noise, but common mode noise accounts for a high percentage. Y-capacitor are used to counter common mode noise. Insert the EMI filter modeled in the high-frequency equivalent circuit shown in Fig.6 to verify the effect.

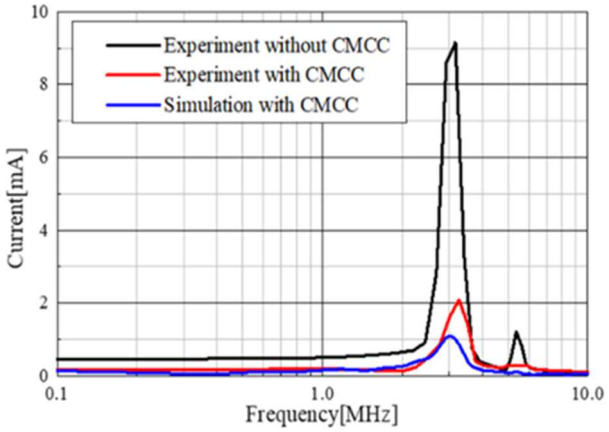

Fig.11: Experimental and simulation FFT analysis result of leaking current with CMCC

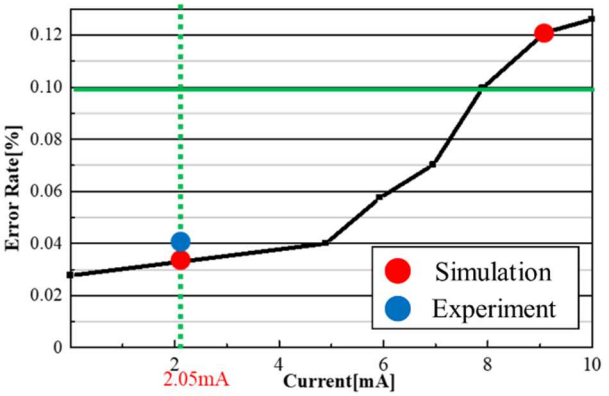

Fig.12: Change in error rate with CMCC

i. *Y-capacitor Selection*

Design the Y-capacitor by simulation so that the leakage current flowing through the power supply line is within the specified value. The value of the leakage current is to be suppressed to 7.98 mA or less. Since the peak frequency of the target noise is 3.24 MHz, select a Y-capacitor with the maximum impedance at that frequency. The impedance characteristics of the selected Y-capacitor are shown in Fig. 13, and the Y-capacitor inserted into the derived equivalent circuit is shown in Fig. 14, which is inserted on the input side of the DC/DC converter. The FFT results for that case are shown in Fig. 15, showing a decrease from 9.08 mA to 1.02 mA at a peak frequency of 3.24 MHz Furthermore, Fig. 14 shows the experimental results when the designed Y-capacitor was installed in the actual device, which shows a decrease from 9.08 mA to 1.20 mA at the peak frequency of 3.24 MHz Although there are some errors, the reduction of noise at 3.24 MHz is generally consistent. Thus, the modeling method is validated.

ii. Y-capacitor Insertion on Power Line Communication Quality

Fig. 16 shows the relationship between the leakage current flowing into the power line and the error rate of power line communication at 3.24 MHz This is the same as the error rate when actually inserted into the actual device. This is in general agreement with the experimental result of 0.030% when actually inserted into the actual device. This indicates that the relationship between the leakage current flowing into the power line at 3.24 MHz and the error rate of power line communication is reasonable, and that this method can also be used for the error rate.

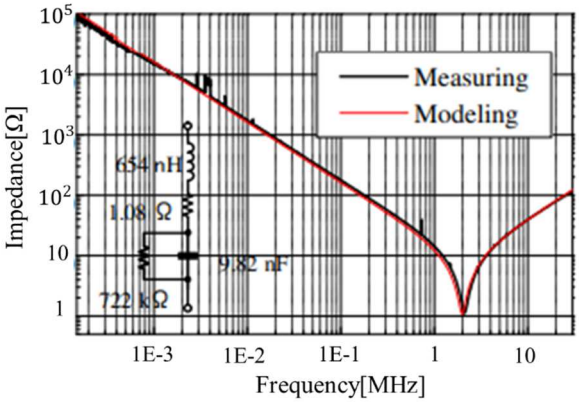

Fig.13: Impedance characteristics of Y capacitor

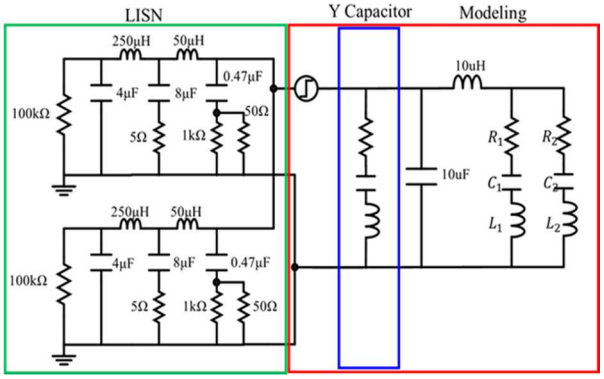

Fig.14: High frequency equivalent circuit with Y -capacitor

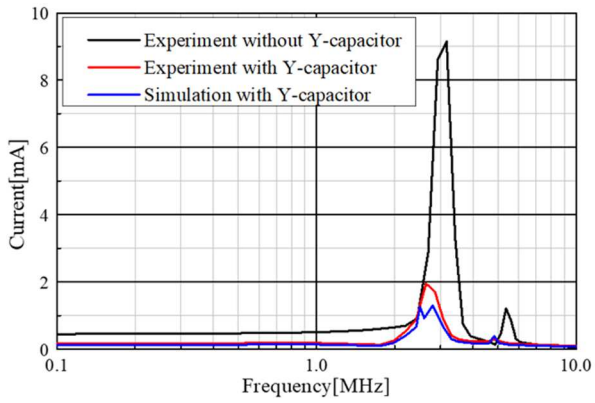

Fig.15: Experimental and simulation FFT analysi s result of leaking current with Y-capacitor

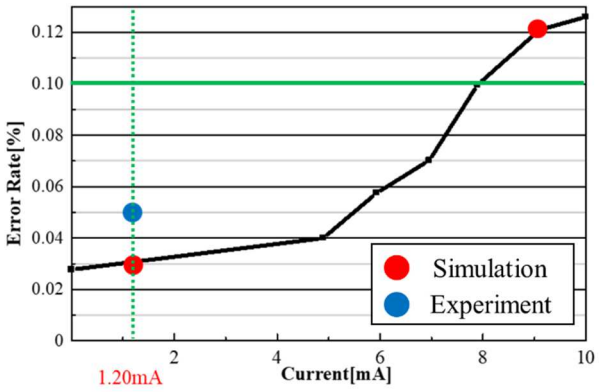

Fig.16: Change in error rate with Y-capacitor

IV. Conclusions

This paper describes an EMI filter design method to maintain proper power line communications. Based on IEEE802.3j, the standard for wired communications, the value of leakage current when the error rate is 0.10% is obtained. Perform an EMI filter to keep it within the limit value. Leakage current was modeled using RLC series circuit because it is an attenuated waveform. Insert CMCC and Y-capacitor into the derived equivalent circuit to reduce noise. The validity of the method was confirmed by comparing the experimental and simulated values with the designed filter inserted. Furthermore, the effect of conducted noise on power line communication was evaluated by error rate, and an evaluation by error rate was also performed. The results were also in good agreement, indicating that the relationship between leakage current and error rate is also correct and that the simulation method can be used for power line communication quality.

V. Acknowledgment

This research was partially supported by JSPS Grant-in-Aid for Scientific Research JP22K04043.

REFERENCES

[1] GA Akpakwu, BJ Silva, GP Hancke, Adnan M. Abu-Mahfouz"A Survey on 5G Networks for the Internet of Things: Communication Technologies and *Challenges", IEEE 2017*

[2] A Hakiri, P Berthou, A Gokhale, Slim Abdellatif "Publish/subscribe-enabled software defined networking for efficient and scalable IoT communications"

[3] T. Kitamura, M. Yamada, S. Harada, M. Koyama, "Development of Highpower-density Interleaved DC/DC Converter with SiC Devices", IEEJ Transactions on Industry Applications, Vol. 134, No. 11, pp. 956-961, 2014 J. Clerk Maxwell, *A Treatise on Electricity and Magnetism*, 3rd ed., vol. 2. Oxford: Clarendon, 1892, pp. 68-73.

[4] T.Hattori, W Kitagawa, T Takeshita, "Modeling Method for conducted noise flowing in power lines of

DC/DC converter r", 2022 24th European Conference on Power Electronics and Applications
[5] T.Hattori, W Kitagawa, T Takeshita, "Modeling Method for Bidirectional Conducted Noise Simulation of DC-DC Converter", 2022 25th International Conference on Electrical Machines and Systems
[6] T. Shimizu, "Historical Review of EMI Measures in the Field of Power Electronics", Annual Meeting Record, I.E.E Japan (CD-ROM), ROMBUNNO.S12-8, 2021
[7] C. Nan, R. Ayyanar and Y. Xi, "High frequency active-clamp buck converter for low power automotive applications," 2014 IEEE Energy Conversion Congress and Exposition (ECCE), pp. 3780-3785, 2014
[8] L. Zhai , G. Hu, M. Lv, T. Zhang and R. Hou, "Comparison of Two Design Methods of EMI Filter for High Voltage Power Supply in DC-DC Converter of Electric Vehicle," in IEEE Access, vol. 8, pp. 66564-66577, 2020
[9] M. Terasaki, Y. Oohashi, Y. Masuyama and T. Sudo, "Design and analysis for noise suppression of DC/DC converter," 2014 IEEE Electrical Design of Advanced Packaging and Systems Symposium (EDAPS), pp. 109 - 112, 2014
[10] S. Maekawa, J. Tuda, A. Kuzumaki, S. Matsumoto, H. Mochikawa, H. Kubota, "EMI Prediction Method for SiC Inverter by Developing an Accurate Model of Power Device ", IEEJ Transactions on Industry Applications, Vol. 134, No. 4, pp. 461-467, 2014
[11] E. Rondon-Pinilla, F. Morel, C. Vollaire and J. Schanen, "Modeling of a Buck Converter with a SiC JFET to Predict EMC Conducted Emissions," in IEEE Transactions on Power Electronics, vol. 29, no. 5, pp. 2246- 2260, May 2014
[12] D. Drozhzhin, V. Karakasli and G. Griepentrog, "Comprehensive Analysis of Converter Output Voltage for Conducted Noise Simulation," 2019 International Symposium on Electromagnetic Compatibility – EMC EUROPE, pp. 42-47, 2019
[13] I. A. Makda and M. Nymand, "Common-mode noise analysis, modeling and filter design for a phase-shifted full-bridge forward converter," 2015 IEEE 11th International Conference on Power Electronics and Drive Systems, pp. 1100-1105, 2015
[14] Y. Ishii et al., "Accurate Conducted EMI Simulation of a Buck Converter With a Compact Model for an SiC-MOSFET," 2020 IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 2800-2805, 2020
[15] S. Takahashi, K. Wada, H. Ayano, S. Ogasawara, "Review of Modeling and Suppression Techniques for Electromagnetic Interference in power Conversion Systems", 2022 IEEE Journal of Industry Applications, Vol. 11, No. 1, pp. 7-19 ,2022 The Institute of Electrical Engineer of Japan
[16] H. Tanaka, K. Suzuki, W. Kitagawa, T. Takeshita, "Conducted Noise Reduction on AC/DC Converter using SiC-MOSFET ", 2016 IEEE International Conference on Renewable Energy Research and Applications (ICRERA), pp. 341-346, 2016
[17] H. Tanaka, K. Suzuki, W. Kitagawa and T. Takeshita,"Design for conducted noise reduction on AC/DC converter using SiC-MOSFET," 2016 19th International Conference on Electrical Machines and Systems (ICEMS), pp. 1-6, 2016
[18] Y. Kawamura, H. Tanaka, K. Suzuki, W. Kitagawa and T. Takeshita,"Investigation of Modeling for Conducted Noise Reduction on Isolated AC/DC Converter using SiC Devices," 2018 20th European Conference on Power Electronics and Applications (EPE'18 ECCE Europe), pp. 1- 10, 2018
[19] Y. Kawamura, H. Tanaka, K. Suzuki, W. Kitagawa and T. Takeshita,"Consideration of conducted noise reduction on isolated AC/DC converter using SiC devices," 2017 IEEE 6th International Conference on Renewable Energy Research and Applications (ICRERA), pp. 359-364, 2017
[20] K. Kuwana, Y. Kawamura, W. Kitagawa and T. Takeshita, "Modeling for Conducted Noise Simulation Considering Switching Characteristics on AC/DC Converter," 2019 10th International Conference on Power Electronics and ECCE Asia (ICPE 2019 - ECCE Asia), pp. 927-932, 2019
[21] W. Kitagawa, T.Kutsuna, K. Kuwana, Y. Kawamura, T. Takeshita, "Conducted Noise Simulation on AC/DC Converter using SiC-MOSFET," in IEEE Transactions on Industry Applications, vol. 57, no. 2, pp. 1644- 1651, March-April 2021
[22] K. Mitani, W. Kitagawa and T. Takeshita, "Modeling for Conducted Noise on AC/DC Converter by Using Impedance Characteristic," 2019 22nd International Conference on Electrical Machines and Systems (ICEMS), pp. 1-6, 2019
[23] K. Mitani, Y. Kawamura, W. Kitagawa and T. Takeshita, "Circuit Modeling for Common Mode Noise on AC/DC Converter Using SiC Device," 2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe), pp. P.1-P.10, 2019
[24] W. Kitagawa, K. Mitani, Y. Kawamura and T. Takeshita, "Modeling and Simulation for Conducted Noise on AC/DC Converter Using SiCDevice," 2019 10th International Conference on Power Electronics and ECCE Asia (ICPE 2019 - ECCE Asia), pp. 1-6, 2019