Characterization of GaN-on-AlN/SiC transistors towards monolithic integrability

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Keywords

«Monolithic power integration», «Gallium Nitride (GaN)», «Device characterisation», «HEMT», «Double pulse test»

Abstract

A GaN-on-AlN/SiC technology is proposed for monolithic GaN power switch integration. As opposed to conventional GaN-on-Si devices, the insulating SiC substrate results in immunity to back-gating effects and enables monolithic integration without degradation of switching characteristics resulting from the shared substrate. This is validated for a discrete half-bridge, with the substrate of both transistors shorted together, as well as for a monolithic half-bridge. Hard switching transients up to 300 V in a double-pulse test with both half-bridges reveal faster switching transients and reduced switching losses for the monolithically integrated half-bridge.

1 Introduction

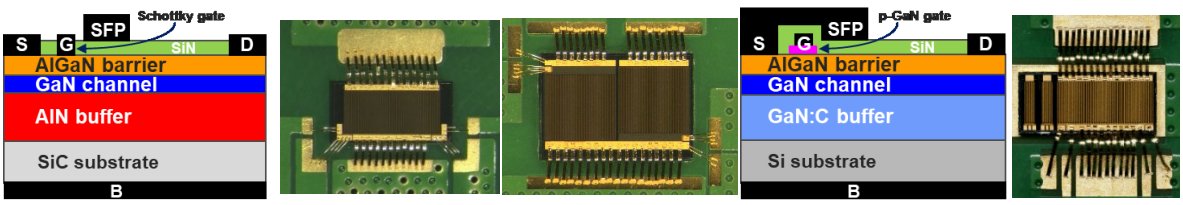
GaN-on-Si high electron mobility transistors (HEMTs) have achieved a mature technology state during recent years and are increasingly employed in commercial power electronic applications. Low on-resistance combined with small intrinsic parasitic capacitances allow for efficient high frequency operation in hard- and soft- switched converters. Due to increased switching speed in comparison to conventional silicon (Si) power transistors, monolithic integration of GaN HEMTs is a suitable approach to minimize parasitic stray inductances of the switching cell in order to achieve stable and clean switching transitions. Monolithic integration of two (or more) conventional GaN-on-Si HEMTs has been successfully demonstrated for Monolithic Half-Bridges (MHB) [1, 2] as well as monolithic bidirectional GaN HEMTs [3, 4]. However, substrate coupling effects can result in oscillations, reduced switching speed and increased on-resistance. Advanced substrate termination schemes can be employed to overcome these limitations but inevitably increase the circuit complexity [5, 6, 7, 4]. On-chip isolation by means of metal oxide layers is a further approach to suppress the substrate coupling effect in GaN-on-Si HEMTs but increase the device fabrication complexity [8]. Instead, the lateral GaN HEMTs presented in this paper are fabricated on a semi-isolating SiC substrate using an AlN buffer layer enabling reduced substrate coupling effects as well as reduced thermal resistance from the GaN channel towards the substrate. The immunity against back-gating has been previously validated for discrete GaN-on-AlN/SiC HEMTs in static and dynamic characterizations [9]. In this paper, dynamic characterizations

are executed in a half-bridge topology and hard-switched double-pulse test using the same discrete GaN-on-AlN/SiC HEMTs with a gate width of w_G = 92 mm. In difference to [9] the substrate nodes of both discrete power transistors forming the half-bridge are electrically shorted in order to share a common bulk-potential similar to an MHB. Furthermore, hard-switched double-pulse tests are performed with an MHB fabricated on the same wafer and based on the same GaN-on-AlN/SiC technology with identical gate widths as the discrete devices. Reduced switching losses for the MHB could be realized because of the monolithic integration and associated changes in PCB layout. Additional device characterizations cover the temperature-dependent on-resistance as well as voltage-dependent parasitic device capacitances. All static characterizations of the proposed GaN-on-AlN/SiC HEMT are compared to a conventional normally-off p-GaN gate GaN HEMT based on a mature GaN-on-Si technology platform [10].

2 Device fabrication and technology

An unintentionally doped AlN layer as buffer material is used for the GaN-on-AlN/SiC transistor instead of a compensation doped GaN buffer as it is used for most conventional power-electronic GaN transistors. The AlN buffer acts as efficient back-barrier giving a good transistor-channel confinement and thus high device breakdown strength [11]. The AlGaN/GaN/AlN hetero structure is MOCVD-grown on top of 4" semi-insulating 4H-SiC substrates. While SiC substrates are more expensive than Si substrates, this is offset by the increased complexity of nitrite growth on Si. Unless sophisticated strain management methods are used, nitrite layers on Si will crack during cool down from MOCVD growth temperatures [12].

Normally-on AlGaN/GaN/AlN HEMTs with Ir-based Schottky-type gates are processed on the 4" wafers. All structures are defined by *i*-line optical stepper lithography. Ohmic source and drain contacts consist of a Ti/Al//Ni/Au based metallization, alloyed with RTA at 870°C in N_2 ambient. The devices were isolated by nitrogen implantation. The hetero structure is further passivated with 180 nm PECVD-deposited SiN_x. An Ir/Ti/Au gate metal was electron-beam evaporated on top of the 0.7 µm gate trench inside the SiN_x passivation layer. Source-connected Field Plates (SFP) are positioned on top of the SiNx layer 2 µm in front of the gate metal towards drain, see Fig. 1a. A benzocyclobutene (BCB) encapsulation was used to prevent any surface arcing during high voltage operation. Fabricated power-switching devices with 92 mm gate width, 0.7 µm gate length, 1 µm source-gate separation and 18 µm gate-drain separation (Fig. 1b) showed a static on-state resistance of approx. 100 mΩ and a maximum pulse current of 70 A at 1.0 V gate bias. MHB structures consisting of two corresponding 92 mm power-switches (Fig. 1c) were fabricated on the same wafer as well.
For comparison, similar GaN-on-Si transistors (Fig. 1e), having the same gate-source and gate-drain separation are studied [10]. Instead of an AlN buffer on SiC substrate, a carbon-doped GaN buffer structure was grown on a conductive Si substrate, see Fig. 1d. In contrast to the GaN-on-AlN/SiC transistor (Fig. 1a), a p-GaN based gate module is used for the device's normally-off characteristic and the SFP is enclosing the gate from the top (Fig. 1d).



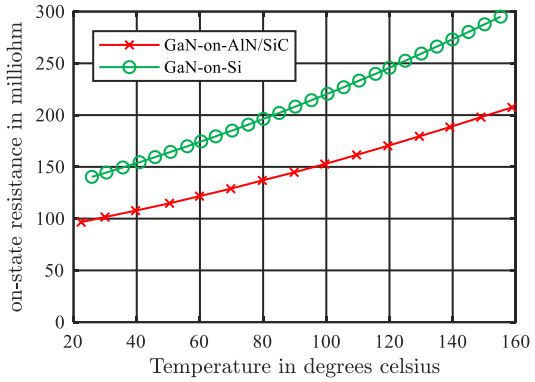
(a) (b) (c) (d) (e)

Fig. 1: Schematic cross-sections and mounted power devices on custom submount-PCBs: (a) Structure, (b) 92 mm transistor chips and (c) 2×92 mm MHB chip of the GaN-on-AlN/SiC transistor structure with Schottky-type gate. (d) Structure and (e) 92 mm transistor chip of the AlGaN/GaN-on-Si transistor with a p-GaN gate module for normally-off operation

3 Static characteristics

3.1 Static on-resistance R_{DSon}

The static on-resistance of GaN HEMTs is known to be strongly temperature-dependent due to reduced electron mobility in the two-dimensional electron gas (2DEG) at increased device temperature. The temperature-dependent on-state resistance is measured inside a temperature cabinet while a time-constant drain current I_D=100 mA is sourced into the device under test (DUT). The fabricated 92 mm GaN-on-AlN/SiC achieve a 29.7 % lower static on-resistance $R_{DSon,GaN\text{-}on\text{-}AlN/SiC}$ =101.4 mΩ compared to their GaN-on-Si counterparts ($R_{DSon,GaN\text{-}on\text{-}Si}$ =144.2 mΩ) at an ambient temperature T=30°C. At elevated temperature T=150°C the static on-resistance is increased up to 198.9 mΩ and 287.5 mΩ in the GaN-on-AlN/SiC and GaN-on-Si HEMT, respectively. Due to a similar transistor design concerning the AlGaN/GaN hetero-junction where the 2DEG is formed, the relative static R_{on}-increase of +96.15 % (GaN-on-AlN/SiC) and +99.37 % (GaN-on-Si) from 30°C to 150°C is similar for both GaN HEMTs.



$$R_{on}(T)=a\cdot T^2+b\cdot T+c \qquad (1)$$

Coefficient	**GaN-on-AlN/SiC**	**GaN-on-Si**
a ($\Omega\cdot K^{-2}$)	$1.44\cdot10^{-6}$	$2.20\cdot10^{-6}$
b ($\Omega\cdot K^{-1}$)	$553\cdot10^{-6}$	$799\cdot10^{-6}$
c (Ω)	$83.5\cdot10^{-3}$	$118.2\cdot10^{-3}$

Fig. 2: Comparison of the temperature-dependent static on-resistance of 92 mm GaN-on-AlN/SiC and GaN-on-Si HEMTs

3.2 Static I-V characteristics

The static I-V characteristics of the GaN-on-AlN/SiC power transistor are acquired using the test bench introduced in [13] and compared with the I-V characteristics of a 210 mm GaN-on-Si transistor variant, see Fig. 3. The I-V curves are measured at gate-source voltage V_{GS} = −3 V to 1 V, drain-source voltage V_{DS} = −5 V to 20 V and different bulk-source bias V_{BS} = –400 V to 400 V for the GaN-on-AlN/SiC transistor and V_{GS} = −3 V to 6 V, V_{DS} = −5 V to 20 V and different bulk-source bias V_{BS} = –450 V to 100 V for the GaN-on-Si transistor. The pulse length was 5 µs to avoid device self-heating during I-V characterization and the data is normalized by the transistors' gate width.

The presented GaN-on-AlN/SiC transistor (Fig. 3a) shows a maximum saturation current of approximately 0.76 A/mm (70 A for the 92 mm transistor) with the bulk-terminal connected to source. The maximum current density of the GaN-on-Si transistor (0.6 A/mm) is less because of its designed normally-off characteristic (Fig. 3b). The bulk-source bias V_{BS} has strong impact on the maximum drain current for the GaN-on-Si transistor which decreases from 0.6 A/mm to 0.2 A/mm with increasing negative V_{BS}, see Fig. 4b. The transistor channel resistivity increases in parallel. Root cause is the capacitive coupling of the conductive Si substrate to the 2DEG transistor channel via the GaN buffer and channel layers of approx. 5 µm thickness. The 2DEG electron density reduces with increasing negative bulk potential. In contrast, V_{BS} has negligible influence on the output characteristics of the GaN-on-AlN/SiC transistor and the I-V curves remain almost identical with varied V_{BS} in the range of –400 V to 400 V and a fixed V_{GS} of 1 V (Fig. 4a). The electrically insulating SiC substrate with 340 µm thickness strongly reduces the capacitance between the bulk (backside of the SiC substrate) and the transistor channel. As a consequence, GaN-on-AlN/SiC transistors are immune to back-gating effects in their static characteristics.

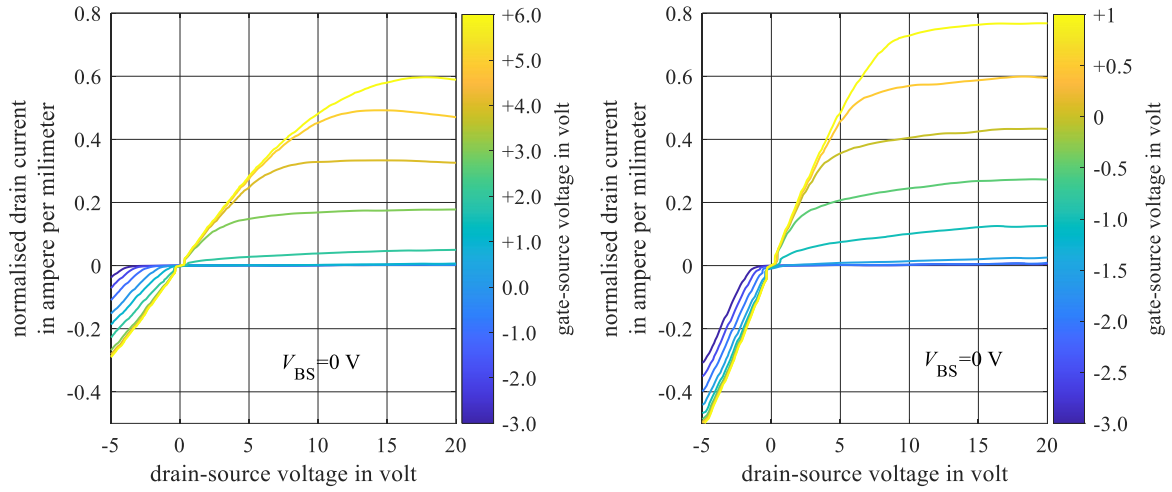


Fig. 3: Output characteristic of (a) GaN-on-Si and (b) GaN-on-AlN/SiC HEMT transistor with bulk-terminal connected to source-terminal for different gate-source voltages.

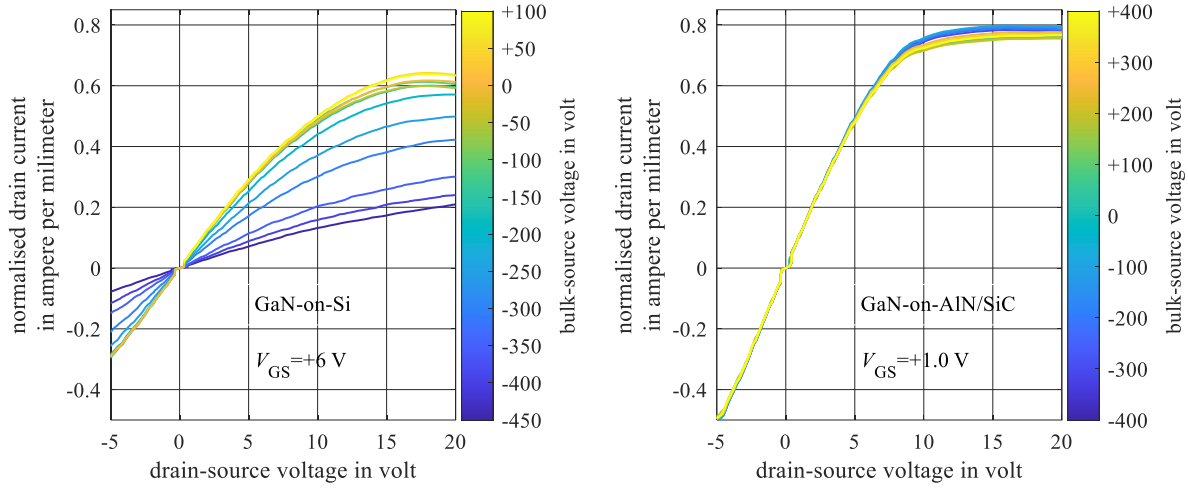


Fig. 4: Output characteristic of (a) GaN-on-Si and (b) GaN-on-AlN/SiC HEMT transistor at a fixed gate-source voltage for different bulk-source bias voltages.

3.3 Static C-V characteristics

GaN transistors show much lower parasitic capacitances due to their lateral structure compared with Si-counterparts, enabling fast switching [14]. The input capacitances C_{ISS}, output capacitance C_{OSS} and reverse transfer capacitance C_{RSS} are acquired via small signal measurements. The measurements are carried out with a Keithley parameter analyzer (Table I and Fig. 5) with an RMS voltage of 100 mV and a frequency of 200 kHz, while the bulk-terminal of the GaN-on-AlN/SiC transistor is shorted to the source-terminal. The drain-source voltage V_{DS} is swept from 0 V to 600 V, the gate-source voltage V_{GS} is kept at a constant value of −6 V. The transistor capacitances show a strong dependence on drain-source voltage V_{DS}. C_{ISS}, C_{OSS} and C_{RSS} have a value of 107 pF, 124 pF and 60 pF, respectively, at V_{DS}=0 V, which decreases with increasing V_{DS}, and reaches a value of 54 pF, 11 pF and 1.6 pF at V_{DS}=600 V (Fig. 6) The low capacitances and the calculated correspondingly low total output charge Q_{OSS} of 9.8 nC and stored energy E_{OSS} of 1.2 µJ at V_{DS}=400V, indicate that the GaN-on-AlN/SiC transistors are promising for fast switching and high-frequency applications. In comparison to the 92 mm GaN-on-Si device, the GaN-on-AlN/SiC transistor has substantially lower input and output capacitances but an increased transfer capacitance at a high drain-source voltage (>120 V). This is beneficial to reduce of switching losses but increases susceptibility to cross conduction. The coupling of source, gate and drain via the substrate is reduced for the GaN-on-AlN/SiC device because of the insulating nature of the

SiC substrate. As opposed to the GaN-on-Si device, the source-connected field plate of the GaN-on-AlN/SiC transistor is not overlapping the gate. That's why the GaN-on-AlN/SiC transistor has a higher C_{RSS}.

Table I: CV profiling setup

CVU	Keithley 4215-CVU
Drain SMU	Keithley 2657A
Drain bias tee	Keithley 2650-RBT-3K
Gate SMU	Keithley 2635B
Gate bias tee	Keithley 2600-RBT-200
Source bias tee	Keithley 2600-RBT-200

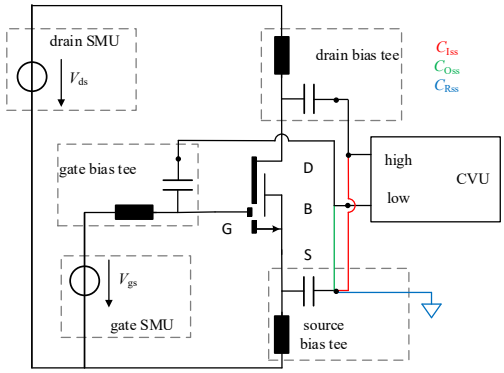


Fig. 5: Schematic of C-V measurements

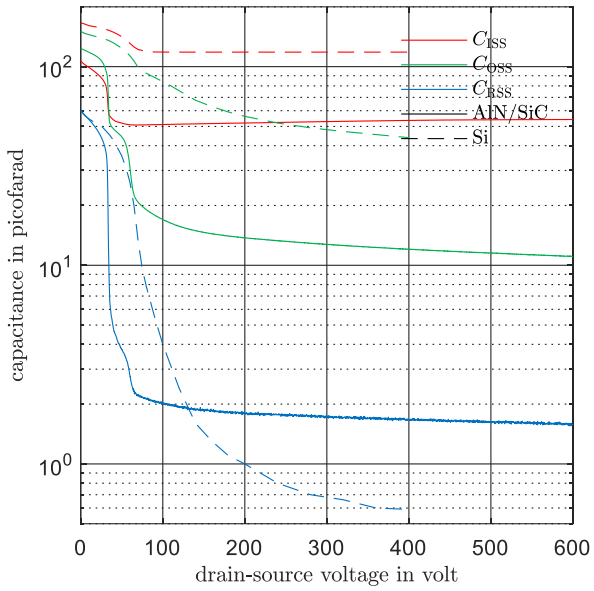


Fig. 6: Capacitance voltage profile of the GaN-on-AlN/SiC transistor with V_{GS}=−6 V, measured with a 200 kHz and 100 mV RMS small signal measurement, compared to capacitance voltage measurements of the GaN-on-Si transistor, recorded using a HP 4280A C-V Plotter at 1 MHz small signal frequency.

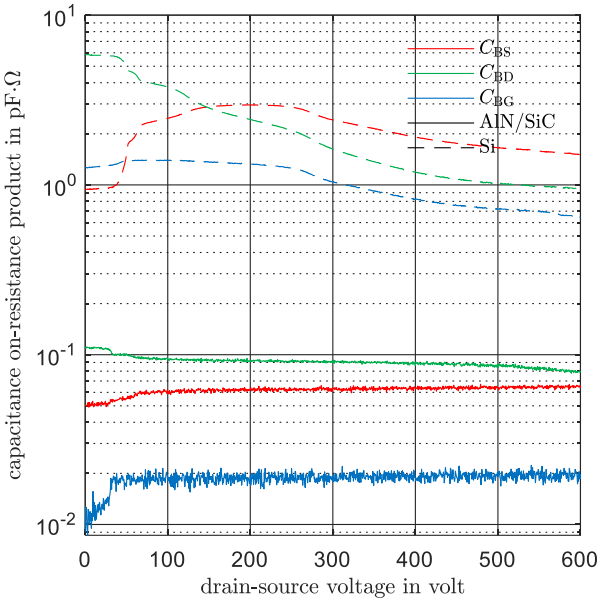
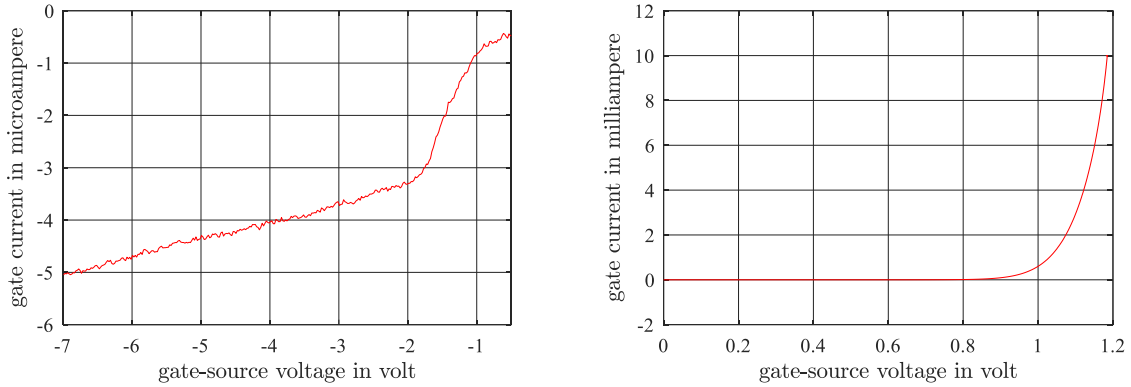


Fig. 7: Bulk capacitances of the GaN-on-AlN/SiC transistor with V_{GS}=−6 V compared to a commercial GaN-on-Si transistor (GS66508P) with V_{GS}=0 V, measured with a 200 kHz and 300 mV RMS small signal.

Additionally, the bulk-source, bulk-gate and bulk-drain capacitances of the GaN-on-AlN/SiC transistor and a commercially available GaN-on-Si transistor with exposed bulk node (GS66508P) are compared in Fig. 7. Because the transistor layout of the commercial device is unknown, the data is normalized to the nominal on-state resistance, 100 mΩ and 50 mΩ, respectively. The GaN-on-AlN/SiC transistor shows significant lower normalized bulk capacitances (between one and two orders of magnitude) than the GaN-on-Si transistor. The reduced coupling from source, gate and drain to the substrate is in favor of fast switching transients.

3.4 Gate-source characteristics

The GaN-on-AlN/SiC transistor Schottky-diode which is formed between the Ir gate metal on top of the AlGaN barrier and the 2DEG beneath features a barrier height of ~0.9 eV. This leads to a gate current as forward diode current, when the transistor is in a typical on-state condition with V_{GS} = 1 V and V_{DS} < 1 V. The characteristics of the gate diode (Fig. 8) are measured with bulk shorted to source while drain is left open. The measurements are performed using a Keithley 2635B SMU. At a typical off-state gate-source voltage of −6 V the gate diode has a leakage current of −4.3 µA. The diode conducts and current flows through the gate in the on-state. This non-insulating gate characteristic, which is similar to GaN Gate Injection Transistors (GIT) with p-GaN gate [15], brings new challenges to driving the transistor, since a large gate current pulse is required during switching transitions to achieve fast switching, while a mA-range continuous gate current is desired during on-state to keep the device in on-state and minimize the conduction losses simultaneously [15, 16].



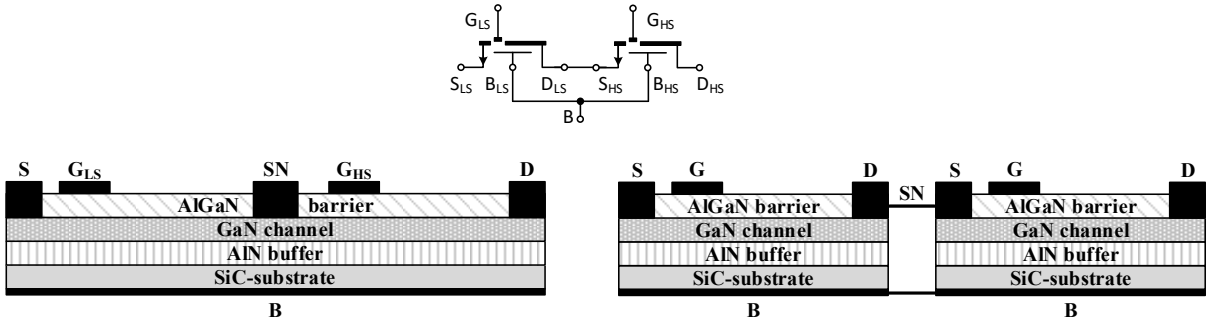
(a) (b)

Fig. 8: (a) Gate reverse characteristic and (b) forward characteristic of gate-source diode, measured with bulk connected to source and open drain.

4 Dynamic characteristics

4.1 Measurement setup

Current collapse is a critical issue for monolithic GaN power transistor integration since the transistors share a common substrate potential (Fig. 9a) and cannot be connected to their respective source-terminal separately to suppress the back-gating effects (see Fig. 4b for the case of GaN-on-Si).



(a) (b)

Fig. 9: (a) monolithic half-bridge chip and (b) half-bridge built via two discrete chips.

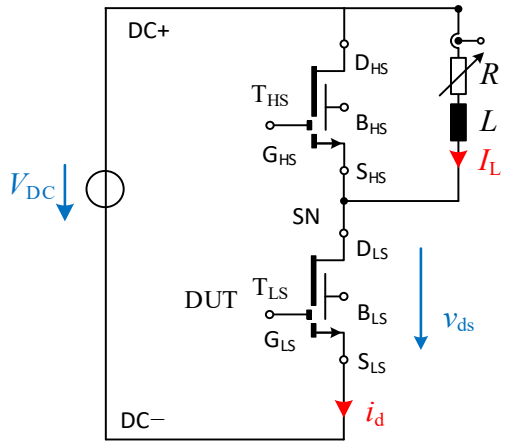


Fig. 10: Schematic of half-bridge used for double-pulse tests.

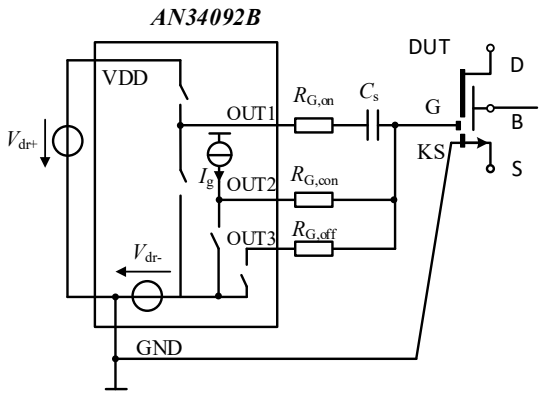
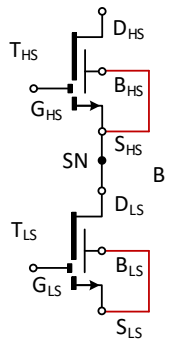
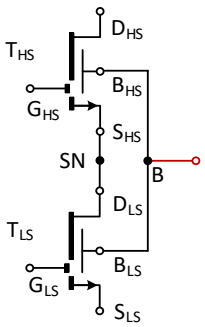
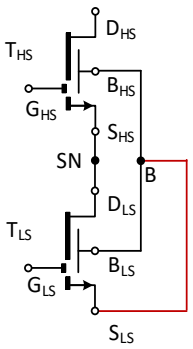
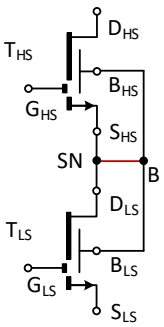
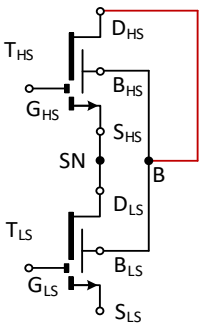


Fig. 11: Schematic of gate-loop circuit.

To study the benefits of the presented GaN-on-AlN/SiC HEMT technology for monolithic integration, a half-bridge using discrete transistors is built and evaluated with the different bulk terminations listed in Table II. Only the bulk-potential is varied while all other conditions are kept completely identical. Conf. 1 represents the typical bulk termination used for discrete transistors, avoiding back-gating effects and enabling fast switching [14]. As this configuration is not feasible for MHBs with a shared bulk potential, configurations with the common bulk potential either floating (conf. 2) or connected to low-side source, switch-node and high-side drain for conf. 3 to 5, respectively are studied. Further, the measurements for conf. 2 to 5 are repeated for the real MHB chip (Fig. 1c) to verify the validity of the results for real monolithic applications and to study the benefits from monolithic integration compared with discrete devices.

Table II: Configuration of different bulk termination

Conf. 1	Conf. 2	Conf. 3	Conf. 4	Conf. 5
				
Bulk of each transistor connected to their respective source-terminal	Bulk of both transistors are connected and floating	Bulk of both transistors are connected to S_{LS}	Bulk of both transistors are connected to switching note	Bulk of both transistors are connected to D_{HS}

The double pulse tests are performed in a half-bridge configuration with an inductive load at different load currents I_L and blocking voltages V_{dc} (Fig. 10). Due to the non-insulating gate characteristics of the GaN-on-AlN/SiC HEMT, the Panasonic driver *AN34092B* [17] with an integrated current source is used (Fig. 11). The turn-on gate resistor $R_{G,on}$ is connected in series with a high-pass capacitor C_s to achieve fast turn-on (OUT1) and the integrated current source (OUT2) offers a constant current in mA-range in on-state. Both gate resistors $R_{G,off}$ and $R_{G,con}$, have an influence on the turn-off speed. The gate configuration is listed in Table III. The drain current of the low-side transistor (DUT) is measured using a high-bandwidth, low inductance SMD shunt [18] and the drain-source voltage is measured via a TPP0850 850 MHz bandwidth voltage probe.

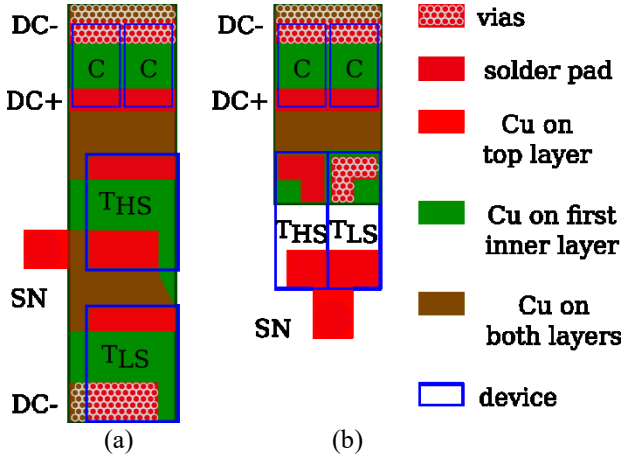


Fig. 12: Simplified layout of the commutation loop of the discrete (a) and monolithic (b) half-bridge. Both layouts are to scale.

Table III: Gate circuit configuration

Parameters	Symbol	Value
Turn-on gate resistor	$R_{G,on}$	5.6 Ω
Turn-off gate resistor	$R_{G,off}$	2 Ω
Continuous gate resistor	$R_{G,con}$	3.9 Ω
Boost capacitor	C_s	330 pF
Continuous gate current turn-on	$I_{G,on}$	5 mA
Turn-on gate voltage	$V_{dr,on}$	5 V
Turn-off gate voltage	$V_{dr,off}$	−5 V

The PCBs for the discrete half-bridge and the MHB where designed almost identical to ensure comparability between the different transistors. The gate drivers, DC-link capacitors and shunts use the same circuitry and layout. However, the commutation loop is changed. While the discrete half-bridge uses a completely vertical commutation loop, the commutation loop of the MHB is vertical at the shunt and DC-link capacitors and horizontal on the MHB as shown in Fig. 12. For the discrete half-bridge, the switching node's copper overlaps the copper on the inner layer, which is connected to the low-side transistor's source. In contrast, there is no overlapping copper at the switching node with the MHB leading to a reduction in parasitic capacitances of the switching node. However, horizontal commutation loops tend to have an increased parasitic inductance, compared to vertical loops [19], which is mitigated by the monolithic integration.

4.2 Measurement results

With conventional bulk termination (conf.1) the GaN-on-AlN/SiC HEMT shows good high-speed switching performance with a turn-on voltage slew rate of −63 V/ns and a turn-off slew rate of 63 V/ns at a blocking voltage of 250 V and an inductor current of 7 A (Fig. 13) over an interval from 20 % to 80 %.

The switching transitions and the switching losses for the different studied bulk terminations are shown in Fig. 14 and Fig. 15(a) respectively. The bulk terminations show only negligible influence on the discrete half-bridge's dynamic characteristics. While GaN-on-Si devices show a strong impact of the bulk termination on the dynamic R_{on} [4], no such effect is observed here. Furthermore, both the current and voltage transients are nearly unchanged for conf. 1 through 4 (Fig. 14). In configuration 5 the drain current peak during turn-on is slightly elevated, leading to increased switching losses (Fig. 15a). Although the capacitive coupling between the top and bottom side of GaN-on-AlN/SiC HEMT is significantly reduced by the larger separation of the conductive layers as compared to GaN-on-Si, the metallized backside of the SiC substrate may still couple to the devices top. Different bulk terminations could change the device's capacitances and could lead to increased cross conduction and correspondingly higher losses. However, since these measurements were conducted consecutively in the order of increasing configuration number, device degradation cannot be ruled out as well.

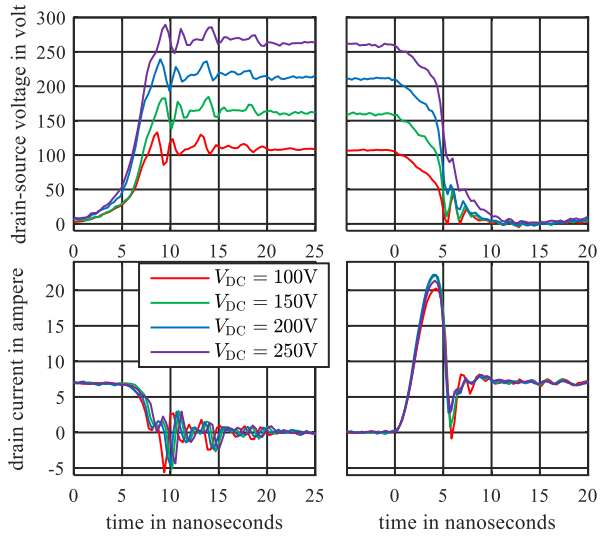


Fig. 13: Turn-off (left) and turn-on (right) transients for conf. 1 at an inductor current of 7 A and 100 V to 250 V blocking voltage, for the emulated MHB.

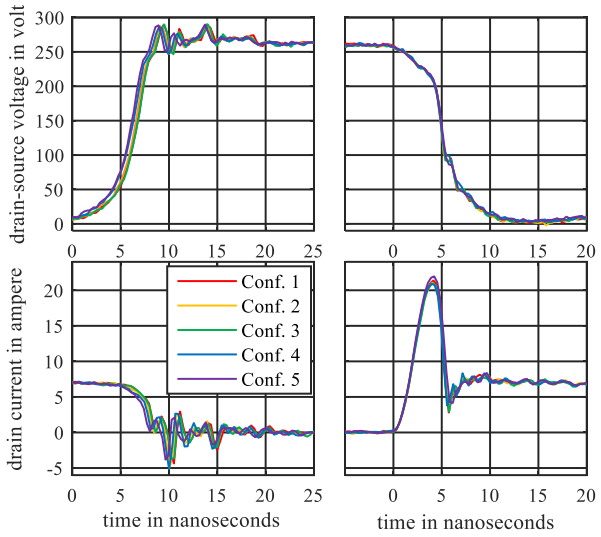
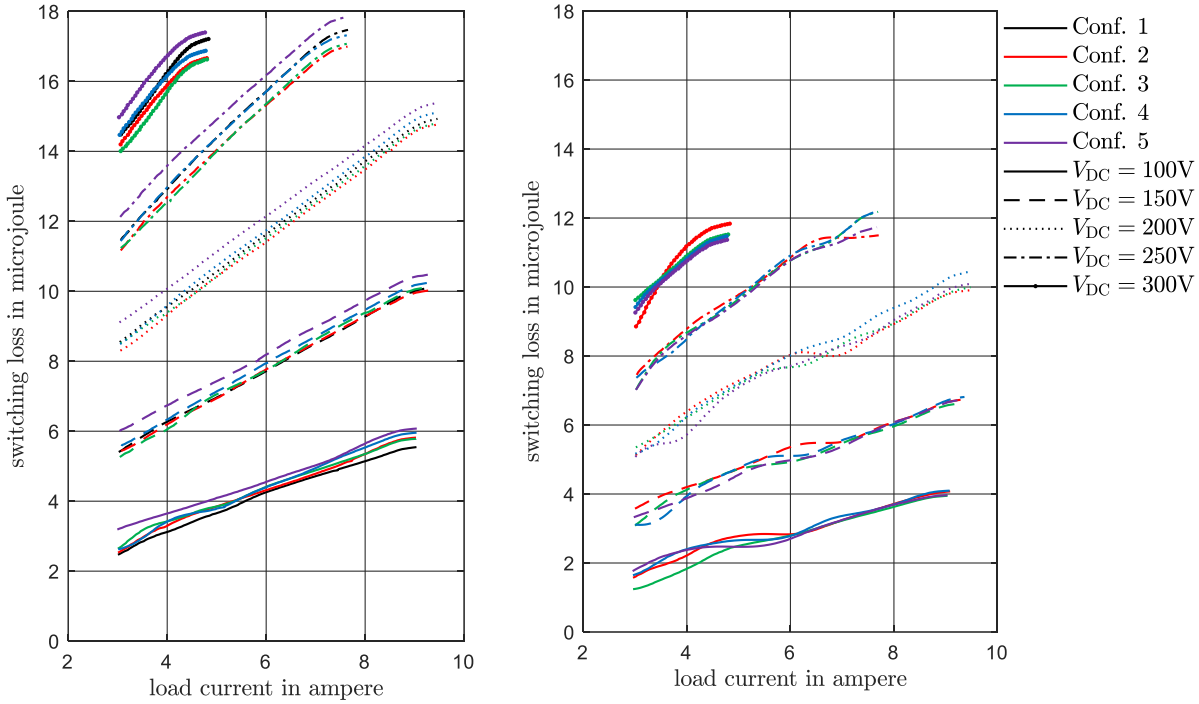


Fig. 14: Turn-off (left) and turn-on (right) transients at an inductor current of 7 A and blocking voltage of 250 V in different configurations, for the emulated MHB.



(a) (b)

Fig. 15: Switching losses for the emulated MHB (a) and the actual MHB (b).

The real MHB, with bulk connected to the lower side source, achieves slew rates of −68 V/ns at turn-on and 133 V/ns at turn-off at a blocking voltage of 250 V and an inductor current of 7 A (Fig. 16) over an interval from 20 % to 80 %. The monolithic half-bridge shows a much higher turn-off slew rate and much lower current peak at turn-on (15 A vs. 20 A) as compared to the discrete half-bridge setup (Fig. 18), reducing the switching losses by 30 % (Fig. 15). This demonstrates the benefit of the monolithic device integration in comparison with discrete devices. The improved switching performance of the MHB is a result of the lower parasitic inductance of the monolithic chip itself, as well as of the reduced parasitic capacitances of the PCB's commutation loop. However, it is currently not possible to separate

both contributions. But we may state that, independent of the studied PCB-based commutation loop, an MHB generally allows for smaller commutation loop designs. The switching transients in Fig. 17 clearly show that the four different bulk terminations have no influence on the switching transients and performance of the MHB, which verifies a sufficient immunity to back-gating effects of the presented technology also for the real monolithic half-bridge.

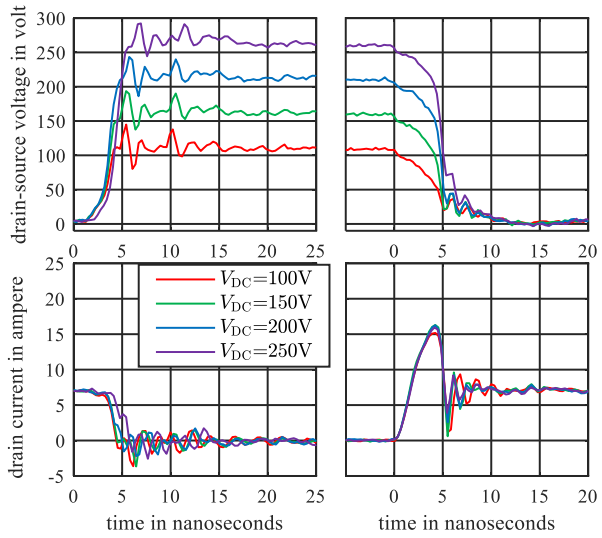


Fig. 16:Turn-off (left) and turn-on (right) transients for conf. 1 at an inductor current of 7 A and 100 V to 250 V blocking voltage, for the MHB.

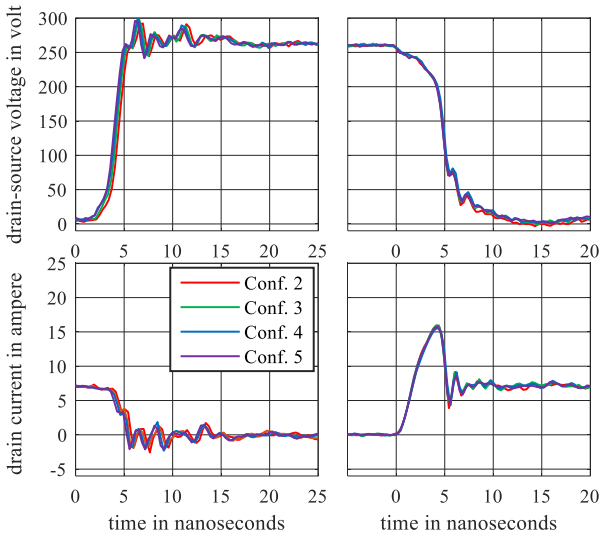


Fig. 17: Turn-off (left) and turn-on (right) transients at an inductor current of 7 A and blocking voltage of 250 V in different configurations, for the MHB.

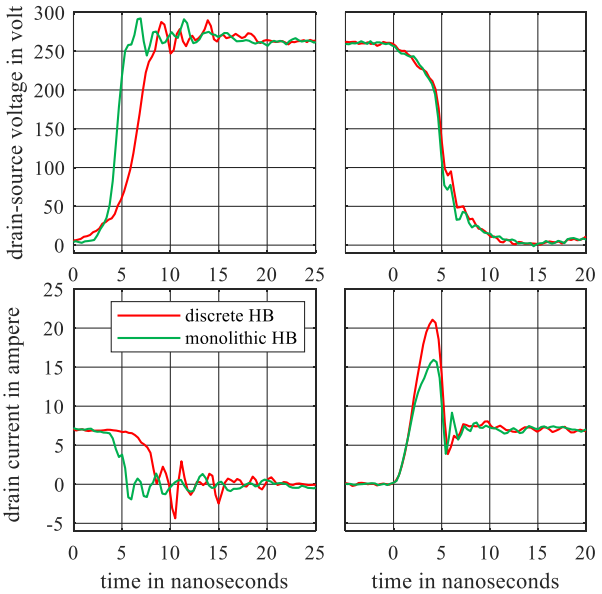


Fig. 18: Turn-off (left) and turn-on (right) transients for conf. 2 at an inductor current of 7 A and 250 V blocking voltage, for the discrete and monolithic HB.

5 Conclusion

Discrete transistors and monolithically integrated half-bridges based on a GaN-on-AlN/SiC technology are characterized to demonstrate efficient power switching with GaN monolithic integration up to 300 V. The immunity of the transistor to back-gating effects, in both its static and dynamic characteristics, is shown through I-V-measurements and double-pulse tests. The reduced coupling between the transistor's top and bottom side leads to low output and input capacitances, resulting in fast switching. The hard-switching tests reveal faster switching transients and reduced switching losses for the monolithically integrated half-bridge as compared to the half-bridge with discrete transistors.

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