Multi Busbar Sub-module Modular Multilevel STATCOM with Partially Rated Energy Storage Configured in Sub-stacks

Chuantong Hao, Wenhao Ma, Michael Merlin, Paul Judge, Stephen Finney
Institute of Energy System, School of Engineering, University of Edinburgh
Edinburgh EH9 3DW, Scotland, UK
Phone: +44 (0) 0736 75 86886
Email: Chuantong.Hao@ed.ac.uk

Acknowledgments

This work is supported by the joint scholarship of China Scholarship Council (CSC) and the University of Edinburgh.

Keywords

≪Modular Multilevel Converters (MMC)≫, ≪Multi-Busbar Submodule≫, ≪Mixed Modulation≫, ≪Static Synchronous Compensator (STATCOM)≫, ≪Partially Rated Energy Storage≫.

Abstract

This paper presents a modular multilevel STATCOM with partially rated energy storage configured in sub-stacks based on full bridge multi busbar Sub-module (SM). The soft-paralleling mechanism and doubled paths increase the current limit. The lower level controller of the proposed topology is detailed introduced and the performances are compared with a conventional single-busbar full bridge STATCOM controlled by classic SM sorting based low level controller. When providing reactive power compensation, power losses is reduced by 14.9%, and the maximum SM voltage deviation is reduced by 35.2%, while active power capability is further improved from power factor = 0.5 to power factor = 0.7 with the proposed control framework of the MBSM STATCOM.

Introduction

Static compensator (STATCOM) is commonly applied for supporting the stability of the grid by continuously absorbing or releasing reactive power in response to voltage variations [1]. Ancillary service such as inertial and frequency support is also provided when integrating STATCOM with Energy Storage (ES) Systems as active power can be extracted from or injected to ES [2]. Besides, Modular multilevel Converter (MMC) [3], [4] allows ES elements to be distributed in Sub-Modules (SM) so that the management of ES conditions can be achieved coping with MMC control algorithm.

Increasingly attention has been attracted for applications of the STATCOM with ES in distributed energy networks. Recent works have proved adapting MMC for ES will reduce harmonic distortion, switching frequency and power losses [5], [6]. Control algorithms that offer the flexibility to directly manipulate the active power components for state of charge (SoC) balancing of the batteries are presented in [7]. A delta-connected partially-rated ES STATCOM and the control structure are developed in [8]. The authors conclude that converters rated at 1 pu active power require 69% of the full bridge (FB) SMs to be integrated with ES (ES-SMs). The ES interface will be modelled as a controlled current source in simulation and analysis as its specific structure is not the focus of this paper.

Generally, additional circulating current is injected into the delta-configured loop in a STATCOM to enhance the voltage balancing of SMs and ES-SMs and increase the amount of power that can be extracted [9], [10]. However, the phase-leg current limit determines that the circulating current can not

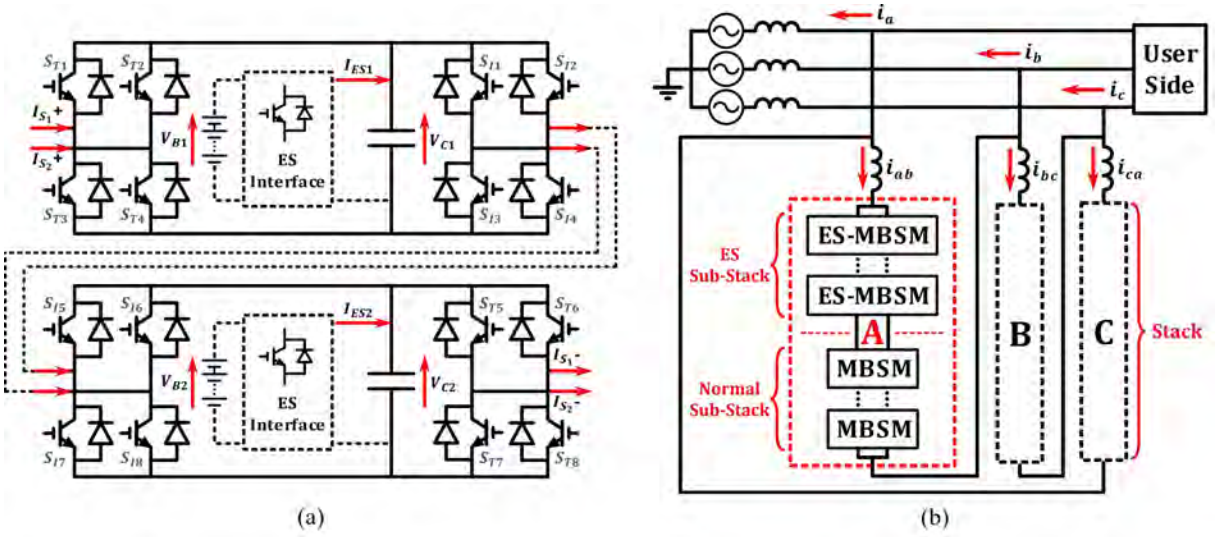


Fig. 1: The proposed topology: (a) ES-MBSMs depicting the connection manner of ES interface and two adjacent MBSMs, (b) The delta-configured MBSM PRES-STATCOM with an ES Sub-Stack and a normal Sub-Stack.

be too large, which prevents further reduction of the required ES-SMs fraction. Besides, the iterative loop algorithm calculates the gate signals at every controller step. Not only will the average switching frequency of semiconductors be large, but also the computational complexity increases sharply with the increase of the number of SMs [11].

This paper proposes a multi busbar sub-module (MBSM) based delta-configured partially-rated ES sub-stack STATCOM (PRES-STATCOM) and the corresponding mixed low level control framework. Capacitors in different MBSMs can be paralleled for energy balancing with soft-paralleling mechanism applied. The switching frequency, together with the maximum SM voltage deviation can be reduced to different extent depending the operation set-points. Since current is able to flow in two paths, MBSMs allow larger circulating current and consequently less fraction of ES MBSMs is required to release the same amount of active power compared with conventional FB based PRES-STATCOM.

The rest of the paper is organized as follows. Section 2 presents the converter topology and states of MBSMs. Section 3 introduces the low level control framework. Section 4 provides simulation results and analysis. Finally, the conclusion is presented in Section 5.

Converter Topology

Structure of MBSMs and the Proposed Converter

The structure of the ES-MBSMs together with the connection manners of the ES interface and two adjacent MBSMs are presented in Fig. 1 (a). Compared with the conventional FBSM, the MBSM consists of twice the number of interfaces, semiconductors and busbars [12] [13]. The capacitors in two adjacent MBSMs can thus be connected in parallel. As illustrated by the dotted lines, stack current is divided into two parts when flowing through MBSMs. The ES interface is connected to the SM capacitor, which could be directly-connected wires or a DC/DC converter. When the interface is disabled, the ES-MBSM becomes a capacitor-only MBSM that can only provide reactive power during normal operation.

Zero sequence circulating current results in delta-configured structure attracts more attentions than its star-configured counterpart. The circulating current amongst all three phases creates additional degrees of freedom for balancing capacitors voltage and managing SoC of the ESs. The MBSM based delta-configured PRES-STATCOM is presents in Fig. 1 (b). The stack in phase A is extended to show the detail of how different type of MBSMs are placed. ES-MBSMs and normal MBSMs are placed into two groups, forming an ES sub-stack and a normal sub-stack. The two sub-stacks can output voltage in

opposite polarities so that SM voltage balancing is promoted. The MBSM STATCOM is different from the FBSM STATCOM in structure only inside the stacks. So the same higher level control method can be applied to both topology while their low level controller should be designed separately. The detailed low level controller will be introduced in the next section.

States of MBSMs

Conventional Sub-module Based States

MBSMs are able to operate in three modes as the same of conventional FBSMs when the same gate signals are assigned to the adjacent half-bridges. Therefore, controllers for FBSMs can also be applied to MBSMs with minor adjustments. Take the upper MBSM in Fig. 1 (a) as an example, the modes and the switching states of semiconductors are:

- Positive Voltage Mode (1), when S_{T1}, S_{T2} and S_{I3}, S_{I4} are on while other switches stay off.
- Negative Voltage Mode (-1), when S_{T3}, S_{T4} and S_{I1}, S_{I2} are on while other switches stay off.
- Zero Voltage Mode (0), when S_{T1}, S_{T2} and S_{I1}, S_{I2} are on while other switches stay off.

Soft-paralleling Based States

Multi busbars can form two paths to connect the anodes and cathodes of the capacitors in two adjacent MBSMs. The capacitors can be paralleled and their voltage will be equal. The example in Fig. 1 (a) is applied again to illustrate. States of MBSMs are defined in two categories in terms of stack terminals ($S_{T1},...,S_{T8}$) and interconnections ($S_{I1},...,S_{I8}$). The modes of terminal and interconnections are presented in Fig. 2 (a) and Fig. 2 (b) respectively. The Soft-Parallel Modes are highlighted here to avoid inrush current caused by the directly paralleling of two capacitors with voltage difference. The directional conduction characteristics of anti parallel power diode limit the inrush current in the envelope formed by the stack current. Two semiconductors in the same half-bridge are blocked in soft-parallel mode, resulting in leakage current passing through the blocked semiconductors, Consequently, the soft-parallel mode can only be activated when the stack current is larger than the leakage current.

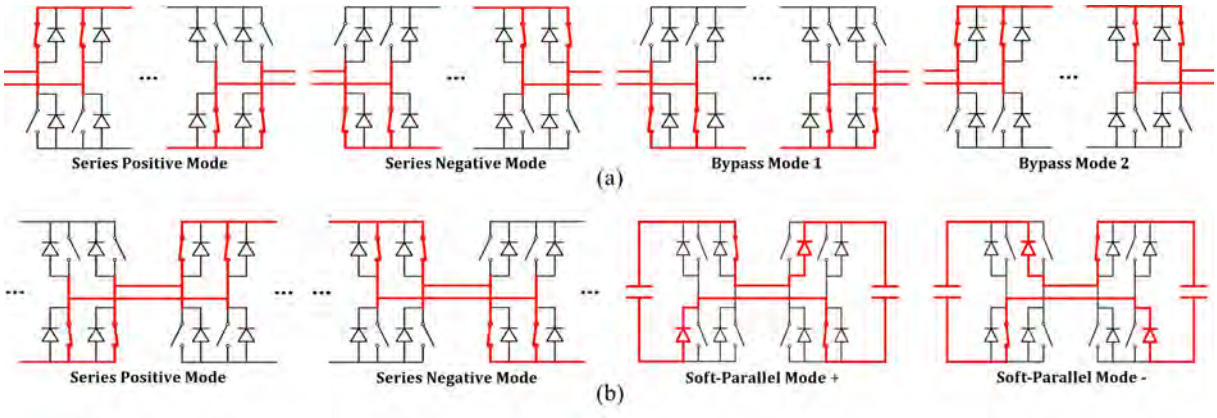


Fig. 2: MBSM states: (a) Terminal states, (b) Interconnection states.

Low Level Control System

Conventional Sub-module Based Controller

When MBSMs act as conventional FBSMs, the modes of two adjacent MBSMs can be opposite to accelerate the votlage balancing. Similar to the method proposed in [2] for PRS-MMC, the controller is an iteration algorithm which is powerful in terms of reducing the voltage differences of different capacitor at the cost of increasing computation complexity and switching frequency. The conventional sub-module based voltage balancing algorithm is summarized in **Algorithm 1**. The controller evaluates the preferential states of all MBSMs based on the SM voltages, stack current and voltage references in every controller step. The principle of preferential states is discharging the MBSM whose $V_{SM} > V_{aver}$

Algorithm 1 Conventional Sub-module based voltage balancing algorithm

Input: V_{stack}: Stack voltage reference; V_{SM}: MBSM capacitor voltages; I_{stack}: Stack current; N_{SM}: Number of MBSMs.

Output: Gate signals

Calculate average SM voltage V_{aver}, calculate sorted index R by ranking $|V_{SM} - V_{aver}|$;
Initial $V_{ref}(1) = V_{stack}$, $V_{avail}(1) = \sum V_{SM}$;
for $i = 1 \rightarrow N_{SM}$ **do**
  Set $j = 1$, calculate preferential states array S_{pref}: if $(V_C(R(j)) - V_{aver}) \cdot I_{stack} \leq 0$, $S_{pref} = [1, 0, -1]$, else $S_{pref} = [-1, 0, 1]$;
  while $(j \leq 3) \wedge (S_{pref}(j)$ is **NOT** accepted based on (1)) **do**
    $j++$;
  end while
  $V_{ref}(i+1) = V_{ref}(i) - S_{pref}(R(i)) \cdot V_{SM}(R(i)), \quad V_{avail}(i+1) = V_{avail}(i+1) - V_{SM}(R(i))$;
end for
Translate states to gate signals.

and charging the MBSM whose $V_{SM} \leq V_{aver}$ with stack current as long as the sum voltage of the rest MBSMs is higher than the remaining output voltage reference. The feasibility of the most preferential state is determined by equations (1).

$$Accept\ \ State = \begin{cases} 1, & if\ \ |V_{ref} - V_{SM}(R(j))| \leq V_{avail} - V_{SM}(R(j))/2 \\ 0, & if\ \ |V_{ref}| \leq V_{avail} - V_{SM}(R(j))/2 \\ -1, & if\ \ |V_{ref} + V_{SM}(R(j))| \leq V_{avail} - V_{SM}(R(j))/2 \end{cases} \tag{1}$$

Soft-paralleling Based Controller

Sub-stack Voltage References

Algorithm 2 Soft-paralleling based sub-stack voltage reference creation algorithm

Input: V_{stack}: Stack voltage reference; V_C: MBSM capacitor voltages; I_{stack}: Stack current; N_{ES}: Number of ES MBSMs; N_{Cap}: Number of Normal MBSMs;

Output: V_{ES}: ES sub-stack voltage reference; V_{Cap}: Normal sub-stack voltage reference; $Flag$: Flag indicating whether control the whole stack (= 1) or two sub-stacks (= 0);

1: Calculate average MBSM voltage V_{aver}, average ES-MBSM voltage V_{ESaver} and average normal MBSM voltage V_{Caver}, calculate the sign of stack current $sgn(I_{stack})$;
2: **if** $(sgn(I_{stack}) \cdot V_{stack}/V_{aver} \geq N_{Cap}) \vee (sgn(I_{stack}) \cdot V_{stack}/V_{aver} \leq -N_{ES}) \vee (V_{ESaver} < V_{Caver})$ **then**
3: $Flag = 1$;
4: **else**
5: $Flag = 0$;
6: **if** $(sgn(I_{stack}) \cdot V_{stack}/V_{aver} \geq N_{Cap} - N_{ES})$ **then**
7: $V_{ES} = V_{stack}/V_{aver} - sgn(I_{stack}) \cdot N_{Cap}, \quad V_{Cap} = sgn(I_{stack}) \cdot N_{Cap}$;
8: **else**
9: $V_{ES} = -sgn(I_{stack}) \cdot N_{ES}, \quad V_{Cap} = V_{stack}/V_{aver} + sgn(I_{stack}) \cdot N_{ES}$;
10: **end if**
11: **end if**

The first step of the soft-paralleling based controller is calculating the voltage references of the whole stack or the sub-stacks. Voltage references for two sub-stacks will be generated when the required voltage output of the whole stack is not exceed the voltage capability of sub-stacks, as presented in **Algorithm 2**. As ES currents are all charged to SM capacitors in the ES sub-stack, their voltages are more likely to

be higher than the rated value. Therefore, the ES sub-stack will be discharged by stack current while the normal sub-stack will be charged to reduce the average voltage differences.

Mixed Modulation Framework

Algorithm 3 Soft-paralleling based gate signals generation algorithm

Input: V_{ref}: Voltage reference of the stack (or sub-stack); V_{sm}: MBSM voltages of the stack (or sub-stack); $Carrier$: Carriers for all MBSMs in the stack (or sub-stack); N_{sm}: Number of MBSMs in the stack (or sub-stack); I_{stack}: Stack current;

Output: Gate signals

1: **for** $i = 1 \rightarrow N_{sm}$ **do**
2: Assign $Carrier(i)$ to the corresponding terminal or interconnections;
3: Compare $V_{ref}/\sum V_{sm}$, Get states: (1) $State(i)$ = 1, if $N_{ref} > Carrier(i)$, (2) $State(i)$ = 0, if $Carrier(i) \geq N_{ref} > -C(i)$, (3) $State(i)$ = -1, if $N_{ref} \leq -Carrier(i)$;
4: **end for**
5: Translate states to gate signals.

The second step of the soft-paralleling based controller is illustrated in **Algorithm 3**. Overall, the principle is to generate gate signals with the voltage references and the carriers. If $Flag$ = 1, the stack will be controlled as a whole part to track the voltage reference. If $Flag$ = 0, the reference voltages of two sub-stacks will be applied to allow the sub-stacks generate different voltage outputs, as long as the sum voltage is equal to the total voltage reference.

Compared to **Algorithm 1**, the computational complexity of the soft-paralleling based controller is greatly reduced. Besides, the average semiconductor switching frequency is also limited by the carrier frequency. The phase disposition and shift carrier (PDSC) modulation framework is proposed here to enhance the voltage balancing of two sub-stacks while the carriers are assigned to the whole stack. PDSC is a mixed framework of phase disposition carrier modulation (PDC) [14] and phase shift carrier modulation (PSC) [15]. The carrier with the largest average value is assigned to the interconnection between two sub-stacks to make it operate longer time at soft-paralleling mode, as illustrated by the red line in Fig. 3 (c).

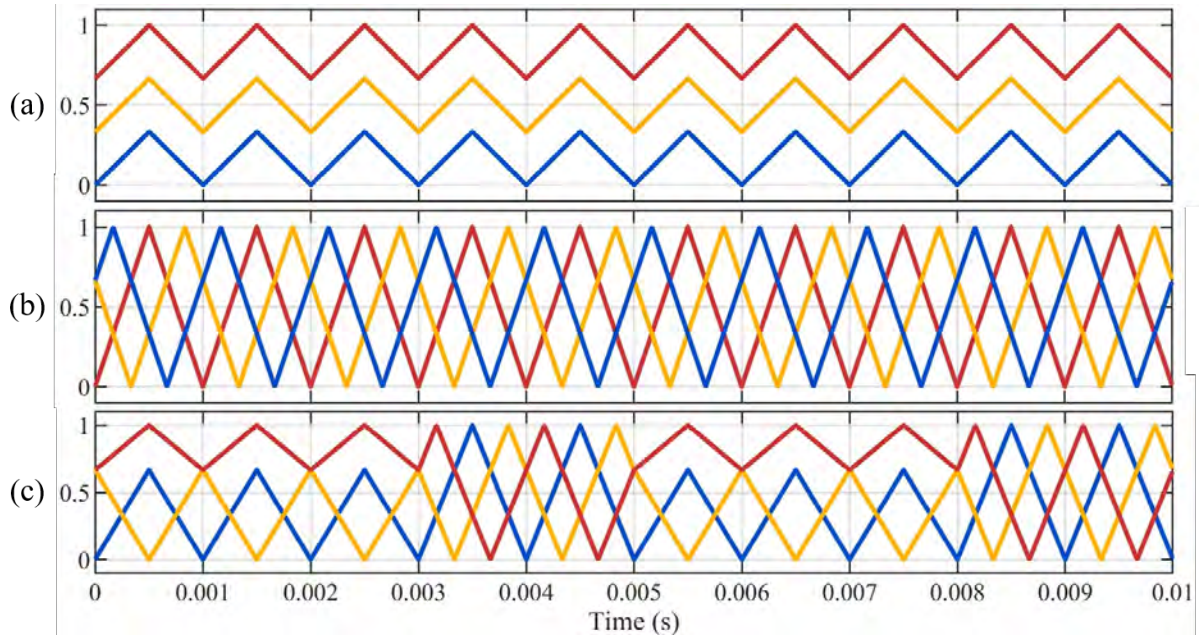


Fig. 3: Modulation frameworks: (a) Phase Disposition Carrier (PDC), (b) Phase Shift Carrier (PSC), (c) the proposed Phase Disposition and Shift Carrier (PDSC).

Controller Switching Criteria

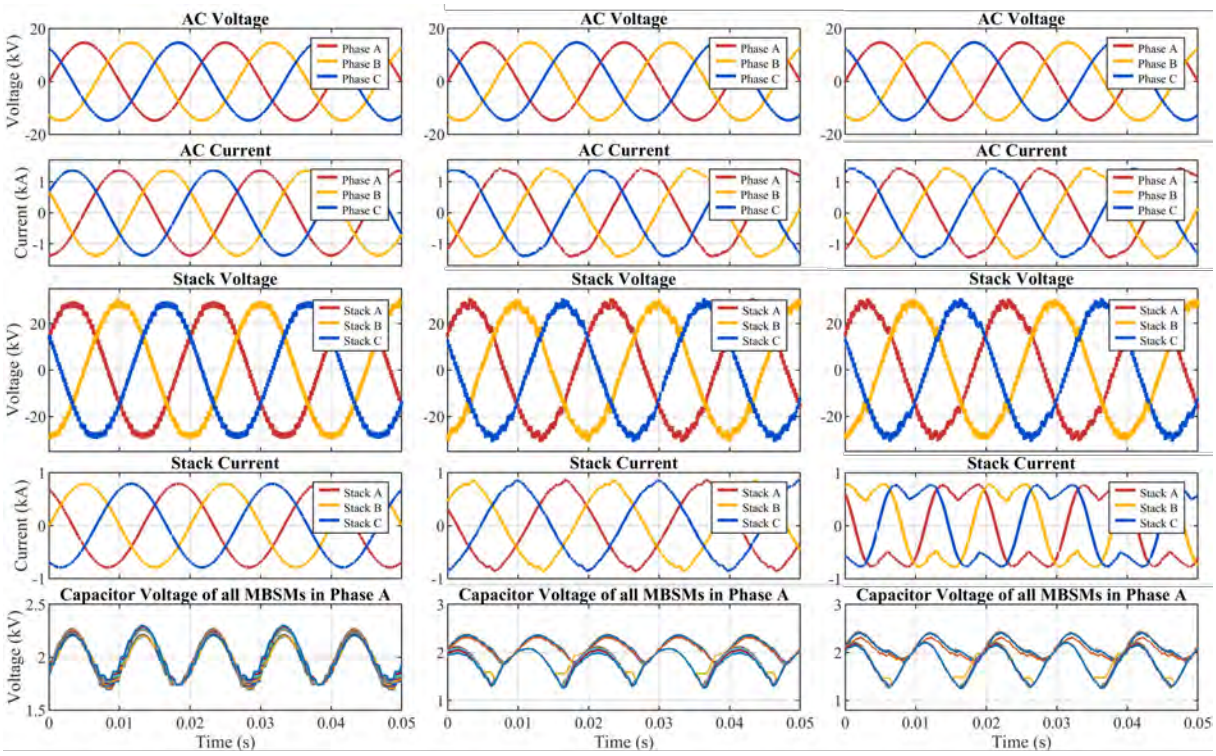
The conventional SM based controller is more powerful in terms of forcing the capacitor voltages to converge however increases the computation complexity and switching frequency. The soft-paralleling mechanism can not function when the stack current is too low to activate the power diodes as interpreted before. A stack current threshold (I_{thres}) is set to select the proper controller mode. Whenever the absolute value of the stack current is larger than I_{thres}, the soft-paralleling based mode is selected, or the MBSM STATCOM will operate in the iteration based mode.

Simulation Results and Analysis

The performances of the proposed converter are verified by a MBSM STATCOM model built in MATLAB/ Simulink and the parameters are listed in Table I. The controller step is set as 5 μs and the PDSC frequency is 500 Hz. The losses curves of the IGBT module FZ1200R33HE3 produced by $Infineon$ are applied for losses analysis.

Table I: Simulation Model Parameters

Parameters	Value	Parameters	Value
STATCOM nominal power	30 MVA	AC side line voltage (RMS)	18 kV
Nominal frequency	50 Hz	Simulation sampling time	5 μs
Branch inductance	0.1 pu	Phase inductance	0.1 pu
Nominal cell voltage	2000 V	MBSM capacitance	2.5 mF
Number of MBSMs per stack	15	Number of ES-MBSMs per stack	9



(a) (b) (c)

Fig. 4: Converter outputs when operating at: (a) $P_{ref} = 0$, $Q_{ref} = 1$ without circulating current, (b) $P_{ref} = 0.6$, $Q_{ref} = 0.8$ without circulating current, (c) $P_{ref} = 0.6$, $Q_{ref} = 0.8$ with constant amplitude (300A) third harmonic circulating current.

Fig. 4 illustrates the converter outputs at different set-points. When realising 100% reactive power, as is shown in Fig. 4 (a), the AC current and stack current are both of high quality with low THD at 0.1%. In addition, the maximum capacitor voltages deviation is approximately 9.1%. At the set-point of $P_{ref} = 0.6$ and $Q_{ref} = 0.8$ (Fig. 4 (b)), where the apparent power is equal to the former set-point, active power generated by ES-MBSMs results in voltage unbalance of different sub-stacks. The maximum SM voltage deviation increases to approximately 22.8% and consequently the output current has larger distortion. Fig. 4(c) presents the results when $P_{ref} = 0.6$ and $Q_{ref} = 0.8$ with constant amplitude (300A) third harmonic circulating current applied. The maximum voltage deviation is reduced to 19.4 %, verifying that additional circulating current is able to promote the SM voltage balancing.

The performances of the proposed MBSM STATCOM together with its low level controller are compared with a conventional FBSM STATCOM controlled by classic SM sorting low level controller [7]. The system parameters are the same as those listed in Table I. The power losses and maximum SM voltage deviation versus varying active powers with constant apparent power are illustrated in Fig. 5 and Fig. 6. The grey columns represent data when the converter is not stable. The MBSM STATCOM is able to release 0.7 pu active power while the conventional FBSM STATCOM becomes unstable when $Q_{ref} > 0.5$. The MBSM STATCOM performs better on conduction losses, switching losses and the maximum voltage deviation than its FBSM counterpart.

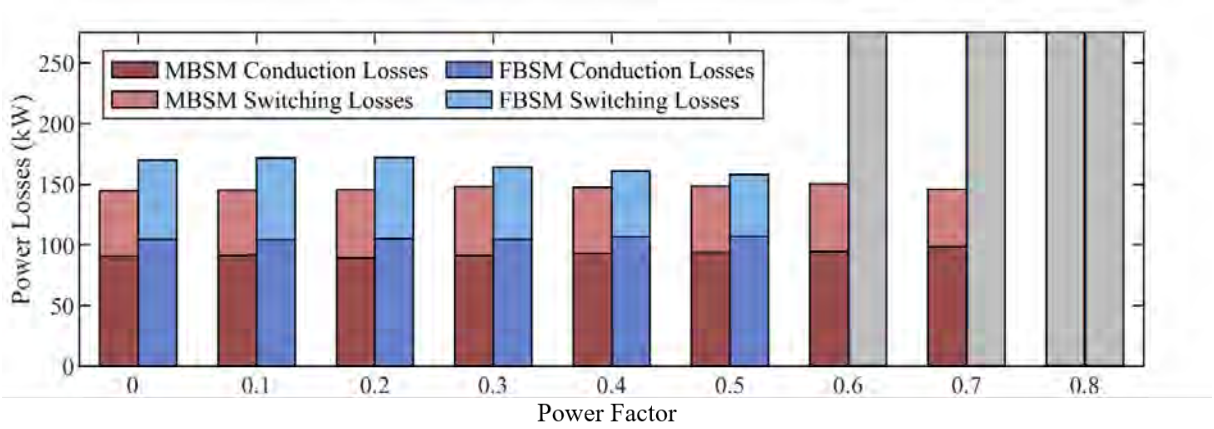


Fig. 5: Conduction losses and switching losses versus varying power factors with 1 p.u. apparent power. Grey columns represent data when the converter is not stable.

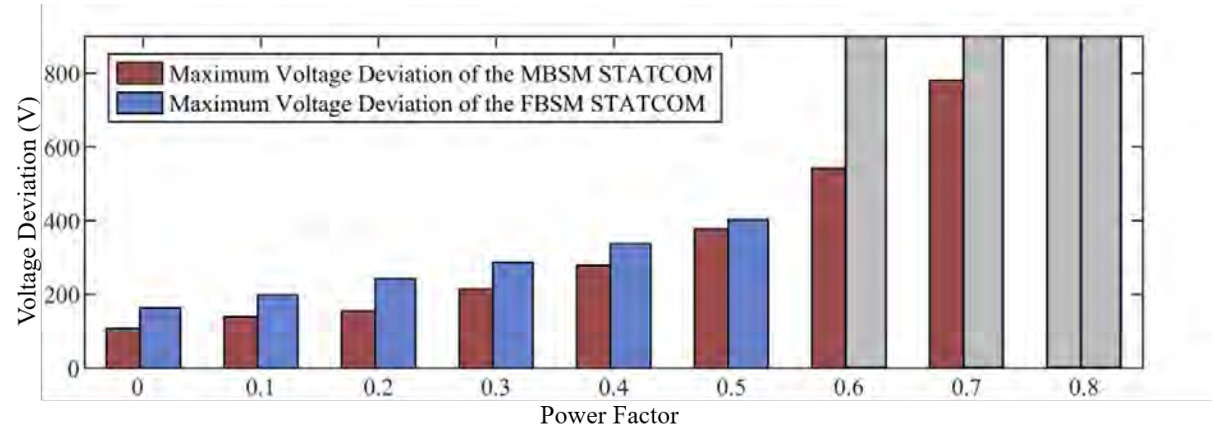


Fig. 6: Maximum SM voltage deviation versus varying power factors with 1 p.u. apparent power. Grey columns represent data when the converter is not stable.

Conclusion

This paper proposes a new type of partially rated energy storage STATCOM configured in ES-MBSM sub-stacks. The mixed control system and modulation framework are also presented. Compared with the conventional FB counterpart, the active power capability is increased from power factor = 0.5 to power factor = 0.7, while the power losses and the maximum SM voltage deviation are reduced by 14.9% and 35.2% respectively when operating at pure reactive power output. Moreover, the active power capability can be further improved with larger circulating current applied.

References

[1] J. A. Barrado, R. Grino and H. Valderrama-Blavi, "Power-Quality Improvement of a Stand-Alone Induction Generator Using a STATCOM With Battery Energy Storage System," in IEEE Transactions on Power Delivery, vol. 25, no. 4, pp. 2734-2741, Oct. 2010, doi: 10.1109/TPWRD.2010.2051565.

[2] P. D. Judge and T. C. Green, "Modular Multilevel Converter With Partially Rated Integrated Energy Storage Suitable for Frequency Support and Ancillary Service Provision," in IEEE Transactions on Power Delivery, vol. 34, no. 1, pp. 208-219, Feb. 2019, doi: 10.1109/TPWRD.2018.2874209.

[3] M. M. C. Merlin et al., "The Extended Overlap Alternate Arm Converter: A Voltage-Source Converter With DC Fault Ride-Through Capability and a Compact Design," in IEEE Transactions on Power Electronics, vol. 33, no. 5, pp. 3898-3910, May 2018, doi: 10.1109/TPEL.2017.2723948.

[4] M. Glinka and R. Marquardt, "A new AC/AC multilevel converter family," in IEEE Transactions on Industrial Electronics, vol. 52, no. 3, pp. 662-669, June 2005, doi: 10.1109/TIE.2005.843973.

[5] S. Yang, J. Fang, Y. Tang, H. Qiu, C. Dong and P. Wang, "Modular Multilevel Converter Synthetic Inertia-Based Frequency Support for Medium-Voltage Microgrids," in IEEE Transactions on Industrial Electronics, vol. 66, no. 11, pp. 8992-9002, Nov. 2019, doi: 10.1109/TIE.2018.2890491.

[6] L. Zhang, Y. Tang, S. Yang and F. Gao, "Decoupled Power Control for a Modular-Multilevel-Converter-Based Hybrid ACDC Grid Integrated With Hybrid Energy Storage," in IEEE Transactions on Industrial Electronics, vol. 66, no. 4, pp. 2926-2934, April 2019, doi: 10.1109/TIE.2018.2842795.

[7] M. Vasiladiotis and A. Rufer, "Analysis and Control of Modular Multilevel Converters With Integrated Battery Energy Storage," in IEEE Transactions on Power Electronics, vol. 30, no. 1, pp. 163-175, Jan. 2015, doi: 10.1109/TPEL.2014.2303297

[8] S. G. Mian, P. D. Judge, A. Junyent-Fer and T. C. Green, "A Delta-Connected Modular Multilevel STATCOM With Partially-Rated Energy Storage for Provision of Ancillary Services," in IEEE Transactions on Power Delivery, vol. 36, no. 5, pp. 2893-2903, Oct. 2021, doi: 10.1109/TPWRD.2020.3029312.

[9] Z. Li, R. Lizana, S. M. Lukic, A. V. Peterchev and S. M. Goetz, "Current Injection Methods for Ripple-Current Suppression in Delta-Configured Split-Battery Energy Storage," in IEEE Transactions on Power Electronics, vol. 34, no. 8, pp. 7411-7421, Aug. 2019, doi: 10.1109/TPEL.2018.2879613.

[10] W. Yang, Q. Song, S. Xu, H. Rao and W. Liu, "An MMC Topology Based on Unidirectional Current H-Bridge Submodule With Active Circulating Current Injection," in IEEE Transactions on Power Electronics, vol. 33, no. 5, pp. 3870-3883, May 2018, doi: 10.1109/TPEL.2017.2722011.

[11] A. Rashwan, M. A. Sayed, Y. A. Mobarak, G. Shabib and T. Senjyu, "Predictive Controller Based on Switching State Grouping for a Modular Multilevel Converter With Reduced Computational Time," in IEEE Transactions on Power Delivery, vol. 32, no. 5, pp. 2189-2198, Oct. 2017, doi: 10.1109/TPWRD.2016.2639529.

[12] S. M. Goetz, A. V. Peterchev and T. Weyh, "Modular Multilevel Converter With Series and Parallel Module Connectivity: Topology and Control," in IEEE Transactions on Power Electronics, vol. 30, no. 1, pp. 203-215, Jan. 2015, doi: 10.1109/TPEL.2014.2310225.

[13] Z. Li, R. Lizana F., Z. Yu, S. Sha, A. V. Peterchev and S. M. Goetz, "A Modular Multilevel Series/Parallel Converter for a Wide Frequency Range Operation," in IEEE Transactions on Power Electronics, vol. 34, no. 10, pp. 9854-9865, Oct. 2019, doi: 10.1109/TPEL.2019.2891052.

[14] A. M. Y. M. Ghias, J. Pou, G. J. Capella, V. G. Agelidis, R. P. Aguilera and T. Meynard, "Single-Carrier Phase-Disposition PWM Implementation for Multilevel Flying Capacitor Converters," in IEEE Transactions on Power Electronics, vol. 30, no. 10, pp. 5376-5380, Oct. 2015, doi: 10.1109/TPEL.2015.2427201.

[15] S. Bal, D. B. Yelaverthi, A. K. Rathore and D. Srinivasan, "Improved Modulation Strategy Using Dual Phase Shift Modulation for Active Commutated Current-Fed Dual Active Bridge," in IEEE Transactions on Power Electronics, vol. 33, no. 9, pp. 7359-7375, Sept. 2018, doi: 10.1109/TPEL.2017.2764917.