

# **A Calorimetric and Electrical Method for Measuring Loss Energies of Half-Bridges**

Jörg Haarer, Mattea Eckstein, Philipp Ziegler, Philipp Marx, David Hirning, Jörg Roth-Stielow  
INSTITUTE FOR POWER ELECTRONICS AND ELECTRICAL DRIVES

University of Stuttgart

Pfaffenwaldring 47

Stuttgart, Germany

Phone: +49 / (711) - 685-67372

Email: joerg.haarer@ilea.uni-stuttgart.de

URL: <http://www.ilea.uni-stuttgart.de>

## **Keywords**

«Device characterisation», «Switching losses», «Conduction losses», «Silicon Carbide (SiC)»

## **Abstract**

For the optimal design of power electronic systems the exact knowledge about the different loss mechanisms of the used semiconductor devices is essential. However, conventional measurement methods based on electrical parameters are facing their limits, as switching speed of modern power devices is steadily increasing enabled by the use of wide bandgap semiconductor materials. For this reason, calorimetric measurement techniques are becoming more and more popular. However, due to the nature of their principle, calorimetric measurement methodologies can usually only determine the total power losses of the device under test. To overcome this disadvantage a methodology which combines different calorimetric and electrical measurements to separately determine the switching and conduction energies in a half-bridge with an ohmic-inductive load while maintaining the accuracy of calorimetric measurement methods is developed. In addition, the presented methodology identifies the switching energies of the two different switching transitions within one switching period, depending on the load current as well as the dead time, considering thermal influences. A hardware setup for the presented methodology, is realized. Using this test setup, the loss energies of a half-bridge based on silicon carbide MOSFETs are investigated. The resulting measurements are presented and verified by measurements with a power analyzer.

## **Introduction**

Half-bridges are fundamental building blocks of numerous topologies in power electronics. Their design is crucial in terms of efficiency, volume and cost for a power electronic system. The most decisive factor is the choice of appropriate power semiconductor devices, depending on the specific application. Whereas conduction losses can be estimated using data sheet values or measured by means of DC measurements, the estimation of switching energies based on data sheet values is only possible to a very limited extent. Also the characterization of switching energies by measuring electrical variables in a double pulse test can no longer be regarded as a reliable and accurate method due to the increased use of power semiconductor devices made from semiconductor materials such as silicon carbide (SiC) and gallium nitride, because of the limited bandwidth, linearity and time synchronization of available measurement equipment [1] [2] [3]. For this reason, calorimetric measurement methods for measuring switching energies are becoming more and more popular, as they achieve a significantly better accuracy in power dissipation measurement [4] [5]. However, a major drawback of calorimetric measurement

methods is, that only the overall power losses of the device under test (DUT) can be measured [3]. In order to separate the loss energies of different loss mechanisms while maintaining the measurement accuracy of calorimetric measurement methods, a methodology, which combines a series of electrical and calorimetric measurements, is developed. This method allows the determination of the energy loss generated by different loss mechanisms during the operation of a half-bridge with ohmic inductive load. By operating a half-bridge in various operating modes, resulting in different loss mechanisms for each of those operating modes, it is subsequently possible to determine different loss mechanisms by a suitable combination of the measured power losses. In addition to the separation between switching and conduction losses, the presented method allows a further subdivision of the switching losses for the two different switching operations within a switching period. Moreover, the conduction losses can be separated into power MOSFET and body diode losses. In order to understand how the different operating modes are chosen and how the resulting losses have to be combined, it is necessary to analyze the relevant loss mechanisms in half-bridge operation of MOSFETs.

## Loss mechanisms

Loss mechanisms in SiC power MOSFETs can fundamentally be categorized into conduction and switching losses. The origin of these different loss mechanisms can be attributed to the different circuit elements in the equivalent circuit in Fig. 1. However, the temporal occurrence during a switching period differs between the different mechanisms depending on the operating conditions of the circuit [6].

The origin of conduction losses can be found in the substrate, the drift layer and, in case of the power MOSFET conducting, in the channel and in the junction field-effect transistor (green) in case of the body diode conducting, in its pn junction (blue). If the transistor is turned on, the current is conducted by the power MOSFET. If the transistor is turned off, the body diode can conduct current in reverse direction. In both cases the resulting conduction losses are calculated by (1).

$$p_{\text{cond}}(t) = i_{\text{D}}(t) \cdot v_{\text{DS,int}}(t) \quad (1)$$

Besides conduction losses, especially switching losses occur in the power MOSFET, caused by the temporal overlap of current and voltage. In the anti-parallel body diode, reverse recovery losses occur when the excess charge is removed. Further origins of switching losses are the charging/discharging process of the output capacitance  $C_{\text{OSS}}$  (orange) and oscillations (purple), induced by the resonance circuit of parasitic inductances and capacitances between drain and source of the MOSFET. In SiC-MOSFETs the reverse-recovery charge  $Q_{\text{rr}}$ , is significantly reduced in comparison to Si-MOSFETs. Oscillations take place in any switching process and are highly dependent on the parasitic inductance of the switching cell. Therefore, the impact of losses, induced by  $Q_{\text{rr}}$  and oscillations, on the overall switching losses are not considered separately. In addition to the losses of the actual power loop of the semiconductor device, gate driving losses (yellow) and ohmic losses (grey), which result from the various packaging technologies, occur. As these loss mechanisms are just a mere fraction of the overall transistor losses, the independent loss mechanisms, gate drive losses and conduction losses of the package, are neglected.

The commutation in a half-bridge always involves two transistors. During this commutation the load current  $i_{\text{L}}$  either commutates from high side to low side or from low side to high side. Each of those commutations can be subdivided into the switching transition of the prior conducting transistor (PCT) which is turned off and the switching transition of the subsequently conducting transistor (SCT) that is turned on. Also, the dependence on the direction of the load current  $i_{\text{L}}$  has to be taken into account. This results in the four cases with their corresponding switching energies listed in Tab. I.

Tab. I shows, that it is sufficient to consider only two of these cases to determine the total switching energy for a single commutation of a half-bridge as only the sign of the current through the PCT is decisive for the total switching energy of the half-bridge. As shown in Fig. 2, depending on the boundary conditions, for each of the possible cases, a tuple of switching energies results. These different switching

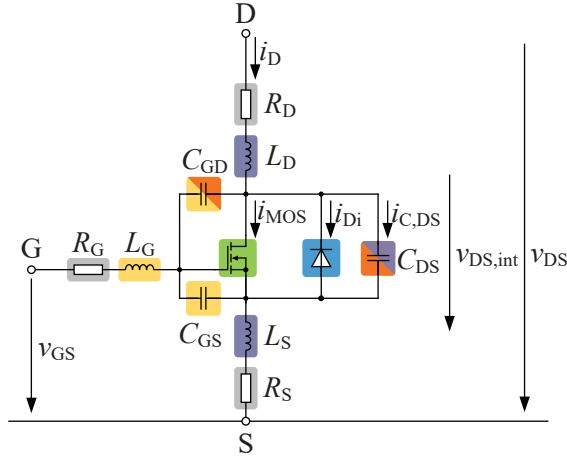


Fig. 1: Equivalent circuit of the investigated SiC-MOSFET

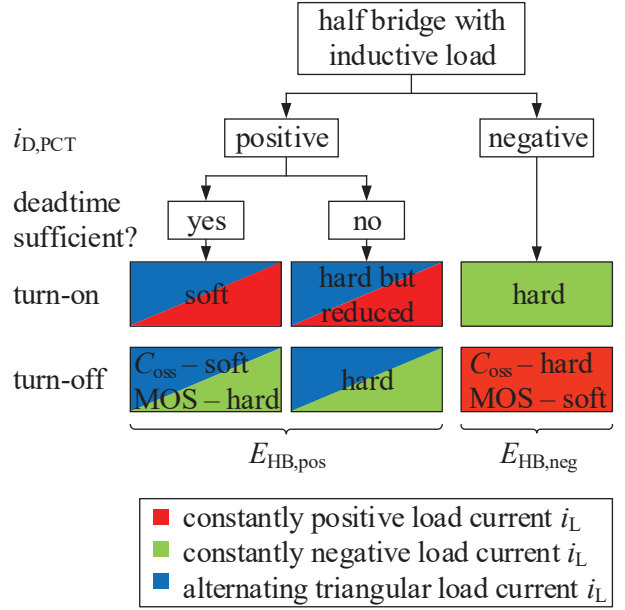


Fig. 2: Dependency of the switching losses on the direction of the PCT's drain current

Table I: Possible cases of commutations in a half-bridge with an ohmic-inductive load

commutation from	sign of $i_L$	sign of $i_{D,PCT}$	high side losses	low side losses	total losses
high side to low side	$i_L > 0$	$i_{D,PCT} > 0$	$E_{off,pos}$	$E_{on,pos}$	$E_{HB,pos}$
low side to high side	$i_L < 0$	$i_{D,PCT} > 0$	$E_{on,pos}$	$E_{off,pos}$	$E_{HB,pos}$
low side to high side	$i_L > 0$	$i_{D,PCT} < 0$	$E_{on,neg}$	$E_{off,neg}$	$E_{HB,neg}$
high side to low side	$i_L < 0$	$i_{D,PCT} < 0$	$E_{off,neg}$	$E_{on,neg}$	$E_{HB,neg}$

energies cover the entire range of switching energies that are relevant for half-bridge operation with ohmic inductive load.

In case of a negative drain current  $i_{D,PCT}$  through the PCT, switching energies are independent from the dead time, assuming a constant load current  $i_L$  for the duration of the dead time [7]. The commutation is initiated by turning off the PCT. Because of the negative drain current  $i_{D,PCT}$  in the PCT and the continuity condition of the load current  $i_L$ , the diode anti-parallel to the PCT starts to conduct the drain current. The output capacitances  $C_{OSS}$  keep their voltages and are not yet charged or discharged. As the voltage across the power MOSFET is clamped by the forward biased diode during the entire turn-off transition of the PCT, the turn off transition is a zero voltage transition regarding the power MOSFET. By turning on the SCT, the actual commutation process of the load current  $i_L$  from the PCT to the SCT is initiated. First, the SCT takes the load current from the PCT, resulting in power losses due to the temporal overlap of the voltage  $v_{DS,int}$  and the current  $i_{MOS}$ . Once the commutation of the load current  $i_L$  is completed, the anti-parallel diode of the PCT is reverse biased. Hence, the output capacitance  $C_{OSS}$  of the SCT is discharged abrupt as it is shorted by the power MOSFET. This results in a high discharge current. The whole energy  $E_{OSS}$ , stored in the output capacitance  $C_{OSS}$ , dissipates in the form of thermal energy. As the gradient of the drain-source voltage  $|dv_{DS}/dt|$  is similar in both transistors, charging the output capacitance of the PCT comes along with a large current as well. On top off the load current and the current resulting from discharging the SCT's output capacitance, an additional current that is required to charge the output capacitance of the PCT, has to be conducted by the SCT. Due to the increased current  $i_{MOS}$  in the power MOSFET, additional conduction losses occur in the power loop and leads of the transistor.

In the case of a commutation with positive drain current  $i_{D,PCT}$  through the PCT, the commutation is initiated by turning off the PCT. In contrast to the commutation with a negative current  $i_{D,PCT}$ , in this case, the charging/discharging of the output capacitances of the two transistors starts immediately when the PCT is turned off. This is due to the inductance of the load, which forces the load current into/out of the switching node of the half-bridge. Although the turn off transition of the PCT is passively relieved by its output capacitance, there are switching losses in the power MOSFET of the PCT which result from the temporal overlap of the voltage  $v_{ds,int}$  and the current  $i_{MOS}$ . The magnitude of these losses depends on the switching speed of the PCT and the load current. If the dead time and the energy stored in the inductance of the load are sufficient, the output capacitances of the transistors are fully charged/discharged by the time the SCT is turned on. The SCT can be turned on without loss at a drain-source voltage of zero volts. In this case, the energy  $E_{OSS}$  stored in the output capacitances is not dissipated into heat but recovered [8]. Furthermore, the conduction losses in the leads and interconnects also decrease due to the reduced charging currents through the PCT compared to the hard switched transition with negative drain current in the PCT.

If the SCT is not turned on immediately after the charging/discharging process, the anti-parallel diode of the SCT conducts the load current until the SCT is turned on. However, for the time period the anti-parallel diode conducts the current, conduction losses in the diode occur, which are typically higher than the conduction losses of the power MOSFET. If the dead time or the energy in the inductance of the load is too low to completely charge/discharge the output capacitances, the result is a partial zero voltage switching of the SCT.

## Measurement Methodology

In a half-bridge three possible combinations of drain currents through the PCT are possible for the individual commutations within one switching period. To investigate them, a suitable configuration of a half-bridge must be found for each combination of drain currents in the PCT. Further, the DUT must be the low side transistor  $S_{A2}$  in all of these configurations to keep the boundary conditions constant for all measurements. A constantly positive load current can be realized by the circuit in Fig. 3. The realization of a constantly negative load current is achieved by the circuit in Fig. 4. A triangular alternating load current can be obtained from the circuit in Fig. 5.

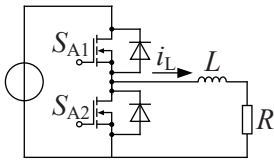


Fig. 3: Configuration for a constantly positive load current

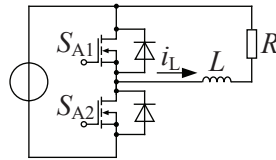


Fig. 4: Configuration for a constantly negative load current

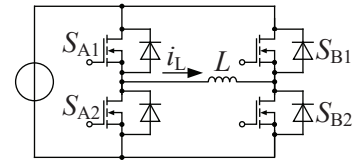


Fig. 5: Configuration for a triangular alternating load current

The overall losses  $E_{DUT}$  of the DUT are measured calorimetrically. To separate the switching energies from the conduction energies, the temporal course of the drain-source voltage  $v_{DS}$  of the DUT as well as the load current  $i_L$  are measured using an oscilloscope. The duration of power MOSFET and diode conduction is determined from the drain-source voltage. The conduction losses are calculated by (1). The voltage drop  $v_{DS,int}$  at the power MOSFET and the anti-parallel diode are predetermined by stationary DC measurements imposing a DC current into the power device [9]. To take the influence of the temperature into account, the DUT is preheated to the temperature that applies at the corresponding operating point by imposing the same overall losses by a DC current. The dependency of the power MOSFET's on state resistance  $R_{DS,on}$  on the drain current is modeled according to the datasheet values. Diode conduction losses are estimated under the assumption of a continuous drain current during dead time. The junction temperature is regarded as constant within a switching period as the duration of the switching period is

in the microsecond range. In this way, the losses in a transistor of the half-bridge can be determined for the different operating modes. The switching energies for the different cases are composed by the sum of the components marked in the same color in Fig. 2. Furthermore, the switching energies  $E_{HB,pos}$  and  $E_{HB,neg}$  that occur during commutation in the half-bridge can be determined from these measurements. As shown in Fig. 2, the switching energy of a commutation in the half-bridge with positive current through the PCT is equivalent to the switching energies of the DUT for a triangular alternating current into the load. Although there is no operation mode where the sum of the turn-on and turn-off energies  $E_{DUT,on+off}$  equals the switching energies for a negative drain current in the PCT, the switching energies for those commutations can be estimated by (2), where  $E_{DUT,iL+}$ ,  $E_{DUT,iL-}$  and  $E_{DUT,iL\sim}$  are the DUT's switching energies for constantly positive, negative or alternating triangular load current.

$$E_{HB,neg} = E_{DUT,iL+} + E_{DUT,iL-} - E_{DUT,iL\sim} \quad (2)$$

## Measurement Setup

The measurement setup is depicted in Fig. 6. The power electronic system consists of a full bridge with exchangeable ohmic-inductive load and can realize all three of the configurations from Fig. 3 to 5 [10]. The system is powered by a remotely controllable power supply (Delta Elektronika SM 500-CP-90) with an output regulation of better than 5 mV and 10 mA, which provides the voltages and currents required for the various measurements. The signal electronics consists of a control computer which implements a sequence control for the measurement procedure. A FPGA is used to generate the PWM signals. A multichannel thermometer (Pico Technology TC-08) is used to measure the DUT and the ambient temperature. An oscilloscope (Tektronix MSO 4034), a high voltage differential probe (PMK Bumblebee) and a current probe (Tektronix TCP0030A) measure the temporal courses of the drain-source voltage of the DUT and the load current. The trigger signal of the oscilloscope is generated by the control computer. For the DC voltage measurements a precision multimeter (Fluke 8845A) that provides an accuracy of 0.4 mV is used.

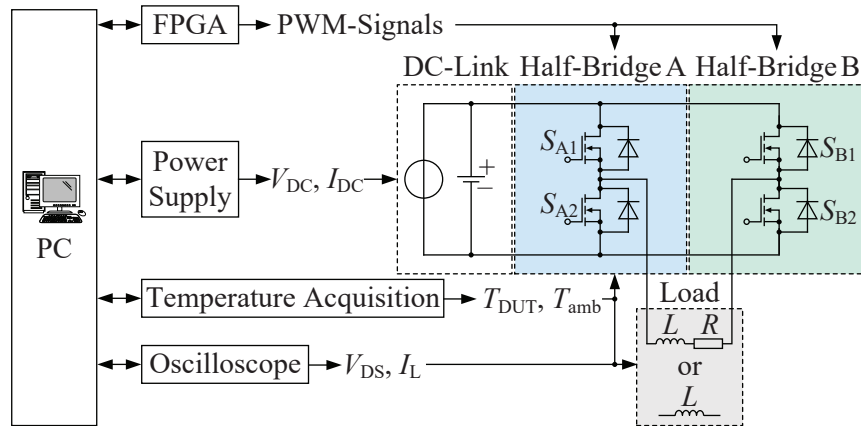


Fig. 6: Overview diagram of the measurement setup

For the realization of the calorimetric measurement system, all transistors of the full bridge are placed on identical heat sinks. In addition, the entire setup is placed in a wind tunnel to achieve the same forced convection for all transistors. By means of the multi-channel thermometer, the DUT temperature as well as the ambient temperature in the wind tunnel are measured. From the temperature difference, the total power dissipation of the DUT is determined by means of a lookup table.

In order to determine the accuracy of the calorimetric measurement method, an arbitrary sequence of measurements is performed in which well-known power losses are imposed by means of a constant DC current. The losses generated in this way are subsequently determined by the calorimetric measurement

method. The setup equals the pulsed calorimetric setup, to ensure the same thermal conditions in both, the reference, and the actual loss measurement. Fig. 7 shows the results of a calorimetric validation measurement. A sequence of operating points with different constant power losses are set one after the other in the automated process. When the thermal steady state is reached the temperature difference as well as the actual power loss are measured. The green bars show the actual DUT power loss. The red bars show the estimated DUT power loss. Most operation points show a relative deviation less than 1 percent. Only operation point three, with overall power loss less than 5 W, exceeds this limit.

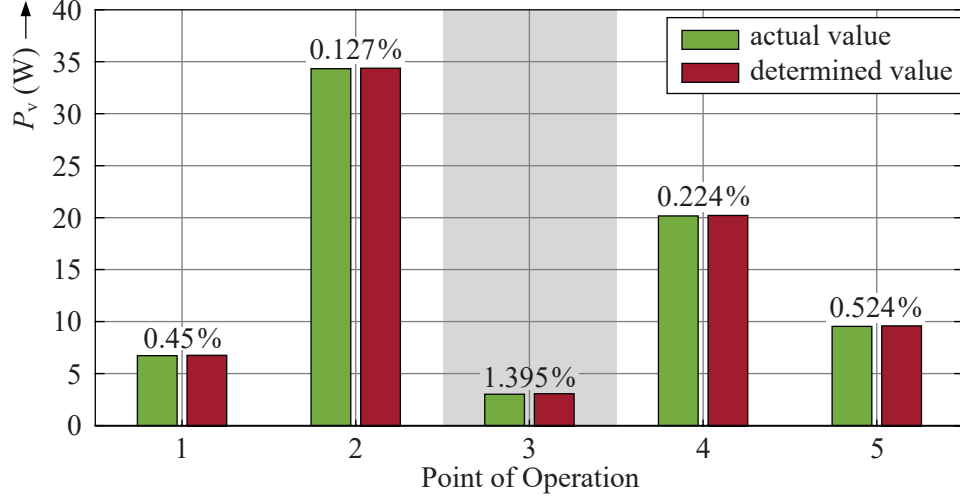


Fig. 7: Comparison between actual imposed and calorimetrically determined losses

## Results

Fig. 8 shows the power MOSFET's conduction energies  $E_{c,MOS}$ , the diode-conduction energies  $E_{c,diode}$  and the switching energies  $E_{DUT,on+off}$  of the DUT for different dead times in the range of 5 ns to 100 ns for a constant load current of 5 A.

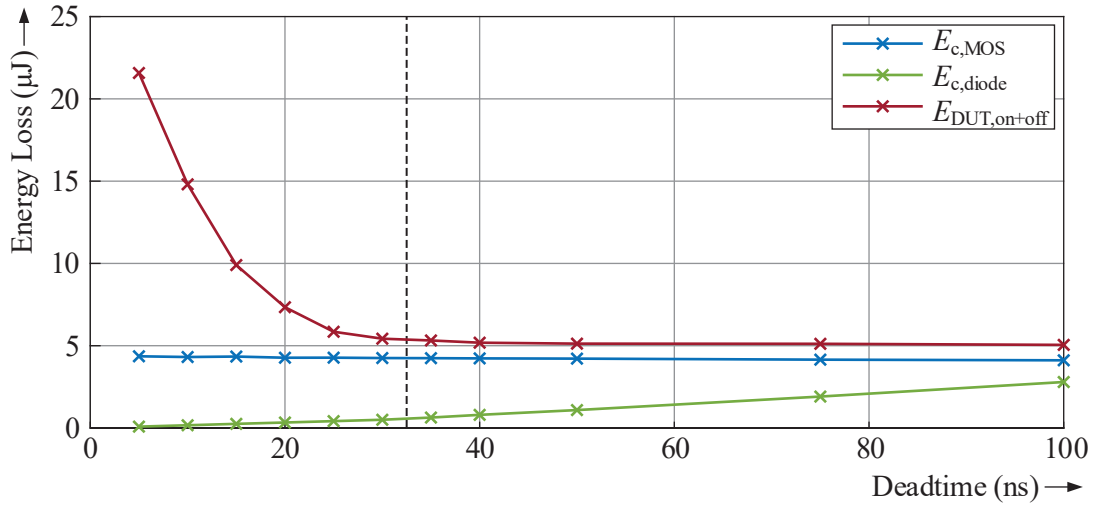


Fig. 8: Switching and conduction energies over dead time for a constant load current of 5 A through the PCT.

Power MOSFET conduction losses stay almost constant for different dead times. In contrast, diode-conduction losses increase steady over longer dead times. If the dead time is insufficient, which results in no diode conduction after turn-on, the diode conducts before turn-off. At the transition from zero voltage switching to partially zero voltage switching, the gradient of  $E_{c,diode}$  changes. For sufficient

dead times, switching losses remain roughly constant as well. As soon as dead time is insufficient,  $E_{\text{DUT, on+off}}$  starts to increase significantly. The shorter the dead time, the sooner the load current induced charging/discharging process is interrupted, the higher the power loss.

The switching energy of the half-bridge for a single commutation of the half-bridge at different load currents, dead times and operation modes is depicted in Fig. 9.

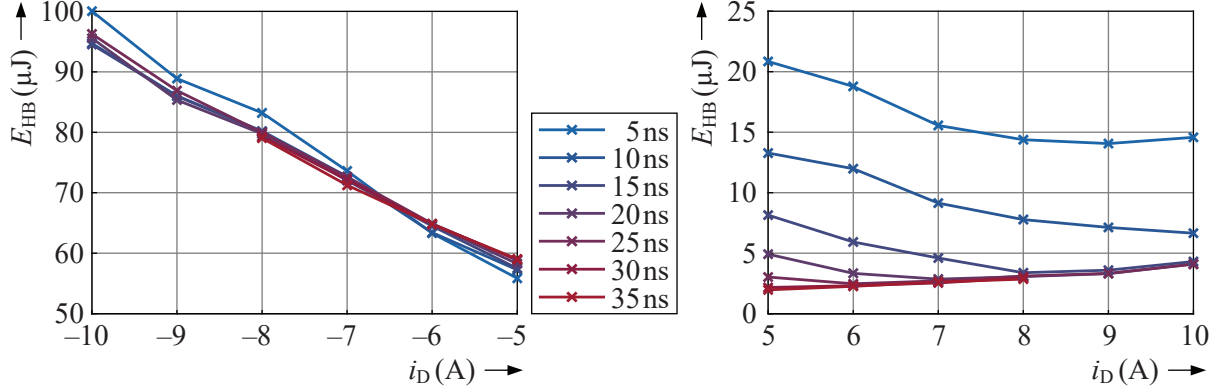


Fig. 9: Loss of a commutation over the drain current through the PCT for different dead times.

The higher the absolute value of the drain current  $i_D$ , the higher the switching energy  $E_{\text{HB}}$ , holds true for both directions of drain current in PCT and sufficient dead time. As the left figure indicates, there is no dependency of the switching energy on the dead time for negative drain currents in the PCT. In contrast, a strong dependency exists in case of a positive drain current of the PCT. A comparison of the switching energies for different positive drain currents in the PCT shows, that a higher drain current, which equals the load current right before the switching process, results in a smaller minimum sufficient dead time. In case of 5 A load current even a dead time of 25 ns is not sufficient to ensure zero voltage switching. In contrast, even 15 ns are sufficient to achieve zero voltage switching at 9 A load current.

To validate the presented methodology, a comparison between the presented methodology and measurements with a power analyzer is conducted. For this purpose, the total losses of a half-bridge for different load currents and dead times are calculated from the loss energies determined by means of the presented methodology. Afterwards, measurements are performed with a power analyzer (Zimmer LMG500). Figure 10 shows the comparison of the estimated and measured losses of a half-bridge for an constantly positive and constantly negative load current plotted over the absolute value of the inductor current for different dead times.

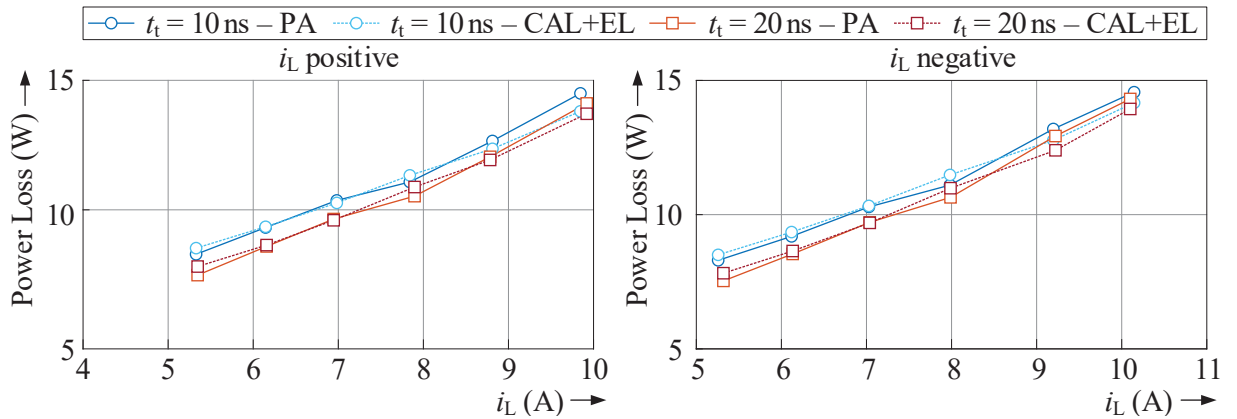


Fig. 10: Comparison between losses determined by means of the presented methodology (CAL+EL) and losses measured with a power analyzer (PA)

The measured power losses show good correlation with the estimated losses. Only minor measurement errors in the range of the measurement accuracy of the calorimetric measurement method and the power analyzer are found.

## Conclusion

The presented measurement method for the loss energies of half-bridges is simple but robust compared to exclusively electrical measurement methods such as the double pulse test. By combining calorimetric measurement methods and static electrical measurements, the complex measurement of the commutation current can be omitted. The presented method is successfully validated on the example of a SiC half-bridge. A comparison of the losses estimated by the presented method and measurements with a power analyzer are shown to validate the presented method. The measurement results show that the presented method allows to determine loss energies from which the losses for a switching operation with a given current through the PCT and the given dead time can be estimated. If operating points with a power dissipation of less than 5 W are to be measured, the thermal resistance of the DUT can be increased to improve the accuracy of the calorimetric measurement. Further the method can be improved by measuring the hysteresis losses of the transistor by means of a Sawyer Tower for more detailed analysis of the loss energies [11].

## References

- [1] M. Nitzsche, M. Zehelein, N. Troester, and J. Roth-Stielow, "Precise voltage measurement for power electronics with high switching frequencies," in *PCIM Europe 2018; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2018, pp. 1–6.
- [2] P. Ziegler, N. Tröster, D. Schmidt, J. Ruthardt, M. Fischer, and J. Roth-Stielow, "Wide bandwidth current sensor for commutation current measurement in fast switching power electronics," in *2020 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe)*, Sep. 2020, pp. P.1–P.9. [Online]. Available: <https://ieeexplore.ieee.org/document/9215686>
- [3] J. Weimer, D. Koch, R. Schnitzler, and I. Kallfass, "Determination of hard- and soft-switching losses for wide bandgap power transistors with noninvasive and fast calorimetric measurements," in *2021 33rd International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2021, pp. 327–330.
- [4] J. Weimer and I. Kallfass, "Soft-switching losses in gan and sic power transistors based on new calorimetric measurements," in *2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2019, pp. 455–458.
- [5] M. Amyotte, E. S. Glitz, C. G. Perez, and M. Ordonez, "Gan power switches: A comprehensive approach to power loss estimation," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2018, pp. 1926–1931.
- [6] A. Wintrich, U. Nicolai, W. Tursky, and T. Reimann, *Application manual power semiconductors*, 2nd ed. Ilmenau: ISLE Verlag, 2015.
- [7] J. Gareau, R. Hou, and A. Emadi, "Review of loss distribution, analysis, and measurement techniques for gan hemts," *IEEE Transactions on Power Electronics*, vol. 35, no. 7, pp. 7405–7418, 2020.
- [8] S. K. Roy and K. Basu, "Analytical model to study turn-off soft switching dynamics of sic mosfet in a half-bridge configuration," *IEEE Transactions on Power Electronics*, vol. 36, no. 11, pp. 13 039–13 056, 2021.

- [9] B. Kohlhepp, D. Kuebrich, R. Schwanninger, and T. Duerbaum, "Switching loss estimation of gan-hemts by thermal measurement procedure," in *PCIM Europe digital days 2021; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2021, pp. 1–9.
- [10] J. Brandelero, B. Cougo, T. Meynard, and N. Videau, "A non-intrusive method for measuring switching losses of gan power transistors," in *IECON 2013 - 39th Annual Conference of the IEEE Industrial Electronics Society*, 2013, pp. 246–251.
- [11] D. Bura, T. Plum, J. Baringhaus, and R. W. De Doncker, "Hysteresis losses in the output capacitance of wide bandgap and superjunction transistors," in *2018 20th European Conference on Power Electronics and Applications (EPE'18 ECCE Europe)*, 2018, pp. P.1–P.9.