New Topology of Superconducting Fault Current Limiter with Bypass Resistor

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Abstract

This paper presents a new type of bridge type SFCL with a bypass resistor. The proposed topology overcomes the drawbacks of the conventional diode bridge SFCL that can limit the fault current only during the first cycles. The proposed SFCL can limit the fault current also in the following subsequent cycles. Extensive simulations validate the proposed topology and demonstrate its advantages. The simulation results are discussed and compared to the conventional diode bridge topology. The conclusions are presented at the end of the paper.

Keywords

<<Fault handling strategy>>,<<Fault ride-through>>.

Introduction

Different types of faults in the power systems can result in destructive short circuit currents that may cause significant damage to the system's components such as generators, transformers, transmission lines, bus bars, and loads. One of the popular approaches for their limiting is to use superconducting fault current limiters (SFCL), which change their state from low impedance to high impedance during the fault currents. One of the advantages of SFCL is a very fast response that allows limiting the first peak of the fault current until the corresponding circuit breaker responds and opens the faulted line. Furthermore, more advanced SFCLs can also limit the current in the following cycles of the short circuit current.

The most common types of SFCLs that are mentioned in the literature are Inductive type SFCL which increases it's inductive impedance during high fault currents [1, 2]; Resistive type SFCL [3-7], Flux-lock type SFCL [8-12]; SMES type SFCL [13]; Shield type SFCL [14]; flux-coupling type [15-17]; Transformer type SFCL [18]–[21]; Matrix-Type SFCL [22-23]; Non-inductively wound solenoid type [24]; Dual reactor type SFCL [25].

This paper aims to improve the conventional diode bridge type SFCL. The bridge type SFCL has several advantages over other types of SFCLs: it has a fast recovery speed and can be used in situations where the protected power circuit requires auto-reclose; the superconducting coil is at the DC side of the bridge, so there is no ac power loss; in a normal situation, the voltage across the FCL is very small, and there is almost no harmonics; without magnetic core, the cost and the weight of the SFCL is lower [26-34]. The configuration of the basic diode bridge type SFCL integrated into the power line fed by voltage V_{in} is shown in Fig. 1. The superconducting coil in the center of the bridge has zero resistance and high inductance. Therefore, the voltage drops are present only on the diodes. During the fault, the reactor has high impedance and limits the first cycle of the short currents.

The major advantage of the diode bridge topology is its simple structure and low price. However, the main drawback associated with the diode bridge topology is the absence of any control, which results in a fault current limiting effect only for the first cycles, until the reactor is fully charged to the maximal value of the fault current. If the fault current continues beyond these first cycles and the corresponding circuit breaker does not respond, then the fault current will cause damage to the power system. The purpose of this paper is to solve the previously mentioned drawback of the conventional diode bridge SFCL. The paper proposes a more advanced bridge-type topology with a bypass resistor that allows limiting fault current not only during the first cycles but also for the next coming cycles.

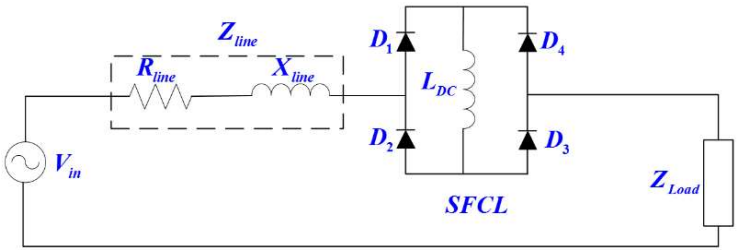


Fig. 1. Conventional diode bridge type SFCL.

The rest of the paper is organized as follows: Section II presents the proposed topology, section III presents simulation results and their analysis, and section IV presents the conclusions.

The proposed topology and its control

The proposed SFCL is shown in Fig. 2. It is comprised of the bridge and parallel-connected bypass resistor R_{Bypass}. The resistor can be connected or disconnected from the bridge by the bypass switch S_{Bypass} comprised of two back-to-back connected thyristors. The bypass switch is used only as an on/off switch without using turn on and off angles. This fact significantly simplifies the control of the SFCL.

The proposed SFCL bridge has two gate turn-off thyristors (GTOs) T_1 and T_4 that allow connection or disconnection of the reactor L_{DC} from the line. It is important to note that the state of the thyristors T_1 and T_4 is always opposite to the state of the bypass switch.

The pair of GTOs is turned on only during the first cycles of the fault current, during which the fault current is limited by the impedance of the reactor L_{DC}. The number of these cycles is defined by the controller. If during these first cycles the corresponding circuit breaker did not trip the power line, then the GTOs T_1 and T_4 are turned off disconnecting the reactor from the line and the bypass switch S_{Bypass} is turned on. In this case, the fault current will be limited by the bypass resistor. When GTOs T_1 and T_4 are turned off, the reactor parallel diode prevents high voltage spikes on the reactor by allowing the reactor to discharge through it.

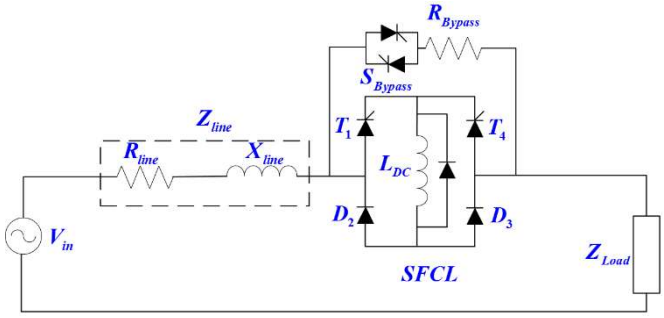


Fig. 2. The proposed SFCL.

The proposed topology can be designed for different values of the fault current by connecting several bypass resistors as shown in fig. 3. In this case, seven combinations of the bypass resistance values can be obtained by simultaneous switching of two or three switches: R_{Bypass_1}, R_{Bypass_2}, R_{Bypass_3}, $R_{Bypass\_1}//R_{Bypass\_2}$, $R_{Bypass\_1}//R_{Bypass\_3}$, $R_{Bypass\_2}//R_{Bypass\_3}$ and $R_{Bypass\_1}//R_{Bypass\_2}//R_{Bypass\_3}$. The value of the bypass resistor can be calculated by:

$$R_{Bypass} = \frac{V_{in}}{I_k} - (Z_{line} + Z_{fault} \,||\, Z_{load}), \tag{9}$$

where I_k is the value of the limited fault current, Z_{line} is the impedance of the line, Z_{fault} is the impedance of the fault to the ground and Z_{load} is the impedance of the load.

The number of bypass resistors is defined by the designer of the SFCL according to the desired resolution of the current limiting and the system's price. The energy rating of the bypass resistors depends on the value of the fault current at

the time point of switching off GTOs and turning on bypass switches.

When the fault current is limited by the reactor (bypass resistor is switched off), the limited fault current has two operation modes. The first mode takes place twice in each period during source voltage positive and negative half-cycles. In the charging mode, during which the current through the reactor equals the absolute value of the load current, the KVL of the charging circuit can be described by:

$$V_{in} = (R_{line} + R_{Load})i_{load} + (L_{line} + L_{Load} + L_{DC})\frac{di_{load}}{dt} + 2V_{TF}. \tag{1}$$

The fault current during the charging mode is described by:

$$i_{load\_ch}(t) = e^{\frac{-(R_{line}+R_{Load})}{L_{line}+L_{Load}+L_{DC}}(t-t_0)}[i_{load\_ch(I.C.)} - \frac{\sqrt{2}V}{|Z_0|}\sin(\omega t_0 - \theta_0) + \frac{2V_{TF}}{R_{line}+R_{Load}}] + \frac{\sqrt{2}V}{|Z_0|}\sin(\omega t - \theta_0) - \frac{V_{TF}+V_{DF}}{R_{line}+R_{Load}}, \tag{2}$$

where V_{TF} is the voltage drop across thyristors (its value is typically 0.8 to 1.0 V), V_{DF} is the voltage drop across diodes, and $i_{load\_ch(I.C.)}$ is the initial condition of the reactor charging current. The charging mode impedance modulus is given by

$$|Z_0| = \sqrt{(R_{line} + R_{Load})^2 + (X_{line} + \omega L_{DC} + X_{Load})^2}, \tag{3}$$

and the angle of the charging circuit impedance, which includes the line, reactor, and load impedances, is given by

$$\theta_0 = tg^{-1}\frac{\omega(L_{line} + L_{Load} + L_{DC})}{R_{line} + R_{Load}}. \tag{4}$$

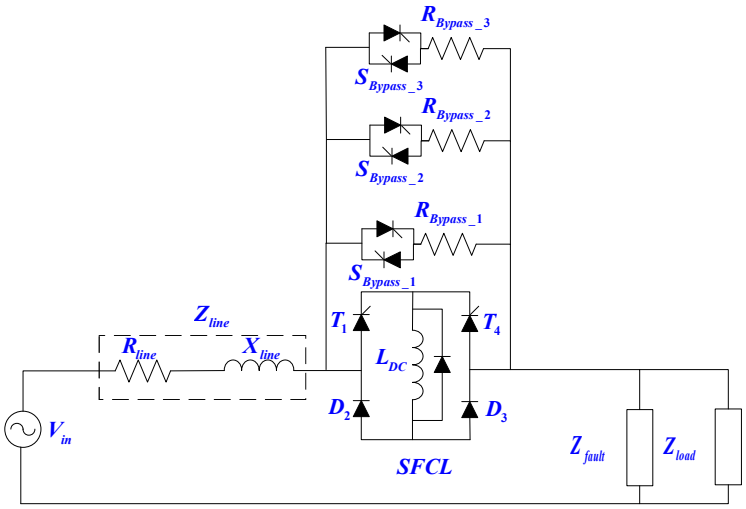


Fig. 3. The proposed SFCL with three bypass resistors.

During the freewheeling mode that takes place when the reactor is charged to its maximum value, the reactor current begins to decrease and the polarity of the voltage drop across the reactor reverses. At this moment, the pair of previously non-conducting thyristors and the diode is turned ON additionally to the thyristors and diode that were already conducting, i.e., all four semiconductors conduct and the freewheeling mode starts. The reactor L_{DC} freewheels, discharging through all four thyristors. The KVL of the freewheeling circuit can be described by:

$$V_{in} = (R_{line} + R_{Load})i_{load} + (X_{line} + X_{Load})\frac{di_{load}}{dt} \tag{5}$$

The fault current during the freewheeling mode is described by:

$$i_{load\_fw}(t) = e^{\frac{-(R_{line}+R_{Load})}{L_{line}+L_{Load}}(t-t_1)}[i_{load\_fw(I.C.)} - \frac{\sqrt{2}V}{|Z_1|}\sin(\omega t_1 - \theta_1)] + \frac{\sqrt{2}V}{|Z_1|}\sin(\omega t - \theta_1), \tag{6}$$

where and $i_{load\_fw(i.c)}$ is the initial condition of the freewheeling current.

The freewheeling mode impedance modulus is given by $|Z_1| = \sqrt{(R_{line} + R_{Load})^2 + (X_{line} + X_{Load})^2}$, (7)

while the angle of the freewheeling mode impedance, which includes line and load impedances, is given by

$$\theta_1 = tg^{-1} \frac{\omega(L_{line} + L_{Load})}{R_{line} + R_{Load}}. \quad (8)$$

The reactor current is given by

$$i_{LDC}(t) \cong \frac{\sqrt{2}V}{|Z_1|} - \frac{V_{TF} + V_{DF}}{L_{DC}} t.$$

The control unit of the proposed SFCL is shown in Fig. 4. The "fault current detection" block receives at its input the measured line current and checks if its value exceeds the defined normal threshold value. While the value of the line current is below this threshold, the current is defined as "normal" and GTOs are turned on while all bypass switches are turned off. When the value of the line current becomes higher than the threshold, the control will turn off the GTOs after the delay that defines how many cycles will be limited by the bridge. The "Bypass resistance selection block" receives at its input the gating pulse of the GTOs and line current. It reverts the GTOs gating pulse by using the "Not" logical operator. Afterward, it calculates the corresponding bypass resistance that will limit the fault current to the desired value in the following cycles. As was explained before, the number of bypass resistor combinations is limited by the number of resistors. Therefore, this block can calculate and choose the limited fault current from several possible options that are defined by the number of the bypass resistors combinations.

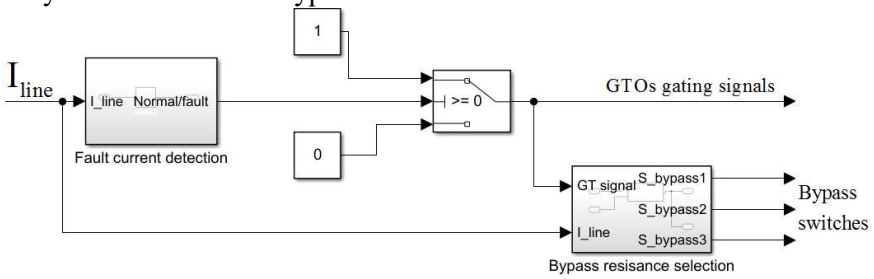


Fig. 4. The control unit of the proposed SFCL with three bypass resistors.

Validation and analysis

This section presents the simulations of the proposed SFCL for different delay times and resistors combinations. All simulations were performed by Simulink program. They are compared to the simulation of the conventional diode bridge that is shown in Fig. 5. The simulation parameters are shown in Table I. In all simulations, the short circuit to the ground starts at the time point of 0.04sec.

TABLE I. SYSTEM PARAMETER VALUES USED IN ACCOMPANYING SIMULATIONS

Parameter	Value	Units
Supply voltage, V_{in}	22	*kV*
SFCL reactance, L_{DC}	40	*mH*
Line impedance, Z_{line}	0	*Ω*
Base frequency, ω	100π	*rad/s*
Load impedance, Z_{Load}	100 + *jπ*	*Ω*
Thyristors forward voltage drop, V_{TF}	1	*V*
R_{Bypass_1}	20	*Ω*
R_{Bypass_2}	30	*Ω*
R_{Bypass_3}	40	*Ω*

The simulations presented in Fig. 6 show that the proposed topology is working and capable of limiting the fault

current to the desired values as long as needed and not only during the first cycles as a conventional diode bridge does. The timing of the transition from the bridge to the bypass path is defined by the user according to the expected fault currents. As shown in the simulations, the value of the limited current can change according to the combination of the bypass resistances. When the fault current is limited by the reactor, its waveform is not sinusoidal and behaves according to the charging and freewheeling modes. When the fault current is limited by the bypass resistors, its waveform is purely sinusoidal. As a result, harmonic pollution is eliminated.

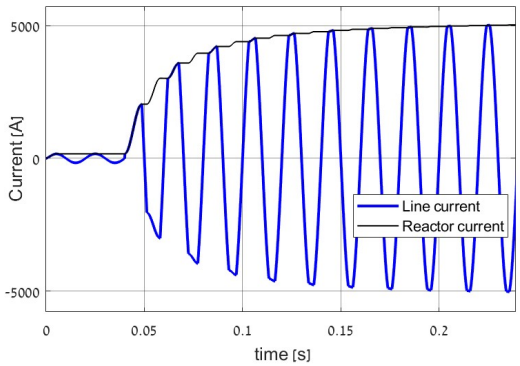
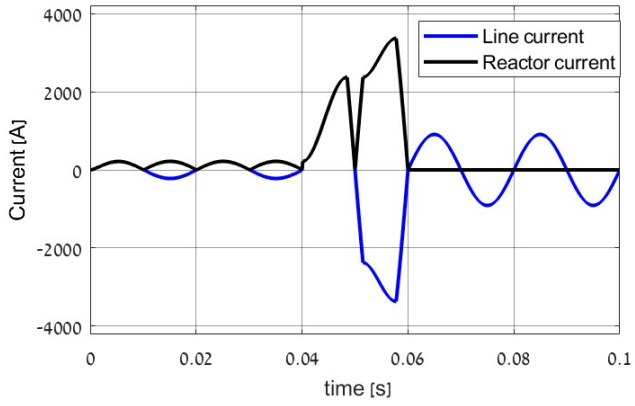
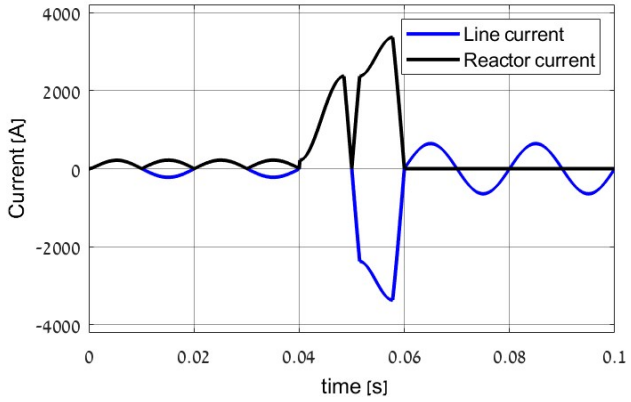


Fig. 5. The simulated line current and reactor current of the conventional diode bridge. Normal operation mode is during the time interval of 0<t<0.04s while 0.04<t- fault state. It can be seen from Fig. 5 that the diode bridge SFCL limits the fault current only during the first six cycles after which the fault current is maximal again.



(a)



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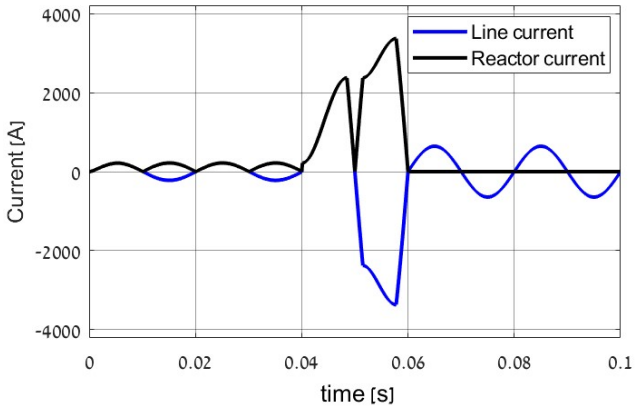

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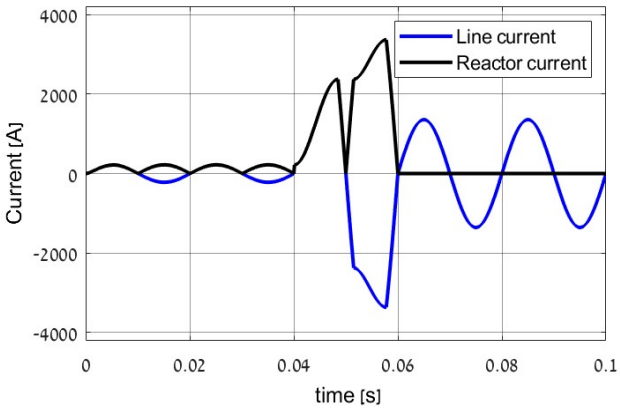

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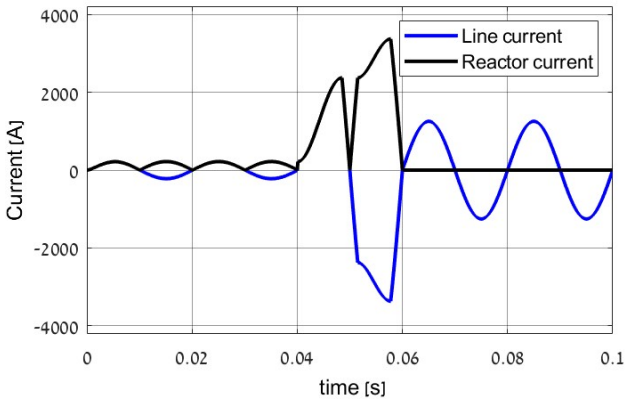
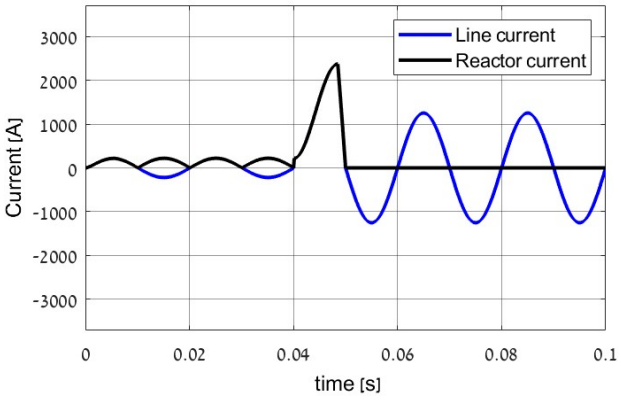
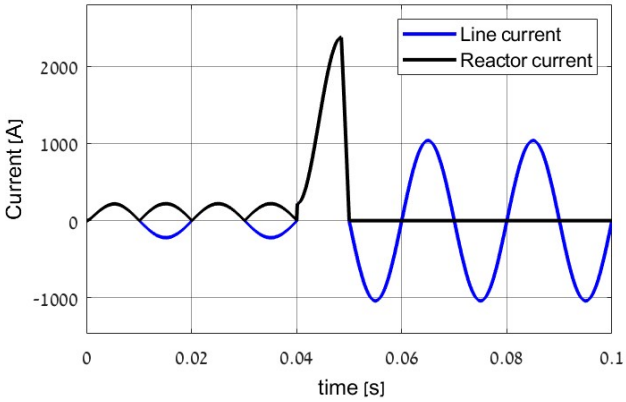


(e)



(f)



(g)

Fig. 6. The simulated line current and reactor current of the proposed SFCL. (a) The switch S_{Bypass}_1 is switched on at a time point of 0.06sec. The bypass resistance is 20Ω; (b) The simulated line current and reactor current of the proposed SFCL. The switch S_{Bypass}_2 is switched on at a time point of 0.06sec. The bypass resistance is 30Ω; (c) The switch S_{Bypass}_3 is switched on at time point of 0.06sec. The bypass resistance is 40Ω; (d) The switches S_{Bypass}_1 and S_{Bypass}_2 are switched on at a time point of 0.06sec. The total bypass resistance is 12Ω; (e) The switches S_{Bypass}_1 and S_{Bypass}_3 are switched on at a time point of 0.06sec. The total bypass resistance is 13.33Ω; (f) The simulated line current and reactor current of the proposed SFCL. The switches S_{Bypass}_1 and S_{Bypass}_3 are switched on at a time point of 0.05sec. The total bypass resistance is 13.33Ω; (g) The simulated line current and reactor current of the proposed SFCL. The switches S_{Bypass}_2 and S_{Bypass}_3 are switched on at a time point of 0.05sec. The total bypass resistance is 17Ω.

Conclusions

This paper proposed a new topology of the bridge type SFCL with parallel bypass resistors. The operation of the SFCL was validated by extensive simulations. The proposed topology has several advantages. The first advantage is simple control and structure. The second advantage is its ability to limit the fault current to the desired value as long as needed and not only during the first cycles. The third advantage is the ability to change limited fault current according to the possible combinations of the bypass resistors. However, the increase in the number of possible combinations results in more parallel paths that complicate the structure of the SFCL and results in a bigger size and higher price.

References

[1] T. Janowski, G. Wojtasiewicz, B. Kondratowicz-Kucewicz, S. Kozak, J. Kozak, and M. Majka, "Superconducting winding for inductive type SFCL made of HTS tape with increased resistivity," *IEEE Trans. Appl. Supercond.*, vol. 19, no. 3, pp. 1884–1887, 2009.

[2] S. Kozak, T. Janowski, G. Wojtasiewicz, J. Kozak, B. Kondratowicz- Kucewicz, and M. Majka, "The 15 kv class inductive SFCL," *IEEE Trans. Appl. Supercond.*, vol. 20, no. 3, pp. 1203–1206, 2010.

[3] S. Imparato, A. Morandi, L. Martini, M. Bocchi, G. Grasso, M. Fabbri, F. Negrini, and P. Ribani, "Experimental evaluation of ac losses of a DC restive SFCL prototype," *IEEE Trans. Appl. Supercond.*, vol. 20, no. 3, pp. 1199–1202, 2010.

[4] A. Morandi, S. Imparato, G. Grasso, S. Berta, L. Martini, M. Bocchi, M. Fabbri, F. Negrini, and P. Ribani, "Design of a DC resistive SFCL for application to the 20 kv distribution system," *IEEE Trans. Appl. Supercond.,* vol. 20, no. 3, pp. 1122–1126, 2010.

[5] Z. He and S. Wang, "Design of the electromagnetic repulsion mechanism and the low-inductive coil used in the resistive-type superconducting fault current limiter," *IEEE Trans. Appl. Supercond.*, vol. 24, no. 5, pp. 1–4, 2014.

[6] H. S. Ruiz, X. Zhang, and T. Coombs, "Resistive-type superconducting fault current limiters: concepts, materials, and numerical modeling," *IEEE Trans. Appl. Supercond.*, vol. 25, no. 3, pp. 1–5, 2015.

[7] S. H. Lim and J. C. Kim, "Quench and recovery characteristics of series connected resistive type SFCL s with magnetically coupled shunt-reactors," IEEE Trans. Appl. Supercond., vol. 18, no. 2, pp. 729–732, 2008.

[8] S. H. Lim, J. C. Kim, and B.-W. Lee, "Improvement of recovery characteristics of a flux-lock type SFCL using a superconductor's trigger," *IEEE Trans. Appl. Supercond.*, vol. 20, no. 3, pp. 1182–1185, 2010.

[9] H. S. Choi and S.-H. Lim, "Operating performance of the flux-lock and the transformer type superconducting fault current limiter using the YBCO thin films," *IEEE Trans. Appl. Supercond.*, vol. 17, no. 2, pp. 1823–1826, 2007.

[10] S. C. Ko and S. H. Lim, "Analysis on magnetizing characteristics due
to peak fault current limiting operation of a modified flux-lock-type SFCL with two magnetic paths," *IEEE Trans. Appl. Supercond.*, vol. 26, no. 4, pp. 1–5, 2016.

[11] S. H. Lim, S. W. Lee, Y. H. Moon, J. C. Kim, and T. K. Ko, "Power quality improving operations of a flux-lock type SFCL integrated with voltage or current controlled-voltage source inverter," *IEEE Trans. Appl. Supercond.*, vol. 18, no. 2, pp. 644–647, 2008.

[12] J. S. Kim, S. H. Lim, and J. Kim, "Study on protection coordination of a flux-lock type SFCL with over-current relay," *IEEE Trans. Appl. Supercond.*, vol. 20, no. 3, pp. 1159–1163, 2010.

[13] G. Zhu, Z. Wang, X. Liu, G. Zhang, and X. Jiang, "Transient behavior research on the combined equipment of SMES-SFCL," *IEEE Trans. Appl. Supercond.*, vol. 14, no. 2, pp. 778–781, 2004.

[14] A. Hekmati, "Proposed design for a tunable inductive shield-type SFCL,"
IEEE Trans. Appl. Supercond., vol. 24, no. 4, pp. 1–7, 2014.

[15] L. Ren, Y. Tang, Z. Li, L. Chen, J. Shi, F. Jiao, and J. Li, "Techno- economic evaluation of a novel flux-coupling type superconducting fault current limiter," *IEEE Trans. Appl. Supercond.*, vol. 20, no. 3, pp. 1242–1245, 2010.

[16] S. Yan, L. Ren, Z. Wang, Z. Yang, Y. Xu, L. Chen, B. Yu, Y. Tang, and
S. Liang, "Simulation analysis and experimental tests of a small-scale flux-coupling type superconducting fault current limiter," *IEEE Trans. Appl. Supercond.*, vol. 27, no. 4, pp. 1–5, 2016.

[17] H. S. Choi, B. I. Jung, and Y. S. Cho, "Transient characteristics of a flux- coupling type superconducting fault current limiter according to winding direction," *IEEE Trans. Appl. Supercond.*, vol. 19, no. 3, pp. 1827–1830, 2009.

[18] S. G. Choi, H. S. Choi, and K. H. Ha, "Analysis of recovery characteristics of three-phase transformer type vol. 20, no. 3, pp. 1242–1245, per types of faults according to reclosing system," *IEEE Trans. Appl. Supercond.*, vol. 22, no. 3, pp. 5 601 204–5 601 204, 2012.

[19] H.-S. Choi and Y.-S. Cho, "Critical current equalization via neutral lines in a transformer-type vol. 20, no. 3, pp. 1242–1245," *IEEE Trans. Appl. Supercond.*, vol. 18, no. 2, pp. 733–736, 2008.

[20] K. Fushiki, T. Nitta, J. Baba, and K. Suzuki, "Design and basic test of SFCL of transformer type by use of Ag sheathed BSSCO wire," *IEEE Trans. Appl. Supercond.*, vol. 17, no. 2, pp. 1815–1818, 2007.

[21] H. Yamaguchi, K. Yoshikawa, M. Nakamura, T. Kataoka, and K. Kaiho, "Current limiting characteristics of transformer type superconducting fault current limiter," *IEEE Trans Appl. Supercond*., vol. 15, no. 2, pp. 2106–2109, 2005.

[22] D. C. Chung, B. H. Pak, Y. S. Cho, B. I. Jung, H. S. Han, M. H. Kwak, S.
B. Kang, H. W. Oh, T. H. Sung, T. H. Han et al., "Increase of current limiting capacity of SFCLs by using matrix-type SFCL

module," *IEEE Trans. Appl. Supercond.*, vol. 21, no. 3, pp. 1280–1283, 2011.

[23] B. I. Jung, Y. S. Cho, H. S. Choi, and D.-C. Chung, "Recovery characteristics of three-phase matrix-type SFCL in ground fault," *IEEE Trans. Appl. Supercond.*, vol. 20, no. 3, pp. 1229–1232, 2010.

[24] J. B. Na, H. Kang, and T. K. Ko, "Numerical analysis and electrical insulation design of a single-phase 154kv class non-inductively wound solenoid type superconducting fault current limiter," *IEEE Trans. Appl. Supercond.*, vol. 22, no. 3, pp. 5 602 104–5 602 104, 2012.

[25] S.-H. Lim, H.-S. Choi, and B.-S. Han, "Fault current limiting characteristics of DC dual reactor type SFCL using switching operation of HTSC elements," *IEEE Trans. Appl. Supercond.*, vol. 16, no. 2, pp. 723–726, 2006.

[26] Fei, Wanmin, and Bin Wu. "A novel topology of bridge-type superconducting fault current limiter" *Canadian Conference on Electrical and Computer Engineering, CCECE'09*, vol. 21, no. 7, pp. 2201 – 2204, 2009.

[27] L. Li, L. Gong, X. Xu, J. Lu, Z. Fang, and H. Zhang, "Field test and demonstrated operation of 10.5 kv/1.5 kA HTS fault current limiter," *IEEE Trans. Appl. Supercond.*, vol. 17, no. 2, pp. 2055–2058, 2007.

[28] H. J. Boenig, C. H. Mielke, B. L. Burley, H. Chen, J. A. Waynert, and J. O. Willis, "The bridge-type fault current controller-a new facts controller," *Power Engineering Society Summer Meeting,* vol. 1. pp. 455–460, 2002.

[29] T. Hoshino, K. M. Salim, M. Nishikawa, I. Muta, and T. Nakamura, "DC reactor effect on bridge type superconducting fault current limiter during load increasing," *IEEE Trans Appl. Supercond*., vol. 11, no. 1, pp. 1944–1947, 2001.

[30] K. M. Salim, T. Hoshino, A. Kawasaki, I. Muta, and T. Nakamura, "Waveform analysis of the bridge type SFCL during load changing and fault time," *IEEE Trans Appl. Supercond*., vol. 13, no. 2, pp. 1992–1995, 2003.

[31] L. Jiang, J. X. Jin, and X. Y. Chen, "Fully controlled hybrid bridge type superconducting fault current limiter," *IEEE Trans. Appl. Supercond*., vol. 24, no. 5, pp. 1–5, 2014.

[32] H. You and J. Jin, "Characteristic analysis of a fully controlled bridge type superconducting fault current limiter," *IEEE Trans. Appl. Supercond*., vol. 26, no. 7, pp. 1–6, 2016.

[33] M. C. Ahn and T. K. Ko, "Proof-of-concept of a smart fault current controller with a superconducting coil for the smart grid," *IEEE Trans. Appl. Supercond.*, vol. 21, no. 3, pp. 2201–2204, 2011.

[34] M. Firouzi, G. Gharehpetian, and B. Mozafari, "Bridge-type superconducting fault current limiter effect on distance relay characteristics," *Int. J. Electr. Power Energy Syst*., vol. 68, pp. 115–122, 2015.