Four-Level Boost Inverter Based on ANPC Topology with Switched-Capacitor Branch

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Keywords

«Multi-level inverters», «DC-AC converter», «Voltage Source Inverter (VSI)», «Boost», «Switched capacitor».

Abstract

This paper presents a novel single-stage four-level inverter with voltage-boosting ability. In comparison to the cascaded topology, the proposed converter allows for the elimination of a power choke on the DC side. The inverter topology and its special switching algorithm are demonstrated and verified by simulations and experiments.

Introduction

Multilevel inverters (MLIs) have been widely investigated for applications at low, medium, and high voltages [1–2]. The special features of MLIs are low voltage stress of switches, low total harmonic distortion, low du/dt load stress, low filtering requirements, and high modularity [3]. Traditional MLIs use three topologies: cascaded H-bridge (CHB), flying capacitor (FC), and neutral point clamped (NPC) inverters. However, these topologies do not ensure any voltage gain, and, therefore, applications that involve low-voltage DC input (such as photovoltaic systems and electric vehicle drives) require a DC-DC boost converter at the input or a transformer at the output. This can cause additional losses and costs [4]. In addition to traditional MLIs, hybrid multilevel topologies, such as active neutral point clamped (ANPC) inverters, have been continuously researched. An example is a five-level NPC inverter (5L-ANPC) [5] that combines the features of a 3L-NPC and a 3L-FC to generate a five-level output voltage waveform. Its advantage is a good trade-off between the reduced number of components and single DC-link operation, but it has no voltage-boosting capability.

Recent research has focused on switched-capacitor-based MLIs (SCMLIs), which can overcome the drawbacks of traditional MLIs. The switched-capacitor principle involves a parallel connection of the capacitors to the DC source for charging and a series connection for discharging. Thus, the SCs add several levels to the output waveform and simultaneously offer a voltage gain [6–17]. The topologies presented in [6–7] are based on the concept of SC and possess modularity characteristics. However, their drawback is a high voltage stress of semiconductor switches, making them unsuitable for high-voltage applications. In [8], the authors demonstrate how a single unit of the basic cell may generate a seven-level output voltage waveform. As the design includes a symmetrical voltage source, the requirement for numerous sources and polarity generation via an H-bridge makes the architecture more expensive and less desirable. The topologies described in [12–14] use a larger number of switching components while achieving a low gain. Moreover, another seven-level structure [16] achieves a gain of less than unity and employs additional switching components. The SCMLI in [17] synthesizes seven levels with a voltage boosting capability three times the input voltage, but has the disadvantage of causing excessive voltage stress of switches. The topologies described in [9–11], [15] offer a limited voltage gain. Further examples of inverters, suitable for single- and three-phase high-power systems, achieved on the basis of NPC or ANPC multilevel inverters, are demonstrated in [18–24].

This paper presents a novel single-stage four-level inverter with voltage-boosting ability (Fig. 1). In comparison to the cascaded topology, the proposed converter allows for the elimination of a power choke on the DC side. The inverter topology and its special switching algorithm are demonstrated and verified by simulations and experiments.

Principle of operation

The proposed inverter is based on the ANPC topology with an auxiliary switched capacitor (SC) resonant branch. The switched capacitor (C_S) transfers energy between the DC-link capacitors (C_1 and C_2) and the third DC capacitor C_3. The SC branch can operate during the states that generate medium voltages on the output; therefore, this circuit can be used in all cases of modulation. Figs. 2 and 3 present the idea of inverter operation with marked current paths.

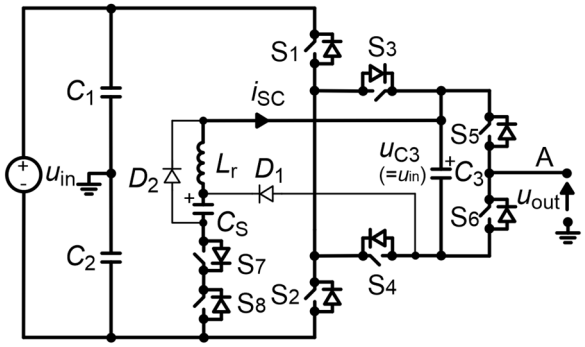


Fig. 1: The proposed four-level switched-capacitor boost inverter in a single-phase implementation

The diagrams presented in Fig. 2 show that the states where the low positive voltage is generated (SP1a and SP1b) are redundant. In state SP1a, the switched capacitor C_S can be recharged in the circuit with the DC-link capacitors and in state SP1b - with capacitor C_3. This allows to maintain the voltage on the DC-link parts equal during the operation with both active or reactive power:

$$U_{C3} = U_{in} \tag{1}$$

The switching pattern for the modulation on the highest positive levels should contain the switching states SP1a and SP1b alternately and is the following:

$$\text{SPp} = \{\text{SP1a, SP2, SP1b, SP2, SP1a, …}\} \tag{2}$$

According to the principle of symmetry, the switching pattern for the modulation on the lowest negative output voltage levels is the following:

$$\text{SPn} = \{\text{SN1a, SN2, SN1b, SN2, SN1a, …}\} \tag{3}$$

The states SN2, SN1a, and SN1b are presented in Fig. 3.

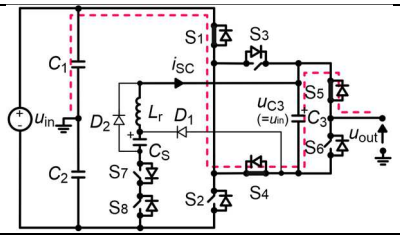
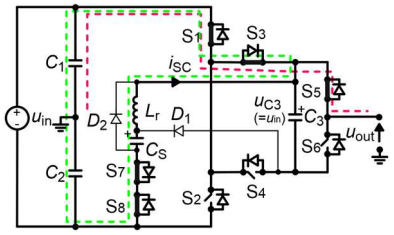
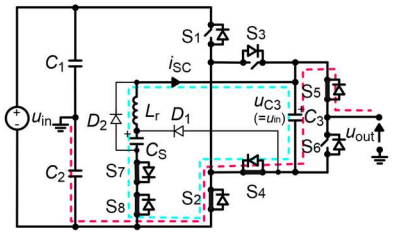
	STATE	OUTPUT VOLTAGE
Positive State 2 (SP2) The highest positive voltage of a branch		$U_{out} = 0.5U_{in}+U_{C3} = 0.5U_{in}+U_{in} = 1.5U_{in}$ SC circuit is not triggered.
Positive State 1a (SP1a) Low positive voltage of a branch		$U_{out} = U_{C1} = 0.5U_{in}$ SC circuit connected to the DC-link. Active power operation - C_S is being charged from the DC-link. Reactive power operation - C_S is being discharged to the DC-link. Capacitor C_3 is not used to supply the load.
Positive State 1b (SP1b) Low positive voltage of a branch		$U_{out} = -U_{C2}+U_{C3} = 0.5U_{in}$ SC circuit connected to the DC capacitor C_3. Active power operation - C_S is being discharged to capacitor C_3. Reactive power operation - C_S is being charged from capacitor C_3.

Fig. 2: Single phase states with the highest positive voltage ($U_{out} = 1.5U_{in}$) and two redundant states with low positive voltage ($U_{out} = 0.5U_{in}$)

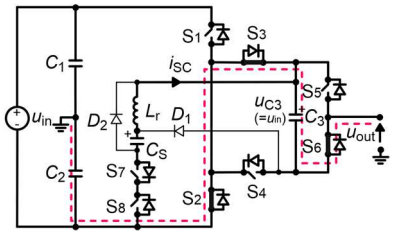
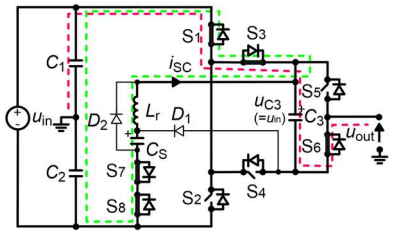
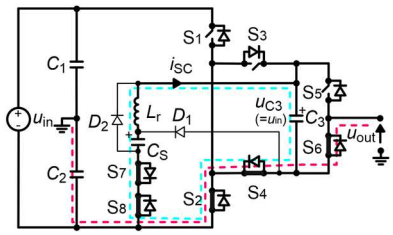
	STATE	OUTPUT VOLTAGE
Negative State 2 (SN2) The highest value of negative voltage of a branch		$U_{out} = -0.5U_{in} - U_{C3} = -0.5U_{in} - U_{in} = -1.5U_{in}$ Circuit SC is not triggered
Negative State 1a (SN1a) Low negative voltage of a branch		$U_{out} = 0.5U_{in} - U_{C3} = -0.5U_{in}$ SC circuit connected to the DC-link. Active power operation - C_S is being charged from the DC-link. Reactive power operation - C_S is being discharged to the DC-link.
Negative State 1b (SN1b) Low negative voltage of a branch		$U_{out} = -U_{C2} = -0.5U_{in}$ SC circuit connected to the DC capacitor C_3. Active power operation - C_S is being discharged to capacitor C_3. Reactive power operation - C_S is being charged from capacitor C_3. Capacitor C_3 is not used to supply the load.

Fig. 3: Single-phase states with the highest value of negative voltage ($U_{out} = -1.5U_{in}$) and two redundant states with low negative voltage ($U_{out} = -0.5U_{in}$)

For modulation on medium levels, the capacitor C_3 may be not affected or may operate as a flying capacitor when the following switching patterns are used:

$$SPpn(1) = \{SP1a, SN1b, \ldots\} \quad (4)$$

In this switching pattern, capacitor C_3 is not affected. Transistors S_7 and S_8 may be turned off during this part of the fundamental frequency period (marked in Fig. 4).

$$SPpn(2) = \{SP1b, SN1a, \ldots\} \quad (5)$$

In this case, capacitor C_3 is charged and discharged as a flying capacitor.

Figure 4 presents the switching pattern for a single-phase inverter in the proposed topology. Four-level modulation is accomplished together with energy exchange between capacitor C_3 and DC-link capacitors C_1 and C_2. The energy exchange is supported by the switched capacitor C_S. The branch composed of the capacitor C_S and the resonant inductor L_r is connected in parallel to the DC link or the capacitor C_3. The current of the L_rC_S branch is oscillatory. Since the duty cycle of switching signals varies, the current oscillation in the L_rC_S circuit is terminated after various time intervals. When the converter operates in non-ZCS mode, diodes D_1 and D_2 allow the current of the resonant choke to circulate, which is presented in Fig. 5.

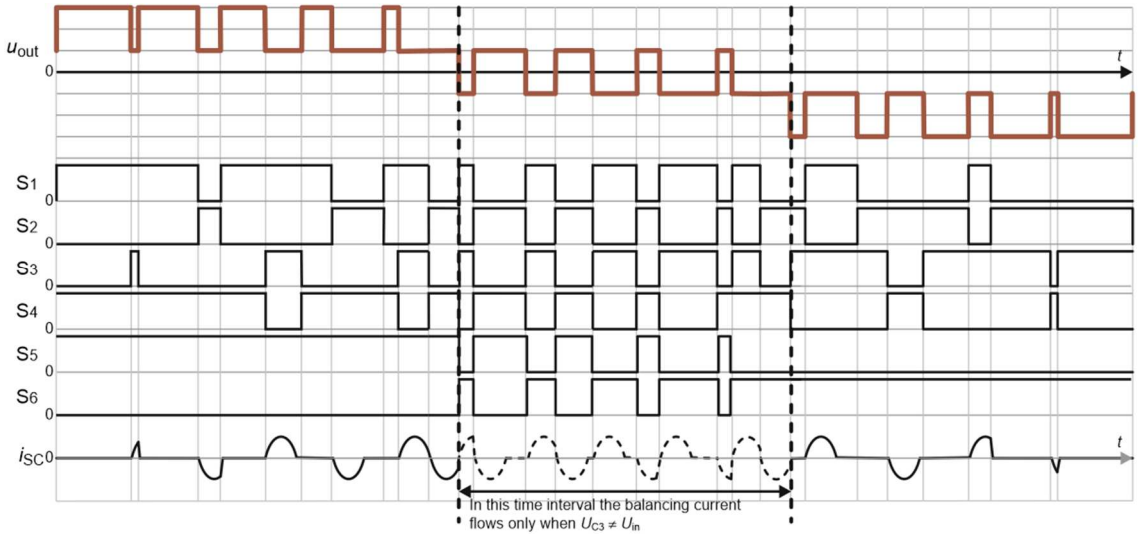


Fig. 4: Operation of a single-phase inverter: output voltage, modulation pattern, and idealized waveform of current in the resonant inductor L_r ($i_{SC} = i_{Lr}$)

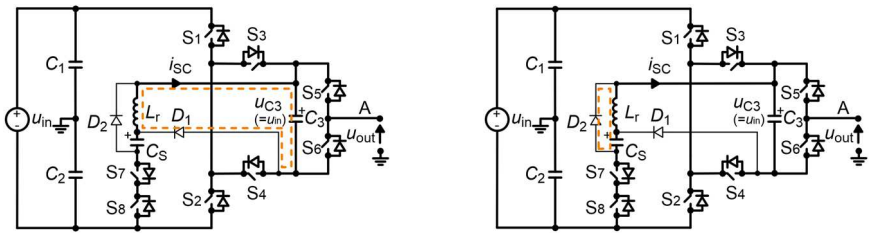


Fig. 5: Operation of auxiliary diodes in non-ZCS mode during the dead time

The SC circuit converts only a fraction of the total converter power and utilizes a very low-volume resonant choke. In comparison to the cascaded topology composed of a boost and an inverter, the proposed converter allows the removal of a power choke on the DC side.

Simulation results

Simulation tests of the proposed circuit have been carried out in MATLAB/Simulink environment for the following parameters: $U_{in} = 300$ V, $L_r = 2$ µH, $C_S = 4.7$ µF, $C_3 = 470$ µF where U_{AC_rms} is 230 V and switching frequency f_{sw} is 50 kHz. As can be seen in Fig. 6, an additional LC filter with the following parameters was used at the output: $L_F = 300$ µH, $C_F = 4.7$ µF (resonant frequency is $f_g = 4.23$ kHz).

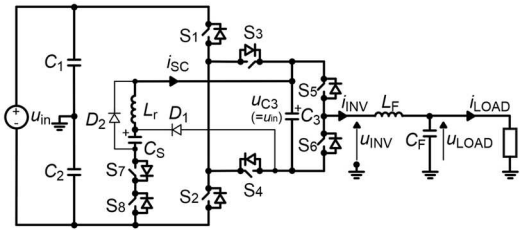


Fig. 6: Schematic of the simulated circuit

Figure 7 presents the switching signals together with the output current and voltage waveforms in a time period of 20 ms, obtained for P_{out} = 1 kW. The current and voltage waveforms of the components are presented in Figs. 8a) and 8b), respectively.

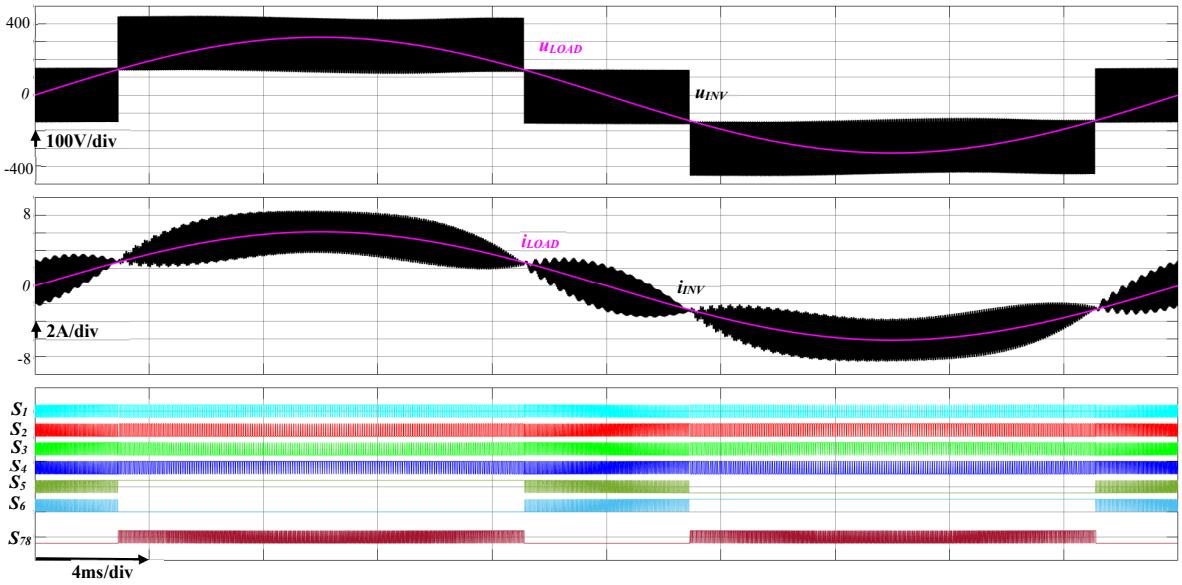


Fig. 7: PWM switching signals, output current, and voltage waveforms in a time period of 20 ms (for P_{out} = 1 kW).

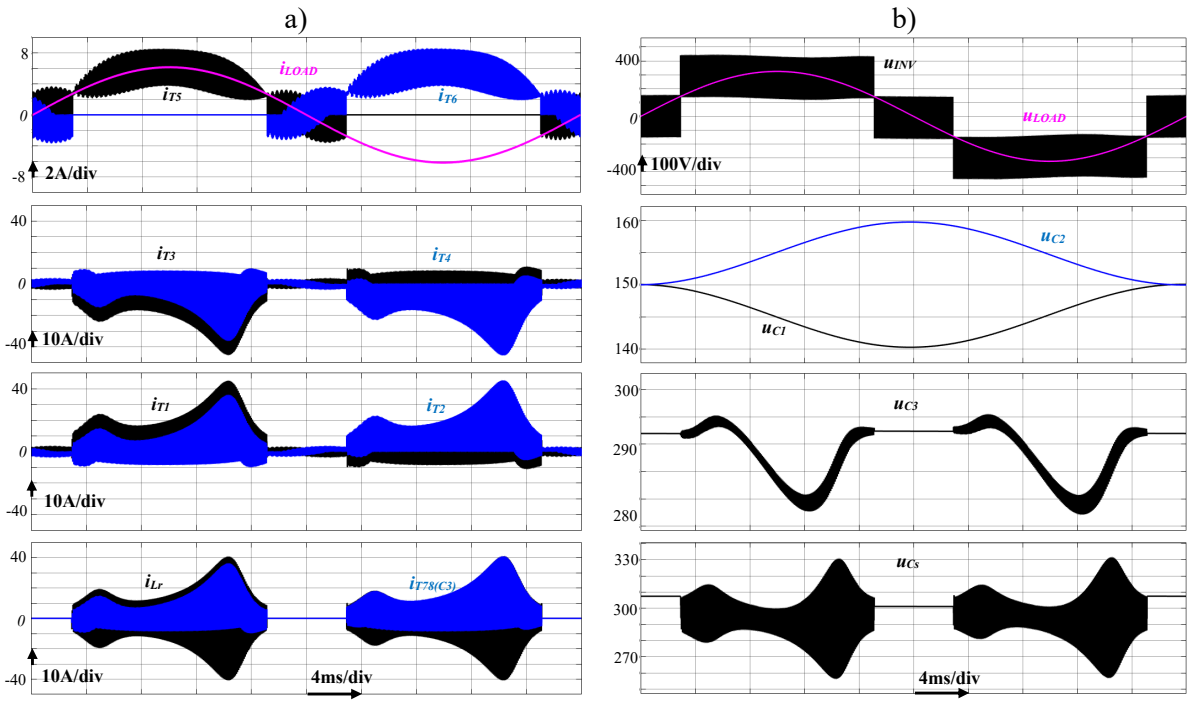


Fig. 8: Current (a) and voltage (b) waveforms of the inverter components

From the simulation results presented in Figs. 7 and 8 it is seen that the four-level modulation is used, the voltage ripple of C_3 is low, the DC-link voltages are self-balanced, and the balancing circuit does not operate in the whole switching period.
The inverter can produce the maximum positive voltage $U_{INVmax} = 450$ V and the minimum voltage $U_{INVmin} = -450$ V from the output to the neutral point of the DC-link divider. The equivalent DC voltage $U_{eq2\text{-}L}$ of the two-level inverter in this output voltage range is:

$$U_{eq2\text{-}L} = U_{INVmax} + U_{INVmin} = 3U_{in} = 900 \text{ V} \quad (6)$$

In Table I, the estimated voltage and current stresses of the components are listed. The voltage stress across the transistors in the proposed inverter is 3 times lower than that in the equivalent two-level inverter.

Table I. Current and voltage stresses of components at P_{load} = 1 kW (i_{OUT_rms} = 4.34 A)

Component	I_{rms} [A]	I_{rms} /I_{OUT_rms}	U_{max} /U_{in}	U_{max} /U_{eq2L}
S_1 (S_2)	7.84	1.8	1	1/3
S_3 (S_4)	7.84	1.8	1	1/3
S_5 (S_6)	3.18	0.7	1	1/3
S_7 (S_8)	10.13	2.3	1	1/3
D_1	0.48	0.1	2	2/3
D_2	0.48	0.1	2	2/3
L_r	10.15	2.3	1	1/3
C_S	10.13	2.3	1	1/3

Experimental results

Figure 9 presents a photograph of the experimental setup and its parameters are assembled in Table II.

Fig. 9: The experimental inverter

Table II. Parameters of the experimental setup

Parameter	Value
Input DC voltage	100 V
Output voltage frequency	50 Hz
Switching frequency	50 kHz
Modulation index	0.75
Capacitors C_1, C_2	150 µF + 4.7 µF
Capacitor C_3	150 µF + 4.7 µF
Capacitor C_S	4.7 µF
Inductor L_r	2 µH

Figure 10a) presents oscillograms of waveforms obtained in the experimental inverter, showing the output voltage u_{INV} of the inverter, its output current i_{LOAD}, the voltage u_{C3} across the capacitor C_3 and the current i_{Lr} of the resonant inductor L_r. Furthermore, Figs. 10b)–10d) show waveforms in zoomed time intervals, presenting the modulation method used according to the switching pattern for a single-phase inverter presented in Fig. 4. They concern the time intervals marked in Fig. 10a).
All of the presented waveforms are in good correlation with those obtained by simulations depicted in Fig. 7 (u_{INV}, i_{LOAD}) and Fig. 8 (i_{Lr}).

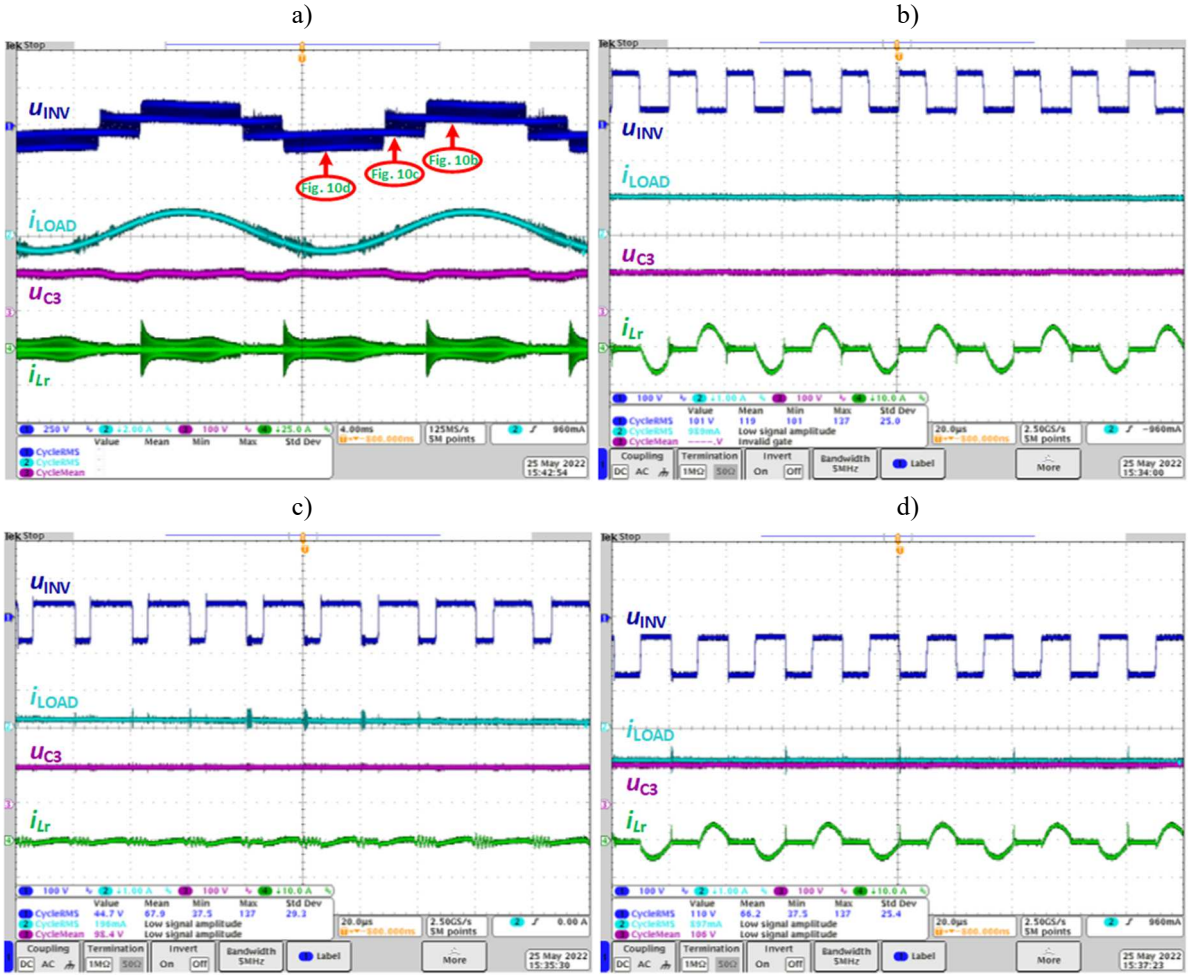


Fig. 10: Waveforms obtained in the experimental inverter setup: output voltage u_{INV}, output current i_{LOAD}, voltage u_{C3} of capacitor C_3, and current i_{Lr} of resonant inductor

Conclusion

In this paper, a novel concept of an inverter topology has been presented. The inverter allows to operate with a voltage gain higher than 1. DC-AC systems with low DC input voltage can operate without a DC-DC boost converter. The proposed inverter utilizes a switched-capacitor branch with a resonant inductor of very low volume. The proposed inverter has positive characteristics compared to the counterpart classic solution with a front-end DC-DC boost converter. The voltage stress of the transistors in the proposed inverter is 3 times lower than that in an equivalent two-level inverter. The entire DC-AC boost/inverter can be designed for MOSFET transistor use. In the boost converter, a larger volume of the inductor is required, and higher voltage stresses of the semiconductor devices occur when operating with the voltage gain $G = 3$. The inverter presented contains a relatively large number of devices, and its efficiency may be deteriorated by losses associated with the operation of the balancing circuit. However, in a classic DC-AC system, the input DC-DC converter operates with high voltage stress of switches and converts 100% of energy. In the proposed solution, the voltage

stress of the switches is lower than the DC-link voltage of an equivalent classic converter. Furthermore, the balancing circuit converts only part of the total energy of the inverter. The presented topology can be extended to a three-phase converter supplied from a single DC source.

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