Efficiently Paralleling GaN-Transistors for High Current and High Frequency Applications Using a Butterfly Layout

Martin Wattenberg, Oscar Lorenz, Juan Sanchez
Infineon Technologies AG
Siemensstraße 2
Villach, Austria
E-Mail: martin.wattenberg@infineon.com
URL: http://www.infineon.com

Keywords

«Gallium Nitride (GaN)», «Device application», «Discrete power device», «High frequency power converter», «High power density systems»

Abstract

This paper presents a scalable design for up to 8 GaN transistors per switch in a three-phase motor drive. To minimize the layout related issues, a fully symmetrical "butterfly" layout was considered. An experimental three-phase prototype with a total of 8 chips per switch was built to verify the concept. Due to the highly symmetrical nature, this work focuses on four half-bridges in parallel, i.e. 4 chips per switch. For evaluation, the design is operated as a 100 kHz buck converter with 50% duty cycle. At 24 and 48 V output currents up to 100 and 60 A respectively are achieved reliably. Measured voltage transition times of 6 ns for all devices and minimal variations between device's temperature (ΔT_j) of 12 and 5 K for 24 V/100 A and 48 V/ 60 A respectively confirm a correct operation.

Introduction

In order to achieve high-current converters the use of power switches in parallel configurations is the most common approach both for Si as well as Gallium Nitride High Electron Mobility Transistors (GaN HEMTs). Due to the typically high-frequency operation in GaN-based applications, getting optimal designs with devices in parallel is a challenging task. Many GaN HEMT-based studies have evaluated the circuit parasitic influence on the switching behavior of GaN transistors in parallel. Others investigated the effects of non-identical electrical properties of those devices [1,2]. The study in [3] showed that board level parasitics had a stronger impact on power loss than device's parameter variation, which was within 10% for V_{th} and 25% for $R_{\mathrm{DS(on)}}$ for investigated commercial devices.

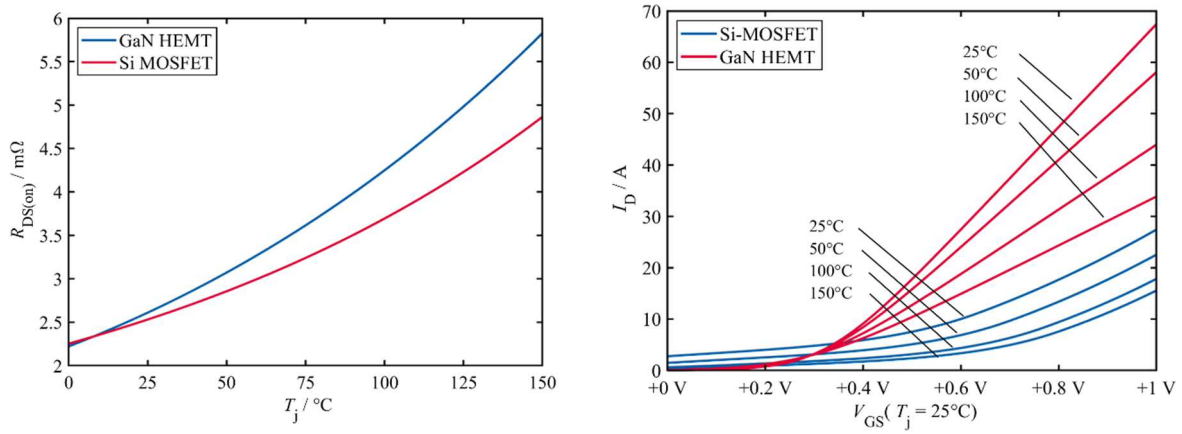
GaN HEMTs are majority carrier devices like silicon power MOSFETs (Si MOSFETs), thus similar design considerations for paralleling apply. A comprehensive overview of the fundamental considerations for parallel operation of Si MOSFETs is given in [4]. Some causes for current unbalance like gate driver and layout mismatch can be avoided or minimized by using a single gate driver and a symmetrical layout respectively. Other effects like threshold voltage variation need to be accounted for. However, it should be noted that some imbalance may in fact be acceptable, depending on the relationship between switching loss P_{sw} and the conduction loss P_{c} as well as the devices safe operating area. Passive balancing method based on cross-coupled transformer feedback presented either in [5] for the phase current or in [6] in the gate path are an interesting solution if the application profile exhibits a high relationship of P_{sw}/ P_{c}. For motor drive applications this is often not the case.

The work presented in [7] uses four 7 mΩ GaN HEMTs in parallel to achieve 35 A output current. A similar layout concept is used in [8] and the output current capability is increased to 70 A_{RMS}. However, the implementation is more complex and requires a larger footprint on the PCB. A separate isolated supply provides bipolar gate voltage to suppress parasitic Miller turn-on caused by the limited hold-down capability of the gate driver used. For the same reason, the turn-on speed needed to be reduced by an additional 6 Ω resistor in the turn-on gate path.

The presented "butterfly" layout concept extends paralleling to 8 devices. Current loops are separated by design. The layout benefits for a more suitable compact gate driver with 4 A peak current capability and integrated charge pump for generation of negative rails. The concept is discussed in detail and experimentally verified.

Impact of Parameter Variation for Paralleled Power Devices

Similar to Si MOSFETs, GaN HEMTs exhibit a positive temperature coefficient for $R_{\mathrm{DS(on)}}$ as shown in Fig. 1 (a). The $R_{\mathrm{DS(on)}}$ is shown versus junction temperature T_j for a gate source voltage V_{GS} of 5 and 10 V for the HEMT and MOSFET respectively. Comparing the $R_{\mathrm{DS(on)}}$ at 25 and 150°C, an increase of 120 versus 91% are observed for the HEMT over the MOSFET. For paralleling, the increased resistance is beneficial as it provides a negative feedback mechanism where hotter devices will conduct less current due to higher resistance compared to cold devices. Similarly, the transfer characteristic of HEMTs is also more strongly influenced by increased temperature than of a MOSFET as can been seen in Fig. 1 (b). Compared to Si MOSFETs, transconductance ($\Delta I_{\mathrm{D}}/\Delta V_{\mathrm{GS}}$) for GaN HEMT falls more strongly when the device heats up. This is especially beneficial during switching transients where hotter devices will conduct less current than cold devices for the same V_{GS}. Based on this data GaN HEMTs already show similar negative feedback mechanisms for paralleling but with strong temperature dependency.



(a) $R_{\mathrm{DS(on)}}$ vs. T_j (b) Transfer characteristic vs. T_j

Fig. 1: Comparison of $R_{\mathrm{DS(on)}}$ in (a) and transfer characteristic in (b). For comparison axis of (b) has been normalized, see Fig. 2

In addition to $R_{\mathrm{DS(on)}}$ and the transfer characteristic another important aspect is temperature dependency of V_{th}. For Si MOSFETs this strong temperature dependency can often be a reason for thermal runaway where a hotter device will have a lower V_{th}, conduct more current, have higher losses and heat up further. Even though a similar temperature dependency exists for GaN, the impact is much less pronounced as Fig. 2 shows. For the GaN HEMT V_{th} only drops by about 1 mV/K whereas for the considered MOSFET close to 4 mV/K.

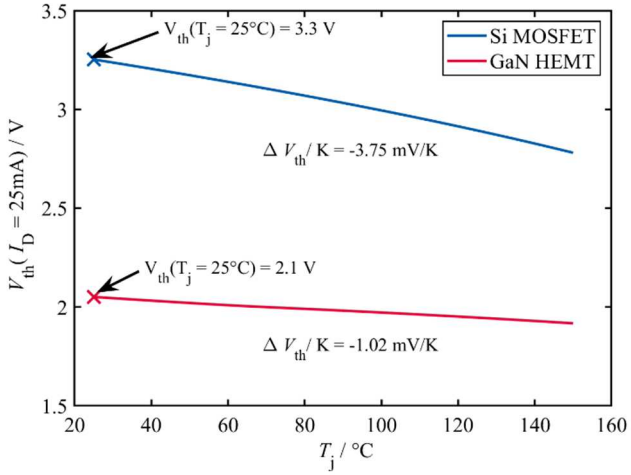


Fig. 2: Threshold voltage V_{th} versus junction temperature for a 100 V 3.1 mΩ GaN HEMT and 100 V 3 mΩ state-of-the-art Si MOSFET.

Design Consideration for a GaN-based Motor Drive

DC-link Capacitance

The DC-link plays a major part in the size of the final inverter. Following the considerations of [9] the current ripple depends on the modulation index M as well as on the $\cos\phi$ of the motor. It is independent of the switching frequency f_{sw}. For a target design with phase current I_0 of 100 A_{rms} the RMS DC-link current I_{DC} can be approximated as follows:

$$I_{\mathrm{DC}} = 0.65 \cdot I_0. \tag{1}$$

This leads to a worst-case RMS current of 65A which can be easily met with multi-layer ceramics capacitors (MLCCs). Providing a similar amount of bulk capacitance compared to electrolytic capacitors can be challenging. However, the voltage ripple $\Delta v_{\mathrm{pp,max}}$ of the DC-link is inversely proportional to f_{sw}. Due to the lower switching losses of GaN HEMTs it is possible to meet the requirements of $\Delta v_{\mathrm{pp,max}}$ at higher f_{sw} and lower bulk capacitance without sacrificing efficiency. In this case $\Delta v_{\mathrm{pp,max}} = 1.5$ V the input capacitance C_{DC} is calculated as described in [10] as

$$\mathrm{C_{DC}} \geq \frac{I_{0,pk}}{4 f_{\mathrm{sw}} \Delta v_{\mathrm{pp,max}}}. \tag{2}$$

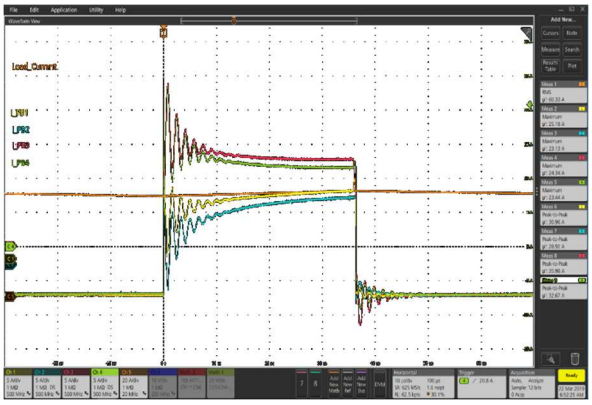
For a switching frequency of 100 kHz this results in 233 µF of capacitance that needs to be distributed across the board. Care must be taken to consider the de-rating when DC-bias is applied. Therefore, some over-provisioning is recommended. Additionally, distributed capacitance produces a lower inductance connection to the DC-link thanks to using many capacitors in parallel.

Low impedance connection to the DC-link

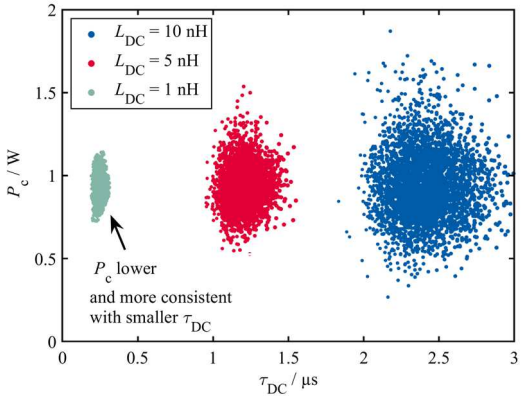
Even though GaN HEMTs exhibit a positive temperature coefficient for $R_{\mathrm{DS(on)}}$ and are self-balancing in steady state, this condition is not immediately reached after the transition occurs. Instead, depending on how uneven the current distribution between devices during the switching transition was, the current will follow an exponential approximation towards steady state with a time constant τ_{DC} defined as

$$\tau_{\mathrm{DC}} = \frac{L_{\mathrm{DC}}}{R_{\mathrm{DS(on)}} + R_{\mathrm{DC}} + R_{\mathrm{CU}}}. \tag{3}$$

As (3) shows, τ_{DC} is proportional to the parasitic inductance of L_{DC} and reciprocal to the effective $R_{\mathrm{DS(on)}}$, ESR of the DC-link capacitor R_{DC} and parasitic resistance of the copper traces R_{CU}. This additional time constant further exacerbates the imbalance in device loss that can occur during the switching transition. Increasing the R_{DC} or R_{CU} in favor of a smaller settling time constant is not practical. Instead, the design should minimize L_{DC} as much as possible by alternating layers between V_{in} and GND in the layer stack up.



(a) Experimental results based on earlier design with four Si MOSFETs in parallel.



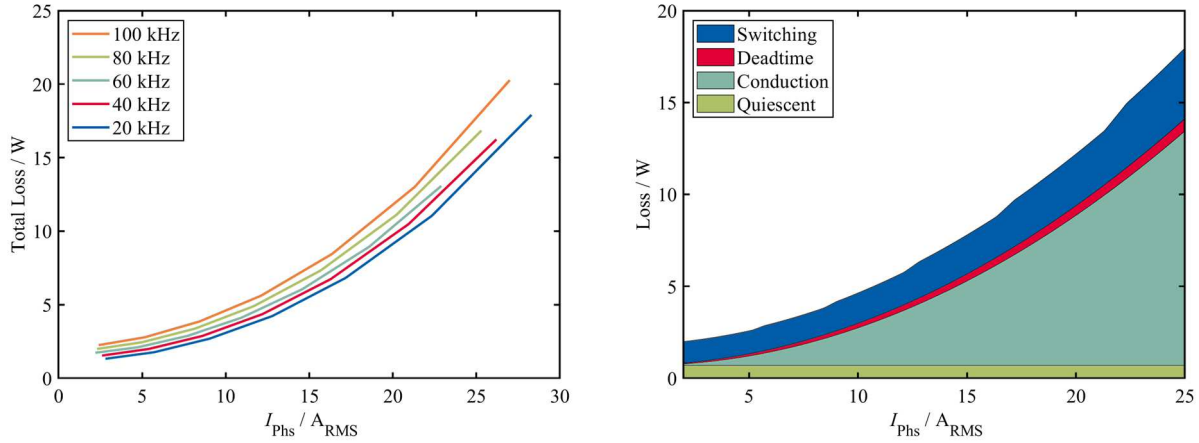
(b) Conduction energy distribution for a typical set of 4 paralleled devices.

Fig. 3: Settling of current waveform in (a) and difference in conduction loss P_{c} caused by settling time constant τ_{DC} in (b).

Fig.3 (a) shows captured waveforms from previous work done on a non-optimized design using Si MOSFETs. The relatively large value for τ_{DC} limits the maximal attainable switching frequency because the impact of asymmetry will grow with shorter periods. For comparison Fig.3 (b) shows a simulated distribution of P_c for four paralleled devices similar to Fig.3 (a). For the $R_{DS(on)}$ and initial current after switching a normal distribution has been assumed and the system has been simulated several times for different values of L_{DC}. A smaller τ_{DC} due to lower L_{DC} ensures lower and more homogenous distribution of P_c. A multi-layered PCB design with interleaved V_{in} and GND planes combined with distributed capacitance is therefore preferred.

Switching Loss Considerations

As stated in the introduction for a motor drive the conduction loss P_C typically dominates. Based on previous work shown in [11] a loss breakdown has been derived by running a non-paralleled motor drive under the same conditions but at different switching frequencies using an inductive-resistive load. Fig.4 (a) shows the measured losses of the inverter at frequencies ranging from 20 to 100 kHz in 20 kHz increments. Thanks to large inductances, current ripple was negligible in all cases. Based on this data a loss model has been derived to distinguish individual loss components. The quiescent power describes the power draw of all auxiliary components as well as gate driver losses when switching at 100 kHz with no V_{DS} applied. Conduction and deadtime loss were derived from measured device parameters. The remaining difference in loss was attributed to switching loss.



(a) Measured inverter losses from 20 to 100 kHz. (b) Approximated loss breakdown at 100 kHz.

Fig. 4: Sweep of inverter loss and approximated breakdown of inverter losses at 100 kHz.

Fig. 4 shows that even for a highly optimized GaN inverter switching loss is not negligible. However, at full-load the dominant loss mechanism is conduction loss with a contribution close to 75% of the total losses. Thus, some imbalance during switching can still be accepted as long as the device safe operating area is not violated.

Overview of the Proposed Layout with Symmetrical PCB Parasitics

It is of critical importance to minimize PCB parasitics to realize the full potential of fast switching GaN HEMTs. Designing the high-frequency (HF) power loop so that the current can flow vertically to under the devices can significantly reduce the loop inductance over a more traditional horizontal power loop design ([12]). However, layer stack-up and prepreg thickness becomes critical. Fig. 5 shows the cross section of the proposed stack-up for one half-bridge. Using the first inner layer as a ground return creates a tight coupling in the HF power loop. A total loop inductance estimate of about 400 pH is obtained applying the approximated expressions given in [12] for a conductor width of 5, a length of 12 and a height of 0.1 mm. This very low inductance results in a minimal amount of overshoot and satisfies the requirements for τ_{DC}.

Equally important is the tight differential coupling of the high-side (HS) and low-side (LS) gate loop. In particular for the low-side the layout needs to be done carefully as it is referenced to the same ground potential as the power loop. When both loops intersect and share common traces the resulting common

source inductance can introduce problematic voltage spikes leading to increased switching loss or even device failure. The high-side devices can exhibit similar issues with respect to the switch node. Thus, a tight coupling of the gate loops with low impedance connection between devices and separated HF power loops are critical aspects of the design.

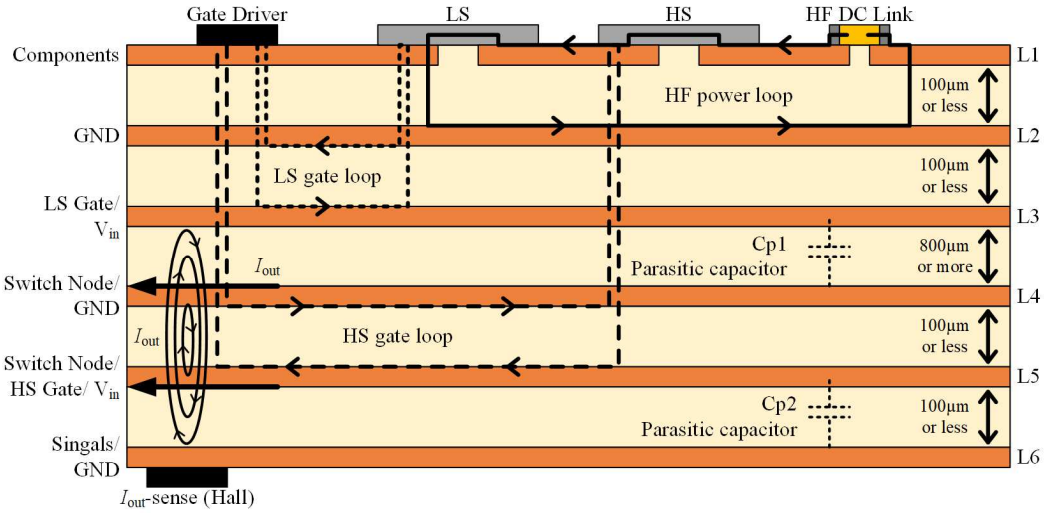
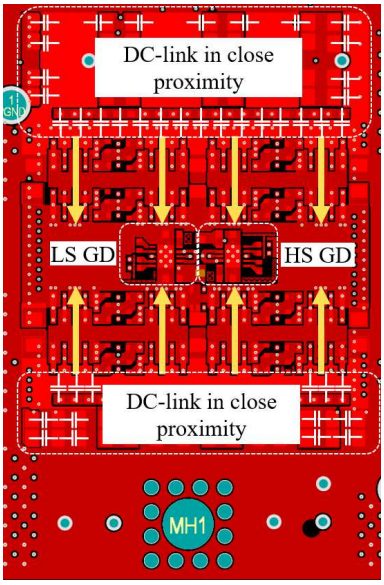


Fig. 5: Layer stack-up for the proposed layout.

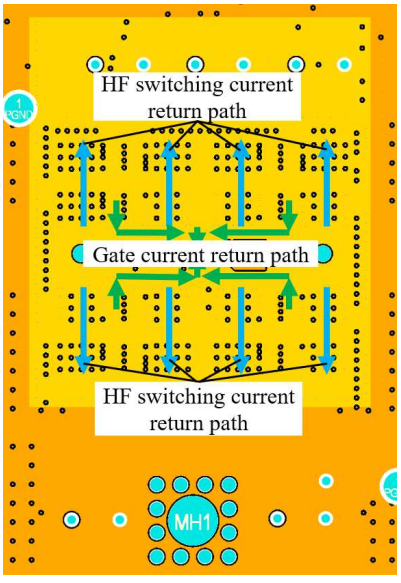
Using an identical layout for the switch node on layers 4 and 5 avoids any capacitive coupling between the two layers. However, some parasitic capacitance exists to toward layer 3 and 6. The capacitance can be approximated as a plate capacitor and calculated with

$$C = \varepsilon_0 \varepsilon_r \frac{A}{d}. \tag{4}$$

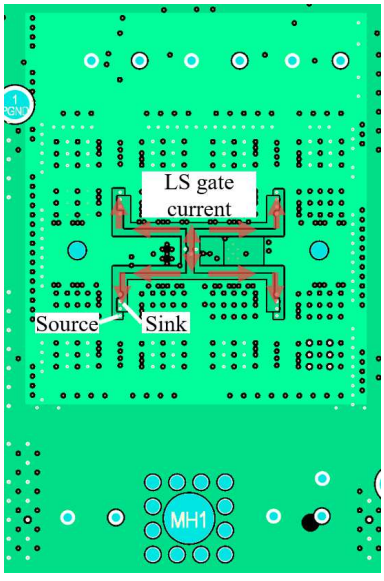
For a total area of (30mm) ² the total capacitance is equivalent to C_{p1}= 40 pF and C_{p2} = 320 pF. The total effective output capacitance at the switch node is close to 10 nF, thus the additional capacitance introduced by the layout is less than 4% and acceptable for the design.
Instead of one large half-bridge with a single power loop the proposed layout mitigates the challenges of asymmetrical inductances by paralleling half-bridges with separate HF loops and one common gate driver in the center. Fig. 6 shows a simplified overview of the proposed layout. The power and gate loops are indicated.



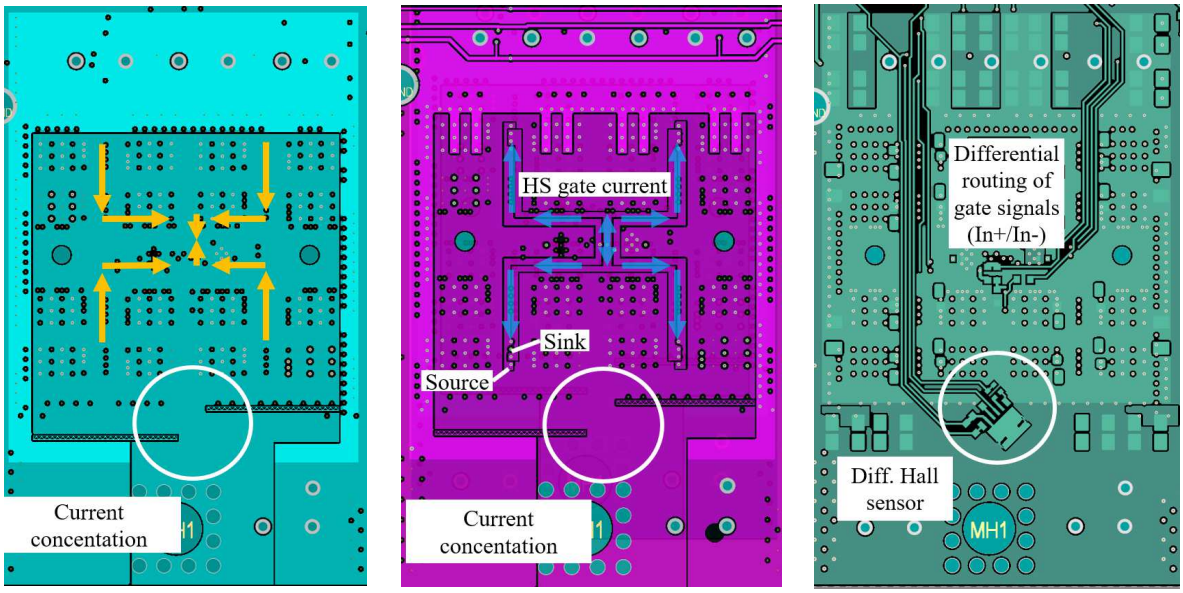
Layer 1: Components and V_{in}.



Layer 2: Ground plane for power loop and gate return.



Layer 3: V_{in} and gate signals.



Layer 4: Switch node, HS gate return and V_{in}.

Layer 5: Switch node, HS gate and ground.

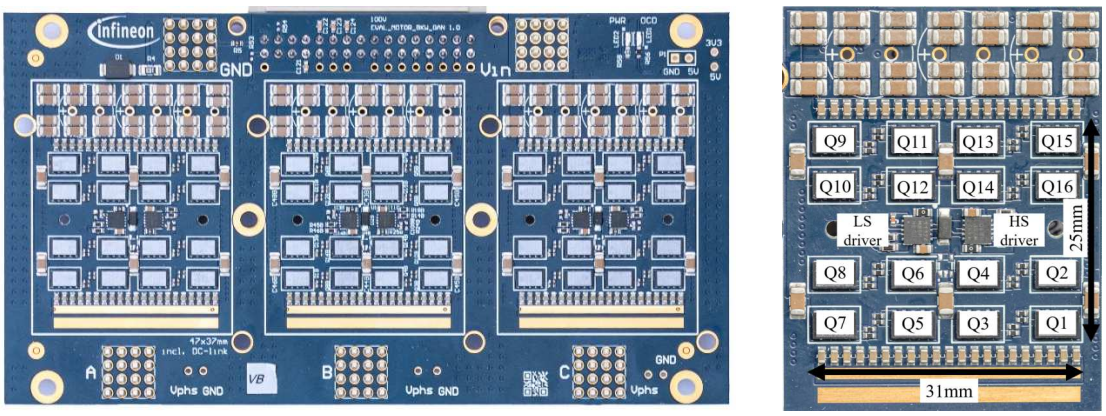
Layer 6: Signals, aux. components and ground.

Fig. 6: Overview of each layer for one phase of the motor drive.

A Hall sensor, shown on layer 6 of Fig. 6, measures the phase current for current control in a DC/DC or motor drive application. In order to maximize the magnetic field intensity, the current is locally concentrated as can be seen in layer 4 and 5 of Fig. 6. Overall this can provide lower insertion resistance and better scalability when addressing large currents with additional layers. However, thermal imaging does show a slight impact on device temperature for HEMTs located close to the current concentration point. For practical applications this is irrelevant but when looking at device temperature as an indication of current sharing performance this effect must be considered.
Top-side cooling allows to decouple the thermal from the electrical path. This way additional PCB layers can be stacked alternating between V_{in} and GND and reducing the parasitic inductance to the DC-link. In addition, thermal coupling between devices can be improved not only via the PCB but also via the heatsink.

Implementation on Prototype

Following the approach presented in Fig. 5 and 6, a prototype has been built and is shown in Fig.6. The devices used are 100 V Schottky-gate GaN HEMTs with a $R_{\text{DS(on),max}}$ of 3.1 mΩ in a 3 x 5 mm package. One 1EDN7116G gate driver is used to drive the gates of the high and low-side switches respectively. The driver features an integrated charge pump capable of generating a negative V_{GS} of up to -3 V and is capable of providing up to 4 A source current with a 5 A miler clamp to avoid parasitic turn-on. In addition, its differential input stage combined with a symmetrical layout of the logic signals significantly reduce the risk of unintended switching events that could otherwise be caused by coupled noise. To sense the phase current, the TLE4972 is used. It features a differential Hall sensor element as well as a differential output. Both significantly mitigate the associated issues of sensing sensitive signals and transmitting analog signals over a comparatively large PCB. The design is copied three times on the circuit board to build a three-phase motor drive.
The use of MLCCs significantly reduces the inverter volume and results in a very low-profile design compared to a more conventional approach with fewer, large electrolytic capacitors. MLCCs are especially attractive for lower voltages where a large capacitance values are available. Optionally, for higher voltages where MLCC often compare unfavorably in energy density the design includes the possibility to use leaded electrolytic capacitors.



(a) Overview of the three-phase design. (b) Close-up of single phase.

Fig. 7: Image of the implemented prototype using the proposed layout structure for 8 chips in parallel.

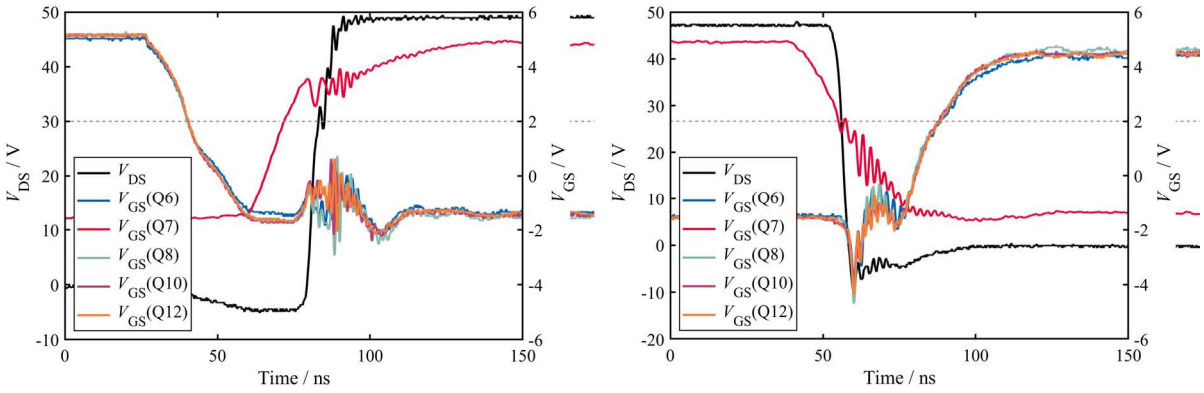
The design in Fig. 7 uses large, low-impedance planes to connect all devices to a common reference (ground or switch node), thus reducing voltage differences as much as possible. However, this approach makes quantifying the symmetry of current sharing impractical. For this reason, a second prototype (not shown) that allows current measurement on each of the eight half-bridges was built. That approach presents its own challenges, some of the low-impedance planes have to be split up and is in general not recommended. The experimental verification was carried out on half of the populated devices. Given the symmetry of the design this does not have any impact on the validity of the results.

Experimental Results

The experimental verification of the design focuses on operating a single phase as a buck converter. If not stated otherwise, a 50% duty cycle at 100 kHz is used.

Symmetry in Transient Waveforms

To judge the symmetry in gate-source voltage waveforms the low-side devices Q6, Q8, Q10 and Q12 as well as the switch node voltage V_{sw} have been measured with 1 GHz passive probes each. For further verification one high-side device (Q7) has been captured with an optically isolated probe (Tek IsoVu) and the total phase current I_{out} was measured with a current probe. Fig. 8 (a) and (b) show the captured waveforms for rising and falling switch-node voltage for 48 V and 60 A output current. The switch-node voltage V_{sw} shows a very clean behavior without overshoot. As initially discussed a stronger gate driver can benefit the design by further bringing down switching losses.



(a) Low side V_{GS} during turn-off. (b) Low side V_{GS} during turn-on.

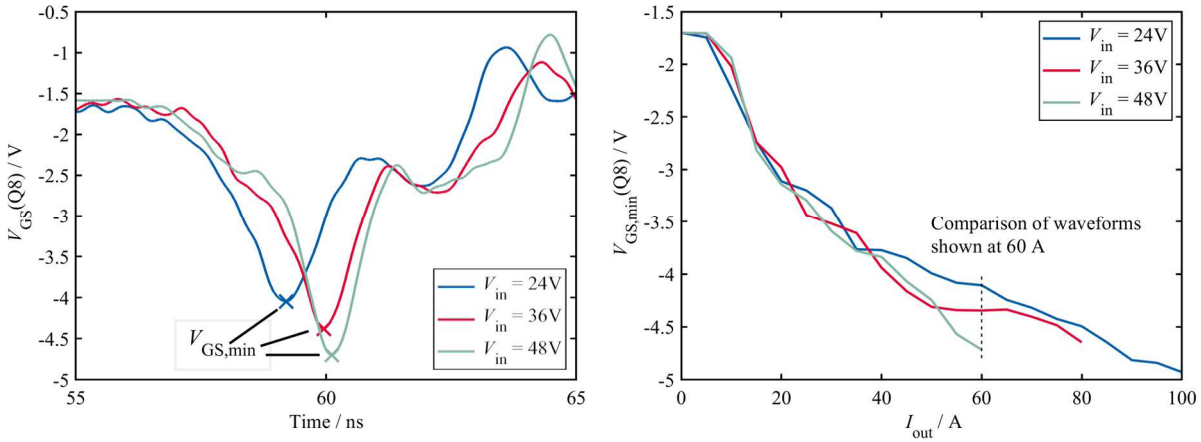
Fig. 8: Comparison of switching waveform for gate-source and drain-source.

Fig 8 (a) gives a closer look at low-side turn-off and high-side turn-on transitions. On close inspection minor differences in V_{GS} can be seen for the low-side devices. The captured V_{GS} for Q7 shows minor

oscillations during the voltage transition. Prior studies indicate that some of these oscillations are artifacts introduced by the twisted pair cables used to connect probe and PCB. This is further supported by Fig. 8 (b) where oscillations are observed at the threshold level but the switch node smoothly commutates to zero (while the low-side devices are OFF).

Peak Low-Side Gate Voltage During Turn-on and Off

If the voltage on the gate is not well-controlled it can lead to false turn-on or even to failure should the device ratings be exceeded. However, at the same time the undershoot during falling V_{DS} must respect device rating. Therefore Fig. 9 evaluates the peak negative voltage during soft transition on the synchronous low-side devices. The peak negative voltage is highlighted in Fig. 9 (a) for 24, 36 and 48 V at 60 A. This spike correlates with the falling voltage of the switching node. The trend of the peak negative voltage is shown in Fig. 9 (b). One clearly sees that it gets larger with both increasing output current and higher voltages.

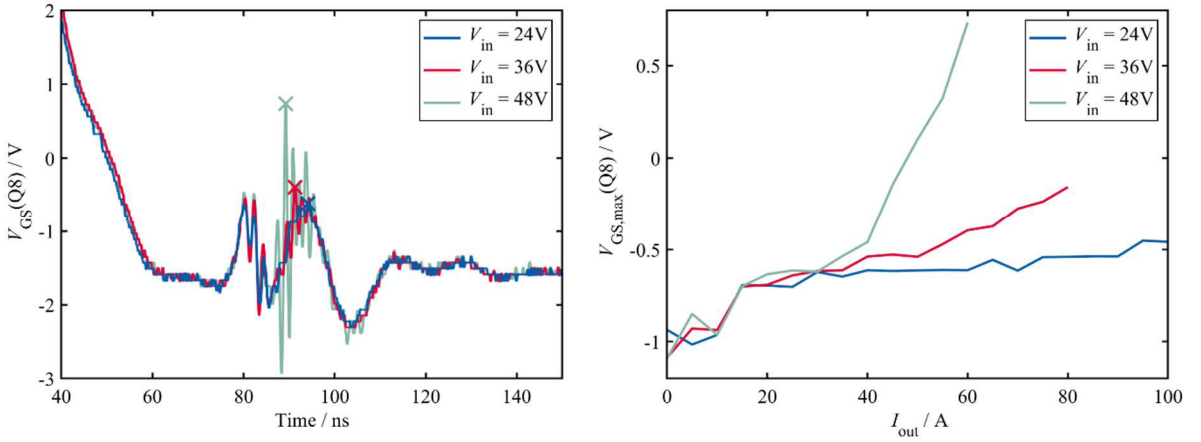


(a) Low-side V_{GS} waveform after turn-off of complementary high-side device.

(b) Peak negative voltage during falling V_{DS} as a function of output current

Fig. 9: Comparison of low-side V_{GS} during soft commutation for 24, 36 and 48 V at 60 A in (a). The trend of peak negative voltage is shown in (b).

Even though a clear trend towards higher negative voltage spike can be observed, it must be noted that the observed levels remain uncritical. The devices rating allows for up to -6.5 V transient gate voltage, thus significant margin still exist in the design.



(a) Low-side V_{GS} waveform during turn-on of complementary high-side device.

(b) Peak positive voltage during turn-on of complementary high-side device.

Fig. 10: Low-side V_{GS} during high-side turn-on / rising V_{DS}.

Similar to the negative voltage spike in Fig. 9 a positive spike on V_{GS} maybe be introduced during turn-on of the complementary switch as shown in Fig. 10.

Symmetry in Current Sharing

To evaluate the symmetry of current sharing individual phase currents are measured on the separate design variant. The average output current of each of the four phases are shown as a function of total output current in Fig 11. The current difference is less than 8% in one of the phases and indistinguishable for the others.

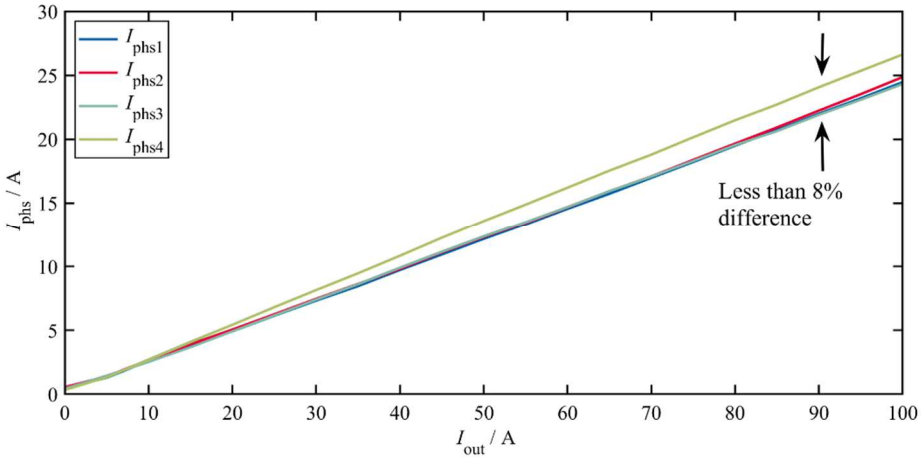
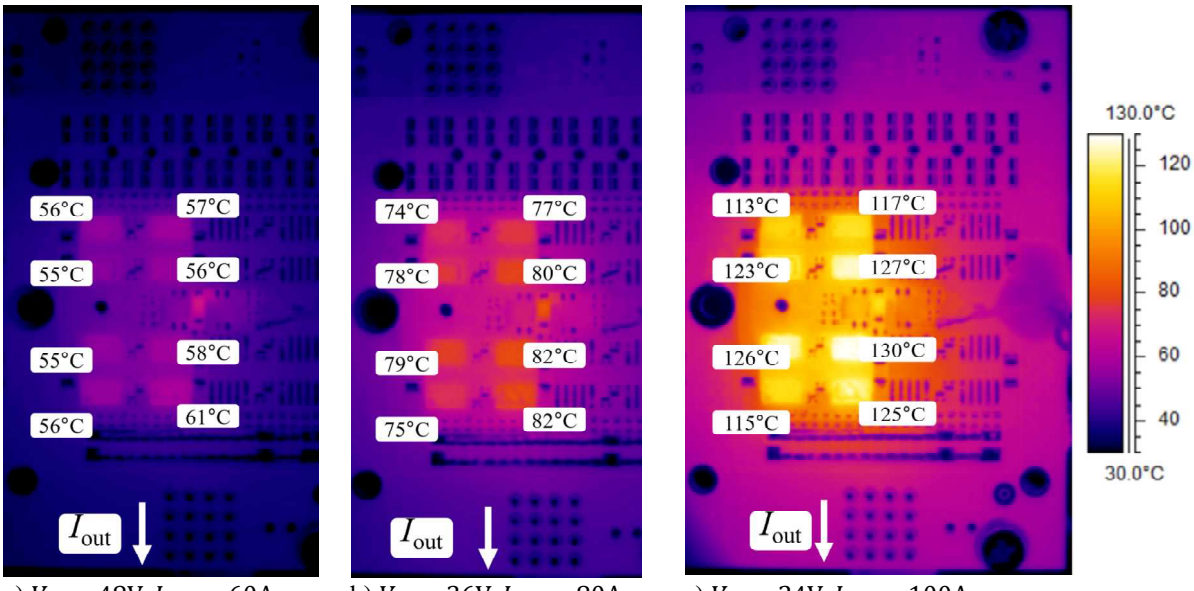


Fig. 11: Current of the four investigated phases.

In addition, the temperature distribution of the devices was captured as a secondary way of evaluating current distribution in paralleled designs. The exposed top-side of the die was covered in black paint and temperatures were observed with a thermal camera. Under normal operation conditions a heatsink can be placed directly on the HEMTs to lower thermal resistance. Fig. 12 (a), (b) and (c) show the temperature for all considered devices for 48, 36 and 24 V respectively. When operating at V_{in} = 36 or 48 V the output power is 1.44 kW. For the operation at 24 V the output power is limited to 1.2 kW due to a thermal limit of 130°C. It should be noted that some thermal difference is created due to the current concentration in the layout nearby the Hall sensor. Slightly elevated temperatures in the vicinity around Q5 are therefore expected.

When operating at 48 V with I_{out}= 60 A the temperature distribution across all the devices is very even. The peak temperature is observed for the high-side at Q5 with 61°C and the lowest for the low-side at Q8 at 55°C. Lowering V_{in} to 36 V and increasing the output current to 80 A produces a very similar temperature distribution. The peak temperature remains at 82°C on Q5.



a) $V_{in} = 48V, I_{out} = 60A$ b) $V_{in} = 36V, I_{out} = 80A$ c) $V_{in} = 24V, I_{out} = 100A$

Fig. 12: Temperature distribution for different input voltage levels at maximum investigated current.

Conclusion

A scalable layout for paralleling a large number of power transistors with a focus on Gallium-Nitride (GaN) transistors is proposed. Compared to Si, GaN devices exhibit a stronger dependency of both $R_{\mathrm{DS(on)}}$ and transconductance with temperature. This stronger dependency leads to an enhanced self-balancing effect. Although the threshold voltage V_{th} of GaN is significantly lower than that of silicon devices it has a weaker temperature dependency (1.02 mV/K vs. 3.75 mV/K), therefore experiencing a reduced positive feedback effect for current unbalance.

Although not negligible, even at increased carrier frequencies of 100 kHz the switching losses in motor drives applications are shown to play a secondary role with a contribution close to 25% to the total power semiconductor losses. Therefore, some imbalance during the switching transition can be acceptable and the above stated technology parameters considerations hold to be the most relevant.

Still, the fast switching speed of GaN mandates a symmetrical layout with low parasitics in order to ensure a fair spread of current through the PCB board and paralleled devices. In addition, the design benefits from a negative V_{GS} generated directly by the gate driver used. The proposed layout effectively establishes high frequency switching loops of high-side and low-side pairs rather than a single common shared loop for all the paralleled devices. This approach is demonstrated to result in a very even current sharing with less than 8% difference between phases. It achieves as well a uniform temperature distribution with measurements showing less than 5 K of difference between the hottest and the coldest devices at a nominal 48 V input voltage.

References

[1] Wickramasinghe T.: An investigation of current distribution over four GaN HEMTs in parallel configurations, WiPDA, Oct. 2019

[2] Wu Y.-F.: Paralleling High-speed GaN Power HEMTs for Quadrupled Power Output, APEC, Mar. 2013

[3] Wickramasinghe T.: Electrical property variability of GaN transistors in parallel and their impact on fast switching operations, EPE'20 ECCE Europe, Sept. 2020

[4] Forsythe J.: Paralleling of Power MOSFETs For Higher Power Output, International Rectifier, 1996

[5] Lu S.: A Passive Transient Current Balancing Method for Multiple Paralleled SiC-MOSFET Half-Bridge Modules, APEC, Mar. 2019

[6] Hackel J.: A Novel Gate Driving Approach to Balance the Transient Current of Parallel-Connected GaN-HEMTs, CIPS Mar. 2018

[7] Reusch D.: Effectively Paralleling Gallium Nitride Transistors for High Current and High Frequency Applications, APEC, Mar. 2015

[8] Burkhard J.: Paralleling GaN switches for low voltage high current half-bridges, ECCE, Sept. 2019

[9] Kolar J.W.: Paper on DC link, IEEE Transaction on Industry Applications, Mar. 2021

[10] Vujacic M.: Analysis of dc-Link Voltage Switching Ripple in Three-Phase PWM Inverters, Energies, Nov. 2018

[11] Wattenberg M.: A Low-Profile GaN-Based Integrated Motor Drive for 48V FOC Applications, PCIM, May 2021

[12] Sun B.: Research of Power Loop Layout and Parasitic Inductance in GaN Transistor Implementation, IEEE Transaction on Industry Applications, Mar. 2022