Current Source High Step-Up Push-Pull Resonant Converter for Low Wide-Input Source Based on Front-End Photovoltaic Cells Application

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***Abstract*-- This paper present current source high step-up push-pull resonant converter (CSPPRCs) for low wide input source based on front-end photovoltaic cells application. The power state receives DC voltage of 10.5-12 V_{DC}, which two switches (MOSFETs) would operate under zero current switching (ZCS) conditions with a frequency of 260 kHz. The both switches would operate alternately half-period. The output voltage is 330-370 V_{DC}, the approximate around efficiency of the prototype is 92 percentage, the output power is 270 watts at maximum load. Experimental results for prototype was built and operated at fixed switching frequency, 330 V_{DC} output voltage, and 180 W output power at 10.5 V_{DC} input voltage, the efficiency is 90 percentage. From state-of-the-art power state connected to DC voltage is supplied to the both switches. which have a characterization of operated under ZCS conditions. The AC high frequency voltage of power state is provided to the high frequency transformer to matching circuit. To generate a current signal as a sinusoidal signal to be used as an input signal to a bridge full-wave rectifier. Consider, the voltage drops and the current flows through the diode in a bridge full-wave rectifier, While the diode are operated. A voltage drop will occur, it can turn-off under zero current switching. To reduced transition losses of diode. Overall efficiency in both input voltage of the prototype more than are 90 percentage during in full load range.**

***Index Terms*-- current source, high step-up, push-pull, converter, photovoltaic cells**

I. INTRODUCTION

Oil and power prices have increased as the world's energy supply has become more inadequate. On a worldwide basis, energy resource constraint is becoming inescapable. Therefore, saving energy and limiting carbon emissions are essential tasks for modern society. The objective of earlier technological advances has been to eliminate inconveniences while enhancing human life. Currently, energy derived from natural resources is generated with an emphasis on user convenience and environmental protection. In addition to emphasizing the significance of reducing environmental harm and pollution, these technologies highlight the production of inexpensive and efficient energy sources. Solar energy is one of the most extensively used forms of efficient natural energy. Increasing numbers of governments and research institutions are spending extensively in solar energy-based efforts, both monetarily and laboriously. Some renewable energy sources, such as fuel cells and PV panels, have stringent criteria for current ripple and are characterized by low-voltage, high-current output. This requires a dc-dc converter with a large step-up capacity, galvanic isolation, low input current ripple, and stable performance. Due to its inherent characteristics of high boost capacity and minimal input current ripple, current-fed converters are gaining popularity in these applications. As a consequence, the turns ratio of the transformer may be lowered relative to conventional voltage-fed converters (VFCs), and the bulk input filters can be scaled down. In principle, isolated voltage-fed step-up converters have several issues, such as high ripple current input, high turn ratio (transformer), and voltage spikes across the power switch. For applications requiring a low-voltage, high-current input, current-fed step-up converters (CFCs) may be preferred than VFCs [1-3].

Itself with inherent high boost capacity and low input current ripple, CFCs are garnering a significant amount of attention for such applications. In spite of this, CFCs pulse width modulated (PWM) continue to struggle with issues such as high voltage and current spikes brought on by the leakage inductance and winding capacitance of the transformer, as well as high voltage stress on the rectifying diodes as a result of the diodes inability to recover from their reversed state. As a result, their working frequency need to be low, and the efficiency of their power conversion should also be restricted. It causes a high-voltage spike at the power switch when it operates at a high frequency, and when there is a lot of electromagnetic interference, the switching loss and the loss caused by passive devices are both increased. A number of active clamping approaches have been offered as a means to both recycle the energy that is stored in the leakage inductance and reduce the surge voltage that is experienced on the switches. Nevertheless, the extra clamping circuits make the application more difficult to use, reduce its dependability, raise its cost, and invariably produce triangle switch currents, which raise the current rms values [4-5]. Current fed resonant techniques promise high-efficiency power conversion while employing a high switching frequency. This is made possible by their innate

capability of well utilizing the circuit parasitic and achieving zero-voltage switching (ZVS) or zero-current switching (ZCS) for the active power switches. matching resonant circuits concentrated the majority of their efforts on obtaining ZVS of the main switches, regardless of whether the active switches were managed with dead time or overlapped. Nevertheless, in low-voltage high-current input applications, ZVS is not as critical as ZCS, which is the important to minimizing switching loss. This is despite the fact that the transformer's existing leakage inductance still causes high voltage spikes on the switches [6-8]. In the utilization leakage inductance and parasitic capacitance to achieve ZCS it can be reduced majority power loss for both of the main power state. To achieve full load range ZCS of the primary switches, however, the leakage inductance was manipulated according to the heavy load condition, resulting in a large redundant circulating current flowing through the antiparallel diodes of the MOSFET and as a result, the efficiency at light load was drastically reduced. There is still an issue with the reverse recovery of the rectifying anti-parallel body diodes, which causes high voltage spikes at the main power switches if there are significant quantities of circulating energy present at the input size of the inductors. Because of this, the use of ultrafast recovery diodes that have lower forward voltage drop and lower voltage ratings is restricted [9-10].

The detailed operation principle of the proposed converter is introduced in Section II. Section III modelling analysis and design guideline. Section IV experimental results of the proposed converter on a 270- W prototype. Finally, Section V concludes this paper.

II. Operation Principle Description

Figure.1. depicts configuration element CSPPRCs consist of two power switches MOSFET M_1, M_2 and two power diodes with rapid reverse recovery D_{i1} and D_{i2}. L_{p1} and L_{p2} are primary sides of the inductor. The matching resonant circuit consists of a first resonant inductor L_{ms} and a second resonant inductor L_{lks} that participates in the resonance only during the commutation period of the primary current i_{Lp1}+ i_{Lp2}. The secondary of a transformer performs the magnetizing inductance L_{ms}, which is substantially greater than L_{lks}. This paper includes anti-parallel parasitic capacitance C_{D1}= C_{D2}= C_{D3}= C_{D4} of the Full-Bridge Class-D Rectifier (FB-CDR.), which has a reduced influence on the operating point of resonance condition. Also, the transformer leakage inductance L_{lks} and the series-parallel capacitor resonance C_r, C_p are discussed. The rectifying FB-CDR. has a parasitic capacitance, and that capacitance is absorbed into C_p as well. The output inductor L_o and capacitors C_o are much larger than L_{lks} and C_p can be smooth voltage and current output side.

In order to assumption clarify the analysis of the proposed circuit, begins with these following assumptions. Input capacitors with values of C_B, C_o, and L_o that are sufficiently high ensure that the input/output voltage and

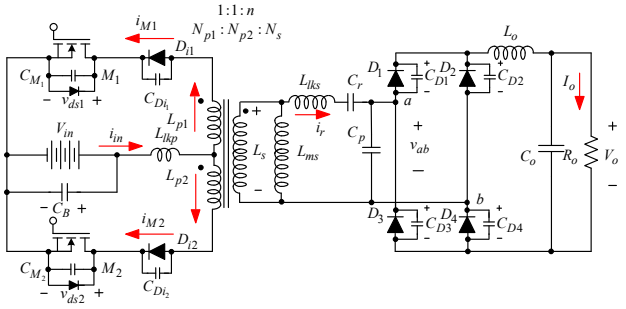

Fig. 1. Schematics of the proposed converter

current remain stable during the switching time. The optimum FB-CDR. configuration includes active switches M_1 and M_2, as well as rapid recovery power diodes D_{i1} and D_{i2}, followed by D_1-D_2-D_3-D_4 in that order. The starting state is set to zero, and the circuit's passive components are all perfect examples of their respective ideal types.

Brief the first four operating modes of the proposed converter are depicted in Figure. 2. (a)–(d) during the first half of the switching cycle. The other two operation modes during the second half of the switching cycle are symmetrical to the first four operating modes. The appropriate theoretical key waveforms are represented in Figure. 3, which may be found here.

The fundamentals of how CSPPRCs maintain their power states are broken down and shown in Figure. 2. (a-d). The ZCS condition is met when the main power switch and the diode rectifier are put into operation. It is reasonable to think of the secondary side of the transformer as a sinusoidal current source i_r, which is also a high-frequency current source for the FB-CDR. This is a beneficial way of thinking about this side of the transformer. Figure. 3. demonstrates that the key waveforms include a gate that is driven by switches v_{gs1} and v_{gs2}; voltage across v_{ds1} and v_{ds2}; current of switch i_{M1} and i_{M2}; voltage across resonant v_{ab}; current across resonant i_r; overall voltage across v_{D1}-v_{D2}-v_{D3}-v_{D4}; and a current of the diode rectifier i_{D1}, i_{D2}, i_{D3}-i_{D4} The suggested circuit has the capability of operating in four different modes, as seen in Figure. 4. The examination of the circuit starts with the assumptions that are listed below.

Mode1: In the initial state, active switch M_1 is active and active switch M_2 is disabled, and current flows from the supply to the input V_{in} and the handling diode D_{i1}. The active switch M_1 interrupts the flow of current; the switch functions as a ZCS. As a result of a conditional energy exchange between the transformer's leaking inductor L_{lk1} and the capacitor C_{M1} of the active switch, the capacitor C_{M1} of the active switch M_1 is simultaneously discharged. Once it equals zero, and taking into account the voltage drops across v_{ds2} of the active switch, the value of M_2 is raised to the value When the power on the main side of the high frequency transformer is transferred to the secondary side, diodes D_1 and D_4 will begin operating at about triple the input power supply V_{in}. The diodes D_2 and D_3 will stop operating at zero current.

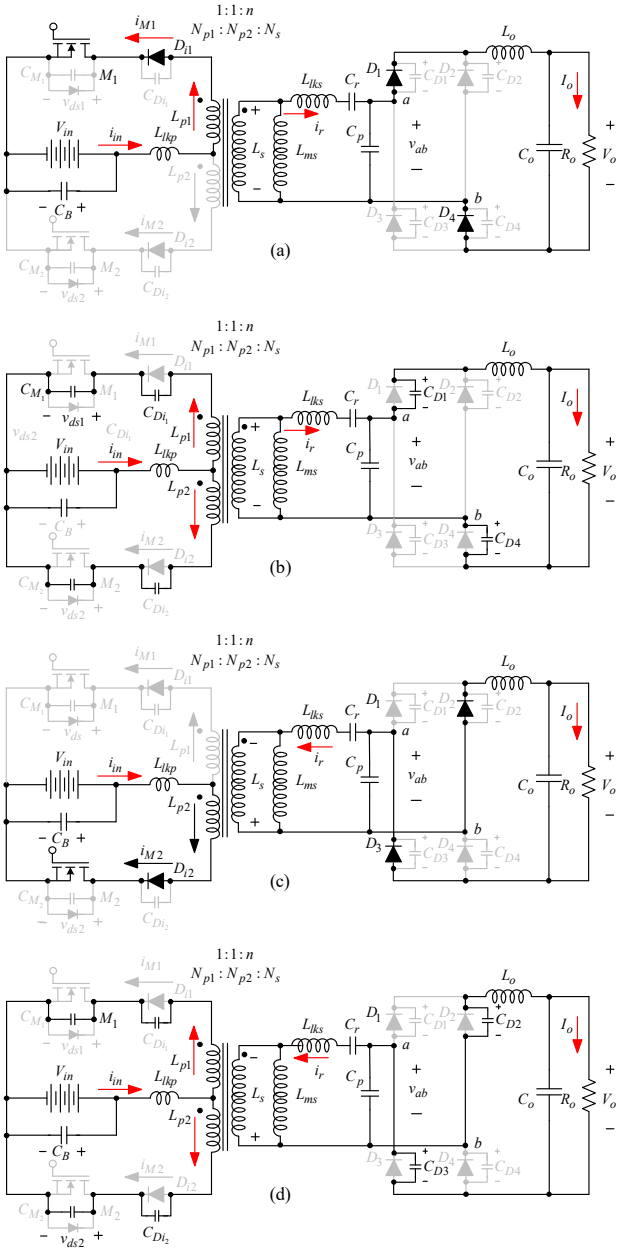

Fig. 2. Operating modes and waveform of the CSPPRCs (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4.

Mode2: It is the operating condition exchange time in the operating mode of active switches M_1 and M_2 that is cancelled when the active switch gate drive signal overlaps the capacitor C_{M1} of the first active switch. The input voltage, v_{ds1}, is charged until it reaches a voltage equal to three times the input supply voltage V_{in}. In the portion of the voltage at the C_{M2} capacitor of the second active switch, v_{ds2} is discharged from the voltage at until it equals zero, while the series-parallel resonant capacitor C_r, C_p also experiences a voltage discharge. As more sine waves are sent to the rectifier. Passive capacitors C_{D1} and C_{D4} of diodes D_1 and D_4 are discharged negatively, while passive capacitors C_{D2} and C_{D3} of diodes D_2 and D_3 are charged to a negative voltage of zero volts.

Mode3: The behavior resembles operation mode 1 when the switch is set to mode 1. Active M_2 is active, while

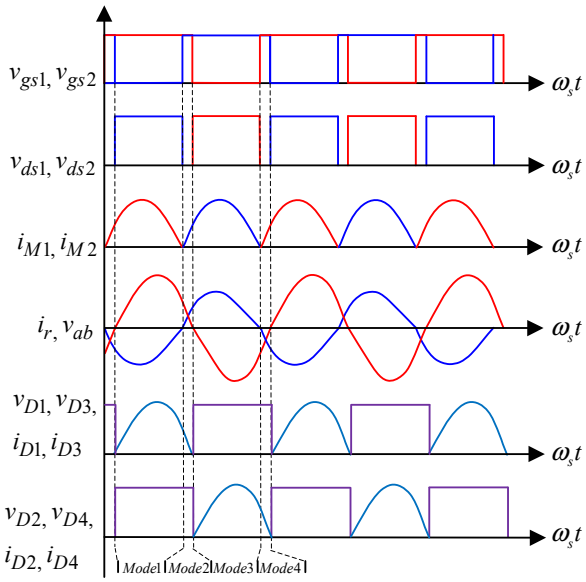

Fig. 3. Key theoretical waveform

active M_1 is disabled. Electricity comes from the supply at the input V_{in}, and the diode D_{i2} produces a discontinuous current via the active switch M_2. Will function as a zero-current switch under the circumstances of an energy exchange between the transformer's leaking inductor L_{lk2} and the active switch's capacitor C_{M1}. Simultaneously, the capacitor C_{M2} of the active switch M_2 is drained to zero, and the voltage drop across v_{ds1} of the active switch M_1 climbs to approximately triple the input power supply V_{in}. When the power from the main side of the high frequency transformer Diodes D_2 and D_3 is transferred to the secondary side, the zero-current stop diodes D_1 and D_4 are activated.

Mode4: It functions similarly to mode 2 of operation, which is the operating condition exchange interval. In this functioning state, the active switches M_2 and M_1 disable the second active switch's capacitor C_{M2}. At the part of the voltage at which the C_{M1} capacitor of the active switch M_1 is discharged from the voltage v_{ds1}, the voltage v_{ds2} is charged until it reaches a value equal to three times that of the input supply voltage V_{in}. Likewise, the voltage drops of the series-parallel resonant capacitor C_r, C_p is more sinusoidal. forwarded to the corrector. The diode capacitors C_{D2} and C_{D3} are discharged with a negative voltage. And the passive capacitors C_{D1} and C_{D4} of diodes D_1 and D_4 are charged to zero with a negative voltage.

III. Modeling Analysis and Design Guideline

This section examines the FB-parasitic CDR's capacitance in a resonant circuit. The model initially combines the FB-CDR. and CSPPRC circuits. When the main switch M_2 operates on the negative half-cycle, main switch M_1 operates on the positive half-cycle. When the main switch M_2 operates on the negative half-cycle, main switch M_1 operates on the positive half-cycle. According to Figure. 4. (a). , two windings on the primary side are used transfer the high-frequency square wave current source is in to the secondary side. The basic component amplitude

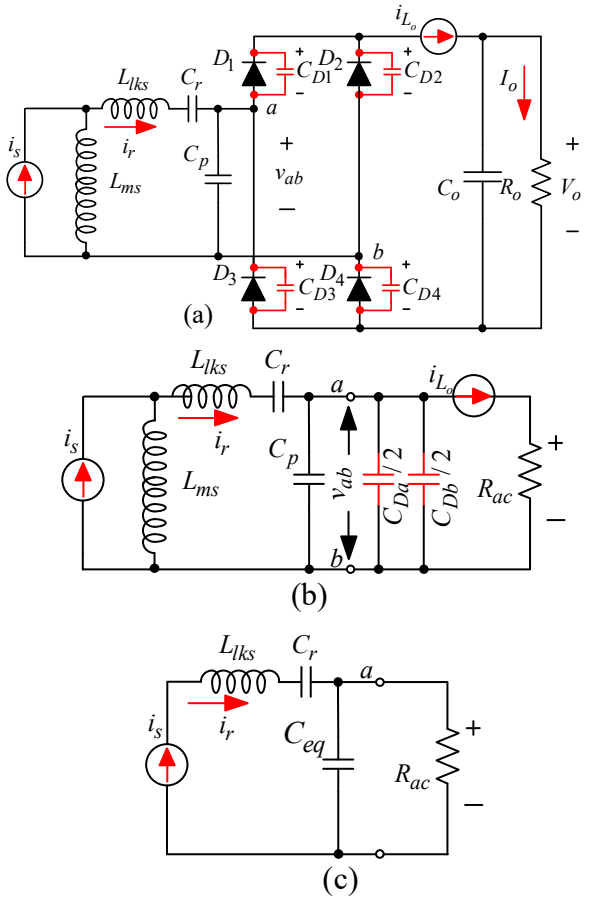

Fig. 4. Equivalent circuit for CSPPRCs and FB-CDR. (a) Semi-equivalent circuit of the FB-CDR. (b) Equivalent circuit including parasitic junction capacitance in FB-CDR. (c) Final equivalent resonant circuit.

of the parasitic junction capacitance in the FB-CDR. for the CSPPRCs, when diodes D_1 and D_4 of the rectifier operate during the positive cycle of a high-frequency sinusoidal-wave current-voltage source, are equal to v_m sin $\omega_s t$ and i_s sin $\omega_s t+\varphi$, which is the main parameter secondary side. Its magnitude is comparable to that of the rectifier's diodes D_2 and D_3, which operate during the negative cycle. The comparable circuit influences the parasitic junction capacitance of the FB-CDR. diode under high switching frequency and high voltage conditions. As indicated in Figure. 4. (b), due to the short circuit of the AC voltage source on the secondary side, the junction capacitor $C_{Da}/2$ is derived from diodes D_1 and D_3, and the junction capacitor $C_{Db}/2$ is formed from diodes D_2 and D_4. C_{Dab} = $C_{Da}/2$ + $C_{Db}/2$, which may be seen as a single capacitor. The C_e parameter is parallel to the AC resistance R_{ac} that has been converted from the DC resistance of the output side.

$$Z_{in}(s) = sL_r + \frac{1}{sC_r} + Z_o \tag{1}$$

$$Z_o(s) = \frac{R_{ac}}{1+sC_{eq}R_{ac}}. \tag{2}$$

Hence, the normalized voltage gains as shown Figure. 4 (c) can be transfer function is described as (4).

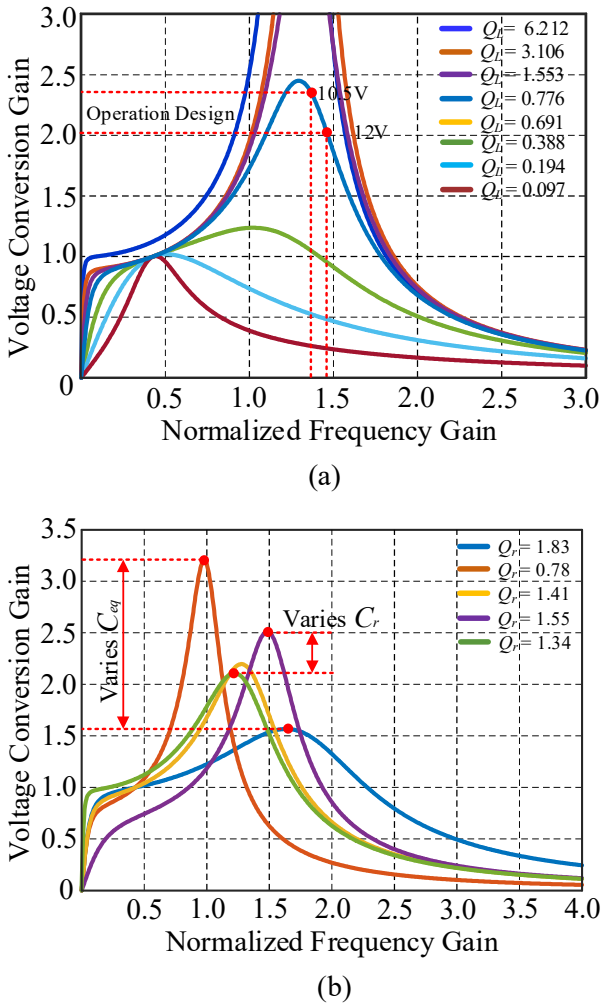

Fig. 5. Relationships of the matching resonant tank of the proposed circuit (a) Normalized voltage gain of resonant parallel circuit versus frequency at varied R_{ac} (b) Normalized voltage gain of resonant circuit versus frequency at varied capacitor resonant.

$$TF(s)=\frac{sC_rR_{ac}}{s^3L_rC_rC_{eq}R_{ac}+s^2L_rC_r+s\left(C_{eq}R_{ac}+C_rR_{ac}\right)+1} \tag{4}$$

Figure. 5. (a) depicts the relationships between the voltage conversion ratio and the normalized frequency gain f_r/f_s for varying values of the AC resistance. The range of the AC resistance varies from R_{ac}. when with us design uses various input voltage, the operating point of the circuit increases from maximum 12 V_{DC} to critical input voltage 10.5 V_{DC}, where varying input results in an increase in the voltage conversion ratio and a decrease in the f_r/f_s ratio. Figure. 5. (b) demonstrates that when the parallel capacitance varies between $2C_{eq}$ and $C_{eq}/2$ of load C_{eq}, the f_r/f_s operating point of the circuit rises from around 1.6 to less than unity. An increase in the parasitic junction capacitance causes changes that range from $4C_r$ to $C_r/4$. These changes are observable in the series-parallel resonant tank, where a change in C_r causes the operating point switching and voltage gain to move from = 2.5 to approximately = 1.6 and f_r/f_s about 0.1. Additionally, the operating point of the resonance shifts from high frequencies to low frequencies.

The suggested power state may be divided into three parts. The major power source is the ZCS push-pull resonant converter, followed by the *LCC* matching network, which contains the parasitic capacitance of the full-wave bridge rectifier, and the ZCS Class-D bridge rectifier, which is designed as follows: 1) Selects the output voltage V_o and output power P_o, and then calculates the AC equivalent resistance R_{ac} before converting from the DC side. 2) Determine the value of the load quality factor Q_L when resonant frequency f_r is nearly equal to switching frequency f_s. 3) Calculate the parasitic capacitance C_e in the FB-CDR using the characteristic diode and the *LCC* series-parallel matching network. The circuit was intended to operate in steady-state mode at a set switching frequency of 260 kHz, an input voltage of 12 V_{DC}, and a maximum power output of 270 W at an output voltage of 380 V_{DC}. Hence, the output resistance at full load is $R_o = V_o^2/P_o = 507.03\,\Omega$, the ac resistance can be calculated from below

$$R_{ac} = \frac{8R_o}{\pi^2} = 410.988\,\Omega \tag{5}$$

To simplify the corresponding circuit in Figure. 4. (c), the parallel resonant capacitor C_p, which is a parallel combination of R_{ac} and C_e, is used. The circuit technique proposes a possible absolute parasitic capacitance of (6), from which the semi-equivalent C_{pe} is obtained

$$C_e = \left(\frac{\pi}{16R_o f_s}\right)\left(\frac{b_1}{a_1^2 + b_1^2}\right) = -268\,\text{pF} \tag{6}$$

$$C_{pe} = C_p + C_e = 1.563\,\text{nF} \tag{7}$$

Assigned to the $a_1 = \sin^2(\omega_s\tau)/16f_sRoC_{Dab}$, $b_1 = \sin(2\omega_s\tau) - 2\omega_s\tau/32f_sR_oC_{Dab}$, when ω_s is angular switching frequency and τ is commutation time of power diode during turn on and turn off period, final equivalent C_{eq} is given as

$$C_{eq} = \frac{C_r \times 2C_{pe}}{C_r + 2C_{pe}} = 2.558\,\text{nF} \tag{8}$$

Subsequently, is obtain resonant frequency $\omega_r = 381$ kHz and the characteristic output impedance $Z_o = 1/\omega_o C = 219.842\ \Omega$, when the equivalent capacitance base on corner frequency $C = C_1(C_p+C_e)/C_1C_pC_e = 1.407$ nF.

$$\psi = \tan^{-1}\left(\frac{1}{R_{ac}/Z_o \times (1+\text{A})}\right) = 21.265 \tag{9}$$

Finally, ψ ship angle of normalized frequency $f_r/f_s = 1.467$ based on this fixed ratio of capacitance $A = C_{pe}/C_r = 0.11$ and load quality factor $Q_r = 0.776$, respectively.

IV. Experimental Results

The operational sector of the proposed converter is shown in Figure. 6., where the range of R_o is between nearly light load to maximum load. The primary benefit of the

TABLE I
CIRCUIT PARAMETER OF THE PROTOTYPE

Parameter	Symbol	Value/Description
Input/Output voltage	V_{in}	10.5-12 V_{DC}
Maximum output power	P_o	270 W
Output capacitance/Inductance	C_o, L_o	0.47 μF, 190 μH
Input inductance	L_i	33 μH
Switching frequency/Mode	f_s	260 kHz
Power MOSFETs	M_1, M_2	IRFP3205s/N-Channel
Schottky diode primary	D_{i1}, D_{i2}	DSS600045B/ Diode
Fast recovery diode secondary	D_1 - D_4	MUR860
Inductance primary	L_{p1}, L_{p2}	9.26 μH, 9.26 μH
Inductance secondary	L_s	3.79 mH
Resonant inductance	L_{lks}	68 μH
Resonant capacitance	C_r, C_p	14.1 μF, 1.566 μF
Parasitic junction capacitor diode	C_{D1}-C_{D4}	75 pF

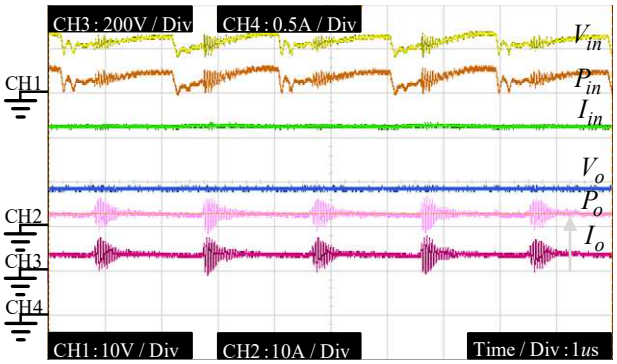

Fig. 6. Experimental result of input/output voltage V_{in}, V_o current I_{in}, I_o and power P_{in}, P_o waveforms at $V_{in} = 12$ V_{DC}

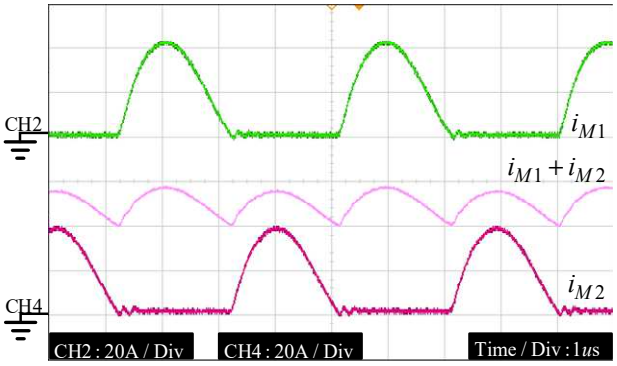

Fig. 7. Experimental result of both current power switch i_{M1}, i_{M2} and summation current power switch primary waveforms at $V_{in} = 12$ V_{DC}

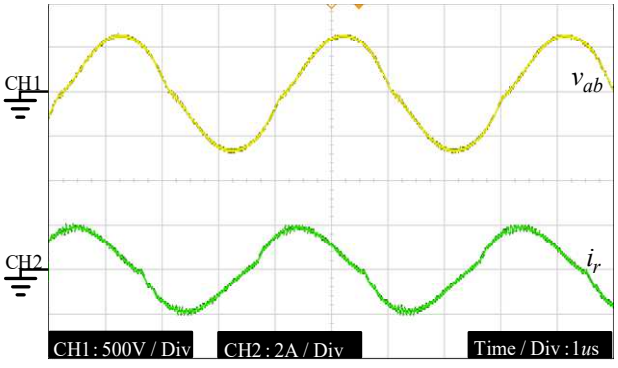

Fig. 8. Experimental result of input voltage rectifier v_{ab} and resonant current i_r waveforms at $V_{in} = 12$ V_{DC}

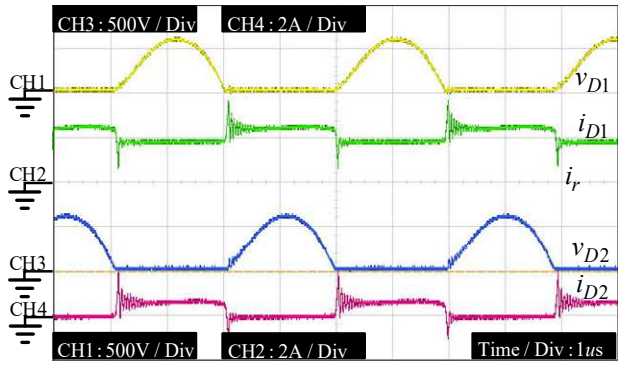

Fig. 9. Experimental result of input voltage V_{in} current I_{in} and power P_{in} waveforms at V_{in} = 12 V_{DC}

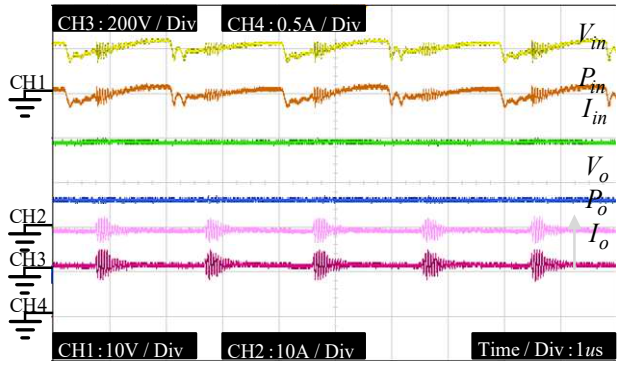

Fig. 10. Experimental result of input/output voltage V_{in}, V_o current I_{in}, I_o and power P_{in}, P_o waveforms at V_{in} =10.5 V_{DC}

series-parallel matching network is that, in the operating region with a light load, the switching frequency rises slightly to maintain output voltage regulation. Hence, the CSPPRCs with ZCS of the FB-CDR. and *LCC* series-parallel matching network presented in this research is appropriate for a wide load range input 10.5-12 V_{DC}. The prototype's circuit parameters are shown in Table I. Overall, the result voltage, current, and power input waveforms. In these the approximate V_{in} = 10.5,12 V_{DC}, I_{in} = 17.14 A ≈ 22.5 A and P_{in} = 180 W ≈ 270 W are illustrated in Figure. 6. and Figure. 10. Both currents will be indicated by the signal that is sent by the power switch M_1, M_2 as a result of this, a curvature will form in the current. Because of the property of continuous conduction mode, which CCM is shown in Figure. 7. According to these numbers, the estimated nominal both rate maximum current of i_{M1} + i_{M2} is less than ≈ 50 A. On the high-frequency input side of the FB-CDR., both the voltage v_{rec} and the current resonant i_r have a sinusoidal waveform, as illustrated in Figure. 8.; the rms v_{rec} is less than 470 V, and the i_r is less than 1.45 A. Figure. 9. illustrates the waveform as well as a zoomed-in view of a diode's voltage v_{D1}, v_{D2} as well as its current i_{D1}, i_{D2} when all of the diodes are being operated under the ZCS condition.

V. Conclusions

In this study, CSPPRCs for low-wide input sources based on applications using front-end photovoltaic cells were given. While running at 260 kHz, the circuit's overall performance at range load is more than 90%. The circuit accepts a wide input voltage ranging from 10.5 to 12 V_{DC}. This allows for the conversion of the low side to the high side output voltage, which is 330-370 V_{DC} and 180-270 W. The use of this approach has a number of advantages, including the following: a high voltage gain conversion ratio, usable components, never recovery current of power switch and a low wide input, easily reduced design parameters in the circuit produce an analogous circuit, and the fundamental theory presented may be used to non-isolated conversional dc-to-dc converter topologies.

Acknowledgment

This work was supported in part by an International Research Partnership "Electrical Engineering – Thai French Research Center (EE-TFRC)" under the project framework of the Lorraine Université d'excellence (LUE) in cooperation between Université de Lorraine and King Mongkut's University of Technology North Bangkok and in part by the National Research Council of Thailand (NRCT) under Senior Research Scholar Program under Grant No. N42A640328

References

[1] Q. Li and P. Wolfs, "A Review of the Single Phase Photovoltaic Module Integrated Converter Topologies With Three Different DC Link Configurations," in *IEEE Transactions on Power Electronics*, vol. 23, no. 3, pp. 13201333,May2008, doi:10.1109/TPEL.2008.920883.

[2] W. Li and X. He, "Review of Nonisolated High-Step-Up DC/DC Converters in Photovoltaic Grid-Connected Applications," in *IEEE Transactions on Industrial Electronics*, vol. 58, no. 4, pp. 1239-1250, April 2011, doi: 10.1109/TIE.2010.2049715.

[3] S. Kouro, J. I. Leon, D. Vinnikov and L. G. Franquelo, "Grid-Connected Photovoltaic Systems: An Overview of Recent Research and Emerging PV Converter Technology," in *IEEE Industrial Electronics Magazine*, vol. 9, no. 1, pp. 47-61, March 2015, doi: 10.1109/MIE.2014.2376976.

[4] H. Liu, H. Hu, H. Wu, Y. Xing and I. Batarseh, "Overview of High-Step-Up Coupled-Inductor Boost Converters," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 2, pp. 689-704, June 2016, doi: 10.1109/JESTPE.2016.2532930.

[5] S. Chen *et al.*, "Research on Topology of the High Step-Up Boost Converter With Coupled Inductor," in *IEEE Transactions on Power Electronics*, vol. 34, no. 11, pp. 10733-10745, Nov. 2019, doi: 10.1109/TPEL.2019.2897871.

[6] T. -J. Liang, R. -Y. Chen and J. -F. Chen, "Current-Fed Parallel-Resonant DC–AC Inverter for Cold-Cathode Fluorescent Lamps With Zero-Current Switching," in *IEEE Transactions on Power Electronics*, vol. 23, no. 4, pp. 2206-2210, July 2008, doi: 10.1109/TPEL.2008.926945.

[7] Q. Wu, Q. Wang, J. Xu, H. Li and L. Xiao, "A High-Efficiency Step-Up Current-Fed Push–Pull Quasi-Resonant Converter With Fewer Components for Fuel Cell Application," in *IEEE Transactions on Industrial Electronics*, vol. 64, no. 8, pp. 6639-6648, Aug. 2017, doi: 10.1109/TIE.2016.2638800.

[8] B. Yuan, X. Yang, X. Zeng, J. Duan, J. Zhai and D. Li, "Analysis and Design of a High Step-up Current-Fed Multiresonant DC–DC Converter With Low Circulating Energy and Zero-Current Switching for All Active Switches," in *IEEE Transactions on Industrial Electronics*, vol. 59, no. 2, pp. 964-978, Feb. 2012, doi: 10.1109/TIE.2011.2158036.

[9] J. -K. Park, W. -Y. Choi and B. -H. Kwon, "A Step-Up DC–DC Converter With a Resonant Voltage Doubler," in *IEEE Transactions on Industrial Electronics*, vol. 54, no. 6, pp. 3267-3275, Dec. 2007, doi: 10.1109/TIE.2007.906174.

[10] S. -S. Lee, S. -W. Rhee and G. -W. Moon, "Coupled Inductor Incorporated Boost Half-Bridge Converter With Wide ZVS Operation Range," in *IEEE Transactions on Industrial Electronics*, vol.56,no.7,pp. 2505-2512, July 2009, doi: 10.1109/TIE.2009.2017559.