GaN HEMT and SiC Diode Commutation Cell based Dual-Buck Single-Phase Inverter with Premagnetized Inductors and Negative Gate Driver Turn-off Voltage

Tobias Brinker, Hendrik Gräber, and Jens Friebe
Leibniz University Hannover
Institute for Drive Systems and Power Electronics
Hanover, Germany
Email: Tobias.Brinker@ial.uni-hannover.de
URL: http://www.ial.uni-hannover.de

Acknowledgments

Parts of this work were funded by the German Federal Ministry for Economic Affairs and Climate Action under Grant No. 03EE1057A (Voyager-PV) on the basis of a decision by the German Bundestag and also by the Ministry of Science and Culture of Lower Saxony and the Volkswagen Foundation. The authors are responsible for the content of this publication.

Keywords

≪Single phase system≫, ≪Switching losses≫, ≪Magentic device≫, ≪Gallium Nitride (GaN)≫, ≪Silicon Carbide (SiC)≫.

Abstract

This paper presents a highly efficient single-phase dual-buck inverter topology for the use in photovoltaic (PV) micro inverters with specific advantages for the application of switching cells composed of Gallium Nitride enhancement-mode high electron mobility transistors (GaN E-HEMTs) and Silicon Carbide (SiC) diodes. For this inverter topology, the opportunity to use negative gate driver turn-off voltage without affecting the reverse conduction loss is identified as a significant advantage in terms of efficiency and cross talk immunity. However, the low magnetic utilization of the filter inductors is a well-known drawback. Therefore, permanent magnet premagnetization is proposed as a way to alleviate this issue.

Introduction

Single-phase photovoltaic (PV) micro inverters require high efficiency and compact size as well as high reliability, making them an interesting field of application for 650 V GaN E-HEMTs. Their inherent advantages include high switching speed, high breakdown voltage and low on-resistance [1]. Despite all these, GaN E-HEMTs suffer from false turn-on phenomena due to their low threshold voltage and reverse conduction loss when switched-off during dead-time [1]. A highly efficient single-phase dual-buck inverter topology, with specific advantages for the use of GaN E-HEMTs by avoiding conventional half-bridge circuits, is presented and discussed in this paper. The topology allows high efficiency and reliability but suffers from low magnetic utilization and bulky inductor dimensions [2]. For further optimization, specific benefits regarding the use of GaN E-HEMTs and Silicon Carbide (SiC) Schottky diodes will be introduced and discussed.

For typical full-bridge inverters, the influence of the gate driver turn-off voltage $V_{\mathrm{GS,off}}$ on transistor loss has been investigated in [3]. With the reduction of $V_{\mathrm{GS,off}}$, a negative effect on the reverse conduction loss and a positive effect on the turn-off loss has been observed, prevailing slightly for higher currents.

In contrast to the full bridge topology, dead-times can be omitted in the dual buck topology due to the specific switching cells, consisting of a SiC Schottky diode and GaN E-HEMT. Therefore, the opportunity to use negative $V_{GS,off}$ without affecting the reverse conduction loss is identified as a significant advantage in terms of turn-off loss with the side effect to prevent false turn-on phenomena.

The dual buck inverter topology and its modulation scheme leads to unipolar excitation of the filter inductors during a single half-period of the output voltage [4]. For optimization of this low magnetic utilization, permanent magnetic premagnetization has been proposed as a suitable method in [5]. On this basis, an alternative configuration of permanent magnet and core is proposed and compared in this work.

This paper is structured as follows: The first section presents the dual buck inverter topology and its modulation scheme. Then the impact of negative $V_{GS,off}$ on switching losses is described analytically. For validation, double pulse tests with a hardware prototype were performed. Furthermore, the improvement of the low magnetic utilization by permanent magnetic premagnetization is discussed and the alternative concept is presented. Conclusions are given in the final section.

Dual-Buck Inverter Topology

Fig. 1 shows the proposed dual buck single-phase inverter topology and the active power driving scheme. The circuit is composed of two parallel buck converters (T1-L1-T2-D2 and T3-L2-T4-D1), whose outputs are connected to the load with opposite polarity [6, 7]. Each buck converter is modulating the output current i_{ac} for one polarity of the grid voltage v_{ac}. For the positive (negative) polarity, v_{ac} is modulated by T2 (T4) with switching frequency f_{sw}, while T1 (T3) controls the polarity of v_{ac} with low ac frequency f_{ac}. This enables an arrangement of transistors optimized for either low conduction losses (T1, T3) or low switching losses (T2, T4).

The inverter is capable of providing active and reactive power, as can be derived from the switching states depicted in Fig. 2 [6, 8]. In the figure, modulating inductor currents are indicated by the blue lines and freewheeling currents are indicated by the orange lines. In quadrants I and III, active power is fed into the grid and the switching scheme shown in Fig. 1 applies. For the reactive power quadrants (II and IV) the transistors (T1, T3) operated with f_{ac} are both turned-off, while the switching scheme of T2 or T4 does not need to be adjusted. To reduce diode conduction losses, T2 and T4 can be switched complementary in order to bypass the low ac frequency current from the diodes (dashed lines).

For the well-known issue of leakage currents in single-phase inverters, the common mode voltages over the module capacitances are relevant [4, 9]. These voltages can be measured between DC+ or DC- and the grounded neutral terminal (N) of the transformerless inverter. For active power operation (quadrants I and III), N is always connected to either the high- or low-side of the DC link (DC+, DC-, respectively). During the positive half-wave of v_{ac} (quadrant I) T1 clamps the DC+ potential to v_{ac}, while T3 clamps it to the grounded neutral terminal during the negative half-wave (quadrant III). Therefore, no discontinuities of the voltage between DC+ or DC- and ground are possible and leakage currents are considered low. [9]

For reactive power operation (quadrants II and IV), the potential of N depends on the current flow direction since T1 and T3 are turned-off. For quadrant II, D2 clamps it to v_{ac}, while D4 clamps it to DC- in quadrant IV. Regarding the voltage between DC+ or DC- and ground, a discontinuity appears when changing from any active power state to any reactive power state. As a result, peak leakage currents

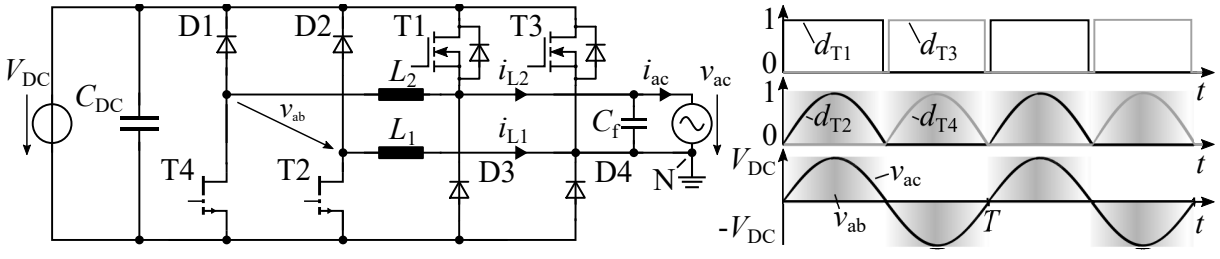


Fig. 1: Circuit diagram of dual buck inverter with control signals for active power operation.

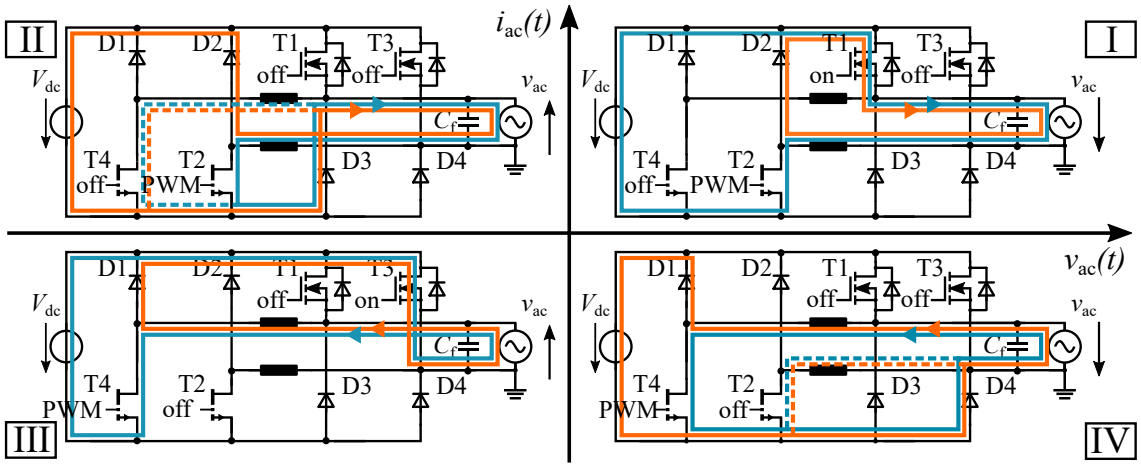


Fig. 2: Overview of the active and reactive power switching states. Modulating inductor currents are shown by the blue lines and freewheeling currents are shown by the orange lines. Dashed lines indicate additional current paths to reduce diode conduction losses.

can occur at the transition between active and reactive power states. In contrast to the conventional full-bridge inverters, the dual-buck inverter is not recommended for the use in transformerless PV inverters when reactive power capability is required. For the investigations in this paper, only active power states are considered.

Hardware Prototype

For the measurements, a prototype with adjustable $V_{GS,off}$ and exchangeable inductors has been assembled (see Fig. 3). Components were selected according to their specific characteristics (see Table I). Conduction loss optimized Silicon superjunction MOSFETs are used for the ac frequency operated transistors T1 and T3 as their switching losses are too small to be considered [7]. Due to their dynamic performance, GaN E-HEMTs and and SiC Schottky diodes are used for the high-frequency (HF) stage (T1,T4,D1-D4). Both of these are wide-bandgap devices that do not exhibit any bipolar behavior, such as reverse recovery charge Q_{rr}. Since there are no conventional half-bridge circuits, it is possible to omit dead-times for T2 and T4. Nevertheless, T1 and T3 still require a dead-time to prevent short circuiting the grid, but are only operated slowly (f_{ac}). As described in the section above, there are no reverse conduction losses for T2 and T4, which allows to use negative $V_{GS,off}$ without losing efficiency. This is expected to reduce switching loss [10] and to prevent false turn-on phenomena [1].
For the prototype a driver supply with adjustable turn-on and turn-off voltage is used. It is based on a

Table I: Hardware prototype components and operational parameters.

Parameter	Symbol	Value
GaN HEMTs	T2, T4	GS66504B
Si MOSFETs	T1, T3	IPT60R022S7XTMA1
SiC Schottky diodes	D1-D4	STPSC4H065DLF
Gate driver IC	–	Si8271 series
Adj. driver supply	–	RP-1209D, TPS7A39
Filter capacitance	C_f	250 nF (C0G)
DC-link capacitance	C_{DC}	3x 180 µF, 2x 2 µF
DC-link voltage	V_{DC}	400 V
Ext. turn-on res. (GaN)	$R_{G,on}$	3 Ω
Ext. turn-off res. (GaN)	$R_{G,off}$	0 Ω
Gate turn-on voltage (GaN)	$V_{GS,on}$	6 V

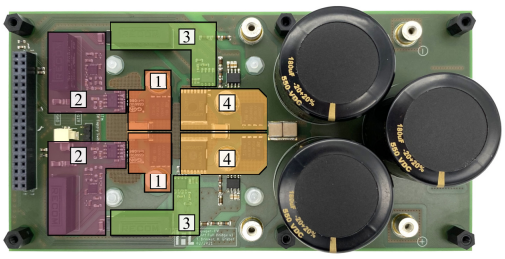


Fig. 3: Photograph of the hardware prototype.
1: GaN HEMT and SiC diode switching cells.
2: Adjustable gate driver supplies for GaN HEMTs.
3: High-side driver supplies for Si MOSFETs.
4: Si MOSFET and SiC diode commutation cells.

bidirectional low dropout regulator with the ability of regulating the negative rail down to zero volts [11]. Conventional high-side drivers with isolated driver supplies are used for all transistors of this prototype. No isolated gate driver supply is required for the low-side gate drivers [5]. The absence of di/dt in reverse conduction also allows normally-off depletion mode GaN cascodes or super junction MOSFETs to be considered, since the reverse recovery of their slow body diodes is irrelevant here [12].

Impact of Negative Gate Driver Turn-off Voltage

The effects of a negative $V_{\mathrm{GS,off}}$ on the switching characteristics were investigated with the inverter prototype configured for an inductively clamped double pulse test according to Fig. 4. The double pulse test is usually used to characterize the turn-on and turn-off energies of a transistor in dependence of the drain current. For this purpose, a high bandwidth measurement of the commutation current as well as the drain source voltage of the device under test (DUT) is required. Installing a suitable current sensor would insert additional inductance to the commutation cell and affect the measurement result. For this reason, the evaluation of the switching energies is omitted here and instead qualitative conclusions about the switching energies are drawn on the basis of slew rate measurements of v_{DS}. Thereby, an increased slew rate is associated with lower switching energy.

The results obtained from the slew rate measurements are presented in Fig. 5 and indicate faster switching transients and therefore lower switching losses for negative $V_{\mathrm{GS,off}}$ during turn-off, while for turn-on transients no significant effect can be observed. In the figure, the $R_{\mathrm{DS(on)}}$ for a junction temperature of 150° is used as an indicator for the the usable operating current range preventing saturation of the GaN E-HEMT (GS66504B [13]). The current range of the hardware prototype is highlighted to show that negative turn-off voltages do not affect the efficiency in typical inverter operation current range. In the following sections, the turn-on and turn-off sequences are examined to explain the effects more in detail.

Turn-on

The turn-on slope depends indirectly on the drain current i_{T4} via the Miller plateau voltage v_{pl} and is rather determined by the gate driver, the transconductance g_{fs} and the output capacitance C_{OSS} of the device under test (DUT) and the output capacitance of the diode $C_{\mathrm{OSS,D}}$ [14, 15, 16, 17]:

$$v_{\mathrm{pl}} = V_{\mathrm{th}} + \frac{i_{\mathrm{T4}}}{g_{\mathrm{fs}}} \tag{1}$$

$$\frac{dv_{\mathrm{DS}}}{dt} = \frac{-g_{\mathrm{fs}}(v_{\mathrm{GS}} - v_{\mathrm{pl}})}{C_{\mathrm{OSS}} + C_{\mathrm{OSS,D}}}. \tag{2}$$

As indicated in (1) v_{pl} increases for higher drain currents. For the turn-on process, this leads to a slight reduction in slew rate (see (2)) and consequently higher switching energies for higher drain currents, regardless of the gate driver turn-off voltage [15]. This explains the downward trend in turn-on speed for increasing drain currents.

Another cause for the slight enhancement in turn-on speed can be identified in the interaction of the parasitic gate inductance and the negative gate turn-off voltage [10]. While the GaN E-HEMT is switched-off, the gate-source capacitance C_{GS} is charged to $V_{\mathrm{GS,off}}$. During the turn-on process, C_{GS} is then first

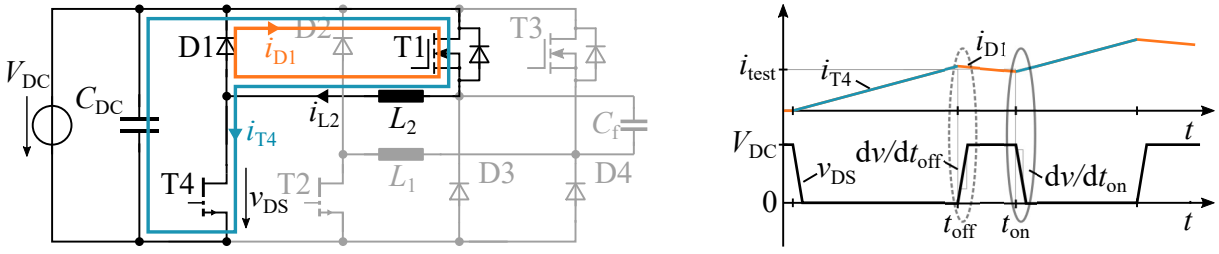


Fig. 4: Double pulse test setup of the prototype board and basic operation waveform. Slew rates dv/dt are used as indicators for switching energy. T4 is the DUT, while T1 is constantly switched-on.

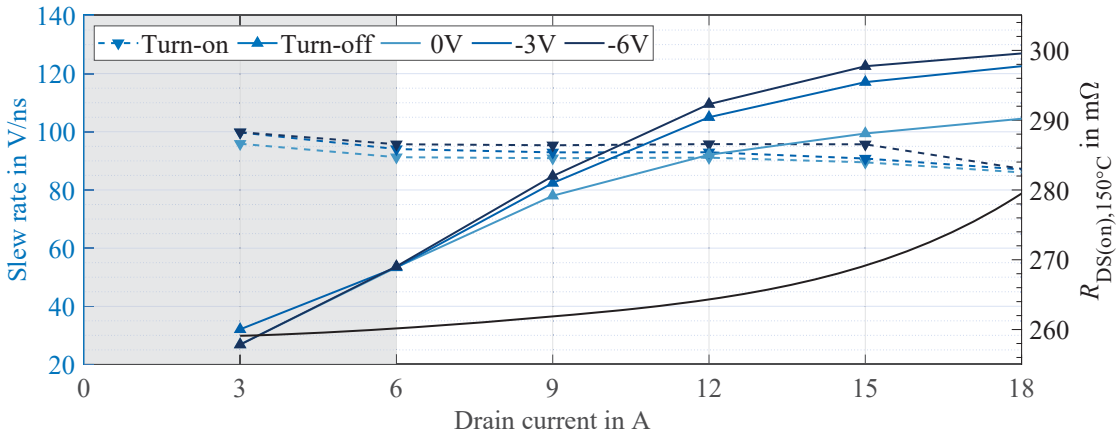


Fig. 5: Turn-on and turn-off slew rates $(10\,\% - 90\,\%)$ of v_{DS} for different $V_{GS,off}$ with respect to the drain current I_{T4}. The inverter current range is highlighted. $R_{(DS(on))}$ indicates saturation region of GaN HEMT.

charged up to V_{th}. As the threshold voltage is reached, the drain-source voltage of the semiconductor drops rapidly, causing a capacitive displacement current (Miller current) that effectively counteracts the gate current and stops the charge process of C_{GS} until C_{GD} is discharged (Miller plateau). At the same time, the nonlinear voltage dependent output capacitance C_{OSS} rises rapidly for lower V_{DS}. When a negative turn-off voltage is applied, the parasitic gate inductance is exposed to a larger voltage-time area, which results in a higher gate current being present when v_{GS} reaches the miller plateau [10]. This higher current can compensate the Miller current more effectively, keeping the gate of the semiconductor more stable above V_{th} and thus accelerating the turn-on process and in turn reduces the turn-on losses.

Turn-off

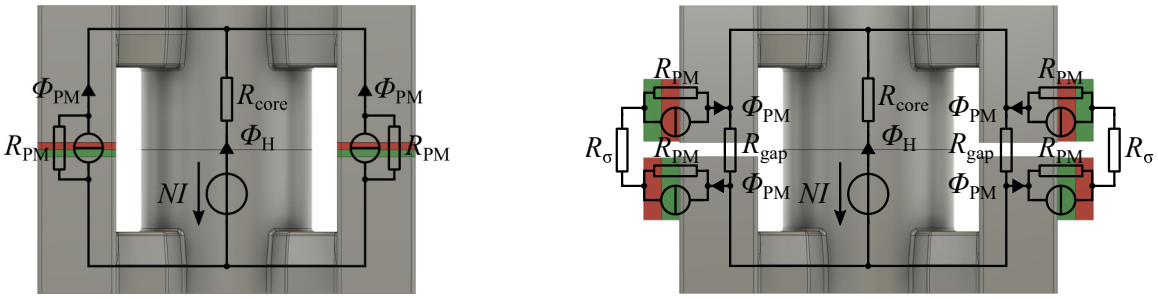
In contrast to the turn-on slope, the gate voltage can actually drop below v_{th} during the turn-off transient, at which time no 2DEG current flows at all. Therefore, (2) has to be separated for turn-off as a piecewise equation [14]:

$$\frac{dv_{DS}}{dt} = \begin{cases} \frac{i_{T4}}{C_{OSS}+C_{OSS,D}} & v_{GS} \leq V_{th} \\ \frac{g_m(v_{pl}-v_{GS})}{C_{OSS}+C_{OSS,D}} & v_{GS} > V_{th} \end{cases} \tag{3}$$

For $v_{GS} > v_{th}$ the turn-off process can exemplary be described as follows [1, 14, 15]: First, the gate current i_G starts to discharge the input capacitance C_{GS}. The load current i_{T4} continues to flow through 2DEG, with no current flowing into the output capacitance C_{OSS}. When v_{GS} drops down to v_{pl}, 2DEG starts to pinch-off and i_{T4} redirects from 2DEG into C_{OSS}. In this case, the Miller plateau voltage shift with increasing currents accelerates the turn-off transition (see (3)). During this period, the gate driver partially controls the turn-off transition by keeping v_{gs} below V_{pl}. When v_{GS} drops below V_{th}, 2DEG is completely pinched-off and entire i_{T4} charges C_{OSS} until it reaches V_{DC}. During this interval, the gate driver does not affect the turn-off slew rate at all. [16, 17]

After v_{GS} falls below V_{th}, 2DEG is completely pinched-off and the entire i_{T4} charges C_{OSS} until it reaches V_{DC}. For GaN E-HEMTs, applying a negative gate driver turn-off voltage reduces v_{pl} [16, 17]. In principle, v_{GS} can be immediately dropped below v_{th} by selecting a proper negative gate driver turn-off voltage. Then no Miller plateau is visible and the turn-off transition is completely controlled by the drain current, potentially accelerating the switching transient and lowering the switching energy.

From the experimental data provided in Fig. 5 an increase in turn-off slew rate can be observed for negative $V_{GS,off}$ and higher drain currents. For lower drain currents in the range below approx. 9 A, no significant deviation of the slew rate from zero volt can be observed for negative $V_{GS,off}$. For drain currents above 9 A, the 2DEG is apparently pinched off by v_{GS} for each investigated negative turn-off voltage of the gate driver, since no significant change in the slew rate can be observed between negative $V_{GS,off}$.



(a) (b)

Fig. 6: (a) Serial concept of premagnetization with PM inserted into the air gaps and (b) parallel concept with PM located in the vicinity of the air gaps. Magnetic north and south poles of the PM are marked in red and green, respectively.

Permanent Magnet Premagnetized Filter Inductors

From Fig. 2 can be derived, that in each switching state, current only can flow in one direction through one of the two inductors, leading to a poor magnetic utilization, which depicts the main drawback of the topology. Although, this significantly affects the weight and volume of the system, it does not affect the efficiency [6, 8]. Due to their low utilization, the inductors can be designed with at least twice the specific core losses during switching operation of their corresponding half-bridge. As a direct consequence of this, the inductor design of both inductors will lead to a higher switching frequency of which the saturation flux will limit the design instead of the thermal limit [5]. A optimization possibility is offered by PM premagnetization [5]. Single inductor variants of the inverter have been introduced, but suffer from higher conduction loss due to additional switches or diodes in the power loop [8].

The concept of PM premagnetization is as follows: One or more PM is used to insert a negative flux into the core to extend the saturation flux density for unipolar excitation. As a result, a smaller core volume can be used and thus a higher magnetic utilization can be achieved.

The most conventional and intuitive approach of PM premagnetization is illustrated in Fig. 6a and relies on inserting PM into the air gap of the power inductor [5]. This imposes several intrinsic constraints on the available magnetic cross section A_{PM}, demagnetization by the flux ϕ generated by the coil, and eddy current losses in the PM material at high switching frequencies [18]. However, this approach provides the most compact volume and can be used with standard cores. Other variants of this concepts include inserting PM into all air gaps or in the central leg only.

To prevail the limitations mentioned above, PM can be placed in the vicinity of the air gaps according to Fig. 6b. In this configuration, the PM may not be crossed by the magnetic flux generated by the coil, resulting in lower eddy current losses. Eddy currents are rather generated by deviations in the PM reluctance which are caused by the change of the PM operating point, but are smaller than those caused

Fig. 7: Parameters of conventional and premagnetized inductors with 40 % copper filling factor.

Parameter	Air gap (no PM)	Parallel concept	Serial concept
Core type	PQ32/20	PQ26/20	PQ26/20
Effective magnetic cross section	154.2 mm^2	122.6 mm^2	122.6 mm^2
Core box volume	15 cm^2	12.57 cm^2	10.57 cm^2
Permanent magnet material	-	Neofer 41/100p	Neofer 41/100p
Number of turns	31	26	26
Air gap width (central/outer leg)	0.8/0.8 mm	0/1 mm	0/1 mm
Dimensions	(32x22x21.3) mm	(31.5x19x21) mm	(26.5x19x21) mm
Core box volume	15 cm^3	12.57 cm^3	10.57 cm^3

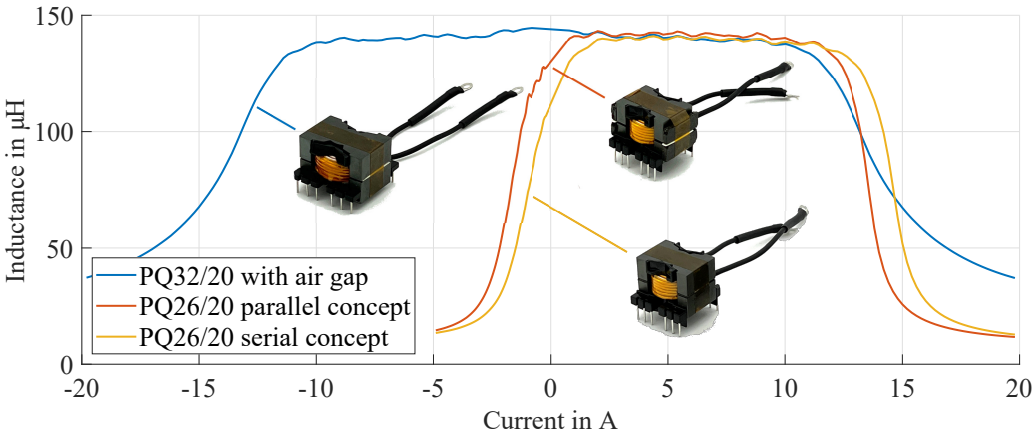


Fig. 8: L-I curves of conventional PQ32/20 inductors and premagnetized PQ26/20 inductors.

by direct induction. There are also no limitations in space in terms of magnetic cross-section and PM length. However, when using standard cores, this configuration results in an increased box volume due to the external PMs. [18]

The dimensioning of the magnetic circuit is not different from conventional air gapped inductors and is dominated by the relucatance of the air gaps (see Fig. 6). For a complete shift of the L-I characteristic the relation given in (4) can be used. The dimensioning of the combined magnetic circuit can be performed following the methodology presented in [19], considering the lumped magnetic circuits given in Fig. 6.

$$B_{\mathrm{PM}} = \frac{L \cdot I_{\mathrm{sat}}}{N A_{\mathrm{PM}}} \tag{4}$$

Table 7 compares a conventional PQ32/20 inductor with two premagnetized configurations based on smaller PQ26/20 cores. Polymer-bonded (PA11) rare earth magnets (NdFeB) of Neofer 41/100p type were used for both configuration. These magnets are characterized by a residual flux density B_{r}, that fits to the saturation flux density of the TDK N95 ferrite core material. They also have good mechanical properties and are easy to shape. All inductors were set up with the same copper filling factor of 40 % and same litz wire (100x0.1 mm). The air gap is adjusted in order to reach the inductance of 140 µH. Fig. 8 shows the measured L-I curves, which show almost equal saturation currents of the premagnetized and conventional inductors.

For unipolar excitation, as it appears for the investigated inverter topology, a premagnetized inductor with up to 30 % smaller core volume can be used. Another advantage of using smaller cores is the reduced number of turns, which improves winding losses.

Conclusion

In this paper, two design improvement options for a specific single-phase dual-buck inverter topology using GaN E-HEMTs and SiC Schottky diodes were identified and investigated. For this purpose, an analysis of the switching states for both, active and reactive power operation has been performed. This revealed a low utilization of the magnetic components and the possibility to omit dead-times for the GaN E-HEMTs and SiC Schottky diode based switching cells. The absence of dead-times eliminates reverse conduction losses when the GaN E-HEMT is switched-off. This gives the opportunity to use a negative gate driver turn-off voltage $V_{\mathrm{GS,off}}$ without affecting the reverse conduction losses.

A prototype with adjustable $V_{\mathrm{GS,off}}$ and exchangeable inductors has been assembled and double pulse tests were performed. Instead of evaluating of the switching energies, qualitative conclusions about the switching energies are drawn on the basis of slew rate measurements of v_{DS}. From the experimental data an increase in turn-off slew rate can be observed for negative $V_{\mathrm{GS,off}}$, but only for higher drain currents, while no significant effect on slew rate could be observed. Thus, it could be shown that a negative $V_{\mathrm{GS,off}}$

cannot affect the efficiency, since a significant reduction of switching loss only becomes evident beyond the current range of a typical inverter configuration.

Permanent magnet (PM) premagnetization has been proposed to overcome poor magnetic utilization. Therefore, two PM configurations were proposed and compared based on their specific characteristics and design limitations. A comparison of premagnetized and conventional PQ core-based inductors on the basis of L-I curve measurements showed that a premagnetized inductor with a 30 % smaller PQ26/20 core can be used instead of the conventional PQ32/20 inductor for the investigated inverter topology.

References

[1] Jianchun Xu, Yajie Qiu, Di Chen, Juncheng Lu, Ruoyu Hou, Peter Di Maso, "An Experimental Comparison of GaN E-HEMTs versus SiC MOSFETs over Different Operating Temperatures," *GaN Systems Inc.*, Online: http://www.gansystems.com, accessed: 10/28/2021.

[2] P. Zacharias, "Inverter capable of providing reactive power," U.S. Patent 8 638 581 B2, Oct. 9, 2009.

[3] H. Qin, W. Wang, Z. Peng, A. Liu, and S. Bai, "Characterization and optimization of gate driver turn-off voltage for eGaN HEMTs in a phase-leg configuration," Energy Reports, vol. 8. Elsevier BV, pp. 908–919, Apr. 2022. doi: 10.1016/j.egyr.2021.11.093.

[4] W. Li, Y. Gu, H. Luo, W. Cui, X. He and C. Xia, "Topology Review and Derivation Methodology of Single-Phase Transformerless Photovoltaic Inverters for Leakage Current Suppression," in IEEE Transactions on Industrial Electronics, vol. 62, no. 7, pp. 4537-4551, July 2015.

[5] J. Friebe, S. Lin, L. Fauth and T. Brinker, "Premagnetized Inductors in Single Phase dc-ac and ac-dc Converters," *2019 IEEE 15th Brazilian Power Electronics Conference and 5th IEEE Southern Power Electronics Conference (COBEP/SPEC)*, 2019, pp. 1-6.

[6] S. V. Araujo, P. Zacharias and R. Mallwitz, "Highly Efficient Single-Phase Transformerless Inverters for Grid-Connected Photovoltaic Systems," in *IEEE Transactions on Industrial Electronics*, vol. 57, no. 9, pp. 3118-3128.

[7] Y. Wang, L. Yang, Z. Meng, G. Li and P. Chen, "Power loss distribution analysis for a high frequency dual-buck full-bridge inverter," *2017 IEEE Transportation Electrification Conference and Expo*, (ITEC Asia-Pacific), 2017, pp.1-6.

[8] L. Zhou and F. Gao, "Dual buck inverter with series connected diodes and single inductor," *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2016, pp. 2259-2263.

[9] D. Barater, E. Lorenzani, C. Concari, G. Franceschini, and G. Buticchi, "Recent advances in single-phase transformerless photovoltaic inverters," IET Renewable Power Generation, vol. 10, no. 2. Institution of Engineering and Technology (IET), pp. 260–273, Feb. 2016. doi: 10.1049/iet-rpg.2015.0101.

[10] L. Will, S. Sprunck and P. Zacharias, "Impact of Negative Turn-Off Voltage On Turn-On Losses in GaN E-HEMTs," *PCIM Europe digital days 2020; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2020, pp. 1-5.

[11] Texas Instruments Incorporated, "TPS7A39 Dual, 150-mA, Wide VIN Positive and Negative LDO Voltage Regulator," Datasheet, SBVS263A, 2017.

[12] T. Kerekes, R. Teodorescu, P. Rodríguez, G. Vázquez and E. Aldabas, "A New High-Efficiency Single-Phase Transformerless PV Inverter Topology," in *IEEE Transactions on Industrial Electronics*,vol.58,no.1,pp.184-191,Jan.2011.

[13] GaN Systems Inc, "GS66504B Bottom-side cooled 650 V E-mode GaN transistor," Datasheet, Rev 200402, 2020.

[14] E. A. Jones, Z. Zhang and F. Wang, "Analysis of the dv/dt transient of enhancement-mode GaN FETs," *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2017, pp. 2692-2699.

[15] B. Sun, Z. Zhang and M. A. E. Andersen, "Switching transient analysis and characterization of GaN HEMT," *2018 3rd International Conference on Intelligent Green Building and Smart Grid (IGBSG)*, 2018, pp. 1-4.

[16] Z. Wang, Y. Wu, J. Honea and L. Zhou, "Paralleling GaN HEMTs for diode-free bridge power converters," *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2015, pp. 752-758.

[17] L. Lu, G. Liu and K. Bai, "Critical transient processes of enhancement-mode GaN HEMTs in high-efficiency and high-reliability applications," in *CES Transactions on Electrical Machines and Systems*, vol.1, no.3, pp.283-291, Sept.2017.

[18] A. R. Aguilar and S. Munk-Nielsen, "Design, analysis and simulation of magnetic biased inductors with saturation-gap," *2014 16th European Conference on Power Electronics and Applications*, 2014, pp. 1-11.

[19] S. Lin, J. Friebe, S. Langfermann and M. Owzareck, "Premagnetization of High-Power Low-Frequency DC-Inductors in Power Electronic Applications," PCIM Europe 2019; *International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2019, pp. 1-7.