dV/dt-Based Filter Design for Motor Inverters with Continuous Output Voltage

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Keywords

≪DC-AC Converter≫, ≪Inverter-output filter≫, ≪Passive filters≫, ≪Gallium Nitride (GaN)≫, ≪dV/dt≫

Abstract

Wide bandgap semiconductors enable high switching frequencies and thus the integration of filters into the inverter. The current paper addresses the design problem for the filter components such that a given dV/dt at the inverter terminals is obtained.

Introduction

The application of wide bandgap (WBG) semiconductors opens the option for higher switching frequencies in a range well above 500 kHz. Due to these switching frequencies, a new inverter concept becomes feasible, where filters are integrated into the inverter printed circuit board (PCB) to produce quasi-continuous output voltages. In [1] such a concept was presented for a three-phase inverter for fractional power synchronous machines.

The research activities conducted so far, illustrated, that in spite of the high switching frequencies the passive components are still significantly determining the size of this converter type. As one of the main benefits of this converter type is given by the reduction of the dV/dt values at the motor terminals, a minimum size of the filter components can be obtained by specifying a maximum dV/dt and deriving the filter inductor and capacitor size such, that this requirement is satisfied with minimum passive component sizes. This question is addressed in [2] for a LRC filter, that is, a filter with a passive damping, based on the analysis of the filter step response or in [3] based on transfer function considerations for an LC filter. An additional aspect is discussed in [4], where the effect of motor cables is considered as well.

In [2], as well as in other publications, the need for damping of the LC resonant structure is emphasized and a passive resistor based damping is applied. In the concept discussed in [1], an active damping based on inductor current feedback is introduced. The current publication discusses the LC filter design for the concept from [1]. A new design procedure is given, that determines the filter parameter such that a

maximum dV/dt is respected. To preserve the active damping capabilities, the influence of the design on the inductor current feedback based damping is considered in the design process, as well.

The paper is organized as follows: First, the power electronics module with the output filter for quasi-continuous output voltage is described. Then, the relationship between the filter parameters and the dV/dt of the output voltage is derived, followed by design considerations for the LC filter parameter. Next, some simulations and measurements are illustrated. Finally, conclusions are given.

Inverter system

The inverter for three-phase motor control with quasi-continuous output voltage from [1], considered in this paper, is illustrated in Fig. 1. Each phase consists of a half-bridge (HB) with DC voltage V_B, where the modulation is achieved by a asynchronous delta-sigma ($\Delta\Sigma$) modulator. The input signals of each modulator are the reference input signal $v_{O\,Ref}$, the voltage v_{HB} at the HB switching node and the filter inductor current i_{LF} for the respective phase. This is illustrated in more detail for one phase in Fig. 2.

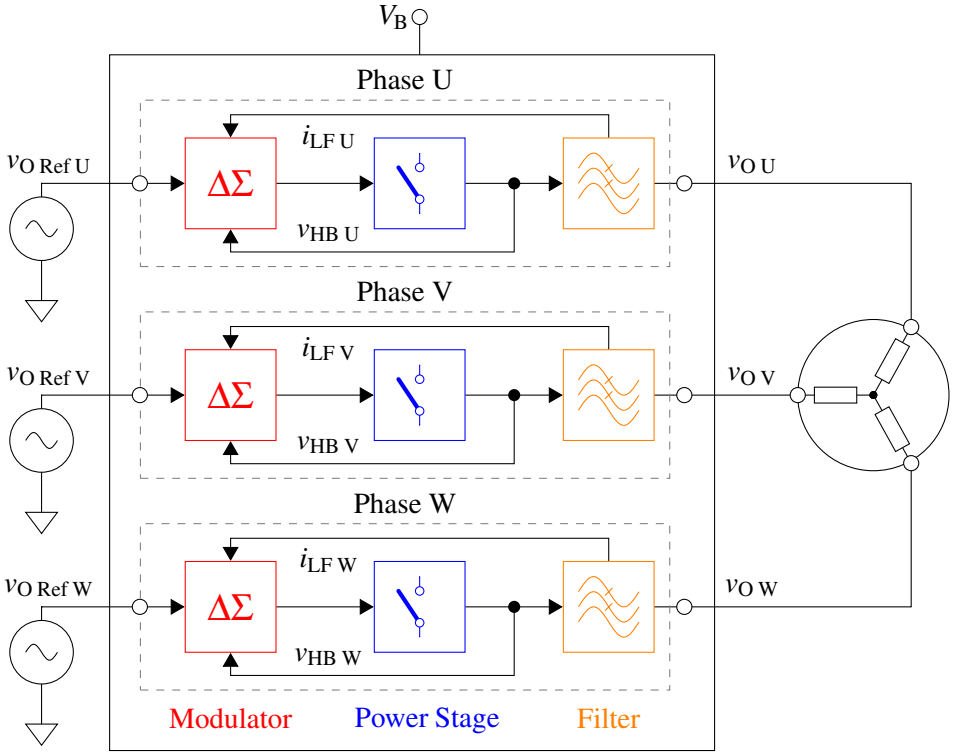


Fig. 1: GaN-based motor inverter with quasi-continuous output voltage

The output voltage v_O for each phase results from filtering the pulsed voltage v_{HB} with an LC filter. For active damping as in [1] an inductor current feedback with the transfer characteristic G_{FB} [5] is applied. A motor winding is connected to the filter output terminals, where the back-emf is not illustrated for simplicity. In the following section, design considerations for the parameters L_F and C_F of the filter are given.

Filter design

The design rule calculation approach depends on the relationship of the filter resonance frequency and the switching frequency [2]. If the filter resonance is higher than the switching frequency, then the dV/dt analysis can be done based on the step response of the filter as e.g. in [2]. For the discussion given below the motor winding will not be considered yet, that is, the phase module will be operated with open terminals. The influence of the motor winding on the results, obtained below, will be investigated in simulations.

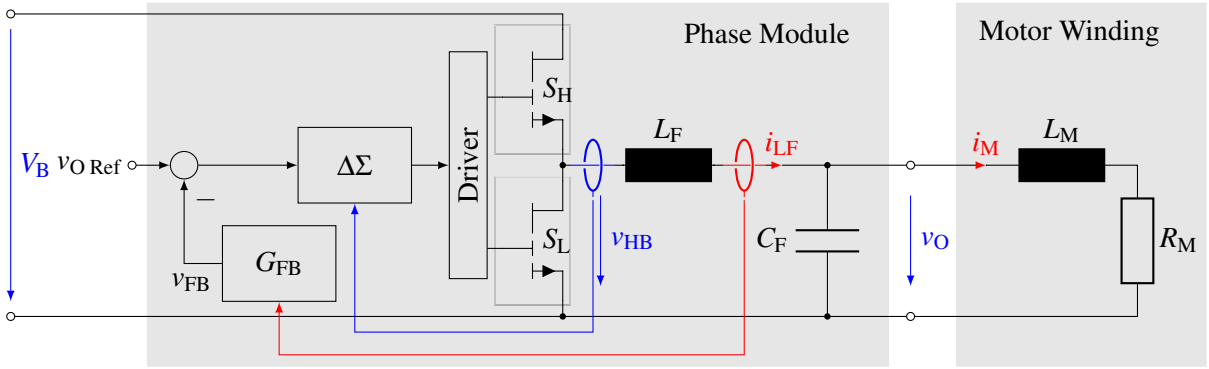


Fig. 2: Phase module with motor winding

We denote with

$$G_{VO} = \frac{1}{L_F C_F\, s^2 + 2\sqrt{L_F C_F}\, s + 1} \tag{1}$$

the transfer function with v_{HB} as input and v_O as output variable using the feedback rule

$$G_{FB} = 2\sqrt{\frac{L_F}{C_F}}$$

as in [1]. The step response $h_{VO}(t)$ of this transfer function is then calculated using (1) and the inverse Laplace transform. Differentiating the step response $h_{VO}(t)$ yields

$$\frac{\mathrm{d}h_{VO}}{\mathrm{d}t} = \frac{t}{L_F C_F}\, \mathrm{e}^{-\frac{t}{\sqrt{L_F C_F}}}$$

with the maximum at

$$t = \sqrt{L_F C_F} \qquad \text{as} \qquad \left.\frac{\mathrm{d}h_{VO}}{\mathrm{d}t}\right|_{t=\sqrt{L_F C_F}} = \frac{1}{\mathrm{e}\sqrt{L_F C_F}}\,,$$

corresponding to the maximum dV/dt, given an input voltage step of 1 V. Note, that this value will slightly differ from the value in [2], where dV/dt is determined based on two selected points in the step response.

In the case, when the filter resonance frequency is between the signal frequency and the switching frequency, the approach given above is not valid. Here, a new approach for determining a relationship between the dV/dt, that is, the slew rate, values and the filter parameters are developed. It is based on the idea that the filter structure from Fig. 2 is the output filter of a buck converter. In the sequel, we assume a triangular current shape during one switching interval of duration T_S as illustrated in the left-hand side of Fig. 3.

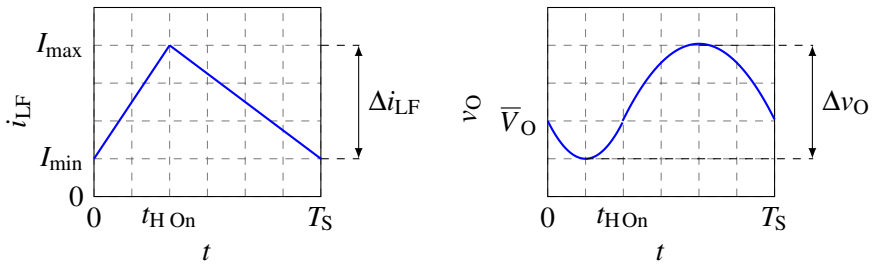


Fig. 3: Inductor current i_{LF} and output voltage v_O

In addition, we denote by t_{HOn} the on-time duration of the upper switch S_{H} of the half-bridge, by $\overline{V}_{\mathrm{O}}$ the output voltage at the beginning of the switching interval in steady state, Δi_{LF} the inductor current ripple and $\Delta v_{\mathrm{O}}(t) = v_{\mathrm{O}}(t) - \overline{V}_{\mathrm{O}}$. Then, we obtain after some calculations for $t \in [0 \quad t_{\mathrm{HOn}}]$

$$\Delta v_{\mathrm{O}}(t) = \frac{\Delta i_{\mathrm{LF}}}{2\,C_{\mathrm{F}}}\left(\frac{t^2}{t_{\mathrm{HOn}}} - t\right) \qquad \Rightarrow \qquad \frac{\mathrm{d}\Delta v_{\mathrm{O}}}{\mathrm{d}t} = \frac{\mathrm{d}v_{\mathrm{O}}}{\mathrm{d}t} = \frac{\Delta i_{\mathrm{LF}}}{2\,C_{\mathrm{F}}}\left(\frac{2\,t}{t_{\mathrm{HOn}}} - 1\right) .$$

The maximum slew rate is obtained for $t = t_{\mathrm{HOn}}$

$$\left.\frac{\mathrm{d}v_{\mathrm{O}}}{\mathrm{d}t}\right|_{t=t_{\mathrm{HOn}}} = \frac{\Delta i_{\mathrm{LF}}}{2\,C_{\mathrm{F}}} \quad \text{where} \quad \Delta i_{\mathrm{LF}} = \frac{V_{\mathrm{B}}(1-d)}{L_{\mathrm{F}}} dT_{\mathrm{S}} \quad \text{as} \quad \left.\frac{\mathrm{d}v_{\mathrm{O}}}{\mathrm{d}t}\right|_{t=t_{\mathrm{HOn}}} = \frac{V_{\mathrm{B}}(1-d)}{2\,C_{\mathrm{F}}L_{\mathrm{F}}} dT_{\mathrm{S}} , \quad (2)$$

where

$$d = \frac{t_{\mathrm{HOn}}}{T_{\mathrm{S}}} \quad (3)$$

is the duty cycle. For a more detailed analysis, the modulator structure and the corresponding signals are illustrated in Fig. 4.

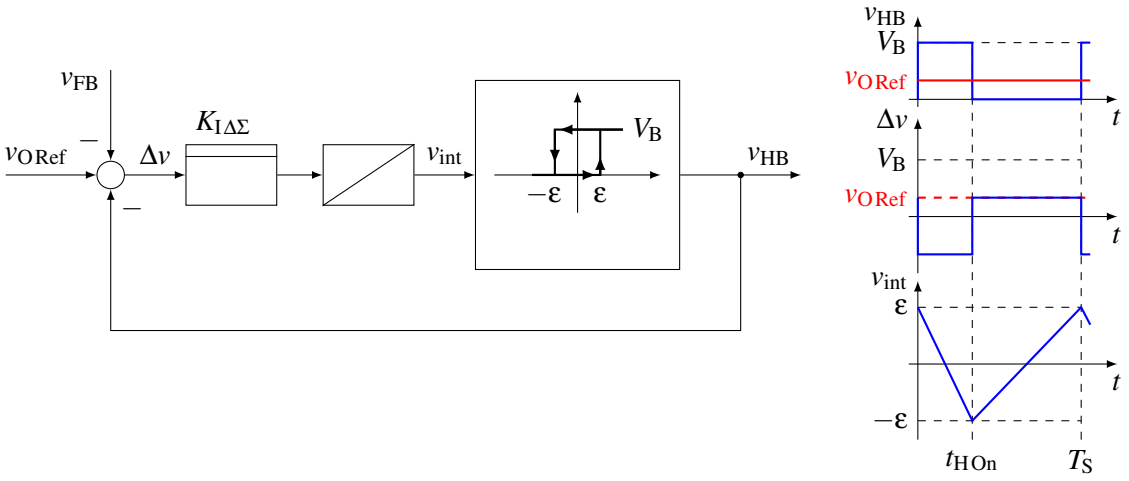


Fig. 4: Modulator structure and modulator signals

First, we do not consider the current feeback, that is, $v_{\mathrm{FB}} = 0$. From Fig. 4 one obtains

$$t_{\mathrm{HOn}} = -\frac{2\,\varepsilon}{K_{\mathrm{I}\Delta\Sigma}(v_{\mathrm{ORef}} - V_{\mathrm{B}})} ,$$

$$T_{\mathrm{S}} - t_{\mathrm{HOn}} = \frac{2\,\varepsilon}{K_{\mathrm{I}\Delta\Sigma}\,v_{\mathrm{ORef}}} \qquad \Rightarrow \qquad T_{\mathrm{S}} = \frac{2\,\varepsilon}{K_{\mathrm{I}\Delta\Sigma}\,v_{\mathrm{ORef}}}\frac{V_{\mathrm{B}}}{V_{\mathrm{B}} - v_{\mathrm{ORef}}} . \quad (4)$$

From (4) one obtains after some calculations

$$(1-d)dT_{\mathrm{S}} = \frac{K}{V_{\mathrm{B}}} \qquad \text{with} \qquad K = \frac{2\,\varepsilon}{K_{\mathrm{I}\Delta\Sigma}} , \quad (5)$$

where K is proportional to the modulator hysteresis width $2\,\varepsilon$ and to the inverse of the integrator gain $K_{\mathrm{I}\Delta\Sigma}$. Introducing the result from (5) into (2) we obtain

$$\Delta i_{\mathrm{LF}} = \frac{K}{L_{\mathrm{F}}} \quad (6)$$

and

$$\left.\frac{\mathrm{d}v_\mathrm{O}}{\mathrm{d}t}\right|_{t=t_{\mathrm{HOn}}} = \frac{K}{2\,C_\mathrm{F}L_\mathrm{F}} \quad . \tag{7}$$

This result illustrates that, assuming the filter resonance frequency below the switching frequency, the dV/dt value can be influenced by both output filter component values, as well as the constant K, depending on the modulator design parameters ε and $K_{\mathrm{I}\Delta\Sigma}$. From (4) it is obvious, that K is related to the switching period T_S or equivalently the switching frequency f_S, such that this relationship is reasonable, as well.

Besides the slew rate of the output voltage, the inductor current ripple Δi_{LF} is relevant for the system design. A high current ripple increases the stress in the switches. It increases the inductor losses and influences the inductor design as the core size will typically increase in order to avoid saturation [6]. In addition, a high current ripple influences the modulator via the voltage v_{FB} (see Fig. 4). A detailed analytical evaluation of this effect is beyond the scope of this paper. However, the influence will be evaluated in a simulation.

The design steps are basically the same as in [2] or [3]. Note however, that the design equations are different.

1. Specify the maximum admissible current ripple $\Delta I_{\mathrm{LF\,max}}$ and the maximum dV/dt value,
2. Calculate L_F from (6) given K,
3. Calculate C_F from (2) given K and L_F from step 2,
4. Check whether the filter resonance frequency is below the minimum switching frequency and adapt design requirements and/or K if necessary.

If the design results in a filter resonance frequency that is too high, the switching frequency can be increased by modifying K. Alternatively, the filter parameters can be modified to reduce the filter resonance frequency. This will either reduce the inductor current ripple or the dV/dt value or both.

These considerations were developed based on the buck converter concept, thus implicitly assuming a constant output voltage v_O. For sinusoidal output voltages, these results will give a reasonable approximation, if the frequency of the sinusoidal signal is below the resonance frequency by a reasonable factor. This will be illustrated in simulations.

Simulations

For simulation, the system illustrated in Fig. 2 was implemented in a Simulink-Simscape environment with the parameters given in Table I. To illustrate the influence of the filter design on the output voltage, three different values were used for the filter inductance L_F and the output capacitor C_F, respectively.

V_B	ε	$K_{\mathrm{I}\Delta\Sigma}$	G_{FB}		L_F	C_F	f_0
48 V	0.1	2×10^4	$\frac{T_\mathrm{F}\,k_{\mathrm{IL}}}{T_\mathrm{F}\,s+1}$	$k_{\mathrm{IL}} = 2\sqrt{\frac{L_\mathrm{F}}{C_\mathrm{F}}}$	4.7 µH	330 nF	127.8 kHz
				$T_\mathrm{F} = 1\,\mu\mathrm{s}$	15 µH	680 nF	49.8 kHz
					33 µH	1.36 µF	23.8 kHz

Table I: System parameters

Fig. 5 illustrates the trajectories of the inductor current i_{LF}, the output voltage v_O and the corresponding estimated value for $\mathrm{d}v_\mathrm{O}/\mathrm{d}t$ estimated from v_O using the filter

$$\frac{s}{1\times10^{-7}s+1} \tag{8}$$

in the time interval marked in Fig. 6 by the red rectangle for the output voltage v_O for the variations of L_F and C_F from Table I.

Fig. 6 displays the output voltage v_O for a input reference signal $v_{ORef} = (24 + 15\ \sin(2\pi f\, t))$V where f is 1 kHz. Note, that the offset in v_{ORef} results from the HB configuration as shown in Fig. 2 producing a DC offset of $\frac{1}{2}V_B = 24$ V. The simulation data in Fig. 5, 6 and 8 was produced with a load resistance of $R_L = 1\,\text{k}\Omega$ at the output terminals of the phase module, thus simulating a situation close to the open terminal case.

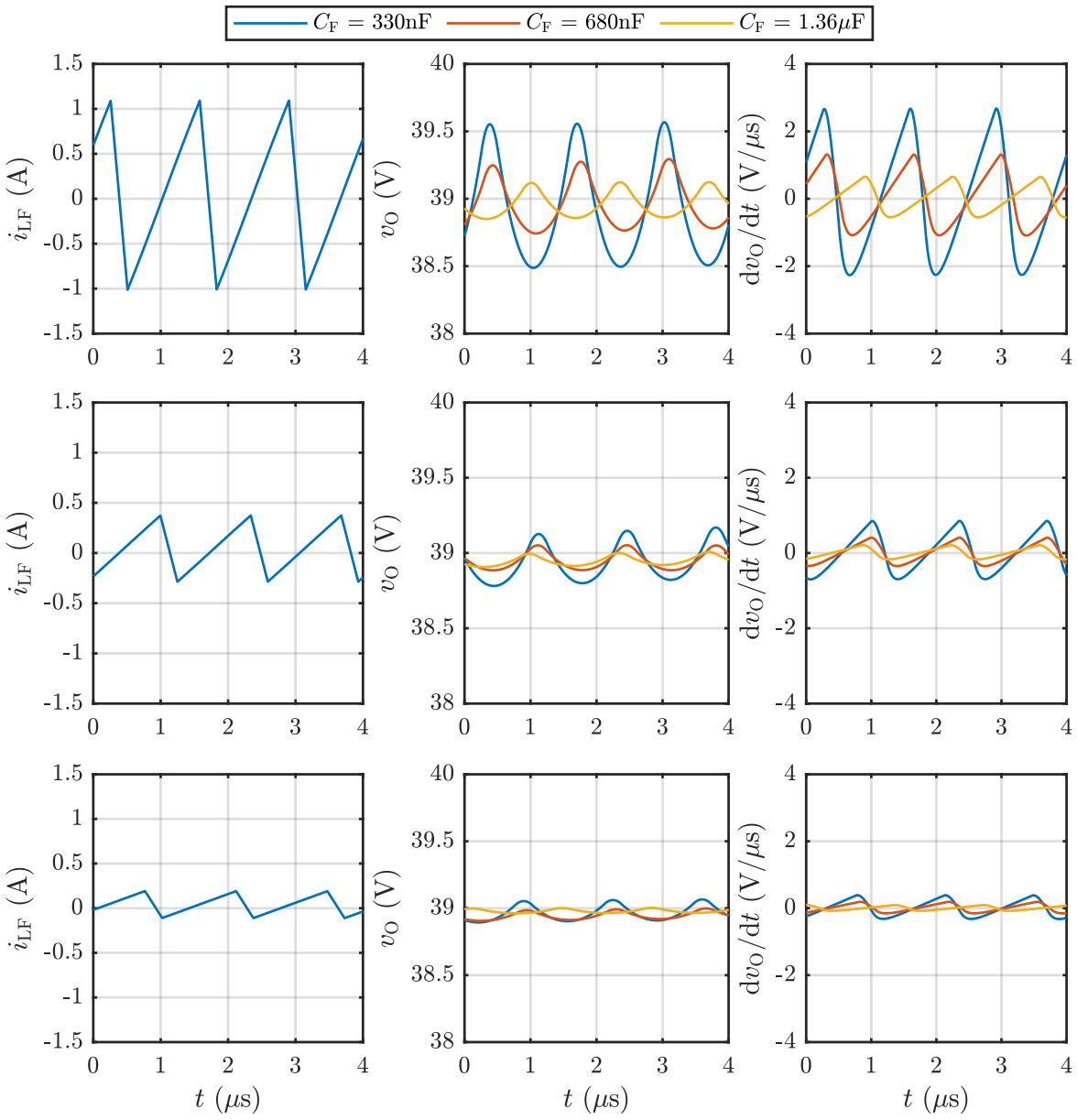


Fig. 5: Detailed view of simulation results for $R_L = 1\,\text{k}\Omega$ with variation of L_F, C_F: Upper row: $L_F = 4.7\,\mu$H, middle row: $L_F = 15\,\mu$H, lower row: $L_F = 33\,\mu$H

In Table II the inductor current ripple values Δi_{LF} and the slew rate dv_O/dt for all combinations of L_F and C_F given in Table I are calculated using (6) and (7), respectively, for comparison with the trajectories in Fig. 5. Note, that according to (6) the current ripple Δi_{LF} does not depend on the filter capacitor C_F, such that it is the same for all three capacitor values. The slew rates given in Table II correspond to the maximum values in the right-hand side plots in Fig. 5.

In Fig. 7, the effect of filter parameter variation is illustrated in simulations, where a motor winding with

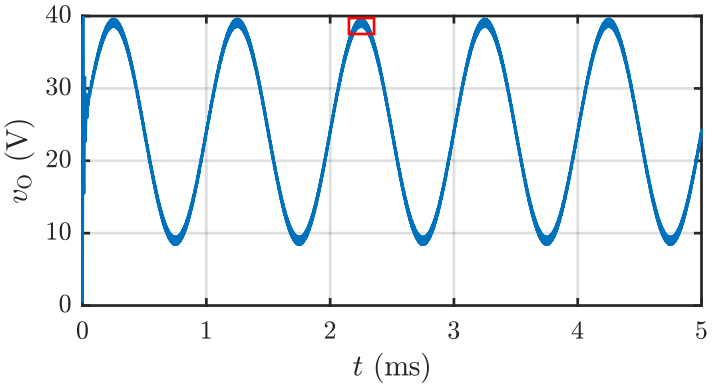


Fig. 6: Simulation result for the output voltage v_O with $L_F = 4.7\,\mu H$, $C_F = 330\,nF$

L_F	Δi_{LF}	C_F	330 nF	680 nF	1.36 µF
4.7 µH	2.13 A		3.22 V/µs	1.56 V/µs	0.78 V/µs
15 µH	670 mA	dv_O/dt	1.01 V/µs	0.49 V/µs	0.24 V/µs
33 µH	300 mA		0.46 V/µs	0.22 V/µs	0.11 V/µs

Table II: Values calculated with (6) and (7)

$R_M = 0.4\,\Omega$ and $L_M = 1\,mH$ is connected to the phase module terminals as illustrated in Fig. 2. The results and the comparison with Fig. 5 illustrate, that the effect of the motor winding on the slew rate of the phase module output voltage is small, as expected due to the large difference between the filter inductance L_F and the motor inductance L_M.

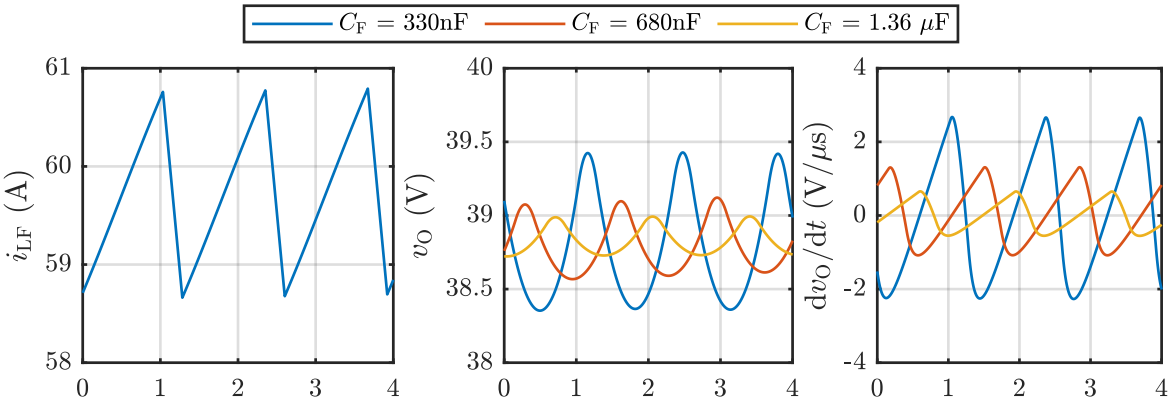


Fig. 7: Detailed view of simulation results with motor winding, $L_F = 4.7\,\mu H$ and variation of C_F

Finally, Fig. 8 displays the effect of the current ripple due to a low filter inductance value on the modulation. It is observed, that for $L_F = 0.47\,\mu H$ the switching frequency increases with respect to the case with $L_F = 15\,\mu H$ due to the higher values of Δv. From the given filter parameter one obtains a filter resonance frequency in the range of the switching frequency such that this design parameter set is out of the range given by the above mentioned design procedure.

Measurements

The hardware setup is given in Fig. 9. Fig. 9b illustrates the laboratory measurement setup with phase module, oscilloscope, power supply and signal generator for generating the input reference signal $v_{O\,Ref}$, whereas Fig. 9a displays the phase module PCB, where the GaN HB is marked by a red rectangle. The output voltage is measured with open terminals of the phase module, using a voltage probe with a

bandwidth of 500 MHz connected to an oscilloscope with a bandwidth of 500 MHz. The inductor current trajectory is not displayed in the measurements as the bandwidth of the current sensor integrated into the phase module for current feedback is given by 80 kHz. Although this is sufficient for the feedback illustrated in Fig. 2 it is not sufficient for displaying the current ripple.

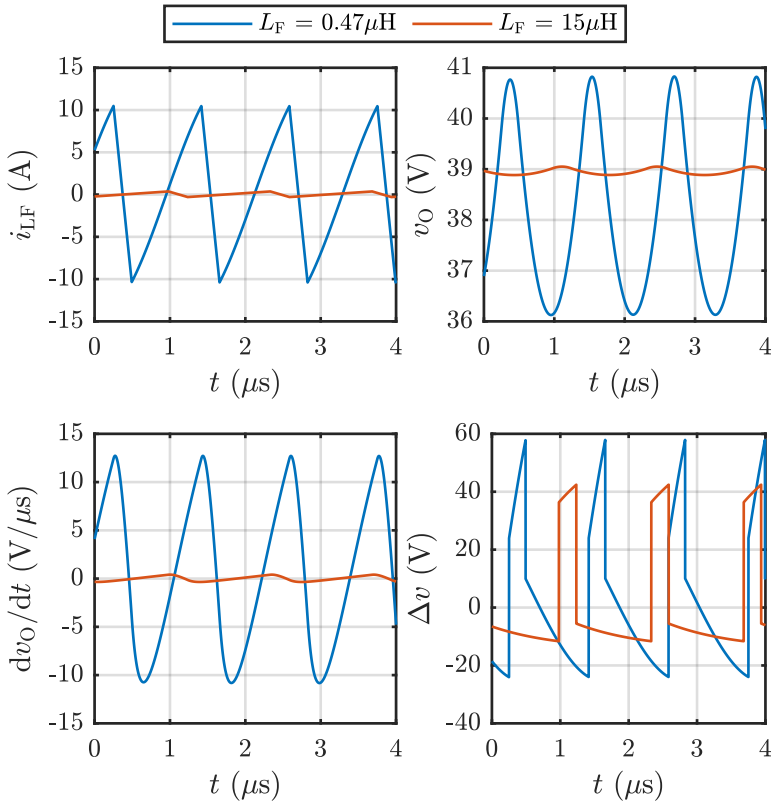
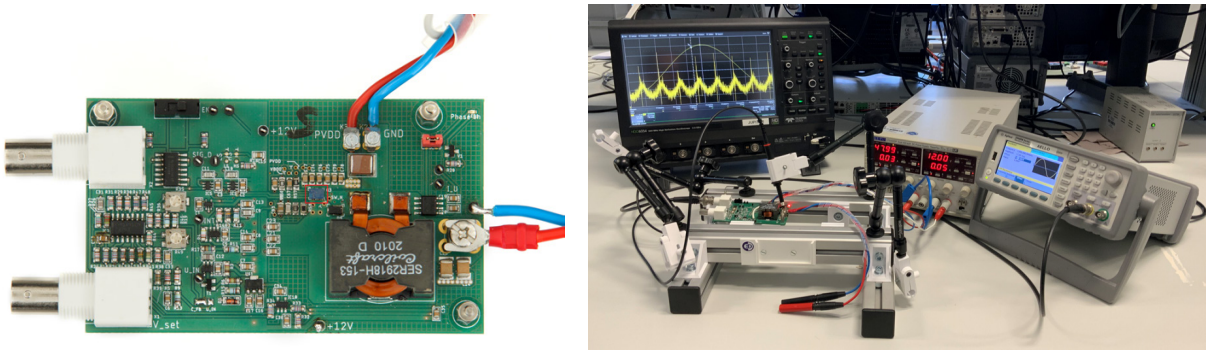


Fig. 8: Simulation results with influence of current ripple on the modulator behavior for $C_F = 680\,\text{nF}$



(a) Single phase module

(b) Laboratory measurement setup

Fig. 9: Hardware setup

Fig. 10 shows the output voltage v_O for a signal period based on $v_{O\,Ref}$ used in simulations with the parameters $L_F = 15\,\mu\text{H}$ and $C_F = 1.36\,\mu\text{F}$. Fig. 11 displays a detailed view of the measurements, marked in Fig. 10 by a red rectangle, for the parameters given in Table I. Although some deviations between simulations and measurements are observed, which can be attributed to device tolerances, the measurements support the simulation results and illustrate the theoretical discussion.

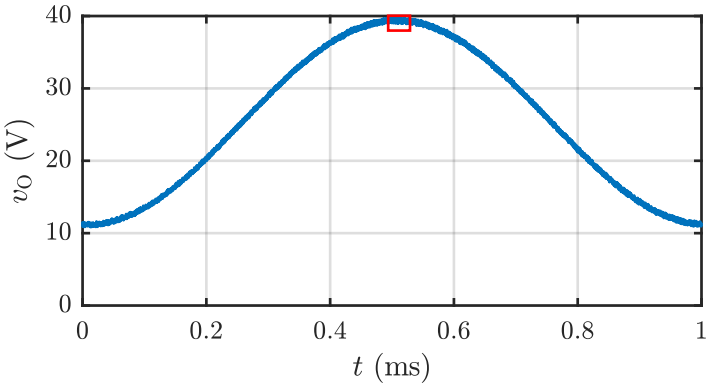


Fig. 10: Measurement result of the output voltage for one period

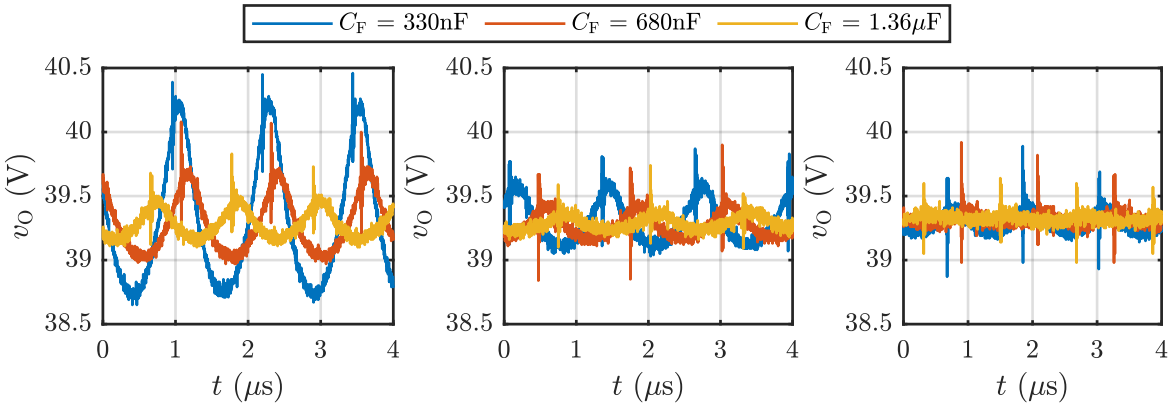


Fig. 11: Detailed view of measurement result of the output voltage with variation of L_F, C_F: Left: $L_F = 4.7\,\mu H$, middle: $L_F = 15\,\mu H$, right: $L_F = 33\,\mu H$

Conclusion

This contribution presents a new filter design approach for designing the output LC filter of a GaN based inverter such that a required dV/dt at the power electronic module is obtained with minimum filter component parameters. The design method is based on the idea, that the output filter can be considered as the output filter of a buck converter. A relation between the output filter parameters and the output voltage slew rate was developed and the effect of different filter values on the output voltage slew rate was investigated in simulations and measurements.

References

[1] Ulmer S., Walz-Lange A., Maatz A., Schullerus G., Sönmez E. and Hennig E.: Active Filter Damping for a GaN-Based Three Phase Power Stage with Continuous Output Voltage, 23rd European Conference on Power Electronics and Applications (EPE ECCE Europe), 2021

[2] Kim H., Anurag A., Acharya S. and Bhattacharya S.: Analytical Study of SiC MOSFET Based Inverter Output dv/dt Mitigation and Loss Comparison With a Passive dv/dt Filter for High Frequency Motor Drive Applications, IEEE Access, Vol. 9, 2021

[3] Vadstrup C., Wang X. and Blaabjerg F.: LC Filter Design for Wide Band Gap Device Based Adjustable Speed Drives, International Power Electronics and Application Conference and Exposition (PEAC), 2014

[4] Chen X., Xu D., Liu F. and Zhang J.: A Novel Inverter-Output Passive Filter for Reducing Both Differential- and Common-Mode dv/dt at the Motor Terminals in PWM Drive Systems, IEEE Transactions on Industrial Electronics, Vol. 54, Iss. 1, 2007

[5] Ulmer S., Schullerus G. and Sönmez E.: High Pass Design in Active Filter Damping, International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM Europe), 2022

[6] Hurley W. G. and Wölfle W. H.: Transformers and Inductors for Power Electronics. Theory, Design and Applications, Wiley, 2014