Design of a High-Dynamic Test Bench for Accelerated Dielectric Lifetime Testing with Adjustable Voltage Slopes and Temperatures

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Keywords

≪Test bench≫, ≪Insulation≫, ≪Wide bandgap≫, ≪Reliability≫, ≪Electrical Machine≫

Abstract

Upcoming future mobility will require high power densities; therefore, wide bandgap semiconductors (WBGs) and HVDC supply voltage could be one solution. One crucial design criterion is the insulation coordination in all drive train components. This paper presents and discusses a test bench design to emulate dielectric stress due to fast switching and hard switching WBGs at high voltages and various environmental conditions.

I Introduction

Future applications in electromobility will require power-dense drives that operate reliably even under changing environmental conditions. Electric cars are increasingly using fast-switching wide bandgap semiconductors and a voltage level of 800 V [1]. Drives in electrified aircraft are also exposed to specific environmental conditions like voltage levels up to 7500 V [2]. The resulting increased stress focuses attention on the electrical insulation system as the percentage of insulation faults in electric motors increases [3].

The increased voltages and specific environmental conditions also place additional stress on the power electronics. In [4] a well-used industrial-based dataset about failure mechanisms in power electronic converters is presented. Out of this dataset, printed circuit boards (PCBs) are responsible for 26 % of faults, but the dataset doesn't distinguish between sub-fault mechanisms. [5] illustrates finite element method-based (FEM) insulation coordination of a high-blocking silicon carbide (SiC) stage. Additionaly, air gaps or silicone are different design elements, but creepage distances must be understood.

More recent research has tended to focus not on the reliability of a particular part or component, but on developing a deeper understanding of the various damage mechanisms [6]. The different damage mechanisms belong to different physical disciplines and can represent both constant and transient loads. In addition, the significance of each damage mechanism varies depending on the individual load spectrum,

so reliability studies must be assigned to a specific mission profile. The combination of multiple damage mechanisms necessitates the research question about the interactions between the individual damage mechanisms. So a lot of tests has to be done. An efficient and frequently used methodology to investigate the significance of individual loads in a load spectrum is the Design of Experiments (DoE) approach [7]. Parameter studies following a mission profile require a test bench that allows dynamic and independent adjustment of the multi-physical parameters. In this paper, the development of such a test bench is presented. For this purpose, first the considered loading factors and then the concept and the setup of the first test bench version are presented. Subsequently, first test results are presented and evaluated. The resulting optimization approaches are then implemented in an improved test bench version and the measurement results are presented.
The paper is structured in four sections. An introduction contains the motivation and state of the art. Ch. II present an analysis of stress factors for PCBs, inductor windings and windings in electrical machines. Additionaly, in Ch. III and Ch. IV the paper discusses two test bench designs in detail and compares different objectives. In the first test bench concept in Ch. III, the power electronics are placed outside the warming cabinet. Since the correspondingly long cables favor transient overvoltages, the power electronics are placed inside the warming cabinet in the second test bench concept in Ch. IV. The last section concludes the presented experiences and gives a future outlook.

II Stress Factors and Methodical Implementation of the Test Bench

Various devices under test (DUT) representing both power electronics and electrical machine components will be examined in the test benches presented in Ch. III and Ch. IV. For example, twisted pair DUTs according to the IEC 60172 standard are used to represent the winding of electrical machines. For creepage distance tests on PCBs, own DUTs have been developed. Investigations at component level offer the possibility to analyze individual weak points or damage mechanisms. In addition, DUTs that represent the entire system will provide more realistic measurement results. In this chapter, the load requirements for the power electronics and the electric machine are derived for this purpose, followed by the resulting requirements for the test bench.
The test methodology is based on the destruction (breakdown) of the DUTs by adaptable stress factors and recording the lifetime. Based on a DoE, the influence of the parameters can be identified and the lifetime extrapolated. An accelerated lifetime test with increased stress factors is practicable to minimise the testing time. Finally, validation measurements prove the extrapolation of the lifetime.

A Failure Modes of PCBs and Inductor Windings

Accelerated altering of printed circuit boards can distinguish in proofing the dielectric strength of FR4 or the creepage distances between different traces. Future studies will face investigations on creepage distances under several conditions. [8] compares diverse electrode models of PCBs and illustrates the influence of several parameters, e.g. temperature, pressure, duty cycle and distances, on the breakdown voltage. Like the IEC 60 664, standards give regulation about the degree of pollution and sine wave voltage changes. The dielectric breakdown time is an important parameter. The mode of action of various aging parameters is shown in Fig 1. This illustration applies to the damage mechanisms in PCBs as well as in electrical machines and will be described in more detail in the next section.

B Failure Modes of Electrical Machines

As mentioned before, the stress on the machine side increases. By failure investigations of electrical machines in [3] it becomes clear that with increasing electrical stress the number of electrical failures in the stator winding of electrical machines with 66 % prevails over other failure phenomena such as bearing or rotor damage (13 % each). The failure mechanisms of the stator winding are shown in Fig. 1. Although materials science has developed high performance thermoplastics, temperature continues to be a dominant aging factor, first studied over 70 years ago [9]. Other dominant damage parameters added by increased electrical stress, and whose influence is being investigated in recent studies, are the voltage signal, consisting of the voltage amplitude and the voltage slope, and switching frequency [10]. It should be noted that in addition to the primary aging factors implemented in the test bench

presented, there are also mechanical aging factors. As already noted, these have a less significant effect on the failure of electrical machines in percentage terms, especially with increasing electrical loads in the future. These are shown in dashed lines in Fig. 1. The aging factors cause erosion processes that damage the insulation. Aging factors can favor several erosion processes. For example, a higher temperature indirectly favors electrical erosion processes, since the permittivities of insulating materials are temperature-dependent and therefore field strength increases occur at higher temperatures. Therefore, coupling mechanisms between aging factors and erosion processes are also of great interest. With greater damage to the insulation materials, erosion trees form and finally an electrical breakdown leads to failure of the machine winding. A detailed analysis of the above-mentioned dominant damage mechanisms from Fig. 1 was carried out in [11] on DUTs with hairpin windings.

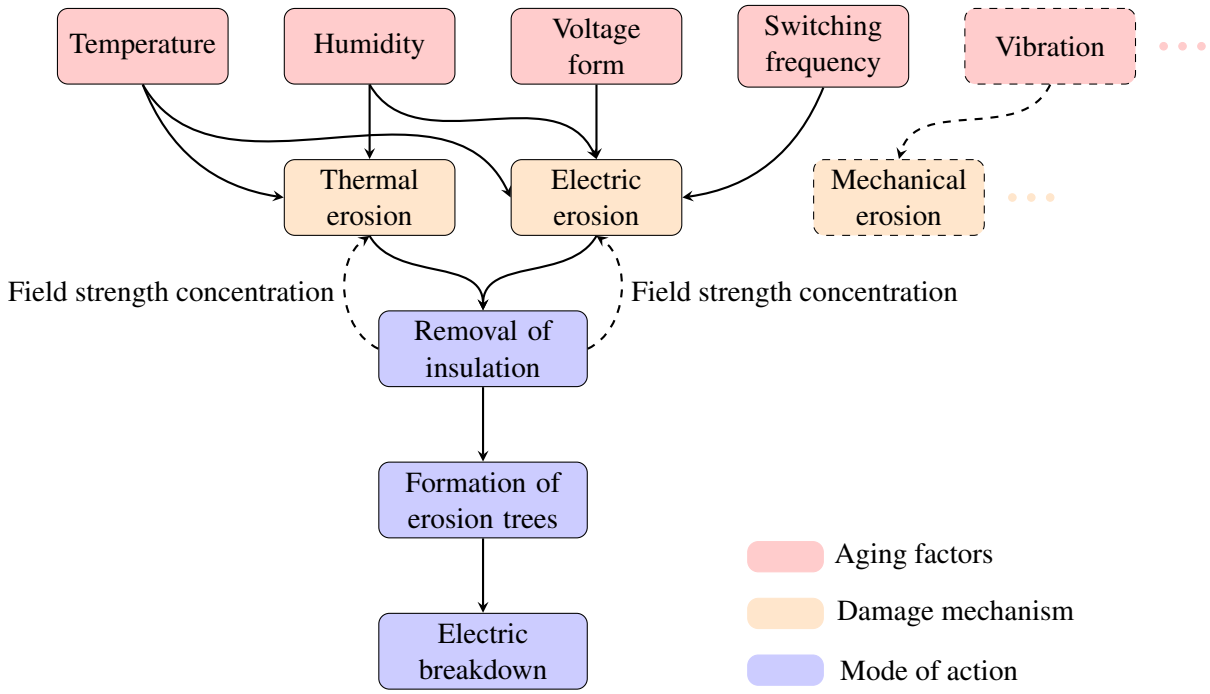

Fig. 1: Damage mechanisms and their modes of action

C Test Bench Requirements

To enable larger parameter studies, new test bench designs must provide independent adjustment of parameters such as rectangular voltage changes, voltage levels, rise- and fall times, frequencies, duty cycle, temperature, humidity and pressures. The independently controllable aging parameters of the test bench are shown in Table I. The number of parameters leads to a DoE to save time, and the test bench has to mature many DUTs at a time [7].

Table I: Independently controllable aging parameters of the test bench and their limits [* climate control]

Parameter	DC Voltage V	Voltage Slope $\frac{\text{kV}}{\mu\text{s}}$	Frequency kHz	Duty cycle %	Temperature °C	Humidity * %
Value	< 800	$< 100\,\frac{\text{kV}}{\mu\text{s}}$	< 100	$5 - 95$	-70 - 300	10 - 95

III Test Bench Version 1: Warming Cabinet

In order to achieve the high voltage slopes required for the test bench, modern semiconductors in silicon carbide technology are available, with whose short switching times the necessary voltage slopes can be impressed into the DUTs.

For the first set-up of the test bench (Fig. 2), a proven six-strand inverter [12] is used, which can be modified to generate independent voltage slopes on six channels (outside the warming chamber: left side).

All DUTs are inside the warming chamber ($T = 0..300\,°C$) and connected to each half-bridge of the six-strang inverter via an approx. 40 cm long cable. The amplitude of the voltage pulses to be applied to the DUTs is influenced by the selection of the DC link voltage (Voltage Source: above the generator), and the slope of the voltage edges can be set individually for each channel by selecting different gate resistors. Especially when testing several similar DUTs, the influence of different voltage slopes can be investigated in parallel under otherwise identical test conditions.

As long as the insulation of the DUT is intact, only the parasitic capacitance of the insulation is charged when the voltage slope is applied. Ideally, no permanent current occurs for the remaining duration of the pulse. If the pulse is subsequently switched off, this capacitance is discharged again. However, if insulation damage occurs during the test, a short-circuit current may flow through the DUT, endangering the semiconductors of the inverter and possibly causing a voltage dip in the feeding high-voltage source, so that the other channels of the test setup are also affected. In order to be able to switch off the affected channel immediately in the event of a short circuit, the output current of the channel must be monitored. Since in this case the knowledge of the absolute amplitude of the DUT current is not relevant, but only the occurrence of an overcurrent event must be detected with the shortest possible delay time, the desaturation (DESAT) detection of the gate driver for the high side switches in the pulse generator is used for this purpose. If a short circuit occurs in the DUT, it is detected by the DESAT detection and the corresponding semiconductor is immediately blocked. The overcurrent detection is thus independent of the driving controller and has a very short reaction time.

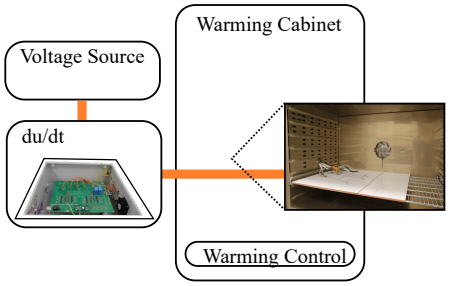

Fig. 2: du/dt test bench V1

IV Test Bench Version 2: High du/dt combined with Temperature / Humidity

For the next test bench generation, specially adapted power electronics were developed to enable higher voltage slopes. First, a prototype with a half-bridge is built to test the electrical properties (Fig. 3).

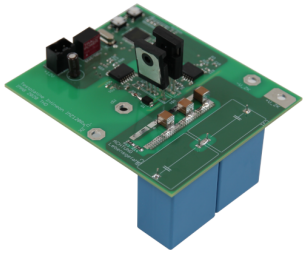

Fig. 3: Pre-study du/dt generator V2

The focus of the development is on the reduction of the commutation mesh and the use of semiconductor switches, which are primarily selected for this application under the aspect of high switching speed. Since no continuous currents have to be carried by the switches in the experimental setup, semiconductors can also be used that have a higher on-resistance, but in return have a high switching frequency. For the test carrier shown, SiC MOSFETs from Infinion's IMZ120R series in the TO-247 package are used, within which different current-carrying capacities and channel resistances are available. To optimise the PCB layout, the high and low side switches are arranged face-to-face, which increases the design effort for cooling, but allows a reduction of the conductor path meshes on the PCB. After initial tests with this setup have been successful, the circuit is expanded for use in the test stand and equipped with the necessary peripherals.

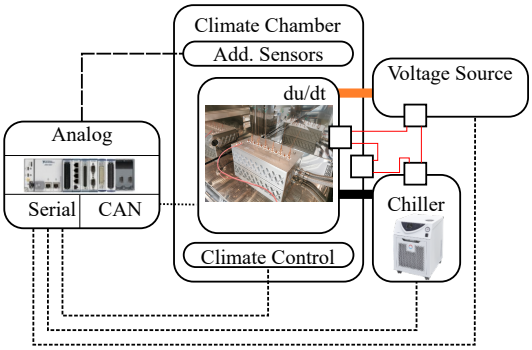

Fig. 4: du/dt test bench V2

The mentioned requirements demand climate adjust-

ing, voltage and high voltage changings. Additionally, the DoE requires a decoupling of different parameters, such as du/dt and the voltage. Due to the understanding of test bench version 1, small impedances between DUT and generator are needed to ensure the decoupling between parameters. The cable impedance leads to high voltage changes due to mismatch, so decoupling of parameters and gate resistance adjusting are difficult. Therefore, small impedances between the generator and DUT can solve these problems and pre-study archives high voltage changing by good blocking characteristics.
Fig. 4 illustrates the test bench design. The new design demands a water-cooled generator inside the climate chamber with low cable impedances. A real-time embedded industrial controller (Ni cRIO, left side) enables the overall test bench control and capture metadata (time, temperature, humidity, voltage, semiconductor temperature, etc.). A voltage source supplies the six-strand inverter in the climate cabinet.

A Electrical Design

Version 2 (Fig. 5 a)) is fitted with six clamping opportunities based on six SiC half-bridges to conduct a DoE, and it is included in a cooler. The DUTs can be clamped to the test bench on the shortest possible path, and the DUTs has to face environmental conditions (humidity and temperature). Inside the housing, SiC half-bridge fed by drivers enables the high required switching speeds. The driver design and the semiconductors are designed in the pre-study (one half-bridge configuration, Fig. 3). Version 2 has slight differences in the electrical design to the pre-study; the sigma-delta modulator captures the DC bus voltage, the used isolated driver measures the semiconductor temperature, and other DC capacitors enable various capacitive loads. Additional functionalities are a Controller Area Network (CAN) interface, multiple isolated in- and outputs, an input for the emergency loop and a potential-free switch.
A field-programmable gate array (FPGA, type: Intel Max 10) enables the highest flexibility and guarantees the calculation of the pulse-width modulation (PWM), duty cycle, bus voltage evaluation, semiconductor temperature verification, high precision timer, self-designed CAN interface, and safety functionalities. All functionalities are implemented, such as the PWM calculation, duty cycle comparison, the DESAT-triggered timers, semiconductor PWM-based thermal measurements, sigma-delta filter for DC Voltage, the safe handling and the CAN interface.

a) b) c)

Fig. 5: du/dt generator V2 [a) commissioned electronic b) heat sink design c) assembled generator]

B Thermal Design

The thermal and mechanical design is crucial because the construction has to protect the electronic devices from harsh environmental conditions and cool SiC semiconductors down. The targeted environmental condition is 150 °C, and the design of the cooler is very challenging. Also, the housing design limits the switching frequency (a stress factor). The critical electronic elements, such as the power electronic semiconductors and the capacitors, are thermally connected to the coolant. A meandering cooling channel directs the fluid to the appropriate places, illustrated in the Fig. 5 b). The liquid is accelerated and decelerated at the corresponding points using various tightening and loosening points. Furthermore, so-called feed-through channels supply cool liquid to the last half-bridges. The chiller offers a cooling power of around 1200 W. A verification of the cooler design is done by a Computer Fluid Design (CFD) study. All electrical power connections are led out through a polytetrafluoroethylene (PTFE) insulator

so that the temperature is limited to 200 °C. At 200 °C, dangerous vapours occur due to fluorinated compounds. A small D-SUB 15 aerospace connector enables the electronic power supply and communication.
Tab. II shows the thermal design verification with a switching frequency of 50 kHz, 600 V DC voltage link and twisted pair wires. Two additional 1 kΩ platinum resistor (PT1000) sensors are implemented in the housing to capture air temperature inside the housing $T_{a,HS}$. The double-walled heat sink possesses a good thermal decoupling to the climate chamber temperature T_a; this is observable by the two PT1000 sensors. The average temperature of all 12 negative temperature coefficient (NTC) sensors $\overline{T_{NTC1..12}}$ (NTCs connected to source potential) illustrates a linear increase over the climate chamber temperature. Two sensors are a little bit warmer (approx. 29 °C at $T_a = 150$ °C); therefore, the thermal interface could be checked or improved. The highest measured temperature of the 12 NTCs ($\mathrm{Max}(T_{NTC1..12})$) is 107 °C under the maximal junction temperature of 175 °C, and the air temperature inside the housing reaches only < 50 °C. Also, the chiller can cool the system with its cooling power of 1200 W. For environmental-friendly long-term studies, thermal insulation with stone wool panels is feasible and can increase the thermal design point to higher temperatures to < 200 °C. Moreover, the thermal design enables also an increase in the switching frequency (a stress factor).

Table II: Temperature verification [T_a : ambient climate chamber temperature, T_c: coolant inlet temperature, $T_{a,HS}$: ambient temperature in the heat sink, $T_{NTC1..12}$: NTC measuring points of the 12 semiconductors]

T_a °C	T_c °C	$T_{a,HS,1}$ °C	$T_{a,HS,1}$ °C	$\mathrm{Max}(T_{NTC1..12})$ °C	$\overline{T_{NTC1..12}}$ °C
25	20	26.8	26.8	55	45.5
50	20	29.9	31.2	60	49.25
75	20	33.7	35.3	70	56.3
100	20	37.4	39.5	75	61.3
125	20	41	43.5	92	69.6
150	20	45.5	48.4	107	78.3

C Verification of the Switching Behaviour

The Fig. 6 shows the measured voltage change by a 400 MHz single-ended passive voltage probe. The left graph illustrates voltages changes defined by an inductive load. Due to the help of a double pulse test, different voltage changing velocities are captured under various gate and voltage settings. The in-

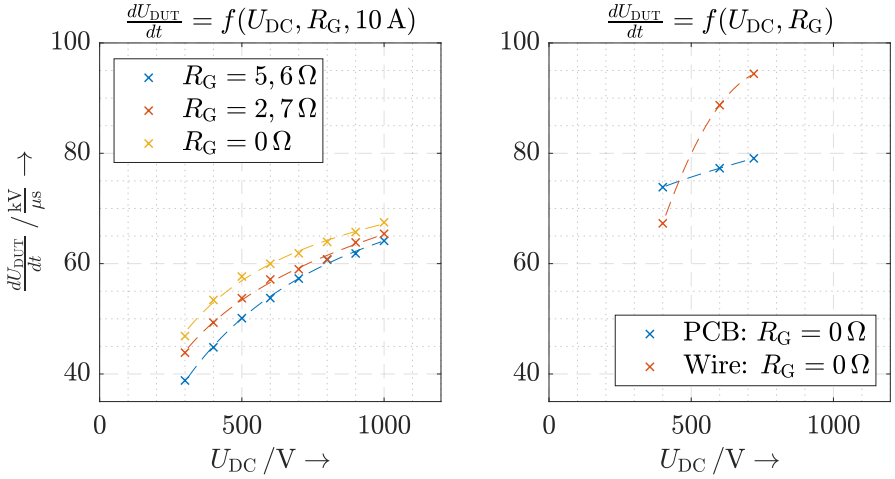

Fig. 6: Verification of the voltage slope of test bench V2 [PCB: electrode distance 500 μm]

ductive load and the various first puls length enable a comparable current level. Moreover, the double pulse test ensures the verification of the DESAT functionality. A Zener diode can easily adjust the drain threshold current to various capacitive loads. In addition, the right graph in Fig. 6 illustrates the changing speeds from two different DUTs. It can be recognized that the wire-based DUT has much higher voltage changes $\frac{dU_{\mathrm{DUT,max}}}{dt} = 95\,\frac{\mathrm{kV}}{\mu\mathrm{s}}$ compared to the PCB-based DUT $\frac{dU_{\mathrm{DUT,max}}}{dt} = 79\,\frac{\mathrm{kV}}{\mu\mathrm{s}}$. Nevertheless, it also has a higher overshoot, which is due to the changed impedance.

V Comparison of Test Bench Versions

In order to compare the two test benches, the voltage load was investigated on a twisted pair wire, which is often used to evaluate the conductor insulation of electrical machines. Fig. 7 shows the slopes of the voltage signals on the DUT at an DC link voltage of 700 V. It can be seen that the transient overvoltage U_σ at the test specimen could be massively reduced by the second test bench version. In the first test bench version, a transient overvoltage of 609 V was measured and the DUT was loaded with a maximum total voltage of 1,309 V. This shows that under unfavorable boundary conditions and long cables between the power electronics and the electrical machine, the maximum voltage load at the machine terminals can be 1.87 times the DC link voltage. Through further development of the test bench, the transient overshoot at 700 V DC link voltage could be reduced to only 139 V in the second test bench version, thus reducing the maximum total load by almost 36 %. at 700 V DC link voltage of the two test bench versions V1 and V2 on a twisted pair DUT.

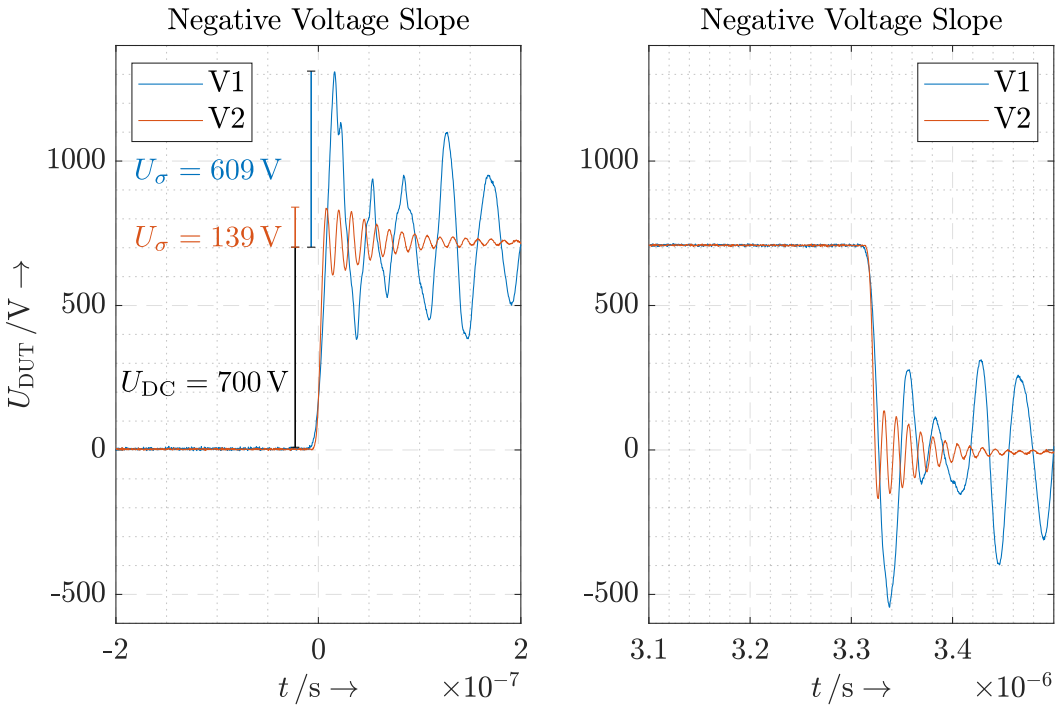

Fig. 7: Comparison of the voltage signals [$R_{\mathrm{G}} = 0\,\Omega$]

Fig. 8 shows the values for transient overvoltages U_σ and voltage slopes $\frac{dU_{\mathrm{DUT}}}{dt}$ at different DC link voltages. The results from Fig. 7 are confirmed, namely that the voltage load could be significantly reduced regardless of the DC link voltage. At the same time, it can be seen in the figure on the right that the voltage slope could be increased. The voltage slope up to the DC link voltage and up to the transient overvoltage are indicated in each case. It is noticeable that the voltage slope seems to saturate at higher DC link voltages. Reducing the voltage load by lowering transient overvoltages has a significant influence on the lifetime of the winding of electrical machines. To confirm this, lifetime measurements were performed with the twisted pair DUTs that were also used for the voltage measurements in Fig. 7

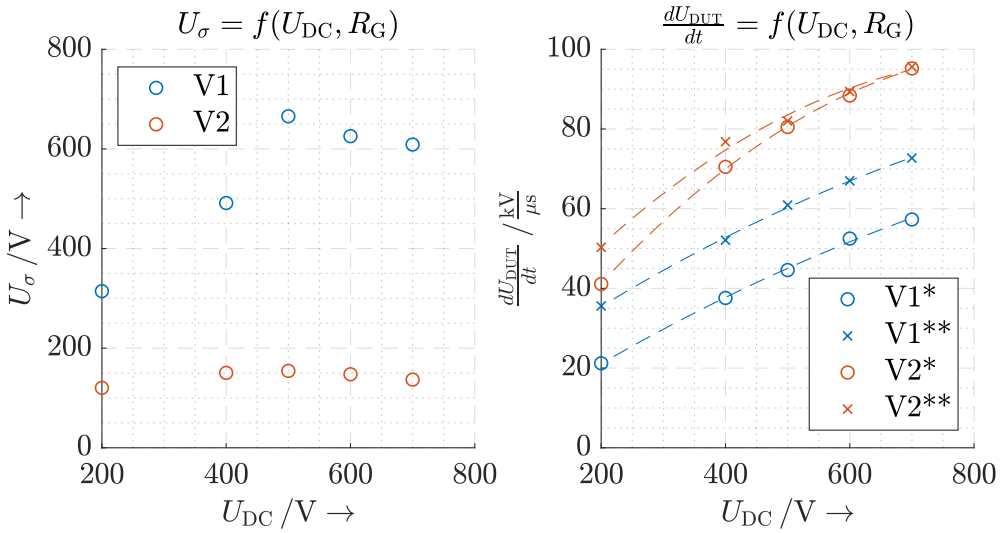

Fig. 8: Comparison of transient overvoltages U_σ and voltage slopes $\frac{dU_{\mathrm{DUT}}}{dt}$ for the two test bench versions [$R_{\mathrm{G}} = 0\,\Omega$, * $10/90\,\%U_{\mathrm{DC}}$, **$10/90\,\%(U_{\mathrm{DC}} + U_\sigma)$]

and Fig. 8. The DUTs were loaded with a DC link voltage of 600 V at a frequency of 30 kHz. In order to investigate the electrical stress individually, environmental conditions such as temperature and humidity were not taken into account. In order to be able to make a statistically significant statement, nine DUTs were subjected to the lifetime measurements. The end of life of the DUTs is reached when the DESAT detection registers a breakdown between the wires and switches off the phase.
Fig. 9 shows the results of the lifetime measurements and how the failure probability of the sample can be described by means of a Weibull distribution function. The Weibull distribution function gives the

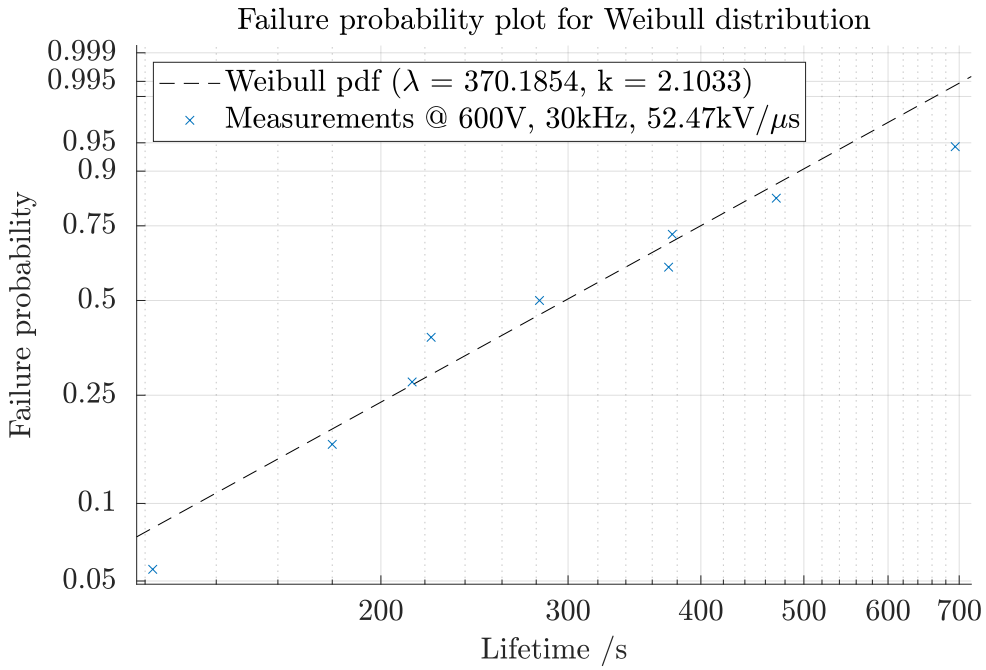

Fig. 9: Lifetime measurements and statistical fit by Weibull distribution function for test bench version V1 (Mean= 327.87s; Standard deviation = 168.8s)

failure probability F as a function of the lifetime L with the scale λ and shape k parameter according to equation (1):

$$F(L) = 1 - \mathrm{e}^{-\left(\frac{L}{\lambda}\right)^{k}} \tag{1}$$

On average, the nine test specimens failed after 327 s. The variation in the measurement results was quite high with a standard deviation of 168.8 s. In contrast, no failure was detected in the second test bench version after 15 h of ageing at 600 V DC link voltage. Since the voltage slope of the second test bench version is even higher than that of the first version, it can be concluded that it is not the voltage slope but the transient overvoltage that significantly damages the insulation and leads to an electrical breakdown.

VI Conclusion

This paper discusses the design of a high dynamic rectangular du/dt generator to stress dielectrics in electrical machines and power electronic devices. A requirement-oriented design study is represented. The first version (Fig. 2) and a pre-study (Fig. 3) have gained a lot of experience. These experiences have influenced the design of V2. A water-cooled du/dt generator within the climate chamber is proposed, and all preparations for metadata analysis are implemented. The measurement results show that the transfer to the climatic chamber and the short cables were able to massively reduce the transient overvoltages. At the same time, higher voltage slopes were achieved with the new design (V2). Furthermore, lifetime measurements could show that the transient overvoltage strongly stresses the insulation and has a more significant influence on the lifetime of the winding of electrical machines than the voltage slope.

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