Design Space Exploration for a Capacitive 36V, 4A, 4:1 DCDC Converter with GaN Switches Using a Performance-Cost-Matrix Including Uncommon Topologies

Adrian Gehl, Malte Kempchen, Simon Disselkamp, Markus Olbrich, Bernhard Wicht
LEIBNIZ UNIVERSITÄT HANNOVER, INSTITUTE OF MICROELECTRONIC SYSTEMS
Appelstr. 4
30167 Hannover, Germany
Phone: +49 / (511) – 762 19670
Fax: +49 / (511) – 762 19694
Email: adrian.gehl@ims.uni-hannover.de
URL: https://www.ims.uni-hannover.de

Keywords

≪DC-DC converter≫, ≪Switched capacitor≫, ≪Wide bandgap≫, ≪Modelling≫, ≪Design optimization≫

Abstract

A systematic approach to compare capacitive DCDC converters regarding performance and cost is presented. All possible topologies for a 4:1 voltage conversion ratio are generated using an algorithm developed in this research. Selected topologies are implemented benefiting from GaN transistors. Experimental results over various operating conditions up to 36 V input, 4 A load and 2 MHz switching frequency confirm theory and simulation. Two uncommon topologies demonstrate superior cost and load performance. The parameter space supports various industrial and automotive applications.

Introduction

Capacitive or switched-capacitor (SC) DCDC converters have become a common solution for small and medium power applications due to their high power density at large voltage conversion ratios [1]. Compared to traditional inductive DCDC converters they can omit a bulky inductor. SC DCDC implementations found in the literature usually rely on a few well-known topologies, such as the Series-Parallel, Dickson, Fibonacci or Ladder topology [2, 3]. However, especially for larger voltage conversion ratios, which require multiple flying capacitors [4], there exist uncommon topologies that have not been investigated in prior art. Therefore, a systematic approach to compare the performance of all possible SC DCDC topologies for a given voltage conversion ratio (VCR) is required. In a second step, a cost metric for the actual implementation of the SC DCDC converters can be derived, yielding a performance-cost-matrix from which a certain topology for a specific use case can be selected. Good understanding of performance and cost/complexity trade-offs in fixed-ratio topologies is crucial when designing multi-VCR SC DCDC converters [5].

This paper is organized as follows: First, constraints for the SC DCDC topologies are chosen, so that a practical comparison is possible with reasonable effort. To achieve this comparison on a PCB level a universal hardware platform is introduced, using the same components for each SC DCDC topology. This hardware platform also allows for a comparable cost metric. Simulations allow to derive a performance figure-of-merit (FOM) for each topology. Based on a cost-performance matrix, six different topologies are chosen to be implemented on PCB level. Measurements finally validate the simulation results.

Topology Synthesis

To achieve a voltage conversion, the flying capacitors in the power stage of a SC DCDC converter are re-arranged in two or more switching phases. As an example, the implemented 4:1 topologies are shown in Fig. 1.

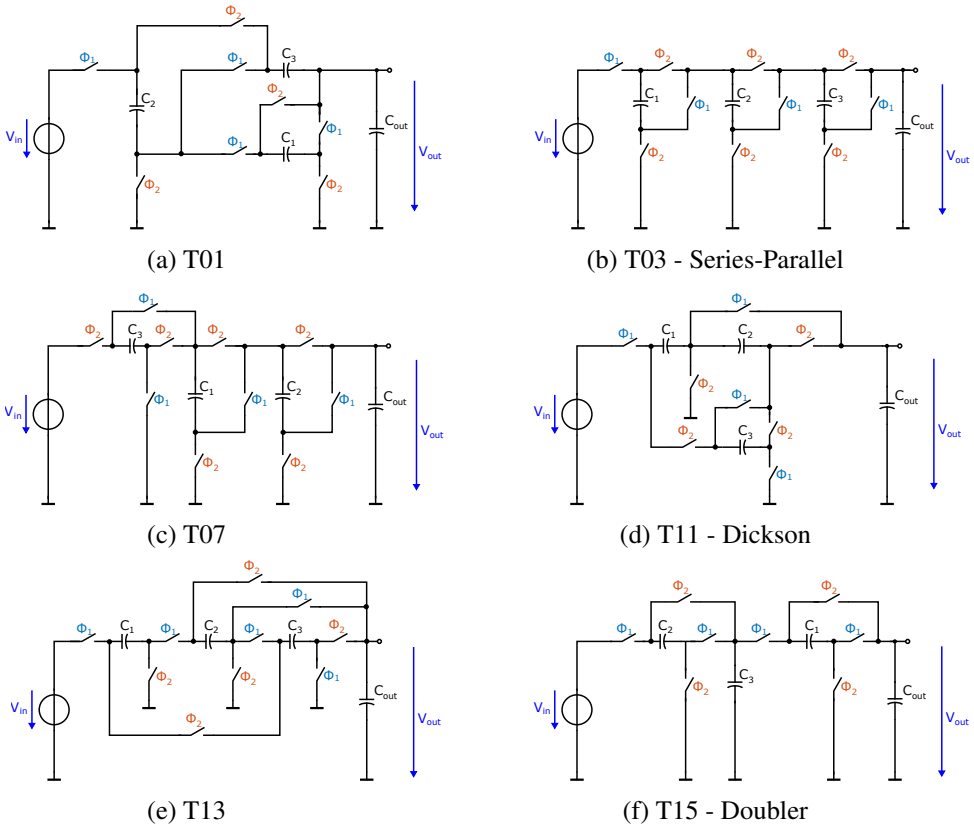


Fig. 1: Implemented SC DCDC converter topologies

To realize a desired VCR, a certain minimum number of flying capacitors and switching phases is required [6]. However, with increasing number of flying capacitors and switching phases, the possibilities to achieve the desired VCR also grow significantly. Hence, it must be ensured to generate all possible topologies for given VCR, flying capacitor and switching phase constraints to enable a comprehensive comparison of the different implementations. A software algorithm based on the charge flow analysis introduced in [1] is developed as part of this research. The algorithm computes all possible SC DCDC architectures under given constraints and checks for realizability by applying Kirchhoff's laws. For the topology analysis, in this work a VCR of 4:1 is chosen. The number of flying capacitors and switching phases is set to three and two, respectively. These constraints give a total of 15 realizable SC DCDC architectures which include the well-known series-parallel, Dickson and cascaded / doubler implementations (Fig. 1).

PCB implementation

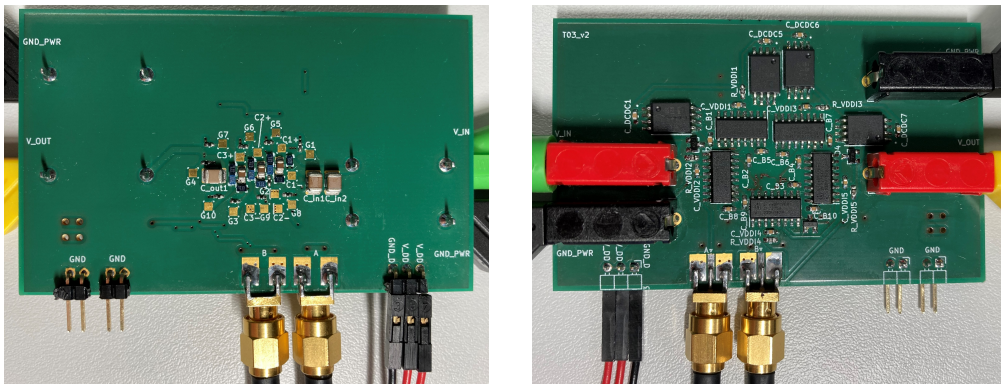
To perform a fair comparison the synthesized topologies are implemented using the same hardware components as shown in Table I. For the power switches EPC2014C GaN-FETs with a rated V_{DS} of 40 V are chosen while the flying capacitors are standard SMD ceramic types. Due to their low C_{OSS} GaN-FETs enable high switching frequencies resulting in low output resistance. This way, high efficiency can be achieved at load currents up to 4 A. The power switches are driven by isolated gate drivers (Infineon 2EDF7275F) since their source potentials can float. Because of the partially floating source potential, the gate drive supplies in a SC DCDC are of particular interest. For the drivers which cannot

be supplied by bootstrapping or directly from the low-side supply, isolated DCDC converters (Analog Devices ADuM5028) are used.

Table I: Selected Components for PCB implementation

Component	Name
Power switches	EPC 2014C
Flying capacitors	1uF 50V MLCC
Isolated gate drivers	Infineon 2EDF7275F
Isolated DCDC converters	Analog Devices ADuM5028

An example PCB implementation is shown in Fig. 2. The gate drivers and power switches are placed on the opposite sides of the PCB to keep the gate loops short which is crucial for GaN-FETs. In addition, this enables a compact powerstage layout to decrease PCB parasitics.



(a) Powerstage with GaN-FETs and flying capacitors

(b) Gate drivers and gate drive supply

Fig. 2: SC DCDC PCB implementation

Performance and Cost Considerations, Methodology, FOM Development

The common SC DCDC converter model in Fig. 3 consists of an ideal transformer with the VCR of the topology and the output resistance R_{out} which models the intrinsic losses in the powerstage.

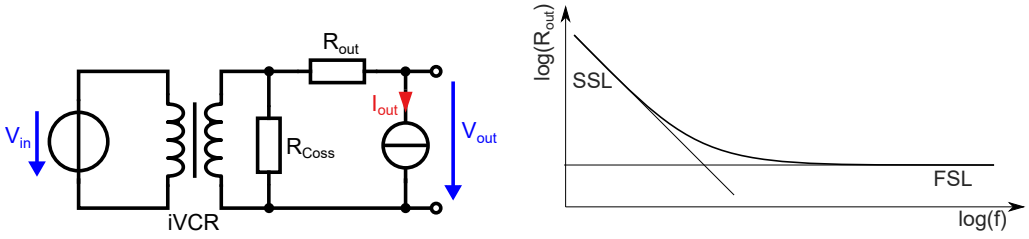


Fig. 3: SC DCDC converter model

The output resistance depends on the switching frequency and can be calculated according to eq. (1).

$$R_{\text{out}} = (V_{\text{in}} \cdot iVCR - V_{\text{out}})/I_{\text{out}} \tag{1}$$

At lower frequencies (Slow Switching Limit, SSL) the charge redistribution losses of the flying capacitors dominate. At higher frequencies the voltage swing across the flying capacitors becomes neglectable and the output resistance approaches the fast-switching limit (FSL) which is determined by the equivalent DC resistance of the powerstage. This FSL resistance also sets the maximum load current for given input

and output voltages. The resistance R_{Coss} models the charging losses in the output capacitances of the power switches. In order to accurately model the efficiency of each topology, other loss mechanisms must be taken into account. Fig. 4 shows a breakdown of the different losses for topology T01 in (see Fig. 1a).

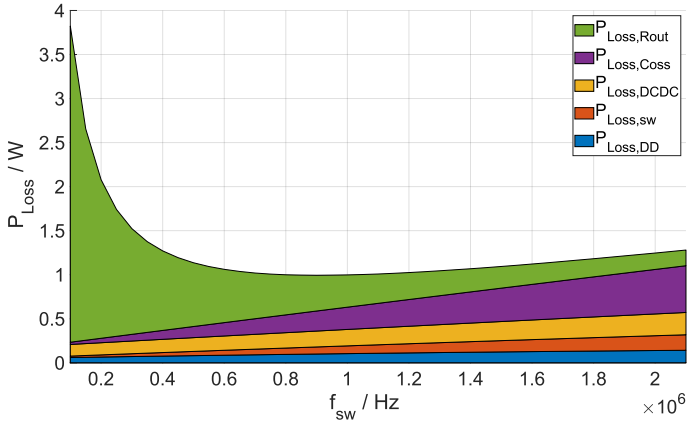


Fig. 4: Losses in SC DCDC Topology T01

At low switching frequencies, the R_{out} losses are dominant while at higher switching frequencies all frequencies dependent losses increase. $P_{\mathrm{Loss,Coss}}$ are the losses during charging / discharging of the power switch output capacitances which are not negligible especially at higher input voltages. For accurate modeling, the voltage dependence of C_{OSS} must be taken into account: For the 4:1 SC DCDC topologies, the drain-source voltage of the power switches varies between $1/4 \cdot V_{\mathrm{in}}$ and $3/4 \cdot V_{\mathrm{in}}$, which corresponds to a C_{OSS} of 130 pF to 180 pF for the EPC2014 GaN-FETs. $P_{\mathrm{Loss,DCDC}}$ accounts for the losses in the isolated DCDC converters, these are mainly topology dependent since the topologies require different numbers of isolated gate drive supplies. $P_{\mathrm{Loss,sw}}$ and $P_{\mathrm{Loss,DD}}$ indicate the gate charge losses of the power transistors and the low-side logic supply, respectively. From these losses the efficiency plots as shown in Fig. 5 can be derived.

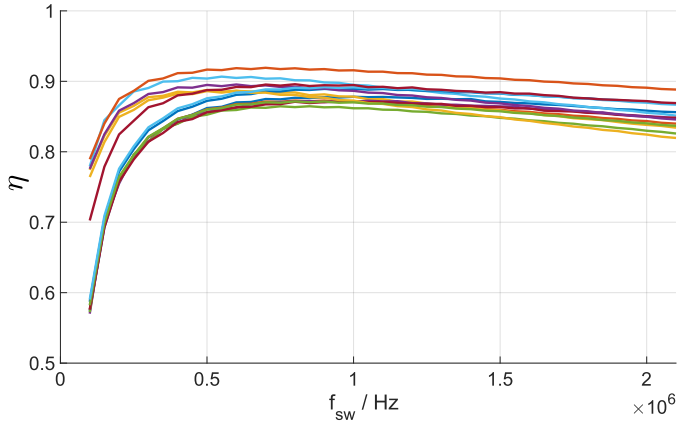


Fig. 5: Simulated efficiencies for all 15 topologies, $V_{\mathrm{in}} = 36\,\mathrm{V}$, $I_{\mathrm{load}} = 1\,\mathrm{A}$

Moreover, a performance figure-of-merit (FOM) can be introduced according to eq. (2)

$$\mathrm{FOM} = \max(\eta)/\min(R_{\mathrm{out}}) \tag{2}$$

with its maximum indicating the best performance. The FOM includes load current capability represented by the minimum Rout and the plain maximum efficiency. To obtain the SC DCDC topologies which are beneficial for actual implementation the gate drive complexity / cost must also be considered. Some topologies need more power switches or more isolated DCDC converters for gate drive supply and have therefore a larger bill of material. A power switch which is directly supplied by the low-side

supply has significantly lower cost than a floating power switch that is supplied by an isolated DCDC converter. The cost considerations also apply directly for an integrated SC DCDC powerstage where cost is determined by silicon area. Here, the main area contributors are usually capacitors, so a topology which requires fewer floating voltage domains is beneficial since a floating voltage domain requires either bootstrapping or a dedicated charge pump.

Using the accumulated component costs, each SC DCDC topology can be entered into the cost-performance matrix as shown in Fig. 6 where the best topology would be located top left.

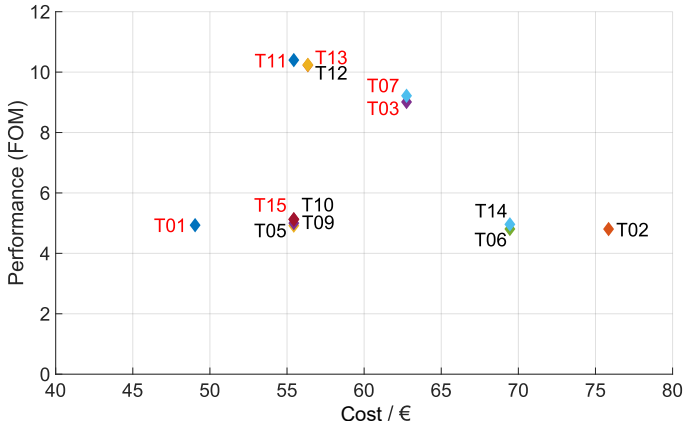


Fig. 6: Cost-Performance-Matrix of the 4:1 SC DCDC topologies (implemented topologies marked in red)

Experimental Results

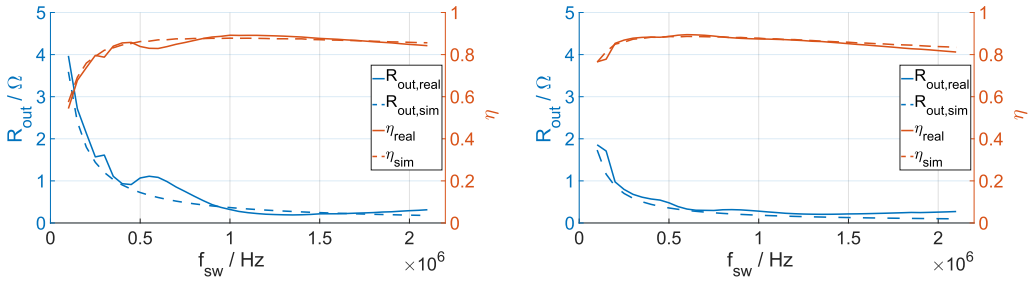
From the complete set of 15 topologies, six were chosen to be implemented on a PCB (see schematics in Fig. 1, also marked in red in Fig. 6). These include the Series-Parallel (T03), Dickson (T11) and Cascaded / Doubler (T15) architecture as well as the three uncommon topologies T01, T07 and T13.

Fig. 7 shows the measured vs. simulated output resistances and efficiencies exemplarily for all implemented topologies. The deviation between simulation and measurement at low switching frequencies, especially for T11-Dickson, is caused by the non-linear flying capacitors where the actual capacitance changes significantly with the capacitor voltage. This is a concern at low switching frequency since the voltage swing over the flying caps at SSL is large (Fig. 8). In addition, T11-Dickson has larger steady-state voltages across the flying capacitors as compared to T01. The occurrence of resonances can be observed caused by parasitic inductances mainly from PCB traces, which is not included in the simulation model. Figure 9 shows the efficiency of each topology vs. load.

The measurements confirm the cost-performance matrix of Fig. 6. T01, T11-Dickson and T13 build the pareto front of all topologies. T01 has mediocre performance while by far the lowest cost. T11-Dickson has a slight performance advantage over T13, mainly due to its higher peak efficiency, while T13 has lower minimum R_{out}. This behavior is also confirmed by an efficiency measurement with fixed input and output voltages (Fig. 9) where T13 and T11-Dickson can provide significantly more load current of more than 4.1 A than the other topologies and also show the highest peak efficiencies.

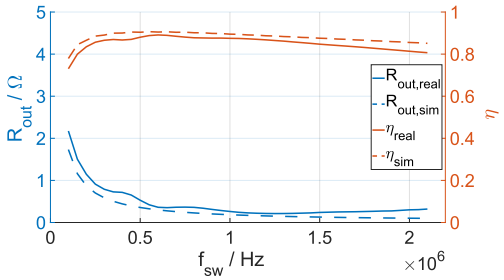
Table II: Comparison between selected SC DCDC topologies

	T01	T11 - Dickson	T13
Peak efficiency	○	++	+
Max. load current	○	+	++
Cost	++	○	−
Max. C_{fly} voltage	$0.5 \cdot V_{\text{in}}$	$0.75 \cdot V_{\text{in}}$	$0.5 \cdot V_{\text{in}}$
Max. switch voltage	$0.5 \cdot V_{\text{in}}$	$0.5 \cdot V_{\text{in}}$	$0.75 \cdot V_{\text{in}}$

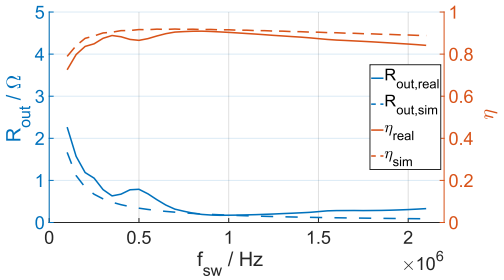


(a) T01

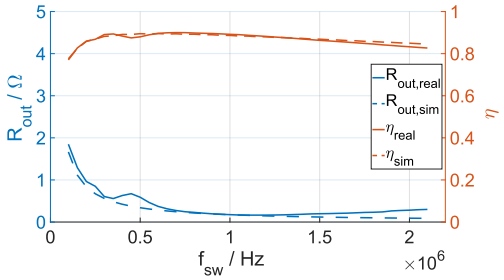
(b) T03 - Series-Parallel



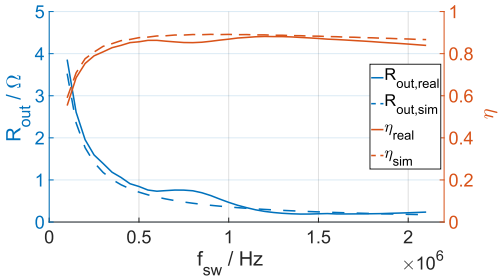
(c) T07



(d) T11 - Dickson



(e) T13



(f) T15 - Doubler

Fig. 7: Simulated vs. measured output resistances and efficiencies

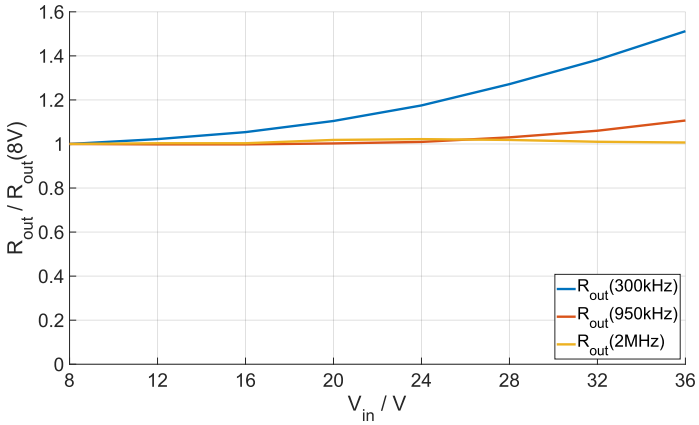


Fig. 8: Output resistance of T11-Dickson vs. input voltage for different switching frequencies

Table II summarizes the results for T01, T11-Dickson and T13 and includes the maximum voltage ratings for flying capacitors and power switches which is an important information for a final DCDC converter design since it determines the maximum input voltage for a given set of components. For an integrated solution, the limits are set by the semiconductor technology, so the topology selection becomes even more important.

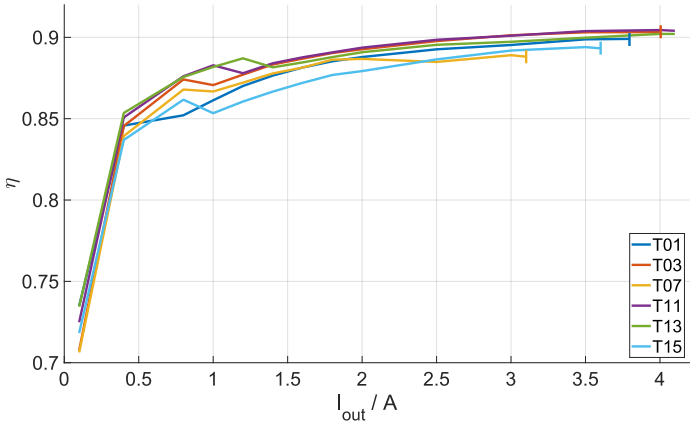


Fig. 9: Efficiencies vs. load current for $V_{\text{in}} = 36\,\text{V}$, $V_{\text{out}} = 8.3\,\text{V}$

Conclusion

This work presents a comprehensive analysis of 4:1 SC DCDC converter topologies with three flying capacitors and GaN power switches. These topologies include not only the well-known Dickson, Series-Parallel and Doubler / Cascaded architectures, but also all other possible topologies for the given constraints are generated using a self-developed software algorithm. The cost-performance matrix shows that the Dickson topology has benefits in terms of efficiency at reasonable implementation costs. However, also uncommon topologies turn out to be attractive. The topology T013 has an advantage due to its minimal output resistance but also requires a slightly more expensive gate drive supply. For applications which do not have the highest performance demands the topology T01 could also be of interest, since it has significantly lower implementation cost. The measurement results are in line with the simulations, also showing practical limitations of the different topologies, such as different maximum voltage ratings of the power switches and flying capacitors.

The presented methodology can be easily adapted for other voltage conversion ratios and more flying capacitors which might lead to even more uncommon SC DCDC architectures since the parameter space grows rapidly with increasing number of flying capacitors and larger voltage conversion ratios.

References

[1] M. D. Seeman and S. R. Sanders, "Analysis and Optimization of Switched-Capacitor DC–DC Converters," IEEE Trans. Power Electron., vol. 23, no. 2, pp. 841–851, 2008, doi: 10.1109/TPEL.2007.915182.

[2] J. Liu and S. Gregori, "Switched-Capacitor Boost-Buck Ladder Converters With Extended Voltage Range in Standard CMOS," IEEE Trans. Circuits Syst. I, vol. 67, no. 12, pp. 4593–4606, 2020, doi: 10.1109/TCSI.2020.3028268.

[3] D. Gunasekaran and F. Z. Peng, "Design of GaN based ultra-high efficiency, high power density resonant Dickson converter for high voltage step-down ratio," in ECCE 2019: IEEE Energy Conversion Congress & Expo : Baltimore, MD, Sept. 29-Oct. 3, Baltimore, MD, USA, 2019, pp. 845–852.

[4] M. S. Makowski and D. Maksimovic, "Performance limits of switched-capacitor DC-DC converters," in Proceedings of PESC '95 - Power Electronics Specialist Conference, Atlanta, GA, USA, Jun. 1995, pp. 1215–1221.

[5] D. Lutz, P. Renz, and B. Wicht, "12.4 A 10mW fully integrated 2-to-13V-input buck-boost SC converter with 81.5% peak efficiency," in 2016 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, Jan. 2016 - Feb. 2016, pp. 224–225.

[6] M. S. Makowski, "Realizability Conditions And Bounds On Synthesis Of Switched-capacitor DC-DC Voltage Multiplier Circuits," IEEE Trans. Circuits Syst. I, vol. 44, no. 8, 1997.