SiC Power Module and PCS for Commercial ESS

Xuancai Zhu[1], Tao Wang[2], Xiaoyu Jia[1], Bin Qi[1], Zhi Yang[1], Yuming Zhang[1]
[1] Wanbang Digital Energy Co. Ltd., China
[2] Suzhou Sizhi Technology Co., Ltd., China

***Abstract*-- Energy storage system (ESS) is a particularly important technology that can help electricity grids to integrate renewable and intermittent energy sources and ensure reliable electricity supply. Safety and cost are the major concern of ESS right now. In this paper, the leverage cost of energy (LCOE) of ESS will be detail analyzed especially the efficiency related coefficient. The target here is to design an ESS with round trip efficiency higher than 90 % with 0.5P. To improve the efficiency and reduce the LCOE of commercial ESS, a SiC based design is introduced and realized. The detail module design and efficiency test are compared based on Si design and SiC based design.**

***Index Terms*-- PCS, ESS, SiC MOSFET, T-type three-level inverter, high efficiency.**

I. Introduction

ESS is viewed as a game-changing technology that can bring multiple benefits to the power system and consumers [1]-[3]. Right now, the major concern of ESS is safety and cost. Currently, most of the ESS application is project based, the battery pack, power conversion system (PCS) and other components are shipped to destination separately and the final assembly and commission is on the final destination. The safety concern and cost are different with different location. The field assembly, testing the commission always brings high additional cost of the whole system. It may also bring quality and safety concerns.

To solve these concerns, we, Star Charge has raised a new proposal to define the standard product of ESS for commercial and industrial application. To reduce the cost and assembly effect, the new PCS is defined to fulfil safety standard. To improve the efficiency of whole system, a new SiC based power module is defined, developed and implanted.

In this paper, the leverage cost of energy (LCOE) of energy storage system (ESS) here is defined and analyzed. The PCS function definition has made to integrated most of the function inside the ESS cabinet. The SiC based power module is analyzed and several layout has been compared. The efficiency result is compared and with final ESS design.

II. LCOE Of The ESS

Considering only the energy consumption by the ESS as cost, the energy stored and export to the grid or load will get paid, the leverage cost of energy of ESS can be defined as below.

$$LCOE = \frac{\text{total cost over life time}}{\text{total energy output}} = \frac{\sum \frac{(I_t + M_t + F_t)}{(1+r)^t}}{\sum E_t}$$

where, I_t is the initial investment, M_t is the maintenance cost, F_t is the fuel (wasted electricity) cost, E_t is the energy output over time, and r is the cash rate.

E_t and F_t are expressed as follows.

$$\sum E_t = \sum \left(1 - \frac{D \times N_y}{N} \times t\right) \times S_t$$

$$F_t = p_t(1-\eta)E_t$$

where, D is the change of end-up SOH, normally 20 % or 30 %, N_y is the average yearly cycles, N is the cycle life, S_t is the battery pack initial capacity (kWh), p_t is the price of energy, and η is the round trip efficiency, from 85 % to 92 % for Li-ion ESS.

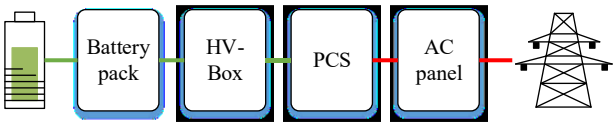
From these equations, we can find that cycle life is the key of energy output, increase of cycle life N will increase the energy output significantly.

Besides, the round trip efficiency is key of fuel cost, as E_t over life time is a big number, increase of η will brings reduction of total cost of life obviously.

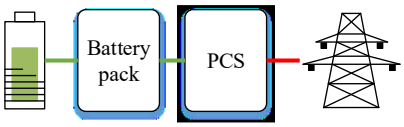
Except the losses of battery cell itself, which has few difference from different vendor but major related on battery chemistry. Among the losses inside ESS, the major portion will be the energy loss inside battery cell, which is related to the temperature and also C rate (or P rate), the conversion loss of power conversion system (PCS), heating ventilation and air conditioning (HVAC) system and others.

III. System Architecture

In conventional design, the main powertrain of ESS including the battery pack, HV-Box, with BMS inside, PCS and AC panel, which is shown in Fig. 1 (a). Inside each one, there are a lot of protection or operational devices such as fuses, breakers and several inter-connection copper bars or cables, and several of the components may also duplicated in different palaces. To improve the efficiency, first of all, we have decided to move all the powertrain except the battery pack to the PCS, which is shown in Fig. 1 (b). Thus, the duplicated components and the protection devices can be minimized. The losses among the components can be also reduced. Power and energy density of the system can be also improved.



(a) Conventional main powertrain of ESS.



(b) The proposed main powertrain of ESS.

Fig. 1. Block diagram of the commercial ESS.

Fig. 2 shows the block diagram of the PCS for ESS. The system consists of a dc switch/breaker, fuses, dc contactors with pre-charge circuit, a dc EMI filter, a neutral point clamped (NPC) three-level inverter, LCL filter, AC relays, an ac EMI filter, surge protective devices, and a ac breaker. All the devices are integrated into the PCS. Besides, a high-accuracy current sensor is integrated in the PCS for battery current sampling for the BMS. Enable signals are available for the BMS to disconnect the main dc contactors during serious system failure. Multiple communication modes, such as RS485, CAN, Ethernet, and Wifi/4G, are available.

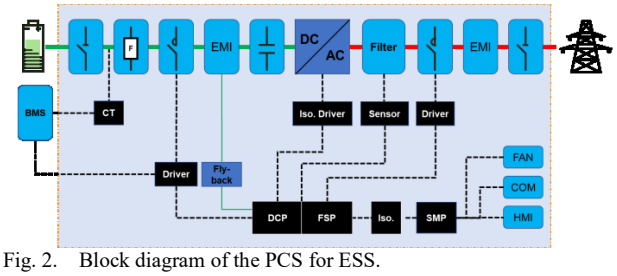


Fig. 2. Block diagram of the PCS for ESS.

Fig. 3 shows the prototype of an I-type NPC three-level inverter with Si based IGBT. The switching frequency is selected as 16 kHz and SVM operation for grid-tied operation. The conversion efficiency at full load condition is about 97.8 % under nominal conditions.

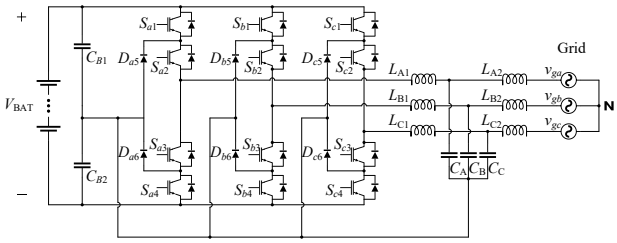


Fig. 3. NPC three-level inverter with Si based IGBT.

For the NPC three-level inverter in Fig. 3, each phase contains an I-type NPC IGBT module. The rating of the power module is 650 V/300 A with full rating for both IGBTs, clamping diodes and freewheeling diodes. Inside each NPC module, there are 4 IGBTs with 4 paralleled diodes and 2 clamped diodes connected to the neutral point of bus capacitors, which is shown in Fig. 4. Each IGBT is consisted of 4 IGBT dies in parallel and 1 anti-parallel protection diode, and each freewheeling diode and clamping diode is composed with 4 diodes dies in parallel. Thus, in total, there are 44 chips inside each power module.

The bonding wires are even 3–4 times higher than this number. This design is complicated and makes the quality and losses hard to control.

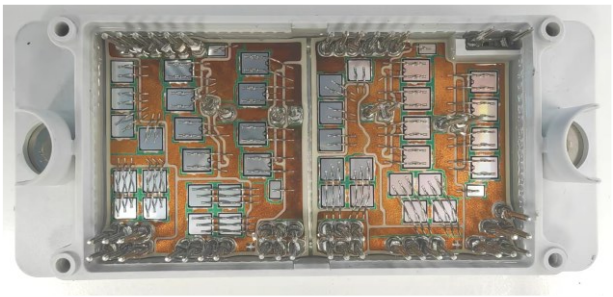


Fig. 4. A picture of the I-type NPC IGBT module.

To improve this, we try to introduce SiC MOSFET without extra anti-parallel diodes to replace the IGBT which need anti-parallel diodes for revering current. To reduce total volume of chips, T-type NPC is selected to replace the I-type NPC. Thus, the SiC MOSFET module is a T-type three-level power module. Each switch is composed by 3 SiC MOSFET dies in parallel. Thus, in total, we will only need 12 chips, which is almost 1/4 of the original number which is 44. Fig. 5 shows the topology of the SiC PCS.

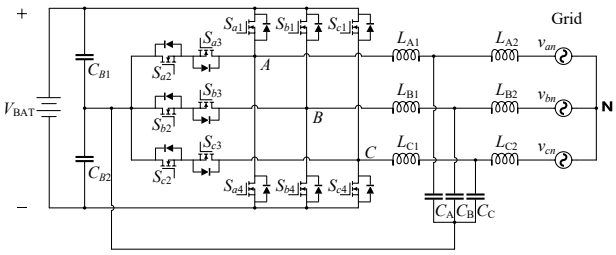


Fig. 5. SiC PCS with T-type three-level inverter topology.

IV. SiC Based Power Module Design

With the new SiC power module design, there are 4 SiC MOSFETs and a negative temperature coefficient (NTC) thermistor in a T-type NPC module, which is shown in Fig. 6. The diodes shown in this figure is the body diodes of the SiC MOSFET. Each SiC MOSFET is consisted of 3 SiC MOSFET dies in parallel. As a result, the chips inside each SiC MOSFET module can be reduced to 12 chips only. The bonding wires can also be reduced a lot.

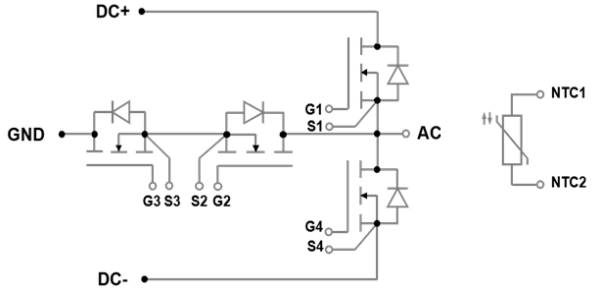
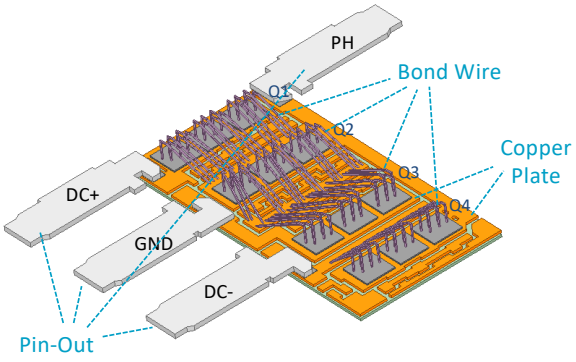


Fig. 6. Circuit diagram of the T-type three-level SiC MOSFET module.

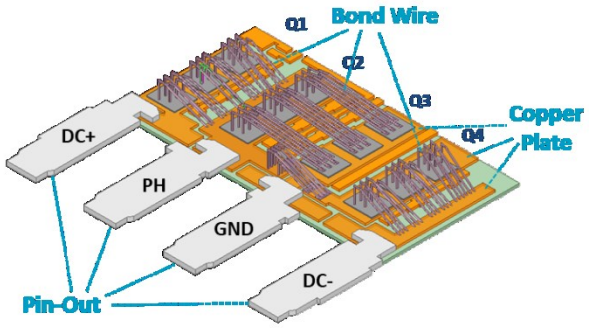
For the inverter, during switching operation, the

commutation are always between Q1 with Q2 and Q3 with Q4, to make each conduction loops with equal length, several layouts are proposed and final selections are shown in Fig. 7, which Q1 and Q4 are at each side with Q2 and Q3 in between. And Q2 is placed near Q1, Q3 is nearby Q4.

Both of the proposed layouts in Fig. 7 have four power terminals, they are the positive dc input terminal (DC+), the negative dc input terminal (DC-), the neutral point terminal (GND), and the ac terminal of vertical arm bridge midpoint (AC). In Fig. 7 (a), the first structure, short for layout 1, places the dc terminals and ac terminal at different sides of the module. The second structure, short for layout 2, shows in Fig. 7 (b), places the dc terminals and ac terminal at the same side of the module.

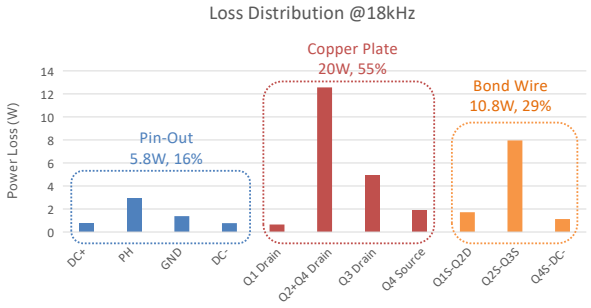


(a) Layout 1: DC and AC terminals are placed at different sides.

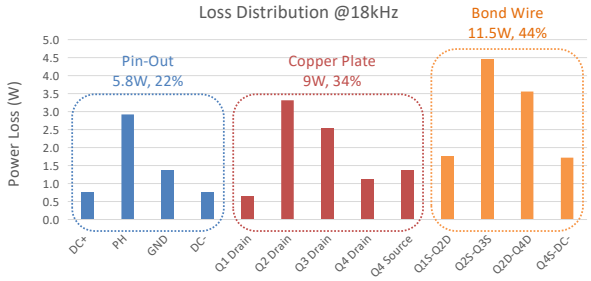


(b) Layout 2: DC and AC terminals are placed at the same side.
Fig. 7. The proposed structures of the SiC MOSFET module.

By calculating with simulation tool, the Cu/Al loss of each layout, including pin-out loss, copper plate loss, and bonding-wire loss, are obtained. Fig. 8 (a) and (b) show Cu/Al loss breakdown of layout 1 and layout 2 respectively. With conditions of battery voltage V_{bat} = 800 V, grid line voltage V_l = 380 V, output power P_{out} = 100 kW, junction temperature T_j = 125 °C, in layout 1, the pin-out loss is 5.8 W, the copper plate loss is 20 W, the bonding-wire loss is 10.8 W, and the total Cu/Al loss is 36.6 W. In layout 2 at the same conditions, the pin-out loss is 5.8 W, the copper plate loss is 9 W, the bonding-wire loss is 11.5 W, and the total Cu/Al loss is 26.3 W.

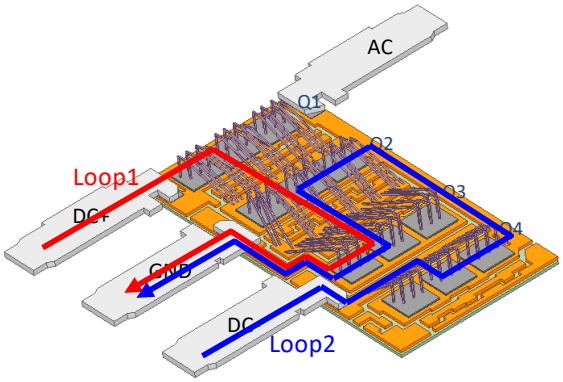


(a) Cu/Al loss breakdown of layout 1.

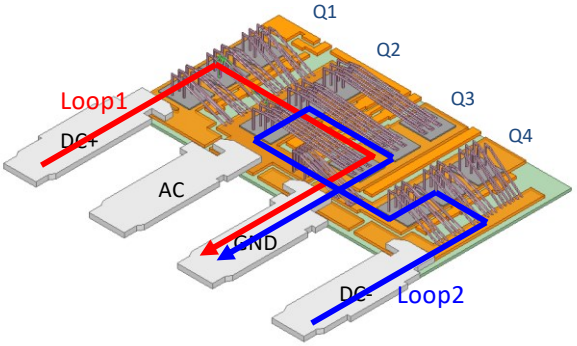


(b) Cu/Al loss breakdown of layout 2.
Fig. 8. Cu/Al loss breakdown of layout 1 and layout 2 at 18kHz switching frequency.

The parasitic parameter, especially the parasitic inductance of the commutation circuit loop is very important, because it has large influence on voltage stress of power switches. The commutation circuit loops, from DC+ to GND (Loop 1) and DC- to GND (Loop 2) for layout 1 and layout 2, are shown in Fig. 9 (a) and (b) respectively.



(a) Commutation circuit loop of layout 1.



(b) Commutation circuit loop of layout 2.
Fig. 9. Commutation circuit loop of the proposed SiC modules.

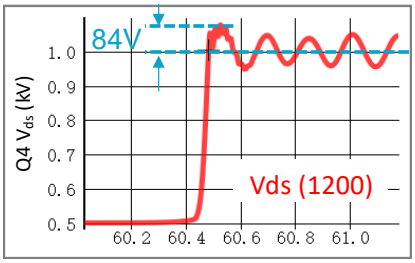
Table I shows the parasitic resistance and parasitic inductance of Loop 1 and Loop 2 in layout 1 and layout 2. The parasitic resistance of layout 2 is small than layout 1 for both Loop 1 and Loop 2. Besides, the maximum parasitic inductance (between Loop 1 and Loop 2) of layout 2 is smaller than layout 1.

TABLE I
LOOP PARAMETER COMPARISON BETWEEN LAYOUT 1 AND LAYOUT 2

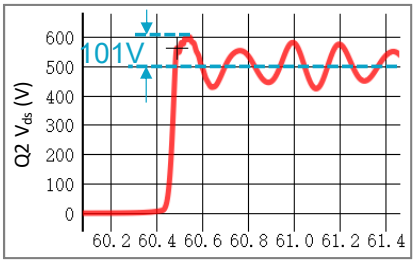
Critical Loop	Layout	Resistance (mΩ)		Inductance (nH)	
		18 kHz	24 kHz	18 kHz	24 kHz
DC+ to GND (Loop1)	Layout 1	1.89	2.00	28.9	28.1
	Layout 2	1.36	1.45	35.1	34.5
DC- to GND (Loop2)	Layout 1	2.91	3.09	37.9	36.6
	Layout 2	2.40	2.54	34.3	33.3

Based on the analysis above, layout 2 has small Cu/Al loss and lower parasitic inductance. As a result, layout 2 is the final selected structure of the T-type three-level SiC MOSFET module.

Fig. 10 shows the voltage stress of the SiC MOSFET module in the condition of dc voltage V_{dc} = 1000 V and turn-off current I_{off} = 250 A. The spike of the vertical SiC MOSFET (Q4) is 84 V, and the spike of the horizontal SiC MOSFET (Q2) is 101 V.



(a) Vertical SiC MOSFET (Q4) voltage stress.



(b) Horizontal SiC MOSFET (Q2) voltage stress.

Fig. 10. Voltage stress of the SiC MOSFET module.

V. PCS EFFICIENCY TESTING RESULTS

Fig. 11 shows the PCS with SiC MOSFET module for commercial ESS. Electrical parameters of the PCS are shown in TABLE II.

Fig. 11. A PCS with SiC MOSFET module for commercial ESS.

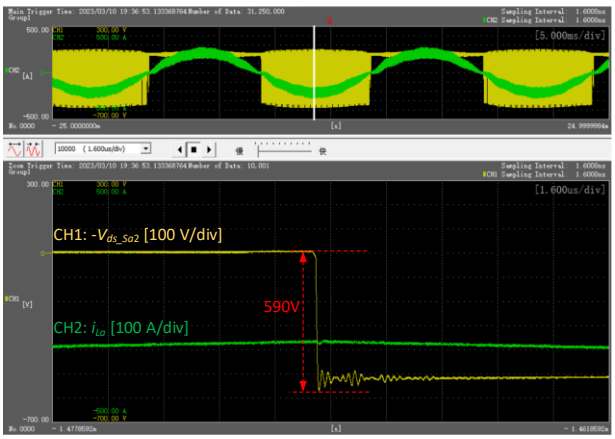
TABLE II
ELECTRICAL PARAMETERS OF THE PCS

Item	Description	Value
Battery Port	Operating voltage range	600–1000 V
	Rated input/ output power	100 kW
	Max. input/ output current	170 A
AC Port (on-grid mode)	Rated power	100 kVA
	Max. current	151 A
	Rated grid voltage	380/400 V, 3W+N+PE
	Frequency	50 Hz
	Power factor range	-1...+1
	THDi	<3 % (rated power)
Mechanical	Dimension (W × H × D)	700 × 266 × 850 mm
	Weight	85 kg

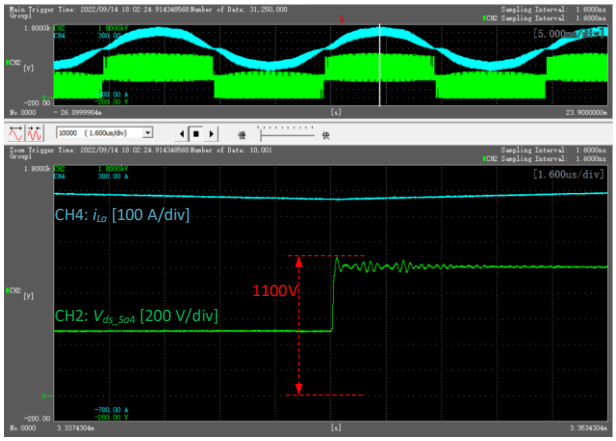
The PCS and battery pack with cooling system are integrated in a commercial ESS product with 215 kWh energy capacity, which is shown in Fig. 12.

Fig. 12. A commercial ESS product with SiC PCS.

Fig. 13 (a) and (b) show the voltage stress of the horizontal switch (S_{a2}) and vertical switch (S_{a4}) at conditions of V_l = 380 V, P_{out} = 100 kW, with maximum battery voltage V_{bat} = 1000 V. The horizontal switch (S_{a2}) voltage stress is 590 V, and the vertical switch (S_{a4}) is 1100 V.



(a) Voltage stress of the horizontal switch (S_{a2}).

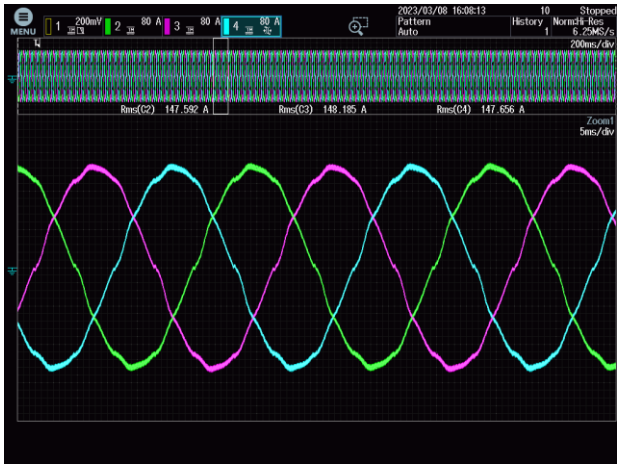


(b) Voltage stress of the vertical switch (S_{a4}).

Fig. 13. Voltage stress of the SiC MOSFET module (V_{bat} = 1000 V, V_l = 380 V, P_{out} = 100 kW).

Fig. 14 (a) and (b) show the three phase output current waveforms of the SiC PCS at conditions of V_{bat} = 800 V, V_l = 380 V, P_{out} = 100 kW in battery charging mode and battery discharging mode respectively. Fig. 15 shows the output current total harmonic distortion (THDi) at V_{bat} = 800 V. it can be seen that THDi under 40 % rated load is smaller than 2 % in battery charging mode, and it is smaller than 3 % in battery discharging mode.

(a) Battery charging mode.



(b) Battery discharging mode.

Fig. 14. Three phase output current waveforms of the SiC PCS (V_{bat} = 800 V, V_l = 380 V, P_{out} = 100 kW).

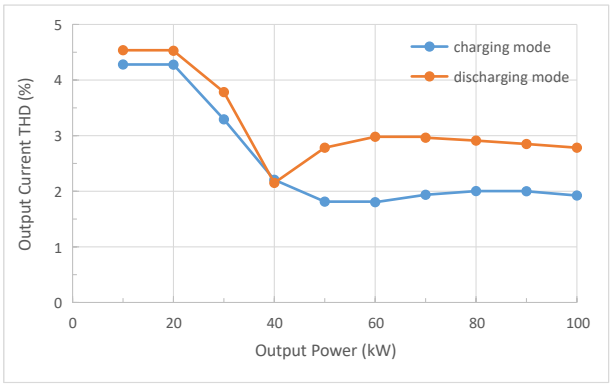
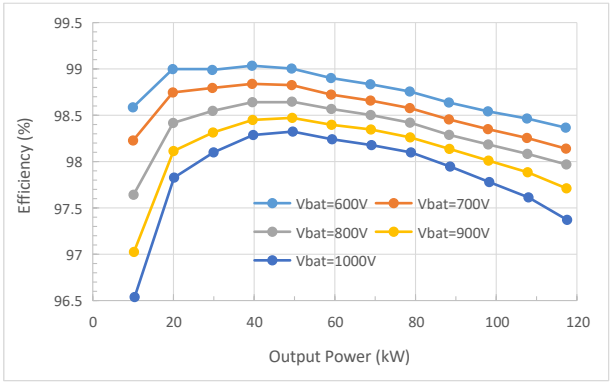
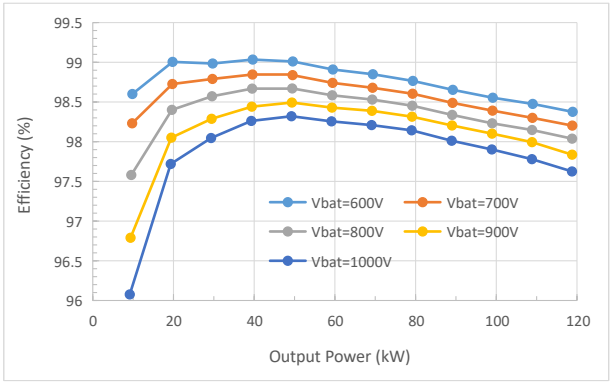


Fig. 15. THDi of the SiC PCS.

Fig. 16 (a) and (b) show the SiC PCS efficiency along with battery voltage and output power at V_l = 380 V and ambient T_a = 35 °C in battery charging mode and battery discharging mode respectively. Both in battery charging mode and discharging mode, the peak efficiency can reach 99.0 %, and the rated power efficiency can reach 98.5 %.



(a) Battery charging mode.



(b) Battery discharging mode.

Fig. 16. Efficiency of the SiC PCS along with battery voltage and output power (V_l = 380 V, T_a = 35 °C).

Fig. 17 shows the efficiency comparison of the SiC PCS and the IGBT PCS along with battery voltage at rated power. Generally, the rated power efficiency of the SiC PCS is about 0.6 % higher in battery charging mode, and 0.5 % higher in battery discharging mode, than that of the IGBT PCS.

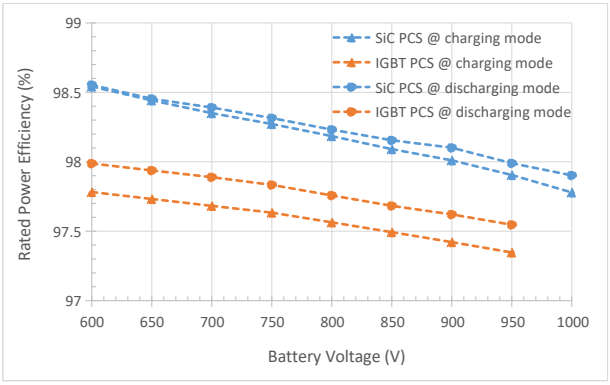


Fig. 17. Efficiency comparison of the SiC PCS and the IGBT PCS at rated power (V_l = 380 V, T_a = 35 °C).

VI. Conclusion

With the new T-type three-level SiC MOSFET module, the maximum rated power efficiency of PCS is improved from 97.8 % to 98.5 % in battery charging mode, and it is improved from 98.0 % to 98.5 % in battery discharging mode. Thus, the round trip efficiency of the ESS is improved 1.6 % to reach the 90 % efficiency goal.

Acknowledgment

The work of T-type three-level SiC MOSFET module design was accomplished by Suzhou Sizhi Technology Co., Ltd., China.

References

[1] H. Qian, J. Zhang, J. -S. Lai and W. Yu, "A high-efficiency grid-tie battery energy storage system," in IEEE Transactions on Power Electronics, vol. 26, no. 3, pp. 886-896, March 2011.

[2] M. Liu et al., "A Review of Power Conversion Systems and Design Schemes of High-Capacity Battery Energy Storage Systems," in IEEE Access, vol. 10, pp. 52030-52042, 2022.

[3] F. Díaz-González, D. Heredero-Peris, M. Pagès-Giménez, E. Prieto-Araujo and A. Sumper, "A Comparison of Power Conversion Systems for Modular Battery-Based Energy Storage Systems," in IEEE Access, vol. 8, pp. 29557-29574, 2020.