An Isolated Grid-Connected Charger with Reduced DC-Link Capacitor and Grid Filter Requirement

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Abstract-- **This paper proposes a grid-tied isolated low-voltage battery charging system. The ac-dc conversion stage is line frequency switched with ZVS capability and reduced grid filter requirement. The rectification is done by a three-level T-type neutral point clamped converter followed by a balancer circuit for power-factor correction. The dc-dc stage is a phase-shifted full-bridge converter which ensures high-frequency galvanic isolation. The rectification is done in such a way that pulsed dc voltage is obtained at the output of the T-type converter that reduces dc link capacitor requirement significantly. A new high-voltage polymer aluminium electrolytic capacitor technology has been proposed instead of conventional metalized film capacitors which leads to a more compact design. The switches in the ac-dc stage and dc-dc stage undergo zero-voltage-switching which improves the system efficiency. The control strategy of different stages and the simulation results for a 2 kW system is discussed here.**

***Index Terms*—AC-DC converter, Balancer, Battery charger, line frequency switching.**

I. Introduction

As the relevance of electric vehicles is increasing with each passing day, it is of utmost importance to design battery chargers of high reliability and good efficiency. While single-phase power factor corrected (PFC) converters are sufficient for low power charging levels, three-phase PFC converters are necessary as the power level increases. For on-board chargers, one of the most important requirements is compact and light-weight power converters. Most of cases isolation is required for safety reasons which mandate the use of an isolated dc-dc converter.

The conventional battery charging system consists of an active front end rectifier followed by a dc-dc stage depicted in Fig.1(a). High-frequency pulse width modulation is implemented to shift the harmonic spectrum to higher frequencies leading to reduction in filter size. However, the switching frequency cannot be increased indefinitely since it leads to higher switching loss.

Three-phase power factor correction rectifiers are required for grid-connected dc distribution systems. Swiss rectifier (SR) [1], [2] is one such topology suitable for grid interfacing. However, for high-power applications, its efficiency degrades. Active third harmonic current injection circuit is also an established method for power factor correction and grid current shaping [3]. In this topology, a current injection circuit is proposed containing bi-directional switches to inject third-harmonic current in the rectifier for grid current control.

Another approach is to use single-stage power factor correction rectifiers to improve power density and reduce circuit complexity. Using Vienna-rectifier a single-stage three-phase isolated rectifier has been proposed in [4]. However, it can only be used for unidirectional power flow. Another single stage isolated ac-dc conversion using Swiss-forward rectifier is proposed in [5].

Three-phase unfolder circuit followed by two series-resonant (SRC) high-frequency isolated converters with series output connection has been proposed in [6], [7]. Modular DBSRC system has been used here to enable dc-dc, dc-ac and ac-dc operation. But the drawback of the system is each series resonant converter has to process peak power P_{ac} meaning the dc-dc stage must be designed for $2P_{ac}$. Current unfolding method has been shown in [8] to control grid currents.

Phase-shifted full-bridge (PSFB) converter is widely used as isolated dc-dc converters in battery charging and telecom applications for high efficiency and simple control. Unlike resonant converters it operates at a constant switching frequency. The optimization and design procedure of a 99 % efficient, 5 kW PSFB has been depicted in [9].

This paper deals with a three-stage ac-dc converter system that uses line frequency switching in the three-phase rectifier to reduce grid filter requirement and a power factor correction stage that makes the line currents perfectly sinusoidal. The dc-dc stage is implemented using PSFB converter that is controlled to meet load-side voltage requirements. The block diagram of the proposed system has been shown in Fig. 1(b)The paper is organized in the following manner. Section II describes the system architecture. The modulation and control strategy are explained in section III. The voltage and current stress expressions of semiconductor devices and passives are given in section IV. Section V contains the simulation results for a 2 kW system. In section VI experimental results regarding the performance of the developed high voltage polymer aluminium electrolytic capacitor are shown and section VII presents the conclusion.

II. System Architecture

The system consists of a three-level t-type neutral point clamped converter (TNPC), a balancer circuit followed by a phase-shifted full-bridge (PSFB) converter as shown in

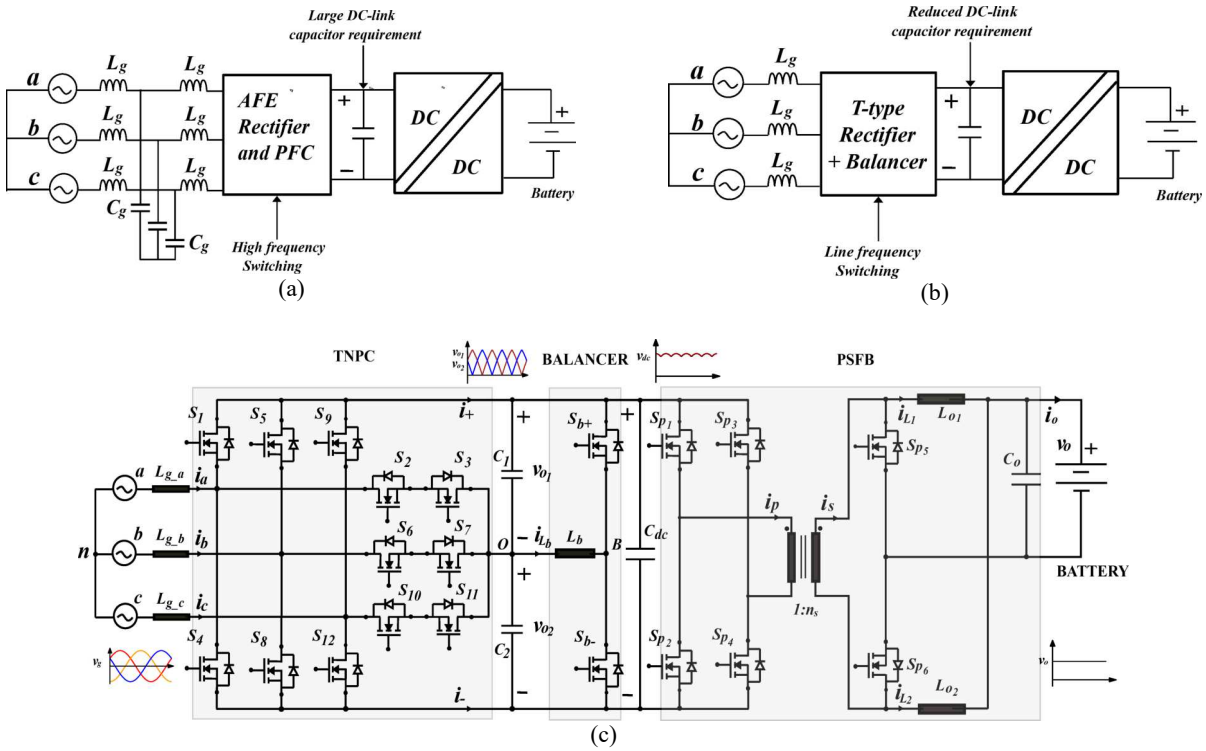


Fig. 1. Circuit block diagram (a) block diagram of conventional battery charger (b) block diagram of proposed topology, and (c) circuit diagram of proposed battery charger

Fig. 1(b). The TNPC rectifies the three-phase ac into a pulsed dc voltage. The balancer circuit is employed to shape the grid currents and maintain almost unity power factor. The last stage is the dc-dc stage which steps down the voltage and provides galvanic isolation. This circuit is capable of bi-directional power flow, so the battery can also feed power to the grid. In this paper the converters are designed for charging 48 V batteries. However, this topology is also suitable for charging high voltage batteries. At the output of TNPC, we get an output voltage pulsating at a frequency six times the grid frequency. The peak of the six-pulse output is equal to the peak value of the line voltage. For a conventional two-level converter out of the three phases, only two phases conduct at a time – the phase having the positive maximum and the phase having the negative maximum. The phase having the minimum absolute value does not conduct current. The advantage of using a three-level converter is that all three phases conduct current simultaneously. The positive bus carries a current (i_+) proportional to the positive most phase voltage (v_{max}) and the negative bus carries a current (i_-) that is proportional to the negative most phase voltage (v_{min}) at each sector. The remaining phase (v_{mid}) pushes current in the balancer inductor. The balancer current has a frequency thrice the grid frequency. The peak value of the balancer current is half the amplitude of the line current. In this circuit, instead of dc link voltage dc link current is controlled with the help of the balancer circuit.

The upper leg (S_1, S_5, S_9) and lower leg switches (S_4, S_8, S_{12}) of the TNPC are switched at 50 Hz, i.e., line frequency (120° conduction period at each cycle) and the mid-leg switches (S_2, S_3, S_6, S_7, S_{10}, S_{11}) are switched at twice the line frequency (two 60° conduction periods at each cycle) as depicted in Fig.2(b). The switches of TNPC undergo zero-voltage switching during both turn-on and turn-off resulting in almost zero switching loss. Line frequency switching at the rectifier stage reduces grid filter size and simple L-filters suffice the filter requirement. As dc link voltage is pulsating in nature, capacitor requirement reduces drastically. Instead of large electrolytic capacitors, a new high voltage polymer aluminium electrolytic capacitor has been developed to use at the dc link. However, the high ESR of traditional aluminum electrolytic capacitor leads to increased self-heating and decreased ripple current handling. To overcome this issue, the poorly conducting liquid electrolyte for traditional electrolytic capacitors, can be substituted for better conducting material. For lower voltages PEDOT: PSS-based electrolytes have been successfully developed providing significantly better ESR and current handling. The performance plots of the capacitor are shown in section VI.

The dc-dc stage has been realized using a phase-shifted full-bridge converter. PSFB is an isolated buck-derived converter. Its control strategy is simpler compared to other commonly used dc-dc converters like Dual Active Bridge (DAB). The secondary side of the PSFB is a current-doubler circuit having two output inductors. The inductor currents are phase shifted and the summation of these two inductor currents flows to the load. Hence, the amount of ripple in total output current is much less than the ripple in individual inductor currents. During turn-on the primary side and secondary side switches of PSFB undergo zero-voltage-switching. Leakage inductance in the high-frequency transformer facilitates ZVS during turn-on of switches.

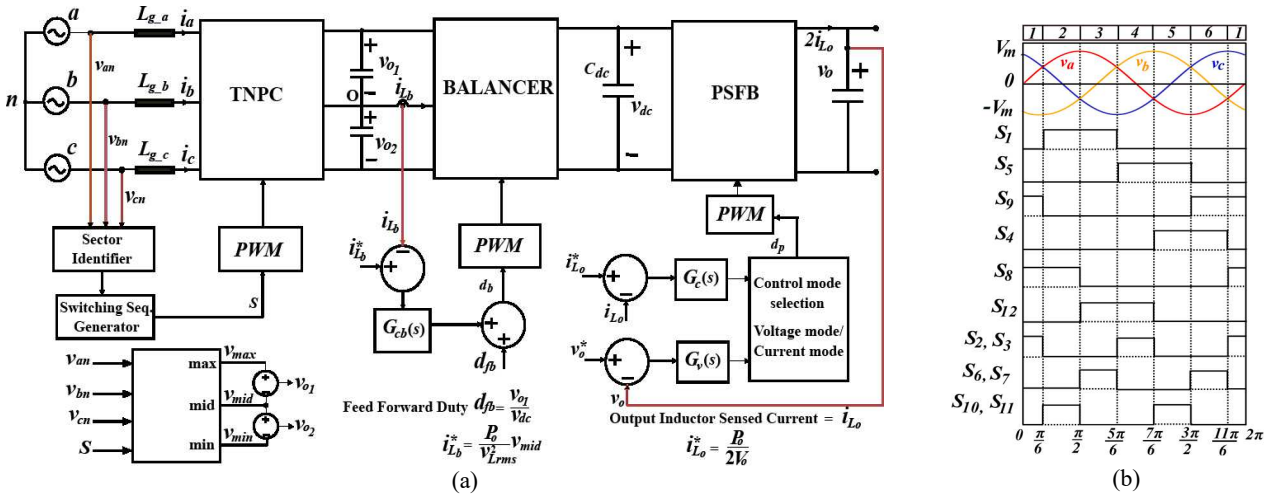


Fig. 2. Control strategy at different stages (a) Controller block diagram and (b) gate pulses of TNPC switches

III. Control Strategy of The Three Stage AC-DC Converter

The control block diagram is shown in Fig.2. Let us take the grid voltages as v_{an}, v_{bn} and v_{cn} with respect to a common neutral point n. Each line cycle is divided into six sectors as shown in Fig. 2(b) and then the switching sequence is generated in such a way that variable dc voltages v_{o1} and v_{o2} are obtained across C_1 and C_2 respectively and six pulse dc between positive and negative bus as shown in Fig.4(a). For example, if sector 2 [30°, 90°] is taken, v_{an} is maximum, v_{bn} is minimum and v_{cn} has a magnitude between v_{an} and v_{bn}. Therefore, v_{an} gets connected to positive bus via S_1, v_{bn} gets connected to the negative bus via S_8 whereas v_{cn} is connected to the mid-rail through S_{10} and S_{11}. The gate pulses provided to the switches of TNPC are shown in Fig. 2(b). The voltages v_{o1}, v_{o2} and v_{dc} can be expressed in the following manner.

$$\begin{cases} v_{01} = max\left(v_{an}, v_{bn}, v_{cn}\right) - mid\left(v_{an}, v_{bn}, v_{cn}\right) \\ v_{02} = mid\left(v_{an}, v_{bn}, v_{cn}\right) - min\left(v_{an}, v_{bn}, v_{cn}\right) \\ v_{dc} = max\left(v_{an}, v_{bn}, v_{cn}\right) - min\left(v_{an}, v_{bn}, v_{cn}\right) \end{cases} \quad (1)$$

The balancer current reference i_{Lb}* and the sensed balancer inductor current are shown in Fig 3(b). Balancer inductor current at any instant is proportional to v_{mid}. The sensed current contains switching frequency ripples as well. The balancer current controller $G_{cb}(s)$ is a high bandwidth controller capable of tracking the reference current. For controller design, Balancer circuit can be modelled as simple buck/ boost converter. Feed forward duty (d_{fb}) is provided to reduce the controller burden. The balancer switches S_{b+} and S_{b-} are given complementary pulses. The voltages across capacitors C_1, C_2, C_3, the phase currents and feed forward duty at each sector have been shown in Table I. Balancer reference current and feed forward duty can be expressed as

$$\begin{cases} i_{L_b}^* = \dfrac{P}{v_{L_{rms}}^2} v_{mid} \\ d_{fb} = \dfrac{v_{01}}{v_{dc}} \end{cases} \quad (2)$$

Table I

Instantaneous Voltages and Feed-Forward Duty at Different Sectors

Sector	v_{01}	v_{02}	v_{dc}	i_+	i_-	i_{mid}	d_{fb}
1	v_{ca}	v_{ab}	v_{cb}	i_c	i_b	i_a	v_{ca}/v_{cb}
2	v_{ac}	v_{cb}	v_{ab}	i_a	i_b	i_c	v_{ac}/v_{ab}
3	v_{ab}	v_{bc}	v_{ac}	i_a	i_c	i_b	v_{ab}/v_{ac}
4	v_{ba}	v_{ac}	v_{bc}	i_b	i_c	i_a	v_{ba}/v_{bc}
5	v_{bc}	v_{ca}	v_{ba}	i_b	i_a	i_c	v_{bc}/v_{ba}
6	v_{cb}	v_{ba}	v_{ca}	i_c	i_a	i_b	v_{cb}/v_{ca}

The dc –dc stage has two modes of control – current control mode and voltage control mode. According to the charging profile requirement of the battery the mode of control is selected. When the battery is heavily discharged constant current mode charging is preferred. When SoC reaches a value near 80 % - 90 %, the charging mode is shifted to constant voltage mode. i_{Lo}* and v_o* are the current and voltage references provided to the controllers $G_c(s)$ and $G_v(s)$ respectively. The average load current value is twice the average current value of each inductor. Both the inductor currents are controlled in order to maintain the same average current in them. During constant voltage mode the reference is v_o*, which is the rated voltage or the required voltage that needs to be maintained at battery output.

$$\begin{cases} i_{L_o}^* = \dfrac{P}{2v_o} \\ v_o = nDv_{in} \end{cases} \quad (3)$$

Here, the output of the controller is basically the phase shift between the two legs of the full bridge circuit in the primary side of PSFB. The output voltage (v_o) of PSFB is directly proportional to the phase shift expressed as the fraction of time period (D) provided turns ratio (n) and input voltage (v_{in}) are constant. Due to the presence of transformer leakage inductance duty loss occurs. The duty loss mode has not been taken into account as its duration is very small compared to power delivery duration.

IV. Design Methodology

This section shows the voltage and current stresses on semiconductor devices and passive components. The design expressions for passive component selection have also been discussed. While deriving the expressions some assumptions were taken – the rectifier draws purely sinusoidal current from the grid and the switching frequency of the balancer stage and dc-dc stage are much higher than the line frequency. The parasitic components in semiconductor devices and passives have not been taken into consideration.

A. Voltage and Current Stresses on Semiconductors

The upper leg (S_1, S_5 and S_9) and lower leg switches (S_4, S_8 and S_{12}) of TNPC need to block a voltage equal to the maximum line-line voltage.

$$v_{S,\max} = v_{l-l,\max} = \sqrt{2}\sqrt{3}v_{rms} \tag{4}$$

Here v_{rms} is the rms value of phase voltage.

The mid-leg switches of TNPC block a voltage $\frac{\sqrt{3}}{2}$ times the maximum line-line voltage.

$$v_{S,mid-leg,\max} = \frac{\sqrt{3}}{2} v_{l-l,\max} \tag{5}$$

The maximum current that upper leg and lower leg switches have to withstand is the peak line current.

$$I_{S,\max} = I_{\max} \quad \text{and} \quad I_{\max} = \frac{\sqrt{2}P}{3v_{rms}} \tag{6}$$

The current stress on mid-leg switches is half the amplitude of line current.

$$I_{S,mid-leg,\max} = \frac{I_{\max}}{2} \tag{7}$$

Balancer switches need to block maximum line-line voltage.

$$v_{S,Balancer,\max} = v_{l-l,\max} \tag{8}$$

Maximum current through balancer switches is half the maximum line current.

$$I_{S,Balancer,\max} = \frac{I_{\max}}{2} \tag{9}$$

PSFB primary side switches blocks the six-pulse dc-link voltage. The maximum dc link voltage is the peak line-line voltage.

$$v_{S,PSFB,pri,\max} = v_{in,\max} = \sqrt{2}\sqrt{3}v_{rms} \tag{10}$$

The maximum current that flows through primary side switches is the reflected maximum output inductor current.

$$I_{S,PSFB,pri,\max} = nI_{L,\max} = n\left(I_L + \frac{\Delta i_L}{2}\right) \tag{11}$$

Where Δi_L is the peak-peak current ripple in each output inductor of PSFB.

The secondary side switches, i.e., the synchronous rectifiers need to block the voltage that appears across the transformer secondary.

$$v_{S,PSFB,\text{sec},\max} = nv_{in} \tag{12}$$

The maximum current through each synchronous rectifier is the maximum load current.

$$I_{S,PSFB,\text{sec},\max} = I_{o,\max} = \left(I_o + \frac{\Delta i_o}{2}\right) \tag{13}$$

I_o is the average load current. Δi_o can be expressed as the summation of instantaneous ripple in each inductor. Due to phase-shifted inductor currents, the effective ripple reduces significantly.

$$\begin{cases} \Delta i_o = \Delta i_{L_1} + \Delta i_{L_2} \\ \Delta i_{L_1} = \left(\dfrac{nv_{in} - v_o}{L_o}\right) DT_s \\ \Delta i_{L_2} = \left(\dfrac{-v_o}{L_o}\right) DT_s \end{cases} \tag{14}$$

B. Voltage and Current Stresses on Passives

The instantaneous currents through capacitors C_1, C_2 and C_{dc} can be expressed as

$$i_c = C\frac{dv_c}{dt} \tag{15}$$

Where v_c is v_{01}, v_{02} and v_{dc} respectively. As capacitor values are very small (Values mentioned in Table III), the current through them is also small.

The maximum voltage appearing across balancer inductor (L_b) is

$$v_{L,Balancer,\max} = \frac{\sqrt{3}}{2} v_{l-l,\max} \tag{16}$$

The maximum current through L_b is given by -

$$I_{L,Balancer,\max} = \frac{I_{\max}}{2} \tag{17}$$

The peak-peak current ripple through each output inductor (L_o) is taken 40% of the average inductor current. The maximum current through PSFB output inductors and the inductor value can be expressed as

$$I_{L_o,\max} = I_L + \frac{\Delta i_L}{2} \tag{18}$$

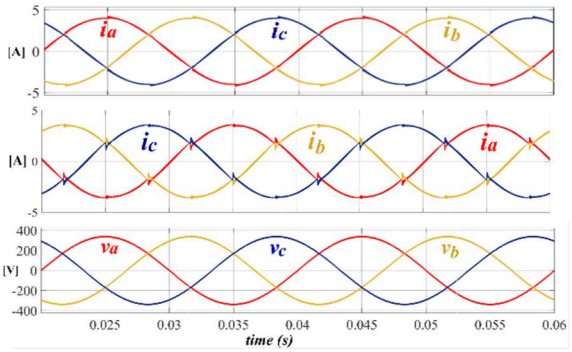
Here I_L is the average inductor current.

$$L_o \geq \left(\frac{nv_{in} - v_o}{\Delta i_{L_1}}\right) DT_s \tag{19}$$

The output capacitor (C_o) of PSFB is designed to limit the output voltage ripple within 0.1 V. The current flowing through C_o has a frequency twice the PSFB switching frequency. The peak current through the output capacitor and the capacitor value can be expressed as

$$I_{C_o,\max} = \frac{\Delta i_o}{2} \tag{20}$$

$$C_o \geq \frac{\Delta i_o}{8 f_c \Delta v_o} \tag{21}$$



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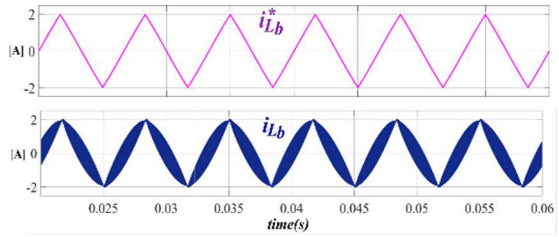

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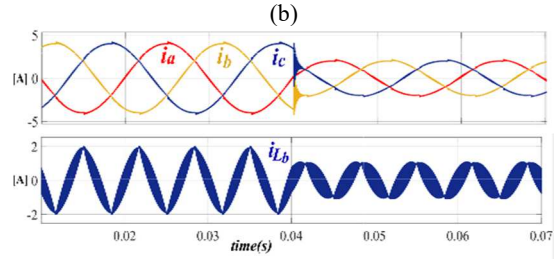
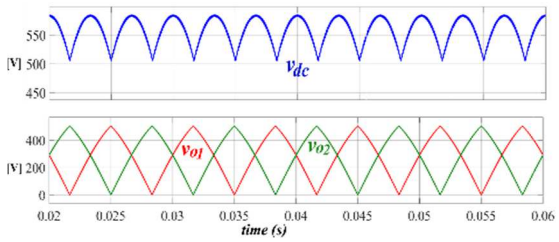


(c)

Fig. 3. Simulation results (a) grid currents (i_a, i_b, i_c) and grid voltages (v_{an}, v_{bn}, v_{cn}) for output power of 2 kW at upf from grid to battery and battery to grid (b) balancer inductor reference current and sensed current, and (c) grid currents and balancer inductor current transition for change in power from 2 kW to 1 kW.

V. Simulation Results

The proposed system was simulated in MATLAB/Simulink to validate the operation of different stages and to monitor controller performance. In Fig. 3(a) the line currents and phase-neutral voltages have been shown for a 2 kW system. The line currents are sinusoidal with less than 2% Total Harmonic Distortion (THD) and in phase with the grid voltages. Fig. 3(b) shows the reference current fed to the balancer controller and the actual balancer inductor current. Fig.3(c) shows the transition from 2 kW to 1 kW for line currents and balancer inductor currents. While transitioning the oscillations die down very quickly and an almost smooth transition can be observed. The simulation is done based on the specification mentioned in Table II. The inductor and capacitor values at different stages are mentioned in Table III. Fig. 4(a) shows the pulsed dc link voltage v_{dc} and voltages v_{o1} and v_{o2}. The individual inductor currents and their summation have been shown in Fig. 4(b). From the simulation results it is evident that although the inductor currents have peak-peak ripple of almost 8 A, the sum of the currents have less than 2 A ripple. Due to the ripple reduction the capacitor value is reduced at the load side. The THD of line current is shown in Fig. (5).



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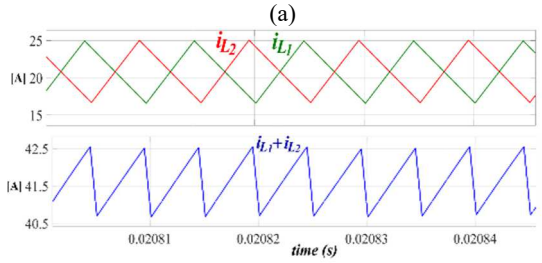

(b)

Fig. 4. Simulation results (a) v_{dc}, v_{o1} and v_{o2} for output power of 2 kW at upf current, and (b) PSFB output inductor currents and their summation.

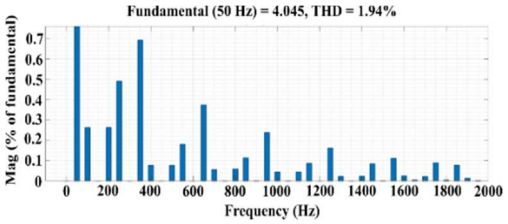

Fig. 5. Total Harmonic Distortion (THD) of line current.

TABLE II
SYSTEM SPECIFICATION

Line voltage RMS	415 V
Line frequency	50 Hz
Power rating	2 kW
Battery voltage rating	48 V
Balancer switching freq.	50 kHz
PSFB switching freq.	100 kHz

TABLE III
DESIGN PARAMETERS

Grid filter inductor L_g	50 µH
DC link capacitors C_1, C_2	0.5 µF
Balancer inductor L_b	2 mH
PSFB input capacitor C_{dc}	1 µF
PSFB HF trf. turns ratio $1{:}n_s$	1:0.25
PSFB output inductor L_{o1}, L_{o2}	33 µH
PSFB output capacitor C_o	16 µF

VI. Experimental Results of The Solid Electrolyte Capacitors.

The use of aluminium electrolytic capacitors as DC-link capacitors instead of the more traditional metalized film capacitors can lead to ultra-compact integrated inverter designs. This technology however has so far not reached the operating voltages that the automotive industry desires for DC-link capacitors in power converters in electric cars. Developing this technology to operate reliably at voltages at about 450 V will allow polymer aluminum electrolytic

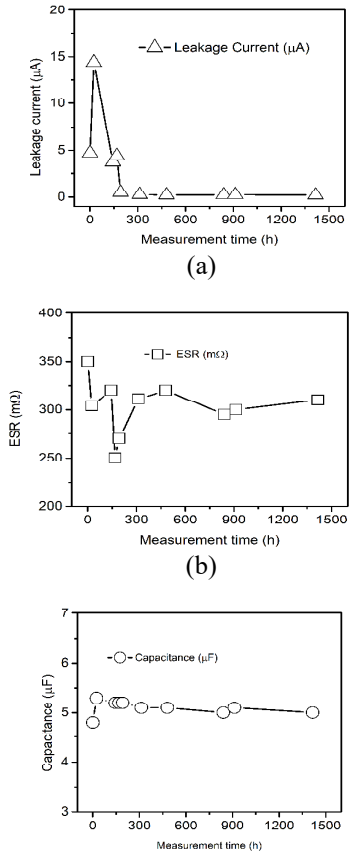

Figure 6: Lifetime measurement of the single stake e-caps a) leakage current, b) ESR, and c) capacitance.

capacitors to compete with film capacitors as DC-link in power converters in electrical vehicles.

An encapsulated capacitor has been made using standard electrolytic capacitor (e-caps) preparation method [10]. The lifetime behavior (aging test) of the successfully prepared e-caps is under measurement. ESR and leakage current of the capacitor have been monitored at 450V and 105°C for 1300 hrs. X-ray tomography measurements have been conducted before and after the aging test in order to know the physical status of the encapsulated e-caps. Leakage current, capacitance, and resistance were measured at regular intervals throughout the lifetime study (Figure 6).

Use the International System of Units (SI - MKSA) as primary units. British units could be used as secondary units in parentheses.

VI. Conclusion

This paper proposes a grid-connected bidirectional isolated AC-DC converter topology suitable for electric vehicle battery chargers. The rectifier stage is line frequency switched which not only reduces switching loss significantly but also reduces grid filter requirement to great extent. This converter topology enables to reduce the dc link capacitor to almost negligible value as compared to conventional ac-dc converters. This paper presents a new aluminium electrolytic capacitor having low ESR value and capable of handling high ripple current. Here the system architecture, the modulation technique at each stage, relevant simulation results for a 2 kW system as well as the lifetime measurement of the high-performance polymer aluminium electrolytic capacitor have been shown.

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References

[1] T. Soeiro, T. Friedli, and J. W. Kolar, "Swiss rectifier – a novel three-phase buck-type PFC topology for electric vehicle battery charging," in *Proc. 27th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Feb., 2012, pp. 2617–2624.

[2] T. Soeiro, T. Friedli, and J. W. Kolar, "Design and implementation of a three-phase buck-type third harmonic current injection PFC rectifier (Swiss rectifier)," *IEEE Trans. Power Electron.*, 2012, DOI: 10.1109/TPEL.2012.2209680.

[3] T. B. Soeiro, F. Vancu, and J. W. Kolar, "Hybrid active third-harmonic current injection mains interface concept for dc distribution systems," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 7–13, 2013

[4] J. Kolar, U. Drofenik, and F. Zach, "Vienna rectifier ii-a novel single-stage high-frequency isolated three-phase pwm rectifier system," *IEEE Trans. Ind. Electron.*, vol. 46, no. 4, pp. 674–691, 1999.

[5] M. Silva, N. Hensgens, J. A. Oliver, P. Alou, Garc´ıa, and J. A. Cobos, "Isolated swiss-forward three-phase rectifier with resonant reset," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4795–4808, 2016.

[6] W. Chen, R. Zane, D. Seltzer, and L. Corradini, "Isolated bidirectional dc/ac and ac/dc three-phase power conversion using series resonant converter modules and a three-phase unfolder," in *2014 IEEE 15th Workshop on Control and Modeling for Power Electronics (COMPEL)*, pp. 1–6, 2014.

[7] W. W. Chen, R. Zane, and L. Corradini, "Isolated bidirectional grid-tied three-phase ac–dc power conversion using series-resonant converter modules and a three-phase unfolder," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9001–9012, 2017.

[8] H. Pham N., T. Mannen and K. Wada, "A Three-Phase Isolated Rectifier using Current Unfolding and Active Damping Methods," *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2020, pp. 4587-4593, DOI: 10.1109/ECCE44975.2020.9235762.

[9] U. Badstuebner, J. Biela and J. W. Kolar, "An optimized, 99% efficient, 5 kW, phase-shift PWM DC-DC converter for data centers and telecom applications," *The 2010 International Power Electronics Conference - ECCE ASIA -*, 2010, pp. 626-634, DOI: 10.1109/IPEC.2010.5543337.

[10] S. Buhrkal-Donau, M. Gruia and T. Ebel, High-Voltage, Low ESR Solid Electrolyte E-Caps for Automotive applications. *2022, 12th International Conference on Integrated Power Electronics Systems*, pp. 1-5.