Three-Phase ZVS Inverter with Variable and Fixed Frequency Operation based on GaN Semiconductors

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Keywords

«ZVS converters», «Voltage Source Inverter (VSI)», «Gallium Nitride (GaN)».

Abstract

As high efficiency is on everyone's lips, this paper studies an inverter using a ZVS modulation scheme promising high efficiency. It uses triangular current mode (TCM) to minimize the ripple while maintaining ZVS. In order to fulfill the required power density, high switching frequencies should be applied. Current threshold detection circuits in combination with this modulation scheme turn the inverter's legs into current sources. Since all phases of the inverter are tied together at the load's star point, there might be issues, if slight current threshold errors exist within the inverter. In order to demonstrate that the modulation scheme can handle situations with and without connection of the load's neutral point to the DC-link midpoint, both configurations are studied in a practical setup. The practical test setup gives satisfactory results with respect to the quality of the output waveforms using the THD of the currents.

Introduction

High efficiency and power density are typical demands in power electronics, which can only be achieved by moving the switching frequency up to several hundred kHz as thereby passives shrink in size. In order to enable that high switching frequencies, switching losses need to be eliminated, because these scale linearly with frequency [1]. Thus, lossless switching, especially zero voltage switching (ZVS), should be exploited [2]. In inverters, triangular current mode (TCM) realizes ZVS and current mode control [3] [4] [5] [6] [7]. Compared to conventional fixed frequency PWM operation, TCM has an increased current ripple, but eliminates switching losses [8]. From this modulation scheme, typically a variable switching frequency results, which has its highest value around the zero crossing of the sinusoidal current [9]. The switching frequency must be limited to a certain value capable for all components within the circuit. This is why, a modulation scheme with two operating modes, fixed (around zero crossing of the sinusoidal current) and variable (in all other regions) switching frequency, results [10].
In order to detect zero crossing of the high frequency inductor current during variable switching frequency operation, which is required to enable lossless switching, a current threshold detection circuit can be used [11]. Hence, the inverter acts like a current mode controlled one. In case all phases of the inverter operate in current mode control, three current sources feed the load. Non-idealities of the components and their tolerances can lead to the sum of the inductor currents (at the load's star point) to be non-zero. Thus, in applications without a neutral point connection at the load, this may results in problems.
Therefore, this paper first theoretically analyzes the modulation scheme and based on promising simulation results, an experimental setup is built. A first study at the practical setup uses a connection of the load's neutral point to the midpoint of the DC-link, which delivers smooth sinusoidal output waveforms as intended. Then, to prove the versatility of the modulation scheme using applications without neutral point connection, the potential of the neutral point is floating.

Inverter Topology and Operating Principles

Each leg of the two-level inverter studied (Fig. 1) comprises a representation of the load (modeling the fundamental frequency), a LC output filter, and a half-bridge. Furthermore, there is a circuit for the study of the star point connection of the load Y consisting of two capacitors C_M connected in series, paralleled to the DC-link.

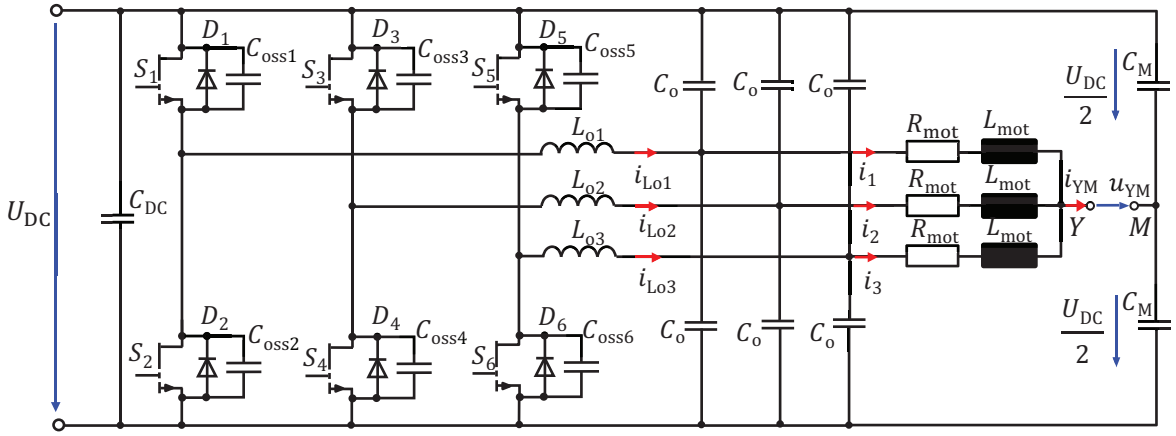

Fig. 1: Three-phase ZVS inverter with LC output filter and load

In order to study the modulation scheme, considering only one leg (half-bridge) of the inverter is sufficient. Thus, Fig. 2 (left) shows the circuit diagram including the modulator and current sensing circuit, all explanations refer to this half-bridge. The output side LC filter minimizes EMI emissions of the inverter. Properly designed, the inverter can achieve zero voltage switching (ZVS) by using a variable switching frequency modulation scheme in combination with the LC filter. Triangular current mode (TCM) allows applying ZVS during the entire sinusoidal period. Voltage sources at the input ($U_{DC}/2$) represent the DC-link capacitors. For explaining the behavior using a single phase representation of the inverter (Fig. 2 (left)), the load is connected to the midpoint of the DC-link capacitors. Using a three-phase inverter, the load is typically connected at the star point (see Fig. 1). The load model comprises an inductor and a resistor (Fig. 2 (right)) and corresponds to the terminal impedance typical of the grid or an electric machine. Simulations can be carried out just using the fundamental frequency to describe the load, as the LC output filter minimizes high frequency noise. Consequently, the resulting output current and component values can be gained by an AC analysis of the circuit for a given operating point of the inverter (output voltage, power and phase angle).

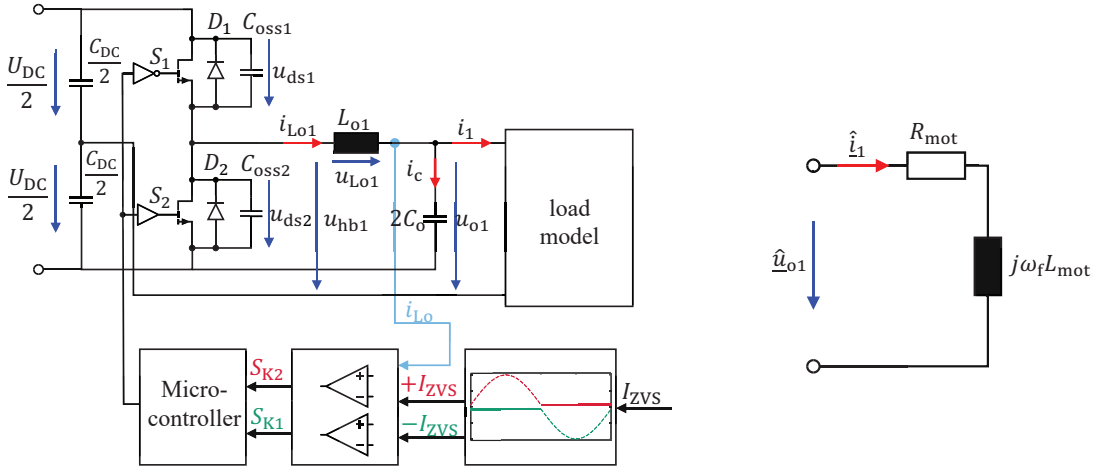

Fig. 2: Schematic of one half-bridge of the inverter including block diagram of the inductor current sensing circuit (left); single phase load model (right)

The inverter's output current is of sinusoidal shape with the fundamental period T_f and is given by:

$$i_1 = \hat{i}_1 \cdot \sin(\omega_f t) \qquad \text{where} \qquad \omega_f = 2\pi f_f = \frac{2\pi}{T_f} \tag{1}$$

The corresponding output voltage generally is phase shifted to the current:

$$u_{o1} = \hat{u}_{o1} \cdot \sin(\omega_f t + \varphi_u) \tag{2}$$

Modulation Scheme

The two aspects, generating a sinusoidal output voltage and reaching ZVS over the entire sinusoidal period, mentioned above require a suitable modulation strategy. In order to discharge the output capacitors (C_{oss}) of the lower and upper switch prior turn-on, which is required for ZVS, the inductor current needs to have a proper sign during each switching action. One switching action per switching period is typically uncritical with respect to ZVS[12]. During the positive half-wave the uncritical switching action is the one, at which the upper switch S_1 is turned off and, after the dead time has elapsed, the lower one turns on. The output current's sign and value certainly brings the voltage across the lower switch u_{ds2} to zero prior the lower switch turning on. In contrast, for reaching lossless turn-on (ZVS) for the other switching action, the modulation must provide a negative inductor current during this switching transition. The switching actions are vice versa during the negative half-wave. In order to reach the second goal (sinusoidal output current), the averaged inductor current over one switching period must coincide to the desired output current and the current phase angle of the sine to ensure high quality output waveforms. In case of fixed switching frequency modulation, a very high current ripple would be necessary to achieve ZVS over the entire sinusoidal period, which is why a variable switching frequency is used.

To reach the goals mentioned above, proper inductor current limits need to be set [13]. That's why a suitable current threshold detection circuitry is used. One approach sets the lower as well as the upper bound by comparators in conjunction with digital-analog converters [5] [6] [7] [14]. As these circuits are both costly and complex, another method, which combines a current threshold measurement and calculation to generate the switching pattern of the semiconductors, significantly minimizes cost [3] [11]. It uses only one comparator per half-wave and avoids digital-analog converters resulting in a hybrid modulation scheme.

The comparator generates the turn-off instant for the lower power semiconductor during the positive half-wave. Once the dead time t_{dead} has elapsed, the upper switch turns on featuring ZVS. The inductor current discharges the output capacitor of the upper semiconductor to reach ZVS during the dead time. A digital control circuit then derives the conduction time of the upper power semiconductor on the basis of theoretical equations. Thus, the digital controller delivers suitable gate signals to achieve ZVS and to provide sinusoidal output waveforms. The switching actions are vice versa during the negative half-wave of the sinusoidal period. Fig. 2 (left) gives the schematic of the converter and the block diagram of the inductor current detection circuit. As the modulation scheme is analogous for the negative half-wave, the explanations refer to the positive half-wave only.

In order to achieve high efficiency and exploit ZVS, the modulation scheme typically features a variable switching frequency. Assuming a resistive load, the lowest switching frequency occurs near the sinusoidal maximum and the highest is present around the zero crossing zone [9]. Especially if the modulation scheme is applied for the whole sinusoidal period, a wide frequency range results from the modulation scheme (see Fig. 3, dashed).

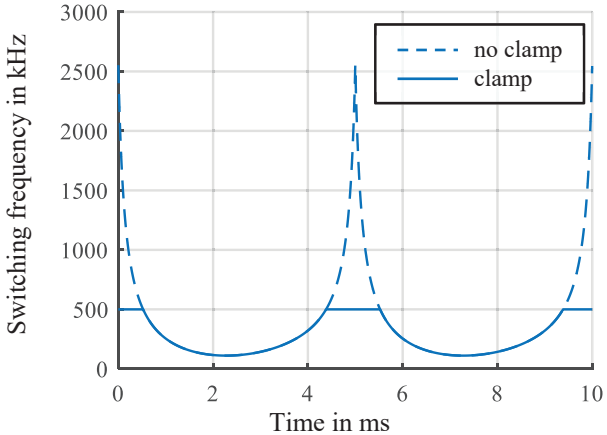

Fig. 3: Simulated switching frequency with and without clamping for a complete sinusoidal period

Since several components in power electronic circuits cannot handle very high switching frequencies, an upper limit for the switching frequency needs to be set. In addition, EMI standards give limits for the switching frequency in some applications to ensure to comply with the standards with a reasonable design of the circuit [10]. In this paper we use an upper limit for the switching frequency of 500 kHz, which is the lower limit for some automotive EMC standards. Another purpose of choosing 500 kHz as frequency boundary is to show the capabilities and limits of an implementation using a digital signal processor (DSP). Of course, some applications may favor lower frequency limits. As a result, the modulation scheme features fixed and variable switching frequency. Fig. 3 shows (solid) that fixed frequency operation occurs near the current's zero crossings, whereas variable switching frequency results in all other regions.
In order to ensure safe operation of the inverter without triggering the filter's resonance, its component values must be chosen properly. (8) shows, that the filter inductance value directly affects the resulting switching frequency. Furthermore, the inductance values as well as the filter capacitor's value impact the filter's resonance:

$$f_{\mathrm{res}} = \frac{1}{2\pi\sqrt{2L_{\mathrm{o}}C_{\mathrm{o}}}} \tag{3}$$

Thus, L_{o} should be selected to set the resulting switching frequency range. Afterwards, the capacitor's values must be chosen to ensure the filter resonance lies significantly higher than the sinusoidal output frequency, as it should pass the low pass filter unaffected. Secondly, the lowest switching frequency occurring within the inverter should be significantly higher than the filter's resonance, to avoid unintended oscillations and proper filtering. Hence,

$$f_{\mathrm{s,min}} \gg f_{\mathrm{res}} \quad \text{and} \quad f_{\mathrm{f}} \ll f_{res}. \tag{4}$$

To ensure ZVS over the whole sinusoidal period, the current at the switching action at which the lower switch turns off and the upper one turns on, must be chosen properly.
The absolute value of the current required to reach ZVS during variable switching frequency operation at the switching instant is:

$$I_{\mathrm{ZVS}} = \frac{Q_{\mathrm{ZVS}}}{t_{\mathrm{dead}}} + \frac{1}{2} \cdot \frac{\frac{U_{\mathrm{DC}}}{2} - u_{\mathrm{o1}}\left(\frac{T_{\mathrm{f}}}{2}\right)}{L_{\mathrm{o}}} \cdot t_{\mathrm{dead}} \tag{5}$$

For this equation, linear current slopes are assumed. Q_{ZVS} is the absolute value of the charge that needs to be provided by the inductor current during the dead time t_{dead} to reach lossless turn-on. $-I_{\mathrm{ZVS}}$ must be present at the switching instant when the lower switch turns off, as (5) gives the absolute value. For a given dead time, the critical transition is present in case of the maximum current slope, which occurs during conduction of the upper switch. Equation (5) uses the maximum voltage across the inductor in this half-wave to ensure the ZVS condition is met over the entire half-wave. Assuming a resistive load, the maximum voltage is present near the zero crossing of the sinusoidal current at $T_{\mathrm{f}}/2$.
The conduction time of the upper switch is given by:

$$t_{\mathrm{on,S1}} = d \cdot T_{\mathrm{s}} \tag{6}$$

The duty-cycle d can be derived from the voltages present in the inverter:

$$d = \frac{u_{\mathrm{o1}}}{U_{\mathrm{DC}}} + 0.5 \tag{7}$$

To obtain the conduction time, also the switching period T_{s} must be known. If current slopes are supposed to be linear, (8) gives the switching period. The average inductor current $\overline{i_{\mathrm{Lo}}}$ over one switching period should coincide the sinusoidal output current i_1 to achieve a high-quality output current.

$$T_{\mathrm{s}} = \frac{2 \cdot (i_1 + I_{\mathrm{ZVS}})}{\frac{\frac{U_{\mathrm{DC}}}{2} - u_{\mathrm{o1}}}{L_{\mathrm{o}}} \cdot d} \tag{8}$$

If (8) delivers a switching frequency higher than the specified maximum frequency, it is clamped (fixed frequency operation). Then, (7) gives the duty cycle of the half-bridge. During fixed switching frequency operation, a higher current ripple results than required for lossless switching (ZVS) of the half-bridge switches.
Table 1 summarizes the inverter's parameters used for the theoretical study and in the practical setup. The intended application is to drive a 48V motor, but the modulation scheme itself can also be used for grid-

tied inverters. Of course, other component values as well as another switching frequency range should be used for grid applications.

Table 1: Inverter operating parameters

Parameter	Value	Parameter	Value
L_o	2.3 µH	$T_\mathrm{s,min}$	2 µs
Q_ZVS	50 nC	T_f	10 ms
U_DC	48 V	t_dead	50 ns
$\hat{u}_\mathrm{o1}$	16.9 V	φ_u	13 °
$\hat{i}_1$	11 A		

Using the described modulation scheme and the parameters given in Table 1 a simulation generates the inductor currents (i_Lo1, i_Lo2, and i_Lo3) for the three-phase inverter (Fig. 1) shown in Fig. 4 (left). Near the zero crossings of the corresponding output currents (i_1, i_2, and i_3, given in Fig. 4 (right)), the inductor currents show an increased ripple compared to the waveforms only using TCM. This stems from fixed frequency operation. Furthermore, the inductor currents and output currents prove that the two goals set initially (ZVS and sinusoidal output waveforms) are reached.

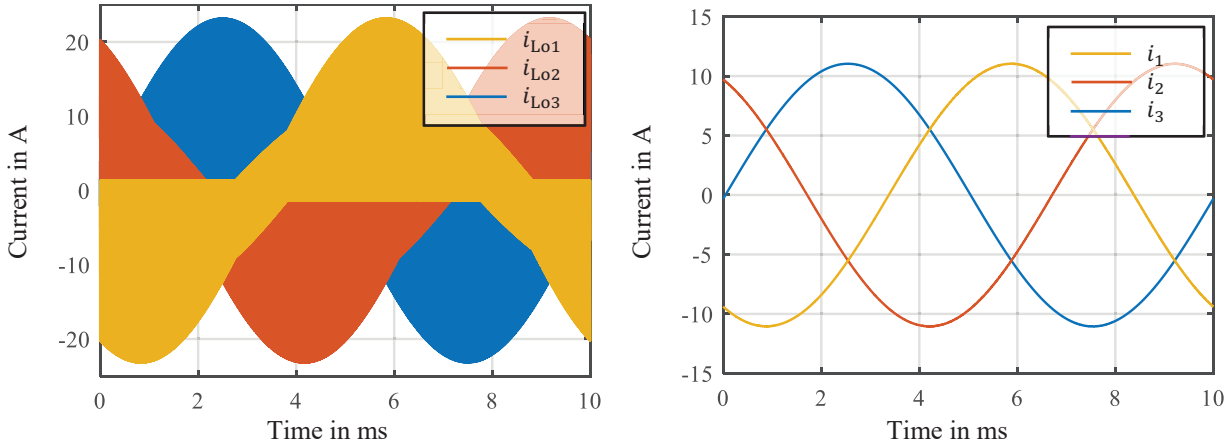

Fig. 4: Inductor current i_{Lo1}, i_{Lo2}, and i_{Lo3} gained by simulation (left); simulated output current i_1, i_2, and i_3 (right)

Analysis of Low-Frequency Behavior

To observe the low-frequency behavior e.g. for studying control algorithms of the inverter, the ripple caused by the switching actions of the half-bridge can be neglected. During fixed frequency operation of the inverter, the modulation scheme sets the averaged half-bridge voltage over one switching cycle $\bar{u}_\mathrm{hb}$ which is of rectangular shape and is defined by its duty-cycle d and the DC-link voltage U_DC. Thus, a voltage source $\bar{u}_\mathrm{hb}$ can be used to describe the modulation scheme's behavior and it behaves like a voltage mode control. Fig. 5 (left) gives the corresponding low frequency equivalent circuit. The half-bridge voltage's high frequency content is eliminated and their low frequency component passes the inverter's LC-filter and is present at the output of the inverter. From the output voltage and the load impedance Z_mot the inductor current $\bar{i}^*_\mathrm{Lo}$ and output current $\bar{i}^*_1$ result. Note that 'derived variables' ($\bar{i}^*_\mathrm{Lo}$ and $\bar{i}^*_1$) are indicated by an asterisk ('*'). This means that these variables result from the circuit topology and are not directly set by the modulation scheme. Therefore, in fixed frequency operation, the output voltage is set by the modulation scheme and the currents $\bar{i}^*_\mathrm{Lo}$ and $\bar{i}^*_1$ result from the circuit topology.

In contrast, during variable switching frequency, a comparator triggers one switching action of the half-bridge, when the inductor current reaches a certain value (I_ZVS). As a consequence, the modulation scheme programs the averaged inductor current over one switching period. Thus, it acts like a current mode control. In the low frequency equivalent circuit (see Fig. 5 (right)), this behavior is considered by replacing the inductor and modulation scheme by a current source $\bar{i}_\mathrm{Lo}$. During variable switching frequency operation, the averaged half-bridge voltage $\bar{u}^*_\mathrm{hb}$ and the output voltage $\bar{u}^*_\mathrm{o}$ result from the modulation scheme and form the derived values.

The derived values (variable with '*') match the intended ones (without '*') if an ideal converter is used, as the modulation scheme assumes an ideal behavior. In a practical setup however, the derived variables differ from the intended ones, as non-ideal behavior inevitably exists. This can be for example losses within the converter's components, load impedance deviations, the dead time of the half-bridge, inaccurate voltage measurements of the DC-link and output voltage, and deviations of the comparator thresholds from the ideal values. All these effects can lead to derived variables to differ from the intended ones.

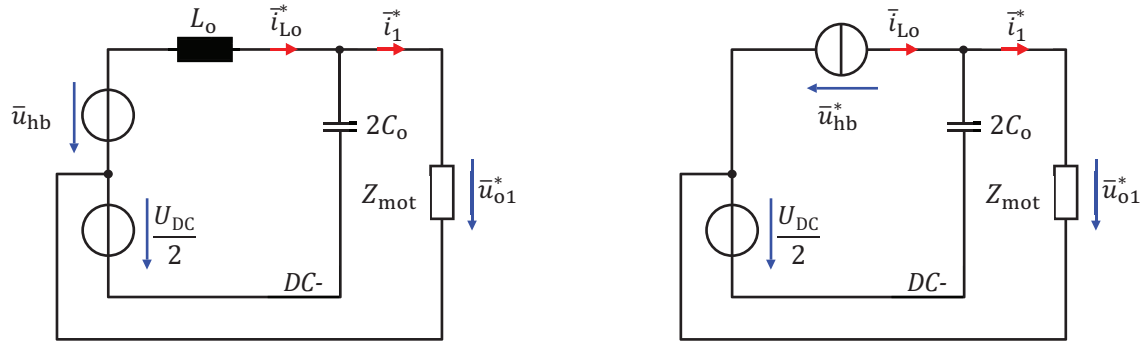

Fig. 5: Low frequency equivalent circuit for fixed switching frequency operating (left); low frequency equivalent circuit for variable switching frequency operation (right)

Experimental Setup

In order to show the applicability of the proposed modulation scheme in a real hardware, a three-phase prototype is built. The inverter uses GaN-HEMTs as half-bridge semiconductors and operates under the conditions mentioned in Table 1.

Study of the Inverter with Star Point Connection

In case the inverter's phases operate in variable switching frequency mode, they act like current mode controlled. As can be seen from Fig. 4 (left), there are time intervals, where all three phases of the inverter are in variable switching frequency operation. Thus, in an idealized inverter three current sources feed the load. As already stated in the previous analysis of the modulation scheme, in a practical setup, due to component tolerances and non-idealities, the averaged inductor currents may differ from the intended ones. Thus, the sum of all load currents at the load's neutral point (or star point) can be non-zero:

$$\sum_{k=1}^{3} i_k = i_1 + i_2 + i_3 = i_{\mathrm{YM}} \neq 0 \tag{9}$$

In Fig. 1, the connection Y to M is left open. But for the first study it is shorted to provide a return path for the residual current i_{YM} resulting from the non-ideal behavior of the modulation scheme and the inverter. With this configuration all phases of the inverter are decoupled, consequently operating independently [6] [15].

Fig. 6 (left) shows the inductor current of all three phases obtained by the practical test setup of a three-phase inverter with the load's star point connected to the midpoint of the DC-link. On the right-hand side of Fig. 6, the load currents as well as the residual current i_{YM} is depicted. Both measurements at the practical setup show that the waveforms look like the intended ones. It is worth noting that the load impedance directly couples the output current and voltage. Hence, studying only the current is sufficient. Fig. 7 shows a zoomed analysis of the star point current i_{YM}, which is less than 4 % of the output current. In order to evaluate the quality of the output waveforms, the total harmonic distortion (THD) is used for the output currents:

$$THD_k = \sqrt{\frac{\sum_{n=2}^{n_{\mathrm{OS}}} \hat{i}^2_{k,\mathrm{FFT}}(n \cdot f_{\mathrm{f}})}{\hat{i}^2_{k,\mathrm{FFT}}(f_{\mathrm{f}})}} \text{ with } k = 1 \ldots 3 \tag{10}$$

The THD delivers one number that represents the harmonic content of each current with respect to its fundamental component. n_{OS} represents the number of harmonics summed up for the calculation of the THD and is set to 500 within this study. $\hat{i}_{1,\mathrm{FFT}}$ is the fast Fourier transforms' (FFT) output for each inverter

output current. The THD for the three output currents is given in Table 2 named as ‘short’ and is below 2 %, which is relatively low. These results show that the modulation method can be used, when the star point is connected to the midpoint of the DC-link.

Table 2: THD with and without star point connection

Current	Short	Floating
$\hat{i}_1$	1.68 %	1.04 %
$\hat{i}_2$	1.67 %	1.05 %
$\hat{i}_3$	1.57 %	0.92 %

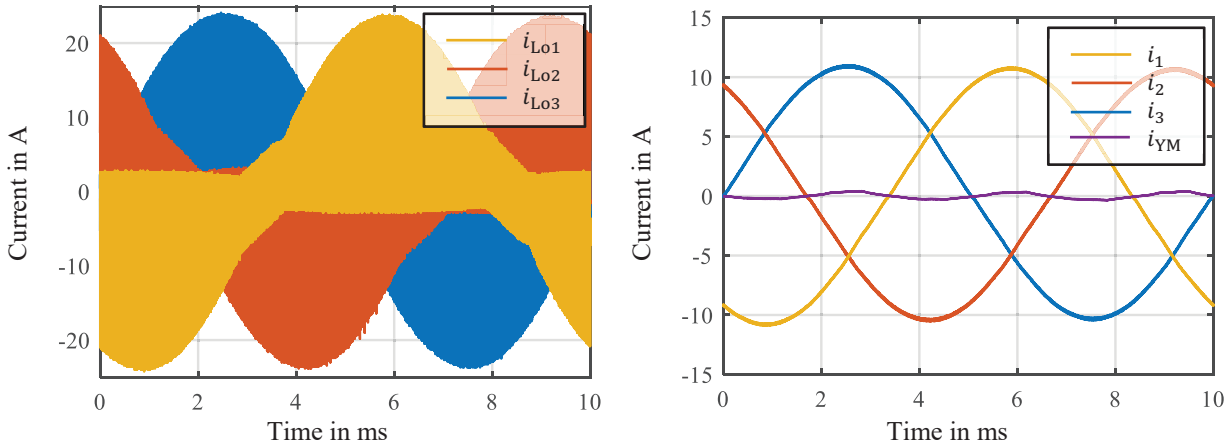

Fig. 6: Measured inductor currents i_{Lo1}, i_{Lo2}, and i_{Lo3} gained by the experimental setup with short connection between Y and M (left); measured output currents i_1, i_2, and i_3 and star point current i_{YM}(right)

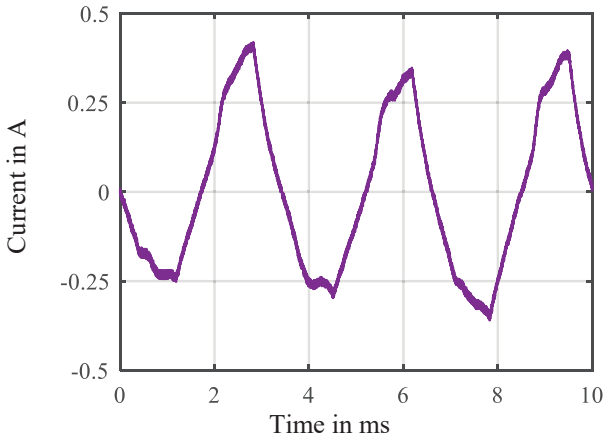

Fig. 7: Zoom of measured star point current i_{YM} with short connection between Y and M gained by the experimental setup

Study of the Inverter with Floating Star Point

Since in many applications the connection of load’s star point to the DC-link is not present, the behavior of the inverter without connection will be investigated in the second part. Therefore, the connection between Y and M is not present anymore, which means that the sum of all load currents at the load’s neutral point (or star point) is forced to be zero:

$$\sum_{k=1}^{3} i_k = i_1 + i_2 + i_3 = i_{\mathrm{YM}} = 0 \tag{11}$$

Thus, the load’s neutral point is floating and the voltage from Y to M u_{YM} can be studied. As already mentioned, due to component tolerances and non-ideal behavior of the modulation scheme and the inverter, the averaged inductor currents can differ from the intended ones. Thus, (11) is not satisfied anymore. If, in case of non-idealities, no return path from the load’s neutral point is given, as the load does not feature a

neutral point connection, the only alternative path for the currents, set by modulation i_{Lo1}, i_{Lo2}, and i_{Lo3} (see Fig. 5 (right)), are the filter capacitors. Consequently, this residual currents will distort the output voltage, as a current flowing through a capacitor will change its voltage. Of course, also in the ideal case, a current flows through the capacitors, since their voltage is ideally sine-shaped during a fundamental period. Assuming an ideal inverter, the capacitor's current can be obtained using:

$$i_{\mathrm{c},\sim} = 2 \cdot C_{\mathrm{o}} \cdot \hat{u}_{\mathrm{o1}} \cdot \omega_{\mathrm{f}} \cdot \cos(\omega_{\mathrm{f}} t + \varphi_{\mathrm{u}}) \tag{12}$$

According to (12), this current is proportional to the output voltage u_{o1}, the filter capacitance C_{o} and the frequency of the sinusoidal current. The modulation scheme takes into account this current component which occurs inherently due to the LC filter. However, if non-idealities occur in the system, additional current may flow through the capacitors:

$$i_{\mathrm{c}} = i_{\mathrm{c},\sim} + i_{\mathrm{c,res}} \tag{13}$$

As the current in this case can differ from the sinusoidal shape, the output voltage can be distorted. In order to investigate the overall influence of this additional current on the output currents and voltages an experiment needs to be performed using the same setup with opened star point connection. Therefore, the inverter's output currents are shown in Fig. 8 (left) to prove that the modulation scheme can also handle this situation.

As the waveforms are of sinusoidal shape and do not differ from the intended ones, the additional current due to the non-idealities $i_{\mathrm{c,res}}$ is negligible compared to the sinusoidal charging current $i_{\mathrm{c},\sim}$ resulting from the sinusoidal output voltage. Fig. 8 (right) shows a zoomed analysis of the voltage between Y and M. Again, the THD is evaluated. When the star point is floating, a THD of around 1% for all three currents results (see Table 2). These results demonstrate that the modulation scheme is capable of operating in applications without the load's star point connected to the DC-link.

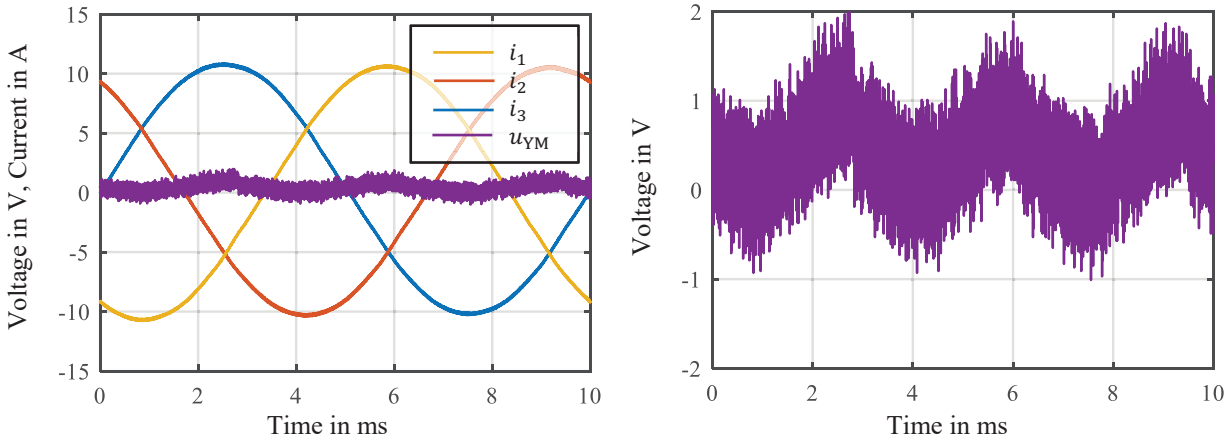

Fig. 8: Measured output currents i_1, i_2, and i_3 and star point voltage u_{YM} gained by the experimental setup with open between Y and M (left); zoom of measured star point voltage u_{YM} (right)

Conclusion

The paper relates to a hybrid modulation scheme for three-phase two-level inverters featuring two different operating modes. It comprises a combination of variable and fixed frequency to reach lossless switching for a whole sinusoidal period. After an analysis of the modulation strategy and its theoretical background, based on promising results gained by simulation, a prototype in real hardware is built. Since non-idealities and component tolerances can cause undesired behavior at the load's neutral point, this paper first conducts a study with the load's neutral point clamped to the midpoint of the DC-link. In order to use this modulation scheme also for applications without neutral point connection, a second investigation proves that this modulation scheme can also be applied at loads with a floating star point. The measurements conducted

demonstrate that smooth sinusoidal waveforms can be obtained and the modulation scheme is suitable for this applications.

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