Fault Current Capability Assessment of Low-Voltage side Inverters in Smart-Transformers

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Keywords

≪Smart-Transformer≫, ≪Overload≫, ≪Overcurrent≫, ≪Thermal model≫ ≪DC-AC converter≫

Abstract

The Smart Transformer (ST) arises as one promising solution for the modern electric grid by providing ancillary services to support AC and DC distribution grid. In this context, as the classical low-frequency transformer (LFT), the ST is prone to experience overload conditions caused by faults and peak loads. However, unlike the LFT, the overcurrent capability of the ST is further limited by the thermal time constant of the power semiconductors. Thus, since the overload operation has been only partially investigated, this paper proposes and presents a comprehensive analysis of the LV-side power converter under normal and overload conditions to estimate its overcurrent capability. For this purpose, the LV-side inverter is assessed in terms of power losses considering continuous and discontinuous modulation strategies and different power semiconductor technologies along with multiple types of cooling systems.

Introduction

The ST is a complex system comprised usually of several power converter stages and, as such, the ST is subject to a multitude of different failure modes that has to handle, e.g., internal faults (e.g. semiconductor failures, thermomechanical failures, control errors, and insulation breakdowns), MV/LV short circuit, switching transients, and non-ideal load [1–3]. Unlike the classical LFTs, STs have limited overcurrent capabilities, where the employed power semiconductors represent the main limiting factor due to their low admissible overcurrent ratios (around $1.5\times$ the nominal current for some minutes and $4\times$ for some milliseconds, while the LFT can withstand $3\times$ the rated current for several minutes [1, 4]). In other words, the safety limit of power semiconductors devices is defined by the maximum operating junction temperature $(T_{j,max})$, which indicates that the operation of ST is possible only when the power devices operate with T_j lower than $T_{j,max}$. Above $T_{j,max}$, thermomechanical failures might happen [5].

For instance, in case of a fault at the LV side, the LV-side inverter should be the last stage of the ST to trip cf. Fig. 1 (a), according to the selectivity requirements. Consequently, the LV-side inverter has to handle higher current values for some time interval until the LV-side protection devices trips (i.e. breakers, and fuse as the last resources). The current values and time interval depend on the adopted protection device and they are usually defined by the time-current curves (e.g. tripping a 1.0 MVA and 0.5 MVA fuse demands 12 s for $5\times$ the nominal current and 20 s for $2\times$ the nominal current, respectively [1]). Therefore, regardless of the adopted protection devices, without prior knowledge of the overcurrent capability information and its maximum allowable limits, the suitable design of the ST's LV-side design, including the protection scheme, is hardly achieved [6, 7].

In the literature, there is an increasing number of works focused on the ST operation [1–4, 8]. Nevertheless, the overcurrent capability of an LV-side inverter has been only partially investigated for ST applications [1, 4, 9]. Understanding that these critical operation modes are essential for inserting ST in future grids, this paper assesses the fault current capability of the LV-side inverters considering different modulation schemes and power semiconductor technologies (Si IGBT and SiC MOSFET). For this purpose, theoretical analysis of the power losses and thermal behavior are systematically addressed in a methodology considering the inherent characteristic of the power devices.

The paper is organized as follows. Section II describes the ST architecture and the investigated scenarios. Then, Section III summarizes the employed methodology and also the adopted assumptions for the overcurrent capability assessment. Next, Section IV and V present the power losses analysis of the power devices and the developed thermal network model, respectively. After that, the obtained results are discussed in Section VI. Finally, the outcomes are provided in Section VII.

LV Side Inverter of the Smart Transformer - System Description

In terms of temperature rise, the ST has the potential to handle more than the designed rated power, depending on the power semiconductor devices and overall design system [2, 4, 8]. However, it is also necessary that the system itself might provide such power. Therefore, it is considered that the MVAC stage provides the rated power (1.0 pu) while the LVDC will support the LVAC with the additional power by means of the storage system, cf. Fig.1 (a). Hence, in this scenario, the overload operation will affect only the LV-side inverter of the ST, such that the other stages are not considered in the next analysis. The DC-AC inverter, or 2L-inverter cf. Fig. 1 (b), considered in this paper is a four-leg inverter due to the requirement of a 3-phase 4-wire system in the distribution grid and for the fault identification (i.e. by using the neutral wire). The overall system's specifications are described in Table I.

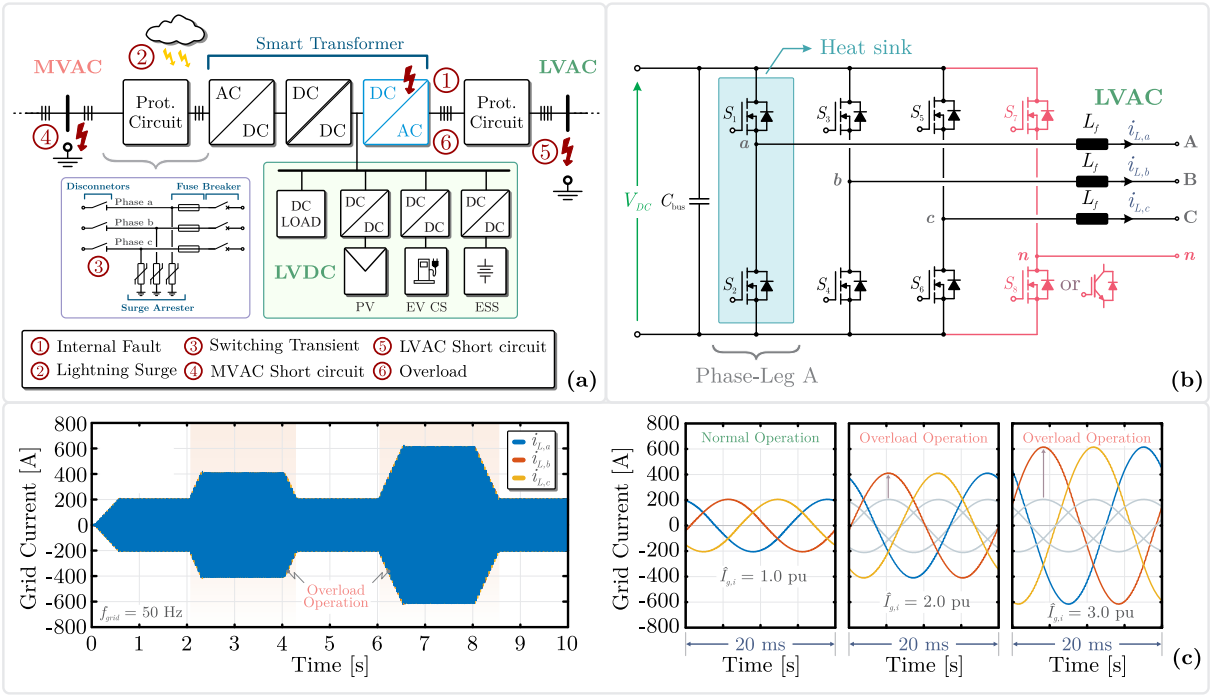

Fig. 1: (a) Electric distribution grid considering the possible abnormal operations on the smart transformer's stage [1]; (b) the four-leg 2L-inverter, and (c) current profile considering the normal operation (1.0 pu) and two different overload conditions (for 2.0 pu and 3.0 pu).

Table I: Electrical specification of the whole System considering the nominal operation.

Power	Voltage (LVAC)	Current (LVAC)	V_{DC} - LVDC	$f_{grid} = 1/T$	$f_{sw} = 1/T_{sw}$	L_f	cos(φ)
100 kVA	400 V	145 A (1.0 pu)	800 V	50 Hz	5 kHz	1.2 mH	1.0

Overcurrent Capability Assessment of the LV side Inverter

The overcurrent capabilities of the 2L-inverter, cf. Fig. 1 (b)-(c), will be investigated by using analytical models taking into account the continuous and discontinuous pulse width modulation (CPWM and DPWM, respectively) strategies, cf. Fig. 1 [10–17]. The semiconductor loss models are based on analytical conduction/switching loss equations considering their equivalent polynomial approximations obtained from the datasheets. The thermal models are based on the equivalent electrical circuits to derive the temperature's evolution. The analysis is carried for two conditions: (i) in normal and (ii) in overload operation (grid current higher than 1.0 pu). Thereby, the focus of the comparison is on the junction temperatures T_j and on the power losses of the power semiconductors. In this context, Simulink/PLECS environment is used to validate the developed models. Further, since the analysis involves complex thermal effects with limited information, the following assumptions are made to proceed with the analysis:

- The phase current presents no current ripple and hence it is perfectly sinusoidal.
- The operation of the 2L-inverter is symmetrical and balanced.
- The phase current is defined by $i_L(\omega t) = \hat{I}_L \sin(\omega t - \varphi)$, where $\hat{I}_L$ is the peak current value and φ is the phase angle (which can particularly define the power factor, i.e. $\cos\varphi$).
- The 2L-inverter is composed of three half-bridge power modules and three individual heat sinks.
- The switching energy of the power devices is phase-current dependent.
- Although power modules for high power applications are usually made of multiple chips in parallel, the analysis is performed considering a single chip (according to the available data).
- The model is only valid for junction temperatures between 25 °C (which is defined as the ambient temperature T_{amb}) and $T_{j,max}$ (which can be either 150 °C or 175 °C).
- The heat flow has a one-dimensional propagation.

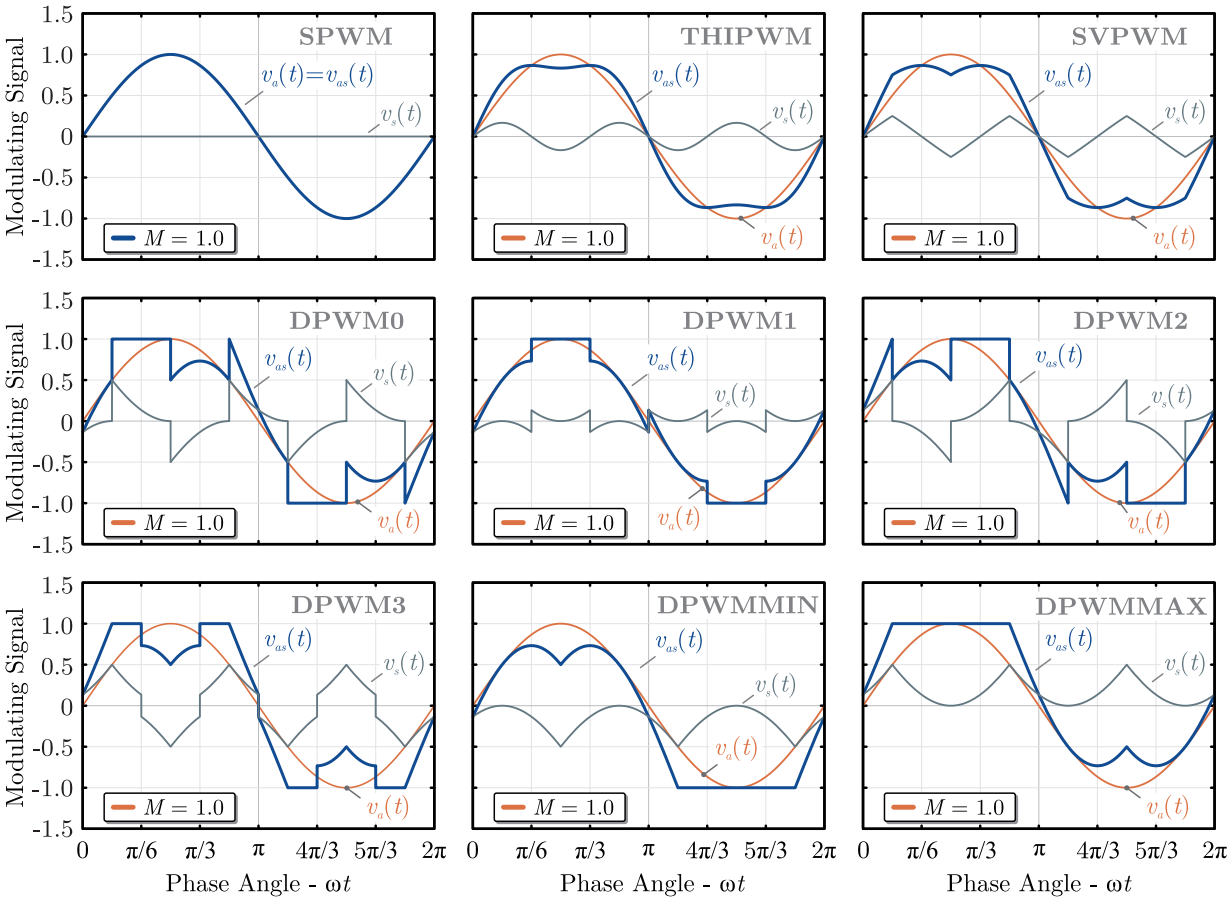

Fig. 2: Modulation strategies for phase a considering a modulation index $M = 1.0$, where v_a is the sinusoidal reference and $v_{as}(t)$ is the modulation functions, which is defined as the sum of $v_a(t)$ and the zero-sequence signal $v_s(t)$, i.e. $v_{as}(t) = v_a(t) + v_s(t)$ [10].

Power Losses Analysis of the Power Semiconductor Devices

The losses in the power devices of the 2L-inverter are comprised of both conduction losses and switching losses. These losses are highly dependent upon the power semiconductor technologies due to the different thermal dependence (i.e. Si IGBT or SiC MOSFET) and the modulation strategy due to the different duty-cycle patterns, as illustrated in Fig. 2. Therefore, the average value of the conduction losses P_{cond} for the most common power semiconductor devices can be mathematically estimated by (1).

$$P_{cond} = \frac{1}{T}\int_0^T v(i,T_j)i(\tau)d\tau \approx \frac{1}{2\pi}\begin{cases} \int_{\varphi}^{\varphi+\pi} d(\theta)\left[V_{CE}(i_L,T_j)+R_{on}(i_L,T_j)i_L(\theta)\right]i_L(\tau)d\theta, & \forall \text{ IGBT} \\ \int_{\varphi+\pi}^{\varphi+2\pi} d(\theta)\left[V_F(i_L,T_j)+R_D(i_L,T_j)i_L(\theta)\right]i_L(\theta)d\theta, & \forall \text{ APD} \\ \int_{\varphi}^{\varphi+2\pi} d(\theta)\left[R_{DS,on}(i_L,T_j)i_L(\theta)\right]i_L(\theta)d\theta, & \forall \text{ MOSFET} \end{cases} \quad (1)$$

Whereas the on-state voltage $v(i(\tau),T_j)$ is approximated around a phase-current value by means of the following thermal-dependent parameters: V_{CE} and V_F represent the forward voltage of the IGBT and anti-parallel diode (APD) respectively; R_{on} and R_D defines the dynamic resistance of the IGBT and APD respectively; and $R_{DS,on}$ represents on-resistance of the MOSFET. These parameters are defined by applying a first-order curve fitting of the on-state voltage. In Fig. 3 (a)-(d), the aforementioned electrical parameters are presented. As can be seen, they are highly dependent on the junction temperature T_j and phase current, which is assumed to be sinusoidal. Further, $d(\theta)$ indicates the duty-cycle function of a specific modulation strategy in one phase-current period. The resulting expressions obtained by using (1) are listed in Appendix (cf. Table V and VI) and depicted in Fig 4 (a)-(b).

It should be noticed that the DPWMMAX and DPWMMIN methods have unequal thermal stress on the power devices. For DPWMMAX, the high-side device of the half-bridge power module has higher conduction losses than the low-side one, while for DPWMMIN occurs the opposite. Thus, both modulation strategies are not considered in the analysis, since the overcurrent capability is inherently reduced. For the other modulation strategies, the conduction losses remain slightly similar, cf. Fig 4 (a)-(b).

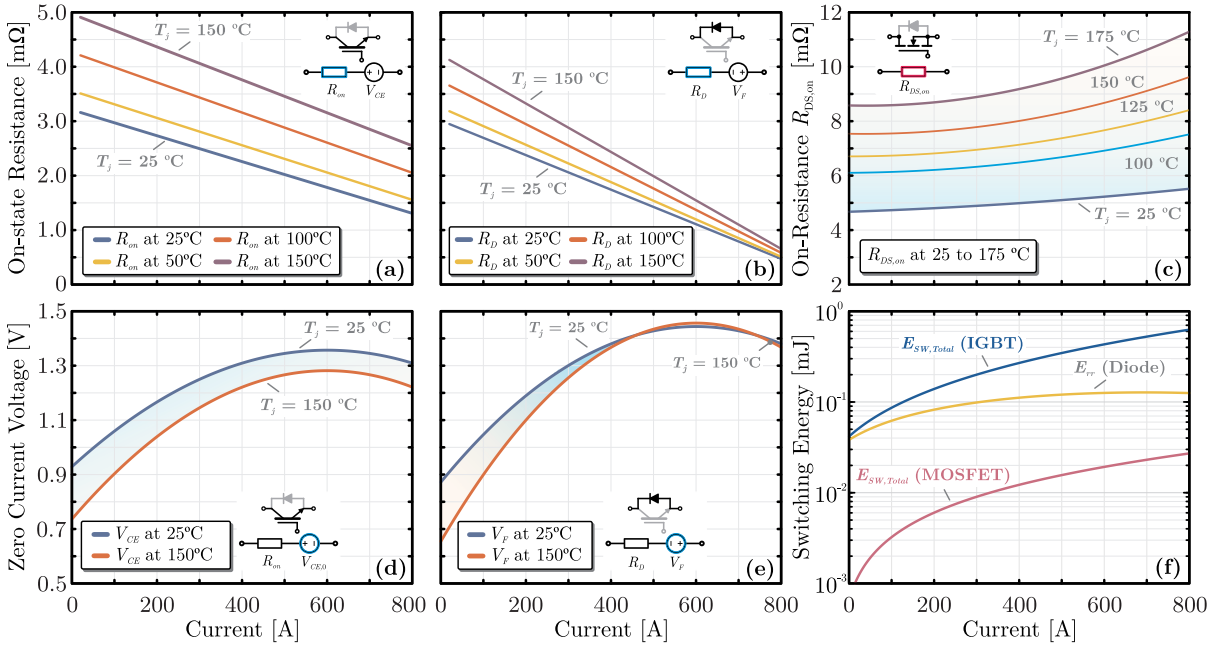

Fig. 3: Thermal-dependent parameters of the IGBT half-bridge module FF400R17KE4 and the SiC MOSFET half-bridge module CAB400M12XM3 considering the approximation of the on-stage voltage around the operating current value. Whereas (a) R_{on}, (b) R_D, and $R_{DS,on}$ represent respectively the on-resistance of the IGBT, APD and MOSFET; while (d) V_{CE} and (e) V_F represent the forward voltage of the IGBT and APD. (c) Switching energy losses extracted from the reference power module datasheets for 800 V, where $E_{sw,Total} = E_{on} + E_{off}$.

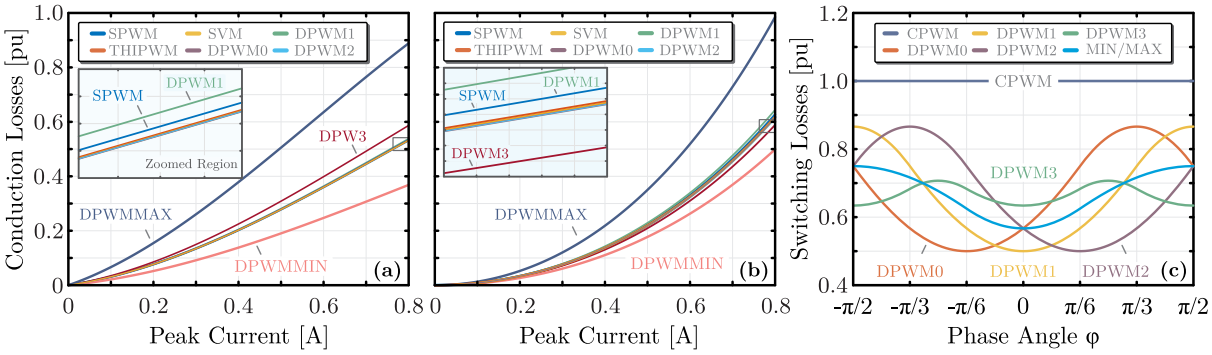

Fig. 4: Normalized conduction losses considering the following power modules for the continuous and discontinuous modulation strategies (where $P_{base} = 1.2\,\text{kW}$): (a) IGBT half-bridge module FF400R17KE4, and (b) SiC MOSFET half-bridge module CAB400M12XM3. Normalized switching losses with respect to the switching losses of CPWM (i.e. $P_{sw,CPWM}$) for: (c) the continuous and discontinuous modulation strategies.

For the calculation of the switching losses P_{sw} considering different modulation strategies (cf. Fig.1), it is assumed a linear dependency of the switching energy losses w_S with respect to the phase current $i_L(t)$, i.e. $w_S \propto k_s i_L$ (where k_s is the constant related to the voltage across the device and to turn-on/off times) [13, 18–21]. Hence, the average value of the switching loss can be calculated according to (2).

$$P_{sw} = \left[\frac{V_{DC}\left(t_{on}+t_{off}\right)f_{sw}}{4\pi}\right]\int_0^{2\pi} F_i(\theta)d\theta \approx \frac{E_{sw}}{2\pi}\int_0^{2\pi} F_i(\theta)d\theta, \quad \text{where} \quad F_i(\theta) = \begin{cases} 0, & |v_{as}| \geq 1.0 \\ |i_L|, & |v_{as}| < 1.0 \end{cases} \tag{2}$$

In (2), $F_i(\theta)$ is the switching current function, which defines generically the characteristic of the continuous and discontinuous modulation strategies. The switching current function is equal to zero during the intervals in which $v_{as}(t)$ is clamped. Otherwise, $F_i(\theta)$ is equal to the absolute value of the phase current $|i_L|$. For instance, by using the CPWM strategies, the phase currents are commutated within each switching period T_{sw} during an entire fundamental period T [10, 22]. Hence, the switching losses are the same and independent of the phase angle φ, which yields $P_{sw,CPWM} = (\hat{I}_L E_{sw})/\pi$. On the other hand, for the DPWM strategies, the switching losses are influenced by the modulation method and phase angle φ, as shown in Fig. 4 (c). As a result, by selecting DPWM strategies, it is noticed that the switching losses can be reduced up to 50 % as compared to the CPWM, cf. Fig. 4 (c).

Thermal Network Model of Half-Bridge Power Modules

A thermal network model is developed to estimate the junction temperature of the half-bridge power modules taking into account the power losses, as shown in Fig. 5 (a). For this reason, a thermal network model is required to represent the transient thermal behavior of the power semiconductor during the normal and overload conditions for different modulation strategies. as a result, the thermal network model allows the estimation of the overcurrent capability of the 2L-inverter by means of the maximum junction temperature $T_{j,max}$ and the respective time interval to reach this value (e.g. 150 °C).

Previous investigations have shown the performance advantage of the Cauer model for the thermal behavior analysis when more elements are considered along with the device's $R_{th}C_{th}$ network (e.g. TIM and heatsink) [23, 24]. In addition, Cauer models are meaningful to describe the internal structure of the device and therefore this model was selected to develop the thermal network model, cf. Fig. 5 (b) and Table II. The complete model based on the state-space representation of the Cauer model is implemented to estimate the T_j of each chip by means of (3) and (4) (cf. Appendix). Whereas, $T_{j,n+1}$ is the chip's junction temperature ($n = 0, 1, 2, 3$), T_{TIM} and T_{HS} are the temperatures on the TIM and heat sink surface respectively, and ΔT_s is the sampling period, which should be $\leq 1.0\,\mu\text{s}$.

The heat sink plays an important role to ensure a specific T_j of the power devices by supporting the heat exchange with the air (or water). For selecting a suitable cooling system, it is essential to know its thermal performance along with the thermal properties of the power semiconductor devices and the requirements given by the operation (e.g. power at normal and overload operation, T_{amb}, and $T_{j,max}$). Therefore, several types of heat sinks are included in the analysis, as shown in Fig. 5 (c)-(f).

Table II: Thermal model of the adopted power semiconductor devices considering the $R_{th}C_{th}$ network.

Device	$R_{th,1}$	$R_{th,2}$	$R_{th,3}$	$R_{th,4}$	$C_{th,1}$	$C_{th,2}$	$C_{th,3}$	$C_{th,4}$
IGBT	0.0050 K/W	0.0117 K/W	0.0429 K/W	0.0036 K/W	0.0371 J/K	0.3840 J/K	0.6328 J/K	155.30 J/K
APD	0.0152 K/W	0.0691 K/W	0.0166 K/W	0.0052 K/W	0.1346 J/K	0.3831 J/K	7.00 J/K	211.39 J/K
MOSFET	0.0588 K/W	0.0398 K/W	0.0524 K/W	-	0.1526 J/K	0.3364 J/K	2.4430 J/K	-

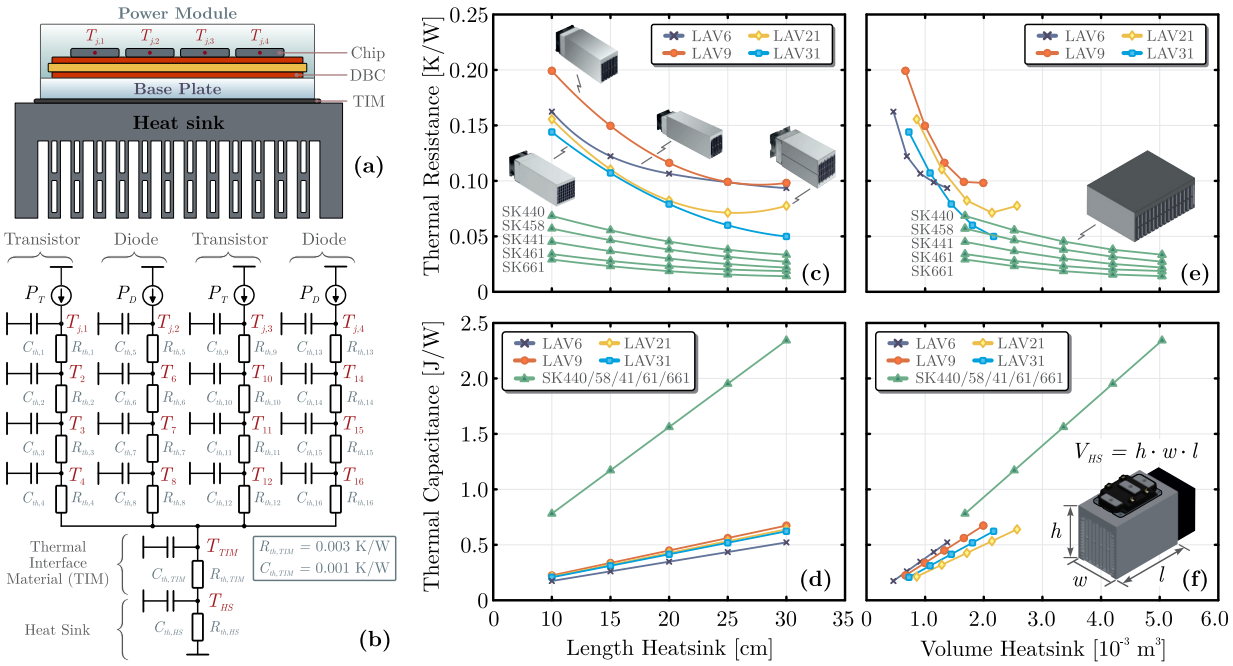

Fig. 5: (a) Cross-section view of a half-bridge power module placed on a heat sink. (b) Thermal network model of the half-bridge considering the thermal interface material (TIM) and the heat sink. Thermal resistance R_{th} and thermal capacitance C_{th} values for different heat sinks in terms of: (a)-(d) length in cm; and (e)-(f) volume in m^3.

$$
\begin{aligned}
T_{j,n+1}[k+1] &= T_{j,n+1}[k] + \left(\frac{P_{loss}[k]\Delta T_s}{C_{th,4n+1}}\right) + \Delta T_s\left(\frac{T_{4n+2}[k] - T_{j,n+1}[k]}{R_{th,4n+1}C_{th,4n+1}}\right) \quad \text{for } n = 0,1,2,3 \\
T_{TIM}[k+1] &= T_{TIM}[k] + \left(\frac{\Delta T_s T_{HS}[k]}{R_{th,TIM}C_{th,TIM}}\right) + \Delta T_s \sum_{n=1}^{4}\left(\frac{T_{j,4n}[k] - T_{TIM}[k]}{R_{th,4n}C_{th,TIM}}\right) \\
T_{HS}[k+1] &= \left(\frac{\Delta T_s T_{amb}[k]}{R_{th,HS}C_{th,HS}}\right) + \left[1 - \frac{\Delta T_s\left(R_{th,TIM} + R_{th,HS}\right)}{R_{th,TIM}C_{th,HS}C_{th,HS}}\right] T_{HS}[k] + \left(\frac{\Delta T_s T_{TIM}[k]}{R_{th,TIM}C_{th,HS}}\right)
\end{aligned}
\tag{3}
$$

Overcurrent Capability Analysis - Results and Discussion

In order to perform the overcurrent capability analysis among the different modulation strategies, power semiconductor devices, and heat sinks, the 2L-inverter was evaluated under multiple overload conditions (i.e. current values from 1.0 pu to 4.0 pu), considering the specifications of Table I. As can be seen, Fig. 6 and Fig. 7 exhibit the junction temperatures in steady-state for the SiC MOSFET and IGBT power module, respectively. Regardless of the modulation strategies, the power module based on SiC MOSFET has an overcurrent capability limited to 3.0 pu, while the IGBT counterpart has the overcurrent capability extended to 4.0 pu when the DPWM strategies are applied (and the proper cooling system is adopted).

Due to the fact that total losses of the power devices depend on the junction temperature, the results illustrated in Fig. 5 and Fig. 6 provide only the junction temperature values after reaching the thermal steady-state for each overload condition. Nevertheless, as part essential of the overcurrent capability analysis, the related time interval to achieve these temperature values should be defined by monitoring the T_j evolution with respect to the time. as a result, it is possible to estimate the time interval in which the device can withstand the overload conditions.

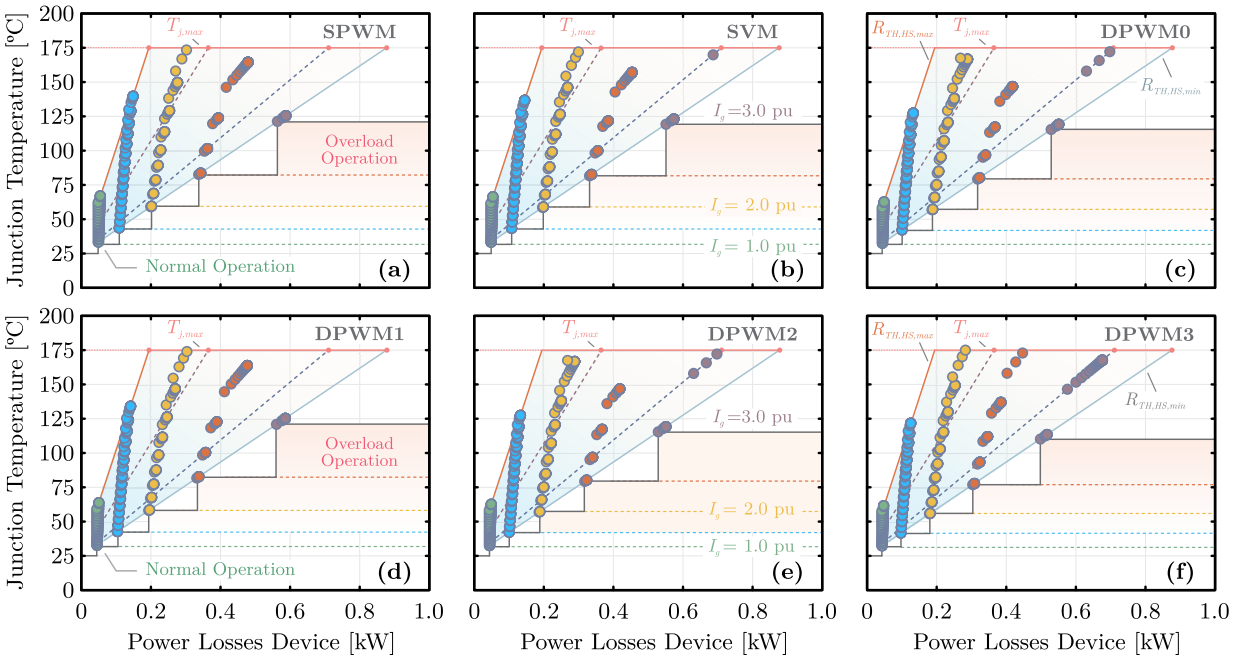

Fig. 6: Steady-state behavior of the junction temperature on the SiC MOSFET CAB400M12XM3 considering the influence of modulation strategies, semiconductor technologies, and cooling systems for different overload conditions. Where the thermal resistance varies within a range cf. Fig. 5, i.e. $R_{th,HS} \in [0.005\,\mathrm{K/W}, 0.30\,\mathrm{K/W}]$.

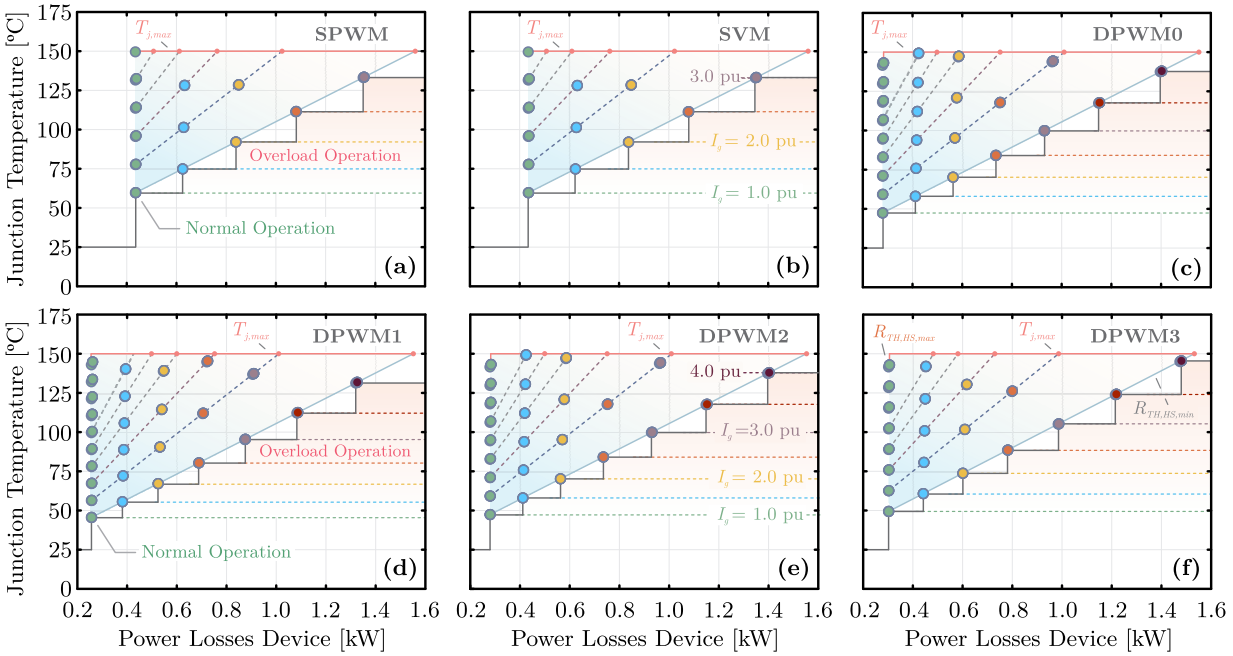

Fig. 7: Steady-state behavior of the junction temperature on the IGBT FF400R17KE4 considering the influence of modulation strategies, semiconductor technologies, and cooling systems for different overload conditions. Where the thermal resistance varies within a range cf. Fig. 5, i.e. $R_{th,HS} \in [0.005\,\mathrm{K/W}, 0.30\,\mathrm{K/W}]$.

For this purpose, in order to reduce the number of data, the number of cooling systems was reduced to only three different types, as listed in Table III. These parameters were extracted from Fig. 5 (c)-(f) to ensure $T_j \leq 75\,^{\circ}\mathrm{C}$ at normal operation (without increasing drastically V_{HS}). As a result, different heat sinks are required for each power device due to their inherent thermal characteristic. Thus, based on these values of $R_{th,HS}$ and $C_{th,HS}$, all junction temperatures are monitored systematically under three overload conditions (2.0 pu, 2.5 pu, and 3.0 pu), considering SPWM and DPWM1 strategies due to the similarity with the other ones, cf. Fig. 8 and Fig. 9. The time is accounting between the overload instant (i.e. 100 s) and the instant which the temperature reach $T_{j,max}$ (i.e. 150 °C for IGBT and 175 °C for SiC MOSFET).

Table III: Thermal resistance $R_{th,HS}$ and capacitance $C_{th,HS}$ of the adopted heat sinks for the analysis, cf. Fig. 5.

Power Device	Si IGBT Power Module			SiC MOSFET Power Module		
Heat sink	Type I	Type II	Type III	Type I	Type II	Type III
Thermal Resistance $R_{th,HS}$	0.018 K/W	0.024 K/W	0.030 K/W	0.024 K/W	0.122 K/W	0.200 K/W
Thermal Capacitance $C_{th,HS}$	1562 J/K	1170 J/K	780 J/K	1170 J/K	260 J/K	206 J/K

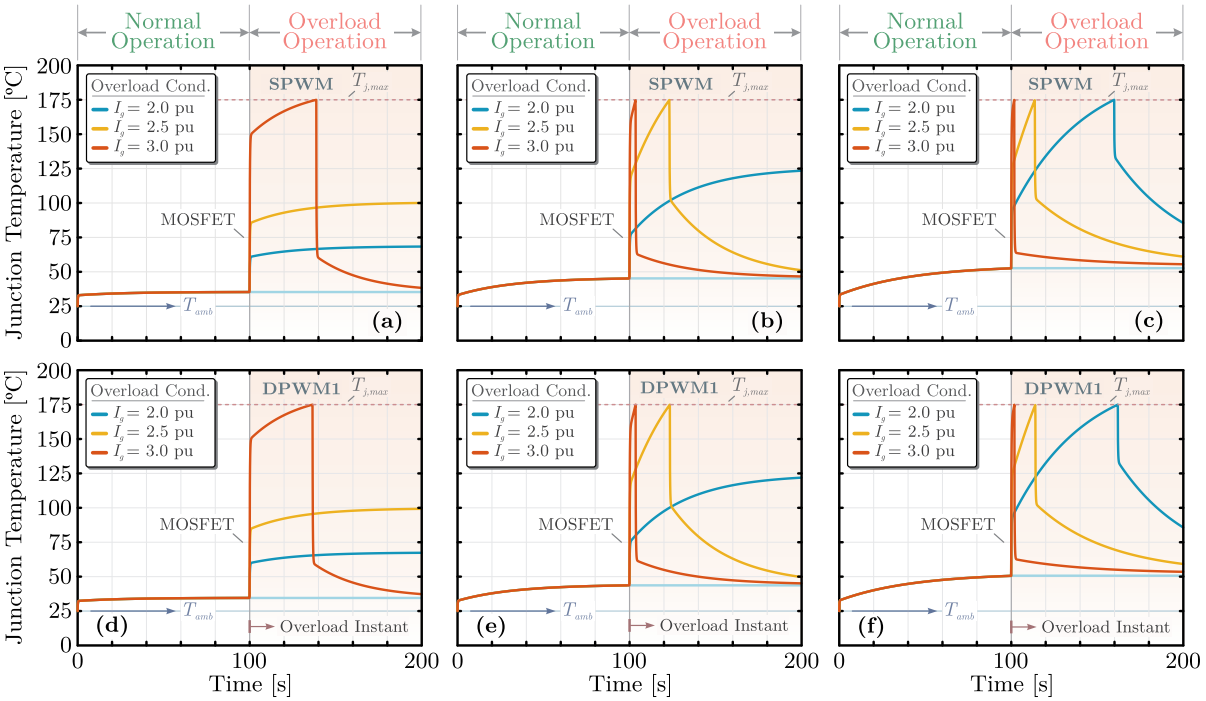

Fig. 8: Dynamic behavior of the junction temperature on the SiC MOSFET considering the influence of continuous and discontinuous modulation strategies along with different heat sinks: (a)-(d) $R_{th,HS} = 0.024\,\mathrm{K/W}$; (b)-(e) $R_{th,HS} = 0.122\,\mathrm{K/W}$; and (c)-(f) $R_{th,HS} = 0.200\,\mathrm{K/W}$. Where T_j is the average value, i.e. $\Delta T_j = 0$.

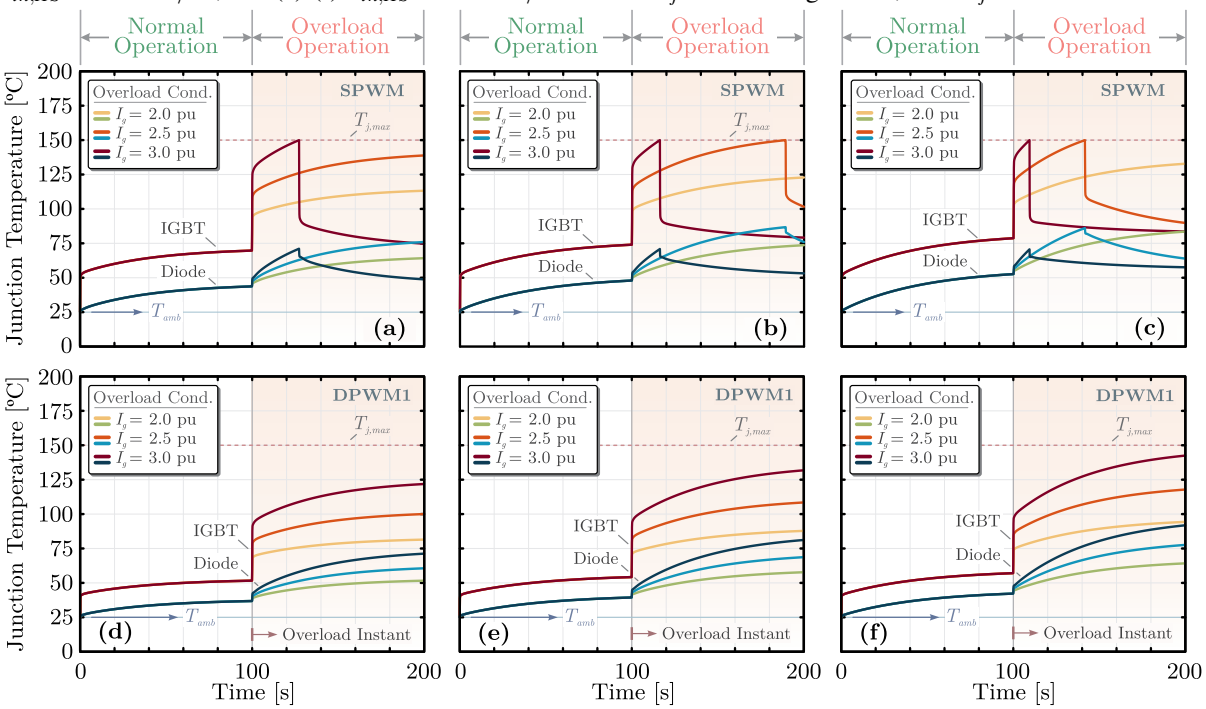

Fig. 9: Dynamic behavior of the junction temperature on the IGBT/APD FF400R17KE4 considering the influence of continuous and discontinuous modulation strategies along with different heat sinks: (a)-(d) $R_{th,HS} = 0.024\,\mathrm{K/W}$; (b)-(e) $R_{th,HS} = 0.122\,\mathrm{K/W}$; and (c)-(f) $R_{th,HS} = 0.200\,\mathrm{K/W}$. Where T_j is the average value, i.e. $\Delta T_j = 0$.

For the dynamic results, as can be seen in Fig. 8 and Fig. 9, the power module based on SiC MOSFET has an overcurrent capability almost independent of the CPWM and DPWM strategies (as already discussed). For the heat sink Type I (lowest value of $R_{th,HS}$), the power module can handle safely overloads conditions below 2.5 pu. However, for an overload condition equal to 3.0 pu, the SiC MOSFET power can operate for approximately 36.5 s before failing. With the modification of the cooling system for Type II and III, the trend is maintained. In this case, since $R_{th,HS}$ increases, the overcurrent capability is further reduced for both CPWM and DPWM strategies, cf. Fig. 8. On the contrary, the power module based on Si IGBT has an overcurrent capability highly dependent on the modulation strategy, since the switching losses are significantly higher for this power semiconductor technology (as demonstrated in Fig. 3 (e)). Therefore, the DPWM strategies can provide a notable reduction of the switching losses and the overcurrent capability can also be enlarged, as shown in Fig. 9 for the DPWM1. It should be noted that the select cooling system for the IGBT power modules has an influence on these results since the $R_{th,HS}$ values are lower as compared to those used with the SiC MOSFET power modules. Therefore, Table IV summarizes the overcurrent capability analysis by means of the time interval for reaching the $T_{j,max}$. Additionally, the analysis is extended to overload conditions of 4.0 pu, as presented in Table IV. Yet, it can be concluded that the obtained results follow the trend of the overcurrent values mentioned in the literature, i.e. some minutes for an overload of 1.5 pu and some milliseconds for 4.0 pu. The main difference is that the obtained values in this paper are numerically estimated.

Table IV: Fault Current Capability Results for the LV side Inverter.

Modulation Strategy	Power Device	Si IGBT Power Module			SiC MOSFET Power Module		
	Heat sink	Type I	Type II	Type III	Type I	Type II	Type III
SPWM	Overload Condition of 2.0 pu	>100 s	>100 s	>100 s	>100 s	>100 s	59.82 s
	Overload Condition of 2.5 pu	>100 s	89.22 s	41.42 s	≈ 100 s	23.12 s	13.60 s
	Overload Condition of 3.0 pu	27.31 s	16.22 s	9.21 s	38.72 s	3.41 s	1.71 s
	Overload Condition of 4.0 pu	95 ms	79 ms	66 ms	57 ms	45 ms	38 ms
DPWM1	Overload Condition of 2.0 pu	>100 s	>100 s	>100 s	>100 s	>100 s	61.90 s
	Overload Condition of 2.5 pu	>100 s	>100 s	>100 s	>100 s	23.40 s	13.91 s
	Overload Condition of 3.0 pu	>100 s	>100 s	≈ 100 s	36.52 s	3.51 s	1.81 s
	Overload Condition of 4.0 pu	34.24 s	23.32 s	16.27 s	55 ms	45 ms	39 ms

Comparatively, the SiC MOSFET devices have lower power losses for normal operation (in particular switching losses are the lowest portion of the losses), while the power losses of the IGBT devices are slightly higher (with the switching as the critical portion). Furthermore, from the thermal network model, the overall losses of the IGBT power module are distributed over two transistors and two APDs, while for the MOSFET counterpart the losses are mainly concentrated in two transistors. This means that the heat flow is better distributed among the $R_{th}C_{th}$ network of the IGBT power module and hence the temperature variation tends to be slower. On the other hand, for the SiC MOSFET, the temperature will be more sensitive to the power variation, which results in a higher temperature rise and hence high T_j.

Conclusion

In this paper, the LV-side inverter of the ST is assessed in terms of its overcurrent capability taking into account the continuous and discontinuous modulations strategies, the most common power semiconductor technologies, and a cooling system with a wide range of characteristics. A systematic methodology was developed to allow the overcurrent analysis for multiple parameters in several conditions. As presented by the previous results, the conduction losses are the major portion of the power losses as compared to the switching losses. However, for overload conditions, the switching losses can still impact the performance of the system, since the switching energy and the phase current have a linear dependency. Therefore, it is expected a better performance when the DPWM strategies are adopted (up to 50 % of reduction). By leveraging this behavior for the overcurrent capability, Si-IGBT power modules have demonstrated more robustness than SiC-MOSFET modules to withstand the overload conditions. For instance, in comparison to the SiC MOSFET power module, the overcurrent capability of the Si IGBT can be enlarged at least 40 % when the heat sink Type I is employed. Therefore, for the performed analysis, the IGBT power module presents more robustness than the SiC MOSFET one.

Appendix

Table V: Conduction Losses in a 2L-Inverter for the CPWM and DPWM strategies - IGBT power device.

	IGBT	Diode
SPWM	$P_{cond} = \frac{\alpha V_{CE}\hat{I}_g}{8\pi} + \frac{R_{on}\hat{I}_g^2}{24\pi}\left[3\pi + 8M\cos(\varphi)\right]$ $\alpha = 4 + \pi M\cos(\varphi)$	$P_{cond} = \frac{\beta V_F\hat{I}_g}{8\pi} + \frac{R_{on}\hat{I}_g^2}{24\pi}\left[3\pi - 8M\cos(\varphi)\right]$ $\beta = 4 - \pi M\cos(\varphi)$
THIPWM	$P_{cond} = \frac{\alpha V_{CE}\hat{I}_g}{8\pi} + \frac{R_{on}\hat{I}_g^2}{8\pi}\left[\pi + \frac{8M}{3}\cos(\varphi) - \frac{4M}{45}\cos(3\varphi)\right]$	$P_{cond} = \frac{\beta V_F\hat{I}_g}{8\pi} + \frac{R_D\hat{I}_g^2}{8\pi}\left[\pi - \frac{8M}{3}\cos(\varphi) + \frac{4M}{45}\cos(3\varphi)\right]$
SVPWM	$P_{cond} = \frac{V_{CE}\hat{I}_g}{2\pi}\left[1 + \frac{k_1 M}{32}\cos(\varphi) + \frac{\pi\sqrt{3}M}{96}\sin(\varphi)\right] +$ $+ \frac{R_{on}\hat{I}_g^2}{8\pi}\left[\pi - \frac{k_2 M}{4}\cos(\varphi) + \frac{k_3 M}{6}\sin(\varphi)\right]$ $k_1 = 7\pi + 2\sqrt{3};\quad k_2 = \sqrt{3} - 12;\quad k_3 = 2\sqrt{3} - 3$	$P_{cond} = \frac{V_F\hat{I}_g}{2\pi}\left[1 - \frac{k_1 M}{32}\cos(\varphi) - \frac{\pi\sqrt{3}M}{96}\sin(\varphi)\right] +$ $+ \frac{R_D\hat{I}_g^2}{8\pi}\left[\pi + \frac{k_2 M}{4}\cos(\varphi) - \frac{k_3 M}{6}\sin(\varphi)\right]$ $k_1 = 7\pi + 2\sqrt{3};\quad k_2 = \sqrt{3} - 12;\quad k_3 = 2\sqrt{3} - 3$
DPWM0	$P_{cond} = \frac{\alpha V_{CE}\hat{I}_g}{8\pi} + \frac{R_{on}\hat{I}_g^2}{8\pi}\left[\pi + \frac{k_4 M}{6}\cos(\varphi) + \frac{k_5 M}{6}\sin(\varphi)\right]$ $k_4 = 24 - 5\sqrt{3};\quad k_5 = 15 - 8\sqrt{3}$	$P_{cond} = \frac{\beta V_F\hat{I}_g}{8\pi} + \frac{R_D\hat{I}_g^2}{8\pi}\left[\pi - \frac{k_4 M}{6}\cos(\varphi) - \frac{k_5 M}{6}\sin(\varphi)\right]$ $k_4 = 24 - 5\sqrt{3};\quad k_5 = 15 - 8\sqrt{3}$
DPWM1	$P_{cond} = \frac{\alpha V_{CE}\hat{I}_g}{8\pi} + \frac{R_{on}\hat{I}_g^2}{12\pi}\left[\pi + \frac{3\sqrt{3}}{2} + 3M\cos(\varphi)\right]$	$P_{cond} = \frac{\beta V_F\hat{I}_g}{8\pi} + \frac{R_D\hat{I}_g^2}{6\pi}\left[\pi - \frac{3\sqrt{3}}{4} - \frac{3}{2}\cos(\varphi)\right]$
DPWM2	$P_{cond} = \frac{\alpha V_{CE}\hat{I}_g}{8\pi} + \frac{R_{on}\hat{I}_g^2}{8\pi}\left[\pi - \frac{k_5 M}{6}\sin(\varphi) + \frac{k_4 M}{6}\cos(\varphi)\right]$	$P_{cond} = \frac{\beta V_F\hat{I}_g}{8\pi} + \frac{R_D\hat{I}_g^2}{8\pi}\left[\pi + \frac{k_5 M}{6}\sin(\varphi) - \frac{k_4 M}{6}\cos(\varphi)\right]$
DPWM3	$P_{cond} = \frac{\alpha V_{CE}\hat{I}_g}{8\pi} + \frac{R_{on}\hat{I}_g^2}{6\pi}\left[\pi - \frac{3\sqrt{3}}{4} - \frac{k_6 M}{4}\cos(\varphi)\right]$ $k_6 = 5\sqrt{3} - 18$	$P_{cond} = \frac{V_F\hat{I}_g}{2\pi}\left[1 + \frac{k_7 M}{48}\cos(\varphi) + \frac{k_8 M}{48}\sin(\varphi)\right] +$ $+ \frac{R_D\hat{I}_g^2}{12\pi}\left[\pi + \frac{3\sqrt{3}}{2} + \frac{k_9 M}{4}\cos(\varphi) + \frac{7\sqrt{3}M}{4}\sin(\varphi)\right]$ $k_7 = \sqrt{3}(6-\pi) - 9\pi;\quad k_8 = \sqrt{3}(6+\pi) + 3\pi;\quad k_9 = 7\sqrt{3} - 24$
DPWMMIN	$P_{cond} = \frac{V_{CE}\hat{I}_g}{8\pi}\left[\frac{3}{2}\pi - \sqrt{3}M\cos(\varphi)\right] + \frac{R_{on}\hat{I}_g^2}{12\pi}\left[6 - \sqrt{3}\cos(\varphi)\right]$	$P_{cond} = \frac{V_F\hat{I}_g}{16\pi}\left[-\pi + 2\sqrt{3}M\cos(\varphi)\right] + \frac{R_D\hat{I}_g^2}{24\pi}\left[-12 + 7\sqrt{3}\cos(\varphi)\right]$
DPWMMAX	$P_{cond} = \frac{V_{CE}\hat{I}_g}{\pi}\left[1 - \frac{k_{10}M}{16}\cos(\varphi)\right] + \frac{R_{on}\hat{I}_g^2}{4\pi}\left[\pi - \frac{k_{11}M}{6}\cos(\varphi)\right]$ $k_{10} = 2\sqrt{3} - \pi;\quad k_{11} = 7\sqrt{3} - 12$	$P_{cond} = \frac{V_F\hat{I}_g}{\pi}\left[1 - \frac{k_{12}M}{16}\cos(\varphi)\right] + \frac{R_D\hat{I}_g^2}{4\pi}\left[\pi - \frac{k_{13}M}{3}\cos(\varphi)\right]$ $k_{12} = 2\sqrt{3} - 3\pi;\quad k_{13} = \sqrt{3} + 6$

Table VI: Conduction Losses in a 2L-Inverter for the CPWM and DPWM strategies - MOSFET power device.

Mod.	MOSFET	Mod.	MOSFET
SPWM	$P_{cond} = \frac{R_{on}\hat{I}_g^2}{8\pi}\left[\pi + \frac{8M}{3}\cos(\varphi)\right]$	**THIPWM**	$P_{cond} = \frac{R_{on}\hat{I}_g^2}{8\pi}\left[\pi + \frac{8M}{3}\cos(\varphi) - \frac{4M}{45}\cos(3\varphi)\right]$
SVPWM	$P_{cond} = \frac{R_{on}\hat{I}_g^2}{8\pi}\left[\pi - \frac{k_2 M}{4}\cos(\varphi) + \frac{k_3 M}{6}\sin(\varphi)\right]$	**DPWM0/2**	$P_{cond} = \frac{R_{on}\hat{I}_g^2}{8\pi}\left[\pi + \frac{k_4 M}{6}\cos(\varphi) + \frac{k_5 M}{6}\sin(\varphi)\right]$
DPWM1	$P_{cond} = \frac{R_{on}\hat{I}_g^2}{12\pi}\left[\pi + \frac{3\sqrt{3}}{2} + 3M\cos(\varphi)\right]$	**DPWM3**	$P_{cond} = \frac{R_{on}\hat{I}_g^2}{6\pi}\left[\pi - \frac{3\sqrt{3}}{4} + \frac{k_{14}M}{4}\sin(\varphi) + \frac{k_{15}M}{8}\cos(\varphi)\right]$ $k_{14} = 4\sqrt{3} - 7;\quad k_{15} = 5\sqrt{3} + 10$
DPWMMIN	$P_{cond} = \frac{R_{on}\hat{I}_g^2}{8\pi}\left[3\sqrt{3}M\cos(\varphi)\right]$	**DPWMMAX**	$P_{cond} = \frac{R_{on}\hat{I}_g^2}{8\pi}\left[4\pi - 3\sqrt{3}M\cos(\varphi)\right]$

$$
\begin{aligned}
T_{4n+2}[k+1] &= \left(\frac{T_{4n+1}[k]\Delta T_s}{R_{th,4n+1}C_{th,4n+2}}\right) + \left(\frac{T_{4n+3}[k]\Delta T_s}{R_{th,4n+2}C_{th,4n+2}}\right) + \left[1 - \frac{\Delta T_s\left(R_{th,4n+1} + R_{th,4n+2}\right)}{R_{th,4n+1}R_{th,4n+2}C_{th,4n+2}}\right]T_{4n+2}[k] \\
T_{4n+3}[k+1] &= \left(\frac{T_{4n+2}[k]\Delta T_s}{R_{th,4n+1}C_{th,4n+2}}\right) + \left(\frac{T_{4n+4}[k]\Delta T_s}{R_{th,4n+3}C_{th,4n+3}}\right) + \left[1 - \frac{\Delta T_s\left(R_{th,4n+2} + R_{th,4n+3}\right)}{R_{th,4n+2}R_{th,4n+3}C_{th,4n+3}}\right]T_{4n+3}[k] \\
T_{4n+4}[k+1] &= \left(\frac{T_{4n+3}[k]\Delta T_s}{R_{th,4n+1}C_{th,4n+2}}\right) + \left(\frac{T_{TIM}[k]\Delta T_s}{R_{th,4n+4}C_{th,4n+4}}\right) + \left[1 - \frac{\Delta T_s\left(R_{th,4n+3} + R_{th,4n+4}\right)}{R_{th,4n+3}R_{th,4n+4}C_{th,4n+4}}\right]T_{4n+4}[k]
\end{aligned}
\tag{4}
$$

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