Single-Arm MMC-based Converter for Transformerless Rail Interties

Simon Beck, Simon Fuchs and Jürgen Biela
LABORATORY FOR HIGH POWER ELECTRONIC SYSTEMS (HPE) / ETH ZÜRICH
beck@hpe.ee.ethz.ch / https://hpe.ee.ethz.ch

Keywords

≪AC-AC converter≫, ≪Solid-State Transformer≫, ≪Modular Multilevel Converters (MMC)≫, ≪Traction Application≫

Abstract

MMC-based converters are suitable to efficiently intertie the 50 Hz three-phase grid with the 16.7 Hz single-phase railway grid without a 16.7 Hz transformer. In this paper, a new single-arm MMC-based converter topology with a multi-winding 50 Hz transformer is presented and simulated. The findings are compared to the direct and indirect MMC variants. The comparison shows a substantial reduction of the required number of modules, switches and installed semiconductor power with the proposed topology, while the system reliability is improved at the same time.

1 Introduction

In many railway systems in Europe, a single-phase medium voltage alternating current (MVAC) system at 15 kV or 25 kV and 16.7 Hz is used for supplying the trains. Initially, the supply voltage was

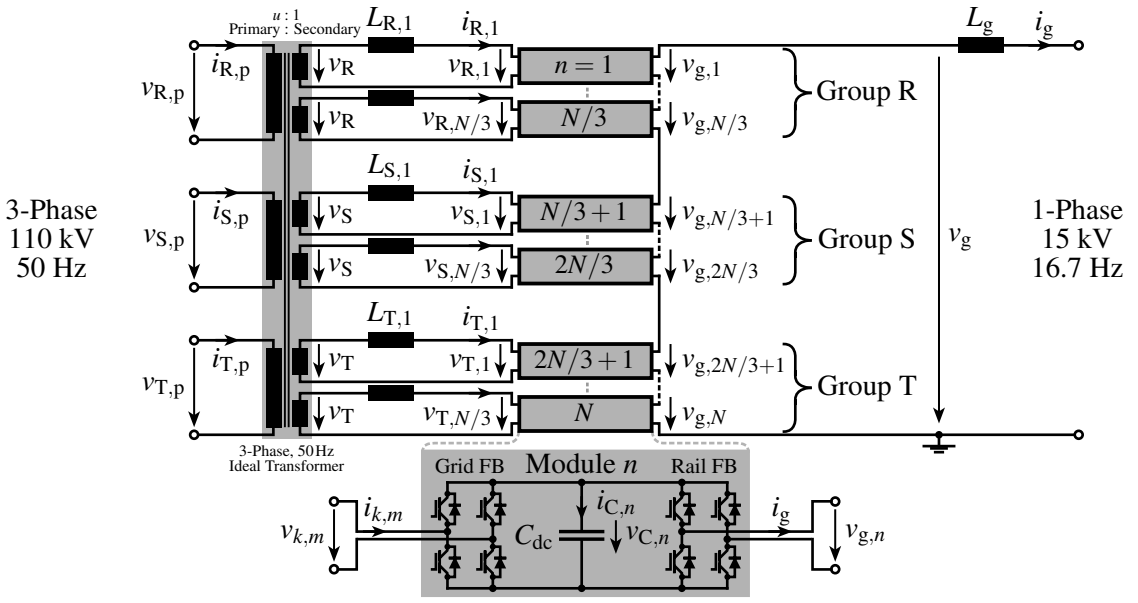

Fig. 1: Basic structure of the proposed single-arm converter with N modules consisting of back-to-back full bridges connected to a common module capacitor C_{dc} (equal for all $n \in \{1,2,\ldots,N\}$). The modules are arranged in three groups, that correspond to the grid phases $k \in \{R,S,T\}$. The PWM carrier for generating $v_{k,m}$ is phase-shifted depending on the module's position $m \in \{1,2,\ldots,N/3\}$ within each group. Thus, the current ripples of $i_{k,m}$ flowing through the combined transformer leakage and module inductance $L_{k,m}$ are cancelled out in the primary phase currents $i_{k,\mathrm{p}} = \frac{N/3}{u} i_k = \frac{1}{u}\sum_{m=1}^{N/3} i_{k,m}$. On the 16.7 Hz side, all N modules produce the catenary voltage $v_{\mathrm{g}} = \sum_{n=1}^{N} v_{\mathrm{g},n}$ using a distributed PWM algorithm.

generated by single-phase generators or from the three-phase 50 Hz national grid by rotary converters at interie stations [1]. With the advent of power electronics, 2L or 3L power electronic converters connected in between a 50 Hz transformer at the grid's side and a 16.7 Hz transformer on the railway's side were introduced. While these converters themselves feature a relatively high efficiency, the required transformers and filters reduce the overall efficiency significantly. To eliminate the 16.7 Hz transformer and filters, various systems based on modular multilevel converters (MMCs) have been proposed [2–6]. These converters have been denoted as "transformerless" interties, static frequency converters (SFCs), modular multilevel frequency converters (MMFCs), power electronic transformers (PETs), or solid-state transformers (SSTs). The indirect and direct MMCs are two interesting PET concepts for grid-to-rail interties as discussed in [3]. While the indirect MMC needs to store more energy in total than the direct MMC, the direct MMC requires more switches. In general, only relatively few publications about MMC systems designed specifically for 16.7 Hz rail interties are available.

Striving for cost effective and more compact solutions, this paper presents a new modular single-arm converter, which connects directly to the 16.7 Hz railway supply line. The new converter minimizes the number of installed semiconductors compared to other "transformerless" solutions by using multiple windings per phase in the three-phase 50 Hz transformer.

In the following, the basic converter structure and control principles are introduced in section 2. Then, the required number of modules is derived and transformer design considerations are presented in section 3.1. Thereafter, the required number of semiconductors and the required installed power of semiconductors for the proposed converter are derived in section 3.2. The required module capacitance as well as the required amount of energy stored within the converter are calculated in section 3.3. In section 3.4, semiconductor losses and reliability are investigated. Finally in section 4, key converter characteristics are compared to the direct and indirect MMC variants as discussed in [3].

2 Basic converter structure and control principles

The basic converter structure is shown in Fig. 1. A single module arm consisting of N modules is inserted between the rail catenary and ground, i.e. the train rails. Each module consists of two back-to-back full bridges sharing a common module capacitor C_{dc} charged to the nominal module voltage V_{C} on average. The back-to-back full bridges enable a bidirectional power transfer between the grid and the railway sides. Possible bypasses to short malfunctioning modules on the railway side are not shown for the sake of brevity. The full bridge connected to the 50 Hz grid side is denoted *Grid FB*. The full bridge on the 16.7 Hz rail grid side is denoted *Rail FB*. Their switching frequencies are typically in the range of a few hundred Hertz with the *Grid FBs* typically operating at a higher switching frequency as will be explained in more detail in subsections 2.1, 2.2 and 3.4. The *Rail FBs* are used to connect all N modules in series on the railway side. The catenary current i_{g} flows through all modules and is assumed to be known in the following.

On the three-phase 50 Hz side, the modules are split into three groups of $N/3$ modules each. Hence, N is a multiple of three. Each group of modules corresponds to one of the three 50 Hz phases $k \in \{R,S,T\}$. The index $m \in \{1,2,\ldots,N/3\}$ denotes the position of each module within the respective group. Every module is connected to its own secondary transformer winding via the combined transformer leakage and module inductance $L_{k,m}$. These inductances are assumed to be equal for all modules in this paper. The transformer turns ratio $u = v_{k,\mathrm{p}}/v_k$ is chosen such that the three primary-side grid voltages $v_{k,\mathrm{p}}$ are transformed to the three secondary-side phase voltages v_k at $N/3$ secondary-side windings each. Consequently, the secondary-side currents $i_{k,m}$ flowing through the modules and their associated inductances $L_{k,m}$ translate to primary-side transformer currents:

$$i_{k,\mathrm{p}} = \frac{N/3}{u} i_k = \frac{1}{u} \sum_{m=1}^{N/3} i_{k,m}, \qquad k \in \{R,S,T\} \tag{1}$$

In steady-state, the module voltages fluctuate due to the currents flowing through the module capacitors. On the railway side, all N modules in series must be able to generate the catenary voltage v_{g} at all times.

Hence, the minimal module voltage is defined by

$$V_{\mathrm{C,min}} = (1-r)V_{\mathrm{C}} = \hat{v}_{\mathrm{g,ov},n} = \frac{\hat{v}_{\mathrm{g,ov}}}{N} \tag{2}$$

Thereby, a nominal module voltage V_{C}, a maximum module voltage fluctuation $\pm rV_{\mathrm{C}}$, and a perfect PWM without overmodulation of the module output voltages are assumed. Peak values are in general denoted by the hat symbol. The highest expected overvoltage $\hat{v}_{\mathrm{g,ov}}$ must be considered instead of the nominal peak catenary voltage $\hat{v}_{\mathrm{g}}$. This overvoltage is typically specified to be 20% higher than the nominal peak catenary voltage [3].

With the nominal (and minimal) module capacitor voltage defined, the transformer turns ratio u is calculated such that the required peak module output voltage $\hat{v}_{k,m}$ on the 50 Hz side does not exceed the minimal module capacitor voltage. If the current ripples in the inductor currents are neglected, i.e. $i_{k,m} = i_k = \pm\frac{2P}{N\hat{v}_k}\cos(\omega t - \varphi_k)$, the maximum phase voltage amplitude $\hat{v}_k$ is given considering the module inductor voltages $v_{\mathrm{L},k,m}$ as

$$v_{k,m} = v_k - v_{\mathrm{L},k,m} = v_k - L_{k,m}\frac{\mathrm{d}}{\mathrm{d}t}i_{k,m} = \hat{v}_k\cos(\omega t - \varphi_k) \pm \omega L_{k,m}\frac{2P}{N\hat{v}_k}\sin(\omega t - \varphi_k) \leq V_{\mathrm{C,min}} \tag{3}$$

$$\iff \quad \hat{v}_{k,m} = \sqrt{\hat{v}_k^2 + 4\omega^2 L_{k,m}^2 P^2/(N^2\hat{v}_k^2)} \leq V_{\mathrm{C,min}} \tag{4}$$

$$\iff \quad \hat{v}_k^2 \leq \frac{1}{2}\left(V_{\mathrm{C,min}}^2 + \sqrt{V_{\mathrm{C,min}}^4 - 16\omega^2 L_{k,m}^2 P^2/N^2}\right) \quad \text{and} \quad L_{k,m} \leq \frac{V_{\mathrm{C,min}}^2}{4\omega P/N} \tag{5}$$

Here, $\varphi_k \in \{0, {}^{2\pi}/_{3}, {}^{4\pi}/_{3}\}$ indicates the phase shift between the phases $k \in \{R,S,T\}$ and only a purely active power transfer is considered in this paper, i.e. $S = P$. However, reactive energy transfer, consumption, and/or generation is generally possible. With the purely active power transfer, v_k and i_k are in phase or 180° shifted if the power flow is inverted. As on the railway side, $\hat{v}_k$ must be chosen below its theoretical maximum to account for the specified overvoltages $\hat{v}_{k,\mathrm{ov}}$ in the 50 Hz grid. It can be seen in the first inequality in eq. (5) that with a bigger inductance $L_{k,m}$, the maximum phase voltage $\hat{v}_k$ decreases. From the second inequality in eq. (5), it is also evident that the inductance is constrained by the chosen minimal capacitor voltage and the transferred power per module.

Since the catenary current i_{g} flows through all modules on the railway side and equal module output voltages $v_{\mathrm{g},n} = {}^{v_{\mathrm{g}}}/_{N}$ are generated on average on the railway side, the averaged transferred power is shared equally among all modules, i.e. (using RMS values)

$$P_{\mathrm{mod,rail}} = V_{\mathrm{g},n}I_{\mathrm{g}} = \frac{V_{\mathrm{g}}I_{\mathrm{g}}}{N} = \frac{P}{N} \tag{6}$$

Consequently, each module group transfers one third of the total power, which is expected since each group corresponds to one of the three grid phases. With the control system presented in the following sections, this is still the case when the grid voltages become unbalanced. Considering further that the averaged energy (or capacitor voltage) within each module must remain constant over time, the power balance on the grid and railway side of each module is evaluated (neglecting current ripples):

$$\frac{P}{N} = P_{\mathrm{mod,rail}} = V_{\mathrm{g},n}I_{\mathrm{g}} = P_{\mathrm{mod,grid}} = V_k I_k \tag{7}$$

In this paper, $V_k = V_{\mathrm{g},n} = {}^{V_{\mathrm{g}}}/_{N}$ is chosen, which consequently also implies $I_k = I_{\mathrm{g}}$. Using these assumptions and further assuming a perfect modulation, the current flowing through the n-th module capacitor is

$$i_{\mathrm{C},n} = |i_{k,m}| - \left|i_{\mathrm{g}}\right| = |i_k| - \left|i_{\mathrm{g}}\right| = \hat{i}_{\mathrm{g}}\left(\left|\cos\omega t - \varphi_k\right| - \left|\cos\omega_{\mathrm{g}} t\right|\right), \qquad |i_{\mathrm{C},n}| \leq \hat{i}_{\mathrm{g}} \tag{8}$$

The current $i_{\mathrm{C},n}$ consists of two rectified sinusoidal components with the respective frequencies of the grid and the railway side. Thus, the lowest frequency component of this current (and hence of the module

energy fluctuation) is twice the frequency of the unrectified current component with the lowest frequency, i.e. $2f_\mathrm{g} = 33.4\,\mathrm{Hz}$. Unlike in a traditional MMC, no circulating currents are needed to balance the module voltages because each module can control its grid side current $i_{k,m}$ individually.

The module capacitors act as a kind of modular DC-link. Hence, the grid and railway sides are decoupled and can be controlled independently as will be shown in the following subsections.

2.1 Control principles for the railway side

On the railway side, all N modules are used in series to generate the bipolar catenary voltage with $2N+1$ voltage levels:

$$v_\mathrm{g} = \sum_{n=1}^{N} v_{\mathrm{g},n} \approx v_\mathrm{g}^* = \hat{v}_\mathrm{g} \cos\left(\omega_\mathrm{g} t\right), \qquad v_{\mathrm{g},n} \in \{-v_{\mathrm{C},n}, 0\,\mathrm{V}, +v_{\mathrm{C},n}\} \tag{9}$$

To do so, a standard distributed PWM with a module sorting and balancing algorithm can be used, where all module voltages are assumed equal and constant during one PWM cycle [2, 7, 8]. Alternatively, also more advanced distributed PWM methods such as [9], where unequal but constant voltages are assumed, or an adapted version of [10] where unequal and varying module voltages are considered, can be used. These modulation schemes ensure that all modules are evenly charged or discharged (depending on the power flow direction) by the catenary current, if the converter is operated within its operating range. The catenary voltage v_g is generated based on the catenary current i_g, which is defined by the load and is assumed to be known. Since only active power is transferred, v_g is chosen to be either in phase (power transfer from grid to rail) or 180° out of phase (power transfer from rail to grid) with i_g. The catenary voltage amplitude is consequently given by the desired transferred power P using the relation $\hat{v}_\mathrm{g} = 2P/\hat{i}_\mathrm{g}$. Thus, the converter acts as a voltage source. Fig. 2a illustrates simulated catenary voltage and current waveforms. Of course, power must also be exchanged with the 50 Hz grid to not accumulate energy within the converter. This is discussed in the next section.

2.2 Control principles for the grid side

This paper's control system for the 50 Hz grid side is based on a cascaded PI-controller structure to keep the module voltages close to their nominal value V_C and the secondary-side transformer currents $i_{k,m}$ in phase (or 180° out of phase depending on the power flow direction) with the grid phase voltages v_k to achieve purely active power transfer. However, other suitable control systems are also conceivable in the future. The chosen controller structure is shown in Fig. 3. The controller structure is implemented in each module. The locally unavailable current and voltage measurements are transferred from a central entity to each module using a suitable communication protocol as described e.g. in [11]. The inner control loop consists of a relatively fast PI-controller, which is shown in red in Fig. 3. It utilizes the transformer's

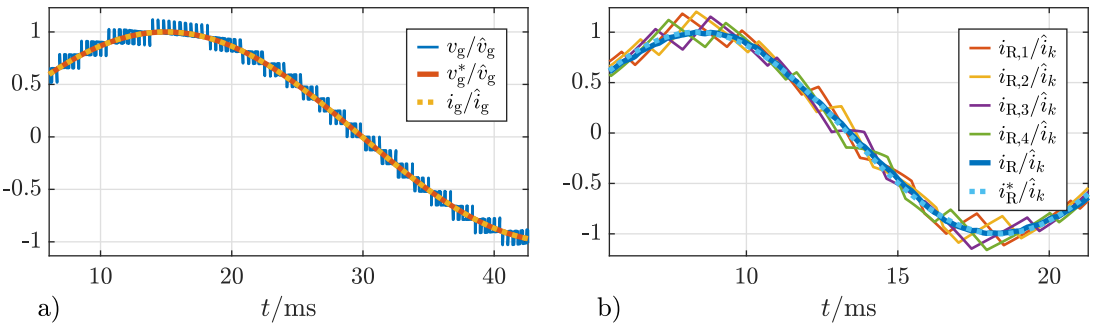

Fig. 2: Simulated voltage and current waveforms (normalized) using the system parameters given in Table I and Table II. Reference waveforms are marked by an asterisk. a) Catenary voltage and current utilizing a distributed PWM scheme that assumes equal and constant module voltages. b) Module currents and the resulting grid current (referred to the secondary transformer side) on the 50 Hz side for phase R.

leakage inductance and/or dedicated module inductors (jointly denoted as $L_{k,m}$) to control the current $i_{k,m}$ flowing through this inductance by generating a suitable voltage reference $v^*_{k,m} = v_k - v_{\mathrm{L,PI}}$ for the *Grid FB*'s voltage modulator. The PWM introduces a delay of $T_{\mathrm{PWM}}/2$ in the generated module output voltage $v_{k,m}$. To compensate this delay, a PLL is used to measure the grid voltage angle $\varphi = \omega t$. Thereafter, $\omega \cdot T_{\mathrm{PWM}}/2 = \omega/2 f_{\mathrm{PWM}}$ is added to the PLL's measured grid angle to compensate the PWM delay of $T_{\mathrm{PWM}}/2$. Hence, a time-shifted (into the future) version of the secondary-side phase voltage v_k is fed forward as stated below.

$$v^*_{k,m}(t) = v_k(t + T_{\mathrm{PWM}}/2) - v_{L,\mathrm{PI}}(t) = \hat{v}_k \cos(\omega t + \omega/2 f_{\mathrm{PWM}} - \varphi_k) - v_{L,\mathrm{PI}}(t) \tag{10}$$

Since a transformer leakage inductance is always present, the primary-side grid voltages $v_{k,\mathrm{p}} = u v_k$ are measured and transformed to the corresponding secondary-side voltages v_k using the known turns ratio u. The resulting reference value $v^*_{k,m}$ is generated using a standard 3L modulator with PWM period $T_{\mathrm{PWM}} = 1/f_{\mathrm{PWM}}$. A low PWM frequency is desirable to keep the switching losses low. However, with a constant and finite inductance $L_{k,m}$, the current ripple in $i_{k,m}$ increases as the PWM frequency decreases. To mitigate this issue, the structure of the proposed topology can be advantageously used because only the sum of one phase's secondary-side currents appears on the primary side, cf. eq. (1). Hence, the module current ripples are largely cancelled on the primary transformer side if the PWM carriers within a given group's modules are interleaved by one $N/3$-th of the PWM period. Fig. 2b illustrates this effect. Therefore, the proposed topology allows to have relatively large module current ripples. Consequently, also smaller module inductances $L_{k,m}$ and/or a relatively low PWM frequency are possible, while the primary-side currents $i_{k,\mathrm{p}} = N/3u \cdot i_k$ are almost ripple-free. On the other hand, large current ripples increase the current RMS values on the secondary-side and therefore also the conduction losses. Thus, a suitable trade-off between conduction and switching losses must be chosen. Large current ripples also make the current control more difficult since the current tracking error is not supposed to consider the current ripple. Therefore, the measured current must typically be low-pass filtered, which introduces a delay and deteriorates the control performance. Again, using the proposed topology advantageously, the primary-side transformer currents may be measured, which represent, due to the cancelled current ripples, a kind of "low-pass filtered" version of the secondary-side currents but without any filter delay. This enables a relatively fast tracking of the current reference. However, the actual module currents $i_{k,m}$ must still be measured and controlled since only controlling the primary-side currents may lead to diverging module currents, which still sum to the desired primary-side currents, cf. eq. (1). Hence, using the weighting factor w, a combination of both transformer sides' currents is used for the measured

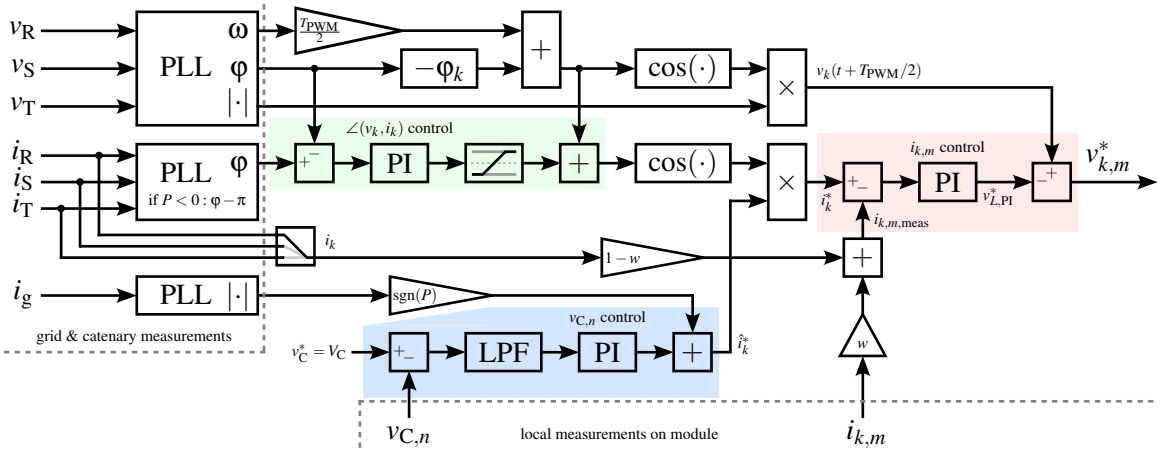

Fig. 3: Block diagram of the considered cascaded controller structure for the 50 Hz-side module currents $i_{k,m}$ and the module voltages $v_{\mathrm{C},n}$ to be implemented on each module. The power flow direction (i.e. sgn(P)) is assumed to be known. The catenary current i_g could also be measured locally on each module.

module current value, i.e.

$$i_{k,m,\text{meas}} = (1-w)i_k + w i_{k,m} \tag{11}$$

This calculated current is then used to track the module current reference i_k^*, which is defined by two outer control loops: One for the current amplitude reference $\hat{i}_k^*$ and one for the current angle reference as explained below.

The current amplitude reference's control loop consists of a relatively slow PI controller, which is used to track the module voltage reference set point $v_C^* = V_C$. This controller is not supposed to track the (unavoidable) module voltage fluctuation due to the catenary and grid currents. Instead, it is only supposed to track the average module voltage deviation from V_C over multiple grid periods. To accomplish this, the measured module voltage error is low-pass filtered (LPF) with a cross-over frequency below $2f_g = 33.4\,\text{Hz}$, cf. eq. (8). Lastly, the desired module current amplitude set point $\hat{i}_{k,\text{ff}}^* = \text{sgn}(P)\hat{i}_g$, is fed forward and added to the PI-controller's output to derive the current amplitude reference as shown in blue in Fig. 3.

Despite the compensation of the PWM delay by adjusting the measured grid angle as explained above, the inductor current will still slightly lag its reference due to the finite control performance. To counteract this in steady-state, another PLL measures the primary transformer side current angle and an additional outer PI-control loop is used to bring the voltage and current angles in phase (or 180° out of phase depending on the power flow direction) by altering the reference current's angle as shown in green in Fig. 3.

3 System design

In this section, key system characteristics are discussed and the considered simulated system for demonstrating the performance of the proposed system is specified.

3.1 Required number of modules and transformer design

The required number of modules N is primarily determined by the maximum catenary overvoltage amplitude $\hat{v}_{g,\text{ov}}$, which the series-connected converter arm must be able to block in worst case. Furthermore, N must be a multiple of three due to the arrangement in three module groups within the arm. Therefore, N can be calculated based on the system parameters given in Table I. The result is given in Table III.

To minimize the number of required secondary windings of the 50 Hz transformer, a low number of modules and a high module voltage is desirable. Just as in the MMC systems presented in [3], 4.5 kV IGBTs with a useable maximum module voltage of approximately 2.9 kV are chosen for the setup in this paper to simplify the comparison. This results in $N = 12$ modules and hence also 12 secondary-side transformer windings. Since the last module ($n = N$) is grounded at one catenary terminal, the corresponding required transformer winding insulation against ground can be calculated as $V_{\text{insul,N}} = \hat{v}_C + \hat{v}_{k,\text{ov}}$, if the voltage across the module inductor is neglected. For the remaining modules, the winding insulation requirements increase step by step by one module's maximum voltage per winding, i.e.

$$V_{\text{insul},n} = (N+1-n)\hat{v}_C + \hat{v}_{k,\text{ov}}. \tag{12}$$

However, for symmetry reasons and to achieve equal transformer leakage inductances, all windings are likely insulated for the maximum voltage $V_{\text{insul}} = V_{\text{insul,1}} = N\hat{v}_C + \hat{v}_{k,\text{ov}}$. With the power balance in eq. (7) follows that each winding must be designed to transfer one N-th of the total transferred power. Despite the required multi-winding design, the transformer can be built using a standard 3-legged core (as indicated in Fig. 1).

3.2 Semiconductor requirements

Every module consists of eight switches, hence the total number of switches is given by $N_{sc} = 8N$. All switches within a module are connected to the same DC capacitor C_{dc}. Therefore, the required voltage rating is equal to the maximum module capacitor voltage, $V_{sc} = \hat{v}_C = (1+r)V_C$. Note that the switches'

"usable" blocking or operating voltage is considered here, which is typically approximately 60% of the rated voltage. Depending on the chosen voltage safety margins on the catenary and on the grid side,

Table I: System parameters adapted from [3].

Variable	Meaning	Value(s)
$S = P$	Transferred power	15 MW
$\hat{v}_\mathrm{g}$	Rated catenary voltage amplitude	$\sqrt{2}\cdot 15\,\mathrm{kV}$
$\hat{v}_\mathrm{g,ov}$	Maximum catenary voltage amplitude	$\sqrt{2}\cdot 18\,\mathrm{kV}$
$\hat{v}_{\mathrm{g},n} = \hat{v}_\mathrm{g}/N$	Rated catenary-side module voltage amplitude	$\sqrt{2}\cdot 1.25\,\mathrm{kV}$
$\hat{v}_k$	Secondary-side phase voltage amplitude	$\sqrt{2}\cdot 1.25\,\mathrm{kV}$
$\hat{i}_\mathrm{g}$	Rated catenary current amplitude	$\sqrt{2}\cdot 1\,\mathrm{kA}$
$\hat{i}_k$	Rated secondary-side current amplitude	$\sqrt{2}\cdot 1\,\mathrm{kA}$
V_C	Nominal module capacitor voltage	$1\ldots 5\,\mathrm{kV}$
$\pm r$	Relative module voltage fluctuation	$\pm 10\,\%$
f	Grid/transformer frequency	50 Hz
f_g	Rail/catenary frequency	16.7 Hz
$\hat{v}_\mathrm{g}/\sqrt{3}$	3-ϕ-side phase voltage amplitude (direct & indirect MMC)	$\sqrt{2/3}\cdot 15\,\mathrm{kV}$
$\hat{i}_\mathrm{g}/\sqrt{3}$	3-ϕ-side phase current amplitude (direct & indirect MMC)	$\sqrt{2}\cdot 575\,\mathrm{A}$

Table II: Simulated system parameters. If not stated otherwise, parameters given Table I are used.

Variable	Meaning	Value
N	Number of modules	12
V_C	Nominal module capacitor voltage	2.6 kV
C_dc	Module capacitance	15.7 mF
$L_{k,m}$	Transformer leakage and module inductance	3.2 mH
u	Transformer turns ratios	50.8
w	Current weighting factor	0.2
f_PWM	Grid-side PWM frequency per module	400 Hz
-	Catenary-side PWM frequency per module	200 Hz
$f_\mathrm{g,PWM}$	Resulting catenary-side PWM frequency	2.4 kHz
-	IGBT model (4.5 kV, 1200 A)	Infineon FZ1200R45HL3

Table III: Comparison of intertie concepts using the parameters given in Table I. The module capacitance and the averaged stored energy for the indirect MMC are omitted, since there are various schemes to optimize these values for the three-phase side, e.g. [12–14].

Characteristic	Variable	Single-arm MMC	Direct MMC	Indirect MMC
Number of arms	-	1	6	10
Modules per arm	N	$3\left\lceil \frac{\hat{v}_\mathrm{g,ov}/3}{V_\mathrm{C,min}} \right\rceil$	$\left\lceil \frac{\hat{v}_\mathrm{g,ov}}{V_\mathrm{C,min}} \right\rceil$	$\left\lceil \frac{\hat{v}_\mathrm{g,ov}}{V_\mathrm{C,min}} \right\rceil$
Number of modules	N_total	N	$6N$	$10N$
Number of switches	N_sc	$8N$	$24N$	$20N$
Catenary voltage levels	-	$2N+1$	$2N+1$	$2N+1$
Installed blocking voltage	$V_\mathrm{sc,total}$	$8N\hat{v}_\mathrm{C}$	$24N\hat{v}_\mathrm{C}$	$20N\hat{v}_\mathrm{C}$
Semicond. current rating	I_sc	$\hat{i}_\mathrm{g}$	$\frac{2+\sqrt{3}}{6}\hat{i}_\mathrm{g}$	$\frac{1+\sqrt{3}}{6}\hat{i}_\mathrm{g}$ (3-ϕ-side) $3/4\cdot\hat{i}_\mathrm{g}$ (1-ϕ-side)
Installed semicond. power	P_sc	$8N\hat{v}_\mathrm{C}\hat{i}_\mathrm{g}$	$4(2+\sqrt{3})N\hat{v}_\mathrm{C}\hat{i}_\mathrm{g}$	$2(4+\sqrt{3})N\hat{v}_\mathrm{C}\hat{i}_\mathrm{g}$
Module capacitance	C_dc	$\approx 0.28\frac{\hat{i}_\mathrm{g}}{\omega_\mathrm{g} r V_\mathrm{C}}$	$\approx 0.28\frac{P}{2\omega_\mathrm{g} r N V_\mathrm{C}^2}$	-
Nominally stored energy	E_total	$\approx 0.14N\frac{V_\mathrm{C}\hat{i}_\mathrm{g}}{\omega_\mathrm{g} r}$	$\approx 0.14\frac{P}{2\omega_\mathrm{g} r}$	-

the switches' current ratings may vary for the two full bridges. As mentioned above, equal current amplitudes on the rail and grid side of each module are assumed in this paper. The current rating for all switches is in this case $I_{\mathrm{sc}} = \hat{i}_{\mathrm{g}}$, if additional current ripples caused by modulation are neglected. This means that all semiconductors can be of the same type and they are equally utilized in terms of blocked voltage and equally utilized in terms of conducted current. The installed semiconductor power can then be derived and it is given in Table III. Also, the chosen IGBT type is given in Table II.

3.3 Module capacitor and energy storage requirements

The required module capacitance C_{dc} is defined by the chosen module capacitor voltage level V_{C}, its allowable relative fluctuation r and the currents flowing through the module capacitors $i_{\mathrm{C},n}$. Numerically integrating the nominal current waveforms and assuming $f \approx 3f_{\mathrm{g}}$ yields a good approximation for the required module capacitance and, based on the number of modules, the nominally stored energy within the converter, which are both again given in Table III.

3.4 Semiconductor losses and reliability

As mentioned above, the proposed topology utilizes the voltage and current capabilities of every installed semiconductor well. However, the *Grid* and *Rail FBs* must be operated at different frequencies, which is explained in the following.

On the railway side, the PWM frequency per module can be kept low due to the distributed PWM scheme, which results in an effective PWM frequency that is N times higher as stated in Table II.

On the three-phase grid side, a higher PWM frequency is necessary since each module must control its grid-side current $i_{k,m}$ individually. Because relatively high current ripples of $i_{k,m}$ cancel out on the primary transformer side, the PWM frequency can still be kept relatively low. In this paper, $f_{\mathrm{PWM}} = 400\,\mathrm{Hz}$ is chosen. Nevertheless, simulations have shown that PWM frequencies as low as 300 Hz and lower are also feasible in steady-state with only minor effects on the quality of the grid currents.

To estimate the semiconductor loss factor of the IGBTs and the built-in diodes, a PLECS Blockset and Simulink simulation is used with thermal models for the IGBTs and the diodes provided by Infineon. Depending on the selected module inductance $L_{k,m}$, the voltage safety margin on the 50 Hz grid side, the PWM frequency and the controller tuning, a semiconductor loss factor in the range of 1.15%-1.4% can be achieved. The semiconductor loss factor is defined as in [3] as the ratio of the thermally lost power within the semiconductors and the total transferred power: $P_{\mathrm{sc,loss}}/P$.

MMCs and also the proposed converter are modular systems in which all modules must be operational in order for the converter to work (neglecting backup/failover modules). If a given switch (incl. driver/control/supply circuits) has an expected mean time to failure (MTTF) of $T_{\mathrm{sc,mttf}}$ and the converter system consists of N_{sc} identical switches, the expected MTTF for the entire system follows as

$$T_{\mathrm{mttf}} = T_{\mathrm{sc,mttf}}/N_{\mathrm{sc}} \tag{13}$$

It is evident that a small number of switches is desirable for the reliability of the system as the MTTF of the overall system scales with $1/N_{\mathrm{sc}}$. Thus, the proposed converter's small number of required switches has a positive impact on the expected reliability of the system. Furthermore, the proposed converter requires only three failover modules (one per module group) to provide $N-1$-redundancy.

4 Comparison to existing MMC-based rail intertie concepts

In this section, the proposed converter is compared to the direct and the indirect MMC variants discussed in [3]. The comparison is conducted using the system parameters given in Table I and the derived system characteristics given in Table III. Resulting key characteristics are shown in Fig. 4 for the considered systems according to Table I and Table II. Fig. 5 illustrates these characteristics as functions of a variable module voltage level V_{C}.

The proposed converter requires only about 17%-21% of the number of modules of the direct MMC and only about 10%-12% of the indirect MMC. Also, only about 33%-43% of the number of switches of the

direct MMC and only 40%-51% of the indirect MMC are required. This substantially reduces the number of active hardware components, such as switches, gate drives, auxiliary supplies or measurement circuits. According to eq. (13), the mean time to failure is expected to be doubled or even tripled compared to the

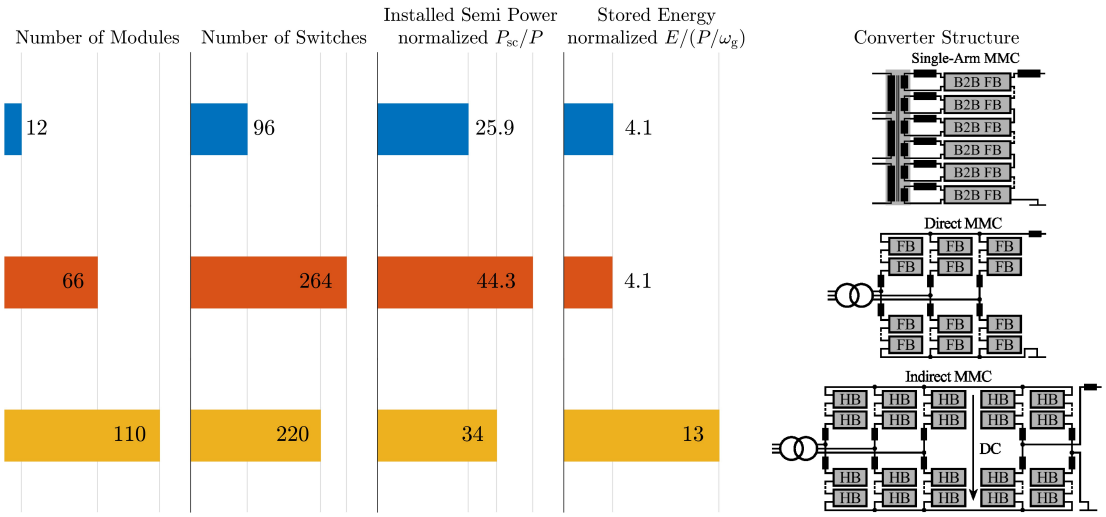

Fig. 4: Key characteristics of this paper's investigated single-arm MMC and the direct and indirect MMC concepts as discussed in [3]. Parameters are given in Table I and Table II with $V_C = 2.6\,\mathrm{kV}$. Full bridge modules are denoted "FB", while half bridge modules are denoted "HB" and back-to-back full bridge modules are denoted "B2B FB".

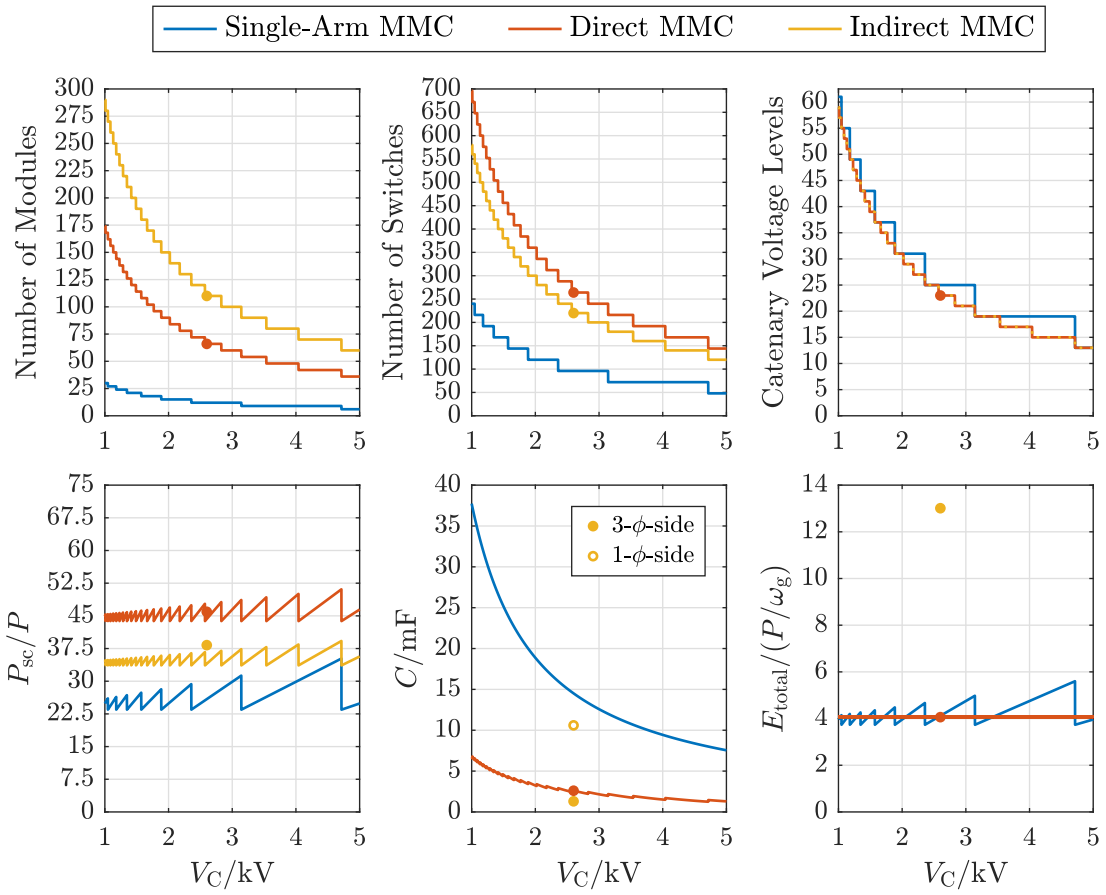

Fig. 5: Comparison of key characteristics of the direct and the indirect MMC concepts presented in [3] with the proposed converter as functions of the chosen module voltage V_C. The parameters given in table Table I are considered. Parameter values of the studied systems in [3] are marked by dots.

indirect and direct MMCs thanks to the reduced number of switches. The number of available catenary voltage levels of the proposed converter are the same or more due to the fact that the number of modules must be a multiple of three.

In the proposed converter, switches with a higher current rating are required, which is about 38% higher compared to the direct MMC and 54% higher compared to the indirect MMC on the three-phase side and 25% higher than on the indirect MMC's single-phase side. This is due to the fact that the total required semiconductor voltage blocking capability (installed blocking voltage) of the proposed system is much lower, while the same power is transferred. This is reflected in the resulting installed semiconductor power requirement, which is up to 46% lower compared to the direct MMC and up to 30% lower compared to the the indirect MMC.

Regarding the energy storage requirements, substantially less energy needs to be stored within the converter compared to the indirect MMC in [3], while the energy storage requirements are comparable to the direct MMC. This is mainly due to the fact that the indirect MMC has to buffer energy fluctuations caused by relatively low frequent 16.7 Hz arm currents and voltages on the single-phase side. In the proposed converter and the direct MMC, a combination of catenary and 50 Hz grid currents and voltages cause less energy fluctuation in the modules. Since the proposed single-arm topology requires only about 1/5 the modules compared to the direct MMC but it must store a comparable amount of energy, the module capacitances need to be about 5 times as big at equal module voltage levels.

In [3], the semiconductor loss factor of both the direct and indirect MMC systems have been calculated to be 1.1%, which is comparable to the 1.15%-1.4% derived from a comprehensive PLECS Blockset and Simulink simulation of the proposed converter using thermal IGBT and diode models by Infineon.

Since the proposed converter's modules require an insulated 50 Hz grid side voltage, a more complex transformer design is needed with $N \geq 3$ insulated secondary windings instead of only three. The power rating per winding is however only one N-th of the total transferred power instead of one third.

5 Conclusion

In this paper, a single-arm MMC-based converter is proposed as a "transformerless" solution for interconnecting the 50 Hz three-phase grid with the 16.7 Hz single-phase railway grid. It is shown that, compared to two MMC variants found in literature, only about 10%-21% of the number of modules are required. The expected mean time to failure is at least doubled thanks to 49%-72% less switches. The total installed semiconductor power is reduced by up to 46%. A disadvantage is the required more sophisticated 50 Hz transformer design. The proposed converter's feasibility is verified by simulation and thereby the semiconductor loss factor is determined to be within 1.15%-1.4% of the total transferred power.

References

[1] Steimel A.: Power-electronic grid supply of AC railway systems, 13th International Conference on Optimization of Electrical and Electronic Equipment (OPTIM 2012), pp. 16–25

[2] Lesnicar A. and Marquardt R.: An innovative modular multilevel converter topology suitable for a wide power range, 2003 IEEE Bologna Power Tech Conference Proceedings Vol. 3, pp. 6–

[3] Winkelnkemper M., Korn A., and Steimer P.: A modular direct converter for transformerless rail interties, IEEE 2010 International Symposium on Industrial Electronics, pp. 562–567

[4] Ängquist L., Haider A., Nee H.-P., and Jiang H.: Open-loop approach to control a modular multilevel frequency converter, Proceedings of the 2011 14th European Conference on Power Electronics and Applications, pp. 1–10

[5] Vasiladiotis M., Cherix N., and Rufer A.: Single-to-three-phase direct AC/AC modular multilevel converters with integrated split battery energy storage for railway interties, 17th European Conference on Power Electronics and Applications 2015 (EPE'15 ECCE-Europe), pp. 1–7

[6] Nami A., Jiang H., and Subramanian S.: A modular multilevel converter for use in a high voltage traction system, Patent WO2 018 091 065A1, Nov. 15, 2016

[7] Li Z., Gao F., Xu F., Ma X., Chu Z., Wang P., Gou R., and Li Y.: Power module capacitor voltage balancing method for a ±350-kV/1000-MW modular multilevel converter, IEEE Transactions on Power Electronics Vol. 31, pp. 3977–3984

[8] Rohner S., Bernet S., Hiller M., and Sommer R.: Modulation, losses, and semiconductor requirements of modular multilevel converters, IEEE Transactions on Industrial Electronics Vol. 57 no 8, pp. 2633–2642

[9] Fehr H., Gensior A., and Bernet S.: Experimental evaluation of PWM-methods for modular multilevel converters, 18th European Conference on Power Electronics and Applications 2016 (EPE'16 ECCE Europe), pp. 1–10

[10] Fuchs S., Beck S., and Biela J.: High output voltage precision pwm for modular multilevel converters, 19th European Conference on Power Electronics and Applications 2017 (EPE'17 ECCE Europe), pp. 1–10

[11] Rietmann S., Fuchs S., Hillers A., and Biela J.: Field bus for data exchange and control of modular power electronic systems with high synchronisation accuracy, 2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia), pp. 2301–2308

[12] Korn A. J., Winkelnkemper M., and Steimer P.: Low output frequency operation of the modular multi-level converter, 2010 IEEE Energy Conversion Congress and Exposition, pp. 3993–3997

[13] Engel S. P. and Doncker R. W. D.: Control of the modular multi-level converter for minimized cell capacitance, Proceedings of the 2011 14th European Conference on Power Electronics and Applications, pp. 1–10

[14] Ilves K., Antonopoulos A., Harnefors L., Norrga S., Ängquist L., and Nee H.-P.: Capacitor voltage ripple shaping in modular multilevel converters allowing for operating region extension, IECON 2011 - 37th Annual Conference of the IEEE Industrial Electronics Society, pp. 4403–4408