

Experimental Verification of Maximum Operating Frequency for a SiC-MOSFET in Class-D ZVS inverter

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Abstract-- This paper experimentally verified a previously proposed analytical model of maximum operating frequency of class-D ZVS inverter. The proposed model included the linearized drain-source parasitic capacitance and was usable at any duty ratio. The verification of the model was once conducted by simulation with a 650V/30A SiC-MOSFET spice model before, and in this paper the experimental verification was further conducted by PCB circuit, resulting in good consistency.

Index Terms—Class-D ZVS inverter, Maximum operating frequency, drain-source parasitic capacitance, any duty ratio, experimental verification.

I. INTRODUCTION

The class-D inverter [1]–[5] is a classical circuit topology to convert DC to AC. The developed wide band-gap power semiconductor enables the class-D inverter to operate in MHz frequency. The high frequency brings about high-power density meanwhile causing high switching loss. By implementing zero-voltage-switching (ZVS) technology [6]–[10], the switching loss can be reduced a lot. It is possible to reconcile the high-power density with the low switching loss if the class-D inverter operated at its maximum frequency under the ZVS condition. As there are a lot of parameters related to ZVS designing, the frequency limitation is difficult to find out. Thus, it is necessary to build an analytical model of the maximum operating frequency of the class-D ZVS inverter to optimize the process of maximum frequency design.

For implementing ZVS in the class-D inverter, the shunt capacitance is a key element. Normally, the shunt capacitance is composed of the sum of the nonlinear parasitic capacitance inside the device and the linear external capacitor outside the device. In high frequency, the required total shunt capacitance becomes small so that the nonlinear parasitic capacitance takes up a certain proportion of the sum and cannot be neglected anymore.

There are some previous researches about the analysis model of maximum operating frequency of class-D ZVS inverter. In [11], the model was built under the precondition of duty=0.25 and the nonlinear parasitic capacitance was neglected. Thus, it lacked accuracy in high-frequency design and cannot be utilized for other duties. In [12], the model was built with any duty ratio and analytically verified, but the nonlinear parasitic capacitance was still neglected. Thus, it lacked accuracy in high-frequency design. In [13], the model was built within

the nonlinear parasitic capacitance under the precondition of duty=0.25. It can be used for design in high-frequency but also cannot be utilized for other duties. Furthermore, for all previous models above, there were no simulated and experimental verifications for the models. Generally, there is still no analytical model including both the nonlinear parasitic capacitance and any duty ratio, with simulated and experimental verification.

Based on the previous research, the paper [14] proposed a new analytical model including both nonlinear parasitic capacitance and any duty ratio simultaneously. As it was difficult to combine the nonlinear parasitic capacitance directly with any duty ratio when building the model, the capacitance was first linearized through the charged-related equation and then added to the previous model with any duty ratio in [12]. The linearized capacitance was a function of input DC voltage. The function showed that high input DC voltage resulted in low linearized capacitance, which was an important characteristic for the analysis of the model. The analytical result of the model showed that at a fixed input DC voltage and load impedance, the maximum operating frequency under ZVS condition can always be obtained at 0° output current phase angle and 0.25 duty. If the input DC voltage changes higher, the maximum operating frequency also increases, and the absolute maximum operating frequency can be obtained when the input DC voltage reaches the highest value, which was determined by the break-down voltage of the switch. As for the verification of the analytical result, a 650V/30A SiC-MOSFET was utilized. The nonlinear drain-source parasitic capacitance of the SiC-MOSFET was accurately modeled, linearized, and substituted into the model. The SPICE simulation verified the result at 400V input voltage, and 50Ω load impedance with good agreement.

In this paper, further verification is conducted by simulation in conditions of 200V and 300V input voltage with 50Ω load impedance. The simulated results show that at each fixed input voltage and load impedance, the maximum operating frequency can always be obtained at 0° output current phase angle and 0.25 duty, and the maximum operating frequency at 300V input voltage is higher than that of 200V input voltage. Besides, a PCB circuit of the class-D ZVS inverter is fabricated with the 650V/30A SiC-MOSFET for the verification. The experimental results show good consistency with the results of analysis and simulation.

II. CLASS-D ZVS INVERTER

A. Circuit

A typical circuit of the class-D ZVS series-resonant inverter is shown in Fig. 1. The inverter is mainly composed of a DC voltage source V_1 , two identical switching MOSFETs M_1 and M_2 which are connected in half-bridge, a series-resonant tank L_r-C_r , and a load resistance R . Each switch contains a nonlinear parasitic capacitance C_{ds} and a parasitic anti-parallel body-diode D . Outside the switch, an extra linear capacitor is connected in parallel with the drain-source. For ZVS operation, shunt capacitance and inductive load are necessary. The nonlinear parasitic capacitance and the extra linear capacitor form the shunt capacitance. And the inductor L_x makes the load impedance inductive.

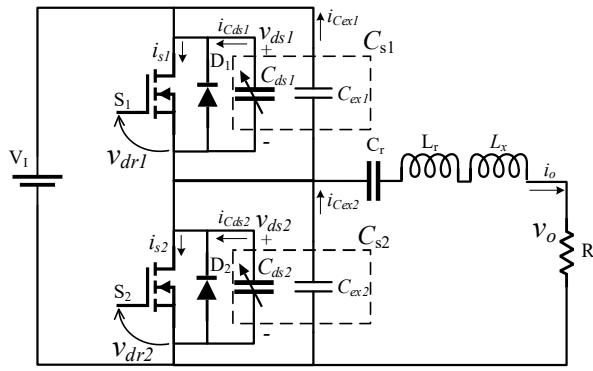


Fig. 1. Typical class-D inverter topology

B. ZVS Operation

Fig. 2. shows the nominal waveforms of the class-D ZVS inverter. In the figure, $\omega=2\pi f$ expresses the angular frequency and $\theta=\omega t$ expresses the angular time. The switching time is assumed to be zero. The input DC voltage is V_1 . The switches are driven by a set of pluses v_{dr1} and v_{dr2} with duty ratio D at frequency f respectively. To achieve ZVS operation, a deadtime t_d between the gate-driving voltages is necessary. During the deadtime t_d , both switches are off, the shunt capacitance becomes a part of the resonant circuit. The output current charges one shunt capacitance and discharge the other. In order to discharge the shunt capacitance during t_d , the load impedance should be inductive. Specifically, the ZVS operation principle can be explained by time sequence as below:

At $\theta=0^\circ$, the phase of output current i_o lags behind by φ the inductive load.

From $\theta=0^\circ$ to $\theta=\varphi$, i_o is minus and flows through D_1

From $\theta=\varphi$ to $\theta=2\pi D$, i_o turns plus and flows through S_1

From $\theta=2\pi D$ to $\theta=\pi$, i_o charges C_{s1} and discharges C_{s2}

From $\theta=\pi$ to $\theta=\pi+\varphi$, v_{s2} is completely discharged to 0V, i_o flows through D_2 , and D_2 keeps on.

During $\theta=\pi$ to $\theta=\pi+\varphi$, if the rising up of the gate-driving voltage arrived, the switch would be turned on at a zero drain-source voltage, which realizes the ZVS. The time interval can be regarded as the ZVS time allowance.

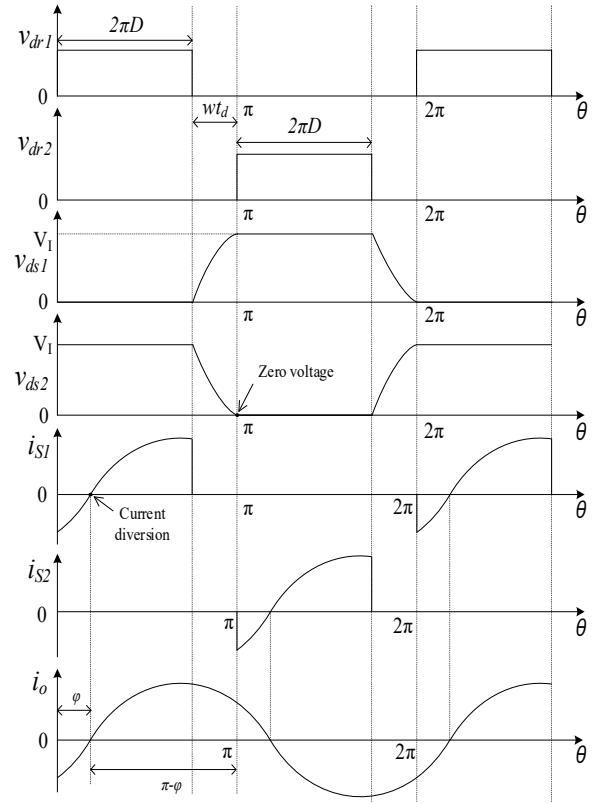


Fig. 2. Nominal waveforms of class-D ZVS inverter

III. NONLINEAR PARASITIC CAPACITANCE LINEARIZATION

A. C_{ds} Modeling

The typical definition equation of the nonlinear drain-source parasitic capacitance C_{ds} can be expressed by (1), where C_{j0} is the capacitance of C_{ds} at $v_{ds}=0V$, V_{bi} is the built-in potential determined by the material of the switch, and m is the grading coefficient.

$$C_{ds}(v_{ds}) = \frac{C_{j0}}{(1 + \frac{v_{ds}}{V_{bi}})^m} \quad (1)$$

According to [11], the expression can be mathematically transformed into (2), where $C_{DS}(V_{DS})$ is a specific value of capacitance at a specific drain-source voltage V_{DS} . For a specific switch, the value of $C_{DS}(V_{DS})$ usually can be read from the datasheet made by the manufacturer.

$$C_{ds}(v_{ds}) = C_{DS}(V_{DS}) \sqrt{\frac{V_{DS} + V_{bi}}{v_{ds} + V_{bi}}} \quad (2)$$

B. C_{ds} Linearization

As it is difficult to directly apply the nonlinear parasitic capacitance to the frequency model, the nonlinear C_{ds} is proposed to be linearly transformed through the charge-related equation. When the C_{ds} is charged to V_1 , the charge stored in the C_{ds} can be expressed as:

$$Q_{ds}(V_1) = \int_{-V_{bi}}^{V_1} C_{ds}(v_{ds}) dv_{ds} \quad (3)$$

If there is a linear capacitance C_{dseq} existed and satisfied (6), when it is charged to V_I , the charge-related equation will be

$$Q_{ds}(V_I) = C_{dseq} V_I \quad (4)$$

Combining (4) with (3) and (2), the nonlinear C_{ds} can be transformed into an equal linear capacitance as (5), for V_{bi} , $C_{Ds}(V_{DS})$ are constants in the function, it is obvious that the dependent variable C_{dseq} is a monotone decreasing function of the independent variable V_I , which means with the increase of V_I , the C_{dseq} decreases.

$$\begin{aligned} C_{dseq}(V_I) &= \frac{1}{V_I - V_{bi}} \int_{V_{bi}}^{V_I} C_{ds}(v_{ds}) dv_{ds} \\ &= \frac{2C_{DS}(V_{DS})}{V_I} \sqrt{V_{DS} + V_{bi}} \sqrt{V_I + V_{bi}} \end{aligned} \quad (5)$$

C. Influence on Phase of Waveform from Linearization

In [13], the waveform equation of the switch's drain-source voltage with nonlinear parasitic capacitance under class-D ZVS condition was derived as a function of V_I/V_{bi} . The waveforms were mathematically simulated by two conditions which were $V_{bi} \rightarrow \infty$ (which means the C_{ds} is set to be linear) and $V_{bi}=40$ (which means the C_{ds} is set to be nonlinear) respectively. The result clarified that the nonlinearities never affect the phase angle of the switch's drain-source voltage as well as that of the output current.

IV. CIRCUIT MODELING

A. Assumptions

In this section, the analytical model of the class-D inverter in ZVS operation is given by mathematical expressions with the proposed model of nonlinear parasitic capacitance. The equivalent circuit for analysis is shown in Fig. 3. and it is based on the following assumptions:

- 1) The shunt capacitances are formed by both the nonlinear parasitic capacitance and the linear external capacitor. And the nonlinear parasitic the linearized in the equivalent circuit for modeling.
- 2) The switch is assumed ideal in this model, meaning zero-switching time, zero on-resistances, and infinite off-resistances.
- 3) The driving voltages are ideal symmetric square waveforms, and their duty ratios range by $0 \leq D \leq 0.5$.
- 4) The loaded quality factor Q of the series resonant filter $L-C-R$, which is defined as

$$Q = \frac{\omega L}{R} \quad (6)$$

is sufficiently high, so that the output current can be assumed as an ideal sinusoidal wave as

$$i_o = \frac{V_m}{R} \sin(\omega t - \varphi) = I_m \sin(\omega t - \varphi) \quad (7)$$

where V_m and I_m are the amplitudes and the φ is the initial phase angle that the output current lags behind

the output voltage which is shown in Fig. 2.

- 5) Only the fundamental-frequency component passes through the resonant filter. It is well known that the resonant filter should be inductive for achieving the ZVS condition. Therefore, the resonant inductance L is divided into L_r and L_x virtually. The resonant filter L_r-C_r is an ideal filter at the operating frequency f , that is, $f = 1/2\pi\sqrt{L_r C_r}$. Additionally, L_x yields a phase shift of the output current.
- 6) All the components have no parasitic components.
- 7) The switches' voltages satisfy the ZVS operation result which are

$$v_{ds1}(2\pi) = 0 \quad \text{and} \quad v_{ds2}(2\pi) = V_I \quad (8)$$

$$v_{ds1}(\pi) = V_I \quad \text{and} \quad v_{ds2}(\pi) = 0 \quad (9)$$

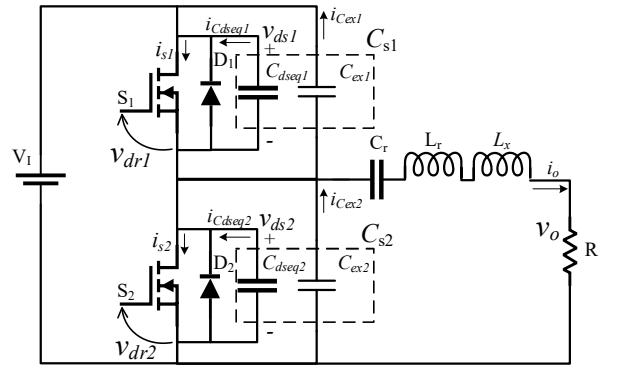


Fig. 3. Equivalent circuit for analysis

B. Waveform Expressions Derivation

Based on assumptions 3) and 4), and the operating waveform shown in Fig. 2. By KCL, the basic equation can be expressed as:

$$i_{s1} - (i_{Cdseq1} + i_{Cex1}) - [i_{s2} - (i_{Cdseq2} + i_{Cex2})] = i_o = I_m \sin(\theta - \varphi) \quad (10)$$

For $0 < \theta \leq 2\pi D$, switch S_1 is on, and switch S_2 is off, so the switch voltages are given as

$$v_{ds1} = 0, v_{ds2} = V_I \quad (11)$$

As there is no current flows through the switch S_2 , and no currents are charged or discharged through the capacitance C_{s1} and C_{s2} , thus

$$i_{s2} = i_{Cdseq1} = i_{Cdseq2} = i_{Cex1} = i_{Cex2} = 0 \quad (12)$$

Substituting (12) into (10), it can be obtained that

$$i_{s1} = i_o = I_m \sin(\theta - \varphi) \quad (13)$$

For $2\pi D < \theta \leq \pi$, which is the dead time interval, both S_1 and S_2 are off. Therefore, the switch currents are

$$i_{s1} = i_{s2} = 0 \quad (14)$$

Additionally, the voltage relationship between the two switches' s is

$$v_{ds2} = V_I - v_{ds1} \quad (15)$$

From (10) and (14), it can be obtained that

$$-i_{Cdseq1} - i_{Cex1} + i_{Cdseq2} + i_{Cex2} = i_o = I_m \sin(\theta - \varphi) \quad (16)$$

According to the defined formula of capacitance

current, it can be obtained from (16) that

$$-\omega(C_{dseq1} + C_{ex1})\frac{dv_{ds1}}{d\theta} + \omega(C_{dseq2} + C_{ex2})\frac{dv_{ds2}}{d\theta} = I_m \sin(\theta - \varphi) \quad (17)$$

Rearranging (17) by using (15)

$$\omega(C_{dseq1} + C_{ex1} + C_{dseq2} + C_{ex2})\frac{dv_{ds2}}{d\theta} = I_m \sin(\theta - \varphi) \quad (18)$$

Define the total sum of the shunt capacitance as

$$C_{st} = C_{dseq1} + C_{ex1} + C_{dseq2} + C_{ex2} \quad (19)$$

Hence

$$\omega C_{st} dv_{ds2} = I_m \sin(\theta - \varphi) d\theta \quad (20)$$

Because of $v_{ds2}(2\pi D) = V_I$, it can be obtained by solving indefinite integral for both sides

$$\omega C_{st} \int_{V_I}^{v_{ds2}} dv_{ds2} = I_m \int_{2\pi D}^{\theta} \sin(\theta - \varphi) d\theta \quad (21)$$

Yields,

$$\begin{aligned} v_{ds1} &= V_I - v_{ds2} = \frac{I_m}{\omega C_{st}} [\cos(\theta - \varphi) - \cos(2\pi D - \varphi)] \\ &= \frac{V_m}{\omega C_{st} R} [\cos(\theta - \varphi) - \cos(2\pi D - \varphi)] \end{aligned} \quad (22)$$

For $\pi < \theta \leq \pi + 2\pi D$, switch S₁ is off, and switch S₂ is on, so the switch voltages are given as

$$v_{ds1} = V_I, v_{ds2} = 0 \quad (23)$$

According to (12), the current relationship is,

$$i_{S1} = i_{Cdseq1} = i_{Cdseq2} = i_{Cex1} = i_{Cex2} = 0 \quad (24)$$

Therefore, the current i_{S2} is expressed as

$$i_{S2} = -i_o = -I_m \sin(\theta - \varphi) \quad (25)$$

For $\pi + 2\pi D < \theta \leq 2\pi$, which is the dead time interval, both S₁ and S₂ are off. Therefore, the relationship between switch currents and switch voltages can be obtained by following a similar procedure of the interval $2\pi D < \theta \leq \pi$,

$$\omega C_{st} \int_0^{v_{ds2}} dv_{ds2} = \int_{2\pi D + \pi}^{\theta} I_m \sin(\theta - \varphi) d\theta \quad (26)$$

Yields,

$$\begin{aligned} v_{ds1} &= V_I - v_{ds2} = V_I + \frac{I_m}{\omega C_{st}} [\cos(2\pi D - \varphi) + \cos(\theta - \varphi)] \\ &= V_I + \frac{V_m}{\omega C_{st} R} [\cos(2\pi D - \varphi) + \cos(\theta - \varphi)] \end{aligned} \quad (27)$$

C. ZVS Condition

From (8), substituting $\theta = 2\pi$ to (27)

$$V_m = -\frac{\omega C_{st} R}{2 \cos(\pi D - \varphi) \cos \pi D} V_I \quad (28)$$

(28) expresses the relationship between the output voltage amplitude and the input voltage, under the condition of ZVS operation. For $\pi + 2\pi D < \theta \leq 2\pi$, v_{ds1} decreases from V_I by the discharging of C_{s1} , therefore, the derivative of v_{ds1} should be minus or zero. When the derivative is just equal to zero at $\theta = 2\pi$, the class-DE zero

derivative switching condition is satisfied. The derivative can be expressed as

$$\alpha = \frac{dv_{ds1}}{d\theta} |_{\theta=2\pi} = \frac{V_m}{\omega C_{st} R} \sin \varphi \quad (29)$$

Substituting (28) into (29)

$$\alpha = -\frac{\sin \varphi}{2 \cos(\pi D - \varphi) \cos \pi D} V_I \quad (30)$$

As discussed above, the derivative should be

$$\alpha \leq 0 \quad (31)$$

V. FOURIER EXPANSION

A. Output voltage

The output voltage is expressed as

$$v_o = R i_o = R I_m \sin(\theta - \varphi) = V_m \sin(\theta - \varphi) \quad (32)$$

From assumption 5), the voltage across the phase shift inductor L_x and the load resistance R is just the fundamental-frequency component of the switch voltage v_{ds1} for $0 \leq \theta \leq 2\pi$, where the voltage across L_x is the cosine function part and the voltage across R is the sine function part. Therefore, from (11), (22), (23), and (27), the amplitude of the voltage across R can be obtained from Fourier series expansion for v_{s1} that

$$\begin{aligned} V_m &= R I_m = \frac{1}{\pi} \int_0^{2\pi} v_{ds1}(\theta) \sin(\theta - \varphi) d\theta \\ &= \frac{1}{\pi} \left\{ \int_{2\pi D}^{\pi} \frac{V_m}{\omega C_{st} R} [\cos(\theta - \varphi) - \cos(2\pi D - \varphi)] \sin(\theta - \varphi) d\theta \right. \\ &\quad \left. + \int_{\pi}^{\pi + 2\pi D} V_I \sin(\theta - \varphi) d\theta \right. \\ &\quad \left. + \int_{\pi + 2\pi D}^{2\pi} (V_I + \frac{V_m}{\omega C_{st} R} [\cos(\theta - \varphi) + \cos(2\pi D - \varphi)]) \sin(\theta - \varphi) d\theta \right\} \end{aligned} \quad (33)$$

The result of V_m is

$$\begin{aligned} V_m &= -2V_I \cos \varphi \left\{ \pi + \frac{1}{\omega C_{st} R} \left[\frac{1}{2} \cos 2\varphi + \frac{1}{2} \cos(4\pi D - 2\varphi) \right. \right. \\ &\quad \left. \left. + \cos(2\pi D - 2\varphi) + \cos 2\pi D + 1 \right] \right\}^{-1} \end{aligned} \quad (34)$$

Combine (34) with (28), it can be obtained that

$$\omega C_{st} R = \frac{\sin(2\pi D - 2\varphi) \sin 2\pi D}{\pi} \quad (35)$$

It can be seen that $\omega C_{st} R$ can be a function of φ and D . We have conditions of I_m in (20), α in (30), and $\omega C_{st} R$ in (35) for achieving the ZVS, namely $I_m \geq 0$, $\alpha \leq 0$, and $\omega C_{st} R \geq 0$. From the above three conditions, the range of φ can be limited to

$$0 \leq \varphi \leq \pi D s - \frac{\pi}{2} \quad (36)$$

VI. MAXIMUM OPERATING FREQUENCY

Fig. 6. shows the plotted graph of $\omega C_{st}R$. We can see that the maximum value of $\omega C_{st}R$ increases as the duty ratio increases from $D = 0.05$ to 0.25 and decreases as the duty ratio decreases from $D = 0.25$ to 0.5 . The maximum value of $\omega C_{st}R$ can be read from the plotted graphs and it is approximately equal to 0.318 at the point of $\varphi = 0$ and $D = 0.25$. It means that when the shunt capacitance and load impedance are fixed, the maximum operating frequency can be always obtained in the condition of $\varphi = 0$ and $D = 0.25$. For $\omega = 2\pi f$, the function in this condition can be expressed as below:

$$(2\pi f C_{st} R)_{\max} = 0.318 \quad (37)$$

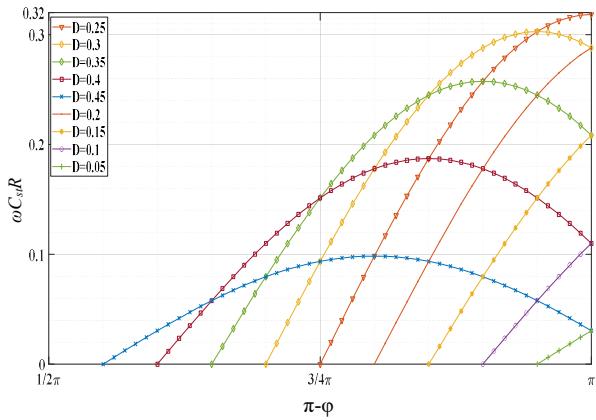


Fig. 4. $\omega C_{st}R$ as a function of φ and D

Under the condition of $\varphi = 0$ and $D = 0.25$, the frequency f can be increased by reducing the load resistance R and/or the sum of shunt capacitance C_{st} , and the maximum operating frequency f_{\max} can be obtained when C_{st} and R take their minimum value. Thus,

$$f_{\max} = \frac{0.318}{(C_{st} R)_{\min}} \quad (38)$$

For R is normally determined by a standard value of 50Ω in a high-frequency system, the f_{\max} is determined by the minimum value of the sum of the shunt capacitance C_{st} . As the linear external capacitor C_{ext} , C_{ext2} can be removed from the circuit, the minimum value of C_{st} becomes the minimum value of the sum of C_{dseq1} and C_{dseq2} , that

$$C_{st-\min} = C_{dseq1-\min} + C_{dseq2-\min} = 2C_{dseq-\min} \quad (39)$$

According to the decreasing property of (5), the minimum value of C_{st} can be obtained when V_I is at maximum value, thus

$$\begin{aligned} C_{st-\min} &= 2C_{dseq-\min} = 2C_{dseq}(V_{I-\max}) \\ &= \frac{4C_{DS}(V_{DS})}{V_{I-\max}} \sqrt{V_{DS} + V_{bi}} \sqrt{V_{I-\max} + V_{bi}} \end{aligned} \quad (40)$$

Substituting (40) into (38), the relationship between f_{\max} , input DC voltage V_I , and load impedance R can be expressed as:

$$f_{\max} = \frac{0.318V_{I-\max}}{8\pi C_{DS}(V_{DS})R\sqrt{V_{DS} + V_{bi}}\sqrt{V_{I-\max} + V_{bi}}} \quad (41)$$

VII. VERIFICATION

A. C_{ds} modeling of a 650V/30A SiC-MOSFET

According to the datasheet [15], the value of $C_{DS}(V_{DS})$ at $V_{DS}=500V$, can be figured out as $20pF$, for $C_{DS}(500V) = C_{oss}(500V) - C_{RSS}(500V)$. And V_{bi} can be typically valued at $0.57V$ refer to [11]. The model of the C_{ds} with the two initially valued parameters is plotted and compared with the reference points extracted from the datasheet. As there is a large gap, the two parameters are fitted step by step and finally optimized as $C_{DS}(500V)=32pF$, $V_{bi}=2V$. Thus, the final model of C_{ds} of the 650V/30A SiC-MOSFET is

$$C_{ds}(v_{ds}) = 32p \sqrt{\frac{502}{v_{ds} + 2}} \quad (42)$$

And the model of linearized capacitance is

$$C_{dseq(M)}(V_I) = \frac{64p}{V_I} \sqrt{502} \sqrt{V_I + 2} \quad (43)$$

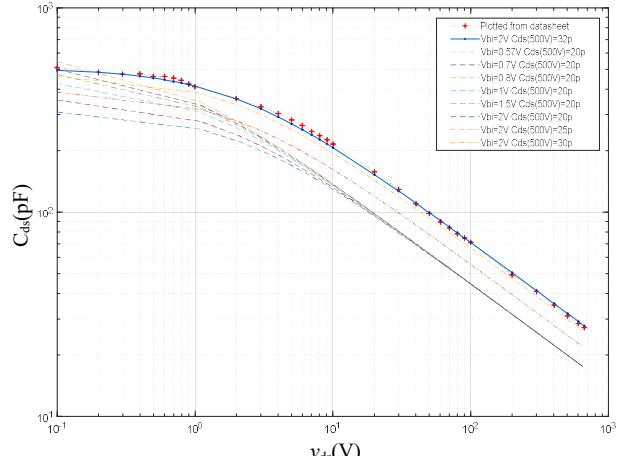


Fig. 5. Graph plotting of C_{ds} model with fitted parameters

Fig. 6. illustrates the graph of the function of C_{ds-eq} given by (43). Note that the graph of calculated C_{ds-eq} does not mean the physical nonlinear characteristics like C_{ds} , it means that when the input voltage V_I is high, C_{ds-eq} results in a low value.

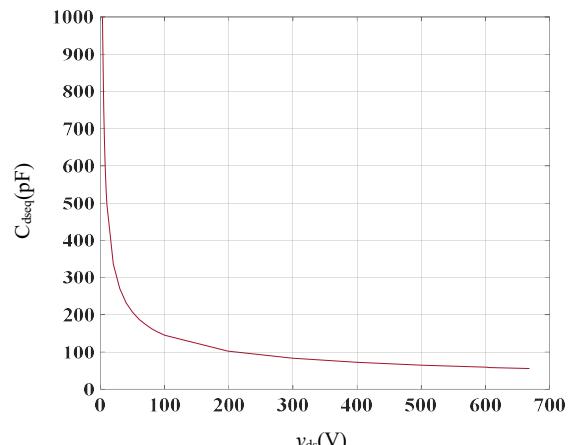


Fig. 6. Plotted graph of linear C_{ds-eq}

Typically, the maximum input voltage of a switch is considered lower than the break-down voltage for the voltage surge especially in a high-frequency system. For the 650V/30A SiC-MOSFET, 400V can be considered as a proper maximum input voltage. Thus, according to (41), (43), assuming R is fixed at 50Ω , the maximum operating frequency of the class-D ZVS inverter with the 650V/30A SiC-MOSFET can be calculated as (44), for other input voltages, the corresponding maximum frequency under ZVS can be calculated respectively as TABLE I shows.

$$f_{\max(M)} = 7.041\text{MHz} \quad (44)$$

TABLE I MAXIMUM OPERATING FREQUENCY FOR EACH INPUT VOLTAGE

Input voltage	Frequency
400V	7.041MHz
350V	6.584MHz
300V	6.094MHz
250V	5.558MHz
200V	4.967MHz
150V	4.294MHz
100V	3.495MHz
50V	2.447MHz

B. Simulation verification

Fig. 7. shows the simulation schematic for verification with the 650V/30A SiC-MOSFET spice model. The parasitic inductance and resistance in the circuit are neglected to match the ideal condition in the analytical model. In terms of the constant common parameters, both switches are driven by a 16V gate-driving voltage. the phase shift inductance is set to zero for $\varphi=0^\circ$. The load impedance is set to a standard value of 50Ω . As the shunt capacitor is only formed by the nonlinear parasitic capacitance inside the model of the switch. The values of resonant L_r and C_r are set exactly to match the operating frequency and the loaded quality factor Q_L is set to a sufficiently high value of 5. The simulation is conducted to verify two analytical results. Verification 1 is to prove that at a fixed shunt capacitance and load impedance, the maximum operating frequency for ZVS can always be obtained at Duty=0.25. Verification 2 is to prove that at $\varphi=0^\circ$, Duty=0.25, higher input DC voltage can be obtained higher operating frequency for ZVS. As the simulation results are obtained from realistic switches models, they are usable for quantitative analysis.

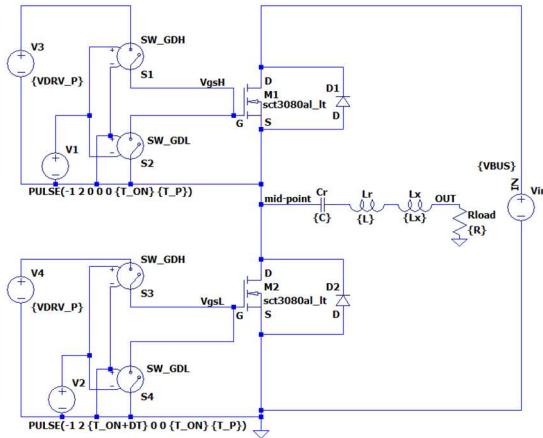


Fig. 7. Simulation schematic

TABLE II shows the simulation condition for verification 1. Under the condition of three various input DC voltage with their corresponding maximum operating frequency, the efficiencies are tested via a range of duties. The junction temperature is set to various values to approximate the real environment. Fig. 8. shows the results that at each fixed input DC voltage, and fixed load impedance, when operating at its corresponding maximum operating frequency, the highest efficiency is always obtained at $\varphi=0^\circ$, Duty=0.25. If the duty deviated from 0.25, the ZVS condition is not satisfied anymore so the efficiency decreases.

TABLE II SIMULATION CONDITION FOR VERIFICATION 1

Parameter	Symbol	Value		
Duty	D_{V1} , D_{V2}	0.1~0.4		
Gate driving voltage	V_1, V_2	16V		
Phase shift inductor	L_x	0H		
Load resistance	R_{load}	50Ω		
Input voltage	V_{in}	400V	300V	200V
Switching frequency	f_{v1}, f_{v2}	7.041 MHz	6.094 MHz	4.967 MHz
Resonant capacitor	C_r	90.416 pF	104.694 pF	128.164 pF
Resonant inductor	L_r	5.651 uH	6.529 uH	8.011 uH
Loaded quality factor	Q_L	5	5	5
Junction temperature	T_j	100°C	75°C	50°C

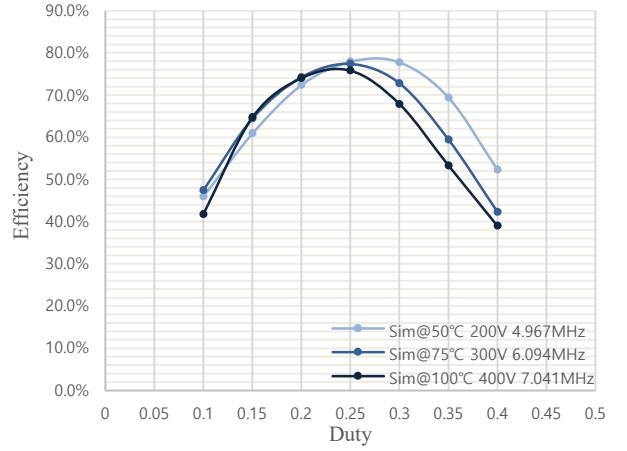


Fig. 8. Simulation result for verification 1

TABLE III shows the simulation condition for verification 2. The duty is fixed at 0.25. The efficiencies are tested at each fixed operating frequency with a range of input DC voltages. Fig. 9. shows the results that at each fixed operating frequency, the highest efficiency can only be obtained at its corresponding input DC voltage. If the input DC voltage deviated from the corresponding value, the ZVS condition is not satisfied, and the efficiency decrease. For example, 7.041MHz is the maximum frequency of 400V input for ZVS. At 7.041MHz, when the input voltage becomes lower than 400V, like 300V, the corresponding maximum frequency for ZVS changes to 6.094MHz, since $6.094\text{MHz} < 7.041\text{MHz}$, the ZVS

condition is not satisfied, thus at 7.041MHz, the efficiency at 300V is lower than 400V. On the other hand, for a fixed input voltage like 200V, when the operating frequency, like 7.041MHz or 6.094MHz, is beyond the corresponding maximum frequency 4.096MHz, the ZVS condition is not satisfied, and the efficiency decreases.

TABLE III SIMULATION CONDITION FOR VERIFICATION 2

Parameter	Symbol	Value		
Duty	D_{v1}, D_{v2}	0.25		
Gate driving voltage	V_{1}, V_{2}	16V		
Phase shift inductor	L_x	0H		
Load resistance	R_{load}	50Ω		
Input voltage	V_{in}	50V~400V	50V~300V	50V~200V
Switching frequency	f_{v1}, f_{v2}	7.041 MHz	6.094 MHz	4.967 MHz
Resonant capacitor	C_r	90.416 pF	104.694 pF	128.164 pF
Resonant inductor	L_r	5.651 uH	6.529 uH	8.011 uH
Loaded quality factor	Q_L	5	5	5
Junction Temperature	T_j	100°C	75°C	50°C

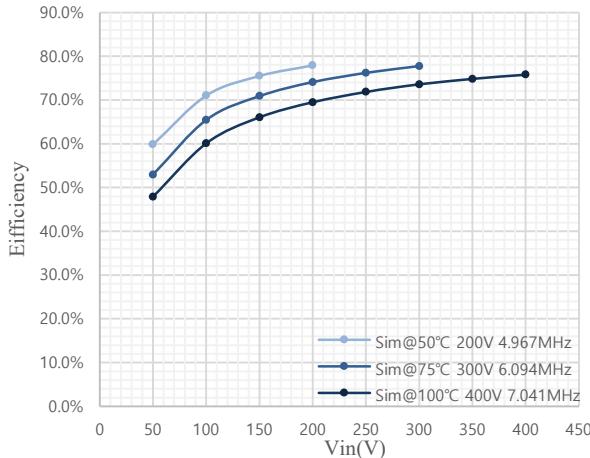


Fig. 9. Simulation result for verification 2

C. Experimental verification

Shown in Fig. 10., a PCB circuit of class-D ZVS inverter is made for experimental verification. The device of the 650V/30A SiC-MOSFET is utilized on the board. The resonant inductor is fabricated with a toroidal core and varnished copper wire. The resonant capacitors are used by the high-voltage MLCC. The parameters of the components are fabricated according to the simulation conditions. The signal is generated by a 200MHz function generator. The duty is adjustable via an RC integral circuit. The gate drivers are fed by the isolated DC-DC converters and provide a 16V gate-driving voltage to the SiC-MOSFET's gate. Both SiC-MOSFETs are attached to the heatsinks and no external capacitors are paralleled with the drain-source. Concerning the danger of overheating of the switch, the situation of 400V input voltage is not tested in the experiment this time.



Fig. 10. PCB circuit for experimental verification

TABLE IV and TABLE V listed the experiment conditions which are consistent with the simulation. There are few deviations between the measured value of the real components and the ideal value set in simulation. To reduce the error, the data are read when the case temperature of the switch reaches the same level as that in the simulation. Fig.11. and Fig. 12. shows the results of both verification 1 and verification 2. For the experimental results of verification 1, both input voltage of 200V and 300V at their corresponding maximum frequency obtained the highest efficiency at $\phi=0^\circ$, $D=0.25$, and the result curves keep the same characteristics as simulation results. For the experimental results of verification 2, it shows that when operating at the maximum frequency of 200V or 300V input, the highest efficiency can only be obtained at the corresponding voltage, if the input voltage changes lower, the efficiency decrease. The characteristics are also the same as the simulation.

TABLE IV EXPERIMENT CONDITION FOR VERIFICATION 1

Parameter	Symbol	Values	
Duty	D_{v1}, D_{v2}	0.1~0.4	
Gate driving voltage	V_{1}, V_{2}	16V	
Phase shift inductor	L_x	0H	
External shunt capacitor	C_{ex1}, C_{ex2}	0F	
Load resistance	R_{load}	50Ω	
Input voltage	V_{in}	300V	200V
Switching frequency	f_{v1}, f_{v2}	6.094MHz	4.967MHz
Resonant capacitor	C_r	104.796pF	129.068pF
Resonant inductor	L_r	6.508 uH	8.010 uH
Loaded quality factor	Q_L	5	5
Case temperature	T_c	75°C	50°C

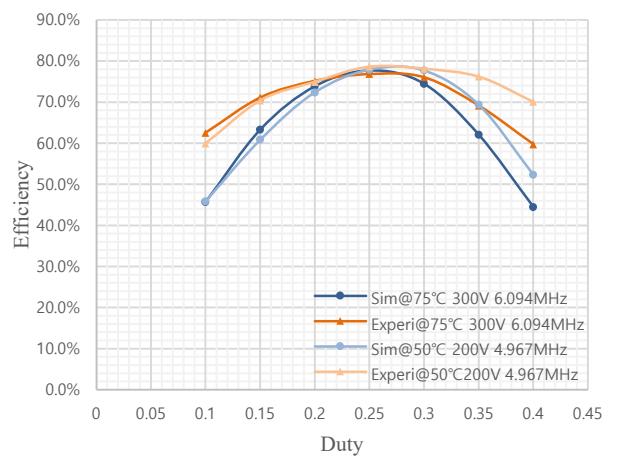


Fig. 11. Experimental result for verification 1

TABLE V EXPERIMENT CONDITION FOR VERIFICATION 2

Parameter	Symbol	Values	
Duty	D_{v1}, D_{v2}	0.25	
Gate driving voltage	V_{1}, V_2	16V	
Phase shift inductor	L_x	0H	
External shunt capacitor	C_{ex1}, C_{ex2}	0F	
Load resistance	R_{load}	50Ω	
Input voltage	V_{in}	50V~300V	50V~200V
Switching frequency	f_{v1}, f_{v2}	6.094MHz	4.967MHz
Resonant capacitor	C_r	104.796pF	129.068pF
Resonant inductor	L_r	6.508 uH	8.010 uH
Loaded quality factor	Q_L	5	5
Case Temperature	T_c	75°C	50°C

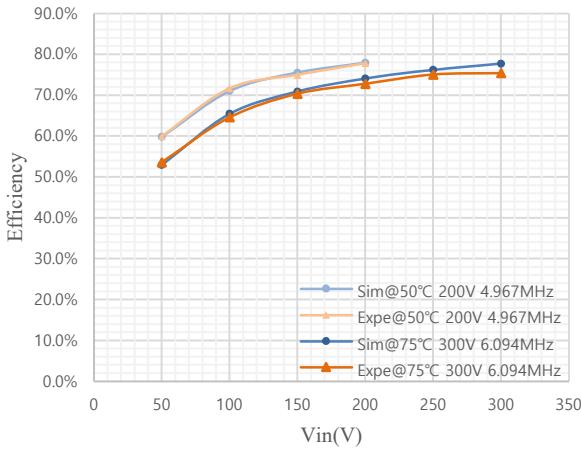


Fig. 12. Experimental result for verification 2

VIII. CONCLUSION

This paper experimentally verified a previously proposed analytical model of maximum operating frequency of class-D ZVS inverter at any duty ratio in consideration of the nonlinear parasitic capacitance. In the beginning, the necessity of analytical model of maximum operating frequency of class-D ZVS inverter is introduced. The previous researches about the analytical model are introduced, and the deficiency that neglects the nonlinear parasitic capacitance or is only usable for 0.25 duty is discussed. Based on the models in the previous researches, the proposed model which includes the linearized parasitic capacitance and is usable for any duty ratio is introduced. In the second chapter, the circuit constitution and the operation principle of the class-D ZVS inverter are introduced. In the third chapter, the nonlinear parasitic capacitance is mathematically expressed and linearized through the charge-related equation. In the fourth chapter, the frequency-related equation is derived and analyzed in the fifth chapter. Finally, the analytical results are verified by both simulation and experimental with good consistency.

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