

Extension and Implementation of a Model-based Lifetime Monitoring System with Parallel Calculation of Multiple Power Semiconductors

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Abstract

The importance of power electronics for future energy supply is steadily increasing. This implies a lot of semiconductor-based power converters and thus, a huge number of power semiconductors. Their operational availability becomes a critical feature of the power converters. Therefore, predictable maintenance is a key element for a stable and reliable energy supply. A new approach for a FPGA based implementation of a lifetime model for parallel monitoring of semiconductors will be presented.

Introduction

Whether in regenerative power generation such as wind and photovoltaics or in storage systems or in substations, frequency converters have become a key element of the electrical energy supply. Due to the fluctuation of regenerative energy sources such as wind and sun, there are always periods during which the systems do not feed in energy. Nevertheless, operational availability must be guaranteed at all times in order to feed energy into the electrical grid when sun and wind become available again. Thus, unplanned down times must be avoided as much as possible. However, wind turbines do fail unexpectedly and power converters contribute their fair share [1]. For this reason, a condition monitoring system for their power electronics would be of utmost value.

There are different approaches for the condition monitoring [2], [3], [4]. For this work a model-based system had been selected and implemented in software. Compared to other approaches, it does not use special hardware circuits. In [5] it was shown that the model can be implemented on a central processing unit (CPU) of an Industrial-PC for the execution in real-time. The measured average execution time for the implemented model was 1.52 µs on an Intel Core i7 CPU running at 2.3 GHz. Compared to a cycle

time of 20 µs, this leaves enough time for data acquisition and transmission. The software already implemented, can be parameterised and stores the state variables for each IGBT in a data structure [6][7]. Only an additional data structure needs to be created for each additional IGBT, while the calculation procedures can all be reused. A disadvantage arises when many IGBTs have to be monitored, e.g. in case of parallel operation of power semiconductors to reach the megawatt range. Then, capturing the needed measurements and the data transfer to the CPU can take a long time. Furthermore, the calculations must be done one by one. A further drawback is, that a CPU has only data types with a fixed width. It was shown in [5], that at least a 64-bit double precision floating point data type has to be used to accumulate the extremely small values, which describe the damage of individual cycles or time steps. Depending on the environmental condition these values can be as low as 10^{-30} and to overcome these disadvantages, an FPGA should be used.

In the following sections, the model for calculating the remaining lifetime is described. Subsections will follow for preparing a thermal model and advantages of additional sensors are discussed. Finally, the advantages and challenges of the new implementation approach will be described.

The life time model

To estimate the remaining life time of a power semiconductor, for example an IGBT, two predominant degradation mechanisms have to be considered. During the blocking phase, i.e. when the switch is open, the electrochemical state is updated with respect to the main acceleration factors: temperature, humidity and bias voltage. The remaining lifetime is estimated using an extended Peck model [8].

Thermomechanical stress is the second, main degradation mechanism covered in this lifetime model. Switching as well as conduction lead to power losses and subsequently to a temperature increase of the chip. Due to volatile operation conditions, the collector current and the duty cycle are continuously changing, resulting in temperature swings. These recurring temperature cycles lead to a thermomechanical stress. The determining parameters are the junction temperature, the applied collector-emitter voltage, the current flowing through the component, and the switching times of the power semiconductors. All variables must be transferred to the model as a "process image", i.e. as a time-consistent, synchronised data set. For the calculation of the damage, an extension of the Coffin-Manson model is used.

The overall model is shown in Fig. 1. The input variables are the voltages applied to the semiconductor, if available the switching times, the currents flowing through the IGBT, the temperature of the heat sink and the relative humidity of the environment. The output value is the remaining lifetime of the extended models according to Coffin-Manson and Peck, respectively.

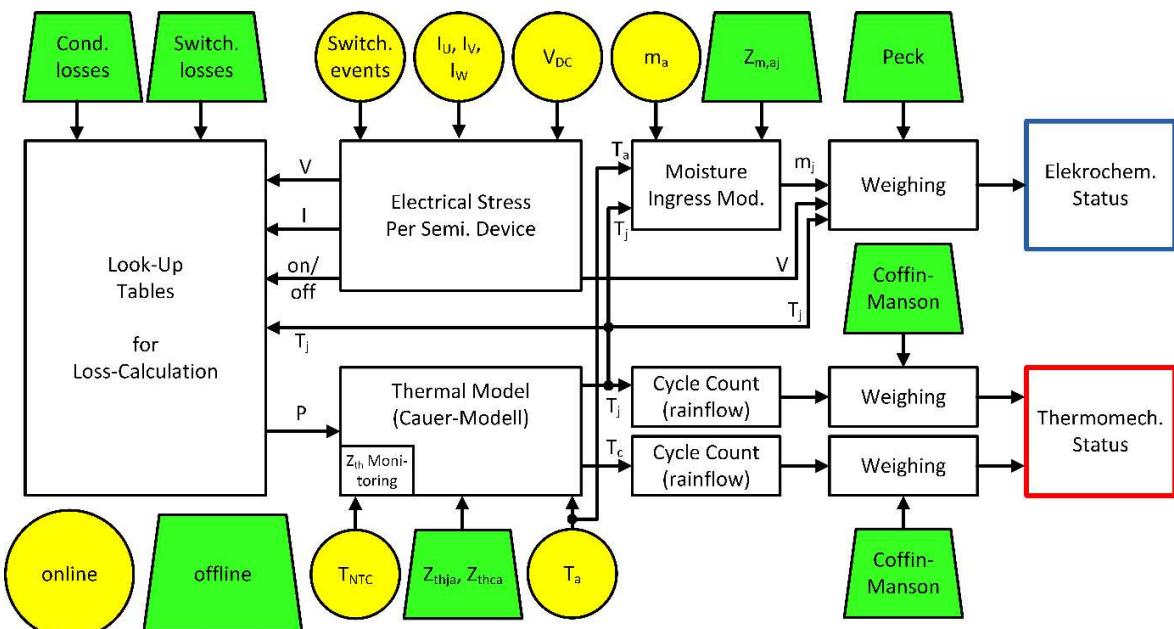


Fig. 1: Lifetime model according to [6] with yellow circles representing online measurements, while green trapezia represent offline data measured in the lab before.

From the input variables obtained by measurements the electrical load per semiconductor is determined. For this purpose, the phase currents I_U , I_V and I_W , the DC-link voltage V_{DC} and the switching events are required. Conduction losses and switching losses occurring during the operation of the semiconductors are taken from look-up tables. The parameters of these look-up tables have to be determined from laboratory measurements, because data sheet information usually includes a safety margin with respect to the typical values.

As previously described, the junction and case temperatures are required for the calculations. Since not all semiconductors are equipped with a temperature sensor and such sensors would anyway yield a package temperature, the required junction temperature T_j is determined using a thermal model.

For the Coffin-Manson model, the temperature swing ΔT_j and the mean temperature $T_{j,m}$ are needed as input values. With a cycle counter, here a rain-flow algorithm [9], completed temperature cycles can be extracted. The parameters α and β will be determined with a power cycle test (PCT) in the laboratory. E_A is the activation energy and k_B Boltzmann's constant. The result of the equation (1) is the life time consumption LC_{CF} for the temperature swing ΔT_j .

$$LC_{CF} = \frac{1}{\alpha} \cdot \Delta T_j^\beta \cdot e^{-\frac{E_A}{k_B \cdot T_{j,m}}} \quad (1)$$

The life time consumption LC_{CF} for the corresponding temperature swing ΔT_j is accumulated to $LC_{CF,\text{total}}$ with equation (2). If this $LC_{CF,\text{total}}$ reaches a value of one, the overall life time limit regarding the thermomechanical state is reached.

$$LC_{CF,\text{total},n} = LC_{CF,\text{total},n-1} + LC_{CF,n} \quad (2)$$

To calculate the life time consumption for electrochemical state a modified model of Peck is used [8]. The input variables are the moisture at the junction m_j , the collector-emitter voltage V_{CE} and the temperature of the junction T_j . In a Temperature Humidity Bias test (THB) the reference lifetime is identified. This reference lifetime is determined at a reference relative humidity RH_{REF} , the reference Temperature $T_{j,REF}$ and the blocking voltage $V_{CE,REF}$. The parameters x and y are adjustment constants determined by the THB test. While the device is operated in the field, the relative humidity RH , ambient temperature T_a and the collector-emitter voltage V_{CE} are measured. With all these input values and equation (3) the acceleration factor a_f can be calculated. E_A is the activation energy and k_B Boltzmann's constant.

$$a_f = \frac{L_{REF}}{L} = \left(\frac{RH}{RH_{REF}} \right)^x \cdot e^{\frac{E_A}{k_B} \left(\frac{1}{T_{j,REF}} - \frac{1}{T_j} \right)} \cdot \left(\frac{V_{CE}}{V_{CE,REF}} \right)^y \quad (3)$$

For a time interval Δt_i the acceleration factor is constant if all inputs values are constant. The lifetime consumption $LC_{Peck,\text{total}}$ (4) is calculated as the sum of the products of the acceleration factor $a_{f,i}$ and the corresponding time interval Δt_i referred to the reference lifetime L_{REF} .

$$LC_{Peck,\text{total}} = \frac{1}{L_{REF}} \sum_{i=0}^n \Delta t_i \cdot a_{f,i} \quad (4)$$

If $LC_{Peck,\text{total}}$ reaches a value of one, the overall life time limit regarding the electrochemical state is reached.

While most of the described submodels are generic for power semiconductor devices with only the parameters varying, the thermal model and the modelling of the moisture ingress depend highly on the monitored device. The look-up tables have a fixed structure, but their contents depend on the IGBT module as well. How to implement such a thermal model will be described in the following subsection.

Thermal model

In the first approach, a passive one-dimensional equivalent thermal network is implemented for each IGBT module based on the parameters given by the data sheet of the module and the data of the cooling

plate and system. The overall goal is to determine the junction temperature $T_{j,n}$ of each chip inside the module. In order to do so, the Foster network specified in the IGBT module's data sheet is converted to an equivalent Cauer network for the diodes as well as the IGBT switches. Thus, a physical and thermal description of the power device can be obtained. Finally, the determined parameters of the Cauer model are fitted in such way, that the time response of both models match exactly in case of subdividing the semiconductor construction into the same number of thermal layers. By knowing the material stack of the power module, the number of layers can be adopted to the number of physically existing or relevant material layers. The physical parameters like the thermal conductivity and thermal capacity describing the thermal behaviour of the material for each layer. Therefore, the mean value and the span of variation for the corresponding parameter per material (copper, ceramics, die attach, etc.) is determined from the literature [9,10,11,12,13] and used as initial and boundary value for the fitting algorithm, respectively. Finally, a Cauer network that matches the data sheet values is established, but has to be verified by Z_{th} measurements. A temperature online monitoring can be further tuned if an integrated NTC-resistor, connected to the base plate inside the power module, is utilised. In this case, the network needs to be extended with a transfer function, considering the position of the NTC with respect to the chip positions. This approach will observe long-term changes of the thermal behaviour of the module itself and offers the possibility to compare calculated values to an actual temperature measurement. In the future, a reduction of calculation time and hardware requirements is pursued with the implementation of a three-layer variant of the matched Cauer model for an online Z_{th} condition monitoring measurement.

Additional environmental sensors

The measurement campaign, carried out in [6] was done with a minimally invasive system on an existing wind turbine converter. The measurements were used in [7]. Within the new approach, the sensors are included in the development process at the manufacturer to ensure an improved climatic mapping inside the cabinet. Every cabinet contains three RHT-, three PT100-, and one flow-sensor together with NTC-resistors inside the power modules. Estimating the micro climate at specific components requires a proper dataset of critical environmental conditions at well-known positions. The remaining thermomechanical lifetime is determined via PT100 on the base plate and NTCs inside the power module, while the electrochemical status is estimated via the same temperature sensors and an RHT-sensor close to the devices. Furthermore, the climate around the DC-link is measured by an RHT-sensor at the bottom and a PT100-sensor at the top to improve the data set. By the integration of the model into the control of the converter and by the accurate climate mapping, the resolution of the lifetime modelling is improved significantly. Moreover, it is possible to obtain critical environmental conditions like condensation within the operational life in real-time.

Implementation of the model

Figure 2 shows the minimum required measurements and the sequence in which the individual sub models have to be processed. For calculation of the damage due to thermomechanical stress switched on, the Coffin-Manson model is used. Therefore, the switching event S_{Evt} , the ambient temperature T_a and the load current I have to be assessed, i.e. must be measured. In the blocking phase of the IGBT the Peck model is used to calculate damage due to electrochemical stress. The switching event S_{Evt} is also used. Additionally, the ambient moisture m_a and the DC-link voltage V_{DC} are required.

The order of execution is as follows: The procedure of accessing the look-up table has to be executed each time a switching event occurs to calculate the switching losses and while the IGBT is in on-state to calculate the conduction losses. The result is fed into the thermal model. This model must be executed with a fixed sampling rate. The sampling rate depends on the desired accuracy, ideally it is in the range of the PWM frequency and must not be higher than the sampling rate of the current. Additionally, the time for processing the sub models has to be considered. The Peck model has to be executed each time an IGBT is switched off and must be executed after a (significant) change in the input values occurred. The cycle counter has to be executed each time when a new output value is available from the thermal model. The Coffin-Manson model has to be executed after each half or full temperature cycle of the cycle counter.

As previously discussed, implementation on an FPGA offers some advantages, if many IGBTs need to be monitored. Nevertheless, some challenges also arise. While the implementation of the Coffin-Manson

and Peck models on a CPU, e.g. in the "C" programming language, represents one line of program code, it is more complex if implemented on an FPGA. For the execution of the whole mathematical description of the models, a state machine has to be designed, which coordinates the correct sequence of mathematical operations. The advantage is parallel execution of several parts of the equations.

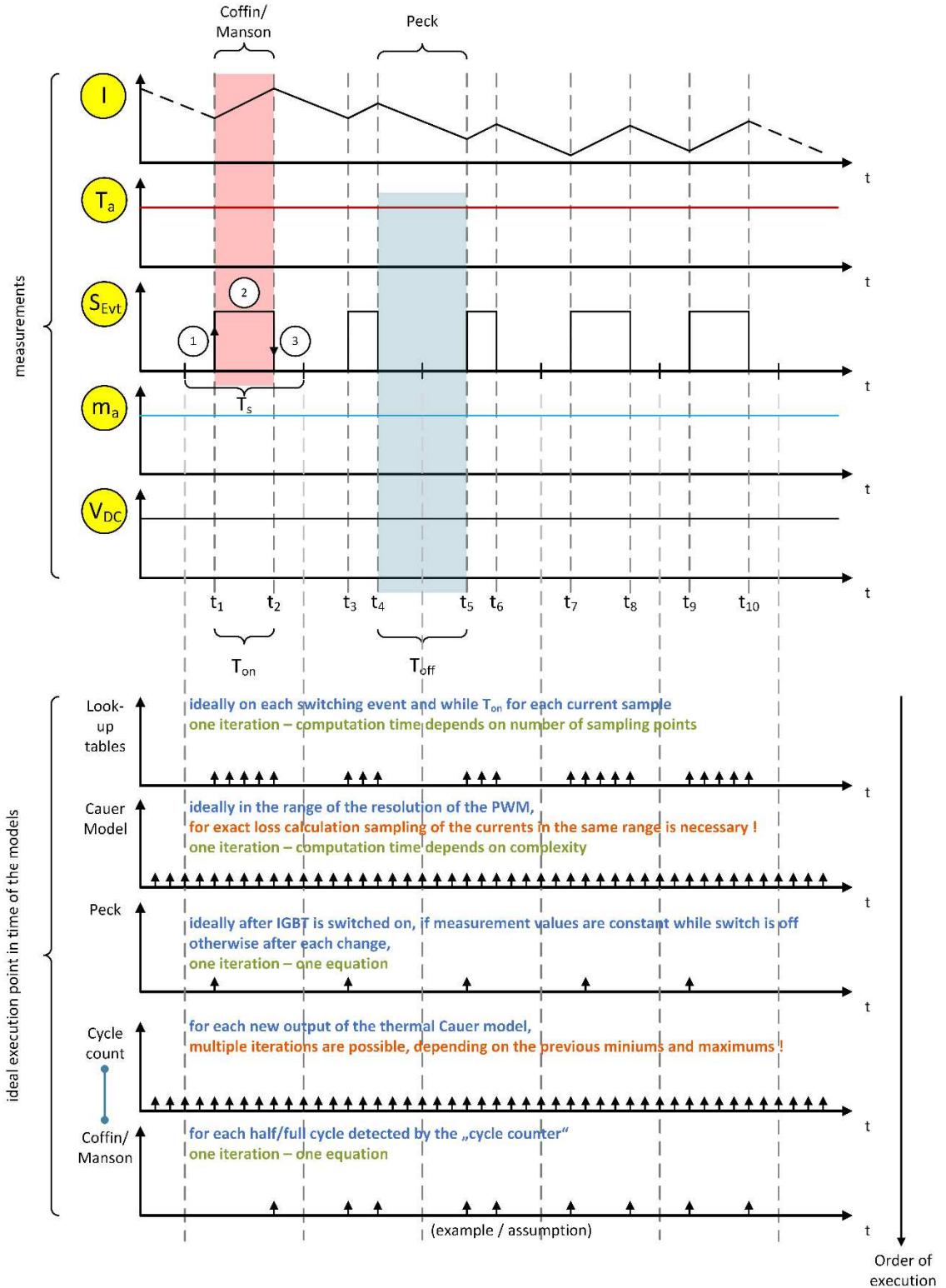


Fig. 2: Switching events and sequence of execution of the submodels

Tools such as Matlab/Simulink can be used to support the developer. However, they do not necessarily generate the hardware description with the necessary degree of optimisation. The limited resources of an FPGA must be considered. Especially the DSP slices, which are used for multiplications and other

complex operations such as the exponential function, are limited. Therefore, a hybrid approach should be used. Tools for the automatic code generation for the hardware description shall be used, while other parts will be optimised by hand. That means that some DSP slices must be reused. Nevertheless, sufficient DSP slices must be available that a parallel calculation of the submodels is still possible, otherwise a CPU with only one thread could be used. This has to be observed when the FPGA-type is selected. To estimate the consumption of the FPGA resources, such as look-up tables (LUT), flip-flops (FF) as well as DSP slices, the loss calculation part of the lifetime model was set up in Matlab/Simulink in a first step. The resulting VHDL code for a Xilinx FPGA target was generated using the HDL Coder and integrated in Xilinx Vivado.

Since the switching events – respectively the gate signals – are provided by the overlaying power converter controller and are transmitted to the FPGA, the current path of each phase leg has to be determined by these signals as well as the measured current values. This functionality has been implemented by an analysis of the states of the components in one phase leg (see Fig. 3). The fundamental table to determine the conducting elements is shown in Table 1.

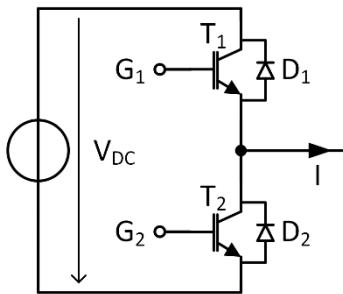


Fig. 3: Power components of one phase leg

Table 1: States of the components

gate signals		I	conducting component
G ₁	G ₂		
0	0	>0	D ₂
0	0	<0	D ₁
1	0	>0	T ₁
0	1	>0	D ₂
1	0	<0	D ₁
0	1	<0	T ₂

For the conduction states of T₁ and T₂ in one phase leg it was assumed, that the dominant current is always flowing through the transistors and not through the anti-parallel diodes D₂ and D₁. This holds for any allowed switching action according to the direction of the current, which relates to the potential at the output of the phase leg. This detection of the conducting components was implemented together with an edge detection of the switching signals by using logic blocks in the loss calculations based on look-up tables, which is shown in Fig. 4.

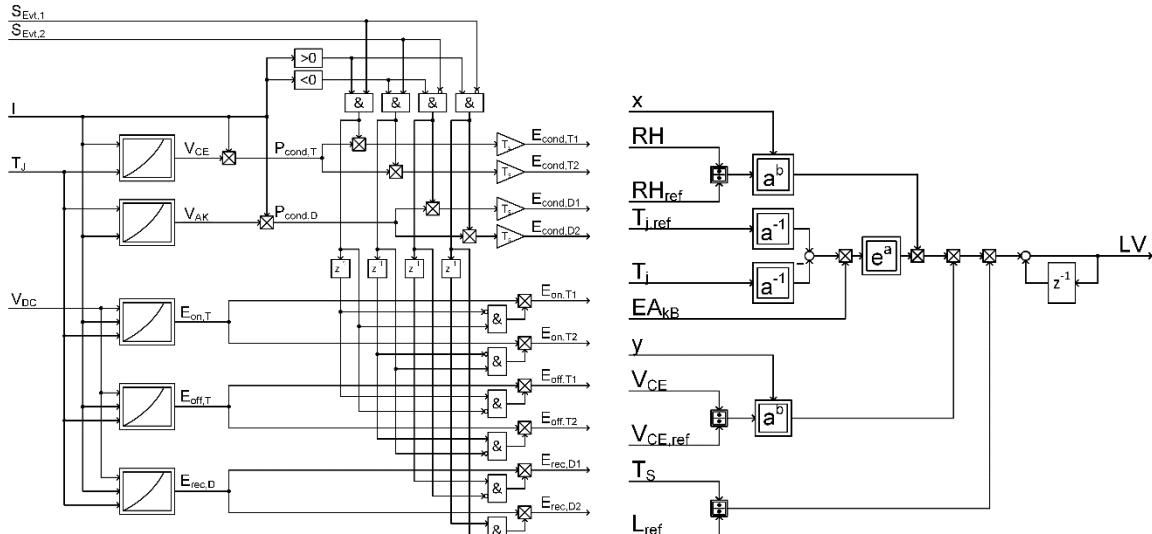


Fig. 4: Implementation of the look-up tables

Fig. 5: Implementation of the Peck-model

For the validation of the model, basic input and output periphery was mapped to avoid the erroneous deletion of code segments, which seem to be unused, by the code generation toolchain. After running the synthesis and implementation, the usage of the resources for different implementation methods of the exponential function was compared. Furthermore, the impact of different data types on the resources

for the same calculations was analysed by choosing different fixed-point formats as well as running the complex parts in floating-point blocks and additionally, using a floating-point core in Vivado. The model that was used for the implementation of the Peck model in that case, is shown in Fig. 5.

Data processing

The input values must be fetched from the analog-to-digital converters at equidistant times and buffered in order to make them available to the sub-modules. To determine the amount of memory for the buffers and the data transfer rates, the number of power semiconductors, which should be monitored have to be evaluated. The number of power semiconductors depends on the topology of the power converter. In case of two-level power converter [14] twelve switches (IGBT) and diodes must be considered. If a chopper is applied to the DC-link an additional switch has to be monitored. If a power converter in three-level neutral-point-clamped (NPC) topology [14] should be monitored, the number of switches is double and six additional diodes must be taken into consideration. Power converters in the range of several megawatt are often a parallel connection of multiple modules, which are implemented in a two-level topology. For the following investigations it is assumed that all measurements are collected in one FPGA.

Initially the sampling rates for the different measurements must be defined. While the ambient temperature and relative humidity changes slowly, the voltages and currents change faster. The measurements have to be taken depending on the switching algorithm and its frequency. If the switching frequency is fixed, the measurements are commonly taken with the same frequency but not necessarily at the moment when the IGBTs are switched. If the switching of the IGBTs is done based on the measured current (current hysteresis method) then the sampling frequency is variable. Thus, the minimum frequency for sampling the currents is given by the change of the signal frequency. The maximum required sampling frequency to fulfil the requirements of the lifetime model is limited by the calculation time of the model itself. The calculation times of the previously described submodels must be determined. Thus, depending on the needed calculation time, the upper limit of the sampling frequency is defined.

For the following example, it will be assumed, that the feedback control of the DC-link keeps the voltage constant, so that the same sampling frequency as for the currents can be applied. For a system consisting of one two-level converter there are 6 IGBTs per inverter and 14 IGBTs for a full converter including a chopper when two IGBTs are in one module. If four of these systems are operated in parallel, the total amount of IGBTs is 56, in case of 8 systems it results in 112 IGBTs.

If a switching frequency of 4 kHz is assumed and only one instance of the lifetime model exists, i.e. updating the lifetime can only be processed for one IGBT at a time, that means: The whole model must be calculated in at most 4.4 μ s to calculate updates for 56 IGBTs and 2.2 μ s to calculate updates of the model for 112 IGBTs. If the switching frequency is increased, the calculation time must be lower. However, if the calculation time is too high, more instances of the lifetime modules have to be calculated in parallel, which is the reason to use an FPGA. In turn, the number of instances that can be implemented in parallel depends on the necessary resources for the implementation of the lifetime model in the FPGA. This will be dealt with in the next chapter.

Simulation and Result

After implementing the parts of the lifetime model in Matlab/Simulink, the following results were achieved by generating VHDL code using the HDL coder and implementing the design in Xilinx Vivado on the target hardware. A comparison of the resources' consumption of the Peck model is shown in the following table. In this case a Zynq-7000 SoC including an Artix-7 FPGA core from Xilinx was used for the reference design. The calculation of the exponential function can be implemented in two different ways. First, the calculation can be done by using the Vivado floating point library and second, the exponential function can be implemented by using a fifth order Taylor series to do the calculation by using fixed point variables to avoid type casting between floating and fixed-point numbers, which requires a large amount of FPGA resources and can lead to inaccurate results of the calculations.

Table 2: Usage of FPGA resources of the Peck model

size of variables	32bit	
	floating point	taylor series
LUT	13871 (26.07 %)	12133 (22.81 %)
FF	9399 (8.83 %)	8479 (7.97 %)
DSP	44 (20.00 %)	72 (32.73 %)

The relative count refers to the overall resources of the used Zynq module. The results of these comparisons lead to a compromise between maximum parallel execution of the model and minimum resources. Another advantage of a FPGA is the use of data types with an adapted bit width to be able to calculate and add up very small damage values. Afterward, a timing analysis of the implementation has been performed for two clock rates of the FPGA, which are shown in the following table.

Table 3: Timing analysis of the Peck model implementation

size of variables	32bit			
	floating point	taylor series		
FPGA clock [MHz]	100	250	100	250
Calculation time [ns]	780	312	830	332
No. of clock cycles per calculation	78	78	83	83

As expected, the overall calculation time decreases for higher clock rates, but the numbers of the necessary clock cycles to perform the calculations are equal. During the calculation of the Peck model several multiplications need to be performed simultaneously, while their results depend on each other. Therefore, many DSP slices as well as LUTs are required for this part.

The results of the lookup table implementation are shown in the following Table 4. Due to restrictions of the array size for 2D-lookup tables in the HDL coder, the calculation of the lookup tables has only been implemented for 32-bit variables. But, in this case the resolution of 32-bit fixed-point datatypes is also sufficient for calculating the losses of the transistor and the diode.

Table 4: Resource consumption and timing analysis of the lookup table calculation

size of variables	32bit	
	100	250
LUT usage	1706 (3.21 %)	1706 (3.21 %)
FF usage	870 (0.38 %)	870 (0.38 %)
DSP slice usage	8 (3.64 %)	8 (3.64 %)
Calculation time [ns]	80	32
No. of clock cycles per calculation	8	8

The results underline one key advantage of the FPGA at performing lookup table operations, since the overall resource consumption is quite low compared to the Peck model calculation before. In this case the lookup tables were stored in the LUTRAM, which significantly decreases the usage of LUTs.

For the calculation of the junction temperature, a simple Cauer model consisting of four layers has been implemented. Each layer represents a physical layer of the thermal network of the power semiconductor module mounted to the heat sink. Therefore, each layer can be modelled with a first-order lag according to the thermal network. The results are shown in the following Table 5. This model requires a high number of DSP slices for the calculation of the temperatures at the different layers and the heat transfer between the layers. But since the DSP slice usage is at only 18.18 % in total, even more complex thermal networks can be implemented.

Table 5: Resource consumption and timing analysis of the Cauer model

size of variables	32bit	
FPGA clock [MHz]	100	250
LUT usage	3626 (6.82 %)	3626 (6.82 %)
FF usage	2380 (2.24 %)	2380 (2.24 %)
DSP slice usage	40 (18.18 %)	40 (18.18 %)
Calculation time [ns]	400	160
No. of clock cycles per calculation	40	40

According to figure 1, the evaluation of the thermomechanical status of the semiconductor is done by a rain flow cycle counter for the thermal cycles and the impact of the life time consumption is weighed by using the Coffin-Manson model. This model has also been implemented on the FPGA and the results are shown in the following table.

Table 6: Resource consumption and timing analysis of the Coffin-Manson model

size of variables	32bit	
FPGA clock [MHz]	100	250
LUT usage	7357 (13.83 %)	7357 (13.83 %)
FF usage	5876 (5.52 %)	5876 (5.52 %)
DSP slice usage	32 (14.55 %)	32 (14.55 %)
Calculation time [ns]	780	312
No. of clock cycles per calculation	78	78

For the overall investigation of one calculation of the lifetime model, the usage of the FPGA resources of all sub modules have been added. This overview is presented in the following table.

Table 7: Resource consumption of the lifetime model for one phase leg

32bit (100 MHz)						
	available	Peck	Lookup	Cauer	Coffin-Manson	sum
LUT	53200	13871	1706	3626	7357	26560 (49.92 %)
FF	106400	9399	870	2380	5876	18525 (17.41 %)
DSP	220	44	8	40	32	124 (56.36 %)
Calculation time	-	780	80	400	780	2040
Clock cycles	-	78	8	40	78	204

The results in Table 7 show, that the main part of the resources of the FPGA core is consumed solely for the calculation of one phase leg. But, in this investigation the shared usage of DSP slices of the different sub modules has not been considered, especially regarding pipelining of different calculations. Therefore, the values represent a worst-case implementation for analysing the feasibility of the FPGA. But according to the number of necessary clock cycles, this FPGA is theoretically capable of performing the calculation of over 490,000 phase legs per second. Considering a switching frequency of 4 kHz of the power converter this results in the calculation of 123 phase legs in only one switching cycle. Assuming a 2-level power converter topology, the online calculation of 20 full-scale converters is possible in this period.

In this work, some resources of the FPGA needed to be used for interfacing the model by physical ports to avoid undesired deletion of parts of the generated program code. So, there is the opportunity of further optimisations of the proposed implementation method. For the calculation of the complete lifetime model, high bit sizes need to be achieved to correctly represent the smallest fractions of lifetime consumption. But regarding the overall calculation capacity per switching cycle, an increase of the bit size of the variables is even possible on this device. For larger power converter systems, the calculation model can easily be ported to a larger FPGA.

Conclusion

This article describes the extension of a model for estimating the remaining lifetime of power semiconductors and the implementation of this system. The model takes the damage caused by electrochemical and thermomechanical degradation into account. An implementation has been drawn up and implemented for an FPGA. The determined timing measurement based on the FPGA based implementation showed an increase in performance of the new approach. Nevertheless, while mathematical operation can be implemented using Matlab/Simulink, for loops which are needed for the cycle counting algorithm this does not hold. Furthermore, Matlab/Simulink currently only supports data types of 64 bits in this toolchain, data types with e. g. 128 bits must be implemented directly in VHDL. That means, a hybrid approach is the best solution, using the FPGA for parts of the model, which can highly be parallelised, and e. g. a CPU for the cycle counting. For this combination the Xilinx Zynq is an example for an optimal choice. Due to the extensible implementation based on basic mathematical operations, the model can easily be adapted to further degradation mechanisms.

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