Measurement of Coss-V characteristic of the 1.7kV/900A SiC power module and estimation of the channel current

Jacek Rabkowski[1], Fernando Gonzalez-Hernando[2], Mariusz Zdanowski[1], Irma Villar[2], Uxue Larrañaga[3]

[1]Warsaw University of Technology
Koszykowa 75
00-662 Warsaw, Poland
jacek.rabkowski@pw.edu.pl

[2]Ikerlan Technology Research Center
Basque Research and Technology Alliance (BRTA),
J. Mª. Arizmendiarrieta, 2
Arrasate-Mondragón, Spain.
fgonzalez@ikerlan.es

[3]CAF Power & Automation
San Sebastián, Spain
ULarranaga@cafpower.com

Acknowledgements

This project has received funding from the Shift2Rail Joint Undertaking under the European Union's Horizon 2020 research and innovation programme under grant agreement No 101015423. The content of this publication does not reflect the official opinion of the European Union. Responsibility for the information and views expressed in the report lies entirely with the author(s).

Keywords

«Silicon Carbide (SiC)», «Zero-voltage switching», «MOSFET», «measurements», «switching losses».

Abstract

This article presents a novel method for dynamic measurements of C_{OSS}-V characteristics of SiC power modules based on the process of charging the output capacitance of the transistors. The technique has been validated for a 1.2kV/450A power module with this characteristic available in its datasheet, showing good compliance. Then, this technique has been used to determine the C_{OSS}-V characteristics of a 1.7kV/900A SiC MOSFET module, which allowed the extraction of the capacitive current while switching off the transistor. Finally, the channel current and the share of the capacitive current in the drain current were determined for various switched currents and switching speeds. According to the capacitive charge calculations for several cases, the accuracy of the method is high enough to perform switching loss estimations.

Introduction

Medium voltage SiC MOSFETs are excellent candidates for soft-switched DC-DC or Inductive Power Transfer (IPT) converters, including these operating at Zero Voltage Switching (ZVS) conditions [1]-[4]. Such systems usually operate at high switching frequencies, and a substantial part of the power losses occurring in semiconductor elements are losses generated during the switching-off process. Therefore, it is essential to correctly determine the switching losses to properly design the converter from an electro-thermal perspective. Several publications, to mention only [5]-[9], have shown that the problem of switch-off losses is quite complex. Without going into deep analysis, it can be concluded that the drain current includes the channel current, which causes conduction power losses in the transistor's channel, and the capacitive current, which is almost lossless [10]. Therefore, to correctly determine the switch-off power losses, it is necessary to distinguish these two components. This can be done by finding the capacitive current from the derivative of the drain-source voltage, for this, the C_{OSS}-V characteristic of the power device must be employed. However, this characteristic is not available for all power modules – this is the case of the 1.7kV/900A SiC power module MSM900FS17ALT discussed in this work [11] or other power modules under development.

The problem of measuring C_{OSS}-V characteristics, including for SiC power devices, was undertaken by many research teams [12]-[17]. There are classic methods using an impedance analyzer or an LRC bridge, but the main problem is the need for high voltage polarisation. Hence, various circuit concepts have arisen to allow measurements at higher voltages [12]-[13]. Another dynamic testing approach is based on running one- or two-pulse tests and observing the corresponding waveforms to determine charges and capacitances [14]-[16]. It is also possible to use a similar method in transistors' continuous operation without load [18]. Considering the specificity of the 1.7kV/900A module, i.e. medium voltage and high rated current, i.e. a large active surface and possibly a large output capacitance, the authors propose a dynamic method of measuring the C_{OSS} capacitance based on a single-pulse test. Observing the drain-source voltage and the current flowing through the power device, it is possible to determine the C_{OSS}-V characteristic precisely.

The paper is organized as follows: after the introduction, the problem of the capacitive current during the turn-off process is discussed. Then, the proposed method for measuring the C_{OSS}-V characteristic is presented. In the next section, this method is validated for a CAB425M12XM3 module, whose C_{OSS}-V characteristics can be found in its datasheet [18]. Finally, a measurement is performed for the MSM900FS17ALT module, and the capacitive currents in a system operating at a frequency of up to 25 kHz are estimated at different switching speeds. The work is concluded with a summary of the main outcomes.

Difference between the drain and channel current

Typical waveforms recorded at the turn-off process of the MSM900FS17ALT at 850V and 600A are presented in Fg.1(a), while idealized equivalents can be seen in Fig.1(b). To simplify, the impact of parasitic inductances and high-frequency oscillations are not considered. In the optimal scenario from the switching losses point of view, the gate driver can quickly discharge the gate-source capacitance C_{GS} to reach threshold voltage V_{TH} before drain-gate capacitance C_{GD} is charged and drain-source voltage V_{DS} achieves high values. The current through the channel of the power transistor i_{CH} is rapidly reduced to zero before V_{DS} is high and, as result, the power dissipated in the transistor (as the product of v_{DS} and i_{CH}) is low. These conditions can be recognized as nearly ZVS and this scenario is preferable as results in nearly zero switch-on losses and therefore leads to higher efficiency [7].

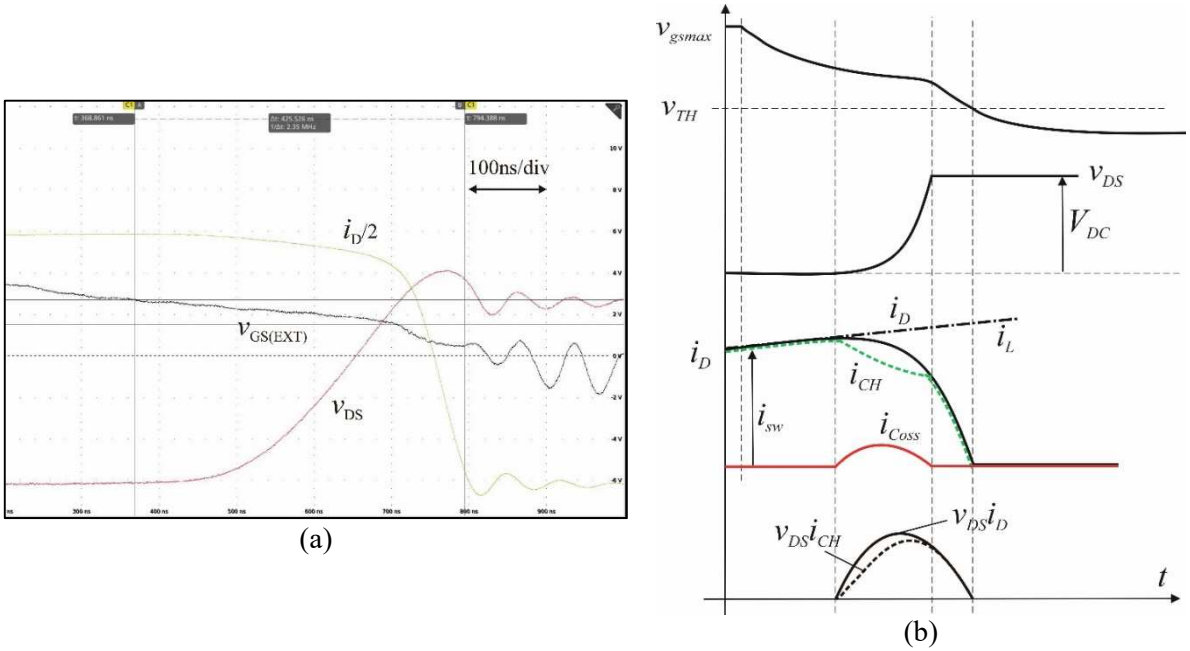


Fig. 1: Waveforms during turn-off – recorded for the MSM900FS17ALT (a) and idealized – without an influence of parasitic inductance (b)

However, this scenario is difficult to achieve in most high-current power modules. The substantial input capacitance C_{ISS} requires the large gate current to be quickly discharged but limited supply voltage of the gate driver and non-zero internal gate resistance are limiting factors. Thus, the real scenario usually observed is presented in the idealized waveforms in Fig. 1(b): during the voltage rising phase the v_{GS} is above the threshold and the channel remains open, generating power losses. Note that the resulting power loss is lower than a product of v_{DS} and i_D multiplication usually provided in the datasheets. Finally, the v_{GS} crosses v_{TH} (and the i_{CH} becomes zero) after v_{DS} has reached V_{DC}. It is worth noting that, at the end of the voltage rise phase, the observed i_D is equal to i_{CH}, since there is no displacement current in the output capacitances when the voltage has reached a constant value. In practice, it will also be increased by voltage overshoots across parasitic inductances in the switching loop, as shown in Fig. 1(a).

Coss-V test method

Similarly to [17], the proposed method uses a half-bridge power module (Fig. 2), but only a single pulse test is performed. The low-side transistor of the half-bridge is the device under test (DUT) and is permanently switched off, with its gate shorted to the source, while the upper transistor plays the role of the switch applying a positive voltage to the DUT. In consequence, the output capacitance of the lower transistor is charged via the upper transistor. There is no resistor in series to limit the current slope, but the gate resistor R_G is applied to control the switching speed and peak of the charging current.
An example of the waveforms is presented in Fig. 3, obtained for the CAB425M12XM3 power module. At the beginning of the process, v_{DS} is low, and the capacitance shows maximum values; therefore, the charging current rises fast and reaches peak value when the v_{DS} slope becomes linear. Then, while the voltage increases, the output capacitance drops and the charging current is reduced. Note that a similar current also discharges the capacitances of the upper transistors. At the end of the test, the v_{DS} slope becomes non-linear again, most likely, due to increased capacitance of the upper transistor. All in all, the single pulse takes a few microseconds, and the recorded voltage and current waveforms are employed to perform the calculations:

$$C_{oss} = i_{coss}\frac{dV_{DS}}{dt} \tag{1}$$

The calculation of (1) based on the waveforms in Fig.3 was conducted in Matlab, and the obtained C_{OSS}-V characteristic is shown in Fig.4. The dashed line presents the characteristic of the power module extracted from the datasheet [18]. Despite minor differences in a few areas, the method provides accurate and realistic C_{OSS}-V characteristic and may be applied to other power modules.

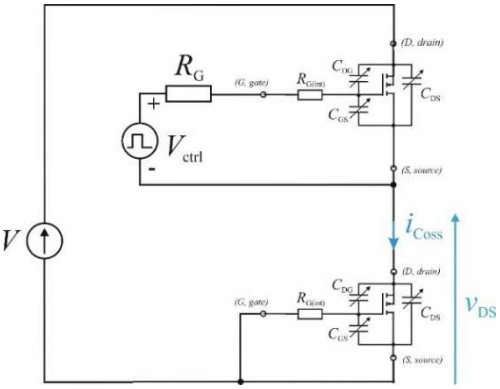


Fig. 2: Half-bridge test setup for the Coss-V characteristic measurements of the SiC power module.

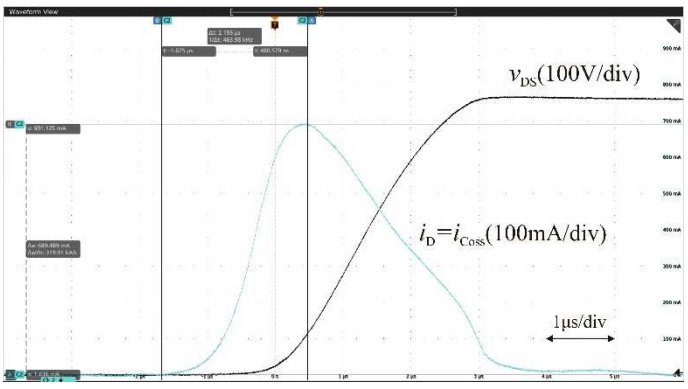


Fig. 3: Waveform of the drain current and drain-source voltage during a test of CAB425M12XM3.

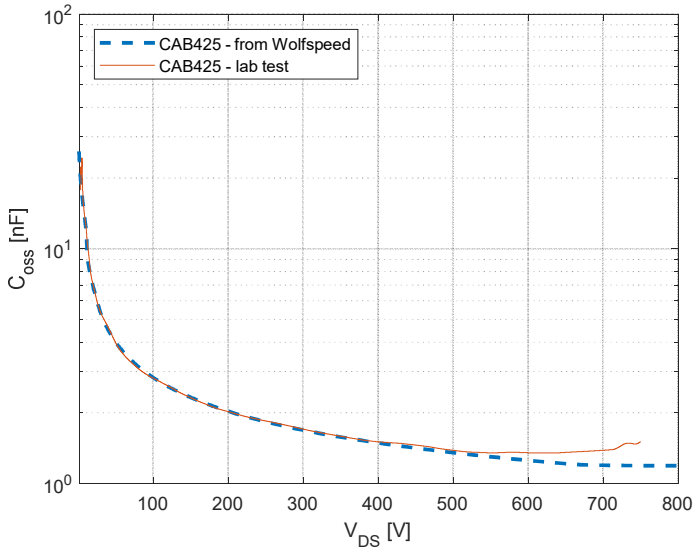


Fig. 4: C_{OSS}-V characteristics for CAB425 – datasheet and measured.

Tests of the 1.7kV/900A module

As the 1.7kV/900A SiC power module is the focus of this paper, the proposed method is employed to extract the C_{OSS}-V characteristics for this module. The test setup was the same as presented in Fig.2, but different values of the supply voltage V_{DC} and gate resistor $R_{G(ext)}$ were employed. The shape of the current and voltage waveforms in Fig.5 is similar to that observed in Fig.3, however, the C_{OSS} is higher and the peak charging current reaches almost 1.8 A. It can be also seen that the process takes more time. Again, with the described methodology, the C_{OSS}-V characteristic was determined for the tested MSM900FS17ALT, and the results are shown in see Fig. 6. Moreover, the Q_{OSS} can be integrated from the current waveform as presented in Fig.5 where the charge was approximately 11.3 µQ.

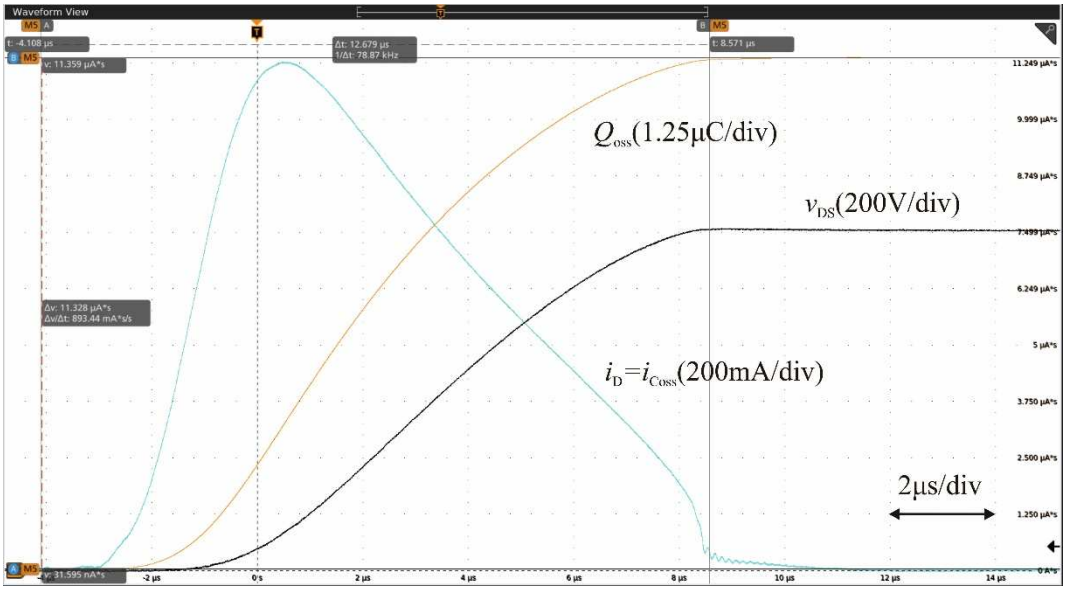


Fig. 5: Waveform of the drain current and drain-source voltage during test of MSM900FS17ALT.

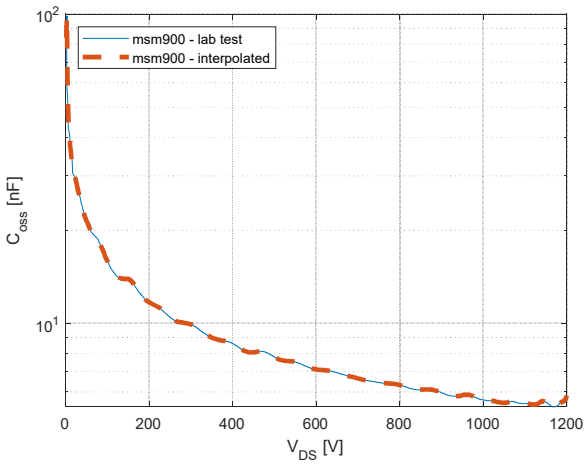


Fig. 6: Measured C-V characteristics for MSM900FS17ALT

Estimation of the i_{COSS} and i_{CH}

The MSM900FS17ALT has been arranged in a half-bridge circuit supplied from an 850V source and loaded with an inductive load (3x114uH/100A in parallel), as presented in Fig.7. Then, the transistors were controlled to generate a square voltage wave in the load with a variable switching frequency up to 25 kHz to obtain a different amplitude of the load current. These conditions lead to a triangle shape of the load current and switching conditions similar to those in soft-switched DC-DC converters. In particular, the transistors perform turn-on at zero voltage and turn-off at peak load current. Thus, most power losses appear during the turn-off event, twice per single switching period. In the circuit in Fig.7, the drain-source voltage and drain current waveforms were measured with the high-bandwidth voltage probe (P5200A) and Rogowski coil. Examples of the waveforms are presented in Fig.8 and Fig.10 for $R_{G(EXT)}$ = 3.3 Ω and without an external gate resistor, respectively, for different switched currents. The switching process is faster for the higher current and lower gate resistance; the same observation can be made for the oscillations – they become more severe for the higher current and lower gate resistance.

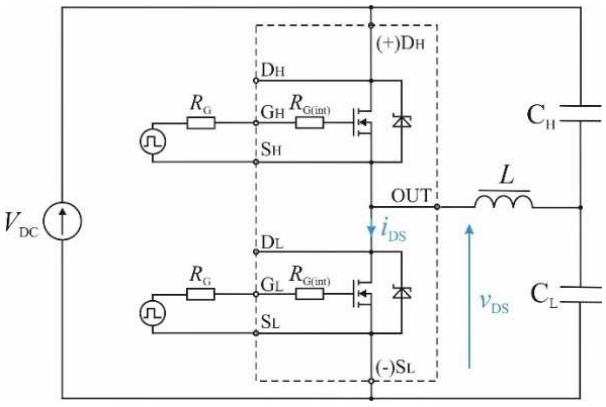


Fig. 7 Scheme of the half-bridge circuit with inductive load.

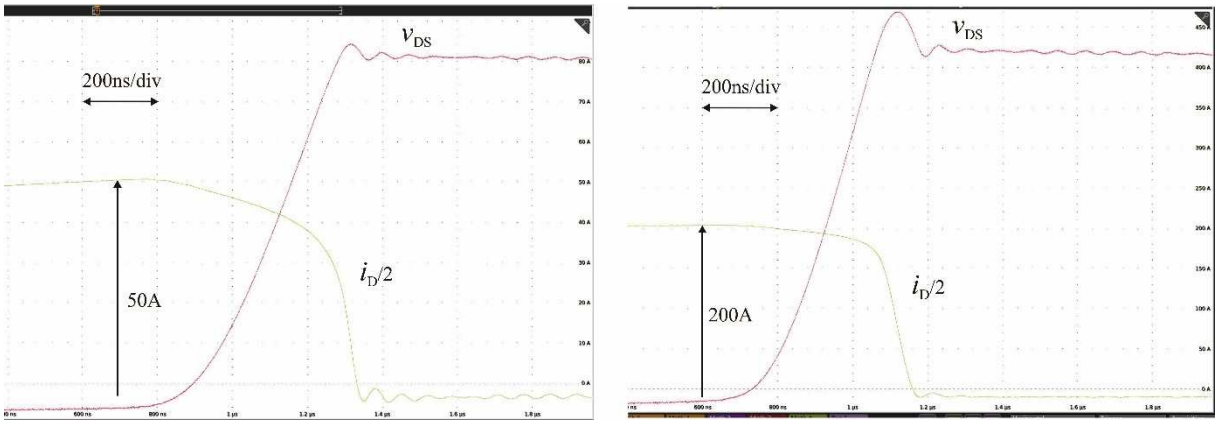
The C_{OSS}-V characteristic determined before has been employed to calculate the capacitive current i_{COSS} during the switching process as:

$$i_{coss} = C_{oss}(V_{DS})\frac{dV_{DS}}{dt} \tag{2}$$

also using the derivative of the drain-source voltage dV_{DS}/dt. In order to take into account the voltage drop in the stray inductance inside the power module, and therefore obtain more accurate results, V_{DS} in (2) was replaced by the internal $V_{DS}(i)$ calculated as:

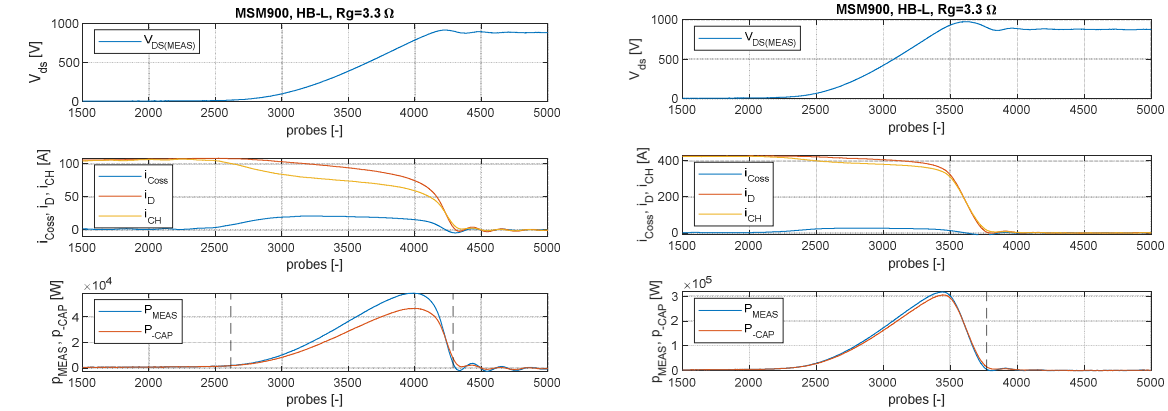
$$V_{DS(i)} = V_{DS} + L_S\frac{di_D}{dt} \tag{3}$$

Where L_s is half of the internal module inductance provided by the datasheet. The obtained results are presented in Fig. 9 and Fig.11 for $R_{G(EXT)}$ = 3.3 Ω and without an external gate resistor, respectively.



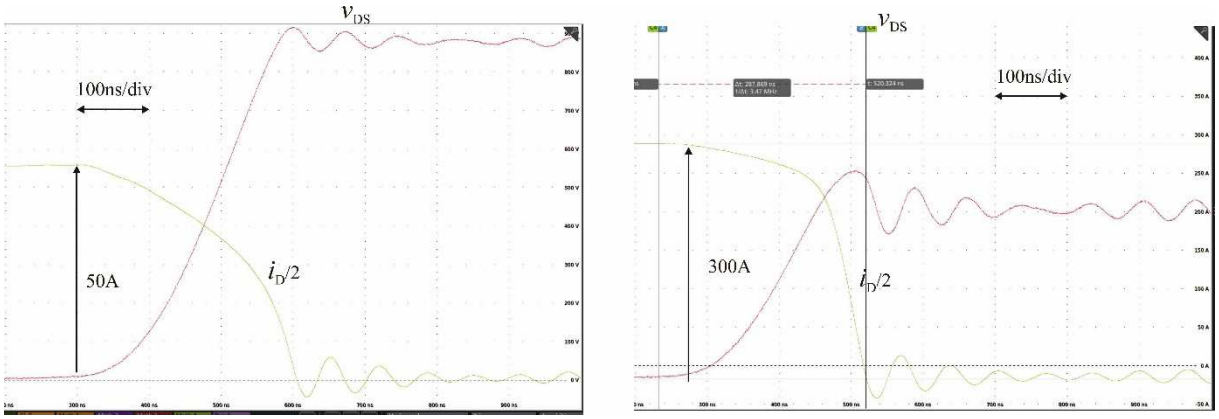
(a) (b)

Fig. 8 Turn-off process for $R_{G(EXT)}$ = 3.3Ω at 850V and 100A (a) and 400A (b)



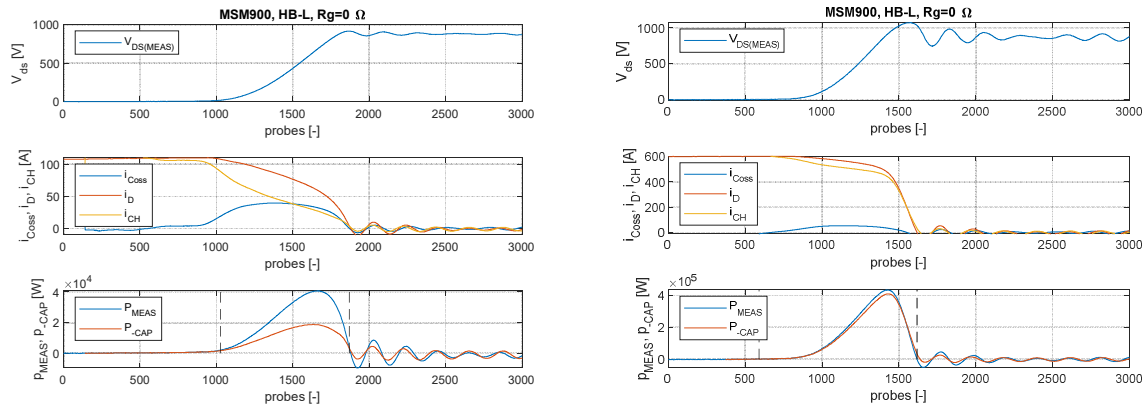
(a) (b)

Fig. 9 Estimation of the i_{COSS} and i_{CH} for $R_{G(EXT)}$ = 3.3Ω at 850V and 100A (a) and 400A (b)



(a) (b)

Fig. 10: Turn-off process for $R_{G(EXT)}$ = 0Ω at 850V and 100A (a) and 600A (b)



(a) (b)

Fig. 11: Estimation of the i_{COSS} and i_{CH} for $R_{G(EXT)} = 0\Omega$ at 850V and 100A (a) and 600A (b)

Discussion

Closer analysis of the i_{COSS} waveforms presented in Fig. 9 and Fig.11 shows that they are almost independent on the switched drain current. The slight dependency is caused by a faster switching at the higher current. Major impact on the shape of the i_{COSS} has the decrease of the gate resistance resulting in much higher switching speed. In particular, the peak value of the i_{COSS} is higher for more rapid switching. Both observations agree that i_{COSS} is mainly the result of the charge displacement related to the changes in the drain potential. For the cases shown in Fig.9 and Fig.11 but also two more gate current values ($R_{G(EXT)} = 1.6\ \Omega$ and $R_{G(EXT)} = 1\ \Omega$), the waveforms of i_{COSS} were integrated to determine the charge Q_{OSS} - see results in Fig. 12. The values should be constant but vary between 8.9 and 9.7 µC (~9% of the total error), which may be considered an acceptable value resulting from the measurement mismatches. They rise with the switched current for all cases, which is most likely, a result of higher voltage overshoot (increasing with the switched current and decreasing with the gate resistance). Note that values for the same switched currents show minimal differences, thus, the error results from the measurements in the half-bridge circuit rather than from the obtained Coss-V characteristic.

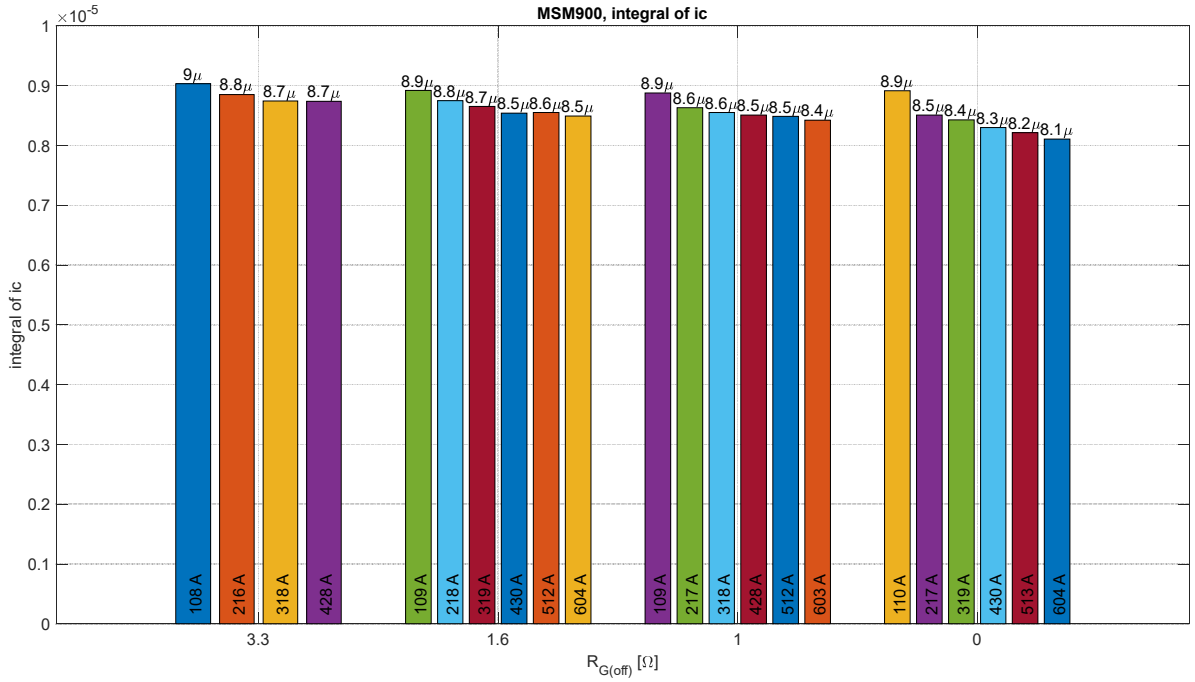


Fig. 12 Calculated Q_{OSS} for all tested cases.

Conclusion

This paper presents a novel method of C_{OSS}-V characteristics for SiC power modules. The main advantage is a simple application within the half-bridge module without additional effort – a low power high-voltage power supply and typical voltage and current probes are necessary. The setup is very similar to that required for double-pulse tests and power loss characterization of power devices. The test for the 1.2kV/425A module shown very good agreement with the C_{OSS}-V characteristic provided by the manufacturer, and the method was applied to the 1.7kV/900A module, whose datasheet is unavailable. Based on the measured characteristic, the capacitive current i_{COSS} has been calculated for this same module operating in the continuous mode at 850V at different switching speeds with currents up to 600A and switching frequencies up to 25 kHz. Then, the Q_{OSS} was determined for all cases. Under the assumption that Q_{OSS} should be constant for all tested cases, the authors have determined errors of the whole procedure on the level of +/-4.5%. It is very possible, that most of the error comes from the different voltage overshoots across the parasitic inductances. All in all, for the fast switching SiC power devices, this is an acceptable value to increase the accuracy of power losses estimation of soft-switched DC-DC converters.

References

[1] R. Chen, S. Shi, C. Zhang and W. Shi, "11 kW High-efficiency bidirectional CLLC converter with 1200 V SiC MOSFET," PCIM Asia 2021; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, 2021, pp. 1-9.

[2] Z. Lu *et al*., "Medium Voltage Soft-Switching DC/DC Converter With Series-Connected SiC MOSFETs," in *IEEE Transactions on Power Electronics*, vol. 36, no. 2, pp. 1451-1462, Feb. 2021, doi: 10.1109/TPEL.2020.3007225.

[3] I. Villar, U. Iruretagoyena, A. Rujas, A. Garcia-Bediaga and I.P. de Arenaza, "Design and implementation of a sic based contactless battery charger for electric vehicles", *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2015.

[4] A. Rodriguez, I. Ayarzaguena, I. Larranzabal, J. Najera, D. Ortega, A. Pulido, M. R. Rogina, "Design and operation of a DC/DC converter to integrate energy storage into a railway traction system", *2021 23rd European Conference on Power Electronics and Applications (EPE'21 ECCE Europe)*, 2021

[5] M. Haider et al., "Analytical Calculation of the Residual ZVS Losses of TCM-Operated Single-Phase PFC Rectifiers," in *IEEE Open Journal of Power Electronics*, vol. 2, pp. 250-264, 2021

[6] B. Agrawal, M. Preindl, B. Bilgin and A. Emadi, "Estimating switching losses for SiC MOSFETs with non-flat miller plateau region," *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2017, pp. 2664-2670.

[7] X. Li *et al*., "Achieving Zero Switching Loss in Silicon Carbide MOSFET," in *IEEE Transactions on Power Electronics*, vol. 34, no. 12, pp. 12193-12199, Dec. 2019.

[8] N. Fritz, G. Engelmann, A. Stippich, C. Lüdecke, D. A. Philipps and R. W. D. Doncker, "Toward an In-Depth Understanding of the Commutation Processes in a SiC mosfet Switching Cell Including Parasitic Elements," in *IEEE Transactions on Industry Applications*, vol. 56, no. 4, pp. 4089-4101, July-Aug. 2020.

[9] Y. Xie, C. Chen, Y. Yan, Z. Huang and Y. Kang, "Investigation on Ultralow Turn-off Losses Phenomenon for SiC MOSFETs With Improved Switching Model," in *IEEE Transactions on Power Electronics*, vol. 36, no. 8, pp. 9382-9397, Aug. 2021.

[10] J. Rabkowski, M. Zdanowski, F. Gonzalez-Hernando, I. Villar, U. Larrañaga, "Experimental Study on Turn-off Process of Medium Voltage SiC MOSFET Modules", *PCIM Europe*, 2022.

[11] MSM900FS17ALT datasheet.

[12] P. Ralston, T.H. Duong, Nanying Yang, D.W. Berning, C. Hood, A.R. Hefner, et al., "High-Voltage capacitance measurement system for SiC power MOSFETs", *Energy Conversion Congress and Exposition 2009. ECCE 2009. IEEE*, pp. 1472-1479, 20–24 Sept. 2009.

[13] T. Funaki, N. Phankong, T. Kimoto and T. Hikihara, "Measuring Terminal Capacitance and Its Voltage Dependency for High-Voltage Power Devices", *Power Electronics IEEE Transactions on*, vol. 24, no. 6, pp. 1486-1493, June 2009.

[14] X. Song, A. Q. Huang, M. Lee and G. Wang, "A dynamic measurement method for parasitic capacitances of high voltage SiC MOSFETs," *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2015, pp. 935-941, doi: 10.1109/ECCE.2015.7309788.

[15] Cristino Salcines, Ingmar Kallfass, Hisao Kakitani, Atsushi Mikata, "Dynamic characterization of the input and reverse transfer capacitances in power MOSFETs under high current conduction", *Applied Power Electronics Conference and Exposition (APEC) 2016 IEEE*, pp. 2969-2972, 2016.

[16] M. Samizadeh Nikoo, A. Jafari, N. Perera and E. Matioli, "Measurement of Large-Signal C_{oss} and C_{oss} Losses of Transistors Based on Nonlinear Resonance," in *IEEE Transactions on Power Electronics*, vol. 35, no. 3, pp. 2242-2246, March 2020, doi: 10.1109/TPEL.2019.2938922.

[17] Wei Xu, Zhicheng Guo, S. Milad Tayebi, Sanjay Rajendran, Ao Sun, Ruiyang Yu, Alex Q. Huang, "Hardware Design and Demonstration of a 100kW 99% Efficiency Dual Active Half Bridge Converter Based on 1700V SiC Power MOSFET", *Applied Power Electronics Conference and Exposition (APEC) 2020 IEEE*, pp. 1367-1373, 2020.

[18] CAB425M12MX3 datasheet.