

Cascaded H-Bridge Converter Designs for Future Short-Range All-Electric Aircraft Propulsion

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Keywords

«Cascaded H-Bridge», «DC-AC converter», «Modular converter», «Green aviation»

Abstract

The cascaded H-bridge converter topology makes a high voltage power supply structure with distributed energy storage for all-electric aircraft possible. In this paper, different cascaded H-bridge converter topologies are compared regarding mass and efficiency, with a focus on the requirements for the energy storage in a battery-powered short-range aircraft.

Introduction

The ongoing electrification of mobility has reached the aviation sector, where multiple research projects are evaluating the possibilities for electrifying aircraft propulsion [1]. The document *Flightpath 2050* expects to see short-range all-electric aircraft (SAEA) as an integral part of the aviation market by 2050 [2]. While for mid-range applications, hybrid concepts are suggested, fully battery-powered all-electric aircraft are being considered for short-range applications [3]. There are different concepts concerning how the onboard power supply can be realized, but all have a common design goal, which is the mass optimization of the whole propulsion system while maintaining a high efficiency. While converter topologies for a single DC backbone have been studied in [4], this paper focuses on a decentralized approach, where the power conversion system does not rely on a centralized battery system, but instead uses multiple battery packs which are distributed across separate modules. One feasible inverter topology is the cascaded H-bridge Converter (CHB), which is examined in this paper in different module variants. The CHB supplies each phase of the machine independently, which results in an H-bridge input current that consists of superimposed DC and AC components. The AC component of the current increases the root-mean-square (RMS) value, which results in higher losses in the internal battery resistance compared to the pure DC current, leading to higher battery temperatures which may negatively affect the battery lifetime [5]. The increased losses furthermore reduce the system efficiency, which results in a higher battery mass.

For this reason, it is considered impractical to directly connect the module battery to the H-bridge and instead additional circuitry is needed to filter the battery current.

To give an example of how a filtered battery current influences the battery mass, a factor $r_I = \frac{I_{\text{bat}}}{\bar{i}_{\text{bat}}}$ is introduced describing the relationship between the RMS current I_{bat} and the DC component \bar{i}_{bat} . Two different values for r_I are compared in a small calculation example, which is based on the reference mission profile from [4], where a battery energy of about 10MWh is needed. Assuming a constant discharge, the battery output power is 2.5MW. Without any filter circuitry, the factor r_I would be 1.31 at a power factor of $\cos\varphi = 0.84$. The battery is assumed to have an energy density of 700 Wh kg^{-1} , which is proposed in [6] as a feasible value for future battery technologies. To consider the losses at the internal battery resistance caused by I_{bat} , the battery resistance is estimated for the resulting parallel and serial cell stack at an assumed battery voltage of 1kV. Due to the lack of data on the internal resistance in ongoing research on new cell technologies, the internal battery resistance is estimated based on a state-of-the-art automotive lithium-ion battery cell [7] which leads to a battery resistance of $11.7\text{ m}\Omega$. With these parameters, an r_I of 1.31 would lead to a battery that is 286kg heavier than that necessary with an r_I of 1.01, which can be achieved with appropriate filter circuitry.

Since an SAEA is expected to be realized by 2050, higher blocking voltages in the upcoming generations of SiC MOSFETs can be expected. This is accounted for in a scalable semiconductor model which is presented in [4] and used in this work.

The CHB variants considered in this paper either contain a single-stage LC filter (CHBSLC), a dual-stage LC filter (CHBDLC), a DC-DC converter (CHBDCDC) or an interleaved DC-DC converter (CHBIL). As the design parameters for the battery and machine are not yet fully specified, the module variants are compared in two parameter studies to give an idea of the inverter designs that can be expected. Regarding the battery, the cell voltage factor $r_{uc} = \frac{v_{c,\text{max}}}{v_{c,\text{min}}}$, resulting from the different cell voltages at the highest and lowest states of charge (SoC), and the factor r_I are key parameters in the inverter design. The influence of these two battery-related parameters on the inverter design is investigated in the first parameter study. Moreover, the design of the passive components of the inverter is strongly affected by the fundamental machine frequency f_1 , and the switching frequency of the DC-DC converter f_{dcdc} . Therefore these two parameters are varied in the second parameter study.

Converter Topology

Fig. 1 shows the topology of the propulsion system for a propeller that is assumed to be driven by a permanent magnet synchronous machine (PMSM). The inverter supplying the PMSM is a CHB, whose phase legs contain a number of n_{mod} modules connected in series, where i_{ph} is the phase current and v_{mod} is the module output voltage. The first module of the first phase is depicted in detail with its H-bridge (blue box), a filter circuit dependent on the module design (gray boxes), and a battery. For simplicity, the other two phases are represented by ideal voltage sources. To modulate the phase voltage v_{ph} , a phase-shifted pulse-width modulation is assumed, whereby each module receives the same sinusoidal reference signal and a shifted carrier signal, resulting in a switching frequency of $f_{s,\text{eff}}$ in v_{ph} . Neglecting the switching components, the H-bridge input current

$$i_d = \frac{\hat{M} i_{\text{ph},1}}{2} (\cos(\varphi_1) - \cos(2\omega_1 t + \varphi_1)) \quad (1)$$

has a second harmonic component that oscillates at twice the fundamental angular frequency $2\omega_1$ and furthermore depends on the modulation index $M = \frac{\hat{v}_{\text{mod},\text{set}}}{v_d}$ and the load angle φ_1 [8]. Here, $\hat{v}_{\text{mod},\text{set}}$ denotes the module's setpoint voltage and v_d the module's input voltage.

The design of the CHB modules follows the calculations in [9], where the sum of all H-bridge input voltages in one phase is defined to be greater than $v_{\text{ph},\text{max}} = a_{\text{res}} \sqrt{2} V_{\text{ph},N}$, where $V_{\text{ph},N}$ is the RMS phase voltage of the machine and a_{res} is a safety factor which accounts for deviations in the control system. The change of the H-bridge's input voltage due to the SoC variation in the battery needs to be accounted for, since it determines the maximum operating voltage of the MOSFETs. The semiconductor model

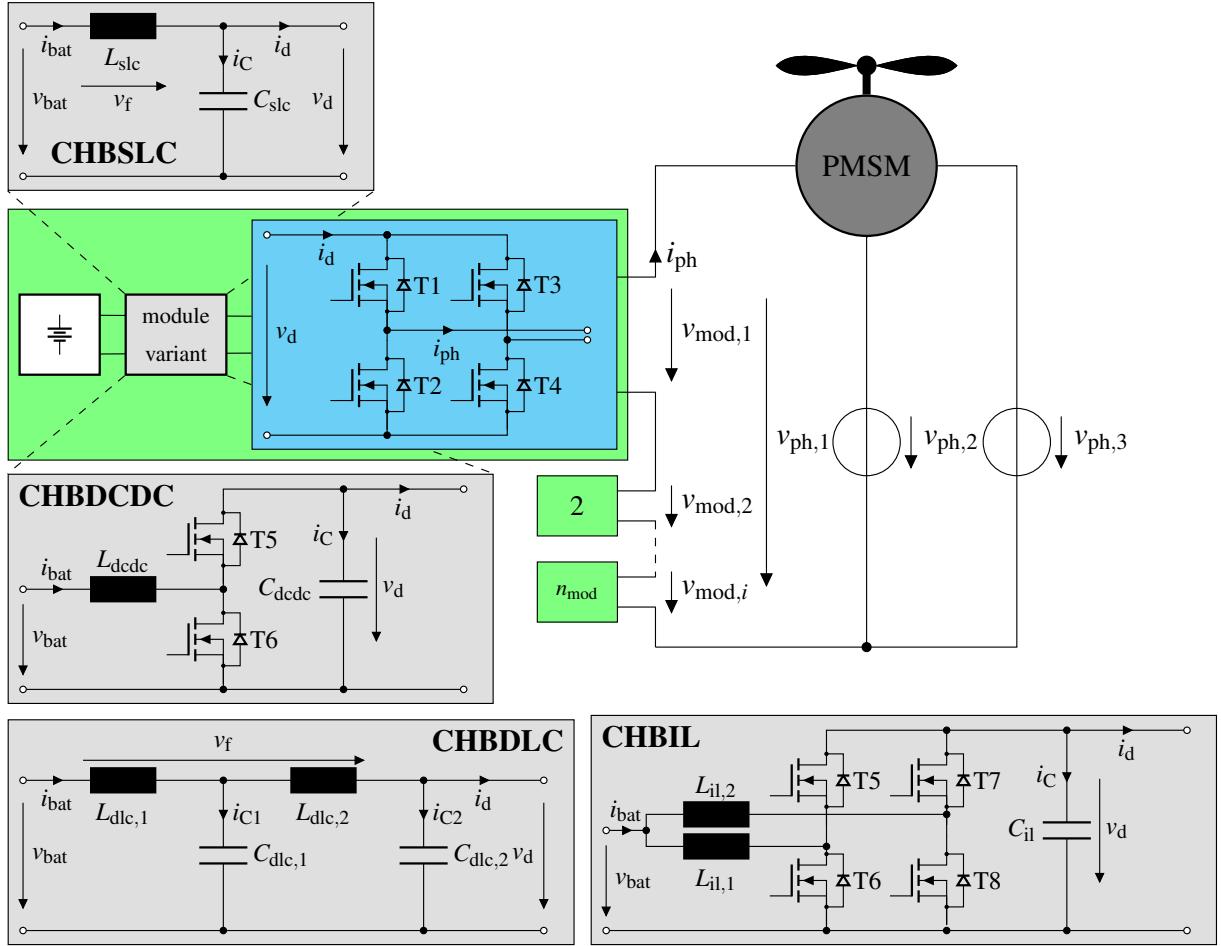


Fig. 1: Topology overview of the propulsion system with a three-phase PMSM supplied by a CHB inverter. The first phase of the CHB containing n_{mod} modules is shown in detail with the H-bridge (blue box) and the CHBSLC, CHBDLC, CHBDCDC, and CHBIL ($n_{\text{IL}} = 2$) module variants in the gray boxes.

implemented allows for an arbitrary breakdown voltage, which is why n_{mod} does not depend on v_{ph} or the battery voltage. Due to cosmic radiation, which can lead to critical failures, the maximum blocking voltage of the MOSFETs is reduced by a derating factor k_{der} [10].

Module Variants

Different module variants can be used to compensate for the power variation in i_d . In this section, the modules of the different CHB variants CHBSLC, CHBDLC, CHBDCDC, and CHBIL are described. To account for the highest possible currents, the module designs are carried out for the lowest SoC of the battery.

LC Filter Variants

The LC filter variants considered in this paper are a single-stage LC filter (SLC) and a dual-stage LC filter (DLC). In both these variants, the H-bridge input voltage is $v_d = v_{\text{bat}} - v_f$, where v_f denotes the voltage drop across the filter inductors L_{slc} or $L_{\text{dlc},1}$ and $L_{\text{dlc},2}$. The filters are designed to achieve the necessary attenuation at the frequency of the second harmonic component in i_d so that the desired value for r_I in the battery current is met. As an additional design constraint, a maximum permissible value for v_f must not be exceeded. The expression for the resonant frequencies of each filter are given in (2) and (3) [11]. Since the DLC has four energy-storage components, but the number of constraints (r_I and v_f) does not increase, it is assumed that both filter capacitors and inductors have the same component values $L_{\text{dlc},1} = L_{\text{dlc},2} = L_{\text{dlc}}$ and $C_{\text{dlc},1} = C_{\text{dlc},2} = C_{\text{dlc}}$. Thus, (3) can be simplified to give (4). The inductance and capacitance combination which meets the design constraints and results in the lowest mass is chosen.

Fig. 2 shows the qualitative bode plots of the transfer functions of an SLC (blue) and a DLC (red) with their corresponding asymptotic approximations (colored dashed lines). It might be assumed that the DLC always results in lower capacitance and inductance values, considering only the asymptotic approximations, since higher resonant frequencies are possible with the same attenuation. However, this does not apply for frequencies to be attenuated close to the resonant frequencies. The horizontal and vertical black dashed lines mark the design point for the filters, where the attenuation of A_z has to be achieved at the specified frequency $\omega_z = 2f_1$ to meet a given r_1 factor. From the asymptotes, the resonant frequencies and the achieved attenuation of $-40\text{dB}/\text{dec}$ for the SLC and $-80\text{dB}/\text{dec}$ for the DLC for frequencies greater than the respective resonant frequencies can easily be deduced. Comparing the transfer functions to their asymptotic approximations makes it obvious that the DLC attenuation is still further away from its potential indicated by the asymptote than the SLC attenuation. This indicates that, for the given combination of ω_z and A_z in Fig. 2, the use of a DLC may not be the optimal choice for a mass-optimized filter. Depending on the required attenuation for a given ω_z , the positions of the filter resonant frequencies vary. With decreasing A_z , the filter resonances shift to lower frequencies at different rates for SLC and DLC. If A_z were to decrease, the resonant frequencies of the DLC $\omega_{0,\text{dlc},1/2}$ would shift less to lower ω due to its higher attenuation than the SLC resonant frequency $\omega_{0,\text{slc}}$. This means that for a certain value of A_z , $\omega_{0,\text{slc}}$ would be smaller than both values $\omega_{0,\text{dlc},1/2}$ and therefore the DLC might prove to be the lighter filter variant.

$$\omega_{0,\text{slc}} = \frac{1}{\sqrt{L_{\text{slc}}C_{\text{slc}}}} \quad (2)$$

$$\omega_{0,\text{dlc},1/2}^2 = \frac{A + B + C \pm \sqrt{(A + B + C)^2 - 4AC}}{2AC} \quad (3)$$

and $A = L_{\text{dlc},1}C_{\text{dlc},1}, B = L_{\text{dlc},1}C_{\text{dlc},2}, C = L_{\text{dlc},2}C_{\text{dlc},2}$

$$\omega_{0,\text{dlc},1/2} = +\sqrt{\frac{3 \pm \sqrt{5}}{2L_{\text{dlc}}C_{\text{dlc}}}} \quad (4)$$

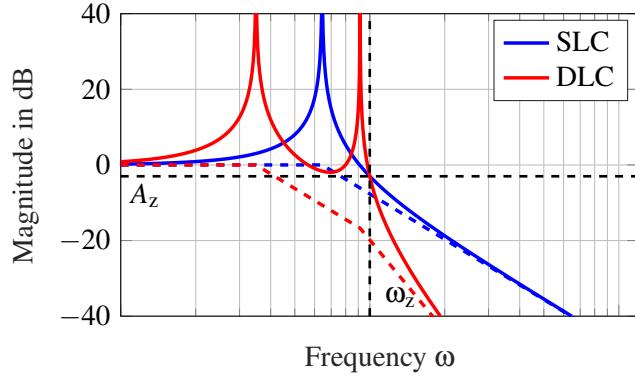


Fig. 2: Qualitative bode plots and their asymptotic approximations (colored dashed lines) for the LC filter variants for a given attenuation A_z and frequency ω_z

DC-DC Converter

For the DC-DC converter, an ideal control is assumed, which completely compensates for the second harmonic component of i_d . Only the current ripple Δi_{bat} originating from the switching of the DC-DC converter's semiconductors is still present in the battery current. Following the DC-DC converter design presented in [9] and [12], the capacitance of the module capacitor C_{dcdc} is designed for a voltage variation of $\pm 10\%$ and has to buffer the energy fluctuation caused by the second harmonic component

of the inverter input current i_d . Since Δi_{bat} directly influences the RMS value of the battery current, the given value of r_I determines Δi_{bat} and thus the inductance

$$L_{\text{dcdc}} = \frac{v_{\text{bat,min}} D_{\max}}{\Delta i_{\text{bat}} f_{\text{dcdc}}}.$$
 (5)

In (5), D_{\max} denotes the maximum duty cycle that may occur at the minimum battery voltage $v_{\text{bat,min}}$ and f_{dcdc} is the switching frequency of the DC-DC converter. Since the second harmonic component of the battery current is controlled by the DC-DC converter, f_{dcdc} needs to be sufficiently high. The influence of f_{dcdc} is subject to investigation in the following parameter study.

Interleaved DC-DC Converter

The CHBIL consists of multiple parallel DC-DC converters with a corresponding number of inductors, where the battery current is divided into the separate interleaved phase legs, leading to a reduced current in each single inductor. The inductance value of each interleaved phase is determined using (5) and is therefore the same as for the simple DC-DC converter. The module capacitor C_{il} is dimensioned the same as in the CHBDCDC. The MOSFETs in each interleaved phase leg are controlled with phase-shifted carrier signals at a frequency of f_{dcdc} . As depicted in Fig. 3, the additional interleaved phases further reduce the battery current ripple Δi_{bat} , and therefore the r_I value, due to phase-shifted control of the separate interleaved phase legs [13]. The resulting factor $r_{I,n_{\text{IL}}}$ for a CHBIL is determined using (6), where n_{IL} is the number of interleaved phase legs and D is the duty cycle. For all DC-DC converter variants, only continuous conduction mode is considered.

$$r_{I,n_{\text{IL}}} = \sqrt{\frac{1}{12} \left(\frac{\Delta i_{\text{bat},n_{\text{IL}}}}{\bar{i}_{\text{bat}}} \right)^2 + 1} \quad \text{and} \quad \Delta i_{\text{bat},n_{\text{IL}}}(D) = \frac{1}{n_{\text{IL}}} \frac{|\sin(n_{\text{IL}}\pi D)|}{|\sin(\pi D)|} \Delta i_{\text{bat},n_{\text{IL}}=1}$$
 (6)

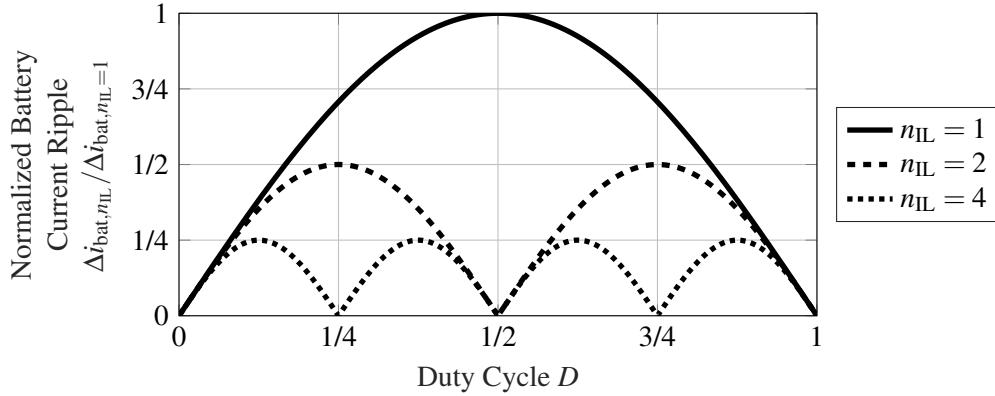


Fig. 3: Normalized battery current ripple vs. duty cycle as a function of the number of interleaved phase legs [13]

CHB Loss Calculation

The losses in the CHB are dissipated by the semiconductors in the H-bridge and the DC-DC converter(s) as well as by the passive components. The conduction loss calculation for the H-bridge semiconductors follows the approach detailed in [14] with minor adjustments, so that the losses can be assigned to a single MOSFET or body diode. The switching loss calculation is implemented according to [4] with slight modifications regarding the switching losses of the DC-DC converter MOSFETs. The switching losses of the H-bridge semiconductors are calculated according to [4], neglecting the current ripple of the machine current i_{ph} , because a sufficiently high machine inductance is assumed. For the DC-DC converter, however, the current ripple can be up to twice its DC value on the verge of discontinuous current mode. Hence, the calculation in [4] is modified to take the current ripple of the DC-DC converter

into account. As for the passive components, the scalable component models from [4] are used to obtain the equivalent series resistance of the capacitor and the ohmic and magnetic losses of the inductor.

Parameter Studies

The parameter studies will give an impression of how certain design parameters influence the respective CHB inverter designs with respect to the resulting mass, efficiency, and power density. Power losses and efficiencies are always calculated for the worst-case operating point, which occurs at the lowest battery SoC. To determine n_{mod} , the inverter design is calculated for $2 \leq n_{\text{mod}} \leq 20$ and the design yielding the highest efficiency is chosen. The switching frequency of the H-bridge MOSFETs in each module f_s is adjusted according to n_{mod} , so that the resulting switching actions in v_{ph} always correspond to an effective switching frequency $f_{s,\text{eff}}$, leading to $f_s = \frac{f_{s,\text{eff}}}{2n_{\text{mod}}}$. Although the CHBDLC has been studied, it will not be discussed in the parameter studies, since it proved to be less efficient than the CHBSLC and did not reach such high power densities. As assumed before, it confirms that the higher DLC attenuation could not be used to benefit mass reduction because the total mass of all passive components of the DLC exceeds the SLC passive components' mass.

The parameter studies are based on the reference aircraft mission profile from [4], where two PMSMs are assumed, resulting in a maximum electrical apparent power of 2.1 MVA for one inverter. Additional parameters assumed for the case studies are listed in Table I. Note that the module capacitor voltage ripple of the CHBSLC and the DC-DC converter variants differ. This is due to the different effects a voltage ripple increase has on the resulting module mass. Since for variants containing a DC-DC converter, the capacitance decreases with rising voltage ripple, an increase in voltage ripple reduces the overall module mass. A voltage ripple of $\pm 10\%$ is considered acceptable here. As for the CHBSLC, an increase in $v_{f,\text{max}}$ both leads to an increased filter inductance and a decreased filter capacitance. The resulting mass decrease of the capacitor does not balance the mass increase of the inductor, therefore a smaller capacitor voltage ripple gives a mass advantage in the case of the CHBSLC.

Table I: Parameters for both case studies

Inverter power	S_{el}	2.1 MVA
Machine phase voltage (RMS)	$V_{\text{ph},N}$	1.15 kV
Power factor	$\cos(\varphi_1)$	0.84
Derating factor	k_{der}	60 %
Effective switching frequency	$f_{s,\text{eff}}$	20 kHz
Max. filter voltage drop	$v_{f,\text{max}}$	2 % of v_{bat}

The contour plots in Fig. 4 show the variation of r_{uc} and r_{I} and the effects on efficiency, mass, and power density for the CHBSLC, CHBDCDC and CHBIL with $n_{\text{IL}} = 2$ or $n_{\text{IL}} = 4$ interleaved phase legs. For this case study, a fundamental machine frequency of $f_1 = 750\text{Hz}$ and a DC-DC converter switching frequency of $f_{\text{dcdc}} = 40\text{kHz}$ have been used.

A number of $n_{\text{mod}} = 2$ modules is calculated to be the most efficient choice for all CHBSLC design points. For the DC-DC converter variants, there are some design points that turn out to be more efficient with $n_{\text{mod}} = 3$. For the CHBDCDC, this is only the case for $r_{\text{uc}} = 1.17$ and $r_{\text{I}} = \{1.0006, 1.0062, 1.0073\}$. For the CHBIL with $n_{\text{IL}} = 2$, this is true for $r_{\text{uc}} < 1.37$ at most r_{IL} values, while for the CHBIL with $n_{\text{IL}} = 4$, this applies to all points.

The value of r_{uc} has a large impact on the CHBSLC mass, because the battery voltage is directly linked to the H-bridge input voltage via the LC filter. Since a large value of r_{uc} leads to higher maximum battery and capacitor voltages and the capacitor volume and ESR are proportional to the capacitor voltage, the capacitor mass increases accordingly. Therefore, a smaller r_{uc} leads to higher efficiency and lower mass. The r_{I} value marginally affects the efficiency, but a minimum for the CHBSLC mass is identified at $r_{\text{I}} \approx 1.015$. Two different effects increase the filter inductor mass for higher and lower values of r_{I} .

Lower r_I values lead to significantly larger inductance values and higher r_I values result in increased peak and RMS current values, both leading to an increased inductor mass. Therefore, at the design point $r_{uc} = 1.17$ and $r_I = 1.015$ a peak efficiency of 99.4% and a maximum power density of 11.7 kVA kg^{-1} are realized for the CHBSLC.

Looking at the CHBDCDC, its efficiency increases at larger r_I values as well as at smaller r_{uc} values, since both indirectly influence the inductance value L_{dcdc} (see (5)). For the CHBDCDC mass, a similar relation can be observed: it is lightest at the highest r_I and lowest r_{uc} values. As introduced before, the effective r_I values of the CHBIL variants are reduced (see (6)) and therefore reach a maximum of $r_I = 1.01$ and $r_I = 1.0006$ for $n_{IL} = 2$ and $n_{IL} = 4$, respectively. Comparing the efficiency, both the CHBDCDC and CHBIL inverter variants are less efficient than the CHBSLC. In terms of mass, the CHBDCDC and CHBIL are lighter than the CHBSLC for almost all parameter combinations, especially for larger r_I values. One reason for using the CHBIL variant was the presumed mass advantage compared to the CHBDCDC. Comparing the CHBDCDC and CHBIL with $n_{IL} = 2$, the assumption is confirmed: the CHBIL has a mass of 154 kg. However, a higher number of interleaved phase legs does not lead to a further mass reduction. This is due to the increased n_{mod} for the CHBIL with $n_{IL} = 4$. The CHBDCDC reaches a maximum power density of 12.8 kVA kg^{-1} at the smallest value for r_{uc} and $r_I = 1.019$, while the CHBIL with $n_{IL} = 2$ has a power density of 13.6 kVA kg^{-1} for the same r_{uc} and $r_I = 1.008$. Again, the CHBIL with $n_{IL} = 4$ does not reach such high power densities because of its higher n_{mod} . To verify

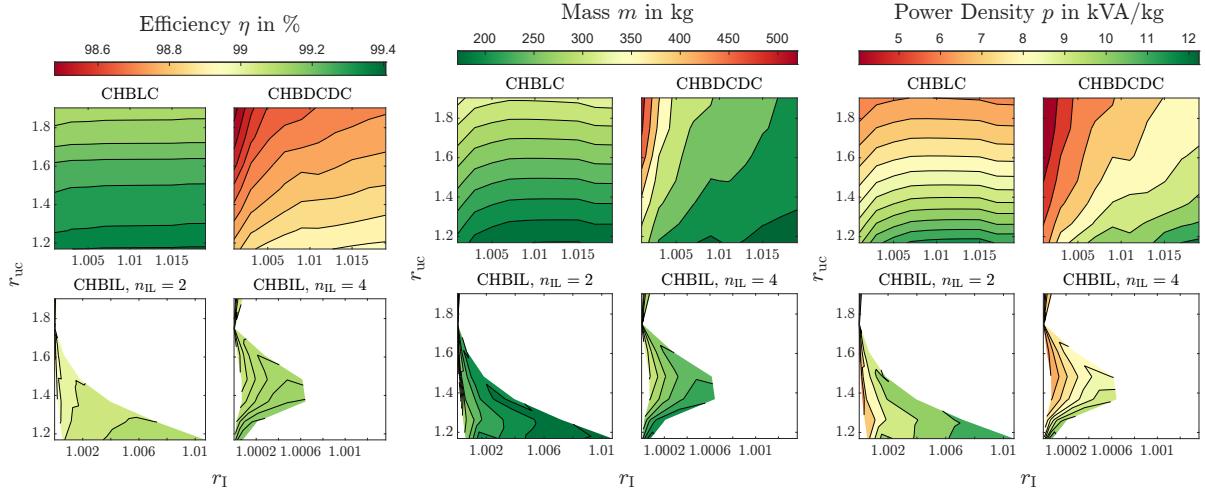


Fig. 4: Efficiency, mass, and gravimetric power density as a function of r_{uc} and r_I for a complete CHB and an apparent power of 2.1 MVA. The contour plot grid resolution in the r_I and r_{uc} direction is 10 by 7.

the analytically calculated results, a simulation of the CHBSLC was performed in Matlab Simulink, as it achieved the highest efficiency of 99.4 %. The semiconductors are modeled in PLECS and the PMSM is modeled as an independent sinusoidal current source. The simulated MOSFET voltages and currents together with the conduction losses and switching energies over one fundamental period of one H-bridge are shown in Fig. 5. Switching energies only occur in the positive half-wave of the MOSFET current, because it is assumed that during the negative half-wave, the integrated body diode fully conducts the current during interlock time, leading to zero-voltage switching. A comparison of the calculated and simulated losses of the H-bridge is shown in Table II. The main reason for the deviation between the calculated and simulated switching losses is the relatively low switching frequency f_s of the single semiconductors. Nevertheless, the analytical error for the total MOSFET losses compared to the simulated losses is below 4 %. At higher values of $f_{s,eff}$, each MOSFET performs more switching operations, resulting in greater agreement between the simulated and calculated losses.

Analogous to Fig. 4, the contour plots in Fig. 6 show the variation of the fundamental frequency f_1 and the DC-DC converter switching frequency f_{dcdc} and their effects on the efficiency, mass, and power density of each inverter type. A lithium-sulfur battery cell is assumed to be used, and a value of $r_{uc} = 1.37$ is taken from the manufacturer's datasheet [15]. Also, a maximum value of $r_I = 1.01$ is set, which

Table II: Comparison of the calculated and simulated H-bridge losses averaged over one fundamental period of one CHBIL module with $r_I = 1.015$, $r_{uc} = 1.17$, and $f_{s,eff} = 20\text{kHz}$

	Conduction Losses in W		Switching Losses in W	
	calculated	simulated	calculated	simulated
T1	484	497	39	34
T2	484	477	39	49
T3	484	500	39	42
T4	484	473	39	61

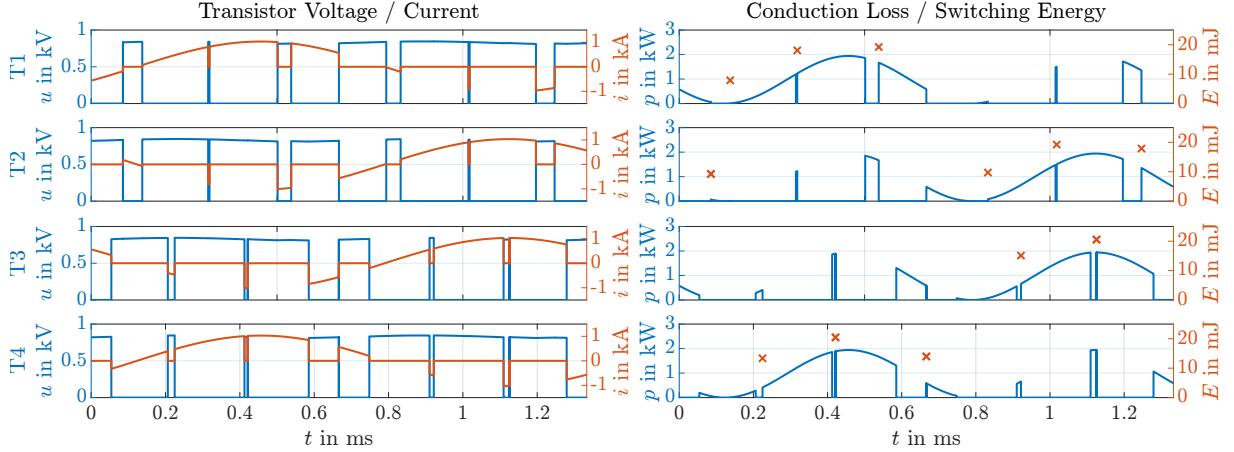


Fig. 5: Simulated MOSFET voltages and currents (left) and conduction losses and switching energies (right) for one H-bridge in a CHBIL inverter with $n_{mod} = 2$, $r_I = 1.015$, $r_{uc} = 1.17$, $f_{s,eff} = 20\text{kHz}$ and a switching frequency $f_s = 5\text{kHz}$ for each MOSFET

leads to reduced r_I values for the CHBIL variants of $r_{I,n_{IL}=2} = 1.0012$ and $r_{I,n_{IL}=4} = 1.0007$. While the CHBIL is most efficient for $n_{mod} = 2$ at all considered points, the CHBDCDC and CHBIL with $n_{IL} = 2$ have $n_{mod} = 2$ for $f_{dcdc} < 45\text{kHz}$ and $n_{mod} = 3$ for $f_{dcdc} > 45\text{kHz}$. The CHBIL with $n_{IL} = 4$ only uses $n_{mod} = 2$ for $f_{dcdc} < 35\text{kHz}$ and is more efficient with $n_{mod} = 3$ at all other frequencies. This is indicated by the dashed blue lines on the contour plots.

Efficiency, mass, and power density of the CHBIL are not affected by f_{dcdc} since no DC-DC converter is used, but at higher values of f_1 , the CHBIL mass is significantly reduced from 508 kg at $f_1 = 200\text{Hz}$ to 183 kg at $f_1 = 1\text{kHz}$. Consequently, the power density increases accordingly. This is because the resonant frequency of the LC filter in each module rises with f_1 and therefore the filter component mass decreases.

The efficiencies of the CHBDCDC and CHBIL variants are only marginally affected by a variation of f_1 . In contrast, the CHBDCDC efficiency strongly depends on f_{dcdc} . Higher values for f_{dcdc} lead to a decreased efficiency for all types containing a DC-DC converter. The abrupt changes in the course of the contour plots for the CHBIL variants, which are most pronounced on the mass and power density plots, are due to the increase of n_{mod} at values for f_{dcdc} of 35 kHz and 45 kHz, which leads to an increased inverter mass and a decreased power density. The overall inverter mass decreases with both increasing f_1 and increasing f_{dcdc} for all CHBDCDC and CHBIL variants because of two effects. First, the capacitor mass is inversely proportional to f_1 , which explains the mass reduction with rising f_1 . Second, the inductor mass is directly related to f_{dcdc} , which leads to decreasing inverter mass for higher values of f_{dcdc} . It can be observed that, for values of $f_1 \lesssim 400\text{Hz}$, a further increase in f_{dcdc} does not result in significant mass savings, since the capacitor mass is already dominant over the inductor mass. The same effect can be anticipated for values of $f_1 > 1\text{kHz}$ and decreasing f_{dcdc} . In this case, a further increase in f_1 would not save significant mass in the capacitor, since the inductor mass is dominant over the

capacitor mass at low f_{dcdc} .

Irrespective of the frequencies f_1 and f_{dcdc} , the CHBSLC is the most efficient inverter type, since there are no additional losses from a DC-DC converter. Especially for low f_1 , CHBDCDC and CHBIL inverter variants are lighter alternatives. When using the CHBIL variants at high f_{dcdc} , they are superior to the CHBSLC in terms of mass and power density.

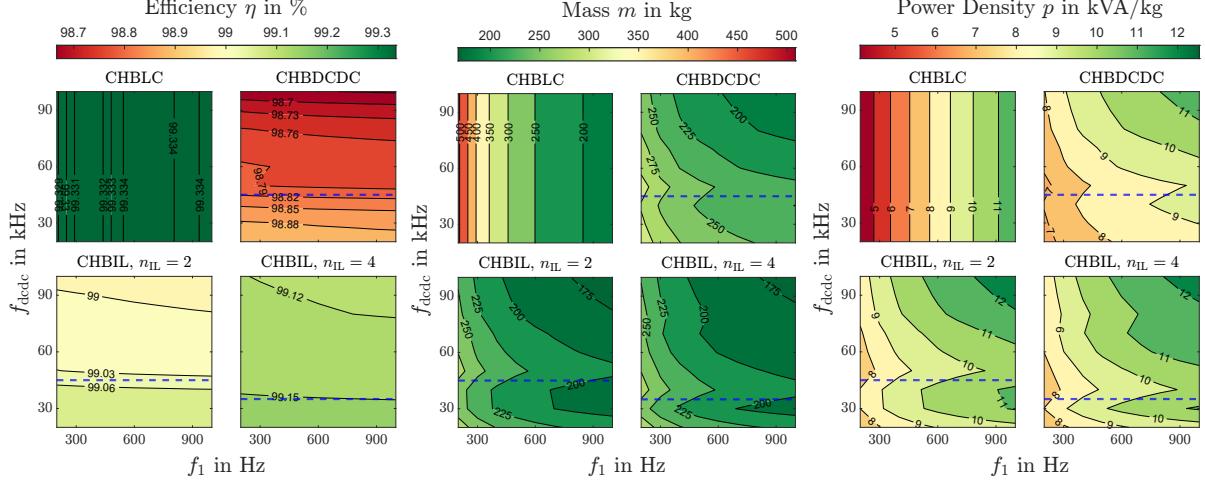


Fig. 6: Efficiency, mass, and gravimetric power density as a function of f_1 and f_{dcdc} for a complete CHB and an apparent power of 2.1 MVA. The grid has a resolution of 9 steps for each frequency. The dashed blue lines indicate the value of f_{dcdc} above which $n_{\text{mod}} = 3$, otherwise $n_{\text{mod}} = 2$.

The mass distribution of the different components in the inverter variants is shown in the pie charts in Fig. 7 for $f_1 = 600\text{Hz}$ and $f_{\text{dcdc}} = 60\text{kHz}$. The slice *Semiconductors* includes chip, cooling, and driver board masses. The dominant mass in the CHBSLC is by far the capacitor, whereas in the inverter variants including a DC-DC converter, the inductors account for the majority of the mass. With rising numbers of phase legs in the CHBIL, the relative inductor mass decreases while the semiconductor mass increases due to the additional half-bridges. Given that the absolute capacitor mass is constant and the inductor mass decreases with rising n_{IL} for all CHBIL, the relative share of the capacitor mass increases.

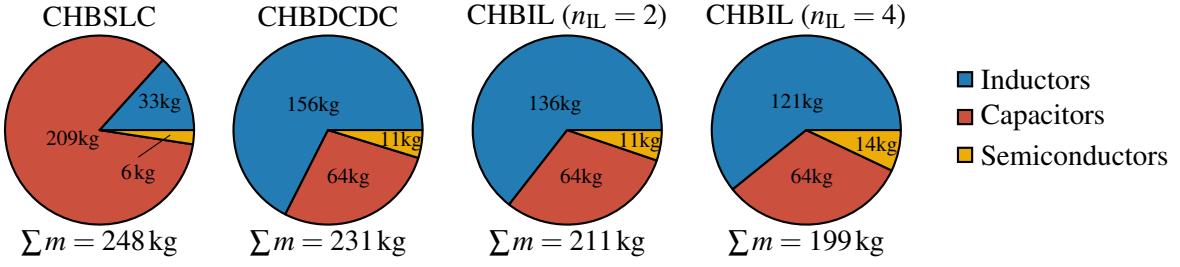


Fig. 7: Mass distribution of the components in a CHBSLC, CHBDCDC, and CHBIL with $n_{\text{IL}} = 2$ and $n_{\text{IL}} = 4$ at $f_1 = 600\text{Hz}$ and $f_{\text{dcdc}} = 60\text{kHz}$. Slice *Semiconductors* includes chip, cooling, and driver board masses.

Conclusion

In this paper, different module variants for a CHB have been studied in order to find suitable solutions for an SAEA. The focus of the module variant designs is the compensation of the second harmonic component in the battery current. In two parameter studies, the influences of the battery cell voltage window r_{uc} , the ratio of the RMS to DC battery current r_1 , the fundamental machine frequency f_1 and the DC-DC converter switching frequency f_{dcdc} on the inverter's efficiency, mass, and power density have

been investigated. To calculate the module components' losses and masses, scalable component models have been employed. The parameter studies show that a narrow cell voltage window is beneficial to the efficiency and power density in all module variants considered. Furthermore, increases in the fundamental frequency and the DC-DC converter switching frequency reduce mass and improve power density. The CHBIL reaches the highest power density but is inferior to the CHBSLC in terms of efficiency.

For a power train design process, the given parameter studies give an idea of how the named parameters of adjacent elements, such as a battery or machine, influence the resulting inverter. The results can also be used to choose the most suitable CHB variant for given battery and machine parameters. In combination with battery and machine models, the inverter model presented here makes an overall system optimization for mass and efficiency of SAEA propulsion systems possible, and this is planned for future studies.

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