

Parameter tuning method for class Φ_2 converters for high-frequency wireless power transfer applications

Yining Liu, Prasad Jayathurathnage, and Jorma Kyrrä,
Aalto University
Maarintie 8, 02150
Espoo, Finland

Phone: +358504366005, +358504477981, +358505639146

Email: yining.l.liu@aalto.fi, prasad.jayathurathnage@aalto.fi, jorma.kyyra@aalto.fi

Acknowledgments

We would like to thank Professor Sergei Tretyakov for the guidance and useful discussions.

Keywords

«High frequency power converter», «resonant converter», «parasitics», «soft switching», «zero-voltage switching»

Abstract

This paper presents a method to compensate detuning of class Φ_2 push-pull converters due to practical disparities such as component values tolerances, parasitic effects, and manufacturing errors. A simple and effective tuning method is proposed based on only four steps. An example 100 W, 6.78 MHz wireless power transfer system is presented, that reaches 82.3% efficiency after tuning using the proposed method.

Introduction

High-frequency power conversion at MHz frequencies has become a very important research topic since the advent of wide-band-gap switching devices including Gallium-Nitride (GaN) and silicon-carbide (SiC) devices. With the increasing of switching frequency, the size of the magnetic components can be reduced significantly, and the power density can be increased. However, the key challenges in MHz-power converters are dominance of switching losses, effects of parasitics, and high voltage/current stresses on the switching components. There have been several research attempts to address these challenges. For example, realization of zero-voltage-switching (ZVS) and zero-voltage-derivative-switching (ZVDS) can reduce the switching losses significantly [6]. Different converter topologies have been extensively studied including class E [3], class EF [2], [5], class Φ_2 [4], and push-pull [1] topologies to realize different characteristics and advantages. Among these topologies, class Φ_2 push-pull topology has the advantages of increased power density with reduced DC current ripple as well as the inductance value. In [1], a theoretical design method is proposed to calculate optimal component parameters. With a proper design, a T-network is able to remove the second harmonic voltage from the power switches and greatly reduce their voltage stress. Meanwhile, its differential branch can provide required inductive current for ZVS, which simplifies coil tuning because no more residual inductance is needed in the load branch. Such structure also helps with an intrinsic constant voltage output, because the total voltage drop on the coil and its series tuning branch is always zero at the operating frequency.

Despite all these advantages, one of the main challenges in all MHz power converters is that the circuit components need to be precisely tuned to their designed values to achieve full advantages. In practical implementations, effects of parasitics and manufacturing tolerances may significantly deteriorate performance parameters, such as efficiency and load-independent constant output features. Converters can

easily lose their soft-switching operations, which results in a much higher voltage and current stress on the components. On the other hand, the large number of design parameters and their coupling effects to circuit performance make it hard to find the detuned parameter(s). In practice, it is almost impossible to tune the circuit to its theoretically designed working point only through simulations or trial-and-error based approaches. Unfortunately, these detuning effects and corresponding parameter design methods are not discussed in the literature, and converters often work at sub-optimal operation points due to aforementioned practical disparities. Therefore, it is important to investigate parameter detuning effects and find a systematic way to tune the system to the desired working point. This paper investigates parameter detuning effects of class Φ_2 converters, and introduces a systematic approach for tuning the system to the proper working condition.

This paper is organized as follows. The working mode analysis of the selected class Φ_2 inverter is presented in Section II, the parameter tuning is presented in Section III, followed by experimental results.

Working mode analysis

The class Φ_2 inverter circuit structure is shown in Fig. 1. The definition of the components, the branch currents, and node voltages are depicted in Fig. 1. Considering the 180° phase shift between the left and right legs in push-pull operations, the current and voltage components can be divided into differential and common modes:

$$i_{\text{odd}}(\omega_s t) = i_{\text{odd1}} + i_{\text{odd2}} = (i_{L1a}(\omega_s t) - i_{L1b}(\omega_s t)) + (i_{L2a}(\omega_s t) - i_{L2b}(\omega_s t)) \quad (1)$$

$$i_{\text{diff}}(\omega_s t) = i_o(\omega_s t) + i_{\text{odd}}(\omega_s t) \quad (2)$$

$$v_o(\omega_s t) = v_{\text{ds1}}(\omega_s t) - v_{\text{ds2}}(\omega_s t) \quad (3)$$

$$i_{\text{even}}(\omega_s t) = \frac{i_{L2a}(\omega_s t) + i_{L2b}(\omega_s t)}{2} \quad (4)$$

$$I_{\text{DC}} = \frac{i_{L1a}(\omega_s t) + i_{L1b}(\omega_s t)}{2} \quad (5)$$

Based on these definitions, differential currents i_{diff} , i_{odd} and i_o circulate around push and pull legs, which results in a 180° phase difference between voltage components on two legs. i_{odd} represents the inductive part of the total differential current i_{diff} , while i_o represents the resistive part with the reference to the output voltage v_o . In comparison, the common-mode current components I_{DC} and i_{even} flow through both legs in parallel, and the voltage components at the same position on left or right legs have also the same phase. Note that the class Φ_2 rectifier can be realized by replacing the AC output and DC source by an AC source and DC load resistance, respectively. The switching components for a rectifier can be either diodes (passive rectifiers) or FETs (active rectifiers). Therefore, the analysis and the experimental work presented in this work are also valid for the class Φ_2 rectifier.

The main working waveforms for inverters are shown in Fig. 1. Four working modes (as depicted in Fig. 1(b) and (c)) are contained in one full switching cycle as detailed in the following.

- **Mode 1** between $[0, \theta_s]$ starts when switch Q_1 is turned off. Both switches Q_1 and Q_2 remain OFF during this period, the circulating current i_{diff} therefore charges C_{1a} and discharges C_{1b} , which contributes to the variation in differential voltage, i.e. makes the output AC voltage v_o to go from negative to positive. At the end of mode 1, $i_{C1b} = 0$, v_{ds2} is discharged to zero by i_{C1b} with a zero derivative which prepares Q_2 for turning on with both ZVS and ZVDS in the next mode.
- **Mode 2** lasts between $(\theta_s, \pi]$. Q_2 is ON in this mode, which clamps v_{ds2} to zero. The output voltage v_o equals to v_{ds1} . Switch Q_2 is turned OFF at the end of this mode, which is at half of the switching period.
- **Mode 3** between $(\pi, \pi + \theta_s]$ and **Mode 4** between $(\pi + \theta_s, 2\pi]$ work in a similar way as Modes 1 and 2. During Mode 3, both switches are OFF, i_{diff} charges C_{1b} and discharges C_{1a} to prepare Q_1 -ON in Mode 4, v_o falls from positive to negative. At $(\pi + \theta_s)$, Q_1 turns ON with ZVS and ZVDS, v_{ds1} is clamped to zero, and v_o equals to $(-v_{\text{ds2}})$ during Mode 4.

The components L_{2a} , L_{2b} , and $2C_2$ constitute a T-network. From the definition in (1), in the differential-mode equivalent circuit, the series-connected horizontal branches, L_{2a} and L_{2b} , form an inductive branch between the push and pull legs to provide a path for the differential current $i_{\text{odd}2}$. In the common-mode, $L_{2a} - C_2$ and $L_{2b} - C_2$ form two separate branches in parallel with Q_1 and Q_2 , respectively. By making L_2 and C_2 resonate at $2f_s$, these two branches provide low-impedance paths for i_{even} , which help to filter out the second harmonic component from v_{ds} and greatly reduce voltage stress.

$2Z_{\text{eq}}$ represents the equivalent load impedance reflected from the receiver side of the wireless power transfer (WPT) network, for a series-series compensation network [7], it can be calculated as

$$2Z_{\text{eq}} = \frac{\omega_s^2 M^2}{Z_{\text{rec}}} \quad (6)$$

where M is the mutual inductance between WPT coils, and Z_{rec} is the input impedance of the rectifier. To ensure the highest possible power transfer efficiency and load-independent characteristics, the impedance Z_{rec} is usually tuned with only a resistive part, therefore, $2Z_{\text{eq}}$ can be simplified as $2R_{\text{eq}}$ in Fig. 1. The output branch is assumed to have a high quality factor, which ensures approximately sinusoidal AC current, i_o , as the load branch acts like a high-Q resonant filter.

As defined in (3), v_o only exists in the differential mode equivalent circuit ($n\omega_s$, $n = 1, 3, 5, \dots$), where $L_{2a,b}$ and $L_{1a,b}$ composed two inductive branches in parallel with the load branch. The currents flowing through $L_{2a,b}$ and $L_{1a,b}$ contribute together to the total inductive current i_{odd} which is 90° lagging from i_o at fundamental frequency. Considering only the dominant harmonics $n = 1, 3$, the total differential current can be written as

$$i_o(\omega_s t) = I_o \sin(\omega_s t + \phi_1), \quad (7)$$

$$i_{\text{odd}}(\omega_s t) = -I_{L,1} \cos(\omega_s t + \phi_1) - I_{L,3} \cos(3\omega_s t + \phi_3), \quad (8)$$

$$i_{\text{diff}}(\omega_s t) = i_o(\omega_s t) + i_{\text{odd}}(\omega_s t) = I_{\text{diff}} \sin(\omega_s t + \theta) - I_{L,3} \cos(3\omega_s t + \phi_3), \quad (9)$$

where I_o and ϕ_1 are the amplitude and phase of the load current. $I_{L,1}$ and $I_{L,3}$ represent the amplitudes of inductive current i_{odd} at the fundamental and third harmonic frequencies, respectively. $\frac{\phi_3}{3}$ provides the phase angle at $3\omega_s$. I_{diff} and β are the amplitude and phase of i_{diff} . All these parameters are shown in

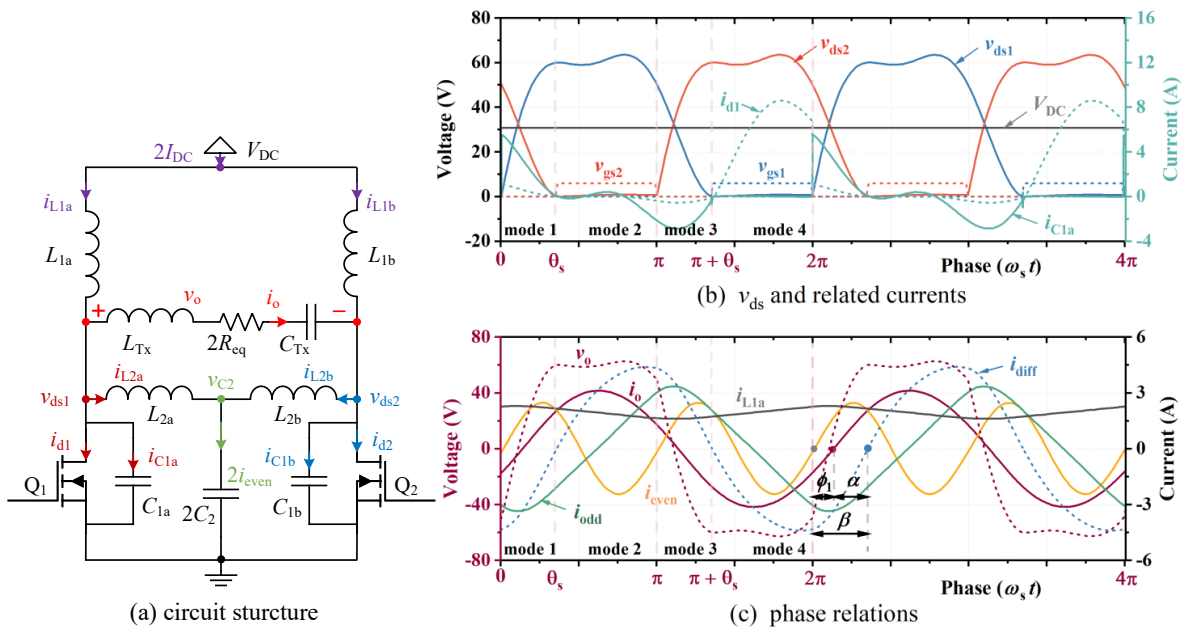


Fig. 1: Class Φ_2 push-pull inverter (a) circuit structure, (b) v_{ds} and its related current waveform, (c) main current waveform and phase relations.

Fig. 1(c), and they are related as

$$\beta = \phi_1 + \alpha, \quad (10)$$

$$\alpha = \arctan\left(\frac{I_{L,1}}{I_o}\right), \quad (11)$$

$$I_{\text{diff}} = \sqrt{I_o^2 + I_{L,1}^2}. \quad (12)$$

According to the working principles and design specifications, all the component values of the push-pull class Φ_2 circuit can be obtained through the design equations given in [6].

Parameter tuning due to parasitic effects

Even though a set of design parameters can be theoretically calculated, the manufacturing tolerances and parasitic effects cause inaccuracy of the component values and shift the circuit away from the optimal working point (with ZVS and ZVDS achieved at the nominal power). Therefore, actual implementations based on commercially available components should be properly tuned to the optimal working point at its nominal working status with full load and the specified mutual inductance.

Parameter detuning

Parameter detuning effects are analyzed based on a practically achievable inductor value L_2 , when considering inaccuracies of C_1 , C_2 , Z_{eq} (or M) and R_{Load} . System power can be further tuned by adjusting V_{DC} . These different practical imperfections will have different effects on either the waveform or the system power level. In Fig. 2 and Fig. 3, v_{ds1} , i_{C1a} (or v_{in} , i_{in}) waveforms as well as the DC output power are given according to $\pm 20\%$ inaccuracies in the above parameters.

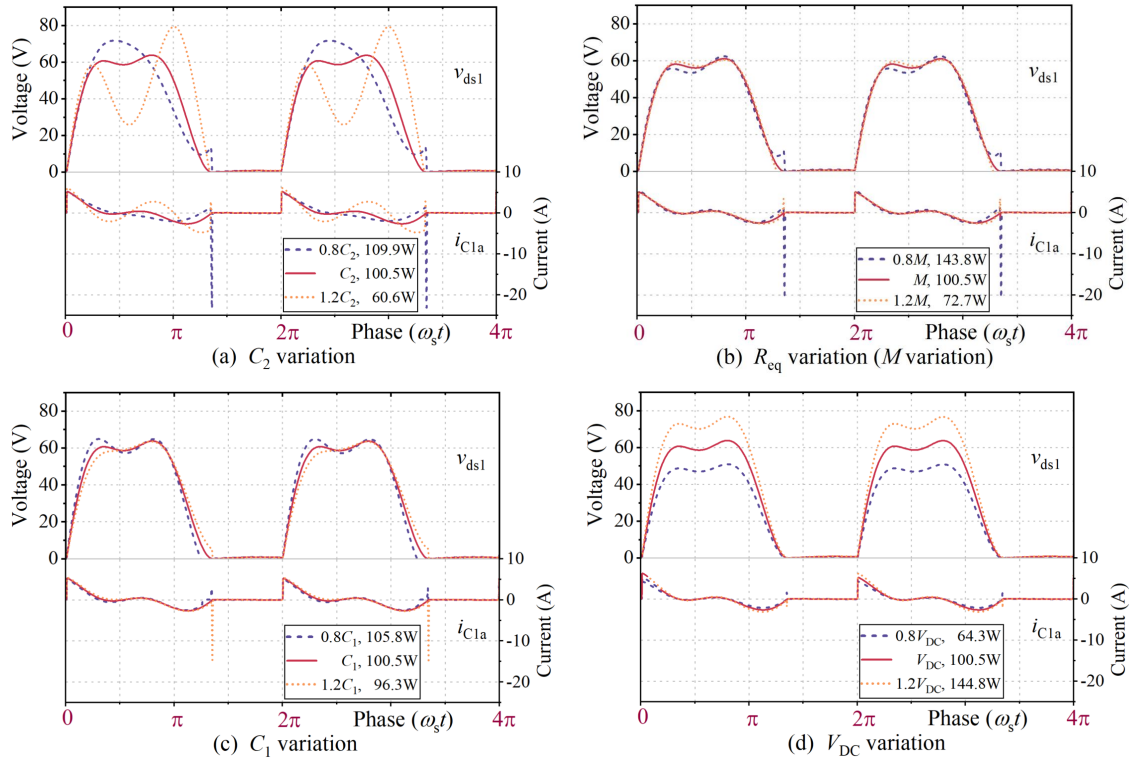


Fig. 2: Main waveform of a inverter with (a) C_2 variation, (b) R_{eq} variation (brought by M inaccuracies), (c) C_1 variation, (d) V_{DC} variation.

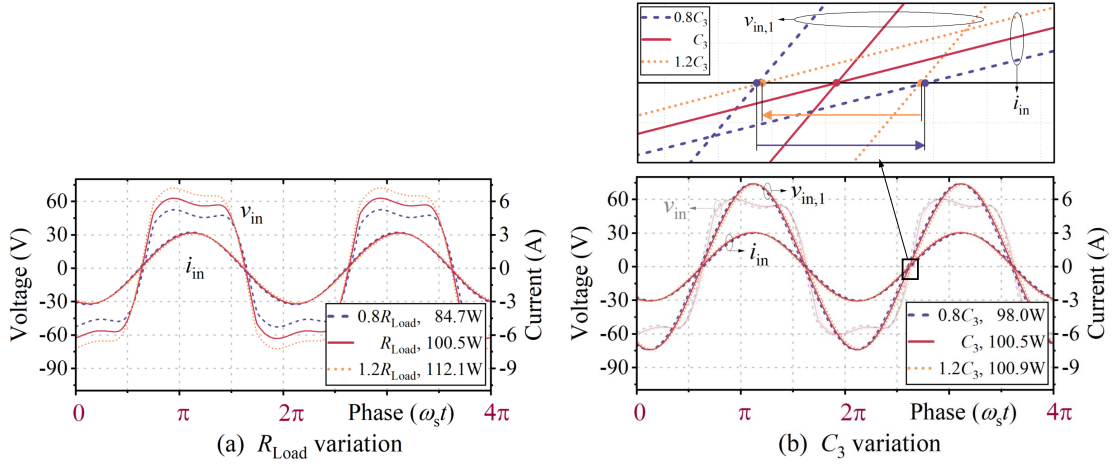


Fig. 3: Main waveform of a rectifier with (a) R_{Load} variation, (b) C_3 variation.

Parameters related to T-network resonance L_2 , C_2 , L_4 , C_4

If each component value has a tolerance of $\pm 20\%$, the inaccuracy of the T-network resonance will have the most significant effect on both v_{ds} waveform and the power level, as seen in Fig. 2. Since the T-networks work in a same way at both inverter and rectifier sides, here the T-network in the inverter (with C_2 and L_2) is taken as an example to analyse parameter detuning effects. When the resonance frequency of the T-network is different from $2f_s$, the amplitude I_2 and phase ϕ_2 of i_{even} shift away from their designed values, which greatly changes the shape of i_{C1a} as well as v_{ds} , according to

$$i_{C1a}(\omega_s t) = I_{DC} - i_{even}(\omega_s t) - i_{diff}(\omega_s t), \quad \omega_s t \in [0, \pi + \theta_s] \quad (13)$$

$$v_{ds1}(\omega_s t) = \frac{1}{\omega_s C_1} \int i_{C1a}(\omega_s t) d(\omega_s t). \quad (14)$$

In addition, ZVS and ZVDS conditions are not met because the instantaneous value of current i_{C1a} becomes non-zero at the switching moment (refer to i_{C1a} waveform in Fig. 2(a)). Detuning of the resonance frequency of T-network also creates a negative effect on voltage stress.

Parameters related to soft switching operations Z_{eq} , R_{Load} , M , C_1 , C_3

Detuning of Z_{eq} leads to similar effects as detuning of R_{eq} , because it brings some additional reactance to the load branch and causes detuning of the load resistance along its whole variation range. Considering (6) and comparing to the inaccuracy on Z_{rec} , detuning of M brings higher inaccuracy on the equivalent load R_{eq} as its effect is squared in the equation. Both R_{eq} and C_1 detuning result in v_{ds} with a similar shape but lost soft-switching characteristics in the inverter. Although the variation in v_{ds} is small at the switching moment, it can lead to high spike current in the circuit which degrade converter efficiency and component lifetime. However, by comparing Fig. 2 (b) and (c), C_1 inaccuracies have little effect on the output power P_o , its negative effect is limited to soft-switching. On the other hand, R_{eq} variation changes the system power significantly, but it can be easily identified through the DC output voltage V_{Load} or the inverter output current i_o .

Similarly for diode rectifiers, the load resistance R_{Load} affects the system power as well as the output DC voltage, while the capacitance in parallel with the switching components (i.e. C_3 on the rectifier side) mainly affects the rectifier input impedance Z_{rec} , as shown in Fig. 3. Since the diodes have naturally ZVDS turning-off, an unsuitable C_3 will result in a reactance in Z_{rec} which can be observed easily through the phase difference between the rectifier input voltage and current. By observing the fundamental voltage component $v_{in,1}$, the zoomed curves in Fig. 3 (b) indicate the phases of input impedance Z_{rec} based on $\pm 20\%$ C_3 inaccuracies. As seen in the figure, only the properly tuned C_3 can provide a purely resistive Z_{rec} , which is important for high WPT efficiency and load independent operations.

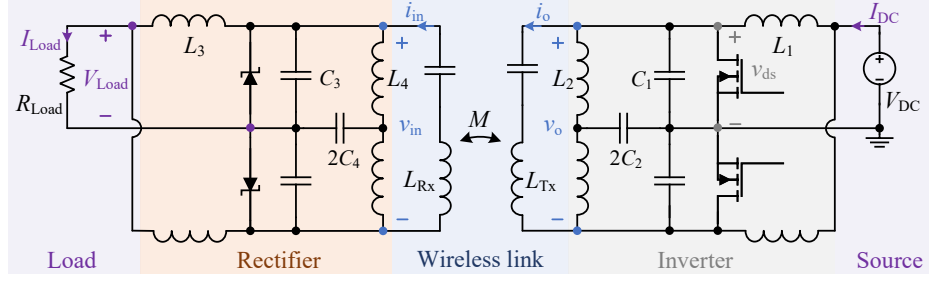


Fig. 4: Schematic of the WPT system.

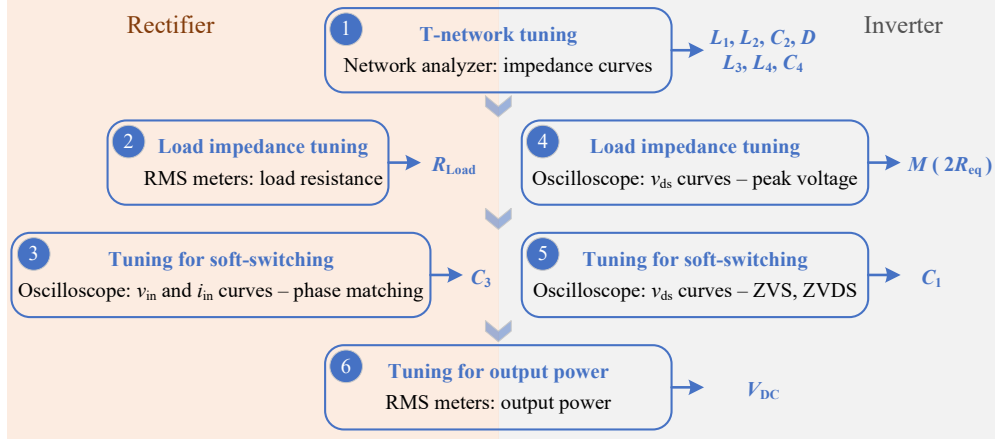


Fig. 5: System tuning steps.

All the inaccuracies in $L_2, L_4, C_{1\sim4}$ come from manufacturing tolerances, while R_{eq} inaccuracy can be a combination of multiple factors, as given in (6). Rectifier-side inaccuracies can bring in reactance for Z_{rec} as well as Z_{eq} , both Z_{rec} and Z_{eq} are not so straightforward to measure during the test. The mutual inductance is also hard to measure after implementation. Considering practical aspects, the system needs to be built for its optimal working status with the full load and the specified mutual inductance as in the design case. But in practical tests, it can be hard to find the specified M and R_{Load} , which even makes the tuning process targeting at a sub-optimal point.

Finally, variations of input DC voltage V_{DC} do not affect soft-switching characteristics. v_{ds} shape, ZVS and ZVDS are maintained while changing the input voltage value. Thus, V_{DC} can be used to adjust the output power based on the load requirement.

Parameter tuning steps

As analyzed above, parameters which have most complex effects on converter operations should be tuned firstly. In addition, similarly to the design procedure, the tuning direction should be from the load to the supply to ensure the required power at the specified load of the whole system. Therefore, based on the system schematic in Fig. 4, it is reasonable to make parameter tuning in steps shown in Fig. 5. T-networks are tuned first, as they have effects on the waveform shapes, power level, and soft-switching. The load impedances are tuned next with effects on the last two components. The next tuning step is about the capacitance in parallel with the switching components, which have effects mostly on soft switching, with negligible effects on the power level. Finally, the system power can be tuned separately by adjusting the input DC supply voltage. The tuning steps for the entire system can be explained as below:

- In **Step 1**, the T-network parameters for both converters are first tuned to resonance at $2f_s$ by adjusting the value of C_2, C_4 using a network analyzer. The designed duty cycle can also be properly adjusted according to the measured inductance value following the design equations in [6].
- In **Step 2**, considering the rectifier circuit, the DC resistance R_{Load} can be easily calculated and then adjusted to their specified full load by measuring the output DC voltage and current as $\frac{V_{Load}}{I_{Load}}$.
- As shown in Fig. 3, the passive class Φ_2 rectifiers have naturally ZVDS-off and ZVS-on because

of the diode operations. Therefore, in **Step 3**, a suitable capacitance C_3 that contributes to the required purely resistive rectifier impedance Z_{rec} can be found based on its related voltage and current waveforms. By tuning C_3 to its optimal value, the fundamental component of input voltage and current of the rectifier $v_{\text{in},1}$ and i_{in} will become in phase. On the other hand, the capacitance in an active rectifier with controllable FETs can be tuned by observing v_{ds} waveforms until they show ZVDS operations.

- After finishing the tuning process of the rectifier, the reactance in its input impedance Z_{rec} is tuned to zero. The remained resistance is the value that contributes to the pre-defined load resistance in (6) for the inverter design. Thus, the inverter load impedance tuning can be simplified to the tuning of mutual inductance M as in **Step 4**. From the current relation of a series-series compensation network [8], the inverter and rectifier ac currents and voltages are related as

$$\frac{i_o}{i_{\text{in}}} = \frac{v_{\text{in}}}{v_o} = \frac{Z_{\text{rec}}}{\omega_s M}. \quad (15)$$

Therefore, with the pre-defined M and Z_{rec} from rectifier parameter design, the ratio between the current (or voltage) at the inverter and rectifier sides is a known value. The required M is reached by tuning the v_{ds} or ac current waveforms on both sides to the given ratio.

- Next, soft-switching on the inverter side is affected only by parallel capacitance C_1 . In **Step 5**, the value of C_1 is tuned by observing the v_{ds} waveforms to ensure the ZVDS operations.
- Finally at **Step 6**, desired output power can be easily achieved by adjusting the input DC voltage, as the variation in V_{DC} does not affect soft-switching characteristics.

Experimental verification

A prototype WPT system has been set up with a class Φ_2 inverter, a wireless link, and a class Φ_2 rectifier, as shown in Fig. 6. The corresponding structure is shown in Fig. 4 and specifications are given as Table I.

Table I: Design specifications and component values

Inverter		Rectifier	
Input Voltage, V_{DC}	30 V	Power, P_{Load}	100 W
Duty cycle, D	31.4 %	Load, R_{Load}	7.5 Ω
Input inductor, L_1	2.7 μH	Output inductor, L_3	2.7 μH
T-network L_2	278 nH	T-network L_4	278 nH
T-network $2C_2$	992 pF	T-network $2C_4$	992 pF
External capacitor, C_1	1 nF	External capacitor, C_3	1 nF

The initial waveforms in Fig. 7(a) lose ZVDS switching and shows lower power and v_{ds} peak voltage

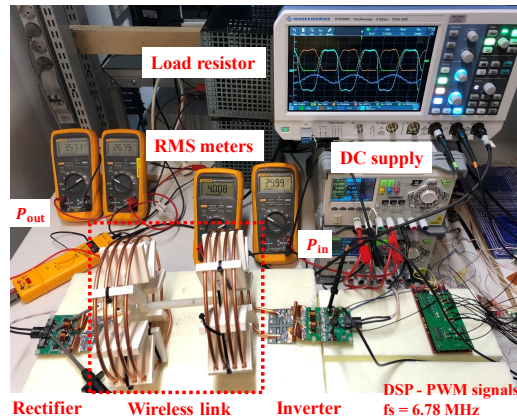


Fig. 6: Experimental system setup.

than designed. Through the tuning steps outlined in Fig. 5, the system is tuned to its designed operation point as in Fig. 7(b). The final v_{ds} and V_{Load} waveforms show that after tuning both ZVS and ZVDS are fully achieved at the designed output power. The achieved ZVDS operations help to reduce fluctuation in v_{ds} waveforms during its ON-period. The system reaches 82.3% efficiency at 100 W output power at 90 mm transfer distance.

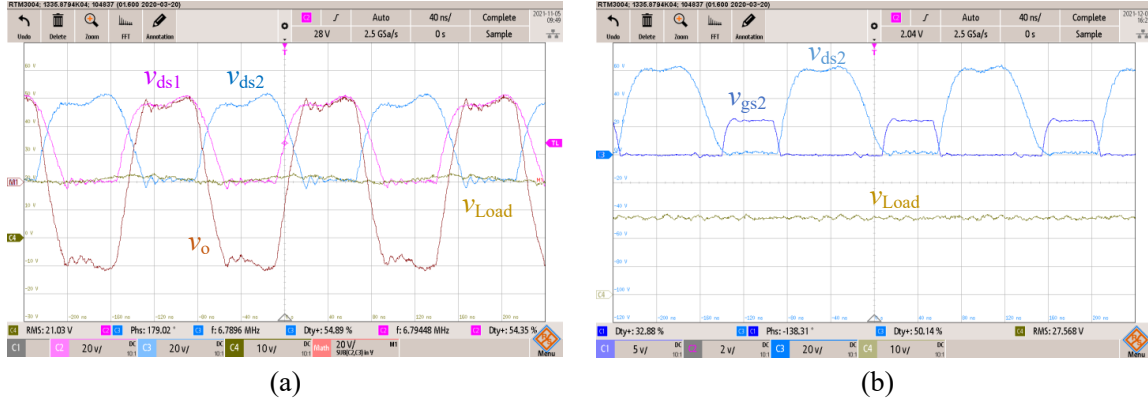


Fig. 7: v_{ds} and V_{Load} waveform. (a) Before and (b) after parameter tuning.

Conclusion

This paper analyzed parameter detuning effects on class Φ_2 push-pull converters. Detailed steps of the proposed tuning method are given based on decoupled features from experimental observation. By implementing the proposed tuning method, the system can be tuned to the designed operation point with both ZVS and ZVDS switching. An experimental realization demonstrated around 100 W output power regardless of existing parasitic effects, with the end-to-end efficiency of 82.3%.

References

- [1] L. Gu, G. Zulauf, Z. Zhang, S. Chakraborty and J. Rivas-Davila: Push-Pull Class Φ_2 RF Power Amplifier, IEEE Transactions on Power Electronics vol 35 no 10, pp. 10515-10531
- [2] S. Aldhafer, D. C. Yates and P. D. Mitcheson: Load-Independent Class E/EF Inverters and Rectifiers for MHz-Switching Applications, IEEE Transactions on Power Electronics Vol 33 no 10, pp. 8270-8287
- [3] G. Kkelis, D. C. Yates and P. D. Mitcheson: Class-E Half-Wave Zero dv/dt Rectifiers for Inductive Power Transfer, IEEE Transactions on Power Electronics vol 32 no 11, pp. 8322-8337
- [4] X. Zou, Z. Zhang, Z. Dong, Y. Zhou, X. Ren and Q. Chen: A 10-MHz eGaN FETs based isolated class- Φ_2 DCX, 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 2518-2524
- [5] Z. Kaczmarczyk: High-Efficiency Class E, EF₂, and E/F₃ Inverters, IEEE Transactions on Industrial Electronics vol 53 no 5, pp. 1584-1593
- [6] H. Tebianian, Y. Salami, B. Jeyasurya and J. E. Quicoe: A 13.56-MHz Full-Bridge Class-D ZVS Inverter With Dynamic Dead-Time Control for Wireless Power Transfer Systems, IEEE Transactions on Industrial Electronics vol 67 no 2, pp. 1487-1497
- [7] S. Y. R. Hui, W. Zhong and C. K. Lee: A Critical Review of Recent Progress in Mid-Range Wireless Power Transfer, IEEE Transactions on Power Electronics vol 29, no 9, pp. 4500-4511
- [8] Chwei-Sen Wang, O. H. Stielau and G. A. Covic: Design considerations for a contactless electric vehicle battery charger, IEEE Transactions on Industrial Electronics vol 52, no 5, pp. 1308-1314