Temperature Distribution of an IGBT Chip during Repetitive Switching Events under Consideration of Front-Side Ageing

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Keywords

«Module temperature measurement», «IGBT», «Reliability»

Abstract

Ageing effects are considered to provoke an inhomogeneous current distribution within power devices. The resulting temperature distribution at the junction and the surface of an IGBT chip was investigated in detail at different ageing states and for different switching frequencies during repetitive hard-switching events. Furthermore, the limitations of utilized methods for temperature determination were discussed. The observations were judged with respect to reliability issues.

1. Introduction

In application, power semiconductor devices such as IGBTs and diodes are exposed to repetitive switching events with a certain setting of frequency, duty cycle, temperature and current level. As a result of the simultaneous presence of current and voltage during switching, conduction, and blocking phase, the power losses are generated in the semiconductor device. Depending on the package structure, the power loss is mainly dissipated to the environment via the front- or backside of the semiconductor. A temperature distribution across the device, including the packaging, is the result. This temperature distribution is expected to reach a steady state, when the generated power losses meet the cooling capabilities.

In order to determine the temperature distribution within and on the surface of a power semiconductor chip, detailed information about the device composition like thicknesses, dimensions and material properties are necessary. However, this distribution is only valid for a virgin device and is expected to vary with respect to the ageing state. In addition, the quantitative results are highly dependent on detailed information about the packaging technology and front-side interconnection technology, like the amount of bond-feet, the back-side interconnection technology, and the used cooling.

In this investigation, the development of the temperature during repetitive switching events across the chip surface, at the case of the module package, and at the die junction is shown, with respect to a certain state-of-life (SoL) up to and beyond end-of-life (EoL). According to AQG324 [1] the EoL state in power cycling is defined as 5 % increase of forward voltage drop $V_{CE,cold}$, which is the result of a degraded front-side interconnection. Or an increase of 20 % in thermal resistance between junction and case $R_{th,jhs}$ which suggests a degradation in the thermal path. The transient response of the temperature was monitored for two different switching frequencies at fixed duty cycle of 50 %.

2. Test setup

The converter-like setup in Fig. 1 was used to perform repetitive hard-switching events for a desired device under test (DUT). The semiconductor devices of the high side (HS) and low side (LS) have been part of one module. This investigation focuses on the behavior of LS-IGBT, which is further referenced as DUT. The investigated module was an IGBT in an Econo package with a nominal current rating of 100 A and a nominal voltage of 650 V. As protection IGBT (PIGBT), a 1500 A and 4500 V IGBT was used with V_{CE} fault detection in order to turn-off right after a destructive device failure.
The clamping circuit, as introduced by [2], was utilized to measure the voltage $V_{CE(on)}$ during the device conduction state with high resolution.
The current I_C was measured by a 30 MHz Rogowski coil close to the DC-Link capacitor in order to avoid voltage slope interferences [3].The voltages V_{GE} and $V_{CE(off)}$ were measured with passive probes of 500 and 400 MHz. Owing to the package without kelvin connections that are directly connected to the emitter surface, the measured voltages did always include package components like bond-wires and copper traces.

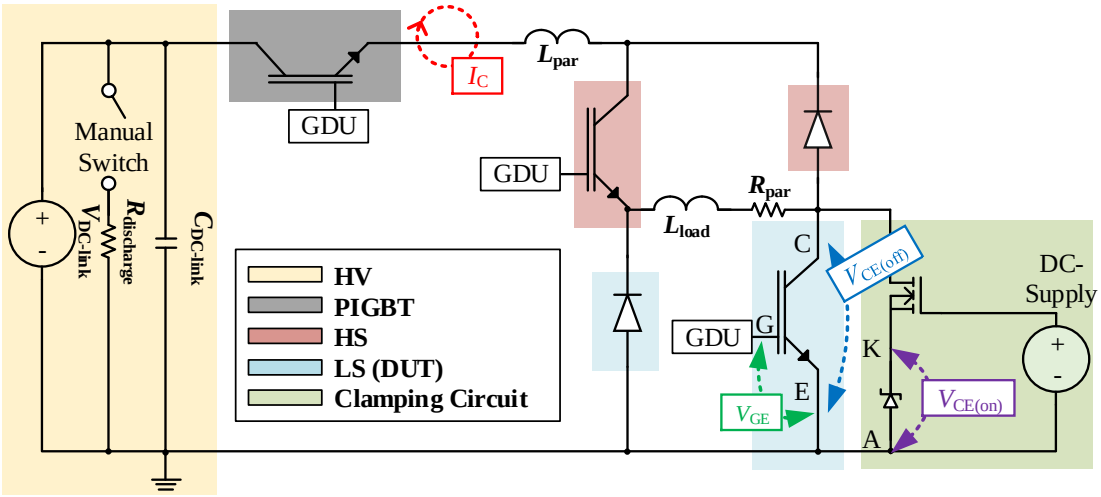


Fig. 1: Converter-like setup for repetitive switching events including relevant measurement points, clamping and protection circuit

3. Pulse pattern and switching principle

By utilizing the pulse pattern in Fig. 2, a converter like application is possible, where only conduction and switching losses have to be compensated by the power source.

During t_1, the HS and LS IGBT are turned on in addition to the permanent-on PIGBT. The current I_C ramps up according the following equation (1):

$$\left(V_{\mathrm{DC-Link}} - V_{\mathrm{CE(on)\_PIGBT}} - V_{\mathrm{CE(on)\_HS-IGBT}} - V_{\mathrm{CE(on)\_LS-IGBT}} - i_C \cdot R_{\mathrm{par}}\right) = L_{\mathrm{load}} \cdot \frac{\mathrm{d}i_C}{\mathrm{d}t_1} \qquad (1)$$

R_{par} is thereby the parasitic resistance of all conducting paths within the test bench, the power modules, and the inherent resistance of the used load inductance of about 10 mΩ.
The duration of t_1 is chosen in order to obtain a slight increase of I_C at the beginning of the subsequent pulse. In Fig. 2, a difference between $I_{C(DC+)}$ and $I_{C(rep)}$ is highlighted. During t_1 and t_3, the current $I_{C(DC+)}$ is flowing from the DC-link capacitor through the LS-IGBT and is recorded by the Rogowski coil. The current $I_{C(rep)}$ is present during the free-wheeling phase t_2 and t_4. The voltage $V_{CE(on)}$ is recorded during the on-time of the DUT and is increasing according to the current level.

During t_2, HS-IGBT is off and the current drops during the free-wheeling phase across LS-IGBT and LS-Diode. During t_3, HS IGBT is on and the current is ramped up again according to equation (1) to compensate the drop within t_2. In section t_4, the LS-IGBT is off and the current commutates to the HS free-wheeling circuit.
A detailed depiction of the initial pulse is given in Fig. 3

Period	1/2f			1/2f
GDU	t_1	t_2	t_3	t_4
PIGBT	on	on	on	on
HS	on	off	on	on
LS (DUT)	on	on	on	off

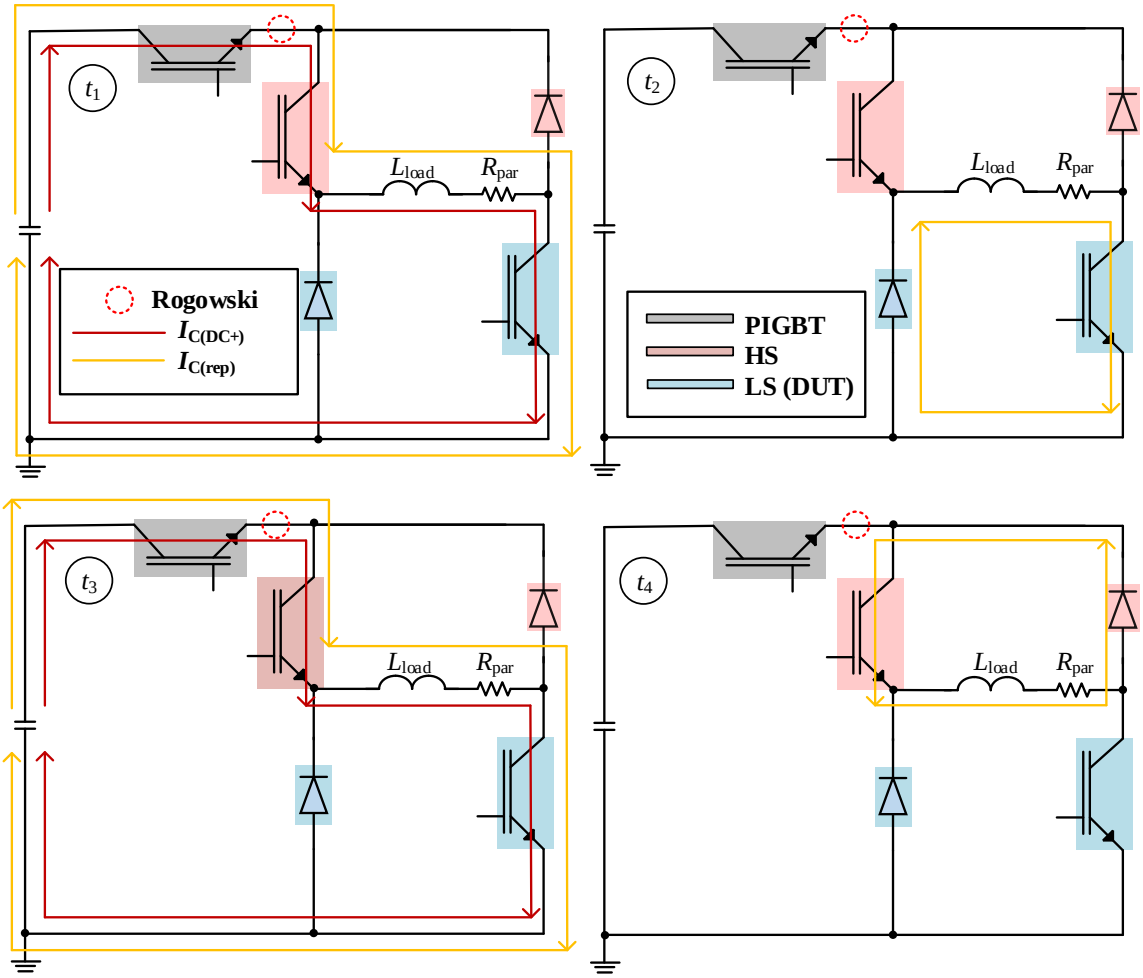


Fig. 2: Pulse pattern and corresponding course of load current for one cycle of the repetitive switching operation. The difference between $I_{C(DC+)}$ and $I_{C(rep)}$ is highlighted for each phase (L_{par} not shown).

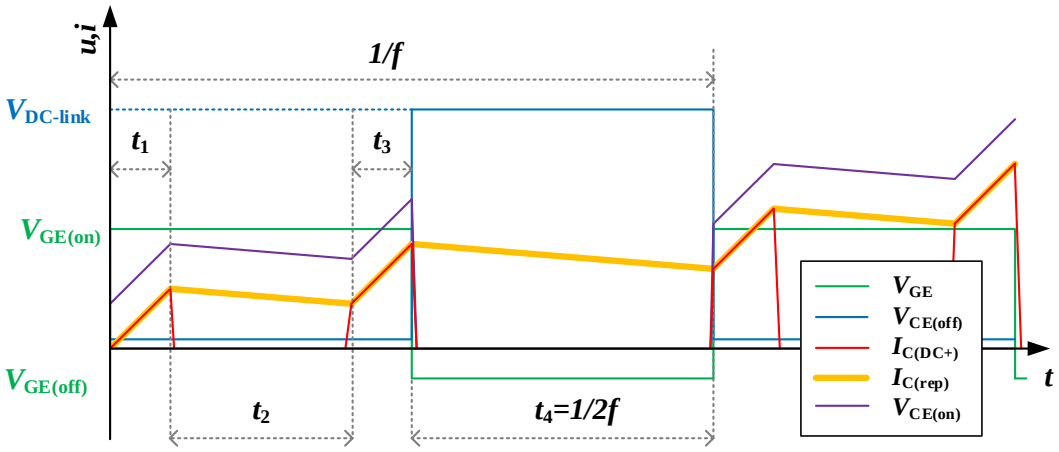


Fig. 3: Initial pulse of the repetitive switching investigation according to Fig. 2

Performing repetitive pulses with fixed periods of t_1 to t_4 results into different phases for the repetitive operation as shown in Fig. 4. The displayed voltages and the current $I_{C(DC+)}$ belong to the DUT.

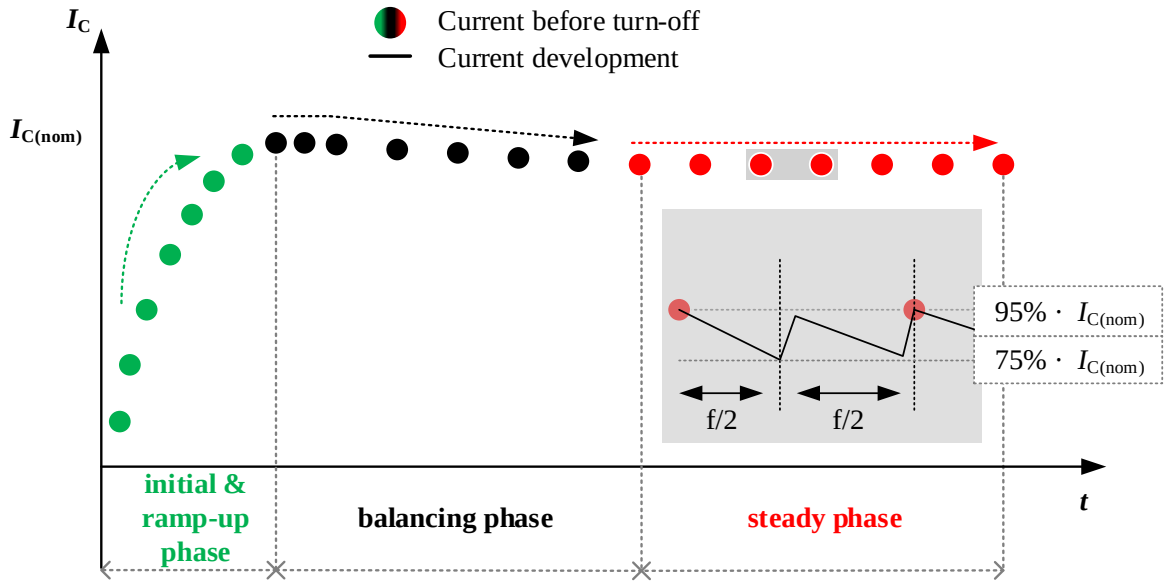


Fig. 4: Different phases of the repetitive switching operation caused by static pulse pattern and self-heating effects. $I_{C(nom)}$ corresponds to the desired nominal current level of 100 A for this investigation.

During the ramp-up phase, the current increases steadily until the desired current level is reached. During the balancing phase, the current level decreases slightly, according to joule heating of conducting elements and self-heating of the active devices. During the steady phase, an equilibrium between static pulse pattern, temperature induced effects and power losses is obtained.

The repetitive switching operation was performed for 20 min with a switching frequency of 500 and 1000 Hz. Within the first 200 pulses the balancing phase was already reached. The balancing phase was unaffected by the ageing state and switching frequency and took about 15 minutes for the tested system. The remaining time was performed within the steady phase. Taking the obtained current development into consideration, as sketched in Fig. 4, an average value of 86 % of $I_{C(nom)}$ was applied during the steady phase, with a minimum of 75 % of $I_{C(nom)}$ and a maximum of 95 % $I_{C(nom)}$. A higher load inductance L_{load} and a dynamically self-adjusting period t_1 would enable higher average values, hence less ripple.

4. Temperature determination

Three different techniques were used to monitor the temperature development during the repetitive switching operation, as depicted in Fig. 5.

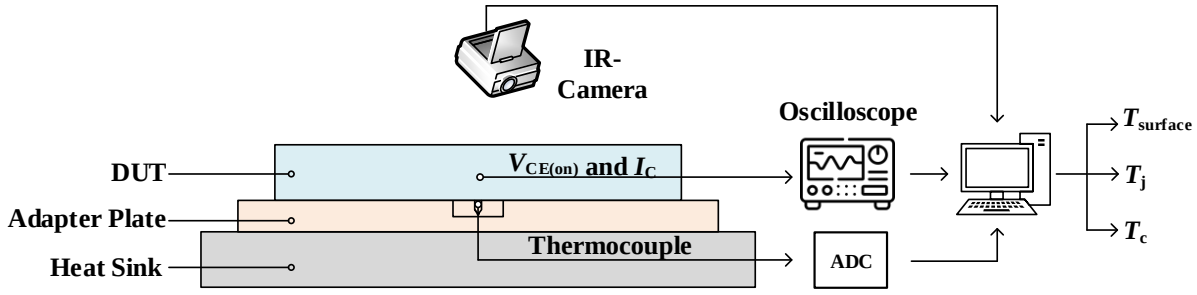


Fig. 5: Different methods of temperature tracking during repetitive switching operation

The case temperature T_c was measured with a thermocouple inserted into an adapter-plate below the power module. Due to the limited accessibility of the adapter plate, a certain distance between thermocouple and DUT had to be taken into account.
The surface temperature $T_{surface}$ was measured by an infrared (IR) camera, after the silicon gel of the DUT was removed and the device was dyed by thermal lacquer to obtain a homogeneous emission coefficient. After the gel removal, the leakage current at nominal blocking voltage was not increased.
For the determination of the junction temperature T_j, different temperature sensitive electrical parameters (TSEPs) were considered according to Table 1. The voltage $V_{CE(on\text{-}sense)}$ corresponds to the on-state voltage drop of the DUT, while a 100 mA sense current is applied. In contrast, the voltage $V_{CE(on\text{-}load)}$ drops across the DUT at load current levels of about $I_{C(nom)}$ = 100 A (shortly before turn-off).

Table 1: Applicability of different TSEPs during repetitive switching operation. Green – beneficial | Light red – adverse | Dark red - disqualifier

TSEP	Self-heating within calibration?	Interruption during repetitive operation?	Additional measurement circuit necessary?	Further drawbacks
$V_{CE(on\text{-}sense)}$	No	Yes	Yes	Measurement delay due to settling times and tail current phase of IGBT [4]
$V_{CE(on\text{-}load)}$	Yes	No	Yes	Re-calibration after (artificial) ageing mandatory
$V_{GE(th)}$	No	No	Yes	Difficult to distinguish due to plasma dominated turn-off process
di/dt_{max}	Yes	No	No	Additional non-linear load current dependency
I_{tail}	Yes	No	No	Current level difficult to distinguish

From this, the following considerations can be derived for the determination of the junction temperature under repetitive conditions:

- $V_{CE(on\text{-}sense)}$: This method could not be used, according to the requirement to not interrupt the repetitive operation. However, this is the method typically applied to measure the T_{vj} during power cycling.
- $V_{CE(on\text{-}load)}$: Owing to the device package, the voltage drop during on-state included bond-wires, copper traces and the semiconductor chip itself. Hence, re-calibration after each artificial ageing step was mandatory. In order to determine the voltage drop during on-state with sufficiently high resolution and to not damage the oscilloscope during blocking state, a clamping circuit according to [2] could be used.
- $V_{GE(th)}$: It was a requirement to determine the temperature at the maximum current level within one switching cycle, hence during turn-off or right before. Limited by plasma-induced effects of an IGBT, a clear link between current zero-crossing and measured gate-voltage during turn-off is not given. As a consequence, this TSEP was not considered.
- di/dt_{max}: For different temperatures and current levels, the maximum current slope was recorded. This investigation revealed a non-linear current dependency. Hence, due to the enormous additional calibration effort for different currents, as present during the repetitive operation, this TSEP was not considered.
- I_{tail}: In [5], the tail current was presented as TSEP and verified by simulation and measurement. However, the determination of the amplitude of the tail current is difficult and unprecise and strongly depends on switching condition and the chip technology.

Taking all requirements into account, the voltage drop during on-state $V_{CE(on\text{-}load)}$ at load current was utilized as TSEP. A strong dependency of $V_{CE(on\text{-}load)}$ on the packaging condition and hence ageing state, as mentioned in [6], was omitted by performing the calibration again for each SoL. The calibration was performed as follows and is depicted in Fig. 6: The DUT was heated up to different temperature levels between room temperature and 150 °C by a heat plate underneath the power module. At different

temperatures, a pulse of about 130 µs with a linear current slope was applied. From this pulse, a calibration matrix could be obtained that links $V_{CE(on\text{-}load)}$ voltage drops to certain current levels at a pre-adjusted temperature. This procedure was repeated for each ageing state. Exemplary calibration curves for different ageing and current levels are depicted in Fig. 7.The junction temperature of the DUT was determined according to Fig. 3 right before turn-off at the end of period t_3.

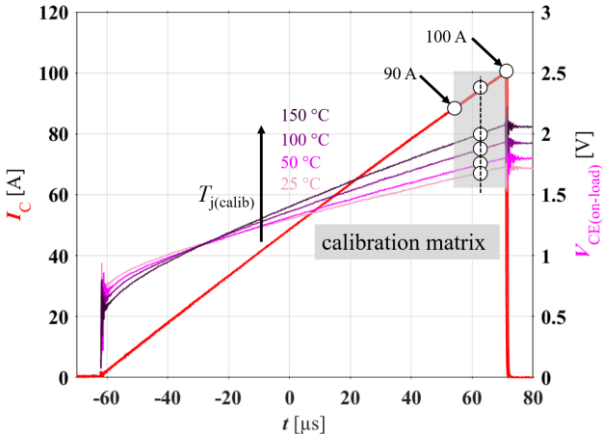


Fig. 6: Calibration pulse at one ageing state for different temperatures.

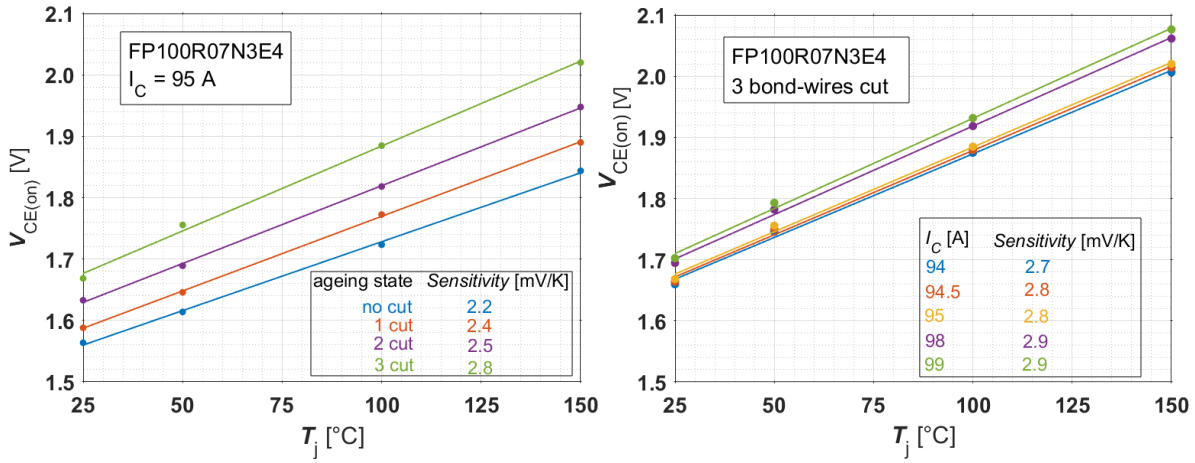


Fig. 7: $V_{CE(on\text{-}load)}$ calibration curves for different ageing states (left) and different current levels (right). Measurement points were fitted by a linear approximation of 1st degree.

5. Measurement results with respect to different ageing states and switching frequencies

A fixed pulse pattern was used to reach a steady state of the switched current level through the load inductance and hence the LS (DUT). Due to the applied current, the device heats up and the forward voltage drop $V_{(CE)on}$ increases. According to equation (1), the di_C/dt decreases slightly, because the remaining voltage across the load inductance decreases. As a consequence, the current level does not remain constant and declines over the whole period of repetitive switching events to about 95 % of the initial current level, which was reached in the balancing phase shown in Fig. 4. This trend is shown in Fig. 8 for 3 different turn-off pulses of the overall 20 min repetitive operation.

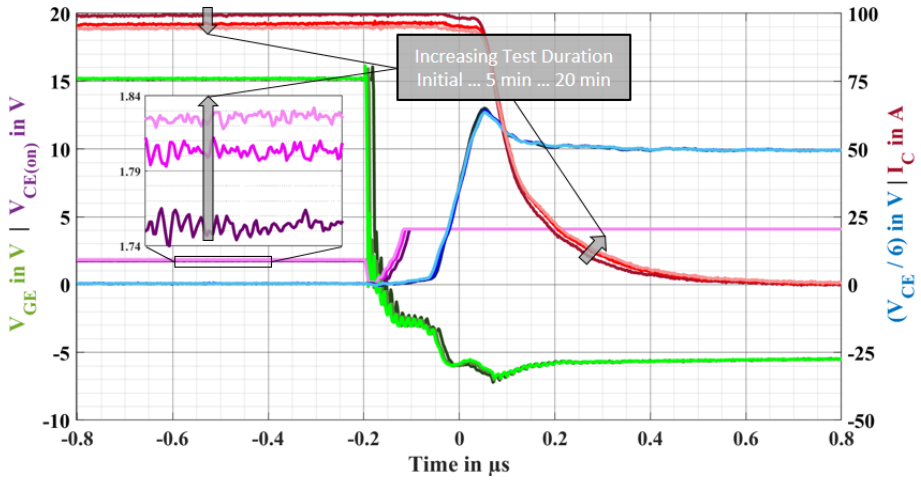
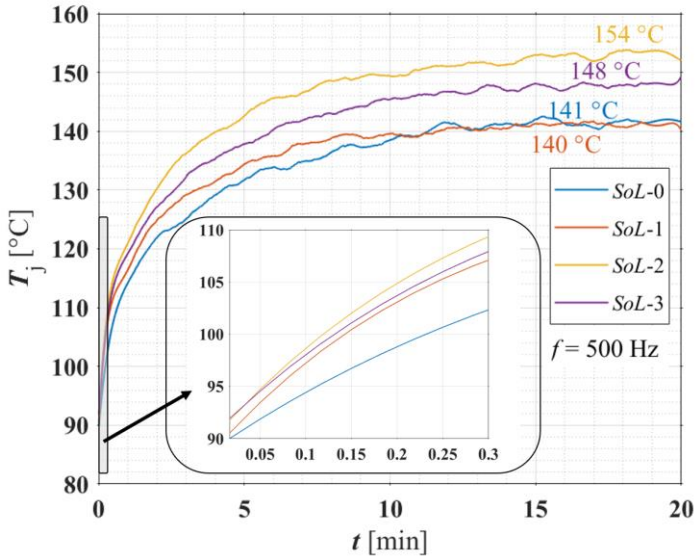


Fig. 8: Recorded turn-off waveforms at the end of t_3 for different test durations within one repetitive switching investigation of overall 20 minutes.
Repetitive Switching at 500 Hz, I_C = 100 A, V_{CE} = 300 V, $V_{GE(on)}$ = 15 V, $V_{GE(off)}$ = -5 V, $R_{G(ext)}$ = 0 Ω

Every two seconds, a turn-off event according to Fig. 8 was recorded and the junction temperature was derived from $V_{CE(on)}$ at a corresponding current level. The courses of the junction temperature is depicted for different SoL in Fig. 9. From this, different slopes of temperature development over the test duration can be seen. The slope increases from ageing state SoL-0 to SoL-3 within the first 3 seconds. After about 3 seconds, the temperature development reveals a higher slope in case of SoL-2. A higher stationary junction temperature T_j follows. This surprising result is addressed within the evaluation in section 6.1.

Starting from the initial state SoL-0, different SoL were obtained by artificially ageing which should simulate a bond-wire lift of during a power-cycling test. In fact, bond-wires were cut intentionally within the loop. The cut location was selected with respect to experiences from active power cycled bond-wire lift-offs [7] and the hot-spot analysis by IR-camera. The chronology of the cuts is shown in Fig. 10b). Due to the consecutive cuts, the $V_{CE(on)}$ at room temperature increased as listed in Fig. 9.



SoL	$V_{CE(on)}$ (@ RT)
0	100.0 %
1	101.6 %
2	104.6 %
3	108.7 %

Fig. 9: Junction temperature development during repetitive switching events at 500 Hz with respect to different SoL. The temperature T_j does not start at room temperature (RT), because the first recorded turn-off pulse was captured after two seconds repetitive operation. A zoomed plot for the first 18 seconds is shown.

The temperature profile in Fig. 10a) was extracted along the 8 different segments and could reveal the position of the bond wires, as well as the point of maximum temperature.

The development of surface temperature was further evaluated as shown in Fig. 11. The displayed temperature T_{surf} was obtained by averaging 2 points close to the bond foot as shown in Fig. 10a) for segment 1.
From Fig. 11 it can be evaluated, that segments with cut bond-wire become thermally relieved, whereas surrounding segments become hotter. For each ageing state, a maximum $T_{surf(max)}$, mean $T_{surf(mean)}$, and minimum $T_{surf(min)}$ surface temperature can be determined. The mean temperature was obtained by averaging all segment temperatures within one SoL.

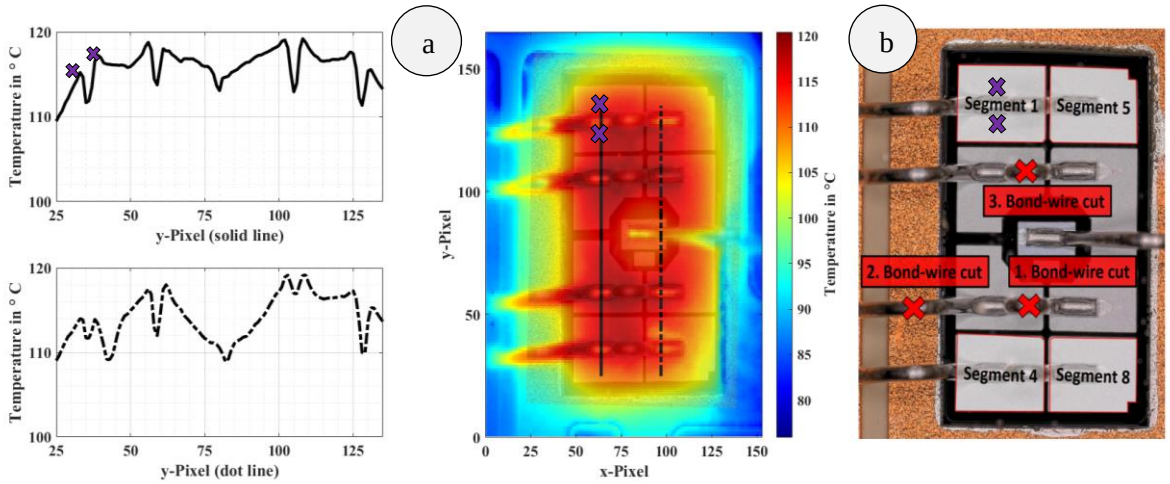


Fig. 10: a) Exemplary surface temperature analysis with IR camera for initial state SoL-0. Image was taken after 20 min repetitive switching operation at 500 Hz. In addition to two temperature profiles along the surface, measurement points (x) next to the bond foot were inserted and evaluated in order to obtain the temperature for each segment. b) Further, the chronology of bond-wire cuts (x) is indicated.

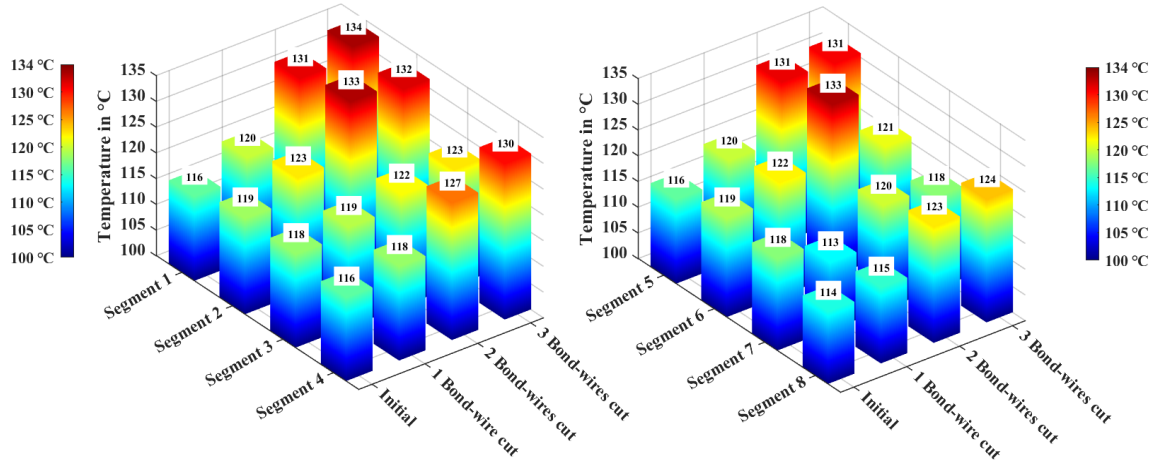


Fig. 11: Evaluation of the surface temperature for each segment of the emitter metallization at different SoL after 20 min repetitive switching events at 500 Hz.

6. Development of temperatures and their distribution with respect to SoL and switching frequency

How the junction, case, and surface temperature have changed with respect to the SoL of the DUT and the applied switching frequency, is described in detail within the following subsections.

6.1. Junction temperature

As shown in Fig. 12, the junction temperature T_j increases more, with respect to the SoL, when a higher switching frequency of 1000 Hz was applied during the test. Already at SoL-1 with 1.6 % $V_{CE(on)}$ increase (the DUT did not reach EoL (PCT 5% limit)) the evaluation reveals an exceedance of the

recommended junction temperature T_{vjopt} of 150 °C, when switched with 1000 Hz. At SoL-2 and an increase of $V_{CE(on)}$ by 4.6 %, the junction temperature is exceeding 150 °C with 500 Hz, too.
An unexpected trend was revealed in case of a switching frequency with 500 Hz. In fact, a further increased ageing state from SoL-2 to SoL-3 revealed a junction temperature drop from 154 °C down to 148 °C. This development for the repetitive operation at 500 Hz contrasts with the investigation at 1000 Hz.

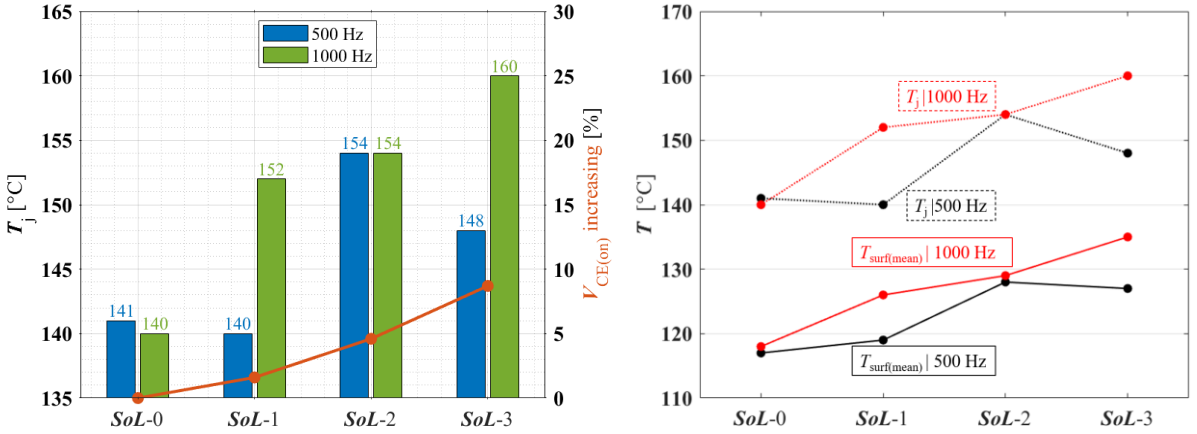


Fig. 12: (Left) Junction temperature T_j in steady state with respect to $V_{CE(on)}$ increase. (Right) Trend of the mean surface temperature $T_{surf(mean)}$ compared with the junction temperature. Both for different frequencies and ageing states.

The trend of the junction temperature T_j for 500 and 1000 Hz was also revealed for the mean surface temperature $T_{surf(mean)}$, as shown in Fig. 12 (right). The hypothesis, that self-balancing mechanisms become effective after a certain ageing state and can only take place up to a certain frequency, has to be proven by FEM simulations.

6.2. Surface temperature

The maximum surface temperature evaluation is shown Fig. 13 (left). A deviation of about 5 K occurs at the initial SoL. The highest temperature within all segments increases stronger in case of 1000 Hz. The deviation between hottest and coldest segment increases for both investigated frequencies with increasing degradation. The deviation can be directly linked to the degree of inhomogeneous temperature distribution at the surface. Within the investigated ageing range, the deviation goes up to 16 K and is almost independent from the switching frequency.

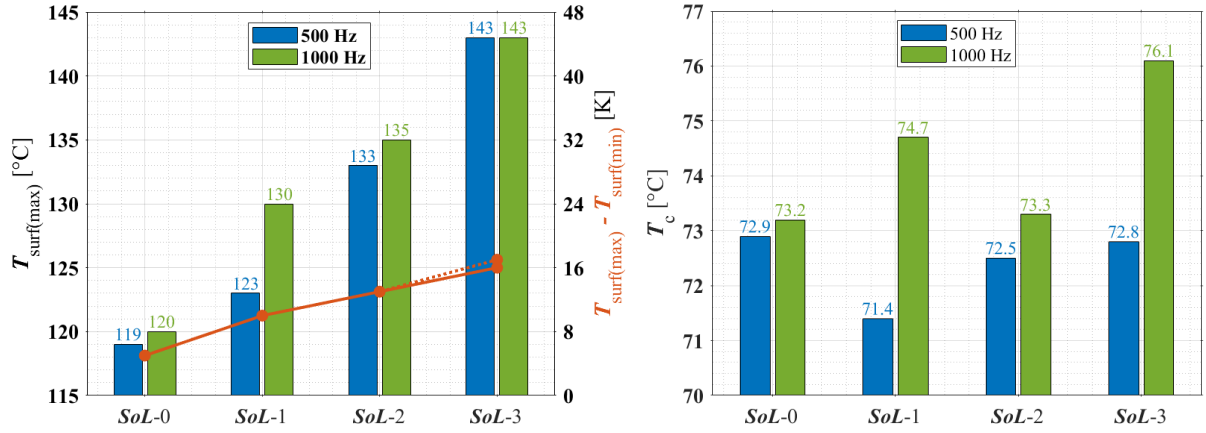


Fig. 13: (Left) Maximum surface temperature in steady state for different switching frequencies and ageing states. The temperature deviation represents the relative difference between hottest and coldest segment temperature with respect to all segments and accounts for the inhomogeneous temperature distribution. (Right) Case temperature in steady state for different switching frequencies and ageing states.

6.3. Case temperature

The case temperature development is presented in Fig. 13 (right). At 1000 Hz, the case temperature reveals an increasing trend with respect to a higher amount of cut bond-wires. At 500 Hz, the case temperature remains almost stable with a small change rate in comparison to the surface and junction temperature. Therefore, the benefit of the TC-measurement for this study is low.

7. Challenges of current adjustment and temperature determination

The presented results are part of the first attempt to evaluate the temperature development during converter-like repetitive hard switching events. Some limitations were found, which must be considered.

7.1. Junction temperature determination

Limited by the package of the DUT without a direct Kelvin connection, $V_{CE(on\text{-}load)}$ consists of the voltage drop across the chip $V_{CE(on\text{-}chip)}$ and a packaging share $V_{CE(on\text{-}package)}$ due to bond-wires and a common conduction path for load and sense current. During the initial and re-calibration after each artificially ageing step, a homogeneous temperature distribution is assumed. However, during repetitive switching operation, the package and the chip face an inhomogeneous temperature distribution, as could be evaluated from IR-camera pictures. Further analysis by FEM simulations and a DUT with kelvin connection have to be conducted in order to estimate the error in junction temperature determination. An additional junction temperature reference by $V_{CE(on\text{-}sense)} = f(T)$ method [4] could be useful.

7.2. Pulse pattern

Again, it has to be pointed out, that due to the static pulse pattern a repetitive turn-off current of 95 % $I_{C(nom)}$ was reached. However, the average current during the repetitive conduction phase, accounted for only 85 % $I_{C(nom)}$. A higher load inductance along with a dynamically adjusted pulse pattern could be used to operate closer to the permitted limits of the datasheet.

7.3. Mismatch between surface and junction temperature

The junction temperature was evaluated right before turn-off, where the heat development within a pulse reached the maximum. Limited by IR camera technology, the image could not be recorded at the same time. A not distinguishable difference in timing makes a quantitative comparison between determined junction temperature and recorded surface temperature difficult.

7.4. Artificial ageing

Front-side ageing mechanisms, as described and reported in detail for accelerated lifetime investigation by [7], are not covered by bond-wire cuts, only. In addition, the modification of the top-side metallization has to be taken into account. In dependency of the applied temperature swing, an increased sheet resistance according to [8] is expected, which could lead to an even higher inhomogeneous temperature distribution between segments [7].

8. Conclusion

In this paper, the development of temperatures at different positions of an IGBT chip and its package was monitored and analyzed with respect to different state-of-life and frequencies during repetitive hard-switching events. The junction temperature was determined by using the forward voltage drop $V_{CE(on\text{-}load)}$ at load current. Different ageing states were obtained by artificial cuts within bond-wire loops. It can be concluded that all investigated temperatures are affected by ageing and the switching frequency. With a higher degree of degradation and higher switching frequency, the found junction temperature and the inhomogeneous temperature distribution on the surface became larger. Following the presented results, before reaching the power-cycling end-of-life criterion of 5 % - $V_{CE(on)}$ increase, the tested device faced a higher peak temperature as it is recommended in the datasheet. The reliability of the results was discussed and further analysis is necessary to clear uncertainties, especially in case of the junction temperature determination.

References

[1] T. Harder, „ECPE Guideline AQG 324 - Qualification of Power Modules for Use in Power Electronics Converter Units in Motor Vehicles," 2019.

[2] M. Goller, M. A. Thiem, J. Song, J. Kowalsky, J. Franke und J. Lutz, „Investigation of the current collapse behaviour in GaN power HEMTs with highly adjustable pulse and measurement concept," in *In31st European Symposium on Reliability of Electron Devices, Failure Physics and Analysis, ESREF*, Microelectronics Reliability, Athen, 2020.

[3] I. Application Note, „High Speed SW Current measurement by Rogowski Coil Current Probe," [Online]. Available: https://www.pmk.de/web/editor/files/High%20Speed%20SW%20Current%20measurement%20by%20Rogowski%20Coil%20Current%20Probe_Iwatsu%20AppNote.pdf. [Zugriff am 18 May 2022].

[4] C. Herold, J. Franke, R. Bhojani, A. Schleicher und J. Lutz, „Requirements in power cycling for precise lifetime estimation," in *Microelectronics Reliability, 58:82-89,* 2016.

[5] C. Chen, V. Pickert, B. Ji, C. Jia, A. C. Knoll und C. Ng, „Comparison of TSEP Performances Operating at Homogeneuous and Inhomogeneous Temperature Distribution in Multichip IGBT Power Modules," IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS, VOL. 9, NO. 5 October, 2021.

[6] N. Degrenne und S. Mollov, „Robust On-line Junction Temperature Estimation of IGBT Power Modules based on Von during PWM Power Cycling," 2019 IEEE International Workshop on Integrated Power Packaging (IWIPP), Toulouse, France, 2019.

[7] C. Bäumler, M. Hernes, J. Kowalsky und J. Lutz, „Short Circuit Robustness of an Aged High Power IGBT-Module," in *EPE*, Genoa, 2019.

[8] J. Lutz, T. Herrmann, M. Feller, R. Bayerer und T. Licht, „Power cycling induced failure mechanisms in the viewpoint of rough temperature environment," Proceedings of the 5th International Conference on Integrated Power Electronic Systems, 2008.