

High Voltage Gain Interleaved DC-DC Converter with Voltage-Lift and Three-Winding Coupled-Inductor Techniques

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Abstract-- A new high voltage gain interleaved DC-DC converter is proposed for the renewable energy systems. The configuration is composed of two-phase boost converter integrating a voltage-lift capacitor and three-winding coupled-inductor-based voltage multiplier modules to achieve high voltage gain without operating at extreme duty ratio. The switch voltage stress is greatly lower than the output voltage such that MOSFETs with low on-resistance are available to reduce the conduction losses. Due to the leakage inductances of the coupled inductors, the switches can turn on with zero-current switching (ZCS), and the diode reverse-recovery problem is alleviated. The input current ripple is decreased due to the interleaved operation. The operational principle, steady-state analysis and design considerations of the proposed converter is presented. In addition, a closed-loop controller is designed to. Finally, experimental a 1000 W prototype with 24-400 V conversion is built and tested to validate the performance of the proposed converter.

Index Terms-- high voltage gain DC-DC converter, three-winding coupled-inductor, voltage multiplier modules, zero-current switching.

I. INTRODUCTION

Due to the global warming problem and the fast exhaustion of the fossil fuel, the demand for renewable energy sources has dramatically increased [1]. The renewable energy grid-connected system with PV panel and fuel cells calls for high voltage-gain and high-efficiency dc-dc converters because their low voltage should be boosted to a high voltage for the system as shown in Fig. 1. If the line voltage is 220 V_{ac}, a 380-400 V_{dc} bus voltage is required for the grid-connected applications. However, the output voltages of PV panel and fuel cells are generally lower than 40 V due to the safety and reliability considerations in the house-hold applications. Thus, a dc-dc converter with a high voltage gain is needed for a renewable energy system.

Theoretically, an ideal boost converter can realize a high voltage gain with an extreme duty ratio. However,

due to the parasitic elements, the voltage gain and efficiency tends to decrease after a given value of duty ratio in practical. In addition, it results in large current ripple, high switching losses, severe diode reverse-recovery problem, high switch voltage stress [2]. These problems are the main limitations for the boost converter in the high step-up voltage gain applications.

In recent years, the high voltage gain DC-DC converters have been researched in depth by different voltage-boosting techniques to improve the aforementioned issues [3-14]. The voltage-boosting techniques include coupled inductor [3-5], switched inductor/capacitor [6-7], built-in transformer [8-9], voltage multiplier cell [10], three-level converters [11-12], and so on. The review papers are good references for the research development of the high voltage gain DC-DC converters [13-14].

A new high voltage gain interleaved dc-dc converter with voltage-lift and three-winding coupled-inductor techniques is proposed in this paper as shown in Fig. 2. The converter has the following features:

- (1) The high voltage gain can be obtained with an appropriate duty ratio.
- (2) The low-voltage-rating MOSFETs and diodes can be adopted to reduce the conduction losses.
- (3) The switches can turn ON under ZCS condition to reduce the switching losses.
- (4) The diode reverse recovery issue is mitigated due to the leakage inductors of the coupled inductors, and the leakage energy is recycled.
- (5) The input current ripple is reduced by interleaved operation.

The operation principle, steady-state analysis, design considerations and controller design of the proposed converter are presented. The experimental results on a 1000 W prototype converter are provided to validate the performance of the proposed converter.

II. PROPOSED CONVERTER AND OPERATIONAL PRINCIPLE

The proposed converter with three-winding coupled inductors is shown in Fig. 2. The configuration is composed of two-phase interleaved boost converter integrating a voltage-lift capacitor and two voltage multiplier modules (VMMs) to achieve high voltage gain. VMM is composed of the secondary and tertiary windings

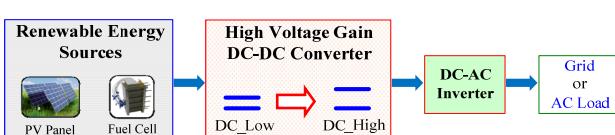


Fig.1. Block diagram of a renewable energy system.

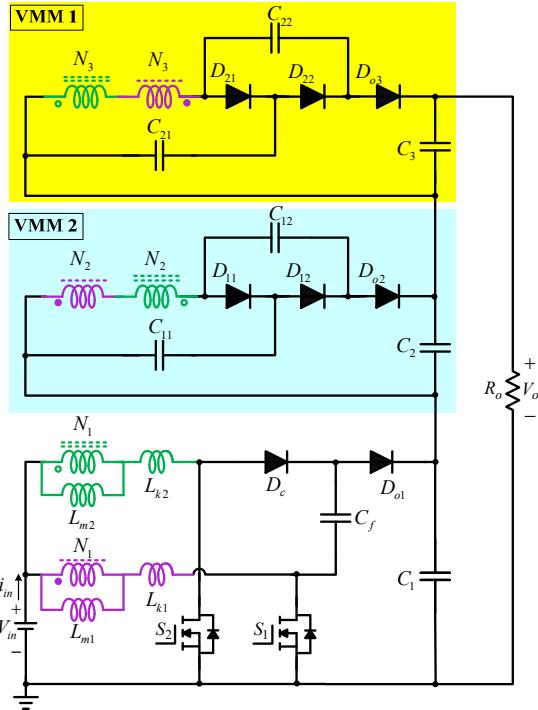


Fig. 2. Proposed converter.

of coupled inductor in series, diodes and capacitors, which is stacked on the output side to extend the output voltage. Each coupled inductor is modeled as a combination of an ideal transformer with a turns ratio $n = N_2 / N_1 = N_3 / N_1$, a magnetizing inductor L_m and a leakage inductor L_k . The coupling references are denoted by the marks “•” and “◦”. The key waveforms are shown in Fig. 3. Two 180° out-of-phase gate signals with the same duty ratio are applied to the switches. There are eight operational stages in one switching period. The corresponding equivalent circuits are shown in Figs. 4(a)~(h).

In order to simplify the circuit analysis, some assumptions are made as follows

- (1) All semiconductors (switches and diodes) are considered to be ideal.
- (2) All capacitors are sufficiently large, and the voltages on these capacitors are regarded as constant during one switching period.
- (3) The parameters of the three-winding coupled inductors are regarded to be identical, that is, turns ratio $n = N_2 / N_1 = N_3 / N_1$, $L_{m1} = L_{m2} = L_m$ and $L_{k1} = L_{k2} = L_k$. The coupling coefficient of coupled inductor $k = L_m / (L_m + L_k)$.

Stage 1 [$t_0 \sim t_1$]: At $t = t_0$, S_1 is switched ON and S_2 remains in the turn-on state. The diodes D_{o1} , D_c , D_{12} , D_{21} and D_{o3} are reverse-biased. The leakage inductor current i_{Lk1} increases rapidly from zero. The energy stored in the inductance L_m still transfers to charge C_{11} , C_{22} and C_2 via the secondary and tertiary windings of coupled inductors. The currents i_{D11} , i_{D02} and i_{D22} decrease when $i_{Lk1} < i_{Lm1}$. This stage ends when $i_{Lk1} = i_{Lm1}$.

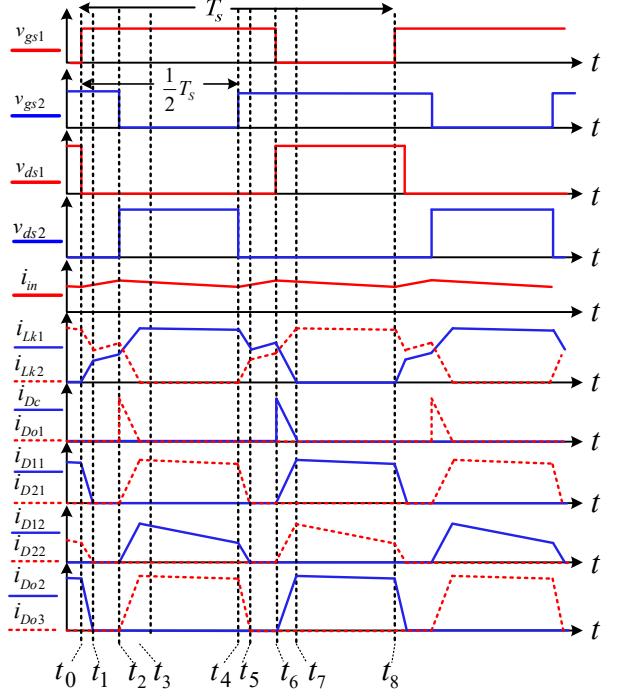


Fig. 3. Key steady-state waveforms.

Stage 2 [$t_1 \sim t_2$]: At $t = t_1$, S_1 and S_2 both turn ON. All diodes are reverse-biased. L_{m1} and L_{m2} as well as L_{k1} and L_{k2} are linearly charged by the input voltage V_{in} . The output capacitors C_1 , C_2 and C_3 supply energy to the output load.

Stage 3 [$t_2 \sim t_3$]: At $t = t_2$, S_1 is turned OFF. Due to the continuity of i_{Lk2} , it makes D_c turn on, and the voltage-lift capacitor is charged. i_{Lk2} decreases and the energy stored in L_{m2} transfers to the VMMs charging C_{12} , C_{21} and C_3 via coupled inductors. C_{11} and C_{22} are discharged. This stage ends when i_{Lk2} decreases to zero.

Stage 4 [$t_3 \sim t_4$]: At $t = t_3$, i_{Lk2} decreases to zero and the diode D_c naturally turns off with ZCS. There is no reverse recovery losses for D_c . The energy stored in L_{m2} is still transferred to the secondary and tertiary sides of coupled inductors. The switch current i_{S1} is equal to the summation of the magnetizing currents i_{Lm1} and i_{Lm2} . This stage ends when S_2 is turned on.

Stage 5 [$t_4 \sim t_5$]: At $t = t_4$, S_2 starts to conduct and S_1 keeps in on-state. D_{o1} , D_c , D_{11} , D_{o2} and D_{22} are reverse-biased. Due to the existence of leakage inductor L_{k2} and $i_{Lk2}(t_4)=0$, S_2 achieves ZCS turn-on. In this stage, the leakage current i_{Lk2} increases rapidly from zero. The magnetizing energy stored in L_{m2} still transfers to the second and third windings of the coupled inductor when $i_{Lk2} < i_{Lm2}$. i_{D12} , i_{D21} and i_{D03} decrease and the descent rate is limited by L_{k1} and L_{k2} . Therefore, the

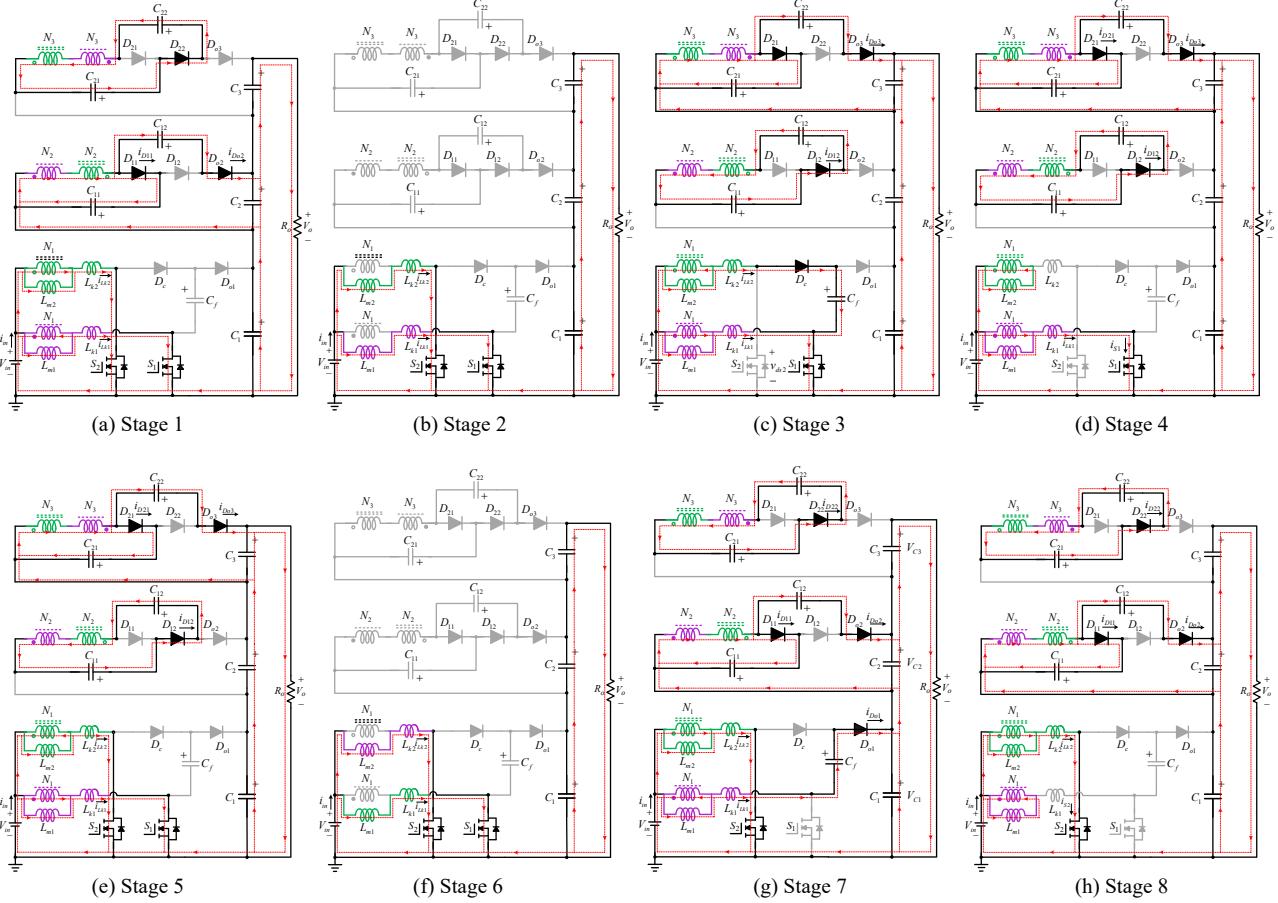


Fig. 4. Operational stages of proposed converter

diode reverse recovery issue is lessened. When i_{Lk2} rises to reach $i_{Lk2} = i_{Lm2}$ at $t = t_5$, The currents i_{D12} , i_{D21} and i_{Do3} decrease to zero.

Stage 6 [$t_5 \sim t_6$]: At $t = t_5$, S_1 and S_2 conduct, and all diodes are reverse-biased. The magnetizing inductors L_{m1} and L_{m2} as well as the leakage inductors L_{k1} and L_{k2} are supplied energy by the input voltage V_{in} . The leakage currents i_{Lk1} and i_{Lk2} increase linearly. C_1 , C_2 and C_3 provide energy to the output load. When the switch S_1 is turned OFF, the stage ends.

Stage 7 [$t_6 \sim t_7$]: At $t = t_6$, S_1 is turned OFF. D_{o1} begins to conduct because i_{Lk1} is continuous. D_{11} , D_{22} , D_{o1} and D_{o2} are forward-biased. i_{Lk1} flows through D_{o1} , C_f and C_1 to charge the output capacitor C_1 and discharge the voltage-lift capacitor C_f . The voltage across S_2 is clamped by the capacitors C_f and C_1 . During this stage, i_{Lk1} decreases and the energy stored in L_{m1} is transferred to charge the capacitors C_{11} and C_{22} via the second third windings of the coupled inductor. In the meanwhile, C_{12} and C_{21} are discharged. When i_{Lk1} decreases to zero, this stage ends.

Stage 8 [$t_7 \sim t_8$]: At $t = t_7$, the leakage energy stored in L_{k1} is released completely. Thus, the output diode D_{o1} is ZCS turned OFF naturally. The magnetizing current i_{Lm1} is reflected from the first winding to the second and third windings completely. The operation of this stage in the VMMs is similar to that of the stage 7. When S_1 returns to conduct at $t = t_8$, this stage ends. Then another new switching cycle begins.

III. STEADY-STATE ANALYSIS

In order to simplify the steady-state analysis of the proposed topology, the transient stages of stage 1 and 5 are disregarded due to significantly short time, the leakage inductors are ignored with coupling coefficient $k=1$.

By applying the volt-second balance principle on L_{m1} and L_{m2} , the voltage on C_f and C_1 can be given by

$$V_{Cf} = \frac{1}{1-D} V_{in} \quad (1)$$

$$V_{C1} = \frac{2}{1-D} V_{in} \quad (2)$$

In the operational analysis of stage 3 and stage 7, the voltages on the different capacitors can be expressed as

$$V_{C11} = V_{C21} = \frac{kn}{1-D} V_{in} \quad (3)$$

$$V_{C12} = V_{C22} = \frac{2kn}{1-D} V_{in} \quad (4)$$

$$V_{C2} = V_{C3} = \frac{3kn}{1-D} V_{in} \quad (5)$$

From the Eqs. (2) and (5), the output voltage of the proposed converter can be derived by

$$V_o = V_{C1} + V_{C2} + V_{C3} = \frac{6kn+2}{1-D} V_{in} \quad (6)$$

Consequently, the voltage gain M_k of the presented converter can be written in the form

$$M_k = \frac{V_o}{V_{in}} = \frac{6kn+2}{1-D} \quad (7)$$

When the turns ratio $n = 1$, the different curves of voltage gain with various coupling coefficients, $k = 1, 0.95, 0.9$, are shown in Figure 5. Clearly, the coupling coefficient k has little influence on the voltage gain. If the leakage inductor is ignored, that is, the coupling coefficient $k=1$, the ideal voltage gain of the proposed converter is written in the form

$$M = \frac{V_o}{V_{in}} = \frac{6n+2}{1-D} \quad (8)$$

From the Eq. (8), it can be concluded that the voltage gain of the proposed converter has two degrees of design freedom, turns ratio and duty ratio. The high voltage gain of the proposed converter can be achieved without an extremely large duty ratio if the designer selects the appropriate turns ratio of the coupled inductor. The voltage gain curves related to turns ratio and duty ratio are plotted in Fig. 6. One can see that the voltage gain is 20 times if the duty ratio $D = 0.6$ and the turns ratio $n=1$.

IV. DESIGN CONSIDERATIONS

A. Design of magnetizing inductor and capacitors

In order to operate in CCM and current-ripple consideration, the magnetizing inductor of the coupled inductor is designed. If the average current through the magnetizing inductor is denoted as I_{Lm} and its ripple current is denoted as Δi_{Lm} , then the condition for the CCM operation can be represented as

$$L_m > \frac{(1-D)^2 V_o^2 D T_s}{(6n+2)^2 P_o} = \frac{D(1-D)^2 R_o}{(6n+2)^2 f_s} \quad (9)$$

where f_s is the switching frequency.

The main consideration of each capacitor is to suppress the voltage ripple to an acceptable level. According to the operational principle of the presented converter, the output capacitor C_1 discharges to the load by the current V_o/R_o

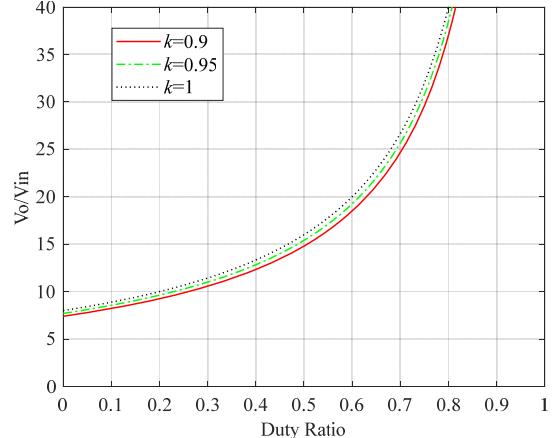


Fig. 5. Voltage gain curves vs. coupling coefficient ($n=1$).

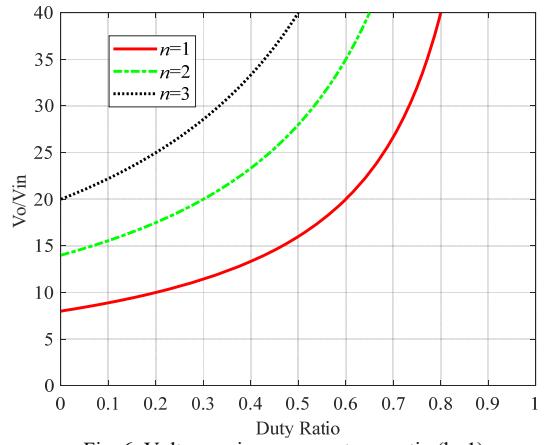


Fig. 6. Voltage gain curves vs turns ratio ($k=1$).

with the total time about DT_s . If the specification of $\Delta V_{C1}/V_{C1}$ is given, then the design condition of the output capacitor C_1 can be given by

$$C_1 = \frac{(3n+1)D}{R_o f_s (\Delta V_{C1}/V_{C1})} \quad (10)$$

Similarly, if the percentage of voltage ripple is specified, the design conditions of the output capacitors C_2 and C_3 can be respectively expressed as

$$C_2 = \frac{(6n+2)D}{3nR_o f_s (\Delta V_{C2}/V_{C2})} \quad (11)$$

$$C_3 = \frac{(6n+2)D}{3nR_o f_s (\Delta V_{C3}/V_{C3})} \quad (12)$$

The average charging current $\bar{i}_{C11(\text{charge})}$ of the regenerative capacitor C_{11} in one switching period is equal to the average current \bar{i}_{D11} of the regenerative diode D_{11} . By applying the amp-second balance principle, the design condition of capacitor C_{11} can be expressed as

$$C_{11} = \frac{(6n+2)}{nR_o f_s (\Delta V_{C11}/V_{C11})} \quad (13)$$

Similarly, the values of the other capacitors can be respectively designed by

$$C_{12} = \frac{(6n+2)}{2nR_o f_s (\Delta V_{C12}/V_{C12})} \quad (14)$$

$$C_{21} = \frac{(6n+2)}{nR_o f_s (\Delta V_{C21}/V_{C21})} \quad (15)$$

$$C_{22} = \frac{(6n+2)}{2nR_o f_s (\Delta V_{C22}/V_{C22})}$$

B. Design Controller

In order to keep the output voltage at a specific value regardless of input voltage fluctuations and load changes, the closed-loop control system is employed to obtain the good output voltage regulation as shown in Fig. 7. In the block diagram, $C(s)$ is the controller transfer function, and $1/V_p$ is the pulse-width modulator (PWM) gain where V_p is the amplitude of sawtooth waveform. $P(s)$ is the transfer function. K is the sensor gain of the output voltage.

The controller is required to design such that the open-loop transfer function $T_{OL}(s)$ meets the following specifications:

- The gain crossover frequency is 1 kHz.
- The phase margin (P.M.) is larger than 45° .
- The low frequency gain of the frequency response of $T_{OL}(s)$ is very high to reduce the steady-state error.

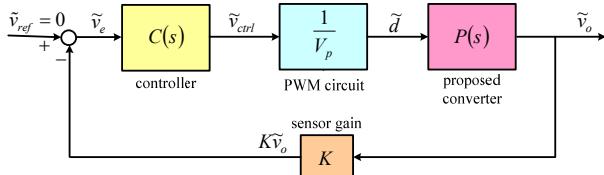


Fig. 7. Block diagram of the feedback system

The frequency response analyzer NF FRA51602 is used to measure the frequency response from the signal \tilde{v}_{ctrl} to the signal $K\tilde{v}_o$. Then the curve fitting method by MATLAB software is used to establish the transfer function of $G(s)$, the result is obtained by

$$G(s) = \frac{K\tilde{v}_o(s)}{\tilde{v}_{ctrl}(s)} = \frac{1.54}{\left(1 + \frac{2.2}{1400}s + \frac{1}{1400^2}s^2\right)}. \quad (16)$$

Then, the K factor approach [15] is employed to design the Type III controller for the $G(s)$. The electronic circuit with six passive components is illustrated in Fig. 8. The controller transfer function is designed and obtained as

$$C(s) = \frac{1.13 \times 10^6 (s + 2024)(s + 1761)}{s(s + 24380)(s + 20903)} \quad (17)$$

with the parameters: $R_1 = 100 \text{ k}\Omega$, $R_2 = 426 \text{ k}\Omega$, $R_3 = 9.2 \text{ k}\Omega$, $C_1 = 1.16 \text{ nF}$, $C_2 = 0.105 \text{ nF}$, $C_3 = 5.2 \text{ nF}$.

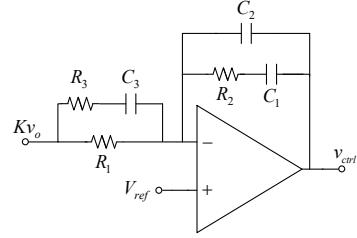


Fig. 8. Controller circuit.

With the designed controller, the frequency response of the open-loop transfer function $T_{OL}(s) = C(s)G(s)$ can be obtained. The control system provides a gain crossover frequency of 1 kHz, a phase margin of 50° , and very high DC gain. Thus, the designed controller satisfies the requirements of the voltage control system.

V. EXPERIMENTAL RESULTS

A 1000 W prototype converter with 24V input, 400 V output V and the switching frequency 50 kHz is built and tested. The parameters are listed in Table 1.

Table 1. Parameters of prototype converter.

Components	Parameters
Magnetizing inductors L_{m1}, L_{m2}	$73 \mu\text{H}$
Leakage inductors L_{k1}, L_{k2}	$0.6 \mu\text{H}$
Turns ratio of coupled inductor n	1
Output capacitors C_1, C_2, C_3	$150 \mu\text{F}$
Regenerative capacitors C_{11}, C_{21}	$82 \mu\text{F}$
Voltage-doubler capacitors C_{12}, C_{22}	$82 \mu\text{F}$
Switches S_1, S_2	FDP036N10A
Diodes $D_{11}, D_{21}, D_{12}, D_{22}, D_{o2}, D_{o3}$	V30120C
Diodes D_c, D_{o1}	30CPQ200

The waveforms of the gate signals, input voltage and output voltage are shown in Fig. 9. The voltage gain over 16 times is achieved without operating at extreme duty ratio. The waveforms of the input current i_{in} and the leakage-inductor currents i_{LK1} and i_{LK2} are shown in Fig. 10. It shows that the input current ripple is very small due to the interleaved operation. The voltage and current waveforms on the switch S_1 are shown in Fig. 11. As can be seen, the ZCS turn-on performance is realized such that the switching losses can be reduced. Moreover, the voltage stress on the switch is only one-eighth of the output voltage. Thus, the low-voltage-rated devices can be adopted to reduce the conduction losses.

The output voltage response and the output current under the load change between 500 W and 1000 W are illustrated in Fig. 12. As shown in the figures, the transient ripples of output voltage are clearly very small. The results demonstrate the good voltage regulation performance due to the well-designed controller for the closed-loop control system. The measured highest efficiency is 95.52 % at 200W, and the efficiency at 1000W full load is 87.36 % for the prototype converter.

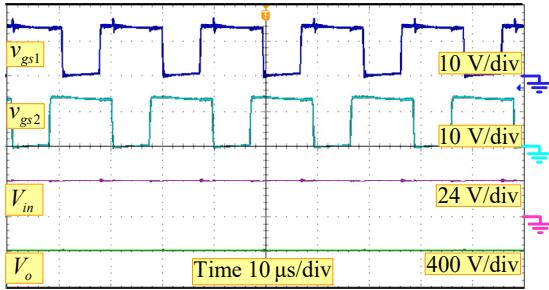


Fig. 9. Waveforms of gate signals, V_{in} and V_o .

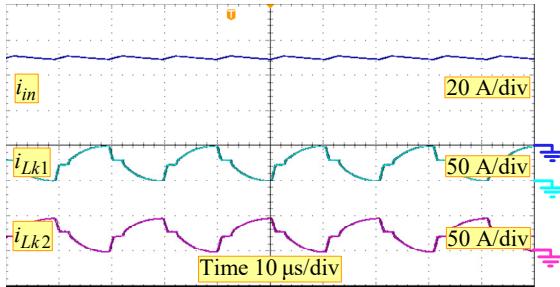


Fig. 10. Waveforms of i_{in} , i_{Lk1} and i_{Lk2} .

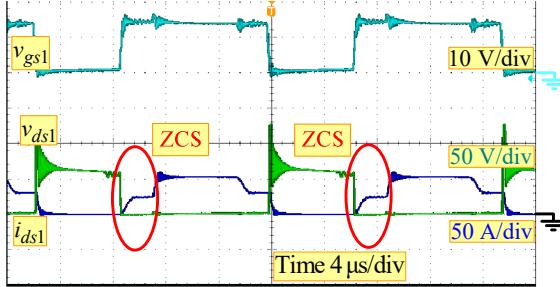


Fig. 11. Waveforms of voltage and current on S_1 .

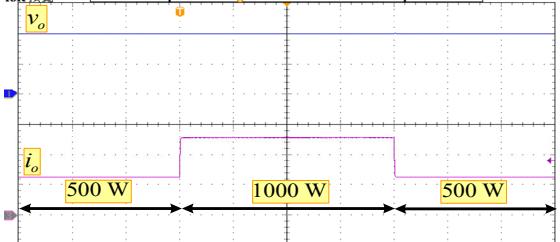


Fig. 12. Output voltage response of step load change.

VI. CONCLUSIONS

This paper presents an interleaved high voltage gain DC-DC converter with three-winding coupled inductors. The voltage conversion ratio is enlarged and the extreme duty ratio can be avoided in the high voltage gain applications. The voltage stresses of the switches and diodes are greatly lower than output voltage such that the lower-voltage-rating semiconductors can be adopted to reduce the conduction losses. The switches can turn on with ZCS performance to reduce the switching losses. The input ripple current is decreased by the interleaved operation. The diode reverse-recovery issue is alleviated by the leakage inductances of the coupled inductors. Finally, a 1000 W prototype with closed-loop control is implemented and the experimental results are given to validate the performance of the proposed converter.

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