Fast Switching Planar Inductance Current Source ZETA Converter with Integrated Common Mode Filter

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Acknowledgments

This research has been funded by the German Federal Ministry for Education and Research (project number 13FH541KX9). We thank the SEW-EURODRIVE GmbH & Co KG in Bruchsal, Germany for supporting this project.

Keywords

≪Planar magnetics≫, ≪Wide bandgap≫, ≪DC-DC power converter≫, ≪Current source≫, ≪Coupled inductor≫.

Abstract

The ZETA topology provides unique opportunities as a source for current-fed inverter systems. This topology enables coupling of input and output inductor to reduce the current ripple. In this paper, design aspects for a coupled inductor with an integrated common mode filter are described and the advantages to provide a current source characteristic using a ZETA converter are discussed. Relevant parasitic inductances and capacitances are calculated using finite element analysis and analytical models. The behavior of the multiphysics system consisting of electrical and magnetical domain is considered using a numerical system simulation including parasitic elements. This simulation shows good results and is compared to experiments. The experimental setup is using gallium-nitride eHEMT transistors with switching frequencies up to 1 MHz.

Introduction

Due to the increasing widespread use and high availability of fast switching wide-bandgap devices, the current source inverter topology is becoming more and more a focus also for the use at small power ranges [1][2][3][4]. When using fast switching devices the design of the dc link inductor is still challenging. Especially when dealing with low inductance loads, the current source inverter performance decreases if the dc link current ripple is increased. Therefore a minimal current ripple is beneficial. When using ac input to feed a current source inverter system the common solution is an active rectifier which is used to control the dc link current [5]. When using dc input (e.g. a battery) the variety of different possible topologies to realize current source characteristic for the dc link is huge. To choose and optimize the best possible circuit and control it is necessary to focus on the advantages and features while using synergetic effects. A basic example is the buck-boost synergetic control strategy described in [6] which shows that it is possible to use a buck converter inductance as dc link and combining the inverter boost capability

with the basic buck converter topology. The key in the design process is to use existing components to create new topological features.

In this paper the well-known ZETA topology [7][8] has been investigated. When removing the output capacitor the ZETA converter is suitable for a current source characteristic. It is also a common practice to use coupled inductors to decrease the output current ripple drastically [8]. Adding another inductance to the coupled inductor enables a new feature by integrating an output common mode filter.

The proposed topology is shown in fig. 1. On the one hand, in order to achieve a high power density, it is necessary to use high switching frequencies to minimize the inductor volume [11]. On the other hand high switching frequencies lead to increased EMI problems. With the aim of low manufacturing costs it is shown advantageous to use planar inductors based on PCB winding systems. Therefore a coupled inductor based on a PCB winding and standard E-I core was designed.

ZETA Converter

The basic ZETA topology provides a positive output voltage from a variable positive input voltage and can be operated in both step-up and step-down mode. Using two active switches it can be operated in bidirectional power mode. With inverted power flow the ZETA converter then operates as a SEPIC converter. Thus the converter is operating in continuous conduction mode and in order to achieve a current source characteristic, the output capacitor has to be removed. The output inductor then becomes

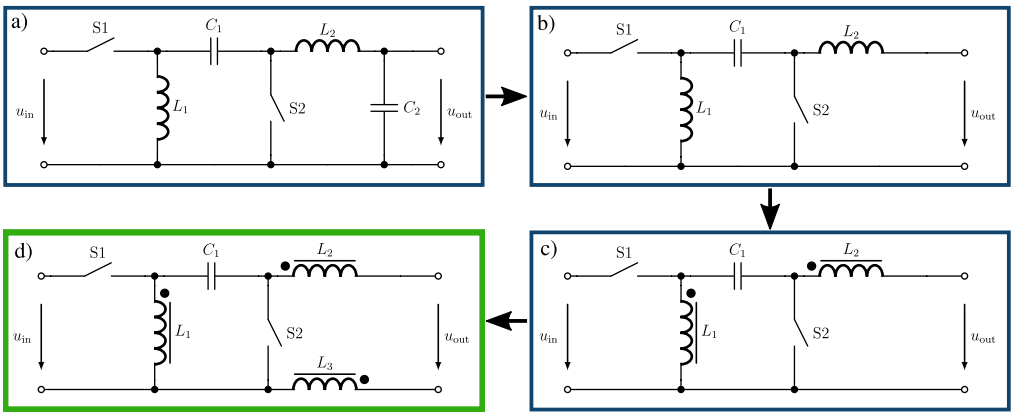

Fig. 1: a) basic bidirectional ZETA topology, b) removed output capacitor, c) added a coupling of the inductors, d) splitting the output inductor

the dc link inductor for use in current source inverter systems. To reduce the common mode noise the dc link inductor is often designed as a common mode choke [5] using coupled inductors. It is possible to further integrate this setup in the ZETA converter as shown in fig.1.

Proposed Topology and Application Ratings

Consequently the proposed topology is shown in fig. 2. The target application is a current source inverter

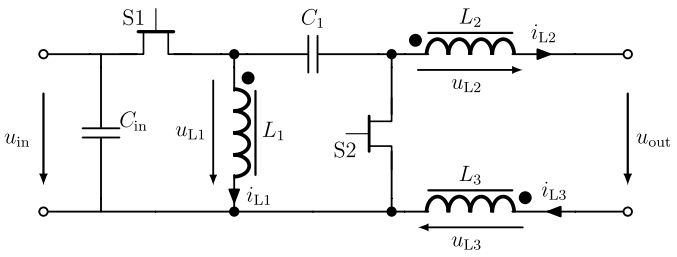

Fig. 2: Enhanced ZETA topology with integrated common mode filter and eHEMT transistors

Table I: Nominal Converter Ratings

input voltage	U_{in}	50 V
output current	I_{out}	5 A
output voltage	$U_{out,max}$	100 V
output power	$P_{out,max}$	500 W
switching frequency	f_{sw}	1 MHz

for a low power electric motor. The desired nominal converter ratings are shown in table I.

Coupled Inductor Design

The coupled inductor must meet multiple requirements. On the one hand the coupling should reduce common mode noise. On the other hand the inductor stores energy for the power conversion and reduces the output current ripple. Additionally the inductor should be reduced in size and use of material. The design process is similar to the design process of a dual-mode choke. A dual-mode choke decreases both common mode and differential mode noises and can be constructed in a single core geometry [12]. However, unlike a standard filter design the ZETA topology has to be considered.

Proposed Inductor Topology

The geometrical setup of the coupled inductor is shown in fig. 3. The inductor winding L_1 is the primary

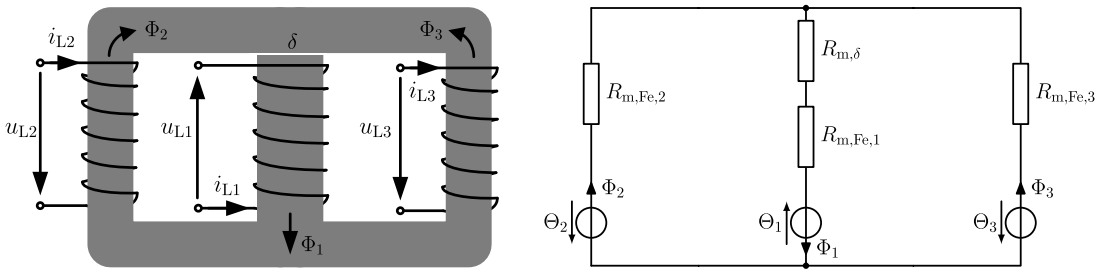

Fig. 3: Core geometry, winding setup and magnetic equivalent circuit

inductor of the ZETA converter and the flux, due to the current waveform, is inducing an additional negative voltage to the corresponding L_2 and L_3 winding terminals. This causes a decreased terminal voltage and thus a decreased current slew rate. The windings L_2 and L_3 are symmetrically coupled with winding L_1. An air gap δ is necessary for energy storage but also prevents saturation of the magnetic core material due to the high dc current in the windings. Thus resulting in a lower volume of the magnetic material. When applying a common mode current to L_2 and L_3 the magnetic flux components add to an opposing field which blocks the common mode noise. Because of the low magnetic resistance path the coupling between L_2 and L_3 is high. The magnetic equivalent circuit as shown in fig. 3 describes the mathematical relations of the coupled winding system. The following analytical terminal voltage model of the coupled inductor also considers the winding resistances R_{L1}, R_{L2} and R_{L3}.

$$\begin{pmatrix} u_{L1} \\ u_{L2} \\ u_{L3} \end{pmatrix} = \begin{pmatrix} R_{L1} & 0 & 0 \\ 0 & R_{L2} & 0 \\ 0 & 0 & R_{L3} \end{pmatrix} \begin{pmatrix} i_{L1} \\ i_{L2} \\ i_{L3} \end{pmatrix} + \begin{pmatrix} L_{11} & L_{12} & L_{13} \\ L_{21} & L_{22} & -L_{23} \\ L_{31} & -L_{32} & L_{33} \end{pmatrix} \cdot \frac{\mathrm{d}}{\mathrm{d}t} \begin{pmatrix} i_{L1} \\ i_{L2} \\ i_{L3} \end{pmatrix} \tag{1}$$

With the described magnetic circuit the inductance matrix can be analytically calculated and is defined by the flux distribution ignoring the leakage fluxes. The inductance values depend on the permeability of the used magnetic material, the geometrical dimension (length, cross-section and air gap) and number of turns of each winding. To consider leakage and nonlinear behavior of the used materials finite element calculations are necessary.

Finite Element Analysis (FEA)

To perform the finite element calculations a 3D model of the inductor is created. The used planar E-I core is a standard catalog part and therefore highly available and cost efficient. Each winding has a turn number of 6 and is distributed on two PCB layers as shown in fig. 4.

Inductance Matrix and Inductive Coupling Coefficients

The FEA yields the inductance matrix and the inductive coupling coefficients of the winding terminals. The calculated values are shown in table II. The coupling coefficient between L_2 and L_3 is limited by the core permeability. The calculated values are used to extend the model described in equation 1 which is then used in the numerical simulation.

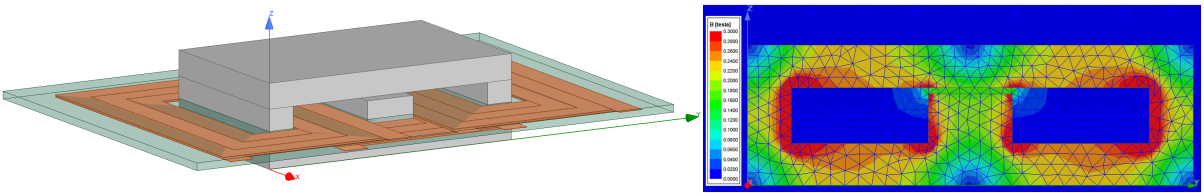

Fig. 4: 3D model of the planar coupled inductance, flux density at maximum power rating

Table II: Calculated inductance values and coupling coefficients

$L_{i,j}$	$i=1$	$i=2$	$i=3$
$j=1$	22.358 µH	10.975 µH	10.975 µH
$j=2$	10.975 µH	81.389 µH	69.308 µH
$j=3$	10.975 µH	69.308 µH	81.389 µH

$k_{i,j}$	$i=1$	$i=2$	$i=3$
$j=1$	1	0.257	0.257
$j=2$	0.257	1	0.852
$j=3$	0.257	0.852	1

Parasitic Capacitances

Because of the expected high voltage gradient du/dt parasitic capacitances can not be ignored. Many different equivalent circuits for parasitic capacitances in transformers and coupled inductors has been presented [13][14][15]. A common way is to differ between the winding self capacitance and the coupled capacitances between windings as shown in fig. 5. To determine the self capacitance values an analytical

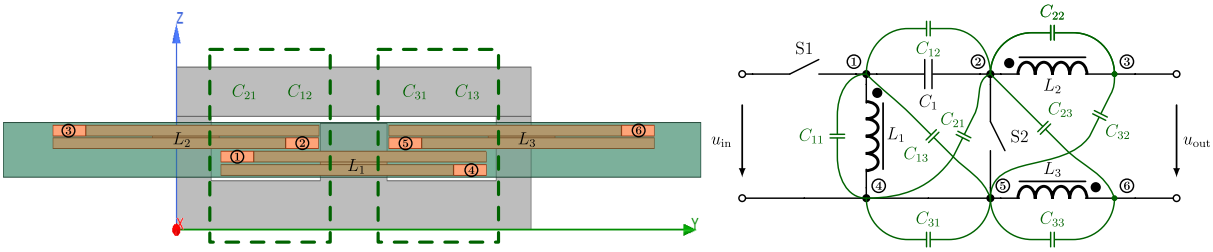

Fig. 5: Schematic layer structure and parasitic capacitances

calculation method for planar inductors is shown in [15], which is proven by FEA and experimental results. The winding coupling capacitances are much harder to determine but the parasitic effect can be avoided or minimized when changing the capacitive coupling of winding systems. In fig. 5 it is shown that due to the special core and winding arrangement the coupling of windings is minimized. Implementing the coupled inductor into the ZETA topology shows that some parasitic capacitances are not relevant (e.g. shorted) or can be used parallel to existing capacitances. The biggest parasitic effect have the self capacitances of each winding, which has to be considered in the simulation and experimental design. Therefore the capacitances have been minimized by using wide distances and a low number of turns. The capacitance matrix of the setup has been calculated by FEA. The relevant coupling capacitance and the self capacitances have been calculated yielding $C_{21} = 90\,\text{pF}$ and $C_{11} = C_{22} = C_{33} = 70\,\text{pF}$.

Simulation Setup and Results

In order to determine the functionality a full parametric numerical system simulation is performed using matlab, simulink and the simscape library. The simulation contains the power electronic system for the ZETA topology, the load model and additionally the magnetic system for the coupled inductor model. Both domains are linked within the conservative simulation environment as displayed in the simulation schematic in fig. 6. Relevant parasitic components as described in the previous section are also consid-

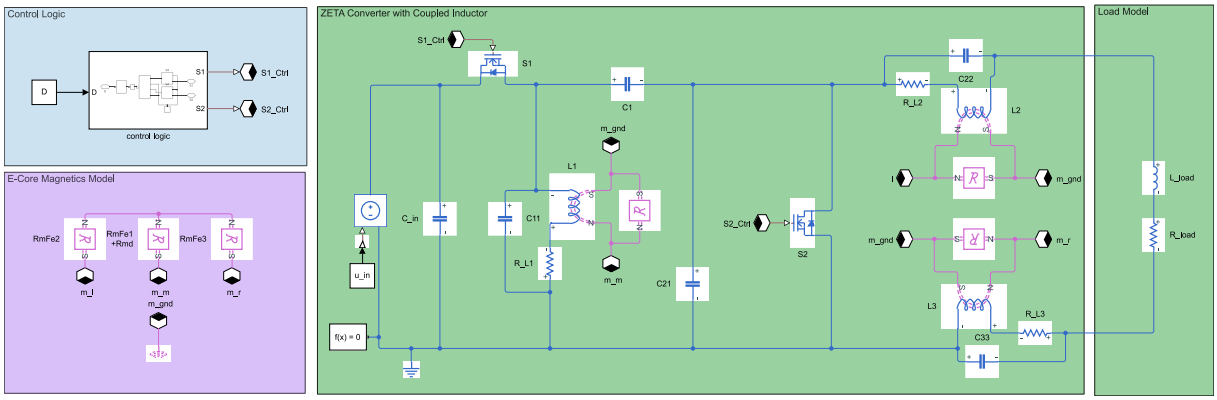

Fig. 6: Multi-domain numerical system simulation schematic in simulink

ered in the simulation. Due to the full parametric approach the influence of the switching frequency can easily be highlighted. Fig. 7 shows the resulting current ripple at different switching frequencies. Also

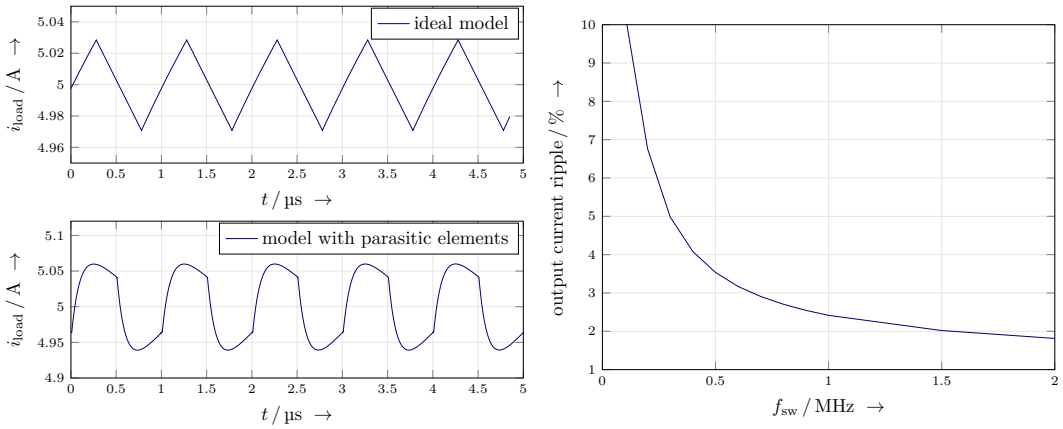

Fig. 7: Simulation results of an ideal converter and with parasitic elements at 1 MHz switching frequency (left). Switching frequency and corresponding current ripple (right).

the parasitic effects are seen in the results in fig. 7. Unfortunately it was not possible to include a dynamic transistor model because the existing models are not compatible with the used simulation environment. To get even better simulation results this can be done in the future. The simulation is using a fixed duty cycle so that the maximum power rating is achieved. Further a small deadtime which is also necessary in the experiment has been inserted.

Experimental Setup and Results

For the experimental evaluation a schematic and PCB layout has been created which is shown in fig. 8. To minimize the current density in the inductor windings parallel layers as well as a stacked PCB are used. The stacked PCB design also further reduces the parasitic capacitances because of the increased distance between winding layers. The used standard E-I core is modified so that the middle path has a 400 µm air gap and is then pressed on the PCB as shown in fig. 8. A standard connector ensures the

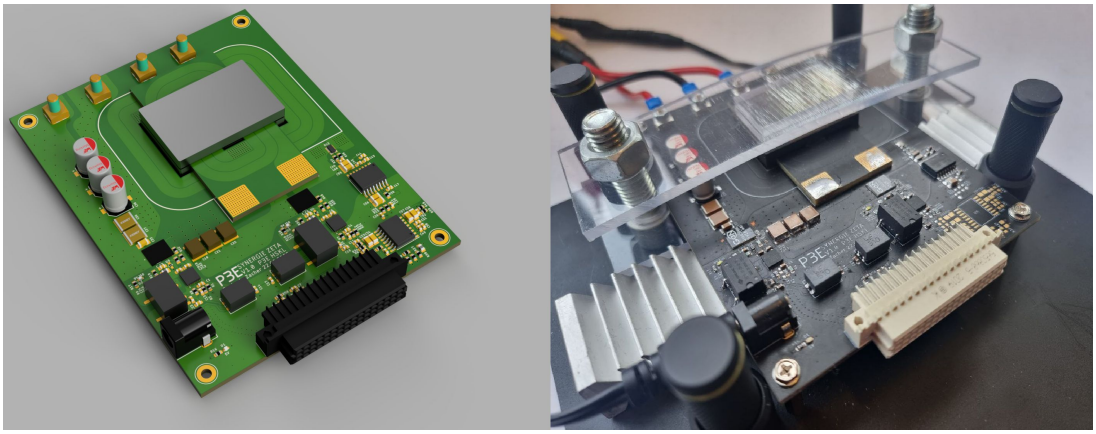

Fig. 8: 3D model of the experiment (left) and realized PCB (right)

safe connection to the controller board. The experimental setup uses GaN Systems eHEMT to realize 1 MHz switching frequency. Further to provide the necessary gate configuration an Infineon Technologies EiceDRIVER is used. The driver provides an isolated gate and supports switching frequencies up to 3 MHz. The driver is typically used to drive ohmic gate contact GaN transistors. Therefore the gate circuit had to be modified for the used schottky gate contact GaN Systems transistor. The gate voltage and the resulting drain-source voltages are shown in fig. 9. The gate voltage is set to negative at the off-switching phase to ensure safe off operation. Also in fig. 9 the drain source voltage of both switches show a ringing. This could not be optimized further because of the used gate circuit and is still a remaining problem. Because of the hard switching application the switching operation defines the switching losses and heat generation. Further a small deadtime is inserted which is improving the switching oper-

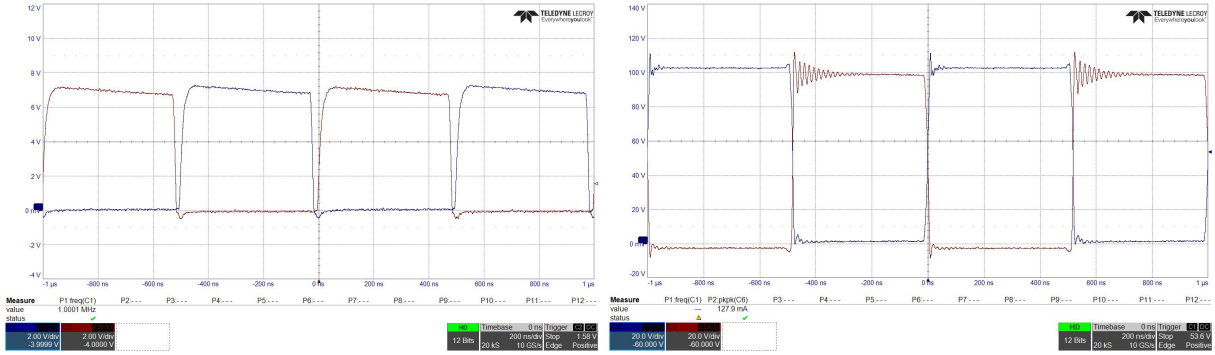

Fig. 9: Gate voltage (left) and drain source voltage (right) for both switches S1 (blue) and S2 (red)

ation. The deadtime has to be compensated in the control algorithm due to the nonlinear transfer function.

In order to measure the ouput current ripple a low inductance resistor was used. The inductance of the load including cables was determined below 8 µH. Because of this parasitic inductance the measurement results can not directly be compared to the simulation results but still the general functionality can be determined. Fig. 10 shows the measured output current at 100 kHz, 500kHz and 1 MHz switching frequency. At low switching frequencies the current ripple is defined by the current slew rate due to the duty cycle of the converter operation. Fig. 10 also shows that the ringing in the switching operation is affecting the resulting current ripple. At high switching frequencies the ringing which is caused by the switching operation is dominating the output current ripple so it remains unchanged at 500 kHz and 1 MHz respectively.

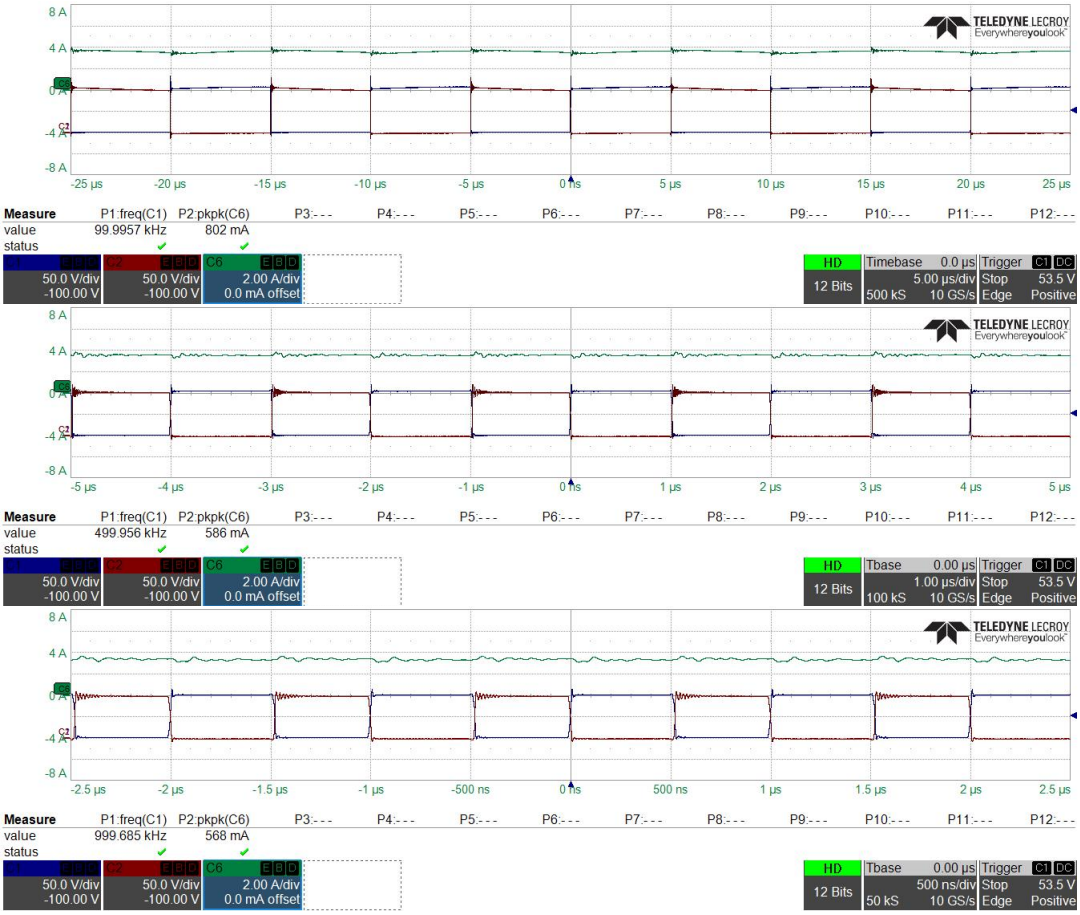

Fig. 10: Measured output current at different switching frequencies. Output current (green). Drain source voltage of S1 (blue) and S2 (red)

Conclusion

In this paper, the ZETA topology has been investigated, which is a good candidate for feeding battery powered current source inverter systems due to its unique possibility for coupled inductors. The further integration of an additional coupled winding system enables the feature of reducing common mode noise. The design of the coupled inductor is challenging and needs to consider parasitic elements. The parasitic inductances and capacitances have been calculated with FEA and are used to enhance the numerical simulation models. The numerical simulations show very promising results. An experiment was performed and it was shown that the basic converter function is working. It was not possible to match and verify the simulation results because the switching operations could not be sufficiently optimized. This research enables a deeper understanding for using PCB winding inductors for converters with high switching frequencies and high current densities. Further it opens up a field for multi-objective optimization of this system. When optimizing the layout and the switching operation the proposed system is a good candidate for current-fed inverters.

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