Transient Liquid Phase Bond Reliability Evaluation of Die-attach for Power Module Packaging

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Abstract

This paper presents the low temperature and pressure-less Sn-Cu solder technology process by means of Transient Liquid Phase (TLP) diffusion phenomena for high temperature power module packaging. The Sn-Cu diffusion process is developed for bonding a large area dies and its reliability are evaluated by the bond strength and accelerated active and passive thermal cycling tests.

1. Introduction

Strong demand of high melting die-attach materials has been driven by rapid progress in power electronics for medium and high-power modules. High lead (Pb) solder alloys with melting temperatures above 280 ºC are not allowed to be use for some application sectors such as automotive and aerospace due to the RoHS (Restrictions of Hazardous Substances) regulations of the European Union. Popular Pb-free solder alloys, such as Sn-Ag-Cu and Sn-Sb, exhibit very poor thermo-mechanical reliability [1]. However, the sinter materials such as silver and copper are good candidates for high temperature applications because of their better electrical and thermal conductive properties, but the material cost is high and the process is complex [2,3]. An alternating solution to the Pb-free die attach process is Transient Liquid Phase (TLP) bonding, also known as solid-liquid interdiffusion (SLID) boding [4-6]. It involves the incorporation of a low melting temperature metal into another high melting temperature metal matrix to create an intermetallic compound (IMC) with an intermediate melting temperature. It enables the use of a low process temperature for creating a high re-melting temperature (>400ºC) joint and shorter process time as the kinetics of liquid-solid diffusion is much faster than solid-state diffusion. In addition, the IMC joints with a high re-melting temperature improve creep resistance at elevated temperatures compared to solder joints [4,7]. Sn-based alloy, specifically Sn-Cu metal matrix, is one of the attractive alloys in the electronics industry as Sn reacts to the Cu quickly and creates intermetallic compounds (IMCs) in the entire bond.

The process development for the large-area die attach is one of the key technologies to enable highly-reliable next-generation standardized power module manufacturing for railway traction inverter applications [8]. The high melting temperature joining technology could be implemented with high-power density, high switching frequencies with a smaller size of wide band gap (WBG) devices such as silicon carbide (SiC) and gallium nitride (GaN) for high temperature operation capability and improved reliability.

This paper describes the large area die attach (area > 100mm^2, FRD and IGBT) by TLP diffusion soldering process on which reliability analysis has been performed by thermal shock and active power cycling test methods. The TLP diffusion soldering process has been optimized by die shear strength using smaller die size whereas bend tests have been carried out for the larger size of dies. Static electrical characteristic tests have been performed before and after the thermal shock reliability test. Scanning acoustic microscopy (SAM) was carried out to detect any die bond degradation after reliability tests whereas SEM-EDS analysis was carried out to investigate the complete formation of the Cu-Sn IMC structure.

2. Experimental works

The design choices of the experiments prepared with Ag back metallization dies and Si_3N_4 ceramic DBC substrates were made to produce binary high melting temperature Cu-Sn IMC. A conventional reflow oven was used for the pressureless TLP soldering process. The Cu-Sn paste was applied onto the substrate via a 100µm thick stencil. The diffusion soldering process was optimized by considering different process temperatures (255ºC -290ºC) and isothermal holding times under a N_2 environment. The diffusion process conditions were optimized by achieving a full conversion of the Cu-Sn matrix into the IMCs in the entire bond and minimizing the void level. Table I shows the process parameters considered for TLP soldering of die size 3x3mm^2.

Table I: Process conditions for each run.

Run No.	Temperature (°C)	Holding time (minute)	Process environment
1	255	3	N_2
2	290	3	N_2
3	255	10	N_2
4	290	10	N_2

Die shear strength is one of the test methods normally used to check the bond strength for optimizing the soldering process. The best characterization method is the hot die shear test, but this is not available in-house. A similar method of combining isothermal ageing and die shear test was used instead. The thermal ageing was carried out at 175ºC for 1000 hours at atmospheric pressure. The die shear strength of thermally aged samples was analyzed, and the best performing process parameters for large area die soldering were selected. SEM-EDS cross-sectional analysis was carried out to investigate the full conversion of IMC matrix which are Cu_3Sn and Cu_6Sn_5.

After optimization of the TLP soldering process for smaller die size, the large size of Si FRD and IGBT (>100mm^2) were considered for TLPS soldering with a lower percentage of voids. The die bond adhesion for large size die was examined with the aid of a qualitative bend test where the mandrel diameter used for the bend test was 13mm. The reliability of large area die bond was carried out by thermal shock and power cycling tests. The test condition for the thermal shock test is ΔT=225ºC (-50ºC to 175ºC) and dwell time 30 minutes. The power cycling test parameters are ΔT=120ºC (T_{jmin}= 30ºC and T_{jmax}=150ºC), I_c=120A to 150A, coolant temperature 15ºC and t_{on}/t_{off}=0.5s/3s. Here T_{jmax}, $T_{jmin,}$ and I_c left variable to keep ΔT constant. Figure 1 shows a typical power cycling test sample. The reliability test samples were inspected optically and with SAM (Scanning acoustic microscopy) to identify any cracks or delamination initiated in the die bond area. The static electrical test was performed at room temperature and at elevated temperature levels on thermal shock samples after 1000 cycles.

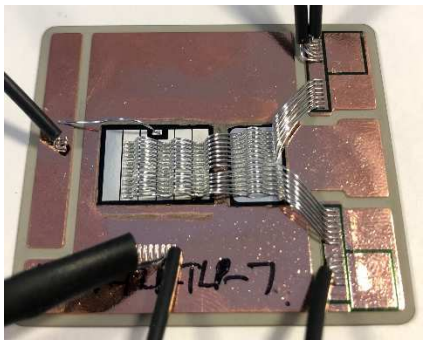


Fig. 1: A typical power cycling test sample of TLP soldered IGBT and FRD (1200V/200A).

3. Results and discussion

3.1. Shear strength analysis

Die shear test was carried out with samples consisting of 3mm×3mm die with varying process conditions (see table I). Die shear test was also carried out of thermal aging samples which were TLP soldered with similar process parameters. Figure 2 shows the average shear strength of as-soldered and after isothermal aging samples. The shear strength drops in Run 2 to Run 4 but increases in Run 1 after thermal aging. This indicates the negative correlation between the post-aging bond strength and process temperature. According to Tatsumi et al., at high temperature ageing, Cu_6Sn_5 IMC structure will transform to Cu_3Sn structure with two possible reactions [9].

$$9Cu + Cu_6Sn_5 \rightarrow 5Cu_3Sn \quad (1)$$

$$Cu_6Sn_5 \rightarrow 2Cu_3Sn + 3Sn \quad (2)$$

The reaction of equation (1) will be the main pathway according to Gibbs free energy change which is a negative value of ~89kJ/mol whereas equation (2) is a positive value of ~10kJ/mol [10]. The hypothesis for such correlation is that higher temperature produces more Cu_3Sn species, which in turn develops Kirkendall voids during thermal aging. For this reason, a lower process temperature or time is preferred in order to minimize the Cu_3Sn phase at the die bonding stage. In Figure 2, a low temperature and shorter holding time (Run1) might have improved the shear strength of the TLP joint up to a 175ºC ageing temperature by a transformation from Cu_6Sn_5 to Cu_3Sn. The TLP process of Run 1 was considered for large area die attach on DBC substrate.

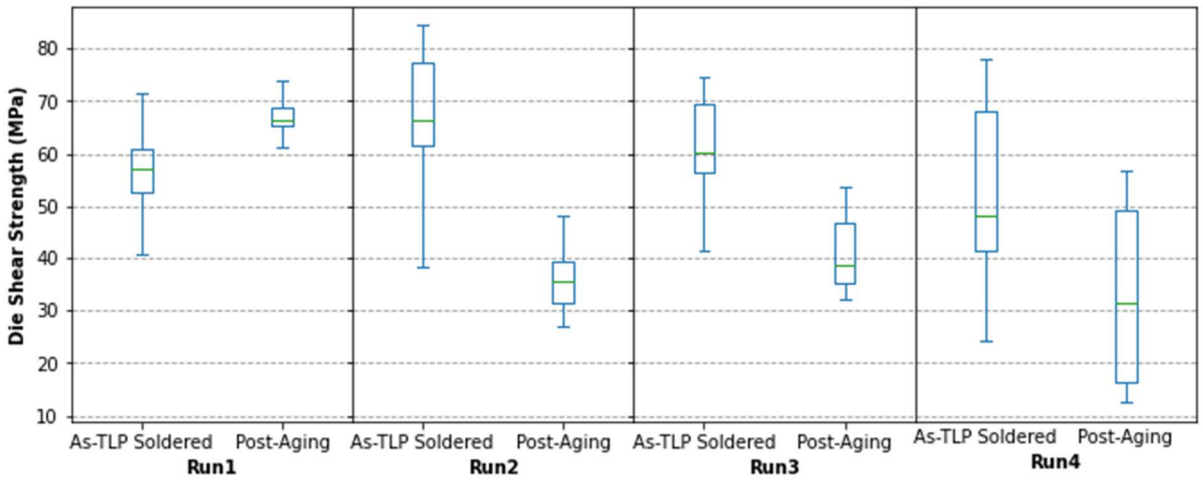


Fig. 2: TLP die bond shear strength, as-soldered and post-ageing in different process conditions.

3.2. TLP Bond Characterization

The metallographic cross-sectional analysis was carried out by SEM-EDX (Scanning Electron Microscopy-Energy Dispersive Spectroscopy) for microstructure evaluation of Sn-Cu matrix's TLP diffusion. Figure 3 shows the full conversion of Sn into intermetallic phases with Cu particles in a bulk structure and at the interface between TLP bond and substrate/die metallization, respectively. Figure 4 also shows the SEM-EDX analysis of the TLP bond. It is confirmed that all bulk Sn is consumed into IMC structure where the atomic ratio of Cu and Sn for Cu_3Sn phase is about 3:1 and for Cu_6Sn_5 phase is about 1.2:1. In addition, a continuous layer of IMC was observed at the die and substrate interface, confirming good adhesion on both interfaces. EDX analysis also confirmed the proportion of Cu_3Sn phase in the bond increases with increasing process temperature and holding time. This is expected as higher temperature causes diffusion growth of Cu_3Sn phase by transforming the Cu_6Sn_5 phase.

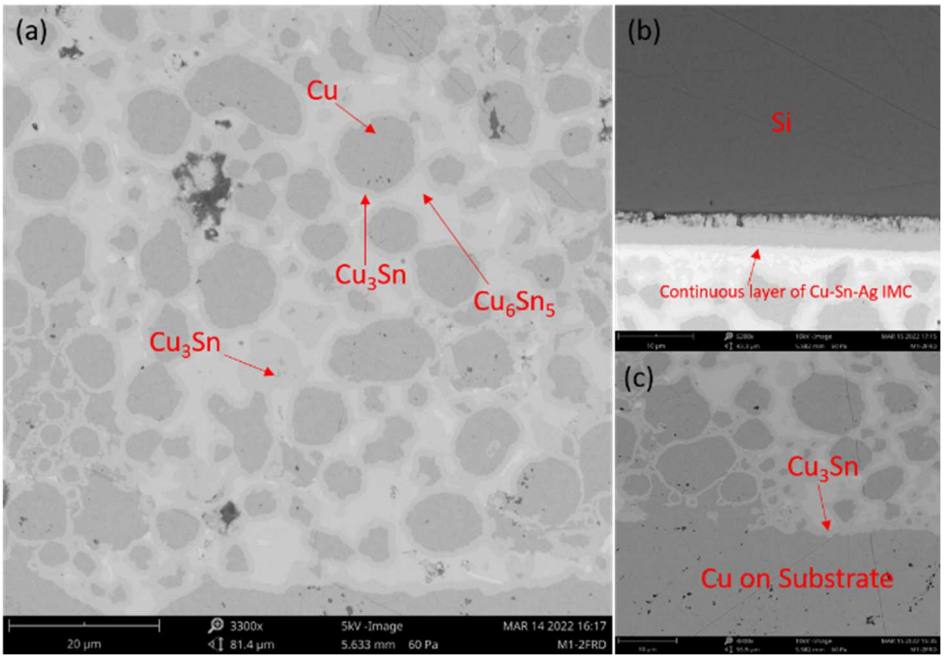


Fig. 3: SEM-EDX analysis on: (a) TLP bond region, (b) the interface between Si and TLP bond, and (c) the interface between TLP bond and substrate.

Figure 4 shows an X-ray image of IGBTs and FRDs bonded on a DBC substrate which has been soldered by the Run1 process. The maximum percentage of voids was observed in a large die area (IGBT) and measured at about 7%. At least three samples were prepared in each reflow process, and the results found the process is repeatable with low voids.

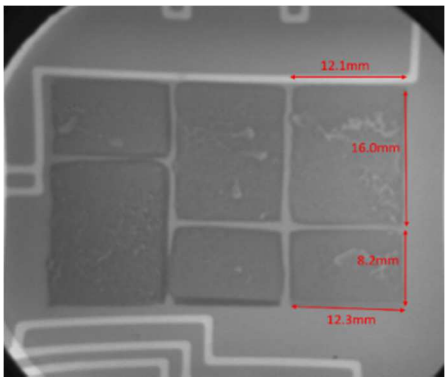


Fig. 4: X-ray image of TLP large area dies (IGBTs and FRDs) attached by Run 1 process.

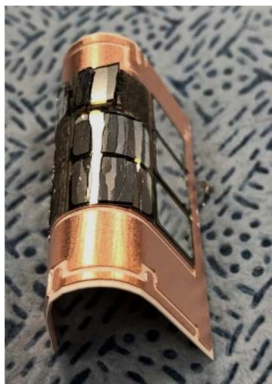


Fig. 5: A typical bend test using a 13mm mandrel diameter for a large area die size.

3.3. Bend Test

Quantitate bend test was carried out for large die samples. The TLP die bond adhesion was also examined with the aid of the mandrel bend test. Here mandrel diameter used was 13mm for introducing a higher bend. Figure 5 shows a typical bend test result where die cracks occur due to cohesive failure indicating good adhesion of die bonding.

3.4. Reliability Tests

A total of 1000 cycles with ΔT=215ºC thermal shock test was carried out. SAM scan analysis showed (as shown in Figure 6) there was no die TLP solder degradation or die cracks visible after the test

indicating the proposed TLP process is good life under high thermomechanical stress. The electrical functionality of the die-attach samples did not deteriorate after the 1000 cycles of the thermal shock test. Figure 7 shows static electrical functionality tests carried out in different cycles of thermal shock. The FRD dies to functional at the room temperature, and elevated temperature levels (125ºC and 150ºC) without a significant change of their I-V characteristic confirm the TLP die bonds could perform well at high-temperature operation. It is believed that the TLP process could also be implemented in high temperature power module packaging applications such as SiC.

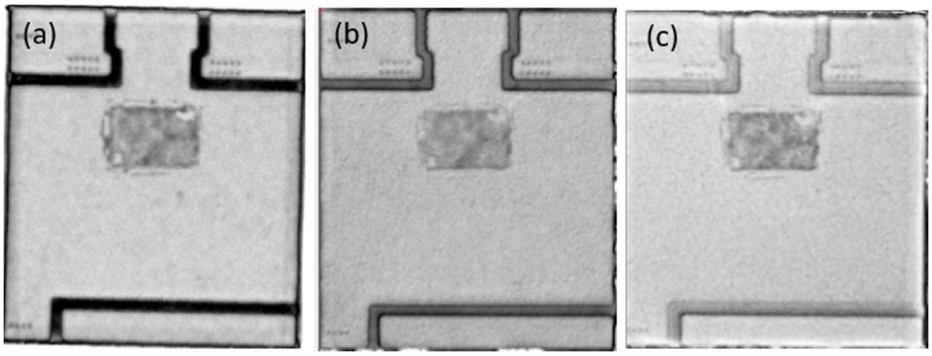
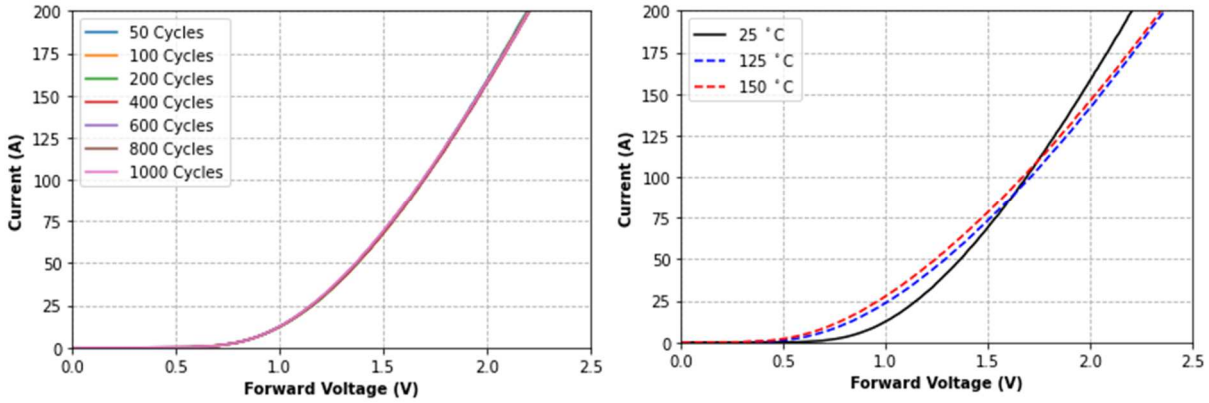


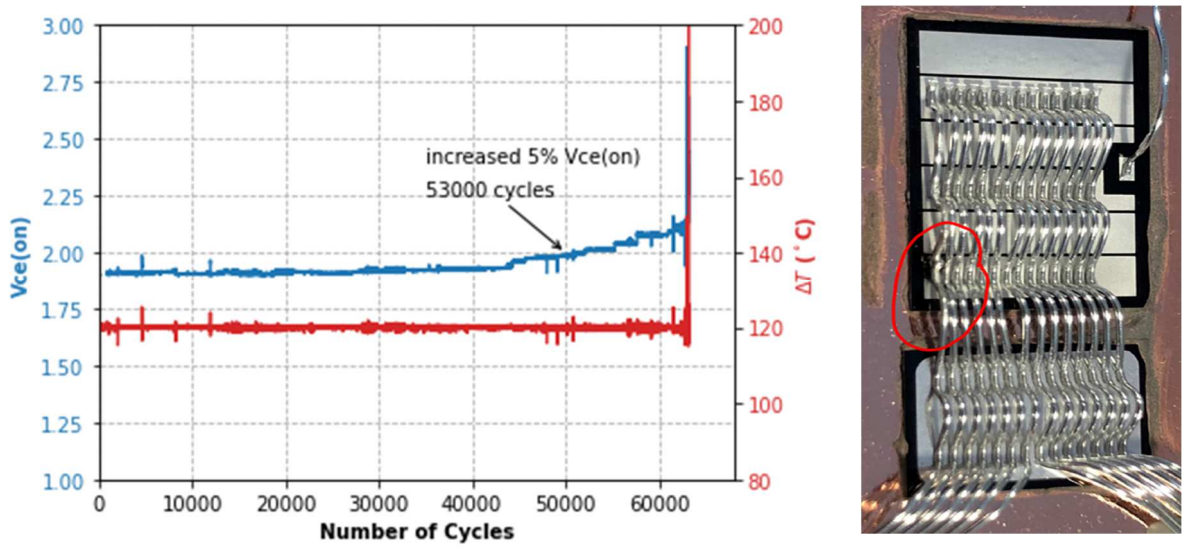
Fig. 6: SAM images: (a) Pre-thermal shock test, (b) after 600 cycles, and (c) after 1000 cycles.



(a) (b)

Fig. 7: Electrical test was done on FRDs: (a) comparing the I-V characteristics of FRD after thermal shock test with the number of different cycles, and (b) comparing the I-V characteristics of FRD electrical testing done at different temperature levels after 1000 cycles of thermal shock test.

Figure 8(a) shows the power cycling test results on IGBT, where the failure criteria was a 5% increase of Vce(on). A total of 53000 cycles were recorded at which the wirebonds started to deteriorate and lift off. An overshoot of Vec(on) was observed at around 63000 cycles due to die short-circuit, which was caused by the localized overheating on the surface of the chip after which wirebonds lift-off. Figure 8(b) also shows the wire bond lifted off confirmed by optical microscopy inspection. The wire bonds lift-off could have been caused by the degradation of the TLP solder material, which increased the thermal resistance. Figure 9 shows the structural function diagram (R_{th} vs. C_{th}) where an increase of the thermal resistance by the degradation of TLP die solder material after the power cycling test can be seen. Higher thermal resistance inside the TLP die solder area could increase the localized chip surface temperature and accelerate wirebond lift-off. Figure 9 shows the degradation of TLP solder material where thermal resistance increased after the power cycling test, confirming that the wire bond lifted off due to localized chip temperature increase.



(a) (b)

Fig. 8: (a) Number of cycles to failure with respect to increasing in Vce(on), and (b) Critical failure location of wire bonds during Power cycling test.

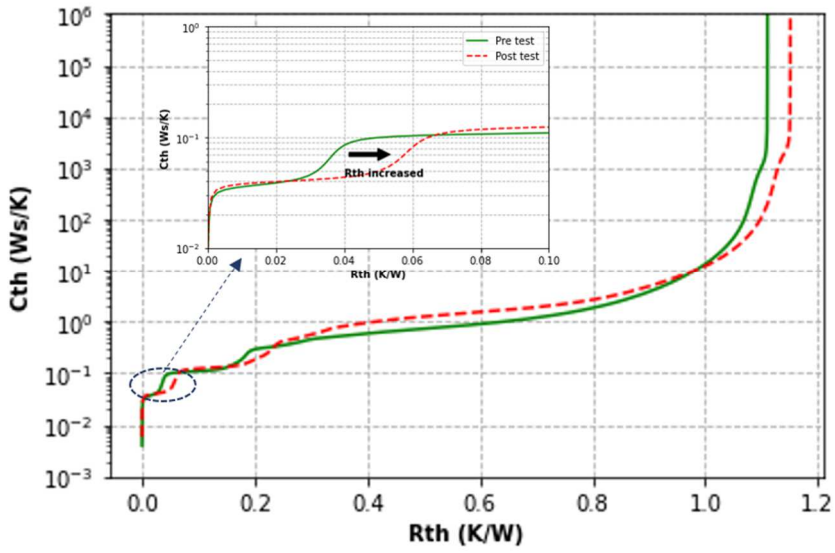


Fig. 9: Rth measurement of TLP soldered die sample using the structural diagram.

4. Conclusion

The TLP bonding for die-attach applications in power module packaging could replace the use of high Pb solder alloys and is a cost-effective solution over Cu/Ag sinter bonds. The TLP diffusion soldering process has been successfully optimized for large area die attach with a fully transformed high melting temperature intermetallic structures with a low percentage of soldered voids. The optimized TLP process improved the die shear strength to an average of 55 MPa, which helped to use SLID soldering of large size die on DBC substrate. The thermomechanical reliability and active power cycling tests confirmed that TLP diffusion soldering for large area die attach can apply to high temperature power module packaging applications.

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