PCB Technology Comparison Enabling a 900V SiC MOSFET Half Bridge Design for Automotive Traction Inverters

Matthias Spieler[1], Che-Wei Chang[1], Ayman EL-Refaie[2],
Muhammad H Alvi[3], Dong Dong[1], Rolando Burgos[1]

[1]Center for Power Electronics Systems
Virginia Tech
1185 Perry St, Blacksburg, VA 24061
United States
mspieler@vt.edu

[2]Opus College of Engineering
Marquette University
1637 W. Wisconsin Ave, Milwaukee, WI 53233
United States
ayman.el-refaie@marquette.edu

[3]General Motors Research & Development
30565 William Durant Blvd. Warren, Michigan 48092-2031
United States
muhammad.alvi@gm.com

Acknowledgments

This material is based upon work supported by the U.S. Department of Energy's Office of Energy Efficiency and Renewable Energy (EERE) under the Advanced Vehicle Technologies Office Award Number DE-EE0009190.

Keywords

≪Silicon Carbide (SiC)≫, ≪Electric Vehicle≫, ≪Traction application≫, ≪Inverter design≫, ≪Parasitic inductance≫

Abstract

The design of automotive traction inverters for an 800 V dc-bus typically utilize 1.2 kV silicon carbide (SiC) metal oxide semiconductor field effect transistors (MOSFET). The 1.2 kV power devices allow for high overshoot voltages during switching transients but experience a high on-state resistance due to the die's thick drift layer region. This paper proposes the usage of 900 V SiC MOSFETs for 800 V automotive traction inverter applications. The proposed half-bridge design combines discrete power semiconductors and the dc-link capacitor on one printed circuit board (PCB). This design approach enables a small current commutation loop and thus a small overshoot voltage. Three different PCB technologies are compared based on their suitability for the traction inverter application. An 800 V half-bridge prototype is designed, simulated, and tested. Measurement results are provided and show an overshoot voltage of 49.6 V at a switching speed of 69 V/ns under maximum load conditions.

Introduction

The transition to electrified automobiles accelerates the push to greater power densities and efficiency targets. Thus, in academia and industry a shift towards higher dc-bus voltages of 800 V and the usage of high voltage SiC MOSFETs is observed [1–4]. SiC MOSFETs offer lower losses and faster switching speeds compared to insulated-gate bipolar transistors (IGBTs). The increase in dc-bus voltage reduces the current stress on the drive train while maintaining the power output constant. These changes help to increase the efficiency and power density [4]. The US Department of Energy defined a research and development road map for automotive traction inverter that pursue an inverter efficiency increase to more than 98%, and power densities exceeding 100 kW/l by 2025 [5].

One step towards achieving the efficiency and power density goals is the transition from 1.2 kV SiC MOSFETs to 900 V SiC MOSFETs. The lower breakdown voltage allows for a thinner die epitaxial layer and thus reduces the MOSFET's on-state resistance [6]. As the dc-bus voltage can reach 850 V under normal operating conditions [2], special attention needs to be paid on a low inductance current commutation loop design to minimize the drain-source overshoot voltage during switching transients.

Many studies focus on reducing the current commutation loop stray inductance [7–14]. These studies can be generally divided into stray inductance reduction achieved by: 1) dc-link capacitor selection, 2) laminated busbars, 3) the placement of decoupling capacitors, 4) and low inductance power module integration.

Moorthy et al. [15] described the usage of a PCB as the dc-busbar for an automotive traction inverter. Their design connects the dc-link capacitors, power modules, and adjacent decoupling capacitors through the PCB. This results in a low current commutation loop stray inductance of 7.56 nH. Their inverter has an overshoot voltage of 163 V at a drain current of 440 A. Although no information on the di/dt is provided, it is unlikely that the stray inductance reduction resulting from the sole usage of a heavy copper PCB as a dc-busbar is sufficient to enable the usage of 900 V devices. Yet, the technology shows promise and is adapted for our half-bridge module design.

The current commutation loop stray inductance previously mentioned originates largely from the high-power module layout. Thus, to shrink the stray inductance further, the traditional half-bridge packaging design needs to be rethought. Plenty of research investigated different power module designs, such as a vertical current commutation loop integration [7, 11], or reducing the commutation loop inductance by inductance cancellation [13]. Yet, the module's spacers and screw connections increase the overall stray inductance and cannot be omitted while using power modules. One approach to reduce the inductance is to use discrete devices instead of power modules for the inverter build-up. The authors in [16] opted for a discrete SiC MOSFET based 15 kW Matrix converter design with PCB embedded ceramic inlays for better heat transfer from junction to heatsink. By choosing this design, the authors were able to integrate a vertical current commutation loop design and thus reduce the overall current commutation loop stray inductance. Another promising approach is to embed SiC MOSFET dies directly into the PCB. Marczok et al. [17] designed a six phase 100 kW traction inverter using embedded dies and achieving a design with a current commutation loop stray inductance of 1.69 nH resulting in an approximate overshoot voltage of 50 V.

This paper investigates which PCB technology is most suitable for a 900 V SiC MOSFET integrated half-bridge design. By combining the dc-busbar, dc-link capacitor, and power stage into one PCB, the current commutation loop is minimized and thus enables the usage of 900 V SiC MOSFETs in traction inverter applications. In section one, a brief overview of the inverter structure is provided, explaining the its build-up and its impact on the overshoot voltage in detail. In section two, a high-level view of the 900 V device selection and the benefits of 900 V SiC MOSFETs over 1.2 kV FETs is presented. The FETs associated losses play a key role in the thermal requirements and current density requirements which the PCB technologies have to fulfill. Section four provides a detailed approach on the PCB technology selection based on thermal, dc-bus current stress criteria, and loop inductance criteria. Section five includes switching transient measurements. Lastly, conclusions are drawn on the efficacy of this study.

Traction inverter build-up

The usage of 900 V SiC MOSFETs implies challenging constraints on the inverter design. The fast turn-off switching transient can induce a high overshoot voltage, causing an increased voltage strain on the low side SiC MOSFET. The maximum drain-source voltage during switching transient can be expressed as follows:

$$V_{DS;max} = L_{stray,sum} \cdot \frac{di_D}{dt} + V_{DC}, \tag{1}$$

where $L_{stray,sum}$ is the pooled current commutation loop stray inductance, di_D/dt is the drain current slope during the turn-off switching transient, and V_{DC} is the applied dc-bus voltage. Fig. 1 depicts the general equivalent electric circuit for one phase leg and the prevalent stray inductances. The total current commutation loop stray inductance can be described as follows:

$$L_{stray,sum} = ESL + L_{busbar} + 2 \cdot (L_D + L_S), \tag{2}$$

where ESL is the dc-link capacitor's parasitic stray inductance, L_{busbar} is the busbar's intrinsic inductance, and L_D and L_S are the MOSFET package's intrinsic inductance.

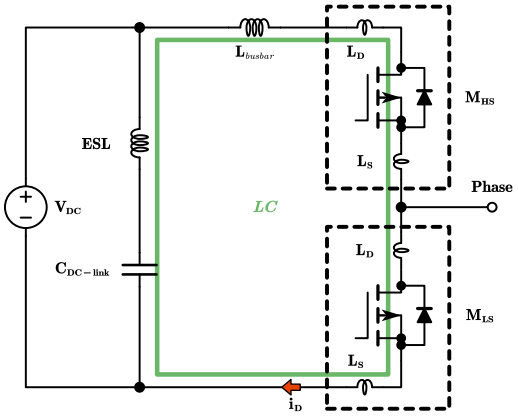


Fig. 1: Equivalent eclectic circuit of current commutation loop with intrinsic inductance of components.

The dc-bus voltage of an electric vehicle fluctuates under normal operating conditions between 650 V and 850 V depending on the battery package's state of charge [2]. This results in an overshoot voltage limit of maximum 50 V, if 900 V SiC FETs are used. As the switching time should be minimized to reduce the MOSFET's switching losses, a small current commutation loop stray inductance must be achieved. The inverter is designed for a switching transient voltage slope of less than 30 V/ns.

The proposed inverter design uses a heavy copper PCB as a base. The dc-link capacitor is directly soldered onto the PCB, a planar busbar can be achieved with multiple PCB layers, and discrete SiC MOSFETs are placed near the dc-link capacitor resulting in a small current commutation loop. Ceramic capacitors were chosen as the dc-link capacitor, as their parasitic inductance is smaller than the traditionally used film capacitors.

The discrete SiC MOSFET's package must be selected with care to reduce the intrinsic stray inductance. A current commutation loop implemented with the standard TO-247 package has a stray inductance of 8.18 nH [18]. Solely this induced stray inductance would result in an overshoot voltage exceeding the MOSFET's break down voltage. Thus, a through-hole mounted device package is not applicable for an 800 V dc-bus traction inverter with 900 V semiconductor devices. More suitable for the inverter application are SMD packages that create a current commutation loop stray inductance of 2.93 nH [18], or similarly the use of bare dies.

The device package constraints and dc-link capacitor design establish the PCB design boundaries. The PCB must combine the three following characteristics: 1) small current commutation loop stray inductance, 2) high thermal conductivity from junction to heatsink to allow reducing the number of paralleled SiC MOSFETs, 3) and an acceptable trace current density for the high current carrying PCB traces. To derive the cooling requirements, the device losses are simulated in the next section.

MOSFET selection consideration

PLECS simulations were conducted to compare losses of different SiC dies. Based on the simulation results, a conclusion can be made about the die type and die quantity needed for the phase leg. Criteria for the minimum number of parallel devices is dependent on the MOSFET's losses at a selected switching frequency. The PLECS simulation uses the switching loss and die's conduction loss to determine the overall MOSFET loss. It needs to be noted that this loss approximation neglects any reverse-recovery losses, input capacitance charge loss, and gate losses. A three-phase inverter with a discontinuous pulse width modulation control (DPWM) is simulated. The inverter's specifications are a nominal dc-bus

voltage V_{nom} of 800 V, maximum output power $P_{out;max}$ of 200 kW, a switching frequency f_{sw} within the range of 5 kHz to 50 kHz, and a die junction temperature T_j of 150 $°C$. The MOSFET's total loss is the sum of conduction and switching loss.

$$P_{tot} = P_{con} + P_{sw} \tag{3}$$

$$P_{con} = i_D^2 \cdot R_{DS;on} \tag{4}$$

$$P_{sw}(i_D) = [E_{sw;on}(i_D) + E_{sw;off}(i_D)] \cdot f_{sw} \tag{5}$$

Where i_D is the drain current, $R_{DS;on}$ is the MOSFET's on-state series resistance, $E_{sw;on}(i_D)$ and $E_{sw;off}(i_D)$ is the turn-on switching energy loss and turn-off switching energy loss respectively as stated in the datasheet as a function of the drain current. By increasing the number of paralleled MOSFETs per phase, the current stress per device is reduced. Thus, the conduction loss decreases. The switching losses per device decrease as the drain current per device is reduced. With increasing switching frequency, the switching loss increases approximately linearly.

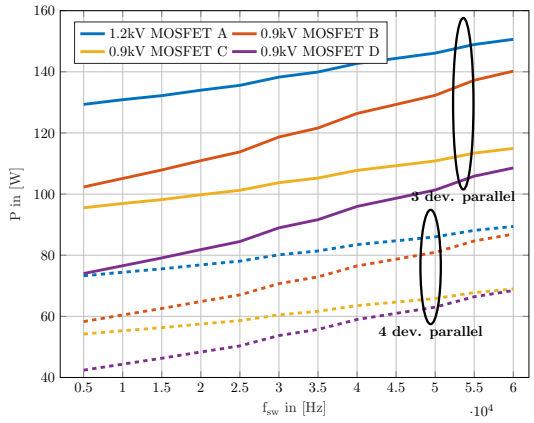


Fig. 2: PLECS simulation based MOSFET die loss for different MOSFETs as a function of switching frequency and number of paralleled devices.

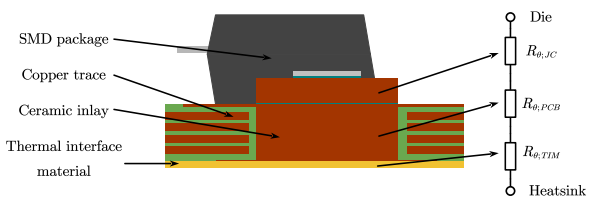
In total four devices were compared with respect to their total losses. Three devices have a breakdown voltage of 900 V, whereas one device has a breakdown voltage of 1.2 kV. Despite choosing a high efficiency 1.2 kV MOSFET, it is worth noting that 900 V devices lead to a significant reduction of losses highlighting the loss savings by using 900 V FETs instead of 1.2 kV FETs for automotive traction inverter applications.. Fig. 2 depicts the total MOSFET die loss at different switching frequencies, and different number of paralleled devices. MOSFET D has the lowest overall losses within the selected frequency range while paralleling three or four devices. MOSFET D is selected for the inverter build-up. The cooling requirements are derived based on MOSFET D's total losses at a switching frequency of 20 kHz.

PCB technology selection

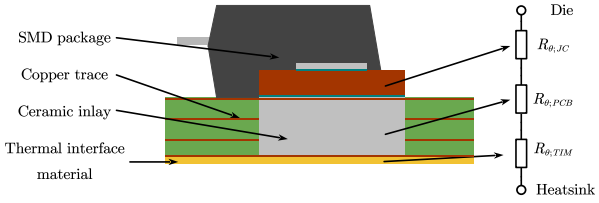
To enable the usage of 900 V devices the current commutation loop stray inductance has to be minimized. As the dc-busbar is integrated within the PCB, the layer cross-sectional area must be sufficient to achieve a current density of less than $5A/mm^2$ [19]. A PCB trace-width calculator is used to determine the minimum trace-width [20]. To ensure no PCB overheating due to trace losses, the thermal conductivity from the device junction to the coolant must be high enough to allow for sufficient cooling. A higher thermal conductivity enables fewer numbers of paralleled SiC MOSFETs and hence reduces the bill-of-material list and increases the power density. All three requirements must be fulfilled by the PCB technologies selected for closer comparison. The PCB technologies are compared based on analytical equations and finite-element simulations.

The three PCB technologies, 1) copper inlay PCB, 2) ceramic inlay PCB, and 3) embedded dies within the PCB were considered for this study. A cross section of the PCB technologies and their thermal resistance path are displayed in Fig. 3.

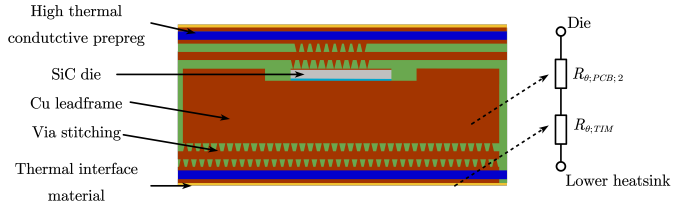
The copper inlay PCB is a heavy copper PCB with small copper coins press fitted into PCB cavities. The maximum diameter of the inlay is 8 mm. By placing the inlay beneath the SiC MOSFET SMD footprint a high thermal conductive path from the SMD package to the heatsink placed at the PCB bottom is created. The bottom side copper polygon has a footprint of 115 mm^2 to allow for better heat spreading



(a) Cross section of copper inlay PCB



(b) Cross section of ceramic inlay PCB



(c) Cross section of embedded die PCB

Fig. 3: PCB technology cross section with resulting thermal resistance path from junction to heatsink. The TIM material is highlighted in yellow. The isolating prepreg material is highlighted in blue.

and a larger thermal interface material area. Due to the manufacturing process, the bottom side is not electrically insulated from the MOSFET's drain pad. Thus, a non-conductive thermal interface material is required. A PCB with a maximum of 6 layers with an outer layer copper thickness of 70 μm and inner layer copper thickness of 500 μm can be manufactured. This allows for a low inductance design, with low trace losses. The copper inlay PCB cross section is displayed in Fig. 3a.

The operating principle of the ceramic inlay is similar to the copper inlay PCB. The inlay provides a high thermal conductive path for the heat transfer from the device junction to the heatsink. A PCB with $10x10\ mm^2$ ceramic inlays is considered for the inverter application. The ceramic inlay's advantage over the copper inlay is its electrical insulating properties. This enables the usage of a non-electrical insulating thermal interface material and thus increases the overall thermal conductivity. A detailed comparison is given in the following sub sections. The ceramic inlay PCB can be manufactured with a layer stack of four 70 μm copper layers. Due to the thin copper layers, it is expected that the dc-busbar current density is the highest of all three PCB technologies. Fig. 3b displays the cross section of a ceramic inlay PCB.

The embedded die technology enables the placement of bare SiC dies into the PCB. Fig. 3c shows the embedded die cross section. The lack of any SMD package omits the intrinsic package stray inductance. While die embedding allows for a compact trace design resulting in a low stray inductance, and a good thermal conductivity to the heatsink. The die is sintered onto a $11x11\ mm^2$ copper lead frame. The lead frame is then embedded into the PCB and electrically connected with buried vias. The bottom side prepreg material (highlighted in blue) electrically isolates the embedded inlay to the heatsink. Thus, a high thermal conductive and electrically non-insulating interface material can be used.

Thermal modeling

Equation based thermal resistance

The PCB design and technology must enable sufficient heat transfer from the power semiconductor to the heatsink. Although the cooling requirements are increased for fewer paralleled SiC-MOSFETs, a lower number of paralleled devices is preferred, as the power density is increased, and the system cost is reduced. Therefore a phase leg design with three devices in parallel at a switching frequency of 20 kHz is chosen. As depicted in Fig. 2, the simulated die loss is 82 W at the selected maximum load operating point. To handle the high-power loss, the thermal resistance between the MOSFET junction and the coolant must be small to keep the junction temperature at a predefined value. The general equation for

Table I: Calculated thermal resistances of each material used for the PCB layer stack up

Parameter	Copper	Ceramic	Embedded
$R_{\theta,j-c}$ in $^{\circ}C/W$	0.31	0.31	0
$R_{\theta,PCB}$ in $^{\circ}C/W$	0.13	0.06	0.177
$R_{\theta,TIM}$ in $^{\circ}C/W$	0.66	0.057	0.057
$R_{\theta,tot}$ in $^{\circ}C/W$	1.1	0.427	0.234

the total thermal resistance is given below.

$$R_{\theta;tot} = \frac{T_{j;FET} - T_{coolant}}{P_{FET}}, \tag{6}$$

where $T_{j;FET}$ is the MOSFET junction temperature, $T_{coolant}$ is the coolant temperature, and P_{FET} is the discrete MOSFET total loss. The predefined maximum junction temperature is set to 150 $^{\circ}C$. The coolant temperature is set to constant 70 $^{\circ}C$ resulting in a maximum thermal resistance for MOSFET D of 0.98 $^{\circ}C/W$ if the devices are switched at 20 kHz.

The previously mentioned PCB technologies need to fulfill the requirement of a junction-to-heatsink thermal resistance not greater than 0.58 $^{\circ}C/W$ under the assumption that the heatsink's thermal resistance is not greater than 0.4 $^{\circ}C/W$ per MOSFET. If a PCB technology doesn't meet the thermal requirements, it will not be considered further for the inverter application.

First, the thermal resistance is derived based on analytical equations. If the analytical based thermal resistance does not fulfill the requirement, the PCB technology is no longer considered. All PCB technologies with an analytical based thermal resistance lower than given maximum thermal resistance will be simulated in ANSYS Icepak. This step is necessary, as the analytical based thermal resistance tends to be lower than the actual thermal resistance, due to the assumed equal heat spreading within the thermal path stack up.

The junction-to-heatsink thermal resistance $R_{\theta;j-h}$ is the sum of thermal resistances introduced by each material within the heat transfer path. The thermal resistance paths for each PCB layout are shown in Fig. 3. Each material thermal resistance is calculated based on the following equation:

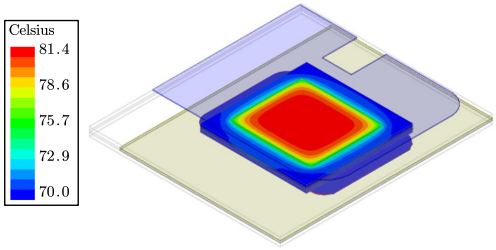
$$R_{\theta} = \frac{\delta x}{A \cdot K}, \tag{7}$$

where δx represents the material thickness, A is the material area, and K equals the material's specific thermal conductivity. The two thermal interface materials Thermflow T777 Material from Parker and TM-TIFX200 from Futura Italia are used for the PCB comparison [21, 22]. The resulting thermal resistances for each material in the junction to heatsink thermal path are listed in Table I.

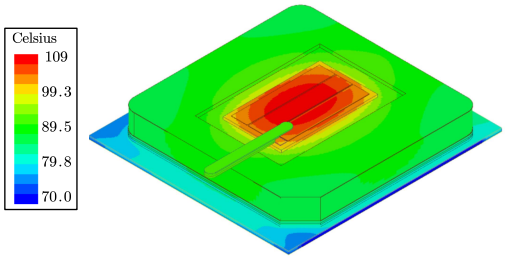
The copper inlay PCB junction-to-heatsink thermal resistance is 1.1 $^{\circ}C/W$. Largest contributor to the thermal resistance is the thermal interface material which electrically isolates the heatsink from the PCB bottom. The high total thermal resistance does not allow for sufficient cooling if only three SiC-MOSFETs are paralleled. Thus, the copper inlay PCB technology is not applicable for a high-power density traction inverter with 900 V SiC devices.

The ceramic inlay PCB has the advantage of an electric isolating inlay over the copper inlay PCB technology. Thus, allowing the usage of an electric conducing thermal interface material. This results in a junction-case thermal resistance of 0.427 $^{\circ}C/W$. As the thermal resistance fulfills the requirement, the thermal heat path will be simulated in the following subsection.

By embedding the die into the PCB, the SMD package is removed from the heat transfer path resulting in a smaller total thermal resistance. The die is sintered to a copper lead frame which is connected to the below layers through via stitching. The electric isolation is achieved via a high thermal conductive



(a) Ceramic inlay PCB ANSYS ICEPAK simulation. The temperature ranges from blue 70 $°C$ to red 81.43 $°C$.



(b) Embedded die PCB ANSYS ICEPAK simulation. The temperature ranges from blue 70 $°C$ to red 109.03 $°C$.

Fig. 4: Simulated die temperature for the ceramic inlay PCB design and double-sided-cooling embedded die PCB design.

prepreg layer without any vias. This results in an analytical-based junction-to-heatsink thermal resistance of 0.234 $°C/W$. The combined embedded PCB thermal resistance is below 0.5 $°C/W$. Thus, the thermal resistance will be investigated closer in the following subsection

Simulation based thermal resistance

To evaluate the thermal behaviour of the ceramic inlay PCB and the embedded die PCB technology, ANSYS Icepak simulations are conducted. The PCB and its layer stack up are designed in Altium designer and exported to ANSYS Icepak.

To further evaluate the PCB thermal resistance, the die temperature or the SMD footprint were assigned with a power loss of 82 W and the PCB's bottom side copper layer is set to a constant temperature of 70 $°C$. The thermal interface material's impact on the junction-to-heatsink thermal resistance is added post simulation. The via stitching is approximated by changing the area specific prepreg material's thermal conductivity to the combined averaged thermal conductivity value of the buried vias and the FR4. The temperature of the die or the SMD footprint is simulated, and its temperature is used to calculate the thermal resistance based on eq. 6. The simulation results are depicted in Fig. 4a and Fig. 4b.

The finite element simulations based thermal resistance for the ceramic inlay PCB stack up and embedded die PCB are 0.44 $°C/W$ and 0.45 $°C/W$ respectively. Both thermal resistances are below the set maximum. Thus, both PCB technologies are considered for further trace resistance analysis.

Trace loss modeling

The dc-busbar is integrated into the PCB. The thinner PCB layers increase the overall conduction loss compared to an external thick copper busbar. Therefore, it is essential to investigate the trace losses created by the PCB design. Too high losses increase the trace temperature. The trace-width must be sufficient to limit the PCB's temperature increase to 25 $°C$. Allocco states that a good rule of thumb is to limit the current density to 5 A/mm^2 for passively cooled busbar designs [19]. Additionally, the designed PCB dc-bus trace-width is compared to the minimum trace-width derived by an online trace-width calculator based on the IPC-2221 standard [20].

The ceramic capacitors are soldered to the top and bottom of the PCB with the dc-busbar connecting all components. The capacitor footprint is adapted for a low impedance design. Through-hole vias connect the PCB layers. The required clearance between the high voltage potentials, defined by the standard IPC-2221B [23], creates the layer layout of one half-bridge dc-link capacitor as shown in Fig. 5.

The high current traces narrow down to 2.4 mm in areas with the through hole vias. It is expected to have the highest current density in these areas. To analyze the current density, finite element analysis were conducted. The trace design is exported to ANSYS Icepak and the current flow path is defined. As the trace layout of $dc+$ and $dc-$ traces are similar, only the $DC+$ trace current density is simulated. The $dc+$

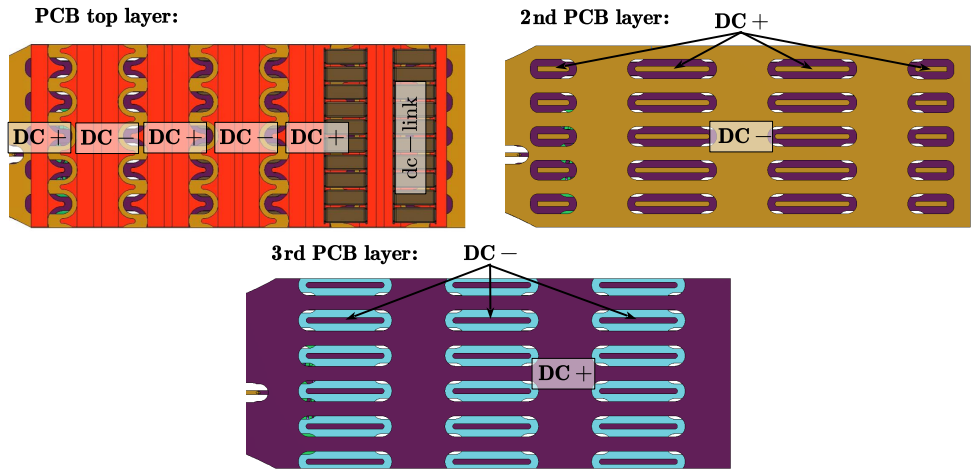
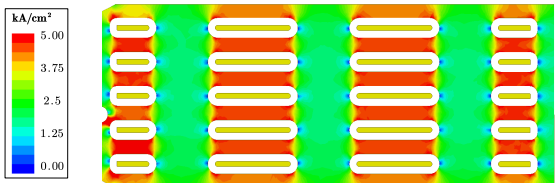
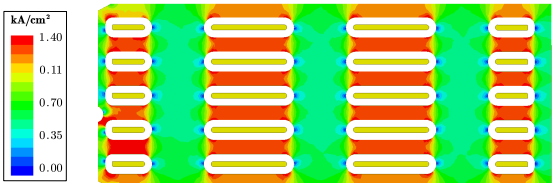


Fig. 5: Top view of layer stack up of first three half-bridge PCB layers. Layer layout of layer two and three alternate for all following four layers



(a) ANSYS Q3D current density analysis for ceramic inlay PCB. The maximum current density is 5 kA/cm^2.



(b) ANSYS Q3D current density analysis for embedded die PCB. The maximum current density is 1.4 kA/cm^2.

Fig. 6: Equivalent electric circuit diagram and simulated die losses of 1.2 kV MOSFET and 900 V MOSFETs

trace-width is 14.7 mm. To minimize simulation time, the busbar of one half-bridge was simulated. The average current stress is derived from the PLECS simulations conducted in Section 2 and is set to 134 A per phase. If three half-bridges are paralleled per phase, the current stress per half-bridge is 44.67 A.

Current density simulation

As previously mentioned the ceramic inlay PCB has four layers with a layer thickness of 70 μm. The top and bottom layers are used to mount the dc-link capacitors restricting the high current flow to the two inner layers. This results in a simulated current density of up to 43.3 A/mm^2 as shown in Fig. 6a. Additionally, the design does not meet the minimum trace-width derived using the trace-width calculator. Hence, the high dc-bus current density of the ceramic PCB technology is not suitable for the inverter application in question.

The eight-layer PCB used for the embedded PCB design has a combined trace thickness of 255 μm for each dc-trace. The current density is reduced to a maximum of 11 A/mm^2, which is above the recommended 5 A/mm^2. Yet, the total dc-bus trace-width of 14.7 mm per half bridge is greater than the PCB trace-width calculator's minimum trace-width limit of 11.7 mm [20]. Future research will include testing the dc-busbar heating to investigate these two contradicting results. Accordingly, the embedded PCB technology is further analyzed.

Current commutation loop stray inductance

The eight-layer PCB used for the embedded build-up allows for a vertical current commutation loop integration. The vertical integration achieves good mutual inductance cancellation resulting in a small current commutation loop stray inductance. The loop design is depicted in Fig. 7. The $dc+$ trace is routed on the third layer and is connected with vias to the high-side lead frame and subsequently to the drain pad. The AC trace is also routed on the third layer connecting the high-side die source pad with the low-side MOSFET drain. The $dc-$ trace is routed from the low-side die source pad on the second

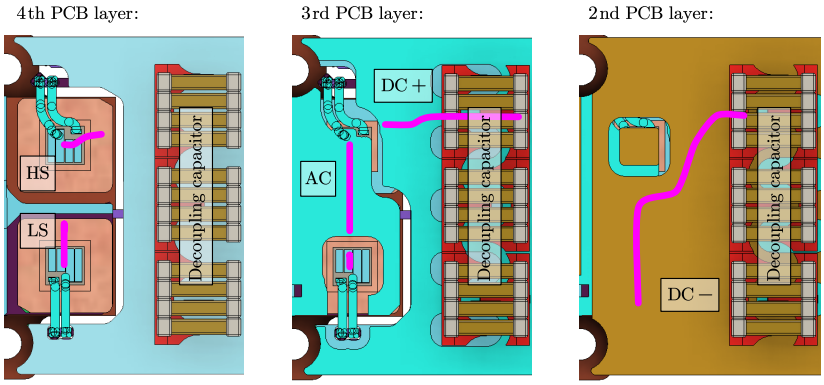
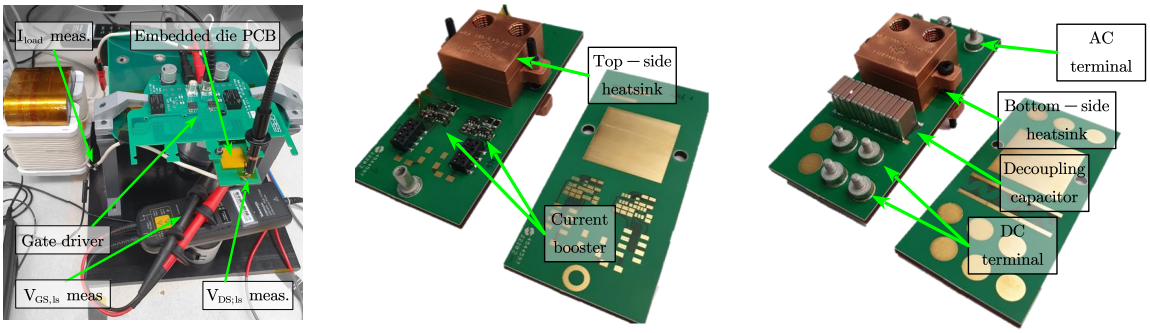


Fig. 7: Current commutation loop design. The current path is highlighted by the pink line on each PCB layer. The abbreviations describe the trace potential.



(a) Double pulse test setup for testing one embedded die half-bridge PCB

(b) Embedded die top side view. The embedded die half-bridge is located beneath the heatsink pad.

(c) Embedded die bottom side view. The embedded die half-bridge is located beneath the heatsink pad.

Fig. 8: Double-pulse setup and turn-off switching transient

PCB layer back to the dc-link capacitor. A cut-out on the second layer above the high side MOSFET allows for a better high thermal conductivity path from the die to a top side heatsink. Future work will show the thermal performance of a double-sided-cooling embedded die PCB design. The PCB design is analyzed in ANSYS Q3D at a frequency of 10 MHz. The design current commutation loop inductance and increase in drain-source capacitance for the high-side and low-side MOSFET are 744 pH, 32.9 pF, and 59.01 pF respectively. To analyze the MOSFET's overshoot voltage during switching transients, double pulse tests are carried out in the next section.

Embedded die PCB double pulse measurement

To evaluate the embedded die half-bridge PCB, a prototype was manufactured. As a safety measure, a SiC MOSFET with a breakdown voltage of 1.2 kV was used instead of a 900 V SiC MOSFET. Also, a modular phase design was chosen to allow for easy replacement of defective half-bridges. The embedded die PCB is shown in Fig. 8b and Fig. 8c. The half-bridge prototype assembly is depicted in Fig. 8a. The following measurement probes were used: passive high voltage probe (TPP0850) for measuring the MOSFET drain-source voltage, two differential probes (THDP0200) to measure the dc-bus voltage and the low-side gate signal, and one Rogowski coil (CWTUM/3/B) to measure the load inductor current.

The double pulse tests were conducted at a dc-bus voltage of 855 V, a drain current of 142 A per half-bridge, and a switching transient speed of 69 V/ns. Due to the lack of a current measurement method with minimal impact on the current commutation loop stray inductance, the switching transient current cannot be measured. Thus, the overshoot voltage is evaluated based on the turn-off voltage switching transient and the drain current. Fig. 9 depicts the turn off switching transient. The resonant frequency between the MOSFET input capacitance and the current commutation loop stray inductance is 273 MHz. The

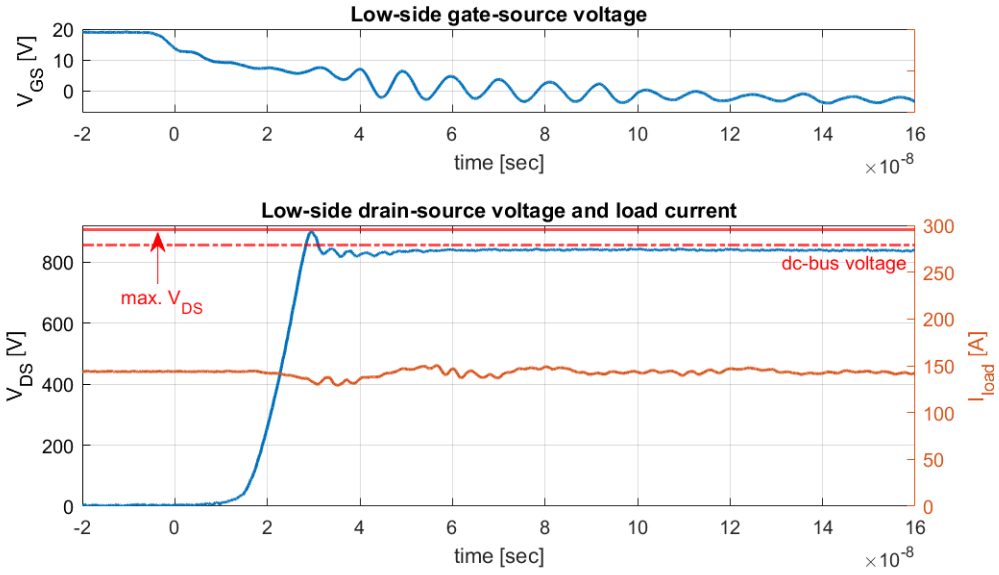


Fig. 9: Experimental test results of low side MOSFET's drain-source voltage during turn-off switching transient at $V_{DS} = 855\ V$, $I_{load} = 142\ A$, $dv/dt = 69.9 V/ns$. The maximum drain-source voltage peak is 904.6 V.

overshoot voltage reaches 49.6 V indicating that the embedded die PCB design is capable of operating at a dc-bus voltage of 850 V, a turn-off voltage transient speed of 69 V/ns, and a drain current of 142 A without reaching the breakdown voltage of a 900 V SiC MOSFET.

Conclusions

A comprehensive PCB technology comparison enabling 900 V SiC MOSFETs for automotive traction inverter applications with a dc-bus voltage of 800 V was presented in this work. The copper inlay PCB technology, ceramic inlay PCB technology, and embedded die PCB technology were compared in terms of the PCB's thermal conductivity, the dc-bus current stress, and the overshoot voltage during switching transients. The copper inlay PCB technology was shown to have an insufficient thermal conductivity form junction-to-heatsink due to the electrically isolated thermal interface material. The ceramic inlay on the other hand led to thin copper traces making it unsuitable for the inverter application, as the dc-bus current density exceeds the recommended of 5 A/mm^2. The embedded die PCB technology also had a current density above the threshold value, but it exceeded the minimum trace-width derived by the trace-width calculator used. Lastly, the switching transient overshoot voltage caused by the current commutation loop stray inductance was evaluated, where the measurements conducted showed a maximum drain-source overshoot voltage of 49.6 V, at a switching speed of 60 V/ns, and a drain current per die of 142 A for the embedded die PCB technology. The embedded die technology consequently showed to be a viable alternative for the use of 900 V SiC MOSFET devices in for automotive traction inverter applications with nominal dc-bus voltages of 800 V.

Future work will include testing multiple paralleled embedded die PCB half-bridges as well as analyzing the thermal resistance based on the standard JEDEC JESD51-14 [24], and conducting continuous maximum load tests to investigate the dc-busbar heating.

References

[1] M. Su, C. Chen, S. Sharma, and J. Kikuchi, "Performance and cost considerations for sic-based hev traction inverter systems," in *2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Conference Proceedings, pp. 347–350.

[2] C. Jung, "Power up with 800-v systems: The benefits of upgrading voltage power for battery-electric passenger vehicles," *IEEE Electrification Magazine*, vol. 5, no. 1, pp. 53–58, 2017.

[3] W. Taha, B. Nahid-Mobarakeh, and J. Bauman, "Efficiency evaluation of 2l and 3l sic-based traction inverters for 400v and 800v electric vehicle powertrains," in *2021 IEEE Transportation Electrification Conference Expo (ITEC)*, Conference Proceedings, pp. 625–632.
[4] J. Zhu, H. Kim, H. Chen, R. Erickson, and D. Maksimović, "High efficiency sic traction inverter for electric vehicle applications," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Conference Proceedings, pp. 1428–1433.
[5] U. D. Partnership, "Electrical and electronics technical team roadmap," p. https://bit.ly/3o1egLl, 2017.
[6] R. W. Erickson and D. Maksimovic, *Fundamentals of power electronics*. Springer Science Business Media, 2007.
[7] C. Marczok, E. Hoene, T. Thomas, A. Meyer, and K. Schmidt, "Low inductive sic mold module with direct cooling," in *PCIM Europe 2019; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, Conference Proceedings, pp. 1–6.
[8] F. Hou, W. Wang, R. Ma, Y. Li, Z. Han, M. Su, J. Li, Z. Yu, Y. Song, Q. Wang, M. Chen, L. Cao, G. Zhang, and B. Ferreira, "Fan-out panel-level pcb-embedded sic power mosfets packaging," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 1, pp. 367–380, 2020.
[9] D. J. Kearney, S. Kicin, E. Bianda, and A. Krivda, "Pcb embedded semiconductors for low-voltage power electronic applications," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 7, no. 3, pp. 387–395, 2017.
[10] A. Tablati, N. Alayli, T. Youssef, O. Belnoue, L. Theolier, and E. Woirgard, "New power module concept in pcb-embedded technology with silver sintering die attach," *Microelectronics Reliability*, vol. 114, p. 113891, 2020. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0026271420305102
[11] L. Zhang, P. Liu, A. Q. Huang, S. Guo, and R. Yu, "An improved sic mosfet-gate driver integrated power module with ultra low stray inductances," in *2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Conference Proceedings, pp. 342–345.
[12] G. Regnat, P. O. Jeannin, J. Ewanchuk, D. Frey, S. Mollov, and J. P. Ferrieux, "Optimized power modules for silicon carbide mosfet," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Conference Proceedings, pp. 1–8.
[13] K. Takao and S. Kyogoku, "Ultra low inductance power module for fast switching sic power devices," in *2015 IEEE 27th International Symposium on Power Semiconductor Devices IC's (ISPSD)*, Conference Proceedings, pp. 313–316.
[14] J. Schnack, J. P. Goerdes, S. Stahl, U. Schuemann, R. Mallwitz, and H. P. Tiedemann, "Design of bypass network for fast switching inverters using an innovative hybrid dc-link," in *2021 IEEE 15th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG)*, Conference Proceedings, pp. 1–8.
[15] R. S. K. Moorthy, B. Aberg, M. Olimmah, L. Yang, D. Rahman, A. N. Lemmon, W. Yu, and I. Husain, "Estimation, minimization, and validation of commutation loop inductance for a 135-kw sic ev traction inverter," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 1, pp. 286–297, 2020.
[16] V. Baker, B. Fan, R. Burgos, V. Blasko, and W. Chen, "3d commutation-loop design methodology for a silicon-carbide based 15 kw, 380:480 v matrix converter with pcb aluminum nitride cooling inlay," in *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, Conference Proceedings, pp. 233–238.
[17] C. Marczok, M. Martina, M. Laumen, S. Richter, A. Birkhold, B. Flieger, O. Wendt, and T. Paesler, "Sic-modul - modular high-temperature sic power electronics for fail-safe power control in electrical drive engineering," in *CIPS 2020; 11th International Conference on Integrated Power Electronics Systems*, Conference Proceedings, pp. 1–6.
[18] F. Denk, K. Haehre, S. Eizaguirre Cabrera, C. Simon, M. Heidinger, R. Kling, and W. Heering, "Rds(on) vs. inductance: comparison of sic mosfets in 7pin d2pak and 4pin to-247 and their benefits for high-power mhz inverters," *IET Power Electronics*, vol. 12, no. 6, pp. 1349–1356, 2019, https://doi.org/10.1049/iet-pel.2018.5838. [Online]. Available: https://doi.org/10.1049/iet-pel.2018.5838
[19] J. M. Allocco, "Laminated bus bars for power system interconnects," in *Proceedings of APEC 97 - Applied Power Electronics Conference*, vol. 2, Conference Proceedings, pp. 585–589 vol.2.
[20] A. Circuits, "Pcb trace width calculator." [Online]. Available: https://www.4pcb.com/trace-width-calculator.html
[21] P. Chomerics, "Thermflow® non-silicone, phase-change thermal interface pads." [Online]. Available: prker.co/3xJCugk
[22] F. Italia, "Thermal interface materials," 2017. [Online]. Available: https://bit.ly/futura-italia
[23] "Generic standard on printed board design," 2012. [Online]. Available: https://bit.ly/IPC-2221B
[24] "Transient dual interface test method for the measurement of the thermal resistance junction-to-case of semiconductor devices with heat flow through a single path," 2010. [Online]. Available: https://bit.ly/jedec-standard