Investigation about Operation and Performance of Gate Drivers for Power Electronics Converters for Cryogenic Temperatures

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Acknowledgements

The authors would like to acknowledge the financial support lended by NASA to carry out this research under ULI: Development of the Cryogenic Hydrogen-Energy Electric Transport Aircraft (CHEETA) Design Concept under award number 80NSSC19M0125. Furthermore, NSF CAREER award numbered 1846917 titled Semiconductor-Based EMI Mitigation Architecture for Future Power Electronics Systems is also acknowledged.

Keywords

«Cryogenic», «Smart Gate Drivers», «More Electric-Aircraft»

Abstract

Utilization of power electronics converters under cryogenic temperatures (CT) offers higher power efficiency and volumetric density. This becomes possible due to reduced channel resistance and switching energies for Si and GaN-based devices. Therefore, both quantities, constituting a figure of merit for power converters; offer lower conduction losses and increased switching speeds with the reduction in temperatures. This leads to increased power efficiency, and lower volume of the passive components involved. Since reliable and efficient operation of a power electronics converter depends upon the operational characteristics of switching devices; gate drivers play a critical role as they not only decide, but also help optimize the operating conditions of such devices. To take full advantage of CT, not only proper working but also the quality of switching performance of gate driving circuits is extremely important. This paper presents operation and performance of numerous commercially off-the-shelf (COTS) gate drivers under cryogenic operating conditions. Gate drivers (GD) selected for the analysis are capable enough to drive high-speed wide band gap (WBG) devices. As part of the experimentation process, whole GD board was designed while selecting all the auxiliary components to be compatible with CT. The paper compares five different GDs and presents successful operation of two of them at CT of 77 K.

Introduction

Power electronics is the key enabling technology for electromechanical drives, transportation, renewable energy systems, and power grids. Cryogenic power electronics technology (CPET) is the next step to obtain higher power efficiency, higher power density, and superior performance for various applications. CPET finds its applications in deep space and terrestrial applications, medical diagnostics, all-electric vehicles, propulsion motors, and superconducting magnetic energy storage systems [1]. Utilization of cryogenically cooled environment offers opportunity to design and manufacture lightweight, and highly efficient power electronics converters. Such cryogenic power conversion systems offer significant improvements in performance, including the reduction in semiconductor losses, higher switching speed, and performances [2].

Power converters are majorly composed of three components as shown in Fig. 1 (a): semiconductor devices, cooling materials, and passive components [3]. These components dictate the efficiency and power density of the overall conversion system, and therefore their appropriate selection is important to ensure high density and efficiency. A framework to select and optimize a converter together with its components is provided in [4]. Considering the operation of converters at low temperatures, numerous literatures have characterized the performance of different passive components for low-temperature applications [5]. Similarly, performance of different semiconductor devices, such as Si MOSFETs and GaN high electron mobility transistors (HEMT), has been reported to improve with reduction in temperature [6].

Although appropriate devices for low temperatures have been identified and their static characterization performed, yet dynamic characterization and full converter development at lower temperatures has not been reported. [6] reports the dynamic characterization of a 650 V GaN until 133 K whereas [7] reports dynamic characterization until 93 K. Similarly, some of the converters developed recently include a three-level active neutral point clamped converter (3L-ANPC) with series cascading of Si devices [8]. Development of a single-phase three-level flying capacitor multi-level inverter using 200 V GaN devices was reported until 133 K in [9]. From the literature, it can be observed that development of power electronics converters with high voltage GaN (> 600 V) devices is not reported at cryogenic temperatures. The reason for this may be attributed to non-availability of gate driving and auxiliary components at such low temperatures. Gate driver (GD) circuitry is used to drive the semiconductor devices as depicted in Fig. 1 (b), and comprise of an isolated auxiliary power supply, integrated circuits (ICs) and passive components. GDs are extremely crucial for the optimized performance of semiconductor switches as both the conduction and switching losses are related to the magnitude and nature of gate driving voltages. Although efforts have been made to successfully operate such components at low temperatures as reported in [10], however not even a single successful operation at a temperature as low as 77 K is reported.

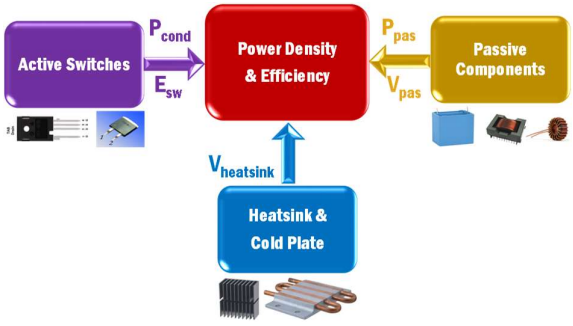


Fig. 1: (a) Building block of a power electronics converter

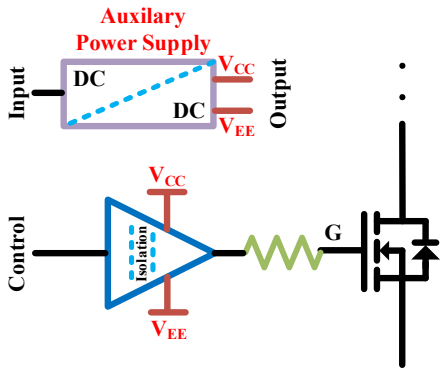


Fig. 1: (b) Basic GD schematics

Keeping in view the significance of gate driving components for CPET, this paper focuses on analyzing the performance of numerous commercially available gate drivers at cryogenic temperatures (CT). Section two of the paper discusses selection of gate driver and its associated components suitable for CT, whereas third section presents development of hardware and setting up of a cryogenic chamber. Discussion on experimentation and results of gate drivers at liquid nitrogen temperature (LNT), i.e., 77 K is carried out in the second last section. The paper concludes afterward.

Selection of Gate Driver and Associated Components

Considering the advantages associated with low-temperature operation of semiconductor devices; both gate drivers and switching devices should preferably be placed together and inside a cold environment [12]. This will not only make the connections short and compact but will also offer noise immune and faster dynamic performances, as [13] placed both the gate driver and power circuitry inside the chamber while using Si devices for a DC-DC converter. To have the whole gate driving circuitry function

properly at low temperatures, all the constituent components, for example, ICs and passive components must be carefully selected and designed.

Gate Driver Integrated Circuit (IC)

Selection of gate driver is critical as it drives the gate-source of any transistor and makes or breaks its channel to establish the current. Keeping in view the faster turn-on and turn-off together with lower operating temperatures, the gate driver ICs should not only ensure higher sourcing/sinking of gate current, but also need to have complementary metal-oxide semiconductor (CMOS) technology. CMOS-based integrated circuits are preferred over other types because of their improved performance in switching speed with reduction in temperature. On the contrary, other technologies, for example, bipolar junction transistor (BJT) suffers from a significant decrease in current gain caused by the reduction in carrier lifetime at reduced temperatures [12], [14]-[15].

To evaluate the performance of GDs, numerous commercially off-the-shelf (COTS) drivers capable enough to drive GaN devices were selected; since these devices offer reduced conduction losses, improved switching performance, and constant breakdown voltage [2]. Combined with CMOS technology and availability in the market, GD must also offer extremely low isolation barrier capacitance, higher common-mode transient immunity (CMTI), and higher current sourcing/sinking capability. Therefore, a thorough survey was conducted, and a brief comparison of key parameters for candidate GD is provided in Table I.

Table I: Key Parameters for Candidate Gate Drivers

PROPERTY	SI8271	SI8235AD	UCC21540A	MAX22702	ADUM4221
CMTI	200 V/ns	45 V/ns	100 V/ns	300 V/ns	150 V/ns
C_{IO}	0.5 pF	1.4 pF	1.2 pF	1 pF	2.2 pF
PEAK CURRENT	4 A	4 A	4 A/6 A	4 A/5.7 A	4 A
FABRICATION PROCESS	--	--	BiCMOS	BiCMOS	Monolithic transformer
TECHNOLOGY	SiC	Si	--	SiC	--

Selection of Auxiliary Power Supply (APS)

In addition to gate driving ICs, numerous auxiliary power supplies (APS) were also selected and tested. For the APS, 5 to 9 V conversion ratio was considered as to offer bipolar +6 V, -3 V to drive the gate of GaN devices, alongside lowest values of isolation capacitance (C_{ISO}). Lower values of C_{ISO} matter as it leads to leakage currents between primary and secondary sides for higher switching speeds. R05P205S and RV-0509S were the APS utilized in most of the test combinations. Since most of the APS use ferrite-based cores, they are highly likely to fail at CT because of reduction in their permeability and increase in core losses [5].

Selection of Auxiliary Components

Operating power electronics circuits at low temperatures need all associated components to be temperature resilient as well. Therefore, for the design of whole circuitry, thin film-based resistors and negative-positive zero (NP0) capacitors were employed since these components have been reported to show negligible variation in performance with reduction in temperature [1], [2].

Development of Hardware and Cryogenic Test Setup

Development of Gate Driving boards

As part of hardware development, separate printed circuit boards (PCBs) were designed for all the gate driver ICs, whereas a similar buffer sage IC, ISO7820x from Texas Instruments was utilized as the first stage. During the PCB development and prototyping, board shape and layout, buffer IC, all the passive components, and soldering materials were kept constant as to only see the influence of GD IC's

performance and operation. Furthermore, initially, two-stage isolation in APS was implemented with the R05P205S COTS converter. Resulting four layered PCBs and assembled gate driving boards are shown in Fig. 2 and Fig. 3 respectively. The resulting PCBs were 61mm wide and 45 high, whereas normal FR-4 material together with Sn42/Bi57.6/Ag0.4 solder paste was used to attach different components.

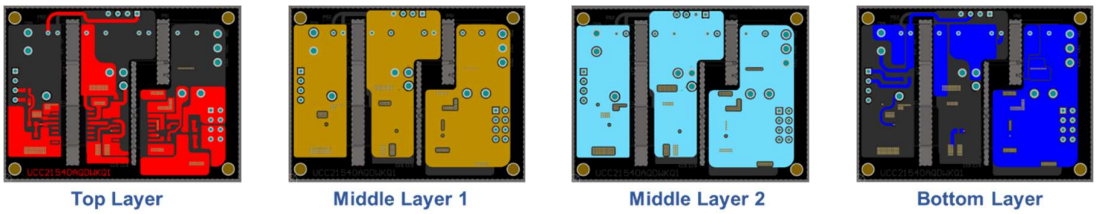


Fig. 2: Symmetric PCB layout for all five gate driver boards

Fig. 3: Development of different gate driver boards

Development of Double Pulse Test (DPT) Platform

In addition to five symmetrical gate driver boards, a DPT platform was also built so that successfully tested gate drivers and auxiliary components can be employed in driving a GaN-based converter at lower temperatures. For the DPT, a two-layered PCB structure having GaN systems GS66516T-MR device was utilized together with a 2 GHz, 101 mΩ current shunt labelled SSDN-10 to monitor the device current. Based on the initial testing observations, gate driver boards were modified while mal-operating components were removed and replaced. Hence, finalized gate driver boards (version 2) together with DPT board containing a current shunt and switching device were developed and are shown in Fig. 4.

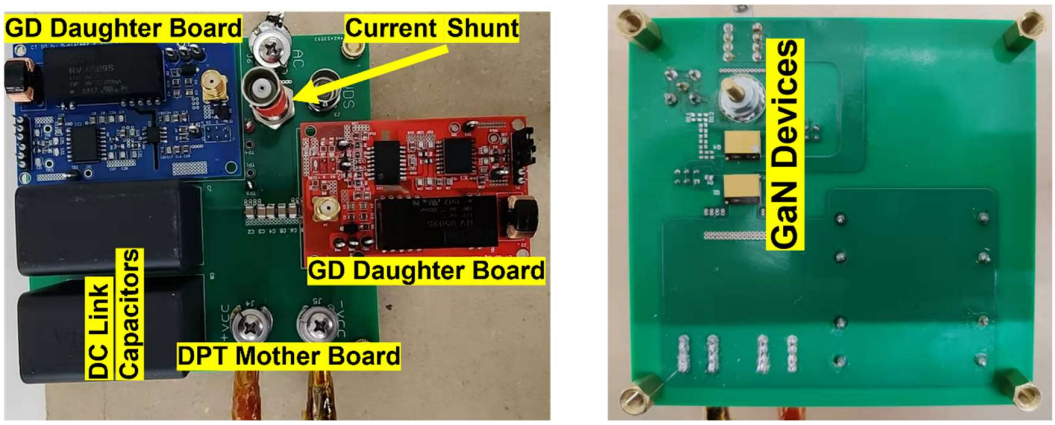
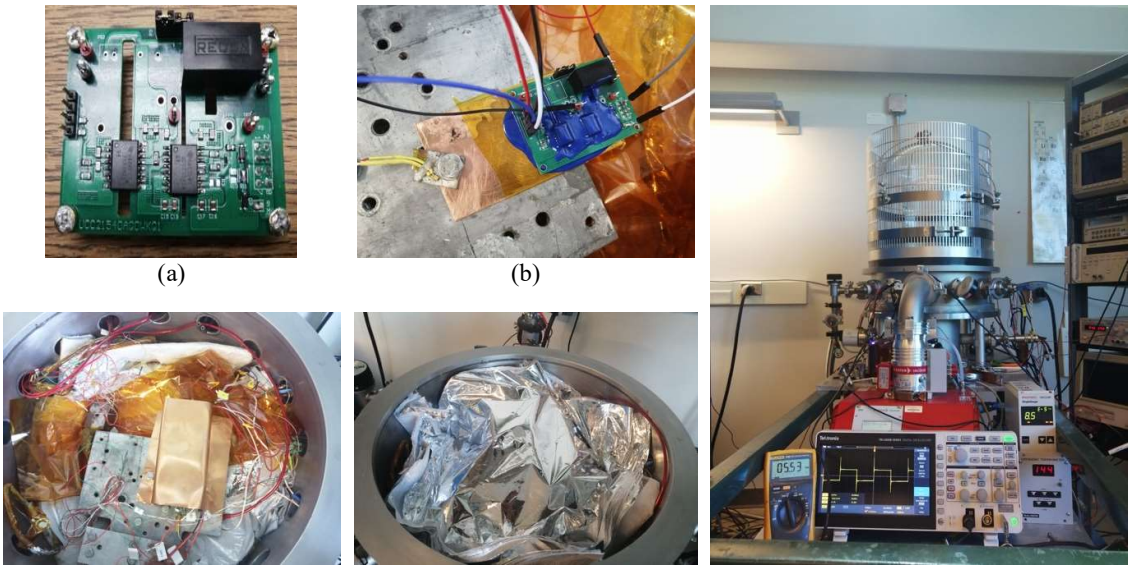


Fig. 4: Development of DPT platform together with (finalized) gate drivers

Development of Cryogenic Test Setup

For the cryogenic testing, a setup having an 18-inch stainless steel chamber integrated with A230 CryoMech single-stage cryopump was used. The chamber was evacuated to 10^{-6} Torr and the assembled gate driver boards were thermally connected to a thick copper plate by a thermally conductive epoxy, StyCast 2850FT. The copper plate was tightened with the baseplate of the chamber, where the cold/base-plate temperature was measured by a Si-diode cryogenic temperature sensor (LakeShore 420 model). The GD assembly was encompassed by a copper radiation shield and ten layers of Mylar multi-layer insulation. All the connections with source voltage, control signals, and measurement were established

using feedthroughs. For the measurements, long jumper wires were involved to bring the signal outside the chamber and displayed on Tektronix TBS 2000 B oscilloscope. Complete test setup containing the cryo-chamber alongside measurement equipment is shown in Fig. 5. The control pulses were generated using a DSP microcontroller F28379d which was also placed outside the chamber.



(a) (b) (c) (d) (e)

Fig. 5: (a) GD at RT (b) GD board connected to base plate of chamber and temperature sensor installed (c) GD covered with copper plate inside chamber (d) GD board covered with multi-layer insulation (e) Overall cryogenic chamber setup from outside containing oscilloscope, cryogenic temperature sensor.

Experimentation and Results

Auxiliary Power Supply

Numerous APS were configured on the gate driver boards assembled, but almost all of them failed except for RV-0509S. RV-0509S was tested numerous times, and was characterized during lowering the temperature to LNT, as well as bringing it back to room temperature. Although the power supply operated fine, yet there were changes in output voltages generated and input currents drawn. This trend has been depicted in Fig. 6 (a) where output voltage drops while the input current rises. The curve shown is for constant output load, which means the efficiency of isolated DC-DC converter in the APS drops as the temperature goes down. This goes well in accordance with the projected increase in core loss and decrease in permeability for ferrite cores, therefore overall efficiency of APS drops [5]. Additionally, the change in output voltage is also related to open-loop control of most of the COTS APS, and therefore an investigation about closed-loop control with variable temperature can be carried out as future work.

Gate Driving Boards

Using the experimental setup shown earlier, all five gate drivers were characterized, and unique temperature performance was observed for different ICs. Even though the gate drivers have been rated from -40 C-125 C, yet they were tested for lower temperatures as not even a single gate driver is available COTS for such applications. From the experiments, two of the gate drivers MAX22702 and Si8235AD stopped working around ~ 130 K, mainly because of their fabrication technology being BiCMOS. However, UCC21540A showed better immunity to temperature and performed well until ~ 93 K. On the contrary, ADUM4221 has a monolithic transformer technology and therefore it performed well until ~ 77 K. Similarly, Si8271 was also found to be operating fine till LNT. It is worth mentioning that numerous samples of a particular IC were characterized, and the results were found to be consistent with each iteration of experimentation. Furthermore, the buffer IC ISO7820x was found to be consistent in all the boards tested. Additionally, both the successfully operating gate drivers were configured to

switch under loaded and unloaded conditions at different switching frequencies. A silicon carbide power MOSFET C3M0016120K was used as a dummy load to verify the operability of the gate drivers. Fig. 6 (b) shows the operation of gate driver at 77 K with an operating frequency around 150 kHz.

During the process of characterization, the gate drivers were found to have variation in rise and fall times with the change in temperature. As can be seen from Fig. 6 (c), it can be observed that overshoot for Si8271 increases at first and then seems to further slowdown. This process can be related to a decrease in resistance of high output transistor of gate driver with temperature, hitting a minimum at 193 K, and starts increasing afterwards. However, looking at the turn-off time in Fig. 6 (e), the trend for undershoot looks similar which means the resistance of low output transistor keeps decreasing. Similar analysis can be carried out for ADUM4221, which shows an increase in resistance of high output transistor until 193 K and starts reducing afterwards. This trend can be inferred from Fig. 6 (d). Whereas the low output transistor impedance seems to decrease until 153 K and increases onwards as inferred from Fig. 6. (f). This variation in resistance of output transistors directly affect the rise and fall times, together with direct influence on amount of current being sourced/sinked.

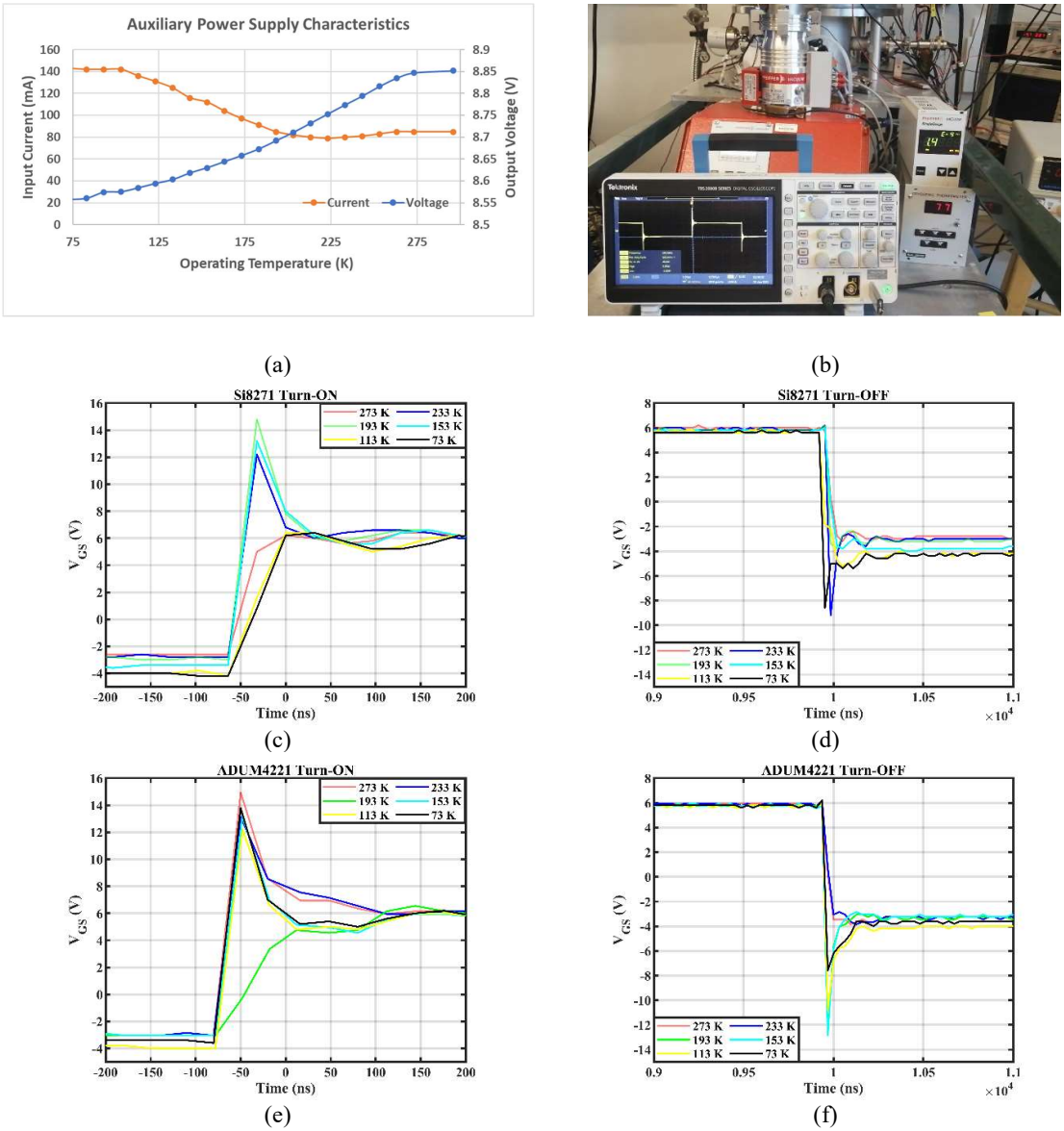


Fig. 6: (a) Performance of APS RV-0509S with temperature (b) GD boards operating fine at LNT (c) turn-on of Si8271 (d) turn-off of Si8271(e) turn-on of ADUM4221 (f) turn-off of ADUM4221

Double Pulse Tests at LNT and Device Dynamic Characterization

Having characterized the operating performance of two gate drivers, a double pulse test (DPT) setup was established and DPT experiments were only conducted at RT and LNT. The characterization gets limited to only two temperatures as DPT board cannot be placed inside the cryo-chamber because of connections involving long leads and feedthroughs of the chamber. The challenge behind doing DPT inside the chamber is related to measurement issues. Therefore, a Dewar having liquid nitrogen was used to insert DPT and gate driving boards together as shown in Fig. 7 (a).

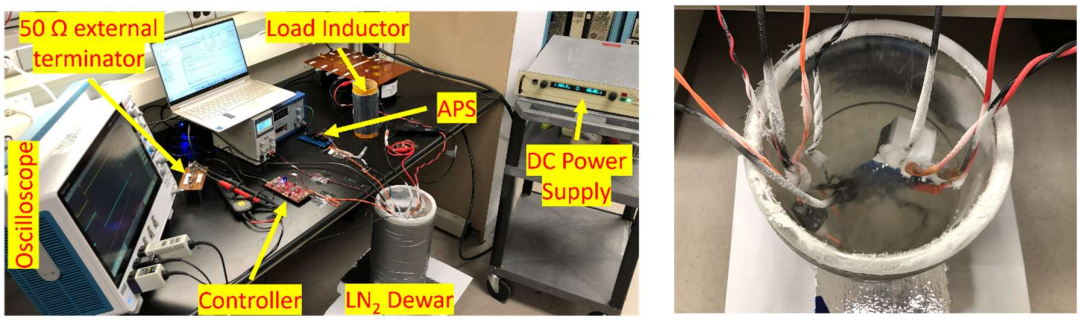
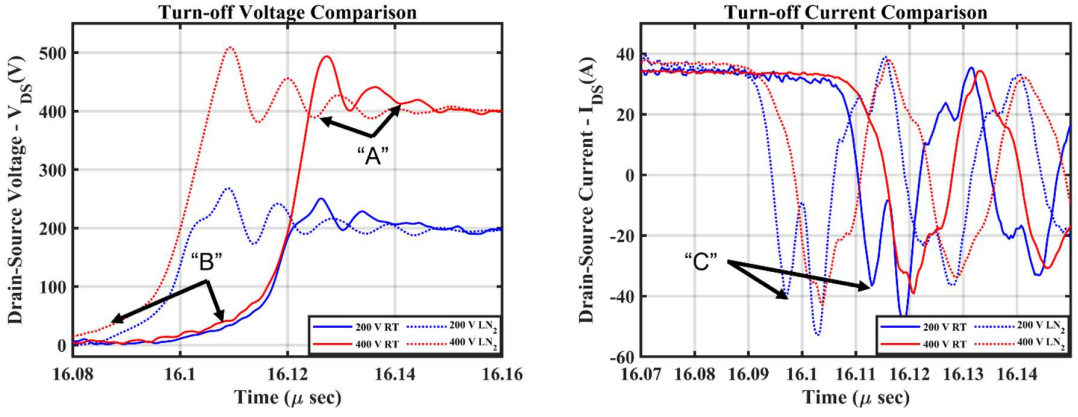


Fig. 7: (a) LN_2 Setup for DPT (b) LN_2 dewar

After characterizing the setup at RT, both DPT and GD board were inserted inside LN_2. Both the boards were subjected not only to LNT, but they were also given sudden thermal shock while inserting in LN_2 Dewar. For the measurements, active probe THDP0200 was used, and it was directly inserted inside the Dewar. Furthermore, V-I alignment with deskew adjustment was conducted before doing the LNT measurements. The results from both RT and LNT measurements are presented in Fig. 8 for device turn off behaviors. As can be seen from Fig. 8 (a), turn-off voltage at 400 V is not only advanced in time, has higher overshoot, but also has more sinusoidal high frequency oscillations at LNT temperature (labelled as A). Moreover, the response during initial time of turning off is also different at LNT (labelled as B). Similarly, turn-off current waveform has also been shown to advance, amplify (labelled as C) and have different profile during the starting times of turn-off process. Turn-off current comparison can be seen from Fig. 8 (b).

From the measurements, it can be observed that switching speeds at lower operating temperatures increase, therefore resulting in reduction in overlap times for current and voltage. This reduction in overlap has a direct influence on calculation of switching energies which can be much lower for LNT.



(a) (b)

Fig. 8: Switching Loss variation (a) Turn-on (b) Turn-off

Conclusion

In this paper, numerous commercially available gate drivers (GD) for wide band gap devices (WBG), particularly for GaN HEMTs, were characterized for low temperature applications. GDs from different manufacturers with different fabrication processes and semiconductor technology were evaluated to find the one which not only works appropriately, but its performance does not get degraded a lot. From the experimentation, two GD and a buffer integrated circuit (IC) were found to operate well until 77 K. As part of investigation, most of the commercially available auxiliary power supplies were found to fail operating except for RV-0509S. The paper characterizes the operating performance of which with temperature.

The paper also demonstrated the change in resistance of high and low output transistors of gate drivers. This change clearly gets reflected onto rise and fall times, and therefore it directly influences the over/under voltages applied at the gate source of power transistors. These over/under voltages can directly impact the switching characteristics together with failure modes of devices being switched. Furthermore, this can in resistance can also have a direct impact onto turn-on/turn-off dV/dt of power transistors. These challenges can be extremely influential for low temperature applications and need to be covered as part of future research.

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