Design of Planar Coupled Inductor Applied to Zero-Current Switching Clamped Current Converter

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Keywords

≪Planar magnetics≫, ≪Magnetic coupling≫, ≪Soft switching≫, ≪ZCS converters≫, ≪Current Source≫.

Abstract

This work focuses on the design and measuremental verification of a current source converter (CSC) with planar coupled inductor in the DC-link. Soft switching is achieved with a pseudo resonance interval between the stray inductor of the MOSFET and the output capacitor. Investigations about the improvement of the inductor are also discussed.

Introduction

Voltage source converters (VSCs) and CSCs play important role in the industry and are continuously studied in academia for improvement, either by describing new topologies or investigating alongside techniques to the conventional arrangement. Each one has its distinct mode of operation, but usually, they have patterns that can be described in a dual way [1].

Among the common characteristics, some issues come with these structures. Regarding the CSCs, it is remarkable that a large DC-link inductor needs to be used in order to compensate the twice grid frequency oscillation in single-phase converters [2]. Also, switching stress and energy dissipation through conduction must be taken into account. In [3], a converter is proposed which achieves zero-current switching (ZCS) at high frequencies by adding an auxiliary circuit between the DC-link side. Moreover, the DC-link reactive element has been part of many studies and plenty ways to reduce it has been proposed. One approach to do this is by using planar inductors in which several papers have introduced ways to design it and interesting experimental results have been obtained. In [4], it is shown a design and modeling FEM-based method due to lack of approaches in simulation tools. In [5], analysis of different types of geometry are done and comparisons between number of turns, width of the track, diameter among other parameters are evaluated.

This work aims to study, investigate and design a single-phase CSC using a technique that involves pseudo-resonating the parasitic inductance of the switches with the output capacitor. With this, no additional switch or passive component need to be added and the soft-switching capability is achieved. These parasitic inductances, called stray inductances, are intrinsic to every semiconductor and its packaging and their presence usually causes undesired overshoot and oscillations, in addition to increasing switching losses [7]. In [6], investigations about the effect of the stray inductance on switching events for a SiC MOSFET is done via simulation and experimental prototype.

This principle of pseudo-resonance was addressed on the literature as in [8], in which is proposed a DC-DC converter topology with ease of control and zero-voltage switching capability, operating in high switching frequency. It is taken from results that quasi-resonant converters working high resonant concept are an interesting alternative, despite it aren't not suitable for higher power levels. In general, the concept of a resonant pole was proposed in a full bridge pseudo-resonant DC-DC converter and some desirable attributes were taken such as simple control, wide control range and constant frequency operation [8]. Also, in [9] is proposed a zero-voltage resonant-transition (ZVRT) with similar approach which uses high switching frequency and the intrinsic C_{oss} of the MOSFET to achieve ZVS.

With increasing switching frequency the power density of the passive components can be increased but also the design process becomes more complex [10]. Basic physical properties are discussed in [11] and serve as a fundamental basis for this design. With natural convection, better heat transfer can be achieved by choosing planar core shapes and allows higher power densities [10]. In this paper, the inductive DC-link is designed as a planar design and the advantages and disadvantages are compared with a conventional inductor design. FEM-based and artificial intelligence-based simulation softwares were used for the theoretical studies and a comparison was made between the measurements of the prototype and the simulation results. In particular, the comparison of the efficiency and temperature rise is to be analyzed.

Topology Description

In this section, the operating principle of the single-phase zero-current switching clamped current (ZCS-CC) converter is presented. The proposed converter and its waveforms are shown in Fig. 1 and 2, respectively. It can be seen that the basic structure is very similar to the conventional single-phase current source inverter (CSI). The main difference is taking account the stray inductance in each MOSFET-diode switch of the H-Bridge to allow the operation of the converter with soft-switching. Also, the topology works with two different types of aproach for each horizontal pair of MOSFETs - switched and clamped. As summarized in Table I, the converter operation mode can be divided into two modes. In mode 1, the switch s_3 is clamped off and s_4 is clamped on while the upper pair is switching in a complementary way. In the second mode, the upper pair is clamped while the bottom one switches. t_{on} indicates the time for when s_1 (or s_4, in case of mode 2) is turned on and therefore the output voltage v_o is increasing, t_{off} is the time when the same switch is turned off, t_{dt_1} and t_{dt_2} are the dead time for the switches s_1 and s_2 (mode 1) and T_s the switching period. Due to the architecture of the H-bridge and the switching characteristic, the converter can operate either as DC/DC or as DC/AC converter [7], [12].

Table I: Switching pattern of the two DC-DC operation modes.

	Mode 1	Mode 2
s_1	$t_{\text{on}} + t_{\text{dt}_1} + t_{\text{dt}_2}$	T_{s}
s_2	$t_{\text{off}} + t_{\text{dt}_1} + t_{\text{dt}_2}$	0
s_3	0	$t_{\text{off}} + t_{\text{dt}_1} + t_{\text{dt}_2}$
s_4	T_{s}	$t_{\text{on}} + t_{\text{dt}_1} + t_{\text{dt}_2}$

In order to simplify the analysis of the converter, it is assumed that the circuit operation is in steady-state, the output inductor is large enough to be considered as a current source, and the output filter capacitance is very small, providing sufficiently fast voltage changes in one switching period to enable the proposed

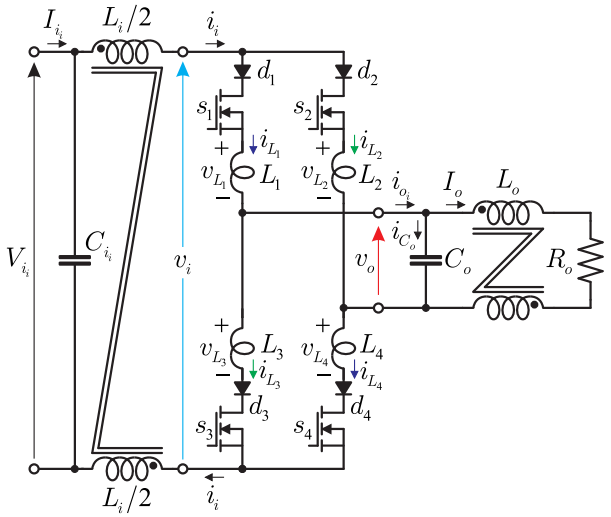


Fig. 1: Proposed ZCS-CC Converter.

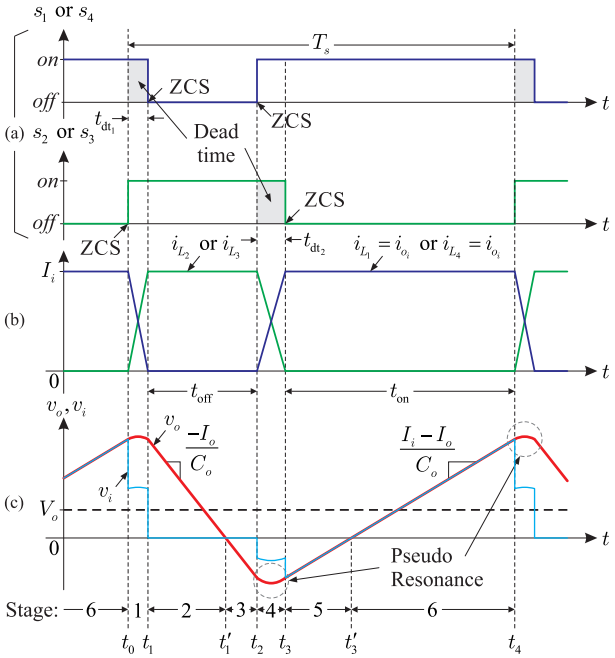


Fig. 2: Main waveforms of the proposed converter.

operation, as shown in Fig. 2 (c).

The proposed converter has six stages of operation during each switching cycle. As mentioned before, the circuit uses one horizontal pair of MOSFETs to be clamped and another one for the switching operation. For the description of this section, the mode 1 will be considered.

Stage 1 $[t_0,t_1]$ - For $t \leq t_0$, s_1 is conducting the input current (I_i) and $i_{C_o} = I_i - I_o$, so the output voltage is increasing linearly with a slope of $(I_i - I_o)/C_o$. In $t = t_0$, s_2 is turned on with zero current due to the presence of the stray inductors, which do not allow sudden current variation. The current through L_2, i_{L_2}, grows more slowly compared to its current rise time (due to resonance). Even at this stage, the inductances resonate with the C_o capacitor. Since L_1 = L_2 is very small (as well as the C_o value), the resonance frequency $f_n = 1/(2\pi\sqrt{L_r \cdot C_o})$ is much higher than the switching frequency of the converter. This small resonance, present in the dead time, is what leads to the naming pseudo-resonant. During this interval, the voltage v_o flows through the two inductors equally with $v_o/2$, causing L_1 to discharge and L_2 to charge. Applying Kirchoff's Law:

$$v_{L_2} - v_C - v_{L_1} = 0 \qquad (1) \qquad -v_{L_1} = v_{L_2} = \frac{v_o}{2} \qquad (2)$$

Stage 2 $[t_1,t_1^{'}]$ - At $t = t_1$, the current i_{L_1} reaches zero and s_1 can be turned off at zero current. At that point, a freewheeling is created and all current from the source runs through s_2. In this interval, the output voltage, v_o, decreases linearly, since the capacitor starts to supply the load. At this moment, its voltage falls to a slope of $-I_o/C_o$.

Stage 3 $[t_1^{'},t_2]$ - With s_2 still on, and with the capacitor-load combined, the current source load type begins to inject energy and the capacitor voltage reverses and becomes negative. The input voltage remains zero due to the presence of the freewheeling.

Stage 4 $[t_2,t_3]$ - At $t = t_2$, s_1 turn on with zero current and the same charge-discharge process of the inductors, as well as the pseudo-resonance, seen in stage 1, will happen again, with the inductor L_1 charging with $v_o/2$ and the inductor L_2 discharging with $-v_o/2$. So:

$$v_{L_2} + v_C - v_{L_1} = 0 \qquad (3) \qquad v_{L_1} = -v_{L_2} = \frac{v_o}{2} \qquad (4)$$

Stage 5 $[t_3, t_3']$ - In this stage, the current in the inductor L_2 reaches zero and s_2 can be opened at zero current. During this stage, a path from the source to the capacitor is created, through s_1, through which the capacitor will be charged and its voltage will increase linearly, by an angular coefficient of $(I_i - I_o)/C_o$; the input voltage is the opposite of the output voltage.

Stage 6 $[t_3', t_4]$ - From t_3', the period in which the output voltage returns to be positive and increases linearly, the capacitor remains being charged along the path created in the previous stage until the switching period is completed, returning to the point $t_4 = t_0$;

It can be observed, that zero-current switching occurs at the following times: $t_0 = t_4$, t_1, t_2 and t_3. Due to the stray inductances, the switches must be triggered only with zero current, otherwise the stored energy in them will be dissipated in the switches. To achieve soft switching, the voltage across the capacitor needs to be positive and negative in each switching period, so that the charging and discharging process of both capacitors is carried out completely, as shown in stages 1 and 4.

In practice, the value of $L_1 - L_4$ are not quite easy to control, which lead to unreliable results, especially regarding the output voltage value. As said before, this voltage need to have a ripple that covers positive and negative values so that the technique will properly work. In order to overcome this stability problem on the inductors values, a control for the length of the dead time can be done [13].

For this converter, the control of the output current can be done using a variable switching frequency PWM. Assuming that the dead times t_{dt_1} and t_{dt_2} are very small in proportion to T_s, the voltage waveform of the capacitor can be approximated to a triangular shape. The relationship between output current and input could be seen as for a buck converter, $I_o = D \cdot I_i$, where D is the duty cycle of s_1. The average output voltage is V_o.

Coupled Inductor Design

Planar inductors with PCB winding offer several advantages such as a high integration density, a defined structure and the associated reproducibility. However, the high parasitic coupling capacitance and low copper fill factor must be taken into account in the design process. The simulative design of the inductor is performed using Frenetic and GeckoMAGNETICs simulation software. Frenetic determines the results based on the input parameters and the artificial intelligence based algorithm and also offers several design proposals. Within the GeckoMAGNETICS simulation environment, there is more freedom regarding the geometric modeling of the winding and is thus more suitable for this specific application. Furthermore a 2D FEM simulation in ANSYS Maxwell is performed to avoid saturation effects.
For the evaluation of the planar design of the coupled inductor, an additional design is generated as a reference inductor using the simulation software Frenetic, which is initially considered as the optimal design with the lowest losses. Accordingly, the manual design of the planar inductor is performed using Gecko MAGNETICs and is based on the design methodology in [10]. This comparison is intended to illustrate the advantages and disadvantages of the planar design in terms of geometric dimensions as well as physical properties. The starting points for the design are, on the one hand, the current waveform shown in Fig. 3 as well as the voltage drop across the inductors and, on the other hand, the required inductance value for the current DC link of approx. 100 µH resulting in 50 µH for each inductor.

$$L = \frac{V_\mathrm{i} \cdot (1-D)}{\Delta i_\mathrm{L} \cdot f_\mathrm{sw}}, \quad V_\mathrm{i} = 24\,\mathrm{V}, \quad D = 0.5, \quad \Delta i_\mathrm{L} = 1\,\mathrm{A}, \quad f_\mathrm{sw} = 125\,\mathrm{kHz} \tag{5}$$

Since the current converter can be used in both DC-DC and DC-AC operation, the requirements for the inductors in the respective operation must be considered separately. In DC-DC operation, sufficient energy should be stored for one switching period, whereas in DC-AC operation, the current ripple and output frequency determine the inductance value. The design procedure shown here refers specifically to DC-DC operation. In order to be able to investigate the influence of different switching frequencies within the topology, the N97 ferrite core material is chosen, which has a low power loss density for the selected operating range between 125 kHz and 500 kHz. For the worst-case consideration of core losses and the amount of stored energy, the design process is performed for the switching frequency of 125 kHz.

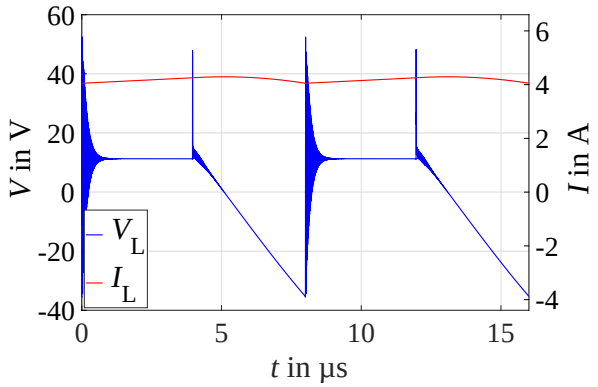
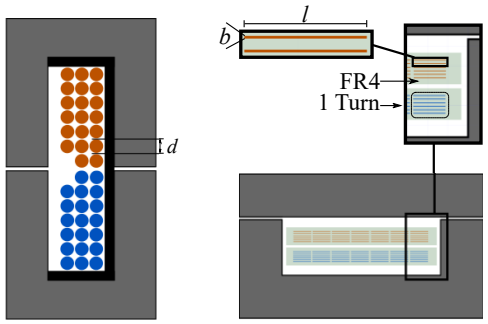


Fig. 3: Voltage and current waveforms of one coupled inductor for simulative dimensioning and loss calculation of the inductor design.



(a) ETD 34 (b) ELPI 43

Fig. 4: Schematic arrangement of the two coupled inductors inside one winding window. The windings are separated by color.

Due to the high number of turns and the associated low magnetic flux density excitation, the winding losses are dominant compared to the core losses. The low harmonic spectrum of the input current additionally leads to very low AC losses within the winding, so that the ohmic losses resulting from the DC resistance of the winding and the RMS-value of the current can be compared in a simplified way.
First simulative design results are shown in Fig. 4 - Fig. 7 and are summarized in Table II. The schematic illustration of the inductors shows a winding window of a core half, in which the windings of the two inductors contrast with each other in terms of color. One advantage of the conventional chokes is the significant high copper filling factor and the associated low DC resistance of the winding as well the smaller construction volume. To reduce the DC resistance of the PCB winding, a 6-layer PCB is chosen to parallel the winding.

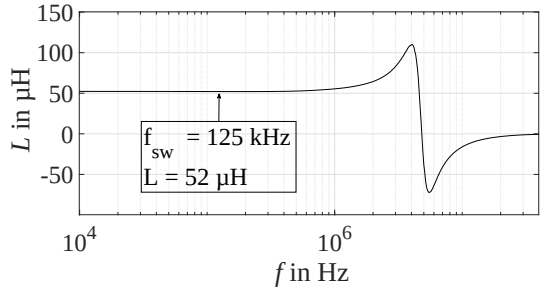


Fig. 5: Inductance measurement of one inductor with an impedance analyzer.

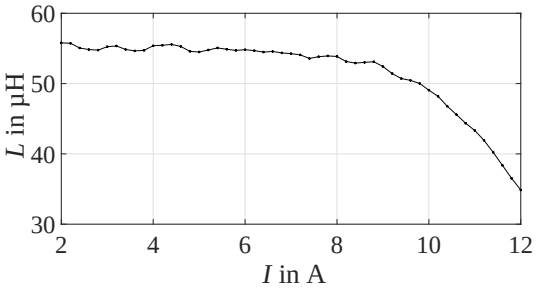


Fig. 6: Saturation current measurement.

A brief cost analysis was worked out on the basis of 1000 units. The result shows that the ferrite costs in the reference design are significantly lower, but due to the additional coil former and the higher copper costs compared to the PCB, the total costs are approximately the same.

Fig. 5 shows the inductance measurement with an impedance analyzer. The resulting value fits to the simulation results and also the frequency range from 125 kHz up to 500 kHz is far away from the resonant frequency causing by the inductance itself and coupling capacitance between both windings which is expected to be much higher than in the reference design due to the large area between both PCB winding. To take care of saturation effects it must be taken into account that both windings are sharing one core caused a doubling of the magnetic flux density. In Fig. 6 it can be seen that saturation effects starts at about 9 A, which is sufficient for this topology.

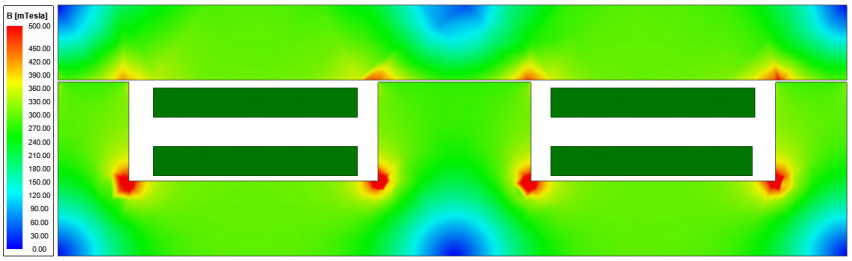


Fig. 7: 2D FEM simulation of the planar ELP core with an air gap of 0.12 mm to determine the magnetic flux density distribution in ANSYS Maxwell.

Table II: Simulation results of an reference inductor in comparison of a planar inductor. Parameters marked with * are refered to one inductor in the coupled inductor design. The cost calculation is an estimation for an order quantity of 1000 pieces.

Parameters	Reference inductor	Planar inductor
Core type	ETD 34/17/11	ELP/I 43/10/28
Core material	N97	N97
Number of turns*	20	7
Winding type	Round	PCB winding
Winding geometry	d = 1.4 mm	l = 1.6 mm, b = 35 µm
Air gap	0.64 mm	0.12 mm
Core boxed volume	23.11 cm^3	32.54 cm^3
Weight	73 g	76 g
Copper filling factor	70.3 %	6.4 %
Inductance*	54.06 µH	57.84 µH
Core losses	-	-
Winding losses*	0.53 W	1.79 W
DC resistance* @ 20 °C	10.12 mΩ	46.9 mΩ
Temperature*	36.2 °C	41.7 °C
Core material cost	2.22 $	4.42 $
Coil former cost	1.07 $	-
Winding cost	2.14 $ (2.4 m winding length)	1.41 $ (PCB 35 cm x 50 cm)

Hardware Setup and Measurements

The hardware setup that was built for validation is shown in Fig. 8. A 200 V MOSFETs IPB107N20NA from Infineon is used in series with the 650 V diodes C6D10065E from Wolfspeed in order to achieve the reverse blocking capability. On the left side of the prototype the planar inductor is shown which consists of two 6-layer PCB, each for one winding. In addition a auxiliary wire make the connections between the two PCBs. Each PCB has a thickness of 1.6 mm, in which the insulation between the different layers is approximately 0.3 mm. At the main PCB, the power and control components are placed (top side) as well as filtering circuits for the gate driver power supply and heat sinks for the MOSFETs and diodes (bottom side). The control signals from the drivers are generated from a microcontroller STM32F411RE from STMicroelectronics and RECOM converters are used to provide an isolated 12 V voltage as a driver supply.

To achieve 100 W rated input power, an input current of 4.2 A and input voltage of 24 V was applied. All of the variables and the respective values of the experimental setup can be seen in the Table III as well as the experimental results for 100 W input power can be seen in Fig. 9. As can be seen in magenta, the output voltage (scaled by a 0.5 factor) reaches positive and negative values, totalizing 104 V of ripple, in

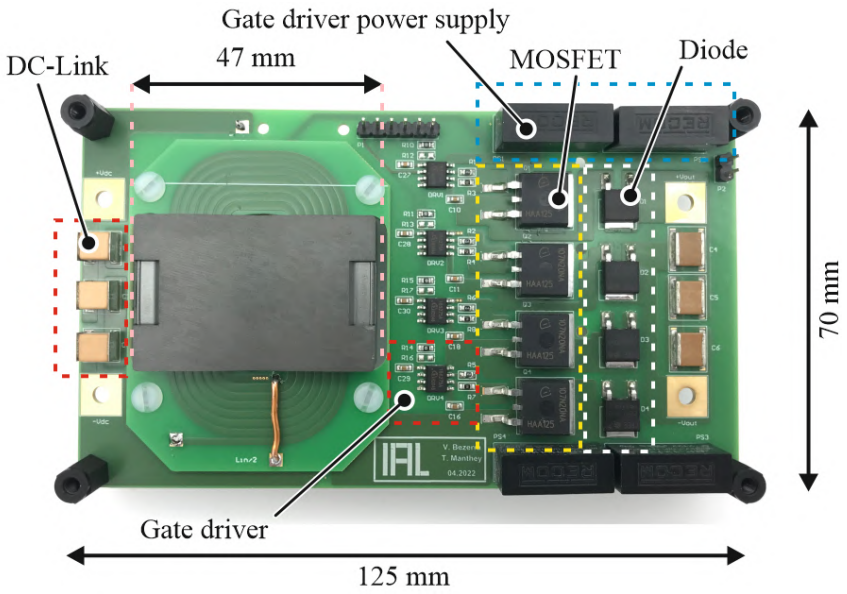


Fig. 8: Hardware prototype of the ZCS-CC with coupled planar inductors at the input side.

one switching period, enabling the proposed operation. The current waveforms in both active switches are shown in Fig. 9 (a) and Fig. 9 (b).

Table III: Variable values for the experimental setup.

Parameter	Variable	Value
Input voltage	V_{in}	24 V
Input current	I_i	4.2 A
Input inductor	$L_i/2$	57 µH
Output capacitor	C_o	220 nF
Switching frequency	f_s	125 kHz
Duty cycle	D	50 %
Deadtime	t_{dt}	200 ns
Output voltage ripple	v_o ripple	104 V
Efficiency	η	83 %

In the zoomed Fig. 9 (c), the zero-current turn-off transition can be seen. When the gate-source signal v_{gs_2} turn on, the current on the switch s_1 decreases and the soft-switching on s_1 can be achieved as expected. However, in Fig. 9 (d), it could be seen a slightly different behaviour on the turn off moment of s_2. There is still a current through the switch, which leads to a pseudo-zcs on this component. Furthermore, an efficiency investigation on the prototype was done and the result can be seen in Fig. 10. Another investigation made is that since the output capacitance value is much smaller when compared to a capacitance value of a conventional DC-AC topology, it becomes extremely sensitive to enviromental changes (temperature changes) therefore the use of capacitors class 1 is more desirable.

A thermal photograph taken in steady state with an IR camera in Fig. 11 shows the heat distribution of the whole prototype. The estimates maximum temperature in the simulation has an deviation of only 3.9 K. Since s_4 is switched on continuously, comparatively high forward losses occur in the associated diode compared to the soft-switching diodes, which leads to a distinct temperature increase. For further optimisation, diodes with a lower forward voltage at nominal current can be selected.

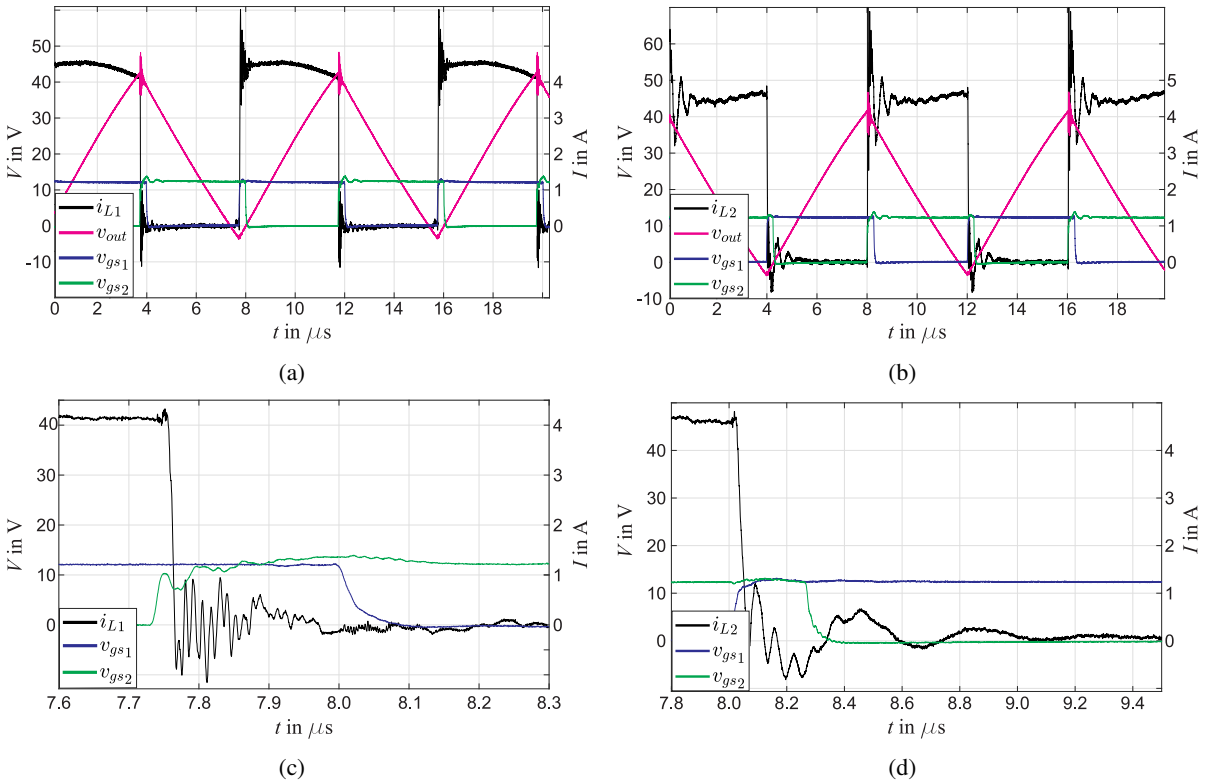


Fig. 9: Experimental results for 100 W and 125 kHz. Waveforms for: (a) S_1 and (b) S_2. Zoomed ZCS in (c) S_1 and (d) S_2. In black, both i_{L1} and i_{L2}, in magenta the output voltage (divided by two) and blue and green the gate signals v_{gs_1} and v_{gs_2}.

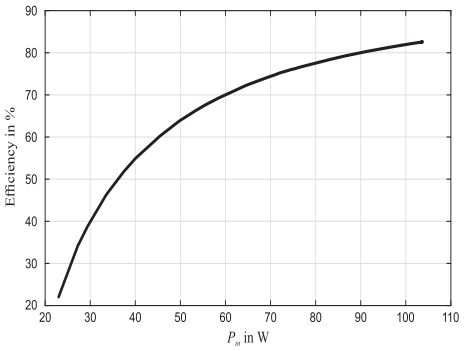
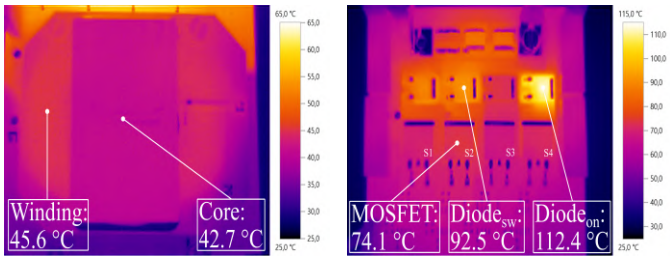


Fig. 10: Efficiency curve of the converter prototype for a maximum input power of 100 W.



(a) Winding and core (b) Power semiconductors

Fig. 11: Thermal photograph taken with an IR camera.

Conclusion

An extensive topology description of the current source converter including switching state analysis is followed by a design methodology of a planar coupled inductor as well a measuremental verification. As part of the inductor design, a reference design was first generated for comparison with the planar inductor. A first design of the planar coupled inductor is presented and the advantages and disadvantages are discussed. A hardware prototype was built and analyzed in DC-DC operation. As in the theoretical approach expected, zero current switching is achieved in the MOSFETs and the switching transients are shown in greater detail. Furthermore an efficiency of about 83 % is achieved at an input power of 100 W.

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