Short Circuit Performance and Current Limiting Mode of a Monolithically Integrated SiC Circuit Breaker for DC Applications up to 800 V

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Keywords

≪Solid-State Circuit Breaker (SSCB)≫, ≪Current limiter≫, ≪Short circuit≫, ≪Self-sensing control≫, ≪Power semiconductor device≫, ≪Silicon Carbide (SiC)≫, ≪JFET≫.

Abstract

This paper presents the short circuit performance of a novel SiC circuit breaker device, which is based on the "thyristor dual" functionality. The developed device structure is motivated with regard to manufacturing aspects and electrical requirements. Furthermore, the basic "thyristor dual" operation is elaborated on the basis of quasi-static electrical measurements of a fabricated prototype. The proposed self-sensing and self-triggering devices make auxiliary circuitry like sensors and micro-controllers expendable and practically have no propagation delay. As a result, short circuit clearance within 122 ns at 800 V is demonstrated in experiments. Moreover, by utilisation of a third device terminal, a temporary current limiter functionality can be obtained. The scalability of the current limit value is discussed on the basis of measurements in time domain. The maximum current limit value achieved is 7.4 times higher than the trigger current level of the circuit breaker device. Additionally, the same circuit configuration which is used for the current limiting mode, allows to remotely reset the circuit breaker after it turned to blocking-state. This opens up a wide range of possibilities to enhance the circuit breaker with intelligent functionalities.

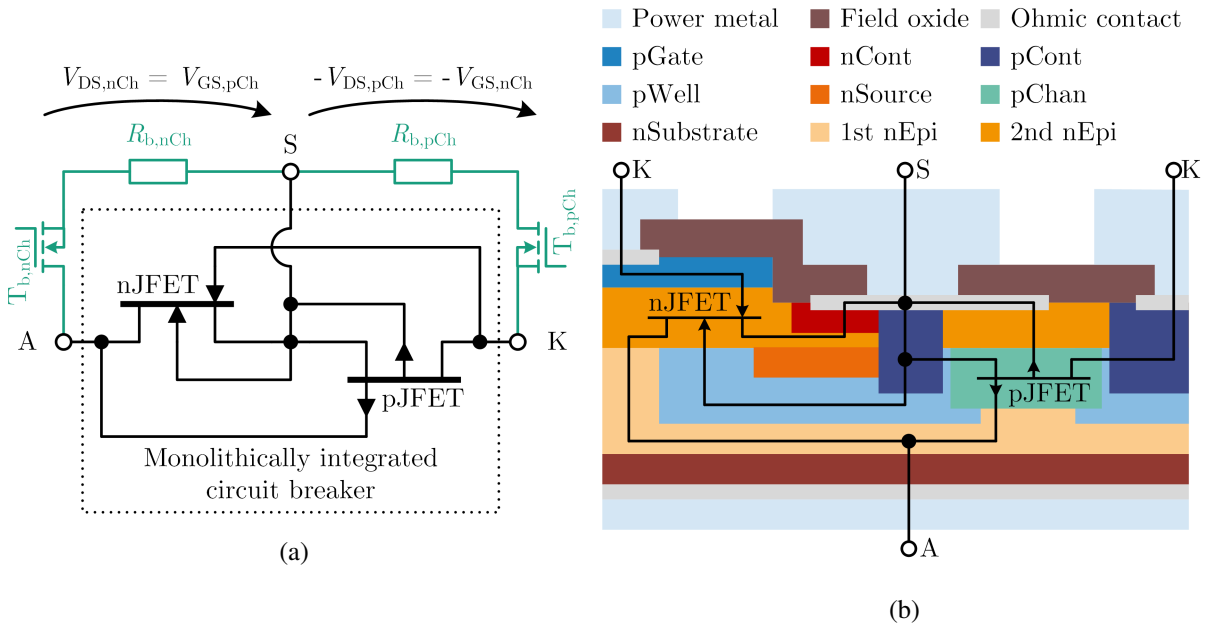

Fig. 1: Equivalent circuit diagram (a) and schematic cross section (b) of the proposed monolithically integrated circuit breaker. The bypasses formed by the transistors $T_{b,nCh}$ and $T_{b,pCh}$ and the resistors $R_{b,nCh}$ and $R_{b,pCh}$ in (a), are used for the proposed current limiter functionality and are not present in default circuit breaker configuration. The indices "nCh" and "pCh" represent nJFET and pJFET, respectively. In (b), the prefixes "n" and "p" indicate n-type and p-type regions, respectively.

Motivation

In recent years, a trend towards power electronic DC-applications exhibiting several hundred volts DC-link voltage is observed. The development of adequate solid state circuit breakers (SSCB) pursued various approaches to overcome challenges regarding arching, complexity and response time [1, 2]. However, even highly integrated state-of-the-art SSCB concepts require sense, supply or drive circuits in addition to the semiconductor switch [3, 4]. Moreover, especially in DC micro-grid applications, inrush currents much higher than the nominal current level occur during the charging period of power converter input capacitances. These currents must be tolerated by the circuit breaker without triggering, which poses further difficulties in terms of system level design [5]. With the discovery of the "thyristor dual" functionality, a potential two-pole device level solution with an intrinsic trigger mechanism has been introduced [6]. Promising characteristics have been observed in experiments at up to 400 V using discrete SiC JFET devices in cascode configuration [7–9]. In an effort towards monolithic integration, TCAD modelling was utilised on a topology suitable for 900 V DC-applications to discuss design and fabrication implications [10, 11]. Finally, the first physical demonstration of a simple two-pole "thyristor dual" device capable of several hundred volts blocking voltage has been realised in a 4H-SiC JFET technology [12]. In this work, we investigate the transient performance of those devices in a short circuit experiment at 800 V DC-link voltage. Furthermore, a temporarily activatable and scalable current limiting function by utilisation of a third device terminal is introduced, which also allows for remote reset of the SSCB.

Monolithically Integrated SiC Circuit Breaker Technology

As shown in Fig. 1a, the "thyristor dual" concept is realised by employing an n-channel JFET (nJFET) and a p-channel JFET (pJFET). Note, that the bypasses formed by the transistors $T_{b,nCh}$ and $T_{b,pCh}$ and the resistors $R_{b,nCh}$ and $R_{b,pCh}$, respectively, are not present in default configuration. The JFETs are arranged in a series configuration, where each gate is interconnected to drain of the other JFET. In this arrangement, intrinsically over-current triggered and self-sustained blocking operation is achieved, which is caused by the positive feedback of forward and control voltage (V_{DS} and V_{GS}) of both JFETs [11].

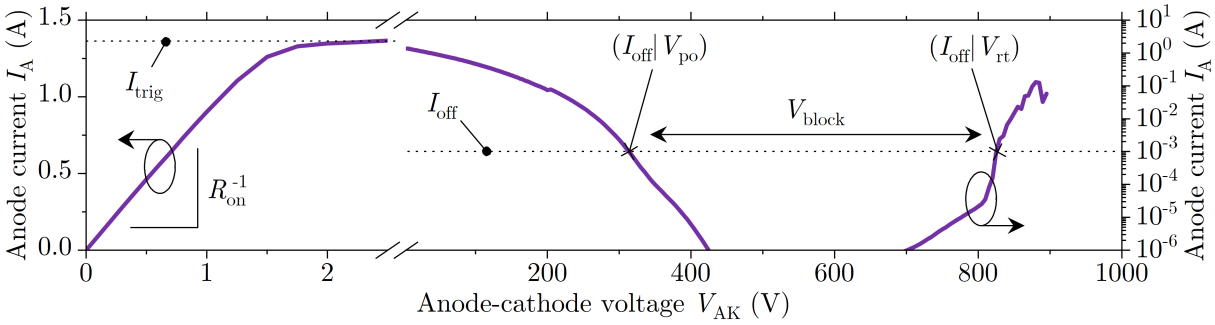

Fig. 2: Measured quasi-static output characteristics $I_A(V_{AK})$ of a proposed monolithically integrated SSCB device. In the low voltage region ($V_{AK} \leq 1\,V$), a static on-state resistance R_{on} is observed. For $I_A \leq I_{off}$, the SSCB is considered in blocking-state. Note, that $I_{off} = 1\,mA$ is chosen rather arbitrarily.

With respect to 800 V DC-applications, several hundred volts must be expected at the JFET gates after the SSCB turns to blocking-state. The schematic cross section of the device topology depicted in Fig. 1b is specifically developed to provide sufficient voltage sustainability at the pJFET gate structure. Regarding fabrication, the employed 4H-SiC technology is based on ion implantation, re-epitaxy and SiC dry etching. Ion implantation of nitrogen and aluminium is used to create n-doped (nSource and nCont) and p-doped regions (pWell, pChan, pGate and pCont), respectively. After finishing the implantations in the first n-type epitaxial system (1st nEpi), a second epitaxial layer is grown (2nd nEpi). The nJFET MESA gate structure is created by ion implantation of pGate and subsequent SiC dry etching. The ohmic contact region in the center of the unit cell allows carriers to overcome the natural pn-junction at the common source terminal (S) of both JFETs. Ultimately, the high potential anode terminal (A) is located at the device bottom side, whereas the low potential cathode (K) and the source terminal (S) are accessible from the top side. As can be obtained from the inserted equivalent circuit diagram, the pJFET gate is facing towards the 1st nEpi drift region. Since the majority of the blocking voltage can be expected to drop across the drift region, high pJFET gate voltage sustainability is obtained.

The measured curves $I_A(V_{AK})$ shown in Fig. 2 represent the quasi-static output characteristics of the SSCB devices investigated in this study. For anode current values I_A below a certain trigger current value I_{trig}, the devices operate in a current controlled linear on-state region. The emphasised linear region reveals a static on-state resistance R_{on}. By exceeding I_{trig}, the intrinsic pinch-off mechanism is triggered and the device turns to self-sustained blocking-state, blocking the DC-link voltage V_{bat}. After triggering, the $I_A(V_{AK})$ trajectory strongly depends on the circuit configuration. However, as long as V_{bat} remains within the blocking voltage window V_{block} between the pinch-off voltage V_{po} and the reach-through voltage V_{rt}, the blocking-state is maintained. Note, that $I_{off} = 1\,mA$ is chosen rather arbitrarily.

Experimental

Measurement Environment

For the experiments in this study, the circuit configuration depicted in Fig. 3a is used. By turning on transistor T_P, the load current I_L is ramped up over time according to

$$I_L(t) = \frac{V_{bat}}{R_{load}} \cdot \left(1 - e^{-\frac{t \cdot R_{load}}{L_{load}}}\right), \tag{1}$$

where $R_{load} = 183\,\Omega$ and $L_{load} = 9.6\,mH$ represent load resistance and load inductance, respectively. The on-state resistances of T_P and the SSCB can be assumed much smaller than R_{load} and are neglected with respect to eq. 1. During current ramping, the SSCB carries the full load current. Therefore, the blocking mechanism is triggered as soon as I_L reaches I_{trig}. After triggering, the current through the SSCB cannot increase any further and the device turns to blocking-state.

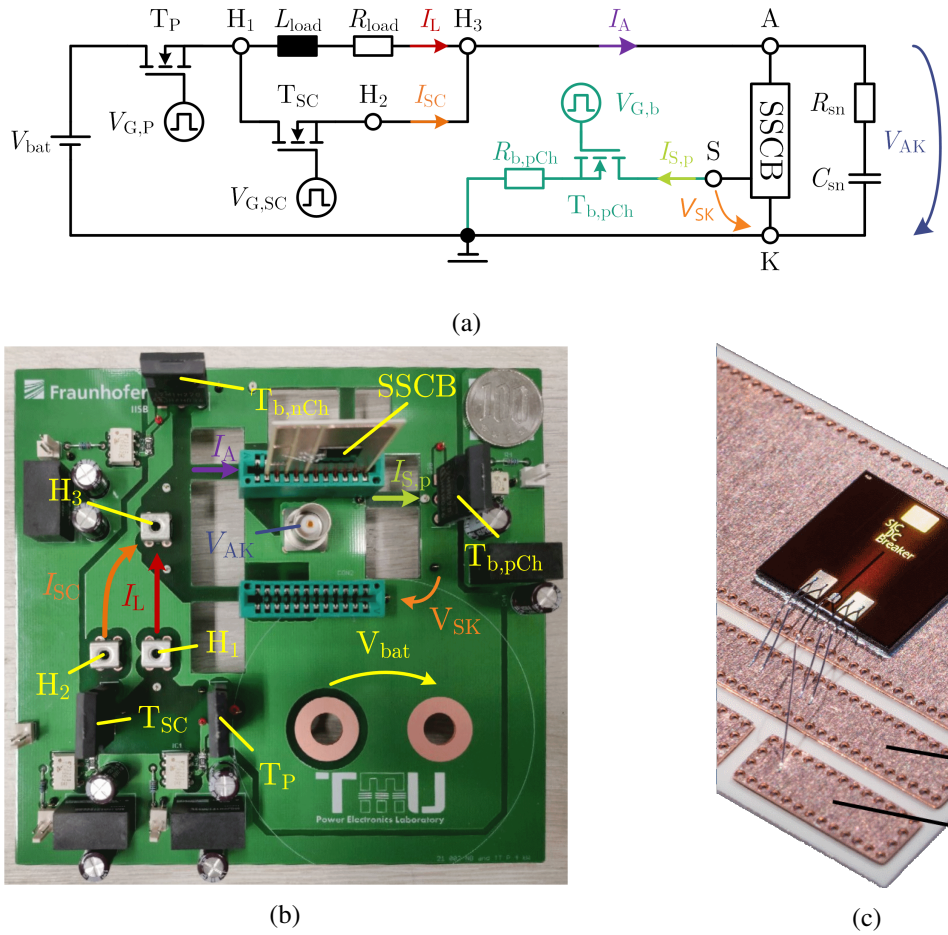

Fig. 3: Simplified circuit diagram (a) and corresponding circuit board (b) used for the experiments. The load is determined to $L_{\text{load}} = 9.6\,\text{mH}$ and $R_{\text{load}} = 183\,\Omega$. 1.2 kV CoolSiC MOSFETs (IMW120R220M1H) are used for T_P, T_SC, $\text{T}_\text{b,nCh}$ and $\text{T}_\text{b,pCh}$. In (c) a photo image of a proposed SSCB chip mounted on DBC substrate is shown.

However, in case of the short circuit experiment, transistor T_SC is turned on before I_{trig} is reached, creating a short circuit in parallel to the load. For the experiments, the SSCB devices are mounted on DBC substrates as presented in Fig. 3c. The corresponding circuit board shown in Fig. 3b, is designed for investigation of up to two circuit breaker devices in parallel by utilisation of card edge connectors. The two-device option is not used in this study. Note, that an empty card edge connector socket represents an open circuit. The load is connected to the screw terminal hubs H_1 and H_3. The short circuit is established between the screw terminal hubs H_2 and H_3, with the aid of a copper wire of several centimeters length. The bypass transistors $\text{T}_\text{b,nCh}$ and $\text{T}_\text{b,pCh}$ are arranged as depicted in Fig. 1a but are only used to activate the proposed current limiting mode or for remote reset. The bypass resistors $\text{R}_\text{b,nCh}$ and $\text{R}_\text{b,pCh}$ are located at the circuit board back side. Furthermore, an RC-snubber can be found on the circuit board backside, close to the card edge connectors. The snubber parameters $R_{\text{sn}} = 4.7\,\Omega$ and $C_{\text{sn}} = 220\,\text{pF}$ are solely chosen to suppress oscillations in the very high frequency band. Due to the rather small value of C_{sn}, no snubber impact on switching speed and surge voltage is expected.

Short Circuit Experiment

At the beginning of the short circuit experiment, I_L is ramped according to eq.1. The short circuit is applied at $t = 0$, which corresponds to $V_{\text{bat}} = 800\,\text{V}$ and $I_\text{L} = 1\,\text{A}$. Fig. 4 shows the transient response of the SSCB device to the short circuit event. After T_SC is activated, $I_\text{A} = I_\text{L} + I_\text{SC}$ increases at a rate of $\frac{\text{d}I_\text{A}}{\text{d}t} = 0.66\,\text{A}\,\text{ns}^{-1}$ and reaches a maximum value of $I_{\text{react}} = 18.1\,\text{A}$ at approximately $t = 52\,\text{ns}$. Notably, I_{react} is more than 10 times higher than the trigger current level I_{trig}, as can be obtained from Fig. 2.

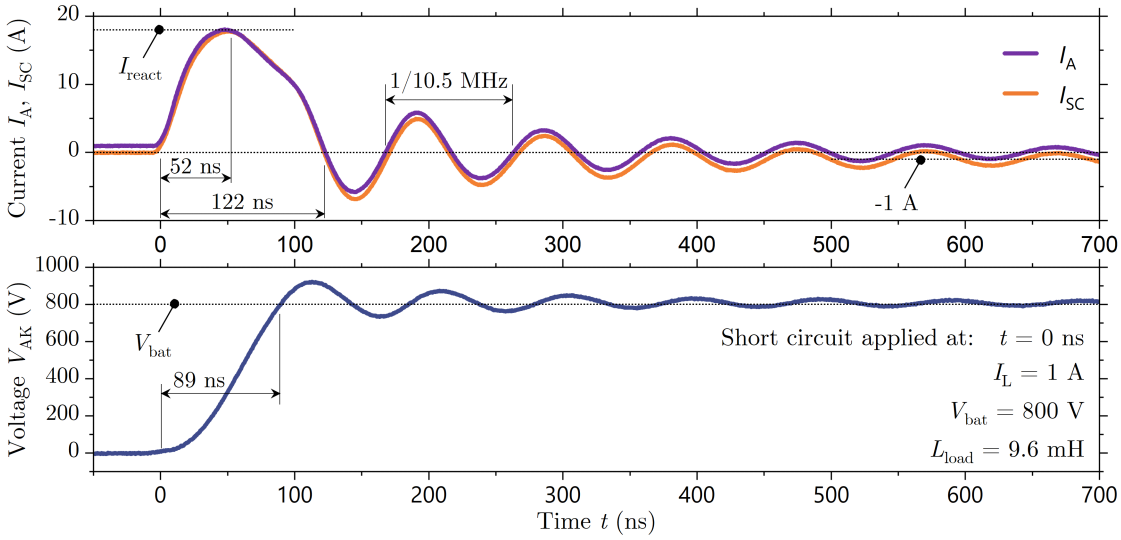

Fig. 4: Measured short circuit response of the proposed SSCB at a battery voltage of $V_{bat} = 800\,V$. The top graph shows the anode current $I_A(t)$ and the short circuit current $I_{SC}(t)$. The anode-cathode voltage $V_{AK}(t)$ is depicted in the bottom graph.

Considering that I_{react} is reached at the inflection point of $V_{AK}(t)$, the origin of these high current values is concluded to a displacement current. As soon as the SSCB device starts blocking the DC-link voltage, every capacitance between nodes A and K is charged to 800 V, including the snubber capacitance C_{sn}. The remaining parasitic capacitances C_{par} related to assembly, packaging and the SSCB chip are estimated to

$$C_{par} = I_{react} \cdot \frac{\partial t}{\partial V_{AK}} - C_{sn} = 1.24\,nF, \tag{2}$$

which seems reasonable, taking into account $C_{sn} = 220\,pF$ and the rather simple packaging approach.

Triggered by the high short circuit current, the SSCB blocks V_{bat} within 89 ns. The first zero-crossing of I_A is obtained 122 ns after the short circuit is applied. Subsequently, oscillations of 10.5 MHz occur for all investigated signals, where V_{AK} and I_A converge to V_{bat} and 0 A, respectively, verifying that the SSCB is in steady and self-sustained blocking mode. Since the SSCB is completely pinched off after triggering, I_L finds the free wheeling path through the body diode of T_{SC}. Therefore, the oscillation of I_{SC} converges to -1 A and, subsequently, declines over time until the energy stored in L_{load} is depleted.

Current Limiting Mode

Since the common source terminal of both JFETs (S) is not connected in default configuration, the ”thyristor dual” circuit breaker resembles a two-pole device. As a consequence, the trigger current level cannot be externally controlled but is solely determined by the device design, which can be scaled by adequate variation of design parameters [11, 12]. Nevertheless, the source terminal (S) can be utilised to tolerate higher current values for a dedicated period of time (e.g. during current inrush). By employing a simple series connection of a transistor and a resistor as proposed in Fig. 1a between the terminals (A) and (S) or (S) and (K), a bypass in parallel to either of the JFETs is established. The bypass is activated by turning on either $T_{b,nCh}$ or $T_{b,pCh}$, whenever a tolerable over current event is estimated. Notably, only one bypass is supposed to be used at a time, while the other one represents an open circuit. In this configuration, the intrinsic trigger mechanism is suppressed, because the positive feedback of the JFET forward voltage V_{DS} and control voltage V_{GS} is prevented. Consequently, instead of turning to blocking-state, the SSCB is limiting the current I_A to the JFET saturation current level, which is controlled by the resistance values of either $R_{b,nCh}$ or $R_{b,pCh}$.

The influence of $R_{b,pCh}$ on the current limit level is depicted in Fig. 5. Here, the course of I_A, I_S, V_{AK} and V_{SK} over time is shown in case of an activated bypass over $T_{b,pCh}$. In this experiment, the measurement set-

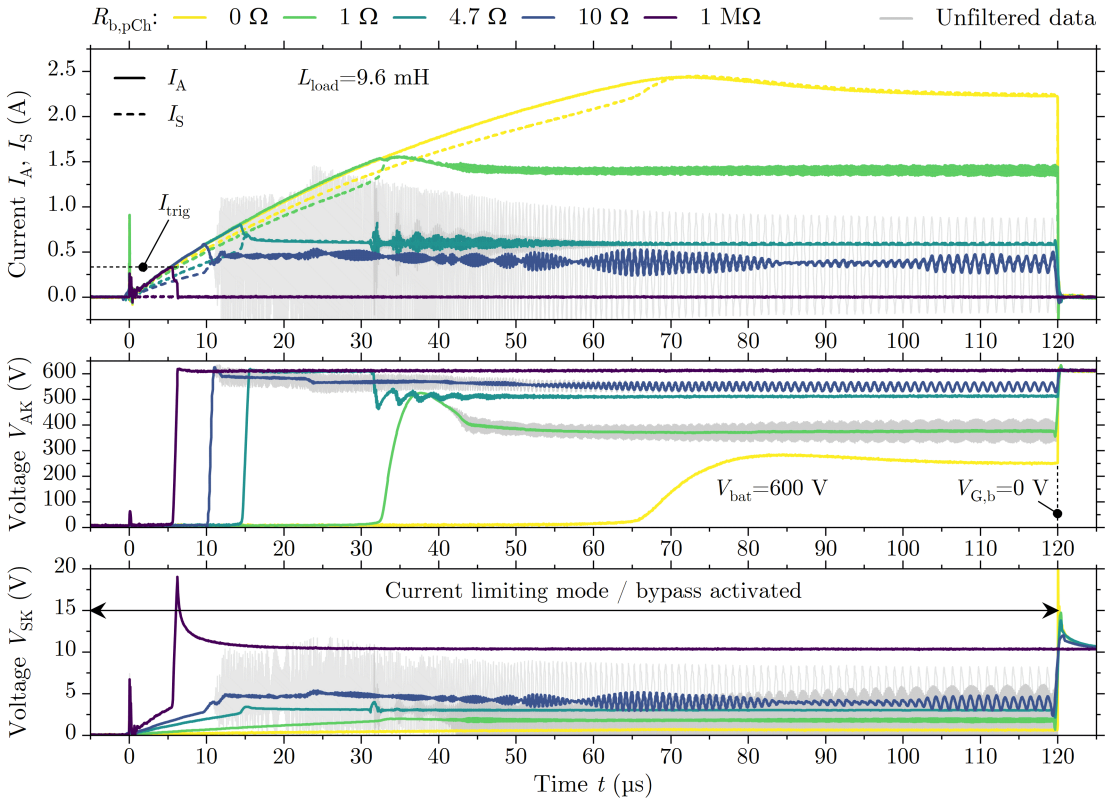

Fig. 5: Illustration of the current limit mode of the proposed SSCB in dependence of the bypass resistance value $R_{b,pCh}$. The graph in the top shows the anode current $I_A(t)$ and the bypass current measured at the source terminal (S) $I_S(t)$. In the middle the anode-cathode voltage $V_{AK}(t)$ is depicted. The course of the floating source-cathode $V_{SK}(t)$ can be obtained from the bottom graph.

up depicted in Fig. 3a is used as well. However, T_{SC} remains turned off. The default SSCB configuration is represented by $R_{b,pCh} = 1\,M\Omega$, showing the intrinsic trigger at $I_A \approx 330\,mA$, which corresponds to the design of this particular SSCB device. Therefore, the SSCB blocks the supply voltage of 600 V as soon as $I_A = I_{trig}$. For this case, the SSCB immediately stops conducting the current after triggering and I_L commutates to T_{SC} as discussed above.

By using an active bypass with a lower $R_{b,pCh}$ value, the SSCB keeps I_A at a constant value, instead of stopping the current flow. At $t = 120\,\mu s$, the bypass is deactivated and the SSCB device is turning to blocking-state since I_A is higher than the trigger current level. Please note, that heavy oscillation occurred during the current limiting experiment. Therefore, a moving average is applied to particular sets of the measurement data. The unfiltered data is depicted in grayscale. Nevertheless, the results sufficiently serve the purpose of illustrating the general behaviour in current limiting mode. As can be observed, the value to which I_A is limited increases as $R_{b,pCh}$ decreases, up to 2.44 A for $R_{b,pCh} = 0\,\Omega$, which is 7.4 times higher than I_{trig}. During the current ramping, the majority of the current, which is measured at the anode terminal (A) is leaving the SSCB at the source terminal (S). The difference $I_A - I_S$ is assumed to flow through the pJFET according to the current divider given by the pJFET channel resistance and $R_{b,pCh}$. As soon as I_A reaches the maximum value, the SSCB forward voltage V_{AK} significantly increases and both JFETs can be considered saturated. In saturation, the pJFET channel resistance is much higher than $R_{b,pCh}$. Consequently, the entire current flows through the bypass and I_S becomes equal to I_S.

In general, the current limit value I_{lim} for an ohmic current limiter can be calculated to

$$I_{lim} = \frac{V_{bat}}{R_{lim}}, \tag{3}$$

where R_{lim} is the current limiting resistance. In the proposed case, R_{lim} results from the series connection

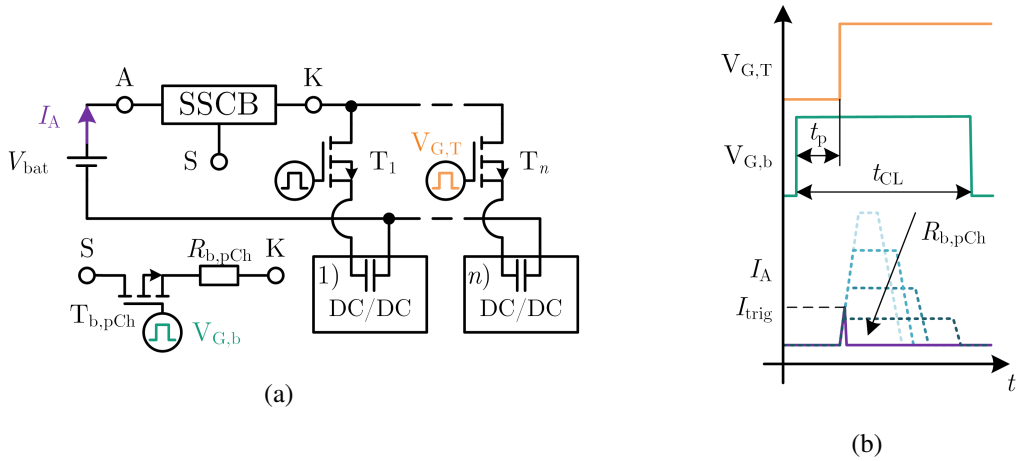

Fig. 6: Schematic circuit diagram (a) and corresponding schematic gate signals (b) to illustrate the utilisation of the proposed current limiting mode.

of R_{load}, $R_{b,pCh}$ and the channel resistance of the nJFET. The on-state resistance of T_P and $T_{b,pCh}$ may be neglected with respect to eq. 3. Note, that in current limiting mode, the JFETs are operating in saturation region. Therefore, the nJFET channel resistance is determined by V_{SK} and, hence, strongly depends on $R_{b,pCh}$. As a result, I_{lim} is not linearly scaling with $R_{b,pCh}$.

Such functionality is particular useful during inrush current events in DC-networks. In Fig. 6a, a schematic circuit diagram of a DC-network consisting of the proposed SSCB with applied (S)-(K) bypass and a number of n DC/DC converters. By turning on the power switch T_n, the input capacitance of the corresponding DC/DC converter is charged to V_{bat}. During this charging period, current values much higher than I_{trig} can occur, which may cause the SSCB to turn to blocking-state. This case is illustrated in Fig. 6b by the purple I_A curve. Applying the bypass for the current limit mode as discussed above, allows the SSCB to tolerate these high currents without triggering. Moreover, the duration of the charging period can be manipulated by variation of $R_{b,pCh}$ as shown by the dotted blue curves. As illustrated by the curves of $V_{G,T}$ and $V_{G,b}$, the current limiting mode must be activated shortly before the inrush event is expected to occur and last at least for the time period t_{CL}, which corresponds to the estimated charging duration. For the pre biasing period t_p, several hundred nanoseconds are sufficient as will be demonstrated in the next chapter.

Remote Circuit Breaker Reset

In addition to the current limiting functionality, the proposed bypass configuration is capable to remotely reset the circuit breaker from blocking-state to on-state by applying a $V_{G,b}$ pulse of several micro seconds. In Fig. 7, the gate signals $V_{G,P}$, $V_{G,SC}$ and $V_{G,b}$, the current signals I_L, I_A and I_{SC} and the voltage signal V_{AK} are shown for a sequence of an intrinsic trigger, followed by a remote reset and a subsequent short circuit event at $V_{bat} = 800\,V$. Turning on T_P in phase I leads to a significant current spike due to current inrush, which potentially triggers the SSCB as discussed above. For this reason, the current limiting mode is activated by turning on $T_{b,pCh}$ for a period of $t_{CL} = 600\,ns$, $t_p = 100\,ns$ before T_P is turned on, preventing the trigger event. In phase II, I_L is ramped according to eq. 1. At the beginning of phase III, I_L reaches I_{trig} and the SSCB starts blocking V_{bat}. As can be obtained, I_A declines rather slowly during the charging period of the parasitic capacitances to $V_{bat} = 800\,V$ as discussed above. However, as soon as $V_{AK} = V_{bat}$, the body diode of T_{SC} is polarised in forward direction. Consequently, I_L commutates to T_{SC} and I_A drops abruptly. The corresponding maximum transients are determined to $\frac{dV_{AK}}{dt} = 1.72\,kV\,\mu s^{-1}$ and $\frac{dI_A}{dt} = -63.5\,A\,\mu s^{-1}$, respectively. The current turn-off in phase III corresponds to a clamped inductive switching event, which is completed within $0.86\,\mu s$ after the trigger current level is reached.

The demagnetisation of L_{load} over a period of approximately $75\,\mu s$ is emphasised in phase IV. Here, the SSCB remains in steady and self-sustained blocking mode. In phase V at $t = 100\,\mu s$, I_L declined to approximately $500\,mA$. At this point a $V_{G,b}$ gate voltage pulse of $1\,\mu s$ is applied to the bypass transistor

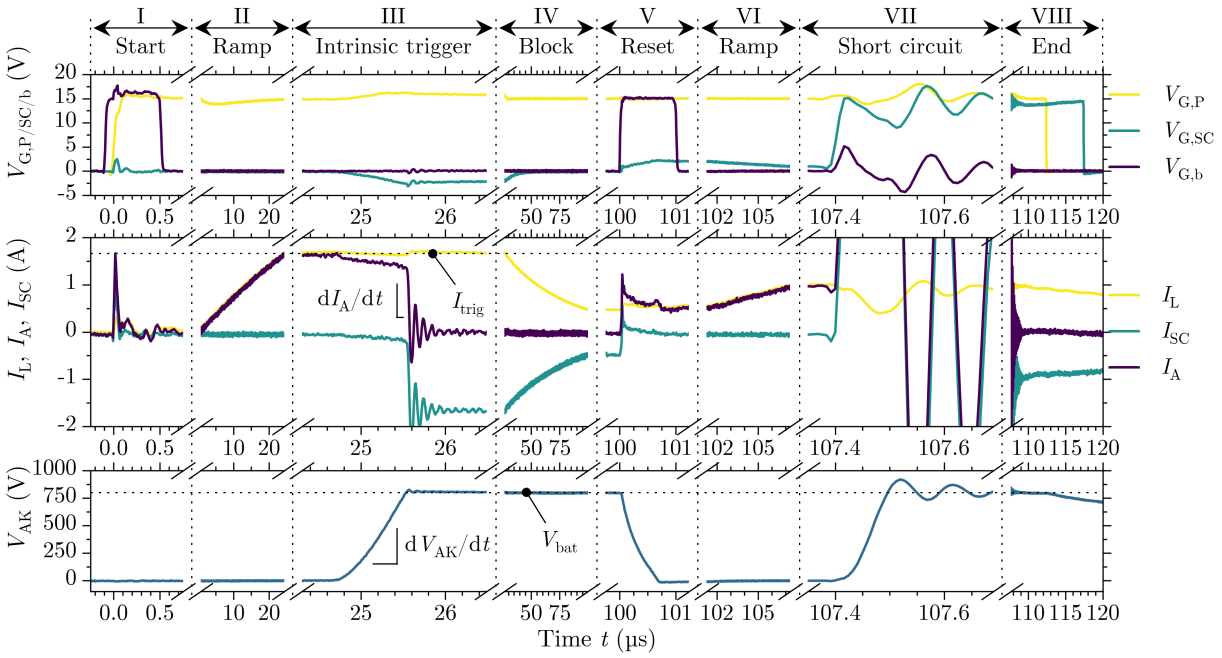

Fig. 7: Measured sequence of events including the intrinsic trigger, remote reset of the proposed SSCB and a short circuit event at $V_{bat} = 800\,V$. The graph in the top shows the gate signals $V_{G,P}(t)$, $V_{G,SC}(t)$ and $V_{G,b}(t)$. In the middle the current signals $I_L(t)$, $I_A(t)$ and $I_{SC}(t)$ are depicted. The course of $V_{AK}(t)$ can be obtained from the bottom graph.

$T_{b,pCh}$. Subsequently, I_L commutates back to the SSCB and V_{AK} drops to a corresponding on-state voltage level. The SSCB is reset and conducts I_L in the linear operating region (see Fig. 2). In phase VI, I_L ramps up over time again. The subsequent short circuit depicted in phase VII is identical to the short circuit event discussed above. In phase VIII, T_P is turned off to end the experimental sequence.

Conclusion

The short circuit performance of a novel self-sensing and self-triggering solid state circuit breaker device is presented in this work. A reaction time of 52 ns to a short circuit event at 800 V DC-link voltage and 1 A short circuit current is demonstrated with the aid of experiments. Short circuit clearance is achieved within 122 ns. These results represent the fastest response among comparable studies published so far. Notably, the two-pole devices ensure safe circuit breaker operation without the necessity of an additional power supply or other auxiliary circuitry. However, in order to obtain additional functions (e.g. scalable current limiter, remote reset), a simple series connection of a transistor and a resistor can be added between the floating source terminal and the anode or cathode terminal. With regard to the oscillation behaviour during current limit mode and considering the rather low trigger current values of the prototypes investigated in this study, the potential of this technology is yet to be exploited in order to be competitive on the market. However, by scaling the trigger current value to several 10 A, from our findings we believe, the proposed device topology is a promising candidate for DC applications in e-mobility and DC micro-grid environments.

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