Improvement of a self-powered gate driver power supply

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Keywords

«Intelligent gate driver», «Smart Gate Drivers», «Driver concepts», «Power supply», «Multi-level converters»

Abstract

In this work, an improved self-powered gate driver power supply is proposed, analyzed by simulation and experimentally validated. This solution is based on the addition of a voltage regulator and it achieves a floating, constant and robust voltage to supply the gate driver and auxiliary circuits (protections, sensors, local control and communications) in switching cells for multilevel converters implementation. The obtained gate driver supply voltage is stable for a wide range of frequencies and auxiliary circuit current consumptions. Moreover, the main characteristics of the main transistor turn-on and turn-off are preserved while decreasing the power dissipation of the gate driver power supply circuit.

Introduction

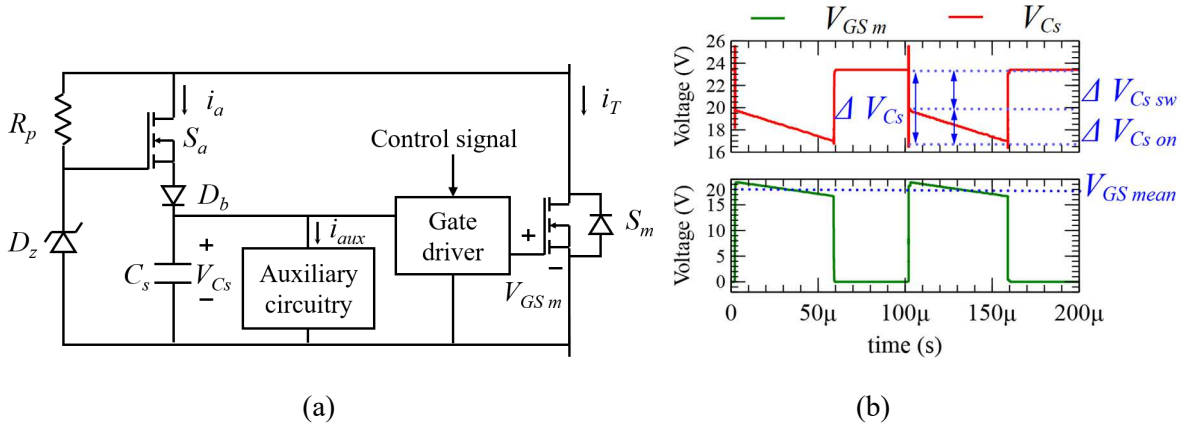
Among all power topologies involved in AC conversion, multilevel converters have been attracting an increasing attention during the last years. Such a solution presents additional advantages compared with the traditional two-level VSI topologies widely spread in the industry. In 2003, the introduction of the Modular Multilevel Converter (MMC) topology [1, 2] drastically boosted the practical implementation of the multilevel approach into the industry for a wide power range. The MMCs are implemented by the interconnection of basic Switching Cells (SC) formed by power transistors with their antiparallel diodes connected in half-bridge configuration and a capacitor across this structure. This passive component on each SC slows down the initialization process and requires specific control strategies at converter level for assuring the correct voltage balancing among capacitors. This fact and the need for bulky and heavy branch inductors are two of the drawbacks of the MMC topology. Among all multilevel solutions, the multilevel active clamped (MAC) topology introduced in 2011 [3], though showing a slightly higher harmonic distortion and switching losses, presents several clear advantages in terms of modularity [3], integrability [3], redundancy [4], and fault-tolerant capability [4], justifying the complexity and over cost coming from the higher number of used active devices and

drivers. The MAC converters are formed by the association of basic SC without any capacitor; only N-1 capacitors are required at the converter input (N-1 = converter levels) and they do not require any inductance, providing practically a "full Silicon" (or "full semiconductor") solution. In return, the number of devices required for an N-level converter increases as N^2 (and not proportionally with N as in MMCs), increasing the complexity of the MAC implementation. As an evolution of the MAC approach, a new paradigm has emerged in 2018 [5], the so-called Switching-Cell Array (SCA) converter topology, which consists of a matrix arrangement of $2N^2$ highly-optimized SCs that can be easily reconfigured to produce converter legs with different voltage and current ratings.

In such a scenario, SC modularity and compactness is a crucial feature in order to tackle with the implementation of a large number of controlled devices in the same converter. Nevertheless, there is a lack of power module solutions specifically designed as elementary building blocks for multilevel topologies to demonstrate their major performances under regular and faulty operating conditions, especially for the SCA case. The present work aims at solving one of the limiting factors to achieve smart and compact SC modular solutions for SCA implementation: the floating gate driver power supply (GDPS).

A usual solution is an external gate driver power supply (EGDPS) using compact dc-dc converters [6], however it becomes costly and inefficient when the number of switches increases. An alternative could be a bootstrap power supply [7][8], but high-power and low-power states are not galvanically isolated and there is a dependence between top-side and low-side switching.

This work will focus on the solution proposed in [9], shown in Fig. 1, which is a self-powered internal GDPS (IGDPS) for the gate driver of the main power switch S_m (a power MOSFET in this case). In [10], an optimization of the design in terms of losses and switching times was performed at high switching frequency (100 kHz), but the driver supply voltage presents significant variations (ripple) that make it unsuitable to power auxiliary circuitry such as short circuit, over-temperature and shoot-through protections, as well as for supplying digital local control and communication devices. In this sense, the present work proposes a significant improvement of this IGDPS scheme based on the implementation of a voltage regulator to stabilize the driver supply voltage. The improved solution proposed in this work (internal regulated GDPS, IRGDPS) has been exhaustively analyzed by simulation (LTspice), and experimentally validated using a buck converter (70V VDMOSFET, V_{bus}= 30V, L=0.4mH).



(a) (b)

Fig. 1: (a) Internal gate driver power supply (IGDPS) circuit schematic. (b) Example of the capacitor voltage V_{Cs} and gate source voltage ($V_{GS\,m}$) of S_m of an IGDPS in a buck converter.

Internal gate driver power supply

In the IGDPS of Fig. 1 (a), the gate driver is powered by the capacitor voltage V_{Cs}. The capacitor C_s is charged during the turn-off of the main transistor S_m. Its maximum voltage ($V_{Cs\,max}$) will be the reverse

voltage of the zener diode (V_z), minus the forward voltage drop of the diode D_b (V_{Db}) and the gate-source voltage drop of the auxiliary transistor S_a ($V_{GS\,a}$).

$$V_{Cs\,max} = V_z - V_{Db} - V_{GS\,a} \tag{1}$$

At the beginning of the S_m switching-off, the voltage at drain and source terminals of S_a start rising, then, S_a switches on and the current i_a charges the capacitor C_s. The capacitor stops charging when the cut off condition of S_a is achieved.

During the on-state of S_m, its gate voltage $V_{GS\,m}$ is V_{Cs} (gate driver supply voltage) minus the gate driver output stage voltage drop (ΔV_{driver}). Therefore, any variation in the C_s capacitor voltage during the on-state of S_m is directly transmitted to $V_{GS\,m}$ affecting the on-state resistance value of S_m. As mentioned before, $V_{Cs\,max}$ depends on V_z, V_{Db} and $V_{GS\,a}$, but its mean value depends also on the switching frequency (f) and the duty cycle (d) (which determine the C_s charging rate), as well as, its discharge process.

The diode D_b prevents the C_s from discharging through the auxiliary transistor when S_m is in on-state. On the other hand, C_s suffers two discharge processes: an abrupt discharge during the turn-on of S_m and a slow discharge during the S_m on-state. The abrupt discharge ($\Delta V_{Cs\,sw}$) associated to the abrupt V_{Cs} falling slopes shown in Fig. 1 (b) corresponds to the charge transfer between C_s and the S_m input gate capacitance during its turn-on. The subsequent slow discharge process is associated to the slow V_{Cs} falling slope shown in ($\Delta V_{Cs\,on}$) which corresponds to the current consumption of the gate driver and the auxiliary circuitry during S_m on-state ($I_{on} = I_{aux} + I_{driver}$) (shown in Fig. 1 (b)). During the off-state, the auxiliary circuitry current I_{aux} will slow down the C_s charge.

The voltage ripple (ΔV_{Cs}) and the S_m mean gate-source voltage ($V_{GS\,mean}$) can be estimated with the equations (2) and (3) respectively, where Q_g is the gate charge. These equations are only valid when the C_s capacitor is fully charged during the turn-off of S_m. This condition may not be true when the capacitance value is too large or the off time of S_m is not sufficiently long. The proper design of the circuit and its control must avoid these conditions during normal operation. As it can be seen in the equations, there is a dependence between the voltage ripple and the mean gate-source voltage of S_m. Besides, only some combinations of V_z-C_s can achieve a certain $V_{GS\,mean}$ which makes this circuit complex to dessign.

$$\Delta V_{Cs} = \Delta V_{Cs\,sw} + \Delta V_{Cs\,on} = \frac{Q_g}{C_s} + I_{on}\frac{d}{f \cdot C_s} \tag{2}$$

$$V_{GS\,mean} = V_{Cs\,max} - [\Delta V_{Cs\,sw} + \frac{\Delta V_{Cs\,on}}{2} + \Delta V_{driver}] \tag{3}$$

Fig. 2 shows ΔV_{Cs}, $\Delta V_{Cs\,sw}$, $\Delta V_{Cs\,on}$, the S_m dissipated power (P_m), and the total dissipated power (P_{total}) for a $V_{GS\,mean}$=15V (simulation parameters in **Table I**). For the estimation of the total dissipated power, only the elements with a significant power consumption have been considered (S_m, driver and S_a). Almost constant V_{Cs} values can be achieved with large capacitances (ΔV_{Cs} = 35mV for C_s=10µF-V_Z=16V), but the circuit performs inefficiently showing the highest total power losses. For large C_s values, the capacitor continues charging after the turn-off of S_m while the auxiliary transistor S_a is conducting causing significant losses [9]. Moreover, there is less or no reduction of S_m power consumption in comparison to EGDPS. In summary, Fig. 3 shows that there is a trade-off between minimum voltage ripple and power losses in S_a when increasing C_s.

Table I: Simulation parameters for the IGDPS

Buck converter	L = 0.4mH,- V_{BUS}=30V	D_b	RSX051VYM30 (30V)
S_m	IPB015N04N (40V)	V_z	TFZ--B
R_G	3Ω	S_a	PMPB14XN (40V)
Driver	1ED44175N01B	R_p	215kΩ

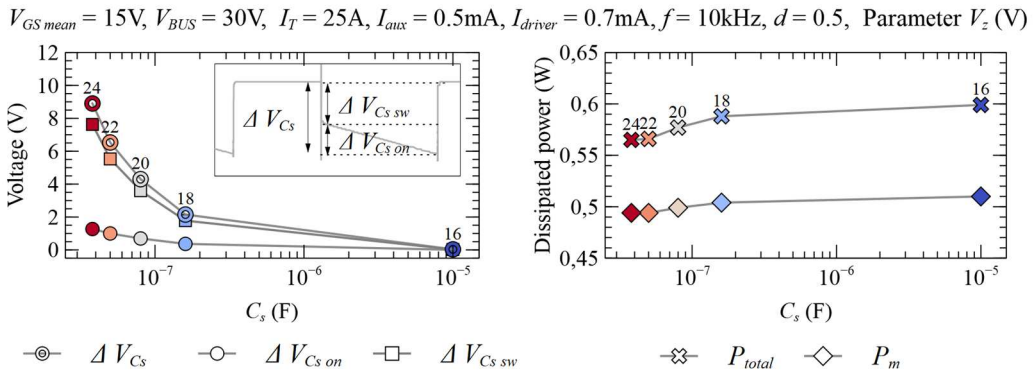


Fig. 2: Simulation of the IGDPS ΔV_{Cs} voltage drop and power dissipation (P_m: S_m power dissipation; P_{total}: driver, S_a and S_m power dissipation) for different combinations of V_z and C_s (24V – 38nF; 22V – 50nF; 20V – 80nF; 18V-160nF; 16V-10µF). The numbers over the symbols indicate zener voltages.

Once the capacitor and the zener diode have been selected (they can be considered as gate-driving design parameters), the $V_{GS\,m}$ and P_{total} can vary with the operating parameters since ΔV_{Cs} changes with I_{aux}, f and d for a given transistor S_m and its associated turn-on gate charge Q_g (equations (2) and (3)). As Fig. 3 (a) and Fig. 3 (b) show, $\Delta V_{Cs\,on}$ and $V_{GS\,mean}$ are more sensitive to I_{aux} and f variations when C_s is small. Increasing the S_m on-state semi-period (by decreasing f or increasing d) or increasing I_{aux} will lead to higher $\Delta V_{Cs\,on}$ values and a reduction in $V_{GS\,mean}$. If the capacitor is too small, at certain operation conditions such as low f or high I_{aux}, the minimum C_s voltage can be lower than the required minimum gate driver supply voltage and the circuit will not be operating correctly, therefore, in Fig. 3 (b) there are no simulations for V_z =24V – C_s = 38nF when I_{aux} is higher than 2mA.

P_{total} increases with I_{aux} (Fig. 3 (b)) due to a slower C_s charge, which causes the transistor S_a to be in on-state for a longer time. Similarly, the P_{total} increases with f or d (Fig. 3 (a)) because of a reduction of the C_s charging time that causes a lower $V_{GS\,mean}$ value. Those effects are more significant when the C_s value is higher. Fig. 4 shows the power dissipation as a function of the main current I_T. As it can be derived, the power consumption of S_a remains almost constant along the I_T sweep.

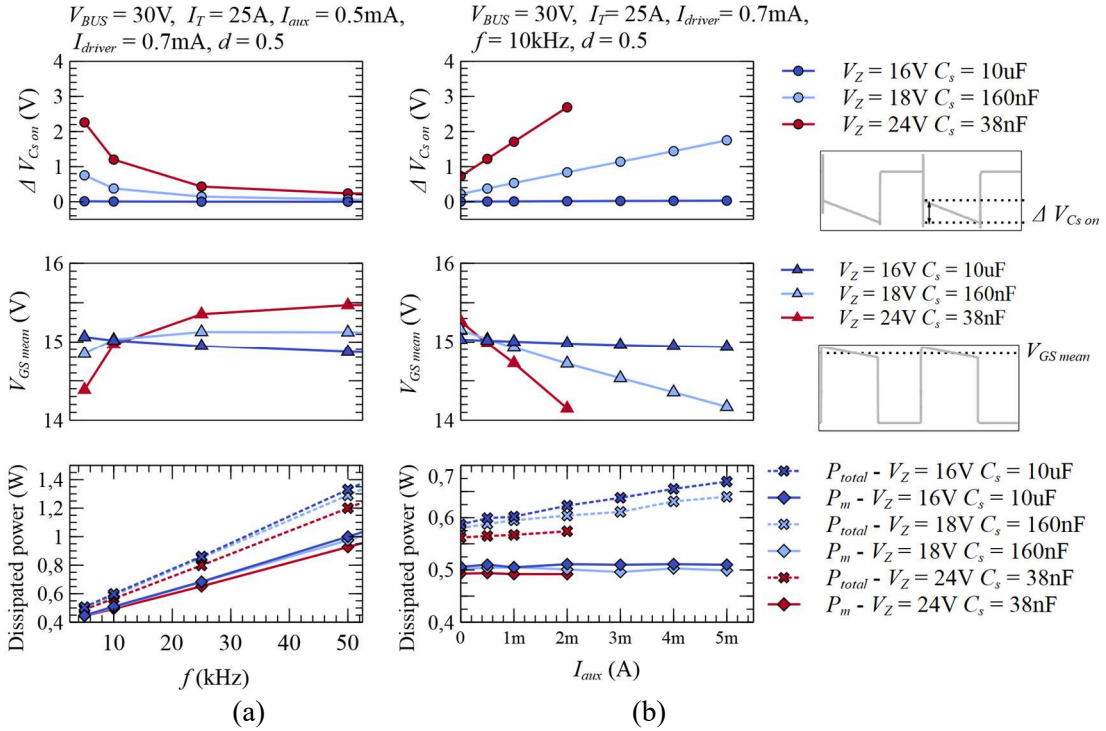


Fig. 3: Simulation of the IGDPS $\Delta V_{Cs\,on}$, $V_{GS\,mean}$ and power dissipation as a function of (a) I_{aux} and (b) f, for three combinations of V_z and C_s (24V – 38nF; 18V-160nF; 16V-10µF).

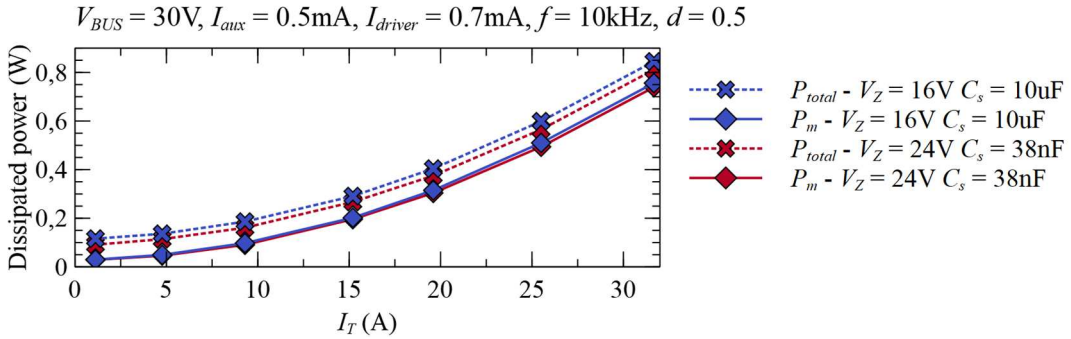


Fig. 4: Simulation of the (IGDPS) power dissipation (P_m: S_m losses; P_{total}: driver, S_a and S_m losses) as a function of main transistor current I_T for three combination of V_z and C_s (24V – 38nF; 16V-10µF).

Internal regulated gate driver power supply

Fig. 5 shows an improved version of the IGDPS circuit presented above, the Internal Regulated Gate Driver Power Supply (IRGDPS), which includes a voltage regulator between C_s and the gate driver. As mentioned before, the main reason for this modification is to achieve a constant and robust gate driver and auxiliary circuitry voltage supply. This approach facilitates the design of the gate driving and protection circuitry in elementary switching cells. The operation principle of the circuit concerning C_s charge remains unchanged, but the discharge process is controlled by the regulator. In the IRGDPS version, the voltage ripple at the gate driver supply voltage is drastically reduced for a wide range of C_s and switching frequency values and, in addition, the dissipation losses can also be significantly reduced in comparison with the lower ripple case of IGDPS (for the V_z-C_s combination16V-10µF).

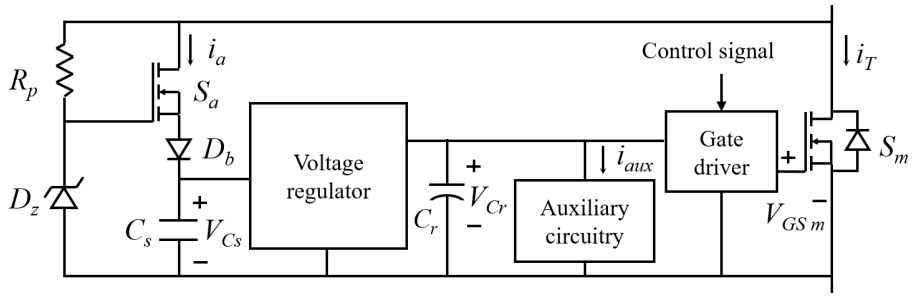


Fig. 5: Internal regulated gate driver power supply (IRGDPS) circuit schematic.

The selection of the voltage regulator is the main design issue of this circuit. A linear voltage regulator is easier to implement and requires less passive components but its losses and the increment of losses in the transistor S_a (due to the regulator high quiescent current) makes it unsuitable for the foreseen application. On the other hand, switching-mode voltage regulators can be considered for the IRGDPS due to their higher efficiency. **Table II** contains the most relevant components used in the simulation of the IRGDPS schematic. For the estimation of the total dissipated power, only the elements with a significant power consumption have been considered (S_m, driver, S_a and voltage regulator).

Unlike the IGDPS circuit, many combinations of capacitors and zener diodes can be implemented in order to achieve a suitable V_{Cs} supply voltage for the voltage regulator. In Fig. 6 (a), a C_s sweep has been performed for two different zener diodes, and it can be seen that the P_{total} (voltage regulator, driver, S_a and S_m) is reduced for zener blocking voltages close to V_{BUS}. Simulations reveal that the power consumption of S_a is drastically reduced while the driver and voltage regulator power consumption remains almost constant when increasing the zener blocking voltage.

A design constrain appears when V_{Cs} is lower than the minimum supply voltage of the voltage regulator, and this happens when C_s is too small, for example in Fig. 6 (a) for V_z=20V, C_s must be at

least 500nF to operate correctly. Fig. 6 (b), (c) and (e) depict a comparison between the power dissipation of the IRGDPS circuit with V_z = 27V and C_s=100nF and the IGDPS circuit with V_z = 16V and C_s=10µF (which is the case with minimum voltage ripple) when varying f, I_T and I_{aux}. The obtained results show that the P_m of the IRGDPS is similar to the 16V-10µF combination of the IGDPS circuit and the P_{total} is significantly reduced for wide ranges of f, I_T and I_{aux}. In this topology, the f, d and I_{aux} variations do not affect the $V_{GS\,m}$ value. In addition, the introduction of the voltage regulator reduces the C_s discharge current. Hence, the P_{total} is less dependent against the operating parameters and the C_s value.

Table II: Simulation parameters for the IRGDPS

Buck converter	L = 0.4mH,- V_{BUS}=30V
S_m	IPB015N04N (40V)
R_G	3Ω
Driver	1ED44175N01B
Voltage regulator	LT3991

D_b	RSX051VYM30 (30V)
V_z	TFZ--B
S_a	PMPB14XN (40V)
R_p	215kΩ
C_r	22µF
C_s	100nF

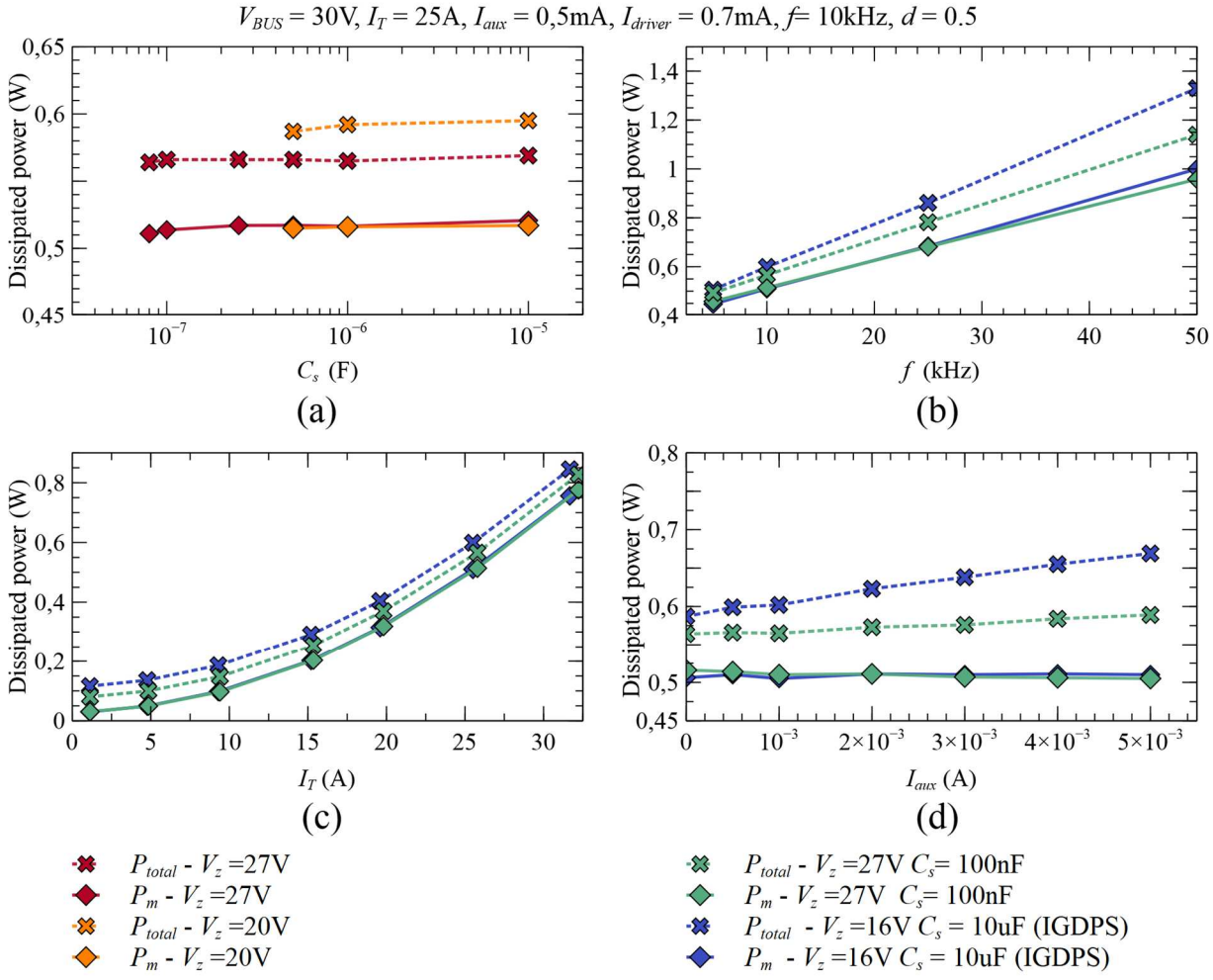
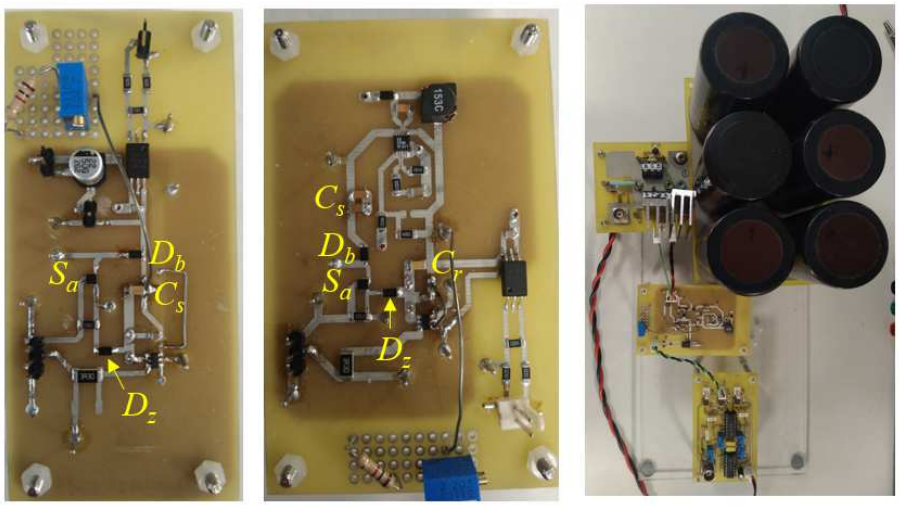


Fig. 6: Simulation of the IRGDPS power dissipation and comparison with IGDPS power losses (P_m: S_m power dissipation; P_{total}: voltage regulator, driver, S_a and S_m power dissipation) for: (a) C_s sweep, (b) f sweep, (c) I_T sweep, (d) I_{aux} sweep.

Experimental results

A conceptual validation and performance comparison among GDPS circuits (EGDPS, IGDPS and IRGDPS) has been experimentally studied in a test buck converter using a 70V MOSFET as the main

transistor S_m. The circuit parameters are shown in **Table III** and the experimental setup is shown in the pictures of Fig. 7. As the main objective of these tests was to demonstrate the main characteristics and trends predicted by simulation of the proposed IRGDPS solution, a similar power MOSFET reference was used as S_m. In order to compare the performances of the different circuits under the same conditions, the IGDPS and IRGDPS were designed in order to obtain $V_{GS\,mean}$ =14V and the lowest voltage ripple.



(a) (b) (c)

Fig. 7: Experimental setup pictures: (a) EGDPS and IGDPS, (b) IRGDPS, (c) Buck converter, IRGDPS and pre-driver stage.

Table III: Main components for the test buck converter and gate driver power supply circuits

	EGDPS	IGDPS	IRGDPS
Buck converter	L = 0.4mH, V_{BUS}=30V, Diode: MRB601000PT (100V, 60A)		
S_m	IXFH76N07-11 (70V, 76A)		
R_G	3Ω		
Driver	1ED44175N01B		
S_a	-	PMPB14XN (40V)	
D_b	-	SD101BW-E3-18 (50V)	
R_p	-	215kΩ	
V_z	-	16V	27V
C_s	-	10µF	430nF
C_r	-		22µF
Voltage regulator	-		LT3991

Driver and auxiliary circuitry supply voltage

Fig. 8 depicts the mean gate-source voltage $V_{GS\,m}$ and the driver supply voltage (V_{Cs} in IGDPS and V_{Cr} in IRGDPS) waveforms. At low frequency (Fig. 8 (a)), the IGDPS supply voltage shows a higher voltage drop during on-state of S_m ($\Delta V_{Cs\,on}$) which directly reduces the gate-source voltage. On the other hand, increasing the frequency (Fig. 8 (b)) has two effects on the capacitor voltage. First, it reduces the $\Delta V_{Cs\,on}$, and second, it reduces the maximum value of V_{Cs} (C_s is not fully charged). The IRGDPS is more robust working at low and high frequency (Fig. 8 (c) and (d)), in both cases, a minimum voltage ripple of V_{Cr} is achieved and the $V_{GS\,m}$ remains constant. Fig. 9 plots the mean gate source voltage ($V_{GS\,mean}$) and voltage drop of driver supply voltage (ΔV_{driver}) versus frequency for different auxiliary currents.

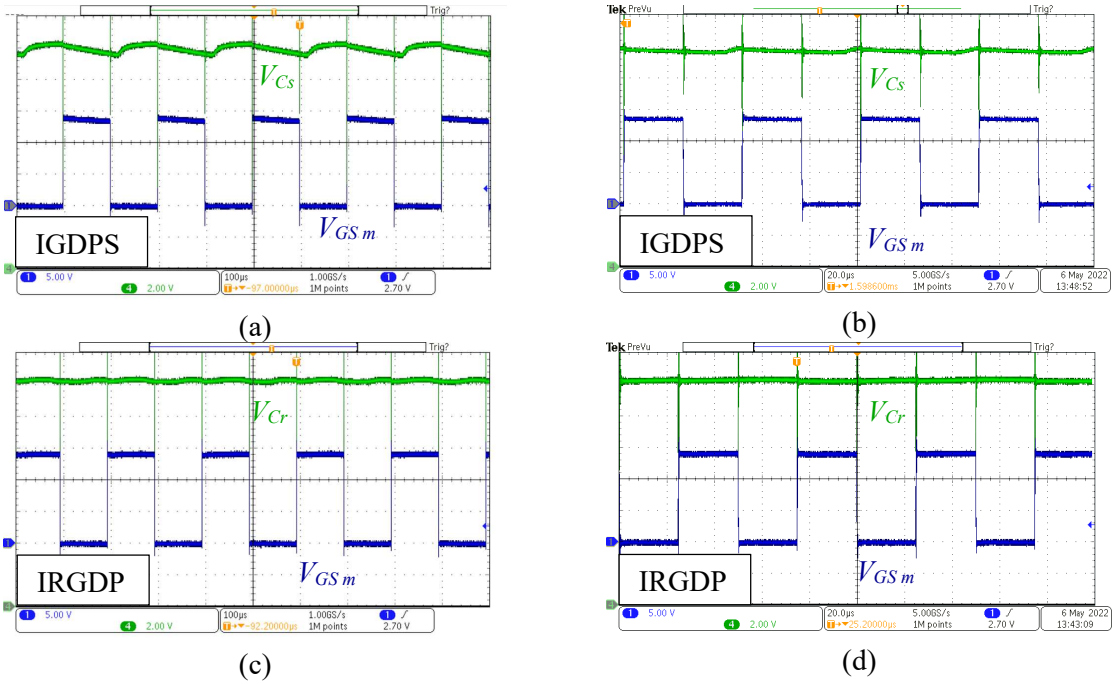


Fig. 8: Gate source voltage waveforms ($V_{GS\,m}$ in blue) and driver supply voltage (V_{driver} in green, V_{Cs} for IGDPS and V_{Cr} for IRGDPS) for: (a) IGDPS f = 5kHz, (b) IGDPS f = 20kHz, (c) IRGDPS f =5kHz, (d) IRGDPS f = 20kHz. All waveforms have been taken for V_{BUS} = 30V, I_T = 10A, I_{aux} = 14mA, d= 0.5.

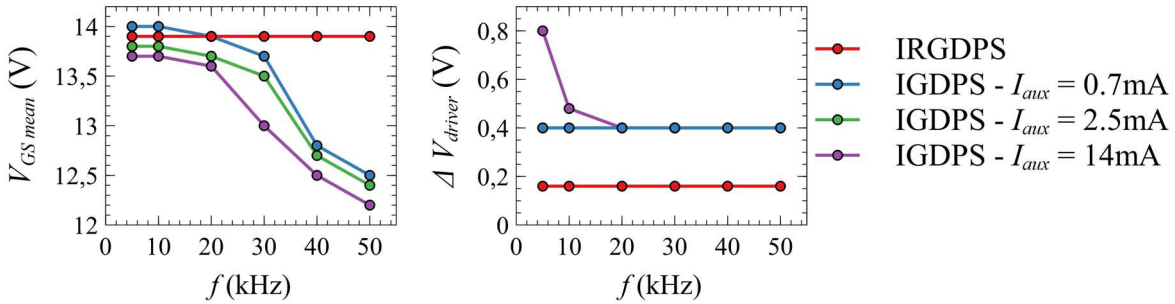
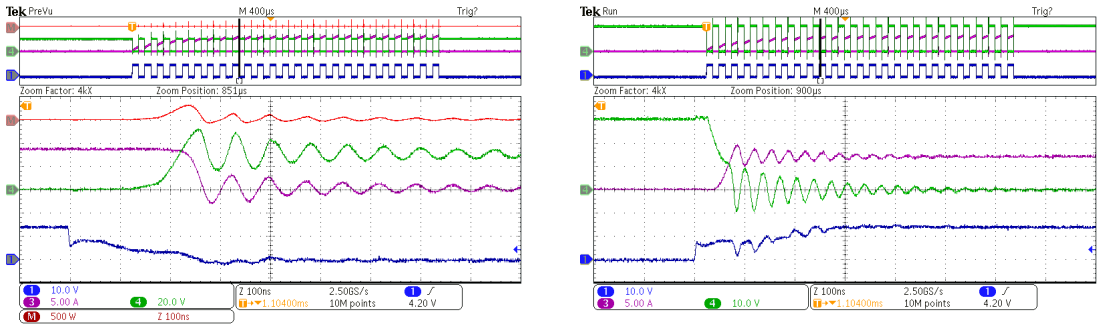


Fig. 9: $V_{GS\,mean}$ and ΔV_{driver} as a function of f, evidencing the superior behavior of the IRGDPS solution in a wide range of switching frequencies. All values have been taken for V_{BUS} = 30V, I_T = 10A, d= 0.5.

Power dissipation of the main transistor and gate driver power supply circuits

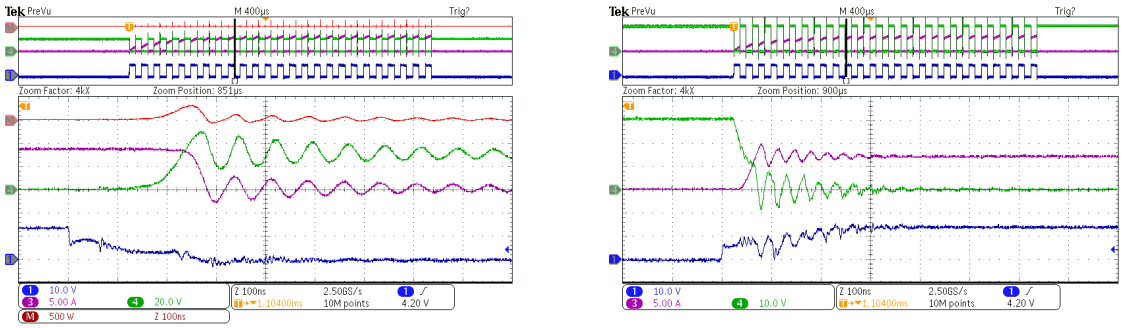
A comparative analysis of the power dissipation of S_m can be obtained from Fig. 10 (EGDPS), Fig. 11 (IGDPS) and Fig. 12 (IRGDPS) where the turn-off and turn-on processes are shown at different conditions and GDPS circuits. The duration of the whole switching process and power dissipation during the turn-off of the main transistor S_m of the self-powered solution are similar to the EGDPS solution (Fig. 10 (a), Fig. 11 (a), Fig. 12 (a) and (b)), although the IRGDPS presents less oscillations and a reduction of the power peak. Besides, in the IRGDPS option, when the auxiliary current increases the power dissipation and oscillations are slightly reduced. During the turn-on process with the EGDPS solution (Fig. 10 (b)), the gate-source voltage shows significant fluctuations caused mainly by the reverse recovery of the free-wheel diode of the buck converter. The self-powered circuits show also this behavior during the turn-on, possibly, enhanced by the turn-off of the auxiliary transistor S_a and the diode D_b (Fig. 11 (b), Fig. 12 (c) and (d)).

Finally, in order to study the power consumption distribution of the self-powered GDPS solutions, a thermography of the circuits working at different conditions is depicted in Fig. 13. An indirect method was selected to study the losses and their distribution among the different components since direct current measurement may alter their operation due to parasitic inductances. The thermographs show that as the auxiliary current increases, the dissipation of the GDPS increases, mainly at the auxiliary transistor S_a (hottest point) in both circuits. Nevertheless the lower S_a temperature obtained for the IRGDPS confirms the lower power dissipation already predicted by simulation for this solution.



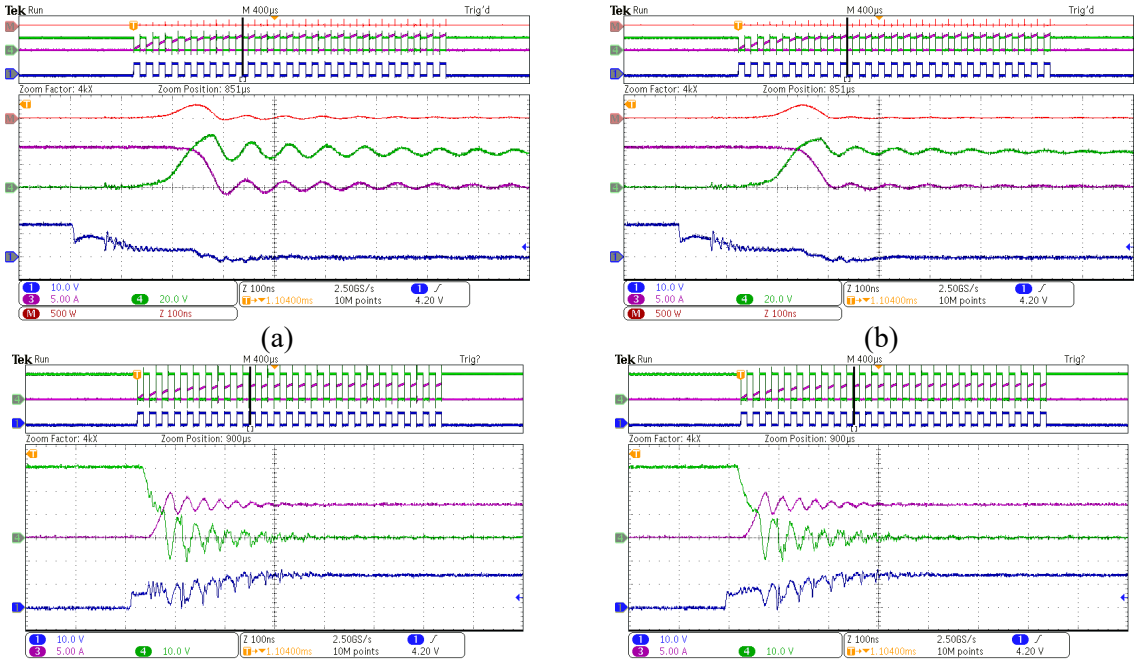
(a) (b)

Fig. 10: Switching waveforms ($V_{GS\,m}$ in blue, I_T in violet, $V_{DS\,m}$ in green, P_m in red) of EGDPS: (a) Turn-off process, (b) Turn-on process. All waveforms have been taken for V_{BUS} = 30V, f = 10kHz, d = 0.5.



(a) (b)

Fig. 11: Switching waveforms ($V_{GS\,m}$ in blue, I_T in violet, $V_{DS\,m}$ in green, P_m in red) of IGDPS: (a) Turn-off process I_{aux} = 14mA, (d) Turn-on process I_{aux} = 14mA. All waveforms have been taken for V_{BUS} = 30V, f = 10kHz, d = 0.5.



(a) (b)

(c) (d)

Fig. 12: Switching waveforms ($V_{GS\,m}$ in blue, I_T in violet, $V_{DS\,m}$ in green, P_m in red) of IRGDPS: (a) Turn-off process I_{aux} = 0.7mA, (b) Turn-off process I_{aux} = 14mA, (c) Turn-on process I_{aux} = 0.7mA, (d) Turn-on process I_{aux} = 14mA. All waveforms have been taken for V_{BUS} = 30V, f = 10kHz, d = 0.5.

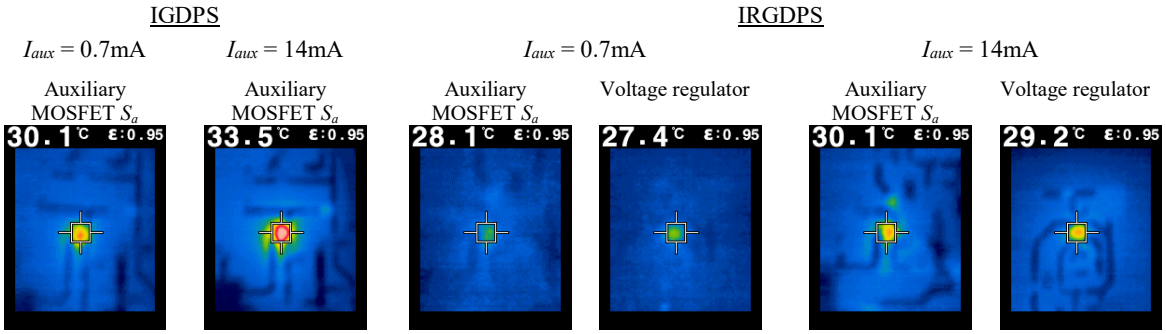


Fig. 13: Thermography of (a) IGDPS with I_{aux} = 0.7mA, (b) IGDPS with I_{aux} = 14mA, (c) IRGDPS with I_{aux} = 0.7mA, (d) IRGDPS with I_{aux} = 14mA. Lower dissipation of S_a is obtained for the IRGDPS.

Conclusion

The proposed IRGDPS circuit improves the main drawbacks of previous IGDPS schemes. It shows a big potential as a compact gate driver power supply solution for multilevel converters.

The simulation and experimental results have shown that the IRGDPS solution behaves as expected and its main operation conditions and constrains have been analyzed and compared with other options (IGDPS and EGDPS). Additional verifications have been carried out at different main current I_T and C_s capacitor values to verify that the experimental behavior corresponded to the simulated one.

The obtained supply voltage for the gate driver and auxiliary circuitry is stable for a wide range of frequencies and auxiliary current consumption. Power losses and switching times of the main transistor are unchanged while the consumption of the auxiliary switch required to ensure the C_s charge is reduced using the IRGDPS solution.

Present investigations are addressed towards the miniaturization of the proposed IRGPDS solution, its integration in smart power modules and the use of higher breakdown voltage devices and switching cells.

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