Current Limiter Circuit to Suppress Inrush Load Current for LVDC Distribution System

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***Abstract*-- This paper proposes an analysis of the inrush load current and a design of the inrush current limiter circuit for a low-voltage DC (LVDC) distribution system. Due to the absence of a zero-crossing point, large fault current during the connection of DC loads with a large input capacitor may cause severe problems in the LVDC distribution system including voltage drop on the DC bus and damage to the system. To analyze the necessity of a current limiter circuit, the voltage control system of a TAB converter for the LVDC distribution system is designed. The stability under the inrush current is analyzed through the small-signal modeling of the TAB converter. Also, the inrush current limiter circuit composed of a switch, a diode, and an inductor is proposed. To obtain the desired current suppression performance, the design methodology is presented. The validity of the proposed inrush current limiter is verified by a lab-level LVDC distribution system with a 4-kW TAB converter prototype.**

***Index Terms*-- Current Limiter, Inrush Current, LVDC Distribution.**

I. Introduction

Globally, for the common goal of carbon-neutral (net-zero-energy), the ratio of power generation to renewable energy sources is increasing. In the case of AC grids, an additional power conversion stage is required to link the DC-based renewable energy source that generates intermittent power. The additional power conversion stages decrease the efficiency of the entire power system and threaten the reliability of the grid. In addition, the AC resistance of the transmission line causes high power losses. To overcome those disadvantages, the interest in DC grids is growing. In particular, research on the Low-voltage DC (LVDC) grid applied to households, buildings, and data centers has actively been conducted [1]-[3].

Although many studies have been conducted so far, it is taking a long time to be commercialized due to the requirements of protection and safety, which are more severe than the AC grid. The characteristic feature of the DC grid is that large fault current flows during a short time due to the absence of a zero-crossing point. One of the reasons for generating such a fault current is the inrush current due to the capacitor connected in parallel, which is an essential energy storage component of the DC/DC converter. Most DC loads connected to the LVDC system include separated DC/DC converters, containing input capacitors. The input capacitor is essential at the input stage of each converter for stabilizing the DC input voltage level. High capacitance

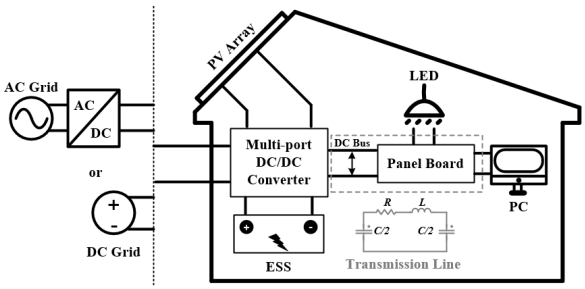


Fig. 1. Schematic of a LVDC distribution system based on the multi-port DC/DC converter.

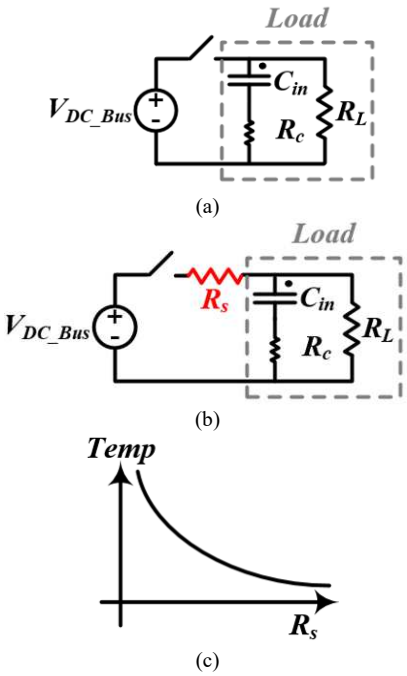


Fig. 2. Generation mechanism of the inrush current: (a) Circuit diagram of inrush current generation, (b) Suppression by thermistor, (c) Characteristics of thermistor according to operating temperature and resistance.

reduces voltage ripple, but may cause high inrush current resulting in voltage drop on the DC bus, and damaging the load. If the voltage drop is severe, it may reset or even damage the other devices connected to the LVDC system.

Several studies have been conducted to reduce the inrush current [4]. In [5],[6], they pointed out the disadvantages of the inrush current limiting method using the thermistor. The suppression performance of the current limiter changes according to the temperature of the thermistor. Therefore, increased temperatures of the

thermistor due to repeated initial start-ups can worsen the suppression performance of the inrush current limiter. Also, it causes high power loss due to its turn-on resistance.

To solve those issues, a switch-mode power supply (SMPS) is adopted. In [5], the current limiter operates under a high switching frequency of 300 kHz to reduce inrush current based on current-mode control. High switching frequency operation can reduce the size of the passive element used in the SMPS. However, it causes high switching loss, and high-speed switching devices are required, which increases production costs. In [6], the DC outlet with an additional control pin is proposed. The duty ratio of the power switch increases or decreases depending on whether the control pin is connected. It can limit the transient current and voltage during the connection and disconnection of the outlet.

In [7], a hiccup startup strategy using short pulses under the linear operation range of the power switch is proposed. The moment the energize pin is connected, a low gate to source voltage close to the threshold voltage of the switch is applied to operate under the linear operation region. In contrast, the energize pin is first disconnected before the positive and negative poles during its disconnection to limit the voltage spike under the disconnection. However, limiting the inrush current in the linear operation mode of the switch causes high power loss due to the turn-on resistance. It can lead to reliability problems due to the heat generation of the power switch.

Although the above studies present the operating principle and structure of the proposed inrush current limiter, it increases the cost of the overall system or causes reliability problems due to heat generated by continuous use. In particular, the proposed inrush current reduction methodologies do not discuss the detailed design of circuit components constituting the inrush current limiter. Therefore, the presented inrush current suppression performance can be different depending on the design. In addition, in the absence of such a methodology, excessive design to suppress inrush current can increase the overall system volume.

In this paper, a current limiter circuit to suppress the inrush current is proposed for the residential LVDC distribution system composed of a multi-port-based distribution network. A triple-active-bridge (TAB) DC/DC converter is configured as a distribution network. The inrush current caused by the input capacitance of the load connected to the distribution network is analyzed in detail. A small-signal model analysis of the distribution network considering the line impedance is conducted and the necessity of additional current limiter circuits is discussed. As a result, an inrush current limiter circuit composed of a switch, a diode, and an inductor is proposed. To obtain the desired current suppression performance, the design methodology is presented. Finally, the validity of the proposed inrush current limiter is verified by a lab-level LVDC distribution system with a 4-kW prototype TAB DC/DC converter.

II. LVDC Distribution System

A. Basic Structure

The multi-port converter can integrate various distribution network components into a single converter. It requires fewer converters in complex grid systems, reducing component count and achieving high power density. In addition, a single controller can control multiple components. In this paper, a multi-port converter-based residential LVDC distribution system including those advantages is a target application. It can be represented as shown in Fig. 1.

Electric power is transferred to the residential LVDC distribution system through the multi-port DC/DC converter connected to the existing AC grid or DC grid. The multi-port DC/DC converter integrates a renewable energy source (PV), and an ESS to support domestic loads. It allows the distribution network within the home to be simple and small. In the case of domestic loads such as LED and PC, electric power is supplied by a panel board through a transmission line. The panel board branches power from the DC bus.

B. Inrush Current Issue

Unlike the AC grid, the DC grid does not have a zero-crossing point. Therefore, when a fault current occurs, the current magnitude is huge and lasts for a short time. One of the reasons for generating such a fault current is the inrush current caused by high load capacitance. The domestic loads connected to the panel board in Fig. 1 include an input capacitor for maintaining stable input voltage. When the capacitor with a high capacitance value is used, for a low voltage ripple that is, the high-quality input voltage can be obtained. However, this capacitor can damage power converters and loads connected to the dc-bus by inducing a high inrush current when the load is connected.

The power distribution network connected to the load can be represented as an equivalent circuit shown in Fig. 2 (a). When the DC bus voltage is supplied through the panel board during the initial startup, a high inrush current is induced due to the instantaneous voltage charging of the input capacitor. To limit the inrush current, a thermistor (R_s) with negative temperature coefficient (NTC) resistance is mainly used as shown in Fig. 2 (b). In Fig. 2 (c), it has a high resistance at low temperatures, so it can limit the inrush current that occurs during the cold start process. In addition, it conducts current with low resistance due to the increased temperature after the start-up. However, due to the NTC resistance characteristic, the inrush current limitation performance cannot be guaranteed due to the increased temperature of the resistor under repeated ON/OFF conditions [4]. Therefore, active inrush current limitation methods are required rather than the passive thermistor method.

TABLE I
PARAMETERS OF THE VOLTAGE CONTROL LOOP OF THE TAB CONVERTER

Parameter		Value
PI Controller	P Gain	0.15
	I Gain	35
Low-Pass Filter	Cut-Off Frequency	5.1 kHz
Cross-over Frequency		89.4 Hz
Phase Margin		58.6°

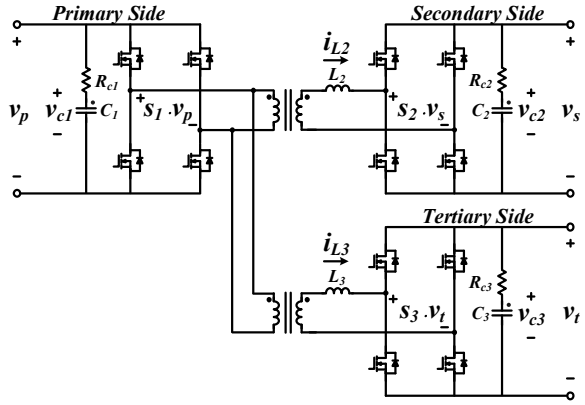


Fig. 3. TAB converter for the residential LVDC distribution system.

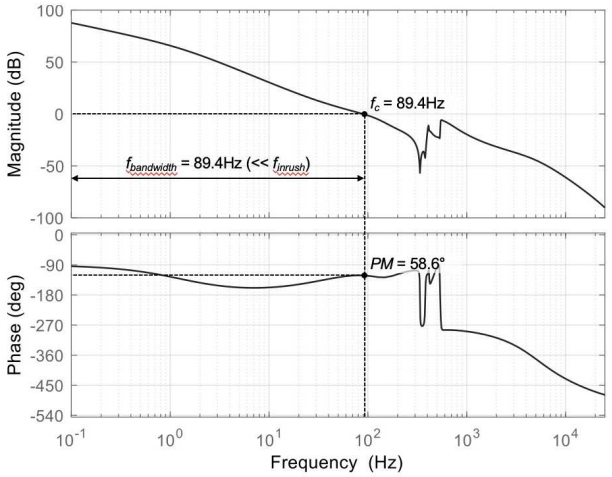


Fig. 4. Bode plot of the voltage control loop and its control bandwidth of the TAB converter.

III. ANALYSIS OF SUPPLY CURRENT CONTROLLED BY POWER CONVERTER

Fig. 3 shows the schematic of a TAB converter for the residential LVDC distribution system. To analyze the impact of the inrush current on the DC bus voltage regulation performance conducted by the control system of the TAB converter, the small-signal analysis is an effective tool. By comparing the harmonics of the inrush current and the bandwidth of the control loop calculated by the small-signal model, control stability under the occurrence of the inrush current is analyzed. The parasitic impedances from the practical LVDC distribution system is considered for the accuracy of the analysis.

TABLE II
CIRCUIT PARAMETERS OF THE TAB CONVERTER

Parameter	Value	Parameter	Value
Input Voltage	380 V	Coupling Inductance	123.7 uH
Output Voltage	380 V	Input and Output Capacitance	470 uF
Power	2 kW per Port	Turn Ratio	1:1
Switching Frequency	50 kHz		

TABLE III
THE IMPEDANCE OF THE DC LOAD AND TRANSMISSION LINE

	Parameter	Value		Parameter	Value
DC Load	P_{in}	2 kW	Transmission Line (100 m)	R	1.27 mΩ
	R_L	72.2 Ω		L	93.37 uH
	C_{in}	1200 uF		C	1.274 mF

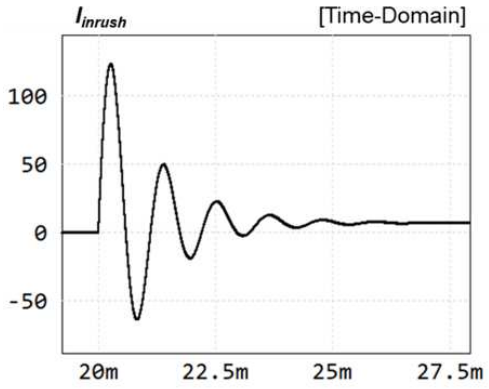
A. Small-Signal Model of TAB Converter

The state variables of the TAB converter's small-signal model include currents i_{L2} and i_{L3} of the coupling inductors, and voltages v_{c2} and v_{c3} of the filter capacitors on the secondary and tertiary sides, respectively. The voltage polarities applied to the transformers and the coupling inductors are periodically changed by full-bridge switching operations. These are expressed as switch functions in differential equation forms. A small-signal model is derived by taking the Fourier Transform to each term of the differential equation, obtaining a generalized average model (GAM)[8]. The s-domain transfer function is used as the load in the modeling, unlike using a dc resistance of an ideal converter, to consider the dynamic characteristics of the transmission line impedance. The loop gain frequency response from the control-to-output voltage small-signal model is shown in Fig. 4. The voltage control loop gain of the TAB converter can be represented as follows: where G_{vd} (s) is the control-to-output voltage small-signal model, F_{PI} (s) is the PI controller, and F_{LPF} (s) is the low-pass filter.

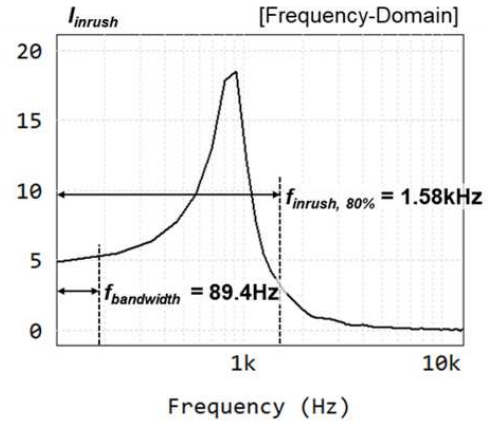
$$T(s) = G_{vd}(s) \cdot F_{PI}(s) \cdot F_{LPF}(s) \tag{2}$$

$$F_{PI}(s) = K_p + \frac{K_i}{s} \tag{3}$$

$$F_{LPF}(s) = \frac{{\omega_c}^2}{s^2 + \zeta\omega_c s + {\omega_c}^2} \quad (\zeta = 0.7,\ \omega = 2\pi f_c) \tag{4}$$



(a)



(b)

Fig. 5. Inrush current waveforms: (a) Time-domain showing the oscillation, (b) Fast Fourier transformed frequency-domain waveform showing the harmonics.

The PI gains are set to achieve 58.6° of phase margin and 89.4 Hz of cross-over frequency, and the cut-off frequency is set to 5.1 kHz.

B. Stability under Inrush Current

Inrush current can be represented as a step-input disturbance to the output voltage of the TAB converter. The step-input signal consists of various multiple-order frequencies, and only limited frequency components are attenuated by the closed-loop control depending on its performance.

In the case of the output voltage-controlled TAB converter for LVDC distribution applications, the frequency range of the disturbance that can be attenuated is limited to the control bandwidth of the voltage control loop transfer function. Compared with the control bandwidth of the TAB converter, the inrush current waveform has incomparably wide harmonic ranges. Fig. 5 (a) shows the inrush current when the load is connected to the DC bus through the transmission line. Fig. 5 (b) shows the frequency response of Fig. 5 (a), which means that 80% of the harmonics are distributed within 1 Hz to 1.58 kHz frequency range. It is wider than the control bandwidth.

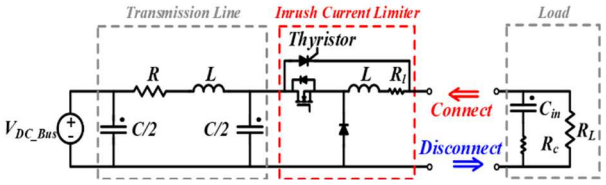


Fig. 6. Circuit diagram of the residential LVDC distribution system based on the multi-port DC/DC converter and the proposed inrush current limiter.

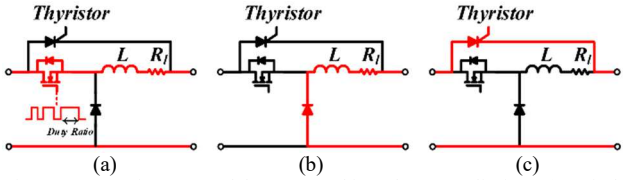


Fig. 7. Operating steps of the proposed inrush current limiter (a) Switch ON, (b) Freewheeling, (c) Thyristor ON.

The analysis indicates that the voltage regulation of the TAB converter's voltage controller is not effective enough for the voltage regulation under the occurrence of the inrush current. Therefore, an additional device that can limit the inrush current is inevitable, and an inrush current limiter is proposed in the next section to prevent this phenomenon.

IV. Proposed Inrush Current Limiter

A. Analysis of the Current Limiter

Fig. 6 shows the configuration of the proposed inrush current limiter which consists of a power switch, a freewheeling diode, an inductor, and a bypass thyristor. It connects the transmission line and the load and operates when the load turns on.

Fig. 7 shows the operating steps of the proposed inrush current limiter. The input capacitor of the load should be gradually charged to reduce the inrush current. So the switch repeats being turned ON and OFF with increasing its duty ratio gradually. The freewheeling diode is additionally configured to maintain the continuity of the inductor current when the switch turns off. At that time, the current freewheels through the diode. If the duty cycle of the switch reaches one, after waiting for the load capacitor voltage to reach the maximum near the DC bus voltage, the thyristor is turned on. The bypass thyristor is used for reducing conduction loss of the power switch and the inductor under the load-connected condition.

B. Design Methodology

Under the turn-on process, the inductor current is divided into continuous conduction mode (CCM) and discontinuous conduction mode (DCM) according to the charged voltage level of C_{in}. The voltage applied to the inductor can be large enough to go under DCM operation when the charged voltage is sufficiently low.

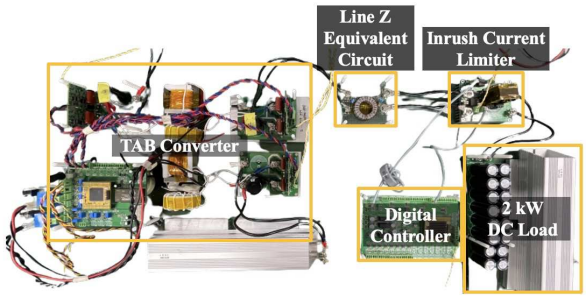


Fig. 8. The prototype of the proposed inrush current limiter

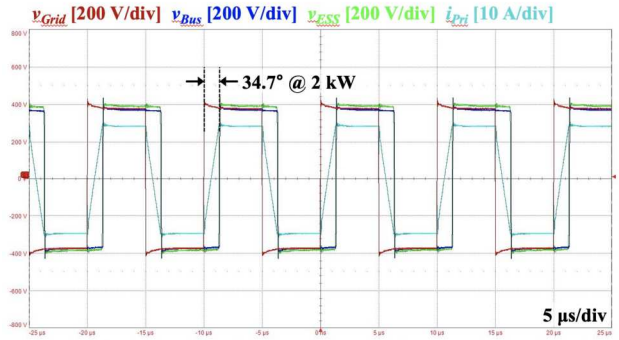


Fig. 9. Operation waveform of the 4 kW TAB converter prototype.

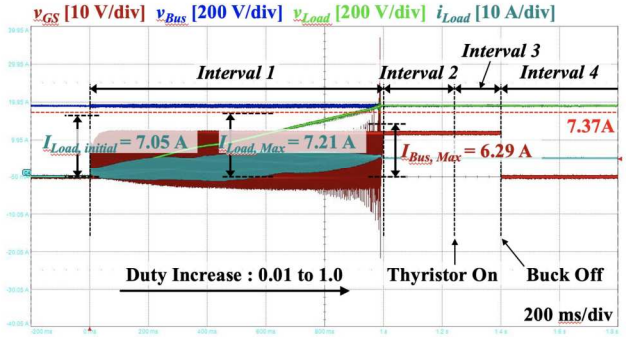


Fig. 10. Operation waveform of the proposed inrush current limiter showing the voltage and current of the DC bus and load.

After that, as the voltage is gradually charged, it goes to a CCM operation.

They are expressed as follows:

$$I_{peak\_DCM} = \frac{V_{in} - V_L}{Lf_s} D \tag{1}$$

$$I_{peak\_CCM} = \frac{DV_{in}}{R_L} + \frac{V_{in} - DV_{in}}{2Lf_s} D \tag{2}$$

where I_{peak_DCM} is the peak current under the DCM operation, I_{peak_CCM} is the peak current under the CCM operation, and fs is the switching frequency. It is advantageous to operate at a higher switching frequency because the higher the switching frequency, the lower the peak current under both the DCM and CCM operations.

V. Experimental Results

The performance of the proposed inrush current limiter has been verified by an experiment. A 4-kW TAB converter prototype has been used as a multi-port converter for the residential LVDC distribution system which has two outputs: one connected to the DC bus, and the other one connected to the ESS. The proposed inrush current limiter is connected between the transmission line equivalent circuit and the DC load, which consists of a 1.2 mF input capacitor and 2 kW resistive load as shown in fig. 8. Parameters of the converters and the transmission line equivalent circuit are specified in Table II and III.

Fig. 10 shows the operation waveform of the proposed inrush current limiter. The inrush current operates with 4 intervals. During interval 1, the inrush current limiter starts to operate, increasing the buck converter duty cycle from the initial duty of 0.005 to 1.0. The input capacitor of the DC load is slowly charged, and if the DC load voltage reaches the DC bus voltage 380 V with 1.0 duty cycle, interval 1 ends. During interval 2, the buck converter maintains its duty to 1.0, and the thyristor is turned on at the start of interval 3. The current flowing in the inrush current limiter is bypassed from the buck converter to the thyristor, due to the parasitic resistance of the MOSFET and the inductor. In interval 4, the MOSFET of the buck converter is turned off and only the thyristor supplies the power, preventing the voltage spike under sudden disconnection of the DC load.

VI. Conclusions

In this paper, the inrush load current is analyzed and the design methodology of the inrush current limiter circuit for the LVDC distribution system is proposed. The voltage controller of the TAB converter for the LVDC distribution system and its stability under the occurrence of inrush load current is analyzed to verify the necessity of the current limiter circuit, through the small-signal modeling of the TAB converter. An inrush current limiter circuit composed of a switch, a diode, and an inductor is proposed. To obtain the desired current suppression performance, the design methodology is presented. The experiment with the 4-kW TAB converter prototype is conducted to verify the proposed inrush current limiter circuit, showing the maximum Load and DC bus current of 7.21 A, which is lower than the design criteria of 7.37 A.

Acknowledgment

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