Adaptive Resonant-Valley Switching for a GaN HEMT Direct AC-AC Auxiliary Resonant Commutated Pole Converter

Kyle Steyn*, Johan Beukes†
Department of Electrical and Electronic Engineering
University of Stellenbosch
Private Bag X1, Matieland, 7602
Stellenbosch, South Africa
* Email: 18171869@sun.ac.za, † Email: jbeukes@sun.ac.za

Keywords

≪AC-AC converter≫, ≪Adaptive control≫, ≪HEMT≫, ≪Resonant converter≫, ≪ZCZVS converters≫.

Abstract

Zero-voltage zero-current switching is not guaranteed with auxiliary resonant commutated pole (ARCP) based topologies. The optimal dead-time is dependant on various parameters and cannot easily be calculated in real-time. A control technique that ensures all phase-arm switches turn on during the first resonant valley is presented. The voltage across one phase-arm switch is sampled during a turn-on transition and stored. The samples are processed by an adaptive zero-crossing algorithm and the optimal dead-time for the next switching cycle is predicted. The proposed technique was validated during a load-transient and at steady-state in simulation and experimentally on a 5-kW direct ac-ac ARCP prototype.

Introduction

The auxiliary resonant commutated pole (ARCP) [1] is a controllable resonant circuit that is added to the phase-arm of a converter. The ARCP is activated during the phase-arm deadband via an auxiliary switch, causing the load current to transfer from the phase-arm to the auxiliary circuit. Once fully transferred, the auxiliary inductor and capacitors begin to resonate, resulting in the oscillation of the phase-arm pole voltage. If timed precisely, the phase-arm switch can turn on during a resonant valley and achieve zero-voltage zero-current switching (ZVZCS). If the resonant valley is missed, ZVZCS will not occur, and the energy stored in the auxiliary capacitors will be dissipated in the phase-arm switch.

The ARCP is controlled by adjusting the phase-arm dead time. Control techniques include fixed [2], load-current-based lookup table [1], equation-based estimation [3], input bus midpoint-voltage monitoring [4], and analog comparator-based zero-voltage detection (ZVD) of the phase-arm switches [5, 6, 7].

The dead time for ZVZCS is predominantly dependant on the input voltage, load current and auxiliary component values; therefore, a fixed dead-time would rarely achieve ZVZCS. Lookup table and estimation techniques require exact knowledge of the auxiliary component values and precisely timed measurements. Propagation delay in analog ZVD circuits results in the late detection of a zero-voltage state. This becomes problematic when the resonant frequency is high and timing-error tolerance low.

An adaptive zero-crossing (AZC) technique that ensures ZVZCS regardless of the input voltage, load current, propagation delay and resonant component values is presented. The voltage across one phase-arm switch is oversampled uniformly by a high-speed analog-to-digital converter (ADC) during each turn-on transition. The samples are used by an adaptive controller on a field-programmable gate array (FPGA) to calculate the dead time for the subsequent switching transition. The technique results in a dead time that rapidly converges to the optimal value at the first resonant valley.

The Direct AC-AC ARCP Converter

Topology Overview

The operation of the ARCP will be examined using the full-bridge direct ac-ac topology seen in Fig. 1.

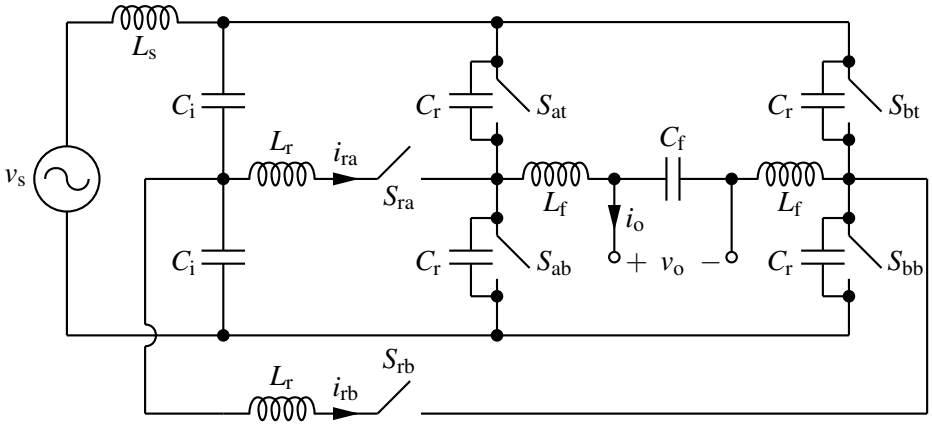


Fig. 1: Full-bridge direct ac-ac ARCP converter topology.

v_s and L_s represent the ac source, C_i the input capacitors, L_r and C_r the resonant inductors and capacitors, L_f and C_f the output filter, and v_o the converter output. Phase-arm switches are labelled S_{xy} and auxiliary switches S_{rx}, where x represents the connected phase-arm and y the bus. Each switch consist of two gallium nitride (GaN) high-electron-mobility transistors (HEMTs) in a common-source configuration.

Operating Principle

Using bipolar pulse-width modulation for the phase-arm switches, $i_{ra} = -i_{rb} = i_r$ and $S_{ra} = S_{rb} = S_r$. The operating states and waveforms during the turn-on of S_{at} & S_{bb} while in quadrant 1 can be seen in Fig. 2.

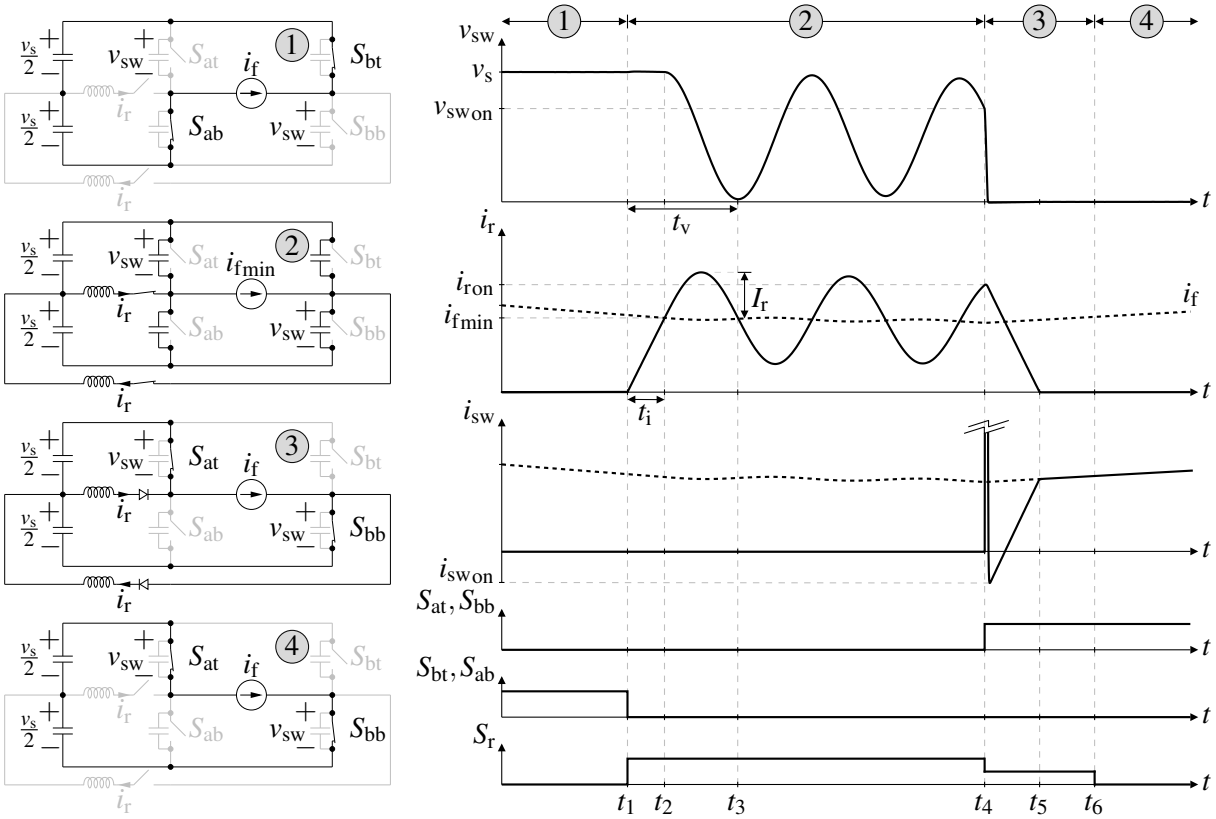


Fig. 2: Operating states and waveforms during turn-on of S_{at} & S_{bb}.

During ① the converter is near the end of the previous inverted-output state. The converter transitions to the deadband state ② where the filter current (i_f) reaches a minimum (i_{fmin}). The auxiliary switches (S_r) are activated at t_1 and the resonant inductor current (i_r) rises linearly until L_r fully conducts i_{fmin} at t_2. L_r and C_r resonate and the voltage at both phase-arm poles oscillate at the natural resonant frequency (f_r). To achieve ZVZCS, S_{at} & S_{bb} should turn on during the resonant valley at t_3. If the resonant valley is missed and S_{at} & S_{bb} turn on at t_4 for example, the charge in C_r would cause the transistors to turn on in the saturation region with high stress and power loss. The large peak current is combined with $i_{swon} = i_{fmin} - i_{ron}$ due to excess energy stored in L_r. S_r operates in diode mode during ③ to allow L_r to demagnetize and can be deactivated at t_6 (any time after t_5) without affecting the converter output ④.

Control Limitations

The dead time would have to be equal to t_v for the phase-arm switches to achieve ZVZCS. An estimation of t_v can be obtained by combining the current rise time (t_i) with half the resonant period as in (1).

$$t_v = t_i + \frac{1}{2f_r} = 2\,L_r \frac{i_{fmin}}{v_s} + \pi\sqrt{2\,L_r C_r} \tag{1}$$

Since v_s is sinusoidal and i_{fmin} is dependant on the duty cycle (D) and value of L_f, a fixed dead-time could only achieve ZVZCS with a resistive load at a constant duty cycle. This is provided that the exact values of L_r and C_r are known and remain constant under all operating conditions. Estimation techniques sample v_s and i_{fmin} and calculate the dead time every switching cycle using (1). Precise timing is required to effectively sample i_f at i_{fmin}. Alternatively, the load current (i_o) or the average value of i_f could be sampled and the steady-state dead-time estimated using additional converter parameters as in (2).

$$t_v = 2\,L_r \left[\frac{i_o}{v_s} - \frac{D(1-D)}{2\,L_f\,f_{sw}}\right] + \pi\sqrt{2\,L_r C_r} \tag{2}$$

The exact values of L_r and C_r are still required and drift in f_r cannot be detected. Analog techniques, such as comparator window-detection, solve the problem by detecting when the phase-arm switch voltage (v_{sw}) is within a set threshold (V_{th}). This can compensate for f_r drift but is sensitive to propagation delay.

Adaptive Zero-Crossing

The AZC technique utilizes one voltage sensor, consisting of a high-speed ADC, to sample v_{sw} and an FPGA to execute the control algorithms. The AZC controller consists of two algorithms, one for late turn-on and one for early turn-on conditions. A late turn-on occurs when the load current is decreased from steady-state, conversely, early turn-on occurs when the load current is increased from steady-state. The algorithms can be described using an illustration of the samples of v_{sw} during each switching cycle. The samples of v_{sw} during the late turn-on of S_{at} & S_{bb} for three switching cycles can be seen in Fig. 3.

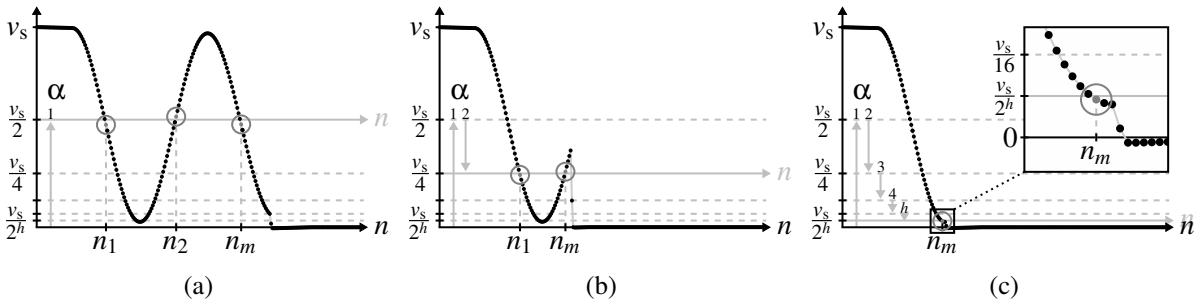


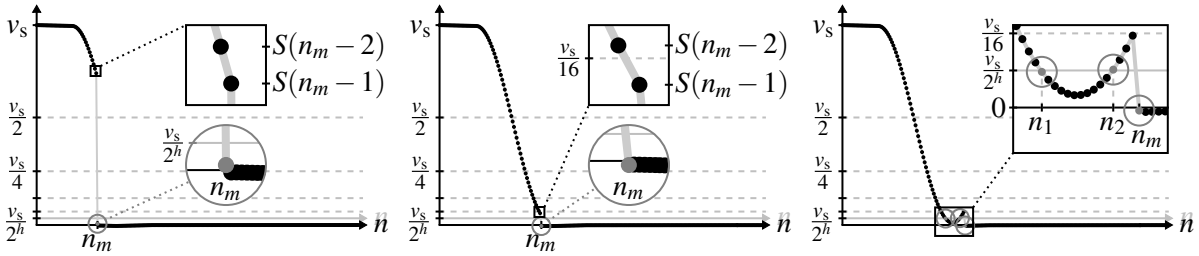
Fig. 3: Samples of v_{sw} during a late turn-on condition. (a) 1st, (b) 2nd and (c) 3rd switching cycle.

A set number of samples (N_{sample}) of v_{sw} are taken during the turn-on transition of S_{at}. The first sample is used to determine the value of v_s, then $\frac{v_s}{2}$ is subtracted from all subsequent samples to center the waveform at zero (Fig. 3a). The subtraction is illustrated as a shift in the x-axis for simplicity (e.g. the

x-axis shifts to $\frac{v_s}{2}$ in Fig. 3a). The samples are iteratively searched for a sign change, indicating a zero-crossing. The zero-crossing sample index (n_i) and total count of zero-crossings (m) are stored. If $m > 1$ then the switch did not achieve ZVZCS and the dead time (t_d) for the next cycle is calculated using (3).

$$t_d(k+1) = t_d(k) - \left[\sum_{i=2}^{m}(n_i - n_{i-1}) - \frac{n_2 - n_1}{2}\right] T_{sample} \tag{3}$$

If $m \leq 1$, it is possible that the resonant oscillation was undetected. The x-axis can be shifted down by a further $\frac{v_s}{4}$ and the zero-crossings re-evaluated (Fig. 3b). To generalize, the x-axis can be shifted by $\frac{v_s}{2^\alpha}$, where α represents a halving parameter $\alpha \in \{1, \ldots, h\}$ with halving limit h. At the start of each cycle, α is reset to 1 and is only incremented each time $m \leq 1$. For $\alpha = 1$ the x-axis is shifted up and for $1 < \alpha \leq h$ the x-axis is shifted down. If $m > 1$, then (3) is repeated and the converter proceeds to the next cycle. If the halving limit is reached and $m \leq 1$ (Fig. 3c), it is assumed that either ZVZCS occurred, or S_{at} turned on too early. An illustration of the algorithm during an early turn-on condition can be seen in Fig. 4.



(a) (b) (c)

Fig. 4: Samples of v_{sw} during an early turn-on. (a) 1st and (b) 2nd switching transition. (c) Overshoot.

$S(n_m - 1)$ represents the value of the sample at $n = n_m - 1$. To differentiate between ZVZCS (Fig. 3c) and an early turn-on (Fig. 4a), the value of the samples before n_m can be used to determine how many T_{sample} should be added to t_d. Since the switch is on at $n = n_m$, the previous sample $S(n_m - 1)$ would be an estimate of the turn-on voltage, and the difference between $S(n_m - 2)$ and $S(n_m - 1)$ would indicate the voltage rate-of-change before turn on. The ratio of these values can be used to update t_d as in (4).

$$t_d(k+1) = t_d(k) + \left[\frac{S(n_m - 1)}{S(n_m - 2) - S(n_m - 1)}\right] T_{sample} \tag{4}$$

The ratio is an estimation of the amount of T_{sample} required to move $S(n_m - 1)$ to zero. The ratio decreases as $S(n_m - 1)$ approaches the resonant valley (Fig. 4b), thereby preventing over-compensation. If t_d is increased by too much (Fig. 4c), the resonant oscillation will be detected and (3) will ensure stability.

The controller effectively assumes that S_{at} turned on at the last zero-crossing (n_m). For (3), the amount of samples between n_m and the center of the first two zero-crossings (the valley) is calculated and multiplied by the sample period (T_{sample}). In (4), the ratio of the samples determine how many T_{sample} to increase t_d by. Since the load dynamics are slower than the switching frequency (f_{sw}), t_d is able to converge to t_v.

Simulation

The AZC controller was simulated in MATLAB Simscape with ac-ac converter parameters in Table I.

Table I: Converter and Simulation Parameters

Parameter	Value	Parameter	Value	Parameter	Value	Parameter	Value
P_s	5 kW	C_i	20 µF	h	5	L_f	110 µH
V_s	230 V	D	75%	T_{pd}	100 ns	C_f	1.5 µF
I_s	21.74 A	f_{sw}	100 kHz	N_{sample}	250	L_r	3.6 µH ±10%
L_s	230 µH	V_{th}	15 V	T_{sample}	10 ns	C_r	4.7 nF ±10%

Load-Transient Performance

The dynamic response of the AZC is evaluated using a load step-up and step-down from steady-state by examining v_{swon}. The results are compared with existing control techniques and can be seen in Fig. 5.

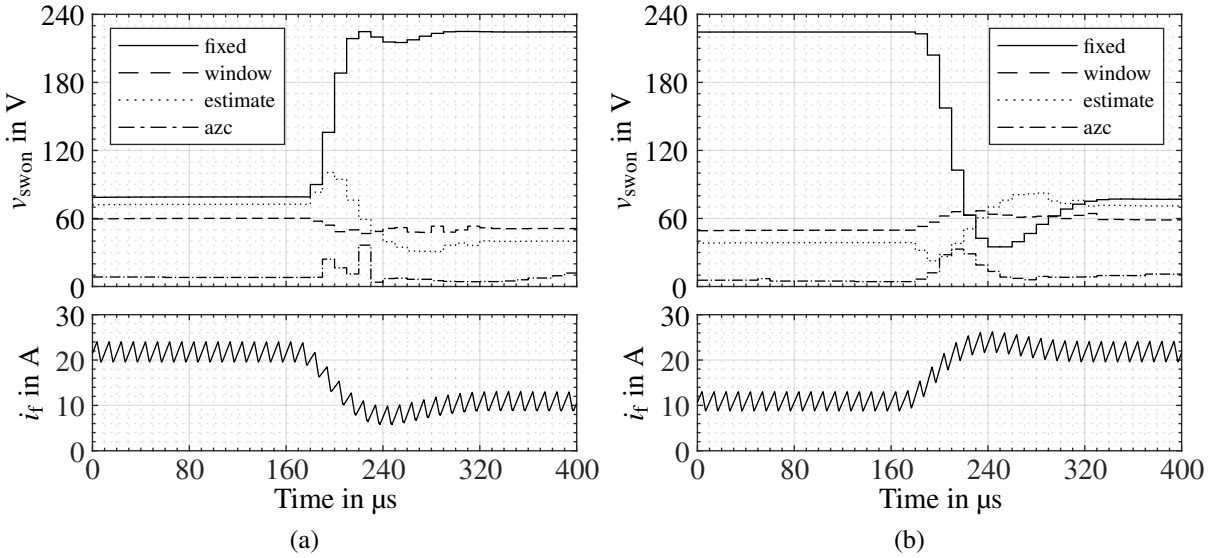


Fig. 5: Load step-response comparing control techniques. Load (a) decreased and (b) increased.

v_{s} is substituted with a dc source of value V_{s} and the converter operates with a constant duty-cycle (D). A tolerance of 10% is applied to L_{r} and C_{r}, and propagation delay (T_{pd}) is added to all sensors. For fixed control, t_{d} is chosen at rated load using (1). For estimated control, t_{d} is calculated each cycle using (2).

Fixed control performed the worst, taking thirteen cycles during step-down (Fig. 5a) and sixteen cycles during step-up (Fig. 5b) to settle. This is mainly due to the dependence of t_{v} on the load current. Estimated control performed the second worst, taking nine cycles during step-down/up. This is mainly due to the reliance of t_{i} on the value of L_{r}. The AZC performed the second-best, taking one cycle during step-down and four cycles during step-up to settle. The comparator window-detector performed the best, taking zero cycles during step-down/up to settle. This is due to V_{th} not being affected by the load current.

Voltage Sensor

The effect of sensor bandwidth and sampling rate on AZC performance was investigated by examining the rms of the turn-on voltage (v_{swon}) over one 50 Hz ac cycle for various ratios of sensor bandwidth (Fig. 6a) or sampling frequency (Fig. 6b) to resonant frequency (f_{r}). The results can be seen in Fig. 6.

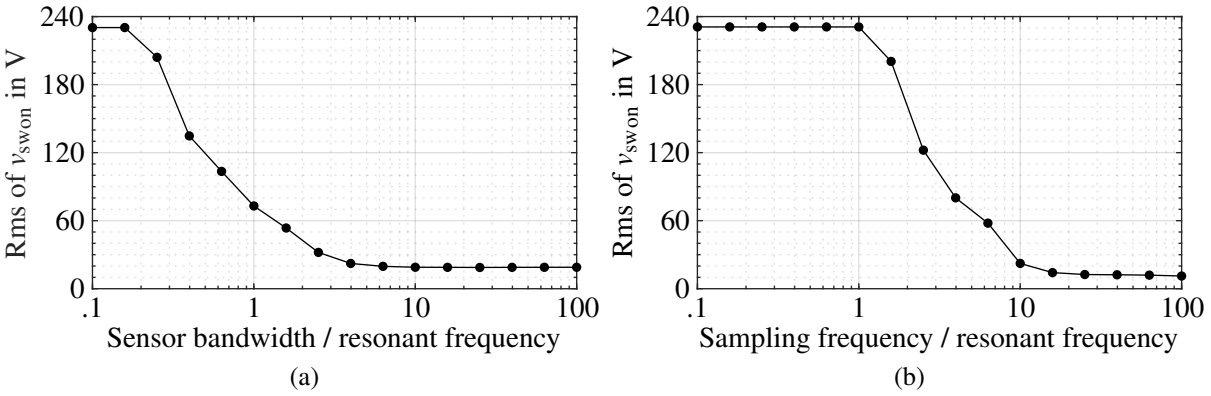


Fig. 6: Effect of (a) sensor bandwidth and (b) ADC sampling frequency on v_{swon} for AZC control.

From Fig. 6, it can be seen that for optimal performance of the AZC, a sensor bandwidth of $\geq 4f_{\mathrm{r}}$ with sampling rate $T_{\mathrm{sample}} \leq \frac{1}{20f_{\mathrm{r}}}$ is required. With values from Table I, $f_{\mathrm{c}} > 3.46\,\mathrm{MHz}$ and $T_{\mathrm{sample}} \leq 57.8\,\mathrm{ns}$.

Steady-State AC Performance

The steady-state performance of the AZC is evaluated by examining the rms of v_{swon} over one ac cycle vs. load current. The results are compared with existing control techniques and can be seen in Fig. 7.

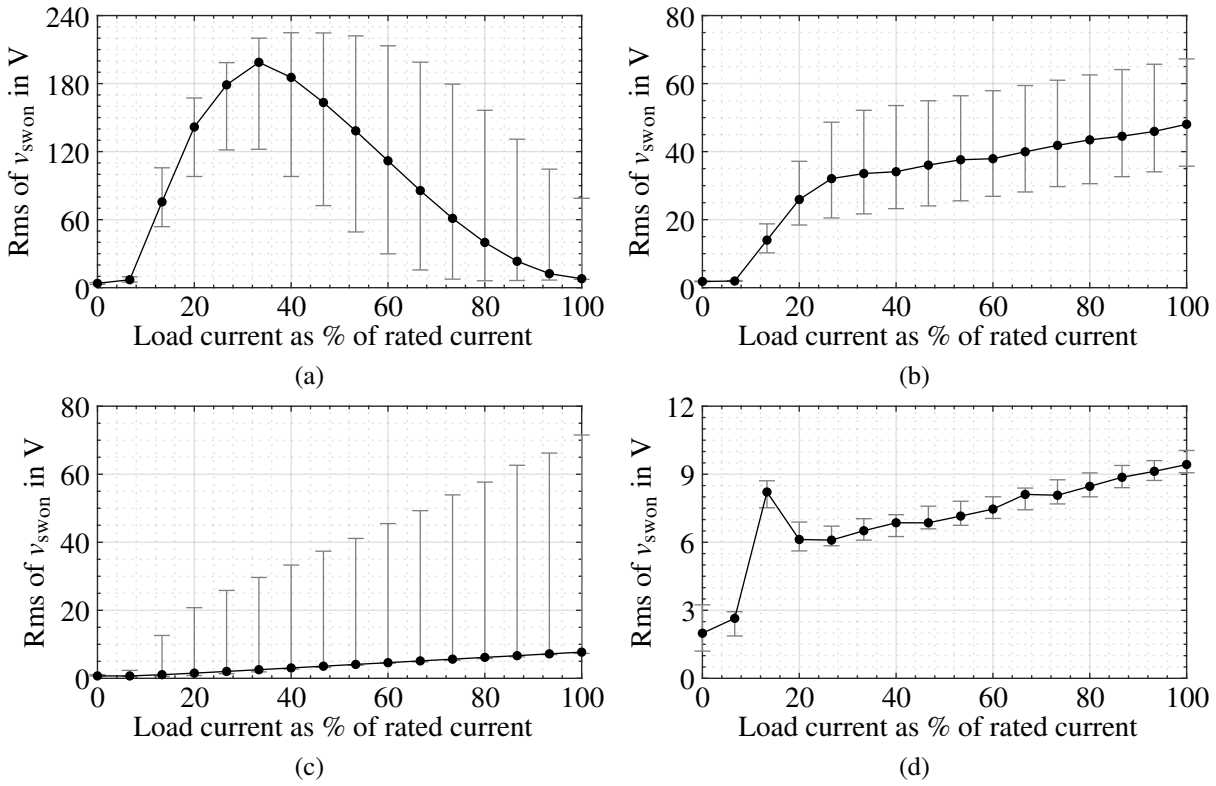


Fig. 7: Simulation results showing the rms of the switch turn-on voltage (with variance caused by L_{r} and C_{r}) vs. load current. (a) Fixed control. (b) Comparator window-detector. (c) Estimated control. (d) AZC.

v_{s} is a 50 Hz ac source with rms value V_{s} and the converter operates with a constant duty-cycle (D). A tolerance of 10% is applied to L_{r} and C_{r}, and propagation delay (T_{pd}) is added to all sensors. For each point (–●–), 128 simulations are performed, each having a random selection of L_{r} and C_{r} within tolerance. The points indicate the nominal values for L_{r} and C_{r} and the bars indicate the variance caused by the tolerance. Each simulation is run for one ac cycle and the rms is calculated of the resultant v_{swon}.

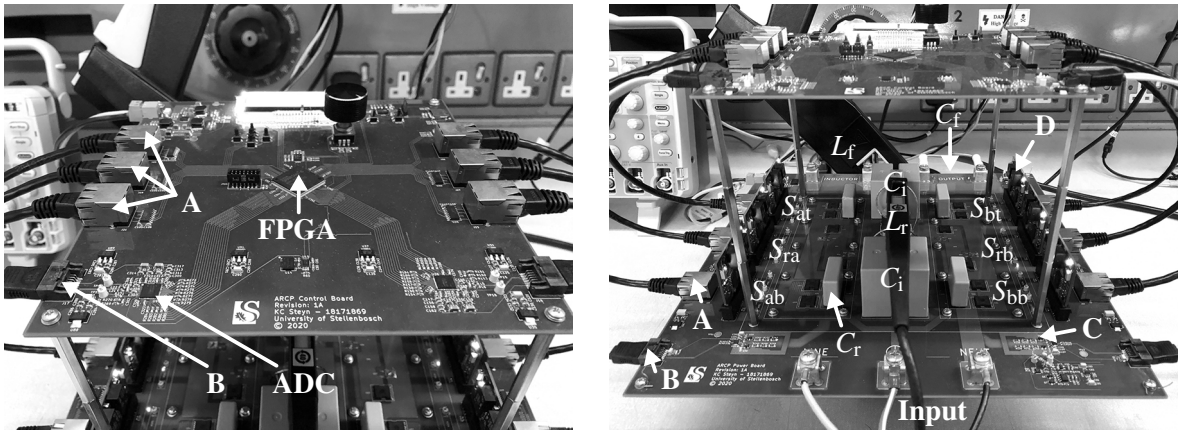
Fixed control (Fig. 7a) only performed well during low and rated current with nominal values of L_{r} and C_{r}. The variance of v_{swon} was high and propagation delay had no effect. This is due to (1) only being valid at rated load. The comparator window-detector (Fig. 7b) was impacted the most by propagation delay ($v_{\text{swon}} > V_{\text{th}}$) and had a large variance. Estimated control (Fig. 7c) was not affected by propagation delay, however, was impacted the most by tolerance. AZC control (Fig. 7d) was not affected by propagation delay and showed minimal variance due to tolerance, with the load slope being due to conduction losses.

Experimental Prototype

The prototype in Fig. 8 was designed with parameters as in Table I and notable components in Table II.

Table II: Notable Prototype Components

Component	Manufacturer	Product Number	Cost per Unit
FPGA	Xilinx	XC6SLX9	20 EUR
GaN HEMT	Infineon	IGT60R070D1	19 EUR
11-Bit Parallel ADC	Texas Instruments	ADC11C125	21 EUR
Fully Differential Op-Amp	Analog Devices	ADA4927	9 EUR

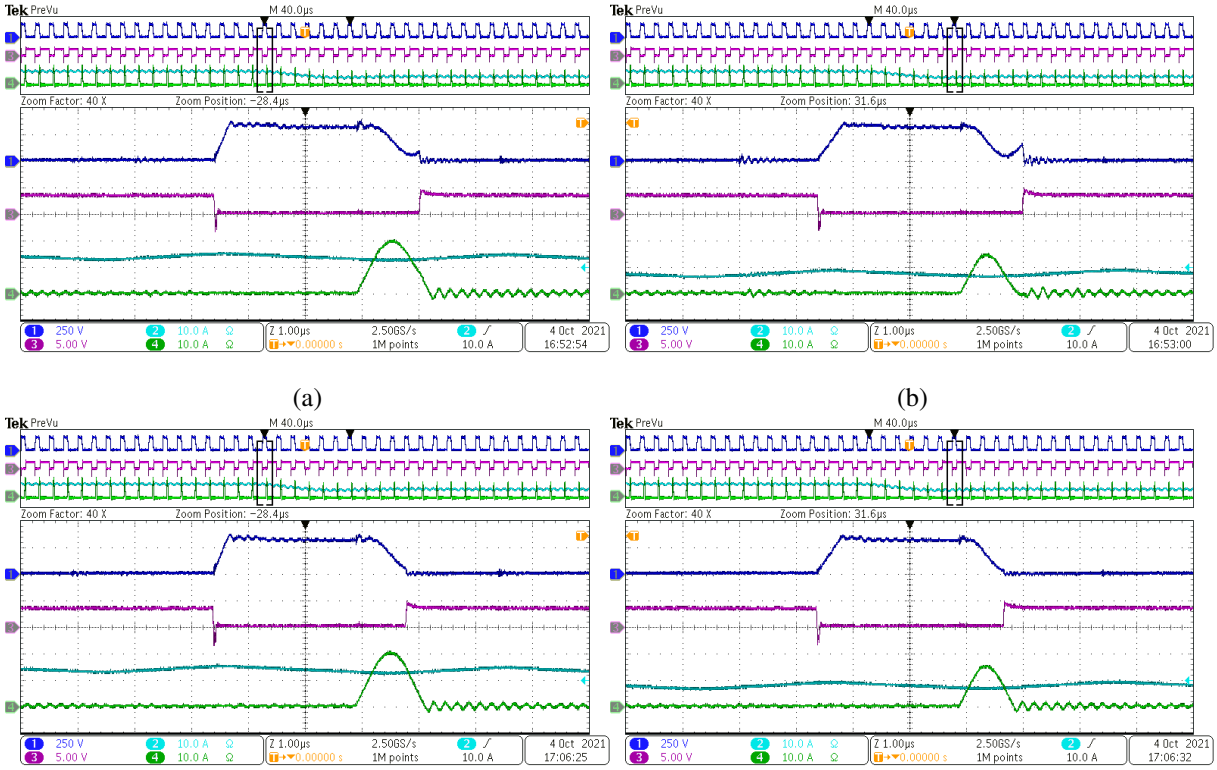


(a) (b)

Fig. 8: 5-kW direct ac-ac ARCP prototype. (a) Control board. (b) Power board.

All switches consist of common-source GaN enhancement-mode HEMTs. One 11-bit parallel ADC is actively used with a differential op-amp for the voltage sensor, which interfaces with an FPGA. Notable indicators A: digital signals, B: analog differential signals, C: voltage sensor and D: gate driver boards.

A transient load test was performed to compare fixed control with the AZC. The results are seen in Fig. 9.



(a) (b)

(c) (d)

Fig. 9: Measurements during load-step. (a) - (b) Fixed control and (c) - (d) AZC. CH1: switch voltage (v_{sw}), CH2: filter inductor current (i_f), CH3: gate-source voltage and CH4: resonant inductor current (i_r).

With fixed control, there is a large difference in v_{swon} before (Fig. 9a) and after (Fig. 9b) the load step. The AZC is able to track the resonant valley and achieve ZVZCS before (Fig. 9c) and after (Fig. 9d) the load step. The measurements also validate the transient simulation results in Fig. 5a and the steady-state values of v_{swon} before and after the transient for fixed control (Fig. 7a) and AZC control (Fig. 7d).

The configuration of the voltage sensor utilized in the prototype for measuring v_{sw} can be seen in Fig. 10.

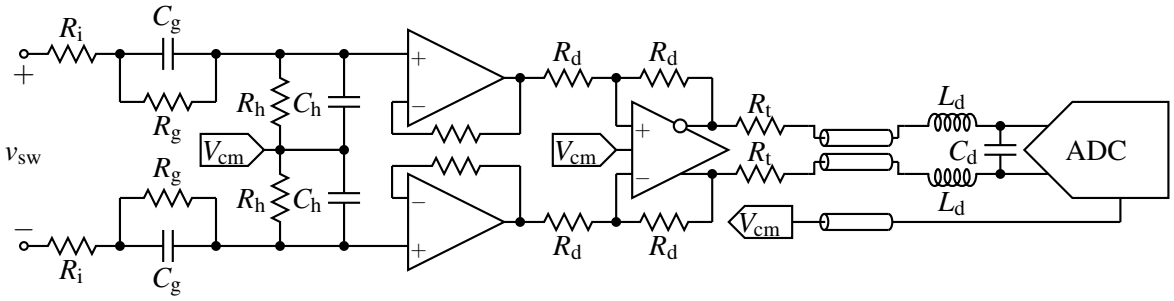


Fig. 10: Sensor for measuring phase-arm switch voltage (v_{sw}).

Resistors R_g and R_h with capacitors C_g and C_h form a voltage divider. R_i is added to limit the bandwidth and impact of the parasitic inductance of C_h. R_g consists of three series 1 MΩ resistors, R_h one 7.5 kΩ resistor, C_g four series 6.8 pF capacitors, C_h one 680 pF capacitor and R_i one 1 kΩ resistor. Buffer op-amps are added to drive a differential op-amp at unity gain ($R_d = 500\,\Omega$). Series termination resistors R_t of 50 Ω are added for the 100 Ω SATA transmission line. A filter ($L_d = 30$ nH and $C_d = 47$ pF) is provided to decouple the line from sampling. The bandwidth of the sensor was measured at 32 MHz in LTspice.

Conclusion

The AZC control technique was presented as a method to ensure ZVZCS for the ARCP topology. Uniform oversampling of the voltage across one phase-arm switch, with a sliding base-2 zero-crossing detector, could eliminate the effect that input voltage, load current, propagation delay and resonant frequency have on achieving ZVZCS with the ARCP. Simulation and experimental results indicated that AZC would reduce the turn-on voltage of the phase-arm switches during steady-state ac operation when compared to existing control techniques. The turn-on voltage exhibited low variance over a wide load range when tolerance was introduced on the resonant components and the sensor was subject to propagation delay.

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