Comparison of Power Cycling Results of discrete GaN Cascodes for Automotive Power Electronics with high Temperature Swings

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Abstract

High voltage rated GaN HEMTs are attractive for automotive applications such as on-board charger or auxiliary power supplies. Nowadays GaN is packaged as single chips in discrete housings. In this paper a power cycling set up and results for GaN components in discrete TO-247 package are presented.

I Introduction

Many automotive qualified semiconductors for power applications are offered in the TO-247 package. The TO-247 package, see Fig. 1a, is available for a long time. New semiconductors are also offered in this package. GaN components can increase the power density or reduce cooling requirements of an existing system. Some manufacturers offer normally-on GaN HEMTs which are combined with a low voltage Silicon MOSFET to reach normally-off behavior. For the new semiconductors different interconnection technologies are used for the upper and lower side of the chip. Nowadays it is common to use bond wires and solder connections. For investigating the lifetime of GaN cascodes in the TO-247 package with new interconnection technologies, power cycling tests are done.
In order to estimate the lifetime of power electronics, it is mandatory to create lifetime models for the used semiconductors. For generating a lifetime model, power cycling tests at different temperature swings and absolute temperatures have to be done. Wide Band Gap (WBG) components like Silicon Carbide (SiC) MOSFETS or Galliumnitride (GaN) also in cascodes are still exotic under lifetime aspects. Only a few results have been published [1, 2]. In [1] the focus was set on the aging effects, rather on lifetime model. In [2] a component in a different discrete package (TO-220) was tested, however the temperature swings were not as high as in this test and the measuring points are relativly close together. The tested GaN cascodes in [1] and [2] were compared with GaN HEMTs, not with different GaN cascodes. A general fitting model like LESIT known from Si-IGBTs still does not exist. The LESIT model [3] is a lifetime model which is the first destination when no information about the inner structure is available. However the new parameters have to be identified by curve fitting of the power cycling results.

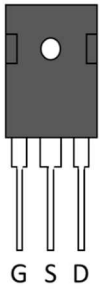

Fig. 1a
TO-247
package

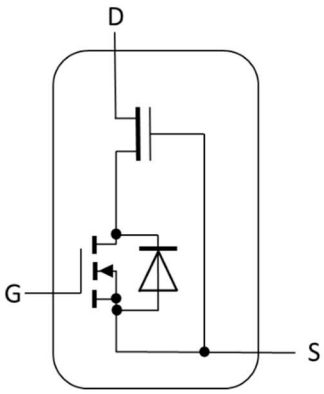

Fig. 1b:
GaN cascode electrical
circuit

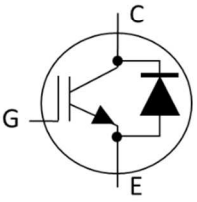

Fig. 1c:
IGBT electrical
circuit

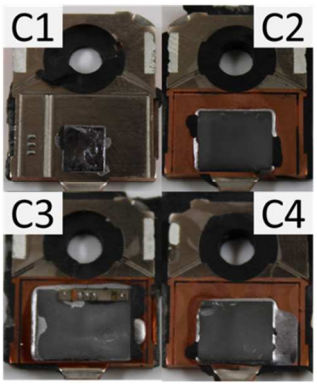

Fig. 1d:
opened cascodes

A GaN cascode, see Fig. 1b, consist of a normally-on GaN HEMT (top) and a normally-off silicon MOSFET (bottom). The MOSFET is used for switching the states of the HEMT, which blocks the high voltage. The load current flows through the HEMT and the MOSFET from Drain to Source. A body diode is included in the MOSFET. In comparison an IGBT, see Fig. 1c, which requires for the diode a separate chip. From this follows that the indirect measurement of the virtual junction temperature T_{vj} of the chips can be done in different ways and at different positions inside the component. The measurement of T_{vj} is described in chapter III “test criteria”.
The structure of the components is shown in Fig. 1d. After removing the plastic housing the top view to the lead frame and the chip is possible. It can be seen that the position of the chips of the GaN cascodes within the package is different. While the chip size of component C2 and C4 (both Rds(on) = 50 mΩ) is very similar, the structure of the components C1 and C3 is very different.

II Mechanical Setup for the Power Cycling Tests

During the power cycling test, the load current flows cyclically through the device under test (DUT), which heats up and cools down afterwards. There is a mechanical expansion in each material layer in each cycle. The virtual junction temperature of the chip rises to $T_{vj,max}$ and sinks to $T_{c/s,min}$. The temperature $T_{c/s}$ is measured below the DUT. Depending on the cooling system, also $T_{c/s}$ can change between $T_{c/s,min}$ and $T_{c/s,max}$. When the dimension of the cooling system is sufficient, the temperature $T_{c/s}$ should be $T_{c/s,max} = T_{c/s,min}$ = constant . The courses of the temperatures are shown in Fig. 2.

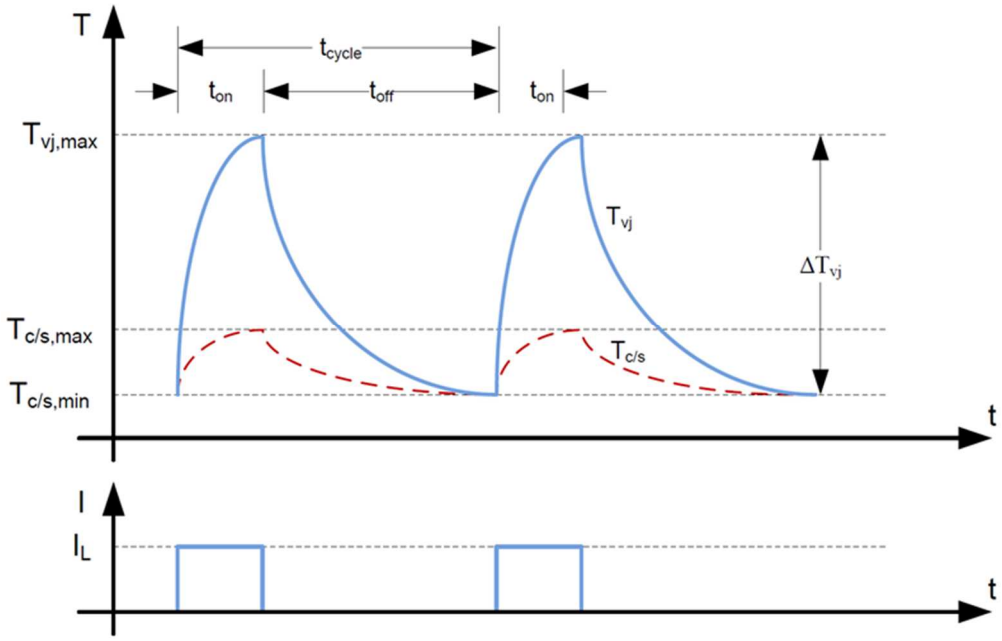

Fig. 2: Test parameters and power cycling definitions [4]

The mechanical setup for the measurements is based on the AQG324 [4] and includes a temperature sensor, a thermocouple type k, 2 mm below the DUT for $T_{c/s}$ (see Fig. 3). The mounting PCB is located at a 90° angle to the cooling plate. Mechanical stresses to the component resulting from temperature changes are compensated by a standard mounting clip. The mechanical construction is shown schematically and in real in Fig. 3a and 3b. The TO-247 housings are always positioned exactly the same using a mounting template.

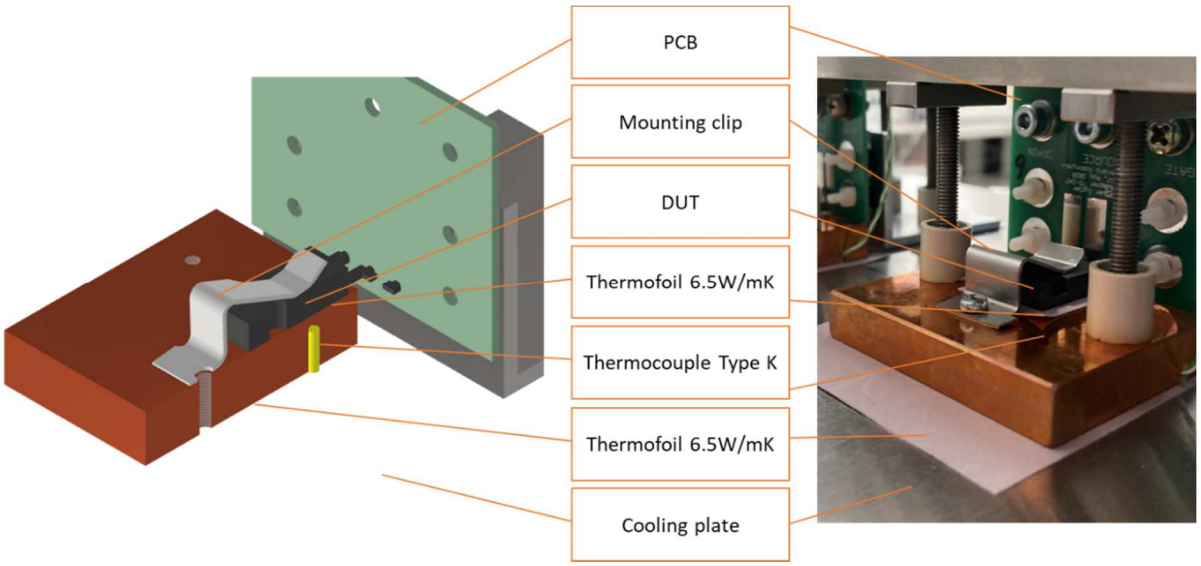

Fig. 3a: schematically setup

Fig. 3b: real setup

III Test Criteria

Different failure modes are known from existing housing and interconnection technologies, such as chip delamination or bond wire defects. A short on-time t_{on} and a short off-time t_{off} are set in order to stress the chip-near interconnections. The mean junction temperature T_{jm}, which is defined as $(T_{vjmax} + T_{vjmin})/2$ should be the same for all tests. High temperature swings for T_{vj} are reducing the test time, because the

stress for the component is higher. Two measuring points M1 and M2 with a large difference between the temperature swings ΔT_{vj}(M1) and ΔT_{vj}(M2) are used, see Table I.
For these tests measuring point M2 was chosen with a maximum junction Temperature T_{jmax} close to the allowed chip temperature of 175°C. The temperature swing ΔT_{vj}(M2) = 130 K is relatively high. The on-time t_{on} and the off-time t_{off} are set to 4 seconds. A fine adjustment is done with the cooling temperature of the liquid cooling system, see Table II.
For the second measurement point M1 a smaller temperature swing ΔT_{vj}(M1) is set with $t_{on} = t_{off} = 0{,}5$s in order to achieve a difference between the two measuring points with about 60 K. The load current I_L for M1 and M2 is the same, see Table II. The planed test criteria are shown in Table I, however there are deviations for each DUT because of tolerances.

Table I: The planed test criteria

	M1	M2
ΔT_{vj}	70K	130K
T_{vjmax}	140°C	170°C
T_{vjmin}	70°C	40°C
T_{jm}	105°C	105°C
t_{on}	0.5s	4s
t_{off}	0.5s	4s

The junction temperature T_{vj} of the GaN cascodes is measured indirectly with the V_{sd}-Method [5]. The measurement current is -20mA from Source to Drain. The HEMT and the MOSFET are close together and heated up by the same load current.
The junction temperature T_{vj} of the IGBT is measured indirectly with a measurement current +20mA through the channel from Collector to Emitter, because the IGBT and the diode are two different chips. For each device a calibration from -25°C up to 125°C is done. The temperature is measured a short time (µs) after the load current is turned off. The tested devices are listed in Table II. For each test four devices were used. All devices have the TO-247 package.

Table II: The tested devices

Component	Manu-facturer	Technology	Voltage class	Rds(on)eff / VCEsat	Load Current I_L	$T_{cooling}$ M1	$T_{cooling}$ M2
C1	A	GaN cascode	650V	35 mΩ	35,5A	25°C	21°C
C2	A	GaN cascode	650V	50 mΩ	27,6A	25°C	22,4°C
C3	B	GaN cascode	650V	35 mΩ	36,2A	26,5°C	23,8°C
C4	B	GaN cascode	650V	50 mΩ	27,3A	26,5°C	25°C
C5	C	IGBT	650V	1,66V	49A	23,8°C	23,8°C

IV Test Results and Discussion

The aging and the following failure of the semiconductors can be observed by different criteria. Here the Drain-Source voltage $V_{DS,on,}$ (see Fig. 4) and $T_{vj,max}$ (see Fig. 5) are recorded. The test was stopped when the junction temperature $T_{vj,max}$ has reached 250°C. Measurements of the thermal resistance from junction to sensor $R_{th,j-c/s}$ are automatically done in constant intervals by the test bench. These measurements are causing brief drops in the course of the temperatures and voltage $V_{DS,on}$ (see Fig. 4). The curves of the Thermal Resistance $R_{th,j-c/s}$ per device are presented in Fig. 6.

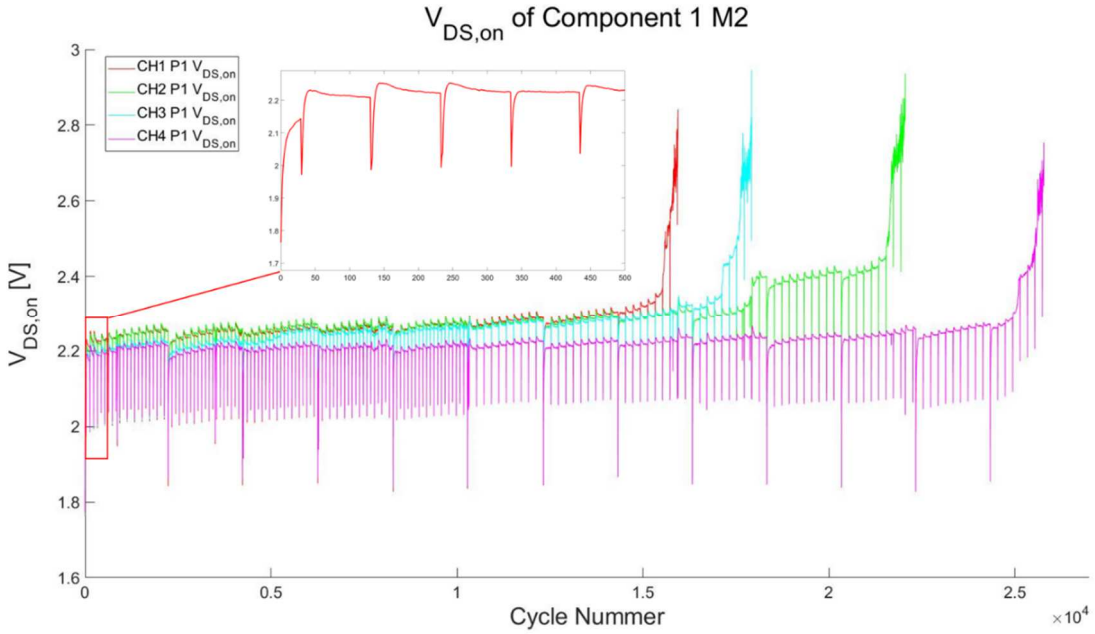

Fig. 4: Drain-Source voltage $V_{DS,on}$ and cycle number

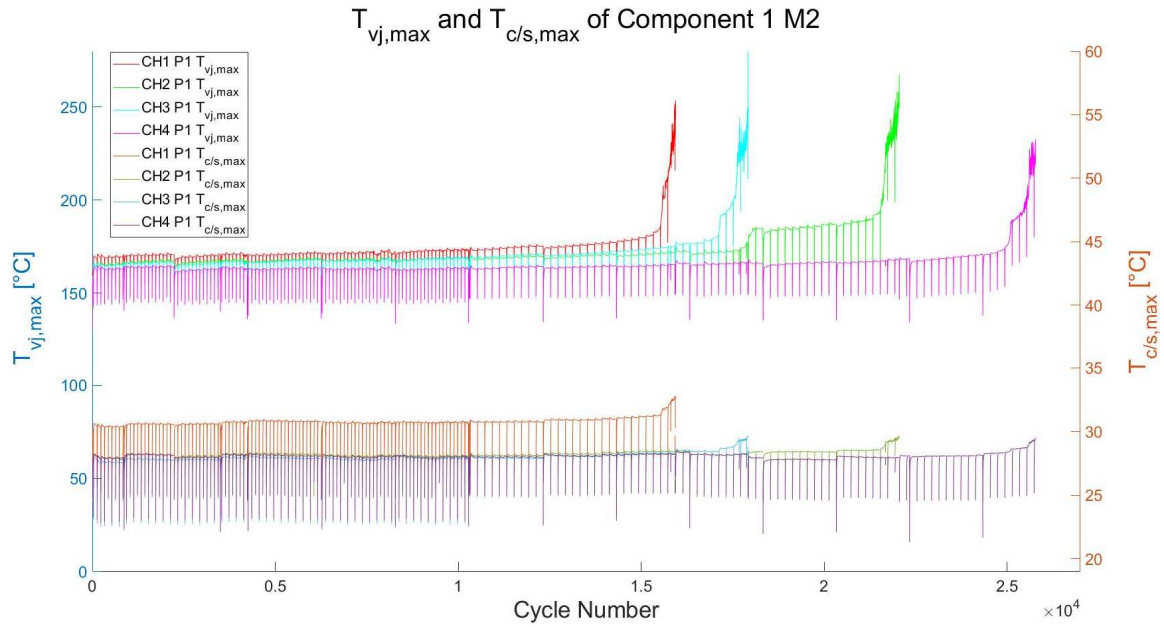

Fig. 5: Maximum junction temperature $T_{vj,max}$ and temperature $T_{c/s,max}$ and cycle number

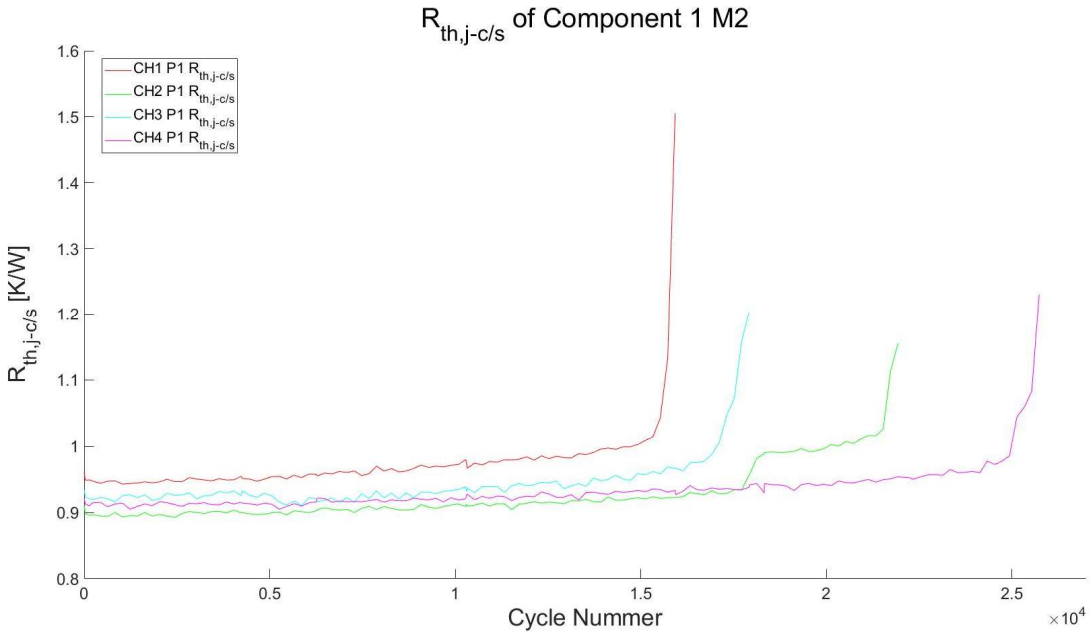

Fig. 6: Thermal resistance $R_{th,j-c/s}$ from junction to sensor $T_{c/s,max}$ and cycle number

The end of life criteria is defined as the starting value of the Drain-Source voltage $V_{DS,on}$ plus 5% and/or the thermal resistance $R_{th,j-c/s}$ starting value plus 20%, see [4]. The drops in the curves of the Drain-Source voltage $V_{DS,on}$ make the evaluation more complex. The end of life criteria of the thermal resistance $R_{th,j-c/s}$ plus 20% was reached when the test was stopped. For the lifetime models the total number of cycles are used. The results of the power cycling tests are shown in Fig. 7 (component 1: blue triangle, component 2: purple dot, component 3: red rectangle, component 4: orange rhombus, component 5: green dot).

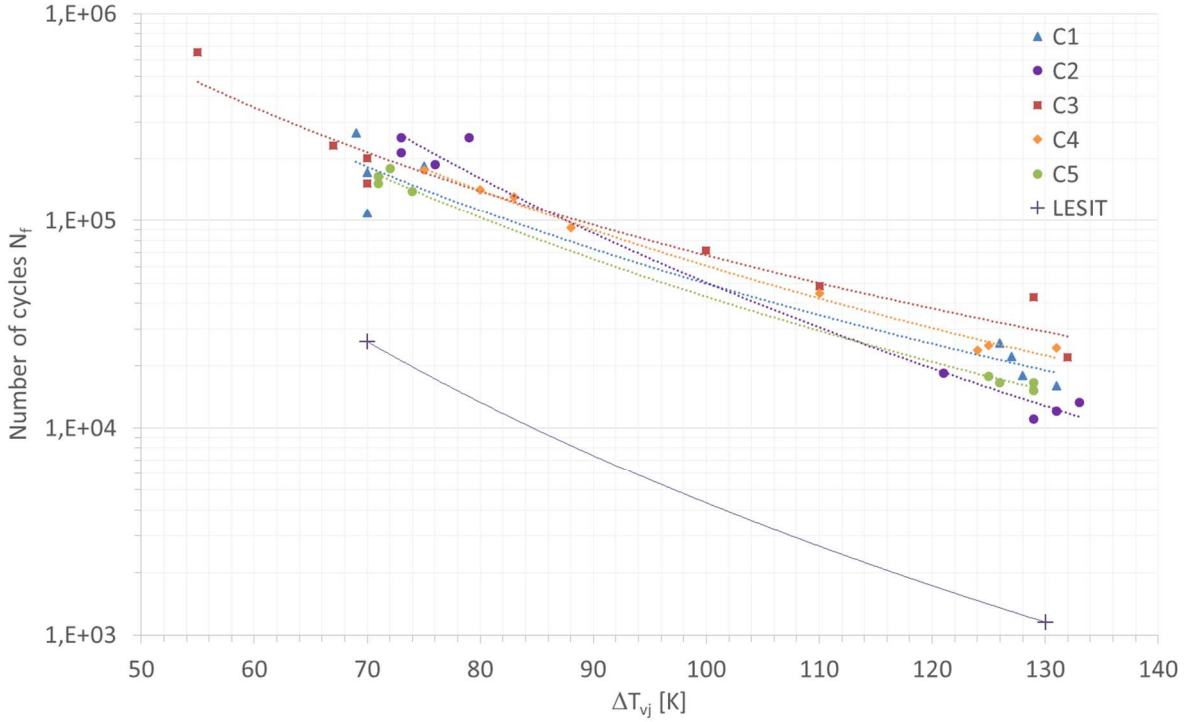

Fig. 7: Number of cycles until failure N_f for GaN cascodes (C1-C4) and IGBT (C5) in comparison to LESIT

The expected curve of the LESIT model for the two temperature swings from Table I and standard IGBT parameter [3] is depicted in Fig. 7. All tested devices reach higher number of cycles than the calculated LESIT values. For the lifetime modelling trend lines are integrated.
In Fig. 8 and 9 the results for GaN cascodes with 35mΩ and 50mΩ and the IGBT are shown in detail.

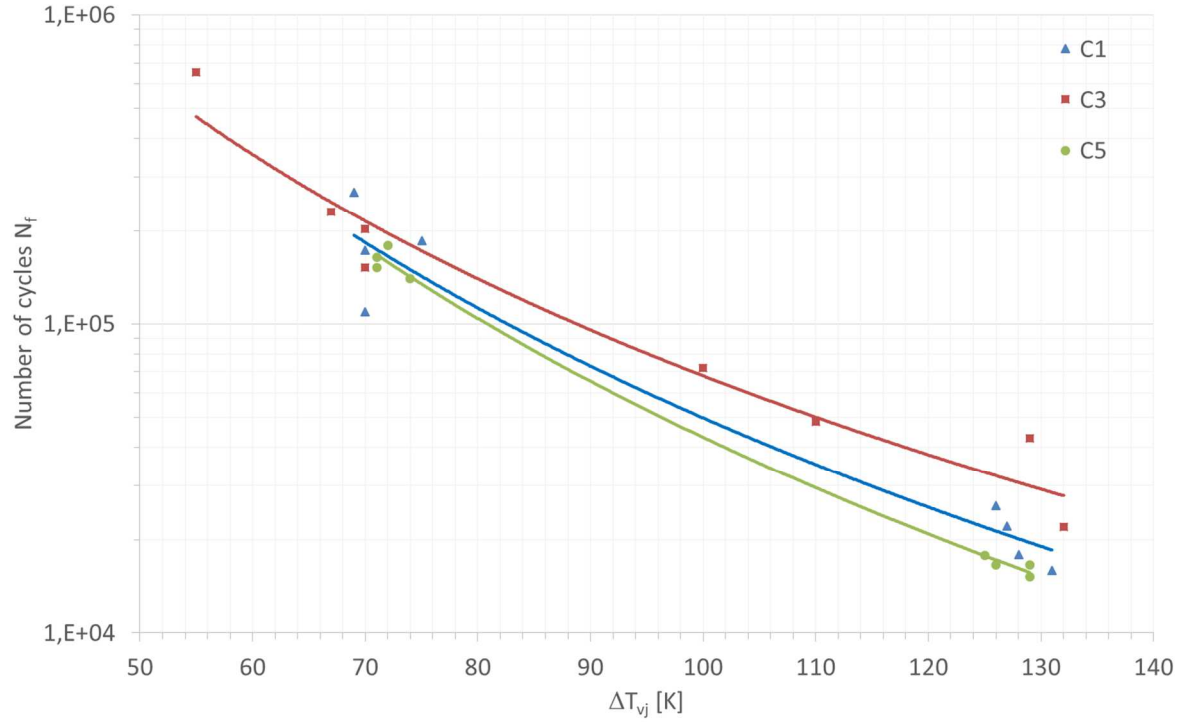

Fig. 8: Number of cycles until failure N_f for GaN cascodes 35mΩ (C1+C3) and IGBT (C5)

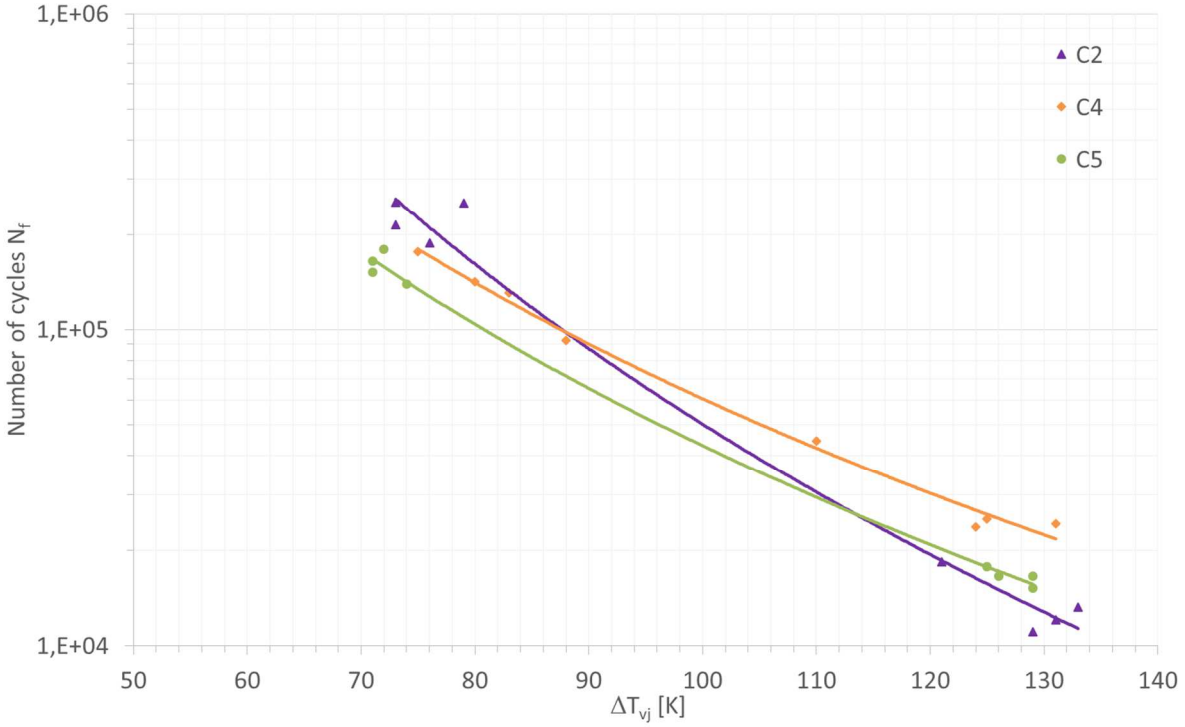

Fig. 9: Number of cycles until failure N_f for GaN cascodes 50mΩ (C2+C4) and IGBT (C5)

The interconnection technologies and inner structures of semiconductors in discrete packages are different than for semiconductors in modules. Failure modes for example bond wire lift off or cracks caused by temperature swings and plastic deformation are though comparable. The LESIT model takes this failure modes into account.

The LESIT formula [3]:

$$N_f = A \cdot \Delta T_j^{\alpha} \cdot e^{\frac{E_a}{k_b \cdot T_{jm}}} \quad (1)$$

For the LESIT model the exponents α and factors A must be extracted from the test results. The trend lines, see Fig. 7 – 9, are composed of potency functions. The exponents α_{new} are directly adopted, see Table III. The factors A_{new} are computed by rearranging the equation (1) of the LESIT model for each device and by using the mean value for the eight tested devices (M1: 4 devices and M2: 4 devices). For the calculations the activation energy $E_a = 9.891 \cdot 10^{-20}$ J and the Boltzmann-constant $k_b = 1.38065 \cdot 10^{-23}$ J/K are used. The modified formula is shown in equation (2).

The LESIT formula with modified exponent α_{new} and factor A_{new}:

$$N_f = A_{new} \cdot \Delta T_j^{\alpha_{new}} \cdot e^{\frac{E_a}{k_b \cdot T_{jm}}} \quad (2)$$

Table III: Trend line formulas, exponents and factors for the LESIT model

	Trend line formula	α_{new}	A_{new}
Component 1	$N_f = 10^{12} \cdot \Delta T_{vj}^{-3.661}$	-3.661	6,018
Component 2	$N_f = 10^{15} \cdot \Delta T_{vj}^{-5.221}$	-5.221	8,125,317
Component 3	$N_f = 20^{11} \cdot \Delta T_{vj}^{-3.231}$	-3.231	718
Component 4	$N_f = 20^{12} \cdot \Delta T_{vj}^{-3.786}$	-3.786	9,448
Component 5	$N_f = 40^{12} \cdot \Delta T_{vj}^{-3.963}$	-3.963	21,043
LESIT	$N_f = 50^{13} \cdot \Delta T_{vj}^{-5.039}$	-5.039	302,500

The exponents α_{new} of component C1 and C3 which have the same Rds(on) are very similar. Whereas component C2 with a higher Rds(on) also has a higher exponent α_{new}. The exponent value of component C4 lies between the values of component C1 and C2. The values of the factors A_{new} are far apart for all components. The power cycling tests show that for every component a different lifetime model must be made.

V Conclusion

In this paper the results of power cycling tests of different, discrete 650V GaN cascodes with high temperature swings were presented. The inner structure of the GaN cascodes varies. The chips of MOSFET and HEMT are placed close together in the TO-247 package and the temperature of the chips was measured indirectly with the Vsd-method. The sample size of four devices per measurement point seems to be sufficient. As end of life criteria the $R_{th,j-c/s}$ was used, the course of the drain-source voltage $V_{DS,on}$ was not clear for the definition of limits.

The results of the power cycling tests show that differences of the lifetime between the GaN cascodes were not as big as expected. The results of [2] with a GaN cascode in TO-220 package were in the same range. For lifetime modelling the parameter of the LESIT model were adjusted. Compared to other lifetime models like CIPS08 no additional information about the inner structure are required. Generating one lifetime model for all tested GaN cascodes would not be useful due to big differences in the inner structure.

The lifetime of the tested GaN cascodes is comparable to the tested discrete, automotive qualified Si IGBTs, what makes the GaN cascodes interesting for automotive applications. In future work further tests with 650V SiC devices as well as semiconductors in other packages will be done.

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