Multilayer busbars for medium voltage ANPC converter dedicated to battery energy storage systems

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Keywords

«Low inductive busbar», « 3.3 kV SiC power modules », «High power», «Medium voltage», «Energy storage system».

Abstract

The increase of energy storage system power leads to open a technological pass which is to increase the voltage level of battery racks. Available 3.3 kV Silicon Carbide (SiC) semi-conductors implemented in an ANPC topology allows tuning a 3.6 kV DC bus.Thus, researches are shifting to medium voltage systems in which battery racks are connected in series with a middle point grounded. SiC modules implementation requires low inductive busbars to achieve high efficiency when rising in switching frequency necessary to shrink the output filter. In this paper, a methodology for reducing the parasitic inductor of the busbars (< 20 nH) is presented.

Introduction

The energy transition leads to speed up the mass use of renewable energies, in particular solar and wind energy instead of fossil fuels [1]. However, to ensure the balance between electricity production and consumption, energy storage systems are combined with renewable energies generators [2]. These storage systems must also meet requirements in terms of efficiency and grid support. European Talent project was proposed to increase the voltage of BESS from conventional low voltage racks [3] 1 kV-1.4 kV to medium voltage racks (2×1 500 V with middle point grounded) achieving a high efficiency (> 99 %) and reducing the quantity of required power components raw materials. The ANPC converter operating in outer switching modulation mode (OSMM) presents the main advantage to use only small switching loops in inverter or rectifier mode allowing a switching speed increase [4]. This paper focuses on the ANPC converter design. The DC/DC converter analysis will be down by the authors in furthers articles.

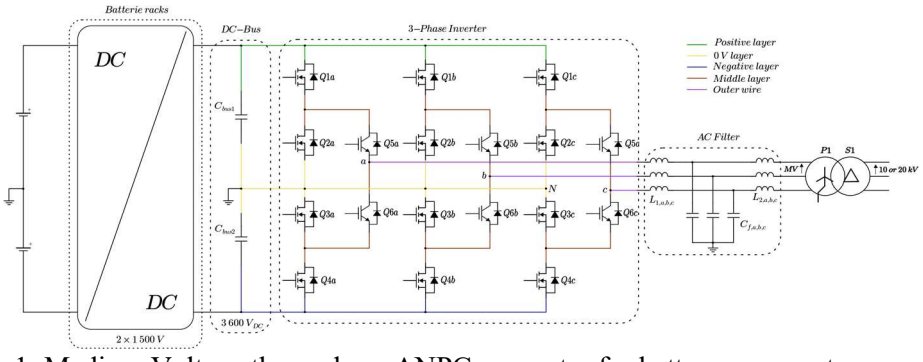


Figure. 1: Medium Voltage three-phase ANPC converter for battery energy storage systems

Several studies carried out to set up laminated busbars which have made it possible to reduce the parasitic inductance of busbars from a few hundred nH to around ten nH [5-6]. All of these papers use multilayer busbars that often requires algorithm to determine busbars sizing. In [7], authors bring an approach to build multi layers layers busbars from two layers busbars once assembled show interesting stray inductor reduction. The methodology presented, is applicable to an ANPC conversion PEBB using 3.3 kV power modules.

A mixed Si/SiC ANPC leg and its control principle are presented Fig. 2. A ANPC leg controlled in outer switch modulation mode consists of using a 3.3 kV IGBT power module operating at grid frequency (50 Hz) connected to the leg output while two SiC modules operating at the switching frequency (…kHz) are connected to poles. The implementation of the ANPC leg is done by an external assembly of 3×2L modules. This allows the manufacturer to take benefits of a wide choice of two-level power modules easy to replace.

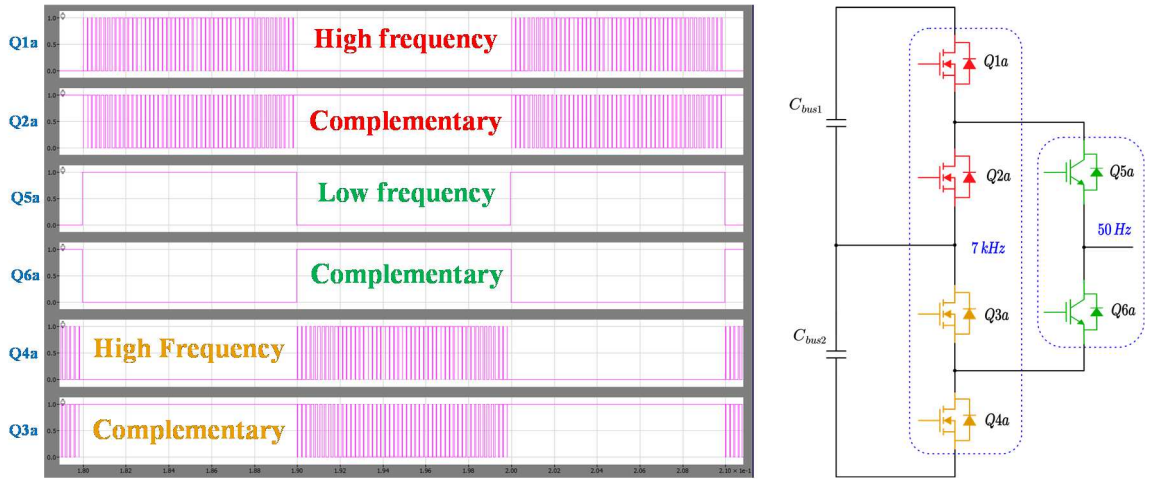
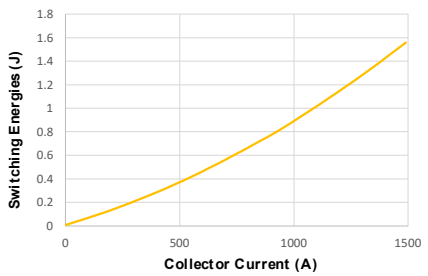


Fig. 2: Principle of operation of an ANPC leg (OSMM)

In order to build a 3MVA converter two 1.5 MVA ANPC PEBB will be connected in parallel. A switching frequency of 7 kHz seems an acceptable compromise to target an efficiency > 99% including output filter losses and DC/DC converter losses. An electro-thermal model was built under PLECS [8] to estimate the power modules losses from power modules datasheet. From switching and conduction characteristics of IGBT and MOSFET power modules, the simulation results show an efficiency range between 99% - 99.6%.



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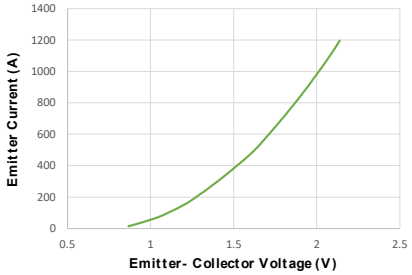

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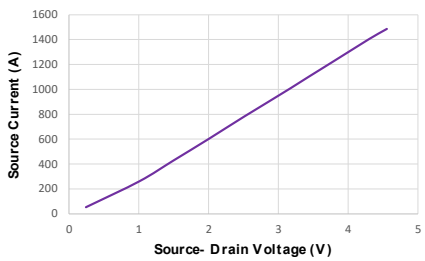

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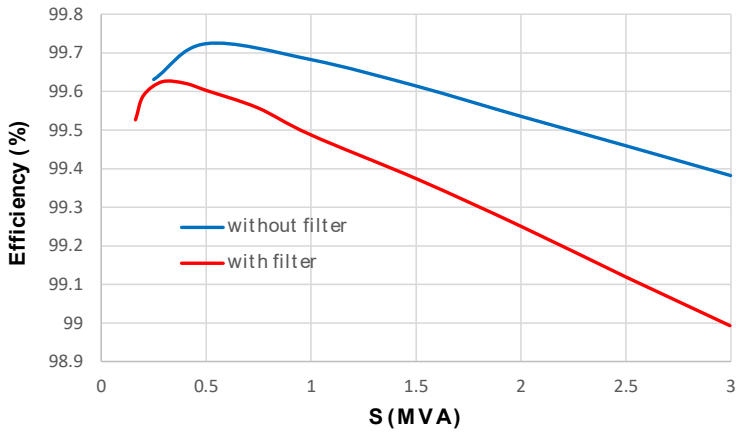


d)

Fig. 3: a) Half-Bridge switching energy characteristics, b) Free-Wheeling diode forward characteristics (MOSFET), c) Free-Wheeling diode forward characteristics (IGBT), d) Efficiency curves for 3 MVA three-phase ANPC converter (7 kHz)

In the section 1, the design methodology of the busbars will be described as well as a Q3D [9] based comparative studies between different layouts possibilities. Finally, the conclusion of this paper and the future work are presented in section 2.

1. Bus bar design and comparison for one phase Leg

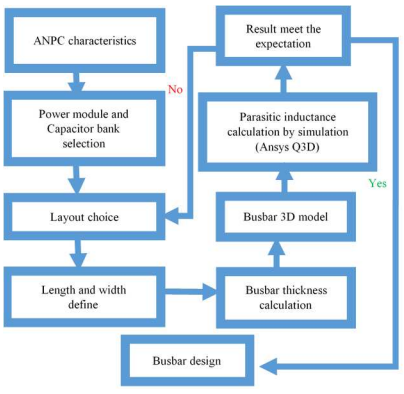
As explained previously, the use of busbars is to ensure the connection between the power modules and the DC capacitor of the converter maximizing capacitive effect. Equations 1 to 4 give the characteristics of classic busbars formed by two conductive layers separated by an insulating layer [7]. L_C: is the parasitic inductance of each active layers, which depends on the length (l), the width (w), the thickness of the layers (e), the insulation layer thickness (d), the vacuum permeability (μ_0) and relative permeability (μ_r), Minimum busbars area (A_{min}). M_c is the mutual inductance between the two conductive layers; it depends on the same parameters as L_C. When the direction of current flow is the same in the two conductive layers the mutual inductance is positive, conversely it is negative. In order to reduce the total inductance of the bus bar (L_T) a design with a reverse flow direction is recommended. Figure 4, presents the flowchart of the design methodology.

$$L_C = 2.10^{-7}.l.\left[2.303\log\left(\frac{2l}{w+d}\right) + 0.5 + 0.2235\left(\frac{w+d}{l}\right)\right] \quad (1)$$

$$M_C = \frac{\mu_r}{2\pi}\left[l.\ln\left(\frac{\sqrt{d^2+l^2}+l}{d}\right) - \sqrt{d^2+l^2} + d\right] \quad (2)$$

$$L_t = 2L_c - 2M_c \quad (3)$$

$$A_{min} = w.e = \frac{400.I.(0.785).[1+0.05(N-1)].(1.10^{-6})}{0.123} \quad (4)$$



Main characteristics of the ANPC converter	
Power	3 MVA
Modulation (PWM)	Outer switching mode modulation (OSMM)
Maximum Input voltage	3.6kV$_{DC}$
Maximum Output voltage	2.2kV$_{RMS}$ 50 or 60Hz (+/-15%) EN50160
Output wiring	3~ (without neutral)
Power modules	3.3kV SI IGBT (operating at 50 or 60Hz) 3.3kV SiC MOSFET (7 kHz)
Power factor	-1 (rectifier mode) to 1 (inverter mode)

Figure. 4: Busbars algorithm design and ANPC converter characteristic

DC bus Capacitor Bank selection:

The capacitor bank ($C_{bat} = C_{bus1} + C_{bus2}$) is calculated to provide the peak I_{rms} current to the AC output of the converter. Its value can be determined by using equation 5 [10] where (f_s) is the switching frequency, (ΔV_{dc}) is the ripple voltage of the DC bus, fixed to 5%.

$$C_{batmin} \geq \frac{\sqrt{2} \times I_{rms\_max}}{2 \times f_s \times \Delta V_{dc}} \quad (5)$$

Based on this criteria and the converter parameter (Figure 4), the minimum value of C_{bat} is 1.2 mF.

ANPC Leg busbars layout comparisons

Figure 5 shows 3 layouts possibilities for inverter legs prototyping using two layer busbars and 3.3kV 2L power modules. Layout 1 consists of placing all power modules on a same line, so the capacitors are placed in front of MOS 1 and MOS 2 power modules (Figure 5b). This placement shows the advantage of using only one heatsink for the 3 power modules. However, placing the IGBT module (IGBT 1) between the negative layer (N) and positive layer (P) reduces the mutual inductance between these two layers. Layout 2 consists of placing the capacitors (C_{bus1} and C_{bus2}) in the center and power modules on the top and the bottom (figure 5c). One of the consequences of this placement is the use of one heatsink per power module; this can increase the costs/complexity of the converter. This placement would also increase busbar's surface area of layers, which may result in increased costs and volume.

Layout 3 consists in placing the MOS 1 and MOS 2 on the same plane line while IGBT 1 is placed back and between the two modules so as to form a triangle (Figure 5d). C_{bus1} and C_{bus2} are placed in front of the SiC power modules and MOS 1 and MOS 2. This type of placement makes it possible to reduce surface area of bus bar layers and therefore the material costs. In addition to this, to bring the MOSFET modules closer together has a positive impact because this increases the mutual inductor. Regarding the cooling of the power modules, depending on the technology used, two heatsinks will be necessary because of the non-alignment of the power modules.

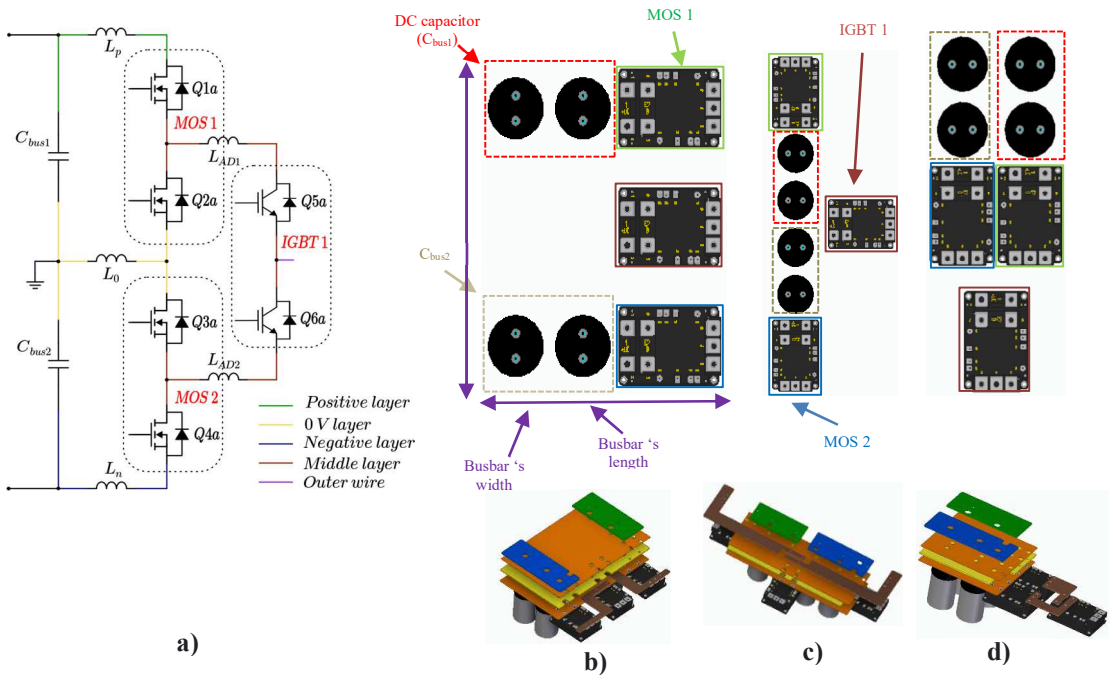


Figure. 5: Layout presentations, a) ANPC leg, b) **Layout 1**: line placement of power modules, c) **Layout 2**: Opposition placement of MOS 1 and MOS 2, d) **Layout 3**: triangular placement of power modules

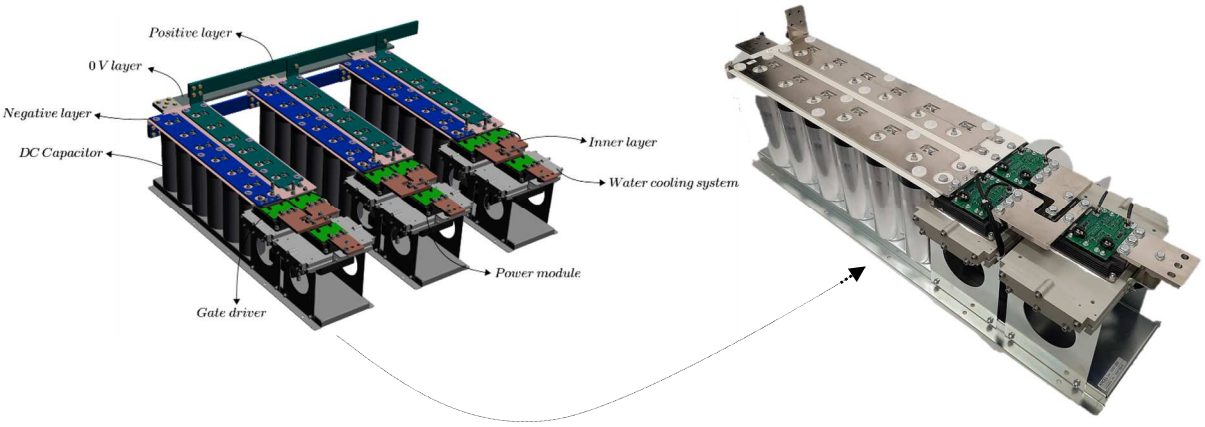
Based on these comparative configurations, it can be concluded that layout 1 and 3 seems to be the most interesting configurations from a power density and cost point of view. However, taking into account the ANPC short switching loop inductance ($L_b = L_0 + L_p$) presented in Table 1, layout 3 is more interesting. These parasitic inductance values were obtained by extracting the 3D model of these different bus bars under Ansys Q3D.

Table 1: Parasitic inductances comparison, inverter leg busbars

	Layout 1	Layout 2	Layout 3
Length [mm]	427	459	259
Width [mm]	259	174	230
Thickness [mm]	3	3	3
L_p [nH]	7	7	4.8
L_0 [nH]	15.88	15.88	15.88

2. Experimental test

After these comparative studies, the paralleling 3 leg of inverter (500 kVA) is chosen in order to obtain 1.5 MVA ANPC power converter. The triangular layout placement of the power modules was chosen (figure 5d) since this solution shows the lowest parasitic inductance loop and busbar's volume (table 1a). Figure 6 presents the 3D model of the PEBB, the prototype ANPC converter phase leg as well as the test bench which made it possible to carry out preliminary tests presented in this part.



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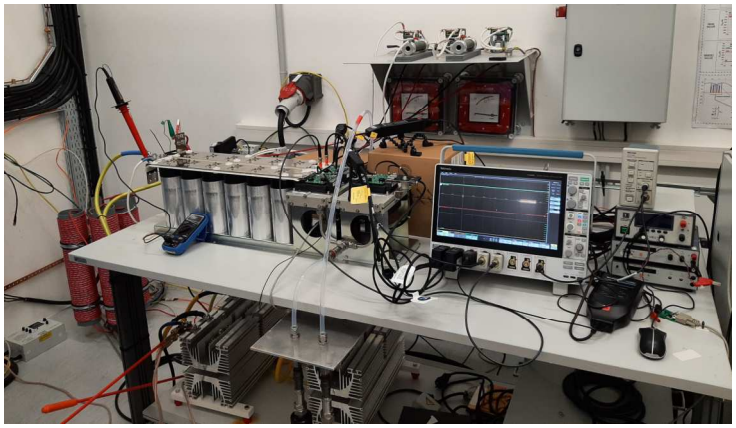

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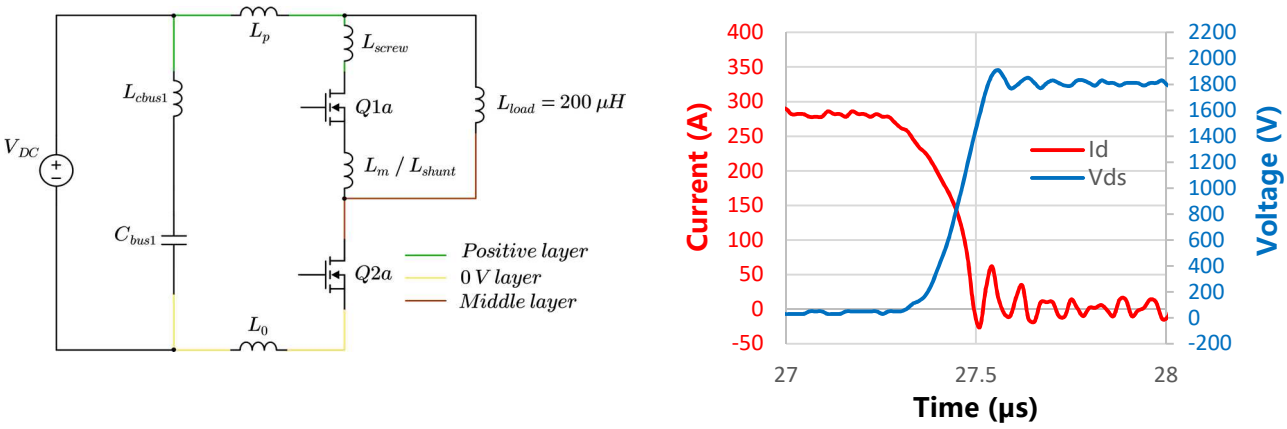
Figure. 6: Inverter leg of the PEBB, a) 3D solid edge model, b) PEBB inverter leg prototype and c) the test bench of the DPT

To evaluate the parasitic inductance of the bar bus, double pulse tests (DPT) are carried out. The electrical schematic of the DPT is shown in Figure 8a. The total inductance of the ANPC short switching loop inductance ($L_{parT} = L_m + L_0 + L_p + L_{shunt} + L_{screw} + L_{cbus1}$) is determined using equation 6 as well as the electrical signals of Q2a (I_d and V_{ds}) measured during the turn off (Figure 8b). L_m is the parasitic of the SiC power module, L_C is the equivalent parasitic inductance of C_{bus1}, L_{screw}, is the parasitic inductance of the screw connection and L_{shunt} the shunt parasitic inductance. These parasitic inductances can be obtained from datasheet or can be calculated by estimation from the mechanical geometry.

$$L_{parT} = L_m + L_0 + L_{shunt} + L_{screw} + L_{cbus1} = \frac{\Delta V_{off\ overshoot}}{di/dt} \quad (6)$$



a) b)

Figure. 7: Evaluation parasitic inductance (L_p and L_0) using Double Pulse Test of the PEBB, a) electrical scheme of the DPT, b) V_{ds} and I_d of Q2a using obtained by DPT

Table 2: Comparison with other works

References	This paper	[7]	[11]
Power [kVA]	500	500	750
V_{dc} (DC bus voltage) [kV]	3.6	1	2
L_{par} [nH]= L_0 + L_p	14.5	6.5	78

The value of the short switching parasitic inductance loop of the busbar ($L_0 + L_p$) obtained is listed in Table 2. It is compared with other work in the same field for ANPC or NPC converter prototyping. The parasitic inductance obtained is lower than the case [11] with a NPC converter, the dimensions of the converter are larger (1 000 × 700 × 500 mm) compared to the Talent converter. However, the study in [7] shows a smaller parasitic inductance. This example uses different kinds of power modules (HT – 3 000 series), with a lower DC busbar voltage (1 kV) than the one in Talent project (3.6 kV).

3. Conclusion

In this paper, a busbar design comparison for a high power and medium voltage ANPC converter has been presented. To validate the methodology, a comparative study is carried out on several types of placement for the power modules around the busbars and the capacitors. Simulation results show that the triangular configuration of power modules reduces the most parasitic inductance of the switching loops. The analysis of the switching waveform obtained by the experimental results shows a total parasitic inductor of 14.5 nH lower as the simulated value (20.68 nH).
Next investigations will focuse on the SiC power modules switching losses measurements. Then gate resistors will be adjusted in order to increase the MOSFET switching speed in order to benefits the selected busbars and reduce the switching losses.

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