Operation and Performance of DC-DC Converter Using Multiple Cascaded Choppers for Future DC Power Grids

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***Abstract*-- This paper proposes an isolated dc-dc converter suitable for the application to future dc power grids and energy storage station. The dc-dc converter is based on the conventional three-phase dual-active-bridge (TP-DAB) converter where a three-phase Yn-Y transformer with a three-limb core and auxiliary converters based on multiple cascaded bidirectional choppers are connected to the primary side of the transformer. Unlike the TP-DAB converter that suffers from large converter current because of the so-called reactive current, the proposed converter can reduce RMS and peak currents in a wide range of operating conditions. The operating principles and control method of the proposed are introduced in this paper, followed by the comparison of the TP-DAB converter with the proposed converter in terms of RMS and peak currents. The feasibility of the proposed converter is verified using a 150 V, 2.5 kW downscaled prototype.**

***Index Terms*-- Dc power grids, energy storage, three-phase DAB converter, multiple cascaded bidirectional choppers.**

I. Introduction

The insufficiency of fossil fuels results in the fast development of renewable energy and dc power grid. Lots of countries are placing emphasis on renewable energy and the associated energy storage technologies as a national strategy [1]. For instance, the Chinese government has published some policies in 2021, which requires that the capacity of battery-based energy storage shall be 5%-20% of the installed capacity of the renewable energy generation [2]. On the other hand, according to the investigation and the statistic [3], at least 7446 GW photovoltaic (PV) systems have been installed by the end of 2020. Meanwhile, the newly installed PV systems account for 42% of new renewable electricity production. Hence, the renewable energy generation with PV as the mainstay and the battery-based energy storage will be the long-term trend on the world.

Recently, attention has been paid to dc power grids which features flexibility, high efficiency, and large capacity, and they can be used as sub-distribution systems or long-distance transmission systems mixed with ac power grids [4]-[8]. Further, the dc power grids are suitable for connecting different renewable different renewable energy sources with power consumption load since there is no concern about phase-locked loop (PLL) and harmonics distortion [4], [9]-[11].

The isolated dc-dc converter is utilized to establish the connection between the dc grid and the battery-based energy storage station [12]. The three-phase dual-active-bridge (TP-DAB) converter is a typical isolated dc-dc power converter with characteristics of simple control and bidirectional power transfer capability. However, the TP-DAB converter applying phase-shift control suffers from undesirable reactive current in the converter due to low power factor and harmonic currents [13]-[15]. The converter current should be suppressed as much as possible to reduce conduction losses in power devices and copper losses in the transformer.

To solve this problem, this paper proposes an isolated dc-dc converter based on multilevel power conversion technologies. The circuit is characterized in that the auxiliary converters with cascaded bidirectional choppers are added to the primary side of the TP-DAB converter. Further, a three-phase Yn-Y transformer with a three-limb core is used, where a dc current corresponding to the zero-sequence current flows in the primary winding of the transformer. As a result, both primary and secondary sides of converters can achieve unity-power-factor operation in all the operating ranges if attention is paid to the fundamental-frequency components. Consequently, the converter RMS and peak currents can be reduced. Moreover, a robust power flow can be achieved by applying the feedback power control to the converter. The operating principles and control method of the proposed converter are discussed in this paper. Besides, the comparison of TP-DAB with the proposed converter in terms of RMS and peak currents is carried out. Finally, the validity of the proposed converter is verified using a 150 V, 2.5 kW downscaled prototype.

II. Circuit Configuration and Operating Principles

A. Circuit Configuration and Basic Operation

The circuit configuration of the proposed dc-dc converter is shown in Fig. 1. The converter is isolated by a three-phase Yn-Y transformer with a voltage ratio of n. For convenience, the left part of the converter is hereafter defined as the primary side while the right part of the converter is defined as the secondary side.

There are two three-phase full bridges configured in the primary and secondary sides of the circuit; the main converter 1 (Q_1 - Q_6) and the main converter 2 (Q_7 - Q_{12}),

where v_{Mu1} and v_{Mu2} are the low-side voltages of the u-phase main converters. The auxiliary converter is formed by the multiple cascaded choppers which are series-connected between each phase of the main converter 1 and that of the transformer. In Fig. 1, the cascade quantity (N) of the auxiliary converter in each phase is set to 3. Although the following explanation assumes that $N = 3$, the operating principles and analysis can be applied to the cases with any cascade quantity.

In Fig. 1, v_{au}, v_{av}, and v_{aw} are the voltages of the auxiliary converters; v_{cu1}, v_{cu2}, and v_{cu3} are the dc-capacitor voltages of the u-phase auxiliary converter; v_{Lu}, v_{Lv}, and v_{Lw} are the inductor voltages; i_{u1}, i_{v1}, and i_{w1} are the primary currents; i_n is the neutral current; v_{tu1} and v_{tu2} are the primary and secondary voltages of the u-phase transformer; i_{u2}, i_{v2}, and i_{w2} are the secondary currents. In addition, a dc current is superimposed on i_{u1}, i_{v1}, i_{w1} and i_n when $V_{dc1} \neq nV_{dc2}$ while it is zero when $V_{dc1} = nV_{dc2}$. Meanwhile, i_{u2}, i_{v2}, and i_{w2} only contain ac components regardless of the relationship of V_{dc1} and V_{dc2}. The auxiliary converters play a role in power regulation by controlling the primary currents.

The switching frequency of the main converters is f_{s1}, and all the power devices operate with a fixed duty ratio of 0.5. In addition, each power device of the main converter 1 operates synchronously with the corresponding power device of the main converter 2. Specifically, the following relationship holds in the logic signals of the u-phase power devices:

$$\begin{cases} S_{Q1} = S_{Q7} = \overline{S}_{Q4} = \overline{S}_{Q10} = 1 \ (0 \le t < \dfrac{1}{2f_{s1}}) \\ S_{Q1} = S_{Q7} = \overline{S}_{Q4} = \overline{S}_{Q10} = 0 \ (\dfrac{1}{2f_{s1}} \le t < \dfrac{1}{f_{s1}}) \end{cases}, \quad (1)$$

where S_{Q1}, S_{Q4}, S_{Q7} and S_{Q10} donate the gate logic signals of Q_1, Q_4, Q_7 and Q_{10}, respectively. The power devices of the main converters in v-phase (Q_2, Q_5, Q_8 and Q_{11}) and w-phase (Q_3, Q_6, Q_9 and Q_{12}) follow the similar logics, while a phase difference of 120° exists in each phase.

The following voltage equation holds in the transformer:

$$v_{tu1} = nv_{tu2}. \quad (2)$$

Furthermore, the following relationship is obtained from KVL as

$$v_{au} = v_{Mu1} - v_{tu1} - v_{Lu}. \quad (3)$$

v_{au} can be divided into $(v_{au})_x$ and $(v_{au})_y$ in (3), where $(v_{au})_x$ is equal to $(v_{Mu1} - v_{tu1})$ and $(v_{au})_y$ is equal to $(-v_{Lu})$. $(v_{au})_x$ contains the following four voltage levels as

$$(v_{au})_x = \begin{cases} (1 - \dfrac{n\gamma}{3})V_{dc1} & \text{(level 1)} \\ (1 - \dfrac{2n\gamma}{3})V_{dc1} & \text{(level 2)} \\ \dfrac{n\gamma}{3}V_{dc1} & \text{(level 3)} \\ \dfrac{2n\gamma}{3}V_{dc1} & \text{(level 4)} \end{cases}, \quad (4)$$

where the coefficient γ is given by

$$\gamma = \frac{V_{dc2}}{V_{dc1}}. \quad (5)$$

TABLE I shows the output voltage levels of the auxiliary converters, where "H" means that the upper device of the main converter is on and "L" means that the lower device is on. For example, when the u-phase main converter is "H", the v-phase main converter is "L", and the w-phase main converter is "H", the output level of $(v_{au})_x$ should be "level 1", that of $(v_{av})_x$ should be "level 4", and that of $(v_{aw})_x$ should be "level 1". On the other hand, $(v_{au})_y$ is another part of v_{au} and it is used for the current control of i_{u1}. Hence, $(v_{au})_y$ can be given by

$$(v_{au})_y = -v_{Lu} = -L\frac{di_{u1}}{dt}, \quad (6)$$

where L is the total inductance which includes the leakage inductance of the transformer in each phase.

In Fig. 1, the phase-shifted pulse width modulation (PS-PWM) is applied to each auxiliary converter to reduce the harmonic components included in $(v_{au})_y$, $(v_{av})_y$, and $(v_{aw})_y$. Let the switching frequency of each chopper be f_{s2}, the equivalent switching frequency of the whole auxiliary converter f_{sa} is given by $3f_{s2}$ $(= Nf_{s2})$ and the relationship $f_{s2} > f_{s1}$ holds.

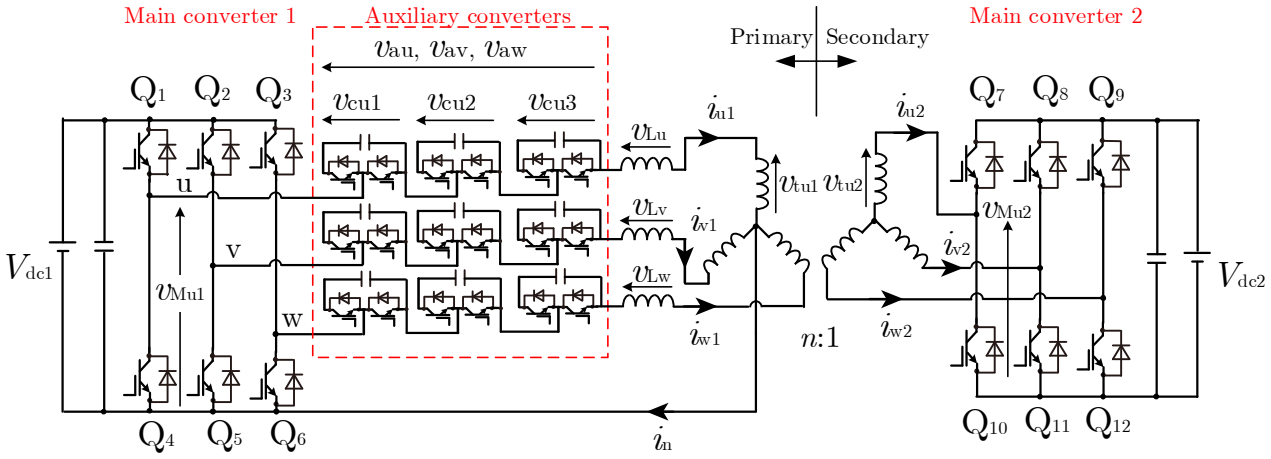
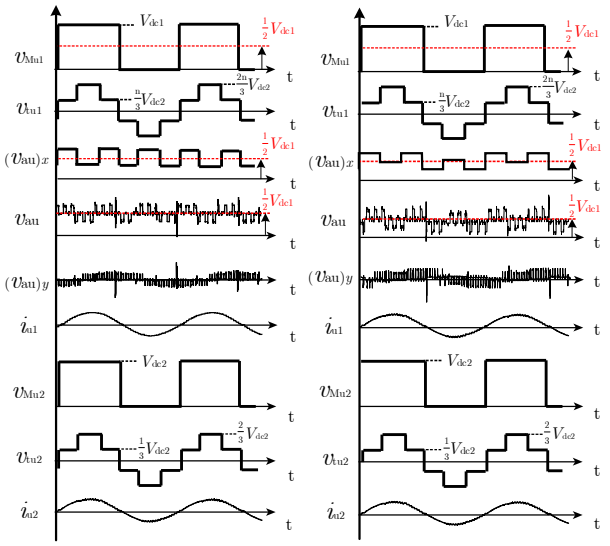


Fig. 1. Circuit configuration of the proposed dc-dc converter with a Yn-Y transformer. ($N = 3$)



(a) (b)

Fig. 2. Examples of operating waveforms obtained from computer simulation. (a) $n\gamma = 1$; (b) $n\gamma > 1$.

Fig. 2 shows waveform examples of the Fig. 1 circuit obtained from computer simulation when the power is sent from the primary side to the secondary side. Fig. 2(a) shows the case when $n\gamma = 1$ and Fig. 2(b) shows another case when $n\gamma \neq 1$. There are two big differences between Fig. 2(a) and Fig. 2(b). One is that $(v_{au})_x$ contains no frequency component of f_{s1} in Fig. 2(a) while it contains the frequency component in the case of Fig. 2(b); the other one is that a dc component is included in the primary current i_{u1} in Fig. 2(b) while it is zero in Fig. 2(a). The dc component will be derived in the next section.

B. Derivation of DC Component

As mentioned in the previous section, an amount of dc component is included in each primary current when $n\gamma \neq 1$. Let i_{u1} be the sum of ac component i_{acu} and dc component i_{dc} as

$$i_{u1} = i_{acu} + i_{dc} = I_{ac}\sin(\omega t) + i_{dc}, \qquad (7)$$

where the angular frequency ω is given by $\omega = 2\pi f_{s1}$ and I_{ac} is the amplitude of the sinusoidal ac component. It should be noted that the switching-ripple component in i_{u1} is not considered in (7). The following relationship between i_{acu} and i_{u2} holds as

$$i_{acu} = \frac{1}{n} i_{u2}. \qquad (8)$$

On the other hand, v_{Mu1} and v_{Mu2} can be expressed as

$$v_{Mu1} = \frac{1}{\gamma} v_{Mu2} = \begin{cases} 0 & -\pi < \theta \le 0 \\ V_{dc1} & 0 < \theta \le \pi \end{cases}. \qquad (9)$$

The circuit loss is not considered so that the following relationship regarding one-period average power holds in the u-phase circuit:

$$\frac{1}{2\pi}\int_{-\pi}^{\pi} i_{u1} v_{Mu1} d\theta = \frac{1}{2\pi}\int_{-\pi}^{\pi} i_{u2} v_{Mu2} d\theta. \qquad (10)$$

Substituting (7), (8), and (9) into (10) yields

TABLE I
OUTPUT VOLTAGE LEVEL OF AUXILIARY CONVERTERS

u	v	w	$(v_{au})_x$	$(v_{av})_x$	$(v_{aw})_x$
H	L	H	Level 1	Level 4	Level 1
H	L	L	Level 2	Level 3	Level 3
H	H	L	Level 1	Level 1	Level 4
L	H	L	Level 3	Level 2	Level 3
L	H	H	Level 4	Level 1	Level 1
L	L	H	Level 3	Level 3	Level 2

$$i_{dc} = I_{dc} = I_{ac}\frac{2}{\pi}(n\gamma - 1). \qquad (11)$$

This equation means that there is no dc component when $n\gamma = 1$. On the other hand, a positive dc current is superimposed on i_{u1} when $n\gamma > 1$ while a negative dc current is superimposed on i_{u1} when $n\gamma < 1$. Furthermore, the neutral current i_n can be given by $i_n = i_{u1} + i_{v1} + i_{w1}$. The ac components included in i_{u1}, i_{v1}, and i_{w1} are canceled each other out and only a dc component is contained in i_n. From the symmetry of the circuit operation, i_{v1} and i_{w1} produces the same dc current as i_{u1} expressed by (11). Hence, the neutral current i_n can be given by

$$i_n = I_n = 3i_{dc} = I_{ac}\frac{6}{\pi}(n\gamma - 1). \qquad (12)$$

III. CONTROL STRATEGY

The control strategy of Fig. 1 circuit can be divided into three parts as follows:

A. Inductor Current Control

The inductor current control and dc-capacitor voltage control of each phase are independent so that only the u-phase auxiliary converter control is discussed in the following, the block diagram of which is shown in Fig. 3.

The reference for the u-phase inductor current i_{u1}^* is given by

$$i_{u1}^* = i_{ac}^* + i_{dc}^*, \qquad (13)$$

where i_{ac}^* and i_{dc}^* represent the ac component and the dc component of i_{u1}^*. i_{ac}^* is set to generate a sinusoidal inductor current that is in phase with the fundamental component of v_{Mu1} and v_{tu1} as shown in Fig. 2. However, the amplitude drop and phase delay occur between the control signal and the actual inductor current with the conventional P control. To solve this problem, the compensation method is applied to i_{ac}^* which can be given by

$$i_{ac}^* = I_{ac}^*\sin(\omega t) + \frac{\omega L I_{ac}^*}{K_p}\cos(\omega t), \qquad (14)$$

where K_p is the proportional gain of the P controller in the current control part. The first term on the right-hand side in (14) donates the desired ac component while the second term $\omega L_1 \cos(\omega t)/K_p$ is used for the compensation. Meanwhile, i_{dc}^* is determined by the feedback control of the dc-capacitor voltages, which will be explained in the next section. Furthermore, to improve

the current control, v_{du} is added for the dead-time voltage compensation, which is given by

$$v_{du} = \mathrm{sgn}(i_{u1})\frac{T_d}{T_{s2}}V_c^* = \mathrm{sgn}(i_{u1})T_d f_{s2}V_c^*, \quad (15)$$

where T_d and T_{s2} represent the dead time and the switching period of the auxiliary converters, respectively. Moreover, $\mathrm{sgn}(i_{u1})$ is the signum function of i_{u1} which is equal to +1 when $i_{u1} > 0$ and -1 when $i_{u1} \le 0$.

B. Overall Voltage Control

The dc-capacitor voltage control is divided into overall voltage control and individual balancing control as shown in Fig. 3.

The aim of the overall voltage control is to regulate the arithmetic average value of the dc-capacitor voltages in each auxiliary converter, and this can be achieved by adjusting the dc component of the inductor current. Firstly, the arithmetic average value of the dc-capacitor voltages in each auxiliary converter is calculated. Then, the reference value of the dc component (i.e., i_{dc}^*) is generated from the feedback control as demonstrated in Fig. 3. The analysis and detailed calculations of the dc component in each phase and neutral point are introduced in Section II. . However, the zero-sequence current does not affect the transformer operation when a three-limb core is used as mentioned in Section II. .

C. Individual Balancing Control

The aim of the individual balancing control is to balance the dc-capacitor voltage of each chopper to the arithmetic average value regulated by the overall voltage control. The input of the PI controller is the difference between the arithmetic average value of the dc-capacitor voltages and each dc-capacitor voltage. On the other hand, the polarity of the output of the PI controller is changed according to the signum function of i_{u1} .

Finally, the sum of the output used for the current and voltage controls is normalized by the corresponding dc-capacitor voltage and the duty ratio of each chopper (i.e., d_{u1} , d_{u2} , and d_{u3}) is produced as shown in Fig. 3.

IV. Comparison of Inductor Current between TP-DAB Converter and Proposed Converter

This section compares the TP-DAB converter applying phase-shift control with the Fig. 1 circuit in terms of RMS inductor current and peak inductor current. In the TP-DAB converter, an additional current, which is called as reactive current, flows in the circuit, and it results in larger RMS and peak inductor currents and larger power losses. On the other hand, an amount of dc current flows in the Fig. 1 circuit when the relationship $n\gamma \neq 1$ holds, and it also produces larger RMS and peak inductor currents and larger power losses. Hence, a detailed comparison of the converters should be carried out.

It should be noted that the basic operating principles of TP-DAB converter are given in [16]; the calculations of RMS current, peak current are based on [16]. On the other hand, the following relationship of the Fig. 1 circuit can be derived from (7), (8), (9), and (10) in Section II. :

$$I_{ac} = \frac{\pi}{3n\gamma V_{dc1}}P_o, \quad (16)$$

where P_o donates the output power. Then, the u-phase inductor current i_{u1} can be presented using P_o as

$$i_{u1} = \frac{\pi}{3n\gamma V_{dc1}}P_o\left[\sin(\omega t) + \frac{2}{\pi}(n\gamma - 1)\right]. \quad (17)$$

Hence, the RMS value of i_{u1} can be calculated as

$$I_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi}(i_{u1})^2 d\theta} = \frac{\sqrt{4\pi(n\gamma-1)^2 + \frac{1}{2}\pi^2}}{3n\gamma V_{dc1}}P_o. \quad (18)$$

Similarly, the peak value of i_{u1} can be calculated as

$$I_{peak} = \frac{\pi}{3n\gamma V_{dc2}}\left[1 + \left|\frac{2}{\pi}(n\gamma - 1)\right|\right]P_o. \quad (19)$$

The following conditions are set to carry out the fair comparison:

- Both converters use the same switching frequency of the three-phase bridges as $f_{s1} = 450$ Hz, the same inductance of $L = 0.5$ mH, the same input dc voltage of $V_{dc1} = 1.5$ kV and the same transformer turns ratio of $n = 1$.
- The inductor loss and the iron loss of the transformer are not considered.

In addition, the switching frequency of the cascaded choppers is set to $f_{s2} = 3.6$ kHz; the dc-capacitor voltages

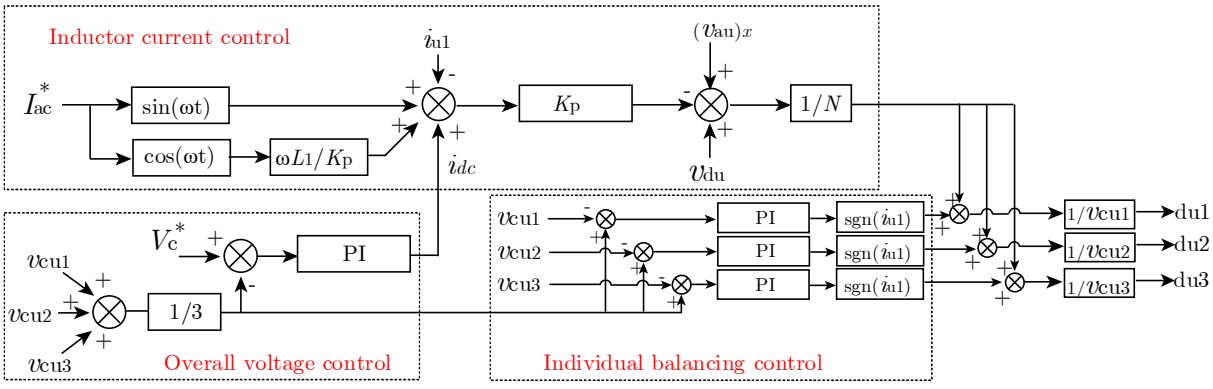


Fig. 3. Control block diagram of u-phase auxiliary converter.

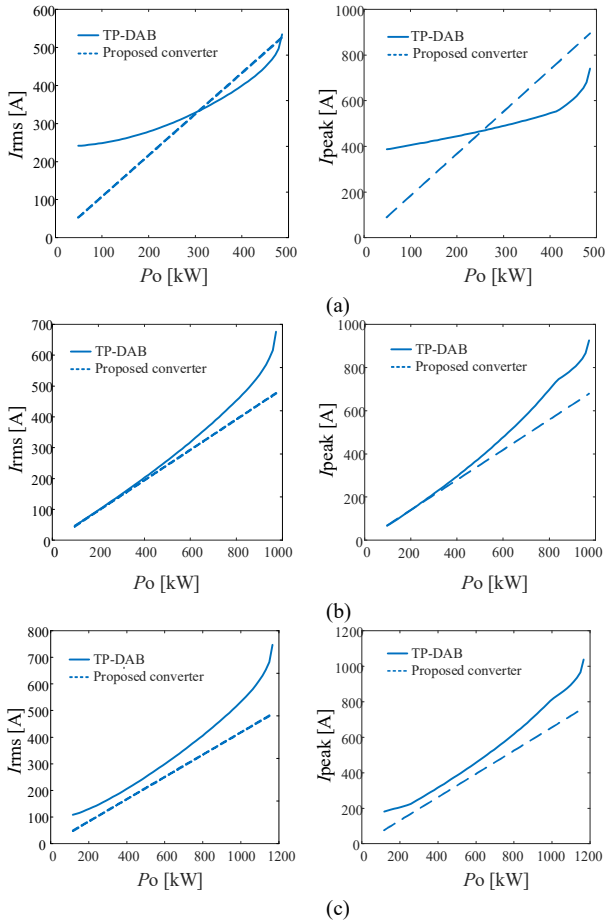


Fig. 4. Comparison of RMS and peak currents under different output power. (a) $n\gamma = 0.5$. (b) $n\gamma = 1$. (c) $n\gamma = 1.2$.

are set to $V_c = 0.5$ kV; the cascade quantity is set to $N = 3$. Further, this paper defines the operation with $n\gamma < 1$ as "buck mode", that with $n\gamma > 1$ as "boost mode", and that with $n\gamma = 1$ as "equivalent mode".

Fig. 4 shows the comparison of RMS and peak inductor currents of TP-DAB and the Fig. 1 circuit under different output power. Specifically, Fig. 4(a), (b), and (c) show the cases of $n\gamma = 0.5$ (buck mode), $n\gamma = 1$ (equivalent mode), and $n\gamma = 1.2$ (boost mode), respectively. In addition, I_{rms} donates the RMS current and I_{peak} donates the peak current. Fig. 4 shows that the TP-DAB converter exhibits nonlinear relationship between P_o and $I_{\text{rms}} / I_{\text{peak}}$ as described in [16]. On the other hand, the Fig. 1 circuit exhibits linear relationship between P_o and $I_{\text{rms}} / I_{\text{peak}}$ as explained by (18) and (19).

The following conclusions can be obtained from Fig. 4:

1) In buck mode, the Fig. 1 circuit produces lower RMS and peak current in light-load condition;
2) In equivalent and boost modes, the Fig. 1 circuit produces lower RMS and peak currents in all load conditions.

It should be noted that the switching-ripple currents (i.e., Nf_{s2} component) are not taken into consideration when calculating the RMS and peak currents of the Fig. 1 circuit, because it is negligible compared with the fundamental and dc components, as will be demonstrated in the experimental results.

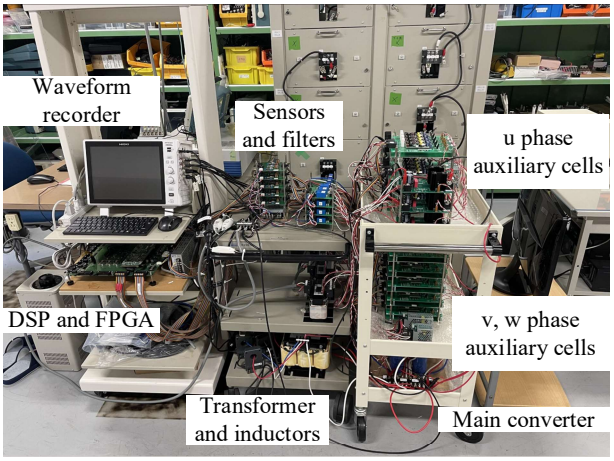


Fig. 5. Exterior of downscaled prototype for experimental verification.

TABLE II
SPECIFICATIONS OF DOWNSCALED PROTOTYPE

Cascade quantity	N	3
Switching frequency of main converters	f_{s1}	450 Hz
Switching frequency of choppers	f_{s2}	7.2 kHz
Winding turn ratio	n	1
Total inductance	L	0.29 mH
Input voltage	V_{dc1}	150 V
Rated power	P_e	2.5 kW

V. EXPERIMENTAL VERIFICATIONS

A. System Exterior and Configuration

To verify the feasibility and test the performance of the proposed converter, the downscaled prototype demonstrated as Fig. 5 is built for the 150 V, 2.5 kW experiment. IGBT modules (2MBI150U2A-060, 600 V / 150 A, Fuji Electric) and discrete MOSFETs (FDH44N50, 500 V / 44 A, Onsemi) were utilized to constitute the main converters and the auxiliary converters, respectively.

TABLE II shows the circuit parameters used for the experiments. The cascade quantity (N) is set to 3; the switching frequencies of the main converters and the choppers are set to $f_{s1} = 450$ Hz and $f_{s2} = 7.2$ kHz. The PS-PWM is applied to the auxiliary converters so that the equivalent switching frequency of entire auxiliary converter in each phase is 21.6 kHz ($= Nf_{s2}$). The winding turns ratio of the three-phase transformer is set to $n = 1$. The total inductance including the leakage inductance in each phase (L) is 0.29 mH. The dc input voltage is set to $V_{dc1} = 150$ V.

The control system is implemented by a DSP using TMS320C6678 from Texas Instruments and an FPGA using Cyclone IV from Intel. All the voltage and current waveforms were recorded using Hioki Memory Hicoder MR6000 shown in Fig. 5.

B. Steady-State Performance

Fig. 6 shows the steady-state experimental waveforms when the power is transferred from the primary side to the secondary side. In the experiment of Fig. 6, V_{dc2} was set

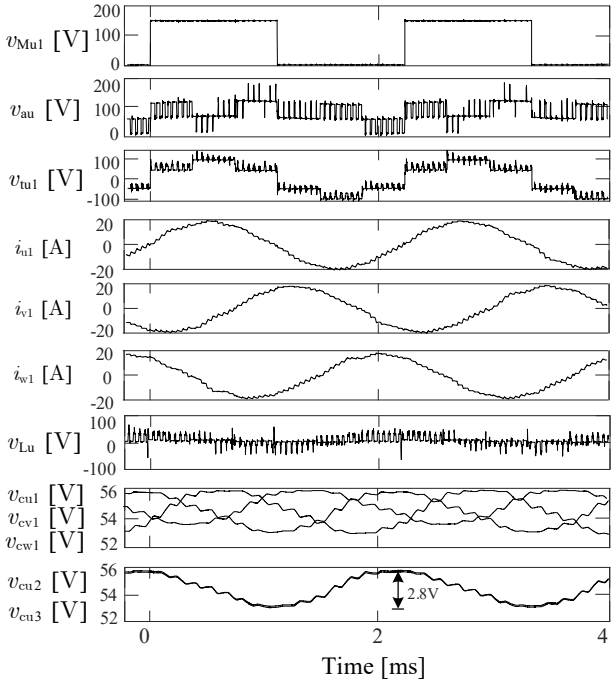


Fig. 6. Steady-state experimental waveforms when $V_{dc1} = 150$ V, $V_{dc2} = 130$ V, $V_c = 55$ V, $I_{ac}^* = 20$ A.

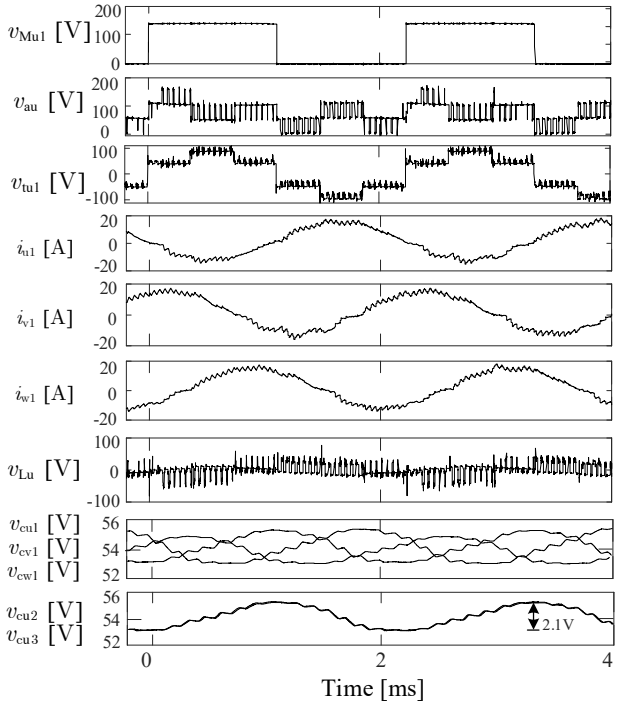


Fig. 7. Steady-state experimental waveforms when $V_{dc1} = 150$ V, $V_{dc2} = 140$ V, $V_c = 55$ V, $I_{ac}^* = -15$ A.

to 130 V; V_c was set to 55 V; I_{ac}^* was set to 20 A, which is simultaneously applied to u/v/w phase. The voltage waveforms of the dc capacitors in the auxiliary converters are kept at 55 V with a voltage ripple of 2.8 V. In addition, the u-phase dc-capacitor voltages (i.e., $v_{cu1,cu2,cu3}$) are almost same and a 120° phase difference for dc-capacitor voltage exists in each phase, e.g., v_{cu1}, v_{cv1}, and v_{cw1}, as shown in Fig. 6.

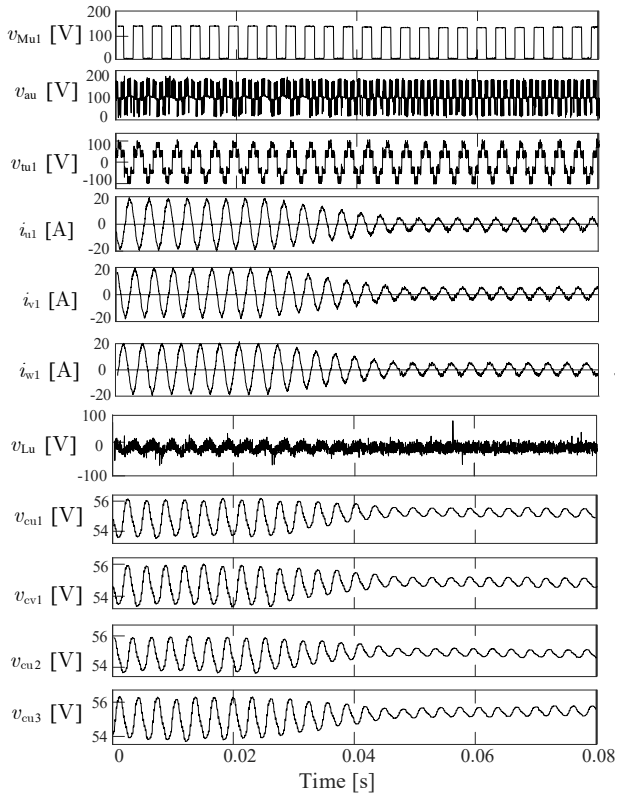


Fig. 8. Transient-state experimental waveforms when I_{ac}^* is changed from - 20 A to - 5 A at 0.02 s.

It can be observed that the inductor current i_{u1}, i_{v1}, and i_{w1} are sinusoidal and its amplitude is 20 A. Meanwhile, i_{u1} is simultaneously in phase with v_{Mu1} and v_{tu1} as described in Section II. .

Fig. 7 shows the steady-state experimental waveforms when the power is transferred from the secondary side to the primary side. V_{dc2} was set to 140 V; I_{ac}^* was set to -15 A. The sinusoidal inductor current with an amplitude of 15 A is confirmed; however, i_{u1} is out of phase with the fundamental-frequency components in v_{Mu1} and v_{tu1}, which means the direction of power transmission is reversed. The voltages of the dc capacitors in the auxiliary converters are also kept at 55 V with a voltage ripple of 2.1 V, which is similar to Fig. 6. Meanwhile, the amplitude of the voltage ripple is proportional to the output power and inversely proportional to f_{s1}.

The waveforms of v_{Mu1} and v_{au} basically match the simulated waveforms shown in Fig. 2. However, there are high-frequency switching-ripple components superimposed on the experimental waveforms of v_{tu1} while the theoretical v_{tu1} does not include the switching-ripple components. The reason is that the theoretical waveforms are given based on the ideal transformer while the actual transformer contains the leakage inductance. On the other hand, the switching-ripple voltages are superimposed on v_{au}, v_{tu1}, and v_{Lu} in Fig. 6 and Fig. 7. However, the switching-ripple currents on i_{u1}, i_{v1}, and i_{w1} are negligible since the high-frequency voltages (i.e., Nf_{s2} components) are filtered by L.

The steady-state experiments initially verify the basic operation and bidirectional transfer capability of the proposed converter. In addition, the validity of the control strategy shown in Fig. 3 has been experimentally verified.

C. Transient-State Performance

Fig. 8 shows the transient-state experimental waveforms with the same conditions of steady-state experiment when I_{ac}^{*} was changed from -20 A to -5 A. The Sudden change of the reference current started at 0.02 s. The gradual changes of current amplitude of i_{u1}, i_{v1}, and i_{w1} were observed from 0.02 s to 0.05 s, which means the entire transient state is completed within 30 ms.

With the effect of the control strategy of Fig. 3, the amplitude of inductor current in each phase are regulated from 20 A to 5 A corresponding to the change of reference value. On the other hand, the dc-capacitor voltages, e.g., v_{cu1}, v_{cu2}, v_{cu3}, and v_{cv1} recorded in Fig. 8 were always kept at 55 V during the entire transient state. In addition, no overshoot voltage or current are appeared according to Fig. 8.

VI. Conclusion

This paper has introduced a novel three-phase dc-dc converter, which can achieve unity-power-factor operation regarding the fundamental-frequency component. As a result, it can effectively reduce the RMS and peak currents in a wide range of operating conditions compared with the TP-DAB converter. The operating principles and control method have been discussed in this paper, followed by experimental verification using a 150V, 2.5kW downscaled prototype.

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