Ultra Low Loss – MMC Submodules favorable for SiC-FET enabling High Functional Safety

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***Abstract*—Further progress of Modular Multilevel Converters (MMC) is mainly related to advanced submodule topologies (SM), semiconductors (SiC) and improved control concepts. Fully electronic failure management for external failures (i. e. DC-short circuit) and protection against internal failures of the converter are key issues. A new submodule for MMC is presented, which meets these requirements. In addition, a novel SiC-JFET super-cascode is investigated, suitable for these and other applications.**

I. Introduction

Modular Multilevel Converters have revolutionized high power voltage source converters (VSC) and have become key components for future HV- and MV-DC-grids, the integration of wind and solar power into the grid and many other important future applications [1]–[4]. The elimination of bulky AC-filters and – more importantly – the elimination of large DC-capacitors from the DC-bus enables fully electronic failure management and protection. These important issues are twofold:

a) Management of external failures, especially electronic current limitation at the AC- and DC-side including overvoltage clamping
b) Management of internal failures, especially protection against explosion of semiconductors, arcing and mechanical damage at submodule level.

A submodule topology, which meets both requirements is investigated in this paper. Ultra low power loss and reduction of capacitor size is enabled, additionally [5]–[7]. The topology is suitable for combining Si- and SiC-semiconductors in a favorable manner. In the following paper, a realization using reverse conducting IGBT and one SiC-cascode switch will be investigated. For a fully SiC-implementation, which may be possible in the near future, even greater advantages – compared to Full-Bridge (FB)-SiC – are achieved [7].

II. Double-Zero Submodule: Modes of Operation

Fig. 1 shows the investigated Double-Zero submodule (DZ-SM). It uses four reverse conducting IGBT ($T_1/D_1 \ldots T_4/D_4$) and one reverse conducting SiC-switch (T_0/D_0). This switch can be implemented in several favorable manners. The most reasonable options are:

- SiC-MOSFET [8]
- SiC-JFET or SiC-SIT [9]
- SiC-JFET cascode switch [10]
- SiC-JFET super cascode switch [11]–[13].

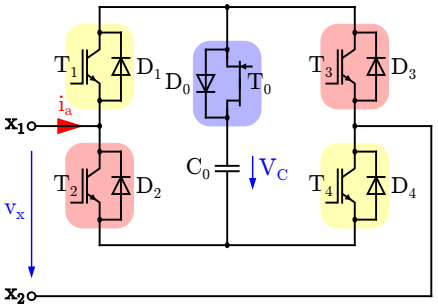


Fig. 1. Double-Zero submodule (DZ-SM)

With respect to development status of high voltage SiC-devices, mainly the first and the last option mentioned have to be considered. The superior current limiting characteristic of JFET (or SIT) combined with high temperature sustainability makes JFET a good choice under these conditions, here. Note that the decision between "normally on" and "normally off" behavior is not an essential issue for this topology.

The DZ-SM (see Fig. 1) meets essential requirements, which seem to be in contradiction, at first glance:

- Full-Bridge functionality with essentially reduced power-losses (see requirement a))
- Three independent semiconductor switches are in the critical "shoot through" path of the SM (see requirement b)).

For further explanation, Fig. 2 shows a typical arm current $i_a(t)$ and corresponding voltage modulation $d(t)$ of an MMC in inverter mode. Because there is no DC-power supply of the submodules in MMC, the energy and charge balancing enforces, that high arm current amplitudes always occur at low voltage modulations. Two intervals with charging the DC-capacitor (I and III) and two intervals with discharging (II and IV) can be distinguished for further analysis (see Tab. I).

A typical switching sequence in interval I is shown in Fig. 3: At zero terminal voltage ($v_x = 0\,\mathrm{V}$), the SiC-switch is kept in off-state and the silicon devices of the high- and low-side are sharing the arm current – reducing the on-state losses especially at high arm currents. In order to switch to the charging state ($v_x = +V_C$), the IGBT (T_2 and T_3) must be

turned off (at approx. half the arm current). When switching back to $v_x = 0\,\mathrm{V}$, these IGBT are turned on, again. This can be done very fast and with very low losses, because no compromise regarding Si-diode recovery is necessary. Evidently, the SiC-switch can be turned on in parallel to the SiC-diode structure to reduce the on-state losses (see right picture in Fig. 3).

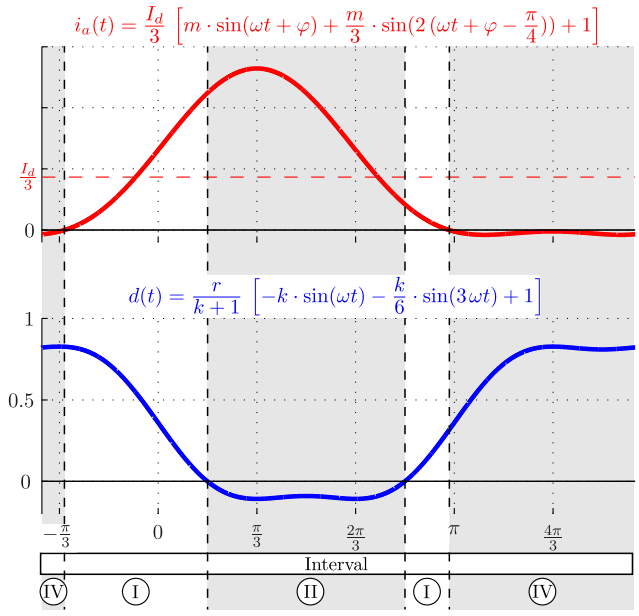


Fig. 2. Arm current $i_a(t)$ and corresponding voltage modulation $d(t)$ of an MMC in inverter mode ($\varphi = 30°$; $k = 1.5$; $r = 0.9$)

TABLE I
SWITCHING SEQUENCES OF THE DZ-SM

Interval	sgn(i_a)	sgn(v_x)	sgn(i_C)	sgn(P_a)	Capacitor
I	⊕	⊕	⊕	⊕	charging
II	⊕	⊖	⊖	⊖	discharging
III	⊖	⊖	⊕	⊕	charging
IV	⊖	⊕	⊖	⊖	discharging

Fig. 4 shows the switching procedure in interval II, where only the SiC-device is switching. Hence, the switching losses are very low, too. Only at SiC-turn-on, reduced speed (with respect to recovery of the Si-diode structures) has to be accepted. The switching conditions in intervals III and IV are similar to I and II, respectively.

In summary, reduced power losses of the DZ-SM can be achieved in the order of minus 20% – compared to a full silicon FB-SM utilizing 3.3 kV semiconductor devices (compare 1st and 3rd bar in Fig. 5). The resulting on-state loss of the SiC-switch is low, caused by the low RMS-current at a typical voltage modulation of an MMC. Therefore, the required chip area of the SiC-switch is very small in comparison to the four main semiconductors [6], [7], [14]. Nevertheless, the improvement of the DZ-SM is even more essential (power loss reduction of minus 30%), when implementing in a fully SiC-version (compare 2nd and 4th bar in Fig. 5). Applying SiC-devices in a FB-SM is evidently not a favorable choice since no conduction loss improvement is achievable with this topology.

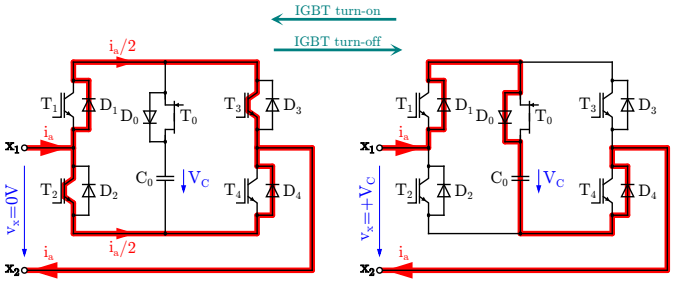


Fig. 3. Switching sequence in Interval I (see Tab. I)

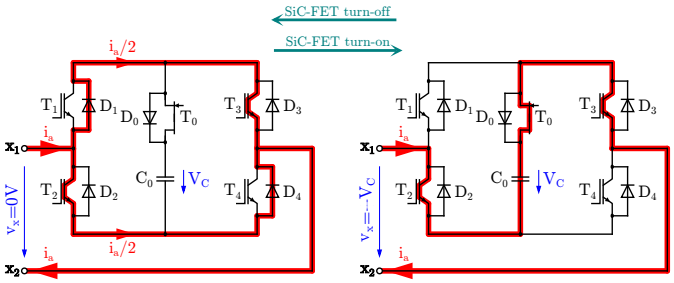


Fig. 4. Switching sequence in Interval II (see Tab. I)

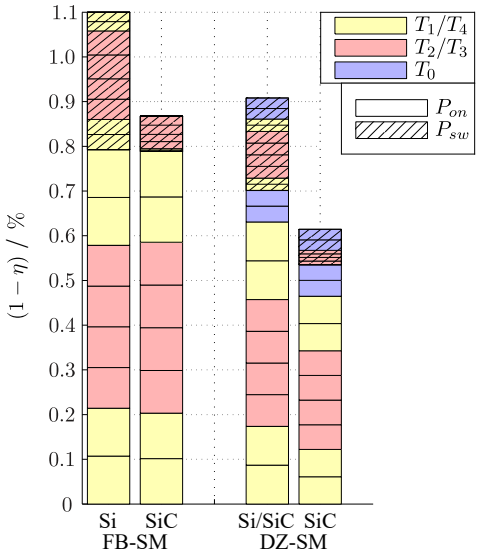


Fig. 5. Normalized submodule power losses (considering only DC- and fundamental components of current and voltage modulation[1]) utilizing 3.3 kV semiconductor devices ($I_d = 2.6\,\mathrm{kA}$; $k = 1.5$; $r = 0.9$; $\varphi = 30°$; IGBT: $U_{T0} = 1.2\,\mathrm{V}$; $R_T = 0.75\,\mathrm{m\Omega}$; FET: $R_{DSon} = 1.5\,\mathrm{m\Omega}$; $f_p = 150\,\mathrm{Hz}$). The colors in the bar graphs are indicating the power losses of the corresponding semiconductor devices in Fig. 1.

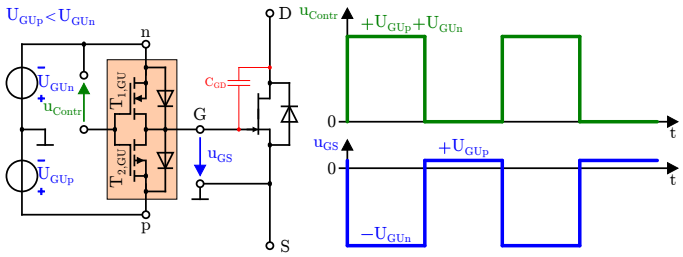
[1] m: current modulation factor, k: voltage modulation factor, r: utilization factor of the MMC arm, f_p: semiconductor switching frequency [7]

III. Cascode Switch

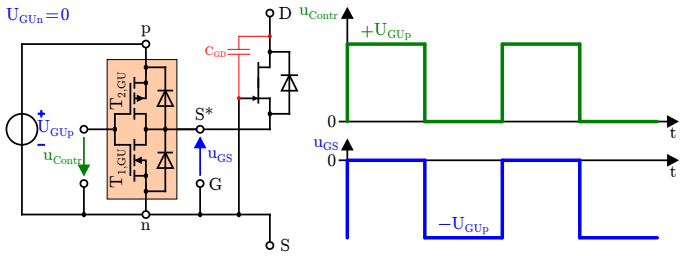
Cascode switches are well known to be favorable for high voltage applications. However, the realization of the low voltage switch was considered as an essential drawback in the past. Tremendous development progress of low voltage silicon FET has changed this situation, completely. The choice between a "standard" gate driver (a) and a "cascode type" gate driver (b) can be explained according to Fig. 6. Both choices have one specific main drawback:

a) The Miller capacitance (C_{GD}) slows down switching speed and aggravates problems with parasitic high frequency oscillations.
b) The n-channel FET of the gate driver circuit ($T_{1,GU}$ in Fig. 6) has to carry the full load current.

Solely, if the small p-channel FET of the gate driver is omitted, additional differences in switching performance occur. On the other hand, these issues are usually not mandatory.



(a) "Standard" gate driver



(b) "Cascode type" gate driver

Fig. 6. Conventional gate drivers of JFET semiconductors

IV. State of the art Super-Cascodes

Generally, super-cascodes – as stacked cascodes – are favorable topologies to achieve higher blocking voltages by internal series connection of semiconductors. In this way, conduction losses can be reduced compared to single semiconductor chips with a high blocking voltage capability. On the contrary, these advantages are coming with a higher complexity of the circuit as well as general challenges for the symmetrical distribution of the semiconductor voltages.

Fig. 7 illustrates an overview of the state of the art SiC-JFET super-cascodes – shown in a three voltage stage implementation. The indices of the devices in the pictures clarify the affiliation to the voltage stages. The main terminals of the structure are indicated as gate (G), main-drain (MD) and main-source (MS).

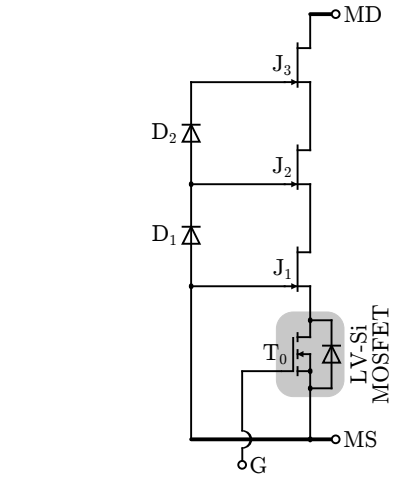
The first version of the super-cascode uses solely avalanche diodes between the gates of the JFET to balance the drain-source voltages (see Fig. 7(a)). The switching process of the different stages is generally sequential. To have a closer look at the super-cascode turn-on process, it can be recognized that the switching is initiated by turning on the low voltage MOSFET T_0. The decaying of its drain-source voltage leads to the exceeding of the (negative) pinch-off voltage of J_1 and therefore also to its turn-on. Since the gate potential of J_2 is initially kept constant, a decay of the drain-source voltage of J_1 leads to the conducting of J_2 as well. This mechanism continues until all transistors in the main path are turned on. The turn-off sequence advances from the bottom to the top stage as well. It can be understood from Fig. 7(a) that the sequential turn-off is mainly dependent on the breakdown voltage of the avalanche diodes. This and the absence of a defined reverse current path through the whole main circuit – since J_3 does not own an avalanche diode – is a fundamental drawback of this circuit.

The super-cascode concept from Fig. 7(b) is an improvement to the previous variant. On the one hand, utilizing RC-elements (R_1, C_1 and R_2, C_2) enables besides the static voltage distribution between the stages also a dynamic voltage distribution. On the other hand, the gate-source resistors R_{Di} counteract the aforementioned reverse current. The absence of a defined reverse current path through the whole main circuit is still problematic. Regarding the stacked structure – the reverse currents of the JFET decrease towards the lower voltage stages as the currents of the avalanche diodes increase – an asymmetrical design of the RC-elements is therefore resulting.

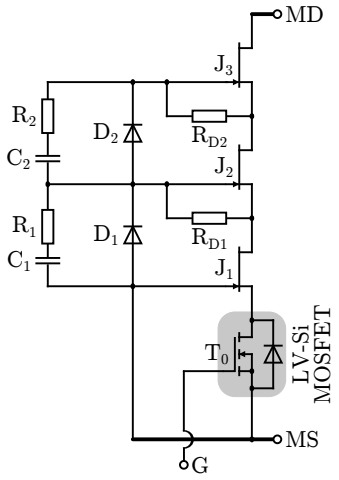
The super-cascode concept from Fig. 7(c) shows a variant with a distributed arrangement of the RC-elements. Due to the independent supply of the gate charge, this design is simpler as the previous version. The defined reverse current path through the whole main circuit represents another advantage compared to the latter version. On the contrary, the capacitor voltages are not identical – the voltage ratio of C_1 is $\frac{1}{3}$ and the voltage ratio of C_2 is $\frac{2}{3}$ to the total circuit voltage. An asymmetrical design is also the result of this super-cascode concept and limits the modularity.

The super-cascode concept from Fig. 7(d) illustrates a combination of the latter two variants – the resistors R_1 and R_2 are solely shifted into the gate path of the SiC-JFET. Series resistors R_{Di} increase the ruggedness of the avalanche diodes. The resistor R_3 ensures a defined reverse current path through the whole main circuit.

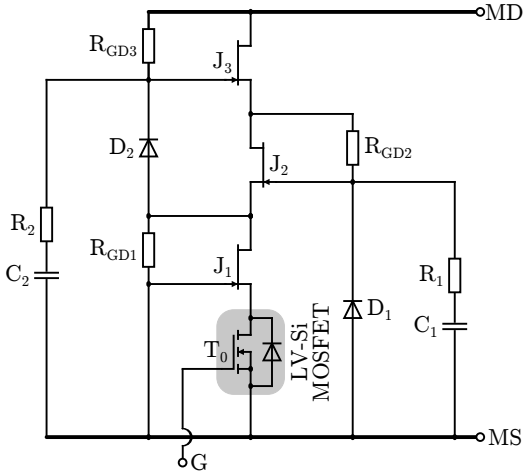
In Fig. 7(e) a super-cascode concept is shown, which looks different to the previous versions, at first glance. The bottom voltage stage is controlled by a HV-SiC-MOSFET with similar ratings to the main SiC-JFET, here. Nonetheless, T_1 could be replaced by a switching unit made of a HV-SiC-JFET and a LV-MOSFET, once more. A general improvement of this structure can therefore not be expected. The main advantage over the previous concepts is the completion of the RC-divider through the whole circuit. High resistor values R_{Si} ensure an improved voltage distribution in static state.



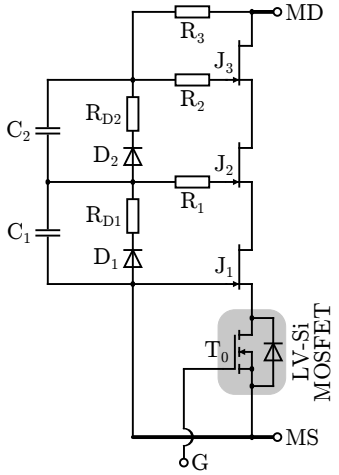
(a) Introduced by P. Friedrichs et al. [15]



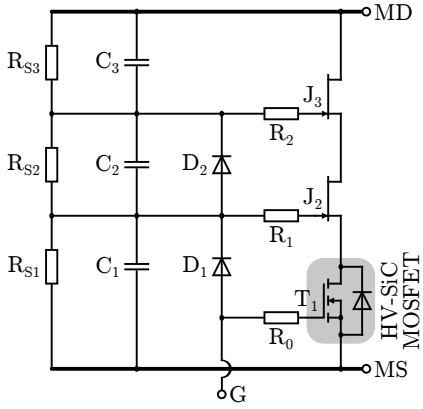
(b) Introduced by J. Biela et al. [16]



(c) Introduced by X. Li et al. [17]



(d) Introduced by B. Gao et al. [18]



(e) Introduced by X. Song et al. [19]

Fig. 7. State of the art SiC-JFET super-cascodes (three voltage stage implementation)

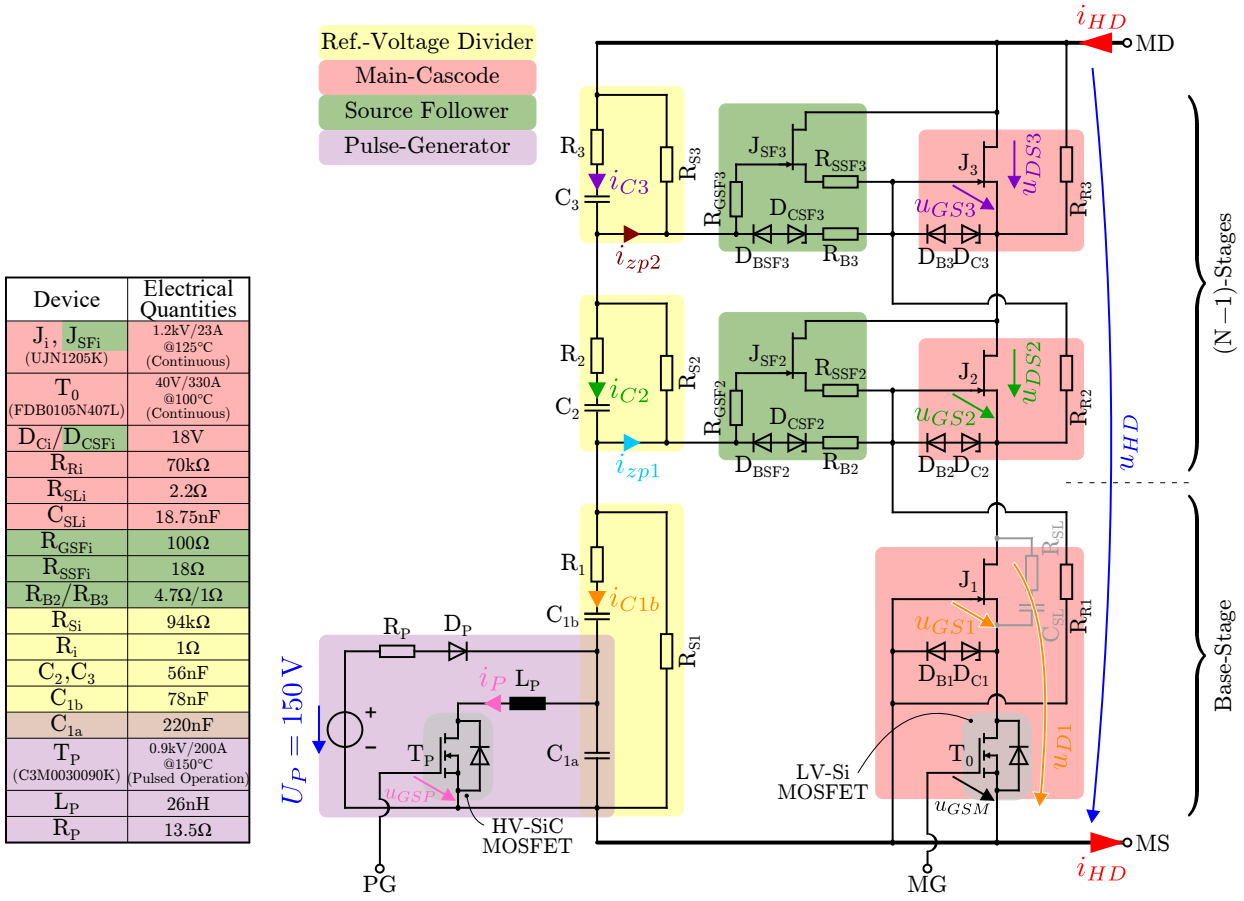


Fig. 8. Novel SiC-JFET super-cascode (three voltage stage implementation)

Regarding the state of the art SiC-JFET super-cascodes, general conclusions can be extracted:

a) The use of avalanche diodes to maintain symmetrical distribution between the voltage stages is disadvantageous. A reliable dimensioning of the current rating and defined reverse currents for the blocking state are critical with respect to semiconductor parameter scattering.

b) The "individual tuning" of the RC-elements to correct the switching sequence of the voltage stages is disadvantageous for industrial series production.

c) The switching sequence of the voltage stages at turn-off – the lower main JFET blocks first – is unfavorable, in principal. The resulting sequence is in contradiction to the balancing requirement of the main JFET – protective turn-on in order to limit individual overvoltage.

V. Novel SiC-JFET Super-Cascode

A. General structure and function

Fig. 8 illustrates the novel SiC-FET super-cascode which has been developed to eliminate the described disadvantages. An improved scalability – in order to enable high currents and voltages – and a uniform design with low sensitivity to component tolerances are achieved, too. An additional current path in the novel super-cascode enables the access to the upper main JFET to allow a favorable turn-off sequence of the voltage stages – the lower main JFET will be turned off after the blocking of the upper JFET is initiated. In addition to a high circuit efficiency, special focus was laid on a high degree of modularity of the super-cascode. High blocking voltages as well as high current rating can be achieved including overcurrent capability.

The novel super-cascode in Fig. 8 can generally be divided into a base-stage (including the driving of the LV-MOSFET) and the $(N-1)$-stages, which build up the super-cascode structure (these are all equipped identically). The circuit can be split into four specific function blocks. The reference-voltage divider and the main-cascode are also implemented in a similar form to the state of the art super-cascode topologies (see Fig. 7(b) to 7(e)). Additional function blocks in the novel topology are a source follower and a pulse-generator. The function blocks can generally be described as follows:

- Reference-voltage divider: The voltage divider is equipped with a dynamic component (R_i, C_i) as well as a static component (R_{Si}). Regarding the use of a source follower, the decoupling of the impedance between the main-cascode and the voltage divider can be achieved. In this manner, the components of the voltage divider can be

designed identically for every voltage stage. Due to the absence of a current path including an avalanche diode, the static component R_{Si} maintains a symmetrical voltage distribution in the blocking state of the super-cascode – resulting in low static power losses. It can be noted that the capacitor C_1 of the base-stage is split into C_{1a} and C_{1b} – the capacitance C_{1a} is providing the interface for the coupling of the pulse-generator.

- Main-cascode: The main-cascode consists generally of the SiC-JFET which conduct the load current and block the super-cascode voltage (the capacitor voltage V_C for application in the DZ-SM). The diode D_{Ci} limits the gate-source voltages to approx. 20 V ensuring safe operation of the main JFET. D_{Bi} blocks this path for positive currents (this will be explained in the segment of the source follower). R_{Ri} provides a quiescent current (from source-to gate-electrode) for the main JFET, which flows through the whole circuit. That way, the (slight) conducting of the main JFET can be avoided.
- Source follower: The function block of the source follower consists of two current paths – one for charging and one for discharging the upper SiC-JFET gates of the main-cascode. The positive path has an additional HV-SiC-JFET (J_{SFi}) and corresponding resistors. The gate charge for the transistor turn-on is provided through the drain-source path of J_{SFi}. Additionally, J_{SFi} raises the gate potential in the on-state, reducing the R_{DSon} of the upper main JFET. For discharging J_2 and J_3, the devices D_{BSFi} and R_{Bi} on the other hand maintain a connection to the RC-divider to evacuate their gates at turn-off.
- Pulse-generator: For an improved balancing between the different voltage stages at turn-off, a switching sequence has to be considered in such way, that the $(N-1)$-stages start to block before the base-stage (T_0 and J_1). The pulse-generator is located at the bottom of the voltage divider (coupled through the capacitor C_{1a}) and has to be initiated (PG) slightly before the main-gate (MG) is turned off. The capacitor C_{1a} is charged from an external (low current) voltage source – this will happen passively, if the super-cascode is in the conducting-state.

B. Switching sequence

To get a deeper understanding of the function of the novel super-cascode, the switching sequence shall be analyzed in this paragraph. Since the turn-on switching sequence of the main JFET – from bottom up – is generally not critical in super-cascodes, the focus will be set on the turn-off sequence, exclusively. Fig. 9 shows SPICE simulation results of the novel super-cascode at turn-off corresponding to Fig. 8 performing a hard commutation in a half bridge configuration with freewheeling diode under inductive load ($I_L = 100\,\mathrm{A}$; $U_{HD} = 1.4\,\mathrm{kV}$). The main JFET ($J_1$, J_2, J_3) are utilized with a parallel connection of 8 TO-247 semiconductor devices in every voltage stage – rated for 23 A per device (see table in Fig. 8). The instances of the turn-off sequence can be described as follows:

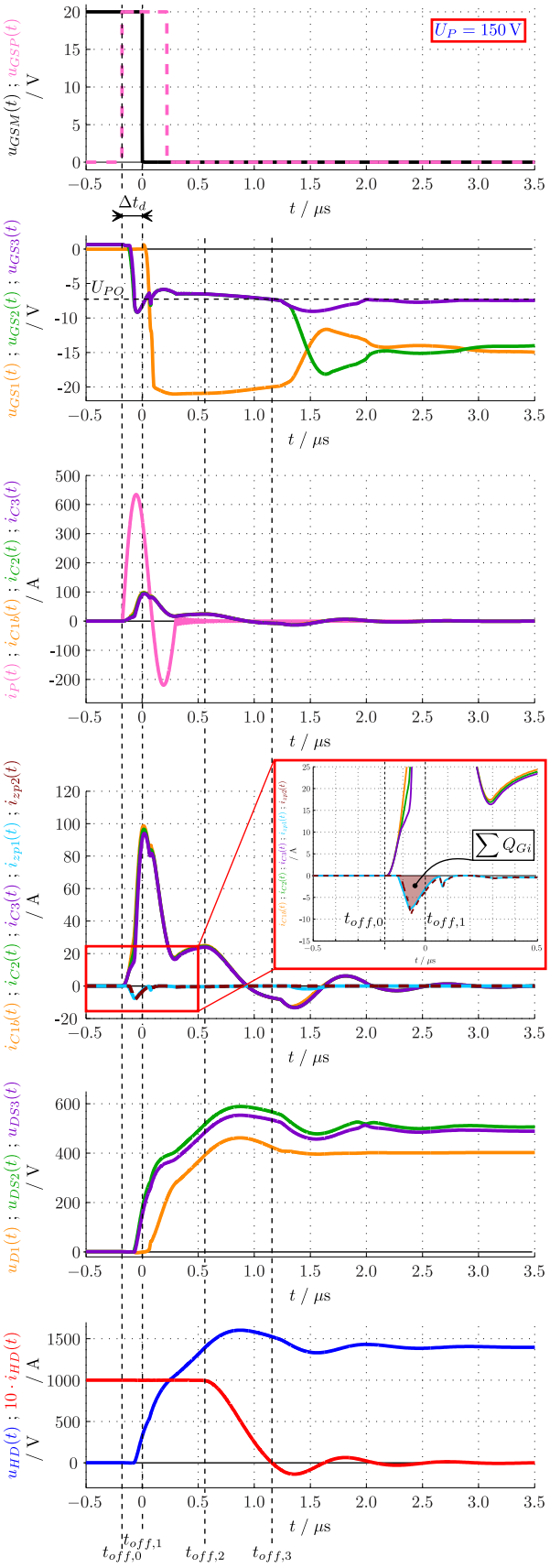


Fig. 9. Simulation of the main electrical quantities of the novel SiC-JFET super-cascode at turn-off ($I_L = 100\,\mathrm{A}$; $U_{HD} = 1.4\,\mathrm{kV}$)

- $t < t_{off,0}$: Before the initiation of the turn-off, the super-cascode is in conducting-state. It can be noted, that the gate voltages of the upper main JFET (u_{GS2} and u_{GS3}) show significantly positive values – provided by the source followers – advantageously.
- $t_{off,0} < t < t_{off,1}$: The turn-off sequence is initiated with a positive pulse of the pulse generator (u_{GSM}). The capacitor C_{1a} is discharged via the (small) loop inductance L_P and generates an impulse current i_P. A partial component of the current is extracted to the reference-voltage divider (i_{C1b}, i_{C2}, i_{C3}) resulting in a negative current of the upper gate-paths of the main JFET (J_2 and J_3) – clearing out their gate charge. The gate-source voltages u_{GS2} and u_{GS3} decay. When reaching the negative maximum of the currents i_{zp1} and i_{zp2}, the voltages u_{GS2} and u_{GS3} fall below their pinch-off voltage resulting in an increase of the drain-source impedance of J_2 and J_3. The voltages u_{DS2} and u_{DS3} increase therefore as well. It can be recognized, that the magnitudes of i_{C1b}, i_{C2} and i_{C3} are primary affected by the super-cascode current i_{HD}, which commutates in this time span to the reference-voltage divider – due to the raising of u_{DS2} and u_{DS3}. The simulation was done with an increased gate-source charge of $\sum C_{GSi} = 45.6\,\mathrm{nF}$ (instead of $8\,\mathrm{nF}$) to illustrate the suitability of the circuit for a high number of paralleled main JFET.
- $t_{off,1} < t < t_{off,2}$: Since J_2 and J_3 already blocking voltage, the main-gate will be turned off (u_{GSM}) – blocking also the JFET J_1 of the base-stage. It can be noted that u_{GS2} and u_{GS3} will rise above the pinch-off voltage once again resulting in a reduced drain-source-voltage slope due to the voltage increase of the voltage divider. Here, these voltages adjust themselves to maintain a quasi-conducting state enabling a uniform dynamic voltage distribution between the different voltage stages (u_{D1}, u_{DS2} and u_{DS3}) near the pinch-off threshold. For a practical realization, it can be favorable to limit the voltage slope of the base-stage (u_{DS1}) applying an RC-element (R_{SL} and C_{SL}, grayed out in Fig. 8) to the circuit. For a better comparison of the later shown experimental results, the optional RC-element was also implemented in the simulation.
- $t_{off,2} < t < t_{off,3}$: The super-cascode voltage u_{HD} reaches the blocking voltage of $1.4\,\mathrm{kV}$. At this instance, no voltage drop occurs at the freewheeling diode, initiating its conducting. The load current i_{HD} trough the circuit is now descending. Regarding the parasitic inductances in the commutation loop and the resulting negative current slope $\frac{\mathrm{d}i_{HD}}{\mathrm{dt}}$ an overshoot (of approx. $200\,\mathrm{V}$) can be noted. The transistors J_2 and J_3 still operate in a quasi-conducting state, enabling a controlled voltage distribution between u_{D1}, u_{DS2} and u_{DS3}.
- $t_{off,3} < t$: The current i_{HD} through the super-cascode is crossing zero – all the main JFET are blocking. A shifting of the upper gate-source voltages is stimulated by the turn-off voltage overshoot. After the decay of the oscillation, the gate-source voltages are pulled towards the static blocking state – via the current path through the resistors R_{Ri}.

Since the source followers are not completely blocking in the time span $t > t_{off,3}$, they supply a quiescent current what slows the clearing of the gate-charge (of J_2 and J_3) down. The opposing operation of the source followers (charging of the upper main JFET-gates) and the path through R_{Ri} (discharging of the upper main JFET-gates) was on the other hand not restricted in the circuit design. A compromise can be found between high switching frequency and steady state power losses. For the utilization of the novel SiC-JFET super-cascode in the capacitor switch of the DZ-SM (see T_0 in Fig. 1, 3 and 4) not more than two switching operations take place within a fundamental period of $20\,\mathrm{ms}$, typically.

C. Dimensioning

The dimensioning of the novel super-cascode will be briefly discussed in this paragraph. A specific focus is laid on the components of the reference-voltage divider and the pulse generator. The selection of the essential components of the main-cascode and the source follower is straightforward and is generally based on the current rating and voltage blocking rating of the super-cascode circuit application:

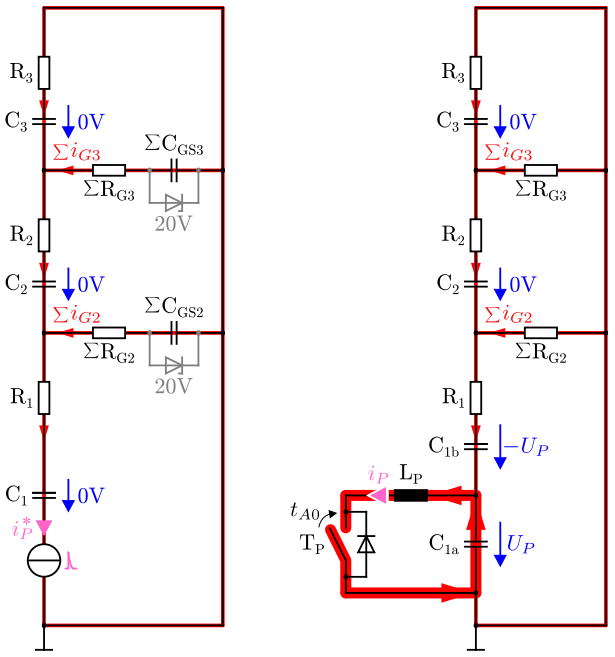
- C_i, R_i, R_{Si}: A basic approach for designing the voltage divider is to define an acceptable limit of energy loss in the capacitors C_i at super-cascode turn-off. The condition for one voltage stage (and $N = 3$) is:

$$C_i \leq \frac{I_L \cdot t_f}{\frac{U_{HD}}{N}}. \tag{1}$$

  For the investigated circuit, a fall time of $t_f = 500\,\mathrm{ns}$ was assumed resulting in a capacitance of approx. $100\,\mathrm{nF}$ – rounded down to $56\,\mathrm{nF}$ for higher ruggedness.
  The selection of the resistance R_i requires a compromise. On the one hand, a low-resistive design of the divider is necessary for minimal impairment of the pulse generator. On the other hand, oscillation at switching has to be dampened – stimulated by the parasitic loop inductances. A value of $R_i = 1\,\Omega$ complies with the aforementioned conditions and also keeps the initial voltage drop well below the per stage voltage:

$$R_i \cdot I_L \ll \frac{U_{HD}}{N}. \tag{2}$$

  The design of the resistance R_{Si} follows a compromise to assure accurate voltage distribution in static state of the super-cascode as well as low static power losses – a value of about $100\,\mathrm{k}\Omega$ is generally adequate.
- C_{1b}, C_{1a}: The most critical issue for designing the pulse generator is – for a sufficient embedding of the pulse generator into the voltage divider – the selection of the capacitances C_{1a} and C_{1b}. Here, it is constructive to separate the design into two steps (see Fig. 10):
  - Step A: Fig. 10(a) shows a simplified equivalent circuit of the novel super-cascode of Fig. 8 and



(a) Step A: Idealization of the pulse generator (b) Step B: Neglecting of the gate-source capacitances

Fig. 10. Equivalent circuit of the novel SiC-JFET super-cascode for the stepwise dimensioning of the pulse generator capacitances

illustrates the pulse generator as an ideal current source with the function of clearing the gate charge of the upper main JFET (J_2 and J_3) prior to the turn-off of the base-stage semiconductor (J_1). The pulse generator needs to provide the negative gate-currents $\sum i_{G2}$ and $\sum i_{G3}$ (of the paralleled JFET) to discharge $\sum C_{GS2}$ and $\sum C_{GS3}$ from $+2\,\mathrm{V}$ to $-18\,\mathrm{V}$ – indicated by the zener diodes. If the voltage at the capacitances C_i as well as the voltage drop at the main JFET are neglected, it can be assumed that the gate-source capacitances will be charged before a voltage raise at C_i is noted. For this matter, C_i need to have significantly larger values than the summarized gate-source capacitances. For a number of 8 paralleled JFET per stage, their ratio can be determined as follows:

$$\frac{C_i}{\sum C_{GSi}} = \frac{56\,\mathrm{nF}}{8\,\mathrm{nF}} \gg 1. \tag{3}$$

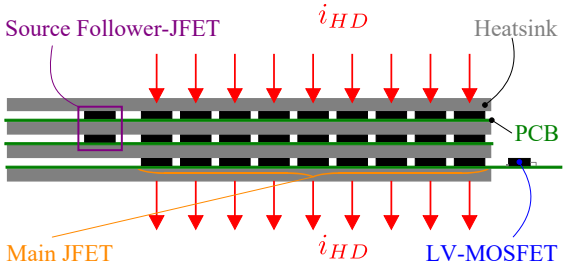
– Step B: Fig. 10(b) shows the integration of the pulse generator into the voltage divider. For an adequate decoupling of pulse generator and voltage divider, C_{1a} has to be greater than the series connection of C_{1b}, C_2 and C_3 (forming C_{ers}). Considering that the series connection of C_{1a} and C_{1b} has to be identical to C_i, the capacitors can be found to $C_{1a} = 220\,\mathrm{nF}$ and $C_{1b} = 78\,\mathrm{nF}$ leading to a ratio of:

$$\frac{C_{1a}}{C_{ers}} = \frac{220\,\mathrm{nF}}{20\,\mathrm{nF}} \gg 1. \tag{4}$$

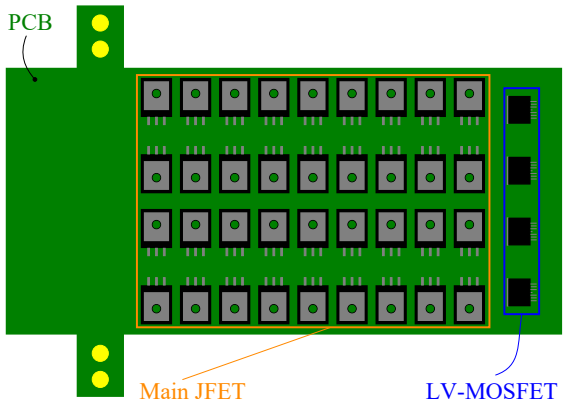
D. Prototype and measurement results

The general structure of a mechanical prototype of the novel SiC-JFET super-cascode is depicted in Fig. 11. The side view (see Fig. 11(a)) illustrates that the cascode-current flows vertically through the (per stage) assembly of:

1) Heatsink
2) Drain-contact of the main JFET (rear contact of the TO-247-package)
3) Source-contact of the main JFET (soldered to the PCB)
4) PCB (its back plane is fully contacted and mechanically pressed to the heatsink of the next voltage stage).



(a) Side view of the three voltage stages



(b) Top view of the (fully assembled) base-stage

Fig. 11. General structure of the mechanical prototype of the novel SiC-JFET super-cascode

The results of a double pulse test applying three voltage stages and 8 paralleled SiC-JFET per stage (connected to a freewheeling diode of a CM400HB-90H IGBT-module) are shown in Fig. 12, 13 and 14.

The oscilloscope graphs are clearly demonstrating the excellent behavior of the super-cascode at turn-off – maintaining uniform voltage distribution between the different voltage stages. The similarity of simulation and experiment verifies the result of the basic dimensioning as an adequate design indicator.

VI. Conclusion

The Double-Zero submodule enables improved functional safety in combination with essentially reduced power losses – compared to Full-Bridge submodules. It is well suitable for SiC-devices or a hybrid Si/SiC-realization. Fully electronic

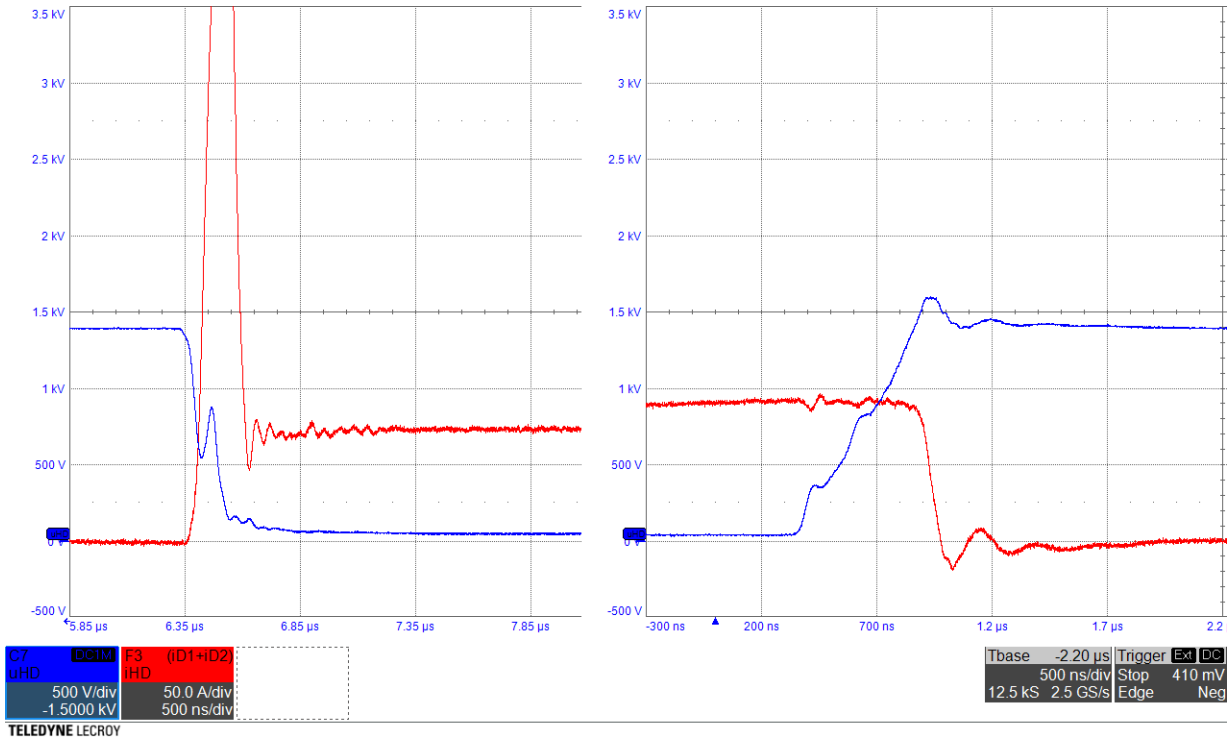


Fig. 12. Measurement of the turn-on (left picture) and turn-off (right picture) of the novel SiC-JFET super-cascode (u_{HD}, i_{HD})

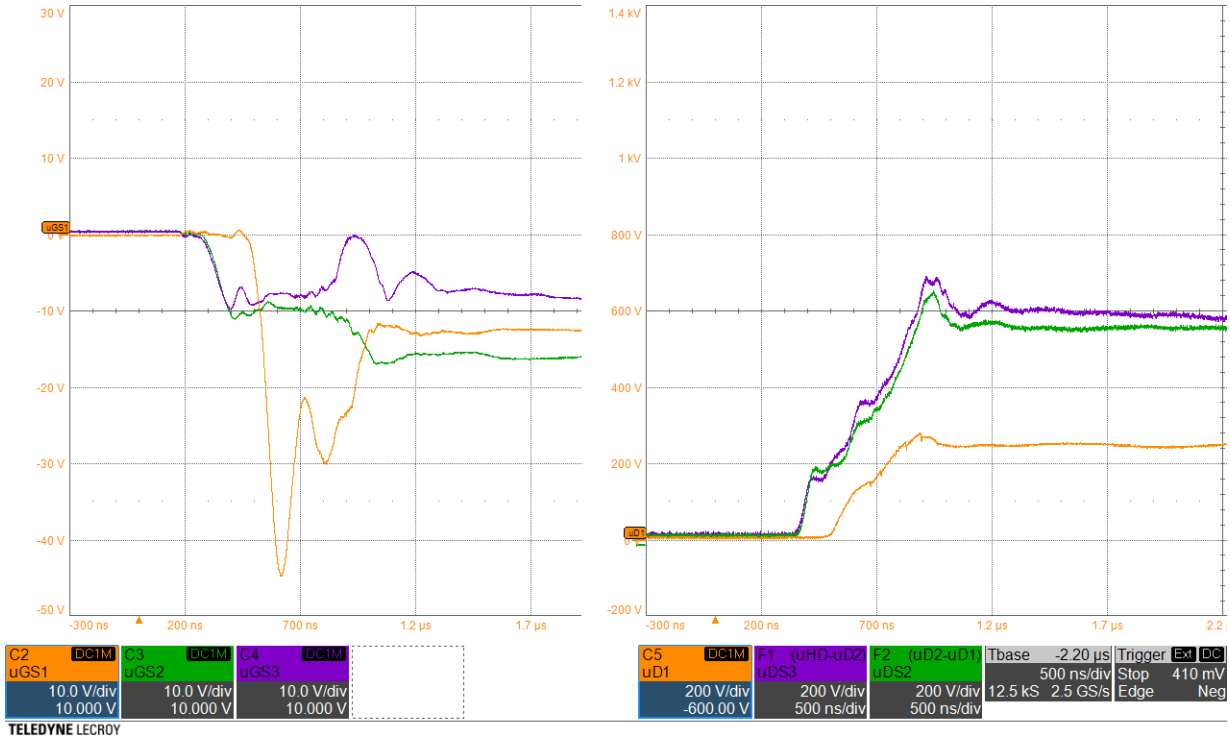


Fig. 13. Measurement of the gate-source voltages (left picture: u_{GS1}, u_{GS2}, u_{GS3}) and drain-source voltages (right picture: u_{D1}, u_{DS2}, u_{DS3}) at turn-off of the novel SiC-JFET super-cascode

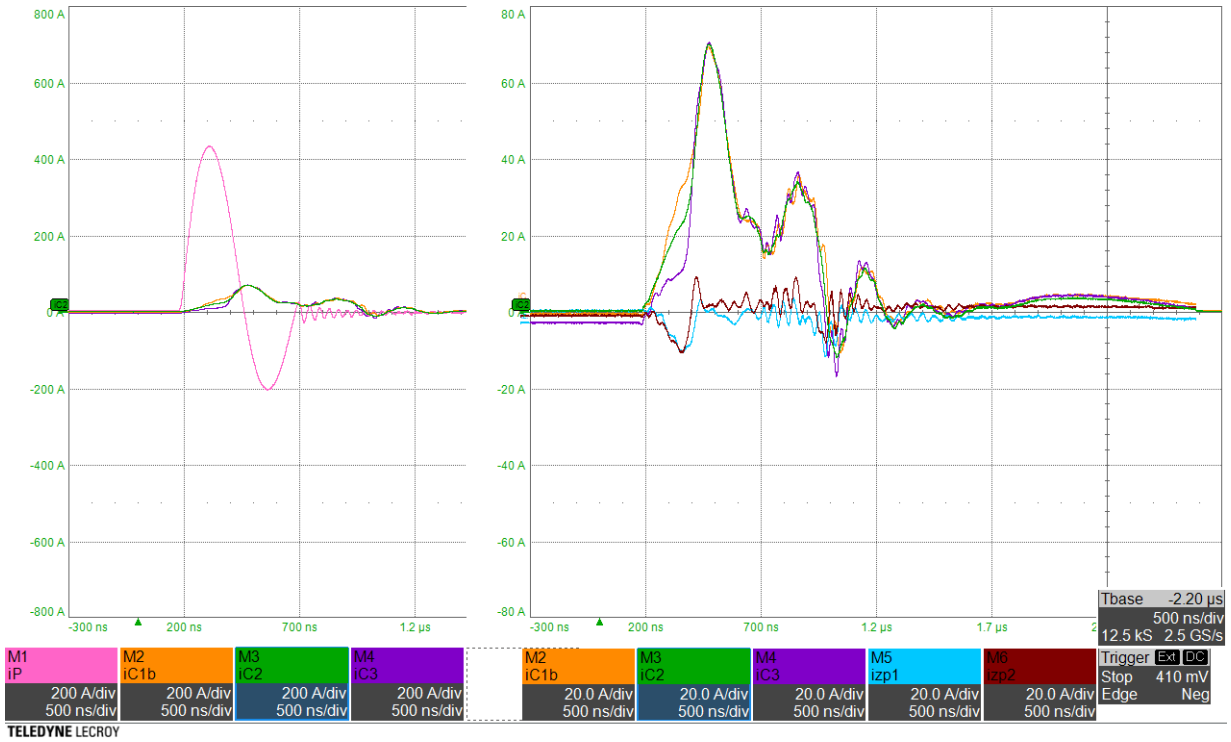


Fig. 14. Measurement of the currents inside the reference-voltage divider (i_{C1b}, i_{C2}, i_{C3}, i_{zp1}, i_{zp2}) of the novel SiC-JFET super-cascode (left picture: including the pulse generator current ; right picture: including the upper main JFET gate-paths currents)

failure management (incl. intrinsic protection against explosion of the submodule) in an MMC is achieved, too. Additionally, a novel SiC-JFET super-cascode is presented and investigated enabling the following improvements with respect to state of the art super-cascode topologies:

- A modular structure allows uncritical scalability of the blocking voltage as well as the current rating of the super-cascode enabling a suitability for highest cascode currents.
- A favorable turn-off sequence is enforced with an additional signal path (implemented with a pulse generator) to maintain a uniform, symmetrical voltage distribution of the drain-source-voltages.

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