Mega-hertz High-power WPT system with Parallel-connected inverters using current balance circuit

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Keywords

«Current balancing», «Transformer», «Gallium Nitride (GaN)», «Wireless power transmission», «High frequency power converter».

Abstract

This paper proposes a new current balancer for the megahertz WPT system. The proposed balancer achieves a current balance between the parallel connection inverter on the transmission side of the WPT system. The balancer consists of two transformers without any additional control to achieve a current balance. The output side of a conventional balancer is not isolated from the input side of the balancer. The proposed balancer isolates the output side and the input side of the balancer. A turn ratio of two transformers is derived by magnet flux under the current balancing condition. Furthermore, the proposed balancer also has the capability of the impedance matching. The leakage inductance of two transformers is applied to achieve an impedance matching with an additional capacitor. The experimental results reveal that the current balance is achieved even if the phase of the output voltage of each inverter has a difference of approximately 8 ns.

Introduction

In recent years, battery chargers have been developed rapidly by increasing the interest in small mobility, for example, drones. Notably, wireless power transfer (WPT) systems for battery chargers have been actively studied for safety and convenience [1–2]. Then, the rapid charging is required to reduce the charging time. Although, the WPT system charger takes a long time to charge the onboard batteries. Thus, increasing the output power of the WPT system to at least ten kilo watts is urgent.

On the other hand, the WPT systems with a transmission frequency of 85 kHz have been commonly used because the WPT system for EVs charger is normalized with 85 kHz. Although, over ten kilowatt system with 85 kHz is bulky and heavy as the charging system of the small mobility. One of the leading causes is a transfer coil. The transfer coil in 85 kHz has a ferrite core at a transmission coil and a receiver coil. Then, the cursing distance of the mobility is affected directly by the weight of the receiver coil that is mounted to the mobility.

Then, applying megahertz band frequency is one of the solutions to decrease the weight and the size of the transfer coil because the air-core coil is able to be applied as the transfer coil by using megahertz

frequency. Thus, the megahertz operation in the WPT system has been actively studied [3–8]. The WPT system employs a GaN device [9–10] to achieve the megahertz operation in a kilowatt order system.

Thus, the increase of the output power of the WPT system in megahertz operation is necessary for the small mobility. A parallel connection of the GaN devices or the inverter circuits [11–12] has been studied to achieve a kilowatt order system. Then, the current unbalance occurs between paralleled circuits or devices to delay the switching timing. The current unbalance causes thermal unbalance, which destroys the devices. Thus, the current balancing method is necessary for paralleled circuits or devices.

However, it is difficult to apply an accurate control to synchronize switching timings of each device or circuit still in the megahertz operation because the control period should be shorter than a few nano-second. Thus, the current balancing method should be composed of the passive components without additional current control. So far, a current balancer circuit for the paralleled inverters in megahertz operation has been studied [13]. The balancer consists of two transformers without any additional control. Although, the wire connection at the balancer circuit is complicate especially of the over three parallel configurations because the primary side is non-isolated from and the secondary side of the two transformers.

This paper proposes the new current balancer, including impedance matching capability, to increase the output power with the parallel connection inverters. The advantage of the proposed balancer is that the configuration of the circuit is simple, and it is easy to expand into the three paralleled configurations. Moreover, the proposed balancer has the capability of an impedance transform to match the impedance of the load. Thus, Zero-Voltage-Switching(ZVS) is achieved in the parallel-connected inverters in any load condition. First, the balance circuit is theoretically analyzed to derive the circuit parameters in the balance condition. Then, the operation of the proposed balance circuit and ZVS is demonstrated by the simulation and the fundamental experiments in the megahertz operation in the several conditions.

Conventional balancer circuit

Figure 1 shows the configuration of the parallel-connected inverter using a non-isolated balancer-[13]. The balancer consists of two transformers. The primary side of each transformer is connected to the output of each inverter. The secondary side of each transformer is connected to a transfer coil in series. Two transformers have the same design parameters and have no magnetic coupling with each other.

On the other hand, two transformers have a leakage inductance. The leakage inductance appears between the inverters and the transfer coil. Thus, the resonant capacitance should be modified to keep the resonant condition. When the leakage inductance has a large value, the voltage of the transfer coil is decreased even if the resonant condition is achieved by adjusting the resonant capacitance. Thus, the transfer power is regulated by the leakage inductance of the balancer circuit.

Proposed balancer circuit

Figure 2 shows the proposed configuration of the balancer circuit. The primary side and the secondary side of each transformer are isolated. The primary side of each transformer is also connected to the output of each inverter.

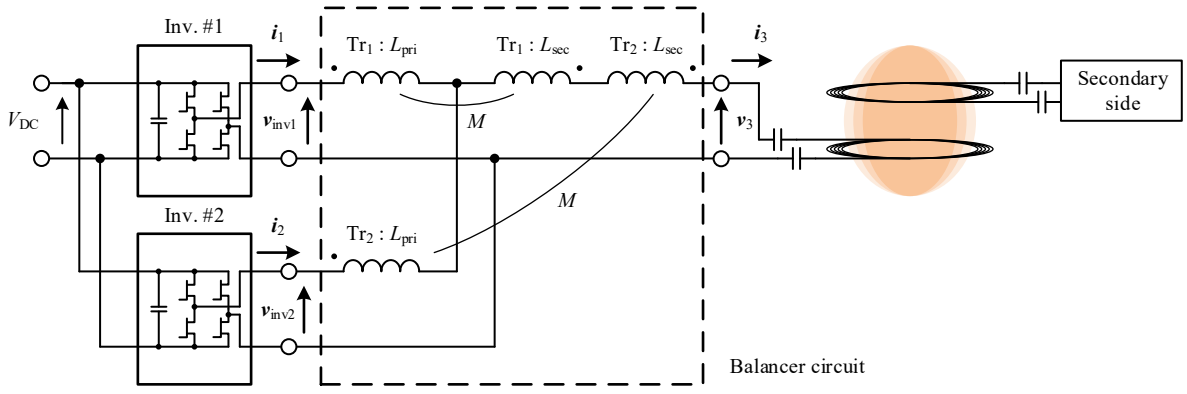


Fig. 1. Configuration of the conventional balancer circuit in parallel-connected inverter system.

Parameters of balancer circuit

Figure 3 shows the detail of the balancer circuit. In the balancer circuit, the transformer currents i_1, i_2, and i_3 are sinusoidal because the transmission coil and the capacitor in the WPT system consider the resonant load. Each voltage v_1, v_2, and v_3 are expressed as

$$\boldsymbol{v}_1 = N_1 \frac{d\boldsymbol{\Phi}}{dt},$$
$$= N_1 \frac{d}{dt}(\boldsymbol{\Phi}_1 - k\boldsymbol{\Phi}_2), \quad (1)$$
$$\boldsymbol{v}_2 = N_1 \frac{d}{dt}(\boldsymbol{\Phi}_3 - k\boldsymbol{\Phi}_4), \quad (2)$$
$$\boldsymbol{v}_3 = N_2 \frac{d}{dt}(\boldsymbol{\Phi}_2 - k\boldsymbol{\Phi}_1) + N_2 \frac{d}{dt}(\boldsymbol{\Phi}_4 - k\boldsymbol{\Phi}_3), \quad (3)$$
$$\boldsymbol{v}_3 = \frac{1}{2}(\boldsymbol{v}_1 + \boldsymbol{v}_2), \quad (4)$$
$$\boldsymbol{i}_1 = \boldsymbol{i}_2 = \frac{\boldsymbol{i}_3}{2}, \quad (5)$$

where $\boldsymbol{\Phi}_1$ is the magnet flux produced by the primary side of the Tr_1, $\boldsymbol{\Phi}_2$ is the magnet flux produced by the secondary side of the Tr_1, $\boldsymbol{\Phi}_3$ is the magnet flux produced by the primary side of the Tr_2, $\boldsymbol{\Phi}_4$ is the magnet flux produced by the secondary side of the Tr_2, N_1 is the number of turns in the primary side, and N_2 is the number of turns in the secondary side. Each magnetic flux under the current condition (5) is considered as

$$\boldsymbol{\Phi}_1 = \boldsymbol{\Phi}_3, \quad (6)$$
$$\boldsymbol{\Phi}_2 = \boldsymbol{\Phi}_4, \quad (7)$$

thus, the voltage equation is expressed by (1), (2), (3), (4), (6), and (7) as

$$2N_2 \frac{d}{dt}\{2\boldsymbol{\Phi}_2 - 2k\boldsymbol{\Phi}_1\} = 2N_1 \frac{d}{dt}(\boldsymbol{\Phi}_1 - k\boldsymbol{\Phi}_2), \quad (8)$$

then, the magnetic flux $\boldsymbol{\Phi}_1$ and $\boldsymbol{\Phi}_2$ are considered as the same value when the coupling factor k is unity.

$$k = 1, \quad (9)$$
$$\boldsymbol{\Phi}_1 = \boldsymbol{\Phi}_2, \quad (10)$$

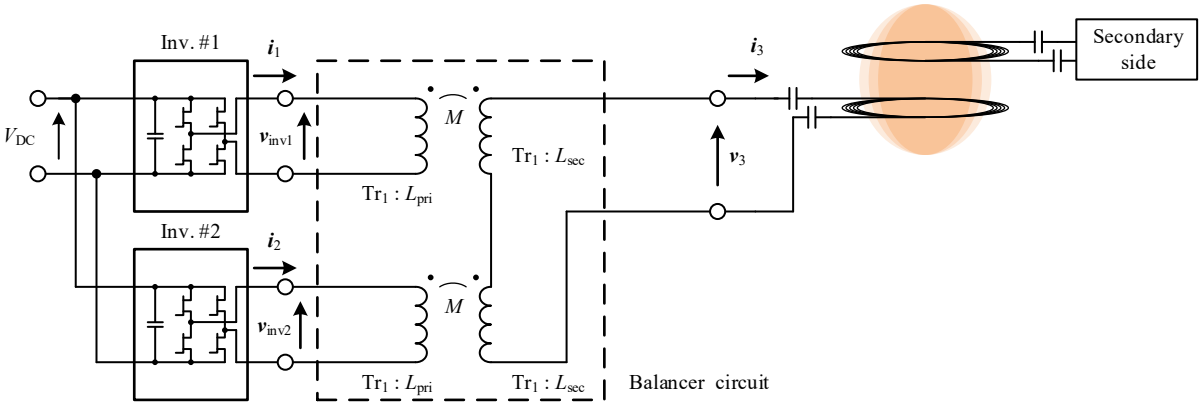


Fig. 2. Configuration of the proposed balancer circuit in parallel-connected inverter system.

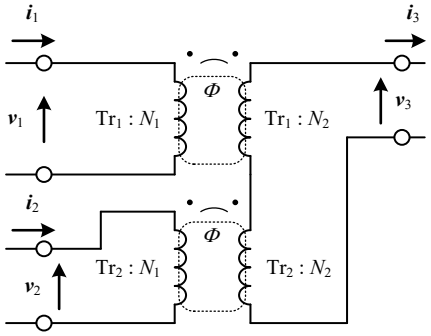


Fig. 3. Configuration of proposed balancer circuit.

The turn ratio of the transformer to achieve the current balance is expressed by using (8), (9), and (10) as

$$\frac{N_1}{N_2} = 2\,, \tag{11}$$

the turn ratio for the current balance (11) is the same as for the non-isolated balancer[13].

Impedance matching using leakage inductance

Two transformers in the proposed balancer also have the leakage inductance between the inverters and the transfer coil. The leakage inductance of the proposed balancer is the same as that of the non-isolated balancer[13] because the turn ratio is also the same. The leakage inductance of the balancer L_{leakage}, which is composed of two transformers, is derived in [13] as

$$L_{\text{leakage}} = 4L_{\text{sec}}(1-k)\,, \tag{12}$$

where L_{sec} is the self-inductance of the secondary side of each transformer. Then, the leakage inductance appears in series on the secondary side of the balancer[13].

Although the balancer has the leakage inductance, the inductance has the capability of the impedance matching using the additional capacitor. Figure 4 (a) shows the connection of the additional capacitor, and (b) shows the equivalent circuit for the impedance matching capability in the proposed balancer. The leakage inductance of the balancer L_{leakage} and the additional capacitor C_{m} compose the impedance matching circuit. The load considers the resistor R_{L} because the power factor of the WPT system is unity under operation in resonant frequency.

The additional capacitor C_{m} is determined to match the impedance of the load and the inverter. Thus, the modification of the resonant capacitance is not needed to achieve the resonant condition. Moreover, the ZVS operation of two inverters becomes easy because the impedance matching circuit adjusts the impedance to the ZVS condition at the input terminal of the matching circuit. Then, the input impedance $\boldsymbol{Z}_{\text{in}}$ is expressed as

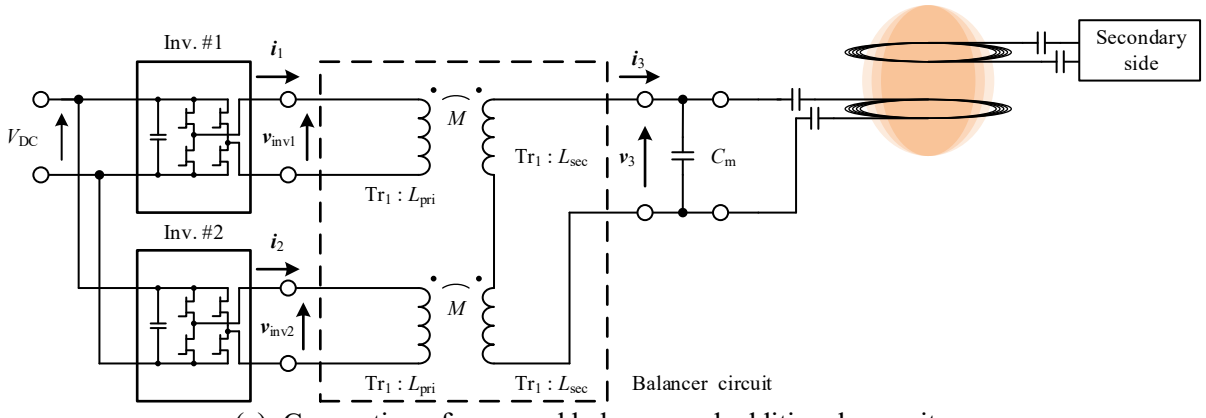
$$\boldsymbol{Z}_{\text{in}} = jX_{\text{L}} - \frac{jR_{\text{L}}X_{\text{C}}}{R_{\text{L}} - jX_{\text{C}}}\,. \tag{13}$$

Then, the input impedance $\boldsymbol{Z}_{\text{in}}$ must be satisfied the following condition to achieve the impedance matching.

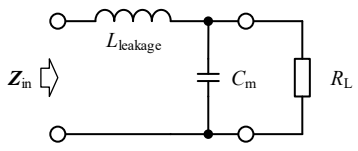
$$R_{\text{out}} = \text{Re}[\boldsymbol{Z}_{\text{in}}]\,, \tag{14}$$

$$X_{\text{out}} = \text{Im}[\boldsymbol{Z}_{\text{in}}]\,, \tag{15}$$

where R_{out} is the resistance of the output impedance, X_{out} is the reactance of the output impedance at the inverter circuit. The capacitance C_{m} and the inductance L_{leakage} under the impedance matching is expressed as



(a) Connection of proposed balancer and additional capacitor.



(b) Equivalent circuit

Fig. 4. Impedance matching capability in proposed configuration.

$$C_{\mathrm{m}} = \frac{1}{\omega R_{\mathrm{L}}}\sqrt{\frac{R_{\mathrm{L}}}{R_{\mathrm{out}}} - 1}\,, \qquad (16)$$

$$L_{\mathrm{leakage}} = \frac{X_{\mathrm{out}}}{\omega} + \frac{C_{\mathrm{m}} R_{\mathrm{L}}^{\,2}}{1 + \omega^2 C_{\mathrm{m}}^{\,2} R_{\mathrm{L}}^{\,2}}\,. \qquad (17)$$

Thus, the self-inductance of the transformer by using (12) and (17) is determined as

$$L_{\mathrm{sec}} = \frac{1}{4(1-k)}\left\{\frac{X_{\mathrm{out}}}{\omega} + \frac{C_{\mathrm{m}} R_{\mathrm{L}}^{\,2}}{1 + \omega^2 C_{\mathrm{m}}^{\,2} R_{\mathrm{L}}^{\,2}}\right\}. \qquad (18)$$

Simulation results

Table I shows the simulation parameters. The transfer coil and the secondary side of the WPT system consider the resonant load. The capacitor of the GaN-FET between drain and source is considered as C_{ds} in the simulation to accurately simulate the output voltage of the inverter. Then, the load resistance R_{L} is selected to 50 Ω to check the impedance matching, although the required impedance is around 15 Ω to achieve the ZVS operation. The simulation was implemented by PLECS*(Plexim Inc.)*.

Table I. Simulation parameters.

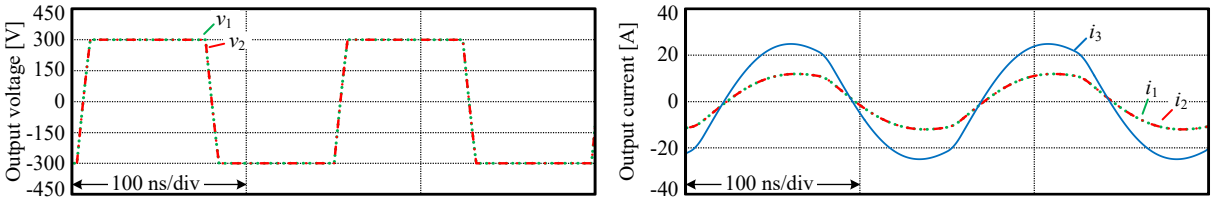
Main circuit		
DC link voltage	V_{DC}	300 V
Switching frequency	F_{s}	6.78 MHz
Duty	d	40%
Parasitic capasitance at drain-source of GaN-FET	C_{ds}	127 pF
Balancer		
Output resistance of inverter	R_{out}	10.0 Ω
Output reactance of inverter	X_{out}	10.0 Ω
Impedance matching capacitor	C_{m}	939 pF
Leakage inductance of balancer	L_{leakage}	0.70 μH
Coupling factor	k	0.9
Inductance of secondary side	L_{sec}	1.76 μH
Inductance of primary side	L_{pri}	7.0 μH
Load		
Resonant inductance	L_{r}	5.8 μH
Resonant capacitance	C_{r}	95.0 pF
Load resistance	R_{L}	50.0 Ω

Current balance working

Figure 5 shows the each inverter's output voltage and current without the amplitude difference and the phase difference of the output voltage. Each output voltage is the same amplitude and phase. The coupling factor k is 0.9. The output current of each inverter is balanced.

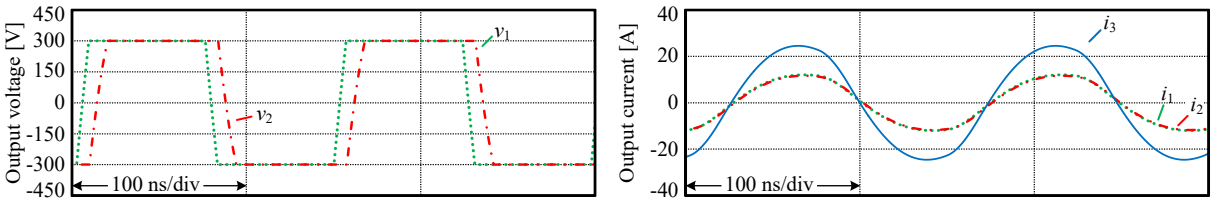
Figure 6 shows the output voltage and the current of each inverter with the phase difference of the output voltage. The phase of the inverter #2 is set to a 5.0% delay. Each current becomes the same amplitude with the phase difference of the output voltage. The output voltage of the each inverter achieves ZVS operation.

Figure 7 shows the output voltage and current of each inverter when each output voltage has a different phase and amplitude. The voltage amplitude of the inverter #2 is decreased to half the value of the inverter #1. The phase of the inverter #2 is set to a 10.0% delay. Each current is also made balanced, and the ZVS operation is almost achieved.



(a) Output voltage. (b) Output current.

Fig. 5. Output voltage and current without voltage difference and phase difference.



(a) Output voltage. (b) Output current.

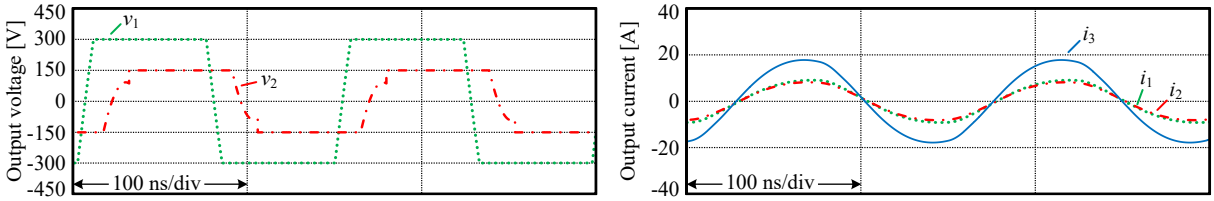
Fig. 6. Output voltage and current with phase difference.

Impedance matching

Figure 8 shows the output voltage and the current of each inverter with different load resistance. The load resistance R_L is selected to 30 Ω and 100 Ω to check the effect of the impedance matching. Then, the capacitor C_m and the leakage inductance $L_{leakage}$ is modified to match the impedance. Table II shows the matching parameters with the R_L changing. The phase of the inverter #2 is set to a 5.0% delay. Each current i_1 and i_2, and the total output current i_3 have no difference with load difference between 30 Ω and 100 Ω. Moreover, both inverters also achieve ZVS operation with load difference. This result indicates that the input impedance of the balancer kept constant by the additional capacitor C_m and the leakage inductance $L_{leakage}$.

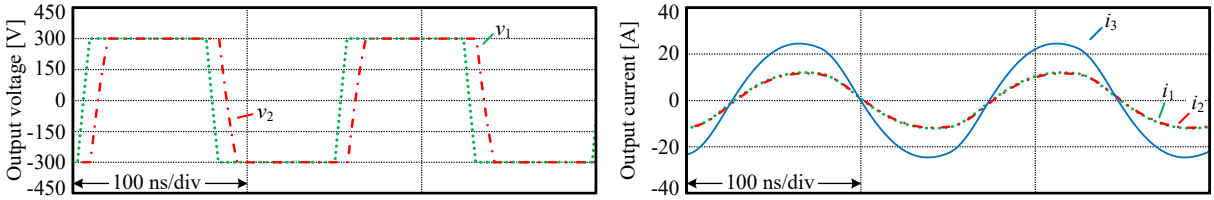
Experimental results

Figure 9 shows the prototype balancer and the parallel connection inverters in the experiment. The prototype balancer consists of two air-core transformers. The output of the balancer connects with the resonant load as the transfer coil and the secondary side of the WPT system. Table III shows the each parameter of the experimental verification. The GaN-transistors (PGA26E07BA: 600 V, 26 A, Panasonic) are used for the mega-hertz switching in each inverter.

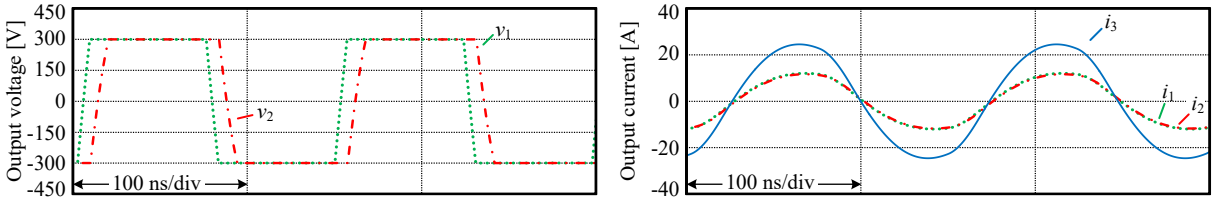


(a) Output voltage. (b) Output current.

Fig. 7. Output voltage and current with voltage amplitude and phase difference.



(a) Output voltage (R_L:30 Ω). (b) Output current (R_L:30 Ω).

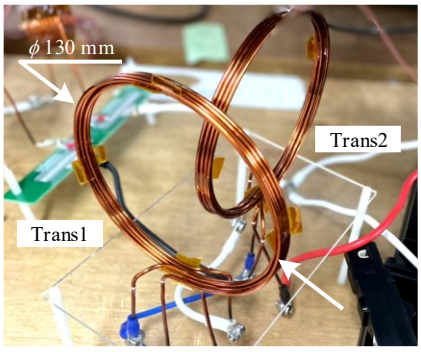


(c) Output voltage (R_L:100 Ω). (d) Output current (R_L:100 Ω).

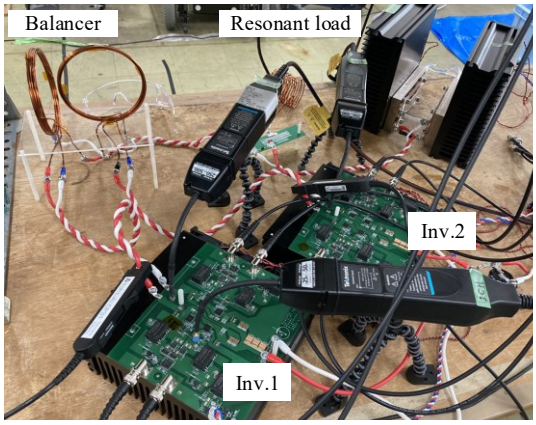
Fig. 8 Output voltage and current with difference of load resistance.

Table II. Balancer parameter with load difference.

Load resistance R_L = 30.0 Ω		
Impedance matching capacitor	C_m	1107 pF
Leakage inductance of balancer	$L_{leakage}$	0.57 μH
Inductance of secondary side	L_{sec}	1.42 μH
Load resistance R_L = 100 Ω		
Impedance matching capacitor	C_m	704 pF
Leakage inductance of balancer	$L_{leakage}$	0.94 μH
Inductance of secondary side	L_{sec}	2.35 μH



(a) Prototype balancer



(b) Overview of experimental circuit.

Fig.9 Experimental circuit.

Table III. Balancer parameters.

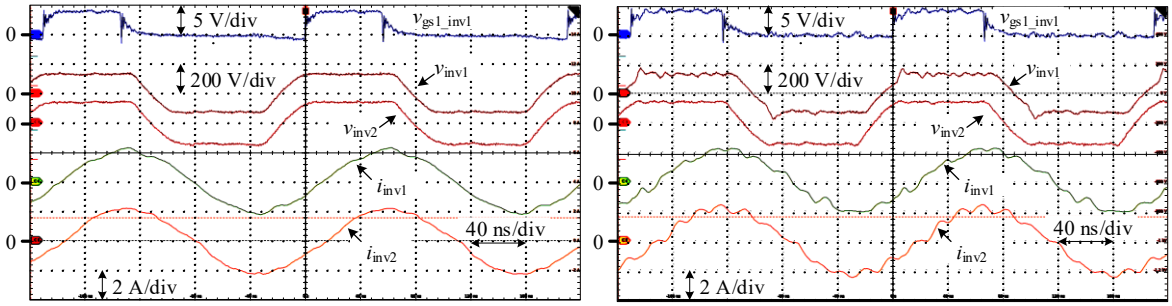
Main circuit		
DC link voltage	V_{DC}	200 V
Switching frequency	F_s	6.78 MHz
Duty	d	20%
Balancer		
Output resistance of inverter	R_{out}	10.0 Ω
Output reactance of inverter	X_{out}	10.0 Ω
Impedance matching capacitor	C_m	940 pF
Inductance of primary side	L_{pri}	4.7 μH
Inductance of secondary side	L_{sec}	1.3 μH
Coupling factor	k	0.84
Load		
Resonant inductance	L_r	5.3 μH
Resonant capacitance	C_r	105 pF
Load resistance	R_L	50.0 Ω

Current balance working

Figure 10 shows the output voltage and the current of the paralleled inverters in the experiment using the prototype balancer. Note that the impedance matching capacitor C_m is not implemented to confirm the fundamental balance operation. Thus, the load resistance is 20.0 Ω to achieve the ZVS. The operation frequency is 5.25 MHz because the resonant frequency of the resonant load is decreased by the leakage inductance in the balancer. The DC-link voltage is 150V. The output current i_{inv1} and i_{inv2} is balanced even if the phase of the voltage has a difference of approximately 5 ns in figure 10(b). The difference between the maximum value of the current is 5.6%. Therefore, the balancer working is achieved fundamentally without any additional control in megahertz operation.

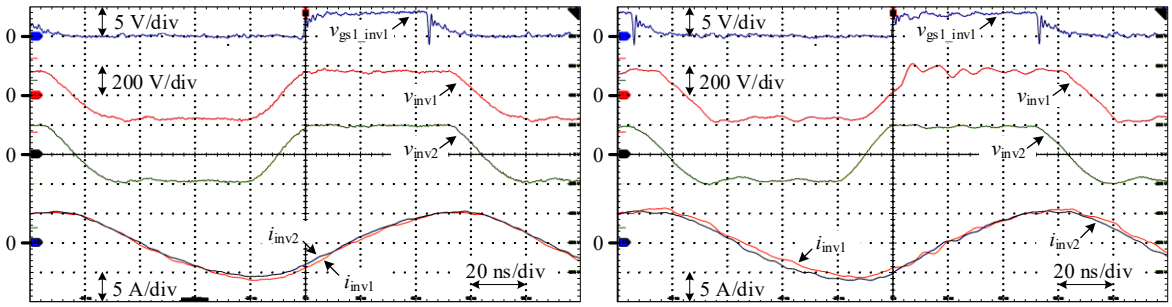
Impedance matching

Figure 11 shows the output voltage and the current of the paralleled inverters with impedance matching capacitor C_m. The load resistance is 50.0 Ω to verify the impedance matching. The operation frequency is 6.78 MHz. The phase difference between the output voltage v_{inv1} and v_{inv2} is approximately 8 ns in figure 11(b). The output current i_{inv1} and i_{inv2} is balanced even if the output voltage has the phase difference. The output voltage v_{inv2} achieves the ZVS operation completely. The v_{inv1} does not achieve ZVS operation because of the phase of the v_{inv1} is delayed from the v_{inv2}. The total output is 620 W at the load resistor RL in figure 11(a).



(a) Without phase difference (b) With phase difference (5 ns)

Fig. 10. Output voltage and current in experiment without impedance matching (5.25 MHz).



(a) Without phase difference (b) With phase difference (8 ns)

Fig. 11. Output voltage and current in experiment with impedance matching (6.78 MHz).

Conclusion

In this paper, the new current balancer, including impedance matching capability for megahertz operation, was proposed. The proposed balancer consists of two transformers without any additional control to achieve the current balance. The turn ratio of two transformers to achieve the current balancing was derived theoretically based on the magnet flux under the current balancing condition. The impedance matching condition is also derived by the leakage inductance of the balancer and the additional capacitor. The simulation results verified the operation of the proposed balancer under the amplitude and the phase difference condition. The input impedance of the balancer kept constant with the impedance matching capability. The experimental result with proposed balancer achieved current balance with a phase difference of the output voltage approximately 8 ns. In addition, the ZVS operation is almost achieved in the each inverter by impedance conversion using additional capacitor.

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