

DC-Bus Control Considerations of Asymmetrical Multilevel Inverters with Embedded Buck-Boost Converter

Theodoros P. Mouselinos and Emmanuel C. Tatakis

UNIVERSITY OF PATRAS

Laboratory of Electromechanical Energy Conversion

Department of Electrical and Computer Engineering

26504, Rion-Patras, Greece

Tel.: +30 2610 996412.

E-Mail: t.mouselinos@ece.upatras.gr, e.c.tatakis@ece.upatras.gr

URL: <http://www.lemec.ece.upatras.gr>

Keywords

«DC-AC Converters», «DC-DC converter», «Multi-level Inverters», «Converter control», «DC voltage control»

Abstract

This paper focuses on the DC-bus control of asymmetrical Multilevel inverter family featuring a Buck-Boost converter to boost the input voltage. To investigate the dynamic performance of the system a thorough analysis is presented on the DC-bus dynamic behavior. It is shown that with higher system bandwidth the input capacitance requirements and the peak current through the boosting inductor are increased, compromising the power density and the efficiency of the whole DC/AC converter. To improve the transient performance of the system without increasing the volume of the passive components, a control scheme with a feedforward current estimator term is proposed. Finally, the correctness of the theoretical analysis is validated via experimental probing on a laboratory prototype.

Introduction

Multilevel inverters (MLIs) show many advantages compared to two-level inverter topologies such as the high-quality multi stepped output voltage waveform, the fault tolerant operation, the reduced blocking voltage of the semiconductor devices and the reduced common mode voltage. The state-of-the-art MLI topologies, named Cascaded H-Bridge MLI (CHB-MLI), Diode Clamped MLI (DC MLI) and Flying Capacitor MLI (FC MLI) are used in many renewable energy sources applications and industrial applications [1].

Even though the mentioned above topologies have been adopted in many applications, their main disadvantage is the increased number of semiconductors needed and the reduction of the switch count is a subject of research in recent years [2]. Also, as it can be seen from [3] the voltage boosting feature is often a must in renewable energy systems. Since, the reduction of the switching devices and the voltage boosting feature are required in many applications, a new research field is introduced and multilevel inverter topologies with embedded Buck-Boost DC-DC converters have been proposed in the literature [4]-[8].

In this paper the DC-bus voltage control of asymmetrical MLI family (AMLI) with embedded Buck-Boost converter is analyzed and a thorough analysis is presented on the dynamic performance of the system. DCM operation is selected over int-DCM and CCM as the magnetic component volume and the RMS value of the current of Buck-Boost main switch are decreased. Moreover, the influence of the controller bandwidth in double line frequency component of the input current is investigated and a full schematic control with a feedforward current estimator term is presented to improve the transient performance without adding extra current measurement circuitry.

Calculation of the Embedded Buck-Boost Converter Load Current

The topology of the five-level Buck-Boost Multilevel Inverter under investigation is depicted in Fig. 1. As presented in [8] the MLI topology is based on the simplified neutral point clamped topology with an active switch added (ANPC topology), since a proper commutation path must be provided to the load current in the case of resistive-inductive load.

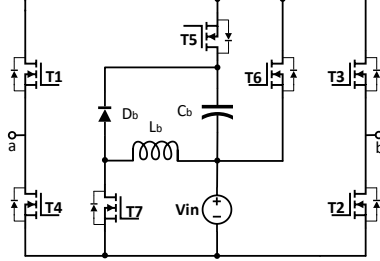


Fig. 1: The ANPC Buck-Boost embedded AMLI topology under investigation.

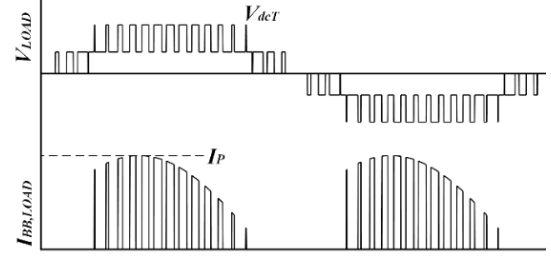


Fig. 2: Output voltage of the five-level MLI and load current waveform of the embedded Buck-Boost converter.

Since the average value of the output current of the Buck-Boost converter must be known for a proper small signal analysis, in this section its value is calculated. Considering the Buck-Boost output current waveform from Fig. 2 and a modulation technique similar to the one presented in [9] its mean value can be written as:

$$I_{BB,Load,AVG} = \frac{1}{T_h} \int_{\arcsin(a)}^{\pi - \arcsin(a)} i_{BB,Load}(t) dt \quad (1)$$

where T_h is the half period of the output voltage waveform and $a = I/[m_a \cdot (1+G)]$, where $G = V_{Cb}/V_{in}$ and m_a is the inverter modulation index. For the analytical calculation of the current value $I_{BB,Load,AVG}$ the following must be considered:

- m is the number of the switching cycles during the T_h time interval and it is equal to $m = \text{round}(T_h/T_s)$ T_s is the carrier switching frequency responsible for the modulation of the upper level
- the random angle ωt_i can be written as $\omega t_i = \pi \cdot i/m$ and
- the inverter output current follows a pure sine wave

Considering the above the mean value of the load current of the Buck-Boost converter is given from eq. (2).

$$I_{BB,Load,AVG} = I_p \cdot \cos \varphi \cdot \left[m_a \cdot \frac{(1+G')}{2} - m_a \cdot \frac{(1+G')}{\pi} \cdot \arcsin(a) - \frac{G'}{\pi} \cdot \sqrt{1-a^2} \right], \quad (2)$$

where I_p is the peak amplitude of the output current waveform, φ is the load angle and G' is equal to $G' = I/G$.

In this point it must be noted that eq. (2) is valid for all the five-level Buck-Boost based AMLI topologies in which the generation of the lower voltage level is achieved only with the input voltage source and the generation of the upper level is achieved with the series connection of the input voltage source and the boosting capacitor C_b . As it can be also deduced from eq. (2) and [8] the load current of the Buck-Boost converter is relatively small, and hence the power processed by the embedded DC/DC converter is only a fraction of the total inverter output power.

In Buck-Boost based AMLI topologies the inductor is used to transfer energy from the input DC voltage source to the boosting capacitor. Due to the low power processed by the integrated Buck-Boost converter, the selection of an inductance for CCM operation will lead to a bulky and costly inductor. Also, for the selection of the operational mode of the embedded DC/DC converter two other indexes are also considered. The first index is the amplitude of the double line component of the input current,

because its value determines the input capacitance value. The other index is the RMS value of the current through the $T7$ switch which determines the conduction power losses of the transistor. In Fig. 3 and Fig. 4 comparative results are presented considering the critical inductance value for each mode of operation and DCM operation is chosen since it offers a good tradeoff between volume and power losses. The critical inductance for CCM is equal to 3.6 mH, for int-DCM it is equal to 120 μ H, while for DCM operation the critical inductance is equal to 200 μ H.

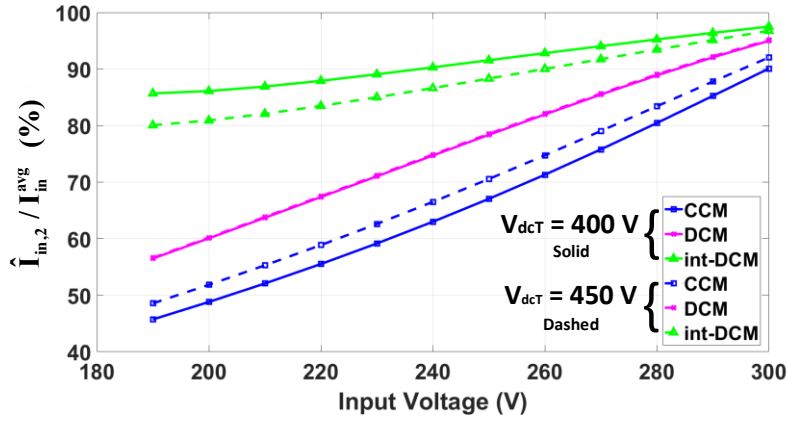


Fig. 3: Amplitude of the double line component of the input current over the average input current of the converter.

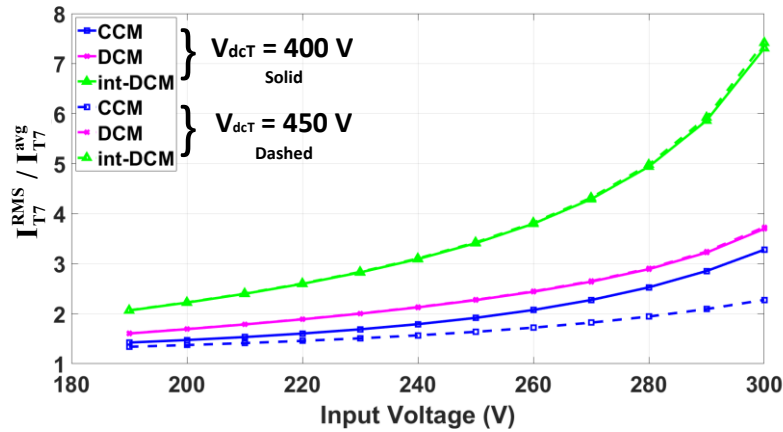


Fig. 4: RMS value over the average value of the current through transistor $T7$.

Small Signal Analysis and DC-bus Control Considerations

Since DCM operation is selected for the embedded Buck-Boost converter the DC-bus voltage should be controlled, since the output voltage of the DC/DC converter V_{Cb} is heavily depended on the output load. To begin with, the output load of the embedded Buck-Boost converter should be identified. This can be achieved considering an equivalent load resistance which it is given from (3) taking into account eq. (2).

$$R_{eq} = \frac{V_{Cb}}{I_p \cdot \cos \varphi \cdot \left[m_a \cdot \frac{(1+G')}{2} - m_a \cdot \frac{(1+G')}{\pi} \cdot \arcsin(a) - \frac{G'}{\pi} \cdot \sqrt{1-a^2} \right]} \quad (3)$$

With the equivalent output resistance of the embedded converter been known the next step is the small signal modeling of the DC/DC converter to quantify its dynamic behavior. As it can be seen from the literature, reduced order models and full order models are presented [10]-[11]. In this paper full order average models with the correction proposed in [11] are used, since they offer increased accuracy in both magnitude and phase response in the high-frequency range.

When the switch $T7$ is ON (d_1T_s interval), energy is transferred from the input DC source to the inductor L_b while the output capacitor C_b supplies the load and hence (4) can be exported. When $T7$ is off, diode D_b conducts (d_2T_s interval) until the inductor current becomes zero. In d_2T_s interval the inductor transfers its stored energy to the capacitor C_b and the load R_{eq} and thus (5) is exported. The final time interval d_3T_s neither the diode D_b nor the $T7$ switch conducts, thus the inductor current is zero, the capacitor transfers energy to the load and hence (6) is exported. Deploying the averaging techniques, the modified average model can be extracted (7).

$$\frac{d}{dt} \begin{bmatrix} i_L \\ u_C \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & -1/R_{eq}C_b \end{bmatrix} \cdot \begin{bmatrix} i_L \\ u_C \end{bmatrix} + \begin{bmatrix} 1/L_b \\ 0 \end{bmatrix} \cdot u_{in} \text{ ,for } d_1T_s \quad (4) \quad \frac{d}{dt} \begin{bmatrix} i_L \\ u_C \end{bmatrix} = \begin{bmatrix} 0 & -1/L_b \\ 1/C_b & -1/R_{eq}C_b \end{bmatrix} \cdot \begin{bmatrix} i_L \\ u_C \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} \cdot u_{in} \text{ ,for } d_2T_s \quad (5)$$

$$\frac{d}{dt} \begin{bmatrix} i_L \\ u_C \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & -1/R_{eq}C_b \end{bmatrix} \cdot \begin{bmatrix} i_L \\ u_C \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} \cdot u_{in} \text{ ,for } d_3T_s \quad (6) \quad \frac{d}{dt} \begin{bmatrix} i_L \\ u_C \end{bmatrix} = \begin{bmatrix} 0 & \frac{-d_2}{L_b} \\ \frac{d_2}{(d_1+d_2) \cdot C_b} & \frac{-1}{R_{eq}C_b} \end{bmatrix} \cdot \begin{bmatrix} i_L \\ u_C \end{bmatrix} + \begin{bmatrix} \frac{d_1}{L_b} \\ 0 \end{bmatrix} \cdot u_{in} \quad (7)$$

After some mathematical manipulations the small signal model of the embedded Buck-Boost converter operating in DCM can be exported (8).

$$\frac{d}{dt} \begin{bmatrix} \tilde{i}_L \\ \tilde{u}_C \end{bmatrix} = \begin{bmatrix} -\frac{2 \cdot G}{D_1 \cdot T_s} & -\frac{D_1}{L_b \cdot G} \\ \frac{1}{C_b} & -1/R_{eq}C_b \end{bmatrix} \cdot \begin{bmatrix} \tilde{i}_L \\ \tilde{u}_C \end{bmatrix} + \begin{bmatrix} \frac{D_1 \cdot (2+G)}{L_b} & \frac{2 \cdot V_{in} \cdot (1+G)}{L_b} \\ -\frac{D_1^2 \cdot T_s}{2 \cdot L_b \cdot C_b} & \frac{D_1 \cdot T_s \cdot V_{in}}{L_b \cdot C_b} \end{bmatrix} \cdot \begin{bmatrix} \tilde{u}_{in} \\ \tilde{d}_1 \end{bmatrix} \quad (8)$$

With the small signal model of the converter been known, a PI controller can be properly tuned to regulate the voltage of the boosting capacitor C_b and hence the total DC-bus voltage V_{dcT} of the multilevel inverter. The main requirement of the control system is to be stable with a fast transient response. The stability and settling time of the overall system depends on the PI controller gains, from which the system bandwidth is determined. In Fig. 5 and Fig. 6 the key waveforms of the converter are depicted for the same step change of the load but with different gains for the PI controller. In Fig. 5 the PI controller gains are $k_p=0.1418$ and $k_i=1.3747$ leading to an 89.8° phase margin (PM) at 1010.25 rad/s and 52 dB gain margin (GM) at $410.389 \cdot 10^3$ rad/s. In Fig. 6 the PI controller gains are $k_p=0.002198$ and $k_i=0.02423$ with $PM=90^\circ$ (at 15.66 rad/s) and $GM=88$ dB (at $410.388 \cdot 10^3$ rad/s). As it can be deduced with a higher bandwidth the system features a faster transient response as it is known from the classic control theory, but in this case a double line frequency component is present in the inductor current waveform (Fig. 5). A part of this double line frequency component is drawn from the input DC source through the switch $T7$, leading to increased input capacitance requirement. In Fig. 6 the controller features narrower bandwidth compared to the controller used for the extraction of the results of Fig. 5. As can be seen, in this case a slower transient response is achieved but the double line frequency component of the inductor current is much reduced. In both cases a saturator is added to the controller output to avoid CCM operation.

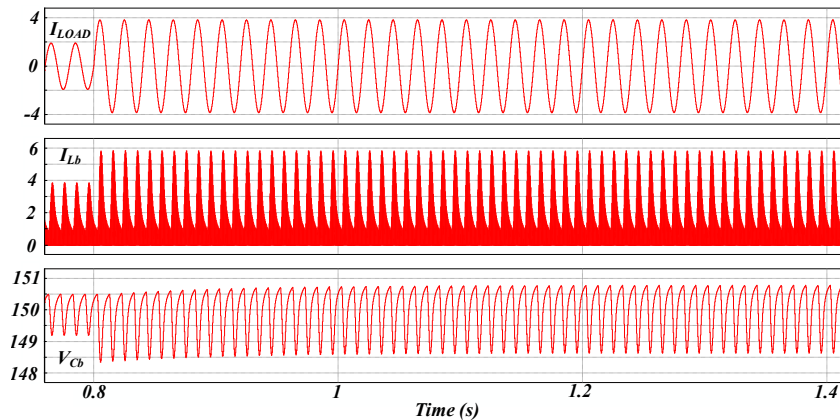


Fig. 5: Transient response of the C_b voltage for a step change of the load with $k_p=0.1418$ and $k_i=1.3747$.

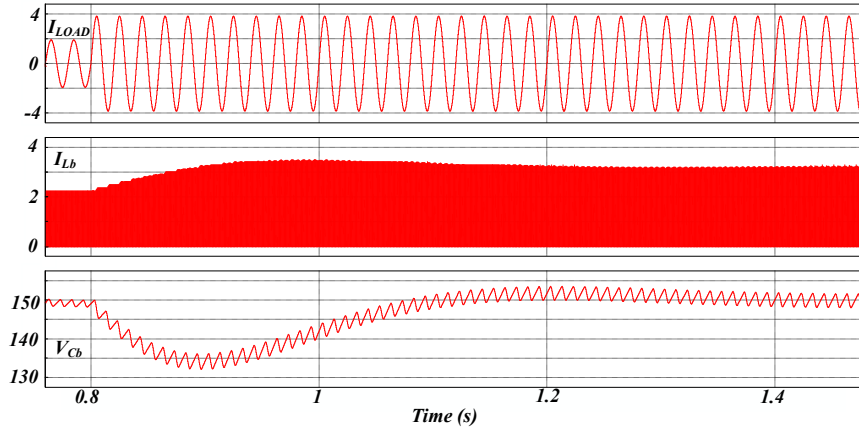


Fig. 6: Transient response of the C_b voltage for a step change of the load with $k_p=0.002198$ and $k_i=0.02423$.

To further investigate the effect of the controller bandwidth to the double line frequency component of the input current waveform multiple controllers are designed and simulated considering a 0.7 kW inverter load. Then, the double line frequency component is extracted along with the peak current flowing through the inductor L_b and the simulation results are depicted in Fig. 7 and Fig. 8. In Fig. 7 the minimum input capacitance requirement is also depicted given a 2% voltage ripple with the average value of the input voltage been equal to 250 V.

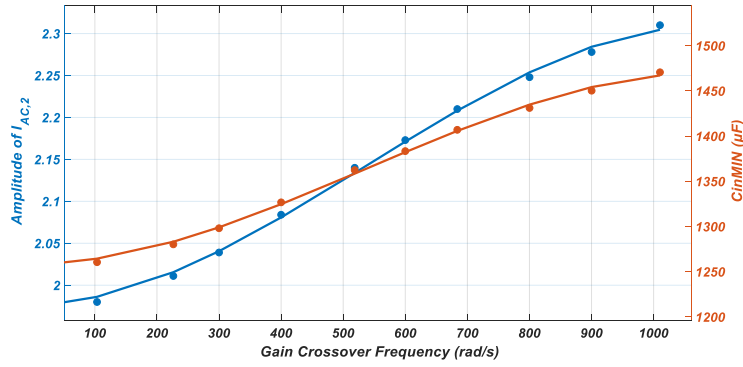


Fig. 7: The effect of the system bandwidth to the double line frequency component of the input current waveform.

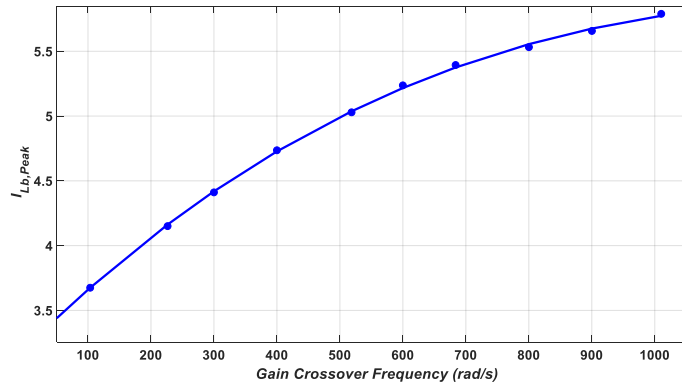


Fig. 8: The effect of the system bandwidth to the peak current flowing through L_b .

From Fig. 7 and Fig. 8 it is visible that the controller bandwidth plays a crucial role to the peak current through the boosting inductor and the double line frequency component of the input current. More specifically the double line frequency component of the input current waveform is increased by 17% and thus the minimum input capacitance requirements are also increased accordingly. Furthermore, if a designed converter for PV applications is considered with a specific capacitance installed on the input DC side, the increase double line frequency on the input current will cause an increased input voltage

ripple, leading to decreased energy harvesting from the PV panels [13]. Moreover, with higher system bandwidth the peak current through the inductor is dramatically increased. Considering the case in which the system bandwidth is 1000 rad/s, the peak current through L_b is almost double compared to the case in which the bandwidth is 100 times smaller, which may lead to the saturation of the inductor if it is marginally designed according to the theoretical calculations. In conclusion, it can be deduced that the system bandwidth can affect the power density of the converter since with higher system bandwidth the input capacitance requirements are increased. Also, the Area Product requirement for the inductor L_b is increased leading to bulkier and more expensive inductor if the above results are taken into consideration in the inductor design procedure.

Closed Loop Control with Feedforward Current Estimator Term

As it is shown the fast transient response in the DC bus voltage control cannot be achieved without adding extra double line frequency component in the inductor current waveform. The design of higher order controllers in this case is a much more complicated procedure since the Buck-Boost converter features a right half plane zero and the output current waveform contains low order harmonics in this application. In this section a control scheme is proposed to meet the fast response requirement without the extra low order harmonic component in the inductor current waveform. This is achieved by estimating the output current of the embedded DC/DC converter to avoid the extra current measurement circuit. Then, the theoretical duty cycle of the embedded DC/DC converter can be estimated, and this value can be used as a feedforward term in the closed loop control system.

From eq. (2) it can be seen that the output current of the Buck-Boost converter depends on the amplitude and the phase of inverter output current. Moreover, the input voltage and the modulation index are also two parameters that must be known to properly estimate the output current of the embedded converter. Thereafter, it is determined that the inverter output current and the input voltage must be measured, which there are measured in almost all the cases for control and protection purposes. Hence, no extra measurement is deployed. The estimation of the inverter output current angle can be achieved using the SOGI PLL [12]. Deploying an orthogonal signal generator, the fictitious component β of the inverter output current can be obtained. Subsequently, the *Park* transformation of the inverter output current can be used to extract the quantity I_d which it is described by (9). Given all the above, the output current of the Buck-Boost converter can be estimated by (2) and the theoretical duty cycle of the embedded Buck-Boost DC/DC converter is given by eq. (10).

$$I_d = I_p \cdot \cos \varphi \quad (9)$$

$$d = \sqrt{\frac{2 \cdot I_{BB,Load,AVG} \cdot V_{Cb,AVG} \cdot L_b \cdot f_s}{V_{in,AVG}^2}} \quad (10)$$

Consequently, the proposed control scheme is presented in Fig. 9. In this point it must be noted that the feedforward term cannot affect the stability of the feedback system as reported in [14], but in order to be applied correctly an accurate dynamic model of the converter must be available, pinpointing the importance of the analysis shown in the previous section.

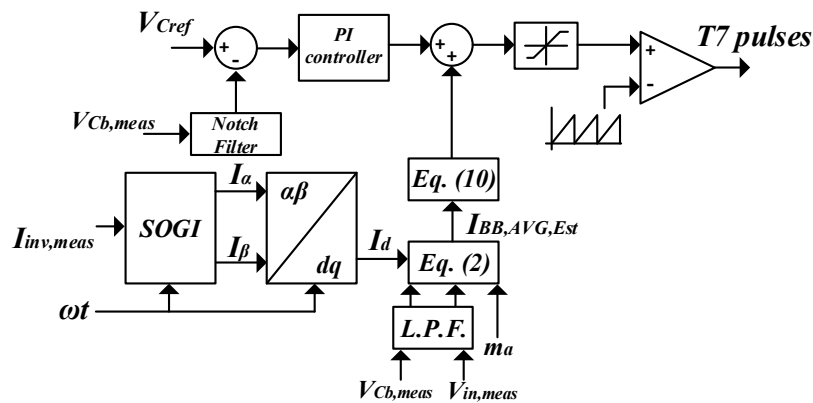


Fig. 9: Block diagram of the closed loop control with the feedforward current estimator term.

In Fig. 10 the performance is shown for the same step change of the load as shown in Fig. 5 and Fig. 6. The PI controller gains in this case are $k_p=0.002198$ and $k_i=0.024423$ leading to a narrower bandwidth and also a 100Hz notch filter is used on the feedback to completely remove the double line frequency component of inductor L_b . Notch filter can be deployed in this case, because the lower crossover frequency can be maintained since the notch filter attenuating frequency is much higher compared to the controller bandwidth.

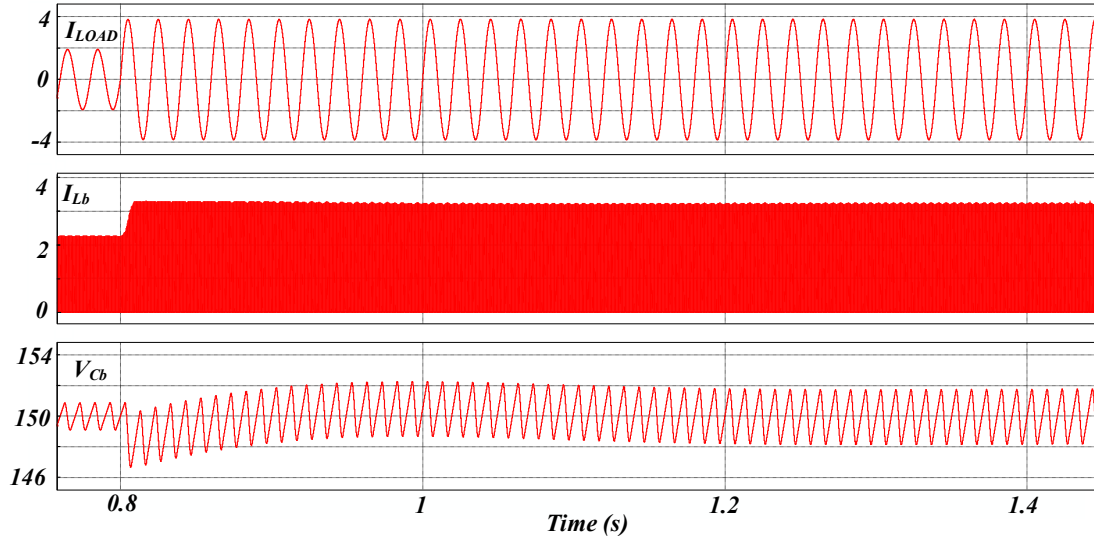


Fig. 10: Transient response of the C_b voltage for a step change of the load with the proposed closed loop control deploying the feedforward current estimator.

Experimental Results

The performance of the proposed control scheme is tested via a 1 kVA experimental prototype of the converter topology shown in Fig. 1. The main components and parameters of the laboratory prototype are summarized in Table I. Also, an LC filter is designed for the AC side of the inverter considering a 30% current ripple in the inductor current waveform and the filter capacitance is selected to obtain a resonant frequency about 10 times lower compared to the switching frequency of the inverter [15]. For the control of the converter the TMS320F28379D is selected. The sampling frequency for the control loop is selected equal to 25 kHz. The input voltage V_{in} , the capacitor voltage V_{Cb} and the output current of the inverter are measured, and then digital low pass filters are deployed featuring a bandwidth of 2 kHz to ensure the measurement quality. Moreover a 100 Hz notch filter is used for the filtering of the capacitor voltage to completely remove the unwanted double line frequency component.

Table I: Converter Parameters and Components

Parameters/ Components	Value/ Parameter
Input Voltage V_{in}	250 V
Output Voltage V_{ab}	230V/50Hz
Output Power P_o	1 kVA
PD- SPWM carrier frequency	25 kHz
Switching frequency of T7 switch	80 kHz
Power Switches	C3M0065090D
Diode D_b	IDW15G120C5B
Boosting Capacitor C_b	10x EEU-EB2V101 (100uF each) (898 uF measured)
Inductor L_b	190 uH (RM14 core, N87)
Output LC filter parameters	Lf: 2x350uH (E42/21/20 core, N27) Cf: 12x0.47uF (5.46uF measured)

In Fig. 11 a step change is taking place on the inverter output current, while the DC-bus voltage is regulated deploying a PI controller with $k_p=0.002198$ and $k_i=0.024423$ and the feedforward term in this

case is disabled. As can be seen large overshoots and undershoots are visible in the capacitor voltage V_{Cb} and no double line frequency component exists in the inductor current waveform since the controller bandwidth is kept at lower levels.

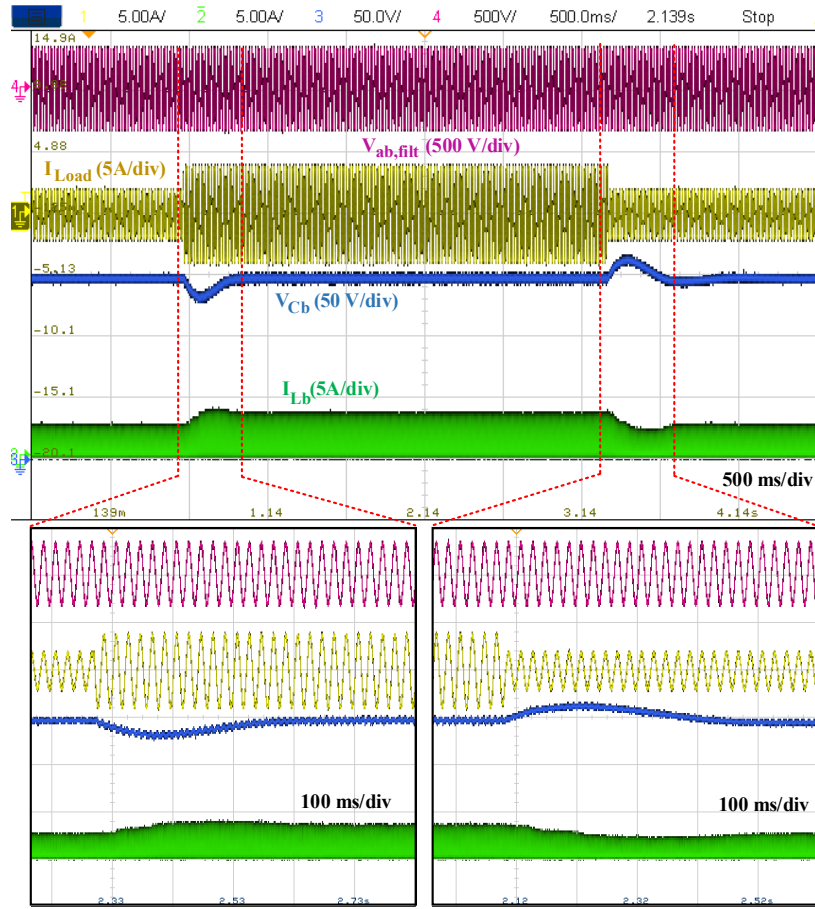


Fig. 11: Key waveforms of the converter for positive and negative changes of the load deploying a *PI* controller for the DC-bus voltage regulation.

In Fig. 12 the control scheme shown in Fig. 9 is deployed for the DC-bus voltage regulation with the feedforward term been activated. The gains of the *PI* controller in this case are the same as the ones used for the extraction of the results presented in Fig. 9 and the same step changes of the inverter load are taking place for comparison purposes. In both cases the input voltage is equal to 250 V, while the reference voltage for the boosting capacitor is equal to 150 V and the fundamental component of the output voltage waveform is kept equal to 230 V/ 50 Hz.

As it can be deduced from the experimental results, superior performance can be achieved using the proposed control scheme with the current estimator feedforward term as shown in Fig. 9, since almost no overshoot or undershoot is reported in the capacitor voltage waveform. Moreover, no double line frequency component is present in the inductor current waveform in this case also denoting the correctness of the analysis and the effectiveness of presented control method.

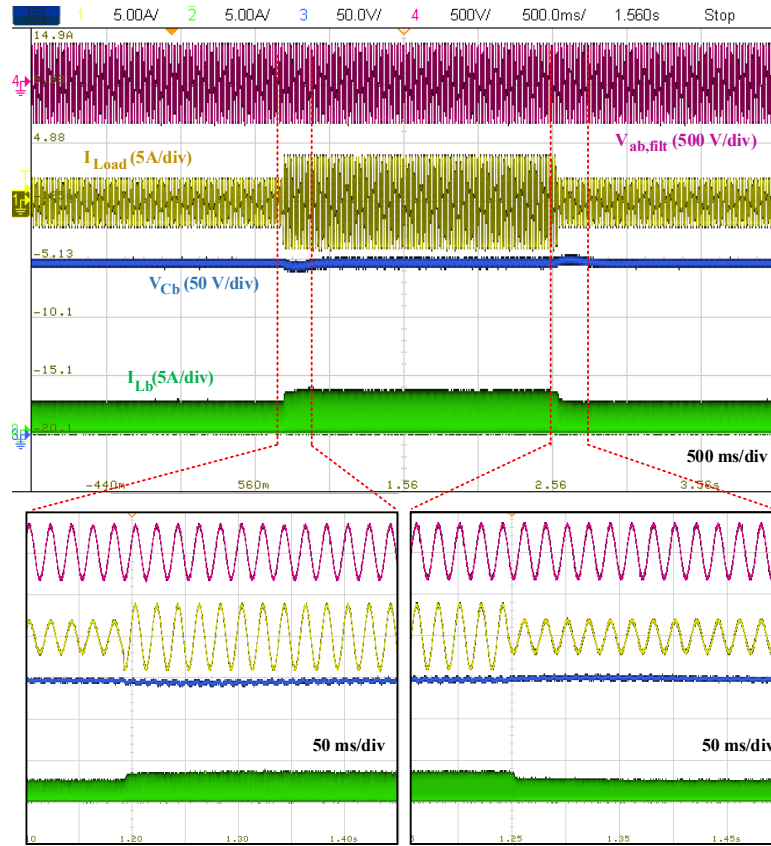


Fig. 12: Key waveforms of the converter for positive and negative changes of the load deploying the schematic control shown in Fig. 9 for the DC-bus voltage regulation with the current estimator feedforward term.

Conclusion

In this paper, the DC-bus control of AMLIs with an embedded Buck-Boost converter is investigated. It is shown that the controller bandwidth can be crucial for the proper operation of the topology despite that it offers the desired stability. The influence of the controller bandwidth on the double line frequency component of the inverter input current is studied via simulation and a full schematic control with feedforward current estimator term is shown to meet all the requirements. Concluding, the performance of the presented control method is also tested via experimental probing.

References

- [1] S. Kouro, M. Malinowski, K. Gopakumar et al., "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553-2580, 2010.
- [2] K.K. Gupta, A. Ranjan, P. Bhatnagar et al., "Multilevel inverter topologies with reduced device count: a review," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 135-151, 2016.
- [3] S. Strache, R. Wunderlich and S. Heinen, "A comprehensive quantitative comparison of inverter architectures for various PV systems PV cells and irradiance profiles," *IEEE Trans. Sustain. Energy*, vol. 5, no. 3, pp. 813-822, 2014.
- [4] A. Anurag, N. Deshmukh, A. Maguluri and S. Anand, "Integrated DC–DC Converter Based Grid-Connected Transformerless Photovoltaic Inverter With Extended Input Voltage Range," *IEEE Trans. Power Electron.*, vol. 33, no. 10, pp. 8322-8330, Oct. 2018.
- [5] S. S. Lee, C. S. Lim, Y. P. Siwakoti and K. Lee, "Dual-T-Type Five- Level Cascaded Multilevel Inverter With Double Voltage Boosting Gain," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 9522-9529, Sept. 2020.
- [6] S. Dhara and V. T. Somasekhar, "An Integrated Semi-Double Stage- Based Multilevel Inverter With Voltage Boosting Scheme for Photovoltaic Systems," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 8, no. 3, pp. 2326-2339, Sept. 2020.

- [7] S. Madhu Babu and B. L. Narasimharaju, "Single-phase boost DC-link integrated cascaded multilevel inverter for PV applications," *IET Power Electronics*, vol. 13, no. 10, pp. 2086-2095, 2020.
- [8] T. P. Mouselinos and E. C. Tatakis, "A Buck-Boost Embedded Multilevel Inverter with Double Voltage Gain," 2021 23rd European Conference on Power Electronics and Applications (EPE'21 ECCE Europe), 2021, pp. 1-10.
- [9] H. Wu, L. Zhu, F. Yang, T. Mu and H. Ge, "Dual-DC-Port Asymmetrical Multilevel Inverters With Reduced Conversion Stages and Enhanced Conversion Efficiency," in *IEEE Trans. on Ind. Electron.*, vol. 64, no. 3, pp. 2081-2091, March 2017
- [10] S. Cuk and R. D. Middlebrook, "A general unified approach to modeling switching DC-to-DC converters in discontinuous conduction mode," in *Proc. IEEE PESC'77*, 1977, pp. 36–57.
- [11] Jian Sun, D. M. Mitchell, M. F. Greuel, P. T. Krein and R. M. Bass, "Averaged modeling of PWM converters operating in discontinuous conduction mode," in *IEEE Transactions on Power Electronics*, vol. 16, no. 4, pp. 482-492, July 2001.
- [12] M. Ciobotaru, R. Teodorescu and F. Blaabjerg, "A new single-phase PLL structure based on second order generalized integrator," 2006 37th IEEE Power Electronics Specialists Conference, Jeju, 2006, pp. 1-6.
- [13] Y. Xue, L. Chang, S. B. Kjaer, J. Bordonau, and T. Shimizu, "Topologies of single-phase inverters for small distributed power generators: an overview," *IEEE Trans. Power Electron.*, vol. 19, no. 5, pp. 1305–1314, Sep. 2004.
- [14] G. C. Goodwin, S. F. Graebe, and M. E. Salgado, *Control System Design*. New York: Prentice Hall, Sep. 2001.
- [15] M. Liserre, F. Blaabjerg and S. Hansen, "Design and control of an LCL-filter-based three-phase active rectifier," *IEEE Trans. Ind Appl.*, vol. 41, no. 5, pp. 1281-1291, Sept.-Oct. 2005.