Potentials to Improve the Post-Fault Performance of a Fault-Tolerant Inverter System in Electrified Aircraft Propulsion System

Yongtao Cao[1,2], Leon Fauth[1,2], Jens Friebe[1,2] and Axel Mertens[1,2]
[1]Cluster of Excellence SE[2]A - Sustainable and Energy-Efficient Aviation
Technische Universität Braunschweig
Universitätsplatz 2
38106 Braunschweig, Germany
[2]Institute for Drive Systems and Power Electronics
Leibniz Universität Hannover
Welfengarten 1
30167 Hannover, Germany
Phone: +49 511 762 14121
Email: Yongtao.Cao@ial.uni-hannover.de
URL: https://www.ial.uni-hannover.de/

Acknowledgments

We would like to acknowledge the funding by the Deutsche Forschungsgemeinschaft (DFG, German Research Foundation) under Germany's Excellence Strategy – EXC 2163/1 - Sustainable and Energy-Efficient Aviation – Project-ID 390881007. The authors are responsible for the content of this publication.

Keywords

≪Fault tolerance≫, ≪Reliability≫, ≪All Electric Aircraft≫

Abstract

Due to the increased exposure to cosmic radiation at higher flight altitude, a significant voltage derating of power semiconductors is required to reduce the failure rate of the inverters designed for electrified aircraft propulsion systems. By utilizing the necessary oversized block-voltage capability of the power semiconductors while employing the concept of variable DC-link voltage, post-fault performance of the inverter system can be improved.

Introduction

To achieve the ambitious goal of net-zero carbon emissions in Europe by 2050, several projects have been proposed to investigate sustainable and energy-efficient aviation through electrified propulsion systems. However, electrification of aircraft propulsion systems is still confronted with several technical challenges, especially in terms of reliability. For the application of power electronic converters in aircraft propulsion systems, the increased exposure to cosmic radiation at high altitude, changing ambient temperature during a flight mission and low air pressure at high altitude all pose new challenges. These working conditions should be carefully taken into account during the design phase. For example, compared to an application on the ground, a greater voltage derating of the power semiconductors due to increased exposure to cosmic radiation at high altitude needs to be considered to reduce the device failure rate in aircraft application [1].

The system reliability can be further improved by using a twin-motor propulsion architecture. However, the loss of one motor is still serious for large passenger aircraft, especially when it happens at

low altitude and low airspeed, where maximum power is needed during take-off, as it could potentially result in a catastrophic accident [2]. In order to avoid the consequences of motor shutdown due to power semiconductor failure and improve the overall system reliability, fault-tolerant inverter systems can be implemented in the electric aircraft propulsion system. In [3], multilevel inverters with potential fault-tolerance such as active neutral point clamped (ANPC) inverter, neutral point clamped (NPC) inverter, modular multilevel converter (MMC) and T-Type inverter are investigated for future electric aircraft propulsion systems. Based on the classic fault-tolerant inverter concepts, this paper introduces the potential to improve their post-fault performance in aircraft applications by utilizing the necessary oversizing of the power semiconductors due to cosmic radiation. These strategies are especially practical when the fault happens at take-off with low flight altitude (less cosmic radiation) and high power demand. Combined with the concept of variable DC-link voltage, the post-fault performance can be improved yet further.

Mission profile and voltage utilization

In Fig. 1, the mission profile of an electric short-range aircraft derived from [4] is shown. Its cruising altitude is at 6 km above sea level. For mid- or long-range aircraft, the cruising altitude could be up to 12 km. As can be seen from the figure, maximum power and maximum output voltage are required at take-off, where the flight altitude is still low. Due to the single-event burnout effect (SEB), necessary voltage derating of power semiconductors needs to be considered to reduce the failure rate for aircraft applications.

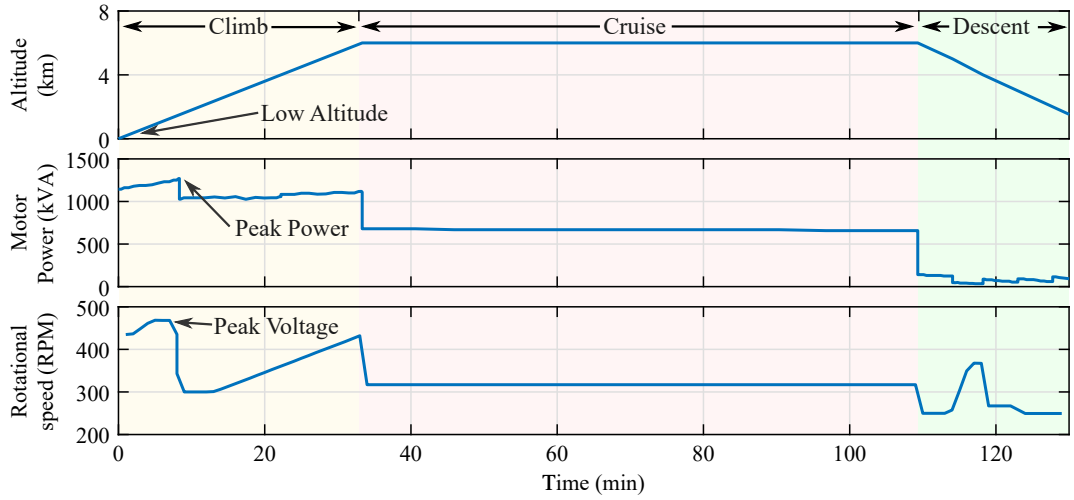

Fig. 1: Typical mission profile for a short range flight, with data based on [4]. The flight altitude (top), motor power (middle) and rotational speed (bottom), which is also proportional to the motor voltage. Most critical for cosmic radiation induced failures is the cruise phase because of the high altitude.

The SEB like all single-event effects (SEE) is a random failure which can not be predicted and can cause a sudden destruction of a semiconductor device. It is generated by a radiation particle interacting with the active area of the semiconductor. These are mainly neutrons in typical aircraft applications, which are generated by spallation from cosmic radiation. The number of available particles increases exponentially with higher altitudes [5]. Due to the stochastic nature of the failure mechanism, a linear dependency of the failure rate on the number of particles is assumed, resulting in an exponential dependency of the failure rate on the flight altitude. Additionally, the failure rate is increased if the device is operated closer to its breakdown voltage level [6]. Based on this, the failure rate of a 1700 V SiC-MOSFET per square centimeter of chip area is depicted as a function of the voltage utilization at different flight altitudes in Fig. 2.

Since the failure rate of the current airliner engine is around 1000 FIT (FIT: failure in time, 1 FIT = 1 Failure in 10^9 device hours) to meet the aircraft safety requirement [7], 1000 FIT can be set as the

reference failure rate of one electrified aircraft propulsion system composed of battery, power electronic systems, electric motor and propeller (or turbofan). The required failure rate of the inverter system in an electrified aircraft propulsion system can therefore be expected to be around hundred or several hundred FIT. Considering the fact that capacitors, driver board, PCB and power semiconductors all contribute to the inverter system failure rate, for a megawatt-level (3 MW to 20 MW) multilevel inverter with large chip areas (200 cm^2 to 1200 cm^2, chip areas are estimated according to the method introduced in [3]), the maximum acceptable failure rate of the power semiconductor is considered to be at least less than 0.1 FIT per square centimeter in this paper. In practical applications, the failure rate requirement of the power semiconductors may vary slightly, depending on the failure rate allocation in the electric propulsion drive system. However, the aim of this paper is only to show the potential to improve the post-fault performance in electrified aircraft applications. As can be seen from Fig. 2, 45% voltage utilization at cruise altitude of 6 km above sea level is required for a 1700 V SiC-MOSFET to maintain this required failure rate. Compared to aircraft applications, 67% voltage utilization of the power semiconductor is typical for the drive systems in electric vehicle on the ground, a 1200 V SiC-MOSFET is usually used to block the 800 V DC-link voltage. In this paper, 67% will be assumed to be the maximum allowed voltage utilization of the power semiconductors for an emergency situation at low altitude.

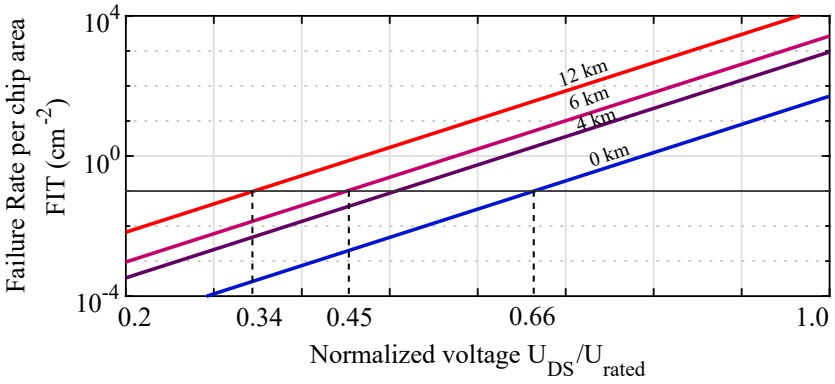

Fig. 2: Example failure rate for a 1.7 kV SiC-MOSFET at different altitude. Failure rate data based on results from [6].

Fixed DC-link voltage while utilizing the necessary oversizing

A multilevel inverter such as an MMC has multiple power semiconductors connected in series per arm (see Fig. 3). By applying an appropriate fault-tolerant control strategy and fault-tolerant isolation methodology in the design, the inverter system can still provide full performance despite the failure of a submodule. However, if the DC-link voltage of the inverter system is fixed, the other healthy submodules in the faulty arm must be able to withstand a higher voltage stress for fault-tolerant operation, meaning that oversized or redundant devices are necessary for classic fault-tolerant design. Nevertheless, by utilizing the necessary oversizing resulting from power semiconductor voltage derating implemented to withstand cosmic radiation and choosing a suitable number of submodules, unnecessary oversizing or redundancy can be avoided for fault-tolerant operations.

In Fig. 3, a fault-tolerant MMC with a fixed 3 kV DC-link voltage U_{DC} is depicted as an example. If SiC-MOSFET with a rated blocking voltage $U_{\mathrm{DS}} = 1700$ V is chosen for this application, at least four submodules per arm are required to block the full DC-link voltage U_{DC} due to their required maximum voltage utilization $u_1 = 0.45$ at the cruise altitude of 6 km:

$$\frac{U_{\mathrm{DC}}}{U_{\mathrm{DS}} \cdot n} = \frac{3000\ \mathrm{V}}{1700\ \mathrm{V} \cdot 4} = 0.44 < u_1 \tag{1}$$

In case of a submodule failure, the failed submodule can be isolated with a bypass switch. If voltage utilization $u_{max} = 0.67$ is allowed for power semiconductors at take-off and emergencies, the rest of the

three submodules can still block the full DC-link voltage U_{DC} with the voltage utilization u_{fault}.

$$\frac{U_{\mathrm{DC}}}{U_{\mathrm{DS}} \cdot (n-1)} = \frac{3000\ \mathrm{V}}{1700\ \mathrm{V} \cdot (4-1)} = u_{\mathrm{fault}} < u_{\mathrm{max}} \tag{2}$$

In this case, no redundant submodule or extra oversizing is required for this fault-tolerant operation. However, additional by-pass switches for fault isolation in the submodules will still bring additional costs.

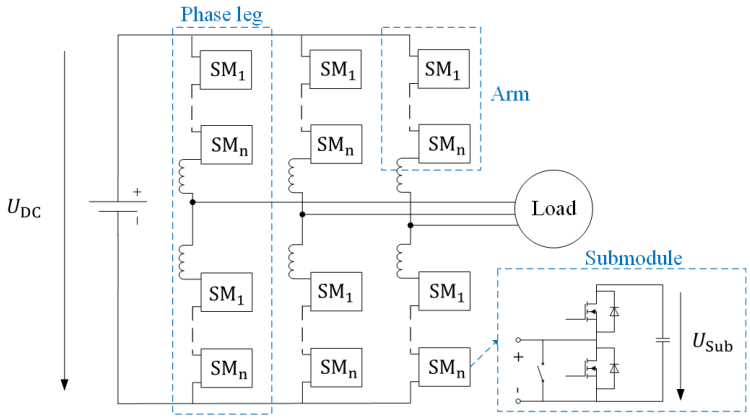

Fig. 3: Fault-tolerant MMC

Optimized variable DC-link voltage for fault-tolerant operation

In the following section, variable DC-link voltage strategies will be introduced to improve the post-fault performance of the power converter by utilizing the block-voltage capability of its power semiconductors. A NPC inverter will be analysed in a case study.

Optimized reduced DC-link voltage for fault-tolerant operation of NPC inverter

As can be seen from Equation (2), for fault-tolerant operation of a multilevel inverter with fixed DC-link voltage and multiple power semiconductors connected in series, a higher maximum voltage utilization u_{max} is required as n decreases. However, u_{max} is limited due to the overvoltage protection requirement. Such a limitation is especially critical for the fault-tolerant operation of a three-phase three-level NPC.

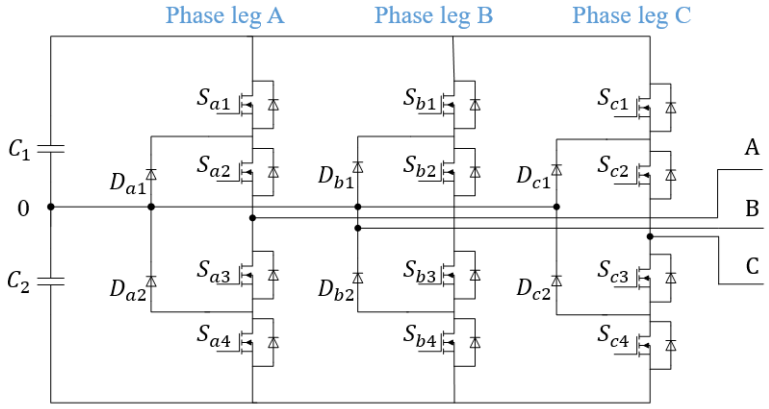

Fig. 4: Three-phase three-level NPC inverter

For example, if the outer power semiconductor S_1 has a short circuit failure (see Fig. 5 left), the inner power semiconductor S_2 has to withstand the full DC-link voltage during '-' state (S_3 and S_4 on). However, power semiconductors of the NPC inverter are usually only designed to be able to block half of the DC-link voltage U_{DC}, the increased voltage of S_2 could lead to a secondary failure and eventually result

in system shutdown. Furthermore, due to the short circuit of S_1, the '0' state can also not be realized (the current flow through D_5 and S_2 is not possible since S_2 cannot be turned on). As can be seen from Fig. 5, only the white area of the space vector diagram can be reached in this case, a symmetric circular vector trajectory therefore cannot be generated [8].

However, if the DC-link voltage of the NPC inverter can be adjusted (reduced) for this fault scenario in such a way, that the voltage stress on S_2 is reduced in an acceptable range, the '-' state is available again, the NPC inverter can at least work in a 2-level mode allowing the use of a full modulation index in this case (see Fig. 5 right). In an emergency, especially when the fault happens during take-off of the electric aircraft, the necessary oversizing of the power semiconductors due to cosmic radiation can be utilized to maximize the post-fault performance. For example, in Fig. 5, 1700 V SiC-MOSFETs are employed in an NPC inverter with 1500 V U_{DC}. The voltage utilization of the power semiconductors is 44%, which corresponds to the required voltage derating in aircraft applications with a cruise altitude of 6 km (see Fig. 2). When employing the strategy of variable DC-link voltage, 1139 V U_{DC} ($1700\mathrm{V} \cdot 67\% = 1139\mathrm{V}$) can be applied to the DC-link in this fault scenario, which corresponds to 76% ($1139\mathrm{V}/1500\mathrm{V} = 76\%$) of the original maximum output voltage of the NPC inverter with fixed DC-link voltage. System shutdown can thus be avoided with this strategy. In Fig. 6, the fault-tolerant strategy is validated in a simulation with constant load parameter, where the fault occurs at 0.05 seconds followed by the proposed fault-tolerant strategy with decreased DC-link voltage.

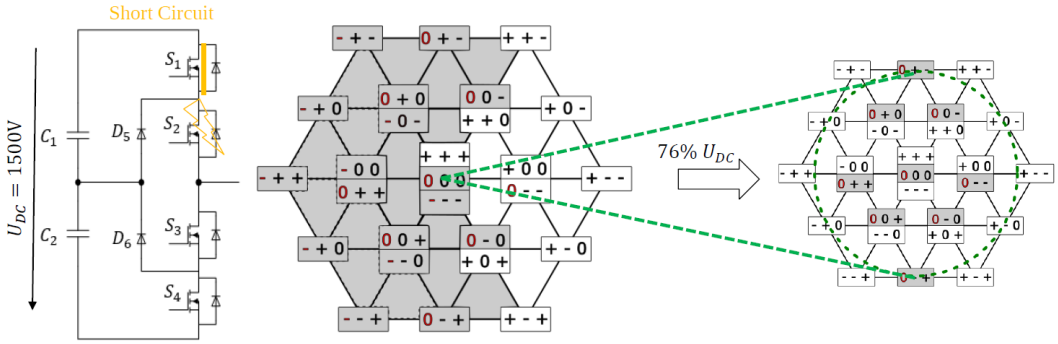

Fig. 5: Improved post-fault performance of an NPC using an optimized decreased DC-link voltage when S_1 suffers a short circuit. Red switching states are not available under this kind of fault, grey areas of the space vector diagram are therefore not reachable anymore. With reduced DC-link voltage (76% U_{DC}), the '-' state is possible again due to the reduced voltage stress on S_2 (67% voltage utilization) to realize fault-tolerant operation (right space vector diagram).

The variable DC-link voltage can either be adjusted with a DC-DC converter at the battery side of the DC distribution system or using the converter system in a serial-hybrid electric aircraft propulsion system.

It should also be mentioned that, such kind of strategy is under the assumption of power semiconductors with safe short circuit capability (in this case: S_1), allowing carrying the current further under its short circuit failure. One of the solutions is to use press-pack packaging. Press-pack packaging also brings the benefit of better cooling capability compared with wire-bonded power semiconductors. However, the higher cost of press-pack technology is one of the main reasons that limited its widespread use [9].

Optimized increased DC-link voltage for fault-tolerant operation of NPC inverter

For a single-event fault scenario such as an open circuit of S_1, or short circuit of S_2, an NPC with fixed DC-link voltage can use its clamping path to connect one faulty phase to the DC mid-point, so that the inner hexagon of the space vector diagram can still be used for fault-tolerant operation with reduced output (50 % degradation) (see Fig. 7). An ANPC inverter has more flexibility in the use of this strategy due to its clamping active controllable power semiconductors in the clamping path [10].

With the help of a variable DC-link voltage in the NPC or ANPC inverter system, the inner hexagon of the space vector can be further increased in the emergency case of take-off by utilizing the necessary

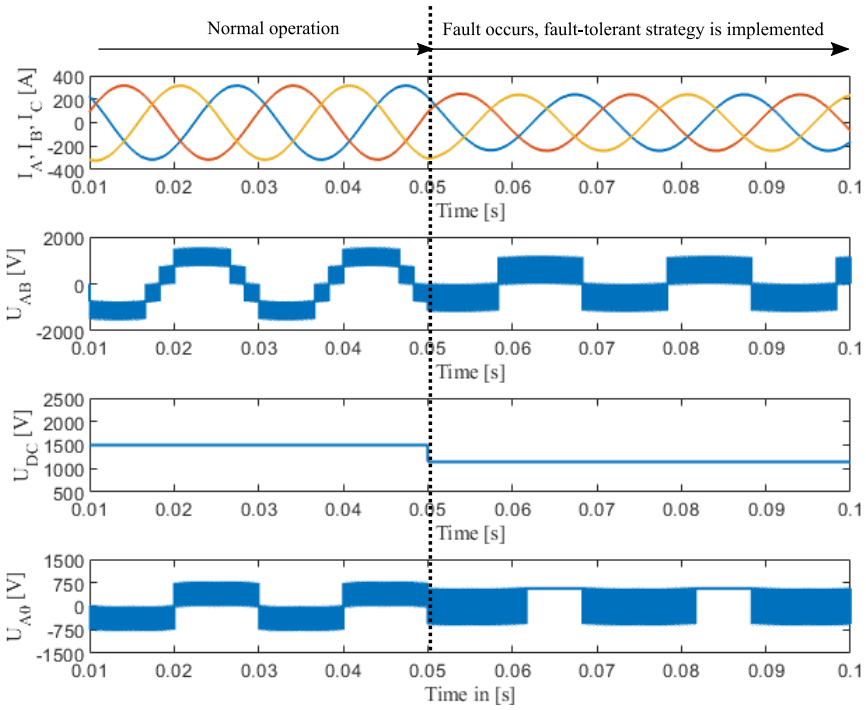

Fig. 6: Improved post-fault performance with proposed strategy under short circuit failure of the outer power semiconductor S_1 in a three-phase three-level NPC inverter (fault occurs at 0.05 seconds)

oversizing of the power semiconductors due to cosmic radiation. To give an example in Fig. 7, 1700 V SiC-MOSFETS are employed on a NPC inverter with 1500 V DC-link voltage, which corresponds to the required 44 percent voltage utilization of the power semiconductor at cruise. Under the condition of open circuit of S_1, 50 percent of the maximum output voltage can still be generated for fault-tolerant operation (see Fig. 7 middle). If the DC-link voltage is adjustable during take-off in this scenario, it can be increased to 2278 V. The voltage utilization on the power semiconductors is increased from 44 % to 67 % (2278 V / 2 / 1700 V = 67 %), allowing the necessary oversizing to be utilized. Compared to the maximum output of the NPC with fixed DC-link voltage during fault-tolerant operation, 76 % (2278 V / 2 / 1500 V = 76 %) of its maximum output voltage can still be provided, instead of 50 %. In Fig. 8, the fault-tolerant strategy is validated in a simulation with constant load parameter, where the fault occurs at 0.05 seconds followed by the proposed fault-tolerant strategy with increased DC-link voltage.

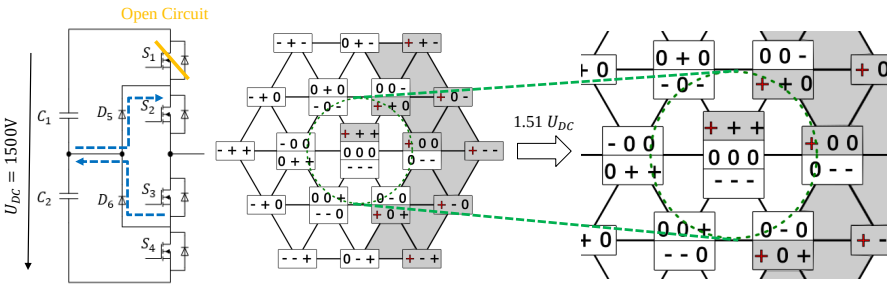

Fig. 7: Improved post-fault performance of an NPC using an optimized increased DC-link voltage strategy under the condition of the short circuit of S_1. Red switching states are not available, grey areas of the space vector diagram are therefore not reachable anymore, a smaller symmetric circular vector trajectory can still be generated. With increased DC-link voltage (151% U_{DC}), the voltage utilization of the power semiconductors can be maximized to increase the inner hexagon of the space vector diagram.

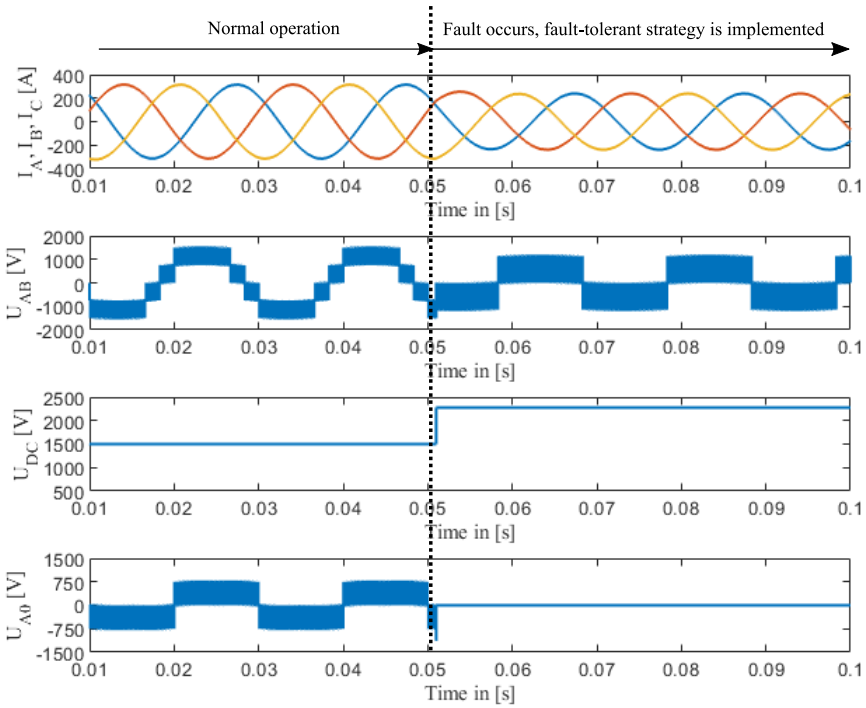

Fig. 8: Improved post-fault performance with proposed strategy under open circuit failure of the outer power semiconductor S_1 in a three-phase three-level NPC inverter (fault occurs at 0.05 seconds)

Conclusion

In this paper, the effect of cosmic radiation on the voltage derating of the power semiconductors in aircraft applications was discussed. By utilizing the necessary oversizing and combining this with proposed fault-tolerant design methodologies, a modular multilevel inverter with a fixed DC-link voltage can still provide full performance if one submodule fails. Considering a conventional 3-level inverter like NPC or ANPC, the post-fault performance of the inverter system can be further improved with the proposed concept of a variable DC-link voltage. The improved post-fault performance can contribute to aircraft safety, especially during take-off, when the maximum power is required and the flight altitude is low.

References

[1] H. Schefer, L. Fauth, T. H. Kopp, R. Mallwitz, J. Friebe and M. Kurrat, "Discussion on electric power supply systems for all electric aircraft," in IEEE Access, vol. 8, pp. 84188-84216, 2020.

[2] D. Kritzinger: "Aircraft system safety - military and civil aeronautical applications," Woodhead Publishing, pp.76-77, 2006.

[3] J. Ebersberger, M. Hagedorn, M. Lorenz and A. Mertens, "Potentials and Comparison of Inverter Topologies for Future All-Electric Aircraft Propulsion," in IEEE Journal of Emerging and Selected Topics in Power Electronics.

[4] S. Karpuk and A. Elham, "Influence of novel airframe technologies on the feasibility of fully-electric regional aviation," Aerospace, vol.8, no.6, pp.163, 2021.

[5] Measurement and Reporting of Alpha Particle and Terrestrial Cosmic Ray-Induced Soft Errors in Semiconductor Devices, JESD89A, JEDEC Solid State Technology Association, Oct. 2006. [Online]. Available: https://www.jedec.org/sites/default/files/docs/jesd89a.pdf

[6] C. Felgemacher, S. V. Araujo, P. Zacharias, K. Nesemann, and A. Gruber, "Cosmic radiation ruggedness of Si and SiC power semiconductors," in 2016 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD), Prague, Czech Republic, Jun. 2016 - Jun. 2016, pp. 51–54.

[7] A. H. Epstein and S. M. O'Flarity, "Considerations for reducing aviation's CO2 with aircraft electric propulsion, " Journal of Propulsion and Power, vol.35, no.3, pp.572–582, 2019.

[8] Y. Cao, L. Fauth, A. Mertens and J. Friebe, "Comparison and Analysis of Multi-State Reliability of Fault-Tolerant Inverter Topologies for the Electric Aircraft Propulsion System," 2021 24th International Conference on Electrical Machines and Systems (ICEMS), 2021, pp. 766-771.

[9] K.-B. Lee and J.-S. Lee, "Reliability Improvement Technology for Power Converters," Power Systems, 2017.

[10] J. Li, A. Q. Huang, Z. Liang and S. Bhattacharya, ”Analysis and Design of Active NPC (ANPC) Inverters for Fault-Tolerant Operation of High-Power Electrical Drives,” in IEEE Transactions on Power Electronics, vol. 27, no. 2, pp. 519-533, Feb. 2012.