Modular multilevel converter control with using a general space vector PWM method in medium voltage hydro power application

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Keywords

≪Space Vector PWM≫, ≪Modular Multilevel Converters (MMC)≫, ≪Converter control≫, ≪Efficiency≫.

Abstract

This paper studies a generalized space vector PWM (SVPWM) method for modulating the modular multilevel converter (MMC) for a medium voltage hydropower application. In addition to the modulation of the MMC, the circulating current control and the submodule capacitor voltage balancing are included in the study. The simulation and experimental results show the feasibility of using the generalized SVPWM method for controlling the MMC. Furthermore, the loss study shows that the switching loss in the MMC can be reduced with 28% when a modification of the generalized SVPWM method is utilized, thus, the total efficiency of the converter can be increased.

Introduction

As the requirement of reducing greenhouse emissions is more and more urgent, the total installed capacity of renewable energy, such as wind power and solar power, are growing. However, renewable energy also brings fluctuations to the energy generation due to intrinsic characteristics. Therefore, to facilitate the integration of renewable energy into the grid, flexible energy storage methods are needed; and the century-old pumped storage hydropower technology can be one of those methods.

Traditionally, the machine and turbine/pump of pumped storage hydropower stations are working under fixed speed, which is associated with the grid frequency. Later, it is found that the overall efficiency of the system can be increased when variable speed operation is employed [1]. Then, the double-fed induction machine (DFIM) technology is widely used in pumped storage hydropower stations. However, DFIM is more suitable for high capacity power stations. For those with the installed capacity below 100 MW, the converter-fed synchronous machine (CFSM) technology is preferred [2]. The key component in the CFSM technology is the converter, which is the interface between the machine and the grid.

Due to the high voltage level in the system, it is natural to think that multilevel converter topology can be employed. The MMC [3], which belongs to the multilevel converter family, has been widely used in the HVDC applications [4], and it is a good candidate for the CFSM hydropower application. For HVDC applications, the voltage levels of an MMC can be a few hundred, thus the nearest level modulation

(NLM) is most suitable [4]. For pumped storage hydro power, since the voltage level is not that high, to optimize the performance of the converter, SVPWM can be utilized [5].

In [6], it is shown that multilevel converter can be controlled with a generalized SVPWM method, however, the application is for cascaded H-bridge (CHB) converter. The SVPWM scheme in [7] is for MMC, while the control of circulating current and submodule voltage balancing are not included. In [5], the circulating current control and submodule voltage balancing are given along with the SVPWM method, however, the controllers structure are complicated, and the controller parameters needs to be tuned.

The purpose of this paper is to study a generalized SVPWM method for the MMC modulation in a hydropower application. In the meanwhile, a simple circulating current control and a submodule voltage balancing control are being studied to show the possibility of integrating different control aspects for the MMC with the generalized SVPWM method. At the end of this study, a modification of the generalized SVPWM is investigated to show the potential of decreasing the switching loss of the converter.

The general SVPWM method

SVPWM has been widely used in some multilevel converter applications, for instance, in the applications where three-level NPC converters are used, and it can be employed for a converter with even higher voltage levels. However, with the increase of the voltage level, the voltage vectors increases drastically. For a $n+1$ level converter, the SVPWM has $(n+1)^3 - n^3$ voltage vectors [6]. Fig. 1 shows the space vector plane for a five-level converter.

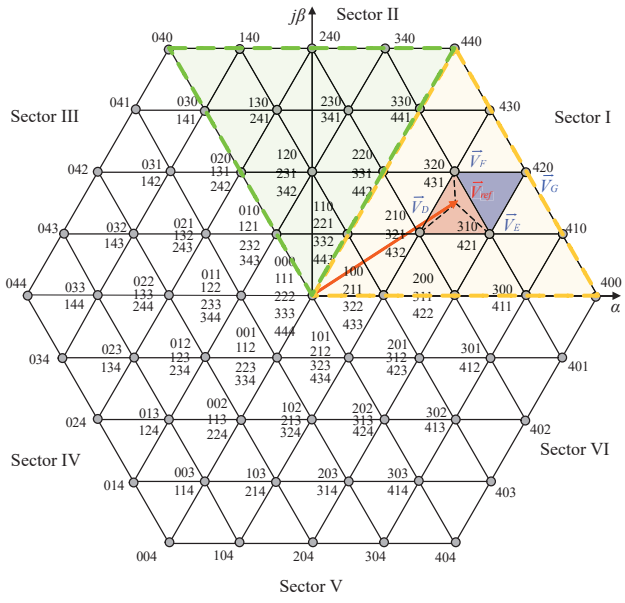


Fig. 1: Space vector plane for a five-level converter

In the same manner as in the two-level SVPWM, the primary task of the SVPWM for a multilevel converter is to find the three closest voltage vectors and its corresponding dwell time which can be used to synthesize the reference voltage vector. For example, the reference voltage $\overrightarrow{V_{ref}}$ in Fig. 1 can be synthesized by small voltage vectors $\overrightarrow{V_D}$, $\overrightarrow{V_E}$, and $\overrightarrow{V_F}$. Some of the small voltage vectors in Fig. 1 contain more than one switching state, for example, the small voltage vector $\overrightarrow{V_D}$ contains three switching states: [210], [321], and [432]; and these switching states in one small voltage vector are called redundant states. The challenge of using SVPWM for a multilevel converter is to select the appropriate switching states to synthesize the reference voltage vector.

One way to tackle this challenge is to use predefined look-up tables for the switching states in the controller, however, the complex lookup table for storing the switching states results in a large burden on the

controller memory. In [6], a generalized SVPWM method for the multilevel converter is proposed, and in [8], this method is being successfully utilized for modulating a five-level NPC converter. The process of this generalized SVM method is being briefly described in the following paragraphs, and the details of the overall process can be found in [8].

Firstly, based on the angle of $\overrightarrow{V_{ref}}$ in the space vector plane, the sector number where $\overrightarrow{V_{ref}}$ is located can be found. If $\overrightarrow{V_{ref}}$ is located in a sector other than Sector I, then the angle conversion which listed in Table I is utilised to converter $\overrightarrow{V_{ref}}$ to Sector I, and this step is the same as in the two-level SVPWM.

Table I: Reference voltage angle transformation

Sector	Angle θ	Angle θ′
1	(0, π/3]	θ' = θ
2	(π/3, 2π/3]	$\theta' = -\theta + 2\pi/3$
3	(2π/3, π]	$\theta' = \theta - 2\pi/3$
4	(π, 4π/3]	$\theta' = -\theta - 2\pi/3$
5	(4π/3, 5π/3]	$\theta' = \theta + 2\pi/3$
6	(5π/3, 2π]	$\theta' = -\theta$

Secondly, $\overrightarrow{V_{ref}}$ is being normalized with respect to $2V_{dc}/3$ to get v^*, then v^* is being transferred from αβ coordinate system to a new 60^o coordinate system (α′β′) according to

$$\begin{cases} v_{\alpha'} = v^* cos\theta - \hat{V} sin\theta/\sqrt{3} & (1) \\ v_{\beta'} = v^* sin\theta \cdot 2/\sqrt{3} & (2) \end{cases}$$

where v^* is the normalized voltage vector and θ is the vector angle. Once $v_{\alpha'}$ and $v_{\beta'}$ are calculated, the following vectors of the parallelogram $DEFG$ which contains the reference vector in the space vector plane can be calculated,

$$\begin{bmatrix} V_D \\ V_E \\ V_F \\ V_G \end{bmatrix} = \begin{bmatrix} floor(v_{\alpha'}) & floor(v_{\beta'}) \\ ceil(v_{\alpha'}) & floor(v_{\beta'}) \\ floor(v_{\alpha'}) & ceil(v_{\beta'}) \\ ceil(v_{\alpha'}) & ceil(v_{\beta'}) \end{bmatrix} \quad (3)$$

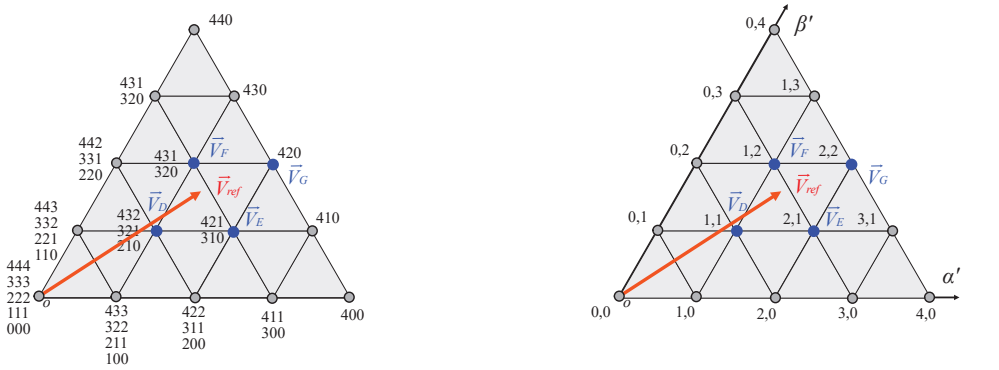
Fig. 2 shows one-sixth of the five-level SVPWM plane when mapping from αβ coordinates to α′β′ coordinates.

Thirdly, based on the new coordinates in the 60^o α′β′ coordinate system, the triangle which contains $\overrightarrow{V_{ref}}$ is decided. There are two types of triangles in general, one is type DEF, and another one is type EFG. If $\overrightarrow{V_{ref}}$ falls in the triangle DEF, then the voltage vectors that used to synthesize $\overrightarrow{V_{ref}}$ are being switched in the following order, $\overrightarrow{V_D} \rightarrow \overrightarrow{V_E} \rightarrow \overrightarrow{V_F} \rightarrow \overrightarrow{V_D}'$, where $\overrightarrow{V_D}'$ is the redundant switching states of $\overrightarrow{V_D}$. If $\overrightarrow{V_{ref}}$ is insider triangle EFG, then the sequence of the switching states are $\overrightarrow{V_E} \rightarrow \overrightarrow{V_F} \rightarrow \overrightarrow{V_G} \rightarrow \overrightarrow{V_E}'$. The dwell time of the corresponding voltage vectors can be calculated in the 60^o α′β′ coordinate system.

At the end, once the switching states and corresponding dwell time are acquired, based on a transformation matrix, the switching states can be acquired in the normal αβ coordinate system, while the dwell time of each voltage vector is the same.

Modification of the generalized SVPWM for the MMC

The schematic diagram of the MMC is shown in Fig. 3. For a $n+1$ level MMC, each arm of the MMC consists of a n number of submodules and one arm inductor L_0. The presence of the arm inductor in the circuit can prevent inrush current [9], and it can limit the circulating current as well.



(a) Space vector plane, αβ coordinates

(b) Space vector plane, 60^o α′β′ coordinates

Fig. 2: SVM vectors converting from αβ coordinates to α′β′

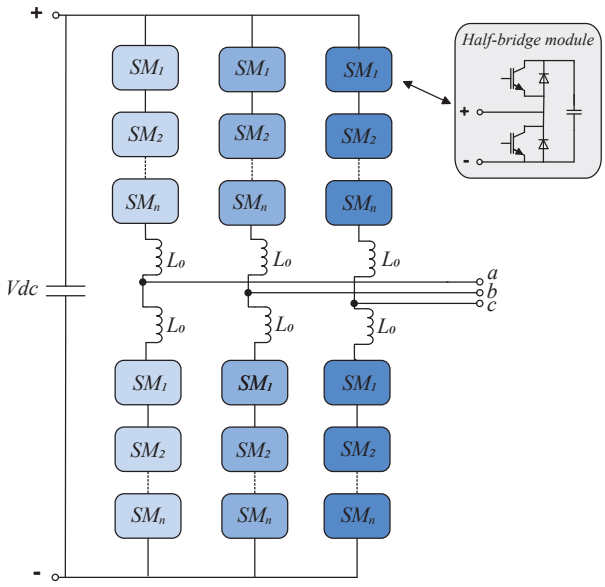


Fig. 3: Schematic diagram of the MMC topology

The studied submodule is a half-bridge IGBT submodule, which has shown the lowest losses and the lowest cost in HVDC applications [10]. The half-bridge submodule consists of two IGBT-diode switch pairs and one capacitor, and the two IGBTs in the half-bridge SM are being switched in a complementary mode. The submodule can be inserted into or bypassed from the circuit, depending on the switching states of the two IGBTs.

For the multilevel NPC converter, the aforementioned SVPWM method can be used directly, whereas, for the MMC, a modification of the SVPWM is needed due to the need of a "dual-modulator" for both the upper arm and the lower arm of the MMC. Fig. 4 shows the two voltage references for the upper arm ($\overrightarrow{V_{ref}}$) and lower arm ($\overrightarrow{V_{ref}}'$) of the MMC when using the SVM modulation. The two voltage references rotate in the same direction with a phase-shift of 180°.

By using the aforementioned generalized SVPWM method, the small voltage vectors for synthesizing the upper arm reference voltage can be determined. For the lower arm, there are two ways to determine the small voltage vectors. The first way is to use the voltage vector $[nnn]$ minus the corresponding upper arm small voltage vectors, where n is the number of submodules in each arm. For example, for the five-level MMC with 4 submodules in each arm in Fig. 4, if the small voltage vectors for $\overrightarrow{V_{ref}}$ are [310] →

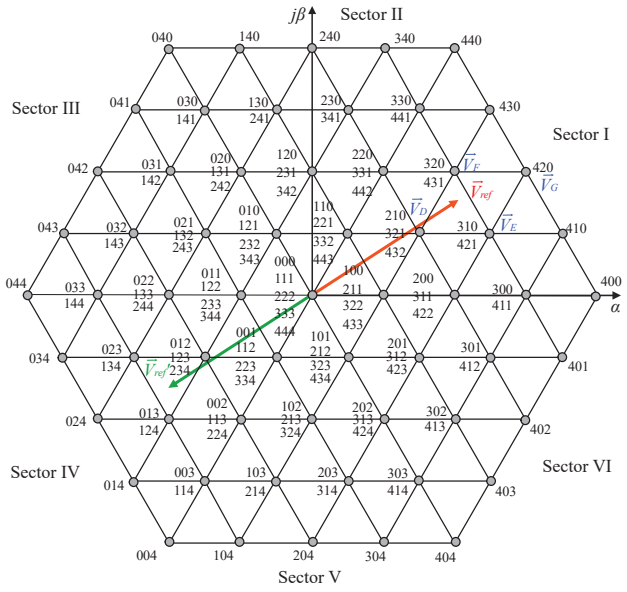


Fig. 4: Dual voltage reference of SVM for MMC

[320] → [321] → [421], then the corresponding small voltage vectors for $\overrightarrow{V}'_{ref}$ would be [134] → [124] → [123] → [023] in Sector IV. However, the drawback of this method is the output phase voltage level would be limited to $n+1$ level, thus, the THD in the output current and voltage would be higher. The second way is to use the redundant switching states of the lower arm small voltage vectors. For example, for the same upper arm $\overrightarrow{V_{ref}}$, instead of using vectors [134] → [124] → [123] → [023], the lower arm small voltage vectors can be [023] → [123] → [124] → [134]. It can be seen that the average number of the total inserted submodules in one phase during one switching period T_{sw} would be equal to n, which is 4 for the five-level MMC.

Circulating current control

The circulating currents flow internally among the converter legs, thus, the converter output voltage and current are not being affected [9]. However, the presence of the circulating currents increases the losses of the power switches in each arm, and that reduces the efficiency of the converter. Thus, it is important to suppress the amplitude of the circulating currents in the MMC.

The circulating currents in the MMC are presented in the form of a negative sequence with the frequency of twice the fundamental frequency, and a double-line frequency circulating current controller [11] can be used to control the circulating currents, and the structure of the controller is shown in Fig. 5.

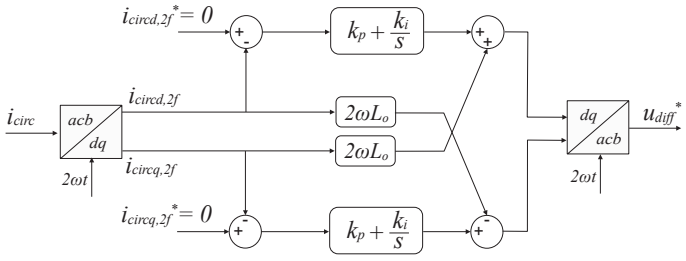


Fig. 5: The double line frequency circulating current controller

The circulating currents are firstly transformed from *acb* to *dq* coordinates. The PI controller is designed in *dq* coordinates, and the parameters of k_p and k_i are acquired by using the loop shaping method to have

a first-order response of the closed-loop system.

Submodule capacitor voltage balancing

For each submodule capacitor, the voltage of it is alternating around the nominal value V_{dc}/n, which is caused by the charging and discharging processes due to the energy exchange. However, the submodule capacitor voltages can be unbalanced and deviate from the nominal value during the operation if no active balancing strategy is applied.

Various submodule voltage balancing methods have been proposed by different researchers, such as in [12], [13] and [14]. In this study, the classical sorting and balancing algorithm, which is based on the submodule capacitor voltages comparison and the polarity of the arm currents, is employed at the modulation stage [15],[16]. The balancing principle is, if the arm current is positive, then the arm submodule capacitor voltages are firstly sorted in ascending order. After that, from the submodule with the lowest capacitor voltage, a certain amount of submodules are inserted into the circuit; the inserted number of the submodule is based on the modulation signal. If the arm current is negative, a similar process is applied, while the order of the sorting for the submodule capacitor voltages is descending. Consequently, the inserted submodule capacitor will be charged or discharged based on the polarity of the arm currents, and the voltage of the corresponding submodule will be increased or decreased, thus, all the submodule capacitor voltages are balanced.

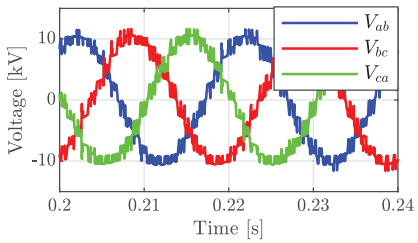
Simulation results

To demonstrate the feasibility of the studied generalized SVPWM method, a simulation model which contains a five-level MMC at the grid side was simulated in MATLAB Simulink and PLECS, and the parameters of the simulation model are listed in Table II. The simulation results are shown in Fig. 6.

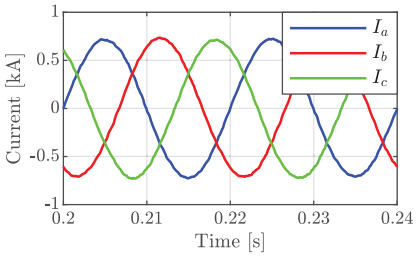
Table II: Submodule and arm parameters of the simulated five-level MMC

Parameters	Value	Unit
Power S	6	MVA
Power factor $cos(\varphi)$	1	/
DC-link voltage V_{dc}	12	kV
Grid phase peak voltage $V_{g,peak}$	5.5	kV
Grid frequency f	50	Hz
PWM frequency modulation ratio m_f	23	/
RL filter Resistance R_f	1.5	mΩ
RL filter inductance L_f	10	mF
Number of submodules in each arm N_{SM}	4	/
Submodule voltage E_{SM}	3	kV
Submodule capacitance C_{SM}	1.41	mF
Arm inductance L_{arm}	5	mH

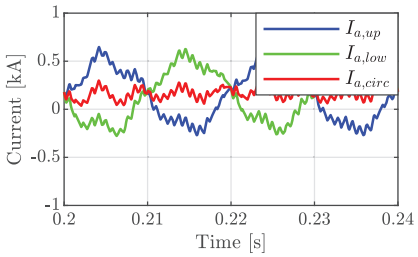
The voltage and current waveforms in Fig. 7a and Fig. 7b show that the generalized SVPWM method works well in the MMC, the line-to-line voltages contain high number of voltage levels and the phase currents are close to sinusoidal shape. The circulating current in Fig. 7c is controlled with the objective to have a minimum oscillation. The submodule capacitor voltages in Fig. 7d are balanced around 3 kV with using the sorting and balancing algorithm. However, it can also be observed that the submodule capacitor voltages are not perfectly symmetrical around 3 kV compared with using PWM method. This is due to the u^*_{diff} signal from the circulating current controller is being subtracted from the modulation signal ($V_{dc}/2 - u_{ref}$), and sometimes this gives a modulation index m_a smaller than 0 or larger than 1, while the actual m_a is being fixed to 0 if $m_a <= 0$ or to 1 if $m_a >= 1$. Due to the fact of two symmetrical arms in the MMC, this change of m_a can cause the modulation signals for the two arms unbalanced, thus, distorts the submodule capacitor voltages.



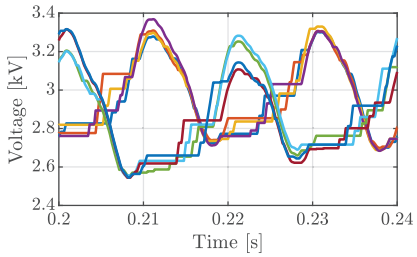
(a) Five-level MMC line to line voltage



(b) Five-level MMC phase currents



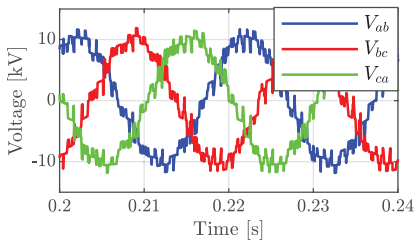
(c) Phase a arm and circulating currents



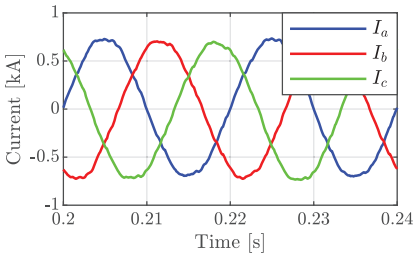
(d) Phase a submodule capacitor voltages

Fig. 6: Five-level MMC converter with SVPWM modulation, 100% power

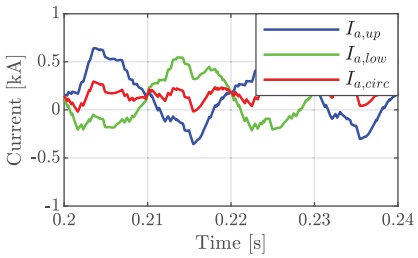
For HVDC applications where the submodules are being switched under the frequency close to fundamental frequency, the switching loss of the converter is not that high, however, for the studied application, the submodules are being switched with 287.5 Hz, which means the switching loss will account for the majority part in the total losses. In addition to this, the submodule capacitor voltages sorting and balancing algorithm will impose more switching events on the submodules, thus, increase the switching loss as well. To decrease the switching loss in the MMC, one way is using the discontinuous SVPWM, which means only five segment of switching states are needed in one switching period. In this study, it is found when using the discontinuous SVPWM for the MMC, that the phase voltage should be maintained with $n+1$ level; if $2n+1$ level operation is utilized, the overall system will become unstable, and the simulation will diverge eventually. The simulation results of using discontinuous SVPWM are shown in Fig.7.



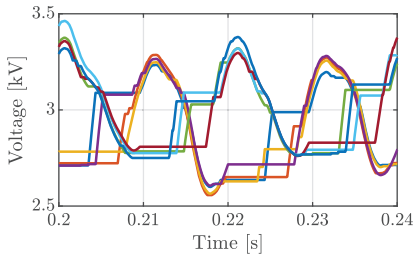
(a) Five-level MMC line to line voltage



(b) Five-level MMC phase currents



(c) Phase a arm and circulating currents



(d) Phase a submodule capacitor voltages

Fig. 7: Five-level MMC converter with discontinuous SVPWM modulation, 100% power

It can be clearly seen that due to the $n+1$ level operation, the current THD in the discontinuous SVPWM case is higher than that in the normal SVPWM case. The circulating current controller and the submodule capacitor voltages balancing algorithm work fine in the discontinuous SVPWM case, while the performance of them are slightly worse when comparing with the normal SVPWM case.

The losses results of the normal SVPWM and discontinuous SVPWM operation are shown in Fig. 8. The value of the losses are being normalized with respect to the nominal power (6 MW) of the system.

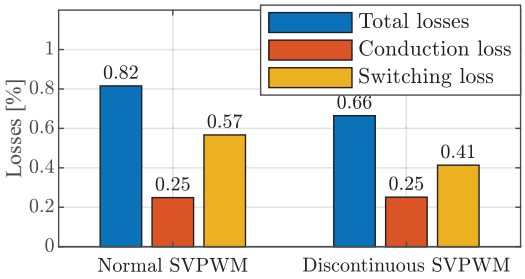


Fig. 8: Loss comparison between normal SVPWM and discontinuous SVPWM

It can be seen that when using the discontinuous SVPWM for modulating the five-level MMC under the defined conditions, the switching loss can be decreased from 0.57% to 0.41%, while the conduction loss are almost the same. The 28% reduction of switching loss is as expected, since the discontinuous SVPWM method requires less switching events for the operation of the MMC, however, the slightly worse waveforms that can be seen in Fig.7 means that the investments on the filter for the discontinuous SVPWM method would be higher in order to have a good voltage and current waveform quality. If the annual power deliver mission profile of the studied application is known, then, a justification of whether the discontinous SVPWM should be employed can be conducted based on the total investment and the total saved energy, i.e., the life-cycle cost.

Experimental results

The experiment focuses on the waveform verification of the SVPWM method for modulating the MMC converter, and the MMC experimental setup is shown in Fig 9.

Fig. 9: Lab set-up of the MMC: 1) DC power supply 2) MMC 3) Three-phase RL load

The lab set-up consists of three main parts: a 400 V DC power supply; a five-level MMC; a three-phase RL load. The five-level MMC contains three B-Box RCP controllers, 24 IGBT submodules, and 6 arm inductors. The used IGBT submodule is shown in Fig. 10.

The submodule includes 4$\times$ IGBT power switches on the board, forming a "H-bridge", while only two of the switches are used in the five-level MMC to form the half-bridge submodule. Apart from the power switches, the submodule also includes 9 $\times$ *PanasonicEET* capacitors to form the submodule capacitor

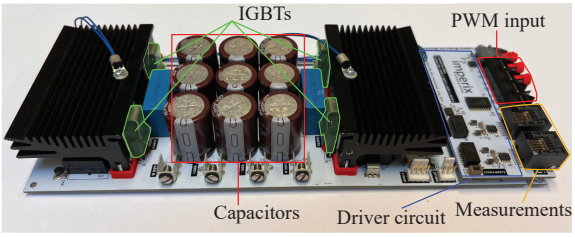
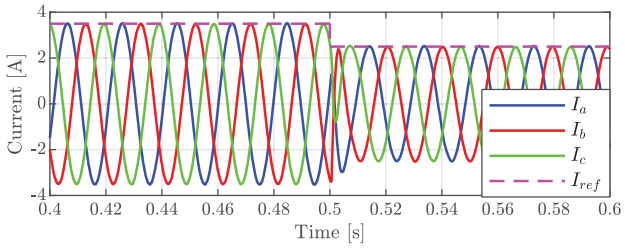


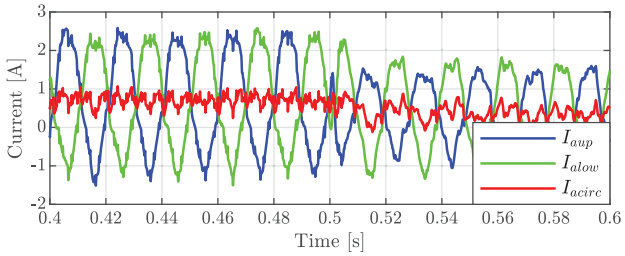
Fig. 10: The IGBT submodule inside the converter cabinet

with a capacitance of 5 mF. The driver circuit, the optical PWM input, and the onboard measurements of the submodule are shown in Fig. 10 as well.

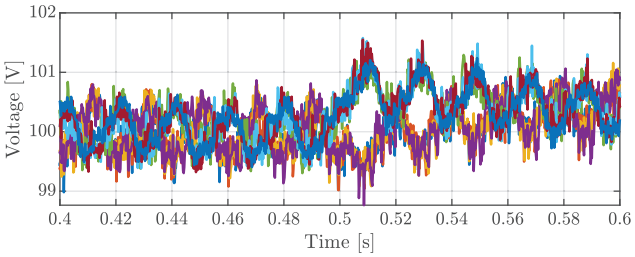
The experimental results are shown in Fig. 11, and a closed-loop current controller is utilized to control the current to follow the reference current.



(a) Three-phase currents and current reference



(b) Phase *a* arm and circulating currents



(c) Phase *a* submodule capacitors voltage

Fig. 11: Experimental results of SVM operation with current step: 3.5 A to −2.5 A

It can be seen that for the current step at $t = 0.5\,\mathrm{s}$, the phase current amplitude can follow its reference value, the circulating currents are minimized, and the submodule capacitor voltages are balanced. This means that the studied generalized SVPWM can be utilized for modulating the MMC.

Conclusion

This paper studies a generalized SVPWM method for modulating the MMC, and in addition to that, the circulating current control and the submodule capacitor voltage balancing of the MMC are included in the study. The simulation and experimental results show the feasibility of using the generalized SVPWM

method for modulating the MMC. However, the waveform qualities of using SVPWM are not perfect due to the distortion of circulating current control signal on the reference modulation signal. On the other hand, this generalized SVPWM shows the flexibility of using discontinuous SVPWM to decrease 28% of the switching loss inside the converter, which can benefit the thermal design of the MMC for the studied application.

References

[1] M. Valavi and A. Nysveen, "Variable-speed operation of hydropower plants: A look at the past, present, and future," *IEEE Industry Applications Magazine*, vol. 24, no. 5, pp. 18–27, 2018.

[2] T. Holzer and A. Muetze, "Full-size converter operation of hydro power generators: A state-of-the-art review of motivations, solutions, and design implications," *e & i Elektrotechnik und Informationstechnik*, vol. 136, no. 2, pp. 209–215, 2019.

[3] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *2003 IEEE Bologna Power Tech Conference Proceedings,*, IEEE, vol. 3, 2003, 6–pp.

[4] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, control, and applications of the modular multilevel converter: A review," *IEEE transactions on power electronics*, vol. 30, no. 1, pp. 37–53, 2014.

[5] Y. Deng, Y. Wang, K. H. Teo, M. Saeedifard, and R. G. Harley, "Optimized control of the modular multilevel converter based on space vector modulation," *IEEE Transactions on Power Electronics*, vol. 33, no. 7, pp. 5697–5711, 2017.

[6] S. Wei, B. Wu, F. Li, and C. Liu, "A general space vector pwm control algorithm for multilevel inverters," in *Eighteenth Annual IEEE Applied Power Electronics Conference and Exposition, 2003. APEC'03.*, IEEE, vol. 1, 2003, pp. 562–568.

[7] Y. Deng, K. H. Teo, C. Duan, T. G. Habetler, and R. G. Harley, "A fast and generalized space vector modulation scheme for multilevel inverters," *IEEE Transactions on Power Electronics*, vol. 29, no. 10, pp. 5204–5217, 2013.

[8] G. Mademlis, "Medium Voltage Generation System with Five-level NPC Converters for Kite Tidal Power," Licentiante Thesis, Chalmers University of Technology, 2019.

[9] B. Wu, M. Narimani, and Knovel, *High-power converters and AC drives*, Second edition., ser. IEEE Press series on power engineering. Hoboken, New Jersey: Wiley : IEEE Press, 2017.

[10] K. Sharifabadi, L. Harnefors, H.-P. Nee, S. Norrga, and R. Teodorescu, *Design, control, and application of modular multilevel converters for HVDC transmission systems*. John Wiley & Sons, 2016.

[11] Q. Tu, Z. Xu, and L. Xu, "Reduced switching-frequency modulation and circulating current suppression for modular multilevel converters," *IEEE Transactions on Power Delivery*, vol. 26, no. 3, pp. 2009–2017, 2011.

[12] M. Hagiwara and H. Akagi, "Control and experiment of pulsewidth-modulated modular multilevel converters," *IEEE transactions on power electronics*, vol. 24, no. 7, pp. 1737–1746, 2009.

[13] F. Deng and Z. Chen, "A control method for voltage balancing in modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 29, no. 1, pp. 66–76, 2013.

[14] K. Ilves, L. Harnefors, S. Norrga, and H.-P. Nee, "Analysis and operation of modular multilevel converters with phase-shifted carrier pwm," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 268–283, 2014.

[15] S. Rohner, S. Bernet, M. Hiller, and R. Sommer, "Modulation, losses, and semiconductor requirements of modular multilevel converters," *IEEE transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2633–2642, 2009.

[16] E. Solas, G. Abad, J. A. Barrena, S. Aurtenetxea, A. Carcar, and L. Zajac, "Modular multilevel converter with different submodule concepts-part i: Capacitor voltage balancing method," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 10, pp. 4525–4535, 2013.