

# Second-Order Sliding Mode Control Strategy With Enhanced DC-link Voltage Stability for PWM Rectifier

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**Abstract--** A PWM rectifier is essential to maintain the DC-bus voltage stable in a power router. However, overshoot or drop of DC-link voltage will be caused by load changing or part power fluctuation. Therefore, a novel variable structure sliding mode control (SMC) strategy based on the super-twisting algorithm (STA) is proposed, improving the rectifier's robustness and fast response capability. The influence of voltage error is fully considered in the design of the DC-link voltage control loop. The DC-link voltage is tracked by using STA, which tremendously suppresses voltage fluctuation. The current inner loop is designed based on the second-order sliding mode (SOSM) algorithm to further accelerate the current grid response. The SMC strategy has a faster voltage and current tracking speed than the traditional PI control. In addition, the stability of DC-link voltage is significantly enhanced. Finally, the OPAL-RT digital experimental platform verifies the proposed control strategy's effectiveness.

**Index Terms**--Sliding mode control, DC-link voltage stability, PWM Rectifier, super-twist algorithm.

## I. INTRODUCTION

The increasing penetration of renewable distributed energy (RDE), such as wind energy and solar energy, in the power grid, may cause fluctuations in the voltage of the power grid, thus affecting the stable operation of the power grid [1]. How to effectively manage different forms of DGS, make full use of it, and reduce the negative impact on the power grid has become an important research direction. A power router was proposed to solve this problem, providing reliable interfaces for different forms of power generation, storage, and consumption equipment through modular topological networks and equipment [2]. Moreover, the power router is the essential equipment of the Energy Internet, which can improve the compatibility and economy of the power grid [3].

As a crucial connection for energy exchange between the power router and the power grid, the PWM rectifier is one of the top pieces of equipment to maintain the stability of the DC-bus voltage of the power router [4]. However, the DC-bus voltage of the power router is easily affected by the switching of different power ports, so voltage

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overshoot or drop often occurs. Thus, the control strategies of DC-link voltage for PWM rectifiers are widely studied.

The most widely used strategy is linear vector control based on the PI regular. However, the PWM rectifier system is nonlinear, and PI control is challenging to suppress DC-link voltage fluctuation under external disturbance [5]. Therefore, a variety of progressive nonlinear controllers are proposed, such as model predictive control [6], adaptive control [7], feedback linearization control [8], and SMC [9]. Among them, the SMC has strong robustness and insensitivity to system parameters transformation, which can resist nonlinear disturbance and achieve a stable tracking effect [10].

However, the chatter problem exists in SMC law due to its inherent characteristics [10]. To suppress the buffeting problem of traditional SMC, an improved saturation function  $sign(s)$  is applied to the SMC [11]. Still, this method has the disadvantage that it cannot converge to the expected value in a finite time. In [12], a second-order sliding mode control strategy based on extended state observer (ESO-SOSM) is proposed to further improve the system robustness and dynamic response of DC-link voltage regulation. However, the above method cannot suppress DC-link voltage fluctuations, and using an observer increases the complexity of the controller.

This article proposes an improved SMC strategy based on the STA, which can suppress DC-link voltage fluctuation better with a fast dynamic response. A controller based on a PWM rectifier system model is designed, which consists of two control loops. For the voltage regulation loop, a composite control method based on voltage deviation function and STA-based SOSM is proposed. Using STA to design the current regulating circuit improves the fast-tracking performance of the current tracking loop. This control structure ensures the fast response ability of DC voltage and the stability of the rectifier.

To highlight the advantages of the proposed control, it is compared with some converter control strategies. Compared with the traditional PI control, the sliding mode control adopted is more robust, and the proposed control strategy can significantly reduce overshoot while ensuring fast tracking. In addition, compared with the [12] control algorithm, the proposed control strategy considers both capacitor voltage's first and second derivatives. The

capacitor voltage fluctuation and recovery time are significantly shortened when the load is switched.

A 20kW three-phase grid-connected converter experimental platform is built to verify the performance of the proposed control. The experimental results show that the proposed control strategy achieves good dynamic response and anti-interference ability under the condition of low total harmonic transmission current, which verifies the effectiveness of the proposed control strategy.

The organization of this paper is as follows. In Section II describes the mathematical model of a three-phase T-type PWM rectifier is described. The proposed control method is designed in Section III. Experimental results comparing the performance of the proposed control strategy with traditional PI and ESO-SOSM in Section IV. Finally, conclusions are drawn in Section V.

## II. MODE OF T-TYPE PWM RECTIFIER

To improve the quality of the output current of the power router, the three-phase three-level T-type grid-connected converter with smaller current harmonics is used as the grid-connected port [13]. A simple three-level T-type PWM rectifier topology is shown in Fig.1. The PWM rectifier is connected to the grid by an inductor  $L$  with a parasitic resistance  $r$ , and the DC capacitor  $C$  is made up of and in series, and a resistive load is connected to the DC capacitor, and the change of the load is regarded as an external disturbance. Assuming the three-phase voltage balance of the power grid, the system model in the synchronous rotating coordinate system through Park transformation is

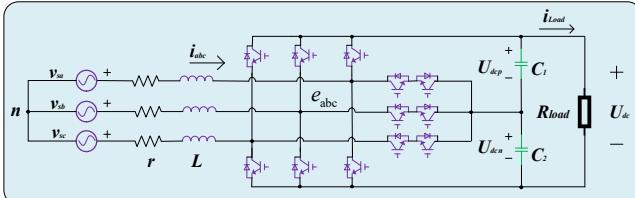


Fig. 1. T-type PWM rectifier circuit.

$$\begin{cases} L \frac{di_d}{dt} = -ri_d + \omega Li_q + v_d - S_d U_{dc} \\ L \frac{di_q}{dt} = -ri_q - \omega Li_d + v_q - S_q U_{dc} \\ C \frac{dU_{dc}}{dt} = (S_d i_d + S_q i_q) - i_{Load} \end{cases} \quad (1)$$

where  $S_d$  and  $S_q$  are the switching function,  $i_d$  and  $i_q$  are the input current,  $v_d$  and  $v_q$  are the grid side input voltage,  $U_{dc}$  is the DC-link voltage of the rectifier,  $i_{Load}$  is the load current,  $\omega$  is the grid angular frequency.

To ensure the reliable operation of the power router, the main control objectives of the three-phase three-level T-type grid-connected converter are as follows.

Firstly, the DC bus voltage is controlled so that it can quickly track the voltage reference command  $U_{dcref}$  sent by the power router, and has certain anti-interference ability and the ability to quickly recover to the command voltage when the load suddenly changes:

$$U_{dc} \rightarrow U_{dcref} . \quad (2)$$

Secondly, in order to achieve unit power factor output,

the reference value should be set to zero in the synchronous rotating coordinate system:

$$i_q \rightarrow i_{qref} = 0 . \quad (3)$$

## III. DESIGN OF CONTROLLER

The power router requires that the PWM rectifier realize stable control of the bus voltage. When the load is within the allowable power range or the power generation equipment is connected to the bus through the port converter, the DC-link voltage ripple range should be as small as possible. In addition, considering that the power router needs to control the operation of multiple converters simultaneously, it has higher requirements for the response speed of the rectifier. Therefore, it is also essential that the PWM rectifier can reach the steady-state operating point as soon as possible when the bus voltage fluctuates.

To achieve the above objectives, the controller of the PWM rectifier is designed by a voltage control loop applying STA strategy and a current tracking loop based on STA in series. First, introduce the primary content of STA, then submit the voltage control and current controller designed with STA.

### A. STA control strategy

Considering a nonlinear representation as [14].

$$\dot{x} = A(t, x) + B(t, x)u \quad (4)$$

where  $A(x)$  represents the  $n \times n$  order system state matrix,  $B(x)$  is the system input matrix,  $x$  is the state of the system,  $t$  is the time and  $u$  is the system input. When there is only one input variable,  $B(x)$  is a vector  $n \times 1$  of one.

When the system input  $u$  is bounded,  $|u| < U_M$ , assume that the system meets the following conditions

$$\begin{cases} |\dot{A}| + U_M |\dot{B}| \leq Q \\ 0 \leq K_m \leq B(t, x) \leq K_M \\ \left| \frac{A}{B} \right| < q U_M \end{cases} \quad (5)$$

where  $Q$ ,  $K_m$ ,  $K_M$ ,  $U_M$ ,  $q$  are all positive constants.

The control law of STA can be defined as

$$\begin{cases} u = -\lambda \sqrt{|x|} \operatorname{sgn}(x) + u_1 \\ \dot{u}_1 = \begin{cases} -u, |u| > U_M \\ -\alpha \operatorname{sign}(x), |u| \leq U_M \end{cases} \end{cases} . \quad (6)$$

From formula (6), we can see that the control law of STA is continuous, and the control law is smoother output, so it can reduce chattering. Compared with traditional SMC, the chattering of STA is smaller, which is more conducive to the control of power electronic devices.

To ensure that the control law (6) can ensure that the system (4) converges in a finite time, that is, the control law  $u$  can enter in a limited time and remain in this interval. If the initial state,  $u$  is in the above range, and it will always move in this range. For this reason, the parameters and requirements of the control law are large enough, and the following restrictions are made.

$$\begin{cases} \alpha > \frac{Q}{K_m} \\ \lambda > \sqrt{\frac{2}{(K_m \alpha - Q)} \frac{(K_m \alpha + Q) K_M (1+q)}{K_m^2 (1-q)}} \end{cases} . \quad (7)$$

### B. Voltage Regulator Loop

The control target of DC-link voltage is to quickly eliminate the error by adjusting the output reference current according to command  $U_{dcref}$  and can stabilize the DC bus voltage fluctuation when the load changes.

Based on formula (1), we can obtain the first and second voltage derivatives on the PWM rectifier's DC-link as formula (8).

The function of the voltage regulating circuit is to continuously adjust the controller output  $i_{dref}$ , fast tracking of upper reference voltage  $U_{dcref}$ . To achieve the above objectives, we define  $e_{dc} = U_{dcref} - U_{dc}$ , establish error feedback sliding surface  $s_{dc} = e_{dc}$ , then

$$\dot{s}_{dc} = \dot{U}_{dcref} + \frac{i_{Load} - s_d i_d - s_q i_q}{c}. \quad (9)$$

Establish relevant error function (10) of  $s_{dc}$ , where  $\zeta$  is the correlation constant of the first derivative of  $s_{dc}$ .

In steady state, when the capacitor voltage tracks the given value  $U_{dcref}$  then  $E(s_{dc}) = 0$ .

In formula (8),  $i_d$  is the reference value of the current control circuit, but is affected by the control quantities  $S_d$  and  $S_q$ . Therefore, it is necessary to eliminate  $S_d$  and  $S_q$  through the following derivation.

According to formula (1)(3), when the output voltage is stable, the current tends to be stable,  $i_d = i_q \rightarrow 0$ , Rectifier works at unit power factor,  $i_q = 0$ , and the switching loss of the converter can be ignored, we can get

$$S_q = -\frac{\omega L i_d}{U_{dc}}, \quad (11)$$

$$S_d = \frac{v_d - r i_d}{U_{dc}} \approx \frac{V_m - r i_d}{U_{dc}} \quad (12)$$

where  $V_m$  is the peak value of phase voltage (under the equivalent rotation Park transformation).

Substituting (11) and (12) into (10) yield gets (13).

It can be found that  $U_{dcref} - U_{dc}$  can be regarded as a proportional error adjustment item with a proportional coefficient of 1, and the above formula can be simplified as follows:

$$i_{dref} = (s_{dc} + \frac{\zeta i_{Load}}{c}) \frac{c U_{dc}}{\zeta (V_m - r i_d)}. \quad (14)$$

To improve the anti-disturbance capability, a new capacitor voltage control equation is obtained by adding STA.

$$i_{dref} = (u_{dc}(s_{dc}) + \frac{\zeta i_{Load}}{c}) \frac{c U_{dc}}{\zeta (V_m - r i_d)} \quad (15)$$

in which  $u_{dc}(s_{dc})$  is the STA that takes its expression is as follows.

$$\begin{cases} u_{dc}(s_{dc}) = u_{dc1} + \lambda_{dc} \sqrt{|s_{dc}|} \operatorname{sgn}(s_{dc}) \\ \dot{u}_{dc1} = \begin{cases} u_{dc}, & |u_{dc}| > U_M \\ \alpha_{dc} \operatorname{sign}(s_{dc}), & |u_{dc}| \leq U_M \end{cases} \end{cases} \quad (16)$$

where  $\lambda_{dc}$  and  $\alpha_{dc}$  are constants and conform to the restrictions of formula (7).

$$\frac{d}{dt} \left[ \frac{U_{dc}}{U_{dc}} \right] = \left[ -\frac{r}{L} \dot{U}_{dc} - \frac{s_d^2 + s_q^2}{LC} U_{dc} - \frac{ri_{Load}}{LC} - \frac{di_{Load}}{C dt} + \frac{\omega (s_d i_q - s_q i_d)}{c} + \frac{s_d U_d + s_q U_q}{LC} \right]. \quad (8)$$

$$E(s_{dc}) = s_{dc} + \zeta \dot{s}_{dc} = U_{dcref} - U_{dc} + \zeta \left( \dot{U}_{dcref} + \frac{i_{Load} - s_d i_d - s_q i_q}{c} \right). \quad (10)$$

$$i_{dref} = \left[ U_{dcref} - U_{dc} + \zeta \dot{U}_{dcref} + \frac{\zeta (i_{Load} - s_q i_q)}{c} \right] \frac{c U_{dc}}{\zeta (V_m - r i_d)}. \quad (13)$$

The proposed improved voltage regulation circuit block diagram is shown in Fig. 2.

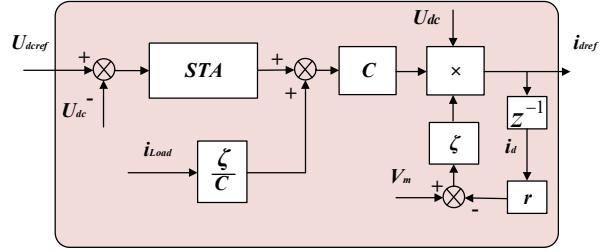


Fig. 2. Block diagram of the voltage tracking regulation loop.

### C. Current Regulator Loop

The purpose of the current regulation loop is to regulate the output  $S_d$  and  $S_q$  to track  $i_{dref}$  and  $i_{qref}$ .  $i_{dref}$  is calculated from the voltage loop.

The sliding variable of current control is defined as  $s_d = i_{dref} - i_d$ ; and  $s_q = i_{qref} - i_q$ .

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Find the first derivative

$$\begin{bmatrix} \dot{s}_d \\ \dot{s}_q \end{bmatrix} = \begin{bmatrix} i_{dref} + \frac{1}{L} (r i_d - v_d) - \omega i_q \\ i_{qref} + \frac{1}{L} (r i_q - v_q) + \omega i_d \end{bmatrix} + \frac{U_{dc}}{L} \begin{bmatrix} S_d \\ S_q \end{bmatrix}. \quad (17)$$

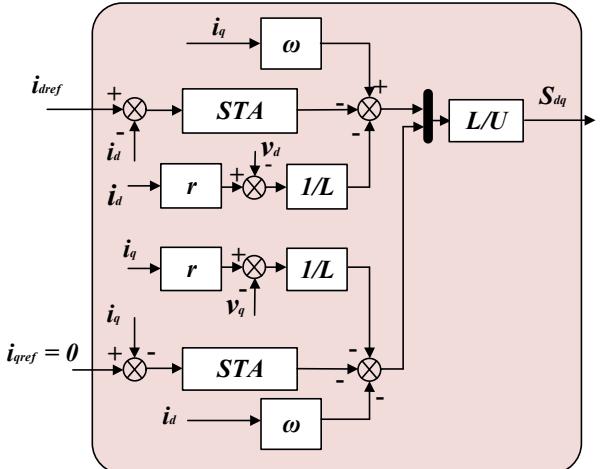


Fig. 3. Block diagram of the current tracking regulation loop.

According to the above formula (17), the output of current loop can be expressed as

$$\begin{cases} S_d = \frac{L}{U_{dc}} \left[ -u_d(s_d) - i_{dref} - \frac{1}{L} (r i_d - v_d) + \omega i_q \right] \\ S_q = \frac{L}{U_{dc}} \left[ -u_q(s_q) - i_{qref} - \frac{1}{L} (r i_q - v_q) - \omega i_d \right] \end{cases}. \quad (18)$$

The adjustment of the voltage loop is relatively slow compared with the current loop, so the change in the current reference value can be ignored, namely  $\dot{s}_d = \dot{s}_q = 0$ . Therefore, the above formula (18) can be simplified as

$$\begin{aligned} & \frac{(S_d i_d + S_q i_q) - i_{Load}}{c} \\ & \frac{ri_{Load}}{LC} - \frac{di_{Load}}{C dt} + \frac{\omega (s_d i_q - s_q i_d)}{c} + \frac{s_d U_d + s_q U_q}{LC} \end{aligned} \quad (8)$$

$$E(s_{dc}) = s_{dc} + \zeta \dot{s}_{dc} = U_{dcref} - U_{dc} + \zeta \left( \dot{U}_{dcref} + \frac{i_{Load} - s_d i_d - s_q i_q}{c} \right). \quad (10)$$

$$i_{dref} = \left[ U_{dcref} - U_{dc} + \zeta \dot{U}_{dcref} + \frac{\zeta (i_{Load} - s_q i_q)}{c} \right] \frac{c U_{dc}}{\zeta (V_m - r i_d)}. \quad (13)$$

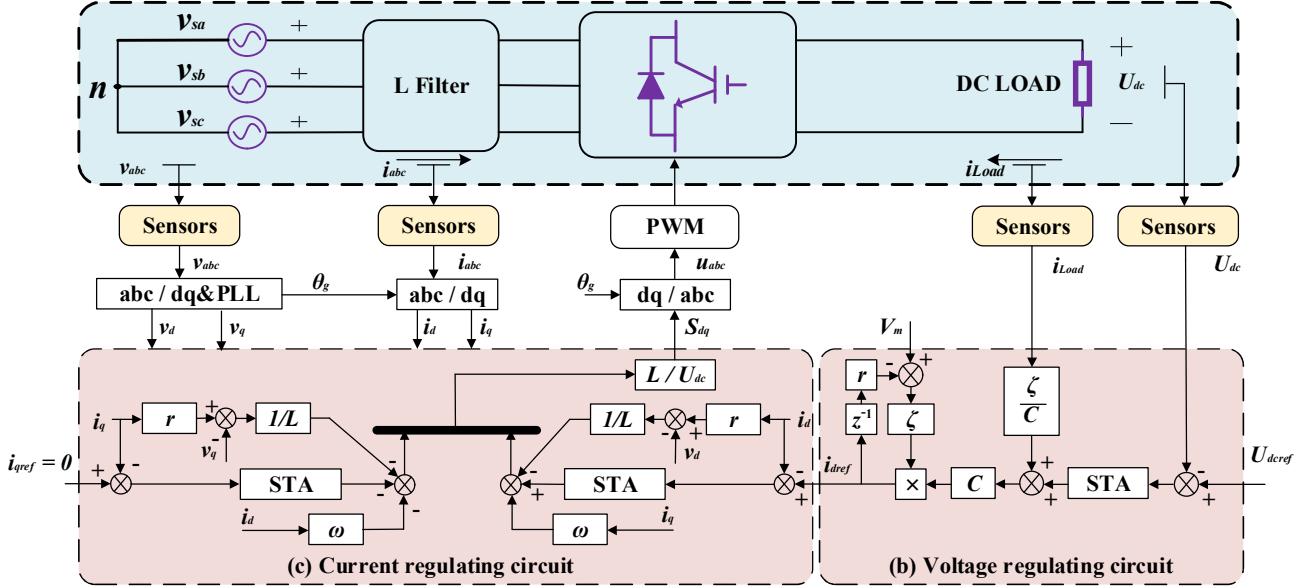


Fig. 4. Control structure of the proposed strategy.

$$\begin{cases} S_d = \frac{L}{U_{dc}} \left[ -u_d(s_d) - \frac{1}{L}(ri_d - v_d) + \omega i_q \right] \\ S_q = \frac{L}{U_{dc}} \left[ -u_q(s_q) - \frac{1}{L}(ri_q - v_q) - \omega i_d \right] \end{cases} \quad (19)$$

where  $u_{dc}(s_{dc})$  is the STA strategy that takes the following form

$$u_d(s_d) = u_{d1} + \lambda_d \sqrt{|s_d|} \operatorname{sgn}(s_d), \\ u_d = \begin{cases} u_d, & |u_d| > U_M \\ \alpha_d \operatorname{sign}(s_d), & |u_d| \leq U_M \end{cases} \\ u_q(s_q) = u_{q1} + \lambda_q \sqrt{|s_q|} \operatorname{sgn}(s_q), \\ u_q = \begin{cases} u_q, & |u_q| > U_M \\ \alpha_q \operatorname{sign}(s_q), & |u_q| \leq U_M \end{cases} \quad (20)$$

$\lambda_d$ ,  $\alpha_d$ ,  $\lambda_q$  and  $\alpha_q$  are positive constants that can be designed according to the formula (7).

The current regulation circuit diagram used is shown in Fig. 3.

TABLE I  
SYSTEM PARAMETERS OF PWM RECTIFIER

Key Parameter	Value
Grid frequency $f$	50Hz
Grid RMS voltage $v_{abc}$	110 V
DC link capacitor $C_1, C_2$	7650 $\mu\text{F}$
Filter inductor $L$	230 $\mu\text{H}$
Sampling frequency $f_s$	10 kHz
Switching frequency $f_{sw}$	10 kHz
Output Voltage $U_{dc}$	400V

Fig. 4 is a complete control block diagram, including the main circuit, voltage and current detection module, phase-locked loop, voltage and voltage control loop based on STA, and current tracking loop based on STA.

#### IV. EXPERIMENTAL VERIFICATION

In this section, a time-domain digital platform of a 20kW PWM rectifier is built on the OPAL-RTLAB real-time digital experimental platform to verify the effectiveness of the proposed control scheme. The main

parameters of the primary circuit are shown in Table I. Fig. 4 shows the overall structure of the PWM rectifier.

TABLE II  
CONTROLLER DESIGN PARAMETERS

Control Strategy	Key Parameter	Value
PI	Voltage regulation loop ( $k_p, k_i$ )	1, 50
	Current regulation loop ( $k_{pd}, k_{pg}, k_{id}, k_{iq}$ )	40, 10, 40, 10
ESO-SOSM	Voltage regulation loop ( $\lambda_{dc}, \alpha_{dc}, \beta_1, \beta_2$ )	60, 100000, 5, 80
	Current tracking loop ( $\lambda_d, \alpha_d, \lambda_q, \alpha_q$ )	8000, 60000, 8000, 60000
STA	Voltage regulation loop ( $\lambda_{dc}, \alpha_{dc}, \zeta$ )	1000, 30000, 3
	Current tracking loop ( $\lambda_d, \alpha_d, \lambda_q, \alpha_q$ )	8000, 60000, 8000, 60000

Since PI is a widely used control method, we chose a linear conventional PI regulator with a well-tuned parameter as the standard control group. In addition, a better sliding mode ESO-SOSM was selected as the control group for the SMC strategy. Three groups of experiments were carried out. The first group of experiments tests the response of different control strategies to the change of filter inductance parameters, aiming to test the proposed method's robustness. The second is to test the ability of different ways to suppress bus voltage fluctuations, which is used to test the anti-interference performance of the proposed strategy. Thirdly, the dynamic response speed of the control algorithm is verified through the no-load start test. The main parameters of PI, ESO-SOSM and the proposed control method STA are shown in Table II.

#### A. Improved PWM Rectifier Stability

Fig. 5 shows the state change of bus voltage when the PWM rectifier works at 10kW and outputs 400V stable voltage, and the inductance at the rectifier network side changes suddenly from 1mH to 2mH. Fig. 5(a) shows the experimental results using a PI controller. The result of using the ESO-SOSM controller is shown in Fig. 5(b).

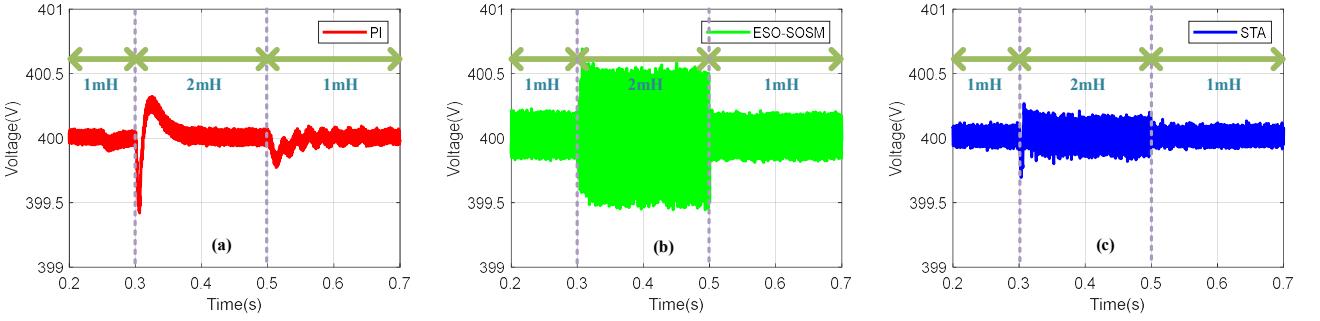


Fig. 5. Dynamic response of bus voltage when filter inductance changes.

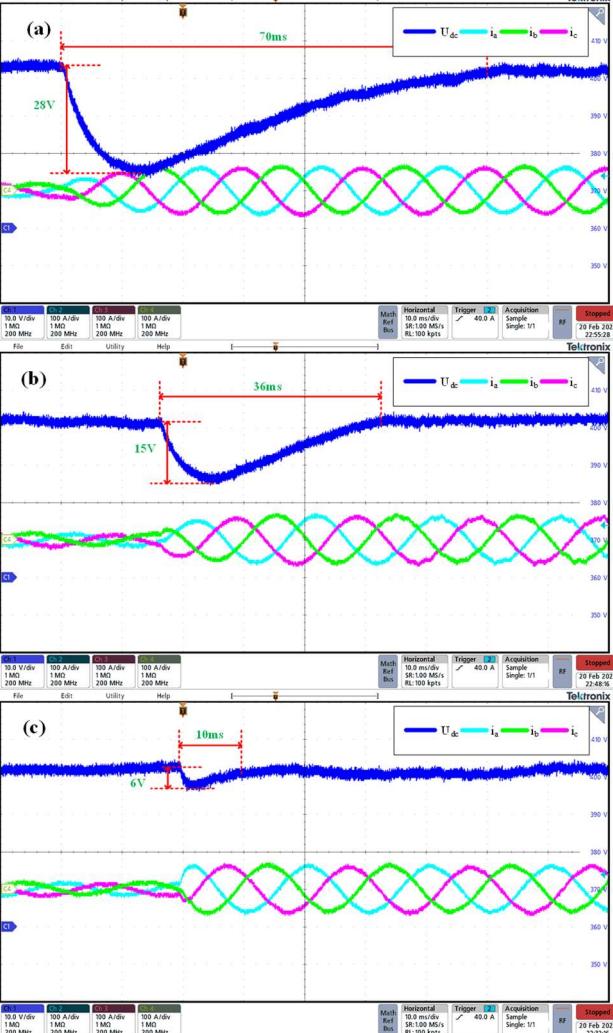
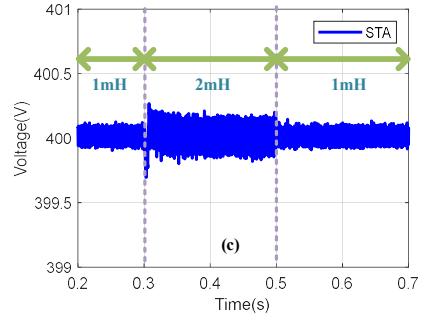


Fig. 6. Transient response of DC-link voltage under 10kW load switching: (a) PI algorithm, (b) ESO-SOSM strategy, and (c) Proposed STA control strategy.

Fig. 5(c) shows the experimental results using the control algorithm proposed in this paper.

Both controllers can overcome the influence of the change of the rectifier network side inductance on the bus fluctuation within a certain range and maintain the bus voltage stability. From the experimental results, it can be seen that the fluctuation amplitude of STA is smaller at the moment of inductance change, which shows that its robustness to suppress the change of converter parameters is better than the traditional PI. However, in a steady state, due to the chattering problem inherent in sliding mode, its



high-frequency voltage fluctuation range is slightly worse than that of traditional PI, but it is still within the acceptable range.

### B. Improved DC-link voltage Stability

Fig. 6 shows the transient response of the DC-link voltage for a load step from a load with 5kW to a load composed of a resistor of  $16\Omega$ . Fig. 6(a) shows the experimental results using the PI controller. The result of using the ESO-SOSM controller is shown in Fig. 6(b). Fig 6(c) shows the experimental results using the control algorithm proposed in this paper.

From the experimental results, the three control strategies have good control effect and can make the bus voltage recover to the given value in a limited time. The experimental results show that the proposed control method can recover to the steady-state value with a response time of fewer than 0.01 s. At the same time, compared with the PI and ESO-SOSM, the voltage drop of the proposed control method is only 6V, which is 21.4% of that of the PI method and 40% of that of the ESO-SOSM method.

### C. Improved DC-link voltage Response Speed

Fig. 7 shows that when the initial DC bus voltage is 0, the DC bus is no-load, the rectifier is directly started, and the voltage directly rises to the normal working voltage of the power router 400V. Fig. 7(a) shows the experimental results using the PI controller. The result of using the ESO-SOSM controller is shown in Fig. 7(b). Fig. 7(c) shows the experimental results using the control algorithm proposed in this paper.

The three control strategies can quickly establish the bus voltage. The main difference is that the overshoot and the time to reach the given voltage are different. It can be seen that the DC-link voltage overshoot under the proposed control strategy is only 5V, lower than the PI control and ESO-SOSM control strategies. In addition, the time for DC-link voltage to reach the reference value is also the fastest, only 20ms.

Based on the above experimental results, it can be seen that the proposed STA-based control strategy has obvious advantages over the traditional PI control in terms of fast response capability, voltage tracking capability, and resistance to DC-link voltage fluctuation, and further improves the anti-disturbance capability compared with ESO-SOSM, which verifies the effectiveness of the proposed control strategy.

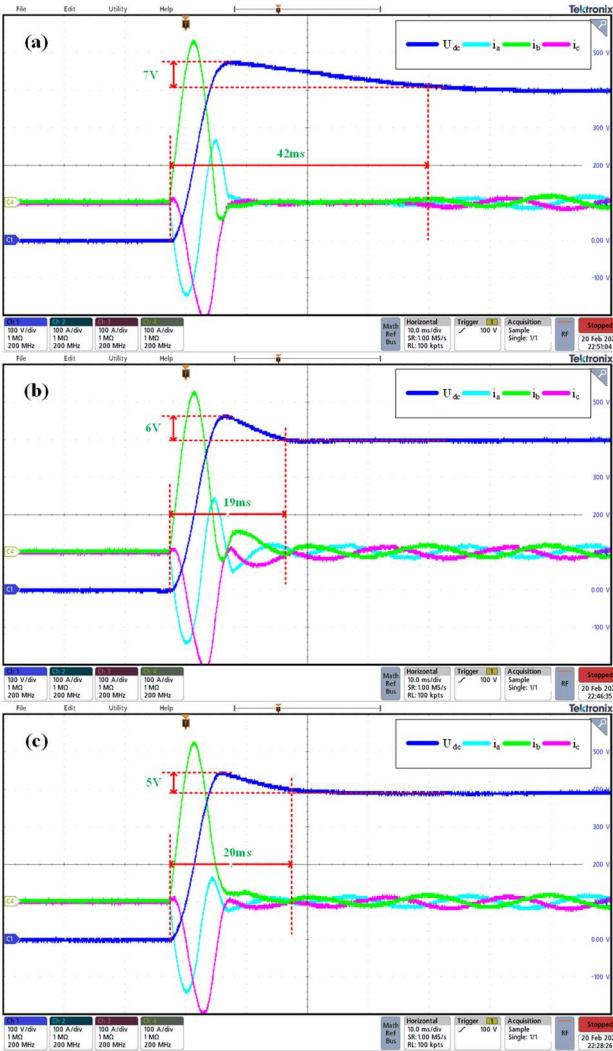


Fig. 7. Transient response of a DC-link capacitor voltage under no load startup: (a) PI algorithm, (b) ESO-SOSM strategy, and (c) Proposed STA control strategy.

## V. CONCLUSIONS

To improve the stability of the DC-link voltage of a PWM rectifier in a power router, based on the mathematical model of a PWM rectifier, a fast response regulation method of DC-link voltage was proposed. Compared with the conventional voltage deviation control, the DC-link voltage control method adopted in this paper considers the current load term, which can significantly improve the fast response capability of the PWM rectifier. At the same time, combined with the STA control strategy, the PWM rectifier dynamic performance was further enhanced, and the DC-link voltage fluctuation was suppressed. Finally, through experiments on OPAL-RT digital experimental platform, the proposed control strategy can quickly respond to load changes and maintain the capacitor voltage stability, proving that the control strategy had good control performance.

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