Design Considerations for Fast On-State Voltage Measurement Circuits

Mathias C. J. Weiser, Manuel Rueß and Ingmar Kallfass
University of Stuttgart, Institute of Robust Power Semiconductor Systems
Pfaffenwaldring 47
Stuttgart, Germany
Phone: +49 (0) 711-685-61704
Fax: +49 (0) 711-685-58700
Email: mathias.weiser@ilh.uni-stuttgart.de
URL: https://www.ilh.uni-stuttgart.de

Acknowledgments

This work has received funding by the German Science Foundation in the frame of the project 440549658, grant number KA 3062/18-1.

Keywords

≪Component for measurements≫, ≪Device characterization≫, ≪Voltage sensor≫, ≪Wide bandgap devices≫, ≪Design optimization≫

Abstract

The recovery time of on-state voltage measurement circuits (OVMCs) is a critical, yet often overlooked aspect of the proper switching characterization of power semiconductor devices. In this work, we aim to provide a deeper understanding of the problem and propose ways to enhance the dynamic performance.

Introduction

Gallium nitride high electron mobility transistors (GaN-HEMTs) are promising devices for power systems with extremely large power density due to their ability to enable power handling at switching frequencies above 1 MHz [1]. Unfortunately, these devices feature parasitic effects like the 'dynamic on-state resistance' or 'current collapse', which describes a momentary increase of the drain-to-source resistance (R_{DS}) in on-state after a high-voltage blocking state [2, 3, 4]. The characterization of this effect is challenging: while the off-state V_{DS} can reach more than 500 V for high voltage devices, the on-state V_{DS} can drop significantly below 1 V, depending on the device and the operating point. While measuring V_{DS} with an oscilloscope, the measurement accuracy is determined by the vertical resolution. E.g., for a measurement with an oscilloscope operating at a $\pm$ 400 V measurement range and an effective 10-bit resolution (ENOB), the least significant bit represents a voltage of $V_{\mathrm{lsb}} = \frac{800\,\mathrm{V}}{2^{10}} \approx 0.78\,\mathrm{V}$.

As this measurement resolution is insufficient to accurately characterize the switching behavior, OVMCs are employed. The aim of these circuits is to limit the maximum output voltage to confine the limited vertical resolution of the oscilloscope to the range of interest. While operating below the clipping voltage V_{clip}, which denotes the maximum observable voltage at the OVMC output, the OVMC should allow an accurate measurement of V_{DS} while limiting the maximum output voltage V_{out} for higher voltages. Furthermore, the transition between both states should be as quick as possible.

Fig. 1 shows a simplified schematic of a commonly used OVMC operating principle [5, 6, 7, 8]. This kind of OVMC consists of a silicon carbide (SiC) Schottky diode, a clipping diode and a current source. For a large V_{in}, the SiC diode D_{in} blocks the incoming voltage and the current flows through the clamping

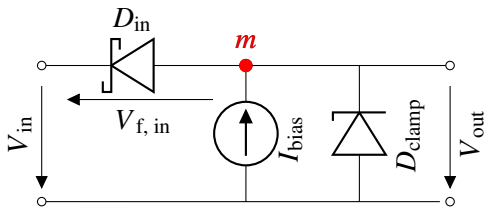

Fig. 1: Basic schematic of a diode-based OVMC.

diode D_{clamp}. V_{out} is therefore limited to the voltage drop over the clipping branch. For low input voltages, i.e., when the device is in on-state, the current flows through the power diode into the DUT drain terminal. With the assumption that the forward voltage of the power diode $V_{\text{f,in}}$ stays constant throughout the measurement, V_{DS} can be reconstructed as $V_{\text{DS,on}} = V_{\text{in}} = V_{\text{out}} - V_{\text{f, in}}$.

Diode-based OVMCs are frequently used for the characterization of the dynamic on-state resistance of GaN-HEMTs, as SiC Schottky diodes features smaller capacitances than alternative technologies, which use, e.g., HV-capable FETs instead of the diode to accomplish the HV-lockout [11, 12]. The limitations of the circuit shown in Fig. 1 are the measurement offset caused by the Schotty diode forward drop, and the temperature dependency of this parameter, which aggravates the characterization at varying temperatures. Both of these drawbacks have been addressed with the usage of subtraction networks made from operational amplifiers (OpAmps) [9, 10].

The measurement node m highlighted in Fig. 1 is the most critical node in this setup. The quicker it can follow the input voltage, the faster the acquisition of $V_{\text{DS,on}}$. Even though SiC Diodes feature capacitances significantly smaller than 100 pF, at several hundreds of V of reverse voltage, a charge of several nC can form on the device. During the turn-on transition of the DUT, this charge has to be fully neutralized to change the diode operation from blocking state to forward bias, plus the time needed to shift the measurement node to the potential which corresponds to the correct V_{DS}, before any accurate measurements of V_{DS} can take place. In this context, we define the recovery time of the OVMC as the time needed to neutralize the charge on the SiC diode and allow the internal voltage node to return to zero-bias conditions. After this, in order to correctly measure V_{DS}, V_{out} has to increase further until steady state has been reached.

Measurement Setup

Measurements were carried out using a half bridge, which consists of two 650 V, 15 A e-mode GaN-HEMTs and an isolated driver circuit. The half bridge can be used as-is, or a load inductor can be added between the supply voltage and the switch node to form a double pulse test (DPT) setup. During the design optimization phase, a 100 µH wirewound air-core inductor was used for this purpose. The coil current was measured at the wire exiting the coil using a 30 A, 100 MHz current clamp. The rise- and fall-times of the half bridge are set to approx. 10 ns to allow for smooth transitions between the states and avoid switching noise. The switching behavior of the DPT setup is shown in Fig. 2. The OVMC is connected to the switch node and the output side ground, measuring the low-side device.

The proposed OVMC is based on the approach shown in Fig. 1. The bias current is generated via a PNP-type current mirror. With a single resistor, the bias current can be altered. The circuit is setup to support variations of recovery acceleration branches and clipping branches to explore the impact of several design parameters on the reaction time.

Both circuits are shown in Fig. 3. For all double-pulse experiments, the evaluation of the proposed OVMC takes place during the second pulse. The static transfer behavior of the OVMC was captured with a parametric 3 kV/50 A curve tracer. It is shown in Fig. 4.

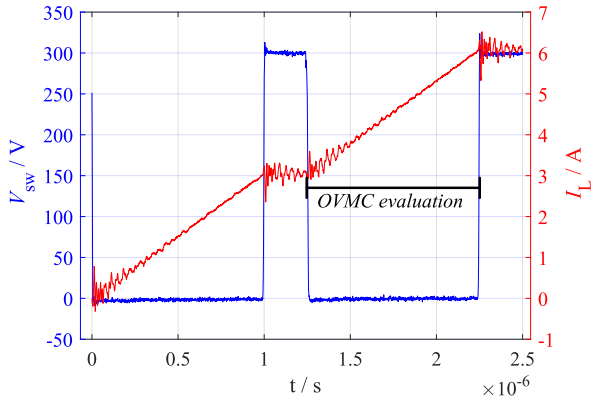

Fig. 2: Current- and voltage waveforms of the DPT.

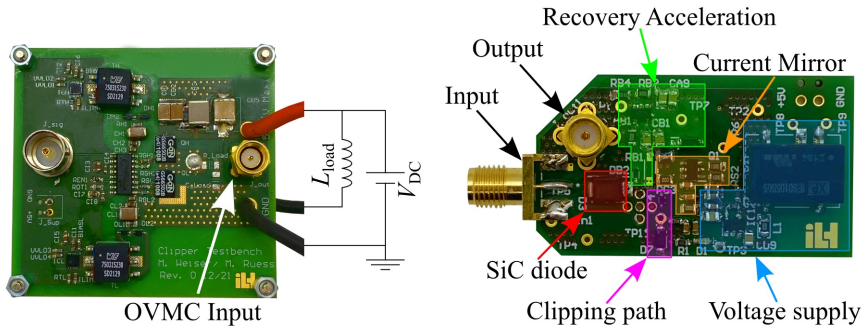

Fig. 3: Physical layout of the test PCB (left) and the proposed OVMC (right).

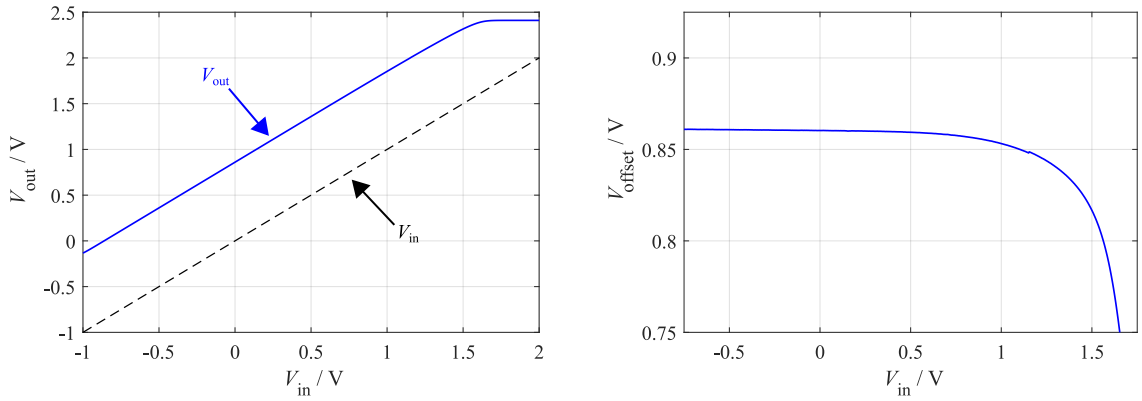

Fig. 4: Static transfer behavior (left) and output offset (right) of the proposed OVMC.

Characteristics of the Stored Charge

To highlight the implication of the stored charge, the OVMC is used as shown, with no additional way to neutralize the stored charge apart from the source current I_{bias}. The half bridge is used without load and the DC voltage is set to 300 V. The bias resistors of the OVMC are set to 3.3 kΩ, 620 Ω and 120 Ω, which corresponds to $I_{\text{bias},1} = 1\,\text{mA}$, $I_{\text{bias},2} = 5\,\text{mA}$ and $I_{\text{bias},3} = 25\,\text{mA}$, respectively. At this voltage, the data sheet value of the stored charge is listed as $Q_{\text{j}} \approx 2.5\,\text{nC}$. For a first approximation, the expected recovery time t_{rec} can be calculated as Eq. 1.

$$t_{\text{rec, n}} = \frac{\Delta Q_{\text{j}}}{I_{\text{bias, n}}} \quad \Rightarrow \quad t_{\text{rec},1} = 2.5\,\mu\text{s}; \quad t_{\text{rec},2} = 500\,\text{ns}; \quad t_{\text{rec},3} = 100\,\text{ns} \tag{1}$$

The output voltage transients of the OVMC after the switching event are shown in Fig. 5.

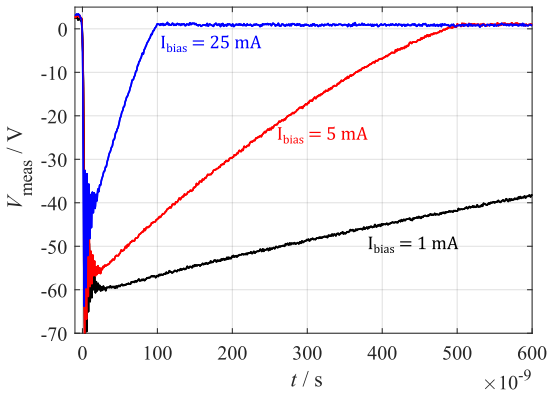

Fig. 5: Recovery time of the OVMC for different bias currents.

Immediately after the switching event, the charge on the parasitic diode capacitance ΔQ_j pulls the internal measurement node to almost $-70\,\mathrm{V}$, after which the stored charge is depleted by I_bias. Higher currents deplete the charge faster, but the negative voltage spike is almost identical in all three cases. Even with a current of 25 mA, the recovery time of the circuit is approx. 100 ns. However, it has to be noted that larger currents also mean an increasing influence of the OVMC on the measurement setup, as I_bias represents an additional current that flows through the DUT, which might not be desired and can alter the calculated resistance of the DUT if not taken into account. Therefore, I_bias cannot be increased indefinitely. It also has to be noted that the observed recovery times are in very good agreement with the estimated ones, which suggests that the observed reaction time of the OVMC is exclusively due to the stored charge.

Variation of the Proposed OVMC

To optimize the reaction time of the circuit, parts of the circuit have been altered and the effect of the changes was evaluated at the second pulse of the DPT. The variations made in this work comprise the clipping branch and a recovery acceleration branch, which are connected between the measurement node and ground. The bias current in the following experiments was set to $I_\mathrm{bias,2} = 5\,\mathrm{mA}$.

Recovery Acceleration

The most straightforward way to accelerate the charge neutralization is by using fast-switching Schottky diodes, which create a conducting path to ground once the voltage at the measurement node decreases below 0 V. Fundamentally, this equals a negative voltage limitation of the output voltage to $V_\mathrm{out,min} = -V_\mathrm{f,Schottky}$. Schottky diodes of varying sizes and blocking voltages are widely available. As for any other semiconductor device, larger maximum currents inevitably lead to larger device dimensions, and thus, larger device capacitances, which in turn slow the device down. As the goal is to supply as much charge in as short of a time as possible, these two properties need to be balanced in order to reach maximum performance. For this reason, the impact of four Schottky diodes as recovery acceleration devices is compared. During this experiment, the fastest variant of the clamping branch has been used to focus on the impact of the recovery diodes. The key parameters of the diodes are listed in Tab. I. The results of the four diodes to the reaction time of the circuit are shown in Fig. 6.

D_1 and D_4 lead to slow reaction behavior, probably due to the low current carrying capability of D_1 and the large capacitance of D_4. D_2 and D_3, however, lead to similarly favorable results, reducing the reaction time to roughly 80 ns. This shows that the choice of the diode has a significant impact on the reaction time and a medium-sized diode offers the best trade-off between capacitance contribution and current carrying capability.

In order to reduce the reaction time even further, the minimum measured voltage can be confined even more to the desired use-case by connecting the anode of the recovery diode to a set potential instead

Table I: Data sheet values of the used diodes at $T = 25\,°\mathrm{C}$.

	C_D at $V_\mathrm{D} = 0\,\mathrm{V}$ (pF)	I_D at $V_\mathrm{D} = 0.5\,\mathrm{V}$ (mA)	$V_\mathrm{rm,max}$ (V)
D_1	3.0	1.6	70
D_2	18	15	40
D_3	37	200	40
D_4	250	3000	30

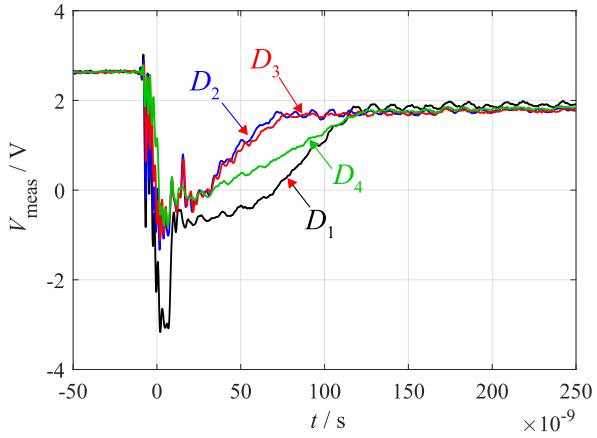

Fig. 6: Reaction behavior of the OVMC with the four diodes.

of ground. A voltage follower can then be used to create the desired offset, and high-frequency buffer capacitors can be used to store the recovery charge. The resulting schematic is shown in Fig. 7. D_2 is used in both cases as diode. In Fig. 8, the results on the reaction behavior are shown.

Clipping Branch Considerations

In order to achieve a voltage limitation at the output, a voltage clipping branch has to be established. In this branch, a highly nonlinear device like a diode is used, which shorts the voltage at the measurement node if above a certain voltage level. Z-diodes are often used for this purpose, as the clipping voltage can be accurately set by selecting a Z-diode with the desired breakdown voltage V_Z. However, Z-diodes usually feature comparably large capacitances, making them rather unsuitable picks for fast-switching circuits. One approach, which has been used in the past to reduce the overall capacitance, is to connect a fast-switching Schottky diode in series to minimize the total capacitance contribution.

A third approach for voltage clipping is to use a separate, independently powered branch. The Z-diode is constantly biased in reverse conduction operation. The measurement node is connected to the anode of the Z-diode by a Schottky diode, which redirects I_bias if the measurement voltage exceeds V_Z. Therefore, the capacitance contribution of the clipping branch is minimized: Schottky diodes feature significantly smaller capacitances and the Z-diode is constantly operated in reverse operation, minimizing its capac-

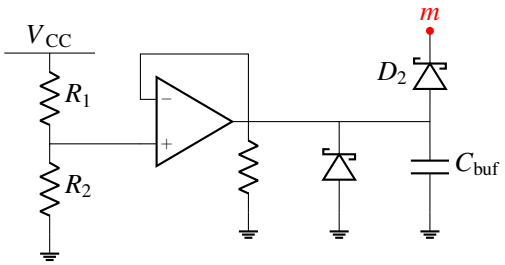

Fig. 7: Topology of the voltage follower recovery acceleration circuit.

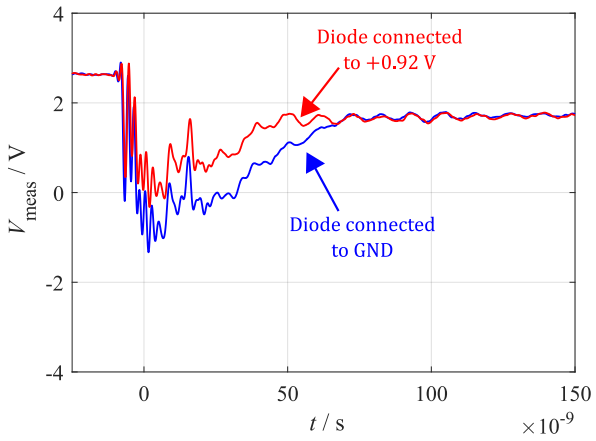

Fig. 8: Reaction behavior of the voltage follower recovery acceleration circuit vs. the GND-connected diode approach.

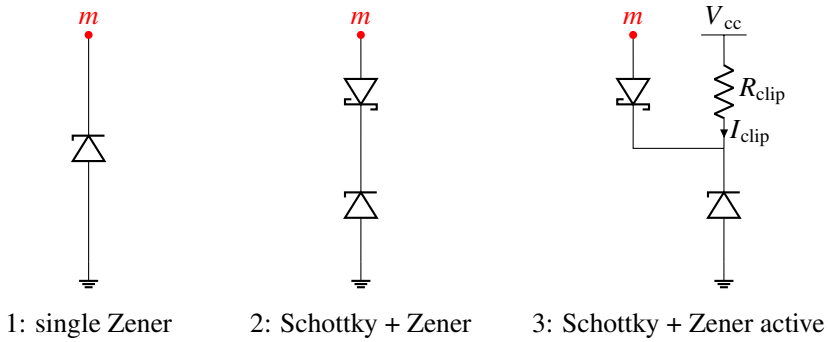

Fig. 9: Topologies of the three clipping branches.

itance. Schematics of the three approaches are shown in Fig. 9. The result on the measured voltage is shown in Fig. 10. During this experiment, D_2 was used as recovery acceleration diode and connected between the measurement node and ground. D_1 was used for the combined Schottky+Zener approaches.

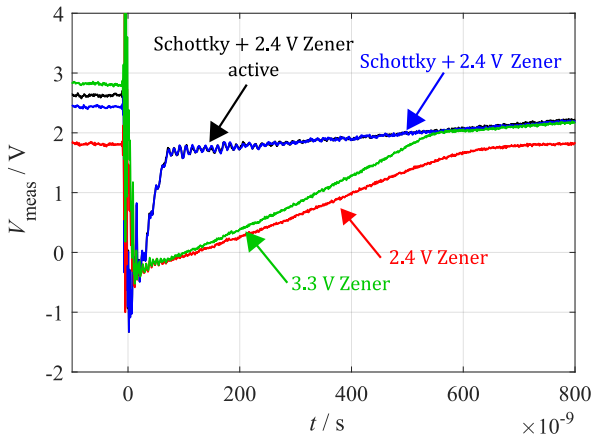

Fig. 10: Recovery behavior for the different clipping branch topologies.

Both Z-diodes feature very long reaction times of approx. 600 ns and more. The 2.4 V Zener diode leads to the slowest transient and the OVMC output voltage saturates before the correct $V_{measure}$ can be reached. Both combined approaches lead to similarly good results, both featuring reaction times of approx. 80 ns. The main drawback of the constantly reverse-biased approach is the obligatory power

supply, making the combined passive approach an ideal solution, especially for passive probes.

Practical Reaction Time Estimation

The different parts of the circuit that yielded the best results in the experiments before are now combined to form the optimized version of the OVMC. The bias resistor was chosen as $R_{\text{bias}} = 300\,\Omega$, resulting in a bias current of $I_{\text{bias,4}} = 10\,\text{mA}$. To reduce the switching noise contribution in the measurement, the air-core coil was removed from the setup and a 24 µH SMD coil was instead added on the PCB, yielding much better confined current return. The drawback is that this setup does not allow for a measurement of the current anymore, and due to the different electrical parameters, the current profile in this setup will be different to the one obtained before. However, since the low-side transistor showed near-perfect ohmic behavior for the on-state currents in the experiments conducted before, the pulse lengths have been adjusted to 25% of their original value, which matches the inductance ratio between the SMD coil and the air-core coil. Therefore, similar currents as observed the experiments conducted before can be expected. The output waveform of the proposed OVMC is shown in Fig. 12. The altered measurement setup is shown in Fig. 11. The switching behavior is again evaluated during the second pulse.

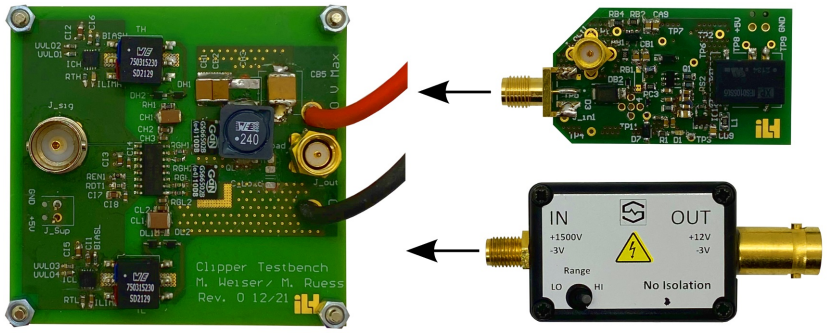

Fig. 11: Altered setup for the reaction time estimation with the two compared OVMCs.

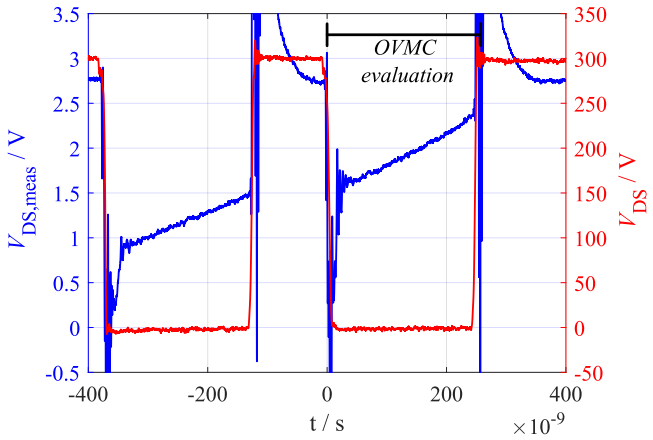

Fig. 12: Voltage waveforms of the altered DPT setup.

To put the performance into perspective, the proposed OVMC is compared to a commercial clipper probe, which is shown in Fig. 11. To compare both output voltages, the voltage offset of the proposed OVMC was evaluated in idle condition with $V_{\text{in}} = 0\,\text{V}$ as $V_{\text{offset}} = 938.9\,\text{mV}$. The reaction time was approximated by fitting a linear function to the reconstructed V_{in} of the proposed OVMC in the linear region in between $t_1 = 100\,\text{ns}$ and $t_2 = 200\,\text{ns}$ after the beginning of the second pulse, and comparing the measured output with the fitline, which is shown on the left hand side of Fig. 13. From this data, the maximum reaction time of the proposed OVMC can be approximated by calculating the difference between the measured curves and the fitted line and calculating the point at which the difference between both curves stays less

than the maximum measurement error of the measurement. The measurement deviation for both probes and the calculated reaction times are shown in the right hand side of Fig. 13.

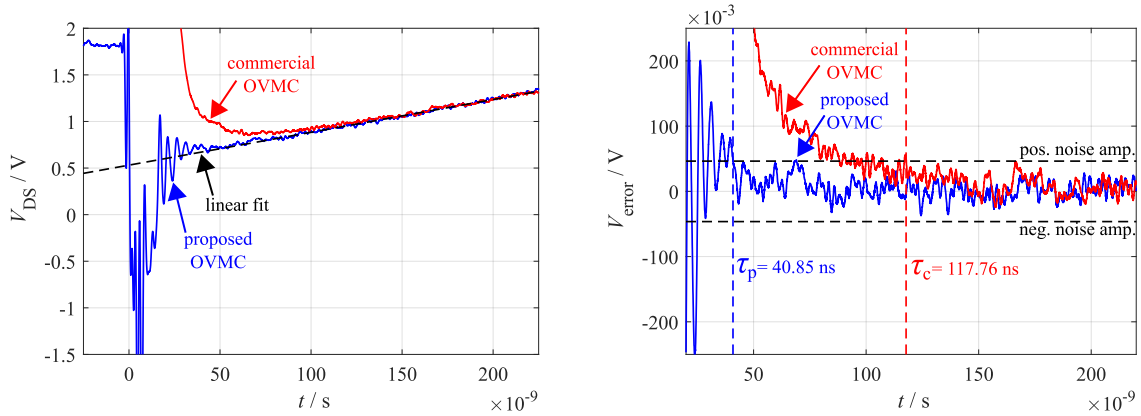

Fig. 13: Linear fit of the drain-source voltage evolution (left) and the resulting reaction time (right).

With this metric, the proposed OVMC is able to reach a reaction time of 40.85 ns, while the reaction time of the commercial clipper circuit is 117.76 ns. It has to be noted that this estimate is based on the time difference between the start of the falling edge of V_{DS} and the time when the switching noise has fully decayed. It is possible that the switching noise, which is present in the measured output voltage from 20 ns until 40 ns, originates from the measurement circuit itself. In this case, the reaction time of the proposed OVMC could potentially be even lower, correctly measuring the switching noise. The reported reaction time therefore represents a conservative approximation.

Conclusion

This work aims to give an overview over some of the design aspects that can be utilized to speed up the reaction time of OVMCs to facilitate their planning and construction. One commonly used OVMC topology has been examined, and the impact of several of its parts with regards to practical performance has been evaluated. A few general conclusions regarding the design of these circuits can be drawn.

- The stored charge on the voltage blocking device is critical to the OVMC reaction time.
- The way this charge is depleted is one of the most impactful performance determinators.
- A simple diode to supply charges from ground is one way to improve the circuit recovery by a lot. However, this leads to a limitation of the minimum measurable voltage.
- By using a voltage follower, the minimum output voltage can be confined more accurately, further improving reaction time. This way, the reaction time can be tailored to the personal needs.
- In general, the capacitance on the measurement node should be kept as small as possible. Devices with a large capacitance contribution should not be connected directly to this node. Instead, they can be connected in series with low capacitance devices to form a series connection, thus reducing the total capacitance contribution.

By combining all these factors, a reaction time of less than 50 ns can be readily reached, enabling the quick acquisition of the dynamic on-state resistance.

References

[1] Gamand F.: A 10-MHz GaN HEMT DC/DC Boost Converter for Power Amplifier Applications, IEEE Transactions on Circuits and Systems II: Express Briefs, Vol. 59, Issue: 11, 2012, pp. 776 - 779

[2] Cai Y.: Impact of GaN HEMT Dynamic On-State Resistance on Converter Performance, 2017 IEEE Applied Power Electronics Conference and Exposition (APEC)

[3] Meneghesso G.: Current Collapse and High-Electric-Field Reliability of Unpassivated GaN/AlGaN/GaN HEMTs, IEEE Transactions on Electron Devices, Vol. 53, No. 12, 2006, pp. 2932 - 2941

[4] Del Alamo J.: GaN HEMT Reliability, Microelectronics Reliability, Vol. 49, No. 9, 2009, pp. 1200-1206

[5] Li R.: Dynamic ON-State Resistance Test and Evaluation of GaN Power Devices Under Hard- and Soft-Switching Conditions by Double and Multiple Pulses, IEEE Transactions on Power Electronics, Vol. 34, No. 2, 2019
[6] Yang F.: Design of a Fast Dynamic On-resistance Measurement Circuit for GaN Power HEMTs, 2018 IEEE Transportation Electrification Conference and Expo (ITEC)
[7] Badawi N.: A new Method for Dynamic Ron Extraction of GaN Power HEMTs, PCIM Europe 2015
[8] Foulkes T.: Developing a Standardized Method for Measuring and Quantifying Dynamic On-State Resistance via a Survey of Low Voltage GaN HEMTs, 2018 IEEE Applied Power Electronics Conference and Exposition (APEC)
[9] Guacci M.: On-State Voltage Measurement of Fast Switching Power Semiconductors, CPSS Transactions on Power Electronics and Applications, Vol. 3, No. 2, 2018
[10] Rossetto L.: A Fast ON-State Voltage Measurement Circuit for Power Devices Characterization, IEEE Transactions on Power Electronics, Vol. 37, No. 5, 2022
[11] Li K.: Modelling GaN-HEMT Dynamic ON-state Resistance in High Frequency Power Converter, 2020 IEEE Applied Power Electronics Conference and Exposition (APEC)
[12] Weiser M. C. J.: A Novel Approach for the Modeling of the Dynamic ON-State Resistance of GaN-HEMTs, IEEE Transactions on Electron Devices, Vol. 68, No. 9, 2021