Virtual Junction Temperature Estimation during Dynamic Power Cycling Tests

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***Abstract*—This work proposes an acquisition concept, allowing measurement of the virtual junction temperature during application-oriented active power cycling tests (PCTs). PCTs are conceptualized with the failure mechanisms of conventional Si-based devices in mind, however, wide-bandgap devices can exhibit parameter inconsistencies like the dynamic ON-state resistance in GaN or the bias temperature instability in SiC. Application-oriented, dynamic active power cycling tests promise more accurate results than conventional quasi-static DC tests, but consistency with conventional accelerated aging tests is difficult to keep, as different parameter acquisition methods must be used. The combination of a novel high-voltage protected current source with a switch node blocking stage enables temperature estimation via the conventional reverse-blocking voltage method to alleviate this challenge. The proposed testbench achieves a time delay in the measurement of the virtual junction temperature of 120 µs in the dynamic PCT of a SiC power MOSFET module.**

***Index Terms*—power cycling, silicon carbide, temperature sensitive electrical parameter, virtual junction temperature**

I. Introduction

Since the controlled switches in power electronics are among the most vulnerable components [1], there is a need to focus on extending their lifetime or ensuring that replacement can be performed quickly and efficiently. To achieve this goal, accelerated lifetime testing and condition monitoring are being used, which monitor the junction temperature T_{J} as one of the major factors in lifetime models [2]. As SiC device development is still ongoing, and device maturity and reliability level improve from generation to generation, many of the reliability tests are not finally defined yet. New standards for active power cycling tests (PCTs) like the AQG-324 [3] are accommodating for testing of SiC semiconductor devices. To keep comparability with state-of-the-art PCTs, novel designs mainly need to establish a relation between their temperature estimation method and the widely used virtual junction temperature T_{vJ}. The estimation of the virtual junction temperature is achieved through the measurement of the voltage drop over the body diode of the device under test (DUT) transistor during off-state, while applying a small measurement current from source to drain [4]. Due to the inherent bias temperature instability of SiC devices in power electronic converters [5], the long-term stability during application is of interest [6]. Dynamic, application-oriented PCTs [7] allow to investigate this behavior, but due to the sophisticated setup necessary during the test, a temperature estimation via the virtual junction temperature is not directly possible. This work proposes a method to enable virtual junction temperature during a dynamic PCT.

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II. Topologies for Power Cycling Tests

PCT is an accelerated lifetime test for power electronic devices. It is used for reliability characterization of new packaging concepts, materials, devices and technologies. A conventional PCT can be described as a source measure unit, consisting of a current source and measurement circuitry. During the heating phase, the current source applies a heating current to the DUT and during the cooling phase a small measurement current is applied to allow for virtual junction temperature estimation. Depending on the type of device (IGBT, diode or MOSFET) the measurement current flows in the same or reverse direction as the heating current [8]. The load current I_{L} is switched by external switches to control on-period for heating and off-period for cooling down the devices. The device is heated up via DC-current by semiconductor power losses. After heating, the samples are cooled down by the heat sink coolant. This process is repeated to simulate the thermal stress that the device would experience in real-world use.

A. Static Power Cycling Tests

Fig. 2 shows the simplified equivalent circuit of a static DC PCT for a MOSFET, with the typical injected power and temperature profile during the test.

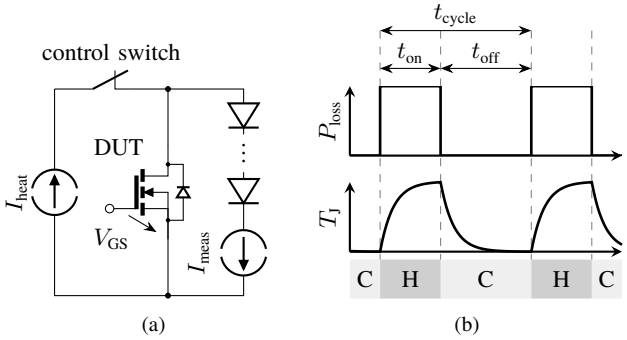

Fig. 2. Equivalent circuit of a static active power cycling test (a) using diodes to direct the heating current through the DUT. (b) Injected power and temperature profile applied to the device under test. (H = heating phase; C = cooling phase)

To induce thermomechanical stress in the DUT, it is repeatedly heated up and cooled down. Closing the control

switch applies the heating current across the device during the heating phase (t_{on}), therefore increasing the junction temperature. During the subsequent cooling phase (t_{off}), the control switch is opened, allowing the DUT to cool down. Depending on the duration of the heating phase different interconnects are stressed. For heating times in the range of 1 s to 15 s only fatigue of wire bond contacts is caused, whereas for phases ranging from 1 min to 15 min additionally cause fatigue of the soft solder contacts [9]. Using the temperature dependency of the pn-junction of the body diode of the device, a temperature sensor can be created. A second current source applies a constant current from source to drain across the body diode to enable the estimation of the junction temperature. In its simplest form a series of diodes is put in series of the extra current source to direct the heating current through the DUT, protecting itself from the heating current.

B. Dynamic Power Cycling Tests

In contrast to the conventional static PCTs, a dynamic PCT introduces switching losses in addition to the conduction losses, while at the same time applying nominal DC-link voltage V_{DC} during the test. It consists of an H-bridge topology, connected on the load side via a load inductor L [7]. Fig. 3 shows the equivalent circuit of a typical setup using two MOSFET half-bridges.

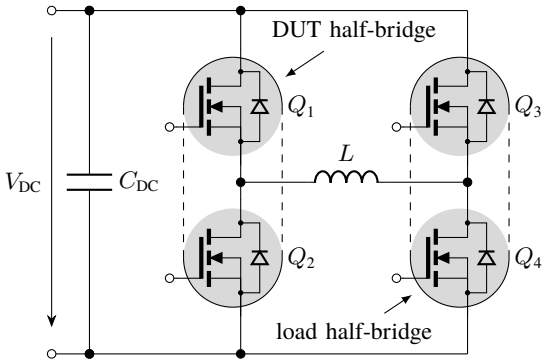

Fig. 3. Equivalent circuit of a dynamic active power cycling test using an H-bridge.

The load inductor L reduces the current ripple during the test and varies depending on the nominal blocking voltage of the DUT. While the conventional static PCT only allows for direct currents, the dynamic method can subject the DUT to arbitrary current waveforms. It is possible to run a test with a DC current, similar to the conventional test, by using the load half-bridge as a buck converter while using only one of the DUT transistors. Such a dynamic PCT enables test conditions resembling the operating points in the field, surfacing nonidealities in the operation of wide-bandgap devices like SiC MOSFETs or GaN HEMTs. Both the bias temperature instability of SiC MOSFETs [10] and the dynamic ON-state resistance $R_{\mathrm{DS,on}}$ of GaN HEMTs [11] are parasitic effects where the severity depends on the dynamic condition of the devices.

To keep comparability with a conventional PCT, however, the overarching test conditions must remain comparable. The swing of the virtual junction temperature is one of the main factors changing the achievable cycles and therefore must be consistent between methods. While it is relatively simple to achieve a virtual junction temperature for a conventional setup, the same approach cannot be used in the proposed dynamic setup.

III. Approach and Method

In the case of conventional static PCTs, the measurement circuitry can be simple, as their requirements are relatively low. When moving to application-oriented dynamic PCTs, mimicking the conditions apparent in the real operation, the implementation of the circuitry for condition monitoring becomes much more complex. On the one hand, it has to be able to withstand high voltages during the blocking state and on the other hand not interfere with the normal operation of the PCT. The main parameter of interest for PCTs is the virtual junction temperature of the DUT which yields the mean temperature of the chip [3]. Acquiring the temperature with different methods can result in a deviation of the acquired junction temperature. This is detrimental, as the mean cycles to failure of a DUT directly depend on the swing of the junction temperature. Direct comparison between different setups is therefore only possible with a common definition of the junction temperature measurement method. The main challenges of measuring the virtual junction temperature in a dynamic PCT, are to protect the measurement circuit from high voltages and to separate the DUT from the other phase leg. These are solved using a combination of a current source to inject a small measurement current, similar to the circuit shown in Fig. 2 and voltage measurement as used in ON-state voltage measurement circuits (OVMCs) [12] to measure the reverse-blocking voltage V_{SD}.

Fig. 4 shows the connection of the current source, necessary for the virtual junction temperature measurement, in the dynamic PCT introduced in Fig. 3 for the low-side transistor of the DUT half-bridge.

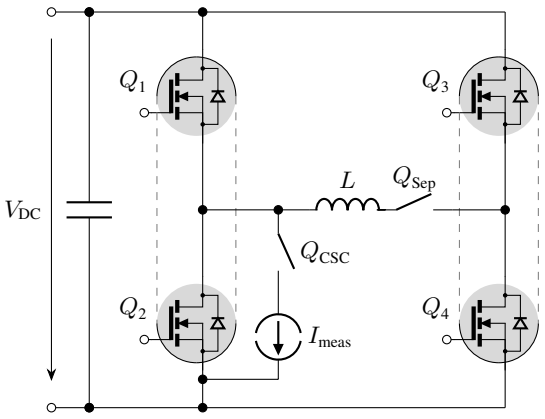

Fig. 4. Extension of the topology in Fig. 3 to allow for virtual junction temperature measurement. Q_{Sep} and Q_{CSC} control the current flow during the measurement, while a current source applies a measurement current between Source and Drain of the DUT.

For measurement of the virtual junction temperature of the high-side transistor, the circuit can be connected

similarly. An additional transistor Q_{CSC} protects the current source from the high voltage on the switch node of the DUT half-bridge when the low-side transistor blocks. Due to the connection of the transistors in the H-bridge, a second parasitic current path through the body diode of Q_4 and the load inductor L is formed. Ignoring the voltage drop over the resistive components in the loop due to the low current, this results in a measurable voltage according to (1).

$$V_{\mathrm{SD,measured}} = \frac{V_{\mathrm{SD,DUT}} \cdot V_{\mathrm{SD,Load}}}{V_{\mathrm{SD,DUT}} + V_{\mathrm{SD,Load}}} \tag{1}$$

As both the $V_{\mathrm{SD,DUT}}$ and $V_{\mathrm{SD,Load}}$ are temperature dependent, the measured virtual junction temperature is influenced by the temperature of both devices. Therefore, an additional blocking stage signified by Q_{Sep} is able to disconnect the two phase legs on the switch node. When Q_{Sep} is open and Q_{CSC} is closed, a constant current source supplies the DUT with the necessary measurement current as shown in Fig. 5.

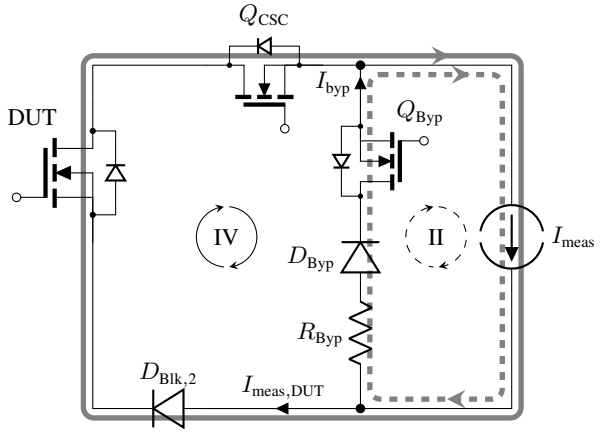

Fig. 5. Proposed connection of the current source to the DUT. Current flow during measurement is marked (IV) commutating from the additional bypass path (III) for improved dynamics.

The current source injects a constant low measurement current in the DUT in reverse direction. The current should be only a fraction of the rated current of the DUT, so that self-heating is minimized. At the same time, the influence of bond-wire degradation is minimized as shown in (2) for a conventional power module using bond-wires.

$$V_{\mathrm{SD,measured}} = V_{\mathrm{SD}} + 2 \cdot R_{\mathrm{bond}} \cdot I_{\mathrm{meas}} \tag{2}$$

where $V_{\mathrm{SD,measured}}$ is the measured voltage, V_{SD} is the reverse-blocking voltage and R_{bond} is the bond-wire resistance. A lower measurement current means a lower influence of the second term of (2) on the measured voltage, increasing the accuracy of the measurement. To protect the current source from potentially high drain-source voltage V_{DS} at the DUT, Q_{CSC} is realized by a transistor and two diodes $D_{\mathrm{Blk},1/2}$. For better dynamic performance, a bypass loop provides an alternative current path with a similar voltage drop as the DUT, consisting of R_{Byp} and D_{Byp}.

Small changes are needed on the system level to allow for virtual junction temperature measurement during the cooling phase of a PCT. When using the current source depicted in Fig. 5 in the topology shown in Fig. 4, the current source should be disconnected from the DUT in the heating phase and only in the cooling phase should the current be injected in the DUT. The necessary switching states for this behavior are shown in Fig. 6.

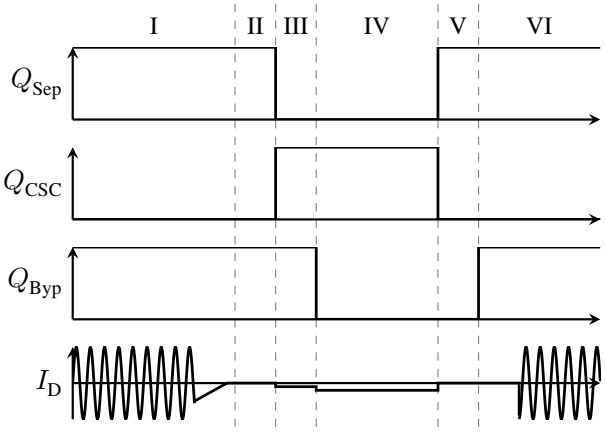

Fig. 6. Switching states of the transistors in the load and bypass path of the current source.

The states can be described as follows:

I) DUT heats up in the heating phase as is the case for a conventional PCT and the current controller regulates the load current to 0 A to initiate the cooling phase.

II) The switch node is discharged to 0 V by setting both half-bridge to their low-state. The remaining energy stored in the load inductor can then discharge through the freewheeling path formed by Q_2 and Q_4.

III) The two phase legs are disconnected by turning off Q_{Sep}, while, at the same time, the current source is connected to the DUT by using Q_{CSC}. The measurement current will now start to stabilize and flow through both the DUT and the bypass path.

IV) After a short delay, which was set to 100 ns in this work through an RC-low pass filter, the bypass path is disconnected by turning off Q_{Byp}. The virtual junction temperature can now be measured throughout the rest of the cooling phase.

V) Before the PCT can move on to the heating phase, the current source is again disconnected from the DUT, and the original state of the H-bridge topology is restored by turning on Q_{Sep}.

VI) Q_{Byp} follows Q_{CSC} after the same delay as in IV and the heating phase can start once again.

Without a bypass path, the current source operates as an open circuit while Q_{CSC} is open, requiring some time to recover from this condition when the current is supposed to flow through the DUT. This case is depicted in Fig. 7, comparing the current flowing through the DUT after closing Q_{CSC}.

In phase II the current path is closed solely by the bypass path leading to a bypass path current I_{byp} equal to the measurement current. After closing the transistor at the

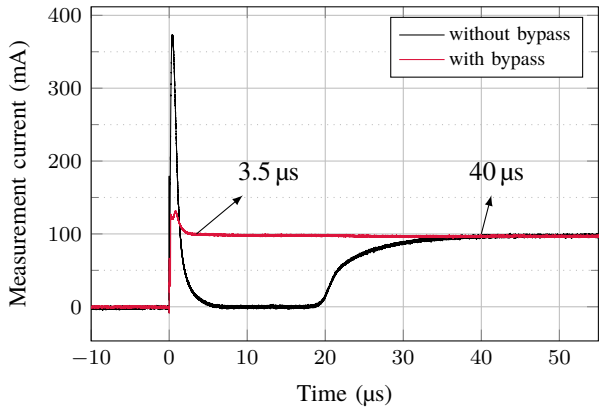

Fig. 7. Current commutation of measurement current at the start of the cooling phase. Corresponds to phase III - IV in Fig. 6. Adding a bypass path cuts down the recovery time more than tenfold.

input of the current source, the current is shared by both the bypass path and the DUT paths. After the set delay of 150 ns, phase IV begins and the bypass path is opened and the measurement current commutates to the DUT. In both cases a certain recovery time is needed before the correct current can flow. This recovery time is 3.5 µs with and 40 µs without the bypass path from the start of the cooling phase.

During phase IV in the cooling phase, an ON-state voltage measurement circuit is responsible for measuring the reverse-blocking voltage for the virtual junction temperature measurement. The circuit is depicted in Fig. 8 [12] and is based on depletion-mode MOSFETs.

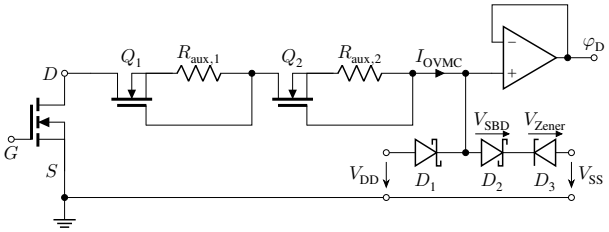

Fig. 8. ON-state voltage measurement circuit based on depletion-mode MOSFETs. Adapted from [12].

The transistors Q_1 and Q_2 in Fig. 8 are normally-on devices, allowing measurement of the drain potential φ_D according to (3):

$$\varphi_\mathrm{D}^{'} = \varphi_\mathrm{D} - I_\mathrm{lkg} \cdot \sum_{k=1}^{2} \left(R_\mathrm{aux,k} + R_\mathrm{DS,on,k} \right) \qquad (3)$$

where $\varphi_\mathrm{D}^{'}$ is the output potential of the clipper circuit, φ_D is the drain potential and I_lkg is the combined leakage current of the diodes and output amplifier. In the half-bridge topology of the PCT, a high voltage is present at the input of the OVMC, causing D_3 to break through. The inrush current causes a voltage drop over the auxiliary resistances, closing the channel of the MOSFETs and limiting $\varphi_\mathrm{D}^{'}$ to safe values. Using the $\varphi_\mathrm{D}^{'}$, a differential amplifier is used to acquire the reverse-blocking voltage. By using a positive voltage V_DD in contrast to the direct connection to the reference potential as used in [12], the measurement range of the OVMC can be extended to negative voltages, which are needed for the virtual junction temperature measurement.

Both the current source and the OVMC are implemented on a printed circuit board (PCB), shown in Fig. 9.

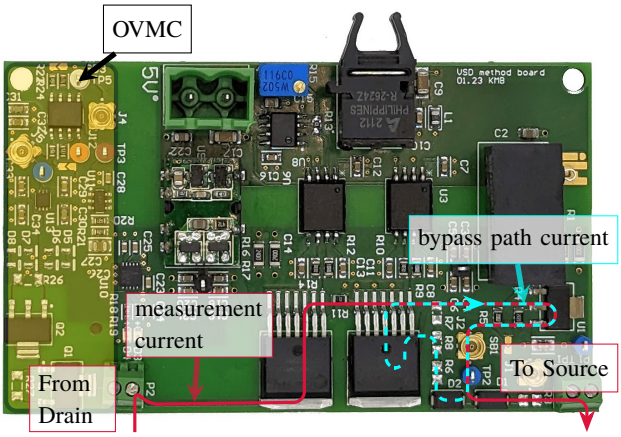

Fig. 9. Image of the reverse-blocking voltage measurement board. An additional ON-state voltage measurement circuit measures the voltage drop over the body diode for virtual junction temperature estimation.

A single fiber optic receiver is used to generate the control signals needed for the grate drivers of Q_CSC and Q_Byp, with the RC-low pass filter introducing the delay for the Q_Byp transistor. The resistance value of the resistor in the bypass path R_Byp is determined empirically and set to 30 Ω in this work. An LT3092 programmable current source provides the measurement current, set to 100 mA, roughly 1/1000 of the nominal current to minimize self-heating, using an external resistance. For SiC devices, it is necessary to use a sufficiently negative gate voltage, while measuring the reverse-blocking voltage, since the channel of SiC-MOSFETs is not completely closed at $V_\mathrm{GS} = 0\,\mathrm{V}$ [13]. The exact value depends on the individual device and has been empirically validated to be −7 V for the device used in this work.

IV. Setup and Results

The proposed circuit is validated through an experimental setup using the H-bridge topology shown in Fig. 4. Fig. 10 depicts the experimental setup described by the equivalent circuit.

The DUT is a 1.2 kV/120 A SiC MOSFET module BSM120D12P2C005. The PCB with the reverse-blocking voltage measurement circuitry is fixed on-top of the gate driver board and connected to the drain and source terminals of the module via short cables. To enable the H-bridge operation, a load module with a higher current rating is added and connected on the switch node through the series connection of the load inductor and the blocking stage. Both modules are connected to a shared, liquid-cooled heatsink used in the virtual junction temperature calibration and for cooling. To prevent the parasitic current loop through the load switches, the two half-bridges have to be disconnected during measurement through the

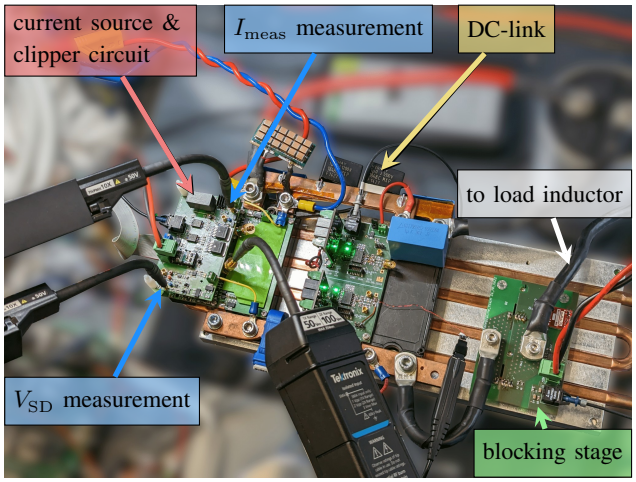

Fig. 10. Image of the implemented setup. The correct operation is validated by measurement of the reverse-blocking voltage and the measurement current through a shunt with differential voltage probes.

blocking stage, consisting of a bidirectional switch. This way, the current injected at the source of the DUT can only flow through the transistor itself. An air coil with an inductance of 200 µH connects the switch node of the two half-bridge modules together. The output of the OVMC is measured by a differential probe. The I_{meas} of the current source is observed through the measurement of the voltage drop over a 10 Ω SMD shunt placed on the same PCB. A rapid control prototyping hardware controls the setup by implementing a state based PCT procedure combining a current controller for the heating phase with the control signals of the switches added for the virtual junction temperature measurement.

A temperature control unit is attached to the setup and varies the temperature of the heatsink in a range of 20 °C to 140 °C for calibrating the reverse-blocking voltage with respect to the virtual junction temperature. Fig. 11 illustrates the measured reverse-blocking voltage and a temperature sensitivity of −1.70 mV/K is obtained.

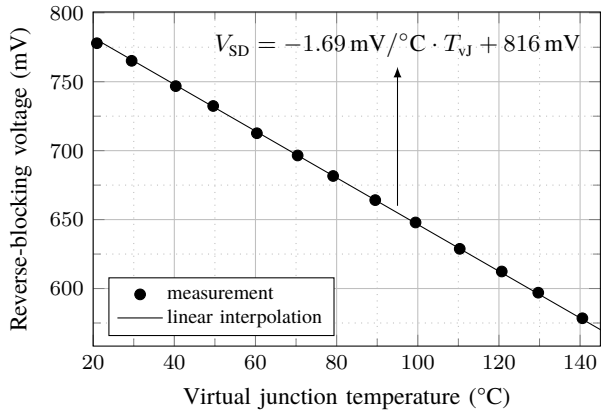

Fig. 11. Calibration curve of the reverse-blocking voltage with respect to the virtual junction temperature with added linear interpolation of the results.

The current source is set to a measurement current of 100 mA. The standard deviation of 0.4 mV shows the high linearity in the acquired reverse-blocking voltage of the current source over the measured temperature range. Due to the inherent Schottky diode parallel to the body diode in the used module, the acquired temperature will not only reflect the overall temperature of the SiC chips, but rather also of the additional Schottky diodes. Implementing a linear interpolation of the data points, the virtual junction temperature can be calculated from the reverse-blocking voltage for the setup in this work:

$$V_{\text{SD}} = -1.69\,\text{mV/K} \cdot T_{\text{vJ}} - 816\,\text{mV} \tag{4}$$

$$T_{\text{vJ}} = -590\,\text{K/V} \cdot V_{\text{SD}} + 482\,\text{K} \tag{5}$$

The exact calibration values will vary from transistor to transistor and must be measured on a per-device basis.

To verify the performance of the proposed current source, a dynamic PCT cycle is run. Using a DC-link voltage of 400 V the current controller of the rapid control prototyping hardware applies an AC current with an amplitude of 120 A to the DUT, to heat it up. At the end of the heating phase, the current source is connected to the DUT as described in Fig. 6. Fig. 12 shows the waveforms of the load current, measurement current and the drain-source voltage during this cycle.

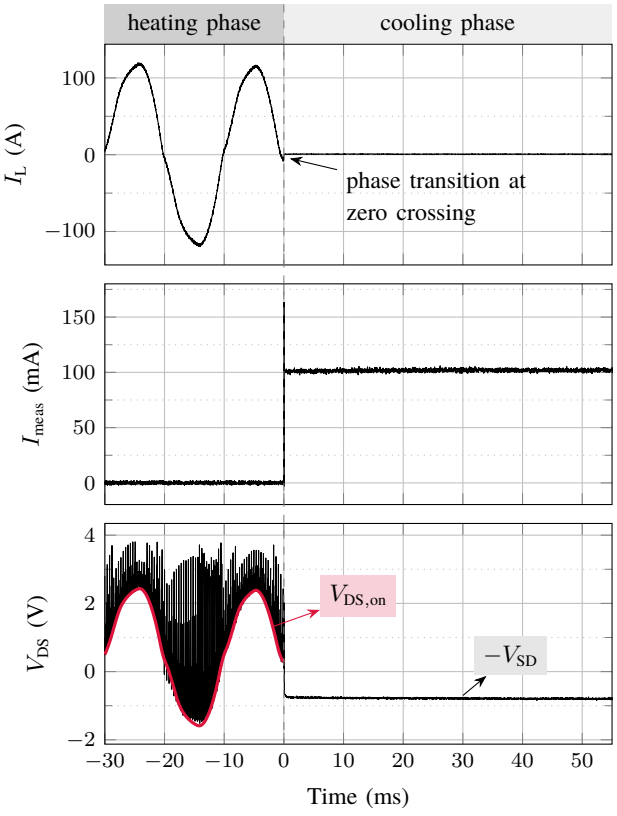

Fig. 12. Load current, measurement current and drain-source voltage during one PCT cycle. The ON-state voltage measurement circuit is able to measure the ON-state voltage during the heating phase, as well as the reverse-blocking voltage throughout the cooling phase.

The heating phase ends after the set period of 10 s, at which point the control system regulates the current down to 0 A, switching to the cooling phase, as soon as a zero transition is registered. Within the cooling phase,

the proposed current source applies a current of 100 mA across the device in reverse direction. The drain-source voltage measured by the OVMC follows the path of the I_{L} during the heating phase with a limit in the negative voltage due to the choice of V_{DD}. In the cooling phase, the reverse-blocking voltage can be calculated by inverting the measured voltage. A detailed view of the waveforms at the beginning of the cooling phase is shown in Fig. 13.

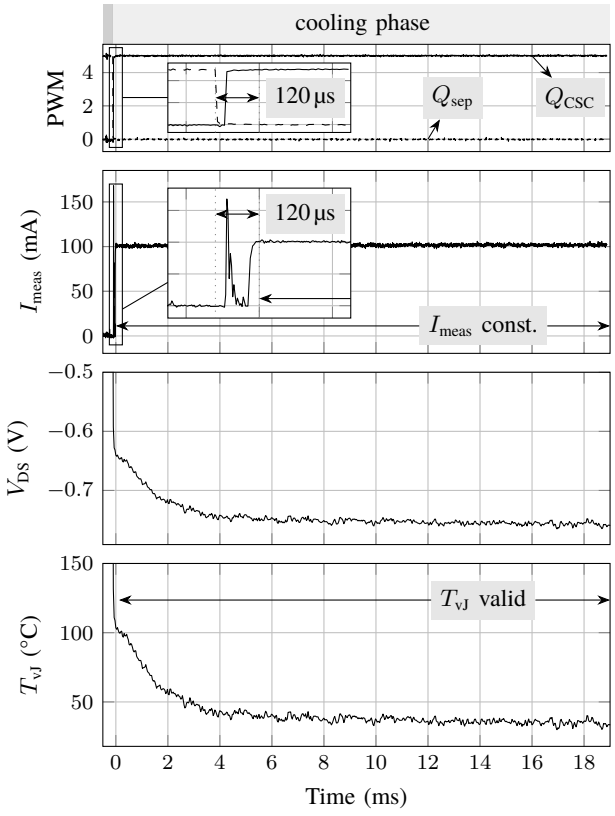

Fig. 13. Measured waveforms of the control signals of the transistor at the input of the current source and the transistor at the input of the current source, measurement current and drain-source voltage at the start of the cooling phase of Fig. 12. Using (5) the virtual junction temperature is calculated from the measured data.

The measurement has been aligned with the point in time when the measurement current has reached steady state. Therefore, all measured values within the cooling phase before this point must be discarded. In the area where the current is constant, the acquired voltage values can be considered valid. The measurement current can commutate quickly, reaching steady state after 120 µs, as the added bypass path lets the current source run without needing recovery from being open. For these operating conditions, a reverse-blocking voltage of 640 mV is acquired in the beginning, increasing to 760 mV after 20 ms. Using (5) to calculate the virtual junction temperature, a value of 105 °C is found as the first usable temperature, dropping down to 35 °C towards the end of the measurement.

V. Conclusion

This work presents a reverse-blocking voltage measurement implementation, enabling virtual junction temperature measurement in dynamic PCTs using H-bridge topologies. Conventional PCTs cannot reflect application-oriented conditions, which can cause reversible parameter shifts in wide-bandgap based devices depending on the current and/or past operating points. Through the combination of a low current source and a blocking stage, the cooling phase of the accelerated aging test is modified to accommodate the reverse-blocking voltage measurement in an application-oriented dynamic PCT. With the proposed method, a dynamic PCT with SiC half-bridge modules is performed, monitoring the virtual junction temperature during the cooling phase. An acquisition of the virtual junction temperature is possible after approximately 120 µs after connecting the current source in the cooling phase. The proposed topology can be further simplified by combining the ON-state voltage measurement circuit with the current source by replacing the blocking transistor with its input stage, if the added voltage drop is manageable. Thus, if a change in the load path to accommodate a blocking stage is possible, this method is a key step in keeping the comparability of novel, dynamic PCTs with conventional static PCTs.

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