# Efficiency Improvement of Single-Stage AC-DC LLC Converter Using a Line Cycle Synchronous Rectifier (SR) Driving Strategy

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## Keywords

«AC-DC converter», «DAB-LLC converter», «Synchronous rectifier (SR)», «Silicon Carbide (SiC) MOSFET», «Gallium Nitride (GaN) HEMT», «Wide bandgap devices».

## Abstract

Synchronous rectification that is being widely used in high-power Inductor-Inductor-Capacitor (LLC) DC-DC converters to improve efficiency can be challenging in single-stage AC-DC LLC converters with high output voltage levels (i.e., >100V) where synchronous driving ICs cannot be used. In this paper, a simple line cycle SR driving strategy with direct MCU control is proposed for single-stage AC-DC LLC converters. The principles of operation and methodology behind the proposed line cycle SR driving strategy are discussed. Simulation and experimental results validated the performance of the proposed SR driving strategy for a 250 V to 400 V output voltage range AC-DC LLC converter. A full-load efficiency of 98.1 % was achieved for the 250 V output voltage condition and a full-load efficiency of 97.3 % was achieved for the 400 V output voltage condition. Compared with a fixed ON time method, around 0.5 %, and 0.8 % efficiency improvements were observed in 250 V and 400 V output voltage conditions, respectively. In addition, it is observed that the proposed simple SR driving method obtains the same efficiency levels as more complex adaptive SR driving approaches.

## Introduction

Resonant converters have been the focus of many research studies over the past decades. Some studies discussed the optimal design of resonant converters using various computer-aided methods [1] and [2]. Some research studies focused on magnetics improvement for resonant converters [3] and [4]. Some studies discussed the impact of wide bandgap semiconductors such as Gallium Nitride (GaN) HEMTs and Silicon Carbide (SiC) MOSFETs in improving the efficiency and power density of resonant converters [5] and [6]. In high-power DC-DC resonant converters diode conduction loss is a major contributor to the total power conversion loss. Hence, using synchronous rectification is a necessity for low voltage and high current applications to achieve high conversion efficiency at kW levels. Therefore, a lot of research has been done on Synchronous Rectifier (SR) driving strategies for LLC DC-DC converters [7]-[12].

One of the common practices for SR driving in resonant converters is the drain-source voltage sensing using SR driving ICs [7]. This method is widely used in many low output voltage high current applications [8] and [9]. The performance of driving ICs is promising; however, it can be highly dependent on the effect of parasitic components of the circuit that reduces the reliability of the converter. On the other hand, the operating voltage of most of these driving ICs is limited to below 100V and hence they are not suitable for SR driving at higher output voltage levels. In [10], some additional components are added to the famous NCP4306 SR driving IC to make it work for high output voltage applications, however, the disadvantages of low voltage sensing still exist.

Another common practice for SR driving is a model-based approach that generates an appropriate gate pulse in the MCU to drive the SR. In [11] the SR driving signal is generated based on the primary bridge

signals using a simulation model to find out the turn ON and OFF delay that was inserted into a look-up table for all the operating conditions. In [12] a rather fixed conduction time is used with specific turn ON and -OFF delays for the LLC converter of an EV battery charger. In this approach, the output voltage and current should be considered to correctly reflect the output power and tune proper driving signal delays accordingly to avoid inaccurate gate signals. In [13], an adaptive sensor-less model-based digital driving scheme is developed for the LLC converter in DC-DC applications. In this method, the output voltage and current are sensed to find out the load conditions, then based on the switching frequency the conduction time of the SR is calculated and tuned online.

Most of the literature for SR driving of resonant converters only discussed the DC-DC application so far. In recent years there is a high interest in the implementation of the LLC converter in single-stage AC-DC conversion with PFC capability which is due to its soft-switching performance [14]-[17]. Near the line Voltage Zero Crossing (VZC) area of AC to DC conversion, the input power delivered to the load is much smaller than the rated power, and in such light load conditions, both SR late turn ON and early turn OFF can happen which makes the SR driving of LLC converter more challenging. For low output voltage conditions, it is still possible to use the same dedicated SR controller ICs as in DC-DC converters. However, this method is not transparent to the designer, is not immune to noise, and there is no full control over the driving signals. Therefore, a proper SR driving strategy for LLC converter in AC-DC conversion is missing to achieve enhanced power conversion efficiency in high-power applications and high output voltage levels (i.e., >100V).

In this paper, a simple line cycle SR driving strategy is proposed for single-stage AC-DC LLC converters. The proposed method is a sensor-less approach with digital driving signals coming directly from the MCU. The principles of the proposed SR driving method are described in the next section followed by simulation results and experimental results from a 500 W wide bandgap-based prototype to verify the performance of the proposed line cycle SR driving strategy for the single-stage AC-DC LLC converters. This paper is concluded in the last section.

## The Proposed Line Cycle SR Driving Strategy

Fig. 1 illustrates the structure of a single-stage AC-DC LLC converter with active switches for input and output rectifiers. Some of the main characteristics of this converter are demonstrated in Fig. 1. The input rectifier bridge switches ($S_1$-$S_4$) operate at line frequency ($f_{line}$) with Zero Current Switching (ZCS) performance, which can be implemented with Si MOSFETs. It is mentioned in the literature that to achieve PFC while maintaining soft-switching the operating switching frequency ($f_{sw}$) of the primary bridge of the LLC converter should vary over the half-line cycle between the parallel resonant frequency ($f_p$) and series resonant frequency ($f_r$) [14]. In this way, primary side bridge switches ($Q_1$-$Q_4$) can take advantage of Zero Voltage Switching (ZVS) and the secondary side bridge switches ($SR_1$-$SR_4$) can take

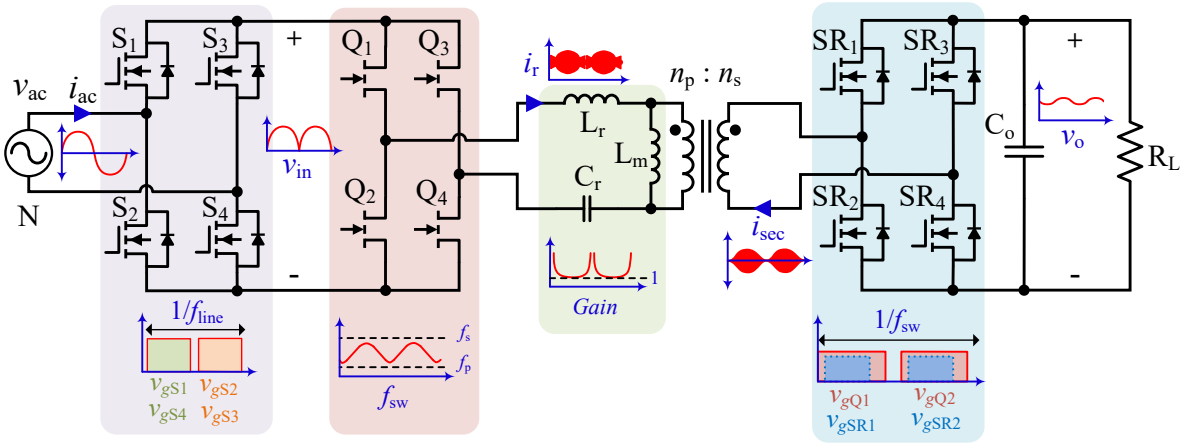



Fig. 1. The single-stage AC-DC LLC converter with synchronous rectifier bridges.

advantage of ZCS. The latter allows high switching frequency implementation leading to high power density designs. Since the output rectifier switches should be controlled based on the synchronized pulses with the respective gate pulses of the primary bridge switches, this method is called synchronous rectification.

Details of different operating conditions over the half-line cycle with primary and secondary bridge driving signals are illustrated in Fig. 2. Over the half-line cycle, the LLC tank goes through a combination of various modes such as O, P, and N modes. Based on the desired operating condition of the LLC converter in PFC mode, the majority part of the line cycle operation is around the peak line voltage while the LLC tank is in PO mode delivering the highest power to the load. It is followed by OPO modes at the sides and O modes near the line VZC where no power is delivered to the load hence the SRs should be turned OFF to avoid reverse power flow. It should be noted that since the PN and PON modes are more likely to lose ZVS, they are avoided in the design procedure, and hence the N mode which normally happens in a very short time is neglected in the analysis. Moreover, the NP, NOP, and OP modes that happen in the above resonant area are avoided in the LLC resonant tank design as it is desirable to operate below the series resonant frequency to take advantage of ZCS for the SRs.

From Fig. 2 it can be observed that in PO mode the turn ON instant of the SR is synchronized with the respective primary switch with a small turn ON delay (1-2% of the switching cycle) considering the propagation delay of the driver ICs. In OPO mode the turn ON delay should be adjusted based on the switching frequency and load condition to avoid reverse power flow. The conduction time of the SR is related to the load and switching frequency that can be calculated from

$$t_{ON}(\theta) = \frac{1}{2f_{sw}(\theta)}\sqrt{-\frac{\pi}{4}\frac{\omega_{sw}(\theta)L_m}{n^2R_L(\theta)} + \sqrt{\frac{\pi^2}{16}\left(\frac{\omega_{sw}(\theta)L_m}{n^2R_L(\theta)}\right)^2 + \frac{\pi}{2}\frac{\omega_{sw}(\theta)L_m}{n^2R_L(\theta)}\left(\frac{f_{sw}(\theta)}{f_r}\right)^2}} \quad (1)$$

where $f_r$ is the series resonant frequency, $\omega_{sw}(\theta)$ is the line phase angle dependent angular switching frequency and $R_L(\theta)$ is the line phase angle dependent load that can be calculated as follows.

$$f_r = \frac{1}{2\pi\sqrt{L_r \times C_r}} \quad (2)$$

$$\omega_{sw}(\theta) = 2\pi f_{sw}(\theta) \quad (3)$$

$$R_L(\theta) = \frac{4 \times \left(n_p/n_s\right)^2}{\pi^2 \sin^2(\theta)} \times R_{L\_FL} \quad (4)$$

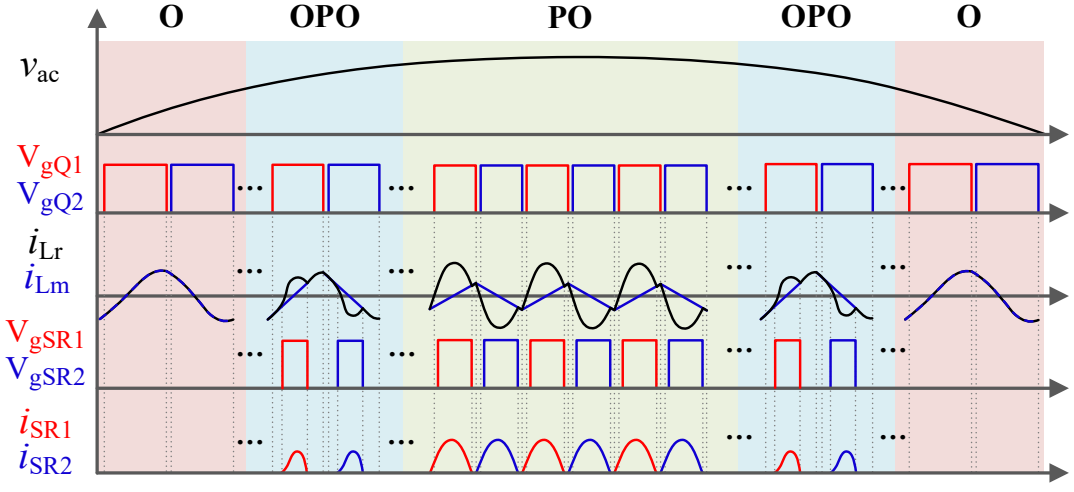
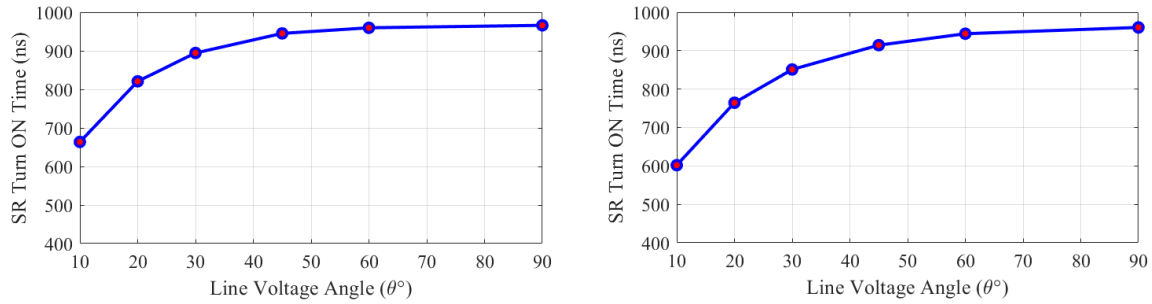



Fig. 2. Different operating conditions and respective switching operations over the half-line cycle.

In (4) $R_{L\_FL}$ is the load resistance corresponding to the rated output power (i.e., $P_{o\_FL}$). Due to brevity, the design of LLC tank parameters for AC-DC conversion is not discussed here as the detailed analysis and design are provided in [15]. The SR turn ON time for two different output voltage and load conditions are plotted over a quarter line cycle in Fig. 3. It can be observed that only after $\theta$=45° a noticeable reduction can be observed in the calculated turn ON time. The latter suggests using a fixed turn ON for the PO mode where the highest power is being delivered to the load. Moreover, to perform a proper SR driving strategy it is crucial to find out the boundary condition between the OPO and PO modes.

In the proposed SR driving strategy, the SRs are turned ON with a fixed calculated ON time for the PO mode and they are turned OFF as soon as the SR turn ON delay becomes large in OPO mode. In this way, the majority of AC power (~70%) is delivered to the load when SRs are operating. This method improves efficiency over fixed turn ON of the SRs by avoiding reverse power flow in O mode. Moreover, it achieves the same efficiency as implementing a complicated online calculation or an adaptive method over the line cycle that requires expensive fast microprocessors and/or additional voltage/current sensing.




(a) for $V_o$=250 V and $P_o$=330 W (b) for $V_o$=400 V and $P_o$=500 W

Fig. 3. Calculated SR conduction time over a quarter line cycle at different line voltage angles ($\theta$).

## Simulation and experimental results

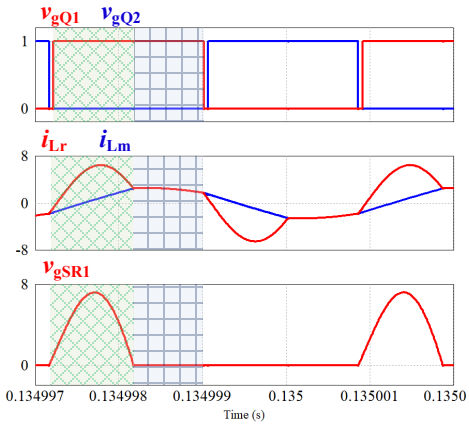
A simulation model is built in the PSIM environment to verify different operating modes of the LLC converter over the AC line cycle. Table 1 listed the design parameters used for computer simulations as well as the components used in the laboratory prototype.

Fig. 4 illustrates the simulation results over the line cycle for $V_o$=400 V, $P_o$=500 W condition to show different operating modes of the single-stage LLC converter in AC-DC conversion. It should be mentioned that in all the simulation results a green background pattern is used to show power delivery P mode and a dark blue background pattern is used to show O mode where there is no power delivery to the output. Both Fig. 4 (a) and Fig. 4 (b) show the PO mode at $\theta$=90° and $\theta$=45°. As can be observed the current of $SR_1$ starts to rise at the instant $Q_1$ turn ON and it ends after a certain conduction time. Fig. 4 (c) shows the OPO mode where the power delivery to the output is reduced and a phase shift between the primary gate pulse and the SR current starts to develop that demands a turn ON delay for the $SR_1$ driving. Fig. 4 (d) illustrates the O mode where there is no power delivery to the output and hence the SRs should be turned OFF in this mode to avoid reverse current flowing.

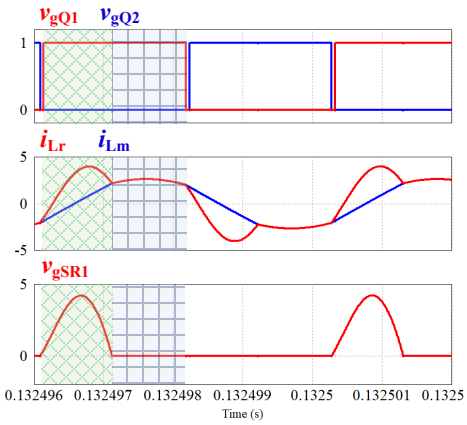
Fig. 5 shows the simulation results over the line cycle for $V_o$=250 V, $P_o$=330 W condition. Operating modes are mostly similar to Fig. 4 for $V_o$=400 V, $P_o$=500 W condition, however, the P mode is mostly longer in PO and OPO modes that is because the switching frequency is closer to the series resonant frequency for $V_o$=250 V, $P_o$=330 W condition.

**Table 1: The parameters used in both simulation and experiment.**

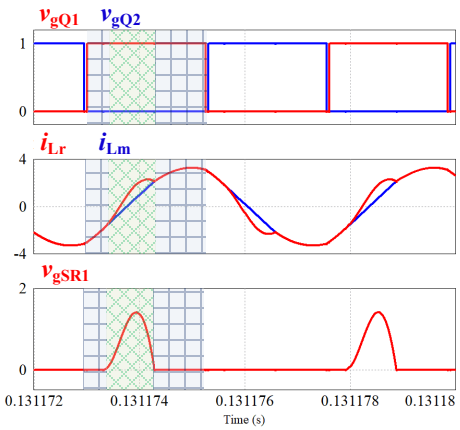
| Parameters/Descriptions | | Values |
|---|---|---|
| Output Power Range ($P_o$) | | 333 W - 500 W |
| AC Voltage ($V_{ac}$) | | 220 $V_{RMS}$ |
| Output Voltage Range ($V_o$) | | 250V - 400V |
| Line Frequency ($f_{line}$) | | 50 Hz |
| Switching Frequency Range ($f_{sw}$) | | 200 kHz - 450 kHz |
| Parallel Resonant Inductance ($L_m$) | | 120 µH (PQ3230 - 3F36) |
| Series Resonant Inductance ($L_r$) | | 23 µH (PQ2620 - 3F36) |
| Series Resonant Capacitance ($C_r$) | | 4.8 nF |
| Integrated Transformer Turns Ratio ($n_p : n_s$ ) | | 24 : 19 |
| Input LC Filter | Inductance ($L_f$) | 15 µH |
| | Capacitance ($C_f$) | 1 µF |
| Output Capacitance ($C_o$) | | 200 µF |
| Input Rectifier Bridge Si MOSFET | | IPP60R099P7 (650V - 31A - 99mΩ) |
| Inverter Bridge GaN E-HEMT | | GS66504B (650V - 15A - 130mΩ) |
| Output Rectifier Bridge SiC MOSFET | | C3M0120065J (650V - 21A - 157mΩ) |



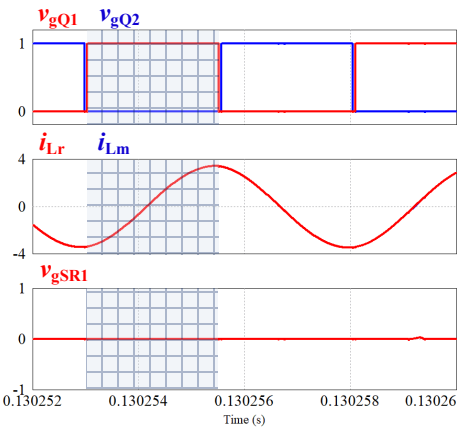

(a) $V_{in}$=311 V, $\theta$=90°




(b) $V_{in}$=220 V, $\theta$=45°

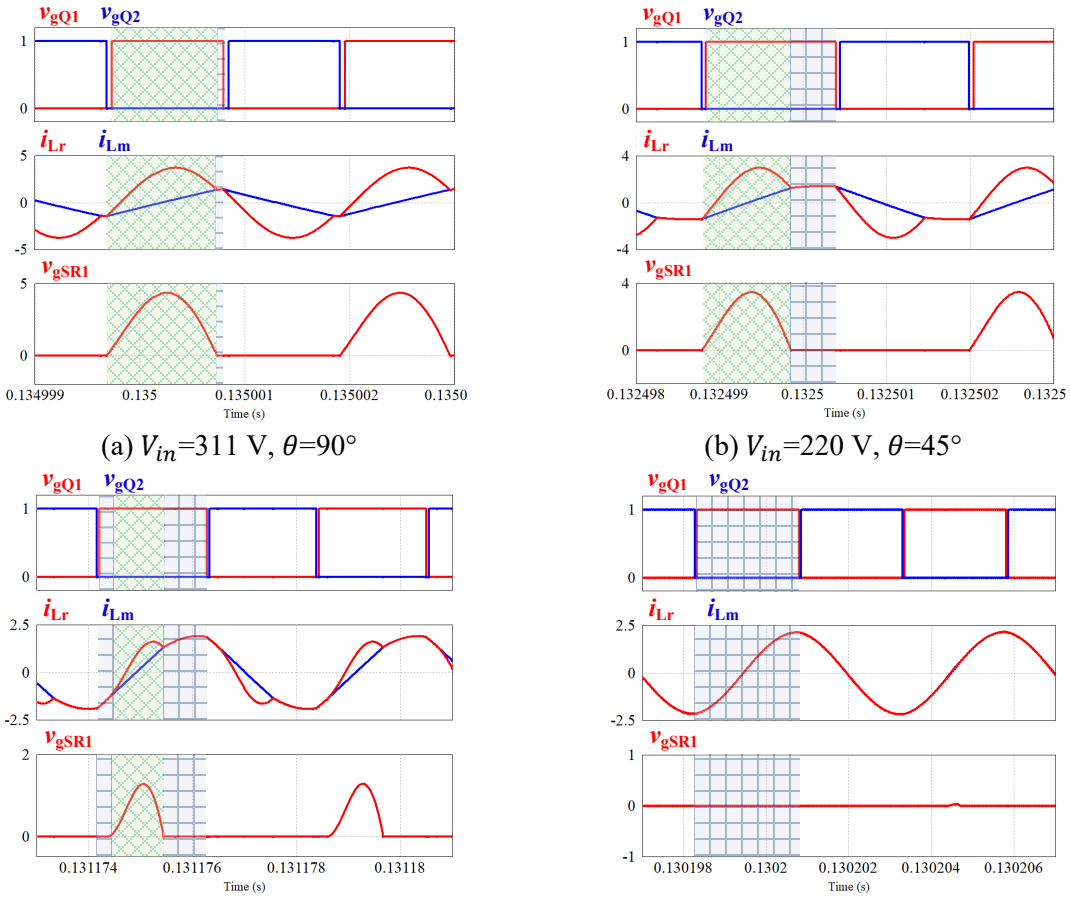



(c) $V_{in}$=105 V, $\theta$=20°




(d) $V_{in}$=27 V, $\theta$=5°

Fig. 4. Simulation results over the line cycle for $V_o$=400 V, $P_o$=500 W condition showing PO, OPO, and O operating modes.




(a) $V_{in}$=311 V, $\theta$=90° (b) $V_{in}$=220 V, $\theta$=45°

(c) $V_{in}$=105 V, $\theta$=20° (d) $V_{in}$=27 V, $\theta$=5°

Fig. 5. Simulation results over the line cycle for $V_o$=250 V, $P_o$=330 W condition showing PO, OPO, and O operating modes.

A wide bandgap-based (GaN and SiC) laboratory prototype is built to verify the performance of the proposed SR driving strategy for single-stage AC-DC LLC converters. A picture of the laboratory prototype is shown in Fig. 6. A low-cost Microchip dsPIC microcontroller is used to implement pulse frequency modulated control and perform PFC by providing proper driving signals for the switching bridges of the single-stage AC-DC LLC converter over the line cycle. It should be mentioned that input rectifiers are 650V Silicon MOSFETs and 650 V GaN HEMTs are used for the primary switching bridge while 650 V SiC MOSFETS are used for the synchronous rectifiers. Different scenarios are implemented in practice for the sake of comparison. First, the SR is turned on with a fixed ON time found from the calculation. Second, the proposed method is implemented by turning OFF the SRs over the line cycle after a certain voltage level that is found from the calculation and fine-tuned based on simulation. Last, an adaptive SR driving is implemented using a look-up table mapped with the delay and conduction time data extracted from the simulation to compare the efficiency with the proposed SR driving method.

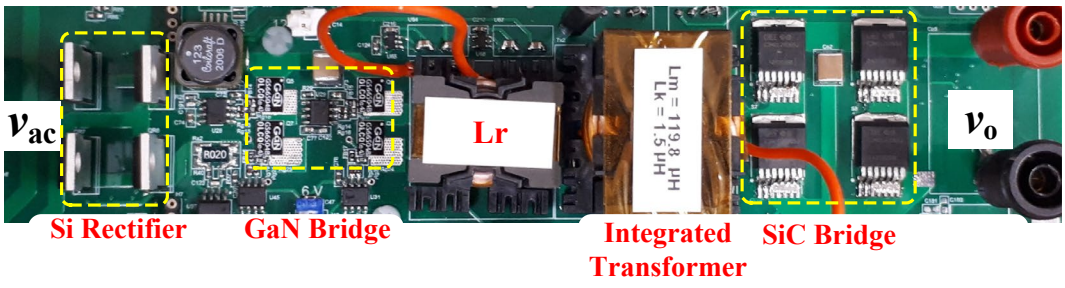
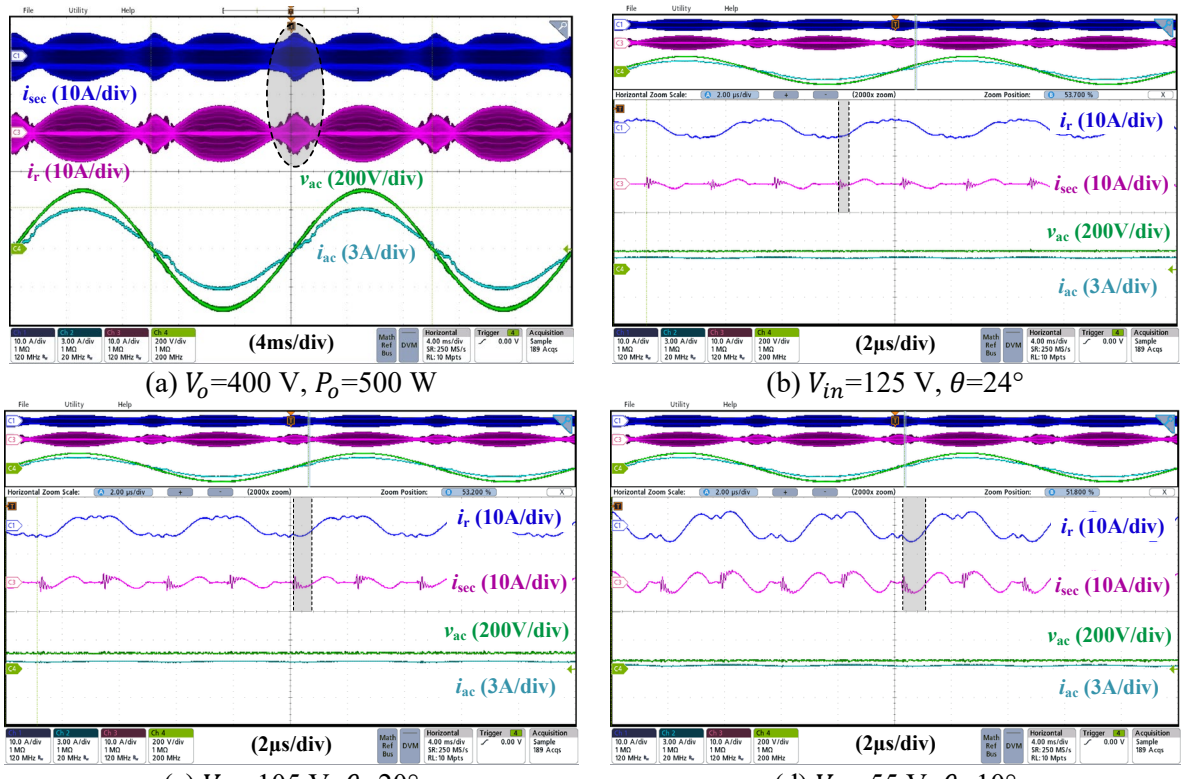



Fig. 6. A picture of the 500W LLC AC-DC converter laboratory prototype.

Fig. 7 (a) shows the experimental results of the single-stage AC-DC LLC converter with a fixed SR ON time over the line cycle. As mentioned before, around the line VZC points the LLC converter operates in O mode, and hence by modulating SRs in that area some reverse power flow is introduced which decreases the power conversion average efficiency over the line cycle. Zoomed-in waveforms for $\theta$=24°, $\theta$=20°, and $\theta$=10° are shown in Fig. 5 (b) to Fig. 5 (d), respectively. The reverse current due to early turn ON of the SRs can be observed in the secondary current waveforms showing the OPO mode operation of the LLC tank. The reverse current problem gets worse when the O stage at the beginning of the OPO mode gets larger at smaller line angles.

The proposed SR driving strategy for $V_o$=400V is shown in Fig. 8 where the SRs are turned ON after $\theta$=26° to avoid reverse power transfer in OPO and O modes. From Fig. 8 (b) to Fig. 8 (d) it can be observed that a fixed conduction time of 940 ns with a 30 ns turn ON delay is providing a proper turn ON and OFF instants for the SRs. Below $\theta$=26° the turn ON delay starts to become larger and hence the SRs are turned OFF after that angle to avoid reverse current flow. The exact border angle at which the SRs need to be turned OFF should be checked with the simulation results as the theoretical values calculated in Fig. 3 are based on First Harmonic Approximation (FHA) and hence are not so accurate for frequencies far away from the series resonant frequency. In Fig. 8 (e) and Fig. 8 (f), the operating condition at $\theta$=20° and $\theta$=10° are shown, respectively. It can be observed that there is no reverse current as the body diode of the SiC MOSFETs are fast enough and hence operating properly.

Furthermore, to emulate online tuning SR driving over the line cycle an adaptive SR driving is implemented via a look-up table using the parameters found from the simulation to compare the efficiency with the proposed SR driving method. The latter resulted in no reverse current in OPO mode, and the SRs were turned ON and OFF at the right instants from $\theta$=90° to VZC points and vice versa. Moreover, it is found that the efficiency with the complicated online tuning SR driving will either be similar to or less than 0.1 % higher than the proposed simple SR driving method, which does not justify the complex implementation via a powerful microcontroller.




(a) $V_o$=400 V, $P_o$=500 W

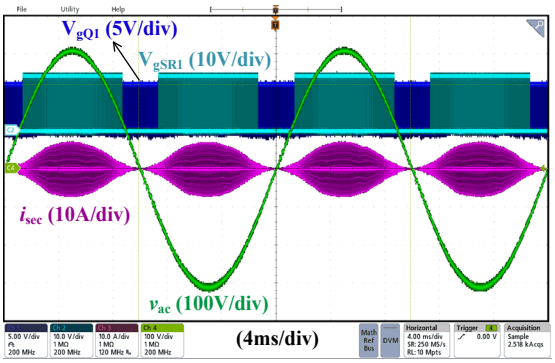
(b) $V_{in}$=125 V, $\theta$=24°

(c) $V_{in}$=105 V, $\theta$=20°

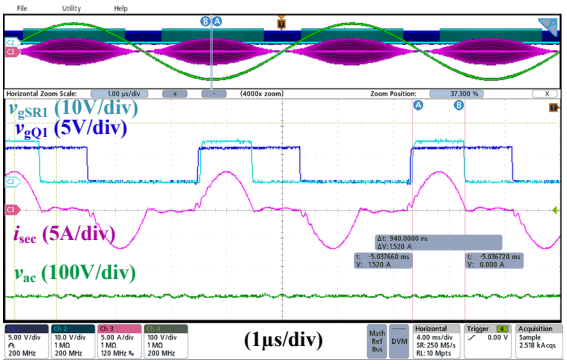
(d) $V_{in}$=55 V, $\theta$=10°

Fig. 7. Experimental results using a fixed SR ON time over the line cycle.

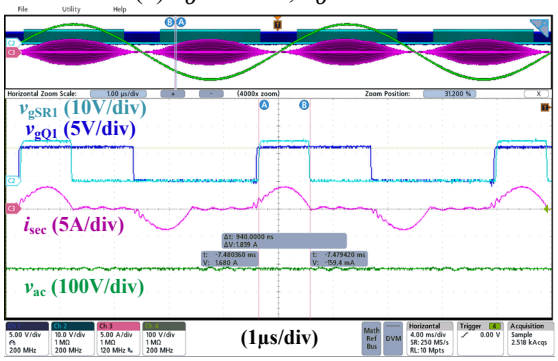
Fig. 9 (a) illustrates the full-load efficiency of 97.3% that was achieved for $V_o$=400 V at $P_o$=500 W condition and is 0.8 % higher than using a fixed SR conduction time over the line cycle. The full-load efficiency for $V_o$=250 V at $P_o$=330 W condition was measured to be 98.1 % which is shown in Fig. 9 (b). For the same output level condition, the efficiency with a fixed SR conduction time was 97.6 %. It should be mentioned that all the efficiency measurements were carried out using an LMG671 Zimmer precision power analyzer.



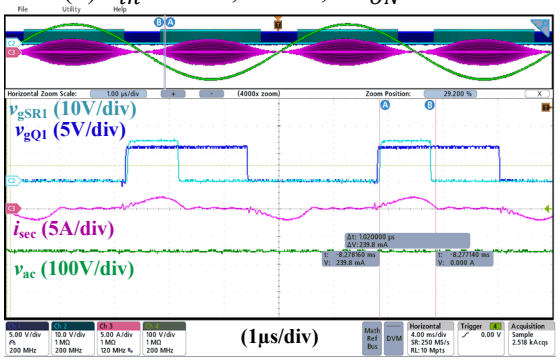

(a) $V_o$=400 V, $P_o$=500 W



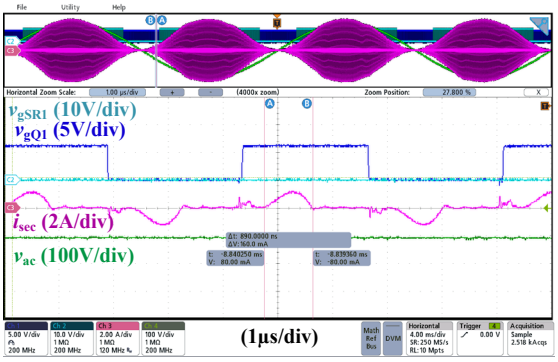

(b) $V_{in}$=311 V, $\theta$=90°, $SR_{ON}$=940 ns



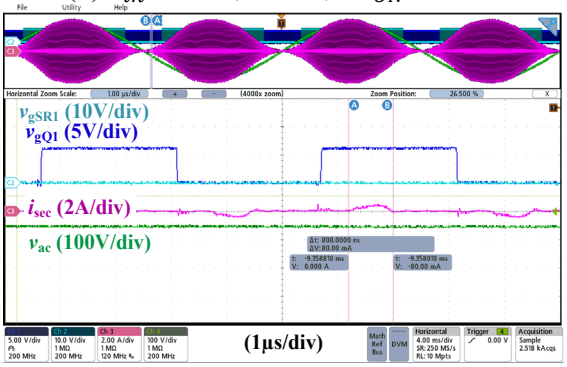

(c) $V_{in}$=220 V, $\theta$=45°, $SR_{ON}$=940 ns




(d) $V_{in}$=155 V, $\theta$=30°, $SR_{ON}$=940 ns

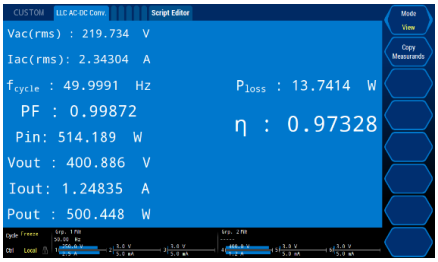



(e) $V_{in}$=105 V, $\theta$=20°, $SR_{ON}$=890 ns

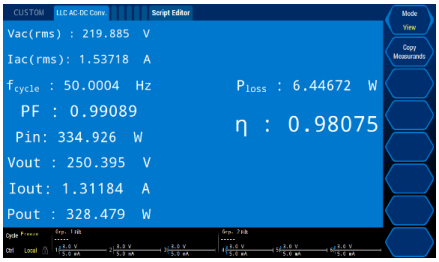



(f) $V_{in}$=55 V, $\theta$=10°, $SR_{ON}$=800 ns

Fig. 8. Experimental results of the proposed line cycle SR driving strategy for $V_o$=400 V, $P_o$=500 W.




(a)




(b)

Fig. 9. Efficiency measurement results with the proposed synchronous rectification strategy for (a) $V_o$=400 V, $P_o$=500 W, and (b) $V_o$=250 V, $P_o$=330 W.

## Conclusion

This paper proposed a new SR driving strategy for single-stage AC-DC LLC converters. The simplicity and effectiveness of the proposed method is a key feature that allows reliable efficiency improvement through proper SR operation of AC-DC LLC converters in high output voltage applications above 100 V. The principles of operation and analysis of the proposed SR driving strategy are discussed. Moreover, simulation and experimental results verified the analysis and the efficacy of the proposed direct MCU SR driving strategy for two different output voltage and load conditions. Furthermore, the experimentally measured efficiency comparison with a more complex alternative method verified that the proposed simple method can effectively improve the conversion efficiency.

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