Grid-Forming Control for Enhanced Microgrid Interconnection

Tobias Erckrath[1], Christian Bendfeld[1], Peter Unruh[1], Axel Seibel[1], Marco Jung[1,2]

[1]Fraunhofer Institute for Energy Economics
and Energy System Technology (IEE)
Joseph-Beuys-Str. 8
Kassel, Germany
Tel. +49 561 7294 - 1569
Tobias.Erckrath@iee.fraunhofer.de
https://www.iee.fraunhofer.de

[2]Hochschule Bonn-Rhein-Sieg
University of Applied Sciences
Grantham-Allee 20
Sankt Augustin, Germany
Tel. +49 2241 865 316
Marco.Jung@h-brs.de
https://www.h-brs.de

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Keywords

«Microgrid», «Grid-forming converter», «Plug and Play control», «Synchronization», «Droop Control»

Abstract

This paper demonstrates the potential of an enhanced grid-forming control for grid-forming converters, to optimize the interconnection process of black started microgrids (MG) after a global blackout. A point of common coupling switch (PCC switch) is proposed, which does not require any higher-level control entities (e.g. MG-controller) since the switching condition only considers phase angle differences, which enables the interconnection of unintended MGs. The verification of the grid-forming control for enhanced interconnection process with overlaid grid is performed by the presented simulation study.

1 Introduction

The increasing integration of distributed generation (DG) is leading to a progressive decentralization of the entire power grid structure. To ensure a secure power supply and stable grid operation in future grids, a trend towards increasing grid-forming capabilities of distributed inverters can be expected [1]. As grid-forming capabilities are increasingly used, inverters will be characterized as independent voltage phasors, contributing to the formation of the grid voltage for other grid participants. In addition to improved secure power supply, this also opens up potential for upcoming challenges such as new black start concepts after a blackout (e.g. [2, 3]). One approach for repowering future power grids is the build-down strategy [2], which aims to restore the power grid by successively synchronizing isolated and black-started low voltage MGs. To achieve this, connecting the local and individual black-started MGs to the medium voltage level (MV) is an essential step to successfully restore the entire power supply [4] (see Fig. 1). Without a supervised control instance, the MG voltage $\underline{U}_{MG}$ at the PCC is expected to deviate significantly from the nominal values, since considered droop controllers without secondary control instances do not force the frequency f_{MG} to its nominal value [5]. Following this reasoning, it is expected that the voltage amplitude of MG U_{MG} at the PCC (see Fig. 1) also have a significant deviation from the nominal amplitude, as without overlaid control, PCC voltage is not forced as a controlled variable. A typical way for MG synchronization is based on centralized microgrid-controllers (MG-C) located at the MV/LV substation [5]. With MG-C, a seamless interconnection can be achieved as the

MG voltage $\underline{U}_{MG}$ (amplitude, frequency, phase angle) is adjusted according to the utility voltage $\underline{U}_{util}$ in terms of synchronization [6]. After minimizing the MG voltage deviation to meet the switching condition of the PCC switch, the interconnection process is performed [4].

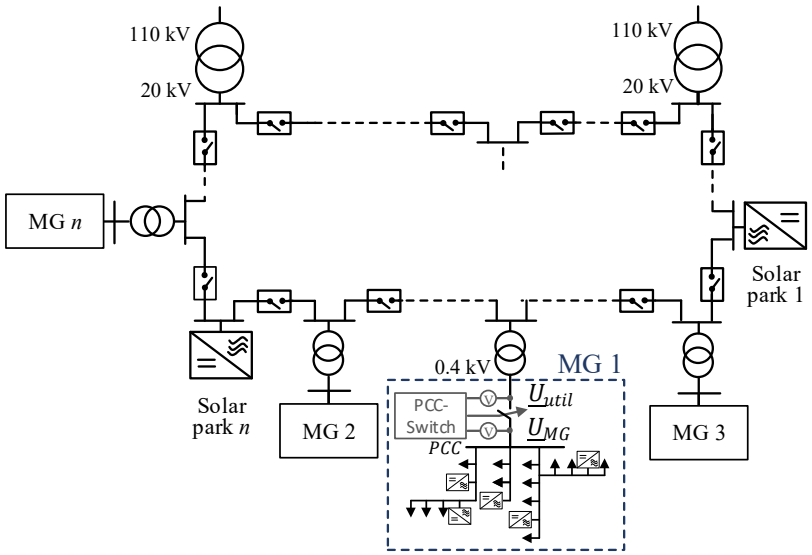

Fig. 1: Build-down strategy based on locally black-started MGs to restore the utility grid.

On the other hand, numerous methods for seamless MG synchronization based on additional or modified control loops within the inverter control can be found in [7, 8].
The paper investigates the connection of a MG to the utility grid with minimum requirements, based on the capabilities offered by grid-forming inverters with presented grid-forming control to handle the resulting dynamics during transients. For the interconnection process considered, only the phase angle deviation of the two grids is taken into account to satisfy the switching condition where all required voltages can measured locally at PCC switch. The synchronization approach does not require MG-C or specific modifications within the inverter control in the form of additional loops specifically designed for the synchronization process. Therefore, the proposed synchronization method can improve the interconnection of undedicated MGs after grid faults, since it does not require individual communication with specific grid participants.
A simulation model of a MG characterized with distributed generation is used to validate the grid-forming control in case of interconnection of MGs with two different grids. First, the interconnection of two MGs connected via MV grid is considered, which represents the first step for grid interconnection after a global blackout in a bottom up approach. Afterwards, the MG connection with stiff MV grid model shows the interconnection in an advanced state of grid restoration.

1.1 Role of Grid-Forming Control for Interconnection

Various grid-forming inverter control schemes have been recently reviewed and discussed [9–11]. The concept of grid-forming inverter control boils down to how the provided voltage phasor of the voltage source converter (VSC) is driven. In grid-forming inverter control, the voltage phasor is supposed to be autonomous in a sense, but still capable of synchronizing with other voltage sources. By imposing inertia on the voltage phasor, meaning that the voltage phasor reacts retarded to grid-side excitations, the provision of a momentary power reserve is inherent [12]. This so-called persistency can be considered in terms of both voltage amplitude and angle. In inductively coupled power grids, the angle persistency leads to an inherent active power provision and the amplitude persistency to an inherent reactive power flow [1].
This relation and the behavior of a grid-forming inverter can be deduced from a very simplified system (Fig. 2, Fig. 3): An inverter voltage $\underline{U}$ is connected to a grid voltage source $\underline{E}$ via an impedance $\underline{Z}$. Thereby the grid voltage source is a composition of several voltage sources, which together set up a more or less stiff voltage. The power flow from node 1 to 2 depending on the angle and amplitude difference of both voltage phasors forms the controlled system. The control task consists in guiding a

voltage phasor with retarded behavior, which is likewise well-damped and experiences a synchronizing torque.

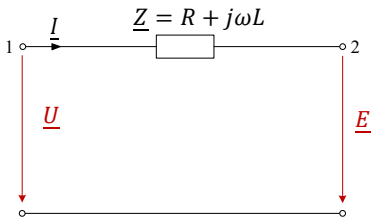

Fig. 2: Simplified equivalent circuit.

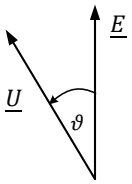

Fig. 3: Phasor diagram of two voltage sources.

The following section presents the study of grid-forming inverter model of MG interconnection.

2 Grid-Forming Inverter Model

Fig. 4 shows the model of a grid-forming inverter with LCL filter and the control instance. For the inverter, the following measurements are assumed: the inverter current I, the voltage at the output filter capacitor U_c as well as the measurement of the output voltage at the output terminal of the inverter U_o.

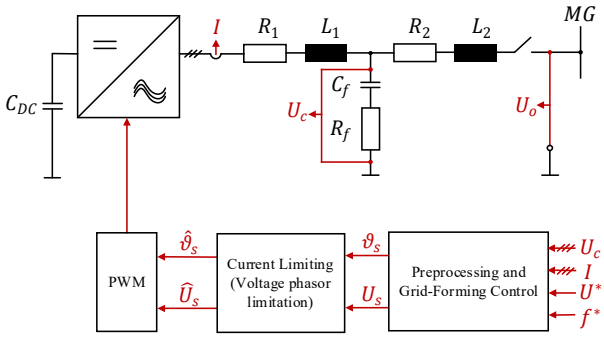

Fig. 4: Overview of grid-forming inverter model.

The grid-forming inverter control is introduced in the following section. For current limiting, a voltage phasor based current limiting is used based on the restriction of the amplitude $\hat{U}_s$ and the phase angle $\hat{\vartheta}_s$ of the provided voltage phasor of the grid-forming control for implicit current limiting. The current limiting will be published in [13].

2.1 Used Grid-Forming Control

The grid-forming inverter control used here, with provided voltage amplitude U_s as well as provided angle ϑ_s is illustrated in Fig. 5. Based on power droops (k_p, k_q) [1], it utilizes angle feedforward loops (k_q', k_p') for improved damping and synchronization [14].

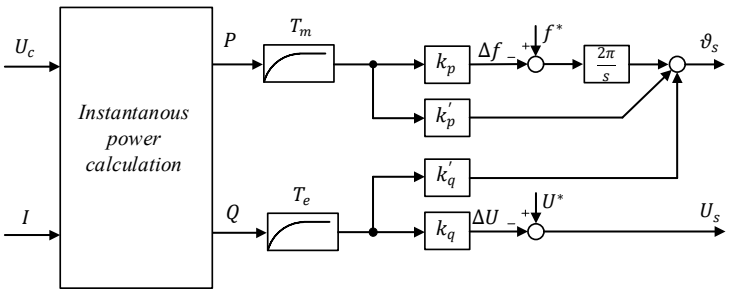

Fig. 5: Schema of the grid-forming inverter control [14].

This assists to align the interconnected grids during transient and reduce overshoot. Notable is the cross-coupling between the Q/U-loop and the phase angle ϑ_s. In this way, synchronization between several voltage sources in low-inductive grid applications can be improved in combination with reduced output filters with respect of high-frequency switching [15]. Furthermore, the grid-forming inverter is equipped with first-order delays with time constants T_m and T_e. With first-order delays, the grid-forming inverter is able to emulate virtual inertia and can therefore be dimensioned according to the time constants of a synchronous machine, for example (see [12]). In the following, a basic simulation model for validating the grid-forming control for the interconnection of MG and overlaid grid models is introduced.

3 System Scenario and Simulation Model

The following investigations are considering bottom-up approach to grid restoration of the overall grid after system blackout. The grid restoration is performed by interconnecting already black-started low voltage MGs (LV-MGs) (see Fig. 1) [2, 3], with appropriate concepts for individual black-start capability (see e.g. [3]). The process for interconnecting LV-MGs with the overlaid grid uses a simplified switching condition for the LV-PCC switch, which is introduced in section 3.2. The presented switching condition enables the interconnection of unintended MGs without the need for additional superior communication or MG-C.

3.1 Basic MG-Simulation Model

A LV-MG connected to an overlaid grid model through MV (see Fig. 6) is used to validate the interconnection process with simplified switching condition for the synchronization switch. Two different overlaid grid models (Grid model 1 and Grid model 2) are used to simulate different stages of the grid restoration process.

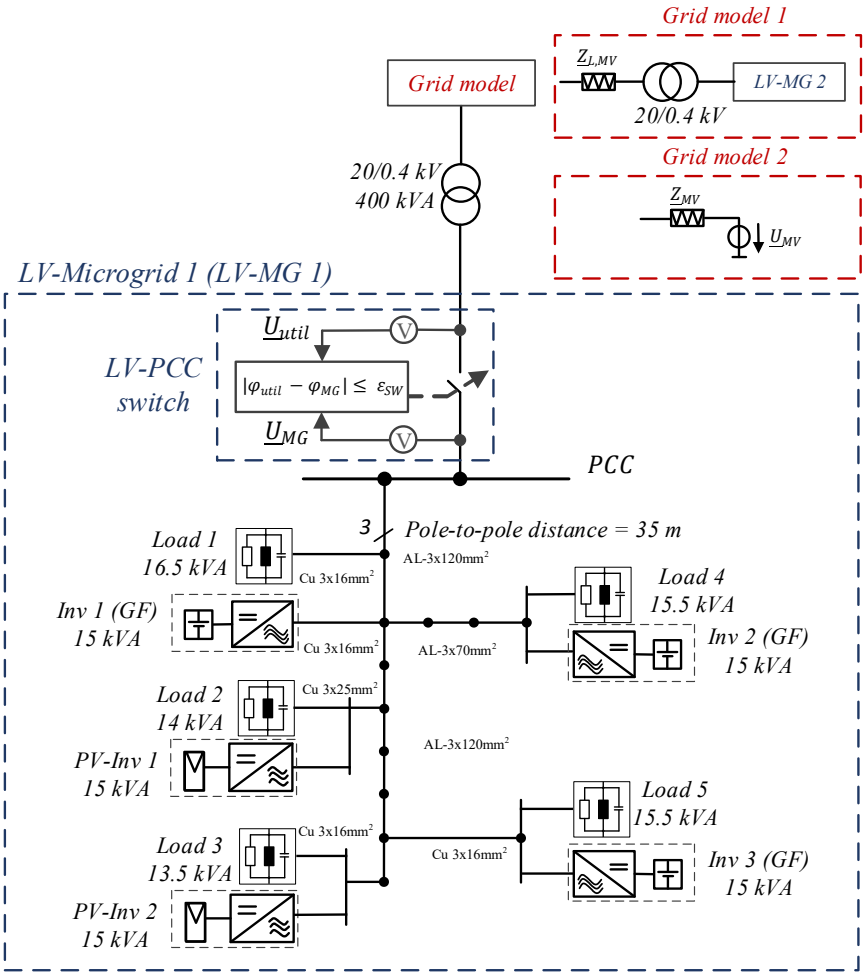

Fig. 6: Basic simulation model for interconnection of LV-MG 1 with overlaid grid-models, with LV-MG 1 defined based on [16].

The interconnection of LV-MG 1 and ”Grid model 1” represents the earliest stage in grid restoration process, in which two individual black-started MGs were interconnected via MV-level. In contrast, the connection of LV-MG 1 with “Grid model 2” represents a more advanced state in which various black-started and interconnected MGs form a stiff grid voltage $\underline{U}_{MV}$.

The simulation model of LV-MG 1 was defined in terms of a modified version of “Benchmark LV-Microgrid” presented in [16]. LV-MG 1 is mainly characterized by decentralized grid-forming battery inverters (Inv1 (Gf) - Inv3 (Gf)), which enable both islanded and grid-tied operation [17]. Furthermore, two grid-following PV inverters (PV-Inv 1- PV-Inv 2), one constant power load (Load 1) and four constant impedance loads (Load 2-5) are included. The two overlaid grid models for the interconnection process are introduced in section 4 and section 5.1. In the following, the model of the synchronization switch (LV-PCC switch) with the corresponding switching condition is presented.

3.2 Concept and Model of LV-PCC Switch

For the following considerations, MG voltage $\underline{U}_{MG}$ and utility grid voltage $\underline{U}_{util}$ are defined as follows: $\underline{U}_{MG} = U_{MG} \cdot e^{j(2\pi f_{MG}+\varphi_{MG})}$, $\underline{U}_{util} = U_{util} \cdot e^{j(2\pi f_{util}+\varphi_{util})}$. Conventional switching conditions aim at equal grid values of both grids (in terms of voltage amplitude, frequency and phase angle), which enables a seamless transition during interconnection process. However, seamless interconnection with the equal grid values requires overlaid control instances of the grid participants to adjust the grid voltage at the PCC.

This publication aims for interconnecting two grids with optimized switching condition to reduce the need for an overlaid control instances such as MG-C, which allows interconnection of unintended MGs with overlaid utility grid. Thus, refurbishing existing LV cells with additional MG-Cs for the ability to interconnect with the utility grid is not required.

The presented approach for PCC switches reduces the switching condition to equal phase angles of both grids, regardless of voltage and frequency deviations (see (1) for $\varepsilon_{sw} = 0$).

$$|\varphi_{util} - \varphi_{MG}| \leq \varepsilon_{SW} \tag{1}$$

The condition of equal phase angles can be repeatedly achieved without an overlaid control instance as long as frequencies of both grids are unequal, where the opportunity to satisfy the switching condition can be achieved every $1/(|f_{util} - f_{MG}|)$ seconds. In the following, a simulation model of the PCC switch with corresponding voltage measurements is introduced (see Fig. 7)

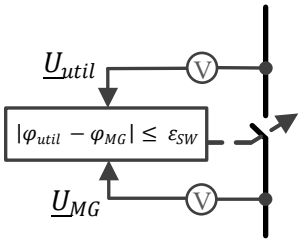

Fig. 7: Schema of synchronization switch.

Due to various delays, the phase angle difference $\Delta\varphi_{SW} = \varphi_{util} - \varphi_{MG}$ may not be equal to zero after the processor unit triggers the closing command. Fig. 8 shows the process from measuring the voltages to the closing process of the load switches. The voltage measurement usually delays the signal by about 10 µs. The time needed for the signal processing depends on the frequency of the processor and might be very small (~1 µs) when using a FPGA. The processor output is amplified using a bipolar transistor, for example, with a likewise negligible delay. However, the load contactor causes by far the largest time delay. The closing process is divided into the coil energization and the closing of contacts itself. The time for closing the load contacts varies in a wide range of several tens of milliseconds. Even if the delays are taken into account and compensated for earlier triggering of the load contactor, the tolerances for the closing time is in the range of milliseconds.

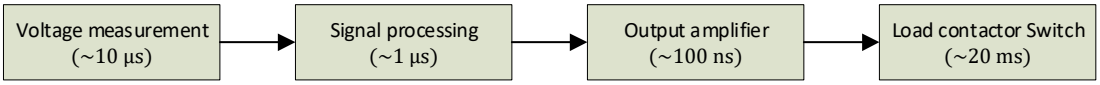

Fig. 8: Chain of delays.

In case the switch is triggered with equal phase angles of both grids according to (1), t_{delay} describes the resulting time for closing the physical load conductors at the switch. For unequal frequencies of both grids, the delay causes a phase angle difference according to (2) at the time of closing the load contactor.

$$\Delta\varphi_{SW} = \left|t_{\mathrm{delay}}(f_{\mathrm{util}} - f_{\mathrm{MG}}) \cdot 360°\right| \tag{2}$$

In the following, a frequency difference of 2.5 Hz is assumed, which is justified in section 4. For the delay time t_{delay}, various data sheets of circuit breakers were evaluated. The closing time varies in a wide range depending on the power category and nominal voltage. In the following, the automatic circuit breaker specified in [18] is assumed. The maximum closing time is specified as 80 ms. This results at 2.5 Hz with (2) with a phase difference $\Delta\varphi_{SW} = 72°$. Furthermore, a smaller delay time of 20 ms ($\Delta\varphi_{SW} = 18°$) is considered, since the closing time can be compensated, so that this only represents the component tolerances. The following section investigates the interconnection process of LV-MG 1 with Grid-model 1 based on Fig. 6.

4 Simulation Analysis 1 – Interconnection of two MG's

The first simulation analysis focuses on the first instance of grid restoration, where two individual black started MGs were interconnected (see Fig. 10 for interconnection of LV-MG 1 and LV-MG 2).
Since the grid-forming inverters used are equipped with active and reactive power droops (see Fig. 5) without superior control instance, the power flow of grid-forming inverters is linked to frequency and voltage deviation (see Fig. 9) [1].

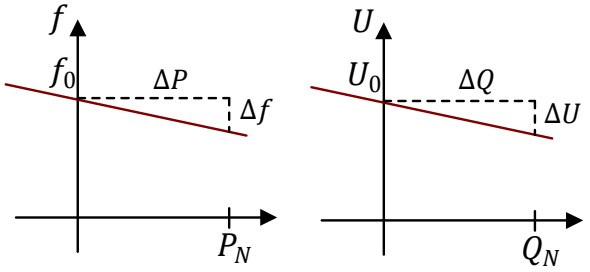

Fig. 9: Active and reactive power droops.

The droop coefficients k_p and k_q are dimensioned with a slope of $k_p = \Delta f / P_N$ and $k_p = \Delta U / Q_N$ which leads to maximum active power flow of P_N at a frequency deviation of $\Delta f = \pm 2.5\ Hz$ and a maximum reactive power flow Q_N at a voltage difference of $\Delta U = \pm 0.2 \cdot U_N$.
The operation points of both voltages $\underline{U}_{MG,1}$ and $\underline{U}_{util,1}$ before interconnection are chosen according to Table I. The specific frequency and voltage deviation between both grids can be realized by proper dimensioning of the loads and set points for the PV inverters in both MGs.

Table I: Operation points for MG interconnection

LV-MG 1 Voltage	Utility Voltage at PCC Switch 1	Differences
$U_{MG,1} = 0.85\ pu$	$U_{util,1} = 1.05\ pu$	$\Delta U = 0.2\ pu$
$f_{MG,1} = 48\ Hz$	$f_{util,1} = 50.5\ Hz$	$\Delta f = 2.5\ Hz$

With the definition of the operation points according to Table I, MG 1 is in a state where grid-forming inverters supply loads together with PV inverters, resulting in frequency and voltage deviation at the PCC that are smaller than nominal values ($f_{MG,1} < f_N, U_{MG,1} < U_N$). In contrast, LV-MG 2 represents a scenario where PV generation exceeds load demand, resulting in battery charging of the grid-forming inverters and voltage and frequency difference at LV-PCC switch 1 that are higher than the nominal values ($f_{util,1} < f_N, U_{util,1} < U_N$). The used grid-forming inverter models are equipped with grid-forming control (see Fig. 5) and current limiting based on [13].
Before interconnecting LV MG 1 and LV MG 2 at LV-PCC switch 1, it is assumed that MV has already been energized by LV-MG 2 (see closed LV-PCC switch 2 in Fig. 10).

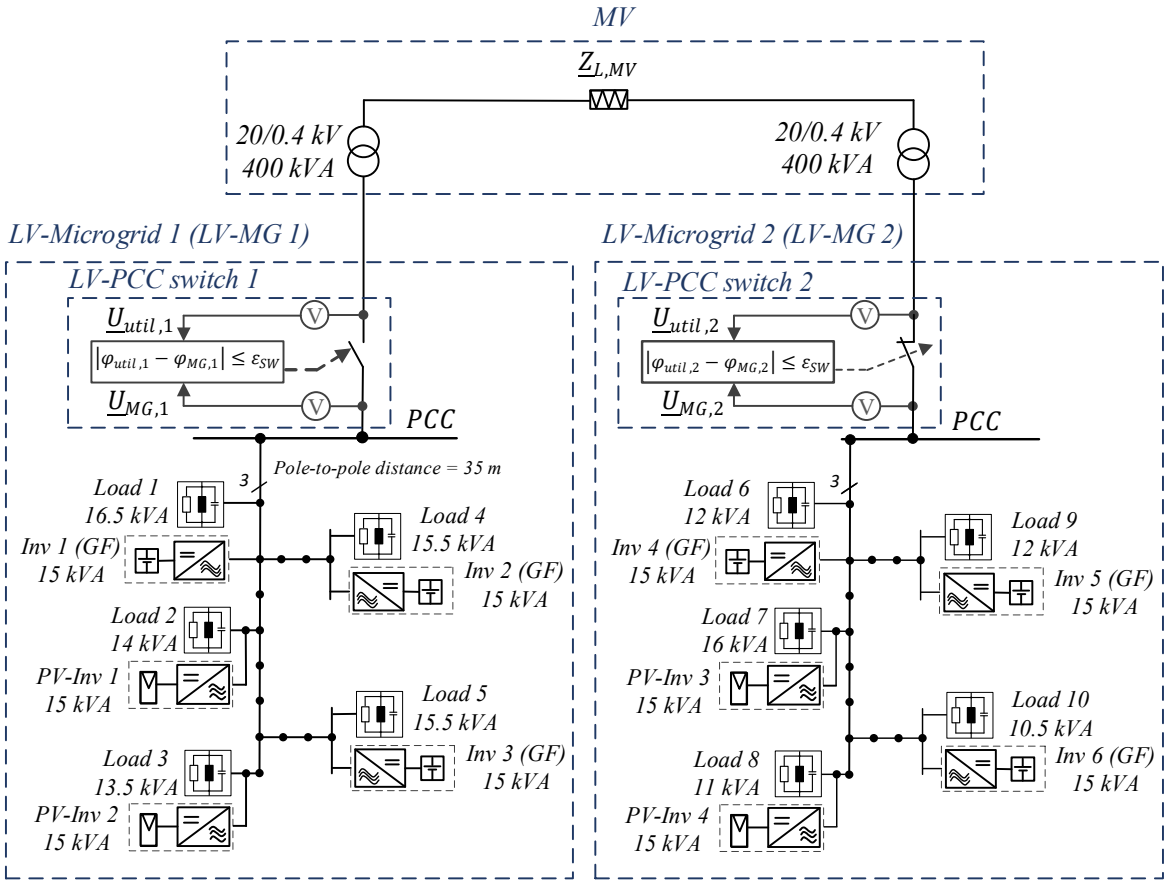

Fig. 10: Interconnection of two MGs (based on Fig. 6) as earliest stage of black start sequence.

With the definition of operation points according to Table I, both grids are interconnected with significant amplitude and frequency deviations before switching.
Fig. 11-Fig. 13 shows the inverter current of Inv 1 (GF) of LV-MG 1 at interconnection for different phase angle differences $\Delta\varphi_{SW}$ at LV-PCC switch 1, according to section 3.2. For the evaluation of the synchronization behavior, the voltage amplitude $U_{util,1}$ of the utility grid 1 is compared with the output voltage $U_{inv,1}$ (referred as U_o in Fig. 4) of Inv 1 (GF). In addition, considering the phase angle difference $\Delta\varphi = \varphi_{util,1} - \hat{\vartheta}_s$ of the internal phase angle set point $\hat{\vartheta}_s$ of inverter 1 (see Fig. 5) and the phase angle $\varphi_{util,1}$ of the three phase voltage $\underline{U}_{util,1}$ at LV-PCC switch 1 (see Fig. 10) serves as an indicator of the synchronization behavior after a dynamic event.
Before synchronization ($t < 50\,ms$), the grid-forming inverters supply the maximum current to the loads (see $I_{Inv1}(GF)$ in Fig. 11, Fig. 12 and Fig. 13), resulting in an overall frequency and amplitude deviation of the voltages, as shown in Table I. Overall, the presented grid-forming control and in case of idealized switching[1] ($\Delta\varphi_{SW} = 0$) as well as switching with common phase angle difference ($\Delta\varphi_{SW} =$

[1] Phase angle difference $\Delta\varphi = \varphi_{util,1} - \hat{\vartheta}_s$ shown in Fig. 11 is an indicator for synchronization between the grid-forming inverters of both MGs. The switching condition of the PCC switch can not be seen in Fig. 11, as it is defined according to (1), based on phase angle of utility grid $\varphi_{util,1}$ and phase angle of LV-MG 1 $\varphi_{MG,1}$ at LV-PCC switch 1.

18°), fast synchronization with well damped behavior after interconnection at $t = 50\,ms$ can be achieved. In addition, over current operation can be prevented due to the used current limiting method. After synchronization, both grids approach the new operation point according to the dynamic of the grid-forming control (See Fig. 11 and Fig. 12). Fig. 13 shows an interconnection with a maximum phase angle difference of $\Delta\varphi_{SW} = 72°$, where the maximum overshoot of the inverter current is limited to 1.3 pu by an additional fast reacting pulse break (see current peak of $I_{Inv1}(GF)$ at 50 ms). In addition, the switching operation causes a voltage drop in both grids to 0.5 pu.

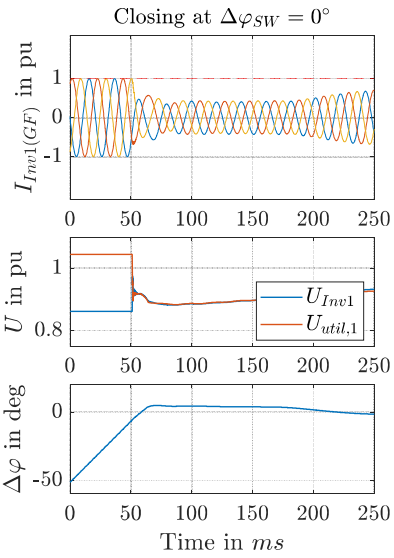

Fig. 11: Inverter current $I_{Inv1(GF)}$, voltage amplitude and phase angle difference for ideal interconnection ($\Delta\varphi_{SW} = 0°$).

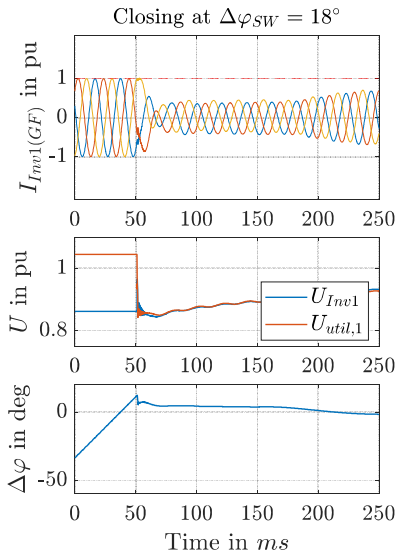

Fig. 12: Inverter current $I_{Inv1(GF)}$, voltage amplitude and phase angle difference for interconnection with $\Delta\varphi_{SW} = 18°$.

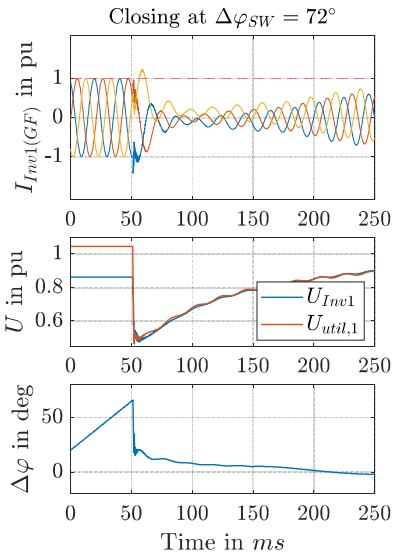

Fig. 13: Inverter current $I_{Inv1(GF)}$, voltage amplitude and phase angle difference for interconnection with $\Delta\varphi_{SW} = 72°$.

Depending on the operation time and the depth of the voltage drop, a fault condition (e.g. FRT-state - Fault ride through) of the inverters may occur during the interconnection for relatively high phase angle delays (see e.g. [19]). After interconnection, synchronization of the two grids depending on the characteristic of the grid-forming control takes place.
Overall, with the grid-forming control and the phase angle difference of LV-PCC switch with $\varphi_{SW} = 18°$ at switching, the interconnection of two MGs can be achieved without violating existing current and voltage limits for normal operation of grid-forming inverters. For switches with higher time delays (see e.g. $\Delta\varphi_{SW} = 72°$), delay compensation methods are proposed to avoid undesirable grid states for voltage amplitude and frequency. The next analysis focuses on interconnection of MG with stiff utility grid.

5 Simulation Analysis 2 – Interconnection of MG and Utility Grid Model

The second analysis focuses on the interconnection of LV-MG 1 with a simplified MV model (see "Grid model 2" in Fig. 6). The consideration of the MV model represents an advanced state in grid restoration process for the bottom-up approach, where the stiff utility voltage is formed as a composition of several black-started and interconnected MGs.

5.1 Equivalent MV Model

Fig. 14 shows an equivalent grid model consisting of an equivalent grid impedance $\underline{Z}_{MV}$ as well as an ideal MV voltage source with $\underline{U}_{MV}$.

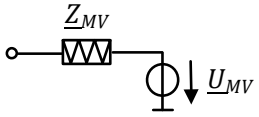

Fig. 14: Thévenin equivalent MV model.

The equivalent grid impedance can be calculated as in [20], depending on short circuit ratio $SCR = SCC/S_N$ [21], with the short circuit capacity SCC and the nominal power at the MV transformer S_N as shown in (3)

$$Z_{MV} = \frac{U_{MV}^2}{SCR \cdot S_N} = \frac{U_{MV}^2}{SCC} \tag{3}$$

SCC is chosen from [22] for MV grids with $U_{MV} = 20\ kV$ between 30 MVA for weak grids and 500 MVA for strong grids. As the strong grid model represents worst case consideration of the interconnection process due to the stiff voltage phasor characteristic of utility grid voltage, the equivalent grid impedance is calculated based on (3) to $Z_{MV} = (20\ kV)^2/500\ MVA = 0.8\ \Omega$. Finally, the equivalent resistance R_{MV} and the equivalent reactance X_{MV} can be calculated as in (4) and (5) [20], with a corresponding short circuit angle of $\Psi_{SC} = 85°$ for a strong MV grid based on [22].

$$R_{MV} = Z_{MV} \cdot \cos \Psi_{SC} = 69.7\ m\Omega \tag{4}$$

$$X_{MV} = Z_{MV} \cdot sin\, \Psi_{SC} = 797\ m\Omega \tag{5}$$

5.2 Simulation Analysis

In the following, the interconnection of LV MG 1 (see Fig. 6) and the equivalent MV model (Fig. 14) is analyzed. The operation points of both grids were chosen in the same way as in the previous simulation study according to Table I.

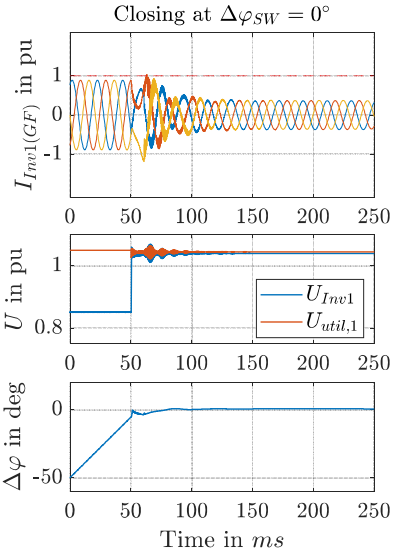

Fig. 15: Inverter current $I_{Inv1(GF)}$, voltage amplitude and phase angle difference for ideal interconnection ($\Delta\varphi_{SW} = 0°$).

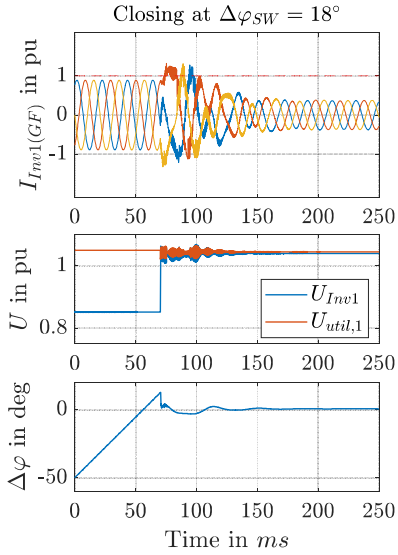

Fig. 16: Inverter current $I_{Inv1(GF)}$, voltage amplitude and phase angle difference for interconnection with $\Delta\varphi_{SW} = 18°$.

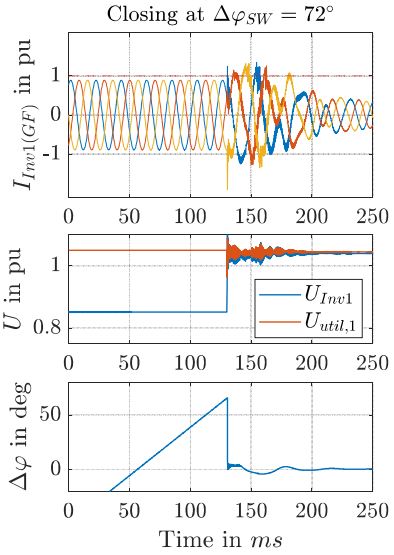

Fig. 17: Inverter current $I_{Inv1(GF)}$, voltage amplitude and phase angle difference for interconnection with $\Delta\varphi_{SW} = 72°$.

Again, the inverter current of $I_{inv1}(GF)$ serves as an indicator of the overall supply to the loads in LV-MG 1 before interconnection, as all grid-forming inverters are equipped with the same droop slope for equivalent active power sharing. For switching with idealized phase angle difference $\Delta\varphi_{SW} = 0$ at LV-PCC switch (see Fig. 15), the interconnection can be achieved with slight noncritical overcurrent, followed by synchronization process of the both grids within around 50 ms (see $\Delta\varphi$ in Fig. 15). Furthermore, the transient response of the inverter leads in high frequency oscillations due to excitation of output filter resonances.

Fig. 16 shows the influence of $\Delta\varphi_{SW} = 18°$ phase angle difference leading to noncritical short-term maximum overcurrent of 1.05 pu as well as a settling time of around 50 ms with additive harmonic oscillations due to filter resonances.

In case of a phase angle difference of $\Delta\varphi_{SW} = 72°$ (see Fig. 17), an additional pulse break [23] of the inverter is activated (see Fig. 17 at $t = 125\ ms$) to avoid undesired overcurrent operation. Furthermore, the settling time of system response increases to 125 ms after the dynamic event.
Overall, in the scope of this simulation analysis, interconnection with simplified switching conditions, combined with appropriate control and current limiting for grid-forming inverters, allows enhanced interconnection of MGs with overlaid grids under consideration of realistic phase angle difference.

6 Conclusion

The potential of the presented grid-forming control and current limitation for successful MG interconnection with minimized switching condition for the PCC switch was demonstrated. The proposed switching condition is based only on the phase angle deviation of both grids. With the presented grid-forming control and the example phase angle deviation of 18°, successful resynchronization could be achieved without violating voltage and frequency limits for interconnection of two MGs as well as interconnection of MG in an advanced grid-restoration process. It is proposed to use delay compensation methods for synchronization switches with significant switching delays (e.g. 72°). Further investigations to verify the presented interconnection approach in a laboratory MG test setup according to [14] are planned.

7 References

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