11th International Conference on Power Electronics-ECCE Asia
May 22 - 25, 2023 / ICC Jeju, Jeju, Korea

Degradation Diagnosis During Active Power Cycling via Frequency-Domain Thermal Impedance Spectroscopy

Sven Kalker
Institute for Power Electronics and Electrical Drives
RWTH Aachen University
Aachen, Germany
orcid.org/0000-0002-2698-6029

Johannes Holz
Institute for Structural Durability and System Reliability
Fraunhofer-Gesellschaft
Darmstadt, Germany
orcid.org/0009-0000-7136-5953

Isabel Austrup
Institute for Power Electronics and Electrical Drives
RWTH Aachen University
Aachen, Germany
orcid.org/0009-0001-9704-1014

Rik W. De Doncker
Institute for Power Electronics and Electrical Drives
RWTH Aachen University
Aachen, Germany
orcid.org/0000-0001-6953-3858

***Abstract*—The increasing reliability requirements of power electronic components demands for a better understanding of their application-dependent aging progression. Active power cycling is a commonly used accelerated-aging method for invoking degradation effects in the thermal path of power devices. For aging diagnosis during power cycling, usually step-response thermal impedance spectroscopy is applied utilizing a temperature-sensitive parameter for thermal sensing. This approach has multiple limitations: Degradation detection close to the power semiconductor is limited since the load step over-proportionally excites low-frequency components. The temperature-sensitive parameter is by itself prone to aging, leading to reduced accuracy or necessitates repeated calibration. To overcome these limitations, this paper proposes online thermal impedance spectroscopy in frequency domain for aging diagnosis during active power cycling. By doing so, aging effects in the thermal path can be detected and localized more robustly and with higher accuracy without testing interruption. Furthermore, by using a near-chip NTC sensor for thermal sensing, calibration effort can be reduced significantly. This paper evaluates the online thermal impedance spectroscopy using data from the active power cycling of an IGBT lead-frame power module with a near-chip NTC.**

***Index Terms*—active thermal cycling, degradation diagnosis, monitoring, impedance spectroscopy, NTC**

I. Introduction

The use of power electronics in safety-critical applications, such as electric vehicles and aerospace, as well as in high-maintenance applications, such as offshore wind farms, places high demands on component reliability requirements [1]. To increase reliability and select appropriate maintenance timing [2], there must be a good understanding of the aging behavior of devices prior to operation. In order to be able to emulate stress encountered in the later application in a shorter time, accelerated aging tests are carried out. One of these tests is active power cycling, which induces thermomechanical stresses by device self-heating that are often particularly critical to aging in the device under test (DUT). Thermal impedance is extracted to monitor aging during power cycling, particularly of the thermal path between the semiconductor and the heat sink. This is usually done by performing thermal impedance spectroscopy in the time domain by extracting the temperature response to a defined load step [3]–[5]. For temperature response extraction often a temperature-sensitive electrical parameter (TSEP), such as the semiconductor forward voltage, is used. This method of aging diagnosis has several limitations:
1) A load step excites over-proportionately low frequency components. This limits the ability to detect aging effects near the semiconductors because they are reflected in the higher frequency range of the thermal impedance [6].
2) While TSEPs offer a high bandwidth [7], [8] that is advantageous for impedance spectroscopy, their extraction is typically complex and susceptible to aging effects, such as gate oxide degradation [9]. Unless the TSEP is calibrated regularly, aging leads to increasing measurement error as the operating lifetime progresses.

To overcome these limitations, this paper proposes the use of frequency-domain thermal impedance spectroscopy for aging diagnosis during power cycling tests. The thermal impedance at relevant frequencies is determined by modulating the gate-emitter voltage and extracting temperature response using a near-chip NTC sensor [10]. By excitation at different frequencies, aging phenomena in the thermal path can be determined and localized up to chip level. For this degradation diagnosis, the phase information of the thermal impedance is used, since it is significantly more robust compared to magnitude information due to estimation errors of the loss model [11]–[13]

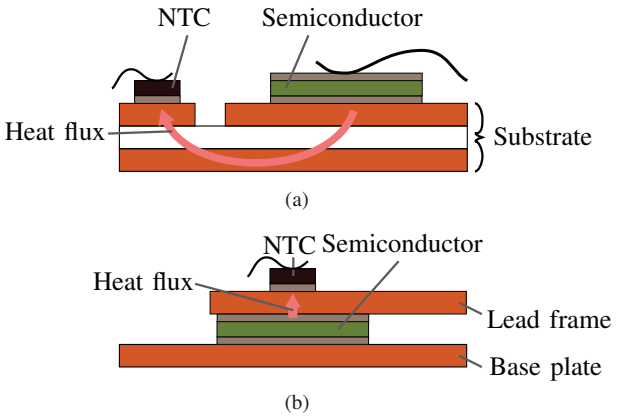


Fig. 1: Schematic representation of the thermal coupling of an NTC thermistor to a power semiconductor (a) in a regular bond-wire module and (b) in a lead-frame module

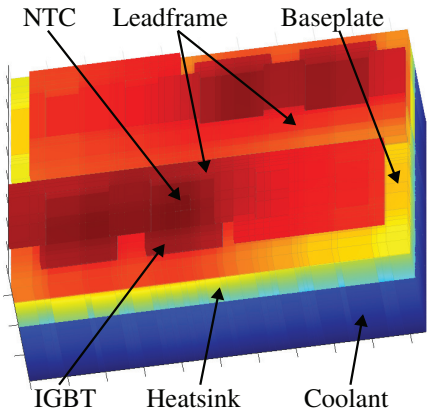


Fig. 2: Representation of the 3D temperature distribution of the considered lead-frame power module for an exemplary operating point

and inaccuracies of the temperature measurement. Another advantage of the diagnostic method is that it can be performed online during power cycling without interruption. Last, by using a near-chip NTC, junction temperature determination becomes less complex and more robust, and the calibration effort is reduced.

The use of online spectroscopy in the frequency domain to determine magnitude and phase of thermal impedance has already been identified in theory as a promising aging diagnosis approach [6], [14]. In [15], [16] it has already been shown that for aging diagnosis phase is preferable to magnitude of thermal impedance due to higher robustness to estimation and measurement inaccuracies. However, the feasibility of the method has not yet been investigated during aging progression, not in the context of accelerated aging testing and not by using a near-chip NTC.

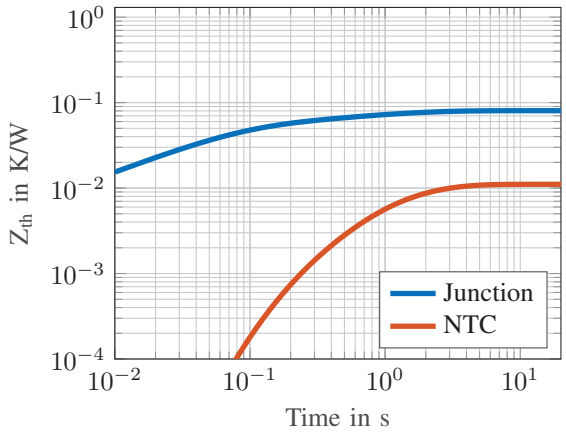
This paper compares the performance of a near-chip NTC sensor in lead-frame modules to common direct bonded copper (DBC) substrate-mounted physical sensors. Subsequently, the method used for thermal impedance determination is presented followed by evaluation using measurement results during active thermal cycling.

II. Near-Chip NTC in Lead-Frame Modules

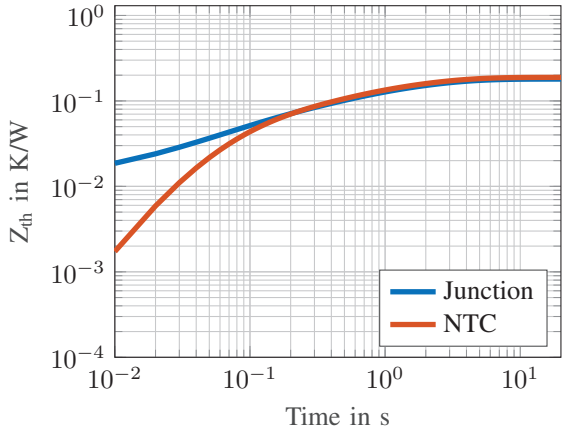
Especially for diagnosing thermally induced damage, a junction temperature measurement with sufficient bandwidth is required. In current bond-wire power modules, physical sensors, such as NTC or PTC, are placed on the DBC at a considerable distance from the switching semiconductors, as shown schematically in Fig. 1a. The thermal path from semiconductor to thermistor is primarily closed via the ceramic layer of the DBC substrate, which is a poor thermal conductor due to its insulating properties. This leads to an attenuation and delay of the thermistor's temperature response to the junction temperature of the semiconductor. To achieve higher bandwidths, temperature-sensitive electrical [8], [9] or optical [17], [18] parameters are applied due to their direct dependence on junction temperature. However, in addition to temperature, TSEPs and TSOPs are often affected by various other parasitic influences, such as device current, dc link voltage or ageing effects, which either affect the accuracy of the measurement or lead to a higher calibration effort, which is not the case to the same extent with physical sensors [19], [20]. Furthermore, the gate-driver integrated [21] temperature extraction via TSEPs is much more complex than the extraction via physical sensors due to low sensitivities, short extraction times or low signal to noise ratios [9].

As an alternative to bond-wire power modules with soft molding compound, modules with lead frame and hard molding compound are increasingly used. With these modules it is possible to place the thermistor on the lead frame directly above the semiconductors, as schematically shown in Fig. 1b. Here, the sensor is directly thermally coupled to the semiconductor via the lead frame, which massively reduces the attenuation and the delay of the temperature response compared to a thermistor in a bond-wire module. Although the bandwidth of the near-chip NTC is less than that of TSEPs, it is sufficient to be able to register aging phenomena even close to the switching semiconductor, as will be shown later.

In order to evaluate the performance of the near-chip NTC, a geometrically simplified 3-D finite volume model according to [3] of a Bosch PM4 B6 IGBT half-bridge lead-frame module is created. Figure 2 shows the model-based temperature distribution of the module for an exemplary operating point. In the following, the sensing performance of the near-chip NTC is evaluated by comparing the created thermal model of the Bosch lead-frame module with the thermal model created in [22] of an Infineon Hybridpack2 IGBT bond-wire module with DBC-placed NTC. Figure 3 shows the transient thermal impedance Z_{th} of the IGBT and the NTC, which results from the loss step response of one IGBT. For the bond-wire module in Fig. 3a, the strong attenuation and delay of the DBC-placed NTC is evident [22]. In contrast, it can be seen in Fig. 3b that the NTC in the lead-frame module can follow the junction

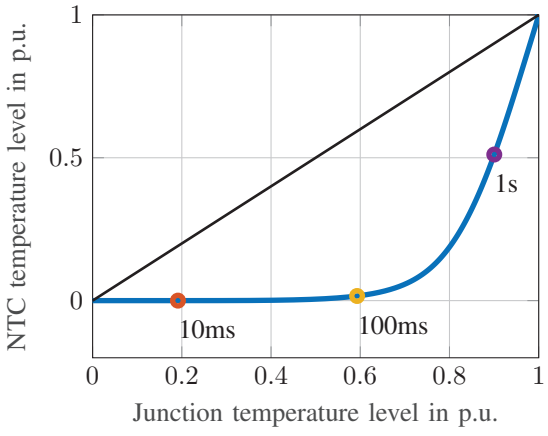


(a)

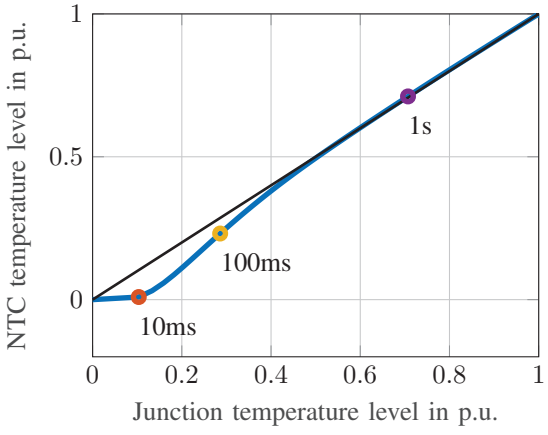


(b)

Fig. 3: Transient thermal impedance Z_{th} of the device and the NTC resulting from the loss step response of an IGBT for (a) a regular bond-wire module [22] and (b) a lead-frame module with near-chip NTC



(a)



(b)

Fig. 4: Relative normalized junction and NTC temperature values after a loss step excitation of the IGBT for (a) a regular bond-wire module [22] and (b) a lead-frame module with near-chip NTC

temperature of the IGBT much more dynamically and with less attenuation.

To further illustrate the performance advantage of the near-chip NTC, Fig. 4 compares the normalized junction and NTC temperature values after a loss-step excitation of the IGBT for both module types. For the DBC-placed thermistor in the bond-wire module in Fig. 4a, it can be seen that even after 1 s, the NTC temperature has not reached the junction temperature level of the IGBT [22]. The DBC-placed thermistor thus has a bandwidth well below 1 Hz, closer to 100 mHz. In comparison, it can be seen in Fig. 4b that the near-chip NTC in the lead-frame module responds much more dynamically. Shortly after 100 ms the NTC has reached the junction temperature level. Thus, the bandwidth of the chip-near NTC is close to 10 Hz.

The one to two decades higher bandwidth of the near-chip NTC compared to thermistors in bond-wire modules allows the diagnosis of thermally induced degradation phenomena even close to the semiconductor, which will be demonstrated in the following.

III. Online Thermal Impedance Spectroscopy in Frequency Domain

To determine thermal impedance in the frequency domain, the on-state gate-emitter voltage is superimposed with a small-signal sine wave of varying frequency to modulate conduction losses. By simultaneously extracting the junction temperature component of the same frequency, thermal impedance can be determined according to:

$$Z_{\mathrm{th}}(\mathrm{j}\omega) = \frac{\mathrm{T_J}(\mathrm{j}\omega)}{\mathrm{P}(\mathrm{j}\omega)}.$$

In this proposed method, only the phase of the thermal impedance $\angle Z_{\mathrm{th}}(\mathrm{j}\omega)$ is measured by determining the phase delay between gate-emitter voltage excitation and thermal response determined using the near-chip NTC:

$$\psi(\mathrm{j}\omega) = \angle\left(\frac{T_{\mathrm{NTC}}(\mathrm{j}\omega)}{V_{\mathrm{GE}}(\mathrm{j}\omega)}\right).$$

This is advantageous because the determination of the phase is more robust and accurate than determination of the magnitude

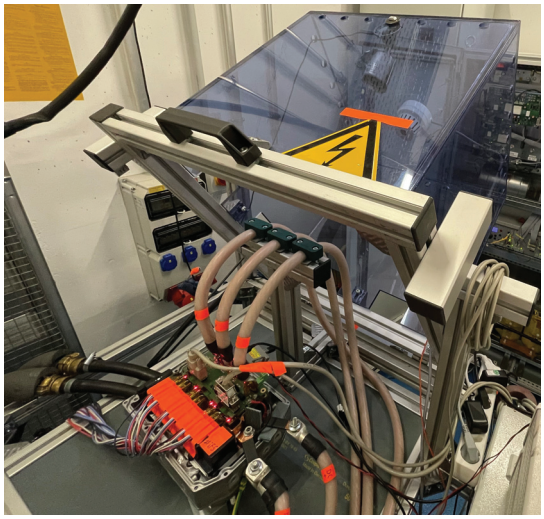


Fig. 5: Experimental setup for characterization and power cycling of the IGBT lead-frame power module and simultaneous measurement of gate-emitter voltage and temperature by means of the near-chip NTC

since no calibration of the loss and temperature data is necessary [15], [16]. Furthermore, the phase information is just as suitable for aging diagnostics as the magnitude of the thermal impedance [6].

To validate the method, a test bench was set up for characterization and accelerated aging of the Bosch lead-frame IGBT module, which can be seen in Fig. 5. The test bench used corresponds to a test bench of [23] adapted in terms of hardware and software. Two stacked circuit boards were designed to control the semiconductors, modulate and measure the gate-emitter voltage, evaluate the near-chip NTC and communicate the data to a test bench computer. Gate-emitter voltage adjustment and modulation were implemented by using a second-order filter connected between the gate driver and the semiconductor. The control of the gate voltage by actuating the gate driver was realized using a Texas Instrument C2000 microcontroller. The measurement of the gate voltage and the temperature via the near-chip NTC was performed by a galvanically isolated 16-bit ADC. The measurement data was continuously transferred to a test bench computer via a USB interface. The extraction of the temperature component at excitation frequency as well as the determination of the phase offset between gate voltage and temperature response were performed on the test bench computer. However, if required by the application, these calculations could also be implemented on the microcontroller.

The amplitude of the superimposed small-signal excitation of the gate-emitter voltage is $20\,\mathrm{mV}$. A frequency sweep was performed from $4.6\,\mathrm{mHz}$ to $10\,\mathrm{Hz}$ with five periods each. Using a Fast Fourier Transformation (FFT), the frequency components of the gate-emitter voltage and temperature at the excitation frequency are extracted and the phase delay is determined.

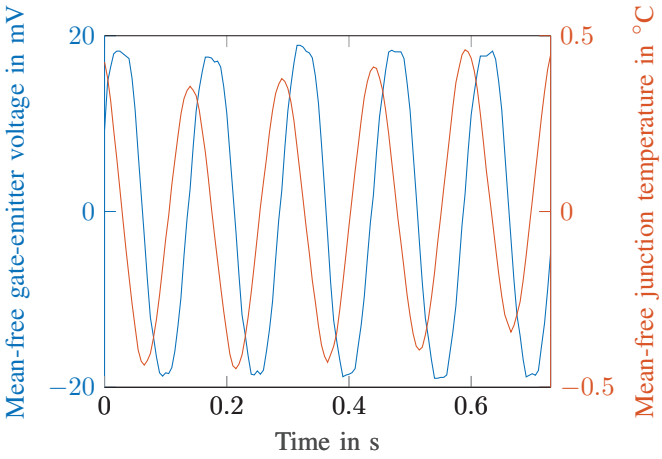


Fig. 6: Exemplary measurement extract of the mean-free gate-emitter voltage over five periods and temperature response for an excitation frequency of $6.8\,\mathrm{Hz}$

Figure 6 shows an exemplary measurement extract of the mean-free gate-emitter voltage and NTC temperature over five periods of the excitation frequency of $6.8\,\mathrm{Hz}$. The phase shift between excitation by the gate-emitter voltage and temperature response is evident. Since the conduction losses of the semiconductor decrease with rising gate-emitter voltage, the measured phase lag ψ is shifted $180°$ with respect to the phase of the thermal impedance:

$$\angle Z_{\mathrm{th}}(\mathrm{j}\omega) = \psi(\mathrm{j}\omega) - 180°.$$

IV. Degradation Diagnosis During Active Power Cycling

To evaluate the aging diagnosis of the proposed method, it was performed during the active power cycling of the semiconductors of the Bosch IGBT lead-frame module. For this purpose, the test setup from Fig. 5 was used. Since the near-chip NTC is placed above one of the two low-side IGBTs of the half-bridge module, only the low side was actively aged. A cycling frequency of $33\,\mathrm{mHz}$ with a heating time of $10\,\mathrm{s}$ was chosen. Since the continuous power of the test bench used was not sufficient to achieve the desired temperature cycling in the semiconductors, the dc component of the gate-emitter voltage had to be limited to approximately $7.5\,\mathrm{V}$.

A. Initial Characterization

At the beginning of the accelerated aging test, a full frequency sweep of the thermal impedance spectroscopy was performed during cycling with a temperature swing of $70\,\mathrm{K}$ and a cooling inlet temperature of $30\,°\mathrm{C}$. This determines the initial nearly-unaged state of the power semiconductors. Figure 7 shows the phase information extracted during this initial characterization as blue markers. No phase information could be extracted between approximately $10\,\mathrm{mHz}$ and $400\,\mathrm{mHz}$. In this frequency range, the excitation of the temperature by

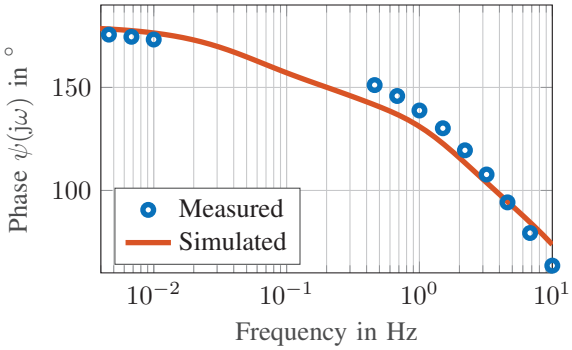


Fig. 7: Comparison between model-based simulated and measured phase information between gate-emitter voltage and junction temperature

the gate-emitter voltage cannot be clearly separated from the excitation by the active cycling. The simulated phase information using the generated 3D finite-volume thermal model is plotted in red in Fig. 7. The measured phase is in good approximation to the simulated results. It is assumed that the remaining deviations are due to inaccuracies in the estimation of material properties in the thermal model, manufacturing tolerances and measurement inaccuracies.

B. Degradation Sensitivity Analysis

Changes in the thermal path due to aging are reflected in a shift in the phase information of the thermal impedance. Depending on the localization of the aging damage, a different frequency range of the impedance is affected. Changes near the heat sink can usually be identified in low frequency ranges and changes near the semiconductor in the relatively higher frequency range [6]. The different influences of aging locations are determined simulatively using the generated 3D thermal model. Its results are shown in Fig. 8 as normalized phase changes. To emulate the degradation of the heat sink convection, the heat transfer coefficient was reduced by 10%. Furthermore, a 20% reduction in the thermal conductivity of each interface material was performed to mimic the aging of the thermal interface material (TIM), the bottom and top solder joints of the IGBT, as well as the solder joint of the NTC. As expected, the degradation of convection is reflected in the low frequency range and the semiconductor near aging effects in the relatively higher frequency range. While the change in convection and aging of the TIM material, are detectable below about 700 mHz and 10 Hz, respectively, the effect of the degradation of the solder joints close to the IGBT extends even past 10 Hz. However, all aging effects show a significant influence within the bandwidth of the near-chip NTC sensor of about 10 Hz and are thus detectable.

It is expected that during accelerated aging, a combination of several aging phenomena will occur in the thermal path. Thus, the actual phase change will be formed by a combination of the effects in Fig. 8.

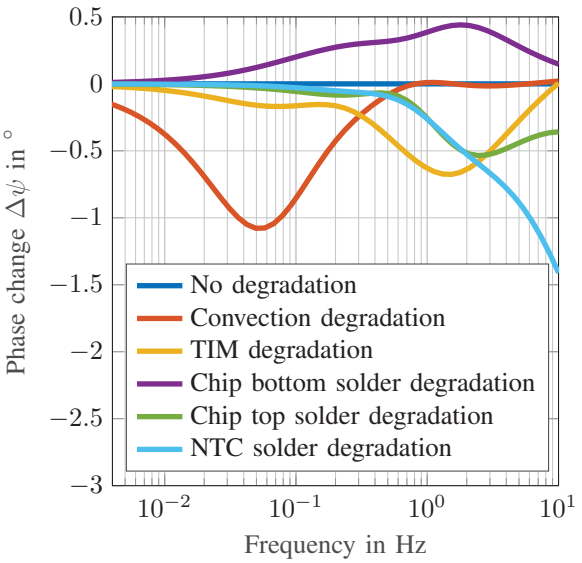


Fig. 8: Simulatively determined phase change normalized to the undegraded state caused by various aging effects in the thermal path of the semiconductor

C. Evaluation of Degradation Diagnosis

After the short cycling period with a temperature swing of 70 K to characterize the phase information as described in subsection IV-A, for 20 cycles a temperature swing of 110 K with a cooling inlet temperature of 10 °C was performed. This interim cycling with high temperature swings is intended to forcibly initiate aging processes that can further develop during the subsequent cycling with lower temperature swings. After this brief aging initiation, the accelerated aging test continued with a temperature swing of 70 K and an inlet temperature of 30 °C for 20,000 cycles. To further accelerate the aging processes, for the next 9,000 cycles the temperature swing of 70 K was increased to 80 K. At about 29,000 cycles, the IGBT under consideration was destroyed and the aging test was terminated.

Since conduction loss modulation via the gate-emitter voltage is only possible during the heating phase of the cycling, only these time periods were considered for the phase extraction. If not at least one period fits into the heating phase for an excitation frequency, i.e. $f_{\mathrm{ex}} < 100\,\mathrm{mHz}$, multiple cycling periods were analyzed together. To compensate for minor measurement variations, a moving median filter was applied to the extracted phase values.

Figure 9 shows the change in phase information $\Delta\psi(\mathrm{j}\omega)$ from the initial state determined in subsection IV-A. In addition to the initial state, the phase change after about 7,000, 15,000, 22,000 cycles and at the end of life of the IGBT at about 29,000 cycles is shown. As with the characterization in Fig. 7, the phase information between 10 mHz and 400 mHz cannot be extracted since the influence of the cycling on the temperature response prevents a precise extraction in this frequency range. A steadily increasing change in phase

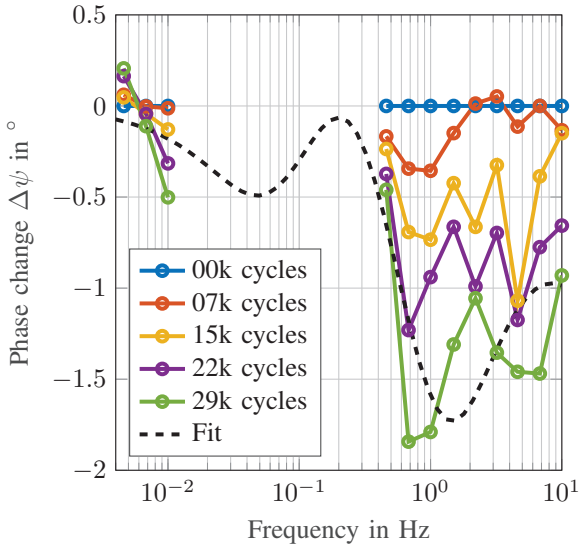


Fig. 9: Measured phase change for four aging states normalized to the undegraded state

information over the cycling is evident, especially in the frequency range between 460 mHz and 10 Hz. Detection of the aging progress of the thermal path of the IGBT is thus possible with the proposed thermal impedance spectroscopy in the frequency domain. However, it is not only of interest whether aging has taken place, but also where and to what extent it has occurred. For this purpose, the simulative sensitivity analysis of the phase information to various aging processes from subsection IV-B is used. By combining the simulative-determined phase influences of the aging processes, a good approximation of the measured phase change shall be achieved. Therefore, an optimization procedure based on the interior-point method was applied to find the best possible fit to the phase progression at 29,000 cycles in Fig. 9. For the fitness function, the root-mean-square error (RMSE) was applied. The result of the optimization can be seen in Fig. 9 as a dashed black line. A good approximation to the real phase change was achieved. Remaining deviations can be attributed to the limited number of considered aging processes as well as to modeling errors, e.g., due to incorrectly estimated material properties and manufacturing tolerances. Table I shows the aging parameters determined by the optimization. Here, mainly an aging-related change in the TIM material and in the bottom solder connection of the IGBT was detected. In order to validate the quantification and localization of the aging effects with the help of the optimization procedure, a metrological characterization of the aging phenomena, e.g., by cross-sectional cuts, must be carried out in the future. These investigations will be presented in a future publication.

V. Conclusion

This paper proposes the use of thermal impedance spectroscopy in frequency domain during active power cycling for aging diagnosis. Thermal impedance phase is determined by the phase offset between a sinusoidal loss excitation through small-signal modulation of the gate-emitter voltage and the corresponding temperature response. It has been shown that near-chip NTCs in lead-frame power modules are particularly suitable for this application because they have a significantly higher bandwidth than conventional module-integrated thermal sensors. Furthermore, the extraction of the NTC is more robust and less complex than for TSEPs. The method was evaluated using an active power cycling test of a Bosch IGBT half-bridge module. By comparing the measured phase information with the simulation results of a specifically generated 3D thermal model, the functionality of the method was proven. Furthermore, it could be shown that aging phenomena during power cycling can be detected and localized by the method even close to the semiconductor.

TABLE I: Quantification and localization of aging effects in the thermal path

Location of degradation	Change
Convection	1.1 %
TIM	61.9 %
Chip bottom solder	48.4 %
Chip top solder	13.8 %
NTC solder	10 %

Acknowledgment

The authors would like to thank the Institute for Power Electronics and Electrical Drives (ISEA) at RWTH Aachen University as well as the Institute for Structural Durability and System Reliability (LBF) of Fraunhofer-Gesellschaft for supporting this research. This research was funded by the German Federal Ministry of Education and Research (BMBF) within the project ZuLeSELF funded according to a resolution of the German Federal Parliament (BMBF, Support Code 16EMO0324).

References

[1] N. Baker, M. Liserre, L. Dupont, and Y. Avenas, "Improved reliability of power modules: A review of online junction temperature measurement methods," *IEEE Industrial Electronics Magazine*, vol. 8, no. 3, pp. 17–27, 2014.

[2] C. H. Van der Broeck, S. Kalker, and R. W. De Doncker, "Intelligent monitoring and maintenance technology for next generation power electronic systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, pp. 1–1, 2021.

[3] A. Henlser, D. Wingert, C. Herold, J. Lutz, and M. Thoben, "Thermal impedance spectroscopy of power modules during power cycling," in *2011 IEEE 23rd International Symposium on Power Semiconductor Devices and ICs*, 2011, pp. 264–267.

[4] U.-M. Choi, F. Blaabjerg, and S. Jørgensen, "Power cycling test methods for reliability assessment of power device modules in respect to temperature stress," *IEEE Transactions on Power Electronics*, vol. 33, no. 3, pp. 2531–2551, 2018.

[5] A. Hensler, D. Wingert, C. Herold, J. Lutz, and M. Thoben, "Thermal impedance spectroscopy of power modules," *Microelectronics Reliability*, vol. 51, no. 9-11, pp. 1679–1683, 2011.

[6] C. H. van der Broeck, T. A. Polom, R. D. Lorenz, and R. W. De Doncker, "Real-time monitoring of thermal response and life-time varying parameters in power modules," *IEEE Transactions on Industry Applications*, vol. 56, no. 5, pp. 5279–5291, 2020.

[7] N. Baker, S. Munk-Nielsen, F. Iannuzzo, and M. Liserre, "Igbt junction temperature measurement via peak gate current," *IEEE Transactions on Power Electronics*, vol. 31, no. 5, pp. 3784–3793, 2016.
[8] Y. Avenas, L. Dupont, and Z. Khatir, "Temperature measurement of power semiconductor devices by thermo-sensitive electrical parameters—a review," *IEEE Transactions on Power Electronics*, vol. 27, no. 6, pp. 3081–3092, 2012.
[9] S. Kalker, L. A. Ruppert, C. H. van der Broeck, J. Kuprat, M. Andresen, T. A. Polom, M. Liserre, and R. W. De Doncker, "Reviewing thermal-monitoring techniques for smart power modules," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, no. 2, pp. 1326–1341, 2022.
[10] E. Ogawa, T. Nakayama, S. Yoshida, S. Takenoiri, S. Ewald, and M. Otsuki, "Ultra-high accuracy on-chip temperature sensor in rc-igbt module for xev," in *PCIM Europe 2019; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2019, pp. 1–4.
[11] K. Ammous, H. Morel, and A. Ammous, "Analysis of power switching losses accounting probe modeling," *IEEE Transactions on Instrumentation and Measurement*, vol. 59, no. 12, pp. 3218–3226, 2010.
[12] A. P. Arribas, M. Krishnamurthy, and K. Shenai, "Accurate characterization of switching losses in high-speed, high-voltage power mosfets," in *2015 IEEE International Workshop on Integrated Power Packaging (IWIPP)*, 2015, pp. 95–98.
[13] S. Kalker, D. Meier, C. H. van der Broeck, and R. W. De Doncker, "Self-calibrating loss models for real-time monitoring of power modules based on artificial neural networks," in *2022 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2022, pp. 1–8.
[14] C. H. van der Broeck, S. Kalker, T. A. Polom, R. D. Lorenz, and R. W. De Doncker, "In-situ thermal impedance spectroscopy of power electronic modules for localized degradation identification," in *PCIM Europe 2019; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2019, pp. 1–8.
[15] T. A. Polom, C. H. van der Broeck, R. W. De Doncker, and R. D. Lorenz, "Exploiting distinct thermal response properties for power semiconductor module health monitoring," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 4, pp. 4865–4878, 2021.
[16] I. Austrup, C. H. van der Broeck, T. B. Albert, S. Kalker, and R. W. de Doncker, "Diagnosing degradation in power modules using phase delay changes of electrical response," in *2022 IEEE 7th Southern Power Electronics Conference (SPEC)*, 2022, pp. 1–6.
[17] S. Kalker, C. H. van der Broeck, L. A. Ruppert, and R. W. De Doncker, "Next generation monitoring of sic mosfets via spectral electroluminescence sensing," *IEEE Transactions on Industry Applications*, vol. 57, no. 3, pp. 2746–2757, 2021.
[18] L. A. Ruppert, S. Kalker, and R. W. De Doncker, "Junction-temperature sensing of paralleled sic mosfets utilizing temperature sensitive optical parameters," in *2021 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2021, pp. 5597–5604.
[19] D. Herwig, T. Brockhage, and A. Mertens, "Impact of parasitics in power modules and gate drivers on tsep-based temperature estimations," in *2020 23rd International Conference on Electrical Machines and Systems (ICEMS)*, 2020, pp. 804–809.
[20] L. A. Ruppert, S. Kalker, C. H. van der Broeck, and R. W. De Doncker, "Analyzing spectral electroluminescence sensitivities of sic mosfets and their impact on power device monitoring," in *PCIM Europe digital days 2021; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2021, pp. 1–8.
[21] J. Henn, C. Lüdecke, M. Laumen, S. Beushausen, S. Kalker, C. H. v. d. Broeck, G. Engelmann, and R. W. d. Doncker, "Intelligent gate drivers for future power converters," *IEEE Transactions on Power Electronics*, vol. 37, no. 3, pp. 3484–3503, 2022.
[22] C. H. van der Broeck and R. W. De Doncker, "Thermal monitoring of power electronic modules with minimal sensing effort," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019, pp. 5989–5996.
[23] C. v. d. Broeck, H. Zeng, R. D. Lorenz, and R. W. d. Doncker, "A test bench for thermal characterization of igbt power modules over mission profiles," in *PCIM Europe 2018; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2018, pp. 1–8.