Current Distribution Control in Parallel Connected Power Converters with Continuous Output Voltage

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Keywords

≪Paralleling≫, ≪Current sharing≫, ≪Converter control≫, ≪Inverter design≫, ≪Gallium Nitride (GaN)≫.

Abstract

This contribution presents a hardware-based current distribution control concept of parallel connected power converters with quasi-continuous output voltage as part of a scalable and modular power electronic system for motor control using wide bandgap semiconductors.

Introduction

The increased switching frequency of wide bandgap semiconductor switches leads to new hardware concepts for motor control. It enables the integration of filters into the power electronics to provide quasi-continuous voltages to a load thus avoiding the drawbacks of pulsed output voltages applied to motor terminals. Typically, LC filters are used to produce the quasi-continuous voltage at the terminals. However, such filter structure topologies exhibit a poor damping. This issue can be addressed by a dissipative damping as proposed in [1]. A more efficient and flexible alternative is to shape the filter transfer characteristic by a state feedback of the measured capacitor current [2] or the filter inductor current [3].

The sustainability of much higher switching frequencies also simplifies modular concepts. Power modules with continuous output quantities can be easily connected in parallel and/or in series to extend the current and/or voltage range to deal with the high power requirement and thus reducing the stress on the switches. For the connection of several power modules in parallel, several design objectives, such as equal current sharing, have to be considered. To ensure symmetric current sharing between the parallel power modules, different structures have been proposed. In [4] a comprehensive review based on a comparative analysis of current sharing control strategies of parallel-connected inverters modules is presented.

The active current distribution control can be divided into instantaneous average current sharing (IACS) control [5], master-slave control (MSC) [6] and circular chain control (3C) method [7]. In the MSC

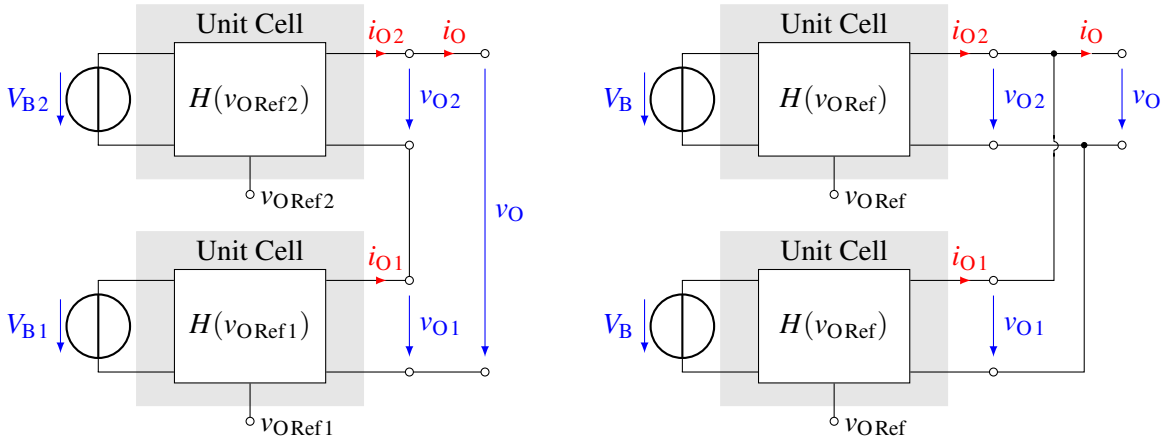
technique one power module is chosen as master acquiring voltage control mode while the remaining modules are selected as slaves embracing current control mode.

The current paper extends the idea for the parallel connection of power electronic modules from [8] and proposes a hardware-based current sharing control strategy for power modules connected in parallel such that a sufficient damping is ensured [3] and the motor current is equally distributed among the parallelized modules. In this contribution MSC is implemented. In contrast to conventional methods each power module controls its quasi-continuous output voltage.

The paper is organized as follows: First, the system model is introduced and the design of the control system is discussed in detail. Next, the simulation setup and results are illustrated. Then, preliminary measurement results for the implemented current distribution control are presented. Finally, conclusions are given.

System model

The power electronics module concept for controlling one motor phase considered here is based on so called *unit cells*. Each unit cell provides a quasi-continuous output voltage with a signal frequency f_S. By appropriately connecting unit cells, three-phase configurations can be obtained [3]. In addition, parallel [8] or series connection [9, 10] is feasible to increase the voltage and/or current range as illustrated in Fig. 1.



(a) Series connection of unit cells

(b) Parallel connection of unit cells

Fig. 1: Connection concept of unit cells

The internal structure of the unit cell used in this contribution is shown in Fig. 2. The output voltage v_O results from filtering the pulsed voltage v_{HB} with an LC filter. The maximum switching frequency $f_{SW\,max}$ is specified with 500 kHz at a duty cycle of 50 %. In this concept asynchronous delta-sigma ($\Delta\Sigma$) modulation is used. For active damping according to [3] an inductor current feedback with the transfer characteristic G_{FB} is applied. A motor winding is connected to the filter output terminals where the back-emf is not illustrated for simplicity.

The parallel connection of two unit cells is illustrated in Fig. 3. Both unit cells share the same DC voltage source V_B. For simplicity only the output filter structure is represented. The unit cells implemented in hardware will not exhibit exactly the same characteristic behavior with respect to each other due to parasitic and component influences resulting in an unsymmetrical current distribution among the unit cells. To avoid this problem, an external current controller based on a master-slave-principle was implemented as in [8]. In the new concept presented in this paper, a hardware-based solution is proposed. It is designed based on an extension of the state space model for each unit cell. Thus, a hardware-based current control is achieved and the motor current control scheme from a potential field oriented control is not affected.

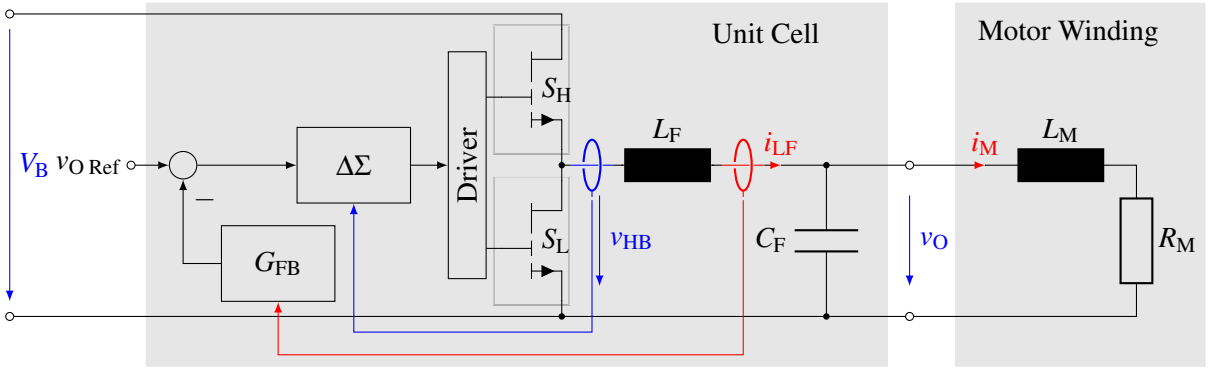


Fig. 2: Unit cell with motor winding

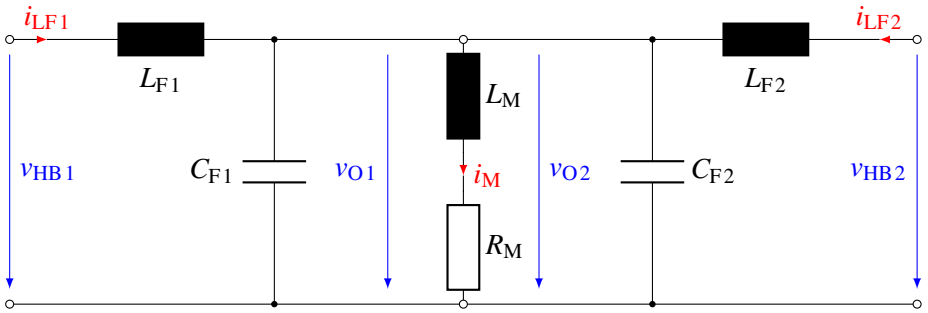


Fig. 3: Two parallel unit cells feeding one motor winding

By applying the mesh and nodal equations, as well as assuming $v_O = v_{O1} = v_{O2}$, the following system of equations can be created:

$$\dot{i}_{LF1} = -\frac{1}{L_{F1}} v_O + \frac{1}{L_{F1}} v_{HB1} \quad (1) \qquad \dot{v}_O = \frac{1}{C_{F1}+C_{F2}} (i_{LF1} + i_{LF2} - i_M) \quad (3)$$

$$\dot{i}_{LF2} = -\frac{1}{L_{F2}} v_O + \frac{1}{L_{F2}} v_{HB2} \quad (2) \qquad \dot{i}_M = -\frac{R_M}{L_M} i_M + \frac{1}{L_M} v_O \quad (4)$$

Based on the structure in Fig. 3, the state space representation of the system without inductor current feedback of i_{LFn} for $n = 1,2$ is given by obtaining $x = [i_{LF1}\ i_{LF2}\ v_O\ i_M]^T$

$$\dot{x} = \begin{bmatrix} 0 & 0 & -\frac{1}{L_{F1}} & 0 \\ 0 & 0 & -\frac{1}{L_{F2}} & 0 \\ \frac{1}{C_{F1}+C_{F2}} & \frac{1}{C_{F1}+C_{F2}} & 0 & -\frac{1}{C_{F1}+C_{F2}} \\ 0 & 0 & \frac{1}{L_M} & -\frac{R_M}{L_M} \end{bmatrix} x + \begin{bmatrix} \frac{1}{L_{F1}} & 0 \\ 0 & \frac{1}{L_{F2}} \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} v_{HB1} \\ v_{HB2} \end{bmatrix} \quad (5)$$

The following two subsections discuss the extension of (5) with respect to the control system objectives.

Integration of the inductor current feedback and current symmetrization

The feedback system illustrated in this section serves two objectives:

1. To introduce a sufficient damping for the LC filter.
2. To enable the symmetrization of the output currents of the two modules.

Although in principle, both functions could be implemented by one single feedback structure, they are

considered separately here. The symmetrization function is not needed for single unit cells. The master unit cell does not need to fulfill the second objective either.

Damping is achieved by the transfer function G_{FB} illustrated in Fig. 2 where the time constant T_{F} and the gain k_{I} are determined following the procedure discussed in [11].

$$G_{\mathrm{FB}}(s) = \frac{s\,T_{\mathrm{F}} k_{\mathrm{I}}}{1 + T_{\mathrm{F}}\,s} \tag{6}$$

To integrate this feedback into (5), an additional state variable $x_{\mathrm{F}n}$ with $n = 1,2$ is introduced. An additional control variable $v_{\mathrm{s}n}$ with $n = 1,2$ for current symmetrization for each unit cell is used. Then, we have for the control signals $v_{\mathrm{HB}\,n}$ in (5) as illustrated in Fig. 4

$$v_{\mathrm{HB}\,n}(t) = v_{\mathrm{ORef}}(t) - x_{\mathrm{F}n}(t) + v_{\mathrm{s}n} \qquad \text{with} \qquad X_{\mathrm{F}n}(s) = G_{\mathrm{FB}}(s) I_{\mathrm{LF}n}(s) \tag{7}$$

where $X_{\mathrm{F}n}(s)$ and $I_{\mathrm{LF}n}(s)$ are the Laplace domain representations of $x_{\mathrm{F}n}(t)$ and $i_{\mathrm{LF}n}(t)$, respectively, and v_{ORef} is the reference input signal for both modules. Thus, we obtain using (5)

$$\dot{x}_{\mathrm{F}n} = -\frac{1}{T_{\mathrm{F}}} x_{\mathrm{F}n} + k_{\mathrm{I}} \dot{i}_{\mathrm{LF}n} \qquad \text{with} \qquad \dot{i}_{\mathrm{LF}n} = -\frac{1}{L_{\mathrm{F}n}} v_{\mathrm{O}} + \frac{1}{L_{\mathrm{F}n}} \left(v_{\mathrm{ORef}} - x_{\mathrm{F}n} + v_{\mathrm{s}n} \right) \tag{8}$$

$$\dot{x}_{\mathrm{F}n} = -\left(\frac{1}{T_{\mathrm{F}}} + \frac{k_{\mathrm{I}}}{T_{\mathrm{F}}} \right) x_{\mathrm{F}n} - \frac{k_{\mathrm{I}}}{L_{\mathrm{F}n}} v_{\mathrm{O}} + \frac{k_{\mathrm{I}}}{L_{\mathrm{F}n}} v_{\mathrm{ORef}} + \frac{k_{\mathrm{I}}}{L_{\mathrm{F}n}} v_{\mathrm{s}n} \tag{9}$$

Integrating (9) into (5) for $n = 1,2$ we obtain using $C_{\mathrm{F}} = C_{\mathrm{F}1} + C_{\mathrm{F}2}$ and $x = [i_{\mathrm{LF}1}\; i_{\mathrm{LF}2}\; v_{\mathrm{O}}\; i_{\mathrm{M}}\; x_{\mathrm{F}1}\; x_{\mathrm{F}2}]^T$

$$\dot{x} = \begin{bmatrix} 0 & 0 & -\frac{1}{L_{\mathrm{F}1}} & 0 & -\frac{1}{L_{\mathrm{F}1}} & 0 \\ 0 & 0 & -\frac{1}{L_{\mathrm{F}2}} & 0 & 0 & -\frac{1}{L_{\mathrm{F}2}} \\ \frac{1}{C_{\mathrm{F}}} & \frac{1}{C_{\mathrm{F}}} & 0 & -\frac{1}{C_{\mathrm{F}}} & 0 & 0 \\ 0 & 0 & \frac{1}{L_{\mathrm{M}}} & -\frac{R_{\mathrm{M}}}{L_{\mathrm{M}}} & 0 & 0 \\ 0 & 0 & -\frac{k_{\mathrm{I}}}{L_{\mathrm{F}1}} & 0 & -\left(\frac{1}{T_{\mathrm{F}}} + \frac{k_{\mathrm{I}}}{T_{\mathrm{F}}} \right) & 0 \\ 0 & 0 & -\frac{k_{\mathrm{I}}}{L_{\mathrm{F}2}} & 0 & 0 & -\left(\frac{1}{T_{\mathrm{F}}} + \frac{k_{\mathrm{I}}}{T_{\mathrm{F}}} \right) \end{bmatrix} x + \begin{bmatrix} \frac{1}{L_{\mathrm{F}1}} & 0 \\ 0 & \frac{1}{L_{\mathrm{F}2}} \\ 0 & 0 \\ 0 & 0 \\ \frac{k_{\mathrm{I}}}{L_{\mathrm{F}1}} & 0 \\ 0 & \frac{k_{\mathrm{I}}}{L_{\mathrm{F}2}} \end{bmatrix} \begin{bmatrix} v_{\mathrm{s}1} \\ v_{\mathrm{s}2} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_{\mathrm{F}1}} \\ \frac{1}{L_{\mathrm{F}2}} \\ 0 \\ 0 \\ \frac{k_{\mathrm{I}}}{L_{\mathrm{F}1}} \\ \frac{k_{\mathrm{I}}}{L_{\mathrm{F}2}} \end{bmatrix} v_{\mathrm{ORef}}\,. \tag{10}$$

The model presented in Fig. 4 will be considered in the next section for current symmetrization.

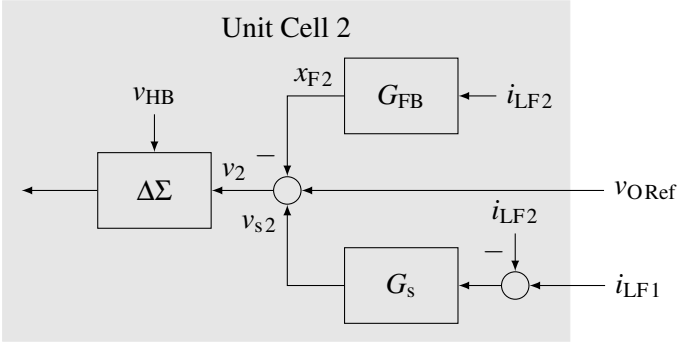


Fig. 4: New control signal generation

Current symmetrization

The controller structure for current symmetrization we will set $v_{\mathrm{ORef}} = 0$ in (10). This is reasonable, as the symmetrization should work independently from the reference voltage. As already indicated by Fig. 4, the symmetrizing controller G_{s} considers the difference between the master current i_{LF1} from unit cell 1 and the slave current i_{LF2} in unit cell 2 which is expected to follow the master current.

A control design could be achieved to control the difference $\delta = i_{\mathrm{LF1}} - i_{\mathrm{LF2}}$ to zero based on the complete system (10). However, the complexity of this system does not allow the direct application of the standard design methods for designing G_{s}. Therefore, a simplified model will be used, where only the unit cell 2 is considered as process model and i_{LF1} is considered as a given reference value. The simplified model is given by obtaining $x_2 = [i_{\mathrm{LF2}}\ v_{\mathrm{O}}\ i_{\mathrm{M}}\ x_{\mathrm{F2}}]^T$

$$\dot{x}_2 = \underbrace{\begin{bmatrix} 0 & -\frac{1}{L_{\mathrm{F2}}} & 0 & 0 & -\frac{1}{L_{\mathrm{F2}}} \\ \frac{1}{C_{\mathrm{F}}} & 0 & -\frac{1}{C_{\mathrm{F}}} & 0 & 0 \\ 0 & \frac{1}{L_{\mathrm{M}}} & -\frac{R_{\mathrm{M}}}{L_{\mathrm{M}}} & 0 & 0 \\ 0 & -\frac{k_{\mathrm{I}}}{L_{\mathrm{F2}}} & 0 & 0 & -\left(\frac{1}{T_{\mathrm{F}}} + \frac{k_{\mathrm{I}}}{T_{\mathrm{F}}}\right) \end{bmatrix}}_{A_2} x_2 + \underbrace{\begin{bmatrix} \frac{1}{L_{\mathrm{F2}}} \\ 0 \\ 0 \\ \frac{k_{\mathrm{I}}}{L_{\mathrm{F2}}} \end{bmatrix}}_{b_2} v_{\mathrm{s2}} \tag{11}$$

For objective 2, in the control signal generation in Fig. 2 an additional system input is included in the unit cell 2 as shown in Fig. 4. The controller G_{s} is designed such that i_{LF2} is sufficiently close to i_{LF1}. From the system matrices in (11) using the matrix $c^T = [1\ 0\ 0\ 0]$ and the identity matrix I a single-input-single-output (SISO) system transfer function can be computed

$$G_2(s) = c_2^T (sI - A_2)^{-1} b_2 \qquad \text{such that} \qquad I_{\mathrm{LF2}}(s) = G_2(s) V_{\mathrm{s2}}(s)\ . \tag{12}$$

The controller G_{s}(s) with $V_{\mathrm{s2}}(s) = G_{\mathrm{s}}(s)(I_{\mathrm{LF1}}(s) - I_{\mathrm{LF2}}(s))$ (see Fig. 4) can then be designed using standard control theory methods based on the process model $G_2(s)$.

Controller design

The controller G_{s} will be designed using the root locus method. Other design methods may be applied, as well. This design uses the system parameters as given in Table I. Note, that the difference between $R_{\mathrm{F\,2}}$ and $R_{\mathrm{F\,1}}$ is used for illustrating the influence of parameter variations between the modules on the current sharing in the simulations. The parameters of the module will be used in correspondence to the datasheet values of the passive components.

Table I: Design parameter

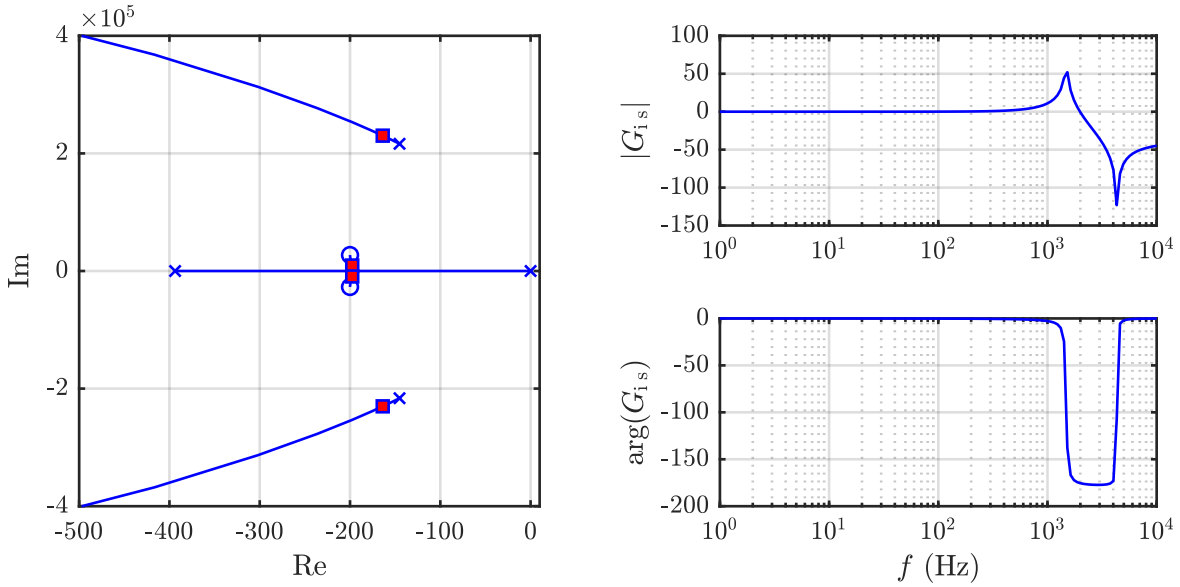
Description M_1	Parameter	Setup
Filter inductance	L_{F1}	15 µH
Resistance of L_{F1}	R_{F1}	12 mΩ
Filter capacitance	C_{F1}	1.36 µF
Motor inductance	L_{M}	0.5 mH
Resistance of L_{M}	R_{M}	1 Ω

Description M_2	Parameter	Setup
Filter inductance	L_{F2}	L_{F1}
Resistance of L_{F2}	R_{F2}	$0.5\,R_{\mathrm{F1}}$
Filter capacitance	C_{F2}	C_{F1}
Motor inductance	L_{M}	0.5 mH
Resistance of L_{M}	R_{M}	1 Ω

For the control system an I-Controller

$$G_{\mathrm{s}}(s) = \frac{k_{\mathrm{s}}}{s} \, .$$

was selected, resulting in the root locus plot of Fig. 5a. This root locus plot is used to determine k_{s} such that the poles have the desired position chosen by the designer. The displayed poles (red squares) of the closed loop transfer function $G_{\mathrm{i\,s}}$ result from the choice $k_{\mathrm{s}} = 1 \times 10^5$ in the root locus design process. Note, that the root locus plot just displays the dominant poles. An additional pole-zero pair is located outside of the shown plot area and is not relevant for the system dynamics. Fig. 5b illustrates the frequency response of the closed loop transfer function $G_{\mathrm{i\,s}}$. It is observed that the controller produces a reasonable behavior with respect to magnitude and phase of the closed loop in a frequency range up to 1 kHz.



(a) Root locus

(b) Frequency response

Fig. 5: Root locus and frequency response for closed current control loop

Simulation

A Simulink model for a parallel connection of two unit cells is shown in Fig. 6. Each of the cells M_1 (Master) and M_2 (Slave) exhibit the structure from Fig. 2 implemented in Simulink as shown in Fig. 7.

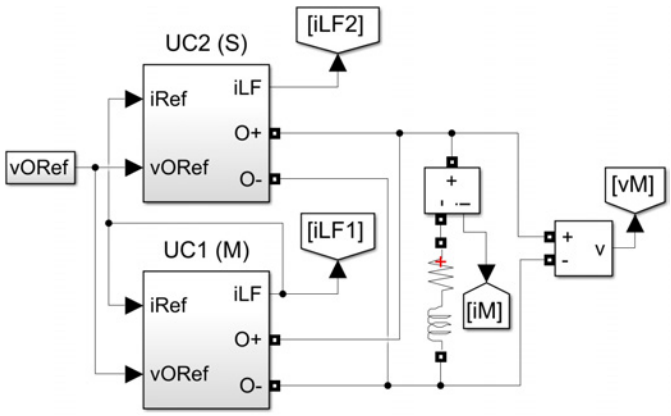


Fig. 6: Simulation model of parallel connected unit cells

The inductor current $i_{\mathrm{LF}\,1}$ is the reference current $i_{\mathrm{Ref}\,2}$ for unit cell M_2 and is fed back to M_1 just for consistency. Note, that the feedback path inside M_1 is deactivated. The load is represented by a motor winding. As this paper focuses on the properties of the power electronics rather than the motor behavior, the back-emf is not considered here and set to zero.

The unit cell simulation model shown in Fig. 7 can be divided into five main parts: ΔΣ modulation, power stage in half-bridge (HB) configuration, passive LC low-pass filter, inductor current feedback and current distribution control.

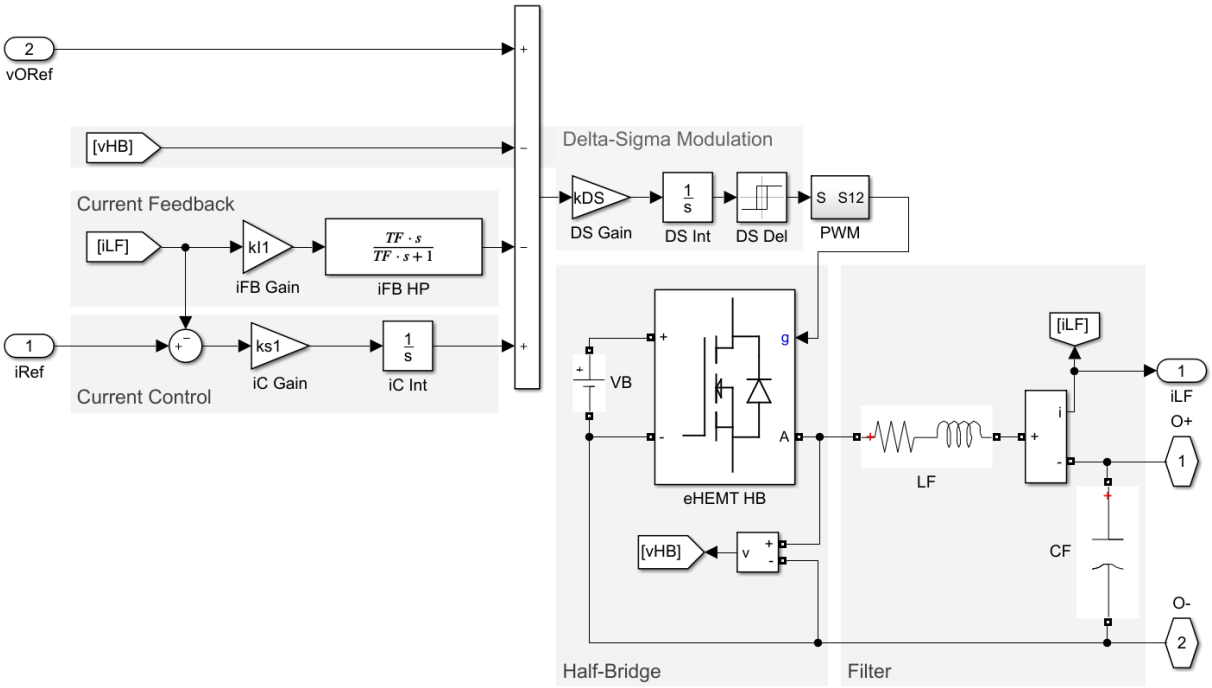


Fig. 7: Simulation model of one unit cell

The current feedback path based on the measured filter inductor current $i_{\mathrm{LF}\,n}$ ensures the filter damping as discussed for the design of a three-phase power stage in [3]. The additional high-pass filter in the current feedback path is used to additionally shape the transfer characteristic. Its design and implementation is discussed in [11].

The implementation of the current sharing control between the modules based on the feedback gain $k_{s\,i}$ is illustrated in Fig. 7 as well. The filter inductor current $i_{\mathrm{LF}\,2}$ is compared to the reference current $i_{\mathrm{LF}\,1}$ to calculate the input for the symmetrizing controller.

Assuming a sinusoidal reference input signal $v_{\mathrm{O\,Ref}}$, Fig. 8 illustrates the simulation results for the motor terminal voltage $v_{\mathrm{M}} = v_{\mathrm{O}}$ and the motor current i_{M} that are the same for the controlled and uncontrolled system.

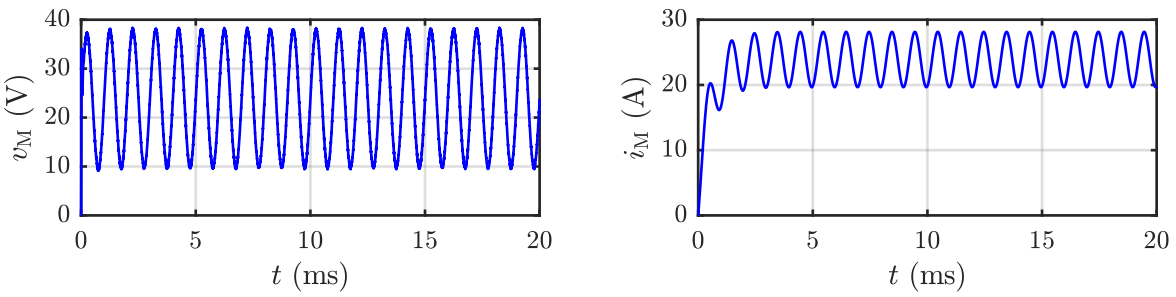
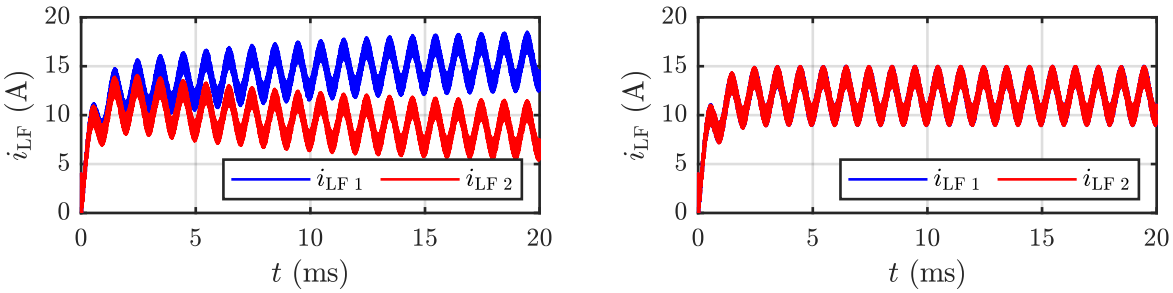


Fig. 8: Simulation results for motor signals v_{M}, i_{M}

Fig. 9 shows the inductor current signals $i_{\mathrm{LF}\,1}$, $i_{\mathrm{LF}\,2}$ of the two unit cells . In Fig. 9a the current control path is not activated, that is, $k_{s\,1} = k_{s\,2} = 0$. The current distribution among the unit cells is not equal due to the deviation from $R_{\mathrm{F}\,2}$ as shown in Table I. By adjusting $k_{s\,2}$ to the designed value 1×10^5 an equal current distribution is achieved as shown in Fig. 9b.



(a) Without control

(b) With control

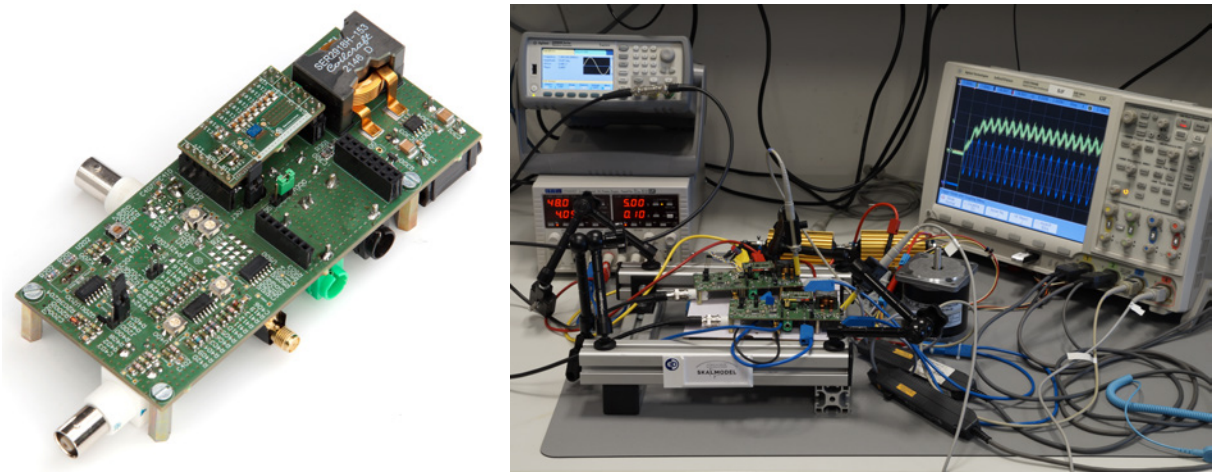
Fig. 9: Simulation results illustrating current distribution control

Note, that the extension to several parallel unit cells is straightforward. Each unit cell receives the current output i_{LF} of its subsequent neighbor unit cell as current input i_{Ref}.

Measurement

In Fig. 10 the hardware setup for the parallelization of unit cells is presented. The representation of a single unit cell based on Fig. 2 and 4 is given in Fig. 10a. Note, that custom in-house developed plug-in HB modules based on *EPC2152* from *EPC Corp.*, that is, a GaN HB with monolithic integrated driver, are used. A second plug-in location is considered for the parallelization of two HB modules within a unit cell. The laboratory measurement setup is illustrated in Fig. 10b. Each unit cell is supplied with the same DC voltage source $V_{\mathrm{B}} = 48\,\mathrm{V}$ and the same reference input signal $v_{\mathrm{O\,Ref}}$ provided by a waveform generator.

In these measurements only one system of parallel unit cells is connected to the terminals of a realistic motor winding. As the simulations illustrate, this leads to a high load current for the target applications. To avoid this situation an additional ohmic load is connected in series to the motor winding. The values of the motor winding ($L_{\mathrm{M}} = 3.3\,\mathrm{mH}$, $R_{\mathrm{M}} = 3.2\,\Omega$) of a stepper motor *L32RFD-00N-NN-00* are determined by measurements. By energizing only one winding, the stepper motor is at stand still, which means no back-emf has to be considered.



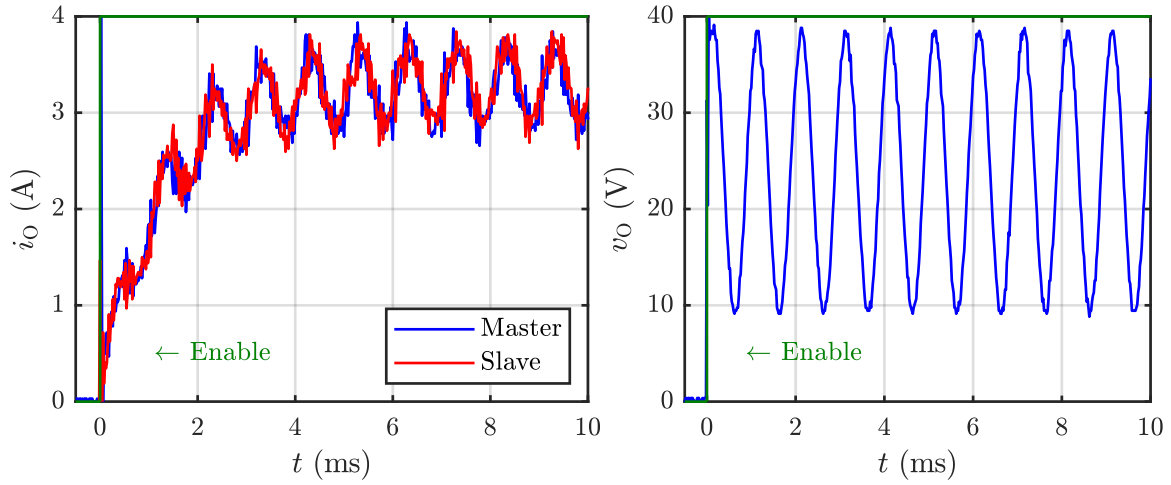
(a) Single unit cell

(b) Laboratory measurement setup

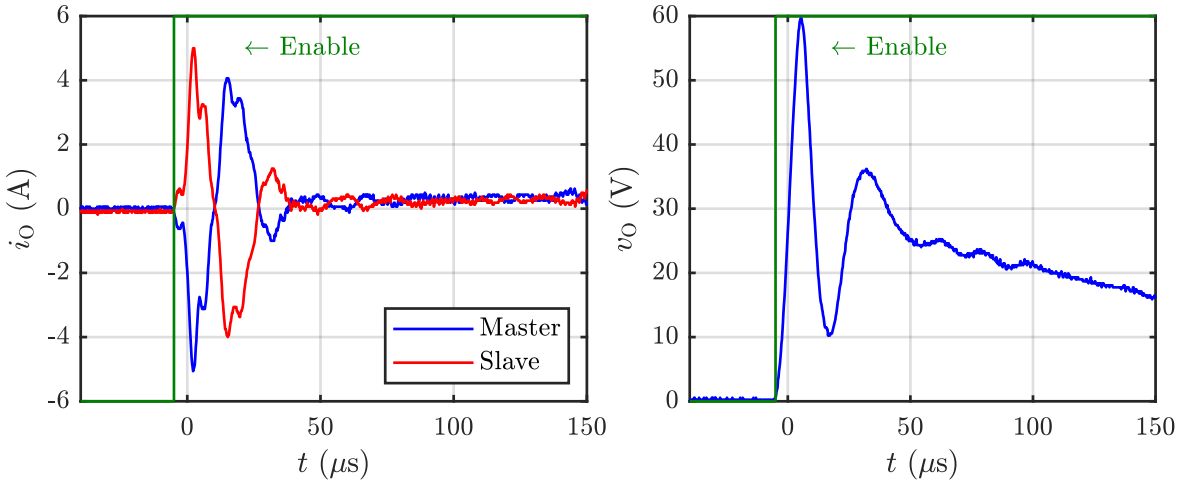
Fig. 10: Hardware setup for parallelization of unit cells

Fig. 11-12 show measurement results with two parallel connected unit cells and the current distribution control. The additional offset observed in the output current signals $i_{\mathrm{O\,M}}$, $i_{\mathrm{O\,S}}$ at $t < 0$ is an effect of the utilized current probe and can be neglected. The enable signal indicates the simultaneous turn-on event for both unit cells in all measurements.

Fig. 11 illustrates the measurements obtained with a sinusoidal reference input signal $v_{\mathrm{O\,Ref}}$. The measurements given in Fig. 11a on the left-hand side illustrate the symmetrical current distribution among the unit cells. The output voltage v_{O} is given on the right-hand side. The DC offset of 24 V of the output voltage occurs from working with a half-bridge.



(a) Current distribution control



(b) Detailed view of current distribution control

Fig. 11: Measurement results for the output signals $i_{\mathrm{O\,M}}$, $i_{\mathrm{O\,S}}$, v_{O} of parallelized unit cells

A detailed view of the output signals v_{O}, $i_{\mathrm{O\,M}}$, $i_{\mathrm{O\,S}}$ for two parallelized unit cells is illustrated in Fig. 11b. It is illustrated that the currents initially diverge. The output currents $i_{\mathrm{O\,M}}$, $i_{\mathrm{O\,S}}$ increase rapidly in opposite directions as long as the current control is not in its operating point. Operating the parallelized unit cells without current control would lead to permanent damage due to the contrary eloping currents.

Finally, Fig. 12 shows a DC step $v_{\mathrm{O\,\Delta DC}}$ of 10 V to illustrate the system dynamics. As expected, a symmetrical current distribution for the parallelized unit cells is achieved.

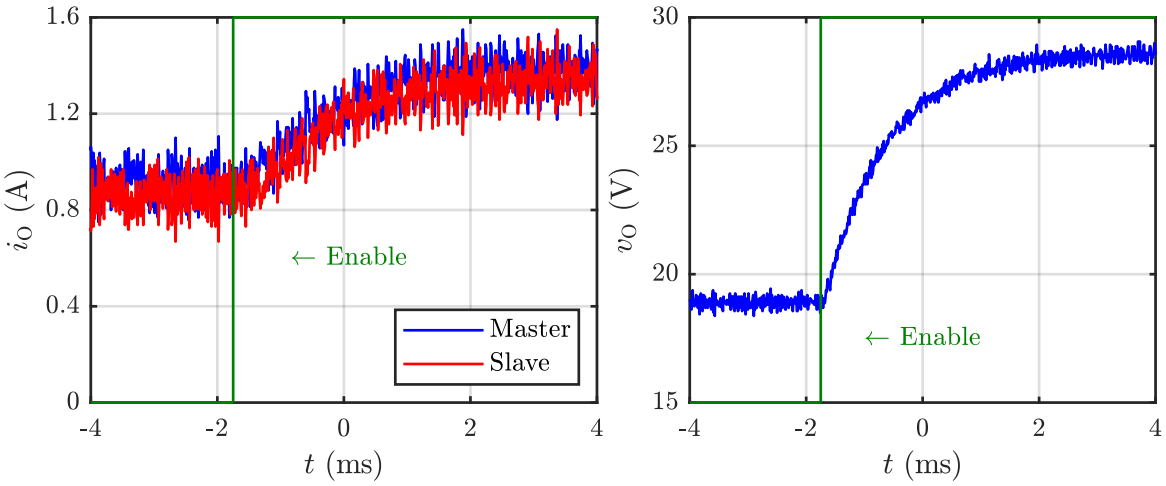


Fig. 12: Measurement results for the output signals $i_{O\,M}$, $i_{O\,S}$, $v_{O\,M}$ for a DC step $v_{O\,\Delta DC}$ of 10 V

Conclusion

This contribution presents a new hardware-based concept for current distribution control between two power electronic modules with quasi-continuous output voltage connected in parallel. The system model and the design of the control system are discussed in detail. Simulation and measurement results are given.

In future work, the extension to several unit cells will be demonstrated. In addition, the extension of the concept to a the combination of parallel and series connection of unit cells will be addressed. Furthermore, the impact of the controller on the modulation as well as the robustness of the controller will be a matter of research, finally resulting in a robust and flexible modular and scalable system.

References

[1] Stubenrauch F., Seliger N. and Schmitt-Landsiedel D.: Design and Performance of a 200kHz GaN Motor Inverter with Sine Wave Filter, 2017 International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM Europe)

[2] Maislinger F., Ertl H., Stojcic G., Lagler C. and Holzner F.: Design of a 100kHz Wide Bandgap Inverter for Motor Applications with Active Damped Sine Wave Filter, Journal of Engineering, Vol 2019, No 17

[3] Ulmer S., Walz-Lange A., Maatz A., Schullerus G., Soenmez E., Hennig E.: Active Filter Damping for a GaN-Based Three Power Stage with Continuous Output Voltage, 2021 23rd European Conference on Power Electronics and Applications (EPE ECCE Europe)

[4] Sinha A. and Jana K. C.: Comprehensive review on control strategies of parallel-interfaced voltage source inverters for distributed power generation system, IET Renewable Power Genereration, 2020, Vol. 14 Iss. 13, pp. 297-2314

[5] Sun. X, Lee Y.-S. and X. D: Modeling, Analysis, and Implementation of Parallel Multi-Inverter Systems With Instantaneous Average-Current-Sharing Scheme, IEEE Transactions on Power Electronics, 2003, Vol. 18 No. 3, 2003

[6] Prodanovic M., Green T. C. and Mansir H.: A Survey of Control Methods for Three-Phase Inverters in Parallel Connection, 8th International Conference on Power Electronics and Variable Speed Drives, 2000

[7] Wu T.-F., Chen Y.-K. and Huang Y.-H.: 3C Strategy for Inverters in Parallel Operation Achieving an Equal Current Distribution, IEEE Transactions on Industrial Electronics, 2020, Vol. 47 No. 2, 2000

[8] Ulmer S., Schullerus G. and Soenmez E.: A Modular and Scalable Power Electronics Device for the Control of Electric Drives, 2019 20th International Symposium on Power Electronics (Ee)

[9] Ulmer S., Schullerus G. and Soenmez E.: Active Damping in Series Connected Power Converters with Continuous Output Voltage, 2021 IEEE 19th International Power Electronics and Motion Control Conference (PEMC)

[10] Ulmer S., Schullerus G. and Soenmez E.: Active Damping in Series Connected Power Modules with Continuous Output Voltage, Power Electonics and Drives (PED), 2021 Vol 6 (41)

[11] Ulmer S., Schullerus G. and Soenmez E.: High Pass Design in Active Filter Damping, 2022 International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM Europe)