Three-phase Four-wire Voltage Converter with D-Σ Control and Phase-Amplitude Compensation

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***Abstract*—This paper proposes a converter with division-summation (D-Σ) control and phase-amplitude compensation. The system allows independent adjustment of specific harmonic voltage, reducing the tracking error. Compared with the D-Σ control alone, the converter can track the command more accurately. Moreover, it retains the characteristics of high inductance degradation tolerance. Finally, the proposed control is validated by measurement results.**

I. Introduction

Many experts have devoted themselves to the research of grid-connected converters [1]-[3]. However, the use of grid-connected converters and non-linear loads caused distortions in the power grid. Among them, renewable energy generation systems are affected by climatic conditions, which may cause grid failures. Non-linear loads also affect the grid [4].

Conventionally, when researchers develop electronic products, they test their performance through the real grid, but the actual grid is costly, time-consuming, and bulky. Therefore, experts have proposed the concept of a "grid simulator" [6]-[9]. Paper [6] proposed a new architecture of grid simulator using fundamental and higher-order harmonic converter modules as a grid simulator. The authors in [7] proposed to combine the high and low switching frequency converter modules with coupling inductors to simulate the grid. [8] proposed to simulate utility disturbances based on the finite-control-set model predictive control. [9] proposed a modular multi-level converter to simulate grid anomalies. However, multiple inverters in parallel or modular multi-level architectures [6]-[9] use a large number of switches or frame transformation, making the control more complicated.

In 3Φ converter applications, the D-Σ control is widely used [10]-[12], and the control incorporates the inductance drop into the control-law calculation, so that inductors with relatively small size can be used as filters for power converters. However, the control is limited by the system bandwidth, causing phase and amplitude shifts and leading to large tracking errors.

To solve the above problem, phase-amplitude compensation (PAC) is proposed. It can correct the phase and amplitude of the fundamental and specific harmonic components of the output voltage. Compared with the conventional D-Σ control alone, the proposed control architecture improves the tracking errors caused by the limited bandwidth, and retains the characteristics of high inductance-drop rate.

II. D-Σ Voltage-Type Control

Fig. 1 shows the power stage of a 3Φ4W converter, in which L_{ik} is the filter inductance, C_{fk} is the filter capacitance, Z_{Lk} is the load impedance, and k represents the phase sequence $\{R,S,T\}$. Therefore, The power stage can be equivalent to a single-phase system, as shown in Fig. 3.

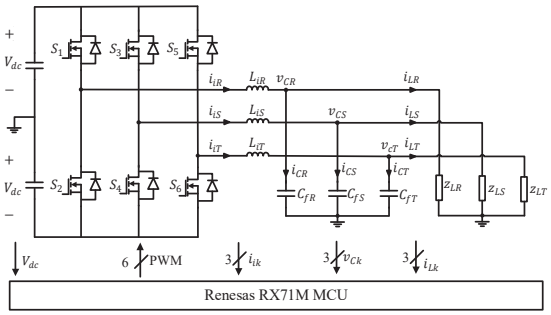


Fig. 1. Three-phase four-wire voltage converter architecture.

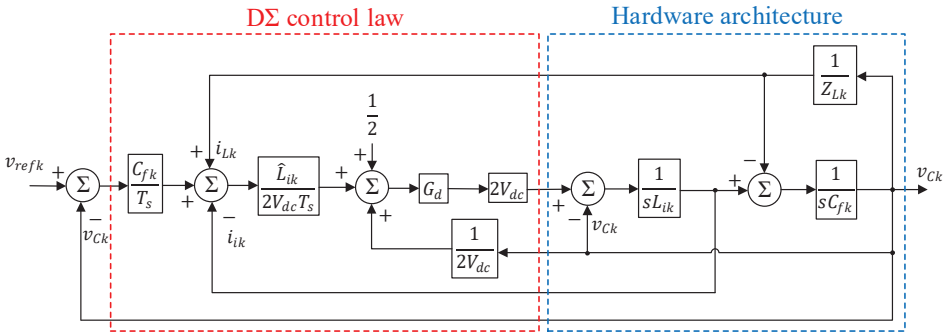


Fig. 2. 3Φ4W voltage converter control system architecture

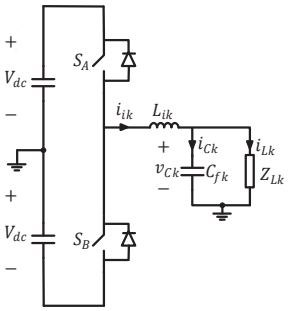


Fig. 3. Single-phase equivalent circuit diagram.

From Fig. 3, Δi_{ik}^{+} occurs when switch S_A is on and S_B is off, and Δi_{ik}^{-} occurs when S_A is off and S_B is on, and the related expressions are as follows:

Magnetization mode ($S_A = 1, S_B = 0$):

$$\Delta i_{ik}^{+} = \frac{V_{dc} - v_{Ck}}{L_{ik}} \cdot D_k \cdot T_{sw} \quad (1)$$

Demagnetization mode ($S_A = 0, S_B = 1$):

$$\Delta i_{ik}^{-} = \frac{-V_{dc} - v_{Ck}}{L_{ik}} \cdot (1 - D_k) \cdot T_{sw} \quad (2)$$

where D_k indicates the duty ratio of phase k and T_{sw} is the switching period. Adding (1) and **Error! Reference source not found.** together to obtain the current change in one cycle can be expressed as

$$\Delta i_{ik} = \frac{V_{dc} - v_{Ck}}{L_{ik}} \cdot D_k \cdot T_{sw} + \frac{-V_{dc} - v_{Ck}}{L_{ik}} \cdot (1 - D_k) \cdot T_{sw} \quad (3),$$

and then organizing it, the duty ratio can be derived as

$$D_k = \frac{1}{2} + \frac{L_{ik}}{2V_{dc}T_{sw}} \cdot \Delta i_{ik} + \frac{v_{Ck}}{2V_{dc}} \quad (4)$$

In order to regulate the output voltage, the capacitor current should be estimated [14], where the estimated capacitor current can be expressed as

$$i_{Ck}[n+1] \approx \frac{C_{fk}}{T_s}\left(v_{refk}[n+1] - v_{Ck}[n]\right) \quad (5)$$

and Δi_{ik} can be rewritten as (5):

$$\Delta i_{ik}[n+1] = i_{Ck}[n+1] + i_{Lk}[n] - i_{ik}[n] \quad (6)$$

Finally, the D-Σ based voltage control block diagram can be derived as shown in Fig. 2, where T_s is the sampling period, and G_d is the sampling and calculation delay [13]. The estimated ($\hat{L}_{ik}$) and actual (L_{ik}) inductance values can be expressed as:

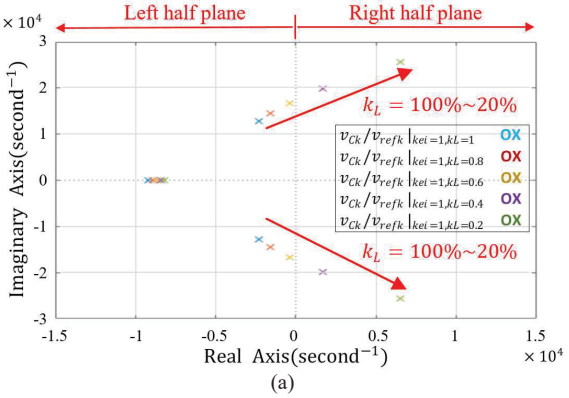
$$\hat{L}_{ik} = k_{ei}\, L_{ik,nom} \quad (7)$$

and

$$L_{ik} = k_L\, L_{ik,nom} \quad (8)$$

where $L_{ik,nom}$ is the undecayed inductance value. Parameters k_{ei} and k_L are the estimated and actual inductance drop rates, respectively.

However, if (4) does not include the inductance-drop, it will cause system oscillation. Taking resistive load as an example, Fig. 4 shows the pole-zero plots without and with considering inductance drop. Without taking into account the inductance drop, the poles shift to the right-half plane, causing instability. Considering inductance drop, the system remains stable.



(a)

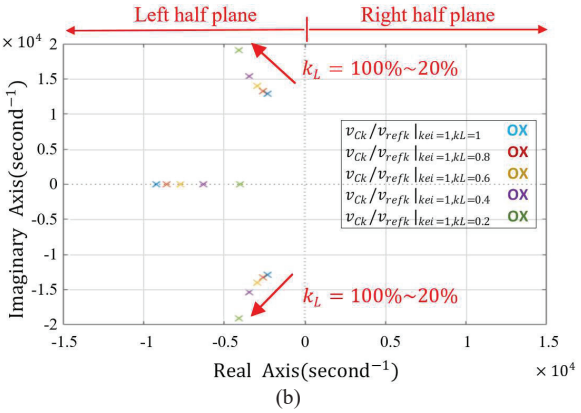


Fig. 4. Pole-zero plots: (a) without and (b) with considering inductance drop in the duty-ratio calculation.

III. Proposed Control Approaches

Fig. 5 shows the control with PAC. To simplify the derivation process, the fundamental component is defined as the 1^{st} harmonic.

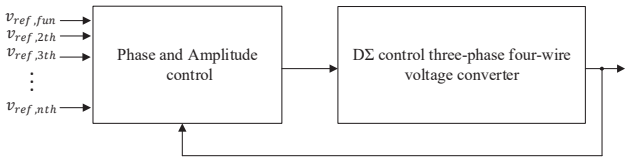


Fig. 5. Phase and amplitude compensation system

A. Phase compensation

Fig. 6 shows the equivalent model of a specific harmonic phase control loop, where θ^*_{nth} is the phase command, $k_{PD,nth}$ is the derived error gain, $\omega_{ff,nth}$ is the feedforward term of the angular frequency and $\hat{\theta}_{nth}$ is the estimated phase.

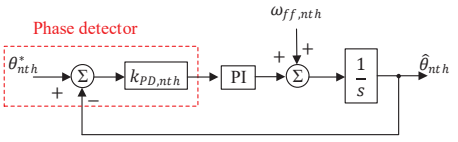


Fig. 6. Equivalent model of specific harmonic phase control loop.

To estimate the phase error between the command and output, the command, output, and their orthogonal values are included in the calculation. The related equation can be expressed as (9) when θ_1 is close to θ_2, and the equivalent phase error with its gain can be expressed as (10):

$$K\sin(\theta_1-\theta_2)=\overbrace{\sin(\omega t+\theta_1)}^{Command}\cdot\overbrace{K\cos(\omega t+\theta_2)}^{Orthogonal\ Output}-\overbrace{\cos(\omega t+\theta_1)}^{Orthogonal\ Command}\cdot\overbrace{K\sin(\omega t+\theta_2)}^{Output} \tag{9}$$

$$\approx K(\theta_1-\theta_2) \tag{10}$$

where $\sin(\omega t+\theta_1)$ and $\cos(\omega t+\theta_1)$ are the command and its orthogonal values, respectively. $K\sin(\omega t+\theta_2)$ and $K\cos(\omega t+\theta_2)$ are the measured signals and its orthogonal values, respectively.

In the grid simulator, the voltage command of a particular harmonic can be expressed as:

$$v^*_{nth}=V^*_{amp,nth}\sin\left(n\omega_{fun}t+\theta^*_{0,nth}\right) \tag{11}$$

where n represents the order of a harmonic command, ω_{fun} is the angular frequency of the fundamental component, $V^*_{mag,nth}$ is the amplitude command of a particular harmonic, and $\theta^*_{0,nth}$ is the initial angular position of a particular harmonic.

To simplify the derivation process, the scalarized specific harmonic command and output voltage can be expressed as:

$$v^*_{pu,nth}=\sin\left(n\omega_{fun}t\right) \tag{12}$$

and

$$v_{fb}=\sum_{k\in a}V_{fb,amp,kth}\sin\left(k\omega_{fun}t+\Delta\theta_{fb,kth}\right) \tag{13}$$

where a represents the order of a specific harmonic component in the output voltage, And $\Delta\theta_{fb,kth}$ is the phase error between specific harmonic command and its corresponding output.

Therefore, the phase error between the nth harmonic command and its gain can be expressed as:

$$\begin{aligned}\hat{\theta}_{err,nth}&=V_{fb,amp,kth}\sin\left(-\Delta\theta_{fb,kth}\right)\\&\approx V_{fb,amp,kth}\left(-\Delta\theta_{fb,kth}\right)\end{aligned} \tag{14}$$

B. Amplitude compensation

Fig. 7 shows the equivalent model of the specific harmonic amplitude control loop, where $V^*_{amp,nth}$ is the amplitude command, and $|T_{D\Sigma}(j\omega_{nth})|$ is the output voltage gain of the general D-Σ control at the specific harmonic.

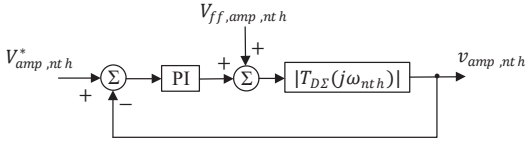


Fig. 7. Equivalent model of a specific harmonic amplitude control loop

To estimate the amplitude of signal, the command, output and their orthogonal values are included in the calculation, and the equation can be expressed as:

$$\begin{aligned}K\cos(\theta_1-\theta_2)=&\cos(\omega t+\theta_1)\cdot K\cos(\omega_2 t+\theta_2)\\&+\sin(\omega t+\theta_1)\cdot K\sin(\omega_2 t+\theta_2)\end{aligned} \tag{15}$$

where $sin(\omega t + \theta_1)$ and $cos(\omega t + \theta_1)$ are the command and its orthogonal value, respectively. $K\ sin(\omega t + \theta_2)$ and $K\ cos(\omega t + \theta_2)$ are the measured signals and its orthogonal signals, respectively. When θ_1 is close to θ_2, the estimated amplitude can be approximated as:

$$\hat{v}_{amp} = K\ cos(\theta_1 - \theta_2) \approx K \quad (16)$$

Therefore, the amplitude of the nth harmonic in the output voltage can be expressed as

$$\hat{A}_{nth} = V_{fb,amp,kth}\ cos(-\Delta\theta_{fb,kth}) \approx V_{fb,amp,kth} \quad (17)$$

where $\Delta\theta_{fb,kth}$ can be approximated as "0" in the steady state.

IV. Experimental Results

Fig. 8 shows a photograph of the 3Φ4W voltage converter verified with resistive load. The system hardware parameters are listed in TABLE I.

TABLE I
SYSTEM CONFIGURATION

Parameter	value
DC bus voltage, each capacitor (V_{dc})	390 V
Filter Inductance (L_{ik})	2mH~0.4mH
Filter Capacitance (C_{fk})	15 μF
Switching frequency (f_{sw})	20 kHz
Sampling frequency (f_s)	10 kHz

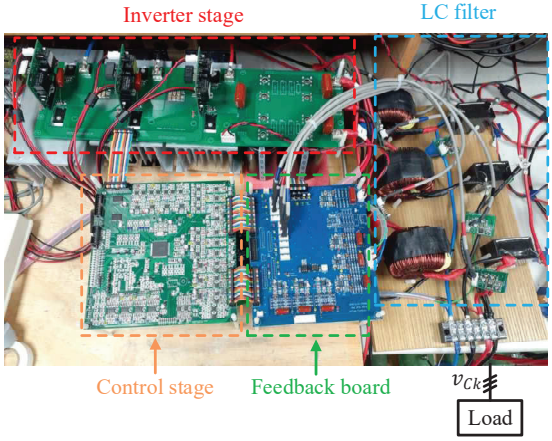
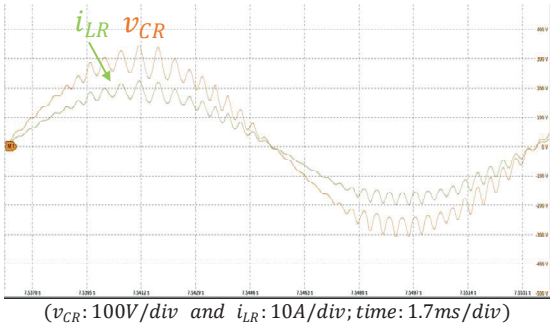


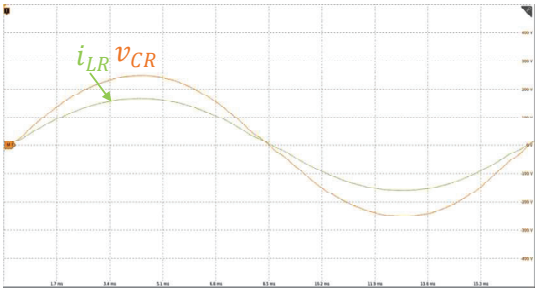
Fig. 8. Testing platform.

Fig. 9 shows the measured results without and with considering inductance variation. The inductance drops from $2mH$ to 400 μH with the increase of current. If the inductance drop is not included in the control laws, the system will seriously oscillate. Considering the inductance drop, the system will remain stable.



(v_{CR}: 100V/div and i_{LR}: 10A/div; $time$: 1.7ms/div)

(a)



(v_{CR}: 100V/div and i_{LR}: 10A/div; $time$: 1.7ms/div)

(b)

Fig. 9. Measured results of resistive load voltage and current (a) without, and (b) with considering inductance drop.

The voltage command contains 250V fundamental component and 10% of the 5^{th}, 7^{th} and 11^{th} harmonics for each. Fig. 10 shows the measured results and spectrum before and after compensation with resistive load. Before compensation, the fundamental component of the output voltage is about 213.21 V, and the 5^{th}, 7^{th} and 11^{th} harmonic components are 18.65 V, 18.73 V, and 16.36 V, respectively. After compensation, the fundamental component is about 251.41 V, and the 5^{th}, 7^{th} and 11^{th} harmonic components are 24.87 V, 25.13 V, and 24.75 V, respectively.

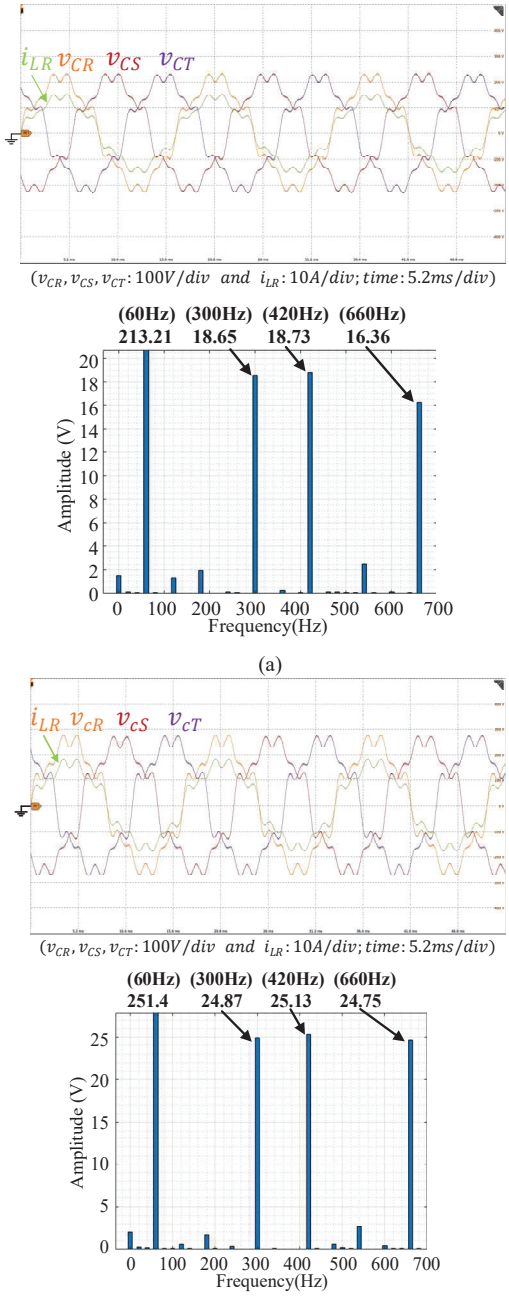


Fig. 10. Measured results and spectra of simulated high harmonic contamination under resistive load conditions, (a) without, and (b) with PAC.

Fig. 11 shows the voltage command, measured waveform, and tracking error before and after compensation under resistive load. Before compensation, the peak-to-peak error is about 130.27 V, and after compensation, it drops to 18.15 V.

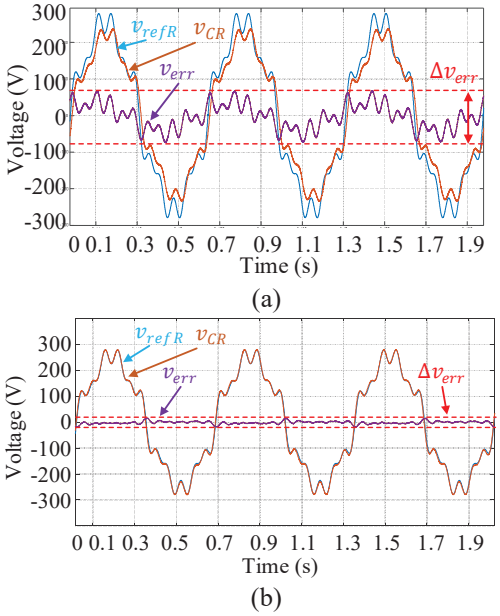


Fig. 11. Measured results of output voltage and tracking error, taking phase R rectified load as an example: (a) without and (b) with PAC.

V. Conclusions

This paper proposes a converter with a PAC and D-Σ control architecture, which can compensate the phase and amplitude of the fundamental and specific harmonics in the output voltage independently. Therefore, when a specific harmonic is required in the output voltage, the corresponding controller can be used to compensate for it, which makes the application more flexible. Compared to uncompensated inverters, the tracking error between the command and the actual output is improved. Finally, the feasibility of the proposed control method has been verified by the actual test results.

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