Reliability Assessment of Fault-Tolerant Multilevel Inverter Topologies with Reduced Switch Count

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***Abstract*-- Multilevel inverters (MLIs) are becoming increasingly popular in medium and high-power applications due to benefits of low total harmonic distortion (THD) and lower voltage stress across switches. The proper operation of these multilevel inverter topologies is heavily dependent on the reliable operation of semiconductor devices. The role of the inverter is very crucial and in case of failure of the switches, the output voltage of the MLI is significantly affected which leads to degraded performance or in some cases complete shutdown of the overall system. Recently, several fault-tolerant (FT) MLI topologies have been proposed, however, in most of cases, the design has been accomplished for the open circuit faults (OCF) only. The switches of any topology can suffer from another type of fault namely short-circuit fault (SCF). In this paper, a reliability assessment of the different FT-MLI has been carried out by considering OCF and SCF in single as well as double switches. A comparison has been provided to assess the reliability of the FT-MLI topologies with the scope for improvement in a more robust design. Finally, a 5-level FT-T-type converter has been simulated and results have been analyzed for different types of faults.**

***Index Terms*— Reliability, Fault-tolerant, Multilevel Inverter, Fault Analysis.**

I. Introduction

Multilevel inverter (MLI) topologies for dc-to-ac power conversion have gained widespread acceptance in the power electronics field. Better power quality, lower voltage stress, good electromagnetic compatibility, and smaller passive filter components are just a few of the ways in which MLI topologies excel over traditional two-level counterparts. Multilevel inverters find widespread use in the areas of the flexible ac transmission system, active filters, electric drives, and renewable energy systems. "Cascaded H-Bridge (CHB)," "Flying Capacitor (FC)," and "Neutral Point Clamped" (NPC) are the most well-known and fundamental multilevel inverters[1], [2]. Despite the aforementioned benefits, such converters have the drawback of necessitating a larger number of components. The fundamental drawback of adding new components is drop in reliability, in addition to increase in cost, complexity, and size. Reliability demands in power electronics are growing in tandem with the widespread adoption of power electronics converters in various industrial as well as residential applications. Power devices are the weak link, leading to unreliability in MLIs and system failure. The contribution of failure of the power semiconductor devices and soldering joints in the power electronic converter is 34% [3]. There are two types of faults in switching devices: open switch and short switch. Incorrect gate voltage, overvoltage, avalanche stress, and extremely high temperatures are some of the many potential causes of converter system failure (CSF). Since an excessive overcurrent can severely harm the components of the system, this fault type is extremely crucial and challenging to handle. As the bonding wire lifts and unplugs owing to thermal cycling, an OCF results. In addition to the primary issue of current distortion, this also generates secondary issues in other components like gate drivers. In most cases, the OCF does not cause major damage but does degrade system performance. Recently, several MLI topologies with claims of FT ability have been proposed. In [4]–[7], different FT-MLI topologies with claims of OCF reliability have been proposed. In this paper, these topologies have been analyzed for different types of faults and results have been summarized.

II. Reliability Assessment of FT-MLI

In this section, reliability assessment of different FT-MLIs for OCF and SCF has been carried out. OCF has been considered with the gate pulse being "0" or in *off* condition whereas SCF has been realized by considering the gate pulse being "1" or *on* condition. T-type topology is a conventional topology in which the dc-link is used to split the input voltage to increase the number of levels. Fig. 1 shows the 5-level T-type inverter with an addition switch S_6 which has been used to improve reliability of the converter [4]. The overall topology consists of four unidirectional switches and two bidirectional switches. The four unidirectional switches form the H-bridge and the two bidirectional switches connect the mid-point of dc-link capacitors with each terminal of the single-phase load. As claimed by the authors that this topology can tolerate open circuit faults in any switch. Table I gives all the possible switching combinations for the topology shown in Fig. 1. In the case of a single switch with OCF, the output voltage is either 50% or 100% of the output voltage (OV) in healthy operating conditions, however, in case of

OCF in two switches, the output voltage is zero. The SCF is very common as it can happen due to the localized hot spot formation within the switch, high *di/dt*, and gate driver failure. Prolonged operation (just few cycles) with SCF may lead to fault (usually bond wire lift off or delamination of die attach) in other switches due to high current damage. In the case of SCF in either one or two switches, the output voltage is zero. The analysis is summarized in Table II.

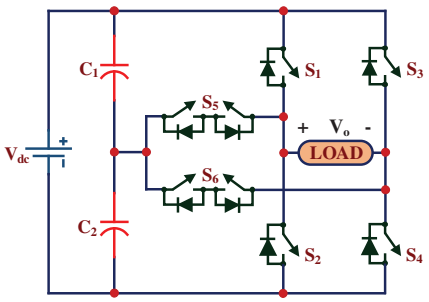


Fig. 1: FT 5-level T-type Inverter topology [4]

TABLE I:
SWITCHING STATES FOR FIVE LEVEL T-TYPE TOPOLOGY

S_1	S_2	S_3	S_4	S_5	S_6	V_o
1	0	0	1	0	0	V_{dc}
0	0	0	1	1	0	$0.5V_{dc}$
1	0	0	0	0	1	
0	1	0	1	0	0	0
1	0	1	0	0	0	
0	0	0	0	1	1	
0	0	1	0	1	0	$-0.5V_{dc}$
0	1	0	0	1	0	
0	1	1	0	0	0	$-V_{dc}$

TABLE II:
OCF / SCF ANALYSIS OF FIVE LEVEL T-TYPE TOPOLOGY PROPOSED IN [4]

Fault Type	Faulty Switch/es	N	Voltage Levels	% of OV
OCF	S_1 / S_2 / S_3 / S_4	3	0, and $\pm0.5V_{dc}$	50%
	S_5 / S_6	5	0, $\pm0.5V_{dc}$ and $\pm V_{dc}$	100%
	Combinations of S_i and S_{i+1} (i= 1,2,…5)	3	0, and $\pm0.5V_{dc}$	50%
SCF	S_1 / S_2 / S_3 / S_4 / S_5 / S_6	0	0	0
	Combinations of S_i and S_{i+1} (i= 1,2,…5)	0	0	0

A development in the T-type topology has been proposed in [5] in which three dc voltage sources of the same magnitude have been used. The topology as shown in Fig. 2 consists of eight unidirectional and two bidirectional switches. Compare to the FT-MLI topology proposed in [4], the topology proposed in [5] uses two additional sources with their associated two switches forms as a half-bridge. In normal operating conditions, a seven-level output voltage waveform can be achieved. The different voltage states which can be realized have been provided in Table III. With additional switches, the voltage levels of $\pm2V_{dc}$, $\pm V_{dc,}$ and zero have several redundant switching states. Based on these switching states, the OCF and SCF analysis has been provided in Table IV.

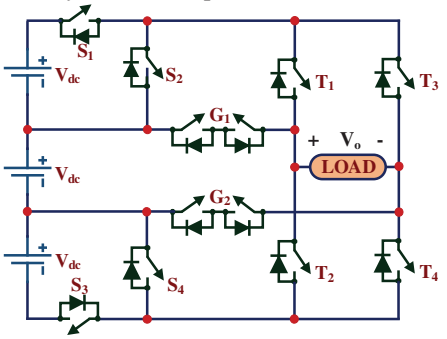


Fig. 2: FT topology proposed in [5]

TABLE III:
POSSIBLE SWITCHING STATES FOR TOPOLOGY PROPOSED IN [5]

S_1	S_2	S_3	S_4	T_1	T_2	T_3	T_4	G_1	G_2	V_o
1	0	1	0	1	0	0	1	0	0	$3V_{dc}$
0	1	1	0	1	0	0	1	0	0	$2V_{dc}$
0	0	1	0	0	0	0	1	1	0	
1	0	0	0	1	0	0	0	0	1	
0	0	0	1	0	0	0	1	1	0	V_{dc}
0	1	0	1	1	0	0	1	0	0	
0	1	0	0	1	0	0	0	0	1	
0	0	0	0	0	0	0	0	1	1	
0	0	0	0	1	0	1	0	0	0	0
0	1	0	0	0	0	1	0	1	0	
0	0	0	0	0	1	0	1	0	0	
0	0	0	1	0	1	0	0	0	1	
0	0	1	0	0	1	0	0	0	1	$-V_{dc}$
1	0	0	0	0	0	1	0	1	0	
0	1	0	1	0	1	1	0	0	0	
1	0	0	1	0	1	1	0	0	0	$-2V_{dc}$
0	1	1	0	0	1	1	0	0	0	
1	0	1	0	0	1	1	0	0	0	$-3V_{dc}$

Another FT-MLI topology has been proposed in [6] which consists of 12 unidirectional switches and 4 dc voltage sources of the same voltage magnitude, i.e., V_{dc}. The schematic of this topology is shown in Fig. 3. Under normal operating conditions, this topology can generate nine level voltage waveform. Two redundant switches, i.e., S_7' and S_8' have been included in the topology to create more redundant states. Table V list all the possible voltage state combination for the topology proposed in [6]. The different switching states for the topology shown in Fig. 3 have several redundant switching states for all nine-voltage levels. The topology highly depends on the switches S_7 and S_8 as switch S_8 is in *ON* state for all positive voltage levels while S_7 is in *ON* condition for all the negative voltage levels. As switches (S_7' and S_7) and

TABLE IV:
OCF / SCF ANALYSIS OF TOPOLOGY PROPOSED IN [5]

Fault Type	Faulty Switch/es	N	Voltage Levels	% of OV
OCF	T_2 / T_3	3	0, and $\pm V_{dc}$	33%
	S_1 / S_3 / T_1 / T_4	5	0, $\pm V_{dc}$, and $\pm 2V_{dc}$	67%
	S_2 / S_4 / G_1 / G_2	7	0, $\pm V_{dc}$, $\pm 2V_{dc}$, and $\pm 3V_{dc}$	100%
	(T_1, G_1), (T_2, T_3), (T_2, G_1), (T_3, G_2), (T_4, G_2)	0	0	0
	(S_1, S_2), (S_1, S_3), (S_1, T_2), (S_1, T_3), (S_1, T_4), (S_2, S_4), (S_2, T_2), (S_2, T_3), (S_3, S_4), (S_3, T_1), (S_3, T_2), (S_3, T_3), (S_3, G_2), (S_4, T_2), (S_4, T_3), (T_1, T_2), (T_1, T_3), (T_1, T_4), (T_2, T_4), (T_2, G_2), (T_3, T_4), (T_3, G_1)	3	0, and $\pm V_{dc}$	33%
	(S_1, S_4)	3	0, and $\pm 2V_{dc}$	67%
	(S_1, T_1) , (S_1, G_1), (S_1, G_2), (S_2, S_3), (S_2, T_1), (S_2, T_4), (S_3, T_4), (S_3, G_1), (S_4, T_4), (S_4, G_2), (T_1, G_2), (T_4, G_1), (S_4, T_1),	5	0, $\pm V_{dc}$, and $\pm 2V_{dc}$	67%
	(S_2, G_1), (S_2, G_2), (S_4, G_1), (G_1, G_2)	7	0, $\pm V_{dc}$, $\pm 2V_{dc}$, and $\pm 3V_{dc}$	100%
SCF	T_1 / T_2 / T_3 / T_4	0	0	0
	G_1 / G_2	3	0, and $\pm V_{dc}$	33%
	S_2 / S_4	5	0, $\pm V_{dc}$, and $\pm 2V_{dc}$	67%
	S_1 / S_3	7	0, $\pm V_{dc}$, $\pm 2V_{dc}$, and $\pm 3V_{dc}$	100%
	(S_1, S_3)	3	0, and $\pm 3V_{dc}$	100%
	(S_1, S_4), (S_2, S_3)	5	0, $\pm V_{dc}$, and $\pm 2V_{dc}$	67%
	(S_2, S_4)	3	0, and $\pm V_{dc}$	33%
	All other combinations of switches	0	0	0

(S_8' and S_8) are in parallel, the additional two parallel switches create an alternate switching state by bypassing the other switch in parallel in case of an open-circuit fault. The topology shown in Fig. 3 has been analyzed for different types of switch faults and the results have been summarized in Table VI. The performance of the topology proposed in [6] is better in the case of OCF compared to the SCF.

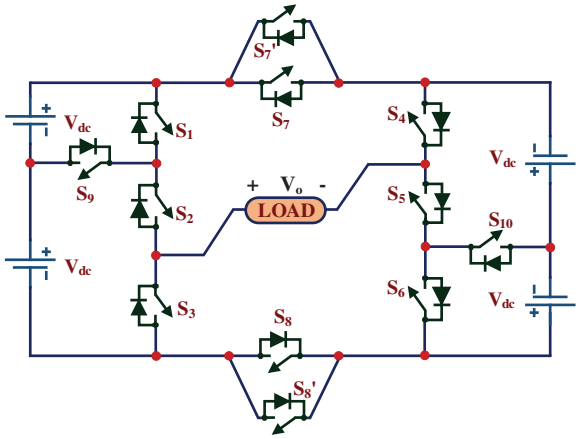


Fig. 3: Symmetrical FT topology proposed in [6]

Another FT topology derived from conventional T-type MLI has been proposed in [7] and is shown in Fig. 3 (b). It consists of three bidirectional and six unidirectional switches. The topology without fault-tolerant ability can be formed without two bidirectional switches (S_8, and S_9), and under normal operating conditions, a seven-level output voltage waveform can be generated. The different available switching states have been provided in Table VII, whereas Tale VIII gives the fault analysis for the topology proposed in [7].

TABLE V:
POSSIBLE SWITCHING STATES FOR TOPOLOGY PROPOSED IN [6]

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_7'	S_8	S_8'	S_9	S_{10}	V_o
1	1	0	1	0	0	0	0	1	0	0	0	$4V_{dc}$
1	1	0	1	0	0	0	0	0	1	0	0	
1	1	0	0	1	0	0	0	1	0	0	1	$3V_{dc}$
1	1	0	0	1	0	0	0	0	1	0	1	
0	1	0	1	0	0	0	0	1	0	1	0	
0	1	0	1	0	0	0	0	0	1	1	0	
1	1	0	0	1	1	0	0	1	0	0	0	$2V_{dc}$
1	1	0	0	1	1	0	0	0	1	0	0	
0	1	0	0	1	0	0	0	1	0	1	1	
0	1	0	0	1	0	0	0	0	1	1	1	
0	0	1	1	0	0	0	0	1	0	0	0	
0	0	1	1	0	0	0	0	0	1	0	0	
0	1	0	0	1	1	0	0	1	0	1	0	V_{dc}
0	1	0	0	1	1	0	0	0	1	1	0	
0	0	1	0	1	0	0	0	1	0	0	1	
0	0	1	0	1	0	0	0	0	1	0	1	
0	0	1	0	1	1	0	0	1	0	0	0	0
0	0	1	0	1	1	0	0	0	1	0	0	
1	1	0	1	0	0	1	0	0	0	0	0	
1	1	0	1	0	0	0	1	0	0	0	0	
1	1	0	0	1	0	1	0	0	0	0	1	$-V_{dc}$
1	1	0	0	1	0	0	1	0	0	0	1	
0	1	0	1	0	0	1	0	0	0	1	0	
0	1	0	1	0	0	0	1	0	0	1	0	
1	0	0	1	1	1	1	0	0	0	0	0	$-2V_{dc}$
1	0	0	1	1	1	0	1	0	0	0	0	
0	0	1	1	0	0	1	0	0	0	0	0	
0	0	1	1	0	0	0	1	0	0	0	0	
0	1	0	0	1	0	1	0	0	0	1	1	
0	1	0	0	1	0	0	1	0	0	1	1	
0	1	0	0	1	1	1	0	0	0	1	0	$-3V_{dc}$
0	1	0	0	1	1	0	1	0	0	1	0	
0	0	1	0	1	0	1	0	0	0	0	1	
0	0	1	0	1	0	0	1	0	0	0	1	
0	0	1	0	1	1	1	0	0	0	0	0	$-4V_{dc}$
0	0	1	0	1	1	0	1	0	0	0	0	

TABLE VI:
OCF / SCF ANALYSIS OF TOPOLOGY PROPOSED IN [6]

Fault Type	Faulty Switch/es	N	Voltage Levels	% of OV
OCF	S_2 / S_5	3	0, and $\pm 2V_{dc}$	50%
	S_1 / S_3 / S_4 / S_6	7	0, $\pm V_{dc}$, $\pm 2V_{dc}$, and $\pm 3V_{dc}$	75%
	S_7 / S_7' / S_8 / S_8' / S_9 / S_{10}	9	0, $\pm V_{dc}$, $\pm 2V_{dc}$, $\pm 3V_{dc}$, and $\pm 3V_{dc}$	100%
	(S_2, S_3), (S_2, S_4), (S_3, S_5), (S_4, S_5), (S_4, S_{10}), (S_7, S_7'), (S_8, S_8')	0	0	0
	(S_1, S_5), (S_2, S_5), (S_2, S_6)	2	$\pm 2V_{dc}$	50%
	(S_1, S_2), (S_1, S_4), (S_1, S_9), (S_2, S_7), (S_2, S_7'), (S_2, S_8), (S_2, S_8'), (S_2, S_9), (S_3, S_6), (S_3, S_9), (S_5, S_6), (S_5, S_7), (S_5, S_7'), (S_5, S_8), (S_5, S_8') (S_5, S_9), (S_5, S_{10}), (S_6, S_{10})	3	0, and $\pm 2V_{dc}$	50%
	(S_4, S_9)	5	0, $\pm V_{dc}$, and $\pm 3V_{dc}$	75%
	(S_9, S_{10})	5	0, $\pm 2V_{dc}$, and $\pm 4V_{dc}$	100%
	(S_1, S_3), (S_1, S_6), (S_3, S_4), (S_4, S_6)	6	$\pm V_{dc}$, $\pm 2V_{dc}$, and $\pm 3V_{dc}$	75%
	(S_1, S_7), (S_1, S_7'), (S_1, S_8), (S_1, S_8'), (S_1, S_{10}), (S_2, S_{10}), (S_3, S_7), (S_3, S_7'), (S_3, S_8), (S_3, S_8'), (S_3, S_{10}), (S_4, S_7), (S_4, S_7'), (S_4, S_8), (S_4, S_8'), (S_6, S_7), (S_6, S_7'), (S_6, S_8), (S_6, S_8'), (S_6, S_9)	7	0, $\pm V_{dc}$, $\pm 2V_{dc}$, and $\pm 3V_{dc}$	75%
	(S_7, S_8), (S_7, S_8'), (S_7, S_9), (S_7, S_{10}), (S_7', S_8), (S_7', S_8'), (S_7', S_9), (S_7', S_{10}), (S_8', S_9), (S_8', S_{10}), (S_8, S_9), (S_8, S_{10})	9	0, $\pm V_{dc}$, $\pm 2V_{dc}$, $\pm 3V_{dc}$, and $\pm 3V_{dc}$	100%
SCF	S_7 / S_7' / S_8 / S_8'	0	0	0
	S_1 / S_3 / S_4 / S_6	3	0, and $\pm 2V_{dc}$	50%
	S_2 / S_5 / S_9 / S_{10}	7	0, $\pm V_{dc}$, $\pm 2V_{dc}$, and $\pm 3V_{dc}$	75%
	(S_9, S_{10})	2	$\pm 2V_{dc}$	50%
	(S_1, S_5), (S_1, S_6), (S_3, S_4), (S_5, S_6), (S_5, S_9),	3	0, and $\pm 2V_{dc}$	50%
	(S_2, S_5), (S_2, S_{10})	5	0, $\pm V_{dc}$, and $\pm 2V_{dc}$	50%
	(S_2, S_9)	6	$\pm V_{dc}$, $\pm 2V_{dc}$, and $\pm 3V_{dc}$	75%
	(S_5, S_{10})	7	0, $\pm V_{dc}$, $\pm 2V_{dc}$, and $\pm 3V_{dc}$	75%
	All other combinations of two switches	0	0	0

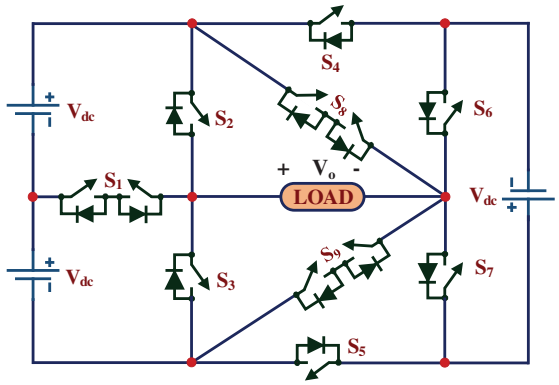


Fig. 4: 7 level symmetrical FT-MLI topology proposed in [7]

III. COMPARISON OF DIFFERENT FT-MLI

Fig. 5 shows a comparison of different topologies in OCF and SCF for a single switch (SS) and double switch (DS) fault. In the case of OCF in SS, the performance of the FT-MLIs is better as all these topologies have been designed on an SS fault-tolerant approach. Except for the topology of [5], the SS fault in all other three topologies results in 100% output voltage. In the case of DS fault, all the combinations of topology proposed in [4] result in 100% output voltage whereas in case of topology proposed in [6], 92% of the combinations result in voltage waveform higher than 50%. In the case of SCF in SS or DS, the output

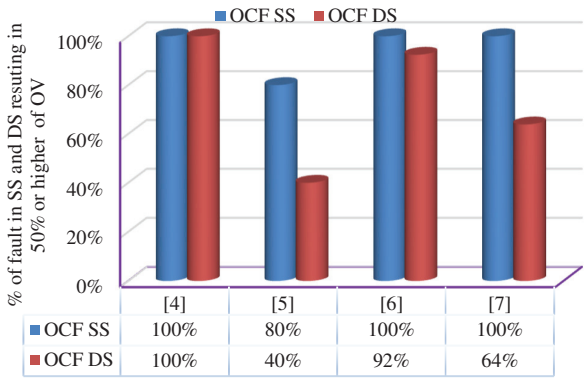
TABLE VII:
POSSIBLE SWITCHING STATES FOR TOPOLOGY PROPOSED IN [7]

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	V_o
0	1	0	0	1	1	0	0	0	$3V_{dc}$
0	1	0	0	1	0	1	0	0	$2V_{dc}$
0	1	0	0	0	0	0	0	1	
1	0	0	0	1	1	0	0	0	
1	0	0	0	1	0	1	0	0	V_{dc}
1	0	0	0	0	0	0	0	1	
0	0	1	0	1	1	0	0	0	
0	0	1	1	1	0	0	1	0	
0	0	1	0	1	0	1	0	0	0
0	0	1	0	0	0	0	0	1	
0	1	0	1	0	1	0	0	0	
0	1	0	0	0	0	0	1	0	
1	0	0	1	0	1	0	0	0	$-V_{dc}$
1	0	0	0	0	0	0	1	0	
0	1	0	1	0	0	1	0	0	
0	1	0	1	1	0	0	0	1	
0	0	1	1	0	1	0	0	0	$-2V_{dc}$
0	0	1	0	0	0	0	1	0	
1	0	0	1	0	0	1	0	0	
0	0	1	1	0	0	1	0	0	$-3V_{dc}$

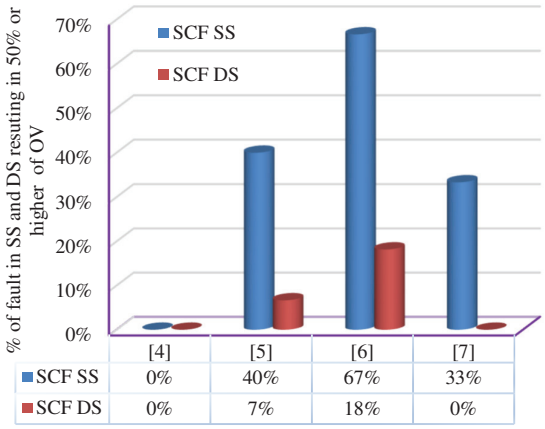
TABLE VIII:
OCF / SCF ANALYSIS OF TOPOLOGY PROPOSED IN [7]

Fault Type	Faulty Switch/es	N	Voltage Levels	% of OV
OCF	S_3 / S_4 / S_5 / S_6 / S_7	5	0, $\pm V_{dc}$, and $\pm 2V_{dc}$	67%
	S_1 / S_2 /S_8 / S_9	7	0, $\pm V_{dc}$, $\pm 2V_{dc}$, and $\pm 3V_{dc}$	100%
	(S_1, S_2), (S_1, S_3), (S_4, S_8), (S_5, S_9)	0	0	0
	(S_2, S_5), (S_2, S_6), (S_3, S_4), (S_3, S_7)	3	0, and $\pm V_{dc}$	33%
	(S_1, S_4), (S_1, S_5), (S_1, S_6)	3	0, and $\pm 2V_{dc}$	67%
	(S_2, S_3)	4	$\pm V_{dc}$, and $\pm 2V_{dc}$	67%
	(S_1, S_7), (S_2, S_4), (S_2, S_7), (S_2, S_8), (S_2, S_9), (S_3, S_5), (S_3, S_6), (S_3, S_8), (S_3, S_9), (S_4, S_5), (S_4, S_6), (S_4, S_7), (S_4, S_9), (S_5, S_6), (S_5, S_7), (S_5, S_8), (S_6, S_7), (S_6, S_8), (S_6, S_9), (S_7, S_8), (S_7, S_9)	5	0, $\pm V_{dc}$, and $\pm 2V_{dc}$	67%
	(S_1, S_8), (S_1, S_9), (S_8, S_9)	7	0, $\pm V_{dc}$, $\pm 2V_{dc}$, and $\pm 3V_{dc}$	100%
SCF	S_1 / S_6 / S_7	5	0, $\pm V_{dc}$, and $\pm 2V_{dc}$	67%
	S_2 / S_3	0	0	0
	S_4 / S_5 / S_8 / S_9	3	0, and $\pm V_{dc}$	33%
	All other combinations of switches	0	0	0

voltage is zero for the topology proposed in [4]. The performance of the topology proposed in [6] has the better fault-tolerant ability as 67% of the combinations result in higher voltage in SS fault whereas for the topologies proposed in [5] and [7], the higher number of switch SCF results in lower or zero output voltage. In the case of SCF in two switches, the performance is not good as only 18% of the two-switch combination results in higher voltage for the topology of [6].



(a)

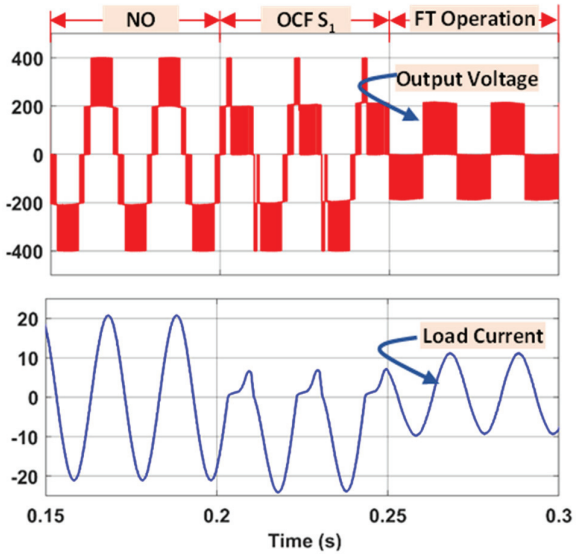


(b)

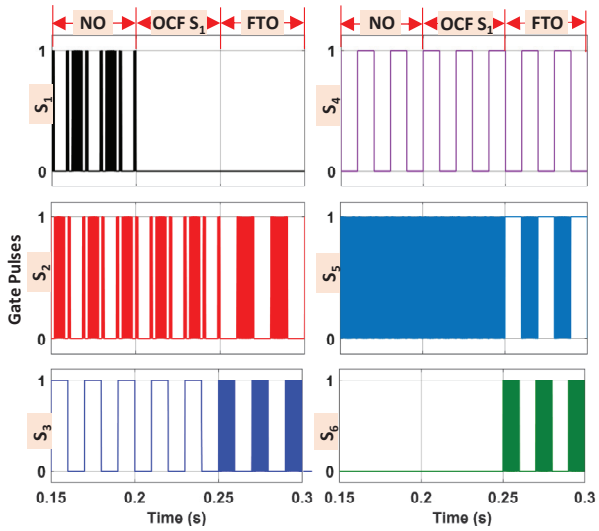
Fig. 5: Comparison of different topologies for (a) OCF and (b) SCF

IV. SIMULATION RESULTS AND DISCUSSION OF FT 5 LEVEL T-TYPE INVERTER TOPOLOGY

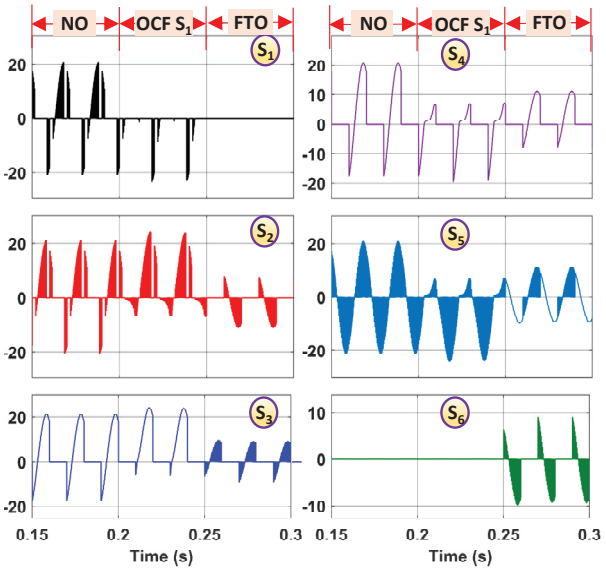
The FT topology proposed in [4] has been simulated and the results with different fault cases have been analyzed. Input voltage has been selected as 400V with a load parameter of 10Ω resistor and 50mH inductor connected in series. A conventional level-shifted PWM technique has been used with a carrier frequency of 2.5 kHz. This topology has been simulated for OCF and SCF for switches S_1 and S_5. Fig. 5 shows the simulation results of OCF and SCF to switch S_1. Fig. 6 (a) shows the output voltage and current waveform in case of OCF to switch S_1. In normal operating (NO) conditions, the output voltage is a perfect five-level waveform with a peak output voltage of 400V. In the case of OCF to switch S_1, the peak of the output voltage in positive half becomes 200V which leads to the distortion in the output voltage and current waveforms. As the topology is designed for the fault-tolerant feature, the FT operation gives the three level voltage waveform with the reduction in the peak voltage as 200V. Fig. 6 (b) shows the gate pulses in all these cases, i.e., NO condition, OCF to S_1 and FT operation. Fig. 6 (c) shows the six switch currents.



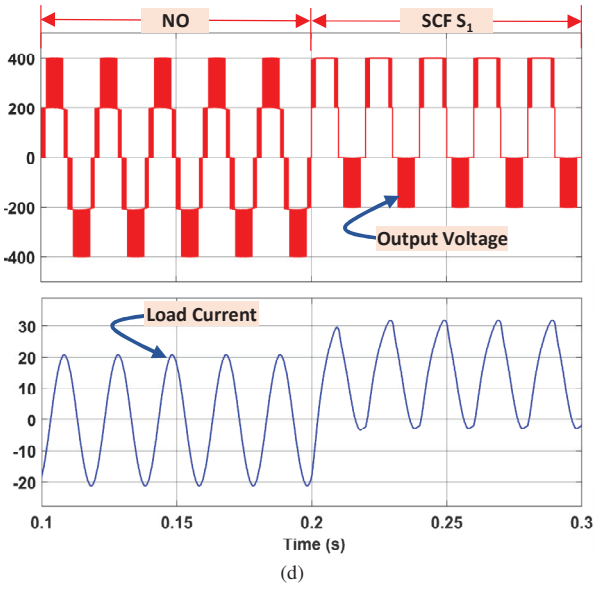
(a)



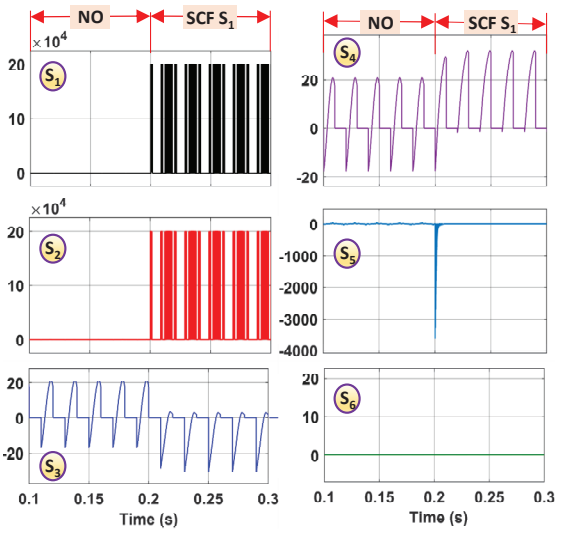
(b)



(c)



(d)

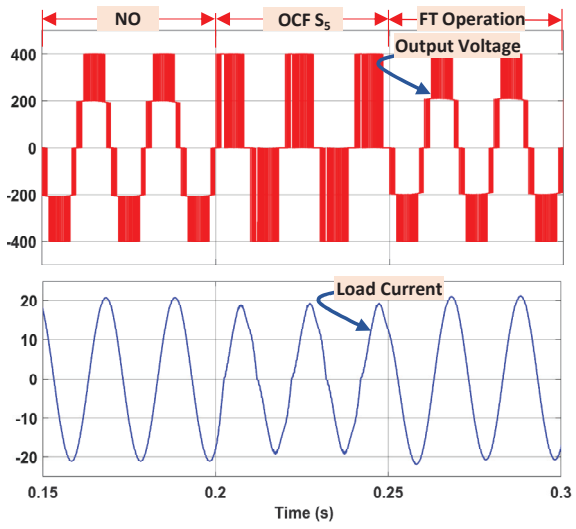


(e)

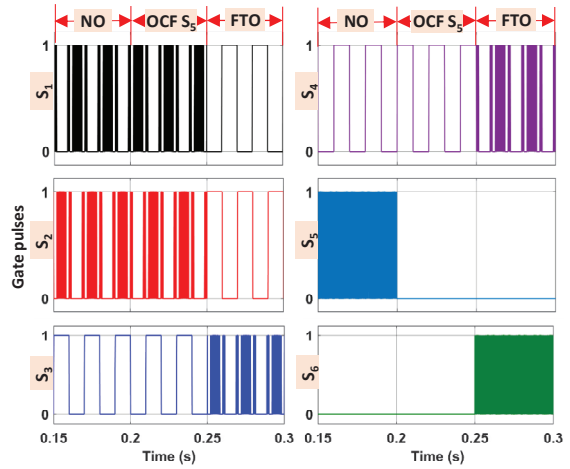
Fig. 6: Simulation results with (a) output voltage and current with OCF to switch S_1, (b) gate pulses with OCF to S_1, (c) current for all switches with OCF to S_1, (d) output voltage and current with SCF to switch S_1, (e) current for all switches with SCF to S_1.

Fig. 6 (d) depicts the output voltage and load current in case of SCF to switch S_1. With SCF to switch S_1, the negative of the output voltage becomes 200V, however the more serious issues appears when the observation regarding the switch currents are taken into the consideration which is shown in Fig. 6 (e).

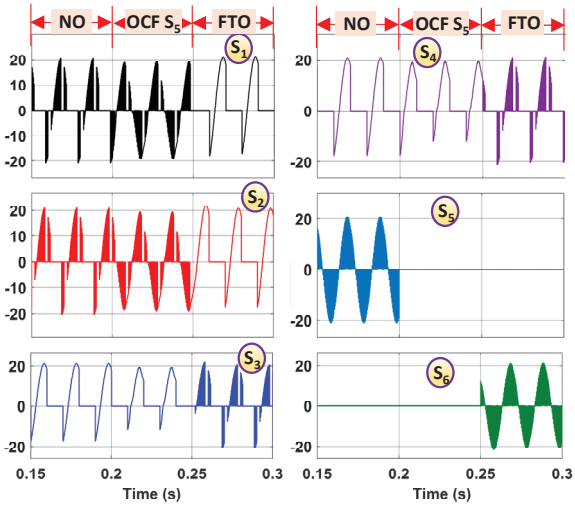
The simulation results with OCF and SCF to switch S_5 has been depicted in Fig. 7. With the OCF to switch S_5, the before and post fault condition gives 5 level output voltage waveform. With OCF to S_5, the mid-point of the dc-link is disconnected and the converter works as H-bridge. Fig. 7 (b) shows the gate pulses for the NO, during fault and FT operation. As OCF occurs to switch S_5, switch S_6 is utilized to get the same number of levels are pre-fault or normal operating conditions. Fig. 7 (c) shows the switch current for all the switches in case of OCF to switch S_5.



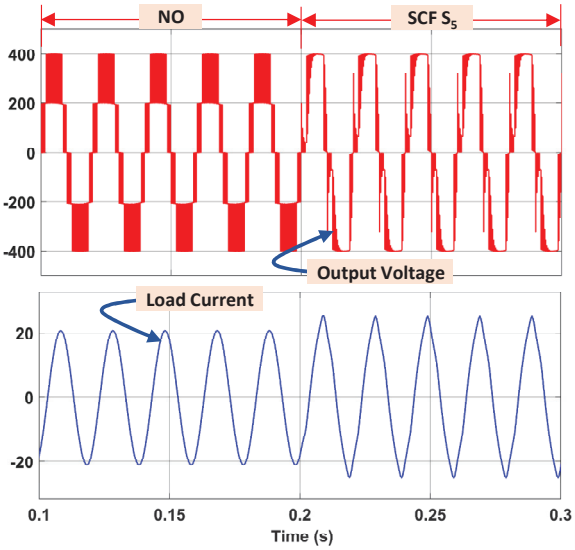
(a)



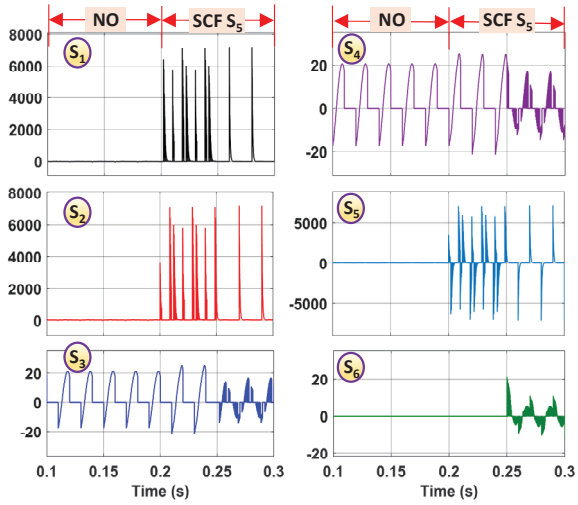
(b)



(c)



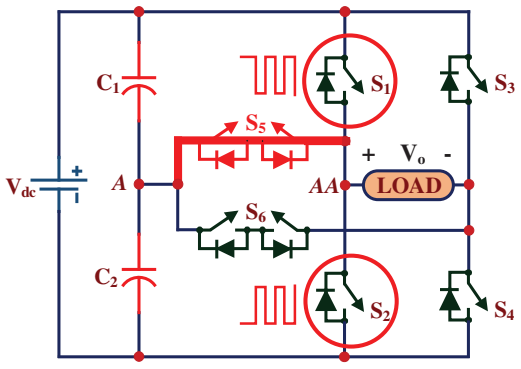
(d)



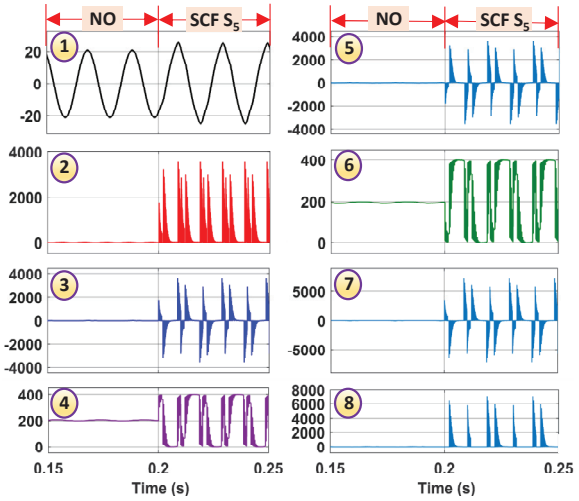
(e)

Fig. 7: Simulation results with (a) output voltage and current with OCF to switch S_5, (b) gate pulses with OCF to S_5, (c) current for all switches with OCF to S_5, (d) output voltage and current with SCF to switch S_5, (e) load current for all switches with SCF to S_5.

Fig. 7 (d) shows the performance of the topology with output voltage and current waveforms and Fig. 7 (e) shows the switch currents in the case of SCF to switch S_5, respectively. The SCF in one switch will lead to a high magnitude of currents due to the short-circuiting of the source or capacitors. Fig. 8 (a) shows the schematic of the topology with SCF in switch S_5. In this case, the mid-point of capacitor "*A*" and the one load terminal "*AA*" get shorted. If switch S_1 is turned ON, the capacitor C_1 is discharged to zero with a large discharge current flowing through capacitors. Capacitor C_2 attends a voltage of magnitude V_{dc}. A similar pattern has been observed in the case of switch S_2. Fig. 8 (b) show the different voltage and currents of different capacitor and switches. The SCF causes the increase in the currents in switches S_1, S_2, and S_5 and capacitors C_1 and C_2 to a very high value. Such a high value of current will lead to the permanent failure of all these switches and capacitors.



(a)



(b)

Fig. 8: (a) Schematic of the 5L T-type topology with SCF to switch S_5, and (b) simulation results with [1] load current, [2] input current, [3] current of C_1, [4] voltage of C_1, [5] current of C_2, [6] voltage of C_2, [7] current of switch S_5 and [8] current of switch S_1.

V. Conclusion

In this paper, reliability assessment of recently proposed FT-MLI topologies has been carried out. Four different FT-MLI have been analyzed for OCF as well as SCF in either a single switch or a combination of two switches. The analysis has been performed based on the redundant switching states. From the analysis, it has been concluded that in the case of single switch having OCF, the output voltage is maintained at a higher value for all the topologies. However, in the case of OCF in two switches, the fault leads to lower output voltage. Similarly, in case of SCF, the performance is not good as a higher percentage of switches or combinations of switches results in lower or zero output voltage. Therefore, based on the analysis, there is a need for the design of robust fault-tolerant topologies which can handle different types of faults in at least two switches. A 5 level T-type MLI has been simulated and results corespindgin to various fault cases have been presented.

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