A Seamless Modulation Strategy for Step-up/down Partial Power Processing Converter (SUD-P3C)

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Keywords

« DC-DC converter», « Seamless transfer», «Efficiency», «DC voltage control», «Partial power processing».

Abstract

This paper proposes a seamless modulation strategy for a step-up/down partial power processing converter (SUD-P3C), to realize smooth mode transition and continuous output regulation. Due to the implementation of zero volt switching (ZVS) on the high voltage side, the proposed method effectively suppresses voltage spikes caused by hard switching of the high voltage side switches, resulting in improved system reliability. Moreover, according to the small-signal analysis, the two operating modes have the same output-to-control transfer function, so the converter can adopt only one unified controller rather than two dedicated ones and reduce controller design complexity. A 400 V-3 kW prototype has been built, and the experimental results verified the effectiveness of the proposed modulation strategy. Compared to the conventional modulation strategy, the power losses are reduced by up to 14 % due to ZVS switching.

Introduction

Partial Power Processing (PPP) technology has been widely used in different applications, such as solar photovoltaic systems [1]-[4], energy storage systems (ESSs) [5], and electric vehicle (EV) fast-charging stations [6],[7]. In PPP converters (P^3C), only a small portion of the power being processed, i.e., the most considerable amount of energy flows directly from the source to the load without being processed, resulting in power converter downsizing and efficiency improvement.

Depending on the regulation target, P^3C configurations can be divided into two main categories: Parallel-connected configurations (P-P^3C) and Series-connected configurations (S-P^3C) [8]. The P-P3Cs are usually employed in PV module strings, also widely called differential power processing, which maintains distributed local maximum power point operation by only processing a fraction of the total power. On the other hand, for S-P^3C, the output voltage regulation is achieved by adjusting the difference between the input and output voltages. S-P^3Cs can be further divided into three types: step-up P^3C (SU-P^3C), step-down P^3C (SD-P^3C), and step-up/down P^3C (SUD-P^3C). The experimental results in [9] reveal that the SUD-P^3C processes the least active power over the same voltage variation range compared to the other type of P^3Cs, resulting in higher efficiency and power density. Ref [10] proposed a unified modulation strategy for SUD-P^3C, simplifying the pulse width modulation (PWM). However, the different operation modes in SUD-P^3C pose new challenges, such as achieving reliable regulation between different modes and smooth mode transition.

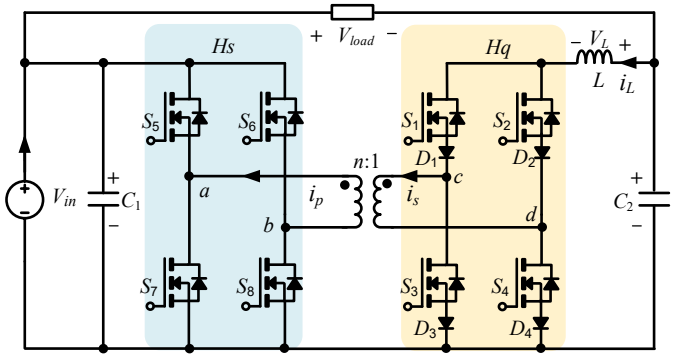


Fig. 1: Configuration of the SUD-P^{3}C in [10].

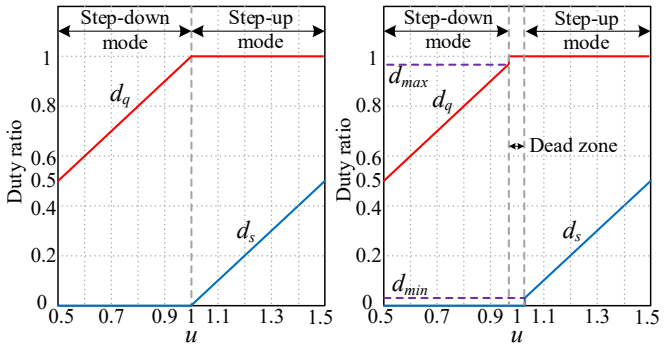


Fig.2: Duty ratios variation with u (a) without dead zone; (b) with dead zone

In addition, the converter suffers from mode transferring issues such as discontinuous current and power spikes due to parasitic parameters existing in the power stage when the transition goes through the region where the output voltage is very closed or equal to the input voltage. Therefore, this paper proposed a novel modulation strategy that achieves seamless mode transition, continuous output regulation, and ZVS operation of the high voltage side switches.

Topology and modulation

A. Mode Transfer Issue in Conventional Modulation Strategy

Fig.1 shows the topology of SUD-P^{3}C in [10], which consists of two H-bridges, i.e., *Hq* and *Hs*, and a high-frequency transformer. The switches in *Hq* and *Hs* are modulated by the duty ratio d_q and d_s, respectively. In the conventional modulation strategy, the diagonal switches have the same duty ratio, while the duty ratios for upper and lower switches in the arm are phase-shifted by 180°. d_q and d_s in [10] are expressed by the unified modulation ratio u, as given in (1) and (2).

$$d_q = \begin{cases} u \ , 0.5 \le u < 1 \\ 1 \ , 1 \le u \le 1.5 \end{cases} \tag{1}$$

$$d_s = \begin{cases} 0 \quad , 0.5 \le u < 1 \\ u - 1 \ , 1 \le u \le 1.5 \end{cases} \tag{2}$$

Obviously, $S_{1\text{-}4}$ are switched in high frequency while $S_{5\text{-}8}$ keep OFF when $0.5 \le u < 1$, i.e., the converter operates as the traditionally isolated Boost converter. Similarly, it operates as an isolated Buck converter at $1 \le u \le 1.5$, when PWM signals drive $S_{5\text{-}8}$ while $S_{1\text{-}4}$ keeps ON. $D_{1\text{-}4}$ avoids blocking the reverse voltage when C_2 voltage is negative. Neglecting power losses, the following function expresses the converter voltage gain.

$$G(u) = \frac{V_{load}}{V_{in}} = \frac{n + 2u - 2}{n} \ , 0.5 \le u \le 1.5 \tag{3}$$

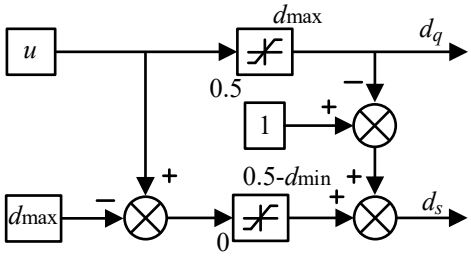
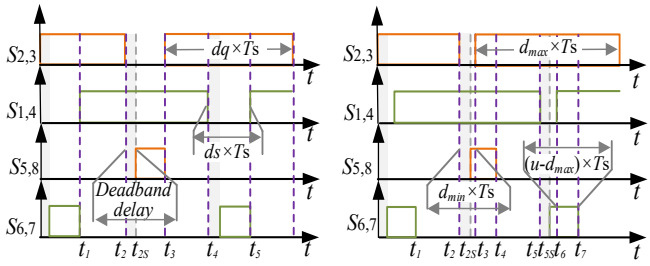


Fig.3: Diagram of the seamless modulation strategy.



(a) $0.5 \le u < d_{max}$ (b) $d_{max} \le u < 1.5\text{-}2d_{min}$

Fig.4: PWM signals of the proposed modulation strategy.

Fig. 2 (a) indicates the operation area of two modes when the dead zone is not taken into consideration. Ideally, the mode transfer occurs at $u = 1$, i.e. $V_{load} < V_{in}$ when $u < 1$ and $V_{load} > V_{in}$ when $u > 1$.

When $u = 1$, the voltage over capacitor C_2 is zero, i.e. $V_{in} = V_{load}$, and thereby the source is directly connected to the load, and the converter processes zero power, thereby the system presents the peak efficiency. However, as u gradually approaches 1, the switching time will become very short, e.g., at a switching frequency (f_{sw}) of 100 kHz and $0.99 < u < 1.01$, the OFF time of $S_{1\text{-}4}$ and the ON time of $S_{5\text{-}8}$ are less than 100 ns, which is very challenging for switches and drivers to complete commutation. As presented in [10], incomplete charging and discharging of the switch's capacitor leads to a non-ideal voltage across the transformer.

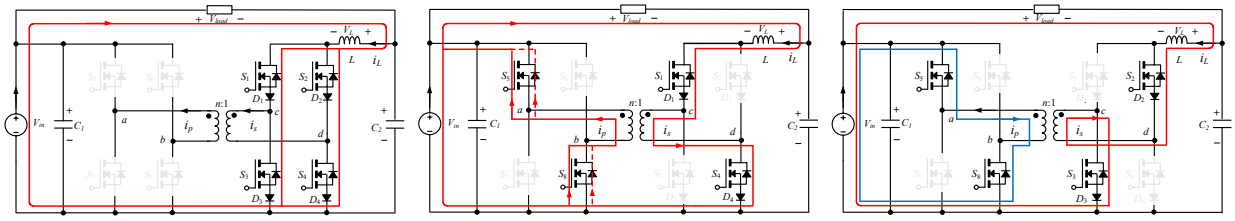
Furthermore, the duty cycle limitation is necessary to recharge the bootstrap capacitor periodically when using half-bridge gate drivers. As a result, the duty cycle limitation is usually implemented to ensure the switching-time constraint, resulting in the dead zone in the duty cycle, as shown in Fig.2 (b). Define $d_{max} = 1 - d_{min}$, and there is a nonadjustable voltage range, i.e., $((1 \pm (2d_{min}/n)) \times V_{in}$. When the SUD-P^{3}C is operated under the closed-loop control, the discontinuity leads to random jumps in the regulated voltage, i.e., the converter works at burst mode. It increases the controller design's complexity and leads to low-stability voltage regulation when u approaches 1.

B. The proposed Novel modulation strategy

In order to overcome such mode transferring issues, a novel modulation strategy is proposed and expressed in (4) and (5).

$$d_q = \begin{cases} u & , 0.5 \le u < d_{\max} \\ d_{\max} & , d_{\max} \le u \le 1.5 - 2 \cdot d_{\min} \end{cases} \tag{4}$$

$$d_s = \begin{cases} 1 - u & , 0.5 \le u < d_{\max} \\ u - d_{\max} + d_{\min} & , d_{\max} \le u \le 1.5 - 2 \cdot d_{\min} \end{cases} \tag{5}$$



(a) State 1 in boost mode (b) State 2 in boost mode (c) State 3 in buck-boost mode

Fig. 5: Equivalent circuits for boost mode and buck-boost operating modes.

Fig. 3 shows the diagram of the proposed modulation strategy. Fig.4 (a) and (b) show the PWM signals when $0.5 \le u < d_{max}$ and $d_{max} \le u <1.5\text{-}2d_{min}$, respectively. When $0.5 \le u < d_{max}$, d_q and d_s are complementary. The operating mode is called boost mode as the converter works as an isolated boost converter, which has four symmetrical operating states. The first two states are analyzed below.

State 1 in boost mode: t_1 - t_2

From t_1 to t_2, $S_{1\text{-}4}$ keeps ON while $S_{5\text{-}8}$ keeps OFF. Power is transferred from source to load directly, as shown in Fig.5 (a). v_L can be expressed by (6).

$$v_L = L \cdot \frac{di_L}{dt} = v_{in} - v_{load} \tag{6}$$

State 2 in boost mode: $t_2 - t_3$

At t_2, S_2 and S_3 are turned off, i_L is forced to flow through $S_{1,4}$. In *Hs*, i_p flows through the antiparallel diodes of S_5 and S_8, dash line in Fig.5 (b), until S_5 and S_8 are turned on at t_{2S}, solid line in Fig.5 (b). Therefore, the dead-band delay between $S_{2,3}$ and $S_{5,8}$ as well as $S_{1,4}$ and $S_{6,7}$ can guarantee ZVS switching of $S_{5\text{-}8}$, as shown in the grey shaded area of Fig.4. v_L is expressed by (7).

$$v_L = L \cdot \frac{di_L}{dt} = v_{in} - v_{load} - \frac{v_{in}}{n} \tag{7}$$

Consequently, when $0.5 \le u < d_{max}$, this novel modulation strategy's voltage gain can still be expressed by (3). When $u \ge d_{max}$, d_q is limited at d_{max} while $d_s = u - d_{\max} + d_{\min}$. To ensure d_s is smaller than 0.5, the maximum of u is $1.5\text{-}2d_{\min}$. Compared to the boost mode, two symmetrical operating states are added in this operating mode. v_L for State1 and State 2 in this mode can also be expressed by (6) and (7), respectively. Fig.5 (c) shows the equivalent circuit for State 3 in this operating mode. At t_3, S_2 and S_3 are turned on again. i_L migrates from $S_{1,4}$ to $S_{2,3}$. As a result, the currents across the transformer (i_p and i_s) start to reduce. When currents pass through the $S_{1,4}$ and $S_{2,3}$ are equal, i_p and i_s are zero. Then i_p reversely increases. Due to the blocking of D_1 and D_4, the current pass through $S_{1,4}$ continues to reduce until it reaches 0. In contrast, the current pass through $S_{2,3}$ continues to increase. v_L in this period is expressed by (8).

$$v_L = L \cdot \frac{di_L}{dt} = v_{in} - v_{load} + \frac{v_{in}}{n} \tag{8}$$

Applying the volt-second balance principle, the output voltage function for $u \ge d_{\max}$ is derived, which is the same as for $u < d_{\max}$, thereby the $G(u)$ of the proposed strategy is expressed by (3), but the range of u is reduced to 0.5 to $1\text{-}2d_{min}$. As a result, the maximum output voltage is reduced to $(n + 1\text{-}4d_{min}) \times V_{in}/n$. Although the mode switching occurs at $u = d_{\max}$, the output voltage equaling the input voltage still occurs when u=1. In other words, this operating mode achieves step-down voltage regulation when $u \ge d_{max}$ and step-up voltage regulation at $u \ge 1$, and is called buck-boost mode. Similar to the boost mode, the minimum switching-off time on $S_{1\text{-}4}$ is ensured. On the one hand, the regulation dead zone when u approach 1 is avoided. On the other hand, the transformer is not short-circuited by the low-voltage side when $u = 1$. As a result, the proposed strategy addresses the transfer issue, and the only sacrifice is that the maximum regulation voltage is slightly reduced. Although compared to the step-up mode in the conventional modulation strategy, the proposed modulation strategy has a bit higher processing power due to the additional operating states.

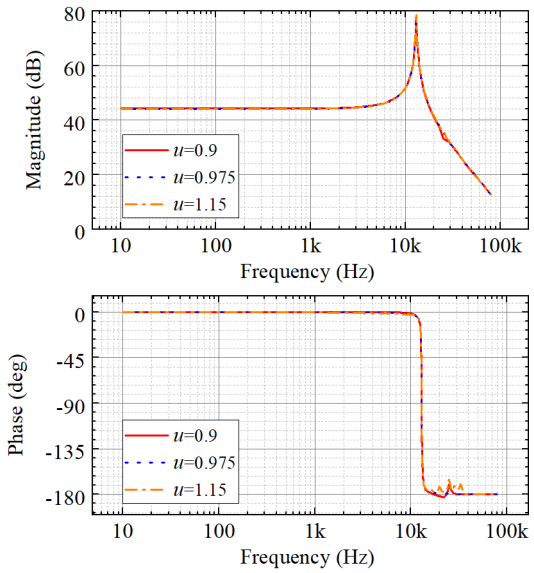


Fig. 6: Frequency response of the control to output voltage transfer function.

Thanks to the ZVS switching of $S_{5\text{-}8}$, the proposed strategy improves efficiency when $u < d_{\max}$ and suppresses spikes caused by the hard switching of $S_{5\text{-}8}$ when $u \geq d_{\max}$.

C. Small Signal Analysis

Based on the operation principle, the averaged equations of inductor voltage and the capacitor current for the two modes are the same,

$$L\frac{d\langle i_L\rangle_{Ts}}{dt} = \frac{(n+2u-2)\langle v_{in}\rangle_{Ts}}{n} - \langle v_{load}\rangle_{Ts} \tag{9}$$

$$C_2\frac{d\langle v_{C2}\rangle_{Ts}}{dt} = \frac{\langle v_{load}\rangle_{Ts}}{R} - \langle i_L\rangle_{Ts} \tag{10}$$

Introducing perturbation to the state variables and other quantities and neglecting the second-order terms, the linearized small-signal equations are given by (11) and (12).

$$sL\,\hat{i}_L = \frac{\hat{v}_{in}}{n}(n+2u-2) + \frac{2V_{in}}{n}\hat{u} - \hat{v}_{load} \tag{11}$$

$$sC_2\left(\hat{v}_{in} - \hat{v}_{load}\right) = \frac{\hat{v}_{load}}{R} - \hat{i}_L \tag{12}$$

Arranging (12), $\hat{i}_L$ is derived.

$$\hat{i}_L = \frac{\left(1+sRC_2\right)\hat{v}_{load}}{R} - sC_2\hat{v}_{in} \tag{13}$$

Introducing (13) to (11), the control-to-output transfer is derived by (14).

$$\left.\frac{\hat{v}_{load}}{\hat{u}}\right|_{\hat{v}_{in}=0} = \frac{2RV_{in}}{s^2nLC_oR + snL + nR} \tag{14}$$

In order to verify the proposed small-signal analysis, the AC sweep simulation was carried out in the converter circuit model constructed by PLECS. The system specifications are listed in Table. I.

Table I: System specification of the simulation

Name	V_{in}	L	C_2	n	R	f_{sw}	d_{max}
Value	400 V	15 µH	10 µF	5:1	70 Ω	100 kHz	0.95

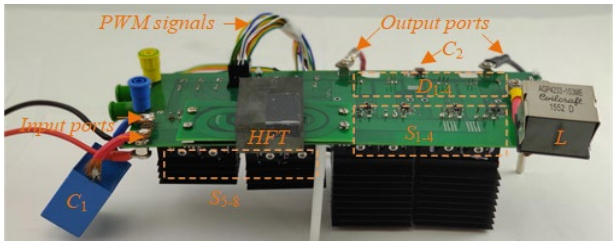


Fig. 7: Experimental prototype of the SUD-P^{3}C.

TABLE II: Main Parameters of prototype

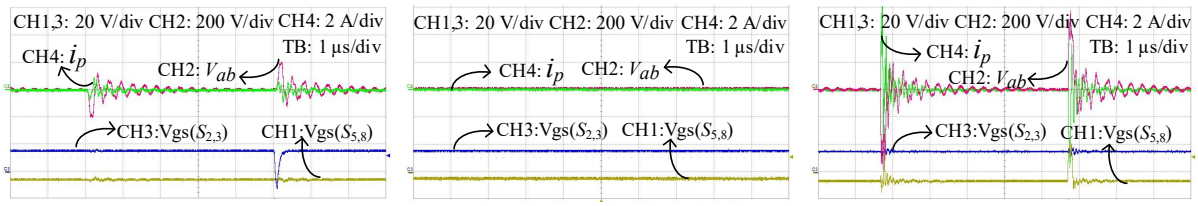
Parameter	Value	Notes
S_{1-4}	IRF200P223, 200 V/100 A	R_{dson}: 8.5 mΩ,
S_{5-8}	IMW65R072M1H, 650 V/26 A	R_{dson}: 72 mΩ, C_{oss}:100 pF
D_{1-4}	V30200C, 200 V/2×15 A	V_F @ I_F = 15 A: 0.648 V
L	AGP4233-153ME	Inductance: 15 µH, R_{dc}:2.85 mΩ
HFT	PCB transformer	20:4, Core: ELP58/11/38 N87

The frequency response curves in the case of u = 0.9 (Boost mode, V_{load} = 384 V) and u = 0.975 (Boost-buck mode, V_{load} = 396 V) and u = 1.15 (Boost-buck mode, V_{load} = 424 V) are plotted in Fig.6. The proposed strategy has the same frequency response for different operating modes and voltage regulation ranges. In the novel strategy, the transfer functions are almost identical in the frequency spectrum of 10 Hz - 80 kHz, so only one unified controller is required for the two operating modes.

Experimental results

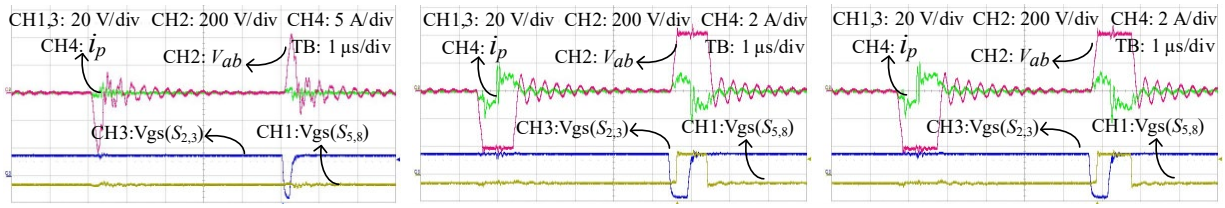
A 3kW prototype, as shown in Fig.7, is designed, constructed and tested in order to verify the proposed modulation strategy. The specifications of the experimental system are listed in Table I. Table. II shows the parameters of the main components.

A 200 ns dead time is set to ensure ZVS switching of S_{5-8}. Fig. 8 shows the operating waveforms of the conventional modulation strategy in [10]. In Fig.8 (a), S_{5-8} can't be fully charged or discharged due to the too-short switching time, resulting in V_{ab} being only half of the theoretical value. The converter does not process power at u = 1 because S_{1-4} is ON while S_{5-8} is OF, as shown in Fig.8 (b). The hard switching of S_{5-8} results in a large voltage spike, 577 V, as shown in Fig.8 (c). As shown in Fig.9, the proposed modulation strategy ensures enough OFF time for S_{5-8} and ON time for S_{1-4} even at u = 1, and the voltage spike is suppressed. In order to observe the behavior during the mode transition, the control signal u was programmed to increase linearly from 0.7 to 1.2, as shown in Fig. 10. The variation of output is continuous and linear. Moreover, the transformer's voltage gap is avoided compared to the waveforms reported in [10]. Therefore, the proposed strategy effectively solves the switching issue between different modes. Fig. 11 shows the output voltage and system efficiency versus u for the modulation strategy in [10] and the proposed one.



(a) u = 0.99 (b) u = 1 (c) u = 1.01

Fig. 8: Operating waveforms of conventional modulation strategy in [10].



(a) u = 0.98 (b) u = 1 (c) u = 1.01

Fig. 9: Operating waveforms of proposed conventional modulation strategy.

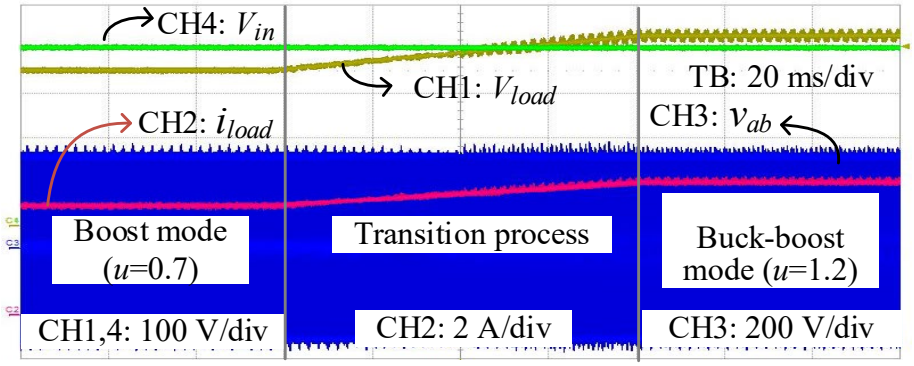


Fig. 10: Waveforms of operating mode transition.

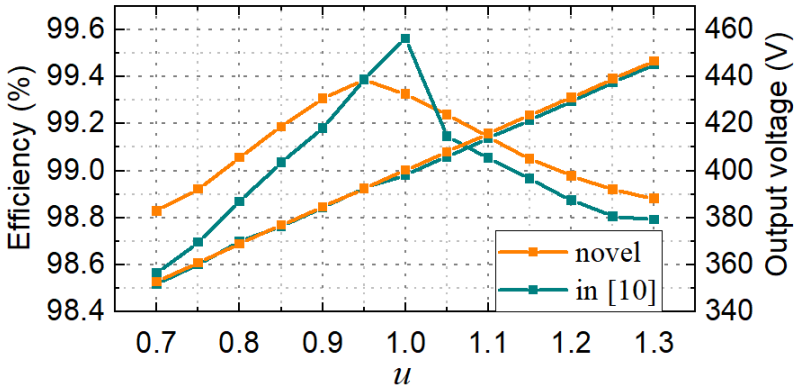


Fig. 11: Output voltage and system efficiency versus u.

The output voltage curve with the novel proposed strategy is highly linear, consistent with Fig.10. The novel approach presents a higher efficiency when $u < 0.95$ and a 14 % reduction in power losses at u = 0.7 due to ZVS switching.

CONCLUSION

This paper presents an improved modulation strategy with seamless mode switching, solving the stability problem when the input and output voltages are close to each other and achieving continuous regulation.

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