Optimized Control Scheme to Achieve ZVS for the Complete Pre-Charging Phase of Supercapacitors with a 500 kHz SiC- and GaN-Based Dual Active Bridge

Patrick Lenzen, Martin Pfost
TU Dortmund University
Martin-Schmeisser-Weg 4
44227 Dortmund, Germany
Phone: +49 231-7557844
Email: patrick.lenzen@tu-dortmund.de
URL: https://ewa.etit.tu-dortmund.de/

Acknowledgments

This contribution was supported by the European Union and the Ministry of Economic Affairs, Innovation, Digitalization, and Energy of the State of North Rhine-Westphalia as part of the ERDF program under the funding code EFRE-0801621.

Keywords

≪Supercapacitor≫, ≪Dual Active Bridge (DAB) DC-DC converter≫, ≪Zero-voltage switching≫, ≪Energy storage≫, ≪High frequency power converter≫

Abstract

Large energy storage systems are used in many applications. If they are not in operation continuously, they will discharge themselves. To restart the operation, the supercapacitors should be pre-charged again to reach the nominal voltage range. Mostly, the capacitors are connected to a source via a DC/DC converter. For a fast reaction on load transients, fast-switching DC/DC converters are needed. Due to the high switching frequencies, soft switching is essential to keep the losses low. This is important for the normal operation but also for the pre-charging phase because pre-charging takes up to several minutes for large capacities. This work presents a zero-voltage switching (ZVS) analysis and extended-phase shift (EPS) modulation to reach ZVS switching for all semiconductors of the DC/DC converter during the complete pre-charge procedure. The analysis is done with a capacitance time-domain-based model and experimentally validated on a prototype.

Introduction

Energy-storage systems with supercapacitors become more and more attractive for many applications, e.g. for peak shaving in industrial applications like intralogistics. Supercapacitors have the advantage of a 500 times larger cycle life and higher power densities [1]. Nevertheless, supercapacitors have higher self-discharge than batteries [2]. If the system is not used continuously, the supercapacitor might be completely discharged and must be charged from 0 V before normal operation.

In industrial applications, AC and DC grids are used to supply all electrical loads. Lower losses can be reached with high voltage DC grids. In our case the nominal grid voltage is 650 V, much higher than the voltage of the supercapacitor modules, here 48 V. Therefore, the connection of supercapacitors to the DC grid is mostly handled by bidirectional DC/DC converters to overcome the voltage difference. Dual Active Bridges (DAB) and resonant converters, e.g CLLC converters, are commonly used bidirectional DC/DC

converters with galvanic isolation, high conversion ratio possibility, and full bidirectional power flow. The DAB topology was first introduced in [3] and the CLLC converter in [4]. For high currents, the CLLC converters will need synchronous rectification to lower the losses. But for high switching frequencies, a realization of the synchronous rectification is challenging. Therefore and due to the multiple control options, the DAB is the more attractive choice. If using large supercapacitors, in this case 165 F, the pre-charging process to 48 V with constant 50 A takes around 2 min. For converters operating with high switching frequencies, which is necessary to reach a fast reaction on load transients, low switching losses are essential. Switching losses can be reduced by using zero-voltage switching. Nevertheless, a minimum dead time is required to reach zero-voltage switching (ZVS).

For the design process of the converter, the loss calculation for the starting process is as important as for the steady-state performance. To achieve soft switching during the pre-charging process, different charging techniques with soft switching are proposed in [5]-[6]. [5] presents a controlled trapezoidal current modulation. The authors calculate the switching points for zero-current switching (ZCS) from ideal current curves. However, the switching point is not controlled, the real current differs slightly from the ideal calculation. For high switching frequencies with high $\mathrm{d}i/\mathrm{d}t$, small time deviations result in large current changes. Therefore, switching at 0 A is not realizable and results in high switching losses.

[6] presents different pre-charging techniques. One solution uses a controlled primary and secondary full bridge. The source full bridge is under duty cycle control and the load full bridge has a constant duty cycle of 50 %. The two rectangular voltages are phase-shifted. The parameters are optimized with a current-based ZVS analysis. This work only considers if the current through the inductor flows in the right direction to reach ZVS. However, for fast-switching converters, the current-based ZVS analysis is not sufficient. This is because at low power and low currents, the dead time of the half bridge is often not large enough and the current changes during the transition. Moreover, the current direction can be reversed and it is impossible to reach full ZVS.

This paper presents an optimized extended phase-shift modulation scheme to reach ZVS for all switches during the pre-charging process for a fast-switching 500 kHz DAB. The ZVS area calculation relies on a capacitance time-domain-based model (CTD) as previously presented in [7]. The calculation is validated on a prototype.

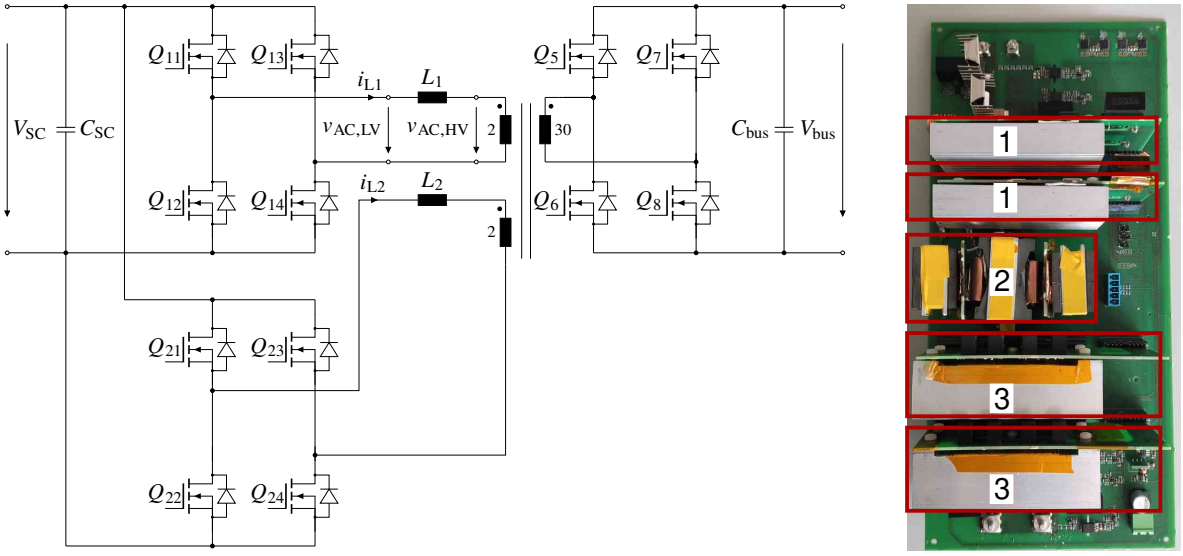
Proposed System

The schematic of the proposed bidirectional DAB is shown in Fig. 1(a) and realized as a modular design with two LV and one HV full bridge, which was first introduced in [8]. For the LV and the HV full bridge, EPC GaN HEMTs and Wolfspeed SiC MOSFETs, respectively, are used. The practical realization is shown in Fig. 1(b). The normal operation voltage V_{SC} on the supercapacitor varies between 38 V and 48 V with a nominal value of 43 V and the DC bus voltage V_{bus} ranges from 580 V to 750 V with a nominal voltage of 650 V. The switching frequency is 500 kHz and the permissible maximal dead time is set to 100 ns. The DAB is in normal operation controlled by single phase-shift modulation.

Extended Phase-Shift Modulation

At the beginning of the pre-charging process of the supercapacitor, the voltage at the capacitor is usually 0 V. The modulation scheme should minimize the inrush current and enable soft switching also in this case. As previously described, for simplicity the converter is controlled by phase-shift modulation. Three different phase-shift modulation schemes are possible: Firstly, the single phase-shift scheme where the duty cycle of the primary and the secondary bridge voltage is $v_{\mathrm{AC,LV}} = 50\,\%$. The primary and secondary voltages are shifted by the angle φ. Secondly, the extended phase shift where the voltage of the primary HV bridge $v_{\mathrm{AC,HV}}$ has a duty cycle D_{p} which is lower than 50 % (see Fig. 2). Thirdly, the triple phase shift where the duty cycle D_{s} of the voltage of the secondary LV bridge $v_{\mathrm{AC,LV}}$ is lower than 50 % in addition to the previous shifts.

For fast-frequency converters, it is obvious that the modulation scheme should be as simple as possible. However, if using the single-phase-shift control, ZVS is not possible for all switching events. If the supercapacitor is discharged, the current is triangular. Consequently, ZVS will only be achieved for the



(a) (b)

Fig. 1: (a) Schematic of the converter with two LV full bridges. The series inductors are placed on the LV side (L_1 and L_2). The supercapacitor is connected to V_{SC} and the DC bus to V_{bus}. (b) Modular realization of the converter. (1) HV half bridge (Q_5 - Q_6, Q_7 - Q_8), (2) Transformer, series inductors L_1, L_2, (3) LV full bridge (Q_{11} - Q_{14}, Q_{21} - Q_{24}). Transformer and full bridges are realized on pluggable PCBs.

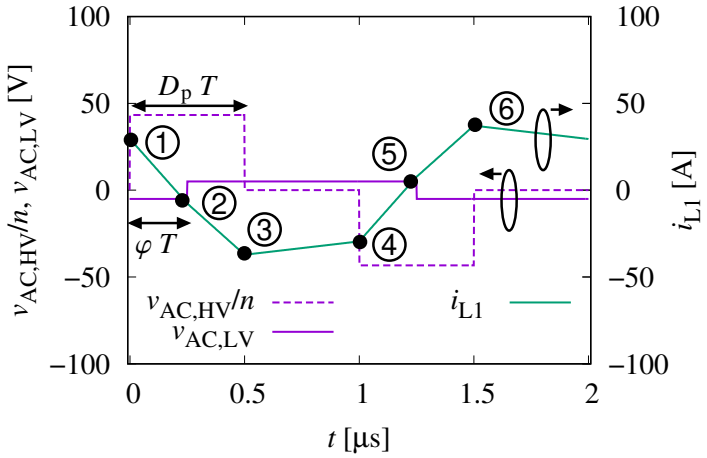


Fig. 2: Extended phase-shift control scenario. An outer phase shift φT is implemented between the low voltage $v_{AC,LV}$ and the high voltage $v_{AC,HV}/n$. The duty cycle of the high voltage is D_pT. The current i_{L1} flows through the inductor L_1. The same current flows also through the inductor L_2. All switching positions are marked with a specific number from ①-⑥.

HV switches and not for the LV switches. Therefore, this work investigates the extended phase-shift modulation to minimize the losses during the pre-charging procedure. In the following work, the phase shift φ and the duty cycle D_p are defined in degree, i.e. 360° corresponds to the PWM period T.

ZVS Switching Analysis with Equivalent Circuits

Clearly, low conduction losses and low switching losses are necessary to keep the converter in the specification, also during startup. The conduction losses can be minimized with a low current during startup. To reduce the switching losses, soft-switching methods are inevitable. As previously mentioned, zero-voltage switching (ZVS) is necessary. To identify which parameter combination of φ and D_p (see Fig. 2) enables ZVS for the complete pre-charging procedure, an accurate time-domain ZVS analysis as previously presented in [7] is used.

To analyze the switching behavior, equivalent circuits are constructed for each switching event, see Fig. 3. Therefore, the interaction of the output capacitance of the switches, the series inductor of the DAB, and the bulk capacitor is analyzed. The interwinding and the parasitic capacitance of the PCB are neglected in this work because they are much lower than the output capacitance of the switches. The source of the DAB is connected with a filter to the bulk capacitors (not shown in Fig. 1). Due to the low cut-off frequency of the filter, the energy of transient events will be provided by the bulk capacitors. Therefore, it is not necessary to add the input and output voltage source to the equivalent circuits. In the analysis, it is assumed that the switching operations of the LV full bridge and both HV half bridges are not simultaneously. This is achieved if at least the necessary dead time is between both events.

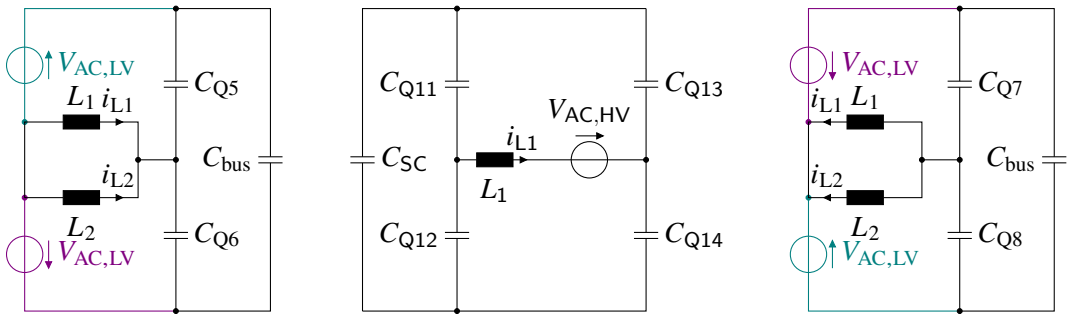


Fig. 3: Resonant commutation circuits for (a) the half bridge with switches Q_5, Q_6, (b) the full bridge with switches Q_{11}, Q_{12}, Q_{13}, Q_{14}, and (c) the half bridge with switches Q_7, Q_8.

For the ① switching event, see Fig. 2, the HV semiconductor Q_5 is turned on, Q_6 off, the equivalent circuit is constructed in Fig. 3(a). For the commutation only the output capacitances of the switches Q_5 and Q_6 are important. Therefore, the switches Q_5 and Q_6 are replaced in the equivalent circuit by the output capacitance C_{Q5} and C_{Q6}, respectively. Because the bridges do not switch simultaneously, the states on the other HV half bridge and on the LV full bridge does not change. Because of this, the LV full bridge can be replaced by the violet voltage source $V_{AC,LV}$. Moreover, Q_7 and Q_8 are replaced by a short and open, respectively. The teal voltage source is necessary for the ④ switching event and is removed for the ① switching event. To eliminate the transformer in the equivalent circuit, the capacitance of the switches and the C_{bus} capacitor are transformed to the low-voltage side with n^2C. The assignment for the other switching events ②-⑤ is shown in Table I.

The effective capacitance $C_{oss,eff}(V_{DC})$ of the SiC HV and GaN LV switches is voltage-dependent. The effective output capacitance is calculated with the voltage-dependent stored energy from the datasheet as $C_{oss,eff} = 2E_{oss}/V_{DC}$. For the HV semiconductors only one constant capacitance $n^2C_{oss,HV,eff} = 15.7\,\text{nF}$ is used because the bus voltage is fixed to 650 V. For the LV switches, the capacitance is calculated for each supercapacitor voltage. At the nominal voltage, here of the GaN LV switch, is $C_{oss,LV}(48\,\text{V}) = 1.7\,\text{nF}$.

The ZVS analysis for all supercapacitor voltages, φ, D_p, and $v_{AC,LV}$ combinations is done with a state-space model of each equivalent switching circuit in Fig. 3. The assignment of the switching states in Fig. 2 to the mathematical models (1) or (2) with the state vectors $\mathbf{x_1} = [i_{Ls1}\ i_{Ls2}\ v_{C,SC}\ v_{Q,x}\ v_{Q,y}]^T$, $\mathbf{x_2} = [i_{Ls1}\ v_{C,SC}\ v_{Q,m1}\ v_{Q,m2}\ v_{Q,m3}\ v_{Q,m4}]^T$, the input scalars $u_1 = V_{AC,LV}$, $u_2 = V_{AC,HV}$, and the necessary additional parameters are shown in Table I. To prevent numerical problems, very small identical resistors R are added in series to the capacitors (not shown in Fig. 3). The input voltages and initial values on the capacitors and inductors at each switching state are calculated with an ideal analytical model of the DAB. The output capacitance of the switches is mapped to voltage-dependent capacitors in the circuit diagrams in Fig. 3.

Table I: Assignment of the different switching states to the equivalent circuits and the necessary additional model parameters.

Switching event	①	②	③	④	⑤	⑥
prior switch status	Q_6 on Q_5 off	Q_{x2}, Q_{x3} on Q_{x1}, Q_{x4} off	Q_8 on Q_7 off	Q_5 on Q_6 off	Q_{x1}, Q_{x4} on Q_{x2}, Q_{x3} off	Q_7 on Q_8 off
target switch status	Q_5 on Q_6 off	Q_{x1}, Q_{x4} on Q_{x2}, Q_{x3} off	Q_7 on Q_8 off	Q_6 on Q_5 off	Q_{x2}, Q_{x3} on Q_{x1}, Q_{x4} off	Q_8 on Q_7 off
Equivalent circuit	Fig. 3(a)	Fig. 3(b)	Fig. 3(c)	Fig. 3(a)	Fig. 3(b)	Fig. 3(c)
LV source	violet	-	violet	teal	-	teal
State-space model	Eq. (1)	Eq. (2)	Eq. (1)	Eq. (1)	Eq. (2)	Eq. (1)
model parameter z_1	1	–	1	1	–	−1
model parameter z_2	−1	–	1	1	–	1
model parameter $C_{Q,x}$	$x = 5$	–	$x = 7$	$x = 5$	–	$x = 7$
model parameter $C_{Q,y}$	$y = 6$	–	$y = 8$	$y = 6$	–	$y = 8$

$$\dot{\mathbf{x}}_1 = \begin{bmatrix} \frac{-R}{2\,L_{s1}} & \frac{-R}{2\,L_{s1}} & \frac{z_2}{2\,L_{s1}} & \frac{z_1}{2L_{s1}} & \frac{-z_1}{2L_{s1}} \\ \frac{-R}{2L_{s2}} & \frac{-R}{2L_{s2}} & \frac{z_2}{2L_{s2}} & \frac{z_1}{2L_{s2}} & \frac{-z_1}{2L_{s2}} \\ \frac{-z_2}{2C_{bus}} & \frac{-z_2}{2C_{bus}} & \frac{-1}{2RC_{bus}} & \frac{1}{2RC_{bus}} & \frac{1}{2RC_{bus}} \\ \frac{-1}{2C_{Q,x}} & \frac{-1}{2C_{Q,x}} & \frac{1}{2RC_{Q,x}} & \frac{-1}{2RC_{Q,x}} & \frac{-1}{2RC_{Q,x}} \\ \frac{z_1}{2C_{Q,y}} & \frac{z_1}{2C_{Q,y}} & \frac{1}{2RC_{Q,y}} & \frac{-1}{2RC_{Q,y}} & \frac{-1}{2RC_{Q,y}} \end{bmatrix} \cdot \mathbf{x}_1 + \begin{bmatrix} \frac{1}{L_{s1}} \\ \frac{1}{L_{s2}} \\ 0 \\ 0 \\ 0 \end{bmatrix} \cdot u_1 \tag{1}$$

$$\dot{\mathbf{x}}_2 = \begin{bmatrix} \frac{-R}{L_s} & 0 & \frac{-1}{2L_s} & \frac{1}{2L_s} & \frac{1}{2L_s} & \frac{-1}{2L_s} \\ 0 & \frac{-1}{RC_{SC}} & \frac{1}{2RC_{SC}} & \frac{1}{2RC_{SC}} & \frac{1}{2RC_{SC}} & \frac{1}{2RC_{bus}} \\ \frac{1}{2C_{Q,m1}} & \frac{1}{2RC_{Q,m1}} & \frac{-1}{2RC_{Q,m1}} & \frac{-1}{2RC_{Q,m1}} & 0 & 0 \\ \frac{-1}{2C_{Q,m2}} & \frac{1}{2RC_{Q,m2}} & \frac{-1}{2RC_{Q,m2}} & \frac{-1}{2RC_{Q,m2}} & 0 & 0 \\ \frac{-1}{2C_{Q,m3}} & \frac{1}{2RC_{Q,m3}} & 0 & 0 & \frac{-1}{2RC_{Q,m3}} & \frac{-1}{2RC_{Q,m3}} \\ \frac{1}{2C_{Q,m4}} & \frac{1}{2RC_{Q,m4}} & 0 & 0 & \frac{-1}{2RC_{Q,m4}} & \frac{-1}{2RC_{Q,m4}} \end{bmatrix} \cdot \mathbf{x}_2 + \begin{bmatrix} \frac{1}{L_s} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \cdot u_2 \tag{2}$$

An exemplary commutation at the switching event ① (Q_5 switches on) is shown in Fig. 4. The voltage before 0 ns is calculated with the ideal analytical model of the DAB (violet, solid). The transition is calculated with the state-space model (teal, solid). If the voltage at output capacitance of the switch Q_5 reaches the forward voltage of the body diode of Q_5, the body diode conducts and the voltage follows the violet solid line. Then, ZVS is achieved. If the body diode conducts, the solution of the state-space model is not valid anymore (teal, dashed). The minimum dead time t_c until the switch reaches ZVS can

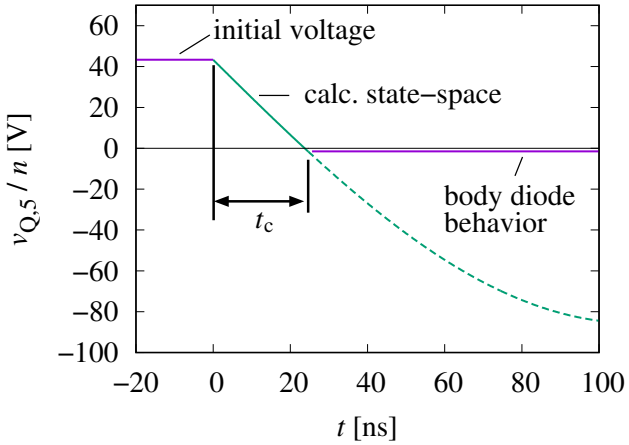


Fig. 4: Commutation of switch Q5. Violet: Initial voltage before the commutation and voltage if the body diode conducts. Teal (solid): Valid calculated commutation voltage of switch Q5 for switching event ①. Teal (dashed): Invalid calculated commutation voltage if the body diode conducts.

be extracted from the calculated resonant commutation. This time is also used during the calculations to ensure that the necessary dead time between the two HV half bridge switching events exists. A variable dead time that follows the calculated t_c could increase the efficiency. In our case, for simplicity, a 100 ns dead time for all operation points is implemented. After 100 ns, semiconductor Q_6 switches on.

As a result of the calculation of all operation points, a 3-dimensional ZVS boundary for different outer phase shifts φ and duty cycle D_p combinations is extracted, see. Fig. 5. For all operation points in the area, ZVS can be guaranteed for all switching events.

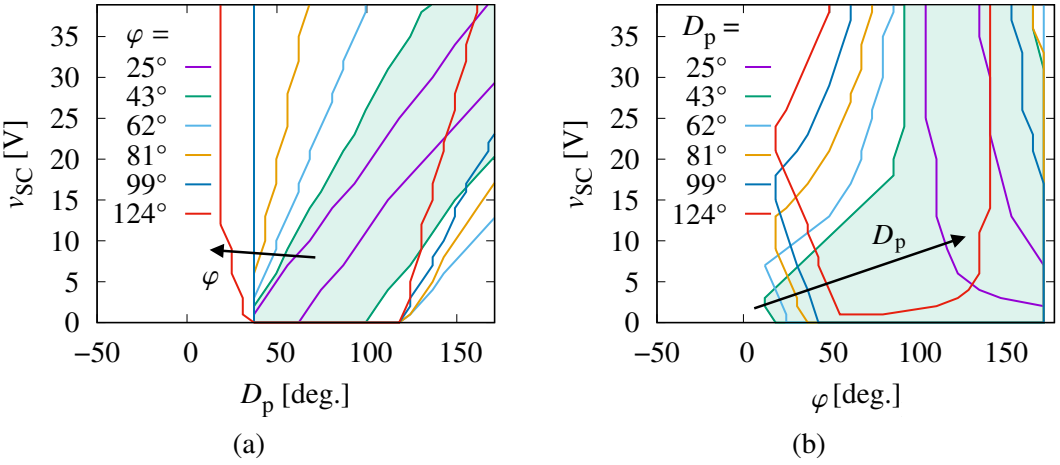
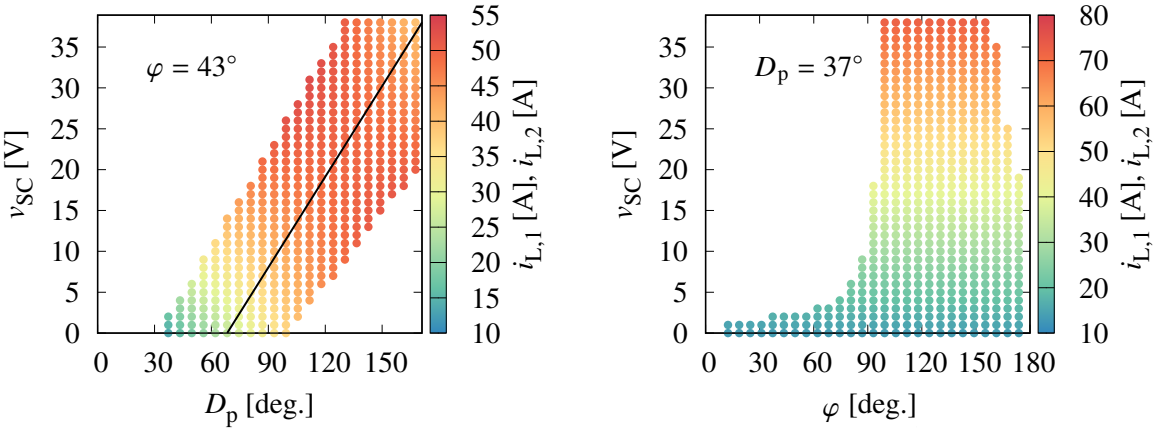


Fig. 5: The boundary of the inner ZVS switching area for all switching actions is shown for different combinations of supercapacitor voltage v_{SC}, outer phase shift φ, and primary duty cycle D_p. The different colors represent (a) the outer phase shift φ and (b) the primary duty cycle D_p. For clarification, an exemplary ZVS area for $\varphi = 43°$ and $D_p = 43°$, respectively, is filled.

As can be seen from Fig. 5, ZVS for the complete voltage range can be reached if both control parameters (φ, D_p) are varied, but also if one parameter is kept constant and only one parameter is varied. This is desirable to minimize the control expense. If a constant φ is chosen out of the range 19° and 174° and D_p varies, ZVS can be reached. Otherwise, if a constant D_p is chosen out of the range 37° and 112° and φ varies, ZVS can also be reached. Not all operation points are shown in Fig. 5. The optimal D_p, φ combination is achieved if 1) ZVS for all switches is reached, 2) the current through the inductors L_1 and L_2, respectively, does not exceed the maximum current of 60 A, and 3) only one parameter (either D_p or φ) is varied. Moreover, ZVS should be possible from 0 V to the minimum normal operating voltage of the converter, here 38 V.

Fig. 6(a) shows the ZVS operation area with its associated inductor currents for a constant $\varphi = 43°$, Fig. 6(b) for a constant $D_p = 37°$, respectively. The inductor currents for different operations points are shown with different colors to clarify that the inductor currents do not exceed the current limit. In Fig. 6(a) a possible control characteristic is shown in black. Nevertheless, also for lower φ even with lower inductor currents ZVS can be reached, but the area will be smaller, see Fig. 5(a).



(a) const. $\varphi = 43°$ (b) const. $D_p = 37°$

Fig. 6: Possible ZVS operation points for supercapacitor voltages in the range $0\,\text{V} < v_{SC} < 39\,\text{V}$. Shown are (a) constant $\varphi = 43°$ with a variation of the primary duty cycle D_p and (b) constant $D_p = 37°$ with a variation of the phase shift φ. The different colors represent the inductor currents i_{L1} and i_{L2}. The black line displays a possible control characteristic.

For a small ZVS area and if slight variations occur, e.g. due to temperature changes, ZVS can not be guaranteed. Moreover, the pre-charging time will be extended due to the lower inductor currents. Therefore, the largest ZVS area which agrees with the current limitation is chosen. For a constant D_p, no ZVS area can be found which does not exceed the maximum current and simultaneously enables ZVS for the complete voltage range.

Keeping φ constant has the advantage that no additional DC offset current through the magnetizing inductance of the transformer occurs because of the phase shift during the starting procedure. Consequently, the modulation with a constant phase shift φ and a rising duty cycle D_p is chosen. Due to the minimal current variation around each operation point, all points are used to find the control characteristic. The duty cycle follows as

$$D_P = 2.64 v_{SC} + 68 \tag{3}$$

and is also shown in Fig. 6(a) in black.

Practical Realization

The previously presented extended phase-shift control for pre-charging the supercapacitor is implemented in the system shown in Fig. 1, also described in [8]. To verify that ZVS is possible for the previously presented area in Fig. 5(a), the switching behavior is tested for four different supercapacitor voltages 5 V, 10 V, 20 V, and 30 V. According to the previous calculations, the optimal outer phase shift should be $\varphi = 43°$.

Fig. 7 shows the voltages $v_{AC,HV}$, $v_{AC,LV}$ and the inductor current i_{L1}. From the voltage curves of $v_{AC,HV}$ and $v_{AC,LV}$ it is observed that at the end of the switching events the voltage increase slightly and the body diodes of the primary and secondary side conduct, see the small circles in Fig. 7. Consequently, ZVS is achieved for all switching events. The calculated ZVS area is verified by the four measurements.

The complete pre-charging procedure from 0 V to 38 V of a 165 F supercapacitor is shown in Fig. 8. It can be seen that the current through the inductor matches with the ideal calculations in Fig. 6(a). The maximal current of 60 A will not be exceeded.

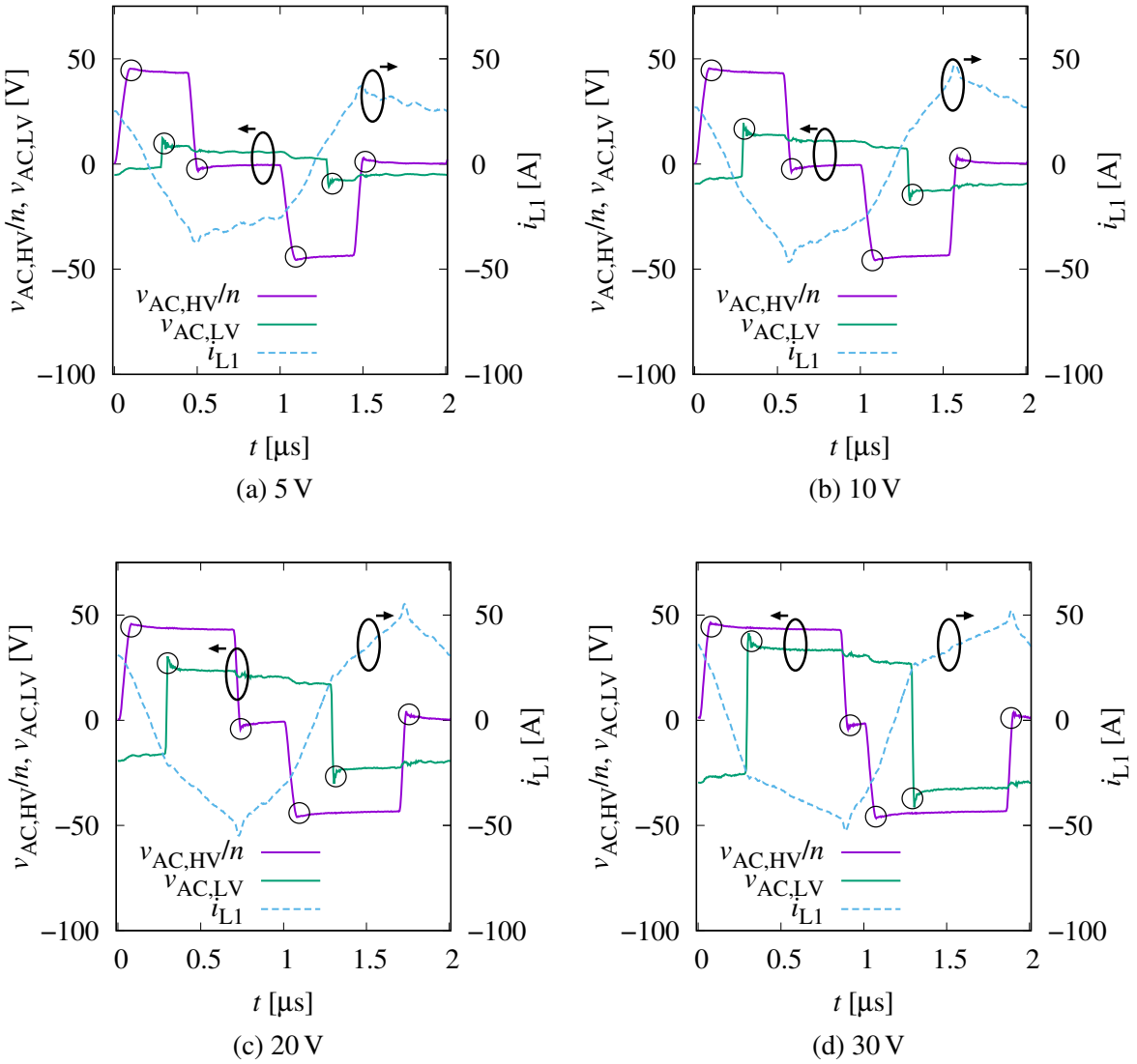


Fig. 7: Measured switching behavior for four different voltages (a) V_{SC} = 5 V, (b) 10 V, (c) 20 V and (d) 30 V. V_{bus} = 650 V and D_p is determined from (3). The small circles show the phases when the body diode is conducting.

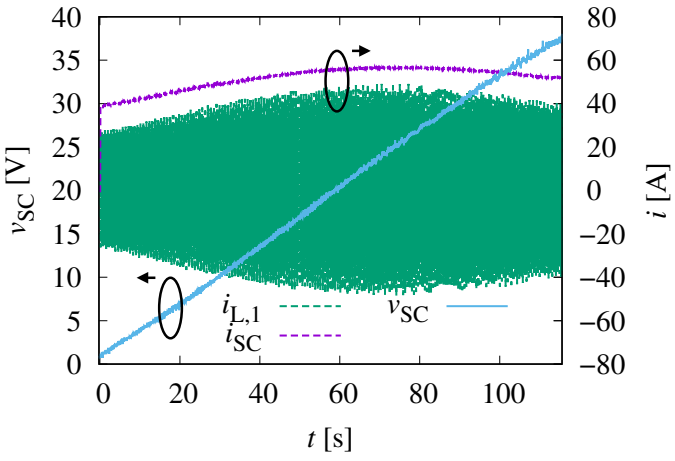


Fig. 8: Pre-charging procedure of a 165 F supercapacitor. The capacitor charging current i_{SC}, the capacitor voltage v_{SC}, and the inductor current $i_{L,1}$ are shown.

Conclusion

This paper presents an optimized control scheme to achieve ZVS for the complete pre-charging phase for a dual active bridge (DAB). A capacitance time-domain-based model is used to identify φ and D_p combinations to achieve full ZVS. Without a constant φ and rising D_p, full ZVS switching is possible for a supercapacitor voltage between 0 V and 38 V. Measurements confirm the correctness of the calculations. The presented extended phase-shift modulation is attractive for applications with supercapacitors that are often discharged completely and need to be pre-charged. With this modulation, an over-dimensioning of the DC/DC converter because of the pre-charging phase is not necessary.

References

[1] A. González, E. Goikolea, J. A. Barrena, and R. Mysyk, "Review on supercapacitors: Technologies and materials," *Renewable and Sustainable Energy Reviews*, vol. 58, pp. 1189–1206, 2016. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S1364032115016329

[2] Y. Wu and R. Holze, *Electrochemical energy conversion and storage*. Wiley-VCH GmbH, 2022.

[3] R. De Doncker, D. M. Divan, and M. H. Kheraluwala, "A three-phase soft-switched high-power-density DC/DC converter for high-power applications," *IEEE Transactions on Industry Applications*, vol. 27, no. 1, pp. 63–73, Jan 1991.

[4] W. Chen, P. Rong, and Z. Lu, "Snubberless bidirectional DC-DC converter with new CLLC resonant tank featuring minimized switching loss," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 9, pp. 3075–3086, 2010.

[5] J. Hu, S. Cui, and R. De Doncker, "Closed-loop black start-up of dual-active bridge converter with boosted dynamics and soft-switching operation," *IEEE Transactions on Power Electronics*, vol. 36, no. 10, pp. 11 009–11 013, 2021.

[6] P. Yao, X. Jiang, and F. F. Wang, "Soft starting strategy of cascaded dual active bridge converter for high power isolated DC-DC conversion," in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2020, pp. 1031–1037.

[7] F. Sommer, N. Menger, T. Merz, and M. Hiller, "Accurate time domain zero voltage switching analysis of a dual active bridge with triple phase shift," in *2021 23rd European Conference on Power Electronics and Applications (EPE'21 ECCE Europe)*, 2021, pp. 1–9.

[8] P. Lenzen and M. Pfost, "500 kHz SiC- and GaN-based dual active bridge with voltage conversion between 48 V and 650 V," in *PCIM Europe 2022; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2022.