Analysis and Estimation of Neutral-Point Voltage Balancing Ability of an Optimized Balancing Algorithm for Grid Connected Active-NPC converter

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Keywords

Neutral point clamped inverter, Capacitor voltage balancing, Grid-connected converter, multi-level converters, Neutral current ripple

Abstract

Neutral-point (NP) voltage balancing is a well-known challenge associated with Neutral Point Clamped (NPC) multi-level voltage source converters. Most of the literature on multilevel NPC converters discusses on multiple balancing techniques that are used to nullify dc or ac unbalance and claims the adaptability of these techniques over wide range of modulation indices and power factors. This paper details out the analysis for estimating the maximum balancing ability of an optimized neutral point balancing technique applied on a grid connected 3-Level Active-NPC (ANPC) converter with supporting simulation and experimental results. Also, a simplified analysis to study the impact of grid harmonics on the neutral point potential is presented and validated with the help of simulation results.

Introduction

Multilevel converters are widely used for medium-voltage high power applications regarding the integration of renewable energy sources like wind and solar. The major advantages they offer include increased voltage capability thereby reducing the overall system losses, reduced total harmonic distortion, lower Common Mode Voltages (CMV) [1]. Because of its simplicity, reliability and higher manufacturing readiness level, NPC converter is one of the well accepted 3-level topologies by the industry. The additional third level is realized by clamping the pole voltage to the dc-link mid-point. The mid-point is achieved by splitting the dc-link into two halves using series connected capacitors. In such converters, it becomes essential to control the voltage of each series connected capacitor, or mid-point voltage, also known as neutral-point (NP) voltage.

Various balancing techniques have been proposed in the literature to control the neutral point voltage of NPC converter over a wide range of power factors and modulation indices [2-11]. In [2], a comprehensive study around NP balancing controls with mathematical derivations for various operating conditions is discussed. A new balancing strategy is proposed in [3] to modify bridge currents for better performance under no load or light load conditions. The bigger challenge of balancing the neutral point voltage occurs at higher modulation indices as there will be no margins to modify the modulation indices. Such a case is discussed in [4] and the introduced method is power flow direction independent. Closed loop small signal transfer function is presented in [5] to design the NP balancing proportional-integral (PI) regulator. This technique aims to reduce the injected common mode voltage for neutral point balancing, thereby limit the size of the dc link capacitance. In [6], an attempt to utilize 3 level NPC for active filtering is proposed and a 6^{th} harmonic zero sequence component is utilized for balancing the neutral point voltage. As 6^{th} being the lowest even and triplen harmonic that produces the non-zero neutral-point current and doesn't reflect in phase currents of the converters. Some attempts were made to optimize the balancing algorithms based on the chosen pulse width modulation (PWM) technique [7]. Theoretical expressions for the maximum zero sequence voltage are derived using interpolation methods

in [8]. Inherent neutral point balancing ability of the converter is comprehensively studied in [9] and dependency of switching frequency of the converter is highlighted and methodologies were suggested for improving this inherent balancing ability. In [10], zero sequence voltage is utilized for balancing scheme to reduce both dc balancing and ac oscillations at the neutral point. With a little compromise on the output voltage harmonic distortion, new strategy is proposed in [11] for enhanced balancing ability. To summarize, any balancing algorithm injects either dc, or specific harmonics into modulation signal or modify bridge currents for getting nonzero average mid-point current. These techniques differ in terms of their ability to do NP balancing w.r.t the power factor range, dependency on load currents, and amount of CMV injected, etc. In this paper, the analysis of optimized NP balancing algorithm mentioned in [12,13] has been performed to estimate the true maximum balancing ability. The impact of even harmonic sequence in grid voltage on NP potential has also been analyzed. The challenge of NP voltage balancing is identical for NPC and ANPC converters. The additional advantage with ANPC is the flexibility to choose the path for the mid-point current during zero pole voltage level thereby achieving uniform loss distribution across the devices. In this paper, ANPC converter has been chosen for the validation in simulation and hardware. Theoretical analysis of balancing algorithm has been performed at two critical modulation indices, and validation of analysis is done using simulation and hardware results.

Grid connected Active-NPC (ANPC) converter

Fig. 1 shows a single line and single-phase schematic of grid connected ANPC converter with an output LC filter. The switching pulses for the devices S_1-S_6 for A-phase are based on the logic in Table-I, where M_a is the phase-A modulation signal and S is the switching state. S is logic high (represented as 1) when M_a is greater than the carrier signal and logic low (represented as 0) vice versa. $\bar{S}$ is complement of S. The gate pulses for the devices are derived from the control logic shown in Fig. 2 using third harmonic injected PWM with 2 level shifted carriers. The converter is operating as Active Front End (AFE) rectifier, where in the d-axis controls the total dc-link voltage (V_{dc}) and q-axis-the reactive power flow (I_q). Feedback quantities are the 3-phase grid voltages (V_{grid}) and inductor currents (I_{abc}). Inputs to the phase-locked-loop (PLL) block are grid voltage V_{grid} and estimated angle θ_{pll}, PLL aligns the grid voltage space vector along the d-axis [14-15]. The modulation signals $M_{(abc)}^*$ coming out of dq control is getting added with V_{cmv} coming out of the dc-link balancing control block as in Fig. 2. A detailed analysis of the dc-link NP balancing control is done in the following section.

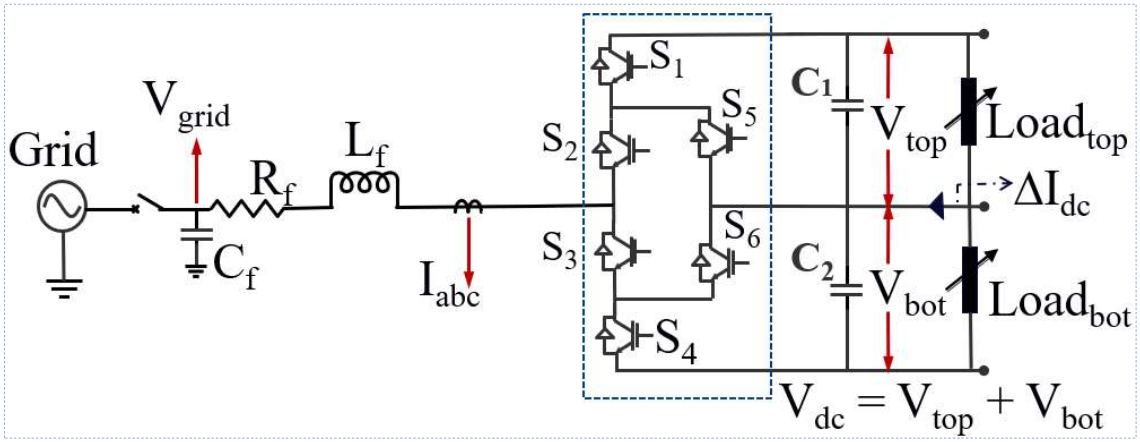


Fig. 1: System configuration of grid connected ANPC converter with grid voltage-oriented control

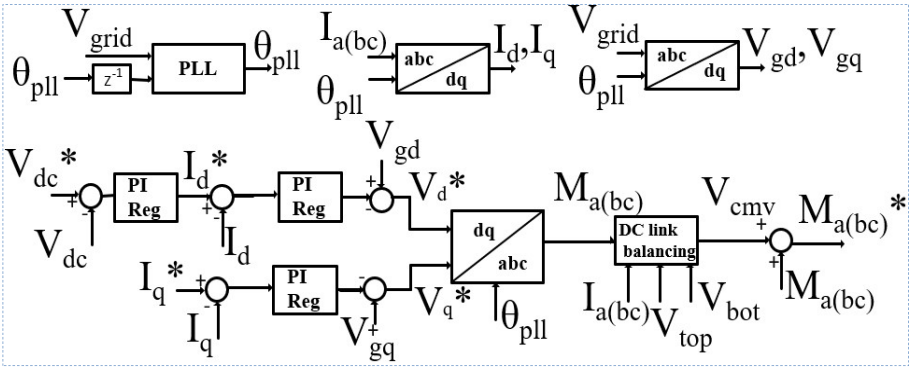


Fig. 2: *dq* control blocks for AFE rectifier operation of ANPC converter

Table I: Switching logic of ANPC converter

Condition	S1	S2	S3	S4	S5	S6
$M_a \geq 0$	S	1	0	0	$\bar{S}$	S
$M_a < 0$	0	0	1	S	S	$\bar{S}$

NP balancing and midpoint current in ANPC converter

3-Level ANPC converter uses active devices (IGBT/IGCT/MOSFET) with anti-parallel diodes that creates a path for the current to flow to the mid-point when the pole voltage is clamped to the mid-point of dc-link. Ideally, the sum of these instantaneous currents from all the 3 phase legs will result in zero mid-point current when averaged over a modulation cycle. But practically, there could be slight mismatch in the components of the converter, system dynamics, line voltage distortions from the grid resulting in the distorted modulation indices which produces a non-zero average mid-point current that could drift the NP voltage [16]. This could make the entire dc-link voltage appears across one capacitor and zero voltage across the other. Hence, while implementing any NP balancing algorithm, it becomes crucial to establish theoretical relationship of mid-point current with modulation signal, line current, power factor and grid harmonics to compensate the non-zero averaged mid-point current by injecting suitable CMV without distorting the converter line to line voltage and currents.

$$\sum I_{mp}(k)_{k=1,2,3} = -(|m_a|i_a + |m_b|i_b + |m_c|i_c) \quad (1)$$

$$I_{\text{mp}} = -3 * \Sigma i * m * sign(m) \quad (2)$$

$$i = I_0 + \sum_{h=1,2,3\ldots}^{\infty}(I_h \sin(h\theta + \varphi_h) \quad (3)$$

$$m = M_0 + \sum_{v=1,2,3,..}^{\infty}(M_v \sin(v\theta + \varphi_v) \quad (4)$$

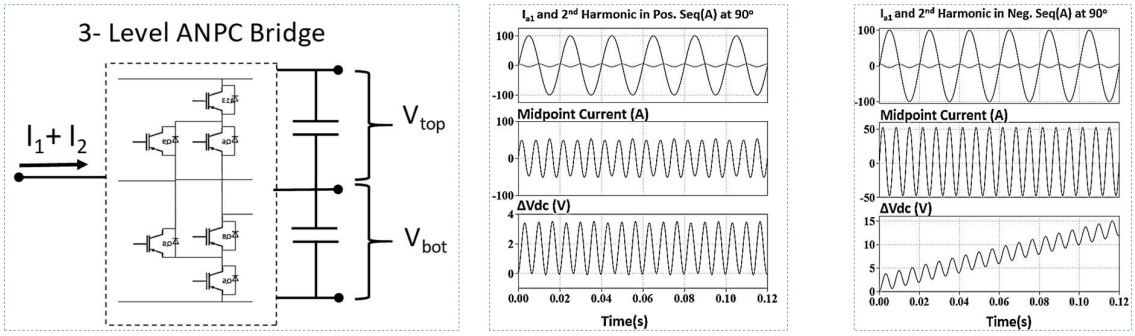
$$sign(m) = \frac{4}{\pi}\sum_{n=1,3,5}^{\infty}\frac{1}{n}(sin(n\theta + n\theta_1) \quad (5)$$

$$I_{mp(avg\_e)} = (M_1 * I_{h\_e} * \frac{2}{\pi}) * C * sin(\varphi_h) \quad (6)$$

The generalized method for the estimation of mid-point current is given by eqns. (1)-(5) for a 3-phase 3-level ANPC converter with harmonics in modulation signal and line current. where, I_{mp} is the mid-point current, m_a, m_b, m_c are the modulation signals, i_a, i_b, i_c are the line currents, *i, m, sign(m)* are the distorted phase current, modulation signal, and signum function of modulation, respectively. Here, I_0, M_0, I_h, M_v are the dc and ac harmonic components in line current and modulation, respectively.

Impact of grid harmonics on neutral point balancing

In eqns. (1)-(4), I_h, M_v represent the peak of the harmonic component in line current and modulation signal, respectively. These two components are modified to obtain dc bias in the mid-point current over a fundamental cycle, as given in (6), where I_{h_e} is the peak of even harmonic component in current and C is algebraic constant. If I_{h_e} is introduced by the grid voltage distortion, as shown in Fig. 3(a), it can create NP imbalance, when there is no active control of NP potential. As given in (6), even harmonics can result in a non-zero average mid-point current under certain conditions. In Fig. 3(b), 5% of 2^{nd} harmonic is added in positive sequence to the line current of 100 A peak at unity modulation index, and the resultant mid-point current does not have any dc-bias and there is no drift in ΔV_{dc}. Here, phase angle (φ_h) is 90°. However, in Fig. 3(c), 5% of 2^{nd} harmonic when applied in negative sequence drifts the NP voltage. On the contrary, 4th harmonic current in positive sequence will create drift in ΔV_{dc}, however, 4th harmonic in negative sequence does not create drift in ΔV_{dc}.



(a) (b) (c)

Fig. 3: (a) 3L-ANPC converter with 2nd harmonic in line current, fundamental line current, 5% of 2nd harmonic current at 90° phase, mid-point current and ΔV_{dc} in positive sequence in (b), and negative sequence in (c), respectively.

Optimal Neutral point balancing algorithm

Optimal NP balancing algorithm compensates for the dc unbalance by CMV injection [12-13,17-18]. It is superior to other balancing techniques as it does not inject CMV aggressively and prevents overmodulation operation across all power factors and modulation indices. As shown in Fig. 4, the difference in the top and bottom capacitance voltages (V_{top} & V_{bot}) has been calculated and same has been passed through Low-Pass Filter (LPF) and a Proportional-Integrator (PI) regulator. Output of PI controller (*DCBalRegOut*) acts like a dynamic gain whose value depends on the magnitude of voltage imbalance and sign decides the direction for generating the compensating mid-point current. To improve the dc bus utilization, third harmonic injection has been done in modulation signals (M_{a_cmd}, etc.) [10]. The modified modulation commands ($M_{a\_cmd\_th}$, etc.) are passed through a min-mid-max classifier to obtain instantaneous maximum and minimum values.

The limit calculator module computes the maximum, minimum and mid common mode offset voltages that can be added to modulation commands, at a particular instant. It is the key benefit of this algorithm as instantaneous offset computation is done dynamically considering the available margin in modulation commands. Using three instantaneous computed offset voltages (CMV_{Max}, etc.) and instantaneous line currents (I_{a_phase}, etc.), the NP current calculator block (I_{NP}) generate three NP currents ($I\_{}_{CMVMax}$, etc.) by the addition of these offset voltages (CMV_{Max}, etc.) to modulation indices using eqn. (1). Dynamic CMV calculator compares the three currents and computes the product of PI regulator output (*DCBalRegOut*) with the offset voltage that produces maximum positive or maximum negative neutral point current based on the sign of regulator output (*DCBalRegOut*). The final output from the NP algorithm (CMV^*) is added to modulation signals to generate final modulation command ($M_{a\_cmd}^*$, etc.). These modulation commands are used to generate PWM signals using sine-triangle switching technique [18]. Therefore, as described above, optimum NP balancing algorithm prevents

overmodulation and ensure maximum balancing capability at an operating point. In next section, maximum balancing ability of this NP balancing scheme has been analyzed.

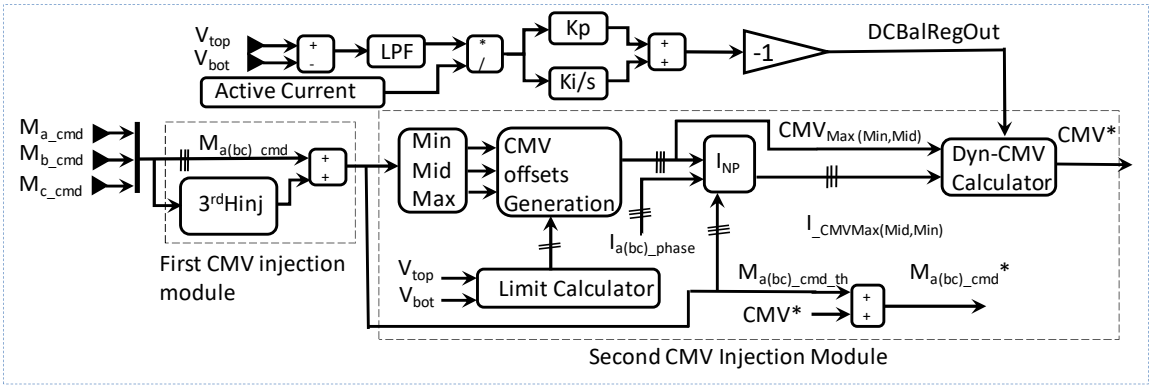


Fig. 4: Control structure of optimal NP balancing with CMV injection.

Dependency of maximum balancing ability on modulation index and power factor

The balancing ability is defined as the ratio of maximum average mid-point current (with CMV injection) to the peak of line current. For optimized balancing algorithm mentioned in the above section, the measure of computed balancing ability with modulation index and power factor angle (Ø = 0°, 30°, 60°, and 90°) is shown in Fig. 5. The balancing ability is highest in unity power factor at modulation index of 0.5 and it decreases as the power factor decrease. The balancing ability is minimum at unity modulation index and zero power factor operation. In Fig. 5, two cases plotted on the dotted line, viz., case-A and case-B have been chosen for further analysis. The power factor angle of these cases is 62°. case-A has lowest balancing ability of 0.042 per unit at unity modulation index and case-B has highest balancing ability of 0.43 per unit at modulation index of 0.5. Fig. 6(a) and 6(b) shows simulated outputs of three CMV offsets (CMV_{Max}, etc.), computed mid-point currents (I_{CMVMax}, etc.) with these offsets added to modulation commands, and the instantaneous maximum NP current (I_{MP_out}) from the converter with optimized balancing technique for case-A and case-B, respectively.

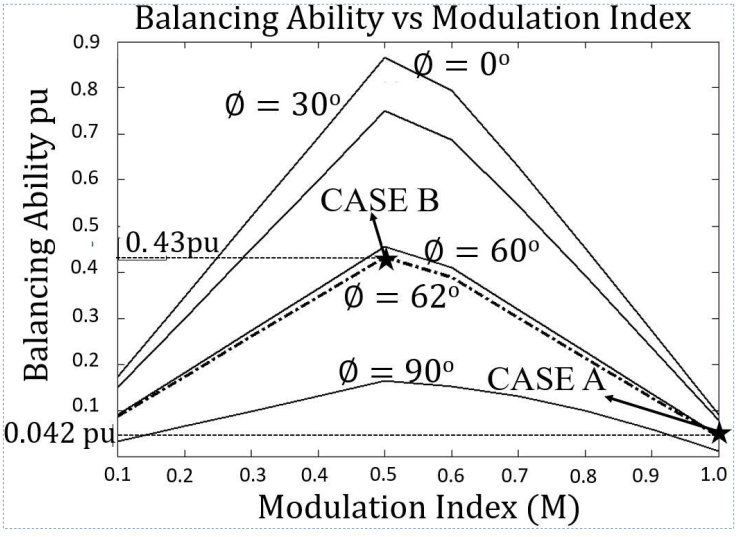
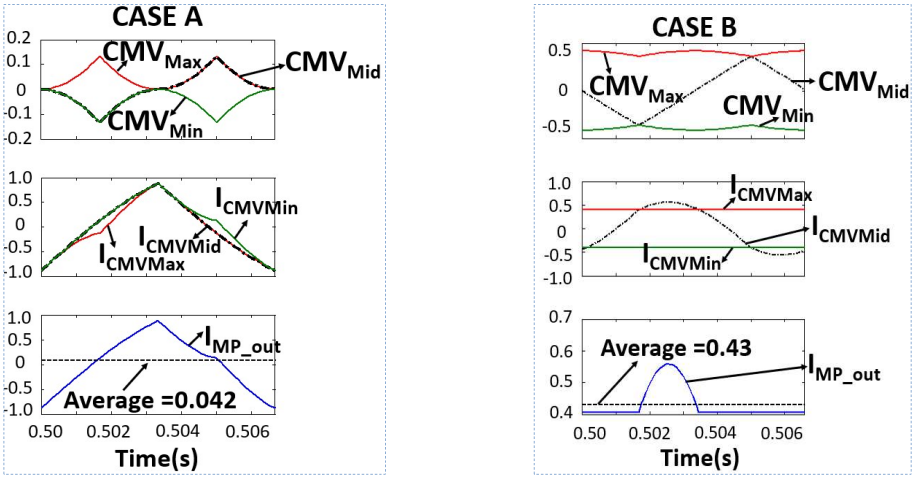


Fig. 5: Maximum balancing capability vs modulation index



(a) (b)

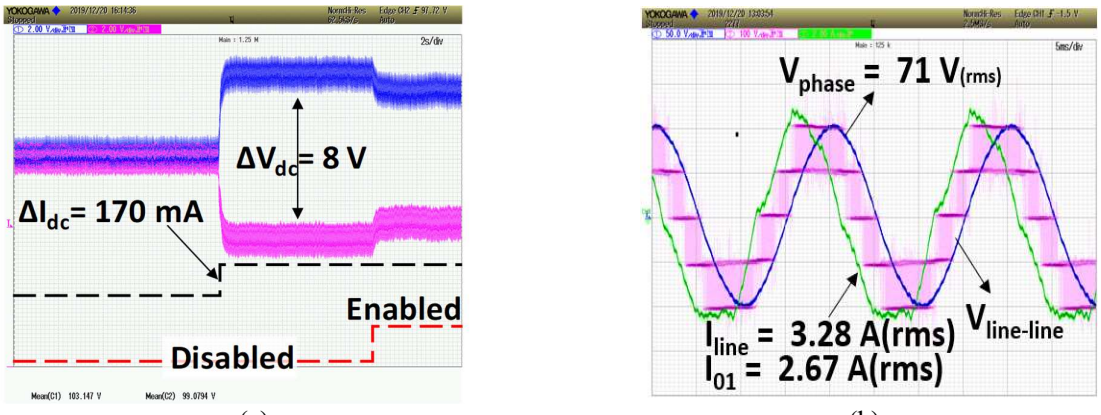
Fig. 6: (a) Common mode offsets, calculated mid-point currents from offsets, maximum mid-point current for Case-A, (b) for Case-B.

Experimental validation

Experimental validation of discussed NP balancing algorithm and analysis was performed on a 3-phase, 10 kVA, grid connected 3-level ANPC converter. Experimental results were obtained for case-A and case-B at operating conditions given in Table-II. The ANPC converter has been operated in rectifier mode using resistors as a load. The top and the bottom capacitors are connected to separate resistors. Unbalance in capacitor voltages is created by choosing appropriate resistor values.

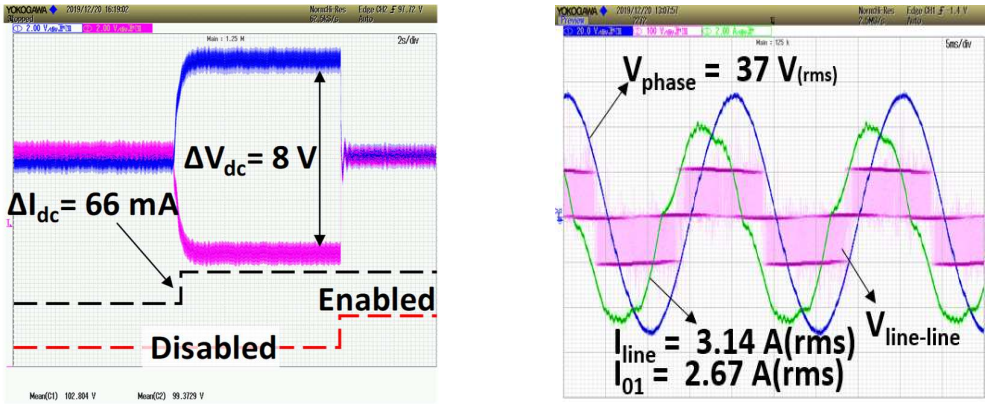
Table II: Operating conditions for experimental validation

Case	Modulation index	Power factor angle	$I_{abc\_peak} = sqrt(2) * I_{01}$ (A)	V_{dctop} (V)	V_{dcbot} (V)	ΔI_{dc} (mA)	I_{mid_max} (mA)
A	1.0	61.6°	3.78	104	96	170	158
B	0.5	61.6°	3.78	104.2	95.7	66	1625



(a) (b)

Fig. 7: Experimental results showing dc balancing ability: (a) top and bottom capacitor voltage and (b) grid current, grid phase voltage, and converter voltage (L-L) for case-A



(a) (b)

Fig. 8: Experimental results showing dc balancing ability: (a) top and bottom capacitor voltage and (b) grid current, grid phase voltage, and converter voltage (L-L) for case-B

In case A, the converter is operating at unity modulation index and power factor angle of approx. 62°. The amplitude of peak fundamental line current is 3.78 A (= 2.67*1.414). Due to unbalance in load resistors across capacitors, a NP current (ΔI_{dc}) of approx. 170 mA flows through dc-link mid-point and creates a dc unbalance (ΔV_{dc}) of 8 V across top and bottom capacitors, as shown in Fig. 7 (a). The computed maximum balancing ability of the converter in this condition is 158 mA (0.042*3.78), which is lower than the unbalance current. Hence, after enabling the algorithm, the unbalance in capacitor voltages reduces but it does not cancel out completely. Fig. 7(b) shows the grid voltage, grid current, and converter line to line voltage for case-A.

In case B, the converter is operating at a modulation index of 0.5 and the NP current (ΔI_{dc}) due to unbalance in load resistor creates 66 mA. At this operating condition, the maximum balancing ability is 1625mA (0.43*3.78) (given in Fig. 5), which is higher than the unbalance current. Therefore, the capacitor voltages get balanced as soon as the balancing algorithm is enabled, as in Fig. 8(a), confirming the analysis. Fig. 8(b) shows the grid voltage, grid current and converter line to line voltages for case-B respectively. In Fig.8(b), grid voltage (phase rms) is reduced to 37 V compared to 71 V in Fig. 7(b). This is done to obtain a modulation index of 0.5 in Case B from 1.0 in Case A without changing the DC link voltage.

Conclusion

In this paper, theory, operation, and analysis of optimized balancing algorithm applied to a grid connected ANPC converter has been discussed. Theoretical expressions for the computation of mid-point current, dependency on the CMV and margins in modulation indices to avoid overmodulation have been presented. The impact of even order sequence of grid harmonics on the NP voltage has been provided. The balancing ability of 3-level ANPC converter with optimized algorithm at two selected operating points has been analyzed and validated using simulation and experimental results.

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