DC Bias Currents in Full-Bridge DC-DC Converters in Context of WBG Semiconductors and High Switching Frequencies

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Acknowledgements

Keywords

DC-DC converter, Dual Active Bridge (DAB), Wide bandgap devices, Silicon Carbide (SiC), Non-identical devices

Abstract

This paper aims to address the challenges of ever higher switching frequencies and better semiconductors with respect to DC currents in DC-DC full-bridge converters. The causes of DC offset currents as non-identical components and higher switching frequencies in combination with wide bandgap (WBG) semiconductors are explained and discussed.

1 Introduction

Many papers have been published to address DC bias currents in DC-DC converters recent years (e.g. [1], [2]). The focus in most papers is eliminating the DC bias current (e.g. [1], [3], [4], [5], [6]). Little was published about the exact causes and influences due to better semiconductors and higher switching frequencies in combination with high DC-link voltages and possible solutions in detail until now. [7] presents a prediction method to calculate the maximum dc bias for a given transformer. This paper aims to present an overview about the causes of DC bias currents, especially in context of high switching frequencies, WBG semiconductors and high DC-link voltages. It provides analytic quantization of the effects proven by simulations and measurement results. Furthermore, it shows solutions to prevent and eliminate these currents to an acceptable level.

2 System Overview

The investigated system of this paper is a dual active bridge (DAB) DC-DC converter, see Fig. 1. However, other topologies without series capacitor show the same behavior. Also, the results can be adapted and used for half-bridge converter.
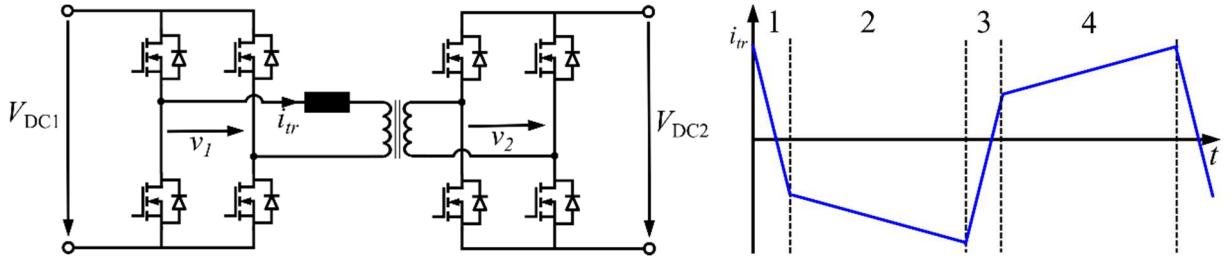
Fig. 1: Typical circuit of a dual active bridge (DAB) left and typical transformer current waveform right

There are two full-bridges, consisting of Silicon Carbide (SiC) MOSFETs and an MF-transformer with integrated leakage inductance. The two full-bridges generate square wave voltages v_1 and v_2. By controlling the phase shift between these voltages, the power transfer and output voltage V_{DC2} can be controlled.

3 Theoretical Considerations

As shown in Fig. 1, the transformer current i_{tr} has different slopes depending on the states of the full-bridges. In interval 1, secondary voltage v_2 is positive and primary voltage v_1 is negative. In interval 2, both voltages are negative. In intervals 3 and 4 the voltages are correspondingly vice versa. Equations 1-4 describes the behavior, $\frac{di_{tr}}{dt}$ is the transformer current slope, V_{DC1} the primary voltage, V_{DC2} the secondary voltage and L_σ the stray inductance of the transformer. The magnetizing inductance L_M is assumed to be large and the influence on the current slope is neglected [8]. Here a transformer transformation ratio of unity is assumed.

$$\left(\frac{di_{tr}}{dt}\right)_1 = -\frac{V_{DC1} + V_{DC2}}{L_\sigma} \tag{1}$$

$$\left(\frac{di_{tr}}{dt}\right)_2 = -\frac{V_{DC1} - V_{DC2}}{L_\sigma} \tag{2}$$

$$\left(\frac{di_{tr}}{dt}\right)_3 = \frac{V_{DC1} + V_{DC2}}{L_\sigma} \tag{3}$$

$$\left(\frac{di_{tr}}{dt}\right)_4 = \frac{V_{DC1} - V_{DC2}}{L_\sigma} \tag{4}$$

Intervals 1 and 3 or 2 and 4 respectively must be the same in terms of current slope $\frac{di_{tr}}{dt}$ and time t, otherwise there occur a DC bias current. This can cause saturation of transformers core material, can be cause higher core losses [9] and asymmetrical losses and stress of the semiconductors.

Due to many effects, the intervals are always slightly different. DC bias currents can be generated by one or both of the full-bridges. This happens when the semiconductors are turned on for different times. This causes a DC offset of the bridge voltages v_1 or v_2. The DC-impedance of the circuit R_{loop} consists of two MOSFETs with On-Resistance $R_{ds,on}$ and the transformer winding resistance R_{tr}:

$$R_{loop} = 2 \cdot R_{ds,on} + R_{tr} \tag{5}$$

In combination with the offset voltage between v_1 or v_2 a DC bias current results. The offset voltage ΔV_{Offset} can be quantified by the switching interval error ΔT_{error}, the switching frequency f_s and the DC-link voltage V_{DC}:

$$\Delta V_{Offset} = 2 \cdot \Delta T_{error} \cdot f_s \cdot V_{DC} \tag{6}$$

In context of high-power density, high switching frequencies and high efficiency there are a lot of challenges to keep the DC offset as small as possible [3].

With the offset voltage ΔV_{Offset} and the circuit DC-impedance R_{loop}, the current offset can be calculated:

$$\Delta I_{Offset} = \frac{\Delta V_{Offset}}{R_{loop}} \tag{7}$$

With higher switching frequencies, differences of the intervals become more critical. Even small timing errors cause large DC bias currents. Furthermore, high DC-link voltages amplify the effect, just like a low resistance of the power loop.

DC bias current is caused by dynamical and steady state timing errors. While earlier papers often describe and handle dynamical time errors caused by sudden phase shifts of control (e.g. [2], [10]), higher switching frequencies and WBG semiconductor amplify the impact of steady state timing error so that these become more important.

Errors of the switching times are mainly caused by steady state tolerances of components: the resolution of the PWM unit, variation of the propagation delay of digital isolators or gate driver ICs, signal runtime on PCB, tolerances of components e.g. capacitors in signal filters, tolerances of switching levels of digital inputs and variation of the MOSFET's threshold voltage. There are further small effects, which also influence the switching behavior. Most of the effects are in picosecond or small nanosecond range, but for high switching frequencies, these effects become important and must be paid attention to. The deviations are component related and therefore not reproducible. Thus, the worst case must be assumed for the analysis and design.

Furthermore, there are also DC currents which are caused by the control, e.g. by changing the phase-shift. This dynamical, transient caused offset occurs only for a short time because of the damping due to the impedance of the power loop. The converter, especially the transformer must be robust enough to handle the sum of static and transient dc bias. Multiple methods are published to overcome the transient, dynamical phase shift with resulting dc bias current (e.g. [2]).

4 System Evaluation

As an example, some practical static component tolerances of a real DAB converter were analyzed:
- High resolution PWM of Microcontroller   195 ps
- Skew time of digital isolator channel to channel   4 ns [11]
- Propagation delay of gate driver part to part   7 ns [12] or 14 ns [13]

Note, that all values can be positive or negative. So, the tolerances are doubled. By using a switching frequency of 100 kHz and a DC-link voltage of 800 V using the equation 2 this results in a DC offset voltage of

$$\Delta V_{Offset} = 2 \cdot \frac{11,2 \text{ ns}}{10,0 \text{ µs}} \cdot 800 \text{ V} = 1,79 \text{ V} \tag{8}$$

when two of the MOSFETs are turned off with the delay. When also the other two transistors are turned on with a delay, the effect will be doubled. If other effects like threshold voltages or filter are considered, the offset increases further.

With two SiC MOSFETs (Infineon IMZ120R090M1H [14]), each with a $R_{ds,on}$ of 90 mΩ and a resistance of transformers primary winding of approx. 20 mΩ, the current offset and the current offset per time difference can be calculated:

$$\frac{1,79 \text{ V}}{200 \text{ m}\Omega} = 8,95 \text{ A} \rightarrow {0,8 \text{ A}}/{\text{ns}} \tag{9}$$

The results show that even small time errors combined with high switching frequency, high voltages and low power loop resistance result in unacceptable DC bias current. Thus, saturation of the transformer is possible and asymmetrical stress of the semiconductors are implied. When using high performance WBG MOSFETs with low $R_{ds,on}$ and increasing frequencies, the effect will continue to intensify.

In contrast, by using a state of the art IGBT converter with switching frequency of 8 kHz and a DC-link voltage of 800 V the DC Offset voltage can be calculated to:

$$\Delta V_{Offset} = 2 \cdot \frac{11,2 \text{ ns}}{125 \text{ μs}} \cdot 800 \text{ V} = 0,14 \text{ V} \tag{10}$$

when two of the IGBTs are turned off with the same delay.

With two IGBT (Infineon IKW50N120CS7 [15]), each with a $R_{ce,on} = \frac{2 \text{ V}}{15 \text{ A}} = 133$ mΩ and a resistance of transformers primary winding of approx. 20 mΩ the bias current is

$$\frac{0,14 \text{ V}}{286 \text{ mΩ}} = 0,49 \text{ A} \rightarrow \frac{43,8 \text{ mA}}{\text{ns}} \tag{11}$$

This DC bias current is much smaller and can be easily handled by using a transformer with small air gap to prevent core saturation, which will be shown in the next section. No DC bias control is needed. The example shows the influence of switching frequency and power loop resistance to the DC bias current. So, the problem becomes more relevant when using WBG semiconductors and high switching frequencies.

In recent literature, there are multiple solutions to overcome this problem. [1] gives an overview about flux measurement and flux balancing methods. In [16] the AC current is measured, and the DC part of the current is separated to then control the duty cycles of the MOSFETs. [17] shows a solution with measurement of transformers flux via a hall sensor and control of the duty cycle. Both methods need an accurate and expensive measurement with a high bandwidth and an additional control loop to adjust the duty cycle. In [3] the average current is measured, and then full-bridges duty cycle is controlled. This method does not need a high bandwidth but also an additional control loop. [18] also control the DC bias by changing the duty cycle. By using current injection [19] remove the DC bias. Another often used method is to place DC blocking caps on primary and secondary side. This is simple to implement, but the capacitors must handle high currents, become large and expensive and decrease the power density. By using MOSFETs with higher $R_{ds,on}$ values and transformer windings with higher resistance, the effect of DC currents also can be reduced but losses increase. Another option is to design the transformer to be resistant to DC currents up to the maximum appearing DC-bias. With this the transformer size may increase since the dc and ac flux density must be considered, but no extra control loop is needed. Depending on the maximum DC bias current, this can be the simplest solution to overcome core saturation. However, the disadvantage is the asymmetric stress of the semiconductors, so that this method is only suitable for small dc bias currents.
Since the currents can never be completely eliminated, DC blocking caps or DC resistant transformer are always required.

5 Design of Transformer

For a first estimation of the flux density in the core a linear magnetization characteristic of the BH-curve can be made if the operation point is below the saturation of the core material. In this case the resulting flux density is the addition of the flux density of the rectangular voltage $\hat{B}_{AC}$ and the flux density of the DC current $\hat{B}_{DC}$.

For a rectangular voltage the flux density of the transformer can be easily calculated with the peak Voltage $\hat{U}$, the turns N and the cross-sectional area of the core A_{Fe}, whereas the DC flux density is calculated by the DC-current i_{DC}, the magnetic resistance of the transformer R_m and the cross-sectional area of the core.

$$\hat{B} = \hat{B}_{AC} + \hat{B}_{DC} = \frac{\hat{U}}{4f_sNA_{Fe}} + \frac{Ni_{DC}}{R_mA_{Fe}} \tag{12}$$

For small air gaps, neglecting the fringing flux, the magnetic resistance is calculated through the mean magnetic path length l_m of the core, the magnetic permeability μ_r, the magnetic constant μ_0 and the air gap δ.

$$\hat{B} = \hat{B}_{AC} + \hat{B}_{DC} = \frac{\hat{U}}{4f_sNA_{Fe}} + \frac{Ni_{DC}\mu_0}{\frac{l_m}{\mu_r} + \delta} \tag{13}$$

As seen in equation (13) the DC flux density can be a problem even with small DC current offsets when a core has a large permeability and no air gaps. An uncut nanocrystalline core tends to have these properties. The DC flux density can be limited through air gaps, however the main inductance also decreases with larger air gaps which has to be considered in the design.

6 Simulation Results

A simulation in PLECS is taken to verify the theoretical considerations, see Fig. 2. Here, the simulation results confirm the theoretical assumptions.
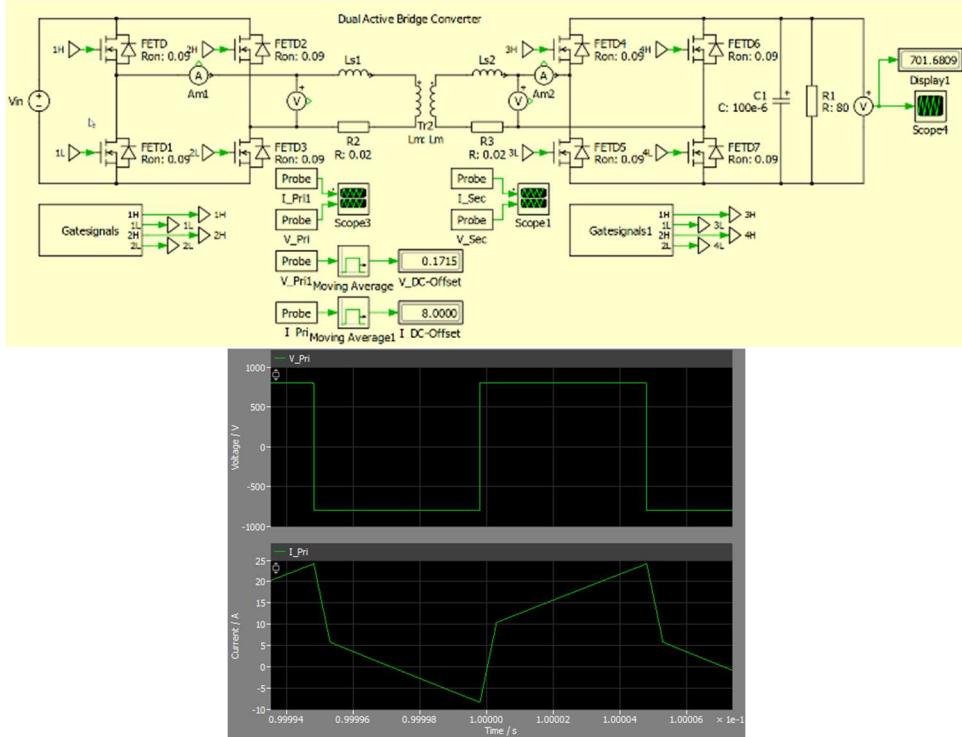

Fig. 2: Simulation setup in PLECS top and primary waveforms bottom

An open loop DAB converter is simulated with a fixed phase-shift at 800 V input voltage. The positive halfwave of primary voltage is about 10 ns longer than the negative (MOSFET 0 and 3 turned off 10 ns later). Therefore, there is a DC-bias voltage of 1,6 V which generates a DC-bias current of 8,0 A with an ohmic impedance of the power loop of 200 mΩ. Multiple simulations with different delays of individual MOSFETs on primary and secondary side verify the theoretical calculations.

7 Test Hardware and Measurements

To verify the theoretical considerations and simulations, a test hardware was built up and measurements were taken. The specifications of the test hardware are shown in Table I, the used measurement equipment in Table II. Here, a transformer with air gap is used to prevent core saturation and allow the measurement of the dc bias current.

Table I: List of relevant components

MOSFETs	IMZ120R090M1H [14]
Gate driver	1EDC60I12AH [13]
Gate-resistor	10 Ω
Isolator	ISO7740 [11]
Core	6x N87 E55/25
Air gap	0.2 mm
Main inductance	410 µH
Leakage inductance	15 µH @ each side
Winding	10 turns of 1400x0,05mm HF-litz-wire

Table II: Measurement equipment

| Oscilloscope	Tek MSO Series 4, 500MHz, 12bit, 6Ch
Voltage probes	THDP0200
Current probe	TCP0150A
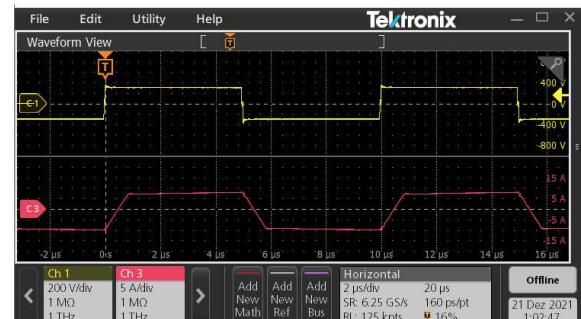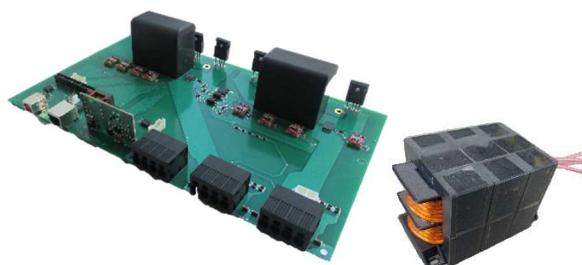
Fig. 3: Test hardware and measurement of DC bias current @ 300 V and 2,5 kW

In Fig. 3 the test hardware and measurement results are shown. To prevent saturation of the transformer only smaller voltages and loads are tested. First the imbalance of full-bridge voltage and then the DC-bias current is measured. Here, only the primary full-bridge is considered.

Table III: Measurement results

	Setup 1 @ 300 V and 2,5 kW	Setup 2 @ 300 V and 2,5 kW
T_{bias}	-9 ns	-12 ns
$I_{bias,measured}$	-1,10 A	-1,39 A
$I_{bias,calculated}$	-1,69 A	-2,25 A

Table III shows the measurement results of two setups. The PWM unit generates 100 kHz signal without an offset. Due to the component variations, the full-bridge voltage shows a DC bias. Time measurements show a time offset of -9 ns and -12 ns between positive and negative half-wave. These timing errors generate DC bias currents of -1,10 A and -1,39 A. With a gate-source voltage of 15 V and an assumed junction temperature of $T_j = 50\,°C$ the $R_{ds,on}$ is about 150 mΩ [14]. The winding resistance of the transformer was measured and is 20 mΩ. With these values the comparison to the theoretical considerations and simulation confirms the assumption with about 50-60 % higher values. These can be explained by a higher loop resistance due to the PCB and component tolerances. The calculations give the worst-case bias current.

8 Conclusion

This paper presents an overview of the main causes of static DC bias currents in DC-DC converters with respect to high switching frequencies and WBG semiconductors. An analytic approach to quantify the DC-offset is given and evaluated with measurements. Solutions to prevent or eliminating the issue are discussed and a preferred method is suggested.

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