Analysis and Implementation of different non-isolated Partial-Power Processing Architectures based on the Cuk Converter

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Keywords

«Partial-Power Processing Converter (PPC)», «non-isolated bidirectional partial-power architectures», «DC-DC switched-mode power supplies», «high power», «Converter Modelling», «DC-fast charges», «battery energy storage system (BESS)», «Converter Design and Optimization», «on-board charger», «Hybrid Cuk converter».

Abstract

This paper presents the analysis and study of different partial-power processing architectures based on the Cuk converter. Thus, the non-isolated topologies analyzed have been considered operative as voltage source converter (VSC). Likewise, the study of the converters is based on the continuous conduction mode (CCM). The partial-power topology has some advantages, such as high power density, small size, the decreased voltage in semiconductor devices, etc., this is because the DC-DC converter only processes a fraction of the total power. The purpose has been to compare the different topologies, Full-Power, Partial-Power, and hybrid-converters, in order to observe the advantages and drawbacks in each case. Among the parameters to be studied is the voltage stress in semiconductors as well as the voltage gain in each architecture. The effectiveness of these new converter architectures has been validated by the *Matlab/Simulink* software simulation. In this way, different simulation results are presented and analyzed throughout the paper. The purpose of this paper has been to study and explore the usefulness of the non-isolated Cuk converter with partial-power processing architecture for industrial power applications.

1. Introduction

The introduction of partial-power processing techniques can allow us to design and optimize converters. In this way, it is possible to implement smaller and cheaper power converters because now the power losses decrease. In recent years, these new design concepts have attracted the attention of engineers, converter designers, and researchers as an attractive solution for the development of industrial applications [1], [2]. While full-power converters process all the power flow that is supplied to the load, partial-power converters only process a fraction of this power flow, see Fig. 1. In this way, its power losses are lower than the full-power topology, meanwhile, the voltage and current stress in its semiconductor components also decrease.

The partial-power architecture has already been implemented in numerous industrial applications, such as battery charging systems in electric vehicles [3], power flow control in hybrid systems based on Fuel-Cell [4], energy distribution subsystems in wind turbines [5], integration of photovoltaic systems [6] [7], DC-power supply [8], active balancing of PV-arrays [9] or MPPT search algorithms in TEG systems [10], spacecraft [11], etc., in order to improve system performance. In summary, the partial-power converter can improve the efficiency of the whole system, while the equipment design costs are reduced. Although, there are also opposing opinions that doubt the improvement of performance in non-isolated partial-power topologies [12]. It is clear that isolated partial-power processing architectures have more advantages, but this does not justify that non-isolated partial-power topologies cannot be used in industrial applications where isolation is not a design condition, or simply in those cases in which an improvement in system efficiency is sought.

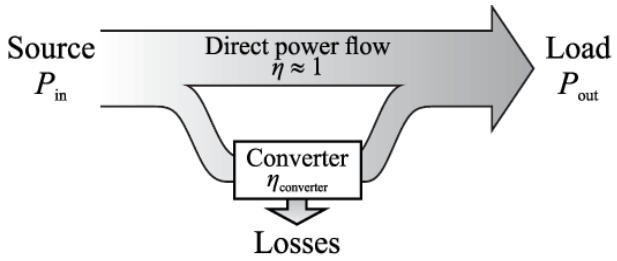

Fig. 1. Concept of power flow in partial-power converter. The converter only processes a fraction of the power supplied to the load. In this case, as an advantage the partial-power processing, the power losses are lower than in the full converter.

Partial-power architecture has some advantages over full converters, such as high power density, small size, and decreased voltage stress in semiconductor devices. These new topologies are being applied in high-power automotive applications. Some examples of applications developed are the fast-charging station for battery electric vehicles (BEV) and plug-in hybrids (PHEV) [13-15], DC-power distribution for LVDC/MVDC systems [16], a DC-DC mode switching power supply [17], a high-power battery energy storage system (BESS) [18] [19], etc.

In this paper, the authors propose different partial-power processing architectures based on the Cuk converter. These DC-DC converter topologies are intended for industrial application design or auxiliary systems in electric vehicles such as smart on-board chargers, auxiliary power supplies, etc. The main objective is to validate the advantages and drawbacks of the partial-power processing strategy in converter design. To increase the conversion efficiency and the voltage gain, different topologies of step-up converters based on the Cuk model have been proposed. Thus, to contrast these ideas, multiple simulations using *Matlab-Simulink* software have been carried out.

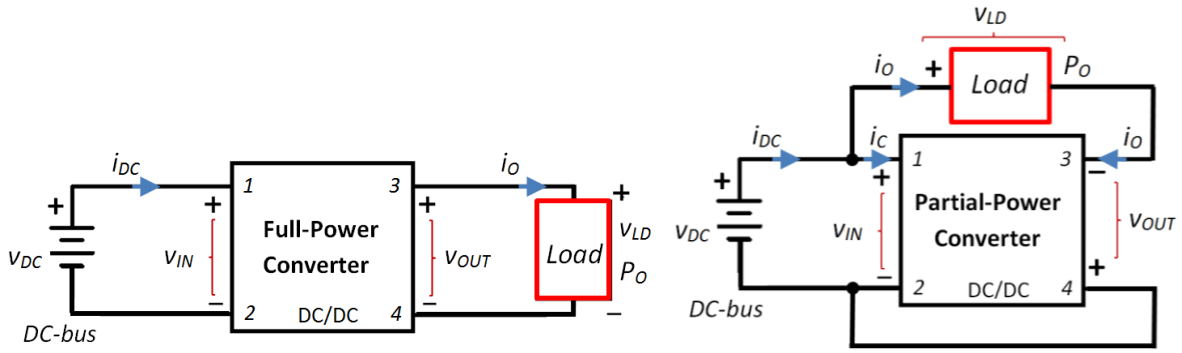

Fig. 2. Block diagram of the power conversion system. Comparison between full-power converter (traditional DC-DC converter system) and partial-power processing architecture (series-connected DC-DC converter system). In this case, the partial-power converter processes a fraction of the load's power.

This document is organized as follows. Section 1 shows a brief introduction associated with the problem addressed. Section 2 presents the mathematical analysis of the Cuk converter in partial-power processing architecture. Different hybrid topologies based on the Cuk converter are analyzed in Section 3. Meanwhile, section 4 shows the simulation results obtained in each case analyzed. The software used

has been *Matlab/Simulink*. Finally, the conclusions and some brief considerations are described in Section 5.

2. Cuk Converter in Partial-Power Processing Architecture

Figure 2 shows the basic concept of power flow in partial-power architecture. The diagram shows a comparison between the full-power converter (traditional DC-DC converter) and the partial-power converter. Its objective is to reduce the power processed by the converter, in order to increase the overall efficiency of the system. The proposed converter has been derived from the typical Cuk converter, see Fig. 3.

To simplify the steady-state analysis of the proposed architecture, some assumptions are made, such as ideal switching devices and inductors, with no delay in the switching process. For a sampling time T_{SW}, the switch is ON-state for $D \times T_{SW}$ and OFF-state for $(1 - D) \times T_{SW}$. Therefore, depending on the state of the switch, two modes of operation can be identified.

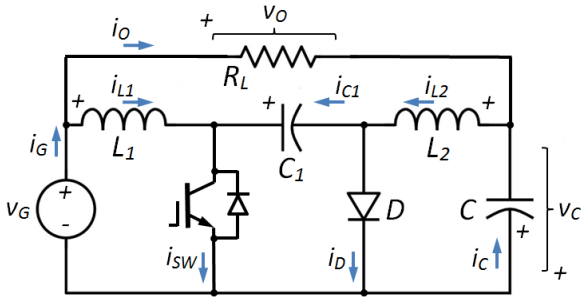

Fig. 3. Cuk converter in partial-power processing architecture.

Mode 1: ON-state $[0 \le t \le D(t)T_{SW}]$.

At the initial time t = 0, when switch SW_1 turns on, diode D_1 turns off. The inductor currents (i_{L1}, i_{L2}) increase from their respective initial value. The voltage and current equations are as follows:

$$v_{L1}(t) = L_1 \frac{\partial i_{L1}}{dt} = v_G \; ; \quad v_{L2}(t) = L_2 \frac{\partial i_{L2}}{dt} = v_{C1} - v_C \tag{1}$$

$$i_{C1}(t) = C_1 \frac{\partial v_{C1}}{dt} = i_{L2} \; ; \quad i_C(t) = C \frac{\partial v_C}{dt} = i_{L2} - i_O \tag{2}$$

$$v_O = v_G - \left(-v_C\right) \tag{3}$$

Mode 2: OFF-state $[D(t)T_{SW} \le t \le T_{SW}]$.

When switch SW_1 turns off at t = D×Tsw, diode D_1 turns on. A similar analysis gives the equations for voltage and current as follows:

$$v_{L1}(t) = L_1 \frac{\partial i_{L1}}{dt} = v_G - v_{C1} \; ; \quad v_{L2}(t) = L_2 \frac{\partial i_{L2}}{dt} = -v_C \tag{4}$$

$$i_{C1}(t) = C_1 \frac{\partial v_{C1}}{dt} = -i_{L1} \; ; \quad i_C(t) = C \frac{\partial v_C}{dt} = i_{L2} - i_O \tag{5}$$

The average inductor voltage (v_{L1}, v_{L2}) must be zero at steady-state. Hence, analyzing the volt-sec balance for inductors (L_1, L_2) during a switching period T_{SW}, we obtain:

$$v_{L1}(t) = 0 \rightarrow v_G \cdot D(t) + \left\{v_G - v_{C1}\right\} \cdot \left\{1 - D(t)\right\} = 0 \tag{6}$$

$$v_{L2}(t) = 0 \rightarrow \left\{v_{C1} - v_C\right\} \cdot D(t) - v_C \cdot \left\{1 - D(t)\right\} = 0 \tag{7}$$

As input voltage (v_G) is assumed to be constant over a switching period. Solving for steady-state output voltage v_O then,

$$v_O = v_G \frac{1}{1 - D} \tag{8}$$

In this way, the voltage gain "*M*" of the Cuk converter in partial-power processing architecture will be

$$\frac{v_O}{v_G} = \frac{1}{1 - D} = M \tag{9}$$

Likewise, the instantaneous value in the duty cycle ratio $D(t)$ depends on the input voltage v_G, and can be expressed as

$$D = 1 - \frac{v_G}{v_O} = 1 - \frac{1}{M} \tag{10}$$

Similarly, the average capacitor current (v_C, v_{C1}) must be zero in steady-state. Hence, analyzing the current-sec balance for the capacitors (C, C_1) during a T_{SW} switching period, we obtain:

$$i_{C1}(t) = 0 \rightarrow i_{L2} \cdot D(t) + \left(-i_{L1}\right) \cdot \left\{1 - D(t)\right\} = 0 \tag{11}$$

$$i_C(t) = 0 \rightarrow \left\{i_{L2} - i_O\right\} \cdot D(t) + \left\{i_{L2} - i_O\right\} \cdot \left\{1 - D(t)\right\} = 0 \tag{12}$$

Solving for the current in the inductors (i_{L1}, i_{L2}) in steady-state then,

$$i_{L1} = i_{L2} \frac{D}{1-D}; \quad i_{L2} = i_O \tag{13}$$

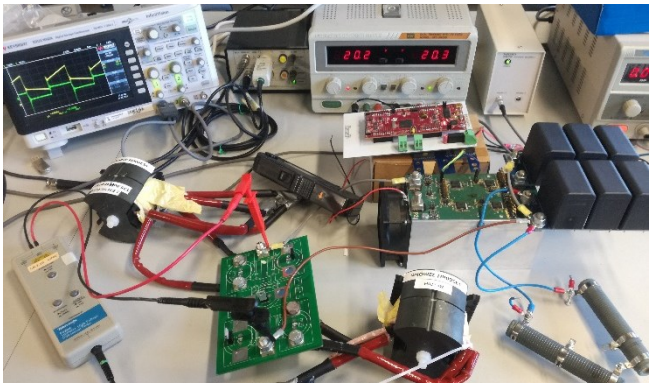

Fig. 4. Experimental testing of the Cuk converter in partial-power processing architecture.

And calculating the current i_G supplied by the voltage source v_G, we obtain (14).

$$i_G = i_{L1} + i_O = i_O \frac{1}{1-D} \tag{14}$$

3. Improved Cuk Converter in Partial-Power Architecture

In this section, some modifications to the typical Cuk converter have been introduced. The objective is to obtain the voltage gain in the partial-power processing architecture in each of the cases analyzed. As in the previous discussion, in order to simplify the steady-state analysis, some assumptions are made, such as ideal switching devices and inductors.

Figure 5 shows the double inductor Cuk converter in partial-power processing architecture. In this case, the inductor L_1 has been replaced by a network of diodes and coils. Again, for a T_{SW} sampling time, the switch is ON-state for $D \times T_{SW}$ and OFF-state for $(1 - D) \times T_{SW}$. Therefore, depending on the state of the switch, two modes of operation can be identified.

Mode 1: ON-state [$0 \leq t \leq D(t)T_{SW}$].

At the initial time t = 0, when switch SW_1 turns on, diode D_1 turns off. Likewise, diodes D_{N1} and D_{N2} are in conduction while diode D_{N3} remains in cut-off. The inductor currents (i_{L1}, i_{L2} and i_{L3}) increase from their respective initial value. In this case, the voltage and current equations are as follows:

$$v_{L1}(t) = L_1 \frac{\partial i_{L1}}{dt} = v_G; \quad v_{L2}(t) = L_2 \frac{\partial i_{L2}}{dt} = v_G \tag{15}$$

$$v_{L3}(t) = L_3 \frac{\partial i_{L3}}{dt} = v_{C1} - v_C \tag{16}$$

$$i_{C1}(t) = C_1 \frac{\partial v_{C1}}{dt} = i_{L3}; \quad i_C(t) = C \frac{\partial v_C}{dt} = i_{L3} - i_O \tag{17}$$

$$v_O = v_G - \left(-v_C\right) \tag{18}$$

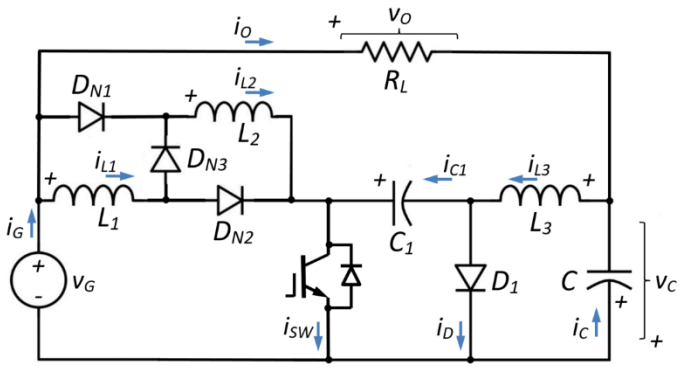

Fig. 5. Improved Cuk converter in partial-power processing architecture. Now the model has a double inductor at the input of the converter.

Mode 2: OFF-state [$D(t)T_{SW} \leq t \leq T_{SW}$].

When switch SW_1 turns off at t = D×T_{SW}, diode D_1 turns on. Now the D_{N1} and D_{N2} diodes turn off, meanwhile, the D_{N3} diode turns on. A similar analysis gives the equations for voltage and current as follows:

$$v_{L1}(t) = L_1 \frac{\partial i_{L1}}{dt}; \quad v_{L2}(t) = L_2 \frac{\partial i_{L2}}{dt} \tag{19}$$

$$v_{L1}(t) = v_{L2}(t); \quad v_{L1}(t) = \frac{1}{2}\left(v_G - v_{C1}\right) \tag{20}$$

$$v_{L3}(t) = L_3 \frac{\partial i_{L3}}{dt} = -v_C \tag{21}$$

$$i_{C1}(t) = C_1 \frac{\partial v_{C1}}{dt} = -i_{L1}; \quad i_C(t) = C \frac{\partial v_C}{dt} = i_{L3} - i_O \tag{22}$$

The average inductor voltage (v_{L1}, v_{L2} and v_{L3}) must be zero at steady-state. Hence, analyzing the volt-sec balance for inductors (L_1, L_3) during a switching period T_{SW}, we obtain:

$$v_{L1}(t) = 0 \rightarrow v_G \cdot D(t) + \frac{1}{2}\left\{v_G - v_{C1}\right\} \cdot \left\{1 - D(t)\right\} = 0 \tag{23}$$

$$v_{L3}(t) = 0 \rightarrow \left\{v_{C1} - v_C\right\} \cdot D(t) - v_C \cdot \left\{1 - D(t)\right\} = 0 \tag{24}$$

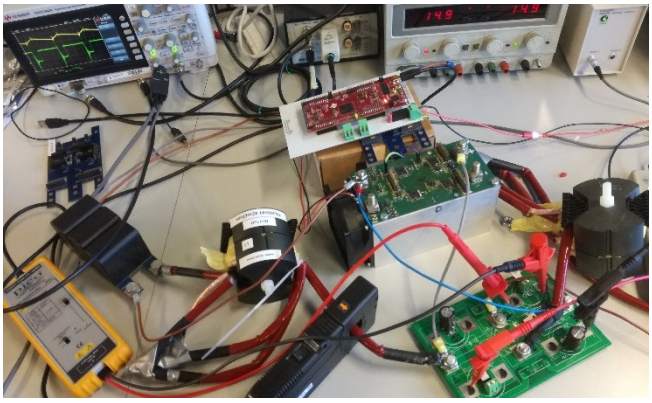

Fig. 6. Experimental testing of the improved Cuk converter in partial-power processing architecture.

As input voltage (v_G) is assumed to be constant over a switching period. Solving for steady-state output voltage v_O then,

$$v_O = v_G \frac{1 + D^2}{1 - D} \tag{25}$$

In this case, a quadratic converter has been obtained, where the voltage gain "M" is,

$$\frac{v_O}{v_G} = \frac{1 + D^2}{1 - D} = M \tag{26}$$

Therefore, for the same value of the duty cycle $D(t)$, the improved Cuk converter with a double inductor provides a higher voltage gain.

Another additional alternative to this Cuk architecture is the incorporation of the double capacitor C_1. Figure 7 shows the double capacitor Cuk converter in partial-power processing architecture. In this case, the capacitor C_1 has been replaced by a network of diodes and capacitors. Again, for a T_{SW} sampling time, the switch is ON-state for $D \times T_{SW}$ and OFF-state for $(1 - D) \times T_{SW}$. Therefore, depending on the state of the switch, two modes of operation can be identified.

Mode 1: ON-state $[0 \le t \le D(t)T_{SW}]$.

At the initial time t = 0, when switch SW_1 turns on, diodes D_1 and D_2 turn off. The inductor currents (i_{L1}, i_{L2}) increase from their respective initial value. In this case, the voltage and current equations are as follows:

$$v_{L1}(t) = L_1 \frac{\partial i_{L1}}{dt} = v_G \; ; \quad v_{L2}(t) = L_2 \frac{\partial i_{L2}}{dt} = 2v_{C1} - v_C \tag{27}$$

$$i_{C1}(t) = C_1 \frac{\partial v_{C1}}{dt} = i_{L2} \; ; \quad i_C(t) = C \frac{\partial v_C}{dt} = i_{L2} - i_O \tag{28}$$

$$v_O = v_G - \left(-v_C\right) \tag{29}$$

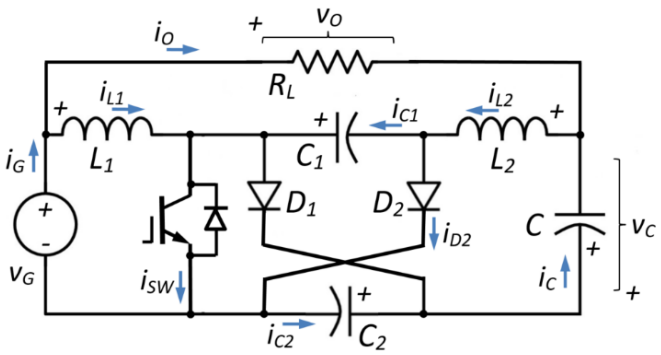

Fig. 7. Improved Cuk converter in partial-power processing architecture. Now the model has a double capacitor in the middle of the Cuk converter.

Mode 2: OFF-state $[D(t)T_{SW} \le t \le T_{SW}]$.

When switch SW_1 turns off at t = D ×TSW, diode D_1 and D_2 turn on. A similar analysis gives the equations for voltage and current as follows:

$$v_{L1}(t) = L_1 \frac{\partial i_{L1}}{dt} = v_G - v_{C1} \; ; \quad v_{C1} = v_{C2} \tag{30}$$

$$v_{L2}(t) = L_2 \frac{\partial i_{L2}}{dt} = v_{C1} - v_C \tag{31}$$

$$i_{C1}(t) = C_1 \frac{\partial v_{C1}}{dt} = \frac{1}{2}\left(i_{L2} - i_{L1}\right) \tag{32}$$

$$i_C(t) = C \frac{\partial v_C}{dt} = i_{L2} - i_O \tag{33}$$

$$i_{D1} = i_{D2} = \frac{1}{2}\left(i_{L1} + i_{L2}\right) \tag{34}$$

The average inductor voltage (v_{L1}, v_{L2}) must be zero at steady-state. Hence, analyzing the volt-sec balance for inductors (L_1, L_2) during a switching period T_{SW}, we obtain:

$$v_{L1}(t) = 0 \rightarrow v_G \cdot D(t) + \left\{v_G - v_{C1}\right\} \cdot \left\{1 - D(t)\right\} = 0 \tag{35}$$

$$v_{L2}(t) = 0 \rightarrow \left\{2v_{C1} - v_C\right\} \cdot D(t) + \left\{v_{C1} - v_C\right\} \cdot \left(1 - D(t)\right) = 0 \tag{36}$$

As input voltage (v_G) is assumed to be constant over a switching period. Solving for steady-state output voltage v_O then,

$$v_O = v_G \frac{2}{1 - D} \tag{37}$$

In this new partial-power topology, the voltage gain "M" obtained in the improved Cuk converter is,

$$\frac{v_O}{v_G} = \frac{2}{1-D} = M \tag{38}$$

Another additional topology is described in Fig. 8. In this case, the dual capacitor Cuk converter is shown in a partial-power processing architecture. Now, the initial capacitor C_1 has been replaced by a network of diodes (D_{N1}, D_{N2}, D_{N3}) and capacitors (C_1, C_2). Again, for a T_{SW} sampling time, the switch is ON-state for $D \times T_{SW}$ and OFF-state for $(1 - D) \times T_{SW}$. Therefore, depending on the state of the switch, two modes of operation can be identified.

Mode 1: ON-state [$0 \le t \le D(t)T_{SW}$].

At the initial time t = 0, when switch SW_1 turns on, diodes D_{N1} and D_{N2} turn on, while D_{N3} turns off. The inductor currents (i_{L1}, i_{L2}) increase from their respective initial value. In this case, the voltage and current equations are as follows:

$$v_{L1}(t) = L_1 \frac{\partial i_{L1}}{dt} = v_G \; ; \quad v_{L2}(t) = L_2 \frac{\partial i_{L2}}{dt} = v_{C1} - v_C \tag{39}$$

$$i_{C1}(t) = C_1 \frac{\partial v_{C1}}{dt} = \frac{1}{2} i_{L2} \; ; \quad i_C(t) = C \frac{\partial v_C}{dt} = i_{L2} - i_O \tag{40}$$

$$v_O = v_G - \left(-v_C\right) \tag{41}$$

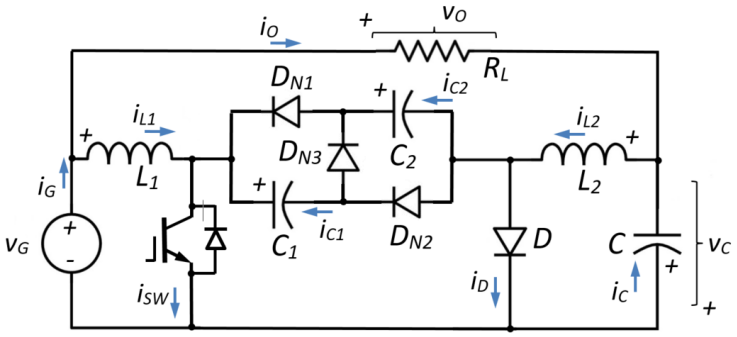

Fig. 8. Dual capacitor Cuk converter in partial-power processing architecture.

Mode 2: OFF-state [$D(t)T_{SW} \le t \le T_{SW}$].

When switch SW_1 turns off at t = D×T_{SW}, diode D_{N1} and D_{N2} turn off, while D_{N3} turns on. A similar analysis gives the equations for voltage and current as follows:

$$v_{L1}(t) = L_1 \frac{\partial i_{L1}}{dt} = v_G - 2v_{C1} \; ; \quad v_{C1} = v_{C2} \tag{42}$$

$$v_{L2}(t) = L_2 \frac{\partial i_{L2}}{dt} = -v_C \tag{43}$$

$$i_{C1}(t) = C_1 \frac{\partial v_{C1}}{dt} = -i_{L1} \; ; \quad i_{C1} = i_{C2} \tag{44}$$

$$i_C(t) = C \frac{\partial v_C}{dt} = i_{L2} - i_O \tag{45}$$

$$i_{D3} = i_{L1} \tag{46}$$

The average inductor voltage (v_{L1}, v_{L2}) must be zero at steady-state. Hence, analyzing the volt-sec balance for inductors (L_1, L_2) during a switching period T_{SW}, we obtain:

$$v_{L1}(t) = 0 \rightarrow v_G \cdot D(t) + \left\{v_G - 2v_{C1}\right\} \cdot \left\{1 - D(t)\right\} = 0 \tag{47}$$

$$v_{L2}(t) = 0 \rightarrow \left\{v_{C1} - v_C\right\} \cdot D(t) - v_C \cdot \left\{1 - D(t)\right\} = 0 \tag{48}$$

As input voltage (v_G) is assumed to be constant over a switching period. Solving for steady-state output voltage v_O then,

$$v_O = v_G \frac{2 - D}{2\left(1 - D\right)} \tag{49}$$

In this additional partial-power architecture, the voltage gain "*M*" obtained in the dual capacitor Cuk converter is,

$$\frac{v_O}{v_G} = \frac{2-D}{2(1-D)} = M \tag{50}$$

Table I shows a comparison between the voltage gains in different full-power and partial-power architectures. It should be noted that in the Cuk full-power topology, the output voltage v_O can be higher or lower than the input voltage v_G, as the duty cycle (D) increases. Whereas in Cuk partial-power architecture, the output voltage v_O is always higher than the input voltage v_G depending on the value adopted by the duty cycle (D). The non-isolated partial-power converter used has shown good results in terms of efficiency and power density. Traditionally, the load is connected to the output (v_C) of the DC-DC converter. In other words, in the full-power topology, this converter processes all the power supplied to the load. Meanwhile, in partial-power architecture, the load is connected in series between the input voltage (v_G) and the Cuk converter output (v_C).

TABLE I. COMPARISON DIFFERENT PROPOSED CUK CONVERTERS IN FULL-POWER AND PARTIAL-POWER ARCHITECTURE.

Converter model	Voltage-Gain in Full-Power	Voltage-Gain in Partial-
Buck-Boost Converter	$\frac{D}{(1-D)}$	$\frac{1}{(1-D)}$
Hybrid-Boost Converter [20]	$\frac{3-D}{(1-D)}$	---
Typical Cuk Converter	$\frac{D}{(1-D)}$	$\frac{1}{(1-D)}$
Improved Cuk Converter (2L)	$\frac{D(1+D)}{(1-D)}$	$\frac{1+D^2}{(1-D)}$
Improved Cuk Converter (2C)	$\frac{1+D}{(1-D)}$	$\frac{2}{(1-D)}$
Dual Capacitor Cuk Converter	$\frac{D}{2(1-D)}$	$\frac{2-D}{2(1-D)}$

TABLE II. PARAMETERS ASSOCIATED WITH THE NON-ISOLATED CUK PARTIAL-POWER CONVERTER MODEL.

Parameter	Symbol	Value
DC-bus voltage	v_G	+25V
Module internal resistance	r_{DC}	0.1Ω
Cuk inductors	L_1, L_2	2.5mH
Cuk capacitor	C_1, C_2	500μF
Switching frequency	f_{SW}	20kHz
Switch resistance S_1, S_2	R_{on}	0.01Ω
Schottky forward voltage	v_F	0.3V
Snubber network	Rs, Cs	100kΩ; 1nF
Output Capacitor	C	250μF
Load resistance	R_L	50Ω

4. Simulation Results

In order to study the properties and characteristics of the improved non-isolated Cuk converter in applied partial-power architecture, the topology shown in the previous figures has been modeled. The simulation software used has been *Matlab-Simulink*. At the same time, an average voltage mode control has been developed. Likewise, Table II contains some of the parameters used in the model.

Figure 8 represents the different voltages (v_{S1}, v_{D1}) in the semiconductor devices and the voltage and current in the capacitor (v_{C1}, i_{C1}) respectively, as well as the inductor currents (i_{L1}, i_{L2}) of the non-isolated Cuk converter in the partial-power processing architecture. These waveforms correspond to the topology shown in Fig. 3. In this case, the switching frequency f_{SW} corresponds to f_{SW} = 20kHz.

Under these conditions, the following values were obtained: DC-bus voltage v_G = +25V, output voltage v_O = +100V, capacitor voltage C_1 (v_{C1} = +100V), average DC-bus current i_G = 8.212A, while the average currents of the inductors i_{L1} = 6.212A and i_{L2} = 2A and the value of the current in the load R_L is i_O = 2A. Meanwhile, the average switch current i_{S1} and the average diode current i_D are i_{S1} = 6.212A and i_D = 2A, respectively. In this case, for the Cuk partial-power topology, the duty cycle results $D_{S1|PP}$ = 0,756.

Figs. 9 and 10 show a comparison of the peak currents i_{L1}, i_{S1} and i_{C1} for the Cuk converter in full-power and partial-power topology. In both cases, an output voltage v_O = +100V has been considered. Now in the full-power topology, the duty cycle corresponds to $D_{S1|FP}$ = 0,807. As can be seen in the figures, for the same power supplied to the R_L load, the peak currents are higher in the full-power topology than in the partial-power architecture. In the extended paper, more oscillograms will be shown comparing the different architectures discussed in the previous sections. In this way, the advantages and drawbacks of

each of the architectures presented will be observed. The limitation of pages in the abstract has limited the simulation results shown.

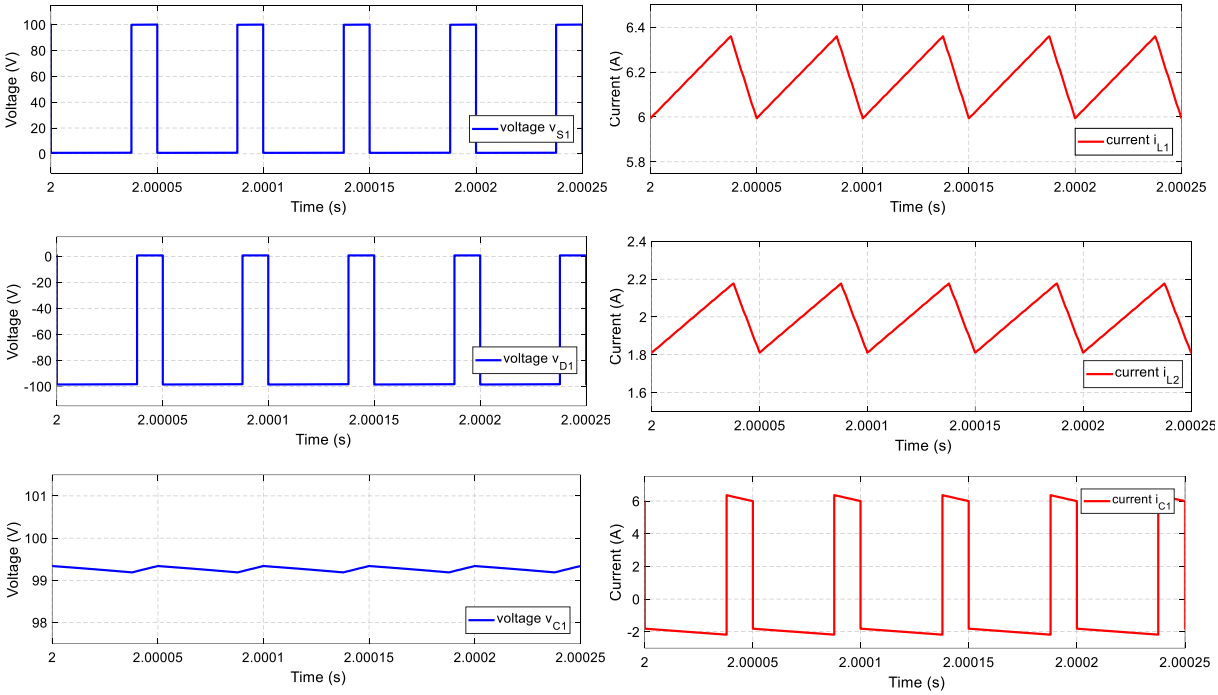

Fig. 9. Steady-state response of the non-isolated Cuk converter in partial-power architecture: v_{S1}, i_{L1}, v_{S2}, i_{L2}, v_{C1} and i_{C1}. Voltages and currents to provide a converter output voltage v_O = +100V (duty cycle D = 0.756).

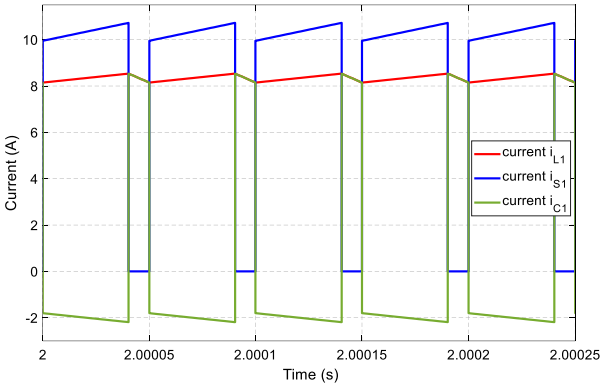

Fig. 10. Steady-state response of the non-isolated Cuk converter in full-power topology. Currents i_{L1}, i_{S1} and i_{C1} to provide a converter output voltage v_O = +100V (duty cycle D_{FP} = 0.807).

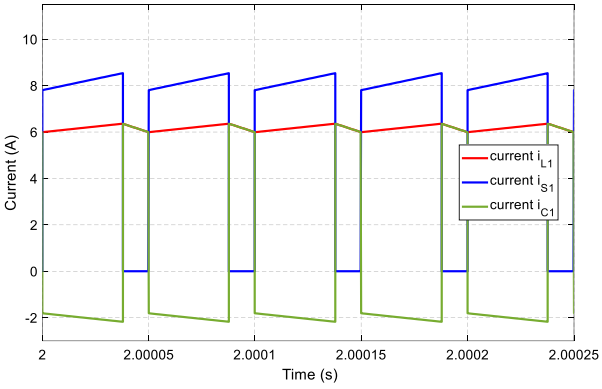

Fig. 11. Steady-state response of the non-isolated Cuk converter in partial-power topology. Currents i_{L1}, i_{S1} and i_{C1} to provide a converter output voltage v_O = +100V (duty cycle D_{PP} = 0.756).

5. Conclusions

This paper presents the analysis of different non-isolated Cuk converters in partial-power processing architecture. The purpose has been to compare both architectures (full-power and partial-power converter) to validate their advantages. In the same way, the improved Cuk converter has been studied, analyzing its use in partial-power architecture. The different simulation models have been developed with the *Matlab-Simulink* software. The results obtained support the different equations of the mathematical model studied.

In view of the simulation results obtained, the stress on the different devices is higher in the full-power architecture than in the partial-power architecture, for the same power supplied to the load. The partial-power topology only processes a fraction of the supplied power, reducing power losses and increasing system efficiency. In this way, it is possible to reduce the cost, volume, and weight of the converter.

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