A bidirectional hybrid DC transformer with high power transmission

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***Abstract*--This paper proposes a bidirectional hybrid DC transformer (BHDC) which can ensure smooth dc currents without DC filter. It has lower cost and weight than traditional MMC-FTF. The effectiveness of BHDC is verified by simulation results that converts 40kV to 400V with rated ±100MW.**

***Index Terms*—Dc/dc converter, High power ,Isolated type, modular multilevel transformer**

I. Introduction

With the exploiting of renewable energy sources, high voltage dc (HVDC) grids based on voltage source converter (VSC) has become one feasible solution to transmit a large amount of renewable energy over long distance [1]. The future development trend of VSC-HVDC is upgrading to the DC grid [2], [3]. However, DC transformer is the technical challenge to be solved, which is very essential to interconnect DC lines with different voltage levels and improve overall operational flexibility and reliability [4].

Modular multilevel converter (MMC) is considered as a promising topology for medium voltage (MW) and high voltage (HV) applications. By using the MMC based front-to-front DC-DC converter (MMC-FTF) [5], the high-power bidirectional power transmission can be realized. However, a large number of power devices and submodules (SM) are used, resulting in high cost and weight [6].

This paper proposes a bidirectional hybrid DC transformer (BHDC) which ensures smooth DC currents without DC filters and has lower cost and weight than the traditional MMC-FTF.

II. Topology Description and Operation Principle

A. Circuit configuration

The circuit configuration of the proposed bidirectional hybrid DC transformer (BHDC) is shown in Fig. 1. It has a front-to-front configuration with the same circuit structure in the medium-voltage dc (MVDC) side and high-voltage dc (HVDC) side. The circuit in each side consists of three series-connected bidirectional thyristors assembly T_j/T_J (for MVDC side j=a, b, c, and for HVDC side J=A, B, C), three arms P_j/P_J cascaded by half-bridge submodules (SMs) and arm inductances L_j/L_J. The circuits in two side are connected through a wye-wye connected 1:n three phase transformer. The terms U_M and I_M are the voltage and current of the MVDC side, U_H and I_H are the[1] voltage and current of the LVDC side, respectively. L_{kj} is the transformer leakage inductor.

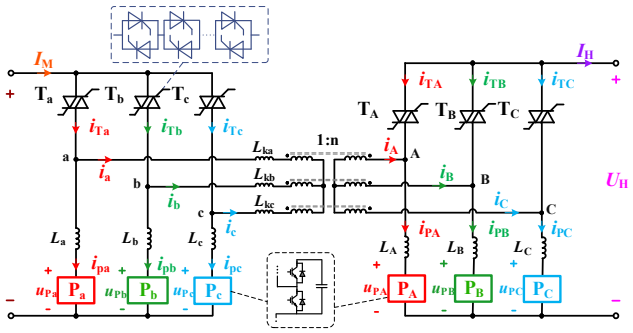

Fig. 1. Circuit configuration of the proposed BHDC.

B. Operation principle

Fig. 2 shows the operation waveforms of the proposed BHDC when the power is transmitted from the MVDC side to HVDC side. The current waveforms of thyristors T_a~T_c and the thyristors T_A~T_C, as show in Fig. 2(a) and Fig. 2(b), respectively, are sequentially conducted, and there is certain overlap time T_i between two conducted thyristors to achieve current commutations. The thyristor currents i_{Tj} and i_{TJ} are controlled to be staggered

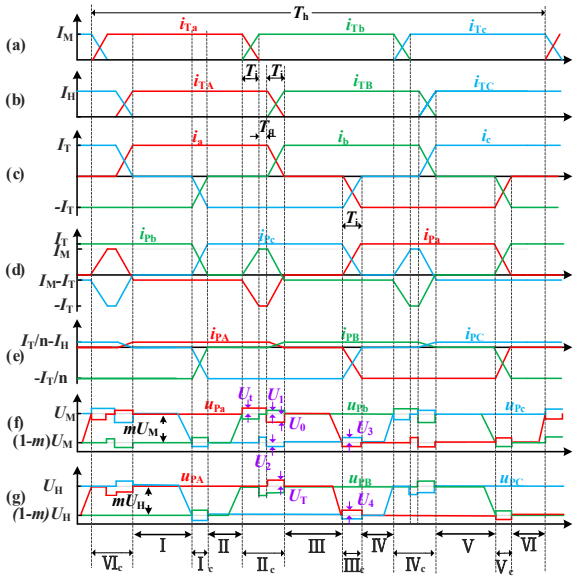

Fig. 2. Principle waveforms of the BHDC topology

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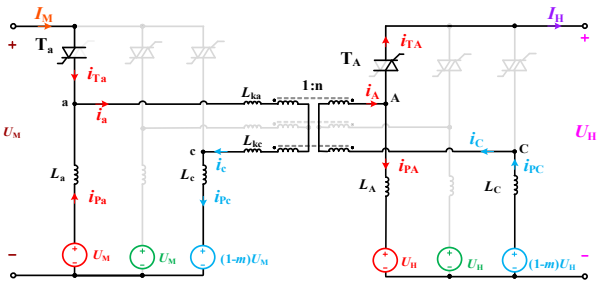
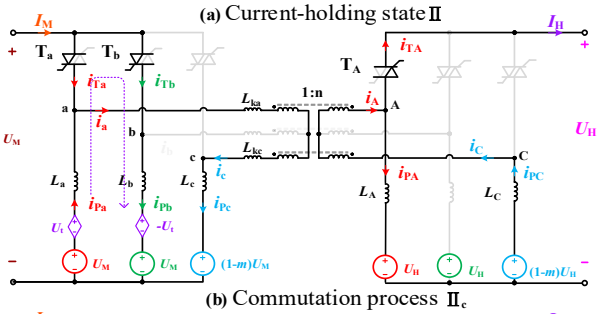
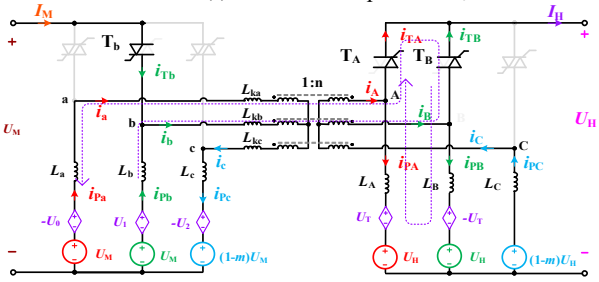


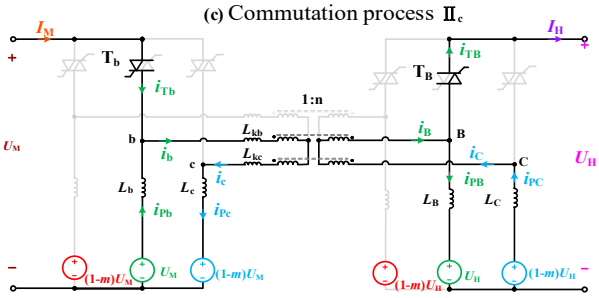
(a) Current-holding state Ⅱ



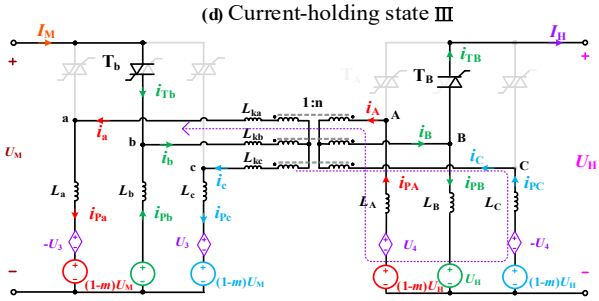
(b) Commutation process Ⅱc



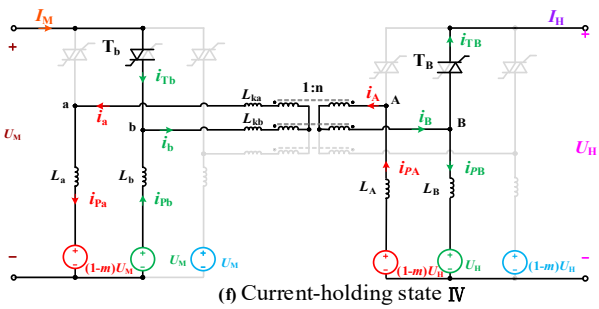
(c) Commutation process Ⅱc



(d) Current-holding state Ⅲ



(e) Commutation process Ⅲc



(f) Current-holding state Ⅳ

trapezoidal waves with amplitudes of I_M and I_H, respectively, so as to synthesize smooth input and output DC currents without additional filters. Meanwhile, as shown in Fig. 2(c), transformer currents i_a~i_c are also staggered trapezoidal waves with the amplitude of I_T. Arm voltages of the MVDC and the HVDC are shown in Fig. 2(f) and Fig. 2(g), respectively.

In each operation cycle T_h, there are six current-holding states I~VI, in which currents of two phase are kept constant while the third phase is with zero current. Taking current-holding state II as an example, the equivalent circuit of BHDC is shown in Fig. 3(a). The power is directly transferred from the MVDC side to the HVDC side through thyristor T_a, T_A, arm P_a, and P_A, in which the transformer currents i_a=−i_c=I_T. The arms P_c and P_C withstand the voltage differences $(1-m)U_M$ and $(1-m)U_H$, respectively. It should be noted that since the arm is consisted of series-connected half-bridge SMs, m<1 should be satisfied to ensure positive arm voltage. Meanwhile, P_a and P_A sustain the current differences I_T-I_M and $I_T/n-I_H$, respectively.

To avoid the transformer saturation, there are six commutation states I_c~VI_c between adjacent current-holding states. As shown in Fig. 2, commutation states can be divided into two types. The first types of commutation state are II_c, IV_c, and VI_c, in which DC currents I_M and I_H are commutated between two conducted thyristors, and the transformer currents are commutated between two phase-windings. The second types of commutation state are I_c, III_c, and V_c, in which thyristor currents and arm currents are commutating between two phases. Both types of commutations are achieved by adjusting arm voltages to generate the commutation voltage across corresponding inductors L_j, L_{kj} and L_J. As a result, the thyristor current or arm current of one phase decreases linearly, whereas current of another phase rises at the same rate, and the DC current I_M and I_H keep constant. In addition, for keeping currents of the third phase as constant, the inductance voltage of this phase should be controlled to zero by properly adjusting the arm voltage. Take commutation states II_c and III_c as examples to explain in detail:

For commutation process II_c, the currents are commutated between phase a and phase b by adjusting voltage difference between u_{Pa}/u_{PA} and u_{Pc}/u_{PC}. However, it can be seen from Fig.3 (b), u_{Pa} should be higher than u_{Pb} to realize the commutation between T_a and T_b. Whereas, as can be seen from Fig.3 (c) that u_{Pa} should be lower than u_{Pb} to commutate currents between a and b phase-windings. Therefore, firstly u_{Pa} and u_{Pb} are adjusted to U_M+U_t and U_M-U_t, respectively, resulting in u_{Lb}=−u_{La}=−U_t. Thus, during the commutation time T_i, thyristor current i_{Ta} decreases linearly from I_M to 0, while i_{Tb} increases linearly from 0 to I_M at the same rate. After i_{Ta} drops to zero, u_{Pa} maintains the voltage U_M+U_t, Therefore, a reverse voltage U_t is applied to T_a within the time T_q to ensure its reliable turn-off. After T_a reliably turned off, the u_{Pa} and u_{Pb} are adjusted to U_M-U_0 and U_M+U_1, respectively, so that i_a decreases linearly from I_T to 0, while i_b increases linearly from 0 to I_T at the same rate, and I_M remains constant. Meanwhile, u_{Pc} is adjusted to $(1-m)U_M-U_2$ to keep i_{Pc} as

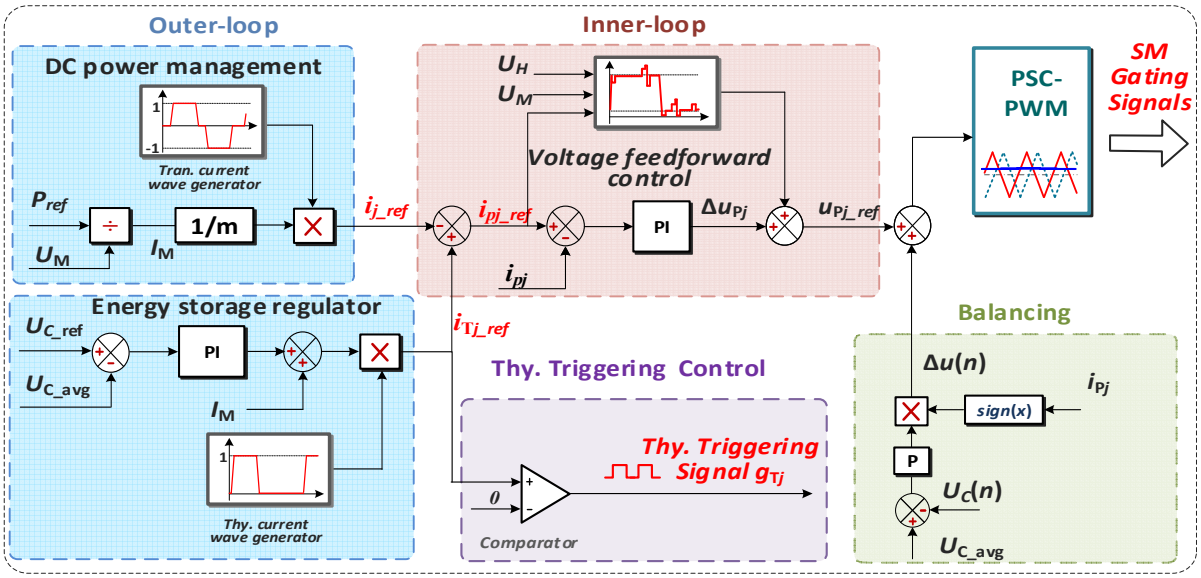


Fig. 4. Control block diagram of supposed BHDC

constant. Besides, adjusting the arm voltages u_{PA} and u_{PB} to U_H+U_T and U_H-U_T, respectively, resulting in $u_{LB}=-u_{LA}=-U_T$. Thus, during the commutation time T_i, the thyristor current i_{TA} decreases linearly from $I_T/n-I_H$ to 0, while i_{TB} increases from 0 to $I_T/n-I_H$ at the same rate. It should be mentioned that the MVDC and HVDC currents (I_M and I_H) are constant DC during the whole commutation state II_c, and no additional filtering device is required.

For the commutation state III_c, the currents are commutated between a and c phase-windings by adjusting voltages between u_{Pa}/u_{PA} and u_{Pc}/u_{PC}. The corresponding circuit is shown in Fig.3 (e). Adjusting the MVDC side arms voltages u_{Pa} and u_{Pc} to $(1-m)U_M-U_3$ and $(1-m)U_M+U_3$, the HVDC side arms voltages u_{PA} and u_{PC} to $(1-m)U_H+U_4$ and $(1-m)U_H-U_4$, respectively. As a result, i_a ($-i_{Pa}$) declines from 0 to $-I_T$, and i_c ($-i_{Pc}$) rises from $-I_T$ to 0.

Based on the above principle, the operation waveforms of other current-holding states and commutation states are similarly achieved to ensure the symmetry of three-phase waveforms. Fig.3 shows the commutation process when the power is transmitted from the MVDC side to the HVDC side. When power is transmitted from the HVDC to the MVDC, all the currents and the commutation voltages are reversed.

C. Component parameters

As showed in Fig. 3(c), in the MVDC side, the maximum arm voltage is U_M+U_0. In the HVDC side, the maximum arm voltage is U_H+U_T. Therefore, the number of SMs per arm of MVDC side (N_M) and HVDC side (N_H) can be derived respectively as:

$$N_M \geq \frac{U_M+U_0}{U_{CM}} = \frac{U_M T_i m + I_T(L_j+2L_{kj})}{U_{CM} T_i m} \quad (1)$$

$$N_H \geq \frac{U_H+U_T}{U_{CH}} = \frac{U_H T_i + I_H L_J}{U_{CH} T_i} \quad (2)$$

where U_{CM} and U_{CH} are the SMs rated voltage in the MVDC side and HVDC side, respectively, L_j and L_J are arm inductances, L_{kj} is the transformer leakage inductance, T_i is the commutation time, T_q is the thyristor reverse voltage time, and n is the transformer ratio.

For the design of the SMs capacitance, it is mainly considered to limit the capacitance voltage fluctuation to a certain range. According the waves of arm voltages and currents in Fig.2, the MVDC side SM capacitance C_M and the HVDC side SM capacitance C_H can be calculated as:

$$C_M \geq \frac{P}{3f_h N_M U_{CM}^2 \varepsilon_{pp}}\left[\left(\frac{1}{m}-1\right)+3f_h(T_i+T_q)\right] \quad (3)$$

$$C_H \geq \frac{P}{3f_h N_H U_{CH}^2 \varepsilon_{pp}}\left(\frac{1}{m}-1\right) \quad (4)$$

where f_h is the operation frequency, and ε_{pp} is the voltage peak ripple rate of the capacitances.

The design of the arm inductances and transformer leakage inductances needs to comprehensively consider the DC voltage ripple, and the slope of current wave in the commutation stages. An undersized inductance value will cause the voltage ripple too large, and an oversize inductance value requires a large commutation voltage. The value of arm inductance L_j and L_J, and transformer lack inductance L_{kj} can be derived respectively as:

$$\frac{U_{CM}}{4\varepsilon_i I_M N_M f_{CM}} \leq L_j \leq \frac{T_i U_t}{I_M} \quad (5)$$

$$\frac{U_{CH}}{4\varepsilon_i I_H N_H f_{CH}} \leq L_J \leq \frac{T_i U_T}{I_H} \quad (6)$$

$$L_{kj} \leq \frac{m T_i U_2}{I_M} \quad (7)$$

where f_{CM} and f_{CH} are the carrier wave frequency of MVDC side and HVDC side, respectively, and ε_i is the allowable arm current ripple rate.

D. Control strategy

Fig. 4 shows the control block diagram of one phase at the MVDC side. As seen in Fig.6, according to rated power P_{ref} and MVDC voltage U_M, rated MVDC current I_M and the transformer reference current i_{j_ref} can be obtained.

Arm energy balance is achieved by controlling the amplitude of thyristor current. According to the difference between SMs average voltage U_{C_avg} and the rated SMs voltage U_{C_ref}, the thyristor reference current i_{Tj_ref} can be generated. If i_{T_ref} is nonzero, the thyristor triggering signals is applied. The arm reference current is determined by the difference of the thyristor reference current i_{Tj_ref} and the transformer reference current i_{j_ref}. Then, an inner current control loop is used to track the desired arm current waveforms. Meanwhile, an arm voltage feed forward control is added to improve the dynamic response performance. The voltage balancing control by adjusting the voltage reference of each SM according to the arm current polarity is adopted. Other phases adopt the same control strategy to achieve integral control of the BHDC.

III. SIMULATIONRESULT

To verify the effectiveness of the proposed BHDC, simulations are carried out to converts 40kV to 400kV with rated ±100MW. The rated SMs capacitor voltage U_C is 1.67kV. The operating frequency f_h is 150Hz. More detailed simulation parameters are shown in Table 1.

As seen in Fig. 5 within 0.1s to 0.2s, the power is transmitted from the MVDC side to the HVDC side, and the rated power is 100MW. During 0.2s to 0.5s, currents I_M and I_H of two dc sides are linearly decreased and reversed polarity, meaning the power flow is reversed. During 0.5s to 0.6s, the rated 100MW power is transmitted from the HVDC side to the MVDC side. As seen in Fig. 5 (b), during this process DC current I_M and I_H are relatively smooth without DC filter.

Fig. 6 further shows the zoomed-in waveforms of the topology at steady-state operating condition. The rated power 100MW is transmitted from the MVDC side to the

TABLE I
SIMULATION PARAMERERS

Parameters	Value
Rated power P	±100MW
Operating frequency f_h	150Hz
MV/HV voltage U_M/U_H	40kV/400kV
SM number of MV side N_M	28
SM number of HV side N_H	280
Capacitance of MV side C_M	25mF
Capacitance of HV side C_H	1mF
Rated capacitor voltage U_C	1.67kV
Reverse voltage time T_q	140us
Modulation ratio m	0.85
Transformer ratio n	10
Arm inductance of MV side L_j	0.7mH
Arm inductance of HV side L_J	70mH
Leak inductance L_{kj}	0.1mH

HVDC side. The DC voltages U_M and U_H are 40kV and 400kV, respectively. The thyristor currents i_{Tj} and i_{TJ} are staggered trapezoidal waves with amplitudes of 2500A (=I_M) and 250A(=I_H), respectively. Meanwhile, as can be seen the DC currents are commutated linearly between two adjacent thyristors. As a result, I_M and I_H are both smooth DC currents (as shown in Fig. 6(a)). As shown in Fig. 6(e), the transformer currents i_j are also staggered trapezoidal waves with the amplitude of 2941A, so as to transmit power stably and continuously. Fig. 6(k) and (l) show the SM capacitor voltages of the MVDC and HVDC sides, respectively. As can be seen both of them are stabled at

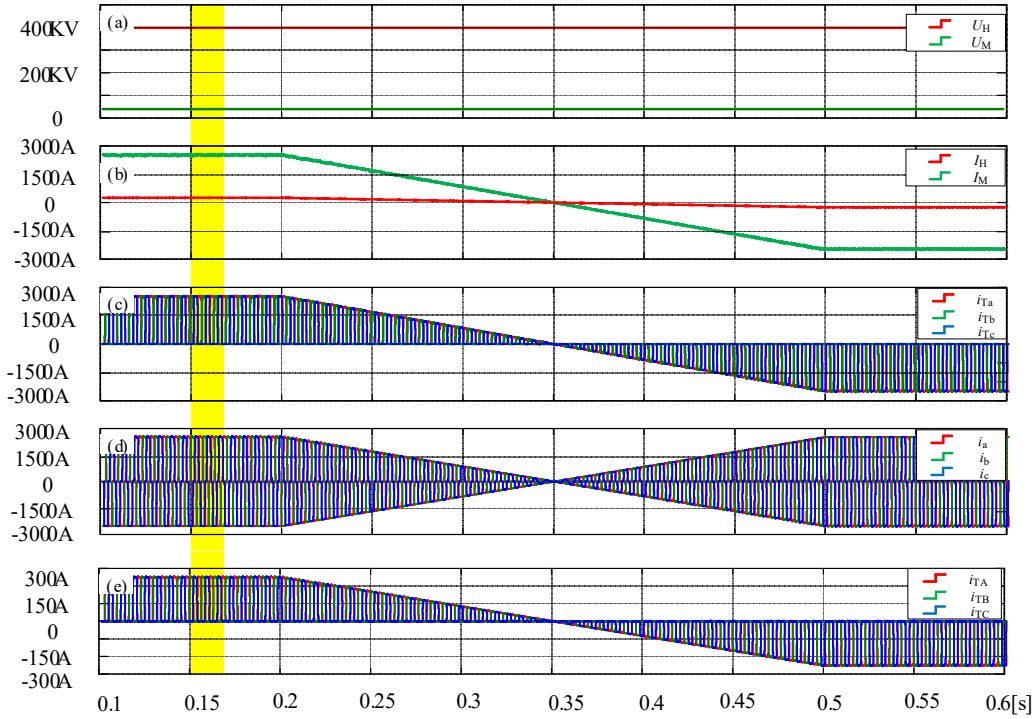


Fig. 5. Dynamical simulation waveforms of the BHDC: (a) Voltages of two DC sides; (b) Currents of two DC side; (c) Thyristor currents of the MVDC side; (d) Transformer currents of the MVDC side; (e) Thyristor currents of the HVDC side;

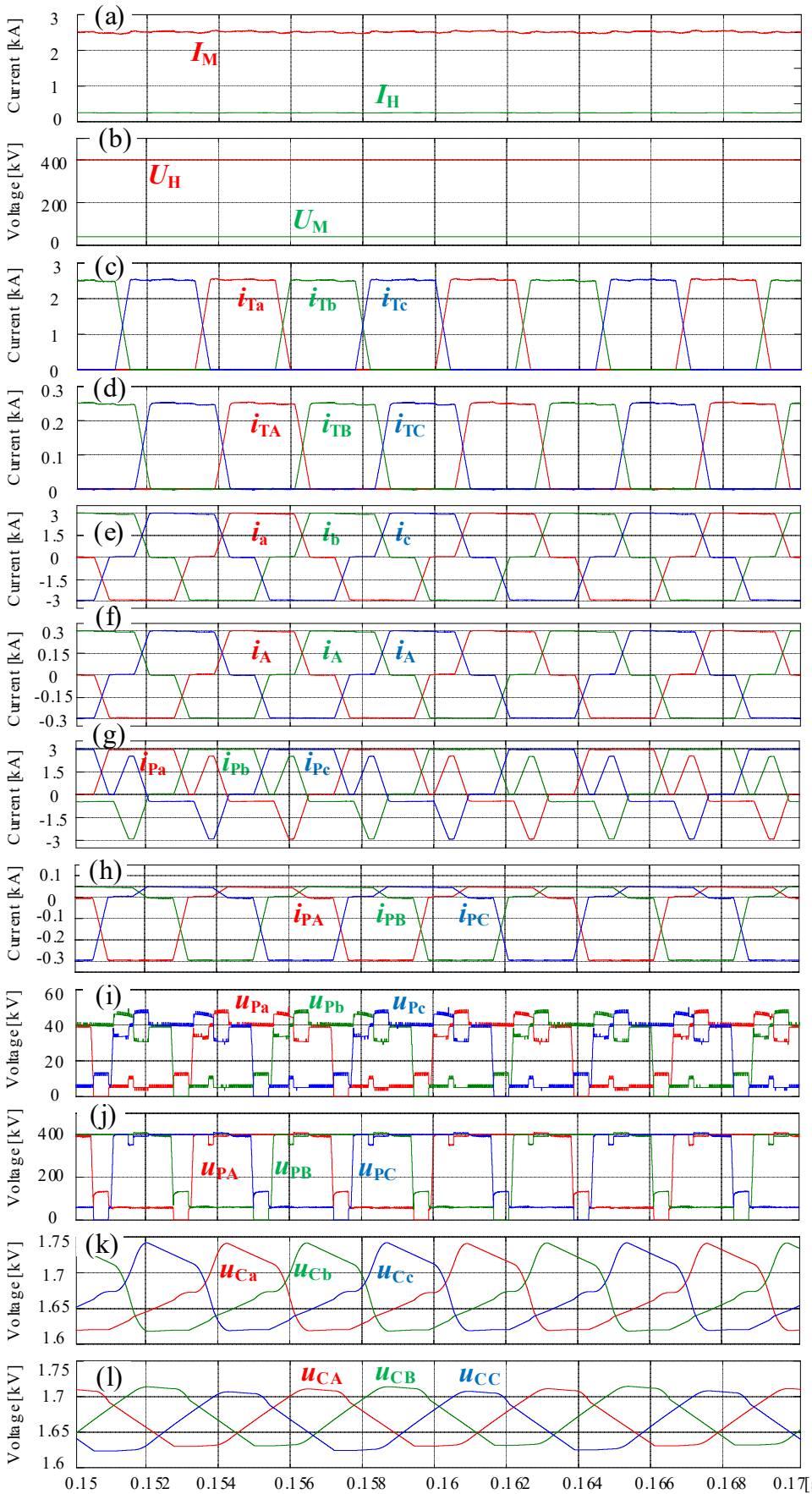


Fig. 6. Steady state simulation waveforms of the BHDC : (a) Currents of two DC sides; (b) Voltages of two DC sides; (c) Thyristor currents of the MVDC side; (d) Thyristor currents of the HVDC side; (e) Transformer currents of the MVDC side; (f) Transformer currents of the HVDC side; (g) Arm currents of the MVDC side; (h) Arm currents of the HVDC side; (i) Arm voltages of the MVDC side; (j) Arm voltages of the HVDC side; (k) Capacitive voltages of the MVDC side; (l) Capacitive voltages of the HVDC side

respectively. rated 1.67kV with a fluctuation of 6% and 4%, respectively. These fluctuations coincide with the calculation results. All of the waveforms confirm the effectiveness of the proposed BHDC.

IV. CONCLUSIONS

A BHDC topology is proposed in this article to realize the power bidirectional transmitting between MVDC and HVDC grids. The proposed BHDC combines the SM arms and the thyristors with low cost and high-power density, which has the advantages of high efficiency, low cost, and light weight. The anti-parallel thyristor and the symmetrical structure enable BHDC to transmit power in both directions. The operation principle is introduced in detail, and their effectiveness is verified by simulation results.

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