High-gain Floating Double Series-capacitor Boost Converter

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***Abstract*-- The floating double boost converter (FBC), including two single boost converters, is a solution for fuel-cell and renewable energy applications. To reduce the inductor currents in the FBC converter, the interleaved boost converters (IBC) are used instead of single boost converters so that the four-phase floating interleaved boost converter (4P-FBC) is formed. However, it is well known that the IBC suffers a significant problem with the unbalanced inductor currents issue, leading to high input current ripple. This paper proposed a floating double series-capacitor boost (FSCB) converter to solve the problem. Moreover, the voltage gain is improved by more than double, and the input current ripple can be minimized. As a result, the proposed converter is suitable for new energy sources, such as fuel-cell and photovoltaic. A 1.6 kW prototype was built and tested to verify the performance of the proposed converter.**

***Index Terms*--current balancing, current ripple, floating boost converter, high gain boost converter, interleaved, input-parallel output-series, series-capacitor converter.**

I. Introduction

With the increasing acquisition of renewable energy sources, the high voltage gain non-isolated DC-DC boost converter has recently been researched in the literature. Among them, the floating double boost converter (FBC) [see Fig. 1] [1]-[6] is a solution when high voltage gain (i.e., $\frac{V_o}{V_{in}} = \frac{1+D}{1-D}$), and low input current ripple is demanded, such as fuel-cell and PV applications. Moreover, on the FBC, the device's voltage rating is lower than the output voltage (V_o), and the inductor currents balancing (or power sharing) is naturally achieved without additional complexity control (i.e., $I_a = I_b$).

The high voltage gain will lead to a high input current. To reduce the inductor current and device current stress, by using the interleaved boost converter (IBC) instead of a single boost converter, the four-phase floating interleaved boost converter (4P-FBC) was introduced [7]-[12] [see Fig. 2]. However, it is well known that the IBC suffers the unbalanced current issue when having a slight mismatch in the gate signals (i.e., $I_{L1a} \neq I_{L2a}$, $I_{L1b} \neq I_{L2b}$), leading to losing the power-sharing and interleaving effect (or higher input current ripple).

To solve the problems of 4P-FBC, the paper proposed a floating double series-capacitor boost (FSCB) converter [see Fig. 3]. By inherent the merits of the series-capacitor boost converter [13]-[19], the FSCB achieves a higher voltage gain (i.e., $\frac{V_o}{V_{in}} = \frac{3+D}{1-D}$), reduces inductor current

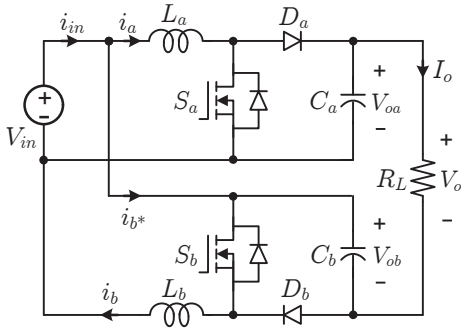


Fig. 1. Floating double boost converter (FBC) [1]-[6].

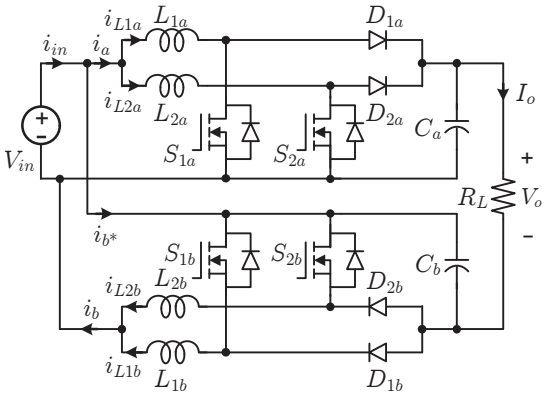


Fig. 2. Four-phase floating interleaved boost converter (4P-FBC) [7]-[12].

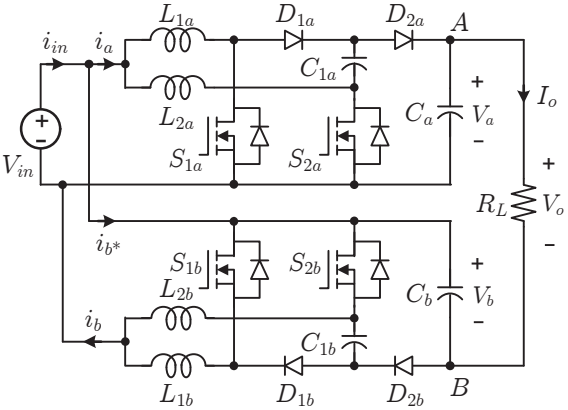


Fig. 3. The proposed converter (FSCB).

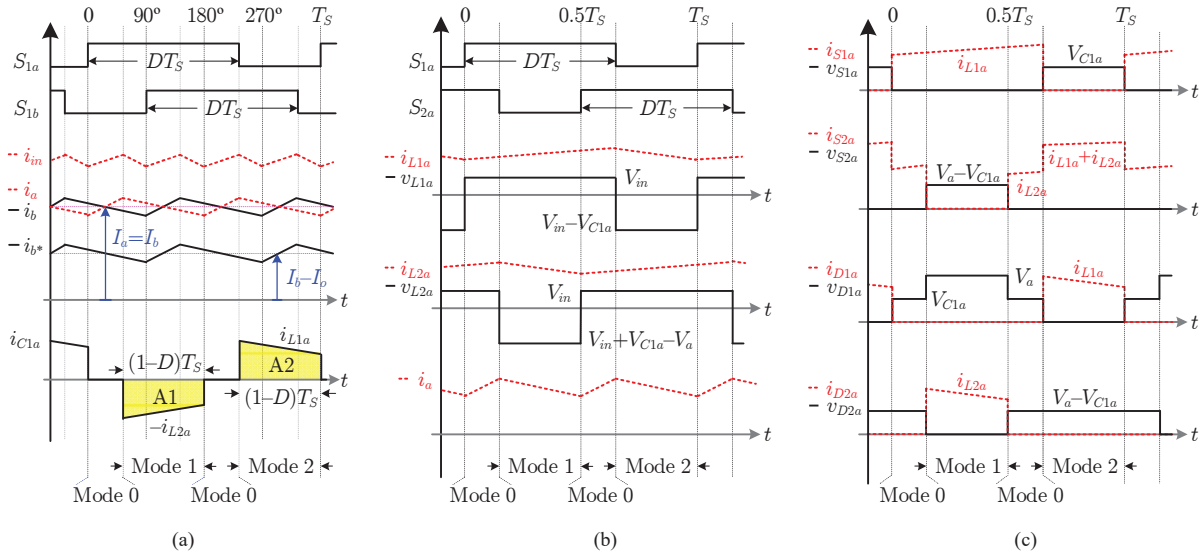


Fig. 4. Key waveforms of the proposed converter. (a) input and capacitor currents. (b) inductor currents. (c) device voltage and current waveforms.

ripple, and natural balances inductor currents (I_{L1a}= I_{L2a}= I_{L1b}= I_{L2b}).

Moreover, with support from capacitor C_1, the voltage stress of S_2 and D_2 reduces by half. Due to the four inductor currents being balanced and equally distributed, the input current ripple is four times the switching frequency waveform. As a result, it can be minimized and achieves zero current ripples at high voltage gain (i.e., D= 0.5 and 0.75). Those mentioned above make it suitable for new energy sources, such as fuel-cell and PV applications. The proposed converter is validated with a 1.6 kW prototype.

II. Characteristics of the Proposed Converter

The proposed converter includes two series-capacitor converters, the a-part is upper, and the b-part is under, as shown in Fig. 3. As shown in Fig. 4(a), the gate signals of a-part and b-part are 90º phase-shifted to achieve the interleaving effect. For simplicity, only the fundamental waveforms of the *a*-part are shown in Fig. 4; those of the *b*-part are similar with 90º phase-shifted. The gate signals of S_1 and S_2 have the same duty ratio and 180º phase-shifted. The detailed characteristics of the proposed converter are summarized in Table. II.

A. Voltage Gain

From the inductor's applied voltage waveform, as shown in Fig. 4(b), by using the flux (volt-sec) balance condition on inductors L_{1a} and L_{2a}, the capacitor's voltage and the output voltage of *a*-part can be obtained as follows. And the same analysis can be applied to the *b*-part.

$$V_{C1a} = V_{C1b} = \frac{V_{in}}{1-D}$$
$$V_a = V_b = \frac{2V_{in}}{1-D} \quad (1)$$

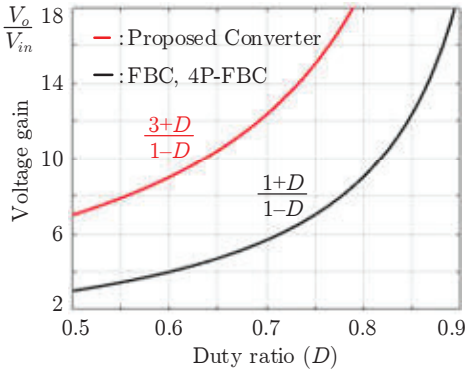


Fig. 5. Voltage gain of the proposed converter.

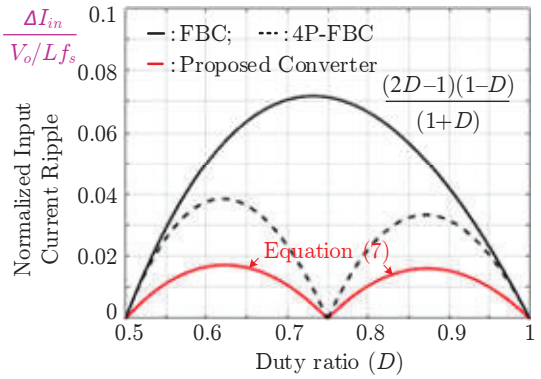


Fig. 6. Normalized input current ripple.

TABLE I
CHARACTERISTIC OF THE PROPOSED CONVERTER

Duty ratio (D)		$D \geq 0.5$
Voltage gain (V_o/V_{in})		$\frac{3+D}{1-D}$
Inductor current balancing		Yes
Voltage stress	S_1, S_2, D_2	$\frac{V_o}{3+D}$
	D_1	$\frac{2V_o}{3+D}$
Current stress	S_1, D_1, D_2	$\frac{I_{in}}{3+D}$
	S_2	$\frac{2I_{in}}{3+D}$
Capacitor voltage	C_1	$\frac{V_o}{3+D}$
	$C_{a\text{-}b}$	$\frac{2V_o}{3+D}$
Inductor current	$I_{L1\text{-}2}$	$\frac{I_{in}}{3+D}$
Input current ripple		Equation (7)

From (1), the total output voltage (V_o) can be determined.

$$V_o = V_a + V_b - V_{in} = V_{in}\frac{3+D}{1-D} \tag{2}$$

From (2), compared with the voltage gain of the traditional FBC and the 4P-FBC (i.e., $\frac{V_o}{V_{in}} = \frac{1+D}{1-D}$), the proposed converter achieves more than double the voltage gain [see Fig. 5].

B. Inductor Current Balancing

From the capacitor current waveform, as shown in Fig. 4(a), by using the charge (amp-sec) balance condition on capacitor C_{1a}, the charging and discharging areas must be the same (i.e., $A_1 = A_2$). As shown, these areas have the same time intervals (i.e., $(1\text{-}D)T_s$); therefore, the inductor currents are equal.

$$I_{L1a} = I_{L2a};\ I_{L1b} = I_{L2b} \tag{3}$$

Based on the device's current waveform, as shown in Fig. 4(c), and using the *KCL* (Kirchhoff's current law) to node A shown in Fig. 3, due to $I_{Ca} = 0$, the following can be achieved

$$\begin{aligned} I_{D2a} &= (1-D)I_{L2a} = I_o \\ I_{L2a} &= I_o/(1-D) \end{aligned} \tag{4}$$

The same procedure can be applied to node B of the b-part, together with (3) and (4), the natural inductor currents have a relationship, and thus, they are naturally balanced.

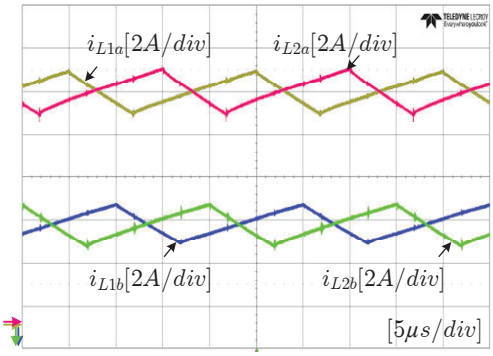
$$I_{L1a} = I_{L2a} = I_{L1b} = I_{L2b} = \frac{I_o}{1-D} \tag{5}$$

C. Input Current Ripple

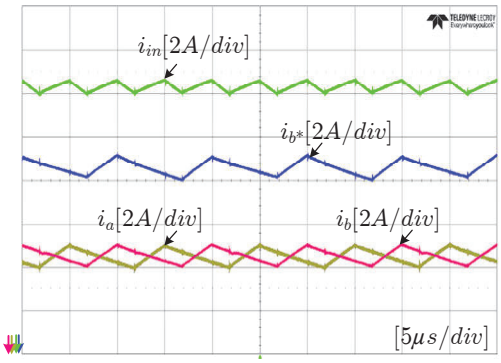
The current ripples can be calculated from the inductor current waveforms, as shown in Fig. 4(b).

TABLE II
CIRCUIT PARAMETERS

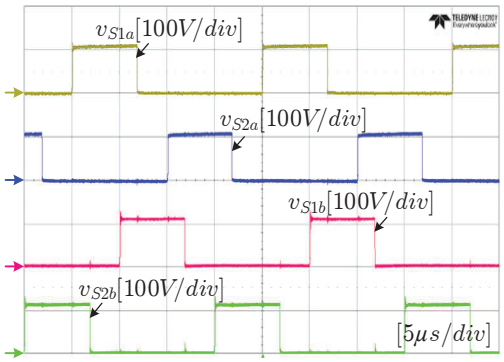
Symbol	Value	Symbol	Value
V_{in}	25~60 V	C_{1a}, C_{1b}	20 µF
V_o	400 V	C_a, C_b	200 µF
P_o	1.6 kW	Switch	IXFH46N65X2
f_{sw}	50 kHz	Diode	RHRG3060
Inductors	240 µH	R_L	100 Ω



(a) Inductor currents.



(b) Input current (i_{in}).



(c) Switches voltage waveform

Fig. 7. Experimental current waveforms (V_{in}= 38 V, V_o= 400 V, D= 0.65).

$$\Delta I_L = \frac{V_{in}}{Lf_s} D;$$
$$\Delta I_a = \Delta I_b = \Delta I_{b*} = \frac{V_o}{2Lf_s}(1-D)(2D-1) \quad (6)$$

Due to the waveforms of i_a and i_{b*} being 90° phase-shifted, as shown in Fig. 4(a), the input current ripple (ΔI_{in}) can be obtained as follows.

$$\Delta I_{in} = \begin{cases} \dfrac{V_o(D-0.5)(3-4D)}{Lf_s(3+D)}, & D < 0.75 \\ \dfrac{V_o(1-D)(4D-3)}{Lf_s(3+D)}, & D \geq 0.75 \end{cases} \quad (7)$$

The input current ripple is minimized and is a four-times switching frequency waveform, as shown in Fig. 4(a). Compared with the FBC and 4P-FBC converters, the proposed converter's input current ripple is significantly reduced. Moreover, it can achieve zero-current ripple at high gains, such as $D = 0.5$ and 0.75, as shown in (7) and Fig. 6.

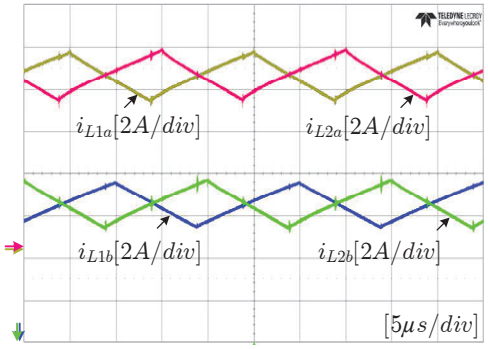
III. Experimental Results

A 1.6 kW prototype is fabricated with the parameters shown in Table II. Figs. 7-9 show the experimental results with different duty ratio (D). The waveforms when D=0.65 are demonstrated in Fig. 7 (V_{in}= 38 V, V_o= 400 V, and D= 0.65). Four inductor currents are shown in Fig. 7(a), which are naturally balanced. The current waveforms (i_{in}, i_a, i_b, and i_{b*}) are shown in Fig. 7(b). Due to the interleaving effect, the input current ripple is significantly reduced. Moreover, it is a four-times switching frequency waveform. The switch voltage stresses are equal and evenly distributed, as shown in Fig. 7(c). The voltage stresses are similar to the capacitor voltages (i.e., $V_{C1a} = V_{C1b} = 38\frac{1}{1-0.65} \approx 109\,V$), and hence are less than the output voltages (i.e., $V_a = V_b = 38\frac{2}{1-0.65} \approx 219\,V$; $V_o = 400\,V$).

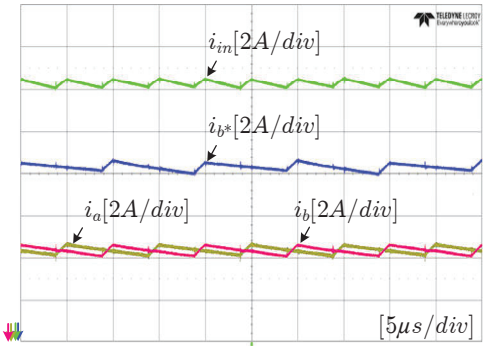
Fig. 8 shows the experimental waveforms when D = 0.55 (V_{in}= 50 V, V_o= 400 V, and D= 0.55). Four inductor currents are well-balanced. And the input current ripple is a four-time switching frequency waveform, significantly reducing compared to the individual inductor current. Furthermore, as expected, the switch voltage stresses are the same and lower than the output voltage (i.e., $V_{S1-4} = V_{C1} = 51\frac{1}{1-0.55} \approx 113\,V$, V_o = 400 V).

The waveforms when D = 0.75 are shown in Figs. 9 and 10 (V_{in}= 27 V, V_o= 400 V, and D= 0.75). As shown, the inductor current balancing is guaranteed, and the input current ripple (Δi_{in}) achieves zero current ripple as anticipated.

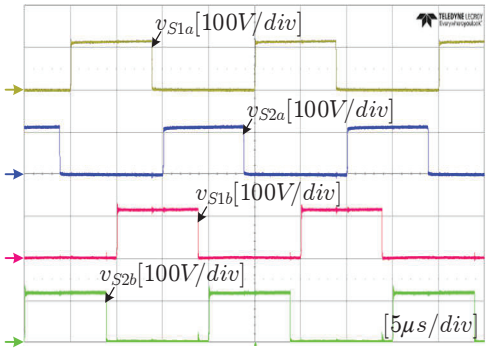
The measurement efficiency versus output power is shown in Fig. 11. The peak value is 95.8% at around 1.2 kW (≈ 75% full power). And a photo of the 1.6 kW prototype is shown in Fig. 12.



(a) Inductor currents.



(b) Input current (i_{in}).



(c) Switches voltage waveform

Fig. 8. Experimental current waveforms (V_{in}= 50 V, V_o= 400 V, D= 0.55, R_L = 100 Ω).

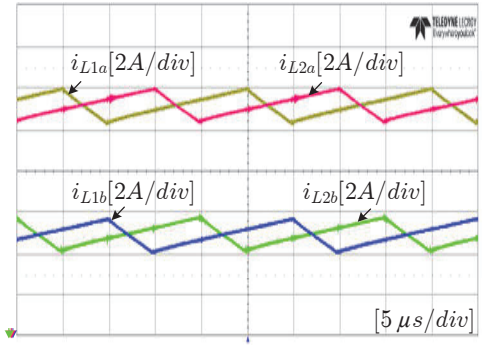


Fig. 9. Inductor current waveforms (V_{in}= 27 V, V_o= 400 V, D= 0.75).

IV. Conclusions

This paper proposes a floating double series-capacitor boost (FSCB) converter, which has the following advantages:

1) The converter achieves high voltage gain (i.e., $\frac{3+D}{1-D}$). The voltage gain is more than double those of FBC and 4P-FBC (i.e., $\frac{1+D}{1-D}$).

2) The switch voltage stresses are lower than the output voltage (i.e., $v_{S1-4} = \frac{V_o}{3+D}$).

3) The input current ripple (Δi_{in}) significantly reduces [see Fig. 6] and is a four-times switching frequency waveform. Moreover, it can obtain zero current ripple at high gain (i.e., D= 0.5 and 0.75).

4) Moreover, the inductor currents are naturally balanced (i.e., $I_{L1a} = I_{L1b} = I_{L2a} = I_{L2b}$).

Consequently, the introduced converter becomes more suitable for new energy sources, such as fuel-cell or PV applications. A 1.6 kW prototype is fabricated to test and validate the performance of the proposed converter.

Acknowledgment

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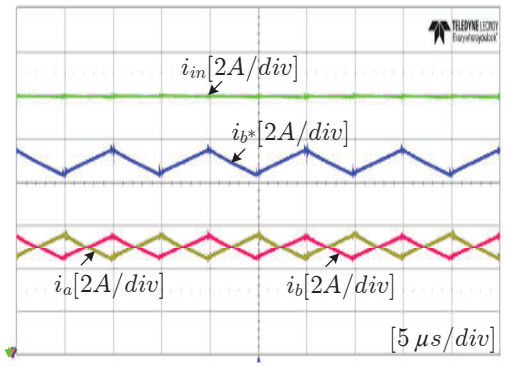

Fig. 10. Input current waveforms (V_{in}= 27 V, V_o= 400 V, D= 0.75).

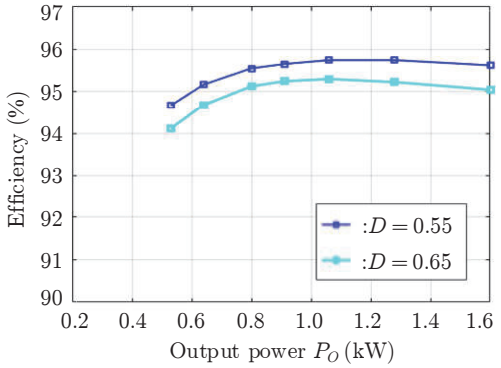

Fig. 11. Efficiency vs. output power.

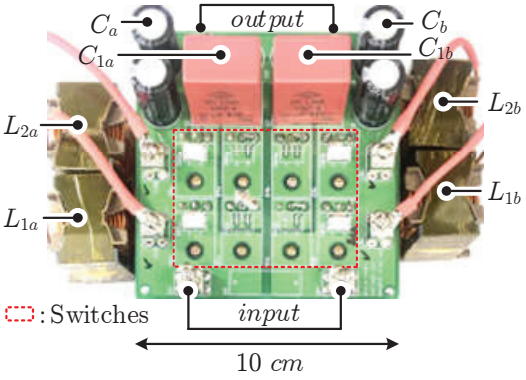

Fig. 12. Photograph of the 1.6-kW prototype.

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