

High Frequency Link Ripple Power Compensation Strategies for 1- ϕ Bidirectional AC-DC Matrix Converters

Subhranil Barman*

Shiladri Chakraborty†

Kishore Chatterjee°

Department of Electrical Engineering, Indian Institute of Technology Bombay, India

Email : subhrahbk@gmail.com*, shiladri@ee.iitb.ac.in†, kishore@iitb.ac.in°

Abstract—Inherent ripple power compensation required during the 1- ϕ operation of direct matrix converters needs to be addressed in order to improve their power density, reliability, cost effectiveness, etc. Existing solutions in literature are scarce; most of the papers relevant to matrix converters are implemented either at the low frequency AC side of the matrix converter or at the DC port side. Two circuits are described in this paper that perform active ripple power compensation of direct matrix converter based high frequency isolated bidirectional AC-DC converters while operating at the high frequency link of the converter. Relevant analysis is given to explain the working principle of the topologies, and simulation results for a 3.45 kW electric vehicle charger, with a 230 V (RMS) AC grid input, feeding a 400 V battery are presented to illustrate the findings.

Index Terms—active power decoupling, high frequency power converters, matrix converters, on-board battery chargers.

I. INTRODUCTION

Direct matrix converter (DMC)-based isolated converters [1] are a promising single-stage candidate topology for high-frequency-isolated, bidirectional AC-DC applications like electric vehicle (EV) chargers, uninterrupted power supplies (UPS), energy storage systems, solid-state transformers etc. Compared to classical two-stage topologies [2], they do not have bulky filter components like boost power factor correction (PFC) inductors and intermediate DC link capacitors, which leads to improved power-density. The power-density advantage is particularly more pronounced for three-phase (3- ϕ) DMCs, since 3- ϕ AC to DC conversion entails minimal low-frequency energy storage. In contrast, operation of single-phase (1- ϕ) DMCs (Fig. 1a) poses power-density challenges that stem from the need for double-line-frequency (DLF) energy storage, inherent in all 1- ϕ AC-DC systems [3].

A commonly adopted approach to address the DLF energy requirement in 1- ϕ AC-DC converters is to place capacitors at the converter's DC port (Fig. 1b). Due to the limited voltage ripple allowed at the DC port in most applications, this approach necessitates high capacitance, which is most often realized using electrolytic capacitors owing to their cost and size advantages. However, the relatively low lifetime of electrolytic capacitors introduces reliability concerns in such

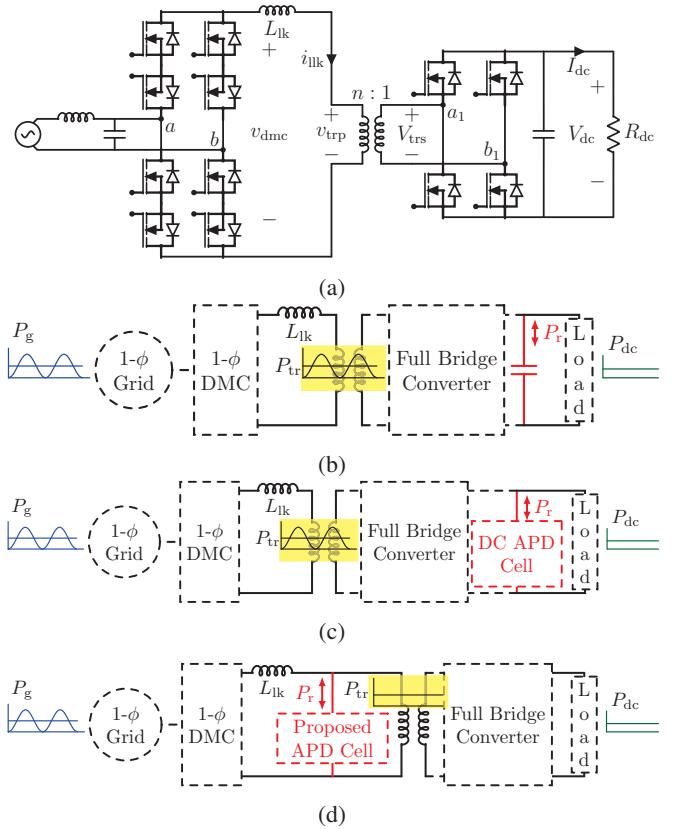


Fig. 1: (a) 1- ϕ DMC; schematics of : (b) DC port energy storage capacitor approach, (c) DC port parallel APD converter approach, (d) and the proposed high-frequency link-based parallel APD circuit approach.

circuits [4]. An alternative solution is to deploy an auxiliary active power decoupling (APD) converter (also referred to as the APD cell in this paper) at the DC port, whose parallel or shunt form [5] is depicted in Fig. 1c. Such a DC APD cell decouples the energy storage capacitor from the DC port, thereby allowing a larger voltage swing across the former, lowering the overall capacitance requirement, and enabling the use of high-lifetime film capacitors. An additional switch-

ing converter is required in this case and metrics such as overall efficiency, component count and costs, etc. need to be considered accordingly. Furthermore, both the passive and DC port APD approaches have the common feature that the transformer and the DC side switches operate with sinusoidal power having a peak value of twice the average DC power. Hence, the current ratings of these components, and the corresponding conduction losses are determined as per the aforementioned sinusoidal power profile.

In majority of reported literature on 1- ϕ AC-DC or DC-AC DMCs, APD implementation is done on the DC side, following the DC port shunt APD principle, or some other circuit modifications. In [6], ripple power compensation is achieved at the DC link by injecting a current synthesized using an extra half-bridge leg and an inductor. Conceptually, this is similar to the shunt APD cell in principle, but absence of a capacitor and the resulting use of an inductor for low frequency energy buffering implies a large inductor value (10 mH) and size. A DC-side interleaved buck converter is proposed in [7], wherein integrated APD action is realized without requiring additional switches. A potential demerit of this approach is that the duty ratio profiles of the DC-side half bridges needed to realize the APD action restricts the overall degrees of freedom of the modulation variables which can result in large RMS currents and/or loss of soft switching operation. Another relevant work includes [8], wherein APD action is realized by using a series L-C branch connected to a center-tapped DC transformer winding. Similar to [6], the inductor size is quite large in this approach (2 mH). An AC-side decoupling method using a third DMC leg and bipolar APD capacitors connected on the AC line side is proposed in [9]. A challenge with this approach is that operation and modulation of the main DMC stage and the DMC leg for APD action need to be considered together, which makes the control scheme somewhat complex. A high-frequency AC (HFAC)-link based decoupling scheme involving a third transformer winding and an auxiliary converter with four-quadrant switches is discussed in [10]. Demerits of this method are that it needs many additional switches and also uses a three-winding (3-w) transformer, which makes the magnetics design challenging. As discussed in [11], the 3-w transformer-based, three-port DC-DC-DC converter of [12] can also be adapted for HFAC link decoupling in a AC-DC application, following the same broad principle as [10]. Compared to [10], the topology of [12] has the advantage of reduced switch count, however its operation for realizing APD action is not extensively discussed in [11]. Moreover, the challenge in magnetics design due to the need for a 3-w transformer still remains.

This paper explores two AC-side APD cell implementations that are specifically realized using auxiliary circuits connected across the HFAC link, without a 3-w transformer. The key objective is to analyze the methods of operating the proposed APD circuits at the HFAC link of the system and

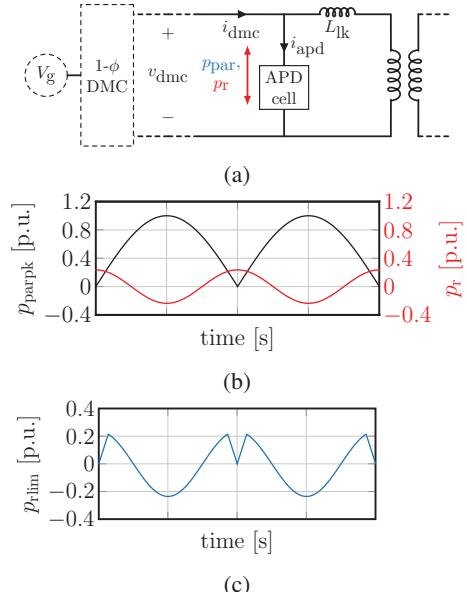


Fig. 2: (a) Placement of the APD cell directly in parallel with the DMC output. (b) Profiles of the peak average power that can be transferred to the parallel APD port ($p_{parallel}$), and requisite average ripple power (p_r), expressed in per-unit (pu). (c) Profile of maximum ripple power that can be compensated (p_{rlim}) for the configuration of Fig. 2a. Due to the sinusoidal variation of the amplitude of v_{dmc} , p_{rlim} is constrained and thus the shown placement is not suitable. Instead, the series inductor L_{lk} is proposed to be placed between the DMC output and the high frequency terminals of the APD cell.

identify optimal design solutions. The rest of the paper is organized as follows. In section II, a preliminary analysis of the relevant aspects for achieving APD action at the HFAC link of a DMC-based AC-DC converter is presented, followed by a discussion on the operating principles of two different topological embodiments. Loss-volume multi-objective design optimization results are presented in section III. Finally, simulation results are presented in section IV to illustrate the operation of the proposed topologies.

II. HIGH-FREQUENCY-LINK PARALLEL APD CIRCUITS

A. Preliminary Analysis

For a 1- ϕ system where the RMS values of grid voltage and grid current, the frequency, and the power factor angle are V_g , I_g , f_g ($\omega_g = 2\pi f_g$, $T_g = 1/f_g$), and θ_g respectively, the instantaneous value of grid power is given by $p_g = p_o - p_r$. Here p_o and p_r denote the instantaneous values of load and ripple power respectively, and can be shown as

$$p_o = V_g I_g \cos(\theta_g), \quad p_r = V_g I_g \cos(2\omega_g t - \theta_g). \quad (1)$$

For compensating the ripple power at the HFAC link of the converter, an auxiliary APD cell is connected across the HFAC link. An initial conceptual placement is depicted in

Fig. 2a, where the APD cell is placed in parallel with the HF output of the DMC. The average power transfer possible through the parallel port, p_{par} , is determined by the magnitude of the DMC output voltage v_{dmc} and the switching period average value of i_{apd} , the current entering the parallel APD port. Due to the HF switching action of the DMC, v_{dmc} consists of positive and negative pulses with a sinusoidally varying amplitude given by $|V_g \sin(\omega_g t)|$.

$$v_{\text{dmc}}(\text{amp}) = |V_g \sin(\omega_g t)|. \quad (2)$$

Since the maximum value of p_{par} is given by $p_{\text{parpk}} = v_{\text{dmc}}(\text{amp}) \times |i_{\text{apd}}|(\text{peak})$ and $v_{\text{dmc}}(\text{amp})$ varies sinusoidally, p_{parpk} also has a rectified sine wave profile, as depicted in Fig. 2b. The average ripple power transfer that can be transferred is given by

$$p_{\text{rlim}} = \min\{p_r, p_{\text{parpk}}\}. \quad (3)$$

It can be observed in Fig. 2c that there is little to no ripple power transfer near the regions of zero crossing of the grid voltage, where $p_{\text{par}} \simeq 0$ (as $v_{\text{dmc}}(\text{amp}) \simeq 0$). Noting that maximum ripple power compensation is needed near the grid voltage zero crossings, it is evident that the APD cell placement of Fig. 2a cannot supply the requisite ripple power. In order to circumvent this issue, the amplitude of the APD cell terminal voltage must be non-zero when $p_r \neq 0$. This can be ensured by connecting the APD cell terminals to the transformer terminals instead of the HF terminals of the DMC and then placing the series inductor L_{lk} at the HF side of the DMC, as shown in Fig. 1d.¹. Since the pulsating transformer terminal voltage v_{trp} has a steady amplitude (determined by the DC-side voltage and the transformer turns-ratio), as opposed to the sinusoidally varying amplitude of v_{dmc} , the aforementioned power transfer constraint is avoided. Working principle of two different embodiments of the parallel APD cell is described next, wherein both the circuits are appropriately placed such that L_{lk} comes in between the high frequency terminals of the DMC and the APD circuits respectively.

B. Full Bridge APD Circuit with Auxiliary Capacitor

1) *Description of the Topology:* This circuit (shown in Fig. 3a) consists of an auxiliary APD capacitor $C_{1\text{fb}}$ that is connected across the dc-link of a full bridge converter, which is then interfaced to the transformer terminals via an intermediate inductor $L_{1\text{fb}}$. The APD capacitor voltage $v_{C_{\text{apd}}}$ has a double grid frequency component in its profile, which is transformed by the full bridge converter to a HF voltage v_{fb} pulsating at f_s . Equivalent circuit of the complete converter including the HF voltage sources synthesized by the DMC and the DC-side full-bridge is shown in Fig. 3b.

¹Note that in this case, the series inductor L_{lk} would not denote the leakage inductance of the transformer. Rather it would be realized using a separate external inductor.

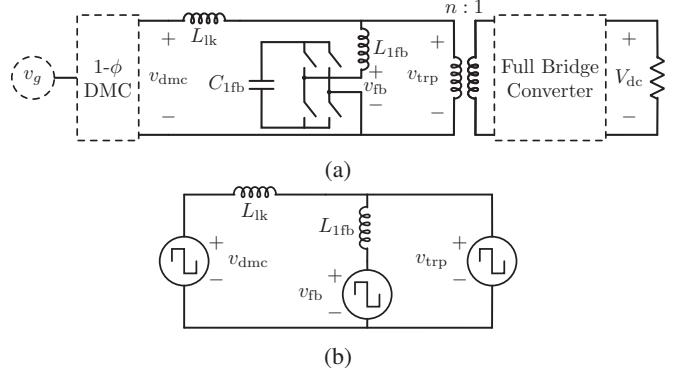


Fig. 3: (a) Proposed APD cell based on full bridge converter, and (b) corresponding equivalent circuit.

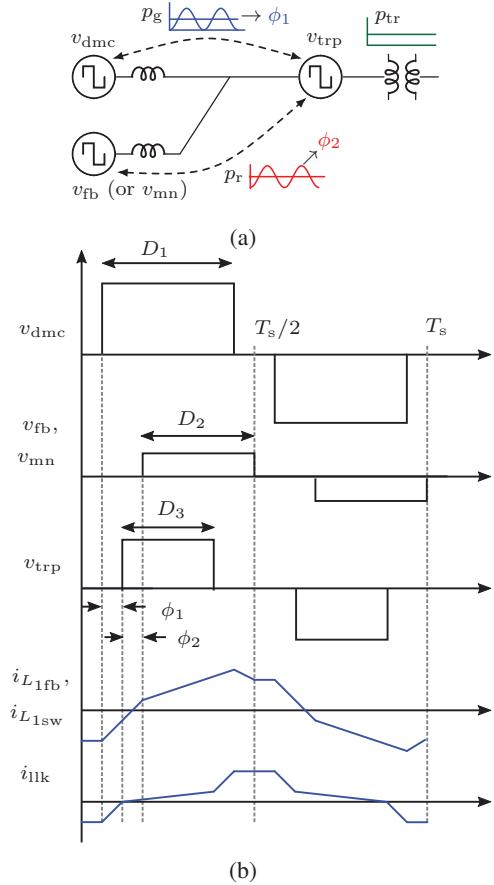


Fig. 4: (a) Block diagram of the control scheme (for both the proposed APD circuits), realized by using duty ratios D_1, D_2 and D_3 of the high frequency voltages $v_{\text{dmc}}, v_{\text{fb}}$ and v_{trp} respectively, and the phase shifts ϕ_1 and ϕ_2 , as control variables. (b) Representative HF waveforms for $p_g > 0$ and $p_r < 0$; the inductor currents are shaped as per the instantaneous magnitudes of $v_{\text{dmc}}, v_{\text{fb}}, v_{\text{mn}}$ and v_{trp} .

it resembles a triple active bridge (TAB) converter, direct connection of the DC-side full-bridge output to the HFAC

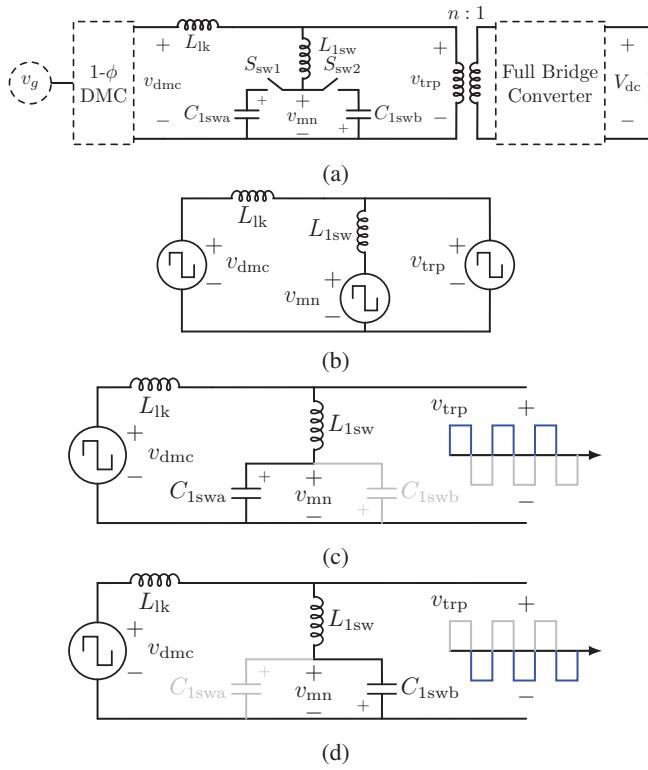


Fig. 5: (a) Proposed APD cell based on oppositely polarized switched capacitors; (b) equivalent circuit; APD circuit configuration during (c) positive cycle of v_{trp} , and (d) negative cycle of v_{trp} .

link² without an intermediate series inductor ensures that the circuit operates functionally as two decoupled dual active bridge (DAB) converters [13]. Such hardware decoupling of the two power-flows significantly simplifies closed-loop implementation of the control scheme.

2) *Control Strategy:* Fig. 4 shows key waveforms explaining the control strategy including the high frequency switching cycle waveforms of the voltages v_{dmc} , v_{fb} , v_{mn} and v_{trp} , and currents of the inductors L_{lk} and L_{1fb} . By controlling the phase shift ϕ_2 between the voltages v_{1fb} and v_{trp} , the requisite ripple power can be suitably absorbed or released from C_{1fb} . Similarly, phase shift ϕ_1 between the voltages v_{dmc} and v_{trp} is used to independently control the DMC operation. Apart from ϕ_1 and ϕ_2 , the duty-ratios D_1 , D_2 and D_3 of the high frequency voltages v_{dmc} , v_{1fb} and v_{trp} respectively are additional control variables, which may be utilized to optimize converter operation. Here, each duty-ratio denotes the ratio of the pulse width of each high frequency voltage to the switching period, realized through phase-shift of the corresponding switch node voltages. In summary, the five control variables are utilized to achieve the following:

²This implies that the transformer must be designed with low leakage inductance.

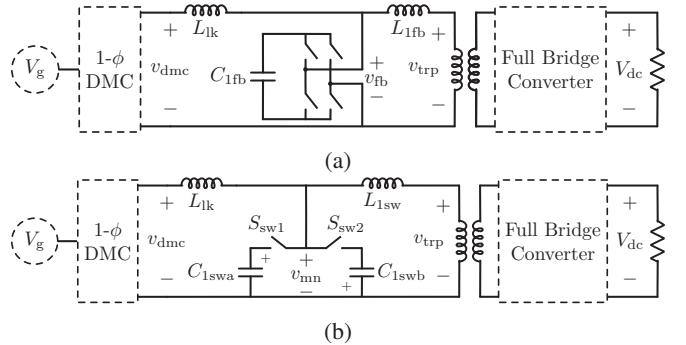


Fig. 6: Alternative implementation of the proposed APD circuits for (a) full bridge converter, and (b) switched capacitor.

- a) draw the requisite power p_g with power factor correction at the AC-side of the converter by changing ϕ_1 ,
- b) fulfill the transfer of requisite ripple power p_r to or from the APD converter by changing ϕ_2 , and
- c) operate the converter such that its overall power loss is minimized by changing the duty-ratios D_1 , D_2 and D_3 .

C. Dual Anti-phase Switched Capacitor APD Circuit

1) *Description of the Topology:* The topology discussed in the preceding subsection is a device-heavy solution due to the requirement of four additional switches for realizing the APD converter. An alternative embodiment having lower switch count is shown in Fig. 5a, where two oppositely polarized capacitors C_{1swa} and C_{1swb} , connected to an interfacing inductor L_{1sw} via two switches, are used for realizing APD action. When v_{trp} is positive, capacitor C_{1swa} is connected via S_{sw1} to L_{1sw} , and when v_{trp} is negative, C_{1swb} is connected via S_{sw2} to L_{1sw} . In this way, the two capacitors are utilized in complimentary fashion for compensating the ripple power. The inductor L_{1sw} interfaces the two high frequency voltages v_{trp} and v_{mn} , and the circuit operation to achieve ripple power compensation is achieved using DAB principle, as before. Even though the two capacitors C_{1swa} and C_{1swb} are oppositely polarized, their voltage profiles are similar in nature (in magnitude) to each other, as well as to that of C_{1fb} in the previously discussed topology. This implies that C_{1swa} and C_{1swb} have the same value, which is equal to $C_{1fb}/2$, and correspondingly they handle only half of the total requisite ripple power, as explained in Section III. While the number of switches is reduced to two, two APD capacitors are required in this topology.

2) *Control Strategy:* The control strategy is similar to that of the full bridge APD circuit, as (Fig. 4), wherein v_{mn} will replace v_{fb} , and v_{mn} is a square wave, and thus the duty-ratio D_2 is not available as an additional control variable.

D. Modified Architecture (Type 2) for Proposed Circuits

As discussed before, the fundamental condition for HFAC link ripple power compensation is that a series inductor must

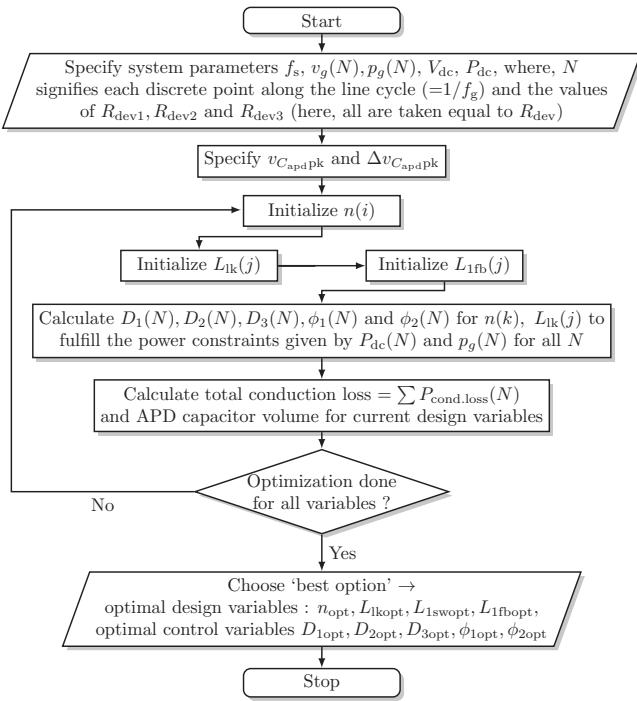


Fig. 7: Flowchart for the design optimization algorithm considering the system parameters mentioned in Table I.

TABLE I: Nominal operating conditions and specifications.

Nominal grid parameters	$V_g = 230 \text{ V (RMS)}$, $f_g = 50 \text{ Hz}$
Nominal DC side parameters	$V_{dc} = 400 \text{ V}$, $P_{dc} = 3.45 \text{ kW}$
Switching frequency	$f_s = 100 \text{ kHz}$

be placed between the link and the DMC output voltage. Fulfilling this criterion, both the previous embodiments can also be operated in an alternative architecture, designated as type 2 implementation. The complete circuits for this form are depicted in Fig. 6, from which it can be noticed that the key difference with the earlier circuits is that the APD terminal HF voltage (v_{fb} or v_{mn}) determines the HFAC link voltage and the inductor in series with the APD cell is relocated to be in series with the transformer terminals. Accordingly, the control strategy needs to be modified, wherein

- a) input ac power ($p_o + p_r$) is drawn from the AC-side by changing the phase-shift (say ψ_1) between the APD terminal HF voltage and the DMC HF voltage v_{dmc} and
- b) constant average power (p_o) is delivered to the DC-side by changing the phase-shift (say ψ_2) between the APD terminal HF voltage and the voltage v_{fb} .

III. DESIGN CONSIDERATIONS

Design trade-offs involving overall converter conduction loss and APD capacitor volume for both topologies are analyzed in this section. For a capacitor used as the energy storage element in an APD circuit, if the capacitance and

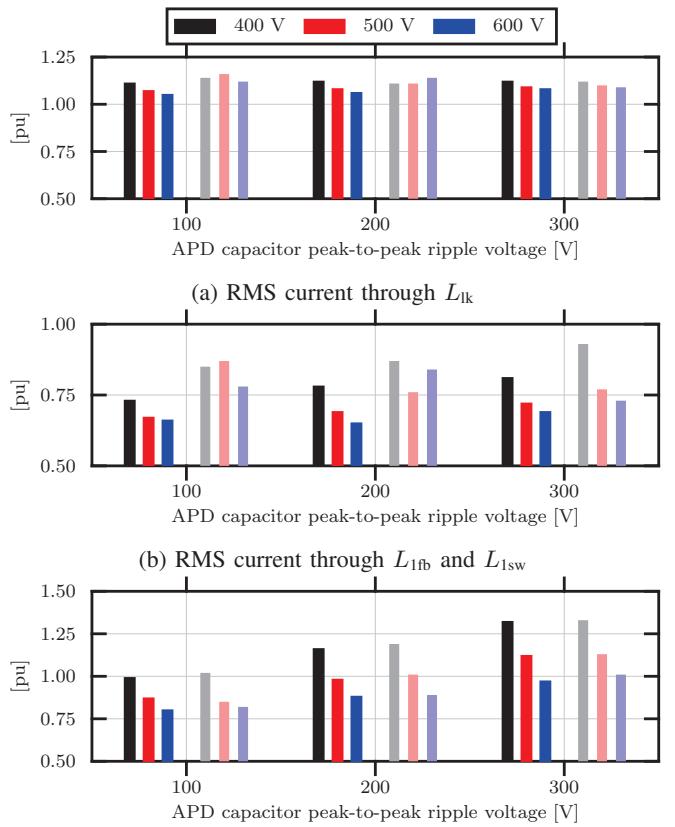


Fig. 8: RMS currents (over a line cycle) for the full bridge APD circuit (dark shade) and switched capacitor APD circuit (light shade) for peak capacitor voltages of 400 V, 500 V, and 600 V. All values, obtained by considering optimal parameters, are normalized to the RMS value of current i_{lik} when there is no parallel HF link APD.

the instantaneous voltage are denoted by C_{apd} and $v_{C_{apd}}$ respectively, then $v_{C_{apd}}$ can be expressed as

$$v_{C_{apd}} C_{apd} \frac{d}{dt} v_{C_{apd}} = p_r. \quad (4)$$

$$\implies v_{C_{apd}} = \pm \sqrt{\frac{V_g I_g}{\omega_g C_{apd}}} \sqrt{K - \cos(2\omega_g t - \theta_g)}, \quad (5)$$

where K is the constant of integration. Accordingly, the APD capacitors for both the full bridge converter based and the switched capacitor based APD circuits are selected based on the peak ripple power requirement for the considered system, that is $|p_r|_{(\max)} = 3.45 \text{ kW}$. The peak value of the APD capacitor voltage(s) and the peak to peak ripple, that are determined by (5), are selected through optimization, since they would ultimately determine the overall capacitor size. Therefore, for various combinations of peak capacitor voltage and peak-to-peak voltage ripple (and the equivalent APD capacitor values), optimal values of transformer turns-ratio n , inductor values L_{lik} , L_{1fb} and L_{1sw} , and the corresponding

Peak to peak voltage ripple voltage values : ‘o’: 75 V, ‘ \triangle ’: 100 V, ‘ \times ’: 150 V, ‘ \diamond ’: 200 V, ‘+’: 250 V, and ‘*’: 300 V

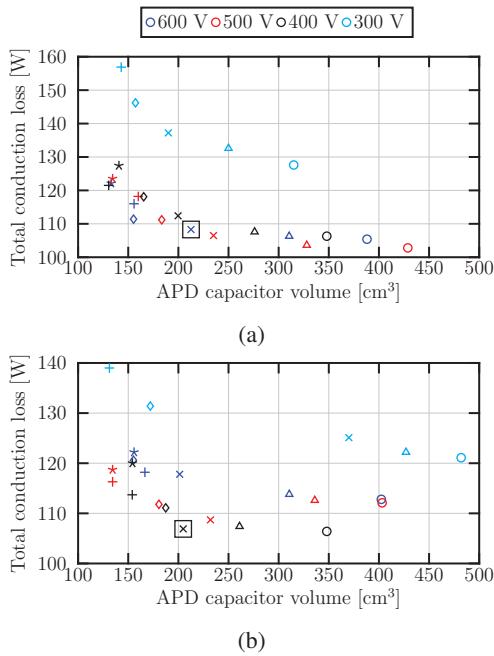


Fig. 9: Scatter plots of total conduction losses in the converter versus requisite APD capacitor volume obtained by considering various combinations of peak voltage and peak-to-peak voltage ripple for the APD capacitor when operated with optimized parameters - (a) for the full bridge converter based APD circuit, and (b) for the switched capacitor based APD circuit. The value of the switch resistance R_{dsON} for all devices is 50 m Ω . Optimal choices of the APD capacitors for the two cases are marked by the black square.

TABLE II: Specifications for the two proposed APD circuits, where V_{cappk} is the peak voltage, and ΔV_{cappk} is the peak-to-peak ripple voltage of the APD capacitors. The parameters without any APD are also shown.

APD type	primary/ secondary turns ratio n	L_{lk} [μ H]	L_{lsw} [μ H]	C_{lsw} ($=C_{lswb}$) [μ F]	L_{lfb} [μ H]	C_{lfb} [μ F]
Switched capacitor ($V_{cappk} = 400$ V $\Delta V_{cappk} = 150$ V)	0.8	13.2	15.1	113	-	-
Full bridge ($V_{cappk} = 600$ V $\Delta V_{cappk} = 150$ V)	0.8	22.6	-	-	18.2	139
No APD	0.8	9.4	-	-	-	-

duty ratios D_1, D_2 and D_3 , and phase shifts ϕ_1 and ϕ_2 , are derived. A flowchart of the overall optimization procedure using the ‘fmincon’ tool of Matlab is shown in Fig. 7.

Fig. 8 shows the variation of the normalized RMS currents flowing through L_{lk}, L_{lfb} and L_{lsw} , and the transformer primary winding for the full bridge APD circuit. Particularly, the currents through L_{lk} and the transformer primary winding

Peak to peak voltage ripple voltage values : ‘o’: 75 V, ‘ \triangle ’: 100 V, ‘ \times ’: 150 V, ‘ \diamond ’: 200 V

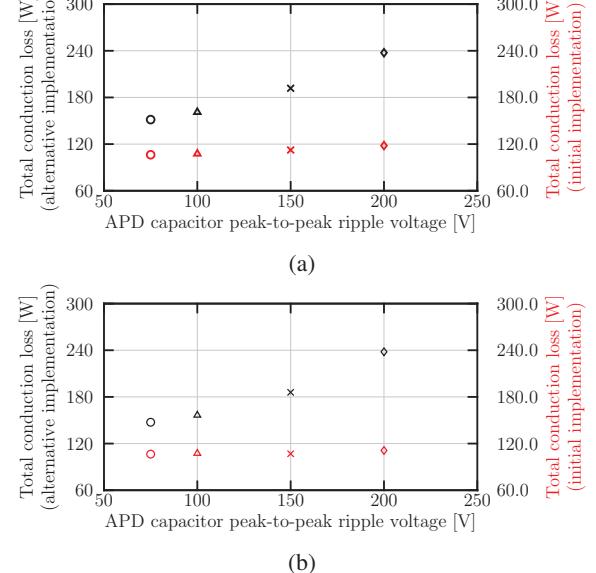


Fig. 10: Plots of total conduction losses, obtained for a peak APD capacitor voltage of 400 V and different peak-to-peak ripple voltages obtained by considering optimal parameters, showing a comparison between the alternative and initially proposed implementations of (a) full bridge APD circuit, and (b) switched capacitor APD circuit. The significantly higher losses incurred in type 2 implementation indicate a relative demerit of this approach.

are generally observed to increase as the ripple voltage across the APD capacitor increases for any given peak voltage.

By obtaining the parameters n, L_{lk}, L_{lfb} or L_{lsw} , and the corresponding variables D_1, D_2, D_3, ϕ_1 and ϕ_2 through optimization, the total conduction loss is calculated for both the proposed circuits, for several combinations of peak voltage and peak-to-peak voltage ripple of the APD capacitor, which is then plotted against the corresponding total requisite APD capacitor volume, as given in Fig. 9. Here, the capacitor volume required for each APD capacitance value is calculated by considering several combinations of numerous off-the-shelf “smaller” capacitors (each having lower capacitance value but similar voltage rating as the corresponding APD capacitor), and then choosing the combination that results in the lowest overall capacitor volume.

The key inference from Fig. 9 is that across most design points, the Pareto-optimal solutions (solutions which reduce both the conduction loss as well as the APD capacitor volume) for the full bridge APD circuit are obtained at a peak APD capacitor voltage of 600 V, and are generally improved by increasing the peak voltage. On the other hand, for the switched capacitor APD circuit, the trend improves by reducing the peak APD capacitor voltage, and is obtained at 400 V, although the trend reverses below 400 V. For both

TABLE III: Comparison table of the proposed APD circuit capacitors selected through optimization, with passive DC capacitors, considering off-the-shelf capacitors; here C1 : C4AULBU5100M18K (10 μ F, 500V), C2 : C4AQLBW5500A3JK (50 μ F, 500V), C3 : BLH306K801B104 (30 μ F 800V), C4 : B32778Z8506K000 (50 μ F, 800 V), C5 : B32718H5177K000 (170 μ F, 500V), C6 : 382LX152M500B102VS (1.5 mF, 500 V).

Circuit or capacitor configuration	Required capacitors	Cap. volume Volume C_{dc1}	Cap. volume Volume C_{dc2}	Additional switches	Additional magnetics	Transformer peak power
Proposed full bridge APD circuit (600 V peak capacitor voltage)	C1+C3+C4×2	0.16	1.03	4	✓	P_{dc}
Proposed switched capacitor based APD circuit (400 V peak capacitor voltage)	C1×2+C2	0.15	0.99	2	✓	P_{dc}
Passive DC Capacitor (Film) → C_{dc1}	C5×9	1	6.44	—	—	$2P_{dc}$
Passive DC Capacitor (Electrolytic) → C_{dc2}	C6×1	0.155	1	—	—	$2P_{dc}$

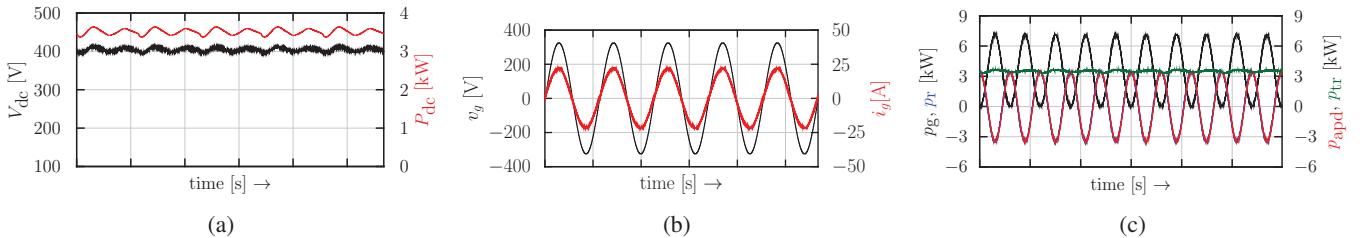


Fig. 11: Simulation waveforms (low-frequency) for the switched capacitor based APD circuit : (a) DC-side voltage and power; (b) AC-side voltage v_g and current i_g ; and (c) power curves; (c) indicates that the peak transformer power for the proposed APD circuit is reduced to the value of the average power.

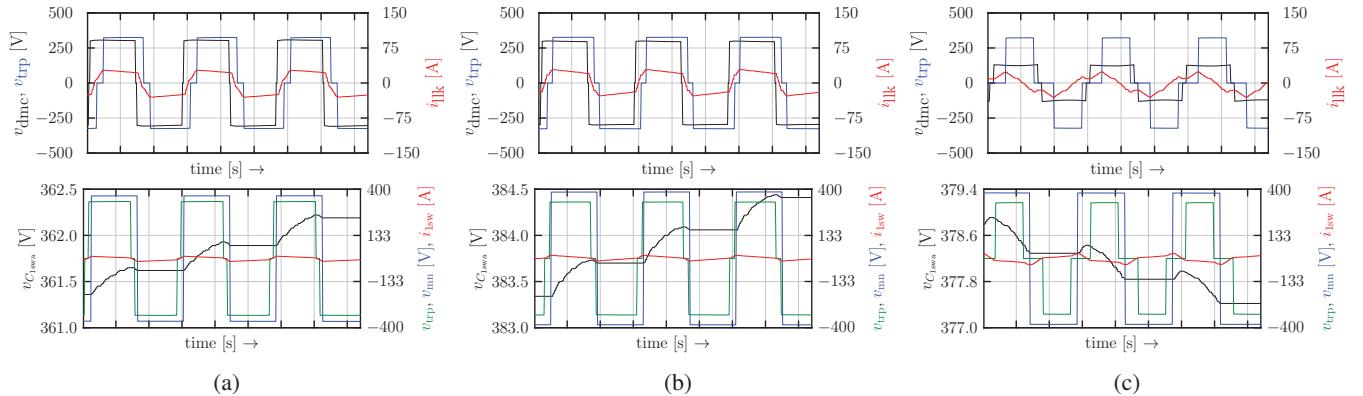


Fig. 12: Simulation waveforms (high-frequency) for the switched capacitor based APD circuit including (top) high-frequency variables corresponding to L_{Ik} , and (bottom) APD converter variables when (a) v_g is near its positive peak, (b) v_g is near its negative peak, and (c) v_g assumes a low positive value close to zero.

cases, the best solutions are attained at a peak-to-peak ripple voltage of 150 V. Finally, by observing the conduction loss value and the APD capacitor volume for the ‘best’ solution of the two embodiments, the switched capacitor APD circuit, considering a peak capacitor voltage of 400 V with a peak-to-peak ripple of 150 V, respectively, is chosen as the APD configuration most suitable to the application at hand based on the optimization method considered.

A comparison plot showing the total conduction losses for the alternative and the initial implementations of the proposed APD circuits is also shown in Fig. 10. It is evident from the plots that the conduction loss metrics are significantly higher in case of the alternative implementation for similar output characteristics, indicating that there are no advantages

gained by changing the position of the L_{1fb} and L_{1sw} . Hence, the alternative configurations are not considered for further discussions as the initial implementations have relatively superior characteristics.

A three-winding transformer based configuration was also evaluated in which the proposed APD circuits are connected to a tertiary winding of the transformer instead of the HF link. Optimization results for the design points considered previously showed a reduction of approximately 10-15 W ($\approx 5\text{-}10\%$) in the total conduction loss.

IV. SIMULATED PERFORMANCE AND OBSERVATIONS

Based on the aforementioned discussions in Section III, the results obtained by simulating the switched capacitor

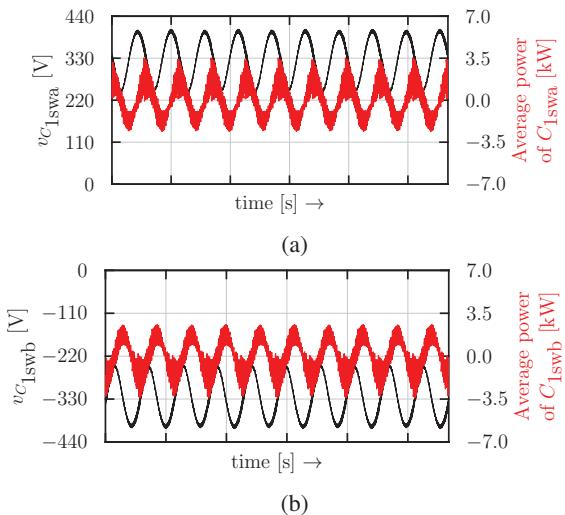


Fig. 13: Simulation waveforms for switched capacitor based APD circuit : power and voltage waveforms for APD capacitor (a) $C_{1\text{swa}}$, and (b) $C_{1\text{swb}}$.

APD circuit in feed forward mode considering the parameters given in Table II are shown in Fig. 11–Fig. 13.

The results show that reasonably steady DC side voltages and currents are obtained. The power waveforms of the switched APD capacitors $C_{1\text{swa}}$ and $C_{1\text{swb}}$ given in Fig. 13a and Fig. 13b respectively, clearly shows that half of the power is handled by $C_{1\text{swa}}$, while $C_{1\text{swb}}$ handles the other half. Table III is shown for a relative comparison between the proposed APD circuits, and a 1400 μF passive DC side capacitor required to restrict the peak-to-peak ripple in the DC bus voltage to 20 V when APD is not performed, based on various metrics, by considering some standard off-the-shelf capacitors. All capacitors are considered to be of film technology for an equivalent comparison. Metrics for an electrolytic capacitor-based passive DC capacitor are also shown. For both the proposed circuits, a low value DC-side capacitor is essential to absorb the high frequency switching ripples of the DC side full bridge converter, and hence the volume of an appropriate capacitor (10 μF , 500 V) is also added to the APD capacitor volume.

The waveform of $V_{1\text{swa}}$ in Fig. 12 clearly shows that $C_{1\text{swa}}$ exchanges power only during the positive pulse of v_{trp} , as is expected, whereas it remains idle for the negative pulse of v_{trp} , during which $C_{1\text{swb}}$ is operated. The switching losses of the system have not been investigated either in simulation or in the aforesaid optimization process. However, the effects of switching behaviour of the DMC, the two embodiments of the APD converters, and the DC side full bridge is a significant aspect to consider that will be strongly focused upon by the authors in their future work.

V. CONCLUSIONS

In this paper, two embodiments of APD topologies suitable to isolated HFAC link matrix converters have been presented. The working principles of the two APD circuits, and the corresponding design strategies employed are described in detail. Simulation results show that proper compensation of the ripple power is achieved with the proposed switched capacitor APD circuit, and a relative comparison among the two embodiments reveals that the switched capacitor based topology is marginally superior to the full bridge APD circuit. As a future scope, the authors would like to investigate the soft switching behavior of all the converters, so as to potentially reduce the overall converter losses and accordingly determine the optimal capacitor specifications and size, and also consider the effects of load variation.

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