Single-Phase 3-Level and 5-Level Boost Inverters without High-Frequency Common-Mode Voltage

Sze Sing Lee[1*], Reza Barzegarkhoo[2], Yam P. Siwakoti[2], Felipe B. Grigoletto[3], and Kyo-Beum Lee[4]

[1]Newcastle University, Singapore
[2]School of Electrical and Data Engineering, University of Technology Sydney, Sydney, Australia
[3]Federal University of Pampa (UNIPAMPA), Alegrete, Brazil
[4]Department of Electrical and Computer Engineering, Ajou University, Suwon, South Korea
[*]Email: SzeSing.Lee@newcastle.ac.uk

***Abstract*- This paper proposes two single-phase boost inverters that are capable of mitigating the high-frequency common-mode voltage (CMV). The conventional two-stage topology that consists of a frontend boost converter and a backend H-bridge inverter is restructured. While retaining the advantages of the conventional topology such as continuous input current and dynamic voltage gain, the proposed 3-level boost inverter achieves constant CMV without requiring any additional components. An extended 5-level boost inverter is also proposed by integrating another capacitor controlled by 4 switches to the 3-level topology. For the same inductor charging duty-cycle and inverter modulation index, the voltage gain of the proposed 5-level boost inverter is double compared to the 3-level counterpart. The operation of the proposed 3-level and 5-level boost inverters is comprehensively analyzed and verified by simulation results.**

***Index Terms*– Boost inverter, common-mode voltage, multilevel inverter, 3-level, 5-level.**

I. Introduction

Power electronic inverters that provide dc-ac power conversion are an essential part of modern power systems for renewable energy applications. For single-phase systems, H-bridge inverter is the simplest topology that has been widely used [1]. Fig. 1 shows the conventional H-bridge inverter with a frontend dc-dc boost converter. Due to the limited voltage gain of the H-bridge inverter, a frontend boost converter is necessary for applications that have insufficient dc source voltage. As the ac neutral is connected to a half-bridge without electrical isolation from the dc source, there is a risk of leakage current due to the high-frequency CMV. To mitigate high-frequency CMV, some structural modifications by the incorporation of a bypass circuit to either the dc or ac side of the H-bridge inverter are attempted [2].

In [3], a power switch is connected in series with the H-bridge to provide more flexibility of using the dc-link capacitor. The capacitor can be switched into parallel with the dc source for charging or disconnected from the dc source for supplying the load. Therefore, the modified H-bridge inverter constitutes a switched-capacitor circuit. By generating the negative voltage level using the pre-charged dc-link capacitor, the negative terminal of dc source can remain connected to the ac neutral which mitigates the high-frequency CMV effectively. Similar concept has been widely explored in recent years. Significant research is focused on integrating more switched-capacitors to extend the number of voltage levels and gain using lowest possible switch count [4], [5]. However, this type of inverters has asymmetric circuit operation for positive and negative half cycles. Due to continuous discharging of switched-capacitors during negative half-cycle, the significant capacitor voltage ripple causes distortion and dc offset in the ac output voltage [6]. In addition, the charging of switched-capacitors by switching them in parallel with the dc source causes current spikes. The input current is discontinuous that is not feasible for some applications such as PV [7].

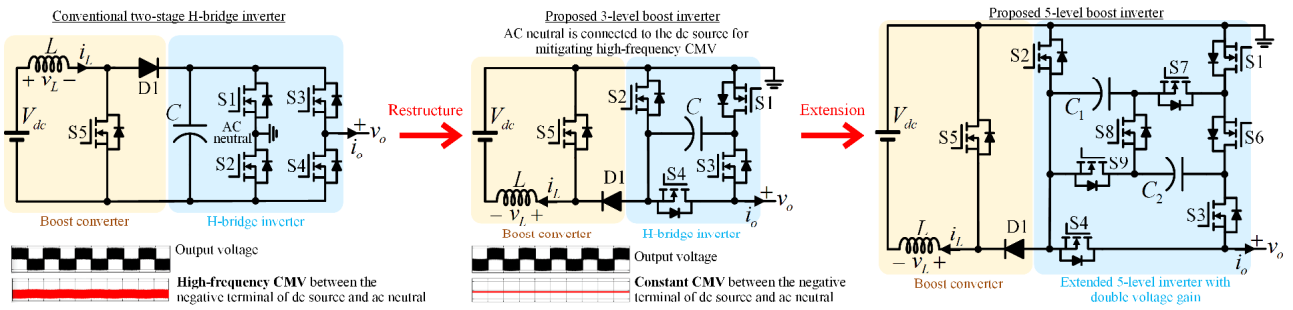
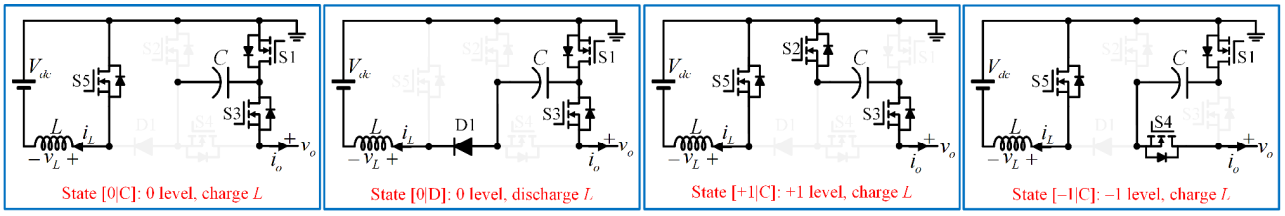
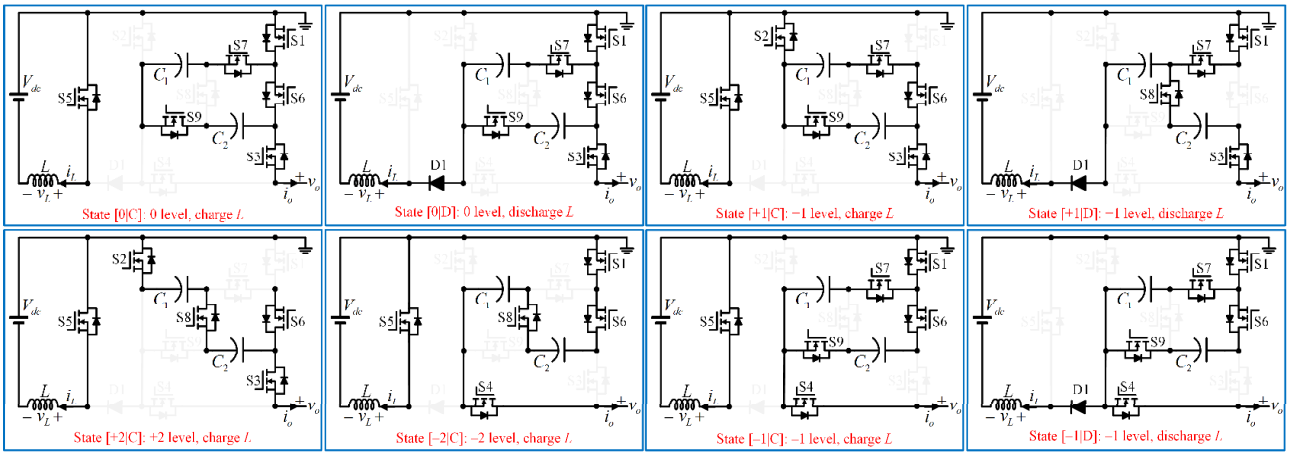


Fig. 1. Derivation of the proposed 3-level and 5-level boost inverters without high-frequency CMV.



(a)



(b)

Fig. 2. Switching states of the proposed boost inverter: (a) 3-level topology, (b) 5-level topology.

This paper aims to resolve the aforementioned drawbacks by establishing novel boost inverters that can achieve continuous input current and dynamic voltage gain with symmetric circuit operation. Following a comprehensive analysis of the conventional two-stage H-bridge inverter, new switching states that couple the operation of the boost converter and H-bridge inverter are deduced. The new switching states enable restructuring of the topology for mitigating high-frequency CMV without requiring any additional components. The novel 3-level boost inverter is further extended to generate 5 voltage levels with enhancement in voltage gain.

TABLE I.
SWITCHING STATES OF THE PROPOSED 3-LEVEL BOOST INVERTER

Switching state	Voltage level	S1 S2 S3 S4 S5 (1 = ON, 0 = OFF)	Inductor *L*
[0|C]	0	10101	charging
[0|D]	0	10100	discharging
[+1|C]	$+V_C$	01101	charging
[–1|C]	$-V_C$	10011	charging

TABLE II.
SWITCHING STATES OF THE PROPOSED 5-LEVEL BOOST INVERTER

Switching state	Voltage level	S1 – S9 (1 = ON, 0 = OFF)	Inductor *L*
[0|C]	0	101011101	charging
[0|D]	0	101001101	discharging
[+1|C]	$+V_C$	011011101	charging
[+1|D]	$+V_C$	101000110	discharging
[–1|C]	$-V_C$	100111101	charging
[–1|D]	$-V_C$	100101101	discharging
[+2|C]	$+2V_C$	011011010	charging
[–2|C]	$-2V_C$	100111010	charging

II. PROPOSED BOOST INVERTER TOPOLOGIES

Fig. 1 shows the derivation of the proposed boost inverters. By restructuring the frontend boost converter and relocating the positive terminal of the frontend boost converter to the ac neutral of the backend H-bridge, an improved 3-level topology is obtained. As the ac neutral is connected directly to the positive terminal of the dc source, CMV between the negative terminal of dc source and ac neutral is $-V_{dc}$. Therefore, the issue of high-frequency CMV in the conventional two-stage H-bridge inverter is mitigated in the proposed 3-level boost inverter without requiring any additional components. By adding 4 power switches, another capacitor is integrated to the 3-level boost inverter for extending the number of voltage levels to 5. Similar to the 3-level topology, each capacitor is charged to V_C by controlling the duty-cycle D of the boost converter. However, the maximum voltage level of the 5-level topology is generated by discharging both capacitors in series which is double ($2V_C$) compared to the 3-level topology (V_C) for the same D. Therefore, the proposed 5-level boost inverter has a benefit of higher voltage gain compared to the 3-level topology, when the same D is considered.

The switching states of the proposed 3-level and 5-level boost inverters are summarized in Table I and II, respectively. Their circuit diagrams are depicted in Fig. 2. Considering the volt-second balance of inductor, the average voltage across each capacitor is

$$V_C = \frac{1}{1-D} V_{dc} \tag{1}$$

where D is the inductor charging duty-cycle. For generating ac voltage, sinusoidal pulse-width modulation (PWM) scheme is used. One triangular carrier and two level-shifted triangular carriers are required for the 3-level and 5-level topology, respectively. The peak of ac voltage at fundamental frequency f_o is a function of modulation index M and maximum voltage level V_{max}:

$$\hat{V}_{o,1} = MV_{\max} = \begin{cases} \dfrac{M}{1-D}V_{dc}, & \text{for 3-level boost inverter} \\ 2\dfrac{M}{1-D}V_{dc}, & \text{for 5-level boost inverter} \end{cases} \quad (2)$$

In the proposed 3-level boost inverter, the constant PWM for controlling the boost converter and sinusoidal PWM for controlling the inverter are generated simultaneously using the same triangular carrier. Therefore, the minimum duty-cycle D_{min} for charging the inductor of 3-level topology is given by the modulation index, i.e., $D_{min} = M$. For 5-level boost inverter, $D_{min} = 2M–1$ because the constant PWM is generated by comparing a constant reference (given by the peak of the sinusoidal reference) with the top triangular carrier. Considering the minimum duty-cycle D_{min} for the frontend boost converter, the voltage gain of both 3-level and 5-level boost inverters can be simplified and written as a function of modulation index:

$$G = \frac{\hat{V}_{o,1}}{V_{dc}} = \frac{M}{1-M}. \quad (3)$$

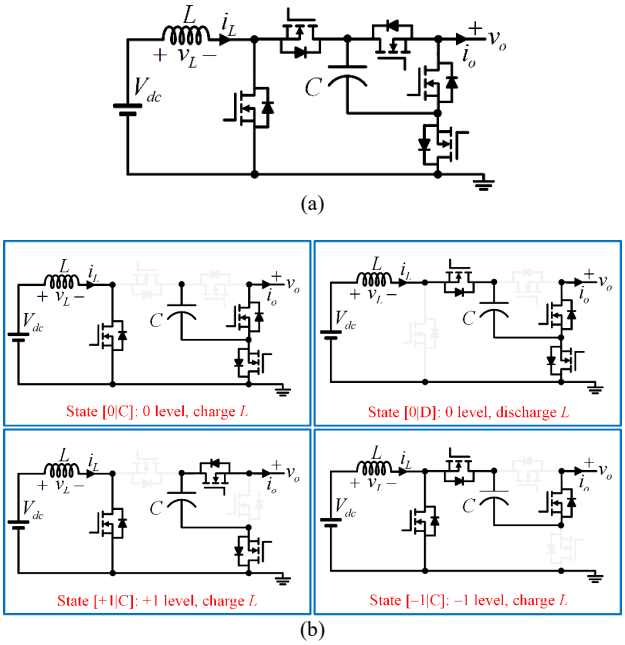


Fig. 3. Existing common-ground 3-level boost inverter presented in [8]–[10]: (a) circuit topology, (b) switching states for achieving continuous input current.

To clarify the contribution of the proposed 3-level boost inverter compared to the latest literature, the common-ground 3-level topology presented in [8]–[10] is considered, as shown Fig. 3. This latest counterpart can achieve the same performance as the proposed topology in the aspect of continuous input current and dynamic voltage boosting. Although it saves one diode compared to the proposed 3-level boost inverter, the number of conducting switches for ac load current during [–1|C] state is more, as shown in Table III. Therefore, reduction of power losses during [–1|C] state is the main advantage of the proposed topology.

TABLE III.
COMPARISON BETWEEN THE PROPOSED 3-LEVEL BOOST INVERTER AND THE LATEST COUNTERPART PRESENTED IN [8]–[10].

Switching state	Number of conducting switches for ac load current	
	Fig. 2(a) (Proposed)	Fig. 3(b)
[0|C]	2	2
[0|D]	2	2
[+1|C]	2	2
[–1|C]	2	3

III. SIMULATION RESULTS

For verification, both 3-level and 5-level boost inverters were simulated in Matlab Simulink for generating 230 V (rms) from a 100-V dc source. According to (3), the required M is approximately 0.77. The required D for the 3-level and 5-level topology is calculated as 0.77 and 0.54, respectively. The remaining simulation parameters are listed as follows: output frequency f_o = 50 Hz, triangular carrier frequency f_s = 10 kHz, inductor L = 3 mH, capacitor $C = C_1 = C_2$ = 1000 µF, apparent power = 1 kVA, and power factor = 0.85.

Simulation results are summarized in Fig. 4. As similar to the conventional two-stage inverter, the input or inductor current is continuous. However, the proposed boost inverters have a significant improvement in mitigating high-frequency CMV. As shown in Fig. 4, the CMV of both topologies is a constant, i.e. –100V without high-frequency component.

By analyzing the inductor current of the 3-level topology in lower timescale, it can be clearly seen that the inductor is charged for 77 µs and discharged for the remaining period in each 10 kHz switching cycle. With D = 0.77, the capacitor voltage is boosted to 434.8 V. Three symmetrical voltage levels, i.e., 434.8 V, 0, and –434.8 V are generated in the ac output of the proposed 3-level topology. The load current is sinusoidal with an amplitude of approximately 5.7 A. Considering the load impedance of 59 Ω, the peak of ac output voltage at fundamental frequency (50 Hz) can be calculated as approximately 336 V.

While generating the same magnitude of ac output voltage, the proposed 5-level topology has 5 symmetric voltage levels between 434.8 V and –434.8 V. In addition to the benefit of lower dv/dt and improvement in the ac voltage quality, the same voltage gain in the 5-level topology is achieved at lower D. The inductor charging and discharging period in each switching cycle is 54 µs and 46 µs, respectively. Therefore, the voltage across capacitors C_1 and C_2 is only 217.4 V which is half compared to the capacitor voltage of the 3-level topology.

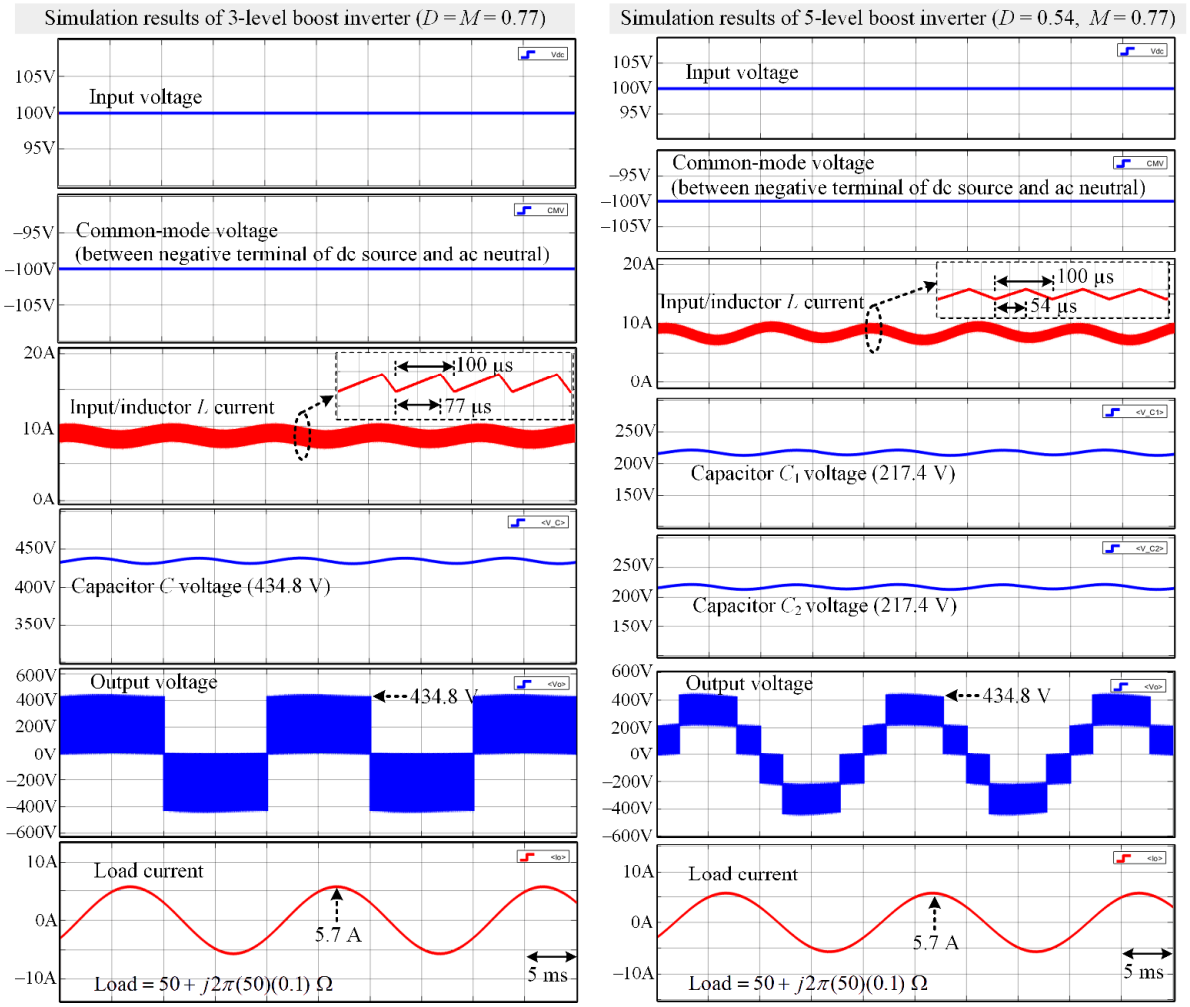


Fig. 4. Simulation results.

IV. Conclusion

Two novel single-phase boost inverters are proposed in this paper. The 3-level topology is an improvement of the conventional two-stage H-bridge inverter by mitigating high-frequency CMV without requiring any additional components. While retaining the good features of the 3-level topology such as continuous input current and dynamic voltage gain, the extended topology increases the number of voltage levels from 3 to 5. In addition, the voltage gain of the extended 5-level topology is double compared to the 3-level counterpart for the same D and M. When the same voltage gain and modulation index M are considered, the proposed 5-level topology can be operated with lower duty-cycle D that reduces the voltage of capacitors. Good agreement between simulation results and circuit analysis has verified the operation of the proposed boost inverters.

References

[1] S. S. Lee, R. J. S. Lim, R. Barzegarkhoo, C. S. Lim, F. B. Grigoletto and Y. P. Siwakoti, "A Family of Single-Phase Single-Stage Boost Inverters," IEEE Transactions on Industrial Electronics, 2022, doi: 10.1109/TIE.2022.3215827.

[2] T. K. S. Freddy, N. A. Rahim, W. -P. Hew and H. S. Che, "Comparison and Analysis of Single-Phase Transformerless Grid-Connected PV Inverters," IEEE Transactions on Power Electronics, vol. 29, no. 10, pp. 5358-5369, Oct. 2014, doi: 10.1109/TPEL.2013.2294953.

[3] Y. Gu, W. Li, Y. Zhao, B. Yang, C. Li and X. He, "Transformer-less Inverter With Virtual DC Bus Concept for Cost-Effective Grid-Connected PV Power Systems," IEEE Transactions on Power Electronics, vol. 28, no. 2, pp. 793-805, Feb. 2013, doi: 10.1109/TPEL.2012.2203612.

[4] R. Barzegarkhoo, Y. P. Siwakoti, N. Vosoughi and F. Blaabjerg, "Six-Switch Step-Up Common-Grounded Five-Level Inverter With Switched-Capacitor Cell for Transformerless Grid-Tied PV Applications," IEEE Transactions on Industrial Electronics, vol. 68, no. 2, pp. 1374-1387, Feb. 2021, doi: 10.1109/TIE.2020.2967674.

[5] R. Barzegarkhoo, M. Forouzesh, S. S. Lee, F. Blaabjerg and Y. P. Siwakoti, "Switched-Capacitor Multilevel Inverters: A Comprehensive Review," IEEE Transactions on Power Electronics, vol. 37, no. 9, pp. 11209-11243, Sept. 2022, doi: 10.1109/TPEL.2022.3164508.

[6] S. S. Lee, Y. P. Siwakoti, R. Barzegarkhoo and K. -B. Lee, "Switched-Capacitor-Based Five-Level T-Type Inverter (SC-5TI) With Soft-Charging and Enhanced DC-Link Voltage Utilization," IEEE Transactions on Power Electronics, vol. 36, no. 12, pp. 13958-13967, Dec. 2021, doi: 10.1109/TPEL.2021.3088443.

[7] S. S. Lee, Y. P. Siwakoti, R. Barzegarkhoo and F. Blaabjerg, "A Novel Common-Ground-Type Nine-Level Dynamic Boost Inverter," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 10, no. 4, pp. 4435-4442, Aug. 2022, doi: 10.1109/JESTPE.2021.3104939.

[8] X. Hu, P. Ma, B. Gao and M. Zhang, "An Integrated Step-Up Inverter Without Transformer and Leakage Current for Grid-Connected Photovoltaic System," IEEE Transactions on Power Electronics, vol. 34, no. 10, pp. 9814-9827, Oct. 2019, doi: 10.1109/TPEL.2019.2895324.

[9] S. S. Lee, C. Shen Lim, Y. P. Siwakoti and K. -B. Lee, "Single-Stage Common-Ground Boost Inverter (S2CGBI) for Solar Photovoltaic Systems," 2019 IEEE Energy Conversion Congress and Exposition (ECCE), Baltimore, MD, USA, 2019, pp. 4229-4233, doi: 10.1109/ECCE.2019.8912963.

[10] S. S. Lee, Y. P. Siwakoti, C. S. Lim and K. -B. Lee, "An Improved PWM Technique to Achieve Continuous Input Current in Common-Ground Transformerless Boost Inverter," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 67, no. 12, pp. 3133-3136, Dec. 2020, doi: 10.1109/TCSII.2020.2967899.