Comparative Study of Single-phase and Three-phase DAB for EV Charging Application

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Keywords

≪Dual Active Bridge (DAB)≫, ≪Three-phase system≫, ≪Analytical losses computation≫ ≪Power converters for EV≫, ≪Battery≫.

Abstract

Bidirectional converters enable vehicle-to-grid (V2G) operations in electric vehicle (EV) charging stations. In this context, dual-active bridge (DAB) DC-DC converter is a preferable solution due to galvanic isolation and reduced volumes compared to other systems. Single-phase DAB (1ph-DAB) and three-phase DAB (3ph-DAB) topologies are usually compared in terms of efficiency and performances with the same rated power. Conversely, this paper focus on a comparison concerning device losses and stresses, medium-frequency transformer (MFT) design and capacitor filter sizing for the same power per switch, considering DABs and batteries coupled in a V2G application. Thereby, the impact of the battery state-of-charge (SoC) variation relative to the grid-side DC voltage is studied. Theoretical analysis and simulations results reveal that, in some respects, 1ph-DAB performance is superior to that of the 3ph-DAB with the proposed comparison approach. While, the main advantage of 3ph-DAB over 1ph-DAB is the reduced size of filter capacitors.

Introduction

Gas emissions restrictions and increasing air pollution suggest that other transportation technologies should be exploited leading to the future loss of oil's role [1, 2]. Nevertheless, conventional vehicles account for most of the global mobility fleet although electrification of transportation is leading to change future outlooks. EVs integration can bring several advantages related to energy sustainability such as

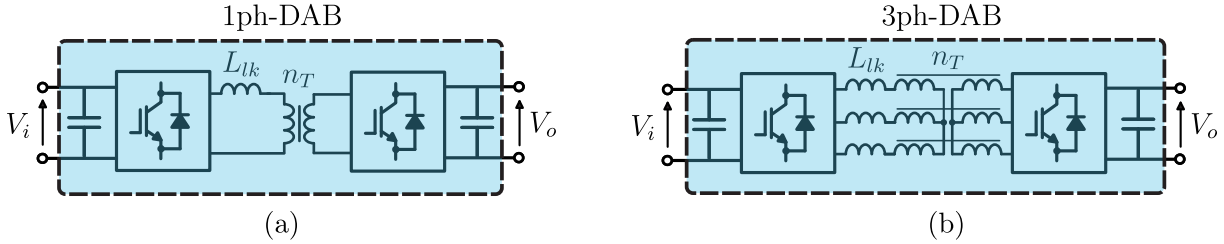

Fig. 1: Schemes for (a) 1ph-DAB and (b) 3ph-DAB

decarbonization and renewable energy integration. A relevant aspect is related to charging stations distribution and charging time, which greatly influences the EV penetration. When EVs are connected to the grid, battery charging has always been the main target. However, new opportunities are investigated for grid support, called V2G technologies [3]. In this context, it is necessary to design highly efficient systems that provide high power levels as powerful DC solutions [4–6].

DAB converter is one of the most popular converter for bidirectional power flow functionality given its high-power density, high efficiency and galvanic isolation [7, 8]. Two topologies are mainly used in the development of a bidirectional DC-DC bridge converter: single-phase and three-phase DABs. However, other several topologies and multi-phase structures are investigated with particular interest [9, 10].

In the existing literature, 1ph-DAB and 3ph-DAB performances are usually unfairly compared from the system utilisation perspectives (i.e. same rated power), leading to the 3ph-DAB outperforming the 1ph-DAB in terms of lower device losses, lower current harmonic content and capacitor size [11, 12]. Nevertheless, a more proper and comprehensive study is shown in [13] where the two topologies are compared with the same silicon area for low-voltage high-current applications. However, the paper focuses on an on-board charger that connects the LV battery to the internal HV-DC bus while the proposed study aims to analyse an off-board charging station solution for direct charging of the existing higher voltage batteries considering V2G applications. Furthermore, the cited efficiency analysis does not accurately consider the MFT losses nor its design. Analytical calculations on filter capacitor sizing are not shown and the gate driver losses are not included in the study. For this reason, considering the higher capability of 3ph-DAB compared to 1ph-DAB, the proposed comparison approach involves analysing the two topologies for a nominal power level related to the actual difference in the switching legs of the converters. Doing this, the 3ph-DAB is not favored. The study includes devices and gate driver losses, MFT design and capacitor sizing where all these aspects are considered with different battery voltages in order to estimate DAB's losses as a function of different EV state-of-charge. This, supported by the ever-increasing studies on DAB and batteries integration as well as the impact of output voltage variations on converter losses [14].

Single-Phase (1ph) and Three-Phase (3ph) DAB Comparison

The detailed structures for 1ph-DAB and 3ph-DAB are shown in Fig.1. Both converters consist of two back-to-back bridges connected together by a transformer and a series inductance. Its operation is based on the exchange of active and reactive power between two alternating voltage sources, which is regulated through the relative phase shift between them. As it is well known, as the active power is mainly defined by phase shift, the reactive power is exchanged in relation to voltage source amplitudes. This means that, especially under unbalanced voltage conditions such as EV batteries charging and discharging process, current stresses and losses must be carefully assessed. Several modulation techniques with different

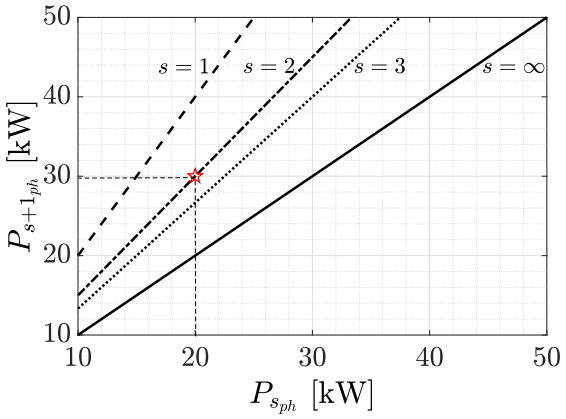

Fig. 2: Characteristic of (2) for different number of phases s which provides the power of the $s+1$-phases converter ($P_{s+1_{ph}}$) in order to have the same power per switch of the s-phase converter with power $P_{s_{ph}}$.

Table I: DABs parameter specifications

Topology	P_N [kW]	V_i [V]	V_o [V]	n_T [-]	L_{lk} [μH]	φ_{max} [rad]	f_{sw} [kHz]
1ph-DAB	20	800	600-800	1:1	61.1	$\pi/12$	20
3ph-DAB	30	800	600-800	1:1	27.7	$\pi/12$	20

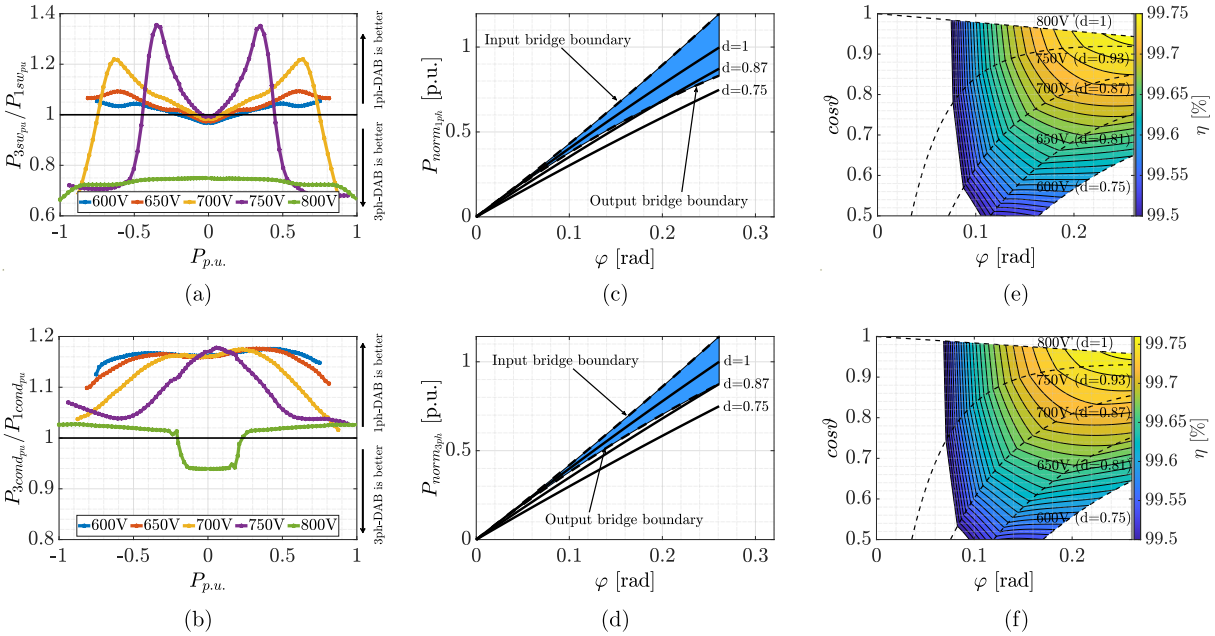

Fig. 3: Different comparison analysis between the two topologies in terms of device switching (a) and conduction (b) losses, ZVS range (c,d) and MFT losses (e,f) for 1ph-DAB and 3ph-DAB, respectively.

purposes are developed in literature although only single phase-shift (SPS) modulation is considered in this paper. More details on DAB operations can be found in [7] for both topologies.

Since the aim is to compare the converters for the same power per switch, the design rated power must be chosen with appropriate values. More in general, given an s-phase converter with a power $P_{s_{ph}}$ and a d-phase converter with $d > s$, the latter is able to provide a power $P_{d_{ph}}$, as described in (1):

$$P_{d_{ph}} = \prod_{M=s}^{d-1} \frac{M+1}{M} P_{s_{ph}}, \quad \forall \quad 1 \leq s < d \tag{1}$$

where s and d are the number of phases of the first and the second converter, respectively. A particular form of (1) can be defined for consecutive number of phases ($d = s+1$) as shown in (2):

$$P_{s+1_{ph}} = \left(\frac{s+1}{s}\right) \cdot P_{s_{ph}} \tag{2}$$

Figure 2 shows the characteristic of (2) for different number of phases s which, given the power of the s-phases converter $P_{s_{ph}}$, defines the the power of the $s+1$-phases converter $P_{s+1_{ph}}$ in order to have the same power per switch. The two nominal powers of the proposed DABs are highlighted by the red mark and the converters specifications are listed in Table I.

Specifically, the comparison approach focuses only on the DC-DC converters installed and operated in an existing DC grid. Thus, no assessment is made on AC grid-side rectifiers. Also, regarding a possible voltage and current imbalances in the 3ph-DAB transformer, it is assumed that the design is carefully performed to avoid them.

Power Losses on the Semiconductor Devices

Conduction and switching losses are the main losses for a switching device. These losses are estimated through simulations by varying the normalised power from -1 to 1 [p.u.], with different battery voltage to evaluate the impact of the SoC. Figures 3 (a) and (b) show the ratio between 3ph-DAB and 1ph-DAB switching and conduction losses in p.u., respectively, with different normalised power and output voltages. Each switching device consists of a SiC-MOSFET and its anti-parallel body-diode, both described by the manufacturer thermal model. The loss increment in 3ph-DAB is noticeable in both cases for most conditions. More specifically, 3ph-DAB switching losses are up to 35% higher for specific power conditions. Conversely, for all power conditions where no voltage mismatch occur switching losses are up to 30% lower with respect to 1ph-DAB. Also regarding conduction losses, 3ph-DAB performs worse causing losses to increase up to 18%. These considerations lead the 1ph-DAB to be more suitable in case of variable voltage applications such as V2G. Although gate driver losses are usually omitted due to their feeble contribution, in this work they are taken into account based on the model shown in [15]. Gate driver losses contribution has been also taken into account, resulting in 50% more losses in 3ph-DAB than in 1ph-DAB due to the larger number of devices.

ZVS Range Comparison

The total efficiency of DAB is highly dependent on the conditions of use. Particularly, the switching losses can worsen during hard-switching. Input and output ZVS boundary conditions can be found by specifying particular constraints to the inductance current as shown in [7] and [16] for 1ph-DAB and 3ph-DAB, respectively. Zero-voltage switching (ZVS) range is compared between the two systems to evaluate the operating spectrum. Figures 3 (c) and (d) show the normalized power relative to the rated power (solid lines) and the ZVS operating range (dashed lines) for the 1ph-DAB and 3ph-DAB, respectively, where $d = n_T V_o / V_i$ is the dc conversion ratio and φ the phase-shift angle. As shown, the ZVS operating range for 1ph-DAB is wider [13], allowing it to enter soft-switching mode earlier than in the three-phase case (see $d = 0.87$ line as reference example).

MFT Design and Losses Evaluation

MFTs were designed based on DABs maximum voltage mismatch and rated power. The purpose of the transformer design is to evaluate its losses at all operating points of the DAB in order to calculate a more accurate overall losses than that obtained with simulations for switching devices only. The transformer apparent power is calculated as in [7]. Considering the worst case scenario (i.e. $d = 0.75$ and $\varphi_{max} = \pi/12$), the apparent power equations are obtained in (3).

$$S_{T_{1ph}} = \frac{1}{2} V_i I_{1_{RMS}} (1+d), \qquad S_{T_{3ph}} = \frac{1}{\sqrt{2}} V_i I_{3_{RMS}} (1+d) \tag{3}$$

where $I_{1_{RMS}}$ and $I_{3_{RMS}}$ are the RMS primary current for 1ph-DAB and 3ph-DAB, respectively. For both topologies, 3C90 Ferroxcube E100/60/28 e-core has been used, changing the number of parallel cores to meet the design specifications. Both MFTs have a fully interleaved structure and a single layer winding. In order not to unnecessarily increase the transformer losses, the leakage inductance is made as small as possible preferring to include an external inductance to obtain the design value shown in Table I. Moreover, shell-type core magnetic structure has been chosen for both MFT.

Winding and core losses are the two main contribution to the total losses in a transformer. Since the MFT's frequency is much more higher than a line-frequency transformer, skin and proximity effects begin a crucial aspect in the correct evaluation of the AC resistance. Usually, Dowell's equations are used to determined the so-called resistance factor, which relates the DC resistance of the winding with its AC value. Following the calculations in [17], where the effect of interleaving structure on leakage inductance and winding losses is studied, it is possible to obtain copper losses as a function of d and φ for both MFTs.

Core losses are due mainly to two effects: eddy currents, which are induced in the core by the time-changing magnetic field and hysteresis losses. Steinmetz's equation provides a simple and easy way to

calculate core losses for sinusoidal voltages. Nevertheless, this equation is not accurate anymore with all those power electronics applications where the voltage excitation is far from sinusoidal. For all these cases, the Improved Generalized Steinmetz Equation (iGSE) [18] was introduced and it is used within this design analysis. The main variables to consider for specific core losses evaluation are the peak-to-peak value and the time derivative of the flux density $B(t)$ as well as the magnetic material parameters. Using a T-model for the MFT as in [19], it is possible to calculate the magnetic flux density integrating the voltage across the magnetizing inductance v_m as:

$$B(t) = \frac{1}{NA_c}\int_0^t v_m(t)dt \quad \text{where} \quad v_m(t) = \frac{v_p(t) + v_s'(t)}{2} \tag{4}$$

where N is the primary winding turns number, A_c is the cross section area of the core column and $v_p(t)$ and $v_s'(t)$ are the primary and secondary reflected MFT voltages, respectively. In general, the magnetic flux density peak changes mainly with the primary and secondary voltage values (and thus d). Many authors have studied the flux density reduction due to blanking times [20,21]. However, only the primary voltage is considered while the total voltage across L_m should be used to calculated the right reduction of $B(t)$ during load operations. In this way it is possible to evaluate the flux density reduction starting from the no-load condition as a function of d and φ allowing to add this losses to the winding losses and finally calculate the total losses of the MFT.

By substituting $v_m(t)$ in (4) and integrating, flux density time-varying equation and its peak value are found. At this point, iGSE equation can be evaluated including the flux derivative over time for the entire period T. Finally, the specific magnetic losses for 1ph-MFT are shown in (5). The same consideration can be done for the 3ph-MFT.

$$P_{s_{1ph}} = \frac{k_i}{\pi}(2B_m)^{\beta-\alpha}\left(\frac{V_i}{2NA_c}\right)^{\alpha} \cdot \left[\varphi|d-1|^{\alpha} + (\pi-\varphi)(d+1)^{\alpha}\right] \tag{5}$$

Figures 3 (e) and (f) show the MFT total efficiency for both topologies as a function of phase-shift and power factor $cos\vartheta$. Dashed lines highlight the MFT operation points for different battery voltages. As can be seen, the efficiency difference between the transformers is negligible and strongly depends on the construction topology of the windings and the ferromagnetic core. It is worth noting that for $d = 1$ (no voltage mismatch), there is a share of reactive power that increases as the phase shift increases for both cases. However, it can be shown analytically that the slope of this curve for the 3ph-DAB is $-3/(4\pi)$ versus $1/\pi$ for the 1ph-DAB, leading 3ph-DAB to process less reactive power for the same φ.

Current Efforts

An important aspect of converters design is the evaluation of the thermal limits of the switching devices and the MFT stresses. In particular, attention must be paid to the peak and RMS value of the full load current with mismatched voltages. For this reason, the current on L_{lk} is analytically calculated and compared performing a sweep analysis of d and φ. Figure 4 (a) shows the percentage difference between 1ph-DAB and 3ph-DAB where it can be seen that 1ph-DAB peak currents is up to 30% lower at high d values. As d decreases, this difference varies up to 10% in favor of 3ph-DAB. It is noticeable to see how the use of the three-phase topology is advantageous with regard to the peak current stress aspect for conditions where high power demands are paired with low DC conversion ratios. On the contrary, during all operations with low voltage mismatch, the 1ph-DAB shows a remarkable peak current reduction.
RMS current values for the same working conditions are analytically calculated and the RMS reduction of 1ph-DAB with respect 3ph-DAB is shown in Fig.4 (b). The RMS current difference varies between 4% and almost 9% for all the conditions, obtaining higher gap during low power. Despite the small difference, this results in the conduction loss ratio values shown in Fig.3 (b), being proportional to the square of the percentage difference.

From the single MOSFET perspective, since each device conducts only for half period, the RMS current is calculated as $1/\sqrt{2}$ times the RMS value of the inductor current whereas the peak current is the same of the inductor current, for both converters. For this reason, the ratios between 1ph-DAB and 3ph-DAB single device peak and RMS currents are exactly the same as shown in Fig.4 (a) and (b), respectively.

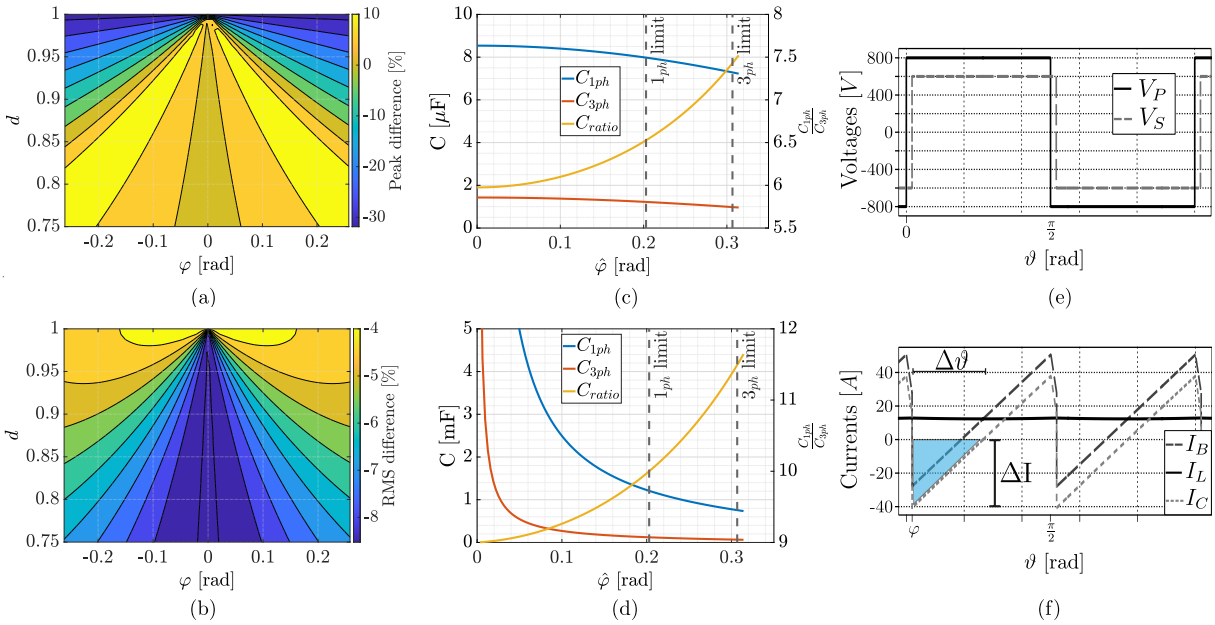

Fig. 4: Different comparison analysis between the two topologies in terms of peak (a) and RMS (b) current differences, filter capacitor values for voltage (c) and current (d) ripple constraints and DAB's voltages (e) and currents (f) waveforms for capacitor sizing calculation.

Filter Capacitor

In order to perform normal operations, DC/DC converters need input and output capacitors which are designed too meet voltage ripple specifications by using the best capacitor technology for each application. The input and output properties of power converters, as well as the allowed maximum voltage ripple, vary depending on the converter application. Low ESR and ESL values and high capacitance densities are particularly needed for filter capacitor solutions due to the tendency towards high switching frequencies and the need for small converter volumes [22]. Electrolytic capacitors are most commonly used when high capacitance values are needed. However, when high voltages are required, it is more appropriate to use film capacitors due to their lower internal resistance and higher current capability.

The purpose of this section is to analyse the worst scenario from the point of view of battery-side filter capacitor sizing. In fact, in order to design the filter appropriately and to meet the ripple voltage and current constraints, the worst case (i.e. the one with the minimum value of d and the minimum phase-shift angle) must be considered to evaluate the maximum amount of charge variation ΔQ.

Considering the voltage and current waveform depicted in Fig.4 (e) and (f), it is possible to calculate the electrical charge ΔQ accumulated during the capacitor charging process (blue shadowed area) as in (6), where I_B is the output bridge current, I_C is the capacitor current and I_L is the battery current.

$$\Delta Q = \Delta V \cdot C = \frac{\Delta\vartheta}{2} \cdot \Delta I = \frac{\Delta\vartheta}{2} \cdot I_C(\varphi), \quad I_C(\varphi) = I_B(\varphi) - I_L \tag{6}$$

In order to calculate the angle variation $\Delta\vartheta$, the output current equation of the bridge from φ to $\pi/2$ has to be considered and set equal to I_L, as in (7), whereas ϑ is the angle variable.

$$I_B(\vartheta) = I_B(\varphi) + \frac{V_i - nV_o}{L_{1ph}}\vartheta = \frac{V_i\left(2\frac{\varphi}{\pi} - 1\right) + nV_o}{4fL_{1ph}} + \frac{V_i - nV_o}{L_{1ph}}\vartheta = I_L \qquad \forall \quad \vartheta \mid \varphi \leq \vartheta \leq \frac{\pi}{2} \tag{7}$$

Solving (7) for ϑ, substituting in (6) and solved for C, the minimum capacity needed to comply the voltage ripple constraint is obtained in (8) and with similar considerations for 3ph-DAB in (9):

$$C_{1ph} = \frac{\Delta Q}{\hat{V}_o \delta_{V\%}} 100 = \frac{V_i \left[\pi^2(1-\hat{d}) + 2\hat{\varphi}[n(\pi-\hat{\varphi})-\pi]\right]^2 \cdot 100}{8\omega^2\pi^2 L_{1ph}(1-\hat{d})\hat{V}_o \delta_{V\%}} \tag{8}$$

$$C_{3ph} = \frac{\Delta Q}{\hat{V}_o \delta_{V\%}} 100 = \frac{V_i \left[2\pi^2(1-\hat{d}) + 3\hat{\varphi}[n(4\pi-3\hat{\varphi})-4\pi]\right]^2 \cdot 100}{432\omega^2\pi^2 L_{3ph}(1-\hat{d})\hat{V}_o \delta_{V\%}} \tag{9}$$

where $\delta_{V\%}$ is the ripple voltage define as $\delta_{V\%} = \Delta V / \hat{V}_o \cdot 100$ and ΔV is the peak-peak DC voltage.
In the above equations, $\hat{\varphi}$, $\hat{d}$ and $\hat{V}_o$ are the minimum value of φ, d and V_o, respectively, which leads to a worst condition.
As can be seen in (6), ΔQ is only valid for a specific φ and d ranges because, by increasing them, the blue shadowed shape changes no longer being a simple triangle. In mathematical terms, it is possible to state that (6) holds only when $-I_B(\varphi) - I_L \geq 0$ is true. Solving $-I_B(\varphi) - I_L \geq 0$, two solutions are found. Whereas one is trivial ($\varphi = 0$ and $d \leq 1$), the second one gives the maximum angle for which the capacitor equation is true for a given d. Now, consider the two topologies and doing same considerations for the 3ph-DAB, (10) shows the φ range for which (6) holds.

$$\text{1ph-limit: } 0 \leq \varphi \leq \frac{1}{2}\left(2\pi - \sqrt{2}\pi\sqrt{d+1}\right), \quad \text{3ph-limit: } 0 \leq \varphi \leq \frac{1}{3}\left(\pi - \pi\sqrt{2d-1}\right) \tag{10}$$

Fig.4 (c) illustrates (8) and (9) for different values of $\hat{\varphi}$ considering a $\delta_{V\%}$=5%. The capacitors ratio ($C_{ratio} = C_{1ph}/C_{3ph}$) is also calculated just to emphasize the capacitance difference which show that C_{1ph} requires more or less 6 times the C_{3ph} size. The limits of (10) are depicted by the dashed vertical lines for $\hat{d} = 0.75$. However, the previous considerations are not useful to limit the current ripple in case of a equivalent battery model, i.e. an impedance in series with a DC voltage source. In this case, the constraint is defined on the current ripple whereas the voltage ripple will be a consequence. The relationship between $\Delta I(s)$ and $\Delta Q(s)$ in the Laplace's domain is represented in (11).

$$\Delta I(s) = \frac{\Delta V(s)}{R_{bat} + sL_{bat}} = \frac{\Delta Q(s)}{C(R_{bat} + sL_{bat})} \tag{11}$$

where R_{bat} and L_{bat} are the total output resistance and inductance of the battery, respectively. As expected, the capacitor size is dependent on the output equivalent impedance and on the allowed current ripple. Since the battery impedance is quite small (few $m\Omega$), the capacitance tends to increase to very high values. A possible solution is to introduce a LC filter to limit the current variations. Fig.4 (d) shows the capacitors value for the two topologies with a 5% ripple current constraint with a pure resistive battery impedance ($R_{bat} = 0.2\Omega$). With these constraints, C_{3ph} appears to be up to 10 times smaller than C_{1ph} for the considered parameters, resulting in a less expensive and less bulky capacitors to be used.

Conclusions and Future Works

In case of variable conditions typical of battery charging process, this paper aims to fairly evaluate 1ph-DAB and 3ph-DAB. Device and MFT losses, ZVS ranges, peak and RMS current stresses as well as capacitor filter sizing have been compared between the two topologies, leading to the following findings and considerations. (1) For most conditions, 3ph-DAB switching and, more clearly, conduction losses are higher compared with 1ph-DAB up to 30% and 18%, respectively. (2) ZVS boundaries for 1ph-DAB result in wider soft-switching operations and thus, for a greater range of normalised transferred power than in the 3ph-DAB case, the 1ph-DAB working points lie within the soft-switching region. (3) Particular operating conditions can reduce peak current stress by up to 30% for the 1ph-DAB while 3ph-DAB RMS current is up to 9% higher despite its lower harmonic content. (4) 3ph-DAB requires much smaller capacitors due to reduced voltage and current ripple resulting in smaller volumes and weights.

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