Non-parasitic induced transient overvoltage in ANPC topology due to critical switching sequences

Michael Geiss, Robert Kragl, Jürgen Thoma, Benjamin Volzer
FRAUNHOFER INSTITUTE FOR SOLAR ENERGY SYSTEMS ISE
Heidenhofstraße 2
79110 Freiburg, Germany
Tel.: +49 / (0) 761 4588-5069.
E-Mail: michael.geiss@ise.fraunhofer.de, robert.kragl@ise.fraunhofer.de,
juergen.thoma@ise.fraunhofer.de
URL: http://ise.link/hpe

Keywords

Multi-level inverters, Wide bandgap devices, MOSFET, IGBT, Converter control

Abstract

This paper describes a semiconductor overvoltage in an Active-Neutral-Point-Clamped Converter (ANPC). This overvoltage occurs in case of inductive load when the output voltage of the ANPC changes its polarity. In case of a grid inverter this occurs twice per grid period at the voltage zero crossing. It can be observed in most of the ANPC-based power electronics with classical PWM patterns and can reach the full DC-Link voltage. Although the ANPC is a well-known and widely spread topology there has been no particular concern in literature about this effect yet. From our point of view, the reason for this is a generous semiconductor dimensioning in terms of blocking voltage utilization and the limited energy due to the nature of the overvoltage. Nevertheless, this overvoltage could become a problem in modern designs when SiC MOSFETs are used, and their Safe Operating Areas (SOA) are pushed even further to the limits.
The shown overvoltage is not a switching overshoot due to parasitic inductances and high switching speeds. It cannot be explained by "hazardous" switching states either.
In the following, the emergence is described in detail and a theoretical model is introduced and evaluated by simulations and measurements. Afterwards, methods to avoid the overvoltage are shown and a risk estimation is performed.

Introduction

Multilevel topologies like ANPC, NPC or Flying-Cap are well-known and used in different applications for decades. They were first used in traction applications and afterwards they found their way to grid-connected inverters and even DC-DC-converters. Apart from the drawback of a higher number of semiconductors, they offer several benefits such as the use of semiconductors with lower blocking voltages, a better Total Harmonic Distortion (THD), and a smaller filtering effort.
In comparison to the Neutral Point Clamped Inverter (NPC), the active-NPC (ANPC) allows several additional zero-switching states. By corresponding implementation of these states, a better loss distribution [1] or a doubling of the apparent switching frequency [2] can be achieved, among others. Due to lower semiconductor blocking voltages the engineer has to ensure that under no circumstances is the full DC-Link voltage applied to a single switch. In addition to the "safe" switching states, there are "hazardous" states that can end up with one switch to be presented to the full DC-link voltage, and "destructive" states, which lead to a short circuit of half or the full DC-link [11]. Moreover, different cases like the emergency shutdown are known as critical in this context and therefore special switching sequences have to be followed [3].

This paper introduces another condition which leads to an overvoltage across one of the ouput switches (T2 or T3). In this case, the cause are not transient overvoltages in the switching moment or static “hazardous” switching states. The problem occurs with the use of - according to [11] - “safe” switching states in a critical sequence, when changing the polarity of the output voltage of the ANPC. The details will be explained in this paper.
The paper is structured as follows. In the first section the emergence of the overvoltage is described in detail and factors that favor its emergence are shown. Furthermore, a theoretical model is introduced and the influence of the output capacitance of the switches, the deadtime and the load current are discussed. Afterwards, the difference between full-SiC and hybrid (SiC MOSFET and Si IGBT) ANPC is explained. The theoretical model is compared with SPICE simulations and measured values. In the second section, possible strategies to avoid the overvoltage are given. The last section gives a risk assessment of the potential danger of the overvoltage.

Emergence of the overvoltage

In this first section, the emergence is explained in detail. All explanations are given for the upper half of the ANPC but apply in mirror image for the lower half as well.
The emergence of the overvoltage is explained based on one example switching sequence. Fig. 1 shows the different steps of this sequence. All switches are drawn as a combination of MOSFET, diode and capacitor. The diode represents the intrinsic diode, and the capacitance represents the output capacitance (C_{OSS}) of the MOSFET. Both is drawn for better understanding. The green rectangles show the actively switched on MOSFETs. The blue voltages show the present drain-source-voltage (V represents $V_{DC\text{-}link}/2$) and the trend (if it rises or falls). An ohmic-inductive load is assumed. Parasitic inductances were intentionally omitted because they have no influence on the occurrence of the overvoltage.

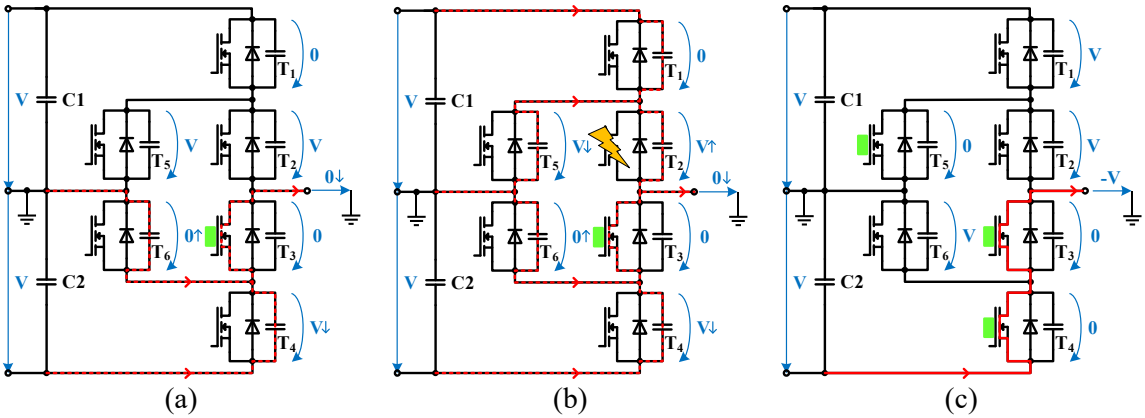

Fig. 1: Example „hazardous“-switching sequence for ohmic-inductive load

Starting point is the state “0L1” with positive output current as shown in Fig. 1 (a). The problem occurs when switching to the safe state “N”. To get there, the MOSFETs T1 and T6 have to be switched off. This step is shown in Fig. 1 (b). At first, the output current charges $C_{OSS,T6}$. At the same time, $C_{OSS,T4}$ gets discharged to obey Kirchhoff's circuit laws. This leads to a falling output voltage. Due to the zero-current switch off of T1, $C_{OSS,T1}$ is not charged and so the problem occurs. Due to the falling output voltage, $C_{OSS,T1}$ has to be charged (Fig. 1 (b)). The only path for the charging current is through $C_{OSS,T2}$. Because this capacitance is already charged, the drain-source voltage of T2 rises above V. The overvoltage remains until the end of the deadtime when the state “N” is switched on by turning on the switches T4 and T5 (Fig. 1 (c)). With T5 on, T1 is clamped to V and $C_{OSS,T2}$ is discharged to V. This shows, that despite the use of only “safe” switching states an overvoltage occurs within the dead-time due to the missing charge of $C_{OSS,T1}$.
In summary, the problem always occurs when the outer switches (T1 / T4) are switched off at zero-current with the inner switches (T2 / T3) turned off, and a following change in polarity of the output voltage. As there is no current flowing through T2 just before the occurrence (Fig. 1 (a)), parasitic inductances have no influence on this effect.

Theoretical description of the overvoltage

In this Subsection, a simplified theoretical model was derived to calculate the maximum amplitude of the overvoltage. It is introduced shortly and evaluated using simulation and measurement data.

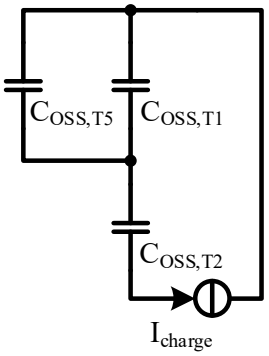

Fig. 2: Equivalent circuit diagram of the upper half of an ANPC to calculate the overvoltage.

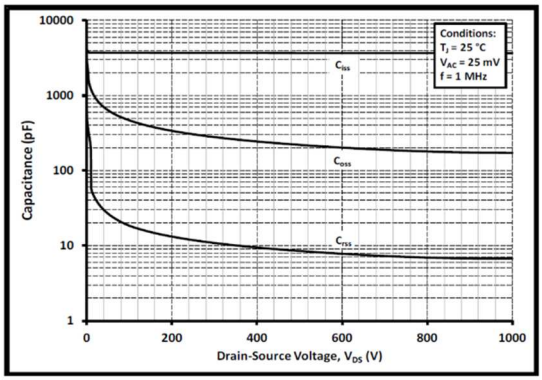

Fig. 3: Example datasheet [12] extract that shows the voltage dependency of C_{OSS} of a 1.7 kV SiC MOSFET.

During the occurrence of the overvoltage, there is no switching action in the upper half. The current flowing in the upper half occurs due to the decrease of the output voltage. Thus, the upper and the lower half of the ANPC can be considered separately. With these assumptions, the upper half can be transferred to an equivalent current source circuit diagram as shown in Fig. 2. This results in a capacitive divider. As charge current, a constant current is assumed as the interest of the calculation is the maximum overvoltage and not the rising speed. With this assumption, and the boundary condition that $V_{COSS,T1} + V_{COSS,T2} = V_{DCLink}/2$ at the end, the formula to calculate the overvoltage ΔV_{T2} can be derived as given in Eq. (1).

$$\Delta V_{T2} = \frac{V_{DCLink}}{2} * \frac{1}{\frac{C_{OSS,T2}(V_{DS,T2})}{C_{OSS,T1}(V_{DS,T1}) + C_{OSS,T5}(V_{DS,T5})} + 1} \tag{1}$$

Considering a full-SiC ANPC with 6 similar MOSFETs, a maximum overvoltage of 66 % could occur when assuming the same and constant C_{OSS} for all switches. This assumption is not correct since the output capacitance is highly dependent on V_{DS} as shown in Fig. 3.
At the starting point of the voltage rise, $C_{OSS,T2}$ is already charged to its rated voltage. Thus, the capacity will not change significantly with a further rising voltage. $C_{OSS,T1}$, on the other hand, is completely discharged and therefore has a much higher capacity at the beginning which becomes smaller with rising voltage. Assuming the same charge to be put into both the capacitors, the voltage of $C_{OSS,T2}$ would rise much faster than the one of $C_{OSS,T1}$. This makes the effect even worse. Therefore, the maximum voltage cannot be calculated directly with Eq. (1). Instead, it has to be calculated iteratively using theoretical equivalent capacities. This procedure is explained in the following.
Core of the iterative calculation is a charge-based replacement capacity. The stored charge at a certain voltage can be derived by the integral over the C_{OSS} curve as given in Eq. (2). From this charge, a constant capacity with the same charge stored at this voltage can be derived as shown in Eq. (3). The start and stop voltages are the drain-source-voltages at the beginning and at the end of the reloading process.

$$Q = \int C_{OSS}(V_{DS})\, dV \tag{2}$$

$$C_{OSS,const} = \frac{\int_{V_{DS,Start}}^{V_{DS,Stop}} C_{OSS}(V_{DS})\, dV}{V_{DS,Stop} - V_{DS,Start}} \tag{3}$$

This replacement capacity can be used in Eq. (1). The difficulty lies in the unknown voltage $V_{DS,Stop}$. Therefore, the calculation has to be done iteratively in the following steps:

1. The overvoltage is calculated by use of the rated output capacities.
2. The replacement capacities for T1, T2 and T5 are calculated using the calculated overvoltage and equation Eq. (3).
3. The new overvoltage is calculated using the replacement capacities.
4. Steps 2 and 3 are repeated until the calculated overvoltage reaches a fixed value

For a full-SiC ANPC with the MOSFETs shown in Fig. 3 and an assumed DC-link voltage of 2 kV, a maximum drain-source voltage across T2 of 1861 V is calculated.
There is no direct dependency between the output current and the resulting maximum overvoltage in case of full-SiC. But the output current determines how fast the reloading takes place and therefore how fast the overvoltage rises. With short deadtimes, small output currents, respectively big output capacities, and the fact that the overvoltage exists only during the deadtime, the theoretical maximum overvoltage value may not be reached.

Simulation and measurement results

The theoretical model was verified by simulations using LT-SPICE. A full-SiC ANPC was simulated using the manufacturers SPICE Models of the MOSFETs shown in Fig. 3. As load, a 15 A current source was used. Fig. 4 shows the simulation results of the switching sequence given in Fig. 1. In the simulation, the maximum drain-source voltage across T2 reached 1877 V. This fits very well into the iterative calculated value of 1861 V. The error can occur due to partly linearization and readout errors of the C_{OSS} curve.

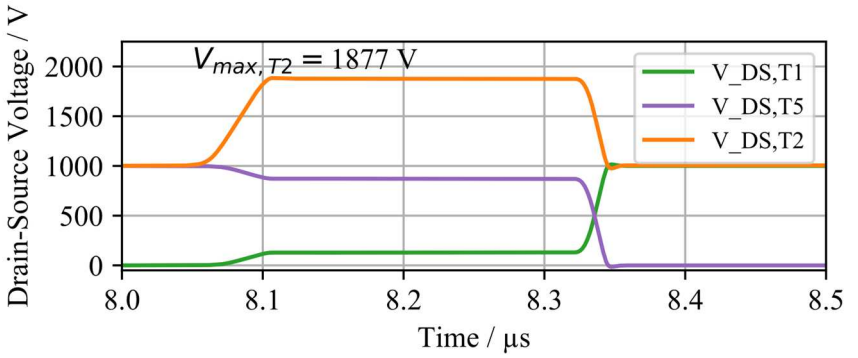

Fig. 4: LT Spice simulation results for the example switching sequence

The overvoltage was measured in different ANPC projects with different configurations. Thus, the formula was also evaluated using measurement data.
One example is given in Fig. 5. The curves were measured at an inverter based on a full-SiC ANPC consisting of 900 V, 120 mOhm MOSFETs. The inverter has a nominal power of 4 kW at an output voltage of 400 V and is driven in open-loop control with a fixed PWM pattern for doubling the output frequency as given in [2].

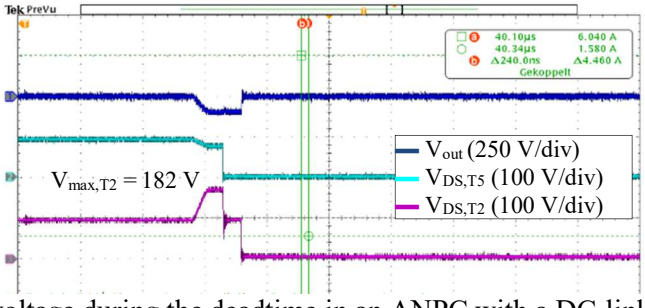

Fig. 5: Measured overvoltage during the deadtime in an ANPC with a DC-link voltage of 200 V

At the shown working point with a DC-link voltage of 200 V, a maximum drain-source-voltage of 182 V could be measured. The calculation for this configuration based on Eq. (1) and Eq. (3) gives a maximum of 185.8 V, a value that fits very well into the measurement data.

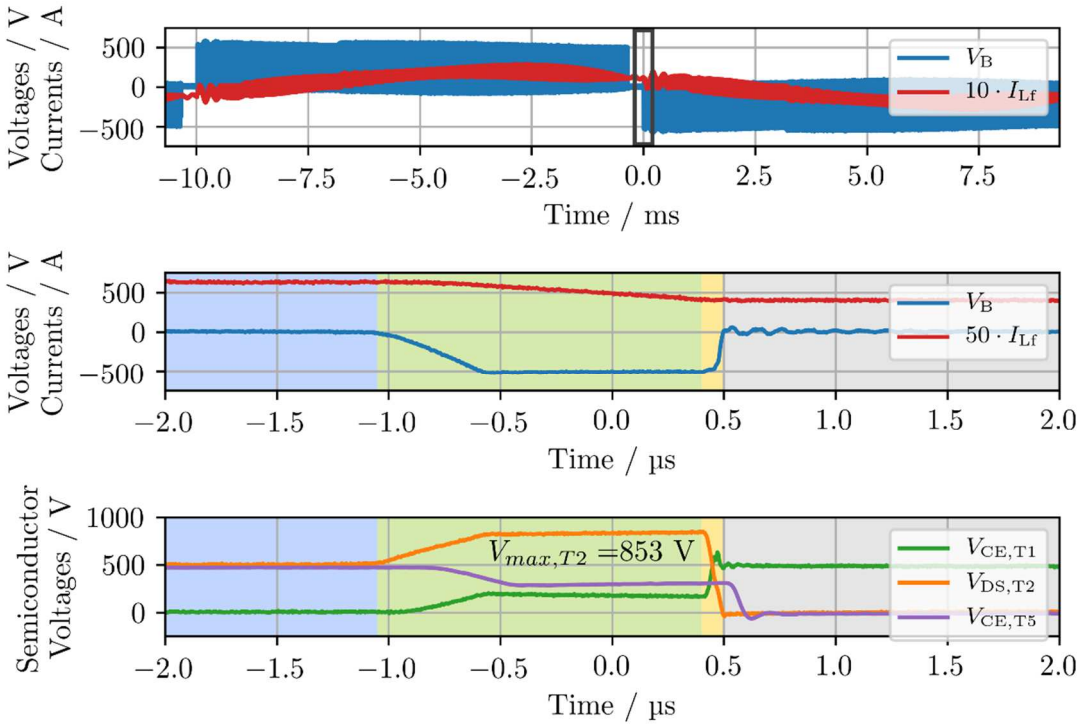

Fig. 6: Measured overvoltage during the deadtime in a hybrid ANPC with a DC-link voltage of 1000 V

Another measurement was performed on a 250 kW three-phase inverter based on a hybrid ANPC. In this case, the ANPC consists of two fast-switching 1.7 kV SiC MOSFETs for T2 and T3 and four slow-switching 1.7 kV Si IGBTs. The inverter is driven in open-loop control with a slightly adapted "ANPC-12" PWM pattern from [2]. The load is 5.16 kvar with a power factor of 0.8_{ind}. The measurement was performed with a lowered DC-link voltage of 1 kV and with an extremely long deadtime of 2 µs for a better visualization of the overvoltage.
Fig. 6 shows the measurement results. The first graph shows the ANPC output voltage and the line-filter current over one grid period. In the second graph, the same values are shown but with a zoom to the point where the output voltage changes its polarity. Graph 3 shows the drain-source respective collector-emitter voltages of the upper three switches at the same time interval.
Two things can be obtained here. First, the overvoltage at T2 of 71 % related to $V_{DC\text{-}Link}/2$. Secondly, the switching pattern is not the one used in Fig. 1 but also in this case overvoltages occur. Unfortunately, the amplitude of the overvoltage cannot be compared to the calculated value because the given formula does not consider the forward recovery charge of IGBTs. The details are explained in the next section.

Comparison of full-SiC MOSFET and hybrid ANPC

In a 4 IGBT and 2 MOS hybrid version of the ANPC [8], the problem is getting worse. In addition to charging the output capacitor of an IGBT, there are carriers needed for the recovery of the junction. When the output voltage starts to fall as shown in Fig. 1 (b), a current flows through T1 an T2. At first, this current effects T1 only in the way of clearing out charge carriers, but already charges $C_{OSS,T2}$. Only then can $C_{OSS,T1}$ be charged. With this delayed charge of $C_{OSS,T1}$, the drain-source-voltage of T2 rises to a higher level and can reach the full DC-link voltage (or the avalanche voltage) even before the junction of T1 is fully recovered.

Due to the additional charge needed for the recovery of the junction, the simplified model behind Eq. (1) does not fit anymore. One option to approximate the forward recovery charge is to add an additional capacitor parallel to $C_{OSS,T1}$ that represents this additional charge. Unfortunately, it is complex to calculate the capacity because the recovery charge is highly dependent on the collector current, the switching speed and other values. Hence, a simple calculation of the overvoltage with the given formula is difficult for a hybrid ANPC. Furthermore, the current dependency of the forward recovery charge results in a load current dependency of the maximum overvoltage.
Another difference of the hybrid ANPC is the slower switching speed of the IGBTs and therefore the slow drop of the output voltage in Fig. 1 (b). Therefore, the rising speed of the overvoltage is more dependent on the switching speed of the IGBTs than on the load current.
As a conclusion it can be said that the overvoltage has a higher amplitude in a 4 IGBT and 2 MOS hybrid version of the ANPC, but the maximum cannot be precalculated with the given formula.

Further causes of occurrence

The direct use of a hazardous sequence as explained is just one possible trigger for the occurrence of the overvoltage. But there are other possibilities. The most important ones are described in the following.

Emergency shutdown

As explained in [3], there is a special switching sequence for an emergency shutdown, where the outer switches (T1/T4) always have to be switched off before the output switches (T2/T3) can be switched off. Otherwise, a difference in the switching speed of the semiconductors can lead to an overvoltage. This fixed shutdown sequence does not help to avoid the overvoltages explained in this Paper. If the emergency shutdown starts e.g. in the state shown in Fig. 1 (a) then this will lead to an overvoltage.

Missing gate signals due to deadtimes

Besides the direct use of a hazardous sequence, the effect can also occur because of missing gate signals due to deadtimes. One example is the sequence „P“ → „0L1“ → „P“ → „0U1“ → „N“. Here, a save sequence is used for the transition from the upper to the lower half of the ANPC. In an ideal inverter without any deadtime everything works fine. In a real converter, however, there are “P” pulses missing around the zero crossing because the pulse duration given by PWM generator gets shorter than the deadtime. In this case, the given sequence is altered to „P“ → „0L1“ → „0U1“ → „N“. In the deadtime between “0L1” and “0U1”, the overvoltage will occur.

Shadowing

Another trigger can be the shadowing function of the digital controller for the PWM. Shadowing means a sample-and-hold of the compare values at some defined point of the PWM period. This is mostly done in the highest and/or the lowest point of the triangular carrier value. Depending on which variant is chosen, the switching sequence can be alternated, and overvoltages can occur.

Occurrence in different PWM patterns

Table I: Overview of different ANPC SPWM

Name	Overvoltage without alternated implementation
ANPC-11-Sync [2]	No
ANPC-12 [2]	Yes
ANPC-DF [2]	Yes
ANPC-ALD [4]	No
ANPC-R2:1 [5]	Yes
ANPC-OOZS [6]	No
ANPC-SSLD [7]	Yes

With sine-triangle-PWM (SPWM) based modulations the used switching states are often fixed. When comparing different SPWM patterns for the ANPC, four out of seven investigated patterns showed the overvoltage in a straight forward implementation without any adjustments. An overview of the investigated PWM patterns is given in Table I.

Strategies to avoid the overvoltage

This section explains different options to solve the overvoltage problem.

Adaption of the PWM pattern

The most obvious way to solve this problem is to avoid the hazardous sequences of switching states. However, this could mean reducing or limiting the respective advantages of the chosen PWM pattern. For example, in a PWM pattern to double the apparent output frequency, all zero states have to be used in a fixed and alternating manner. This can lead to hazardous sequences. If the pattern is alternated in a way that there are no overvoltages, the doubling of the output frequency will no longer work.
Another option is to activate an alternative path to charge the output capacity of T1. In the case of the sequence shown in Fig. 1, a possible charge path would be via T5. Thus, in Fig. 1 (b) T1 and T6 must not be switched off at the same time. First, T1 has to be switched off and after the deadtime, T5 is switched on to charge $C_{OSS,T1}$. Then, T6 is switched off and then T4 is switched on after the deadtime. With this sequence, the overvoltage is avoided. The disadvantage of this sequence is that it takes longer because of two deadtimes. Also, the PWM generation becomes more complicated. Additionally, in case of emergency shutdown, a sequence where switches have to be switched on again is not acceptable.

Additional Switching Cell Capacitor

A very effective way to avoid the overvoltage is the use of a snubber capacitor across T2 and T3 as shown in Fig. 7. This capacitor creates a parallel path to T2 for charging T1. An additional advantage of the capacitor is a shorter commutation path between T2 and T3 as explained in [9], and therefore smaller voltage overshoots in the switching moment due to parasitic inductances. This can be interesting especially for the hybrid ANPC.

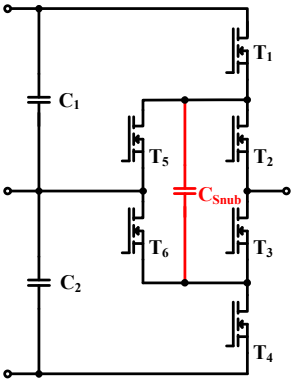

Fig. 7: Full-SiC ANPC with additional capacitor to avoid the overvoltage

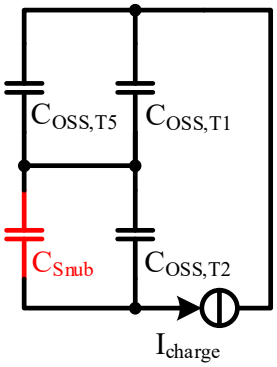

Fig. 8: Equivalent circuit diagram of the upper half of an ANPC to calculate the overvoltage with additional capacitor.

With the additional capacitor the equivalent circuit diagram in Fig. 2 can be extended as shown in Fig. 8. With the same assumptions as made before, a new formula to calculate the overvoltage can be derived and rearranged with the additional capacitor C_{Snub} as given in Eq. (4). With this formula, the size of the additional cap can be calculated for a chosen maximum overvoltage in a full-SiC ANPC. Again, charge-based replacement capacities have to be calculated with Eq. (3) for the chosen overvoltage.

$$C_{Snub} = \left(\left(\frac{\frac{U_{DC}}{2}}{\Delta U_{max}} - 1 \right) * \left(C_{OSS,T1} + C_{OSS,T5} \right) \right) - C_{OSS,T2} \tag{4}$$

Fig. 9 shows the results of the same simulation that was used for Fig. 4 but with the additional capacitor C_{Snub}. The value was calculated with a chosen ΔU_{max} of 100 V. As can be seen, the calculation fits very well into the simulation results.

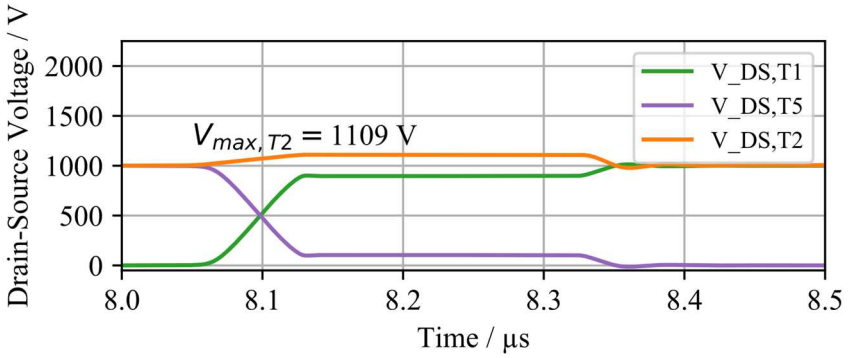

Fig. 9: LT Spice simulation results for the example switching sequence with additional capacitor

The additional capacitor was also successfully implemented in the hybrid ANPC as described before. Since the calculation of the overvoltage does not work for a hybrid ANPC as explained before, the calculation of the additional capacitor does not work either. Thus, the right value had to be found by simulation and was chosen as 100 nF. Fig. 10 shows the measurement results of the same inverter that was used for the measurement results in Fig. 6. But in this case the additional capacitor was added. As can be seen clearly, the capacitor works very well and there is no occurrence of overvoltage.

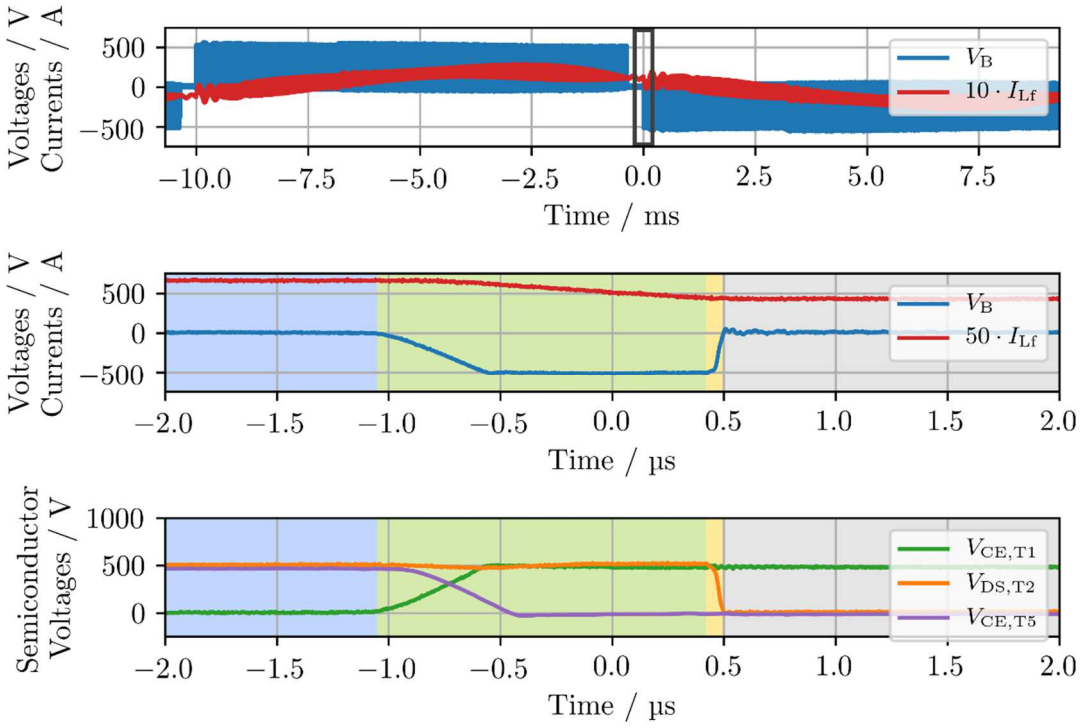

Fig. 10: Measured overvoltage during the deadtime in a hybrid ANPC with a DC-link voltage of 1000 V and additional capacitor

The drawback of this solution is the additional capacitor, which can lead to a ringing between itself, the parasitic inductances of the current path and the DC-Link when switching the outer transistors. This is described in [9] where the capacitor is used to shorten the commutation path of the output MOSFETs T2 and T3. No ringing problems occurred in the inverter presented.

Risk estimation

The ANPC is known and used for decades in different applications but there is no mentioning in the literature about the described overvoltage. So it is likely that the overvoltage does not lead to an immediate destruction of the semiconductors. It is difficult to judge how hazardous the overvoltage really is and depends on different factors. Two influences are discussed in the following.

Limited Energy and repetitive avalanche

One important point is that even if the overvoltage occurs, it will not have to be destructive for the semiconductors. This comes due to the limited energy that is brought into T2 during the overvoltage. The limit is given, on the one hand, by a time limit due to the deadtime. On the other hand, a possible avalanche current can only flow during the charge of $C_{OSS,T1}$, and therefore only until the summed up voltage of $V_{DS,T1} + V_{DS,T2}$ reaches the full DC-link voltage as can be seen in Fig. 1 (b). This limited energy is normally much lesser than the avalanche energy needed for destruction. In the hybrid case, the charge for the recovery of the junction adds on top.
Considering this, depending on the semiconductors, the overvoltage is expected to end with no or just a low energy avalanche and therefore with no immediate destruction. This does not mean that the effect will bring no harm. In the case of a grid inverter, this low energy avalanche occurs with the double grid frequency and in the case of a multilevel DCDC converter, it can occur with the switching frequency. As described in [10], a repetitive occurrence can impact the reliability of the device over its lifetime. Because the amount of energy is hard to predict and there is not much data from the manufacturers about repetitive avalanche withstand capability of the devices, an estimation is difficult for this case and will not be investigated further at this time.

Semiconductor utilization

Another important point is the semiconductor utilization in terms of blocking voltage, so what percent of the maximum blocking voltage is allowed by the developer to be seen by the semiconductors. If the ANPC is equipped with semiconductors that can block nearly the full DC-Link voltage, the additional overvoltage will not affect the semiconductors at all. There are different manufacturers that equip their inverters in such a way that the benefits of the ANPC in terms of smaller filter effort are fully taken but do not have to care about e.g. shutdown sequences.
In addition to a direct use of semiconductors that can block the full DC-Link voltage, there are cases where the semiconductors are utilized to a higher percentage of their blocking voltage for special operating points, but in the normal operating points the utilization is much lower. One example is a PV-inverter without DCDC converter. In this case, the maximum DC link voltage is the V_{OC} of the PV array. If the semiconductors are utilized by 80 % in this case, the utilization in the maximum power point operation will only be around 51 %.
In summary, the application and the chosen semiconductors will have a big influence when the overvoltage really is a destructive overvoltage from the semiconductors side of view. But through an increasing cost pressure in different markets, the semiconductor utilization is pushed further to its limits, so the problem could become more important in future.

Conclusion

In this paper, a drain-source overvoltage was investigated that occurs during normal switching operations in ANPC. It is caused due to critical switching sequences and can reach the full DC-link voltage. A theoretical model is introduced and validated by simulation and measurement results. The influence of the semiconductor output capacity and the load current is explained. Furthermore, strategies to avoid the overvoltage are discussed. Finally, a first risk estimation is given. Summarized, the maximum of the overvoltage has a strong dependency on the used semiconductors and the design of the power electronics. Furthermore, with the given considerations about the limited energy, the effect will most likely not lead to an immediate destruction of the semiconductors but could influence their lifetime.

References

[1] T. Bruckner and S. Bemet, "Loss balancing in three-level voltage source inverters applying active NPC switches," 2001 IEEE 32nd Annual Power Electronics Specialists Conference (IEEE Cat. No.01CH37230), 2001, pp. 1135-1140 vol.2, doi: 10.1109/PESC.2001.954272.

[2] D. Floricau, E. Floricau and M. Dumitrescu, "Natural doubling of the apparent switching frequency using three-level ANPC converter," 2008 International School on Nonsinusoidal Currents and Compensation, 2008, pp. 1-6, doi: 10.1109/ISNCC.2008.4627496.

[3] I. Staudt, “3L NPC & TNPC Topology”, Semikron Application Note AN-11001, 2015, 2015-10-12 – Rev05

[4] Lin Ma, Xinmin Jin, T. Kerekes, M. Liserre, R. Teodorescu and P. Rodriguez, "The PWM strategies of grid-connected distributed generation active NPC inverters," 2009 IEEE Energy Conversion Congress and Exposition, 2009, pp. 920-927, doi: 10.1109/ECCE.2009.5316449.

[5] Bo Zhang, Qiongxuan Ge, Longcheng Tan, Xiaoxin Wang, Qiankun Chang and Jinxin Liu, "A new PWM strategy for three-level Active NPC converter," 2013 International Conference on Electrical Machines and Systems (ICEMS), 2013, pp. 1792-1795, doi: 10.1109/ICEMS.2013.6713292.

[6] E. Gurpinar, D. De, A. Castellazzi, D. Barater, G. Buticchi and G. Francheschini, "Performance analysis of SiC MOSFET based 3-level ANPC grid-connected inverter with novel modulation scheme," 2014 IEEE 15th Workshop on Control and Modeling for Power Electronics (COMPEL), 2014, pp. 1-7, doi: 10.1109/COMPEL.2014.6877124.

[7] G. Zhang, Y. Yang, F. Iannuzzo, K. Li, F. Blaabjerg and H. Xu, "Loss distribution analysis of three-level active neutral-point-clamped (3L-ANPC) converter with different PWM strategies," 2016 IEEE 2nd Annual Southern Power Electronics Conference (SPEC), 2016, pp. 1-6, doi: 10.1109/SPEC.2016.7846157.

[8] Q. -X. Guan et al., "An Extremely High Efficient Three-Level Active Neutral-Point-Clamped Converter Comprising SiC and Si Hybrid Power Stages," in IEEE Transactions on Power Electronics, vol. 33, no. 10, pp. 8341-8352, Oct. 2018, doi: 10.1109/TPEL.2017.2784821.

[9] D. Zhang, J. He and S. Madhusoodhanan, "Three-Level Two-Stage Decoupled Active NPC Converter With Si IGBT and SiC MOSFET," in IEEE Transactions on Industry Applications, vol. 54, no. 6, pp. 6169-6178, Nov.-Dec. 2018, doi: 10.1109/TIA.2018.2851561.

[10] Infineon, “Some key facts about avalanche”, Application Note AN_201611_PL11_002, Version 1.0, 01.01.2017

[11] J. Dodge, “3L ANPC vs. 3L NPC Inverters”, UnitedSiC Application Note UnitedSiC_AN0023, February 2020

[12] Cree, Inc, Datasheet of C2M0045170P, 04-2018