Three-Phase Four-Wire Inverter for Grid Emulator under Wide Filter Inductance Variation

Tsai-Fu Wu, Yun-Hsiang Chang, Jui-Yang Chiu, Chang-Yang Chou and Chien-Chih Hung
Department of Electrical Engineering
National Tsing Hua University, Hsinchu, Taiwan
tfwu@ee.nthu.edu.tw

***Abstract*-- This paper proposes a new three-phase, four-wire grid emulator to simulate possible grid scenarios such as frequency and amplitude fluctuations and high harmonics. When using conventional PI and DDC, there is a phase difference between input and output response. Therefore, a modified DDC (MDDC) is adopted which can track the harmonic voltages precisely. The MDDC is dicussed in detail and the results are verified by simulations and real tests.**

I. INTRODUCTION

In recent years, energy issues have paid attention to everyone, and many experts have been engaged in the research of grid-connected converters. However, renewable-energy power generation systems are affected by seasonal and climatic conditions, and the power generation is not stable. When connected to the grid, it is very likely to cause grid failure and therefore, it needs grid emulator. Many experts have devoted themselves to the related research of power grid simulators [1]-[4],[8]-[10], which are used to simulate the actual power grid fault situation, such as voltage sudden change, frequency sudden change , high-order harmonic pollution, *etc*.

Traditionally, some power grid simulators use the architecture of three-phase three-wire converters [1], [4]. The three phases are coupled together, which is difficult to control and limits the scope of use. It needs to be converted from *abc* to *dq*, which consumes computing resources. References [2] and [11] adopted PR controller which can generate specific harmonics. Literature [8] uses a parallel architecture for repetitive control. [12] proposed model predictive control based on finite control set to simulate mains disturbance. [13] outlined and simulated the state of abnormal power grids. [14] proposed a modular multi-level converter to simulate the power grid containing high-order harmonics. However, the control methods in most papers are transferred from the *abc* domain to the *dq* domain or *αβ* domain, and the three-phase voltages are coupled together, so it is not easy to control individually.

Repetitive control has been intensively applied in industrial fields [15]-[22]. They can achieve zero-error tracking performance. In addition, digital repetitive controllers have simple structures configured by *N* delay units, where *N* is the number of samples in one repetitive period. Thus, a repetitive control is one of the most promising controls for grid emulators since repetitive ac voltages are required to be generated in these applications.

The repetitive control, however, has the limitations of transient response. Moreover, it cannot cover the inductance variation. The control [23] operating in *abc* frame can take into account the inductance variation. It uses only proportional (P) controller which yields significant steady state error. For grid-current control, the steady-state error is not quite important since the current command is variable. However, for the grid-voltage control, the steady-state error is very serious because of constant command.

In order to solve the above problems, this paper proposes a modified direct digital control (MDDC) to improve the steady-state error between input commands and output. The simulation and experimental results verify the proposed theory.

II. CONTROL ALGORITHM

Fig. 1 shows the power stage of a 3Φ4W voltage converter, where C_{fk} is the filter capacitance, L_{ik} is the filter inductance, where k represents the phase sequence {R, S, T}. With load current, capacitor voltage, inductor current and dc-voltage feedbacks, there are three types of controls:

A. Conventional PI Control

A conventional PI control algorithm without considering inductance drop is shown as follows:

$$C(s) = k_p + \frac{K_i}{s} \tag{1}$$

where k_p = 0.053 and k_i = 30. With the conventional PI control, because the inductance attenuation is not taken into account, it causes the output voltage to oscillate near the peak value.

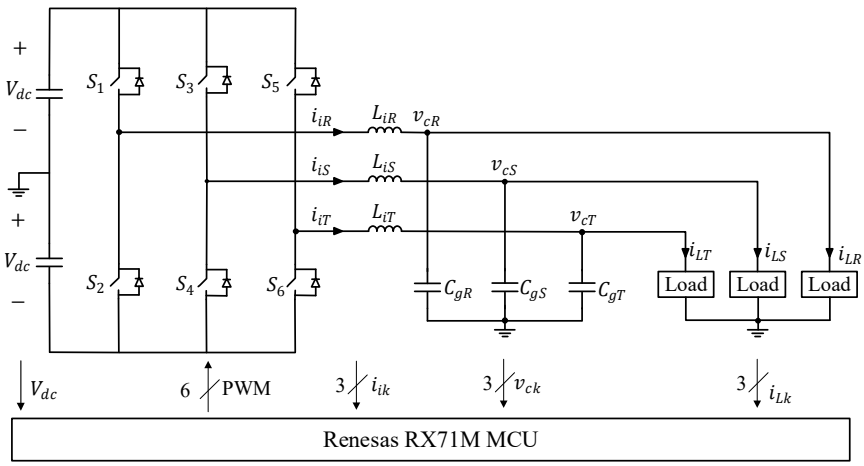


Fig. 1 Circuit configuration of a 3-phase 4-wire inverter.

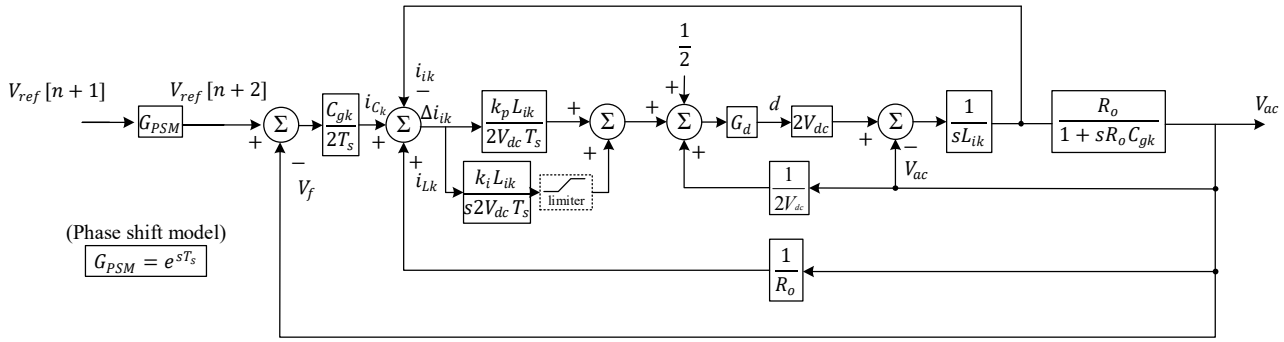


Fig. 2 Overall control block diagram of the modified DDC (MDDC) for each phase.

B. Conventional Direct Digital Control

A conventional direct digital control (DDC) algorithm has been proposed in [23] which takes the inductance drop into account and can improve the output voltage waveform, and is reviewed here for reference. The inner current loop control law of each phase can be derived as follows:

$$d_k = \frac{1}{2} + \frac{L_{ik}\Delta i_{ik}}{2V_{dc}T_s} + \frac{v_{ac}}{2V_{dc}} \tag{2}$$

where d is the duty ratio, V_{dc} is the dc-link voltage, T_s is the sampling period, v_{ac} is the output voltage and

$$\Delta i_{ik}[n+1] = i_{Ck}[n+1] + i_{Lk}[n] - i_{ik}[n] \tag{3}$$

where k denotes phase R, S and T, and

$$i_{Ck}[n+1] = C_{fk}\frac{V_{ref}[n+2] - v_f[n]}{2T_s} \tag{4}$$

The i_{Ck} is the estimated Capacitor Current, while the i_{Lk} and i_{ik} are the feedback values of load and converter side inductor current.

Combined with the outer voltage-loop, the overall control block diagram for each phase is shown in Fig. 2, in which k_i = 0 for DDC, C_{fk} is the filter capacitors, L_{ik} is the filter inductors, R_o is the load, and G_d is the delay which is equal to e^{-sT_s}.

C. Modified Direct Digital Control

Since the inner-current loop is only with proportional control ($\frac{L_{ik}}{2V_{dc}T_s}$), the steady-state error cannot be avoided. Thus, the inner-current loop is modified as follows:

$$d_k[n+1] = \frac{1}{2} + \frac{L_{ik}}{2V_{dc}T_s}\left(k_p\Delta i_{ik}[n+1] + k_i\sum_{k=0}^{n}\Delta i_{ik}[k]\right) + \frac{v_{ac}}{2V_{dc}} \tag{5}$$

where k_p = 1 and k_i = 760 are the proportional and integral gains, respectively. With the control law shown in (5) and the control block diagram shown in Fig. 2, the steady-state error of the output voltage can be effectively reduced.

III. Simulated and Experimental Results

The simulated results of a converter with a conventional PI control is shown in Fig. 3 (a). It can be observed that the output voltage waveform appears to oscillate around the peak value as the inductance value variation.

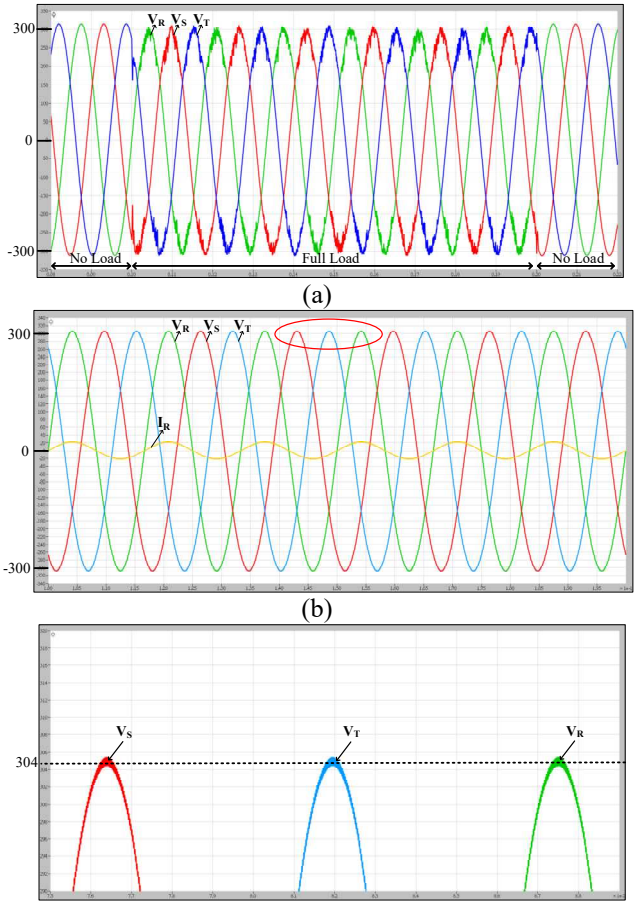


Fig. 3 Simulated results of output voltage waveforms with (a) a conventional PI controlled inverter, (b) the DDC, and (c) its zoom-in waveform.

TABLE I
SPECIFICATIONS AND DESIGN PARAMETERS

Symbol	Description	Value
V_{dc}	DC-bus voltage	$\pm$380V
v_C^*	Reference voltage (line-line)	311 V
f_{Line}	Output voltage frequency	60 Hz
f_{sw}	Switching frequency	20 kHz
L_{ik}	Inductance drop	$2mH \sim 1mH$
C_{gk}	AC filter capacitor	15 μF

While with the DDC, the output voltages present smoother waveforms as shown in Fig. 3(b) and its zoom-in waveforms are shown in Fig. 3(c). It can be seen that the steady-state error is still exist. Thus, we proposed MDDC, the one shown in Fig. 4(a) and the zoom-in waveforms is shown in Fig. 4(b), improved steady-state error.

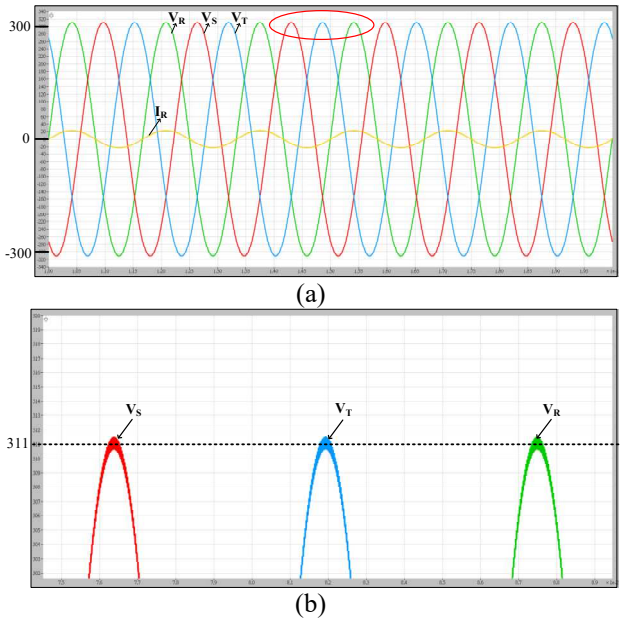


Fig. 4 Simulated results of the inverter with the MDDC: (a) original, and (b) zoom in.

For the system with a step-load change, the results are shown in Fig. 5, in which the black plot is the reference, the red plot is with a PI control, the green plot is the one with DDC, and the blue plot is the one with the MDDC. It can be seen that the blue one is closely tracking the reference and improve the steady-state error.

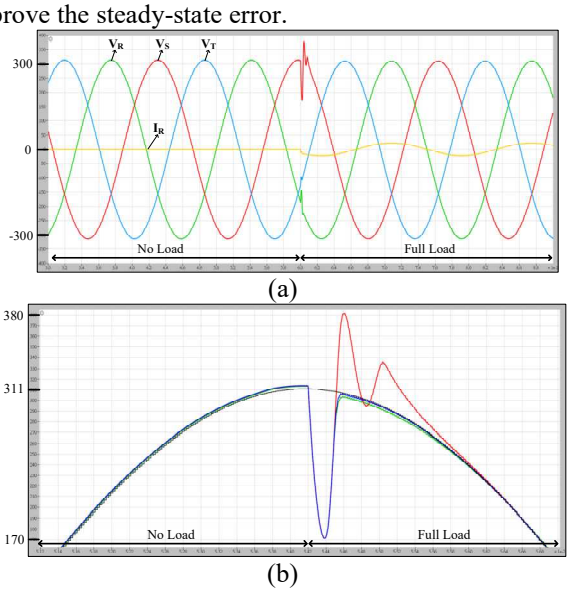


Fig. 5 Simulated results of the inverter with step-load change: (a) original, and (b) its zoom-in waveform.

Fig. 6(a) shows the measured results with the conventional PI control, and it can be seen from the figure that the waveform oscillates. Fig. 6(b) shows the one with DDC, and it can be seen from the figure that the waveform is smoother, but the steady-state error still exists. Fig. 6(c) shows the one with MDDC, and it shows the stable results and the steady-state error has been reduced a lot. It can prove that the proposed control scheme, MDDC, is stable and feasible.

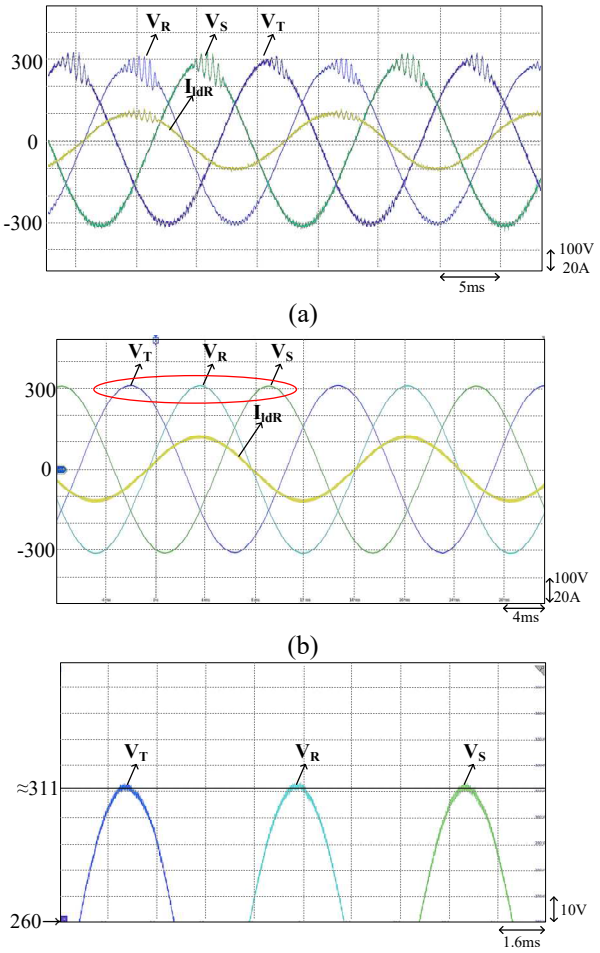


Fig. 6 Experimental results: (a) with a conventional PI control, (b) with DDC, and (c) with MDDC.

With a step-load change, Fig. 7 shows the experimental results with MDDC and without/with limiter, in which Fig. 7(a) is without limiter and Fig. 7(b) shows the one with limiter. The one with limiter shows less overshoot.

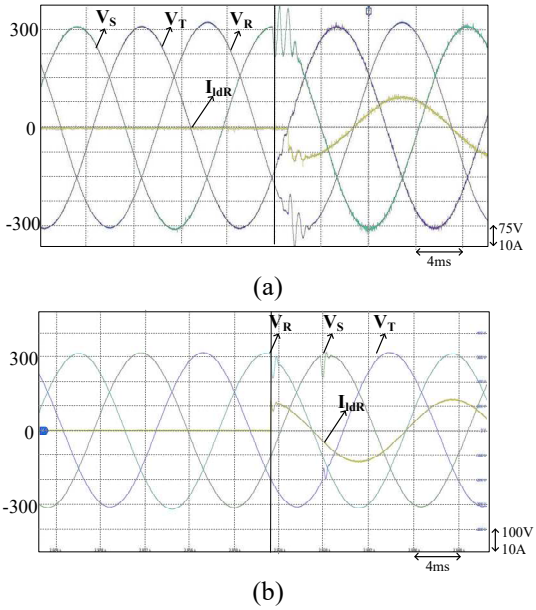


Fig. 7 Experimental results with MDDC control: (a) without limiter, and (b) with limiter.

Fig. 10(a) shows the waveforms under $10\%/7^{th}$ harmonic without angle compensation, while Fig. 10(b) shows that with angle compensation. The compensated angle is obtained from the bode plots of input-to-output transfer function (v_{ac}/v_{ref}) as shown in Fig. 11, where the 7^{th} harmonic frequency = 420 Hz and lagging angle = 10.70°. The compensation angle is selected to be leading angle = 9.15° (=10.70°-1.55°) since the fundamental frequency = 60 Hz whose lagging angle is 1.55°. The angle compensation can help track the references precisely and therefore, the voltage waveforms can be generated accurately even under distortion and can emulate grid voltage properly. The other harmonics can follow the same rule to adjust the compensated angles to achieve the accurate output waveforms.

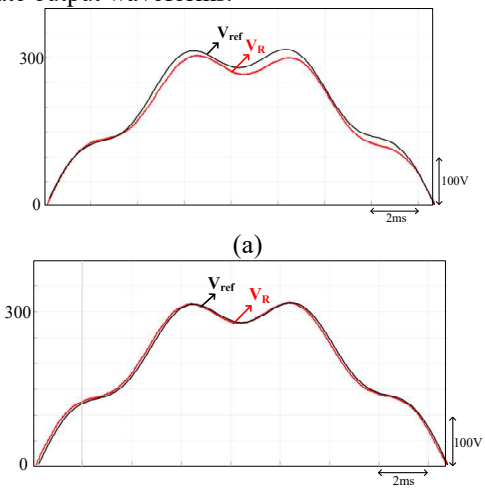
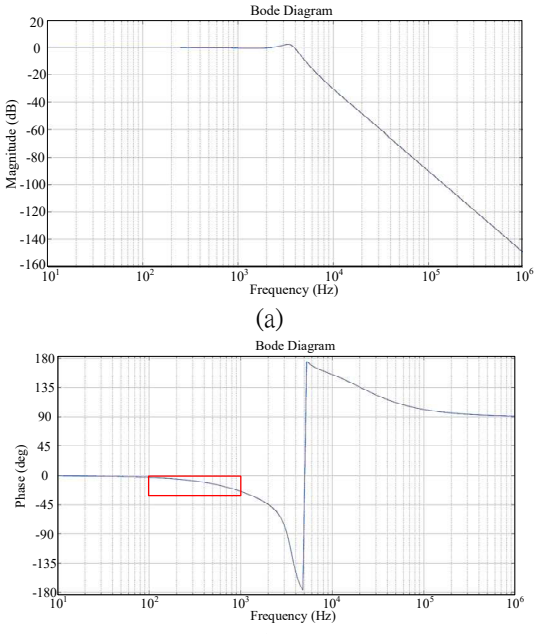
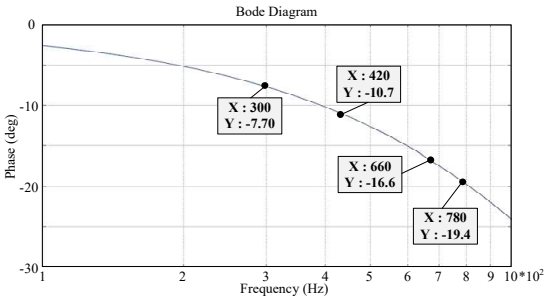


Fig. 7 Experimental waveforms under 10%/7th harmonic: (a) without angle compensation, (b) with angle compensation.





(c)

Fig. 8. Bode plots of the input-to-output transfer function (v_{ac}/v_{ref}) shown in Fig. 2: (a) the original plot, and (b) zoom-in plot of the red-box shown in (a).

The stability of the system can be confirmed through the loop gain. Fig. 9 is the loop gain Bode diagram of the control block diagram shown in Fig. 2. For heavy load (15 Ω) and light load (150 Ω), the phase margin is greater than 50°, and the gain margin is 5 dB. Therefore, the system is stable.

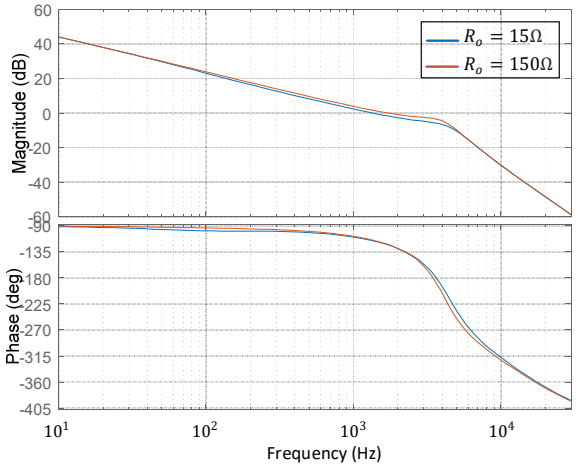
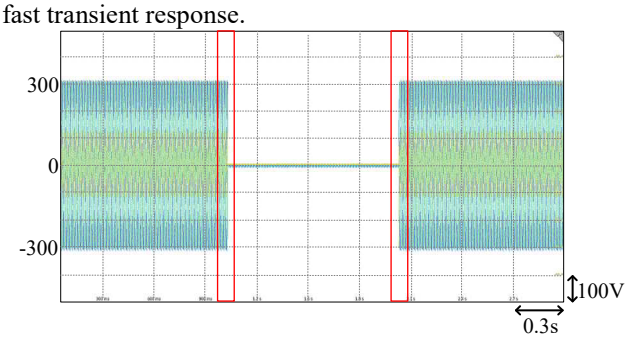
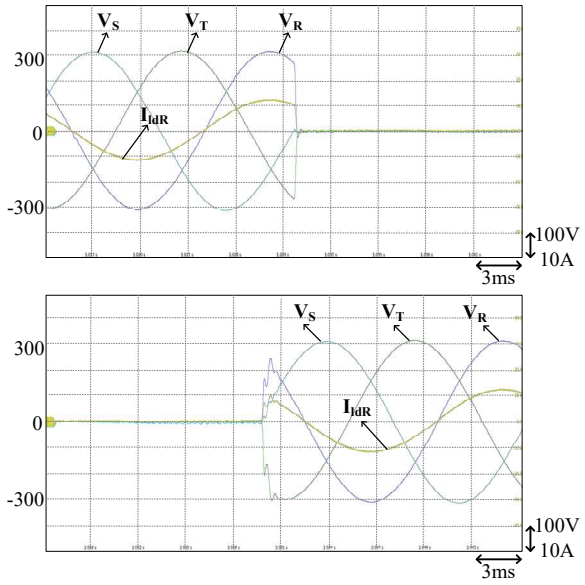


Fig. 9 Bode plots of loop-gain.

Next, we simulate the situation of grid short circuit. Fig. 10 shows the experimental waveforms, where Fig. 10(b) shows an enlarged view of the red box shown in Fig. 10(a). With the proposed control MDDC, it can be seen that the response time is within 0.5 ms under half load and achieve fast transient response.



(a)



(b)

Fig. 10 Experimental waveforms of three-phase voltage faults: (a) original and (b) zoom-in, showing the fast response.

Fig. 11 shows the situation of grid voltage flickering, in which a $220V_{rms}$ 60Hz three-phase voltage with sinusoidal flicker is generated. The amplitude variation is 5% of the main voltage and the flicker-frequency is 4 Hz. The figure can verify the effectiveness of the proposed grid emulator.

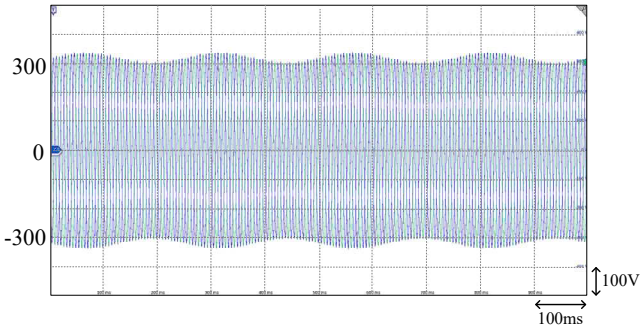


Fig. 11 Voltage flicker.

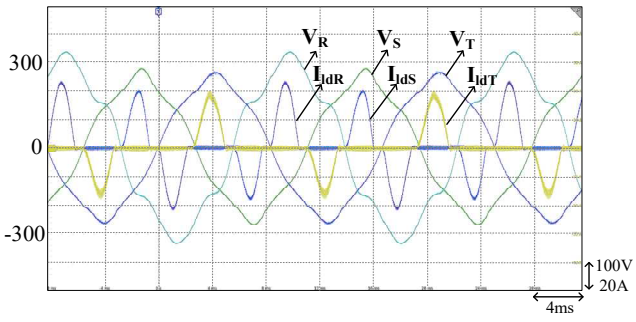


Fig. 12 Hybrid disturbance.

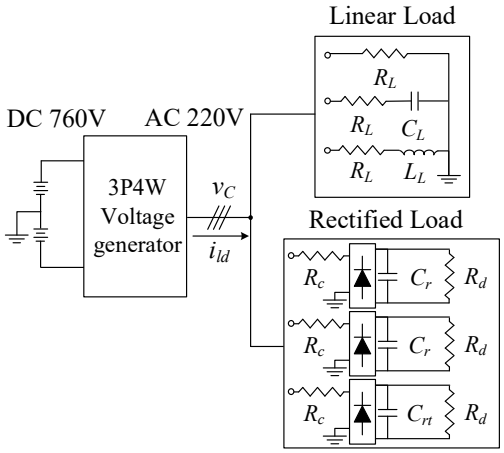


Fig. 13 The rectified load and linear load.

Hybrid disturbances, both voltage dips and harmonic distortion, are included in the main voltage. As shown in Fig. 12, V_R contains the 10%/5th order harmonic and 5%/7th order harmonic, V_S contains the 7%/5th order harmonic and 10% voltage sag at the mains, and V_T contains 5%/5th order harmonic and 10% voltage sag at the mains. The load type is a rectified load which is shown in Fig. 13. From the figure, we can observe the effectiveness of the proposed grid emulator. From the above discussions, the grid voltages can be emulated accurately and thus, it can be used to evaluate the performance of distributed generators.

IV. CONCLUSION

This paper has presented the inverter with MDDC which can achieve the desired outputs. With MDDC, the inductance-drop with bias current-increase has been taken into account; thus, it can avoid the oscillating waveforms and can reduce steady-state error to zero. Moreover, it can reduce voltage overshoot with limiter while step-load changes. In particular, it can compensate angle lagging to precisely track the harmonic references which can generate accurate distorted grid-voltages. The proposed control can achieve fast transient response while voltage faults. It is feasible to emulate grid voltage with the proposed modified direct digital control.

REFERENCES

[1] A. Karuppaswamy, S. Gulur and Vinod John, “A Grid Simulator to Evaluate Control Performance of Grid-Connected Inverters,” *IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, 2014, pp. 103-108.

[2] J. Eloy-Garc´ıa, J. C. Vasquez, and J. M. Guerrero, “Grid simulator for power quality assessment of micro-grids,” *IET Power Electron.*, vol. 6, no. 4, pp. 700–709, 2013.

[3] Nakul Narayanan K and L Umanand, “A Virtual Impedance Based Grid Emulator for the Performance Analysis of Distributed Generations,” the IEEE Applied Power Electronics Conference and Exposition (APEC), 2019, pp. 3013-3018.

[4] Guangye Si and Ralph Kennel, “Comparative Study of PI Controller and Quadratic Optimal Regulator Applied for a Converter Based PHiL Grid Emulator,” *IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, 2016, pp. 1-8.

[5] Yaowei Hu, Jingling Cheng, You Zhou and Guozhu Chen, “Control Strategy of a High Power Grid Simulator for the Test of Renewable Energy Grid Converter.” the 43rd Annual Conference of the IEEE Industrial Electronics Societ *(IECON)*, 2017, pp. 7747-7752.

[6] E. Duymaz, S. Pourkeivannour, D. Ceylan, İ. Şahin, and O. Keysan, “Design of a Power Plant Emulator for the Dynamic Frequency Stability Studies,” XIII International Conference on Electrical Machines (ICEM), 2018, pp. 152-157.

[7] Ming Jia , Nurhan Rizqy Averous and Rik W. De Doncker, “Evaluation and Comparison of Different Topologies for a Grid Emulator,” IEEE 22nd Workshop on Control and Modelling of Power Electronics (COMPEL), 2021, pp. 1-8.

[8] Tianqi Liu, Danwei Wang and Keliang Zhou, “High-Performance Grid Simulator Using Parallel Structure Fractional Repetitive Control,” *IEEE Trans. Power Electronics*, Vol. 31, no. 3, March 2016, pp. 2669-2679.

[9] N. Kim, S.-Y. Kim, H.-G. Lee, C. Hwang, G.-H. Kim, H.-R. Seo, M. Park, and I.-K. Yu, “Design of a grid-simulator for a transient analysis of grid-connected renewable energy system,” *Proc. Int. Conf. Electr.*, Mach. Syst., 2010, pp. 633–637.

[10] Tuomas Messo, Roni Luhtala, Tomi Roinila, *et al.*, “Using High-Bandwidth Voltage Amplifier to Emulate Grid-Following Inverter for AC Microgrid Dynamics Studies,” *the Energies*, 2019, pp. 1-8.

[11] Han Rong, Xu Qianming*, Chu Xu, Ding Hongqi, and Xiong Qiaopo, “Model Predictive Control of Modular Multilevel Grid Simulato,“ *APPEEC 2019*, pp. 1-6.

[12] T. Liu and Z. Xiao, "Finite control set model predictive control strategy of grid simulator for the test of renewable energy system and motor driver," 8th Renewable Power Generation Conference (RPG 2019), 2019, pp. 1-5, doi: 10.1049/cp.2019.0574.

[13] Y. Han, Y. Feng, P. Yang, L. Xu, Y. Xu and F. Blaabjerg, "Cause, Classification of Voltage Sag, and Voltage Sag Emulators and Applications: A Comprehensive Overview," in IEEE Access, vol. 8, pp. 1922-1934, 2020, doi: 10.1109/ACCESS.2019.2958965.

[14] M. Jia, S. Cui, P. Joebges and R. W. D. Doncker, "A Modular Multilevel Converter as a Grid Emulator in Balanced and Unbalanced Scenarios Using a Delta-Wye Transformer," 2021 IEEE Energy Conversion Congress and Exposition (ECCE), 2021, pp. 2950-2957, doi: 10.1109/ECCE47101.2021.9595175.

[15] A. Garcia-Cerrada, O. Pinzon-Ardila, V. Feliu-Batlle, P. Roncero-Sanchez, and P. Garc´ıa-Gonzalez, “Application of a repetitive controller for a three-phase active power filter,” *IEEE Trans. Power Electron.*, vol. 22, no. 1, pp. 237–246, Jan. 2007.

[16] C. Rech, H. Pinheiro, H. A. Grundling, H. L. Hey, and J. R. Pinheiro, “Comparison of digital control techniques with repetitive integral action for low cost PWM inverters,” *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 401–410, Jan. 2003.

[17] Y.-Y. Tzou, S.-L. Jung and H.-C. Yeh, “Adaptive repetitive control of PWM inverters for very low THD AC-voltage regulation with unknown loads,” *IEEE Trans. Power Electron.,* vol. 14, no. 5, pp. 973–981, Sep. 1999.

[18] R. Cardenas, R. Pena, J. Clare, P. Wheeler, and P. Zanchetta, “A repetitive control system for four-leg matrix converters feeding non-linear loads,” *Electr. Power Syst. Res.*, vol. 104, pp. 18–27, 2013.

[19] B. Zhang, K. Zhou, and D. Wang, “Multi-rate repetitive control

for PWM DC/AC converters," *IEEE Trans. Ind. Electron.*, vol. 61, no. 6, pp. 2883–2890, Jun. 2014.

[20] W. Lu, K. Zhou, D. Wang, and M. Cheng, "A generic digital nk±m-order harmonic repetitive control scheme for PWM converters," *IEEE Trans. Ind. Electron.*, vol. 61, no. 3, pp. 1516–1527, Mar. 2014.

[21] W. Lu, K. Zhou, D. Wang, and M. Cheng, "A general parallel structure repetitive control scheme for multiphase DC–AC PWM converters," *IEEE Trans. Power Electron.*, vol. 28, no. 8, pp. 3980–3987, Aug. 2013.

[22] G. Escobar, P. G. Hernandez-Briones, P. R. Martinez, M. Hernandez Gomez, and R. E. Torres-Olguin, "A repetitive-based controller for the compensation of $6l \pm 1$ harmonic components," *IEEE Trans. Ind. Electron.*, vol. 55, no. 8, pp. 3150–3158, Aug. 2008.

[23] T.-F. Wu, Y.-H. Huang, S. Temir, and C.-C. Chan, "3Φ4W Hybrid Frequency Parallel Uninterruptable Power Supply for Reducing Voltage Distortion and Improving Dynamic Response," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, p.1-13, July 2021.