Measurement results of Multilevel Hysteresis Control for paralleled Two-Level Converters

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Keywords

≪Converter control≫, ≪DC-AC converter≫, ≪Interleaved converters≫, ≪Parallel operation≫, ≪Wind energy≫

Abstract

The multilevel hysteresis control strategy was adjusted to four paralleled two-level converters. Simulations were done to compare it with uncoordinated hysteresis control and current control with pulse width modulation. Although this novel control strategy has its greatest advantages for several parallel converters and was originally designed for 14 parallel converters, the results for four converters are still significantly better than state of the art hysteresis cotrol. Furthermore, a test bench with four paralleled converter was build up to prove the simulation results.

Introduction

Paralleled two-level converters can be used to increase the power rating of grid-side converters. The redundancy is advantageous in case of converter failures, too. Moreover, different control strategies can reduce the switching losses and the Total Harmonic Distortion (THD) of the output current. Uncoordinated hysteresis control and PI current control with flattop pulse width modulation (PWM) and interleaved carrier signals are state of the art and widely used in industry [1]. The most significant advantage of hysteresis control is the fast dynamic response, but depending on the hysteresis bandwidth, either switching losses are high, or power quality is poor. In contrast, PI current control is slow but characterized by a high quality of the grid current [1, 2]. In [3] a novel control concept, called multilevel hysteresis control, is introduced for 14 paralleled converters. It is based on a multilevel hysteresis modulator and combines the benefits of a fast dynamic response and a low THD. The coordinated hysteresis control is adjusted to four paralleled inverters, and a test bench was designed to prove the simulation results. The paper is structured as follows: The first part explains the theoretical control concept. In the second part, the coordinated and uncoordinated hysteresis control simulation results are compared with PI current control. The test bench and the measurement results are shown in the third part.

General Concept of Multilevel Hysteresis Control with Current Balancing

The system consists of four parallel converters that are sharing one DC-link (Fig. 1). They are connected via chokes L at the AC-side, and at the Point of Common Coupling (PCC), the sum of the individual converter currents $i_{a1}, i_{b1}, i_{c1}, ..., i_{a4}, i_{b4}, i_{c4}$ gives the grid currents i_a, i_b, i_c. The currents i_a, i_b, i_c are fed via a transformer into the grid. The transformer is modeled with the inductances, L_T, and a constant voltage source provides the DC-link voltage. These four converters can be operated as a multilevel converter with $4+1$ voltage levels [4].

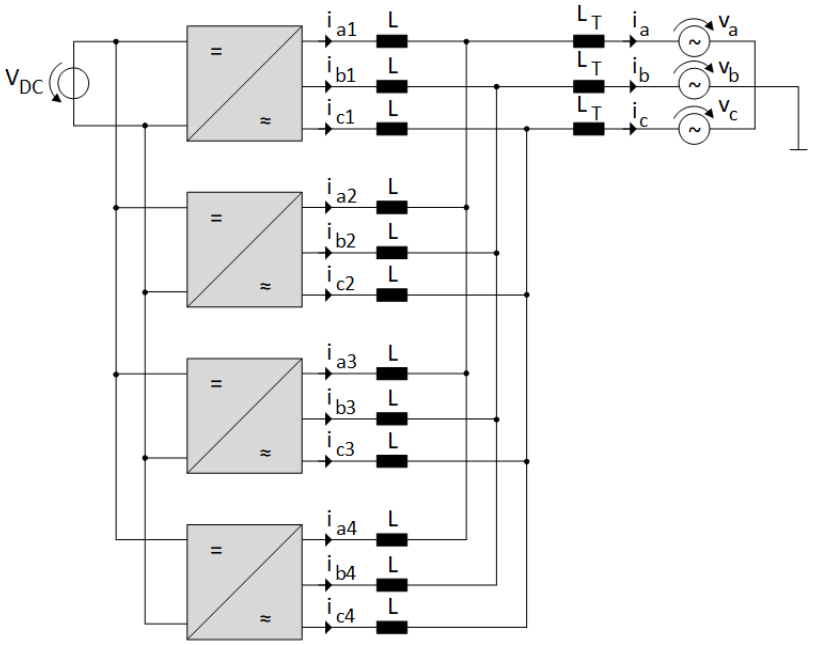

Fig. 1: Structure of the simulated system

The control concept is shown in Fig. 2. The grid current is controlled in the rotating dq-reference frame with Proportional (P) controllers to avoid windup because of the discrete output values of the following hysteresis controller. The angle θ of the measured voltage v_m is used to transform the DC-values into the three-phase abc system and vice versa. The sum v_i of the measured voltages v_m and the required voltage across the chokes v_F are the multilevel hysteresis modulator's input. The output of the multilevel hysteresis modulator is the desired voltage level k. This voltage level can be generated with multiple switching states of the parallel converters. Therefore, it is necessary to choose the optimal switching state. This happens in dependence of the individual current. To reach a one step higher voltage level, the converter with the lowest individual current is switched on and to reach a lower voltage level, the converter with the highest individual current is switched off.

Simulations have shown that this kind of balancing is insufficient to keep the individual currents in a specified band. Therefore, an additional balancing is implemented in the state machine without affecting the actual voltage level k. This concept switches the on/off state of the converter with the highest phase current and the converter with the lowest phase current (explained in detail in [3]). If it is impossible to switch converters because all four are on respectively off, the balancing must change the voltage level. For protection reasons, the individual current must be limited, which can disturb the voltage level, too. This is a real drawback, if only four parallel converters are used, because a state where all converters are switched on respectively off is reached more often than with 14 paralleled converters.

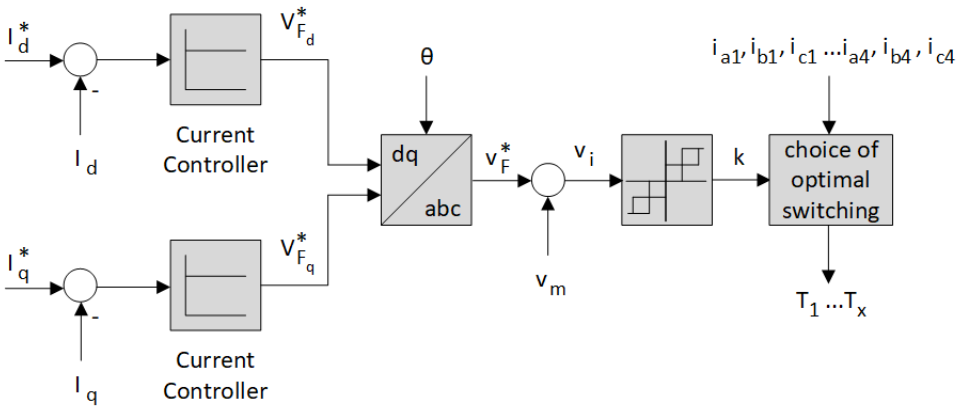

Fig. 2: Multilevel Hysteresis Control with Current Balancing

Simulation Results of Multilevel Hysteresis Control with Current Balancing

The grid-side converter of a wind-energy plant with a nominal power of $P_n = 4.26\,\mathrm{MW}$ was modelled. For nominal power (pure active power) the reference output current is $i_d^* = 4638\,\mathrm{A}$ and $i_q^* = 0\,\mathrm{A}$. To reduce the converter losses, the DC-link voltage is set to the minimal needed voltage with a reserve of 5 % [5]. To calculate the converter losses, the electrical parameters of the traction converter FF1800XTR17T2P5 are used.

The gain of the P controller for d- and q-current and the hysteresis bandwidth i_{diff} influence the performance of the current control, with a higher controller gain, the dynamic increases. However, the switching frequency and the switching losses increase, too. The smaller the hysteresis bandwidth, the smaller is the current error, and the THD decreases, but the switching frequency respectively the switching losses will increase. To find the pareto optimal outcome the P gain was varied between 1 and 4 and the current hysteresis bandwidth between 1000 A and 1100 A. The results are plotted in the pareto chart of Fig. 3. The pareto optimum was defined as the smallest distance to coordinate origin.

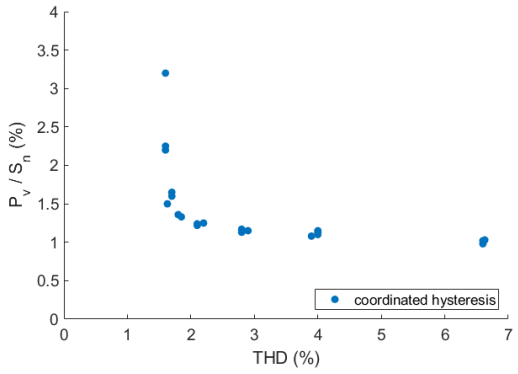

Fig. 3: pareto chart for multilevel hysteresis control

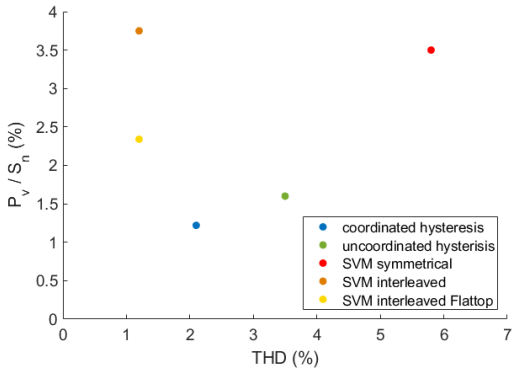

Fig. 4: comparison of different current control and modulation strategies

In Fig. 4 the pareto optimum of coordinated multilevel hysteresis control (blue) is compared with the pareto optimum of uncoordinated hysteresis control (green) and the converter losses and THD of the output current for PI current control with different PWM strategies. PWM strategies (red) can be optimezed by use of interleaved switching, which leads to a better THD (orange) and Flattop Space Vector Modulation, which saves additionally round about one third less losses (yellow). However, multilevel

control can reduce the THD of the output current as well as the converter losses, too. Of course, this effect is even higher for more paralleled converters but is still significant for four paralleled converters.

Measurement Results of Multilevel Hysteresis Control with Current Balancing

The test bench is shown in 5 and 6. It consists of ten paralleled back-to-back converters with identical parameters. The shared DC-link has a nominal voltage of $V_{DC} = 50\,\mathrm{V}$ and a maximum voltage of $V_{DCmax} = 80\,\mathrm{V}$. The nominal current of each converter is $i_n = 5\,\mathrm{A}$ and the maximum current is $i_{max} = 15\,\mathrm{A}$. The thermal design is for a switching frequency of $f_s = 5000\,\mathrm{Hz}$.

Fig. 7 shows the measurement results of a setup with four paralleled converters. The reference output current is $i_d^* = 28\,\mathrm{A}$. At $t = 36\,\mathrm{ms}$ a step in the set point i_d^* from 100 % to 50 % of the current occurs. The maximum allowed current difference is chosen to $i_{diff} = 5\,\mathrm{A}$. The measurement results prove the excellent dynamical behaviour of the multilevel hysteresis control. The measured current follows the reference value nearly instantaneously without any overshoot and the current limits are not exceeded.

Fig. 5: Test bench:
DC-link, filter and grid

Fig. 6: Test bench:
converter

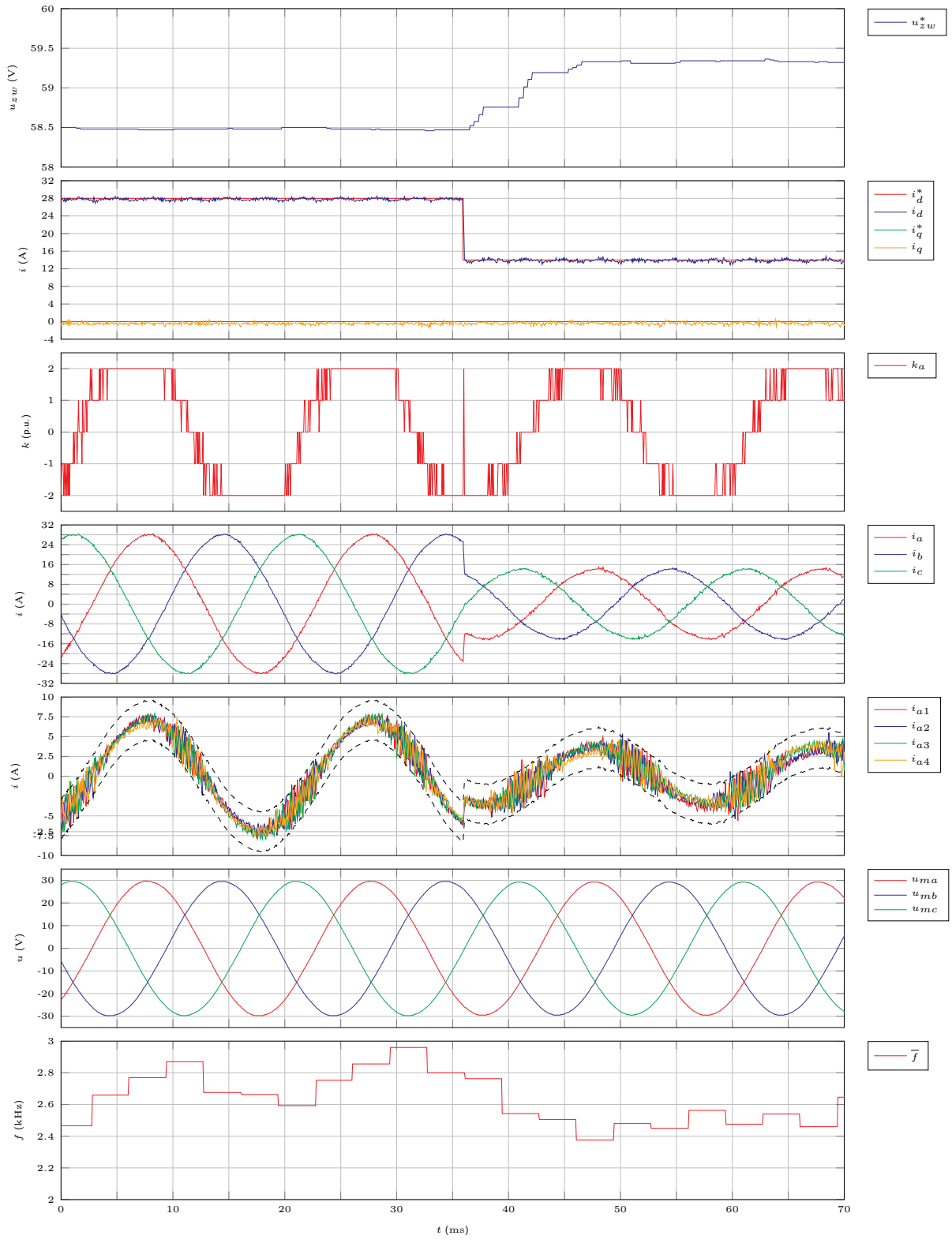

Fig. 7: step in the reference current

Conclusion

The coordinated multilevel hysteresis control strategy was adjusted to four paralleled two-level converters. Simulation results are promising. The THD of the output current, as well as the overall losses of the converter, are minimized. Furthermore, the fast dynamic response of the coordinated multilevel hysteresis control is comparable with the excellent dynamic behaviour of conventional hysteresis control. A

test bench was built, which confirms the expected advantages. This novel current control and modulation strategy can be used for every converter control strategy with an inner current control loop, and it is not limited to grid- side converters with state of the art grid-feeding control concepts.

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