Influence of Power Semiconductor Device Variations on Pulse Shape of Nanosecond Pulses in a Solid-State Linear Transformer Driver

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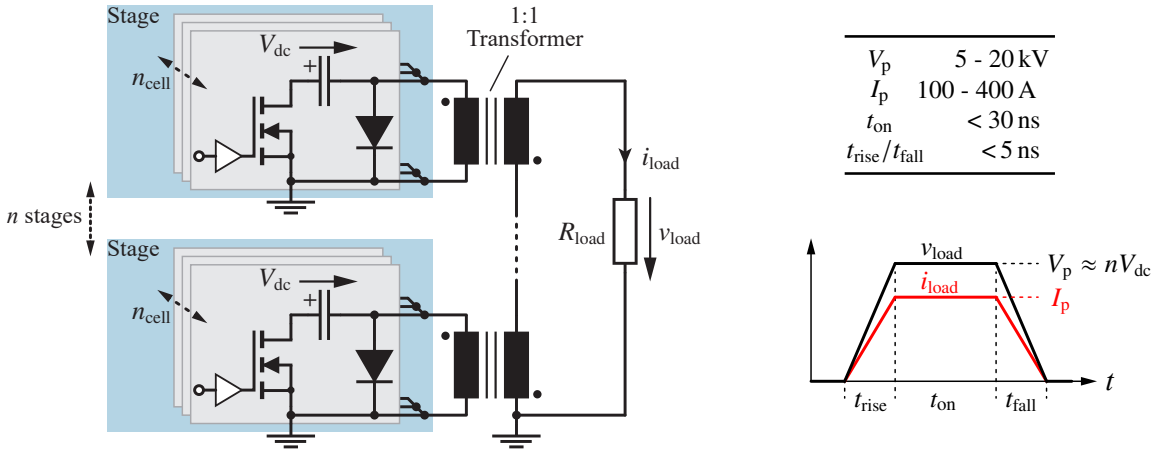
Abstract

Power semiconductors show a significant variation in their electrical characteristics attributed to fluctuations during their fabrication process. This can lead to critical voltage and current imbalances in ultra-fast switching multi-cell topologies/pulse generators. This paper explores this problem based on a statistical model of a SiC MOSFET and Monte-Carlo simulations.

1 Introduction

Silicon carbide (SiC) MOSFETs with high breakdown voltages ($> 1.2\,\mathrm{kV}$) are increasingly used in new pulse generator designs [1], [2]. One reason for this is the fast switching speed of SiC MOSFETs, which enables the generation of very short high-voltage pulses with pulse widths of only a few nanoseconds. Such short pulses could not be achieved with silicon-based IGBT devices in the past. Pulse generators with nanosecond high-voltage pulses are used in various fields, such as the generation of transient plasmas or in injection/extraction systems of particle accelerators.

To achieve high output voltages of several kilovolts, multi-cell topologies such as the solid-state Marx generator [3] or the linear transformer driver (LTD) [4], as depicted in Fig. 1(a), are frequently used. In these topologies, many devices are typically connected in series and/or in parallel. Differences in the characteristics (as e.g. current characteristics, device capacitances or internal gate resistance) of the devices — mainly caused by tolerances during the fabrication process of the semiconductor chips [5] — lead to an unsynchronized switching of the devices. This results in imbalanced device voltages and currents that might eventually cause device failures due to overcurrents in some devices.



(a) (b)

Fig. 1: (a) Solid-state LTD consisting of n series-connected stages. Each stage has n_{cell} SiC MOSFETs connected in parallel. (b) Pulse specifications of the target design.

The influence of device mismatches is even more pronounced when the individual SiC MOSFETs are operated at very high switching speeds. This is often necessary in very fast pulse applications in order to be able to meet the demanding pulse specifications. Therefore, besides harmful voltage and current imbalances, potential device mismatches can also have a significant impact on the output voltage pulse shape. For very fast pulse generators, the achievable rise and fall times of the output pulse are typically of primary interest.

In order to compensate for steady-state and transient imbalances, passive or active synchronization methods can be employed [6]–[9]. However, these methods are limited in their bandwidth and their operation is prone to malfunctioning at very fast switching speeds due to the large influence of parasitics. In addition, they usually slow down the switching speed of the SiC MOSFETs. Hence, these methods are generally not applicable for pulse generators, that aim for ultrafast nanosecond switching times.

Having only very limited possibilities to actively influence the balancing of device voltages and currents, it is crucial to be able to estimate the influence of device variations on the circuit performance. Missed performance goals or potential risks for device failures can be addressed by pre-screening semiconductor chips [10] and defining boundaries for the maximum allowed spread in the device characteristics.

Characteristic measurements of a large number of SiC MOSFETs showing the approximate range of device variations as well as methods for systematically analysing the variations are discussed in [10]–[12]. Methods to statistically analyse device variations are developed in [13], [14], primarily focusing on the current characteristics of the MOSFET. Furthermore, the effects of device variations on the current distribution of parallel-connected SiC MOSFETs are analysed. In [15], a basic analysis of the transient current waveforms is carried out. [16] investigates the unequal switching losses of parallel-connected SiC MOSFETs and the resulting thermal imbalances using statistical methods.

However, an analysis of the current and voltage distribution in multi-cell topologies with several mismatched SiC MOSFETs connected in series and/or parallel is missing. Especially when the switches are operated at very high switching speeds. Therefore, this paper investigates the behaviour of a multi-cell topology, using the example of the solid-state LTD illustrated in Fig. 1(a), under the influence of device variations of SiC MOSFETs. The parametrisation and target specifications of the load pulse are shown in Fig. 1(b). The focus is on the achievable output voltage switching times t_{rise} and t_{fall} and their dependence on the device variations.

Estimating the circuit performance under the influence of device variations requires statistical modelling of the device properties. The statistical modelling approach presented in this paper consists of three steps. First, a suitable device model for the SiC MOSFET is selected. A behavioural model is chosen since only the terminal behaviour of the MOSFET is of interest. In a second step, the variation of the device properties is statistically modelled. This is done based on measurements of different SiC MOSFET samples. In the last step, the statistical models of the SiC MOSFET are implemented in a circuit simulation and Monte Carlo (MC) simulations are performed to investigate the circuit performance of the LTD under the influence of varying device characteristics.

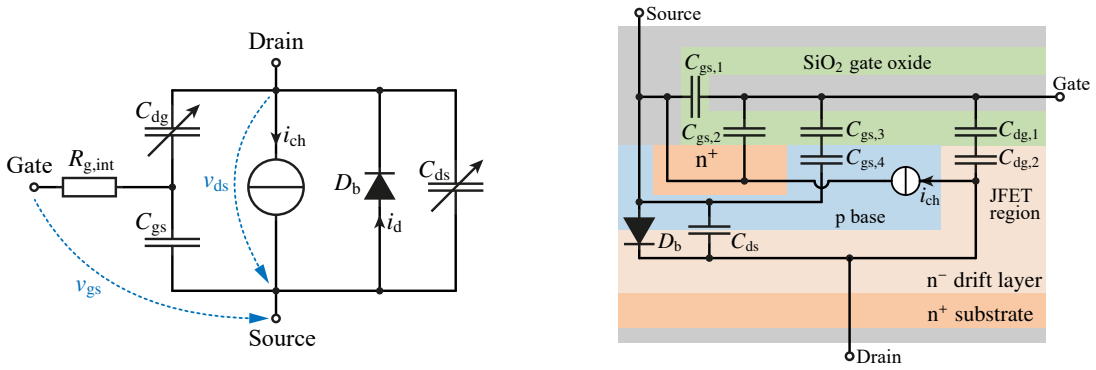
Section 2 of this paper explains the selected behavioural device model for the SiC MOSFET. The statistical modelling of the SiC MOSFETs is described in 3. Finally, section 4 presents the results of the Monte-Carlo simulations.

2 Behavioural Device Modelling of SiC MOSFET

Since only the terminal behaviour of the MOSFET is of interest, a behavioural model is chosen. In behavioural models, the underlying equations only model the electrical behaviour of the SiC MOSFET at its terminals. The equations do not directly describe the physical mechanisms by which the MOSFET operates. The basis for the modelling is usually a series of measurements of the current-voltage behaviour and the impedance behaviour at the terminals of the MOSFET. Based on these measurements, the parameters of the model equations can be determined in such a way that the resulting model behaviour closely matches the measurement curves.

Fig. 2(a) shows the behavioural SiC MOSFET model used in this paper. It contains the following submodels: The voltage-controlled current source i_{ch}, the voltage-dependent capacitances C_{gs}, C_{dg} and C_{ds}, the internal gate resistance $R_{\mathrm{g,int}}$ and the body diode D_{b}.

The electrical behaviour of the submodels is described based on mathematical functions. In this context, four categories of mathematical functions can be distinguished [17]: Continuous functions, segmented functions based on case distinctions, look-up tables or combinations of the three. Due to the large number of simulations required for the statistical investigation in this work, good/fast convergence and short simulation times of the model are



(a) (b)

Fig. 2: (a) Behavioural SiC MOSFET model consisting of: Voltage-dependent current source i_{ch}, voltage-dependent device capacitances C_{gs}, C_{ds} and C_{dg}, internal gate resistance $R_{g,int}$ and body diode D_b. (b) Cell structure of a planar SiC MOSFET indicating the submodels of the behavioural model.

important. Segmented functions and look-up tables tend to have worse convergence properties than continuous functions [17]. Therefore, continuous functions are used in the following.

In addition, the main focus of this paper is on the simulation of very short voltage pulses. Therefore, the self-heating of the switch is neglected. As a consequence, the temperature dependence of the switch characteristics is not modelled and only the switch characteristics at room temperature $T \approx 25\,^{\circ}\mathrm{C}$ are considered.

2.1 Voltage-Controlled Current Source

The channel current i_{ch} of the MOSFET is mainly determined by the applied gate-source voltage v_{gs} and the drain-source voltage v_{ds}. Accordingly, the current function is formulated as a function of these two voltages. The continuous equation (1) is used, which is presented in [18]. It approximates the static current characteristics of the device using the fitting parameters $k_1 - k_{10}$. Essentially, the model equation consists of a multiplication of the terms $i_{ds,tran}$ and $i_{ds,out}$. The term $i_{ds,tran}$ describes the transfer characteristics and the term $i_{ds,out}$ models the output characteristics of the SiC MOSFET.

$$i_{ch}(v_{ds}, v_{gs}) = i_{ds,tran} \cdot i_{ds,out} = \underbrace{k_1 \left[1 + \tanh\left(k_2(v_{gs}+k_3) + k_4(v_{gs}+k_5)^2\right)\right]}_{i_{ds,tran}} \cdot \underbrace{\frac{p(v_{gs})v_{ds}}{1+q(v_{gs})v_{ds}}}_{i_{ds,out}} \tag{1}$$

The parameters $p(v_{gs})$ and $q(v_{gs})$ are exponential functions defined by (2) and (3). They are added to the current equation in order to take into account the dependency of the output characteristics on the gate-source voltage v_{gs}. As a result, a better fit of the output characteristics can be achieved. Compared to the original equation in [18], the fitting parameter multiplied with the exponential function in (2) is omitted because this parameter is not independent of the other fitting parameters and therefore, does not influence the resulting fitting curve.

$$p(v_{gs}) = \exp(k_6 v_{gs}) + k_7 \tag{2}$$

$$q(v_{gs}) = k_8 \exp(k_9 v_{gs}) + k_{10} \tag{3}$$

2.2 Device Capacitances

The gate oxide and the p-n junctions within a MOSFET cell result in distributed capacitances as shown in Fig. 2(b). These capacitances are charged and discharged during each switching operation. Thus, they also have a major influence on the switching behaviour and have to be taken into account for the transient modelling of the SiC MOSFET in addition to the current characteristics.

The distributed capacitances are typically modelled by the three lumped capacitances C_{gs}, C_{dg} and C_{ds}. The distributed capacitances can be related to the lumped capacitances as follows: $C_{gs} = C_{gs,1} + C_{gs,2} + C_{gs,3} + C_{gs,4}$ and $C_{dg} = C_{dg,1} + C_{dg,2}$ [19].

The capacitances C_{dg} and C_{ds} are largely dependent on the p-n junctions within the MOSFET cell. As a result, the capacitance values of C_{dg} and C_{ds} strongly decrease with larger reverse voltage because the widths of the

depletion regions increase. In addition, both capacitance curves, but especially the capacitance curve of C_{dg}, show two different decay rates at low reverse voltages. This is caused by different doping concentrations in the JFET and the drift region of the MOSFET, resulting in two different expansion rates of the depletion region [20].

The decreasing characteristics in the capacitance curves of C_{dg} and C_{ds} are modelled by a sum of exponential functions with negative exponents. The sudden change of decay rates at low voltages is modelled by an additional sum of inverse exponential functions. In summary, (4) is used to model the capacitance curves of C_{dg} and C_{ds}.

$$C(v_{\mathrm{ds}}) = \sum_{i=1} a_i \mathrm{e}^{b_i v_{\mathrm{ds}}} + \sum_{j=1} \frac{c_j}{1+\mathrm{e}^{d_j(v_{\mathrm{ds}}-e_j)}} + f \tag{4}$$

In contrast to C_{dg} and C_{ds}, the gate-source capacitance C_{gs} is mainly determined by the oxide capacitance. This value is largely independent of the drain-source voltage and is therefore assumed to be constant.

2.3 Gate Resistance & Body Diode

A lumped gate resistor $R_{\mathrm{g,int}}$ is used to model the distributed resistance of the gate structure of the SiC MOSFET. Furthermore, the Shockley equation in (5) is used to model the current behaviour of the body diode.

$$i_{\mathrm{d}}(v_{\mathrm{sd}}) = I_{\mathrm{s}} \left(\mathrm{e}^{(v_{\mathrm{sd}}-R_{\mathrm{s}} i_{\mathrm{d}})/N V_{\mathrm{T}}} - 1 \right) \tag{5}$$

The fitting parameters are: The saturation current I_{s}, the series-resistance R_{s} and the emission coefficient N. V_{T} is the thermal voltage at $T = 25\,^{\circ}\mathrm{C}$.

2.4 Fitting of Model Parameters

A series of static current measurements and impedance measurements at different values of v_{gs} and v_{ds} are used to fit the model parameters. In order to achieve high model accuracy over the entire operating range, the measurement points used for fitting the model parameters should also cover the entire operating range. However, this raises an issue regarding the measurement of the static current characteristics. At higher drain-source voltages, the self-heating of the MOSFET distorts the measurement results. For this reason, the current characteristics is only measured up to a maximum drain-source voltage of 10 V. To increase the modelling accuracy over the whole operating range, the measurement range of the curve tracer would need to be extended, e.g. by the method explained in [21].

The fitting of the model parameters to the measurement curves represents a non-linear optimisation problem that is solved using the least squares method. Specifically, the Nelder-Mead simplex algorithm is applied to find a solution to the minimisation problem in (6).

$$\min_{\boldsymbol{p}} \| y_{\mathrm{m}}(\boldsymbol{p}, \boldsymbol{v}) - \boldsymbol{y}_{\mathrm{meas}} \|_2^2 \tag{6}$$

Here, y_{m} represents the model functions (1)–(5), each consisting of $\boldsymbol{p}$ modelling parameters. $\boldsymbol{y}_{\mathrm{meas}}$ are the measurements of the modelled quantities at the measurement voltages $\boldsymbol{v}$.

2.5 Model Implementation in Circuit Simulation

SPICE is used to implement the circuit model. The current equation (1) is implemented based on a voltage-dependent current source. Regarding the implementation of voltage-dependent capacitances in SPICE, there have been various methods presented in literature [22]. With respect to a capacitance-based implementation, there are two general ways: Either using the intrinsic *ddt* function in SPICE, which calculates the discrete time derivative of the capacitor voltage, or using the intrinsic voltage-current relation of a capacitance. Using the intrinsic voltage-current relation of a capacitance has several advantages, which are summarized in [22]. Therefore, this method is chosen. It is shortly described in the following.

The circuit for modelling a voltage-dependent capacitance is depicted in Fig. 3. It consists of a controlled current source G_C, a voltage-controlled voltage source E_C and a reference capacitance C_{ref}. C_{ref} is used to generate the time derivative of the capacitor voltage. The capacitance current i_C is directly determined by G_C, which is equal to the reference current i_{ref} multiplied by the expression $C(v_C)$ for the capacitance. Furthermore, choosing E_C to be equal to v_C/C_{ref} results in equation (7).

$$i_C = G_C = C(v_C) i_{\mathrm{ref}} = C(v_C) C_{\mathrm{ref}} \frac{\mathrm{d}E_C}{\mathrm{d}t} = C(v_C) \frac{\mathrm{d}v_C}{\mathrm{d}t} \tag{7}$$

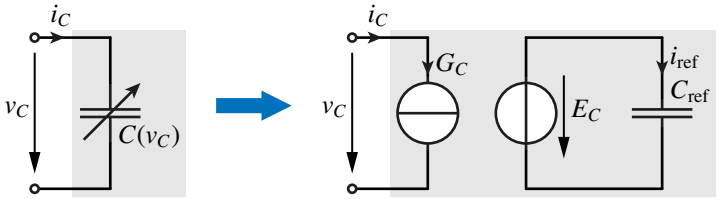


Fig. 3: Circuit used in SPICE to implement voltage-dependent capacitances, specifically C_{dg} and C_{ds}.

For the implementation of the body diode, the intrinsic diode model of SPICE is used. This model directly implements the Shockley equation (5).

3 Statistical Parameter Modelling

Tolerances during the manufacturing cause each switch to have slightly different properties. The switch properties are described by the fitted parameters of the behavioural model derived in section 2. For each switch, this results in N_{param} model parameters. Consequently, the fitting of a sample set with N_{sample} switches results in an N_{param}-dimensional point set consisting of N_{sample} points, where each point corresponds to a modelled switch. The point set determined in this way reflects the variation of the switch properties of the N_{sample} samples.

This set of points can be modelled using statistical equations. This allows to generate an arbitrarily large theoretical sample set, which has the same statistical properties as the measured sample set. Thereby, the correlation between submodels is neglected. Furthermore, not all model parameters have the same influence on the variation of the switch properties. Usually, the switch variation can be modelled with sufficient accuracy by taking into account only a few dominant parameters, as will be shown in the next subsections.

In the following, the statistical modelling of the submodels for the current characteristics, the device capacitances and the internal gate resistance is explained. The variation of the parameters of the diode equation is neglected. The basis for the statistical modelling is the measurement of 10 SiC MOSFETs of the type C3M0075120D. The characteristic measurements were carried out with a B1506A power device analyzer from Keysight.

3.1 Statistical Modelling of Current

The current characteristic of a MOSFET is essentially determined by the structure of the MOSFET cell. The most influential parameters are the epitaxial layer, the channel length, the interface traps and the inversion layer [5]. Variations of these parameters mainly affect the threshold voltage and the transconductance of the MOSFET.

The transconductance essentially describes the current amplification. In the current equation (1), this corresponds to the parameter k_1. The threshold voltage on the other side describes the gate-source voltage at which the MOSFET channel becomes electrically conductive. With reference to the transfer characteristic of a MOSFET, a change in the threshold voltage primarily causes a shift in the characteristic curve along the v_{gs}-axis. The threshold voltage does not explicitly appear as a parameter in the current equation. However, the same effect can be modelled with the parameter k_3.

To determine the statistical distribution of k_1 and k_3 as well as the value of the other parameters of the current equation, the following two steps are performed:

1) First, the mean values of the model parameters $k_1 - k_{10}$ are determined. For this purpose, all measurement curves of the N_{sample} samples are taken into account at the same time for fitting $k_1 - k_{10}$.
2) Subsequently, the statistical distributions of the dominant parameters k_1 and k_3 are determined. For this purpose, the previously determined mean values are first assigned to the other parameters. Then k_1 and k_3 are individually fitted to the N_{sample} characteristic current measurements. The resulting distributions of k_1 and k_3 consist of N_{sample} values, each of which can be fitted by Gaussian distributions [14]. This results in (μ, σ) pairs for both k_1 and k_3, where μ is the mean and σ is the standard deviation of the respective statistical distribution.

The parameters determined in this way are summarised in Table I. To check the accuracy of this procedure, the measured variation of the current characteristic is re-simulated based on 100 Monte Carlo simulations. The results are depicted in Fig. 4(a) and show good agreement with the measured current variation.

Table I: Fitting parameters of SiC MOSFET C3M0075120D. The distributions of statistical parameters are highlighted in bold. They are indicated with (μ,σ) pairs, where μ is the mean value and σ is the standard deviation.

Current model									
$\boldsymbol{k_1}$	$\boldsymbol{(-5.95, 49.6e-3)}$	k_2	$264e-3$	$\boldsymbol{k_3}$	$\boldsymbol{(-8.0, 137e-3)}$	k_4	$21.4e-3$	k_5	-7.78
k_6	$-32.2e-3$	k_7	-1.71	k_8	32.3	k_9	$-631e-3$	k_{10}	$75.9e-3$
Gate resistance & Body diode model									
$\boldsymbol{R_{\text{g,int}}}$	$\boldsymbol{(10.02, 129.4e-3)}$	I_s	$102.6e-3$	R_s	$14.7e-3$	N	41.04		
Capacitance model C_{gs}									
$\boldsymbol{C_{gs}}$	$\boldsymbol{(1.184e-9, 8.6384e-12)}$								
Capacitance model C_{ds}									
$\boldsymbol{a_1}$	$\boldsymbol{(618.1e-12, 3.6e-12)}$	$\boldsymbol{b_1}$	$\boldsymbol{(-94.7e-3, 1.9e-3)}$	c_1	$11.7e-12$	d_1	-1.553	e_1	5.45
a_2	$120.1e-12$	b_2	-1.13	c_2	$23.2e-12$	d_2	$-164.3e-3$	e_2	31.22
a_3	$94.71e-12$	b_3	$-5.47e-3$	c_3	$115.1e-12$	d_3	$-239.9e-3$	e_3	12.12
a_4	$121.8e-12$	b_4	$-27.3e-3$	c_4	$-57.9e-12$	d_4	-3.27	e_4	9.45
f	$-48.8e-12$								
Capacitance model C_{dg}									
$\boldsymbol{a_1}$	$\boldsymbol{(167.6e-12, 7.4e-12)}$	$\boldsymbol{b_1}$	$\boldsymbol{(-257.6e-3, 7.6e-3)}$	c_1	$29.9e-12$	d_1	-2.75	e_1	-75.99
a_2	$181.3e-12$	b_2	-1.86	c_2	$-30.9e-12$	d_2	-15.78	e_2	9.03
f	$3.86e-12$								

3.2 Statistical Modelling of Device Capacitances

Process fluctuations during chip manufacturing also cause a variation of the capacitance curves of C_{gs}, C_{dg} and C_{ds}. The variation of the capacitance curves can essentially be described by a scattering of the DC value $C(v=0)$ and in the case of C_{dg} and C_{ds} by a scattering of the capacitance change $\mathrm{d}C/\mathrm{d}v$.

With respect to the capacitance equation (4) used for C_{ds} and C_{dg}, the DC value and the capacitance change are mainly determined by the sum of the exponential terms with the model parameters a_i and b_i. Therefore, the variation of the capacitance curves is modelled based on these parameters. Usually, several exponential terms are necessary to achieve an accurate fit of the capacitance curves. In the following, only the parameters of one exponential term are used to describe the variation of the capacitance curves, as this already allows for a sufficiently accurate representation of the variation. The remaining parameters are considered constant. Furthermore, C_{gs} is modelled by a voltage-independent capacitance as already described in section 2. Consequently, the statistical parameter in this case is the capacitance value C_{gs} itself.

The procedure for determining the statistical distribution of the dominant capacitance parameters is the same as for the statistical modelling of the current. The resulting parameters are summarised in Table I. The variation of the capacitance characteristics has been again re-simulated based on 100 MC simulations. The results are depicted in Fig. 4(c)-(e) and show good agreement with the measured variation.

3.3 Statistical Modelling of Internal Gate Resistance

The internal gate resistance $R_{g,int}$ primarily depends on the film thickness and the resistivity of the gate electrode material [20]. It is modelled by a single constant parameter $R_{g,int}$. Therefore, $R_{g,int}$ itself is modelled as a statistical variable. The resulting statistical distribution is also listed in Table I. Fig. 4(b) shows the re-simulation, which also shows good agreement with the measured variations.

4 Monte-Carlo Simulation of the LTD

The parallel and/or series connection of switches with different characteristics leads to imbalanced voltage and current distributions within the circuit during switching operations. In a pulse generator, asymmetrical voltage and current distributions have an influence on the pulse shape of the output voltage. In very fast pulse generators, the influence on the rise and fall time of the output voltage is of particular interest. To determine an expected

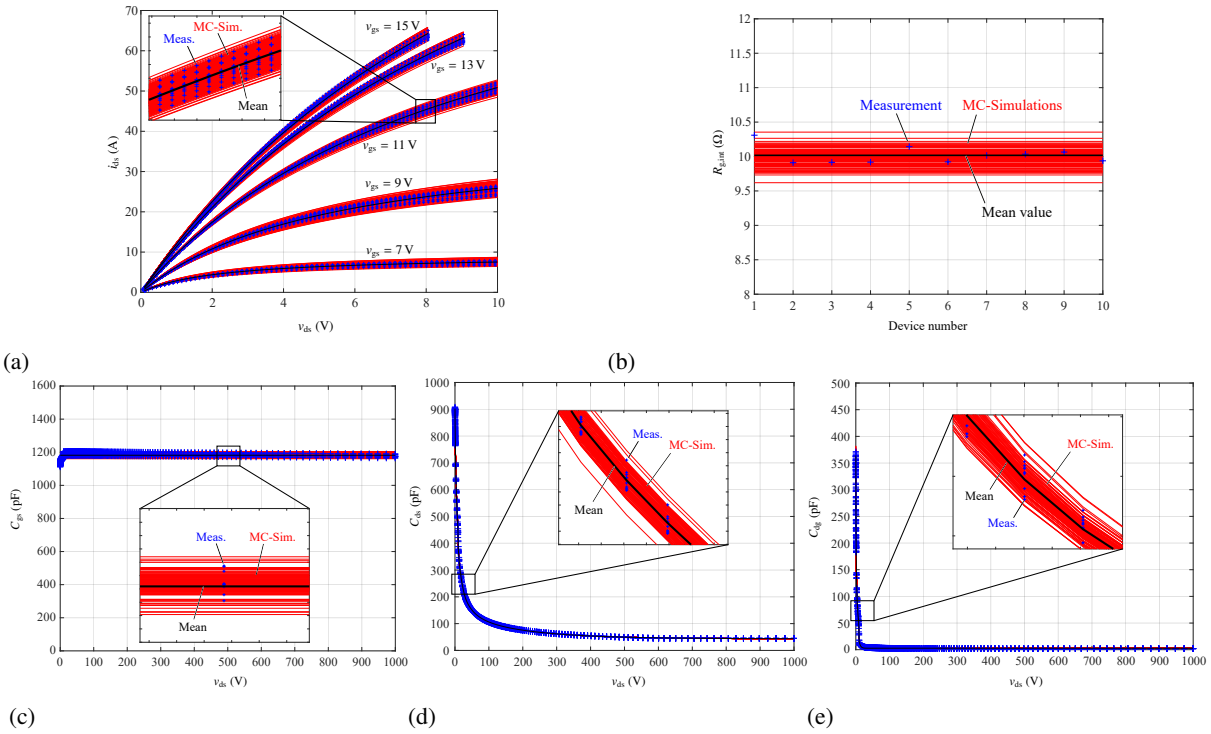


Fig. 4: (a) Output characteristics of current, (b) $R_{g,int}$, (c) C_{gs}, (d) C_{ds} and (e) C_{dg}. The measurement points are marked with blue crosses. The fitted mean value is indicated with a black line. The simulation of the measured spread is shown in red.

value for the rise and fall time under the influence of device variations, a suitable statistical analysis of the circuit is required.

A simple worst-case analysis does not provide any information about the expected value and statistical distribution of the circuit variables. The conclusions drawn from such an analysis are therefore often too restrictive. In contrast, a statistical analysis based on MC simulations is more meaningful because it also takes probabilities into account. The basis for a statistical analysis of a circuit topology is the statistical modelling of the switch, which is discussed in section 3. The behaviour of the topology can then be modelled by independently sampling the statistical equations of each switch.

4.1 Circuit Model & Simulation Parameters

To assess the influence of variations of the switch parameters on the switching behaviour of a pulse generator, the LTD shown in Fig. 1(a) is investigated. A more detailed model of a single stage of the LTD consisting of n_{cell} parallel-connected switching cells is shown in Fig. 5. Component parasitics are highlighted in green. Parasitics from the layout of the switching cell and the mechanical arrangement are highlighted in blue. The transformer core is modelled with a core resistance R_c and a magnetising inductance L_m. The capacitance of the DC link is chosen to be large enough such that the voltage drop due to the discharge of the capacitors during the flat pulse can be neglected. Therefore, the DC link capacitors are replaced by a constant voltage source. A detailed explanation of the modelled parasitics including their values can be found in [23]. The gate driver circuit is modelled by the voltage source v_{drv} and a series resistor $R_{on(drv)}$. The simulation parameters used for the MC simulations are listed in Table II. With these parameters an output voltage amplitude of 5 kV and a load current amplitude of 100 A for the LTD results. Further, it is assumed that synchronised gate voltages are applied to the switches, i.e. that all gate voltages are equal. Considerations of variations in the gate driver circuits or jitter effects in the trigger signals is out of the scope of this paper and are not taken into account.

4.2 Simulation Results of Sample Measurements

In the following, the influence of variations of the switch parameters on the synchronization of the switches and on the rise and fall time of the output pulse are investigated. The variations in the device characteristics are based on the measured samples of section 3.

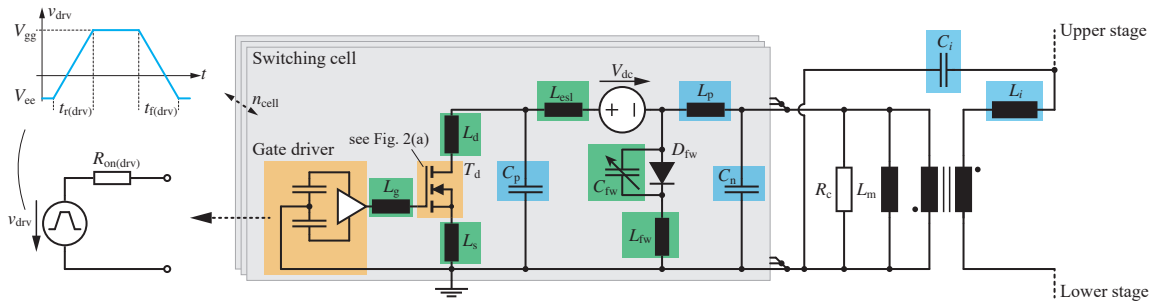


Fig. 5: Circuit model of the i-th LTD stage including stray inductances and capacitances.

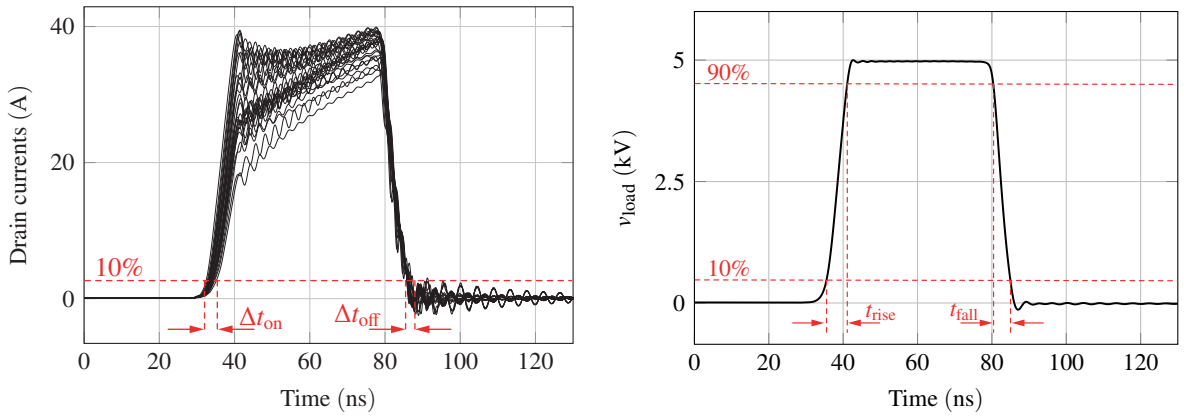
Table II: Parameter values used for the MC simulations. Detailed parameter values of the parasitics are given in [23].

Topology									
V_{dc}	720 V	n	7	n_{cell}	4	R_{load}	50 Ω		
Gate driver									
V_{gg}	18 V	V_{ee}	−5 V	$t_{r(drv)}$	10 ns	$t_{f(drv)}$	10 ns	$R_{on(drv)}$	0.6 Ω

The synchronicity of the SiC MOSFET switching is determined by looking at the turn-on and turn-off times. In this context, the turn-on, respectively turn-off time is defined as the time instant when the drain current of the respective switch reaches 10 % of the nominal switch current. Subsequently, the maximum deviation of the turn-on times Δt_{on} and the turn-off times Δt_{off} of all switches are calculated for each MC simulation. For a better understanding, Δt_{on} and Δt_{off} are illustrated in Fig. 6(a) where, as an example, the switch currents of all 28 SiC MOSFET are plotted for varying current characteristics. The rise and fall time of the output pulse is measured between 10 % and 90 % of the voltage amplitude. The times t_{rise} and t_{fall} are illustrated in Fig. 6(b), where the output voltage of the example simulation is shown.

In the following, the influence of variations in the current characteristics, the device capacitances and the internal gate resistance on Δt_{on}, Δt_{off}, t_{rise} and t_{fall} is investigated. The results are shown in Fig. 7. The expected values are added to each histogram. During the MC simulations of one submodel, the parameters of the other submodels are kept constant. Each histogram is based on 1000 MC simulations.

The parameter variation of the MOSFETs leads to an unsynchronised switching in the range of a few hundred picoseconds. As a result, the current distribution between parallel-connected SiC MOSFETs is no longer balanced and a single MOSFET has to switch a current that is larger than the nominal current. The switching times typically scale with the switched current. As a result, the expected values of the switching times are higher



(a) (b)

Fig. 6: Simulation example for a varying current characteristics: (a) Drain currents of the 28 SiC MOSFETs and (b) the output voltage. Also indicated are the investigated key figures.

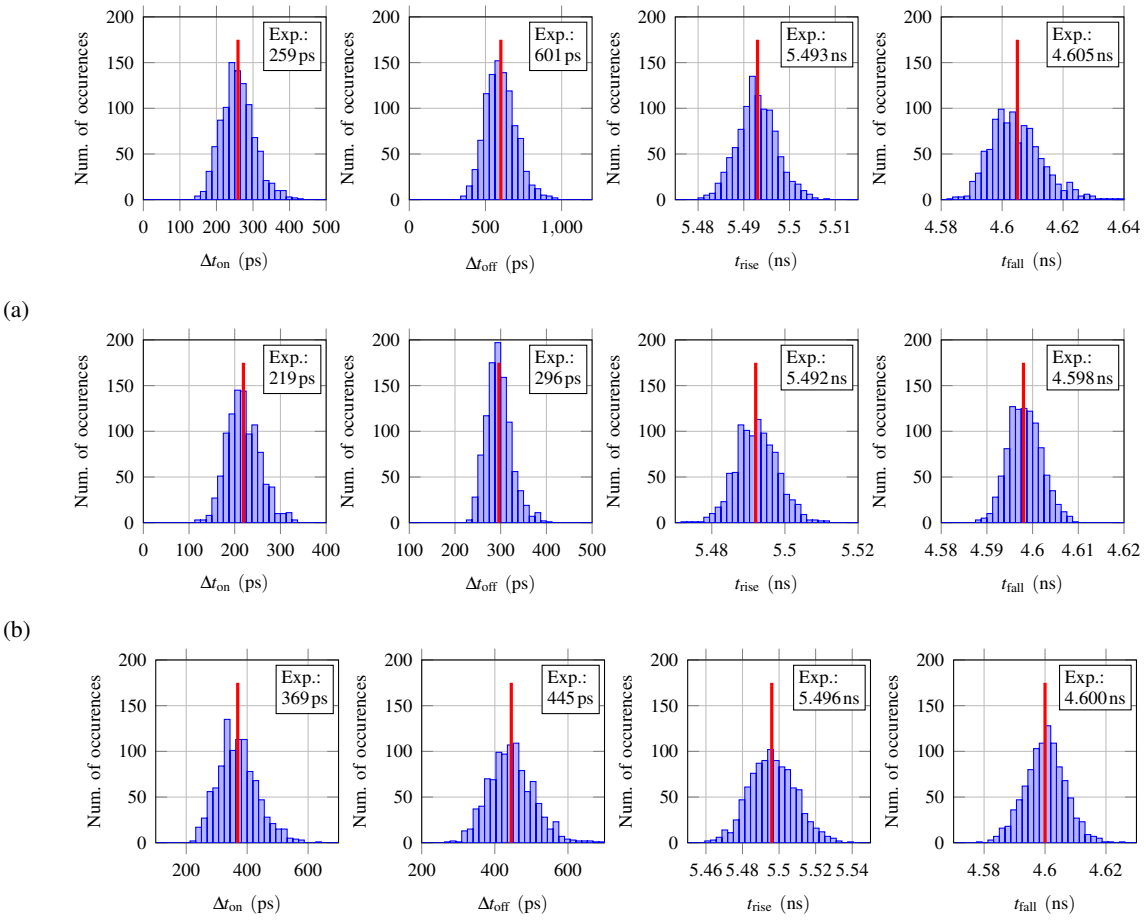


Fig. 7: Histograms of Δt_{on}, Δt_{off}, t_{rise} and t_{fall} for parameter variations in (a) the current model, (b) the device capacitances and (c) the internal gate resistance. Each histogram is based on 1000 MC simulations. The expected values are also indicated and marked with a red line.

than the values for perfect synchronisation, which are $t_{rise} = 5.491\,\text{ns}$ and $t_{fall} = 4.598\,\text{ns}$. However, one has to mention that the switching times only increase by a small amount, partly because the parameter variations of the measured MOSFETs are rather small.

4.3 Dependence on Degree of Variation

The simulation results in the previous subsection have shown that under the influence of device parameter variations, the switches no longer switch synchronously and thus the expected rise and fall time of the output voltage of the LTD increase. This section examines the dependency of the synchronicity and the rise and fall time on the degree of variation, expressed by the respective standard deviations of the submodels.

As a basis σ_{base} for each submodel, the standard deviations extracted in section 3 for the 10 MOSFET samples are used. To increase the degree of variation, the standard deviations are successively increased by a multiple of the respective σ_{base} of each submodel. For each value of the standard deviation, 1000 MC simulations are carried out and the respective expected values are calculated.

The results are summarised in Fig. 8. The Δt_{on} and Δt_{off} increase with a larger degree of variation. Similarly, t_{rise} and t_{fall} slightly increase with a larger range of parameter variation because the transient current distribution is more unevenly distributed. For instance, to limit the increase of the rise/fall time to 5 %, the parameter variation should be confined to approximately $6\sigma_{base}$.

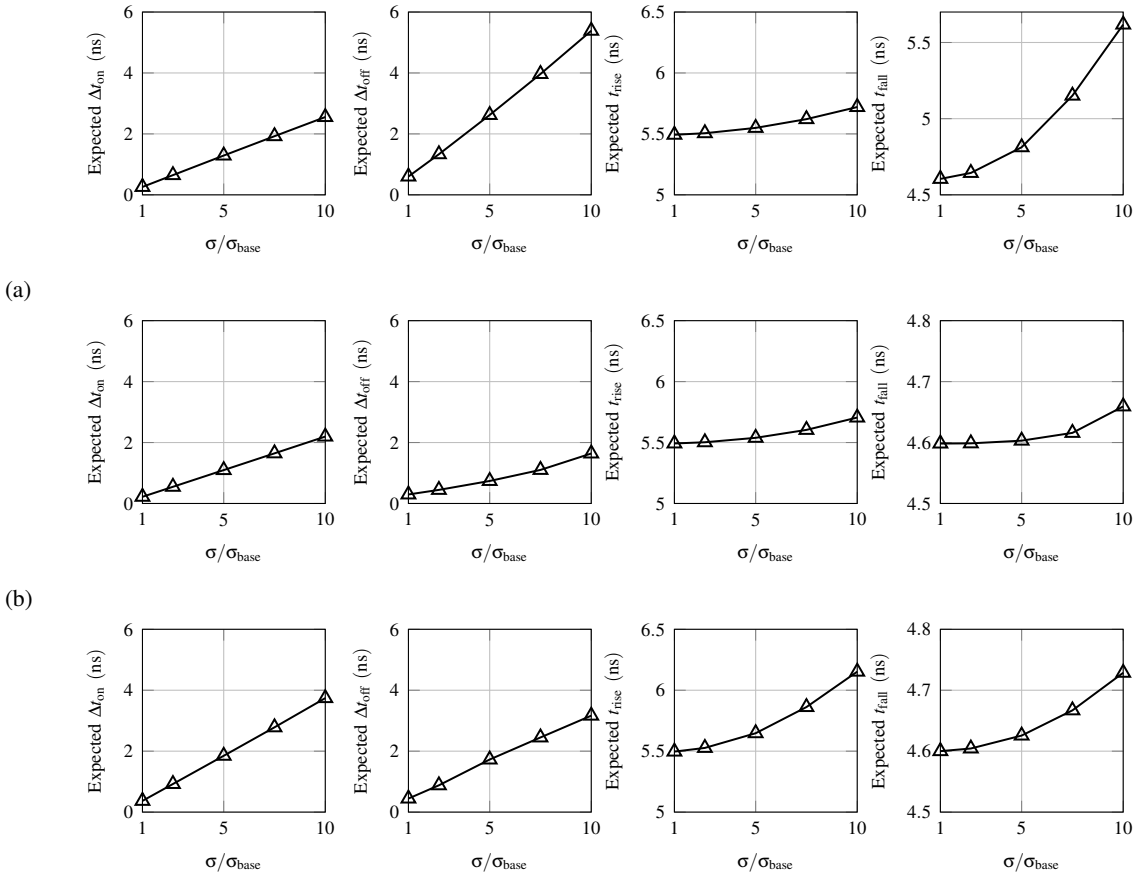


Fig. 8: Expected values of Δt_{on}, Δt_{off}, t_{rise} and t_{fall} for different standard deviations of the parameter variation of (a) the current model, (b) the device capacitances, and (c) the internal gate resistance. Each simulation point is based on 1000 MC simulations.

5 Conclusion

For a comprehensive assessment of the pulse performance of a nanosecond solid-state LTD, parameter variations of the employed power semiconductors have to be taken into account. For this purpose, statistical modelling of the SiC MOSFETs is applied.

In a first step, the SiC MOSFET is modelled using a behavioural model with separate submodels for the current characteristics, the device capacitances and the internal gate resistance. Subsequently, the dominant model parameters, which have the largest influence on the device variations, are identified for each submodel. The statistical distribution of these dominant parameters are then calculated based on characteristic measurements of 10 SiC MOSFETs. In a last step, MC simulations of the LTD are performed in order to investigate the influence of device variations on the synchronicity of the SiC MOSFETs as well as the rise and fall times of the output voltage.

The simulation results show that device variations lead to a unsynchronised switching of the SiC MOSFETs, which can easily reach a few hundred picoseconds and increases approximately linearly with increasing range of variation. This results in an imbalanced current distribution among parallel-connected switches, which can eventually lead to temperature differences among the switches. As a consequence, some switches might experience an overstress, potentially reducing the lifetime and the reliability. As a further consequence of the current imbalance, the expected values of the output voltage rise/fall times of the sample MOSFETs are slightly higher than for perfect synchronisation. With increasing degree of device variation, the expected values of the rise/fall times further increases by several hundred picoseconds.

References

[1] L. M. Redondo, A. Kandratsyeu, and M. J. Barnes, "Marx Generator Prototype for Kicker Magnets Based on SiC MOSFETs", *IEEE Trans. Plasma Sci.*, vol. 46, no. 10, pp. 3334–3339, Oct. 2018.

[2] L. Pang, T. Long, K. He, Y. Huang, and Q. Zhang, "A Compact Series-Connected SiC MOSFETs Module and Its Application in High Voltage Nanosecond Pulse Generator", *IEEE Trans. Ind. Electron.*, vol. 66, no. 12, pp. 9238–9247, Dec. 2019.

[3] T. Huiskamp and J. J. Van Oorschot, "Fast Pulsed Power Generation With a Solid-State Impedance-Matched Marx Generator: Concept, Design, and First Implementation", *IEEE Trans. Plasma Sci.*, vol. 47, no. 9, pp. 4350–4360, Sep. 2019.

[4] F. Yu, T. Sugai, A. Tokuchi, and W. Jiang, "Development of Solid-State LTD Module Using Silicon Carbide MOSFETs", *IEEE Trans. Plasma Sci.*, vol. 47, no. 11, pp. 5037–5041, Nov. 2019.

[5] J. Mueting, P. Natzke, A. Tsibizov, and U. Grossner, "Influence of Process Variations on the Electrical Performance of SiC Power MOSFETs", *IEEE Trans. Electron Devices*, vol. 68, no. 1, pp. 230–235, Jan. 2021.

[6] T. Wang, H. Lin, and S. Liu, "An Active Voltage Balancing Control Based on Adjusting Driving Signal Time Delay for Series-Connected SiC MOSFETs", *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 8, no. 1, pp. 454–464, Mar. 2020.

[7] C. Yang, Y. Pei, Y. Xu, *et al.*, "A Gate Drive Circuit and Dynamic Voltage Balancing Control Method Suitable for Series-Connected SiC MOSFETs", *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 6625–6635, Jun. 2020.

[8] Y. Wen, Y. Yang, and Y. Gao, "Active Gate Driver for Improving Current Sharing Performance of Paralleled High-Power SiC MOSFET Modules", *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 1491–1505, Jun. 2020.

[9] C. Zhao, L. Wang, F. Zhang, and F. Yang, "A Method to Balance Dynamic Current of Paralleled SiC MOSFETs With Kelvin Connection Based on Response Surface Model and Nonlinear Optimization", *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 2068–2079, Feb. 2021.

[10] J. Ke, Z. Zhao, P. Sun, H. Huang, J. Abuogo, and X. Cui, "Chips Classification for Suppressing Transient Current Imbalance of Parallel-Connected Silicon Carbide MOSFETs", *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 3963–3972, Apr. 2020.

[11] J. Ke, Z. Zhao, Q. Zou, J. Peng, Z. Chen, and X. Cui, "Device Screening Strategy for Balancing Short-Circuit Behavior of Paralleling Silicon Carbide MOSFETs", *IEEE Trans. Device Mater. Rel.*, vol. 19, no. 4, pp. 757–765, Dec. 2019.

[12] B. Zhao, Q. Yu, P. Sun, Y. Cai, and Z. Zhao, "Device Screening Strategy for Suppressing Current Imbalance in Parallel-Connected SiC MOSFETs", *IEEE Trans. Device Mat. Rel.*, vol. 21, no. 4, pp. 556–568, Dec. 2021.

[13] H. Tsukamoto, M. Shintani, and T. Sato, "A study on statistical parameter modeling of power MOSFET model by principal component analysis", in *Proc. IEEE Int. Conf. Microelect. Test Struct.*, Mar. 2019.

[14] ——, "Statistical Extraction of Normally and Lognormally Distributed Model Parameters for Power MOSFETs", *IEEE Trans. Semicond. Manufact.*, vol. 33, no. 2, pp. 150–158, May 2020.

[15] H. Li, S. Munk-Nielsen, X. Wang, *et al.*, "Influences of Device and Circuit Mismatches on Paralleling Silicon Carbide MOSFETs", *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 621–634, Jan. 2016.

[16] A. Borghese, M. Riccio, A. Fayyaz, *et al.*, "Statistical analysis of the electrothermal imbalances of mismatched parallel SiC power MOSFETs", *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 7, no. 3, pp. 1527–1538, Sep. 2019.

[17] B. W. Nelson, A. N. Lemmon, B. T. DeBoi, *et al.*, "Computational Efficiency Analysis of SiC MOSFET Models in SPICE: Static Behavior", *IEEE Open Journal Power Electron.*, vol. 1, pp. 499–512, Nov. 2020.

[18] H. Li, X. Zhao, K. Sun, Z. Zhao, G. Cao, and T. Q. Zheng, "A Non-Segmented PSpice Model of SiC MOSFET With Temperature-Dependent Parameters", *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4603–4612, May 2019.

[19] R. Stark, A. Tsibizov, N. Nain, U. Grossner, and I. Kovacevic-Badstuebner, "Accuracy of Three Interterminal Capacitance Models for SiC Power MOSFETs Under Fast Switching", *IEEE Trans. Power Electron.*, vol. 36, no. 8, pp. 9398–9410, Aug. 2021.

[20] J. Ke, Z. Zhao, P. Sun, H. Huang, J. Abuogo, and X. Cui, "Influence of Device Parameters Spread on Current Distribution of Paralleled Silicon Carbide MOSFETs", *J. Power Electron.*, vol. 19, no. 4, pp. 1054–1067, Jul. 2019.

[21] A. Endruschat, T. Heckel, H. Gerstner, C. Joffe, B. Eckardt, and M. Maerz, "Application-related characterization and theoretical potential of wide-bandgap devices", in *Proc. IEEE Workshop Wide Bandgap Power Devices Appl.*, Oct. 2017.

[22] B. W. Nelson, A. N. Lemmon, S. J. Jimenez, *et al.*, "Computational Efficiency Analysis of SiC MOSFET Models in SPICE: Dynamic Behavior", *IEEE Open Journal Power Electron.*, vol. 2, pp. 106–123, Feb. 2021.

[23] R. Risch and J. Biela, "Solid-State Marx Generator vs. Linear Transformer Driver: Comparison of Parasitics and Pulse Waveforms for Nanosecond Pulsers", in *Proc. IEEE Pulsed Power Conf.*, Dec. 2021.