Design and analysis of a voltage clamping active delay control method for series connected SiC MOSFETs

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Abstract

Series connection of power devices is an attractive approach to overcome the obstacle of the blocking voltage limitation of a single power device. However, voltage balancing measures should be taken to assure the anticipated performance of series connected power devices. In this paper, based on emerging silicon carbide (SiC) metal-oxide semiconductor field-effect transistors (MOSFETs), a clamping resistor-capacitor-diode circuit-based voltage clamping active delay control method is proposed to improve their voltage balancing performance. Compared with existing active delay control methods which sample the drain-source voltages of SiC MOSFETs as feedbacks, this proposed method utilizes the voltages of clamping capacitors as control criteria, which exhibits two prominent advantages: (1) an accurate model of the system is easier to attain (2) the feedback loop is simpler to design. After detailed demonstration of this method, the corresponding model is established to help determine appropriate control parameters, and experiments finally validate the effectiveness of the proposed method.

Introduction

The development of wide band gap devices has prompted power electronics converters towards a higher frequency and a higher power density. Among them, emerging silicon carbide (SiC) metal-oxide semiconductor field-effect transistor (MOSFET) has drawn much attention particularly in medium voltage applications. However, the blocking voltage of a commercial single SiC MOSFET is still limited, maximum to 3.3kV according to the data from GeneSiC [1]. Therefore, in order to accommodate a higher voltage rating, series connection of SiC MOSFETs is called for [2 - 5].

To solve the voltage unbalancing problem of series connected SiC MOSFETs, active voltage balancing methods are more prevalent compared with passive ones in published literature, owing to the advantage of lower induced loss [6]. Adding compensating circuits to the gate loop of SiC MOSFET is the general idea of active voltage balancing methods, by considering the inevitable difference of gate loop parameters during the switching transient [7]. In addition, the delay deviation of switching signals between series connected SiC MOSFETs is also one major factor that causes the voltage unbalancing. On the other hand, it can be utilized as a measure to control the voltage balancing by properly adjusting this deviation, and that is the basic principle of active delay control concept [8 - 12].

With additional feedback units and delay executive units, the active delay control methods for voltage balancing feature limited penalty of switching performance of series connected SiC MOSFETs. In general, the drain-source voltages of series connected SiC MOSFETs are divided by resistor network and then sampled by analog-to-digital convertors (ADCs) for comparison, which is used as the control criteria. After calculation by the controller, the additional delay executive units are acting to subtly give the turn-off delay compensations for the voltage balancing purpose. During this process, a potential stability problem exists, as mentioned in [10], in other words, the parameters in the control algorithm should be accurately designed by modelling the entire active delay control system. However, the relationship between the derived delay and the voltage unbalancing degree of series connected SiC

MOSFETs is uncertain, and it is usually identified by an experimental way [10, 11], which increases the design burden and reduces the flexibility.
Consequently, in this paper, a clamping Resistor-Capacitor-Diode (RCD) circuit is combined with the active delay control method to overcome the above drawback since a certain system model can be attained. Besides, the clamping RCD circuit not only helps to improve the voltage balancing performance, but also makes both the feedback unit and the delay executive unit easier to design as: (1) the voltage across the capacitor in the clamping RCD circuit is sampled and converted to frequency through the optic fiber, which provides galvanic isolation; (2) Digital signal processer (DSP) controller detects the feedback frequency by its integrated Enhanced Capture (eCAP) module, then gives the delay compensation through its inside High Resolution Pulse-Width-Modulation (HRPWM) module directly. The demonstration of the proposed hybrid voltage balancing method, also named as the voltage clamping active delay control method, is presented, followed by the detailed modeling and stability analysis. Afterwards, the validity is confirmed by a buck chopper circuit using two series connected SiC MOSFETs.

The demonstration of the proposed voltage clamping active delay control method

The overall hardware structure of the proposed voltage clamping active delay control method is shown in Fig. 1. Two SiC MOSFETs T_1 and T_2 are connected in series for meeting a higher blocking voltage requirement, and the same clamping RCD circuit is equipped with each SiC MOSFET for two benefits: (1) during the static state, the static voltage balancing of T_1 and T_2 is realized by forming a current loop as: diode D_1 → resistor R_1 → diode D_2 → resistor R_2. (2) during the dynamic state, the voltage overshoot of T_1 (T_2) is clamped once the voltage exceeds the clamping value of capacitor C_1 (C_2) in the clamping RCD circuit.

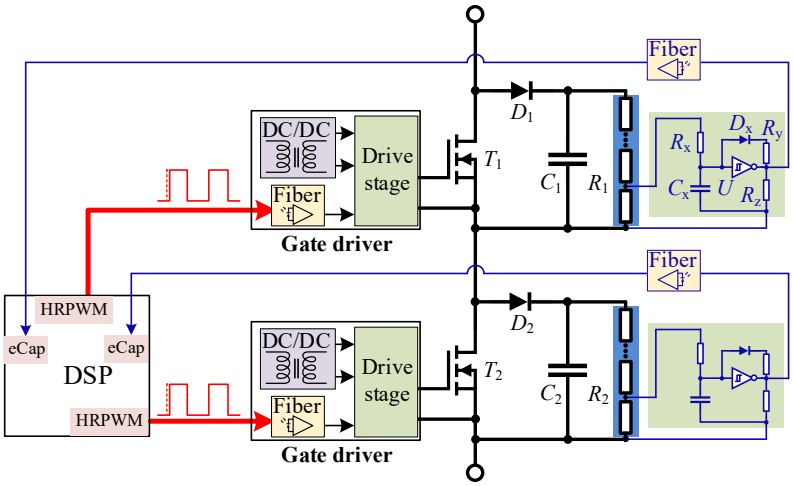

Fig. 1: The overall hardware structure of the proposed voltage clamping active delay control method

General active delay control methods attempt to control the voltage balancing of series connected SiC MOSFETs by sampling the drain-source voltage v_{ds1} (v_{ds2}) of T_1 (T_2), which requires expensive high-speed ADCs. In this paper, instead, the voltage v_{c1} (v_{c2}) across the capacitor of the clamping RCD circuit is sampled as the feedback as follows:
R_1 (R_2) consists of N series connected resistors, and the voltage v_{c1} (v_{c2}) is scaled down by N as the input of the voltage-to-frequency circuit. The voltage-to-frequency circuit, consisting of resistor R_i (i= x, y, z), capacitor C_x, diode D_x and Schmidt-input comparator U, can output a frequency f_1 (f_2) proportional to the input voltage, which will be illustrated in the next section. Then, an optic fiber is applied to provide galvanic isolation, and it is captured by the eCAP module inside the DSP controller as the control feedback. After the calculation with a preset algorithm, the DSP controller directly gives the switching signal delay compensation by using its inside HRPWM module. Then the gate drivers output appropriate

timing-compensated driving voltages after a short-time interval, and the voltage balancing of v_{ds1} and v_{ds2} is achieved. During this interval, the clamping RCD circuit also contributes to tolerating the short-time voltage unbalancing.

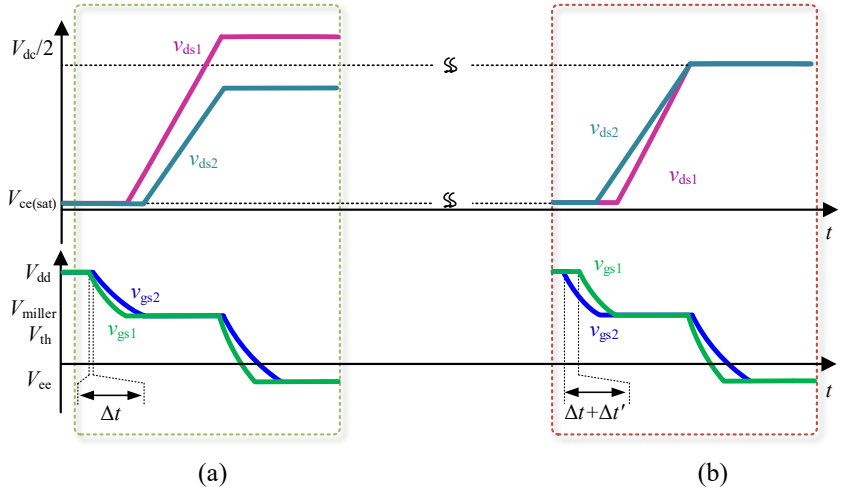

Fig. 2: The voltage sharing of v_{ds1} and v_{ds2} (a) without delay compensation (b) with delay compensation

Without the delay compensation, taking the turn-off process as an example, the voltage sharing of v_{ds1} and v_{ds2} is shown in Fig. 2(a). The DSP controller outputs two identical switching signals for T_1 and T_2. However, due to the total delay deviation of gate driver and optic fiber network, the gate source voltage v_{gs1} of T_1 starts to decrease earlier than v_{gs2} of T_2. In addition, since parasitic parameter variation of the devices exist, the decreasing of v_{gs1} is faster than that of v_{gs2}, and the increasing of v_{ds1} is faster than that of v_{ds2} as well in this assumed case. Consequently, a large voltage unbalancing of v_{ds1} and v_{ds2} occurs. It is pointed out that, the clamping RCD circuit helps to reduce the voltage unbalancing in the initial switching cycles, however, the clamping voltage of T_1 gets much higher as more energy is accumulated in the capacitor C_1, and a stable voltage unbalancing is formed gradually.
Consequently, a closed-loop compensation is required to balance v_{ds1} and v_{ds2}. As presented in Fig. 1, v_{c1} (v_{c2}) is converted into frequency f_1 (f_2), then it is captured when the preset time interrupt arrives and a control algorithm (PI control) in the DSP is applied to generate a compensation delay Δt' for the next switching cycle. To make it clear, the detailed system flowchart is presented in Fig. 3.

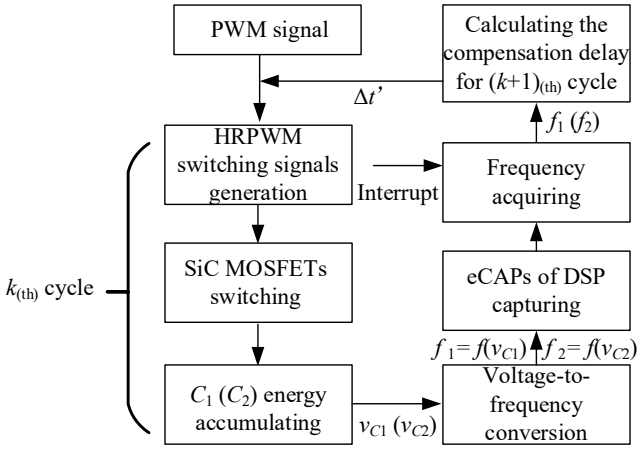

Fig. 3: The detailed system flowchart of the proposed voltage clamping active delay control method

With the delay compensation, the voltage balancing of v_{ds1} and v_{ds2} is shown in Fig. 2(b). Δt' makes v_{gs1} start to decrease later than v_{gs2}, and eventually v_{ds1} and v_{ds2} reach to $V_{dc}/2$ synchronously due to the closed-loop control. Therefore, with a dynamic balance between charging and discharging of C_1 (C_2) in

the clamping RCD circuit, the clamping values of T_1 and T_2 are nearly the same, and v_{ds1} and v_{ds2} are well-balanced.

Modeling and analysis of the proposed voltage clamping active delay control method

As mentioned, PI control is applied as the algorithm in the DSP, and how to properly choose the K_p and K_i parameters remains. Instead of using a method of trial and error, modeling the whole closed-loop system is a more effective way to help choose parameters while maintaining the system stability. Therefore, every separate section presented in Fig. 3 should be modeled accordingly.

In published literatures, the relationship between the derived delay and the voltage unbalancing degree of series connected SiC MOSFETs is generally attained by an experimental way, which limits the design flexibility. Instead, in the proposed circuit, v_{C1} and v_{C2} are sampled as the control feedback, and the relationship between Δt' and the difference Δv_C of v_{C1} and v_{C2} is obtained as:

$$\Delta t' = \frac{C_1 \cdot (v_{C1} - v_{C2})}{I_d} = \frac{C_1 \cdot \Delta v_C}{I_d} \tag{1}$$

where I_d is the power loop current, and C_1 is equal to C_2.

In addition, the voltage to frequency conversion part together with optic fiber connection provides galvanic isolation between the power circuit and the DSP control circuit. Here, a simple Schmitt-trigger-input comparator-based circuit is designed to realize the goal of voltage to frequency conversion, while commercial voltage-to-frequency chips could also be an option. The relationship between f_1 (f_2) and v_{C1} (v_{C2}) can be described as:

$$f_i \approx \frac{v_{Ci}}{N \cdot R_x \cdot C_x \cdot (V_{th}^+ - V_{th}^-)}, \qquad i=1, 2 \tag{2}$$

where V_{th}^+ is the positive threshold voltage of U, and V_{th}^- is the negative threshold voltage of U.

Since the DSP is applied as the controller, the closed-loop system is a discrete system. Defining the sample period as T_s, based on (1) and (2), the control block diagram is shown in Fig. 4.

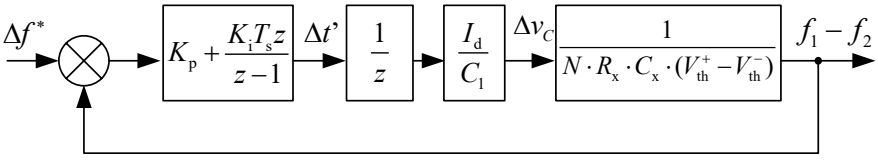

Fig. 4: The control block diagram of the proposed voltage clamping active delay control method

According to Fig. 4, the closed-loop z-transfer function can be solved as:

$$G(z) = \frac{\frac{I_d \cdot K_p + I_d \cdot K_i \cdot T_s}{C_1 \cdot N \cdot R_x \cdot C_x \cdot (V_{th}^+ - V_{th}^-)} \cdot z - \frac{I_d \cdot K_p}{C_1 \cdot N \cdot R_x \cdot C_x \cdot (V_{th}^+ - V_{th}^-)}}{z^2 + (\frac{I_d \cdot K_p + I_d \cdot K_i \cdot T_s}{C_1 \cdot N \cdot R_x \cdot C_x \cdot (V_{th}^+ - V_{th}^-)} - 1) \cdot z - \frac{I_d \cdot K_p}{C_1 \cdot N \cdot R_x \cdot C_x \cdot (V_{th}^+ - V_{th}^-)}} \tag{3}$$

Consequently, by applying Routh–Hurwitz stability criterion, the stability conditions of the system can be obtained as:

$$\begin{cases} \frac{C_1 \cdot N \cdot R_x \cdot C_x \cdot (V_{th}^+ - V_{th}^-)}{I_d} > K_p > -\frac{C_1 \cdot N \cdot R_x \cdot C_x \cdot (V_{th}^+ - V_{th}^-)}{I_d} \\ \frac{2 \cdot C_1 \cdot N \cdot R_x \cdot C_x \cdot (V_{th}^+ - V_{th}^-) - 2 \cdot I_d \cdot K_p}{I_d \cdot T_s} > K_i > 0 \end{cases} \tag{4}$$

Based on the above, according to (4), K_p and K_i can be properly chosen.

Experimental verification

Voltage-to-frequency conversion response

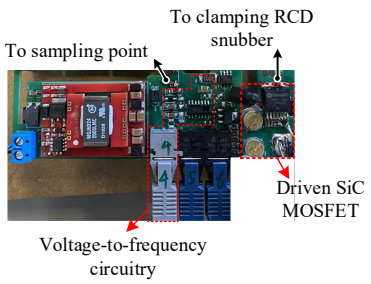

Fig. 5: Photograph of the individual gate driver part of SiC MOSFET

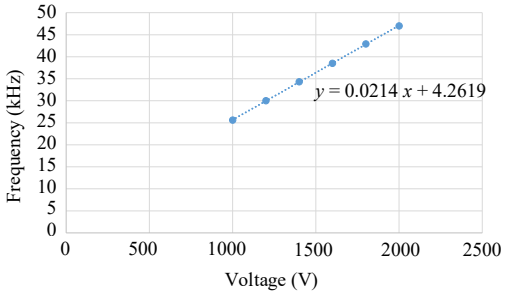

Fig. 6: The measured relationship between input voltage (v_{C1}, v_{C2}) and output frequency

The voltage-to-frequency circuitry plays an important role in the feedback loop, therefore, it is important to evaluate its response firstly. As shown in Fig. 5, this circuitry is integrated in the gate driver part of SiC MOSFET with a fiber connector to send the feedback to DSP controller, and the key circuit parameters relevant to the calculation result is listed in Table I. Based on that, the relationship between the input voltage (v_{C1}, v_{C2}) and the measured output frequency is drawn in Fig. 6. It is observed that their relationship is linear, which is consistent with the derived formula (2).

Effectiveness of the voltage clamping active delay control method

Further, based on the above analysis, the experimental validation is based on a buck chopper circuit, where the circuit diagram is shown in Fig. 7 and the corresponding parameters are given in Table I.

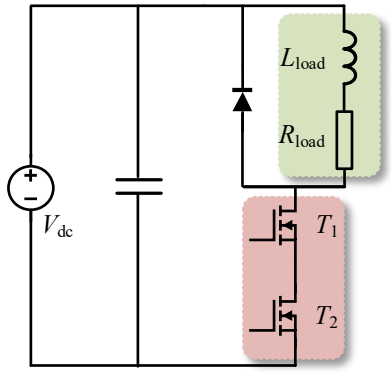

Fig. 7: The buck chopper circuit for testing

Table I: Key Parameters

	Name	Parameters
Gate driver side	N	10
	U	74HC132D
	$C_1(C_2)$, C_x	100 nF, 680 pF
	R_1 (R_2), R_x	2 MΩ, 47 Ω,
Power side	T_1, (T_2)	G2R120MT33J
	L_{load}, R_{load}	70 μH, 30 Ω

When the delay compensation is not applied as shown in Fig. 8, it is observed that a voltage unbalancing of two series connected SiC MOSFETs occurs, and the voltage unbalancing degree is measured to be 10% (maximum (v_{ds1}-v_{ds2})/ (v_{ds1}+v_{ds2})) when the switching frequency is 10 kHz.

Therefore, the delay compensation is applied by using the HRPWM module of DSP, and the time resolution can reach 150 ps, which can satisfy the requirement of active delay control. In this case, T_s is chosen as 0.2 s to ease the controller burden, thanks to the clamping RCD circuit which helps tolerate the short-time voltage unbalancing. Moreover, I_d is set as 20 A, and the calculation could be made according to (4) since the other parameters regarding of the real circuit are known. Therefore, it is concluded that K_i should be smaller than $5.8*10^{-7}$ and larger than 0 when K_p is 0. To verify that, when K_p and K_i are not chosen properly ($K_i = 10^{-6}$, $K_p = 0$), an unstable voltage balancing process is observed as shown in Fig. 9. Since T_s is 0.2 s, during this 0.2 s interval, the unbalancing degree is continuously increased to strike a balance with the clamping RCD circuit. Then in the next 0.2 s interval, the excessive compensation causes reverse unbalancing of v_{ds1} and v_{ds2}, and repeating over time, which is not allowed in series connection.

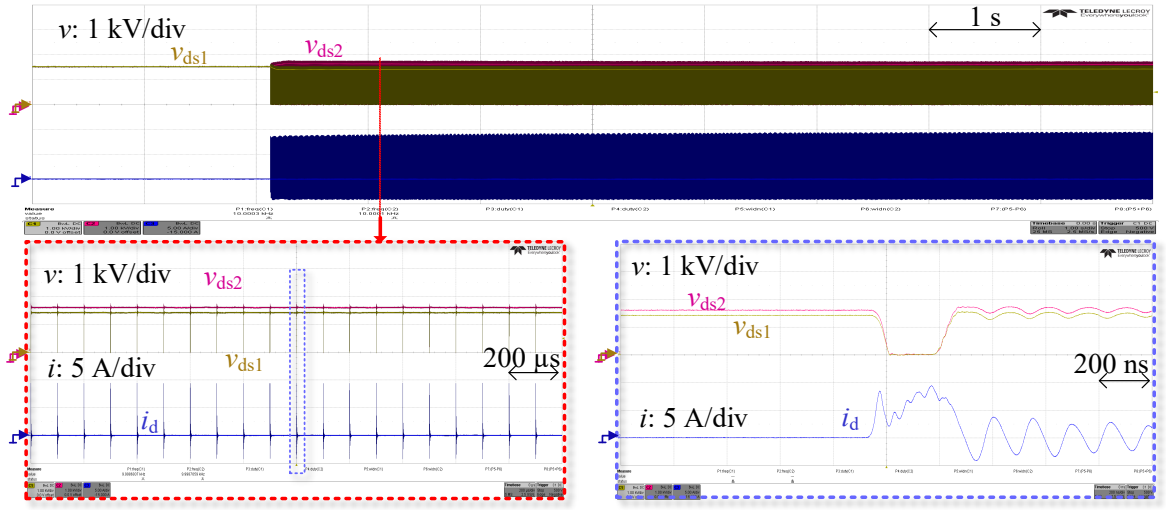

Fig. 8: Voltage sharing of SiC MOSFETs without delay compensation

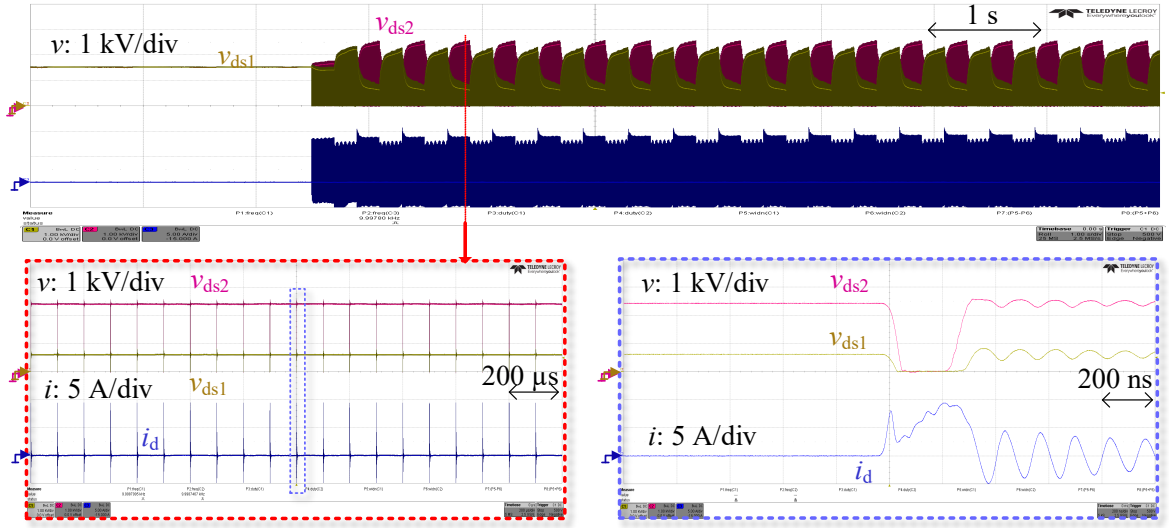

Fig. 9: Voltage sharing of SiC MOSFETs with unstable delay compensation ($K_i = 10^{-6}$)

By contrast, when the delay compensation is applied and K_p and K_i are well chosen ($K_i = 10^{-8}$, $K_p = 0$), a stable voltage balancing is observed as shown in Fig. 10, and the voltage unbalancing degree is measured to be within 1%.

It is worthy of noticing that, despite that the condition $K_i = 10^{-7}$, $K_p = 0$ can satisfy the requirement to be stable as well and it can accelerate the voltage balancing process by choosing a large K_i, but it will cause some undesired oscillation in the meantime, as shown in Fig. 11(a). In the contrary, a smaller value with K_i=0.000000001 can make the voltage balancing process smoother, as shown in Fig. 11(b), but the voltage balancing process becomes slow. Therefore, if a fast response speed is not required, a smaller K_i could be chosen.

Conclusion

In this paper, a voltage clamping active delay control method is proposed and analyzed. Compared with existing active delay control methods, the entire closed-loop system model is simpler to obtain since a clamping RCD circuit is combined and the voltages of clamping capacitors are utilized as control criteria. The feedback unit is designed by using a voltage-to-frequency conversion, and galvanic isolation is provided through an optic fiber. Based on the derived model, the principles to choose the control parameters are provided explicitly. Finally, the experimental results validate the effectiveness of

the proposed voltage clamping active delay control method, also, the accuracy of the established model gets verified as well.

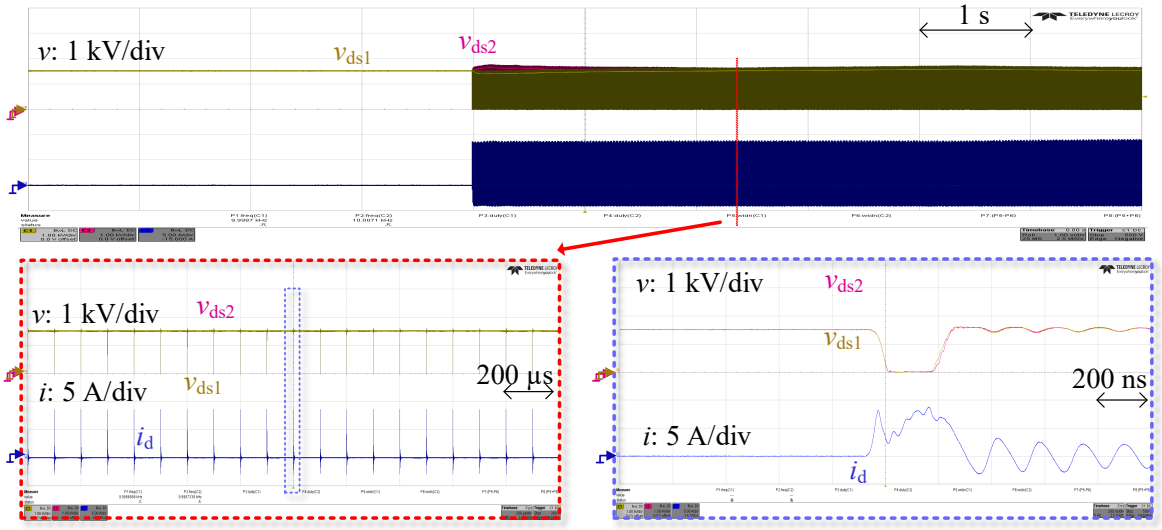

Fig. 10: Voltage sharing of SiC MOSFETs with stable delay compensation ($K_i = 10^{-8}$)

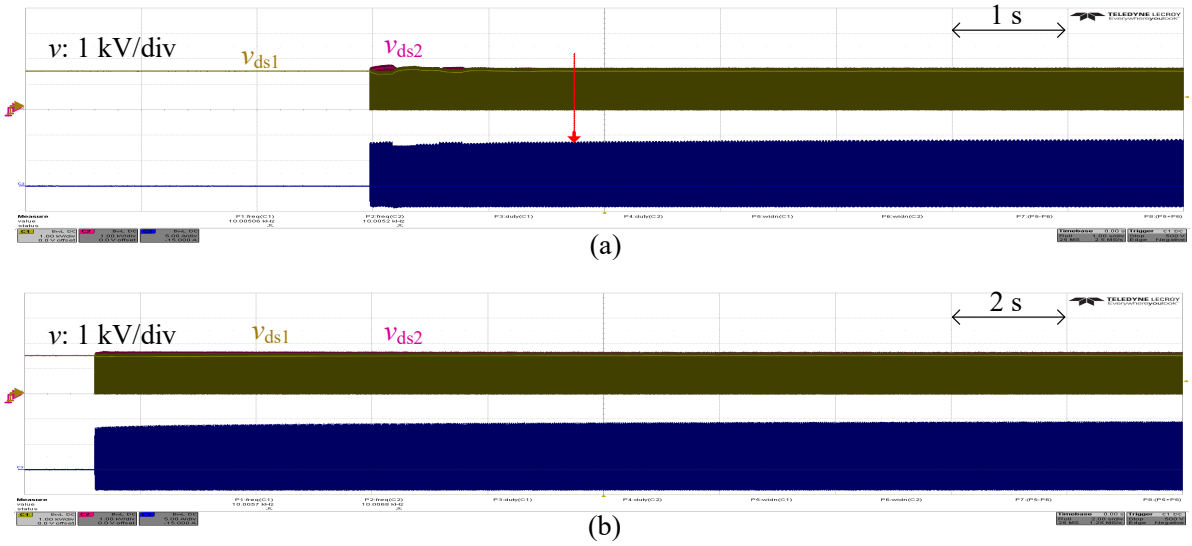

Fig. 11: Voltage sharing cases with stable delay compensation (a) $K_i = 10^{-7}$ (b) $K_i = 10^{-9}$

References

[1] GeneSiC Semiconductor, Accessed 20-12-2021, Online: https://www.genesicsemi.com/sic-mosfet/

[2] R. Wang, A.B. Jørgensen, S. Munk-Nielsen, "An enhanced single gate driven voltage-balanced SiC MOSFET stack topology suitable for high-voltage low-power applications," in IET Power Electronics, vol. 15, no. 3, pp. 251-262, Feb. 2022.

[3] Z. Lu et al., "Medium Voltage Soft-Switching DC/DC Converter With Series-Connected SiC MOSFETs," in IEEE Transactions on Power Electronics, vol. 36, no. 2, pp. 1451-1462, Feb. 2021.

[4] X. Lin, L. Ravi, Y. Zhang, R. Burgos and D. Dong, "Analysis of Voltage Sharing of Series-Connected SiC MOSFETs and Body-Diodes," in IEEE Transactions on Power Electronics, vol. 36, no. 7, pp. 7612-7624, Jul. 2021.

[5] R. Wang, L. Liang, Y. Chen and Y. Kang, “A Single Voltage-Balancing Gate Driver Combined With Limiting Snubber Circuits for Series-Connected SiC MOSFETs,” in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 8, no. 1, pp. 465-474, Mar. 2020.

[6] V. U. Pawaskar, G. Gohil and P. T. Balsara, “Study of Voltage Balancing Techniques for Series-Connected Insulated Gate Power Devices,” in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 10, no. 2, pp. 2380-2394, Apr. 2022.

[7] A. Marzoughi, R. Burgos and D. Boroyevich, “Active Gate-Driver With dv/dt Controller for Dynamic Voltage Balancing in Series-Connected SiC MOSFETs,” in IEEE Transactions on Industrial Electronics, vol. 66, no. 4, pp. 2488-2498, Apr. 2019.

[8] P. Trochimiuk, R. Kopacz, G. Wrona and J. Rąbkowski, “Active Voltage Balancing of Series-Connected 1.7 kV/325 A SiC MOSFETs Enabling Continuous Operation at Medium Voltage,” in IEEE Access, vol. 9, pp. 8604-8614, Jan. 2021.

[9] P. Wang et al. “An Integrated Gate Driver with Active Delay Control Method for Series Connected SiC MOSFETs,” in 2018 IEEE 19th Workshop on Control and Modeling for Power Electronics (COMPEL), 2018, pp. 1-6.

[10] M. Zhao, H. Lin and T. Wang, “An Adaptive Driving Signals Delay Control for Voltage Balancing of Series-Connected SiC MOSFETs,” in 2020 IEEE Energy Conversion Congress and Exposition (ECCE), 2020, pp. 2814-2818.

[11] K. Wada and K. Shingu, “Voltage Balancing Control for Series Connected MOSFETs Based on Time Delay Adjustment Under Start-Up and Steady-State Operations,” in 2018 IEEE Energy Conversion Congress and Exposition (ECCE), 2018, pp. 5495-5499.

[12] C. Li, R. Chen, S. Chen, C. Li, H. Luo, W. Li, X. He, “Analytical Model and Design of Voltage Balancing Parameters of Series-Connected SiC MOSFETs Considering Non-Flat Miller Plateau of Gate Voltage,” in Energies, 2022, 15(5), 1722.