Grounding Points in HV/MV Hybrid Transformer Auxiliary Converters

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Keywords

<<Hybrid Transformer>>, <<Smart Grid>>, <<Distributed Generation>>, <<Power Control>>, <<Voltage Control>>, <<Imbalances Control>>

Abstract

The choice of grounding points in hybrid transformers is important to limit the overcurrents in case of a single line to ground fault. In this paper different grounding points for hybrid transformers are compared based on a controller with active damping for the filter resonances. Based on the comparison the best grounding point for limiting the single line to ground fault current for hybrid transformer auxiliary converters and the MV grid is identified.

1 Introduction

The increasing share of renewable energy generation requires a more flexible and smarter grid [1], [2], for controlling voltage and power fluctuations [3], [4]. To address this, various concepts as for example FACTS, grid expansions, and distribution transformers with controllable tap changer have been investigated [5], [6]. Another interesting solution for controllable transformers are hybrid transformers (HTs). HTs combine a line-frequency power transformer (LFT), which typically transfers the major power share, with an auxiliary AC-AC power electronic converter [7] for controlling the voltage and the power flow. The AC-AC auxiliary converter is typically connected to an auxiliary winding of the LFT as shown in the three-phase representation of a HT in Fig.1. The auxiliary converter system power rating is typically designed only for a relatively small fraction $\approx$ (10%) of the LFT power rating [7], [8]. In general, such power electronic converters as the HT auxiliary converter are relatively sensitive to overcurrents/-voltages, which could occur in the medium voltage (MV) grid in case of a fault, so that a protection system is required.

In the past, various concepts and topologies for HT [8], [9] as well as the protection against grid faults at the low voltage (LV) to medium voltage (MV) gird interface [7] have been investigated. A summary and

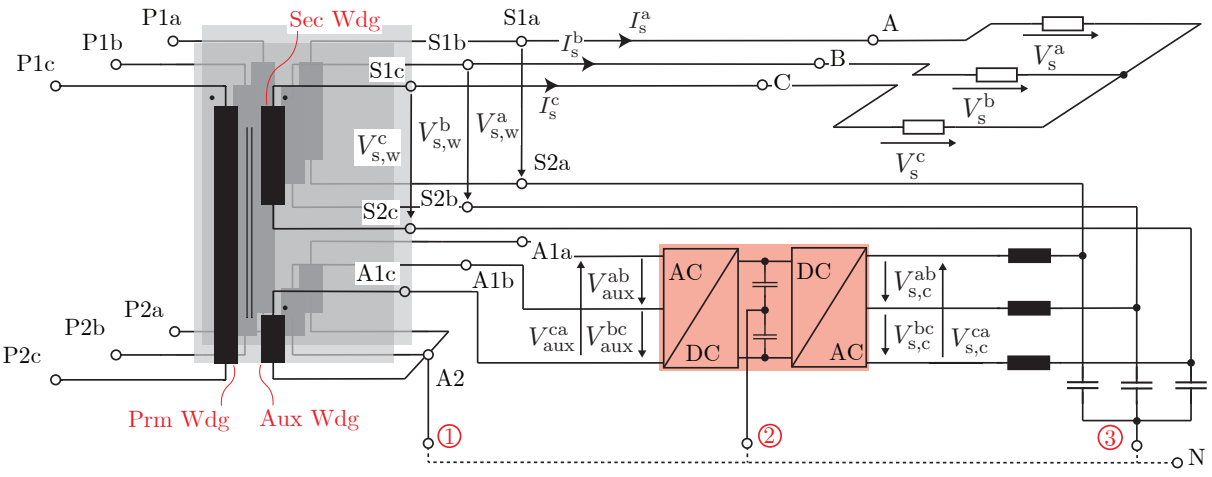

Figure 1: Three-phase HT with LFT, auxiliary converter, and grounding points ①-③, where a load is connected to the secondary winding.

discussion of the most interesting HT concepts can be found in [7]-[10]. Overvoltages and Overcurrents on the HT system level are invesitgated in [11], where it is shown, that the grid grounding method has a significant impact on the fault current through the converter in case of a single line to ground fault. The single line to ground fault is the most common fault in distribution grids and the fault current increases with the grid line length [11]. An increasing grid line length becomes problematic during a single line to ground fault in MV grids with isolated star point. In order to limit the single line to ground fault current for larger grid distances in the MV grid, the neutral point is connected to the ground via an inductance (denoted as resonant grounded grid [12]). The grounding inductance is designed to reduce the capacitive fault current to an acceptable level in case of a single line to ground fault [13], [14].

In general, there are different options for grounding points in HT. Three possible grounding points in HT are indicated by the red numbers ①-③ in Fig. 1. The impact of grounding points on the HT auxiliary converter design including for a resonant grounded grid has not been investigated yet, and is investigated in this paper. In case ①, a grounded star point of the star connected power transformer auxiliary winding is assumed. In case ②, the split DC-link of the HT auxiliary converter is grounded. In case ③, the star point of an assumed LC-filter is grounded. In the following grounding points ①-③ are investigated in terms of overcurrents flowing through the HT auxiliary converter and the reduction of the fault current by a grounding inductance is analyzed for each grounding point. Note that an investigation of the considered grounding points in terms of overvoltages is out of scope of this paper since the considered grounding points are primarily used to limit overcurrents.

As HT AC-AC auxiliary converter a three phase unidirectional AC/AC back-to-back converter is chosen in this paper. The unidirectional HT auxiliary converter has a low number of active switches, but some limiting constrains on the voltage and power controllability as discussed in [15].

In cases ② and ③, the single line to ground fault current flows either directly through the DC-Link capacitors or the LC-filter capacitors of the assumed LC-filter. In order to limit oscillations caused by the DC-Link or the LC-filter capacitors, damping methods are investigated.

In a first step, a simulation model of an unidirectional HT auxiliary converter is presented in **section 2**. Then, the possible grounding points are investigated in detail in **section 3**, and the preferred grounding point is selected. Results for the selected grounding point and a discussion are provided in **section 4**.

2 Simulation Model of the Three-Phase HT Auxiliary Converter

Before we compare grounding points ①-③ of the HT, we derive the simulation model and its parameters for the HT auxiliary converter. The investigation is based on the example of a unidirectional voltage source converter (UNI-VSC) as HT auxiliary converter shown in Fig. 2, where the line to ground capacitances C_{lg} with resistance R_{c} and the grounding inductance L_{co} with resistance R_{co} are neglected for now in order to develop the simulation model. The simulation model for the UNI-VSC is based on the power flow and voltage range considerations presented in [15] and on the exemplary voltage rating of the transformer primary/secondary winding as well as the number of primary N_{prm}, and secondary N_{sec} turns given in [11] and table I. The UNI-VSC allows a unidirectional active power flow, full reactive power flow and control of the voltage within the constrains of the unidirectional active power flow region as shown in [15]. Further advantages of the UNI-VSC are the low number of active switches due to the passive rectifier. With a passive rectifier also a simpler closed loop control strategy is possible [16]. A 2-level topology is assumed for the UNI-VSC as well as IGBTs are chosen as switches. With IGBTs the switching frequency f_{sw} is limited to a range of a few kHz, in order to keep the switching losses low. The current rating of the semiconductors is determined with the nominal current I_{s} of the MV grid, which is calculated based on the nominal power P_{n} of the power transformer and the nominal secondary winding voltage $V_{\mathrm{s,w}}$.

The passive rectifier is connected to the power transformer auxiliary winding terminals A1a-A1c and the inverter is in series to the transformer secondary winding terminals S2a-S2c (see Fig. 1 & 2). The auxiliary and the secondary windings are modeled by the equivalent voltage sources $v_{\mathrm{th,aux/sec}}$ and the inductances $L_{\mathrm{eq}}^{\mathrm{aux/sec}}$. To limit the harmonic injection of the inverter a LC-filter with filter elements L_{f} and C_{f} is included between the inverter and the secondary winding terminals S2a-S2c. The secondary winding terminals S1a-S1c are connected to the load R_{L}.

In a first step only, the inverter side of the UNI-VSC is considered and the DC-link capacitors in Fig. 2 are replaced by a constant voltage source $V_{\mathrm{dc,min}}$. Based on the considered voltage source inverter (VSI) a controller and a plant model are derived in the following section. The controller model is used for controlling the filter capacitance voltages $v_{\mathrm{C,f}}$ of the UNI VSC shown in Fig. 2 and to investigate the advantages of active damping to limit the fault current in case of a single line to ground fault.

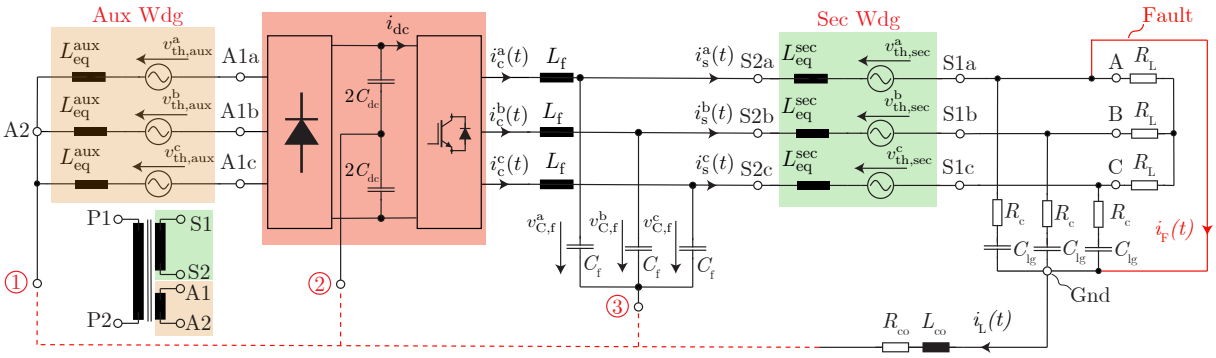

Figure 2: UNI-VSC with MV grid connected to load R_L and the considered grounding points ①-③, where a single line to ground fault is assumed in line "a".

2.1 Plant Model

The plant model for the VSI is derived to design the controller including active damping to limit the single line to ground fault current, by averaging the state space models of the VSI switching states. As PWM strategy space vector modulation (SVM) is chosen. Since the averaged state space model is transferred into dq-domain only a single sector of the SVM hexagon needs to be considered [17]. Within the considered sector the state space matrices are averaged to obtain the averaged state space model based on three phase quantities. Based on the obtained averaged state space model and states i_c^a,...,i_c^c, i_s^a,...,i_s^c, and $v_{C,f}^a$,...,$v_{C,f}^c$ (Fig. 2) the averaged state space model in dq-domain is derived [18]. Transferring the averaged state space model from the dq-domain into the Laplace domain results in the averaged state space model in (1).

$$\underbrace{\begin{bmatrix} s & -\omega & 0 & 0 & \frac{1}{L_f} & 0 \\ \omega & s & 0 & 0 & 0 & \frac{1}{L_f} \\ 0 & 0 & s+\frac{R_L}{L_{eq}^{sec}} & -\omega & -\frac{1}{L_{eq}^{sec}} & 0 \\ 0 & 0 & \omega & s+\frac{R_L}{L_{eq}^{sec}} & 0 & -\frac{1}{L_{eq}^{sec}} \\ -\frac{1}{C_f} & 0 & \frac{1}{C_f} & 0 & s & -\omega \\ 0 & -\frac{1}{C_f} & 0 & \frac{1}{C_f} & \omega & s \end{bmatrix}}_{A_{dq}} \begin{bmatrix} \underline{I}_c^d \\ \underline{I}_c^q \\ \underline{I}_s^d \\ \underline{I}_s^q \\ \underline{V}_{C,f}^d \\ \underline{V}_{C,f}^q \end{bmatrix} = \begin{bmatrix} \frac{\underline{V}_{ref}^d(s)}{L_f} \\ \frac{\underline{V}_{ref}^q(s)}{L_f} \\ \frac{\underline{V}_{th,sec}^d(s)}{L_{eq}^{sec}} \\ \frac{\underline{V}_{th,sec}^q(s)}{L_{eq}^{sec}} \\ 0 \\ 0 \end{bmatrix} \tag{1}$$

By inverting matrix A_{dq} the plant model is obtained to calculate the filter capacitance voltages $\underline{V}_{C,f}^d$ and $\underline{V}_{C,f}^q$ based on the secondary winding voltages $\underline{V}_{th,sec}^d$ and $\underline{V}_{th,sec}^q$ and the reference voltages $\underline{V}_{ref}^d$ and $\underline{V}_{ref}^q$. The plant model for the VSI is shown in Fig. 3a). The plant models to calculate the remaining states in (1) are derived in a similar way. The plant models are utilized to determine the controller variables and the feed forward to damp the filter resonance with active damping.

2.2 Power Transformer Model

For numerical simulations of the UNI-VSC, including the dynamic behavior of the control and plant model, the power transformer needs to be included in the simulation models. The power transformer's auxiliary and secondary windings are modeled by eq. circuits consisting of voltage sources $V_{th,i}$ and inductors L_{eq}^i with $i \in \{sec, aux\}$ in order to increase the simulation speed. To determine the voltage sources $V_{th,i}$ and the inductors L_{eq}^i, the turn numbers of primary and secondary winding N_{prm} and N_{sec} are assumed as described in [11]. The T-equivalent circuit from the primary to secondary winding to derive the eq. voltage source $V_{th,sec}$ and inductor L_{eq}^{sec} is shown in Fig. 3b). In the simulation model the transformer is then represented at the transformer secondary winding terminals S1 and S2 by the eq. voltage source $V_{th,sec}$ and inductor L_{eq}^{sec} shown in Fig. 3c). The calculation of the parameters for the T-equivalent circuits is only explained for the primary to secondary winding T-equivalent circuit since the T-equivalent circuit for the primary to auxiliary winding is calculated in the same way. The T-equivalent circuit is derived with the mutual inductances $L_{n_p n_s}$ of a single primary turn to a single secondary turn, the primary turns self inductance $L_{n_p n_p}$, and secondary turns self inductance $L_{n_s n_s}$ as well as the number

of primary turns N_{prm}, and the secondary turns N_{sec} with (2)-(4). Note that inductances $L_{\mathrm{n_p n_s}}$, $L_{\mathrm{n_p n_p}}$, and $L_{\mathrm{n_s n_s}}$ are calculated with FEM simulations as described in [11].

$$L_{\mathrm{p}} = N_{\mathrm{prm}}[L_{n_{\mathrm{p}}n_{\mathrm{p}}} + (N_{\mathrm{prm}} - 1)L_{n_{\mathrm{p}}n_{\mathrm{p}}+1}] - L_{\mathrm{m}}^{\mathrm{ps}} \tag{2}$$

$$L_{\mathrm{m}}^{\mathrm{ps}} = L_{n_{\mathrm{p}}n_{\mathrm{s}}} N_{\mathrm{prm}} N_{\mathrm{sec}} \tag{3}$$

$$L_{\mathrm{s}} = N_{\mathrm{sec}}[L_{n_{\mathrm{s}}n_{\mathrm{s}}} + (N_{\mathrm{sec}} - 1)L_{n_{\mathrm{s}}n_{\mathrm{s}}+1}] - L_{\mathrm{m}}^{\mathrm{ps}} \tag{4}$$

With inductances L_{p}, $L_{\mathrm{m}}^{\mathrm{ps}}$, and L_{s}, inductance $L_{\mathrm{eq}}^{\mathrm{sec}}$ is calculated as given in (5). The value of the eq. voltage $V_{\mathrm{th,sec}}$ is based on the assumption that the HT auxiliary converter operates at nominal power. Further it is assumed that the power at terminals S1a-S1c is limited to the nominal power P_{n} of the power transformer. Therefore, the eq. voltage $V_{\mathrm{th,sec}}$ is given by $V_{\mathrm{th,sec}} = V_{\mathrm{s,w}} = V_{\mathrm{s}} - V_{\mathrm{s,c}}$. With voltage $V_{\mathrm{th,sec}} = V_{\mathrm{s,w}}$ the voltage $V_{\mathrm{th,aux}}$ on the transformer's auxiliary winding side is calculated from the primary to secondary T-equivalent circuit and the primary to auxiliary winding T-equivalent circuit by (6). Inductances $L_{\mathrm{m}}^{\mathrm{pa}}$ and L_{a} are calculated by replacing N_{sec} with N_{aux}, $L_{\mathrm{n_p n_s}}$ with $L_{\mathrm{n_p n_a}}$, and $L_{\mathrm{n_s n_s}}$ with $L_{\mathrm{n_a n_a}}$ in (2)-(4). Inductance $L_{\mathrm{eq}}^{\mathrm{aux}}$ is then determined by replacing $L_{\mathrm{m}}^{\mathrm{ps}}$ and L_{s} in (5) with inductances $L_{\mathrm{m}}^{\mathrm{pa}}$ and L_{a} for the primary to auxiliary winding. Note that the number of auxiliary turns N_{aux} is determined in **section 2.5**.

$$L_{\mathrm{eq}}^{\mathrm{sec}} = L_{\mathrm{s}} + \frac{L_{\mathrm{p}} L_{\mathrm{m}}^{\mathrm{ps}}}{L_{\mathrm{m}}^{\mathrm{ps}} + L_{\mathrm{p}}} \tag{5}$$

$$V_{\mathrm{th,aux}} = \frac{L_{\mathrm{m}}^{\mathrm{pa}}}{L_{\mathrm{m}}^{\mathrm{pa}} + L_{\mathrm{p}}} \frac{L_{\mathrm{m}}^{\mathrm{ps}}}{L_{\mathrm{m}}^{\mathrm{ps}} + L_{\mathrm{s}}} V_{\mathrm{s,w}} \tag{6}$$

2.3 LC filter Model

With the *LC*-filter at the output of the VSI the harmonic content injected by the converter is limited. Due to the inductance $L_{\mathrm{eq}}^{\mathrm{sec}}$ of the secondary winding, which is in series to the VSI/*LC*-filter, a simple *LC*-filter is sufficient for limiting the harmonics as shown in Fig. 2. The model of the *LC*-filter is based on the *LCL*-filter design scheme given in [19] with base impedance $Z_{\mathrm{b}} = \frac{(V_{\mathrm{c,s}})^2}{P_{\mathrm{n}}}$ and base capacitance $C_{\mathrm{b}} = \frac{1}{\omega_{\mathrm{g}} Z_{\mathrm{b}}}$. The filter capacitance C_{f} is calculated from the base capacitance C_{b} with $C_{\mathrm{f}} = 0.05 C_{\mathrm{b}}$. In order to determine the filter inductance L_{f} the maximum ripple current I_{rip} is defined with the nominal grid current I_{s} by $I_{\mathrm{rip}} = 0.1 I_{\mathrm{s}}$. The filter inductance is then calculated by $L_{\mathrm{f}} = \frac{V_{\mathrm{dc,min}}}{6 f_{\mathrm{sw}} I_{\mathrm{rip}}}$.

2.4 Controller Model

The controller model for the VSI in *dq*-domain is based on a PI controller with a feed forward of voltages $\underline{V}_{\mathrm{C,f}}^{\mathrm{d}}$ and $\underline{V}_{\mathrm{C,f}}^{\mathrm{q}}$. The feed forward of voltages $\underline{V}_{\mathrm{C,f}}^{\mathrm{d}}$ and $\underline{V}_{\mathrm{C,f}}^{\mathrm{q}}$ with parameter K_{d} actively damps the resonance in the *LC*-filter [20]. The controller model is shown in Fig. 3a). The PI controller parameters K_{p} and K_{I} and the feed forward parameter K_{d} are determined with the open loop control transfer function consisting of the *d*-axis PI controller with feed forward K_{d} and the transfer function given by $[A^{dq}]^{-1}(5,1)$. Note that the active damping in the controller model shown in Fig. 3a) is important for limiting the fault current with grounding point ③ as explained in **section 3**.

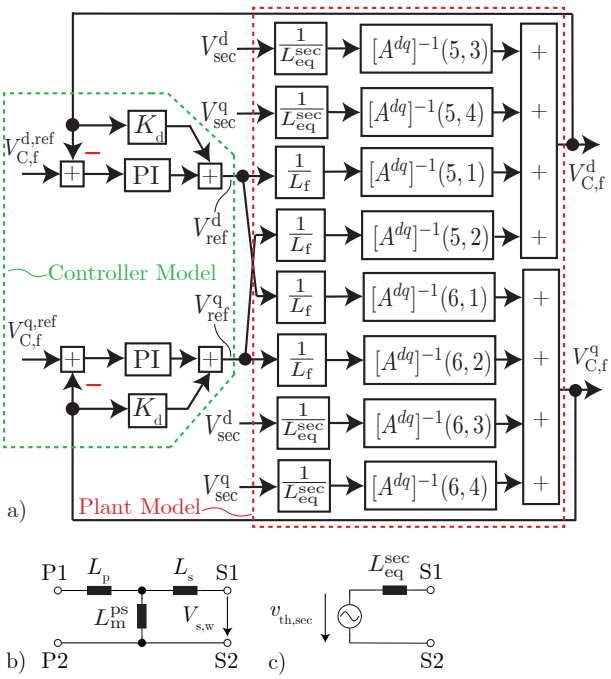

Figure 3: a) Controller and plant model for the VSI. b) T-equivalent circuit of the transformer primary and secondary winding. c) Eq. circuit representing the transformer at the secondary winding terminals S1 and S2.

2.5 DC-Link Model

To implement the simulation model including the passive rectifier and the auxiliary winding, the DC-link capacitance C_{dc} is determined based on the required DC-link voltage $V_{\mathrm{dc,min}}$ of the VSI as discussed in

the following. First the DC-link voltage $V_{\mathrm{dc,min}}$ is determined with the converter current I_{c} at the nominal current I_{s} of the considered MV grid. There, the nominal current I_{s} is simply calculated with the rated power of the transformer P_{n} and the nominal secondary winding voltage $V_{\mathrm{s,w}}$. The converter voltage $V_{\mathrm{s,c}}$ is then determined so that, the chosen voltage range of $V_{\mathrm{C,f}} \approx 13\%$ of voltage $V_{\mathrm{s,w}}$ is achieved taking also the voltage drop across the *LC*-filter into account. The minimum DC-Link voltage $V_{\mathrm{dc,min}}$ is then determined with voltage $\hat{v}_{\mathrm{c,s}}$ including a small margin to avoid over modulation in practical cases.

With the determined DC-link voltage $V_{\mathrm{dc,min}}$, the current i_{dc} through the DC-voltage source $V_{\mathrm{dc,min}}$ of the VSI in Fig. 4a) is analyzed in a next step, in order to simplify determining the DC-link capacitance C_{dc}. For the design of C_{dc} the inverter is modeled by resistance R_{dc} connected to C_{dc} via switch S_{dc} as shown in Fig. 4b). The resistance value R_{dc} is calculated as follows. For determining R_{dc} the averaged DC-current $I_{\mathrm{dc}}^{\mathrm{avg}}$ of the VSI is required. This current is shown qualitatively in Fig. 4a). Resistor R_{dc} models the discharging of the DC-link during the time interval $d_0 T_{\mathrm{s}} \leq t \leq T_{\mathrm{s}}$ of the non zero space vectors. Therefore, the averaged DC-current $I_{\mathrm{dc,act}}^{\mathrm{avg}}$ in Fig. 4a) is determined in (7) with the duty cycles d_1 and d_2 of the non zero space vectors. The resistance R_{dc} is then obtained as $R_{\mathrm{dc}} = \frac{V_{\mathrm{dc,min}}}{I_{\mathrm{dc,act}}^{\mathrm{avg}}}$.

$$I_{\mathrm{dc,act}}^{\mathrm{avg}} = \frac{I_{\mathrm{dc}}^{\mathrm{avg}}}{d_1 + d_2} \quad (7) \qquad i_{\mathrm{L_{dc}}} = \frac{V_{\mathrm{rect,avg}} d}{R_{\mathrm{dc}}} \quad (8) \qquad v_{\mathrm{rip}} = \frac{1}{C_{\mathrm{dc}}} \int_0^{(1-d)T_{\mathrm{s}}} i_{\mathrm{L_{dc}}} \mathrm{d}t \quad (9)$$

With the value for R_{dc} the DC-link capacitor C_{dc} is determined with the equivalent circuit shown in Fig. 4b). There, the resistor R_{dc} is connected in parallel to the DC-link capacitor by switch S_{dc}, which is turned on for the duty cycle $d = d_1 + d_2$ shown in Fig. 4a). The passive rectifier of the UNI-VSC is represented by the voltage source $V_{\mathrm{rect,avg}}$ and inductor $L_{\mathrm{eq}}^{\mathrm{dc}}$. Inductor $L_{\mathrm{eq}}^{\mathrm{dc}} = 2L_{\mathrm{eq}}^{\mathrm{aux}}$ is determined with inductors $L_{\mathrm{eq}}^{\mathrm{aux}}$ in Fig. 2. With voltage $V_{\mathrm{rect,avg}}$, duty cycle d, and resistor R_{dc} the DC-link capacitance C_{dc} is calculated with current $i_{\mathrm{L_{dc}}}$ given in (8). For the time interval $0 \leq t \leq d_0 T_{\mathrm{s}}$ in Fig. 4a) the current through the inductor $L_{\mathrm{eq}}^{\mathrm{dc}}$ and the capacitance C_{dc} are identical. Therefore, the voltage ripple v_{rip} in voltage v_{dc} is determined by integrating the current $i_{\mathrm{L_{dc}}}$ as shown in (9). Solving the integral and rearranging yields the DC-link capacitance C_{dc} in (10), which is similar to the expression for the input capacitance of a single phase buck regulator in [21]. In order to solve (10) for C_{dc} a maximum voltage ripple of v_{rip} and voltage $V_{\mathrm{rect,avg}} = \frac{2\sqrt{3}}{\pi}(V_{\mathrm{dc,min}} + v_{\mathrm{rip}})$ are assumed. Note that the voltage v_{rip} only describes the ripple caused by the switching of the VSI. In the derivation of C_{dc}, the smoothing by C_{dc} of the passive rectifier voltage v_{rect} in Fig. 4c) is neglected for simplicity. Therefore, there is a margin between the minimum voltage shown in Fig. 4c) and the actual minimum voltage. Since the focus is on the selection of grounding points a more detailed modeling of the DC-link is out of scope of this paper.

$$C_{\mathrm{dc}} = \frac{V_{\mathrm{rect,avg}} d (1-d) T_{\mathrm{s}}}{v_{\mathrm{rip}} R_{\mathrm{dc}}} \quad (10) \qquad V_{\mathrm{aux}} = \frac{V_{\mathrm{rect,avg}} \pi}{3\sqrt{2}} \quad (11) \qquad N_{\mathrm{aux}} = \frac{N_{\mathrm{prm}} V_{\mathrm{aux}}}{V_{\mathrm{p}}} \quad (12)$$

With the voltage $V_{\mathrm{rect,avg}} = \frac{2\sqrt{3}}{\pi}(V_{\mathrm{dc,min}} + v_{\mathrm{rip}})$, the required RMS voltage of the voltage V_{aux} for the auxiliary winding side of the UNI-VSC is calculated as given in (11). Further, the number of turns N_{aux} for the auxiliary winding is given by (12).

With the auxiliary converter voltage $V_{\mathrm{s,c}}$, the DC-link voltage $V_{\mathrm{dc,min}}$, and the number of auxiliary winding turns N_{aux}, the UNI-VSC simulation model is defined for investigating the grounding points for the cases ①-③. The results are presented in **section 4**.

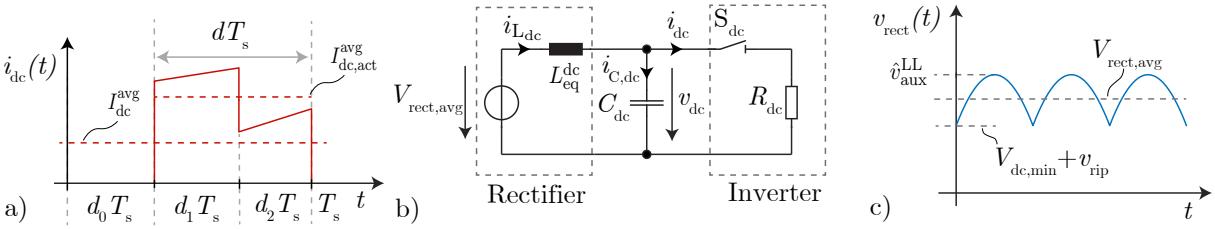

Figure 4: a) Wave form of the DC-link current i_{dc} in the VSI. b) Eq. circuit to design the DC-link capacitance of the UNI-VSC. c) Rectified voltage of the passive rectifier in the UNI-VSC.

3 Grounding Points in Unidirectional VSC

The grounding points ①-③ are investigated based on the developed simulation model in **section 2**. In order to evaluate the grounding points ①-③ the line to ground capacitances $C_{\mathrm{l,g}}$ of a MV grid line are added to the UNI-VSC model in Fig. 2. The values of the line to ground capacitances $C_{\mathrm{l,g}}$ are calculated from the per length capacitance $C'_{\mathrm{l,g}}$ of the considered line and the grid line length l.

The single line to ground fault with short circuit current i_{F} is assumed to occur in phase "a" as shown in red in Fig. 2. The resistances R_{c} in series to capacitances $C_{\mathrm{l,g}}$ are introduced to avoid numeric problems in the simulation due to the short circuit of the line to ground capacitance $C_{\mathrm{l,g}}$ in phase "a" in an event of a single line to ground fault. Note that the star point of the load R_{L} needs to be isolated in order to limit the fault current to an acceptable level for the UNI-VSC in an event of a single line to ground fault. A load with isolated star point is typically given in case of a HV/MV HT connected to MV line, that is connected to a MV/LV distribution transformer with isolated neutral point [14]. To compensate the fault current i_{F} through the line to ground capacitors C_{lg}, a grounding inductor L_{co} is usually inserted. The grounding inductor L_{co} is designed dependent on the grid line length with $L_{\mathrm{co}}(l) = \frac{1}{3\omega_{\mathrm{g}}^2 C_{\mathrm{l,g}}(l)}$ [14]. In a next step, the grounding points ①-③ are investigated for the grounding inductor L_{co} shown in Fig. 2 .

① In case of grounding point ①, a star connected transformer auxiliary winding is assumed, where the grounding inductor L_{co} is connected to the star point A2 shown in Fig. 2. In case of a single line to ground fault, the converter currents $i_{\mathrm{c}}^{\mathrm{a}},..,i_{\mathrm{c}}^{\mathrm{c}}$ as well as the rectifier currents become unbalanced. Inductances $L_{\mathrm{eq}}^{\mathrm{aux}}$, L_{f} and $L_{\mathrm{eq}}^{\mathrm{sec}}$ limit the fault current i_{F}. In order to decrease the fault current i_{F} further, resistor R_{co} is determined, so that the fault current reaches a steady state value below the allowed residual current i_{res} for MV grids [14]. In case passive damping of the *LC*-filter is chosen with damping resistors in series to the *LC*-filter capacitances C_{f}, grounding point ① is preferred over grounding point ③. With passive damping and the damping resistors grounded with grounding point ③, a fault current above the allowed residual fault current i_{res} is reached as discussed below. A disadvantage of grounding point ① are the extra measures necessary to avoid an undesired charging of the DC-link capacitors. In case the filter capacitance C_{f} voltages $v_{\mathrm{C,f}}$ are controlled close to zero, the current i_{L} starts to charge the DC-link capacitors even in normal operation. The path of i_{L} through the converter is shown in Fig. 5. In case voltage $v_{\mathrm{C,f}} \approx 0$, approximately zero power is provided by the VSI and therefore only the passive rectifier conducts the current i_{L} with a single diode turned on. Due to $v_{\mathrm{C,f}} \approx 0$ the VSI is mainly switched between the zero voltage space vectors (111) and (000) current i_{L} flows through the DC-link capacitors during the time the zero vector (000) is generated as shown in Fig. 5. In case a fault occurs at $v_{\mathrm{C,f}} \approx 0$ the converter currents $i_{\mathrm{c}}^{\mathrm{a}},..,i_{\mathrm{c}}^{\mathrm{c}}$ become unbalanced including a DC-offset. The DC-offset in converter currents $i_{\mathrm{c}}^{\mathrm{a}},..,i_{\mathrm{c}}^{\mathrm{c}}$ further contributes to charge the DC-link. The charging of the DC-link is avoided with a sufficiently high reference voltage $V_{\mathrm{C,f}}^{\mathrm{d,ref}}$ so that active power is transferred, which allows to balance the charging of the DC-link by current i_{L} and the DC-offset in currents $i_{\mathrm{c}}^{\mathrm{a}},..,i_{\mathrm{c}}^{\mathrm{c}}$. For the considered case study HT with the parameters in tables I-III, reference voltages of approximately $100\mathrm{V} \leq V_{\mathrm{C,f}}^{\mathrm{d,ref}}$ and $V_{\mathrm{C,f}}^{\mathrm{q,ref}} \approx 0$ are required to avoid a charging of the DC-link for grounding point ①. To avoid an increase of the DC-link voltage v_{dc} for reference voltages $V_{\mathrm{C,f}}^{\mathrm{d,ref}} < 100\mathrm{V}$ and $V_{\mathrm{C,f}}^{\mathrm{q,ref}} \approx 0$, a resistor can be added in parallel to the DC-link capacitors [22], which leads to additional losses.

② With the second grounding point ② the grounding inductor L_{co} is connected to the split DC-link. In case ②, inductances L_{f} and $L_{\mathrm{eq}}^{\mathrm{sec}}$ limit the fault current i_{F} through the UNI-VSC. Since the fault current i_{F} flows through the DC-link capacitors and the grounding inductor L_{co} oscillations can occur. To damp these oscillations, the value of resistance R_{co} needs to be sufficiently high. Typically the value of R_{co}, for limiting the current i_{F} to a minimum residual fault current i_{res} within the permitted value for MV grids is sufficiently high to also damp the considered resonances. In contrast to grounding point ①, the DC-link voltage remains stable during normal operation with voltages $v_{\mathrm{C,f}} \approx 0$ because the average of current i_{L} through the DC-link capacitors is zero. During a fault with voltages $v_{\mathrm{C,f}} \approx 0$ the unbalanced currents $i_{\mathrm{c}}^{\mathrm{a}},..,i_{\mathrm{c}}^{\mathrm{c}}$ lead to an increase of the DC-link voltage v_{dc} due to a DC-offset in $i_{\mathrm{c}}^{\mathrm{a}},..,i_{\mathrm{c}}^{\mathrm{c}}$. The charging of the DC-link is avoided with a sufficiently high reference voltage $V_{\mathrm{C,f}}^{\mathrm{d,ref}}$ so that active power is transferred, what allows to balance the charging of the DC-link by the DC-offset in currents $i_{\mathrm{c}}^{\mathrm{a}},..,i_{\mathrm{c}}^{\mathrm{c}}$. For the case study HT with the parameters in tables I-III, the DC-link voltage remains constant during the fault for reference voltages $5\mathrm{V} \leq V_{\mathrm{C,f}}^{\mathrm{d,ref}}$ and $V_{\mathrm{C,f}}^{\mathrm{q,ref}} \approx 0$. For reference voltages $V_{\mathrm{C,f}}^{\mathrm{d,ref}} < 5\mathrm{V}$ and $V_{\mathrm{C,f}}^{\mathrm{q,ref}} \approx 0$ the increase of the DC-link voltage can be solved by adding parallel resistors to the DC-link capacitances as discussed in [22], which leads to additional losses.

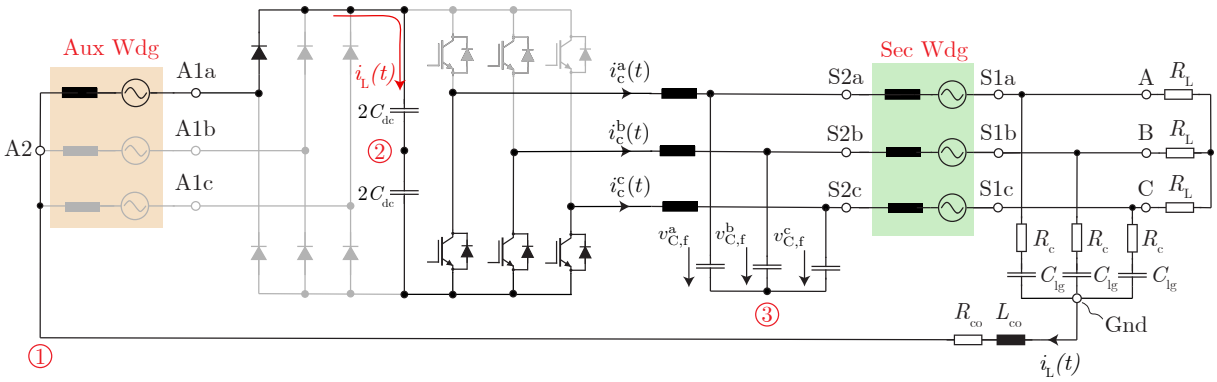

Figure 5: Flow of current i_L during zero space vector $\underline{V}_{(000)}$ with reference voltages $V_{C,f}^{d,ref} = V_{C,f}^{q,ref} = 0$ during normal operation and with grounding point ①

③ The third grounding point ③ is given by connecting the grounding inductor L_{co} to the star connected LC-filter capacitors C_f as shown in Fig. 2. Since the grounding inductor L_{co} is connected to the LC-filter no fault current i_F flows through the converter. However, the fault current i_F flows through the resonant tank consisting of the grounding inductor L_{co} and the filter capacitors C_f, which could lead to oscillations without sufficient damping. In case a passive damping strategy is chosen, the damping resistors in series to the filter capacitances C_f lead to a residual current i_{res} larger than the desired value in MV grids in case of a single line to ground fault with inductor L_{co} and resistor R_{co} connected to grounding point ③. The reason for the high residual current i_F is that the damping resistors lead to a current component that is not compensated by the grounding inductor L_{co}. This is also explained by considering the damping resistors in combination with the load resistors as an unbalanced resistive load, while the line to ground capacitances are compensated by inductor L_{co} during the fault. As a consequence, passive damping leads to unbalanced converter currents i_c^a,...,i_c^c during a fault. Therefore active damping is investigated for grounding point ③, to eliminate the damping resistors of the LC-filter for passive damping. The controllers active damping leads to a residual fault current i_{res} well below the permitted value for MV grids. Furthermore, with active damping the unbalance of the converter currents i_c^a,...,i_c^c is very limited since the value of R_{co} is low in order to achieve a short time for current i_F to reach its steady state value. Another advantage that comes with grounding location ③ is that no DC-link charging occurs due to the very limited unbalance of currents i_c^a,...,i_c^c. This allows to use a simple dq-domain control strategy for the normal and fault operation.

For the reasons mentioned above and as will be shown in **section 4**, the advantages of grounding point ③ compared to grounding points ① & ② are significant. Therefore, grounding points ① & ② are not considered in more detail in this paper.

4 Results and Discussion

Based on **section 3** only results for grounding point ③ are presented in the following. The advantages of active damping during a fault with grounding point ③ is shown for two operation points I & II in Fig. 6. Note that operation points I & II are normal non fault operation points for HT. At operation point I a lower voltage of the secondary winding voltage $V_{s,w}$ is assumed, where the HT auxiliary converter compensates, such that the auxiliary converter voltage $V_{s,c}$ and the secondary winding voltage $V_{s,w}$ add up to the nominal voltage $V_{s,N}$. At operation point I the auxiliary converter current I_c is at its nominal value $I_{c,N}$. Therefore, the highest over current is expected during a single line to ground fault at operation point I. At operation point II illustrated at the bottom of Fig. 6 the auxiliary converter voltage is $V_{s,c} = 0$ and the secondary winding voltage is $V_{s,w} = V_{s,N}$, while the auxiliary converter current I_c is close to its

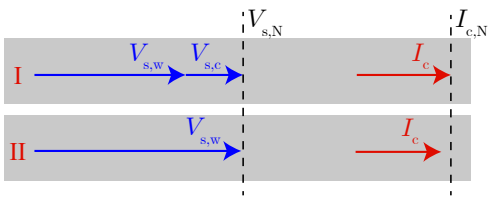

Figure 6: Voltages and currents at operation points I & II of the UNI-VSC for grounding point ③.

nominal value $I_{c,N}$. Operation point II is critical to maintain a stable DC-link voltage v_{dc} for grounding points ① & ② and is therefore investigated during a single line to ground fault with grounding point ③.

Grounding point ③ is investigated for a case study HV/MV HT with basic parameters listed in tables I and II. Since fault currents i_F in cable grids are significantly higher than in overhead line grids [11], only cable grids are investigated. The nominal load resistance R_L is calculated with the nominal current I_s and secondary winding voltage $V_{s,w}$ as R_L=8.9Ω. Further simulation parameters are $L_{eq}^{sec} = 9.1$mH and $L_{eq}^{aux} = 0.24$mH for the inductances in the eq. circuits of the secondary and auxiliary winding calculated with (5). The values for the grid frequency f_g, switching frequency f_{sw}, the DC-link capacitor C_{dc}, the grounding inductor L_{co}, the *LC*-filter as well as the resistors R_{co} and R_c are given in tables I and II.

P_n	V_p	$V_{s,w}$	V_{aux}	I_s	L_{co}	R_{co}	$C'_{l,g}$	R_c	N_{prm}	N_{sec}	N_{aux}
45MW	110kV	20kV	3kV	1.3kA	0.27H	1.35Ω	250nF/km	0.1mΩ	1518	276	41

Table I: General design parameters for the case study HT and the reactance grounded grid.

The converter currents i_c^a,...,i_c^c and fault current i_F for operation points I & II are determined for a cable line length of l =50km, where a single line to ground fault occurs after $t = 4\text{min} = 240\text{s}$. Note, that the converter currents i_c^a,...,i_c^c increase linearly with increasing cable line length l. The reason for investigating the cable line length l of 50km is that the converter currents i_c^a,...,i_c^c reach the nominal converter current $\hat{i}_{c,nom}$ at a line length of l =50km. According to [14], the steady state fault current i_F should not exceed the residual current i_{res} of 60A in MV grids. In cases I & II resistor R_{co} in table II is designed to insure a steady state fault current i_F below the residual current i_{res} of 60A with a settling time of $t_{set} \approx$1s in case of a fault. Since the value of resistance R_{co} is dependent on the settling time t_{set} the chosen value for t_{set} is a compromise between a fast settling time and a low resistance R_{co} to obtain a low unbalance in the converter currents i_c^a,..,i_c^c during a fault. The values of voltages $V_{th,sec}$ and $V_{th,aux}$ and the reference voltages $V_{C,f}^{d,ref}$ and $V_{C,f}^{q,ref}$ for the controller are listed in table III for operation points I & II.

$V_{s,c}$	f_g	f_{sw}	C_{dc}	$V_{dc,min}$	$V_{dc,max}$	L_f	C_f	v_{rip}
2.5kV	50Hz	3kHz	30.9mF	3.57kV	4.2kV	1.1mH	143.2μF	1V

Table II: Parameters for the UNI-VSC including the DC-link and the *LC*-filter of the case study HT.

4.1 Results

Results for operation point I are shown in Fig. 7. After the fault occurs, the UNI-VSC converter current i_c^a reaches a maximum value of 117% of the nominal peak current $\hat{i}_{c,nom}$ as shown in Fig. 7a) & b). From its maximum value current i_c^a drops to a value close to the nominal peak current $\hat{i}_{c,nom}$. After a settling time of $t_{set} \approx$ 1s currents i_c^a,..,i_c^c maintain a peak value very close to the peak value before the fault, with a negligible unbalance caused by resistor R_{co}. The fault currents i_F at operation points I & II are very similar in terms of shape and maximum peak values. Therefore, only the fault current i_F at operation point I is shown in Fig. 7c). With active damping the fault current decreases after the fault within the settling time of t_{set}. In steady state the fault current i_F reaches a peak value of $\hat{i}_F \approx$15.3A.

For operation point II, the converter currents before and after the fault are shown in Fig. 8 a) & b). The converter currents i_c^a reaches a peak current of 113% of the nominal peak current $\hat{i}_{c,nom}$ after the fault. As with operation point I currents i_c^a,..,i_c^c drop within a settling time of $t_{set} \approx$ 1s to a peak value close to

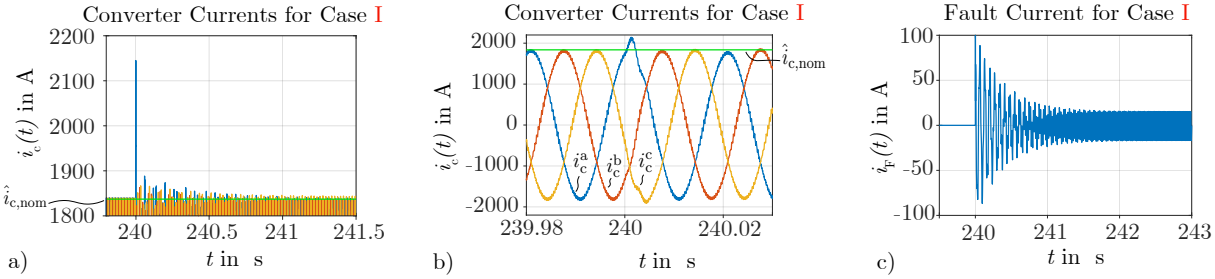

Figure 7: Operation point I: a) Converter currents i_c^a,..,i_c^c during the fault. b) Converter currents i_c^a,..,i_c^c during the fault in higher resolution. c) Fault current i_F.

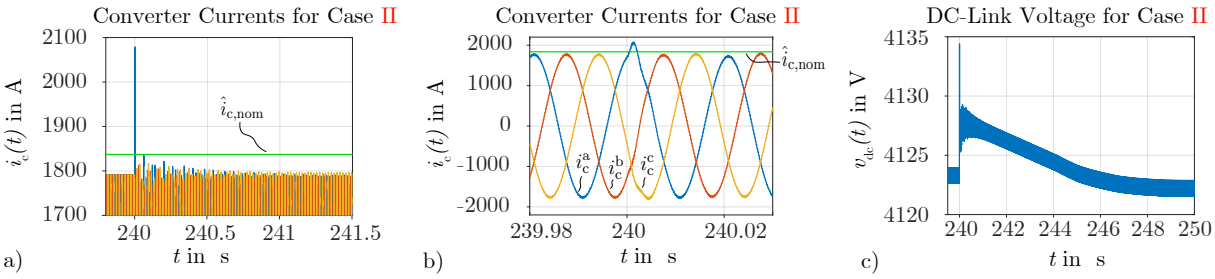

Figure 8: Operation point II: a) Converter currents i_c^a,..,i_c^c during the fault. b) Converter currents i_c^a,..,i_c^c during the fault in higher resolution. c) DC-link voltage during the fault.

the peak value before the fault, with a negligible unbalance caused by resistor R_{co}. Comparing currents i_c^a,..,i_c^c at operation points I & II the shapes of the currents in Fig. 7b) are slightly different as in Fig. 8b) due to the difference in reference voltages $V_{C,f}^{d,ref}$ and $V_{C,f}^{q,ref}$ in table III.

	$V_{th,sec}$	$V_{th,aux}$	$V_{C,f}^{d,ref}$	$V_{C,f}^{q,ref}$
I	18kV	2.67kV	1.75kV	-1.2kV
II	20kV	3kV	0V	0V

Table III: Secondary winding voltage, auxiliary winding voltage, and reference voltages for the case study HT at operation points I & II.

Results for the DC-link voltage v_{dc} during a fault at operation point II with grounding point ③ are shown in Fig. 8c). The DC-link voltage v_{dc} increases to a maximum voltage of $v_{dc} \approx 4.14$kV at the time instant of the fault. After the fault the DC-link voltage v_{dc} settles to a stable voltage of $v_{dc} \approx 4.12$kV. Based on the results for the DC-link voltage v_{dc} in Fig. 8c) the maximum DC-link voltage $V_{dc,max}$ is given in table II.

4.2 Discussion

Due to active damping grounding point ③ is preferred. In case of passive damping only grounding points ① & ② limit the fault current to an acceptable level in MV grids. But additional measures are required to limit the UNI-VSC DC-link voltage v_{dc} for certain operation points with grounding points ①& ②. With grounding point ③ the DC-link voltage remains stable during a fault and normal operation. The advantage of grounding point ③ limiting the fault current and the DC-link voltage is shown for two operation points I & II. Since grounding point ③ is chosen, only a negligible unbalance remains in the converter currents after the fault, while the fault current i_F almost entirely flows through the transformer secondary winding and the filter capacitances C_f in contrast to the other grounding points. Furthermore, active damping allows the fault current to drop to a residual value i_{res} of less than 60A, which is required for MV grids.

5 Conclusion

This paper provides a comprehensive evaluation of possible grounding points in HT. Three possible grounding points are identified and compared for a HT with unidirectional auxiliary converter. Simulation models for the unidirectional HT auxiliary converter are derived based on state space averaging and equivalent circuits for the power transformer. Furthermore simulation results for the preferred grounding point ③ at different operation points are presented. With active damping, the single line to ground fault current for grounding point ③ is reduced below the allowed residual fault current for MV grids.

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