A Novel Technique for the Suppression of the Displacement Current through Power Module Base-plate Capacitance

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Abstract

The voltage gradient is increased to reduce the switching losses in the wide-bandgap (WBG) semiconductors, which causes the higher power density of the system. Fast rise and fall times during switching of WBG semiconductors result in capacitive non-linearities and displacement currents through power module parasitic capacitances, which needs an appropriate filter design During the switching in the power module, the capacitive current flows through the parasitic capacitance of the power module, which causes the disturbances in the system. This leads to the need for a more oversized filter design, which then increases the overall cost and volume of the system and reduces the efficiency of the system. This paper proposes a novel technique to suppress the capacitive displacement currents without switching speed reduction. The proposed method reduces the volume of the common-mode choke (CMC) and addresses the electromagnetic interference (EMI) and electromagnetic compatibility (EMC) issues. The system was experimentally tested using the commercial 1700 V silicon carbide (SiC) half-bridge power module BSM300D12P2E001 to validate the proposed scheme.

Introduction

Achieving a higher power density with lower switching losses has always been a challenge in WBG semiconductor devices. A higher switching speed results in an increase in the displacement current through multi-chip power module (MCPM) parasitic capacitances in the WBG semiconductors. The significant increase in the displacement current causes more electromagnetic interference (EMI) and electromagnetic capability (EMC) problems in high-frequency applications. Therefore, the EMI/EMC problem is a great challenge in WBG-based applications. To overcome this problem, many researchers have already proposed different methodologies to design the common-mode choke (CMC) filters. The switching behavior of semiconductors has to be considered, which affects the overall filter design procedure. Minimizing the size, volume, and cost of the EMI filter is known as the dominant target in the EMI/EMC considerations. Moreover, the EMI filter components must qualify for the EMC standards and should be avoided to increase the cost and complexity of the overall system. Otherwise, it degrades the convertor efficiency and may need active cooling for high-power applications.

The parasitic capacitance between power module chips and the ground is one of the major contributors to the common-mode (CM) EMI noise in power electronic systems with high dv/dt during switching transients. The capacitive CM or displacement current is generated from the higher dv/dt through the parasitic capacitance and the ground. The parasitic capacitance is intrinsic to the power module and cannot be modified. It is desired to minimize the module parasitic capacitances inside of power modules and smaller direct bonded copper (DBC) dimensions and reduced track widths reduce the total output coupling capacitance [1]. The multi-chip power module packages carry more current and are used for high-power applications. The capacitive coupling between chips on DBC and mounting base-plate is inevitable in the packages and leads to parasitic capacitances, which become charged or discharged during switching. The parasitic capacitances in SiC power modules are due to the chip area being smaller than silicon-based semiconductors. Despite small parasitic capacitances, SiC power modules have higher dv/dt, which causes more capacitive current through capacitances. The displacement current flows through the parasitic capacitance between DBC and the mounting base plate of the power module. The higher the dv/dt will be increased the value of capacitive displacement current significantly. It requires a large EMI filter due to such increasing [2]- [6]. Therefore, proper suppression of the capacitive displacement current is needed to avoid the bulky design of the EMI filters. In the literature review, different methods have been suggested to mitigate the displacement current, which is either complicated to implement or increases the overall cost of the system.

In [7], the authors proposed to place CM filtering capacitors inside the power module close to the noise source, which offers a desirable decrease in the CM noise. The integrated capacitors inside the power module for reducing the CM noise have a major drawback of not withstanding higher junction temperatures of the power module. A separate physical heat sink was used to cancel the displacement current flowing into the grounding system [8], which then increases the overall cost of the system and is not desirable for the power module. This solution is a better choice for the discrete switch where independent heat sinks are needed. The optimized filter design was performed by [9], which has investigated the parasitic parameters in the module and switching cell. The parasitic parameters in the SiC power module have been identified by balancing coupling between the base-plate and the terminals of the module [10]. The CM and differential mode (DM) EMI noises can be effectively attenuated in low and high-frequency ranges by adding decoupling capacitors in the voltage source converter (VSC) [11]. A CM model for a multi-chip power module has been proposed for the EMI issues to identify a method to mitigate the displacement current [12]. The proposed method in [12] placed capacitances between the neutral point and the grounding system. The study refers to the analysis of the CM behavior of an ungrounded WBG-based converter by varying the impedance between the multi-chip module and the grounding structure of the system [13]. A method to design the EMI filter is proposed in [13], once the noise source impedance is determined. Moreover, the model constructs the relationship between the noise source impedance and the passive elements where the equivalent values of the noise source impedance are calculated based on the experimental results [13].

An equivalent modeling approach of the CM is presented in [14], which can mitigate the conducted emissions in WBG-based systems in the frequency range between 10 kHz and 30 MHz. This suggested scheme in [14] is based on the circuit analysis methods and can be implemented with the data obtained from the impedance analyzer. The goal of the approach is to reduce the CM emissions of the power electronic systems [14]. Five cancellation methods for parasitic capacitances have been reviewed and analyzed in [15] where the cancellation frequency ranges are identified and the effective frequency range for each cancellation method is derived based on the constraints. Moreover, using the mutual capacitance the method is suitable for the design of the DM and CM filters [15].

This paper proposes a novel and a simple technique to mitigate the displacement current through the parasitic capacitance between power module chips and the mounting base-plate. The suggested methodology includes the various types of inductors connected in parallel to the parasitic capacitance DC- terminal of the power module and the mounting base-plate. This results in the effective reduction of the displacement current by one-third. Moreover, the implementation of the CMC is compared with the combination of the CMC and inductor connected in parallel to the parasitic capacitances of the power module. In

addition, the experimental results have been compared with the reference in [11]. In [11], where the authors have used an array of ≈ 39 capacitors to attenuate the displacement current, which is bulky and costly. The proposed method is implemented on the double-pulse test (DPT) for the measurement of the displacement current to 800 V drain-source voltage.

Proposed Methodology

To achieve effective suppression of the displacement current, one must consider an equivalent circuit, which shows the origin of the displacement current and its path to flow. The high slew rate of voltage during SiC power module switching is generated more the capacitive displacement current. If the switching speed is kept fixed, one must be concentrated on other possible solutions for more generated displacement current. Multi-chip power module got a large chip area, which results in higher parasitic capacitances, which play a key role in the effect of the displacement current. The proposed method is ongoing about the improvement path of displacement current. In [11], was showed an analytical modeling of a common-mode equivalent circuit for power module and approved, how displacement current changes with total parasitic capacitance adjustment.

As shown in Fig. 1a, is proposed to placement an inductor L_{lb} between the DC- terminal and the base-plate as shown, which affects on displacement current path. The parallel connection of the inductor and base-plate parasitic capacitance expresses a new combination of L and C parameters, which provides a different impedance equivalent circuit and resaults in a new displacement current path. The displacement current exhibits high-frequency oscillations which could affect the performance of inductors. Since some inductors are not suitable for high frequencies and will saturate depending on the core material. Because of that, the inductors are selected from different types, inductances, and core materials. According to their frequency-dependent equivalent circuit, the inductor selection in table I is chosen to use in the setup test. Suppressor chokes $L1$ -$L3$ have different inductances values from 60 to 220 μH and different constructions. $L4$ and $L6$ are called air core inductors, which have a difference in the spacing between the windings. $L4$ and $L6$ have different values of parasitic capacitance between the individual windings due to different distance, resulting in an equivalent impedance circuit for each case. Refer to Fig. 1b, which is the placement of a CMC between DC link and power supply. Furthermore, the CMC windings are rebuilt to use as differential mode Choke $L7$ in Table I. The new proposed path can be used in a real application, whereas the proposed method in [11] how far away is from real hardware application.

Fig. 2 shows the value of the parasitic capacitance between the outputs of the MCPM and arbitrary point P is [11]

$$C_{bp} \approx C_{ub} + c_{ab} + c_{lb} \tag{1}$$

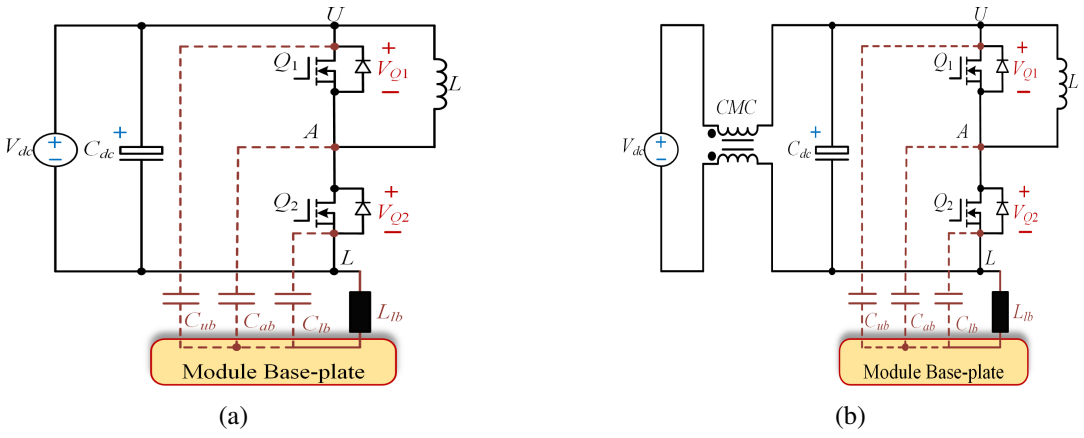


Fig. 1: Equivalent circuit of the SiC multi-chip power module (MCPM) with base-plate parasitic capacitance; (a) without CMC, (b) with CMC

Table I: Inductor Values

Inductors	Values
Suppressor chokes $L1$-$L3$	(60, 150, 220) μH
Big Air core $L4$	4.769 μH
Ferrite core inductor $L5$	2.662 μH
Air core $L6$	2.275 μH
CMC as DM inductor $L7$	3.142 mH

where C_{bp}: total parasitic capacitance between MCPM and mounting base plate.
C_{ub}: parasitic capacitance between DC+ terminal and mounting base plate.
C_{ab}: parasitic capacitance between DC- terminal and mounting base plate.
C_{lb}:parasitic capacitance between AC terminal and mounting base plate.

The total impedance of the parasitic capacitance without using the inductor in parallel to the DC- and the mounting base-plate is

$$Z \approx \frac{Z_{Cbp} \times R_{SHUNT}}{Z_{Cbp} + R_{SHUNT}}. \tag{2}$$

where R_{SHUNT} is used to measure the current. The proposed method suggested is to use the inductor in series to the R_{SHUNT} illustrated in Fig. 3, which changes the total impedance of the parasitic capacitance between the mounting base plate and ground.

$$Z_{new} \approx \frac{Z_{Cbp} \times Z_1}{Z_{Cbp} + Z_1} \tag{3}$$

where $Z_1 = Z_L + R_{SHUNT}$ and Z_L is the impedance of the selected inductors.

Experimental results

Fig. 4 shows the experimental setup of the DPT. The SiC N-canal BSM300D12P2E001 multi-chip power module was chosen for the test. The air core inductor of 245 μH as clamped inductive load was connected for the high side switch. The pulse was given to the low side switch. The displacement current is measured first without any selected inductors using a shunt resistor between the DC- terminal and the base plate as shown in Fig. 1a. The displacement current was measured with and without CMC as shown in Fig. 1 to see the effectiveness of CMC in relation to the use of selected chokes. The DC link voltage

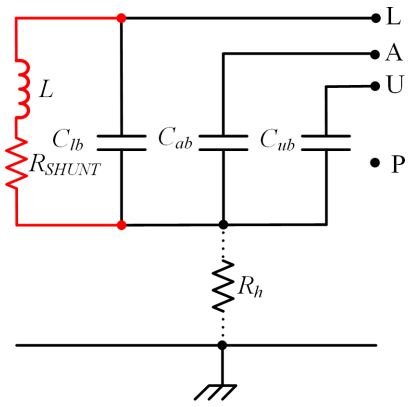


Fig. 2: Parasitic capacitance of MCPM with selected inductor

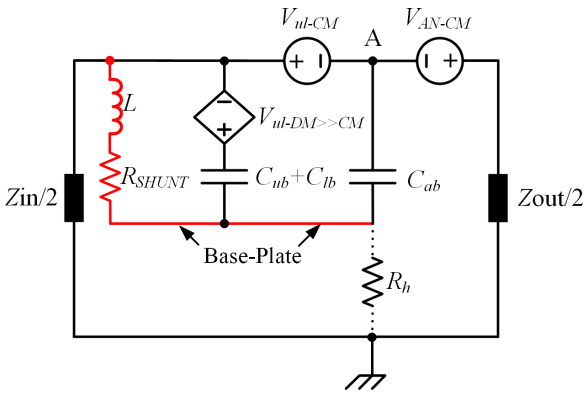
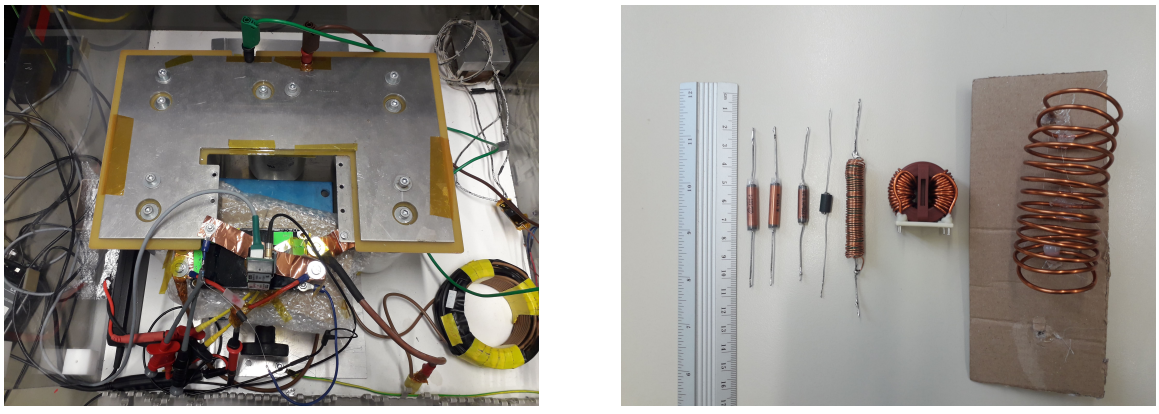


Fig. 3: Common-mode equivalent of half-bridge

was increased in steps of 100 V up to 800 V, which changed dv/dt during power module switching. Fig. 5 shows the experimental results of the drain-source voltage versus the displacement current without the CMC as shown in Fig. 1a.

It shows the implementation of different inductors connected in parallel to the DC- terminal and the power module mounting base plate. The system parameters and the selected inductors are shown in Table I. Fig. 5 shows that the dv/dt is increased and that results in the increase of the displacement current with the higher drain-source voltage (V_{ds}). The displacement current is well suppressed with the inductors of 150 μH and 220 μH compared with other inductors as depicted in Fig. 5. It can be seen that the inductors connected in parallel have mitigated the displacement current from 618 mA to 243 mA at 800 V.

Fig. 6 illustrates the experimental results of the drain-source voltage versus the displacement current where CMC has also been implemented as shown in Fig. 1b. It can be seen that the inductor of 150 μH and 220 μH have mitigated the displacement current better than the other inductors. The combination of the CMC with the inductors in parallel has attenuated the displacement current from 628 mA to 155 mA at 800 V. The displacement current is well attenuated in Fig. 6 as compared to Fig. 5 because of the suppression capability of the CMC filter. As the displacement current is well suppressed maintaining the higher dv/dt with lower switching losses, which results in lower EMI/EMC emissions. Lowering the EMI/EMC emissions assists in the smaller design of the CMC filter, which then helps in reducing the total volume and cost of the system. The results of the proposed technique can be well compared to the results given in [11] wherein [11], they have used an array of around 39 capacitors to suppress the displacement current where we proposed to use a single selected inductor in parallel to the DC- terminal and the intrinsic parasitic capacitance of the base-plate module.



(a) (b)

Fig. 4: Experimental setup; (a) implementation of different inductors under test, (b) selected inductors

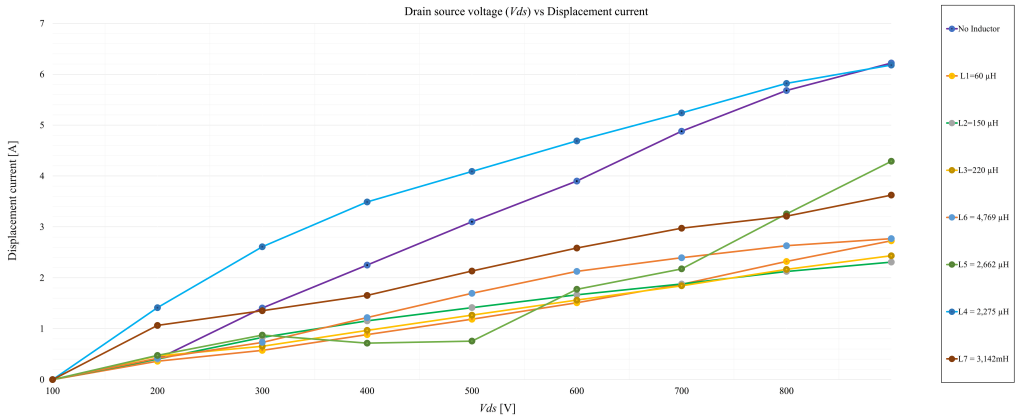


Fig. 5: Drain-source voltage versus displacement current without CMC with the selection of different inductors

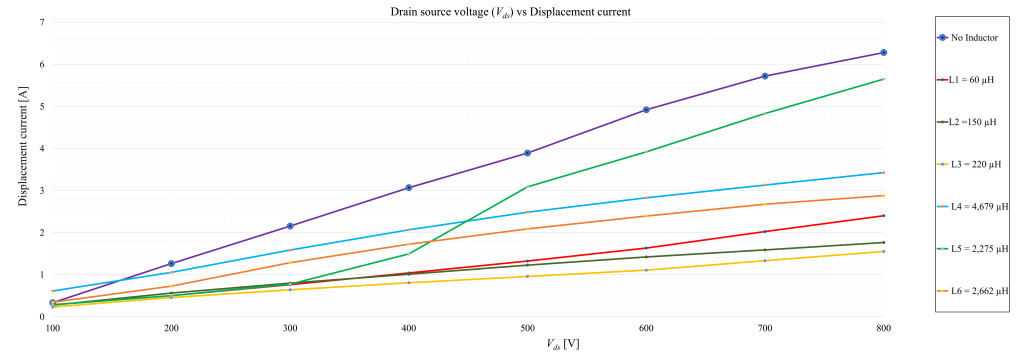


Fig. 6: Drain-source voltage versus displacement current with CMC with the selection of different inductors

Conclusion

The WBG semiconductors such as SiC and GaN are fast switching devices with lower switching losses. The faster switching of the WBG makes higher dv/dt. On the other hand, we have a larger parasitic capacitance base-plate due to the larger area of the power module chip. This results in a higher displacement current, which produces higher EMI/EMC emissions. The suppression of the displacement current needs a bigger filtering system. The proposed technique of connecting a single selected inductor in parallel to the DC-terminal of the module and the base-plate. The experimental results show that the displacement current is well attenuated up to 62.5% without CMC and 75% with CMC. The implementation of the proposed methodology is simple and helps in reducing the overall size, volume, and cost of the system.

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