Implementation of the 160kV High Voltage DC/DC Converter

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***Abstract*-- In this paper, the implementation of 380Vdc to 160kVdc high voltage DC/DC converter is described. The converter was designed based on the parallel loaded resonant converter(PLRC) topology and the parallel-charged symmetrical Cockcroft-Walton voltage multiplier(CWVM). Also, the gate driver was designed for high efficiency operation of PLRC over wide load range. In addition, the high voltage transformer was designed to satisfy the voltage gain, high voltage insulation and required leakage inductance and stray capacitance which are used as resonant inductance and resonant capacitance of the PLRC. The converter has remarkable characteristics such as compact size while considering of high voltage insulation, low output voltage ripple, and long-term stable operation. The converter was verified through PSPICE simulation and experiment. Through simulation, the output of the designed converter was verified, and the loss improvement of the converter switch was analyzed and the output voltage ripple was verified. Finally, the experiment with resistor load was conducted and it was verified that the converter outputs 160kV 6mA.**

***Index Terms*— Cockcroft-Walton voltage multiplier, High voltage DC/DC converter, Parallel resonant converter, Soft switching.**

I. Introduction

Recently, high voltage DC power supply is required in many applications such as X-ray generator, plasma processing, electron beam, and etc.[1]-[3]. To generate high DC voltage, variable DC/DC converter structures have been studied[4]-[12]. For example, it is one of the structure that connects several converters to boost voltage, but in this case, the configuration is not compact and the number of devices increases. Another structure is to use single inverter and extremely high voltage gain transformer. However, the transformer design with extremely high voltage gain and high voltage insulation is so difficult. Also, some applications are sensitive to the output characteristics of high voltage DC power supply, such as overshoot, ripple, and rise time, so it should be considered in design[4].

In this paper, the high voltage DC/DC converter is designed with the parallel loaded resonant converter(PLRC) and the Cockcroft-Walton voltage multiplier(CWVM) to alleviate the difficulty of transformer design. The PLRC not only have boosting voltage gain, but also reduce the switching loss with zero voltage switching(ZVS) turn-on[13]. But the ZVS turn-on condition of the PLRC depends on the load condition. Because the energy, which discharges the voltage of inverter switch to satisfy the ZVS condition before the switch turns on, depends on the load condition. In order to enable the high voltage DC/DC converter to operate with high efficiency in wide load range, a gate driver is designed so that it turns on the switch after detecting the switch voltage is completely discharged.

The CWVM is used in many high voltage power supplies because it can obtain high voltage gain[14]-[16]. However, it has problem that the voltage ripple and voltage drop increase in proportion to the number of stages and the load current, and the voltage for each stage is unbalanced. To overcome this, a symmetrical CWVM in the form of arranging two basic CWVM facing each other has been studied[17]-[18]. The proposed converter consists two symmetrical CWVMs and they are connected to the high voltage transformer in parallel. Also, because this structure has bipolar output, the maximum potential voltage is half of the load voltage. Therefore, it is beneficial in terms of insulation design.

Even though the required voltage gain and insulation strength are reduced with the structure described above, it is still required to design a high voltage transformer to handle several kV. In addition, for the compact configuration, the design was accompanied to match the leakage inductance and stray capacitance to the resonance parameters.

The proposed high voltage DC/DC converter was implemented and verified through PSPICE simulation and experiments

II. Design of the High Voltage DC/DC Converter

Fig.1 represents for the entire structure of the proposed high voltage DC/DC converter. In this section, the design of each component is described in more detail.

A. Cockcroft-Walton Voltage Multiplier

The basic CWVM has many advantages such as high voltage gain, low voltage stress on components, and compactness. Especially, since it has high voltage gain, it is possible to lower the difficulty of transformer design by reducing the number of turns of secondary winding. However, basic CWVM also has problems that are proportional to the load current and number of stages such as output voltage ripple, output voltage drop, and voltage unbalance between each stages. These problems occur because a path charging capacitors of an upper stage

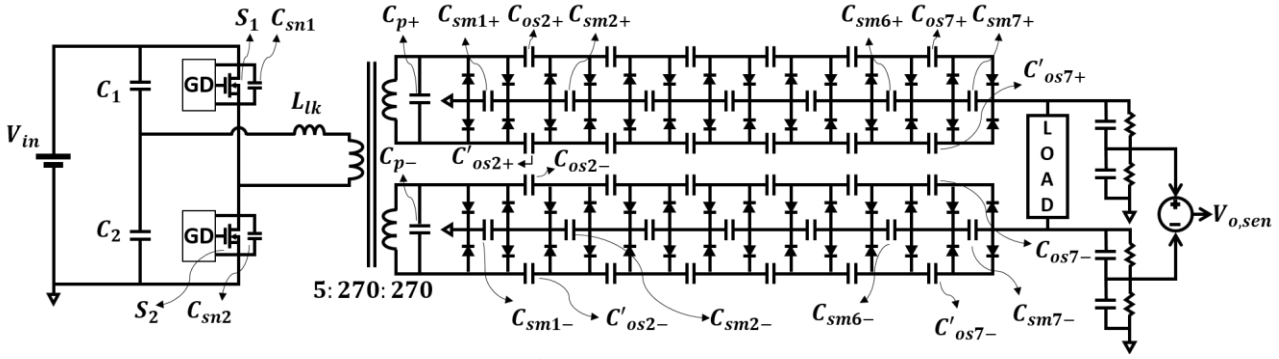


Fig. 1. Entire structure of the proposed high voltage DC/DC converter.

includes capacitors of lower stages. In other words, since charges transmitted to the upper stage pass even in the capacitors of the lower stage, the variation of the lower stage becomes larger than that of the upper stage and the charged voltage becomes relatively larger. The voltage ripple peak to peak value(δV) and voltage drop(ΔV) of the basic CWVM can be expressed in an equation as shown in (1) and (2), respectively.

$$\delta V = \frac{I}{fC}\left(\frac{n(n+1)}{2}\right) \tag{1}$$

$$\Delta V = \frac{I}{fC}\left(\frac{3}{2}n^3 + \frac{1}{2}n^2 - \frac{n}{6}\right) \tag{2}$$

f represents the operating frequency of the driving power, C represents the values of the capacitors of the CWVM, I represents the load current, and n represents the number of stages.

To improve this, symmetrical CWVM circuit is widely used. It consists of two CWVMs arranged symmetrically and has same driving power source. Therefore, the C_{os} facing each other according to the polarity of the driving power source complementarily perform charging and discharging. Accordingly, voltage fluctuations of the C_{os} within one cycle of the driving power source can be reduced, and as a result, voltage ripple and voltage drop can be reduced. The voltage ripple(δV_s) and the voltage drop (ΔV_s) of the symmetrical CWVM are shown in (3),(4).

$$\delta V_s \cong \frac{I}{fC}\left(\frac{n(n+1)}{2}\right)\left(1 - \frac{\pi}{4\sin^{-1}((V_{max} - \delta V)/V_{max}))}\right) \tag{3}$$

$$\Delta V_s = \frac{I}{fC}\left(\frac{3}{2}n^3 + \frac{1}{2}n^2 - \frac{n}{6}\right) \tag{4}$$

In (3), since $\sin^{-1}(V_{max} - \delta V)/V_{max}) > \pi/4$ [19], it can be seen that it always has a smaller value compared to (1).

However, in (3) and (4), even if symmetrical CWVM is used, as the number of connected stages increases, voltage ripple, and voltage drop increase. Therefore, in this paper, two symmetrical CWVMs with opposite diode directions are used to have a bipolar output. The output voltage of each CWVMs is half of the required load voltage. It makes the effective number of stages halved, so that the voltage ripple and voltage drop improved. Moreover, it is advantageous in terms of insulation design because the maximum potential to ground is halved.

In addition, the first stage of each symmetrical CWVM is configured like a general rectifier circuit. Therefore, the voltage is directly charged to C_{sm+} and C_{sm-} without the charging process of C_{os}, and through this, the rising time of the output voltage is improved[18].

B. Parallel Loaded Resonant Converter

As shown in (3), the voltage ripple can be reduced by increasing the operating frequency of the driving power supply. Moreover, increasing the operating frequency can reduce the size of the filter components and magnetic elements. However, soft switching is essential to increase the operating frequency, so that PLRC was adopted in this paper. The main waveform of PLRC is shown in Fig. 2. In the Fig.2, the M1 starts when the complementary switch is turned off, and the voltage of switch(v_{DS}) is discharged by the resonant current(i_{L_k}). When the discharge is completed and becomes 0, the gate driver senses the zero voltage and then applies the gate signal (v_{GS}) to turn on the switch. This results in soft switching in the ZVS condition. After that, when the polarity of the i_{L_k} is changed, M3 starts. And when the switch is turned off, M4 starts. As described above, PLRC enables soft switching during turn-on, but a switching loss occurs during turn-off. To reduce this, snubber capacitors C_{sn1} and C_{sn2} were designed properly.

C. Gate Driver

In the PLRC, the magnitude of the resonant current at turn-off decreases under light load condition. On the other word, the energy that discharges v_{DS} becomes smaller. Therefore, from the light load condition, the v_{DS} may not be discharged before the switch is turned on. In this case, the ZVS turn-on characteristic is lost and hard switching occurs at turn off. To improve this, a gate driver that actively adjusts the dead time before detecting the zero voltage was designed and applied[20].

A brief description of the operating modes is as follows. First, in the section where the positive pulse is applied, the

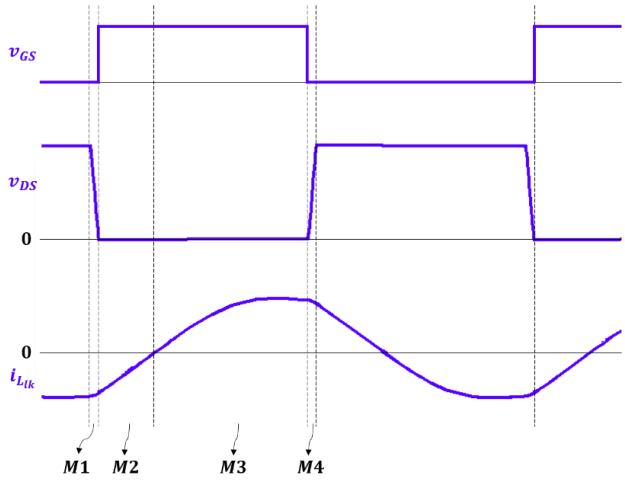


Fig. 2. Waveforms of the PLRC

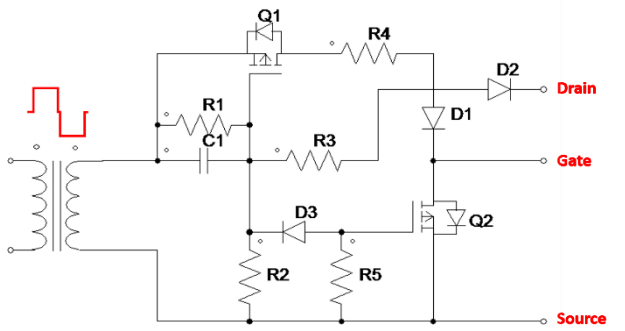


Fig. 3. Circuit diagram of the gate driver.

operation mode is divided into two depending on the drain-source voltage(v_{DS}) of the switch connected to the gate driver. When v_{DS} is not 0, C1 is charged with a voltage through the path formed through R2, and when it becomes higher than the threshold voltage of Q1, Q1 conducts and applies an ON gate signal to the switch. On the other hand, if v_{DS} is 0, D2 is conducted and C1 is charged through the path formed through R3. Since R3 is sufficiently smaller than R2, C1 is quickly charged according to the time constant with R3 instead of R2, and when it exceeds the threshold voltage of Q1, the ON signal is applied to the switch through the same process as described above. When a negative pulse is applied, D3 conducts, the C1 voltage is discharged, Q1 is turned off, and Q2 is turned on, applying an OFF signal to the switch.

Since the switch is turned on after detecting the zero voltage of v_{DS} using such a circuit, ZVS turn-on is possible for a wide load range. The time constants of R2 and C1 are appropriately adjusted so that the switch can be turned on even if v_{DS} does not become zero voltage within the duty. Even in this case, it is not perfect ZVS, but it switches after the voltage is discharged to some extent, so the turn-on loss can be reduced.

D. High Voltage Transformer

A voltage of several tens of kV is applied to the secondary side even though the voltage ratio that needs to be boosted in the transformer is reduced by CWVM, which is described in section *D*. Therefore, high voltage isolation design is essential. In addition, inevitably parasitic components of a high voltage transformer such as leakage inductance(L_{lk}) and stray capacitances(C_{p+}, C_{p-}) were used as resonance parameters to manufacture a compact converter. The high voltage transformer was designed and manufactured with the above two points as the main focus.

E. Sensing and Control

For control to satisfy the output characteristics required by some applications, it is most important to accurately sense the output. Therefore, the resistor and capacitor of the divider circuit for voltage sensing should use high-precision, high-voltage devices with high reliability.

Meanwhile, for more accurate sensing, it is important to select appropriate resistance and capacitance of distribution circuit elements. If too little current flows into the divider circuit, it becomes vulnerable to various leakage currents, making precise sensing difficult. However, if the size of the current flowing through the divider circuit is increased, the sensing circuit may act as a load in applications where load currents of hundreds of μA to several mA flow, causing changes in overall dynamic characteristics. Therefore, an appropriate design considering this trade-off relationship is required.

III. Simulation and Experimental Results

TABLE I
Design Parameter of the High Voltage DC/DC Converter

Input Voltage	380Vdc
Rated Output Voltage	160kV
Rated Output Current	6mA
Switching Frequency	150kHz~310kHz
Resonant Inductance	30μH
Resonant Capacitance	60nF
Transformer Turns Ratio	5:270:270
CWVM Capacitance	220pF

Table 1 summarizes the main parameters of the designed high voltage dc/dc converter. The designed high voltage DC/DC converter was implemented through PSPICE simulation as shown in Fig.4 for verification. The simulation model consists of the designed PLRC, gate driver, CWVM circuit and the controller to which the voltage closed loop control circuit is applied.

Fig.5 is a simulation waveform performed under the condition of a resistive load of 27MΩ. Through this, it was verified that the designed high voltage DC/DC converter was able to target output of 160kV 6mA. The 160kV rising time is about 3ms.

Fig.6 shows the main waveforms during one switching cycle of the inverter switch. Switching loss due to hard switching occurs whenever switch M1 is turned off, and switching loss occurs even when turned on because sufficient time is not secured to discharge the Drain-Source voltage of M1 after M2 is turned off. Fig.6(b) is the waveform when snubber capacitor 5nF is connected to

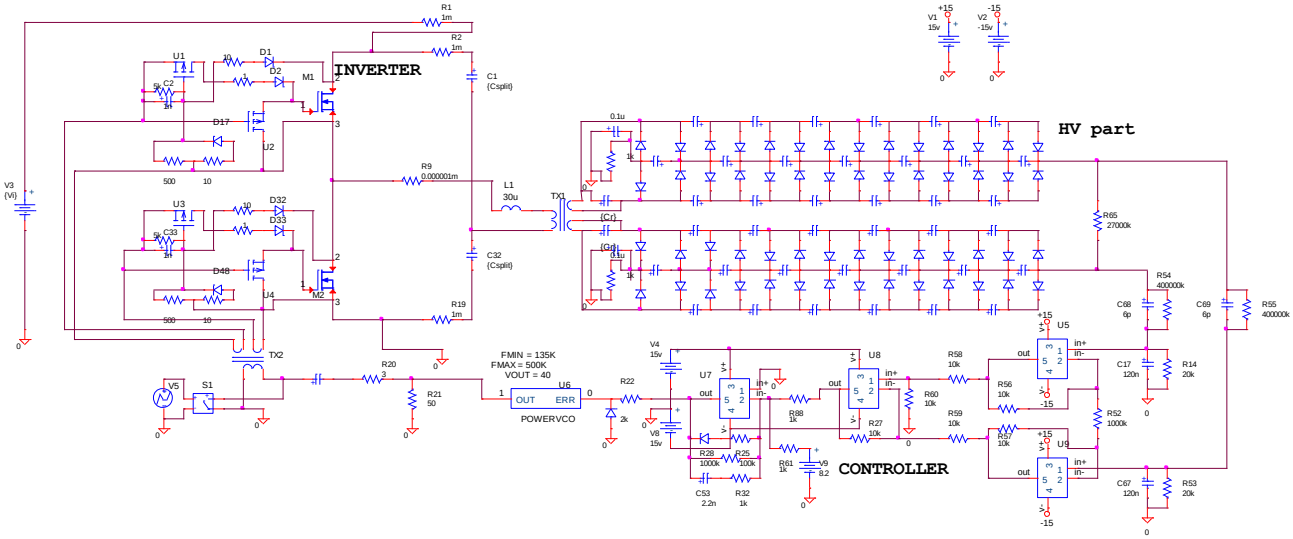


Fig. 4. PSPICE Simulation model of the high voltage DC/DC Converter

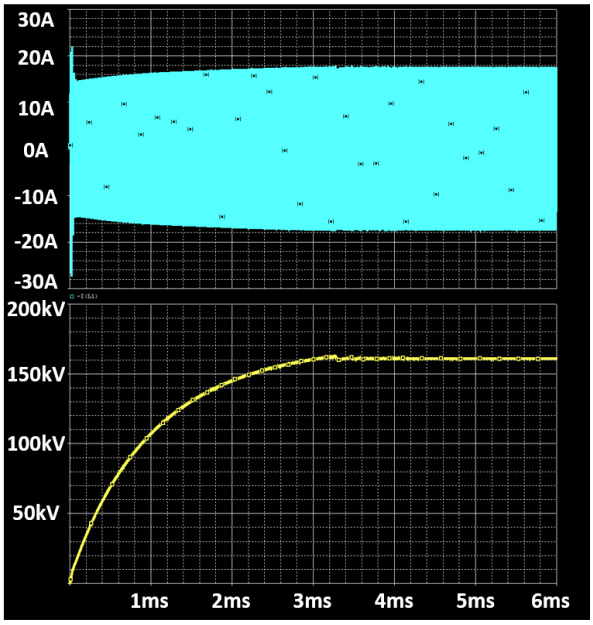


Fig. 5. Waveform of the PSPICE Simulation: 160kV 6mA operation

reduce turn-off loss. Although the switching loss during turn-off has been significantly improved, since the voltage of the snubber capacitor as well as the switch must be discharged before turn-on, the voltage remaining at turn-on is larger, and the turn-on loss is more severe. Fig.6(c) is the waveform after applying the gate driver to solve this problem. It can be seen that the gate signal is not applied until the drain-source voltage of M1 becomes 0, so there is no switching loss because it is turned on under ZVS condition. In addition, when there is no gate driver, the voltage rise rate increases and the turn-off loss increases when M1 is turned off because the switch that operates complementarily turns on and discharges the voltage quickly. Conversely, it can be confirmed that the turn-off loss is further reduced due to the slow voltage discharge rate of the switch operating in a complementary manner due to the application of the gate driver and the slow increase rate of the voltage of M1.

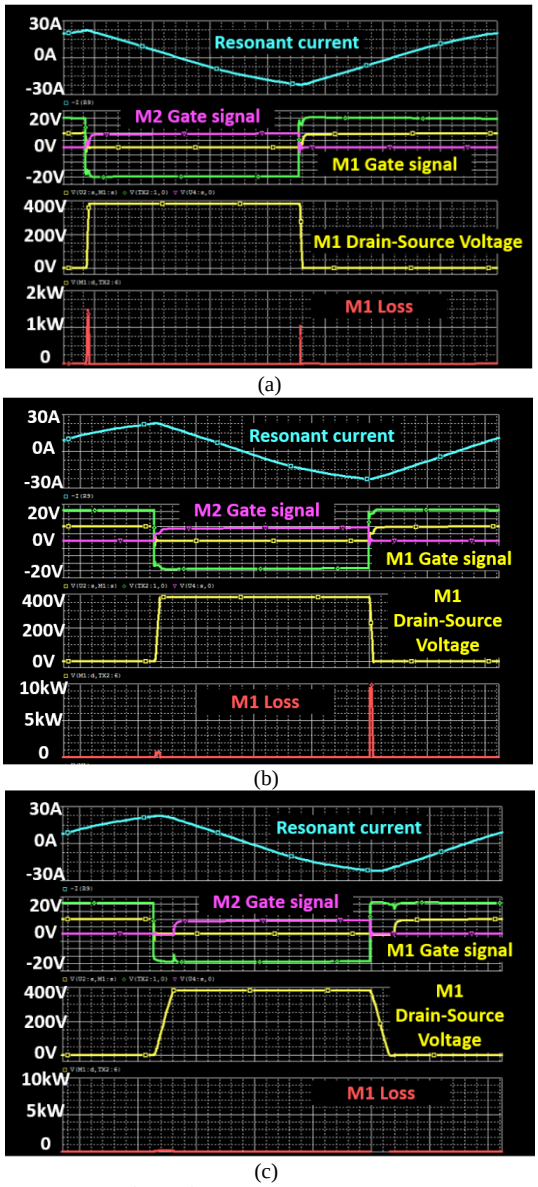


Fig.6. Waveform of the PSPICE Simulation: Switch loss analysis (a) Without snubber capacitor and gate driver (b) With snubber capacitor and without gate driver (c) With snubber capacitor and gate driver

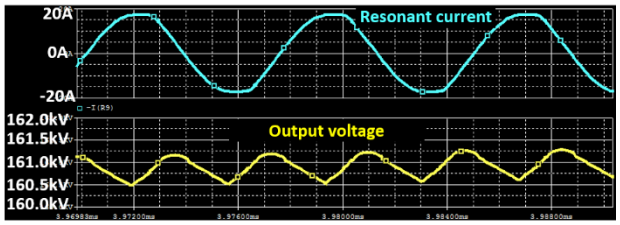


Fig. 7. Waveform of the PSPICE Simulation: Output voltage ripple

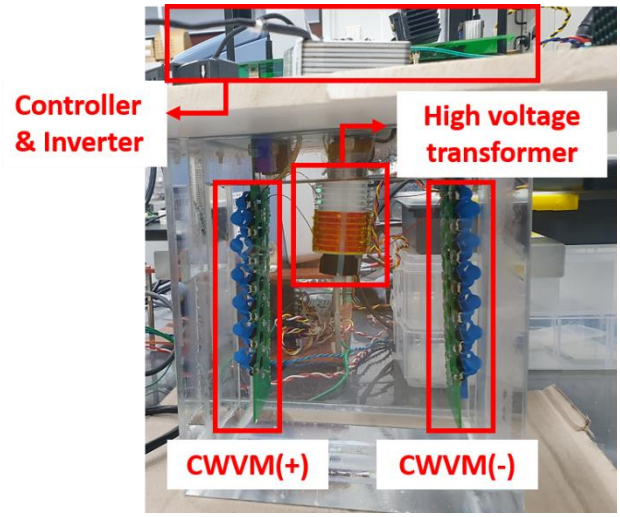
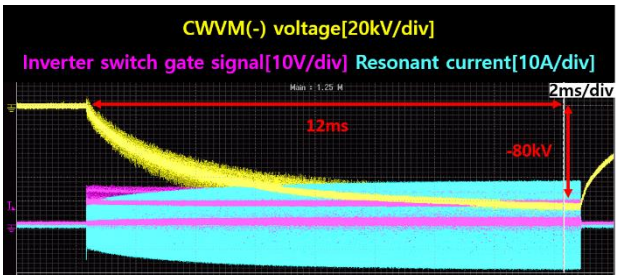
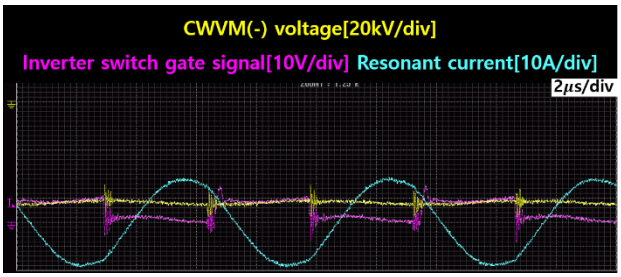


Fig. 8. Prototype of the 160kV high voltage DC/DC converter.



(a)



(b)

Fig. 9. Experimental results of the 160kV DC/DC converter. (a) Transient (b) Steady-state

Fig.7 confirms the ripple of the output voltage under the condition of 160kV 6mA. The magnitude of the ripple is 0.75 kV, which is 0.5% of 160 kV. Due to the effect of the applied Symmetrical CWVM, it has been verified that precise output with a fairly small ripple is possible.

The designed converter was actually implemented as shown in Fig. 8. The low voltage part, the controller and inverter, is located on the top, and the high voltage part, the high voltage transformer and CWVM, is placed on the bottom and impregnated with insulating oil.

The experimental results are shown in Fig 9. Only CWVM(-) voltage was measured, because the voltages of CWVM(+) and CWVM(-) have the same magnitude, only the polarity of the voltage is opposite. Fig. 9(a) is the experimental waveform of the transient section immediately after start-up. It can be seen that the target voltage is reached within 12ms after starting. Fig. 9(b) is the waveform of the steady-state operation, and it has been verified that the implemented high voltage DC/DC converter can output 160kV stably.

IV. Conclusions

This paper describes the implementation of a high voltage DC/DC converter that outputs 160kV based on 380V. For high-efficiency operation and compact configuration, the PLRC capable of ZVS turn-on and reduced turn-off loss by using a snubber capacitor was applied. In addition, a compact configuration was possible using parasitic parameters of a high voltage transformer as resonant parameters without attaching external resonance components. The high voltage transformer was designed to satisfy the resonance parameter with parasitic parameters and to insulate the voltage from tens of kV. The CWVM circuit was applied to the secondary side of the transformer to lower the boosting ratio and design difficulty required for the transformer. Specially, it was designed based on two symmetric CWVM circuits with opposite directions of diodes to compensate for the shortcomings of traditional CWVMs such as voltage ripple, voltage drop, and voltage unbalance between stages, and significantly reduce the difficulty of high voltage insulation design. Finally, the designed high voltage DC/DC converter was actually implemented, and through simulation and experiment, it was verified that it can stably generate 160kV.

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References

[1] M. Ilic, L. Laskai, J. L. Reynolds and R. Encallaz, "An isolated high-voltage DC-to-DC converter with fast turn-off capability for X-ray tube gridding," in IEEE Transactions on Industry Applications, vol. 38, no. 4, pp. 1139-1146, July-Aug. 2002.

[2] J. A. Martin-Ramos, A. M. Pernia, J. Diaz, F. Nuno and J. A. Martinez, "Power Supply for a High-Voltage Application," in IEEE Transactions on Power Electronics, vol. 23, no. 4, pp. 1608-1619, July 2008.

[3] N. Grass, W. Hartmann and M. Klockner, "Application of different types of high-voltage supplies on industrial electrostatic precipitators," in IEEE Transactions on Industry Applications, vol. 40, no. 6, pp. 1513-1520, Nov.-Dec. 2004, doi: 10.1109/TIA.2004.836298.

[4] J. Sun, H. Konishi, Y.Ogino, E. Chu, and M. Nakaoka, "Series resonant high-voltage PFM DC-DC converter with voltage multiplier based a two-step frequency switching control for medical-use X ray power generator." in Proceedings IPEMC 2000. Third International Power

Electronics and Motion Control Conference (IEEE Cat. No. 00EX435). vol. 2, p. 596-601.
[5] J. W. Gong, S. H. Ahn, H. J. Ryoo, and S. R. Jang, “Comparison of DCM and CCM operated resonant converters for high-voltage capacitor charger,” IECON 2013-39th Annual Conference of the IEEE Industrial Electronics Society, pp. 532-537, 2013.
[6] S. R. Jang, H. J. Ryoo, J. S. Kim, and Y. B. Kim, “Design and testing of the high voltage capacitor charger for 150kJ pulsed power application,” 2009 IEEE Pulsed Power Conference, pp. 1376-1379, 2009.
[7] S. R. Jang, S. H. Ahn, H. J. Ryoo, and G. H. Rim, “Novel high voltage capacitor charger for pulsed power modulator,” 2010 IEEE International Power Modulator and High Voltage Conference, pp. 317-321, 2010.
[8] S. H. Ahn, H. J. Ryoo, J. W. Gong, and S. R. Jang, “Design and test of a 35-kJ/s high-voltage capacitor charger based on a delta-connected three-phase resonant converter,” IEEE transactions on power electronics, vol. 29, no. 8, pp. 4039-4048, 2013.
[9] H. J. Ryoo, S. R. Jang, Y. S. Jin, J. S. Kim, Y. B. Kim, S. H. Ahn, and D. H. Kim, “Design of high voltage capacitor charger with improved efficiency, power density and reliability”. IEEE Transactions on Dielectrics and Electrical Insulation, vol. 20, no. 4, pp. 1076-1084, 2013.
[10] S. R. Jang, C. H. Yu, and H. J. Ryoo, “Trapezoidal approximation of LCC resonant converter and design of a multistage capacitor charger for a solid-state Marx modulator,” IEEE Transactions on Power Electronics, vol. 33, no. 5, pp. 3816-3825, 2017.
[11] S. H. Ahn, J. W. Gong, S. R. Jang, H. J. Ryoo, and D. H. Kim, “Design and implementation of enhanced resonant converter for EV fast charger,” Journal of Electrical Engineering and Technology, vol. 9, no. 1, pp. 143-153, 2014.
[12] S. H. Song, C. G. Cho, S. M. Park, H.I. Park, W. C. Jeong, and H. J. Ryoo, “Design and analysis of an LCC resonant converter for xenon flash lamp simmer circuit,” IEEE Transactions on Dielectrics and Electrical Insulation, vol. 26, no. 2, pp. 484-491, 2019.
[13] R. L. Steigerwald, "A comparison of half-bridge resonant converter topologies," in IEEE Transactions on Power Electronics, vol. 3, no. 2, pp. 174-182, April 1988, doi: 10.1109/63.4347.
[14] Weiner, Melvin M. "Analysis of Cockcroft-Walton Voltage Multipliers with an Arbitrary Number of Stages." Review of Scientific Instruments, vol.40, no. 2, pp. 330-333, 1968.
[15] J. S. Brugler, "Theoretical performance of voltage multiplier circuits," in IEEE Journal of Solid-State Circuits, vol. 6, no. 3, pp. 132-135, June 1971, doi: 10.1109/JSSC.1971.1049670.
[16] P. Lin and L. Chua, "Topological generation and analysis of voltage multiplier circuits," in IEEE Transactions on Circuits and Systems, vol. 24, no. 10, pp. 517-530, October 1977, doi: 10.1109/TCS.1977.1084273.
[17] Ruzbehani, Mohsen. "A comparative study of symmetrical Cockcroft-walton voltage multipliers." *Journal of Electrical and Computer Engineering* 2017 (2017).
[18] S. Iqbal, "A Hybrid Symmetrical Voltage Multiplier," in IEEE Transactions on Power Electronics, vol. 29, no. 1, pp. 6-12, Jan. 2014, doi: 10.1109/TPEL.2013.2251474.
[19] F. Hwang, Y. Shen and S. H. Jayaram, "Low-Ripple Compact High-Voltage DC Power Supply," in IEEE Transactions on Industry Applications, vol. 42, no. 5, pp. 1139-1145, Sept.-Oct. 2006, doi: 10.1109/TIA.2006.880845.
[20] S. H. Ahn, H. J. Ryoo, J. W. Gong and S. R. Jang, "Robust Design of a Solid-State Pulsed Power Modulator Based on Modular Stacking Structure," in IEEE Transactions on Power Electronics, vol. 30, no. 5, pp. 2570-2577, May 2015, doi: 10.1109/TPEL.2014.2352651.