Experimental study of interleaved Y-Inverter performance

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Keywords

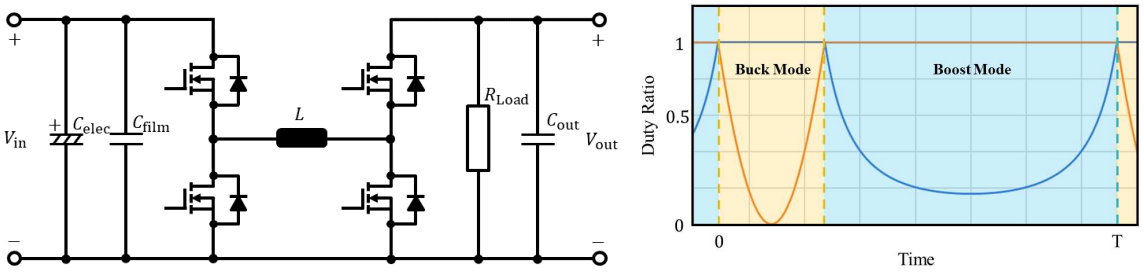
«DC-AC converter», «Inverter design», «Interleaved inverters», «Wide Bandgap devices», « High frequency power converter», « High power density systems».

Abstract

The Y-Inverter is rapidly gaining popularity as an alternative to the “dc-boost plus inverter” configuration in motor drive applications. Recently, advantages of designing with multiple interleaved cells per phase, as opposed to simply paralleling devices, have been pointed out and solutions using both coupled and non-coupled inductors have been proposed. This paper presents a detailed experimental benchmark study of the inverter performance when using non-interleaved and interleaved cells; for the interleaved case, both non-coupled and coupled inductors are considered. The results clearly show that interleaving enables an important reduction of the current stress on the output and input filter capacitors, as well as the possibility to design the magnetic components with higher energy density and higher efficiency. Interleaving clearly appears as a superior alternative to the straightforward paralleling of semiconductor devices, when the current ratings are such as to require multiple transistors anyway. Specific differences in the circuit performance optimization potential exist between the case of coupled and non-coupled inductors. Only the interleaved non-coupled case is presented here in detail, with some comparison results. All cases will be dealt with in detail in the final paper.

Introduction

The Y-Inverter is a sinusoidally modulated inverter topology introduced fairly recently and which has been shown to feature a number of superior properties over conventional Voltage Source Inverters (VSI), particularly to the aim of fully exploiting the characteristics of modern wide-band-gap (WBG) semiconductor devices [1-3]. Fig. 1 illustrates the single-phase circuit schematic (a) and the modulation signals for the buck and boost cells (b). With this modulation, the single cell produces an output voltage which is an offset sinusoidal waveform,



(a) (b)

Fig. 1: Circuit schematic of a single cell of buck-boost Y-Inverter power cell (a); duty and inverse-duty cycles (i.e., high side transistor) for the buck and boost semi-cells, respectively (b).

$$V_{out} = \frac{V_{peak}}{2} \cdot [1 + \sin(\omega t)] \quad (1)$$

Fig.2 which shows the 3-phase system, where all cells share the common ground terminal connection (Y-configuration). In this configuration, the dc-offset gets cancelled and the phase-to-neutral voltage has amplitude equal to Vpeak/2. Fig.3 shows the phase-to neutral voltages and one phase inductor current for the 3-phase load powered by the Y-Inverter operated with continuous sinusoidal S-PWM [1]. Here, the circuit parameters and test conditions are: *Vin*=60 V; *Vpeak*=90 V; f_{LOAD}=50 Hz; *fs*=200 kHz.

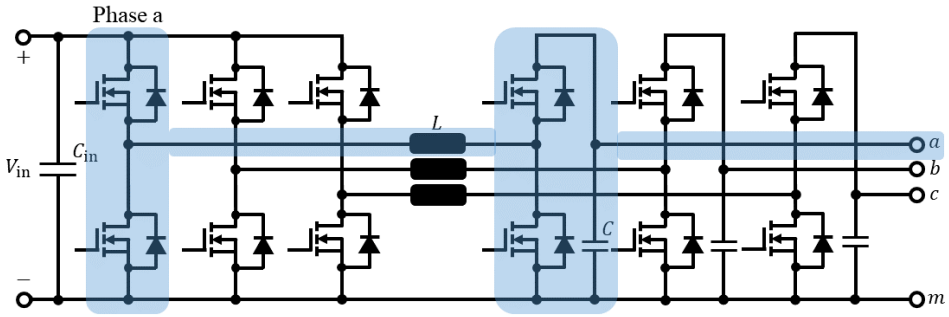
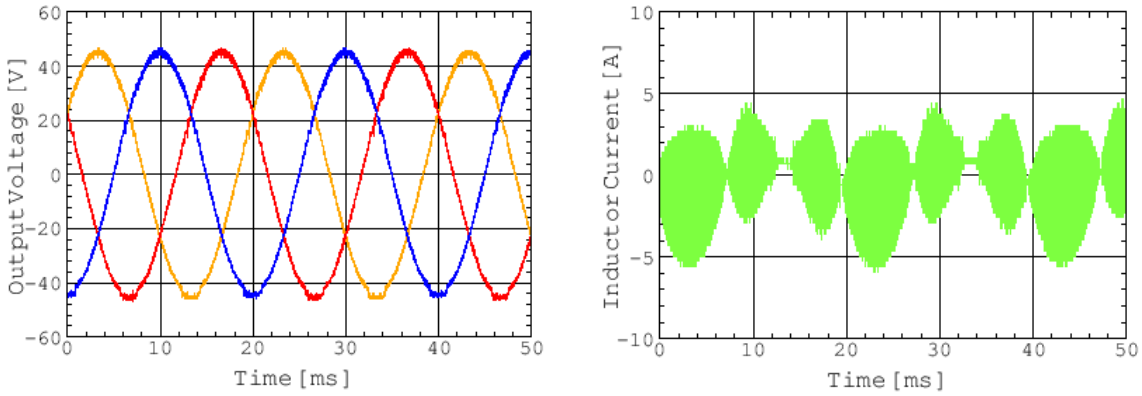


Fig. 2: Three-phase non-inverting buck-boost Y-Inverter.



(a) (b)

Fig. 3: Experimental results for 3-phase Y-Inverter with S-PWM: phase-to-neutral voltages 3(a); one phase inductor current 3(b). The low-level distortion (flat portion) in the voltage waveforms and corresponding zero current are due to an imperfection in the modulation signals during test.

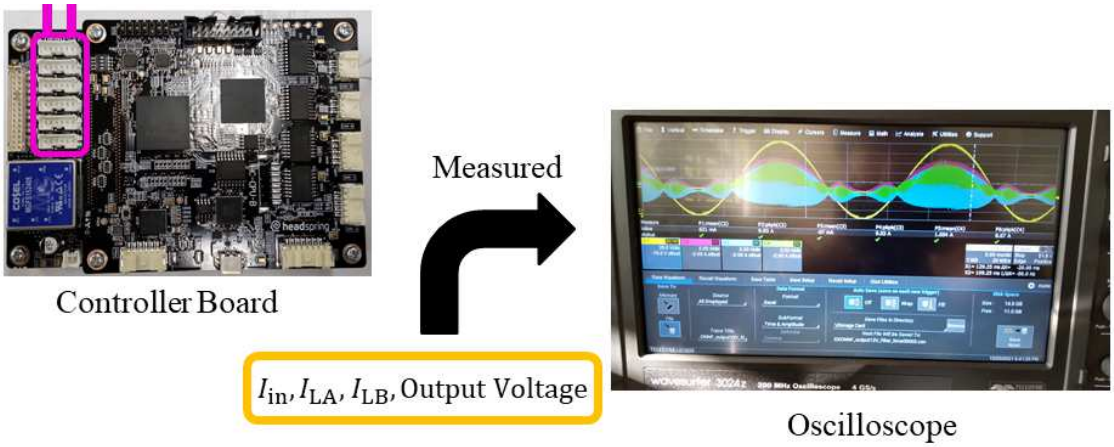
Important innovative aspects of this topology over standard VSI solutions include:

- sinusoidal output voltage synthesis (as opposed to square wave modulated), which: a) eliminates dV/dt related noise and stress, allowing to fully exploit the switching speed of WBG transistors; b) reduces harmonics to essentially the load fundamental and the switching frequency components; c) reduces, on average, the device output-side switching losses, since transitions take place at sinusoidally decreasing drain-source voltage, enabling higher switching frequencies;
- no high-voltage DC-link capacitor: this is oftentimes one of the bulkiest and reliability critical components in the system and, in applications where electrolytic capacitor technology is not admitted (e.g., avionics), a rather costly one, too; indeed, the Y-Inverter requires good film technology capacitors on the output, due to relatively high current levels, but their value can be typically contained within few µF`s; removal of the large DC-link capacitor is an important asset towards higher integration levels.
- integrated voltage boost capability, allowing for the use of devices with different technology and different voltage ratings on the input (i.e., buck cell) and output side cells (i.e., boost cell). Also, the switching frequencies for the two cells can be chosen to be different, so as to optimize the converter design and performance [4].

On the other hand, one inherent challenge of the Y-Inverter is that the inductor current scales in some proportion to the output voltage boost ratio. This has motivated designs using interleaved cells with or without inductor coupling [4, 5], to reduce the magnetic flux density in the inductor and contain its losses and volume, for the same number of semiconductor switches, which is simply dictated by considerations about the current rating: that is, the interleaved configuration is proposed as an alternative to the straightforward paralleling of multiple semiconductor dies.

Experimental prototype test results

Specifically, here two cases are considered: 1) interleaving with 180 degrees phase-shift of the PWM carrier and no inductor coupling; 2) interleaving with 180 degrees phase-shift of the PWM carrier and cross-coupled inductors. The corresponding circuit schematic is detailed ahead for each case. The transistors are all normally-off GaN HEMTs with 650V rating. The value of the electrolytic capacitor on the input side does not correspond to any specific performance target, but rather to the capability of testing in the presence of relatively long cables to the power supply. For all test conditions and results, the following data apply: Vin=60 V; $Vpeak$=140V; f_{Load}=50 Hz and fs=200 kHz; R_{Load}=50 Ω. The test setup includes a Kikusui PWR400L DC power supply, Headspring HECS-B/A Controller, Fig. 4 (a), a Teledyne LeCroy WaveSurfer3024z 200 MHz 4 GS/s oscilloscope, Fig, 4 (b), and PP011 differential voltage probe, CP30 50 MHz and CP150 10 MHz current probes.



(a) (b)

Fig. 4: (a) headspring controller; (b) oscilloscope with capture of experimental current and voltage waveforms.

Single-phase interleaved cells with non-coupled inductors

Fig. 5 shows the circuit schematic for the implemented prototype. With this configuration, interleaving yields a reduction of the current ripple at the output capacitor, with some benefit for the capacitor current stress and voltage ripple. Fig. 6 (a) shows the resulting output capacitor voltage, while Fig. 6 (b) a detail of the inductor currents and their ripple. The overall inductor current waveforms are shown in Fig. 7. Each inductor has a value of 120 µH (more details are included in the next Section). In this configuration, the measured cell efficiency was 97.3%.

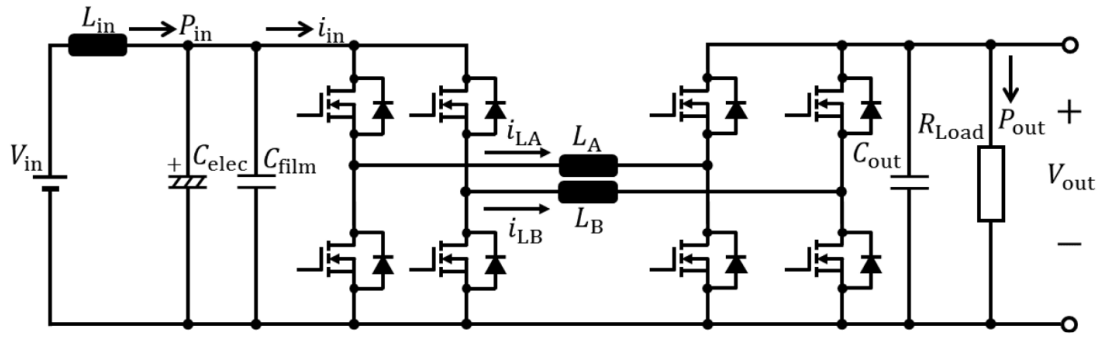
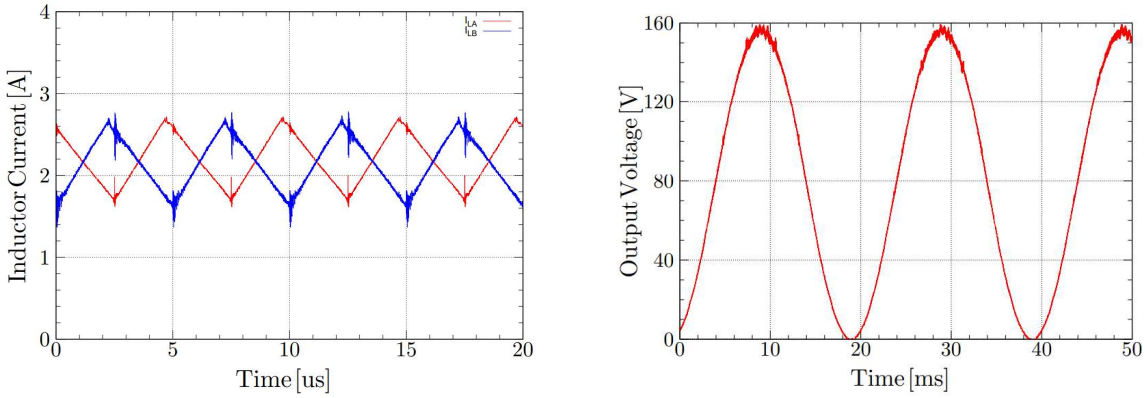
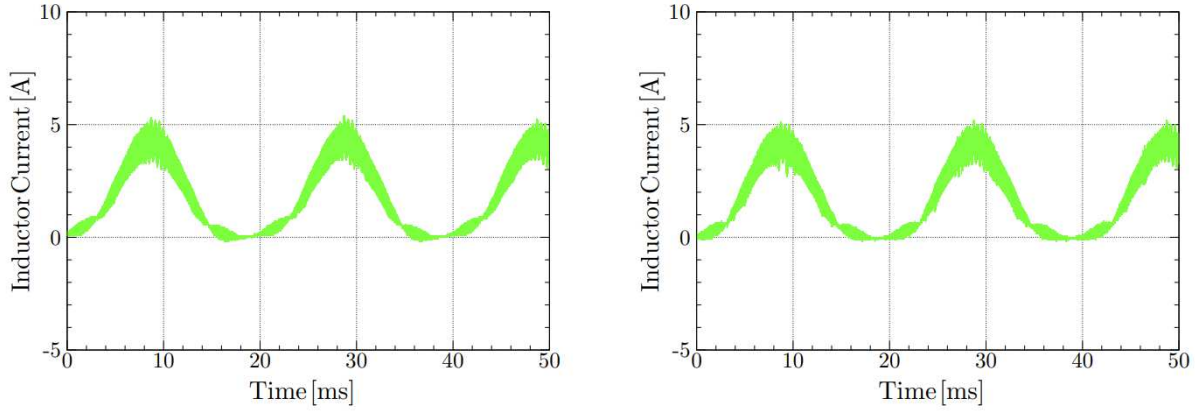


Fig. 5: Single cell of interleaved non-inverting buck-boost Y-Inverter with non-coupled inductors.



(a) (b)

Fig. 6: (a) output voltage; (b) detail of inductor current ripple.



(a) (b)

Fig. 7: (a) current in inductor L_A; (b) current in inductor L_B.

Single-phase interleaved cells with cross-coupled inductors

For this case, the corresponding topology is illustrated in Fig. 8. With this configuration, on top of the reduction of the current ripple at the output capacitor, an effective reduction of the magnetizing inductor current can be achieved, which allows a more compact inductor design.

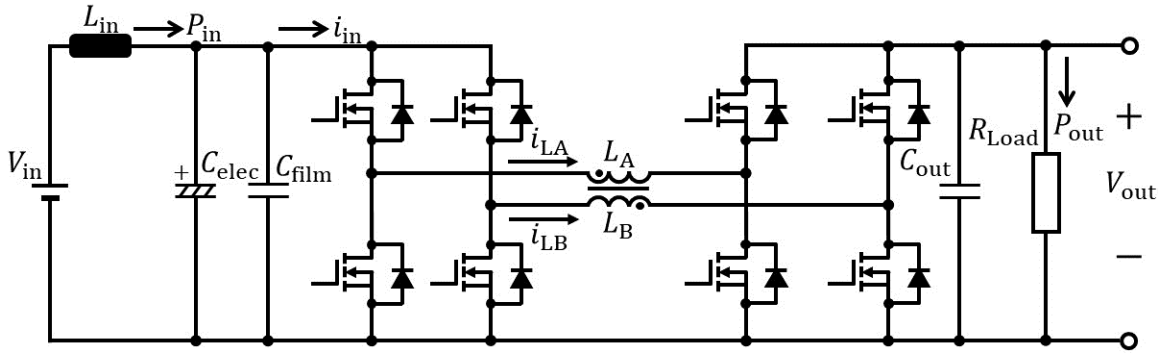


Fig. 8: Single cell of interleaved non-inverting buck-boost Y-Inverter with cross-coupled inductors.

The equivalent inductor model is shown in Fig. 9 and assumes identical values for L_1 and L_2; $M=kL$ is the mutual inductance and $L+M=(1+k)L$ the parasitic inductance of each strand. In our case, the actual inductor was fabricated on a E-shaped core using core material PC40EC70X69X16 manufactured by TDK-Lambda Corporation (Mn-Zn, $A_L = 4845 \pm 25\%$ nH/turns^2), with a nominal gap of 0.2 mm (varied to trim k) and using high frequency Litz wire. For a target self inductance value of 120 µH, 12 turns were wound. It should be noted that this is also the inductor which was used for the tests with separate inductors, in which two separate cores were used, each with a single winding.

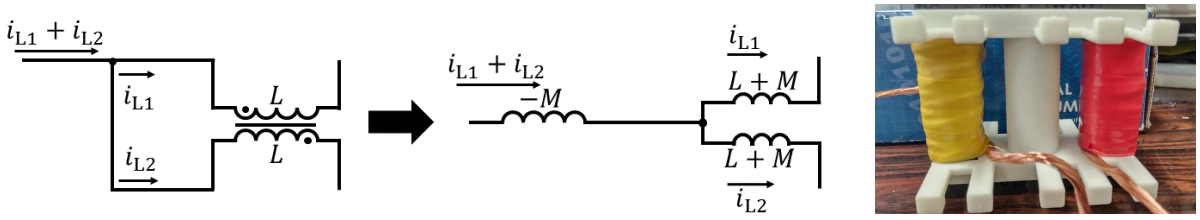


Fig. 9: (a) Cross-coupled inductor equivalent model and (b) inductor prototype.

However, here, it becomes very important to trim the value of the coupling coefficient k to achieve high efficiency. The inductor prototype is shown in Fig. 9 (b), while Fig. 10 shows extensive characterisation results. Specifically: Fig.10 (a) and (b) show the frequency characteristics of inductance and resistance on the secondary side, respectively, when the primary side is open; Fig. 10 (c) and (d) show the frequency characteristics of inductance and resistance on the primary side, respectively, when the secondary side is open. Fig. 10 (e) and (f) show the frequency characteristics of inductance and resistance on the secondary side, respectively, when the primary side is shorted; finally, Fig. 10 (g) and (h) show the frequency characteristics of inductance and resistance on the primary side, respectively, when the secondary side is shorted. At th switching frequency value, 200 kHz, the corresponding values can be summarized as in Table I. From these results, the value of k can be estimated at about 0.58, which yielded best results, with an efficiency of 97%.

Table II: Measured inductor parameters at 200 kHz.

Parameter	Inductance	Resistance
L_{1open}	120.2588 μH	494.048 mΩ
L_{2open}	120.6908 μH	491.577 mΩ
L_{1short}	99.67244 μH	353.06 mΩ
L_{2short}	100.3371 μH	359.287 mΩ

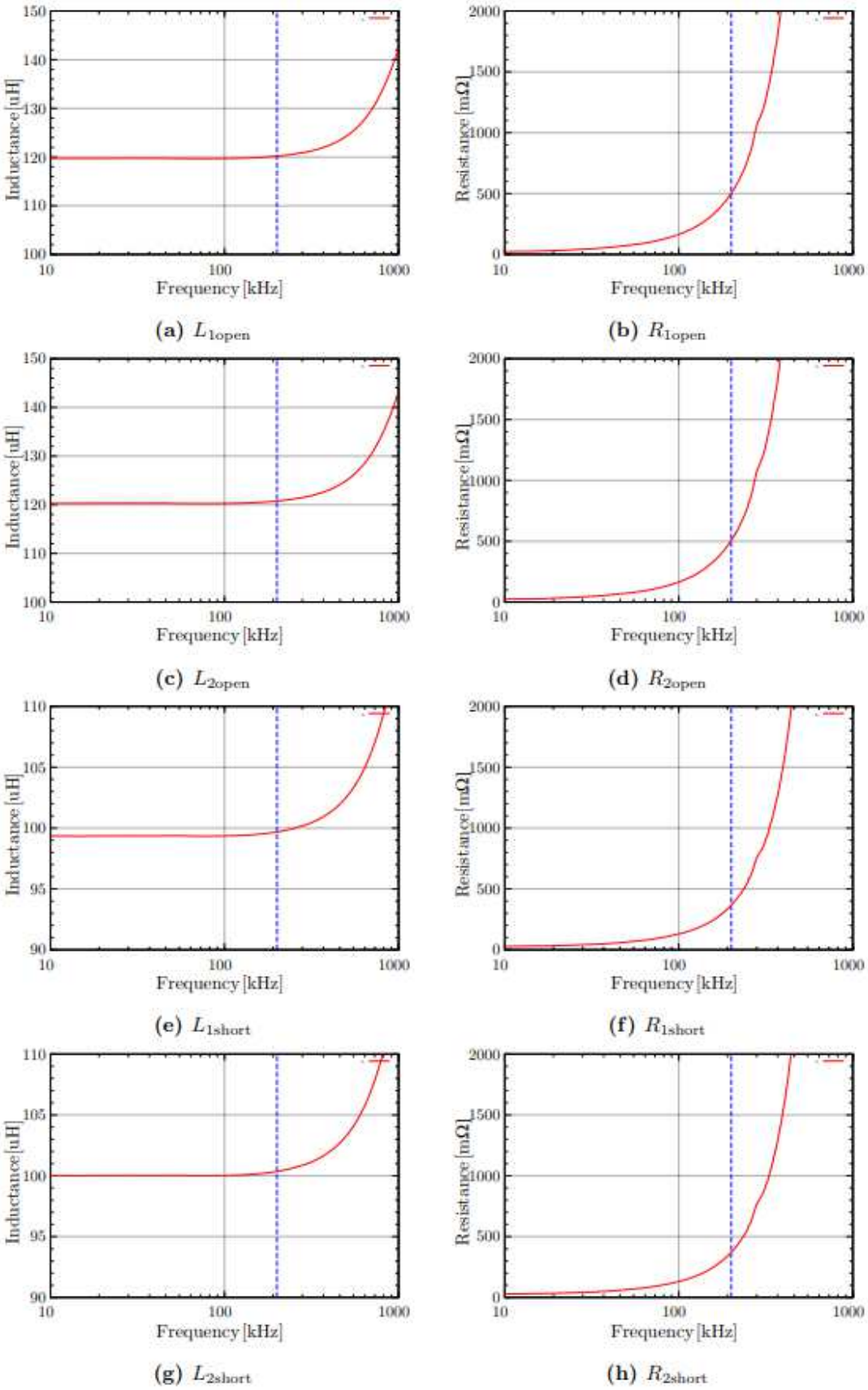
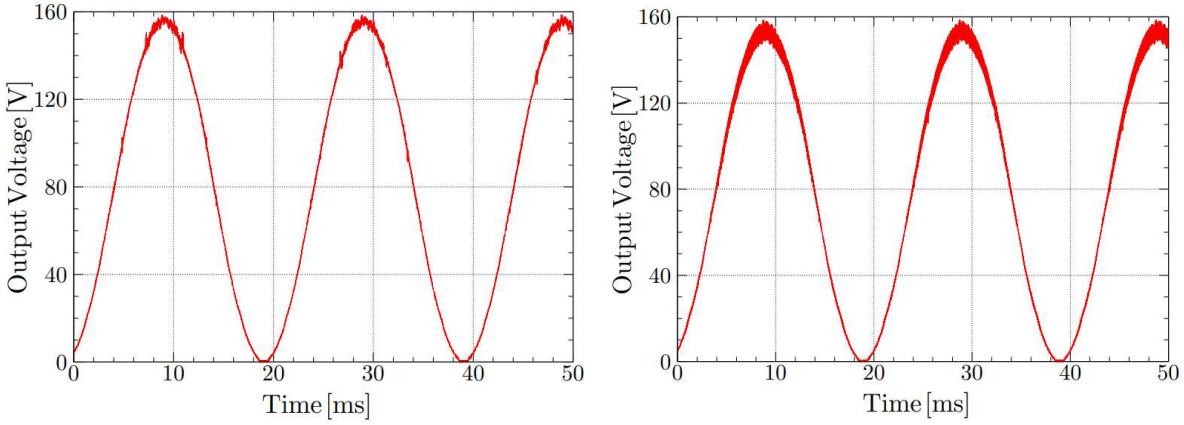


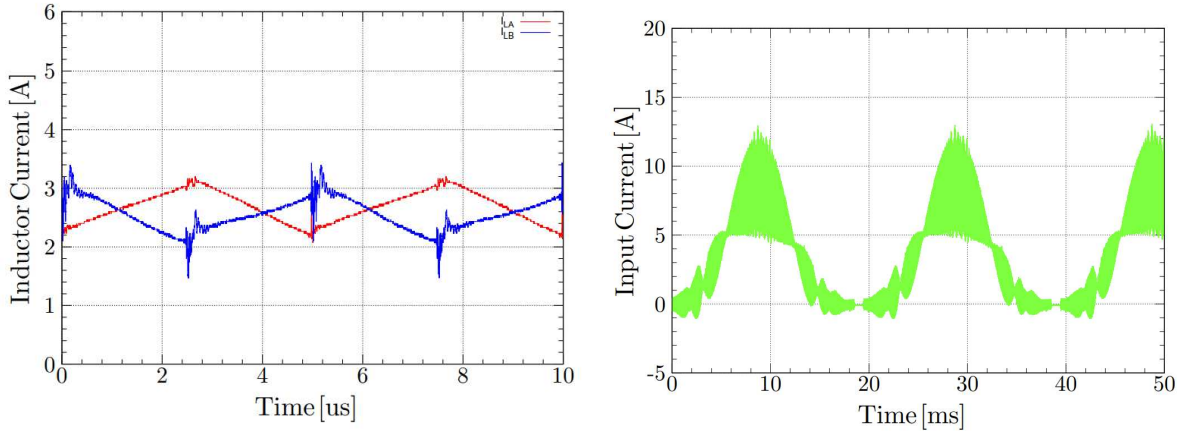
Fig. 10: Frequency characteristics of the coupled inductor; (a),(b): the primary side is open, (c),(d): the secondary side is open, (e),(f): the primary side is short, (g),(h): the secondary side is shorted.

Representative voltage and current waveforms for his case are shown in Figs. 11 and 12. Fig. 11 (a) shows the output capacitor voltage: as can be seen, the ripple is identical to the case of Fig. 6. For direct comparison, Fig. 11 (b) shows the same waveform when the phase-shift in the PWM carrier signals of the two interleaved cells is zeroed.



(a) (b)

Fig. 11: (a) output capacitor voltage with PWM carriers phase-shift of 180 degrees ; (b) output capacitor voltage with PWM carriers phase-shift of 0 degrees.



(a) (b)

Fig. 12: (a) detail of current ripple in the two windings of the inductor; (b) total inductor current.

Fig. 12 shows results for the inductor current: in (a), details of the ripple in each winding of the inductor are given, whereas in (b) the total inductor current is shown.

Conclusion

The Y-Inverter is receiving increasing interest for the development of advanced motor-drives. In particular, its operating characteristics enable the full exploitation of the superior features of wide-band-gap semiconductors to yield disruptive improvements in efficiency and power density. The inverter features not-only benefit the power electronics, but also the machine, which can be designed for much higher efficiency and power density target values. Focusing on the interleaved implementation of the Y-Inverter, this paper showed that such approach can yield important advantages over straightforward device paralleling for meeting current rating requirements. The use of cross-coupled or non-coupled inductors when applying interleaving is left as an option to optimize either the size and efficiency of the

magnetics (e.g., in relatively high current applications) or to reduce the stress in the capacitors (e.g., in the case of relatively high-voltage applications). The achievable reduction of core-size with interleaving using cross-coupled inductors has not been quantified here, but it is deemed considerable for high current applications.

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