Multilevel battery converter with cascaded H-bridges on cell level – battery management system or a renewed attempt for Power Electronic Building Blocks?

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Keywords

«Multi-level converters», «Pulsed current», «Battery», «Battery Management Systems (BMS)», «Cascaded H-Bridge

Abstract

The combination of battery management system and power electronics, using multi-level topologies in general and cascaded H-bridges in particular, offers advantages over the state of the art. Their evaluation must consider possible effects on battery life. Experimental studies of battery cells show that these effects are small compared to typical loads.

Multi-level topologies and the advantage in battery storage applications with Lithium-based battery cells

To achieve the goal of functional and monetary improvements in battery-electric storage systems, the merger of previously separate functions, like battery management and power control, has great potential.

There are a variety of power electronic topologies for converting electrical power – long known solutions, that have so far been used in specialised areas only, are multi-level topologies with more than three levels [1].

Two main motivators drive the use of multi-level topologies, especially cascaded H-bridges. On the one hand, the insufficient dielectric strength of the components, e.g., in HVDC applications. On the other hand, the better efficiency/higher resulting switching frequency with lower blocking voltage of the components with the consequence of lower expenses in the filter technology.

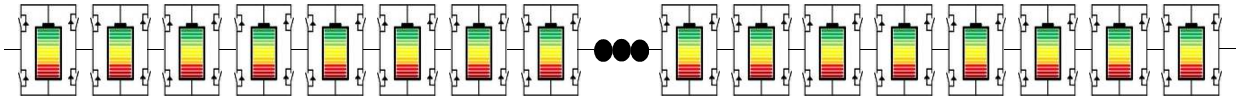

Fig. 1

A disadvantage of most multi-level topologies is the higher complexity of control. Sophisticated control strategies are required especially for voltage balancing of the necessary energy storage devices – in most cases capacitor intermediate circuits.

This is a major advantage of using cascaded H-bridges in battery storage systems. Lithium-based battery cells store more energy per volume compared to capacitors. This allows charge or energy equalization between stages in seconds or minutes rather than milliseconds, several orders of magnitude slower than using a capacitor as a storage device.

The voltage and, if possible, also the temperature have to be monitored for each individual battery cell in the serial connection. Charge equalisation, known as balancing, should be possible between serially connected cells. These functions are usually fulfilled by a Battery Management System (BMS) [2].

This leads to the basic idea – each battery cell gets an H-bridge that brings together the power electronics and the BMS functionality (see Fig. 1) – to borrow Einstein's idea – make things as simple as possible, but not simpler.

There are proposed topologies to include battery cells in a cascaded H-bridge converter, but they are using battery-modules with multiple serial connected cells on each converter-level [3][4]. The use of battery modules with serially connected battery cells requires further cell balancing procedures within the module [3] as well as an additional BMS to monitor the battery cells.

With a battery cell voltage between 2.9 V and 3.6 V (LFP/graphite), at least 120 cascaded stages are required for transformerless grid coupling ($230\ V_{rms}$). Since each battery cell level is equipped with its own H-bridge, the current can be conducted through the cell in positive or negative direction, as well as bypassing the cell. Active cell balancing is possible with operating current up to the nominal current. The small voltage steps between the stages allow operation without high switching-frequency of the H-bridges. Both, DC and AC, voltage can be output.

The proposed topology offers further advantages in terms of safety, availability, repairability and applicability for different applications.

- In the high-impedance state of the bridges, no voltage is present at the output terminals of the battery pack, thus preventing short circuits at the terminals of the battery module during transport and installation without further measures.
- The current can be bypassed at conspicuous, low-power or, in some fault cases, even defective battery cells.
- The failure of one cell does not necessarily lead to the failure of the entire system.
- Due to the active full-power balancing, battery cells with large capacity differences can be used in a system without restrictions. The proposed topology is also suitable for the use of aged, second use cells and grade B cells, as well as for the use of different cell manufacturers or cell types.
- Cascading a simple structure like the H-bridge into a complete system offers a lower market entry barrier for all, who want to do the power electronics integration into their system, e.g. battery cell manufacturers, battery pack manufacturers, battery system suppliers etc.
- Generalised, the presented design offers a competitive solution for battery systems from 12 V to 1500 V output voltage (DC or AC) and for cell capacities from 20 Ah to 500 Ah

With the advantages described, the topology is most suitable for areas of application in which higher battery cell capacities are required, such as electromobility (buses, trains, ships, etc.), stationary energy storage, construction site supply, and so on. This assessment is linked to the attempt to establish a Power Electronic Building Block (PEEB), which has already been carried out several times in power electronics [5–7]. In this case, a PEBB for the power electronics of battery storage systems.

In order to reap the benefits mentioned above, some challenges need to be overcome. Let's name the ones for which there are already promising solutions, but which are still waiting for experimental and economic proof:

- There is a suitable electromechanical connection between the battery cell and PCB-based power electronics that offers low contact resistance and compensation for mechanical tolerances.
- A detachable power connection between battery cell and PCB-based power electronics offers improved repair possibilities.
- The proportional specific costs (€/W) for the proposed power electronics should be lower than those of conventional photovoltaic converters.
- The total costs of the topology are lower compared to a conventional inverter with external BMS due to the integrated BMS functionality and the advantages mentioned (active balancing, availability, etc.) (€/W).
- Despite the higher number of components, there is a lower or equal probability of failure compared to conventional approaches (first considerations below).

The old challenges for new design approaches – temperature and switching overvoltage

For single-phase, transformer less coupling to the 230 V_{rms} AC grid, the sum of the battery cell voltages must exceed the grid peak voltage. Depending on the discharge voltage limit of the battery cells, a series connection of 120 to 140 stages is required. These stages could be combined to cell packs with multiple stages on one PCB (see Fig. 2). Due to the number of stages needed, a large number of MOSFETs is required in the system. Can a low utilization of the components increase their lifetime to such an extent that their number cancels out?

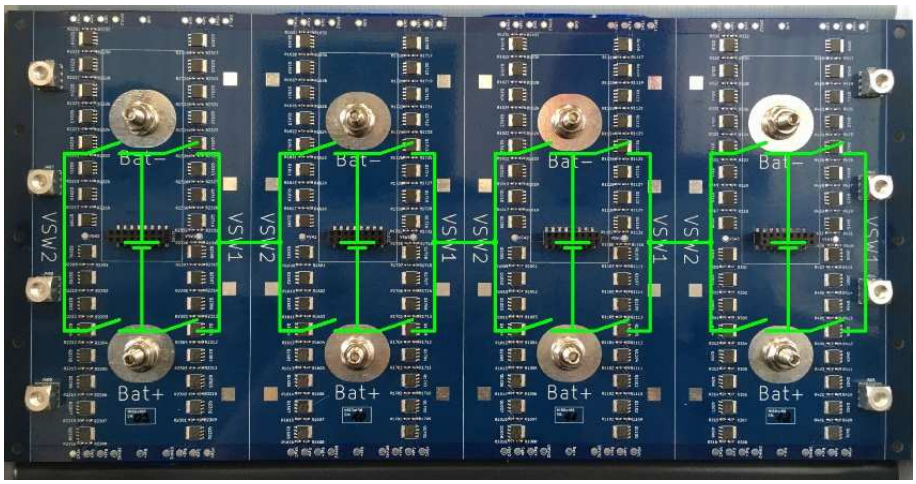

Fig. 2: Top view of a PCB, designed for a nominal current of 150 A, with H-Bridges for a 4s cell pack of 280 Ah cells (72 mm x 173 mm x 208 mm), available from different manufacturers like CATL, EVE, Lishen and others

A simple way to increase the reliability of components is to operate them well below their rated specifications. This method is known as derating. For example, if a component designed to operate reliably at +125°C is only operated at +55°C, lifetime will increase. As a rule of thumb, the life of a component doubles for every 10 K drop in temperature. This relationship between temperature and service life is based on the theoretical framework of the Arrhenius equation, which establishes a relationship between temperature and ageing acceleration. This works for electronic components as well as for the battery cells [1, 8].

Concerning temperature, the limiting part in a battery energy storage system (BESS) is the battery cell itself, which will degrade the least at temperature around 20 to 30°C. With a limited ambient temperature range of 5 to 35°C for the whole system, this leaves enough space for natural cooling of the power semiconductors, which normally work with base temperatures above 80°C.

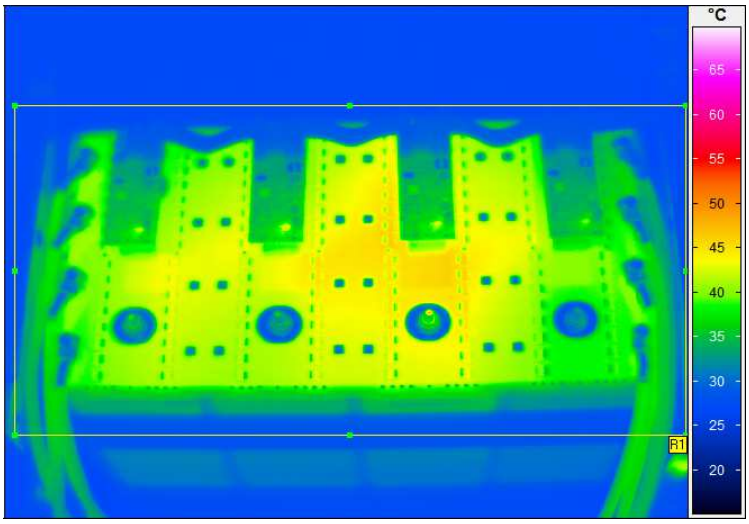

Fig. 3: Infrared image of the PCB shown in Fig. 2 at a current of 150 A, hotspot temperature 50°C

Additionally, investment in silicon MOSFETs also leads to peak efficiencies of over 99 % and thus low additional heat losses. As shown in Fig. 3, at a current of 150 A (around 0.5C) the temperature increases only about 25 K, which leaves the semiconductors at a cosy temperature of 50°C at an ambient temperature of 25°C.

In addition to the low temperature, the low voltage utilization of the MOSFETs also contributes to an increase in lifetime. Stationary the drain-source voltage is the cell voltage and with max. 3.6 V, for LFP cells, is far below the permissible voltage of a 25 to 40 V MOSFET. But what is about switching overvoltage?

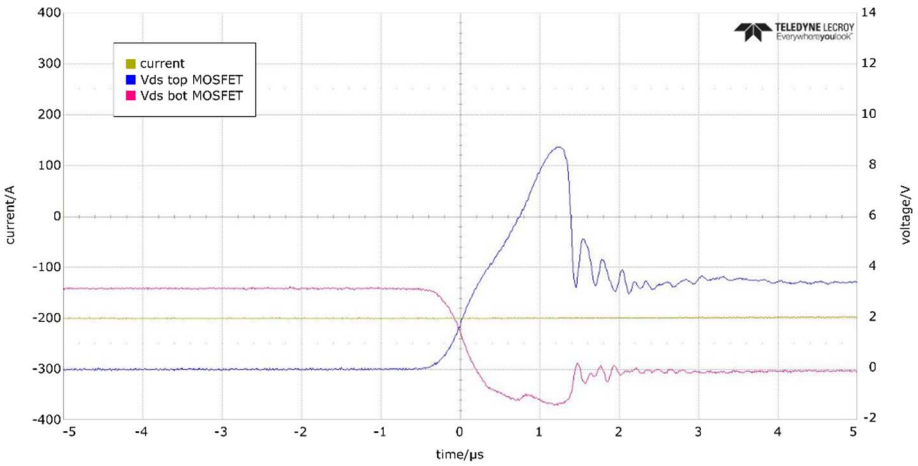

Fig. 4: Switching from positive to bypass state at 200 A discharging current (yellow), drain-source-voltage at bottom MOSFET (red), drain-source-voltage at top MOSFET (blue)

The voltage curve of a commutation event at 200 A discharge current shown in Fig. 4 with 8.8 V_{peak} is safely within the permissible voltage range of the MOSFET. In the proposed topology the battery cell is located in the commutation circuit (see Fig. 7). To avoid an additional DC link capacitor, the cell inductance plays an important role for the design of the commutation circuit.

Determination of the battery inductance

Overvoltage across transistors can be caused by the commutation inductance L_c, due to the rapid current reduction during commutation transient. Together with the battery cell voltage, this overvoltage can endanger the MOSFETs used in the battery converter (see Fig. 7). The absolute maximal drain-source voltage limitation alone is not enough to guarantee a safe operation of the transistor. Fig. 5 specifies the maximum allowable pulse currents that a transistor can withstand when it is in on-state without exceeding the voltage limitation of 25V.
Another approach is to use the transient thermal resistance of the transistor to estimate the maximal allowable power P_{max} generated during the switching transient:

$$P_{max}(t_p) = \frac{T_{jmax} - T_{amb}}{Z_{th}(t_p)} \tag{1}$$

The switching power P_{sw} can be approximated as the power averaged over the period t_p:

$$P_{sw} \approx \frac{1}{t_p} \int_0^{t_p} \left(-\frac{U_d}{t_p} \cdot t + U_d \right) \cdot \left(\frac{I_d}{t_p} \cdot t \right) \cdot dt = \frac{U_d I_d}{6} \tag{2}$$

For those one-time events, such as overcurrent, which lead to the shutdown of the transistors, the maximal permissible current can be estimated for a given pulse duration t_p.

$$\frac{U_d I_d}{6} = P_{sw} < P_{max}(t_p), \; I_{d,max} \approx \frac{6 \cdot P_{max}(t_p)}{U_d} \tag{3}$$

Therefore, a modeling of the commutation inductance is reasonable for the overvoltage and the maximal switchable current investigations during the switching transients. To figure out the inductance introduced by the battery cell, single pulse tests on a battery cell have been implemented, whereby the behavior of the battery cell under different test conditions, such as different states of charge (SoC), temperatures, current directions, and current intensities, has been considered. It is assumed that the pulse length is short and has no influence on the SoC during the test.

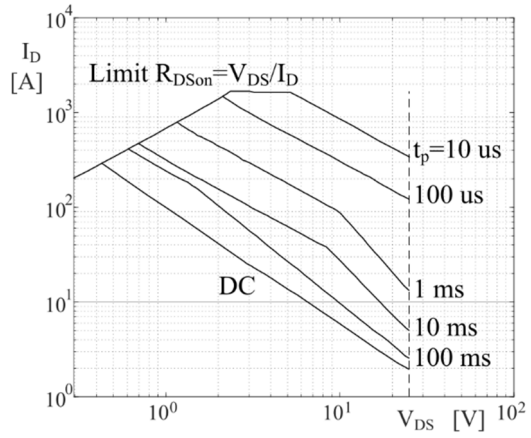

Fig. 5: Safe operation area (redrawn using data from [9])

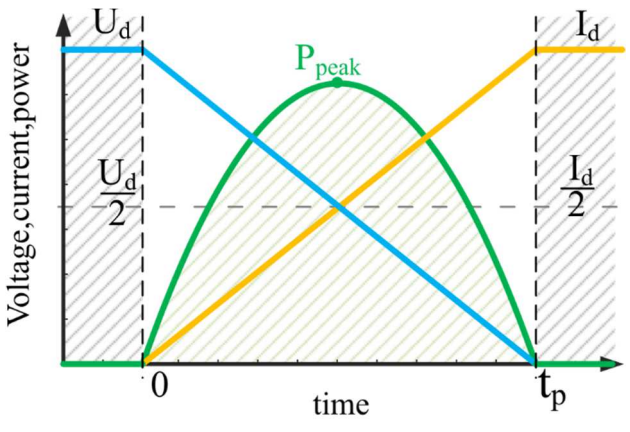

Fig. 6: Simplified voltage (blue), current (yellow) and power (green) profiles during the switching transient

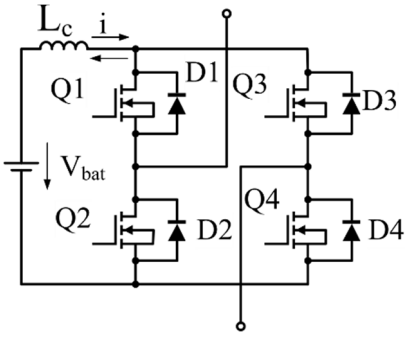

Fig. 7: Commutation inductance

Table I: Test Conditions

Peak Current [A]	136	272	408	544
Current Direction	Positive	Negative		
SoC	20%	50%	80%	
Battery Temperature [°C] (Heating or cooling for at least 5 hours)	5	20	50	

All test conditions are listed in Table I and 72 combinations of test conditions were tested. The object under test is a battery cell (Lishen Battery) with a nominal capacity of 272 Ah. It was tested up to a current peak of 544 A (2C). If the current flows into the battery, it is defined as positive current, and in reverse, it is considered as negative (see Fig. 8). The measurement setup is illustrated in Fig. 9 which is familiar with the widely used double pulse test configuration (DPT) for characterizing of semiconductors. The only difference is that 10 diodes are connected in series in the commutation loop, since the threshold voltage of the lower Schottky diode alone is not enough to block the battery nominal voltage of 3.2 V.

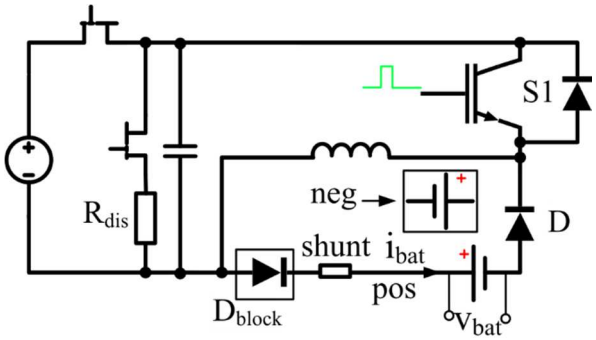

Fig. 8: Schematic of the pulse test

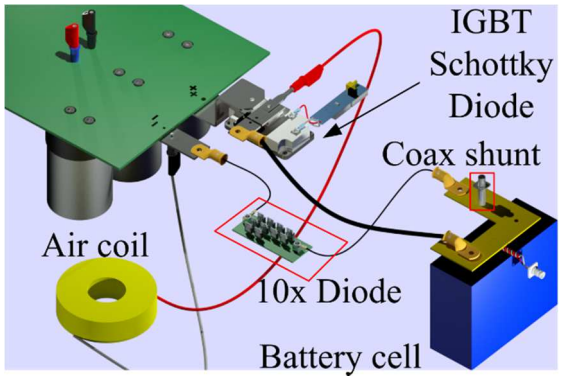

Fig. 9: Measurement setup

For measuring the battery current, the coax shunt SDN-414-10 from T&M research products was connected in series with the battery cell, while the battery voltage v_{bat} was directly measured between two battery terminals. To approximate the effective inductance, the measured currents were filtered, and their first-order derivatives were calculated during the data post-processing. The inductance can be estimated as the ratio between the absolute maximum of the measured battery voltage and the absolute maximum of the current derivative using $L_{bat} \approx V_{bat,max}/(di_{bat}/dt|_{max})$. Fig. 10 shows two of the measurement results under different measuring conditions and the corresponding approximated inductance values. All derived inductance values fall in the range of 4 to 7 nH.

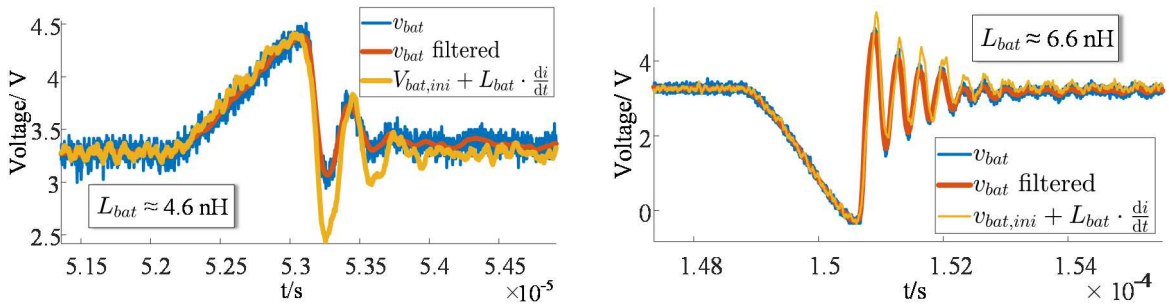

Fig. 10: Approximation of inductance introduced by battery cell: 20 % SoC, positive, 0.5C, 5°C (left); 80 % SoC, negative, 2C, 50°C (right)

What does the battery say about a pulsating load?

A configuration of battery cells with the semiconductor full bridges can provide (almost) any output voltages and frequencies. In mains parallel operation, the voltage is controlled depending on the present voltage value by switching the half-bridges to high and low impedance. Depending on the charging and discharging of the electrical storage system, the cells can be charged and discharged with sections of the mains current.

The influences of the expected load, such as calendar and cyclical ageing, as well as the change in electrical parameters associated with ageing, such as internal resistance and double-layer capacitances, have hardly been researched at present. Two publications on the subject consider on the one hand the load with pure square-wave current and on the other hand the current with a high-frequency AC component superimposed on the charging and discharging current [10, 11].

In addition to the development of the multilevel inverter, cell ageing and the change in electrical parameters during the cycle tests were further investigated.

A test bench designed for the study is cycling lithium iron phosphate cells from two different manufacturers since March 2021. In total, the setup contains 16 cells, 8 cells EVE LF50K and 8 cells Benergy BXL-LFP-50AHP with 50 Ah each (nominal value).

The cell array is divided into two groups, of which one control group is charged and discharged with DC current. The other group is charged and discharged with the pulse sequence shown in Fig. 11. The individual pulses are each a sine half-wave cut in and out at different angles. The pulse sequence thus corresponds in sections to the magnitude of the mains current and thus represents a practical cell current.

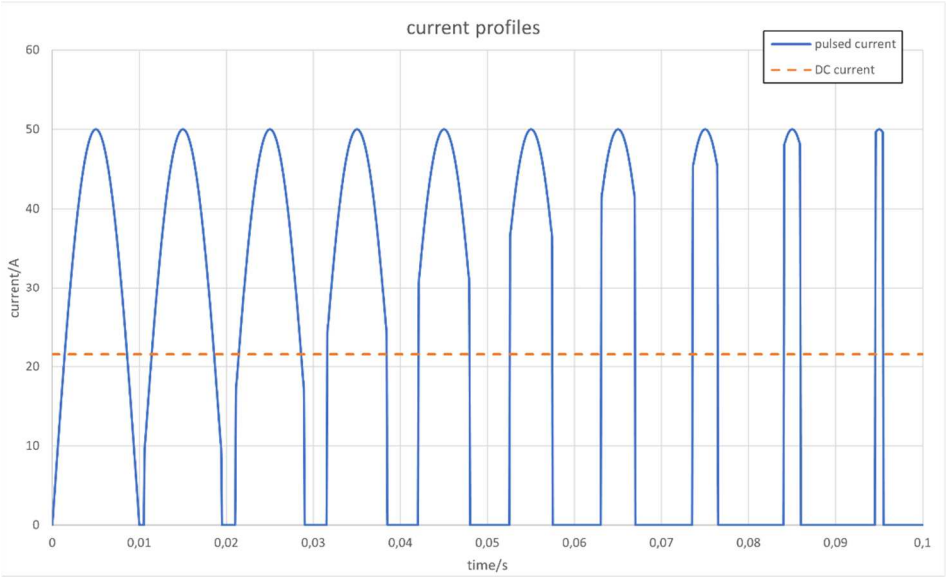

Fig. 11: Imprinted current profiles for DC- and pulsed current with same C-rate

The cell test bench shown in Fig. 12 performs load jumps and capacitance measurements at regular intervals for both load profiles in addition to cycling with DC and the current profile shown. The load steps allow the determination of the electrical parameters mentioned. With the help of the capacitance measurements, it is possible to derive the State of Health.

Fig. 12: Test bench for single cell test

A National Instruments PXI takes control of the test bench and records the measured quantities of voltage, current and temperature for each cell in the setup. Electronic loads imprint the current profile and load step shown in Fig. 11 for the electrical parameters sampled at regular intervals.

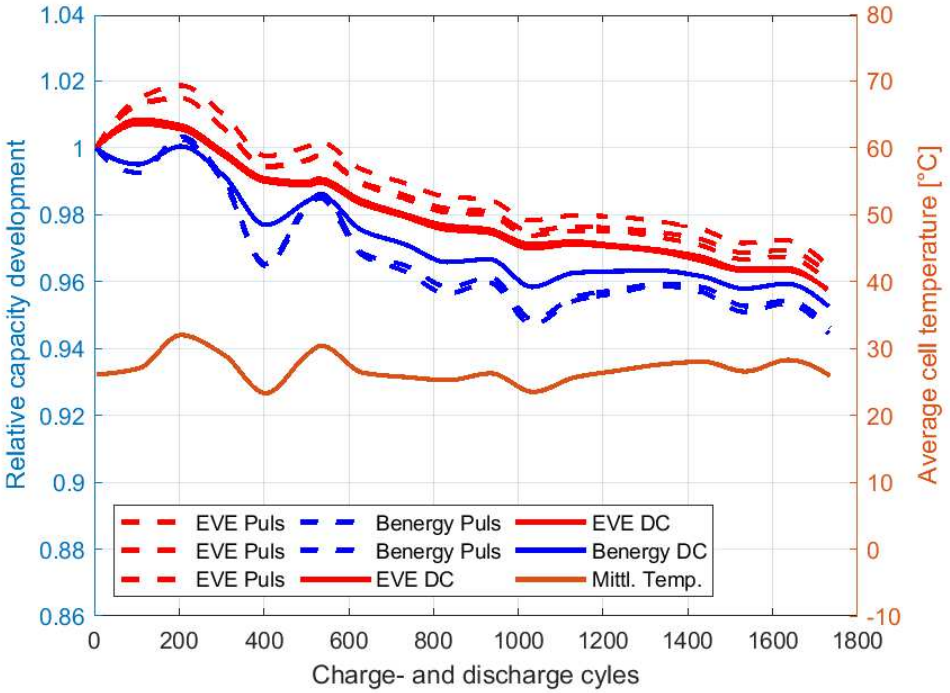

Fig. 13: Relative capacity degradation with different current profiles

So far, a selection of cells has completed almost 1800 cycles between 2.8 V and 3.4 V. Fig. 13 shows the capacity curve of the batteries that have been cycling since March 2021. So far, the pulsating current load appears to cause one of the battery types to age less. The other battery type seems to cycle age less under DC load.

Since, the test bench does not have air conditioning, the temperature has a strong influence on the capacity measurement and is therefore shown in the graph.

Conclusion

The proposed use of cascaded H-bridges for individual battery cells offers a number of advantages. In addition to full coverage of the typical BMS functions for the battery cells, active cell balancing with nominal current on cell level and highest efficiencies is possible. The topology allows arbitrary AC or DC output voltages, so no additional converters are needed. A three-phase AC-system can be built by combining three of the proposed systems.

With regard to lifetime, negative or positive effects of the operating mode on the battery cells cannot be clearly determined at present for unfiltered pulsed currents. What can be clearly stated is that the observed differences are less than 1%.

The investigated topology has no voltage on the output terminals when switched off, thus preventing short circuits. In addition, the presented approach improves repairability and allows the free use of different cell manufacturers – if the battery cell has two poles.

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