

Evaluation of Drain-Source Voltage in Switch Transient Time Intervals as Gate Oxide Degradation Precursor of SiC Power MOSFETs

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«Degradation», «MOSFET», «Reliability», «Silicon Carbide (SiC)».

Abstract

Gate oxide degradation is a major chip-related reliability issue in Silicon Carbide power MOSFETs. Being focused on turn-on/-off transient behavior of the switch, drain-source voltage waveform is employed as a gate oxide degradation precursor in this paper. Precursor evaluation is carried out in various operating conditions of the switch.

Introduction

Silicon Carbide (SiC) metal–oxide–semiconductor field-effect transistors (MOSFETs) present low conduction power loss, high temperature durability, and high frequency operation capabilities. These features pave the way for high-density power electronic applications, including electric vehicle charger, electrified aircraft systems, and DC/DC converters [1–4]. Assuring reliable performance is a major requirement in all of the above-mentioned application areas [5], [6]. SiC MOSFET reliability issues have been categorised into two main groups: Package-level (wire bond and solder layer failure modes) and chip-level (gate oxide layer and body diode failure modes) [1]. The focus of this paper is on gate oxide degradation modes.

Tunneling current into the gate oxide layer leads to gate oxide degradation [7]. Due to thin gate-oxide layer in SiC MOSFETs, a Fowler–Nordheim tunneling can inject additional electrons into oxide layer in high electric conditions [8]. Comparing SiC- and Silicon (Si)-MOSFETs, interface trapped charge at SiC-SiO₂ interface is much higher than Si counterpart. As a consequence, the device mobility is decreased by high coulombic scattering and few numbers of free carriers [9]. A total positive charge created by oxide and interface trapped charges result in a negative shift of the threshold voltage (V_{th}) and vice versa. The effect of trapped charges on V_{th} depends on the distance between trapped charges in the oxide and SiC conduction channel [8].

To detect the gate oxide degradation level in SiC MOSFETs, V_{th} [10], drain leakage current [11], gate leakage current [5], gate Miller plateau voltage (V_{GP}) [12], gate Miller plateau time (t_{GP}) [7], switch turn-on delay [13], switch junction capacitance [8], and on-state resistance (R_{DS-on}) [14] have been employed as condition monitoring (CM) precursors in the literature. The mentioned CM precursors are generally adopted from the conventional Si-based MOSFETs [7]. However, some of the above-mentioned precursors behave differently during the SiC MOSFET gate oxide degradation process in comparison to the ones of Si MOSFETs. For example, in transitioning from brand-new condition to degraded condition in Si MOSFETs, there is a rebound in t_{GP} value [15], while t_{GP} is a strictly increasing function of gate oxide degradation level in SiC MOSFETs [7]. One other problem in the process of adaption of Si MOSFET CM precursors for SiC MOSFETs is that SiC MOSFET operational parameters, such as R_{DS-on} , on-state voltage drop (V_{DS-on}), gate input capacitor (C_{rss}), total gate charge (Q_g), diode reverse recovery time, t_{GP} , etc., are considerably smaller in value in comparison to those of Si-based MOSFETs and IGBTs. Therefore, specialized characterization of the proposed gate oxide CM precursor is required for SiC MOSFETs.

In the process of developing a precursor for CM purposes, it is important to examine the proposed CM precursor in various circuit configurations and conditions. Because the CM precursor should be able to monitor the gate oxide health status in real circuit conditions and without interrupting the switch normal performance [16].

The presented CM precursors in the literature are usually affected by the operational conditions of the switch. For example, increasing switch junction temperature (T_j) leads to a negative shift in V_{th} value [3]. Besides, the transient behavior of the SiC MOSFET in inductive loading condition is different in comparison to the transient behavior in resistive loading condition. Considering this, examining the proposed CM precursor in various switch conditions and circuit configurations is a fundamental requirement in the process of developing a CM precursor for gate oxide degradation.

In this paper, the effect of gate oxide degradation on switch turn-on and -off transient behavior is studied and characterized using drain-source voltage (V_{DS}) waveform. Using V_{DS} waveform, V_{GP} and t_{GP} , as the two main parameters of Miller plateau, are obtained for brand-new and degraded switch conditions. Besides, the changes in switch transient behavior under different circuit and switch conditions are studied. To achieve more comprehensiveness:

- Using the developed degradation set-up based on high electric field stress (HEFS) mechanism, various rates of gate oxide degradation is applied to the switch, and the transient behavior is studied in different rates of degradation.
- Switch transient behavior is evaluated for both resistive and inductive loading conditions on the switch. This basically enables the studies of this paper to be used for resistive loads (such as pulsed power applications) and inductive loads (such as DC/DC converters and resonant converters).
- The evaluations are carried out for normal and high T_j levels of the switch.

Gate Oxide Degradation in SiC MOSFETs

V_{GP} of the switch in both turn-on and -off transient time intervals of the switch is depended on V_{th} and can be written as (1) [17].

$$V_{GP} = V_{th} + \sqrt{\frac{I_D L_{CH}}{\mu C_{ox} Z}} \quad (1)$$

, where I_D is the drain channel current, L_{CH} is the channel length, C_{ox} is the specific gate oxide capacitance, Z is the channel width, and μ is the channel carrier mobility. Since μ is a decreasing function with respect to the applied gate oxide stress time (t_{stress}) [18], V_{GP} is an increasing function of t_{stress} .

In the turn-on process, V_{DS} falls from the off-state blocking voltage (V_{Bus}) to V_{DS-on} . The main part of the V_{DS} decrement process occurs when V_{GS} is constant, and the output current of the driver discharges the gate-drain capacitance (C_{GD}). This time interval is known as Miller plateau. Assuming V_{DS} falls linearly from V_{Bus} to V_{DS-on} during switch turn-on process, Miller time in turn-on transient time of the switch (t_{GP-on}) can be written as (2).

$$t_{GP-on} = R_G C_{GD,avg} \frac{V_{Bus} - V_{DS-on}}{V_{Dr} - V_{GP}} \quad (2)$$

, where R_G and V_{Dr} are the total gate resistance and the applied voltage of the gate driver respectively. Since V_{GP} increases due to gate oxide degradation (according to (1) and Figure.1(a)), it can be concluded that t_{GP-on} also increases over the degradation process. As a result, $d(V_{DS})/dt$ in turn-on process of the switch is decreased during the degradation, as shown in Figure.1(b).

In the turn-off process, V_{DS} increases from V_{DS-on} to V_{Bus} . The same as the turn-on process, the major part of the changes in V_{DS} occurs in the Miller plateau time interval. In this time interval, V_{GS} is approximately constant, and the driver current charges C_{DG} . On this basis, Miller time in turn-on transient time of the switch (t_{GP-off}) is described as (3).

$$t_{GP-off} = R_G C_{GD,avg} \frac{V_{Bus}}{V_{GP}} \quad (3)$$

Regarding (1), V_{GP} increases over the gate oxide degradation (see Figure.1(c)), and t_{GP-off} decreases in the degradation process as the result.

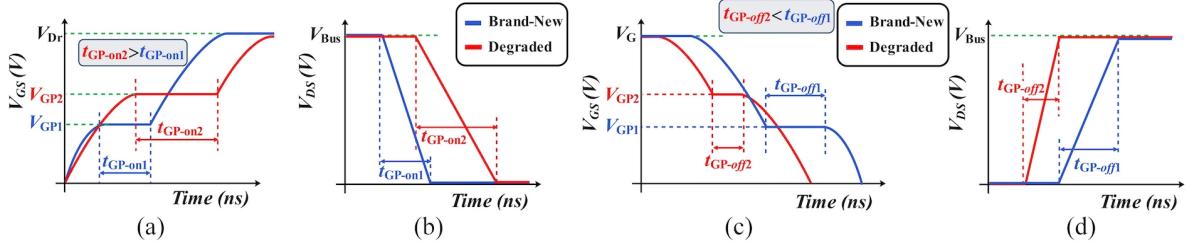


Figure 1: (a) Increment in V_{GP} and t_{GP} , and (b) decrement in $d(V_{DS})/dt$ in turn-on process during degradation; (c) Increment in V_{GP} and decrement in t_{GP-off} , and (d) increment in $d(V_{DS})/dt$ in turn-off process during degradation

Experimental Set-up

Commercially available SiC discrete MOSFETs 650V/22A are used to examine transient changes over the gate oxide degradation process. The switch is employed in a power circuit as shown in Figure.2(a). In Table.1, the circuit specifications and parameters of the power circuit are listed. $R_L = 10 \Omega$ is considered for the resistive load tests. $R_L = 3.4 \Omega$ and $L_L = 220 \mu\text{H}$ is considered for the inductive load tests. $R_{G_{ext}}$ is the external gate resistance (see Figure.2(a)). In Figure.2(b), the laboratory set-up, consisting of the direct switch structure, resistive load and inductive load, is shown.

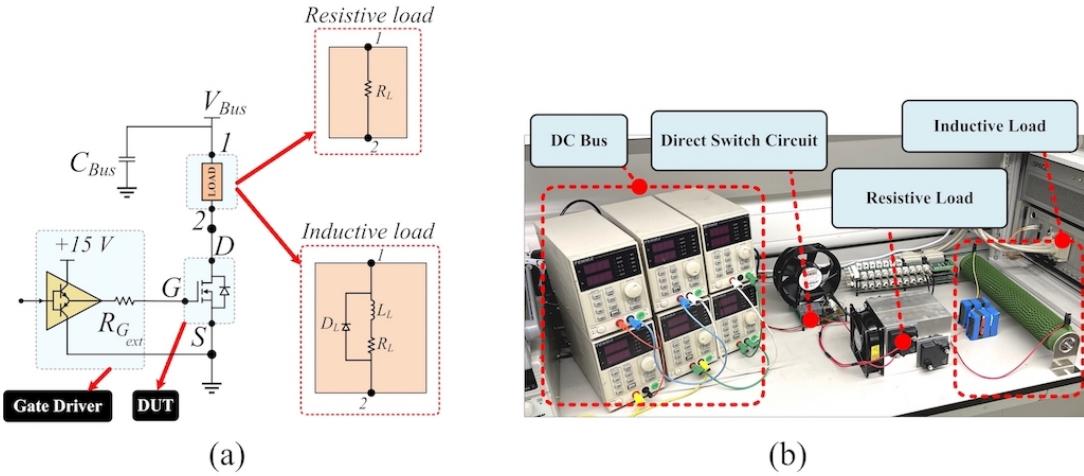


Figure 2: (a) Detailed view of the employed power circuit in the experimental set-up, and (b) overall view of the implemented laboratory set-up

Table 1: The overall specifications and ratings of the implemented power circuit

V_{Bus}	93 V to 232V
C_{Bus}	$34 \mu\text{F}$
f_s	200 kHz
D	10%
$R_{G_{ext}}$	10Ω

Gate Oxide Degradation Rate Effect

Two stressors are introduced for the accelerated gate oxide degradation testings, i.e., high electric field stress (HEFS) and high temperature stress [1], [7]. In Figure.3(a), the employed degradation circuit based on HEFS

mechanism is shown. Using different values of gate stressor voltage (V_{stress}), Miller plateau changes due to the gate oxide degradation is examined. The gate oxide breakdown voltage of the SiC MOSFET case study switch is found as 39 V. In [19], it is shown that for a Si MOSFET with similar gate structure and similar ratings, the breakdown voltage is 65 V which clearly demonstrates the vulnerability of SiC MOSFET gate oxide layer against HEFS.

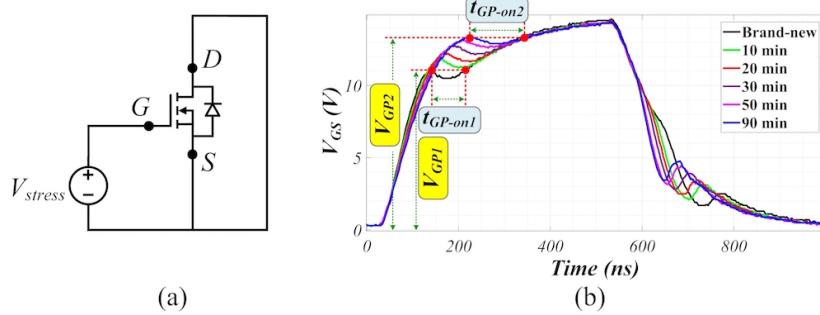


Figure 3: (a) HEFS circuit for gate oxide degradation, and (b) V_{GP} and t_{GP-on} changes during the gate oxide degradation tests with $V_{stress} = 37V$

In Figure 3(b), the effect of degradation on V_{GP} and t_{GP-on} of the switch is shown in $V_{stress} = 37V$ and stress time of 90min. It can be seen that V_{GP} value is changed from $V_{GP1}=11.9V$ to $V_{GP2}=13.4V$ due to gate oxide degradation. Moreover, in the turn-on transient, t_{GP-on} has experienced a value change from 68ns to 114ns.

Based on the gate breakdown voltage of the switch, V_{stress} is chosen as 31V and 37V for the experimental evaluation of the proposed CM technique. In Figure 4 and Figure 5, the overall changes in the transient behavior of the switch are shown for $V_{stress} = 31V$ and $V_{stress} = 37V$ respectively. The gate oxide complete failure occurs at $t_{stress} = 93min$ with $V_{stress} = 37V$, while it occurs at $t_{stress} = 566min$ with $V_{stress} = 31V$. It can be inferred that although the rate of gate oxide degradation is different, V_{DS} rise and fall time intervals are changed similarly in both the experiments.

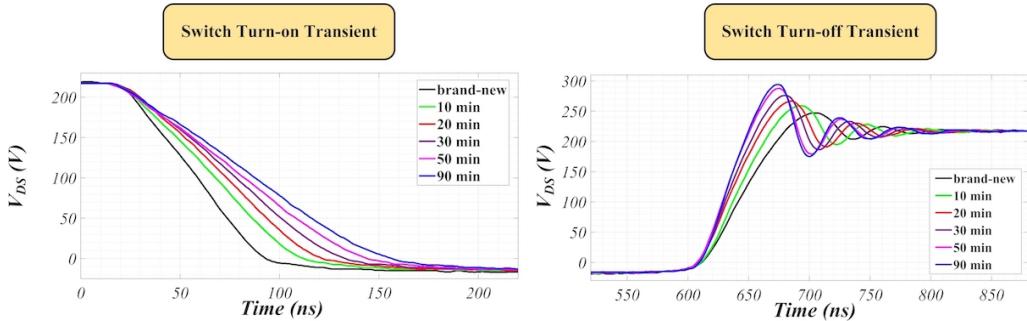


Figure 4: V_{DS} rise time and fall time changes during the gate oxide degradation tests with $V_{stress} = 37V$ and $V_{Bus} = 217V$

Load Type Effect on Switch Transient Behavior

The circuit diagrams of generic resistive and inductive loads are depicted in Figure 2(a). The existence of the free-wheeling diode (D_L) and uninterrupted current of the inductor in the turn-on and turn-off intervals cause I_D to be different in the mentioned transient times.

In the turn-on process for inductive load, D_L conducts the whole of the load current. When V_{DS} decreases from V_{Bus} to V_{DS-on} , D_L is reversed-biased, and the load current is commutated to the switch drain-source terminals. Therefore, in the turn-on process, I_D is constant while V_{DS} decays from V_{Bus} to V_{DS-on} (see Figure 6(a)). Accordingly, (1), (2), and (3) are correct for the inductive load without any approximation. It is because V_{GP} (see

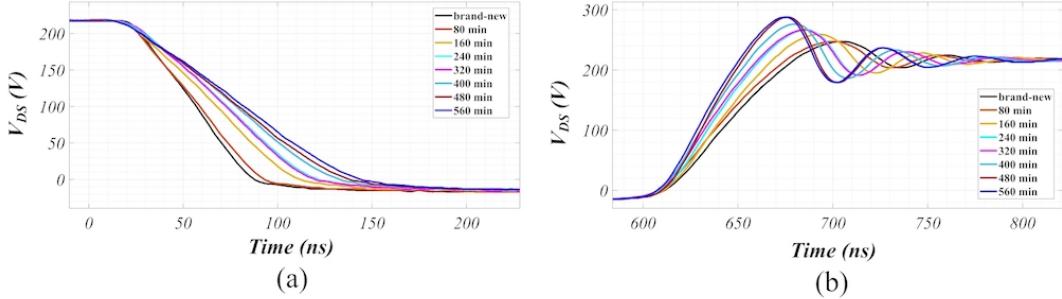


Figure 5: V_{DS} rise time and fall time changes during the gate oxide degradation tests with $V_{stress} = 31\text{V}$ and $V_{Bus} = 217\text{V}$

(1)) is constant during the turn-on process. For the resistive load case, changes in I_D occur simultaneously with V_{DS} changes, and the sudden change in the load current is not detectable as presented in Figure.6(a). On this basis, according to (1), V_{GP} is not constant, and it changes dynamically during the turn-on process. Based on (1), at the beginning of the switch turn-on process, V_{GP} approximately equals to V_{th} , and when the turn-on transient time is terminated, it has its maximum value. Therefore, for the resistive load cases, (1), (2), and (3) can be used with some approximations.

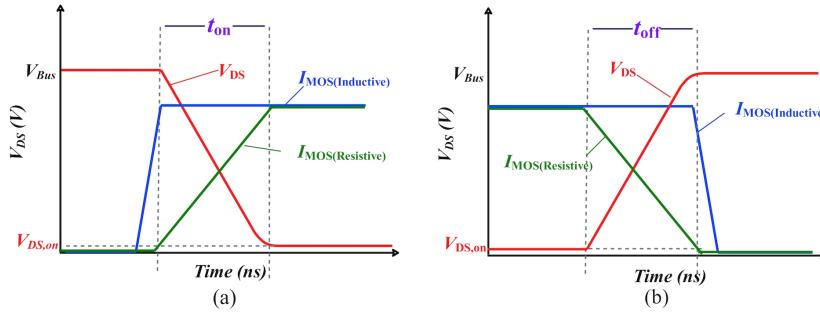


Figure 6: V_{DS} and I_D waveforms of the switch in the resistive and inductive loads; (a) turn-on and (b) turn-off transient behavior

In the turn-off process, V_{DS} increases from V_{DS-on} to V_{Bus} . I_D is constant, since D_L is reverse-biased during this time interval. When V_{DS} reaches to V_{Bus} , D_L starts conducting. Hence, at the end of the turn-off interval, the inductor current is commutated to the D_L path. Accordingly, it can be concluded that during turn-off time interval, V_{GP} is constant, thus (1), (2), and (3) can be served without approximation.

The developed gate oxide degradation set-up is employed to degrade the gate oxide layer with $V_{stress} = 37\text{V}$. The variations in turn-on and turn-off transients of the switch due to the gate oxide degradation in $V_{Bus} = 217\text{V}$ are shown in Figure.4 in power circuit with resistive load. The variations in turn-on and turn-off transients of the switch due to the gate oxide degradation in $V_{Bus} = 232\text{V}$ are shown in Figure.7 in power circuit with inductive load. At the beginning of the turn-on transient time in inductive load tests, V_{DS} fall time shows a slowed-down behavior, which is due to the power path parasitic inductance out of the free-whiling diode path. This inductance acts similar to an on-state snubber and does not allow I_D of the switch to have an instant incremental change. Accordingly, at the beginning of the turn-on process, the current of the parasitic inductance starts increasing. Its voltage is proportional to the integration of its current and approximately has a second order profile. Thus, V_{DS} will have two slopes at the beginning, if parasitic inductance values of the path are considerable. In Figure.7, during the transitioning from brand-new condition to fully degraded gate oxide, the rise time value of the switch has changed from 73 ns to 108 ns and fall time has changed from 54 ns to 45 ns.

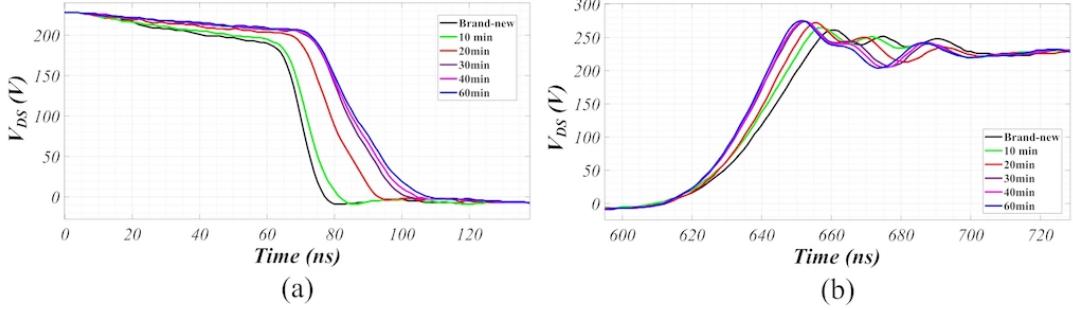


Figure 7: V_{DS} changes during gate oxide degradation test with $V_{stress} = 37$ V and $V_{Bus} = 232$ V in inductive load; (a) turn-on transient and (b) turn-off transient

Junction temperature effect on Miller plateau

To investigate the effect of T_j on V_{DS} transient time intervals, two different heat dissipation topologies are implemented. The case study switch is examined both in the brand-new and degraded conditions in the two heat dissipation topologies. Using the thermal equivalent circuit model for the structure of switch and heatsink, T_j , switch case temperature (T_c), heatsink temperature (T_{HS}), and ambient temperature (T_{Am}) can be modeled as shown in Figure 8. On this basis, T_c and T_j can be obtained using (4) and (5).

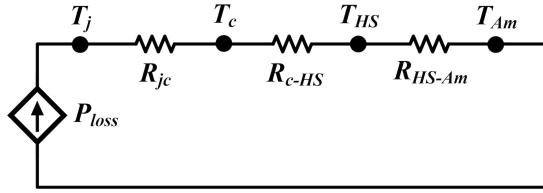


Figure 8: Thermal equivalent circuit of the switch and heatsink configuration

$$P_{loss} = \frac{T_c - T_{Am}}{R_{c-HS} + R_{HS-Am}} \quad (4)$$

$$P_{loss} = \frac{T_j - T_c}{R_{jc}} \quad (5)$$

, where P_{loss} is switch total power loss. Moreover, R_{c-HS} , R_{HS-Am} , and R_{jc} are thermal resistance from case to heatsink, thermal resistance from heatsink to ambient, and thermal resistance from junction to case of the switch respectively. Based on the power circuit specification, which is listed in Table 1, $P_{loss} = 7.41$ W.

A) Normal junction temperature configuration: In this configuration, a forced air-cooled heatsink with $R_{HS-Am} = 0.07$ K/W is employed. A thermal pad with thermal conductivity of 8.2 W/m.K is used as the thermal interface between the switch and the heatsink. In Figure 9(a), the mounted case study switch on the heatsink is shown. Using (4) and (5), it is calculated that $T_c = 34^\circ\text{C}$ and $T_j = 45^\circ\text{C}$. T_c measurement is carried out using thermal camera (model: FLIR ONE PRO LT), and the captured thermal image is shown in Figure 9(c).

B) High junction temperature configuration: In this configuration, a heatsink with relatively large value thermal resistance parameter is used to achieve a high temperature profile of the switch. No air cooling is considered, and the heatsink thermal resistance is $R_{HS-Am} = 15.2$ K/W. Similar thermal pad is employed as the thermal interface between the switch and the heatsink. In Figure 9(b), the switch and the small-size heatsink are shown. In this mode, using (4) and (5), it is calculated that $T_c = 146^\circ\text{C}$ and $T_j = 157^\circ\text{C}$. The thermal image of the switch in this thermal configuration is shown in Figure 9(d).

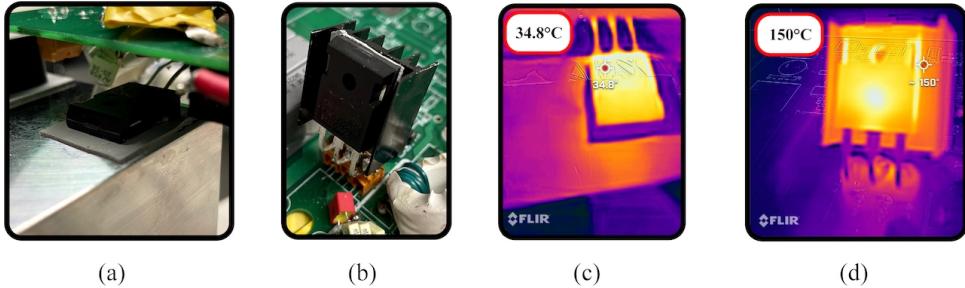


Figure 9: Heatsink and switch configurations of (a) normal temperature design and (b) high temperature design; Thermal images of the switch during operation in (c) normal temperature configuration and (d) high temperature configuration

For the brand-new switch, the results are shown in Figure.10. As can be seen, the rise time and fall time changes are 10ns and 2ns respectively. For the degraded switch, the rise time and fall time changes are 4ns and 1ns respectively, as shown in Figure.11. It can be inferred that changes in V_{DS} rise and fall time values due to temperature rise are considerably smaller than the changes in rise and fall time values due to gate oxide degradation.

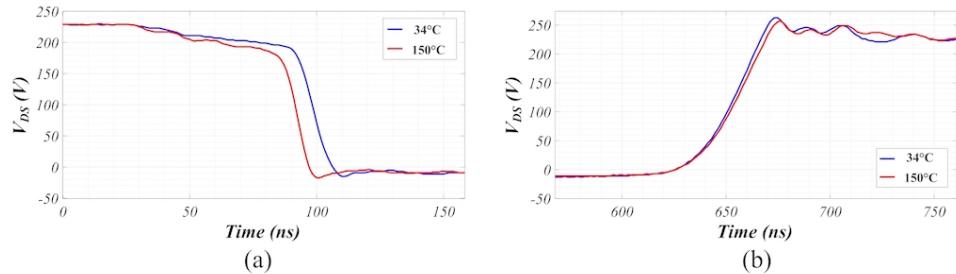


Figure 10: (a) Rise time and (b) fall time changes of V_{DS} due to temperature increment for brand-new switch

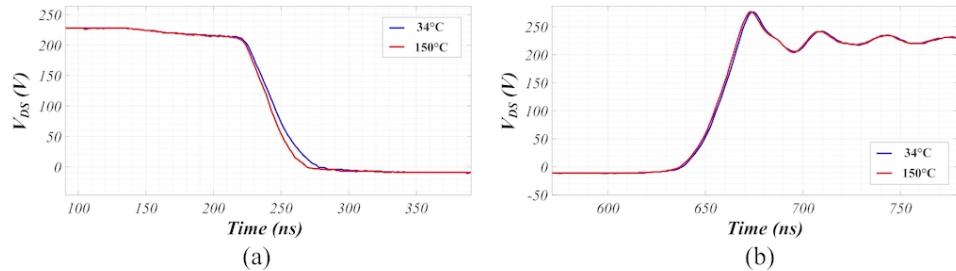


Figure 11: (a) Rise time and (b) fall time changes of V_{DS} due to temperature increment for degraded switch

Conclusion

Being focused on gate oxide degradation failure of SiC MOSFETs, the transient behavior of the switch was studied in different circuit configurations and switch operational conditions to develop an understanding of the effect of gate oxide degradation on drain-source voltage waveform of the switch. Studies on switch drain-source voltage waveform showed that although the drain-source voltage waveform is partially affected by the load type, junction temperature, and rate of degradation, it undergoes major changes in rise time and fall time values during the gate oxide degradation process. Therefore, it can be concluded that the turn-on and -off transient time intervals

of the drain-source voltage waveform of the SiC MOSFET switches can be used as a robust indicator of gate oxide degradation in a wide range of applications.

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