Powercycling Test Bench with Realistic Loss Distribution and Temperature Ripples

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Abstract

An innovative test bench is presented, which allows the powercycling for semiconductors under a superposition of temperature ripples with different frequencies. In addition to the implementation of switching losses, this creates loadpatterns which are similar to the application. Further, the leakage current of the semiconductors as a thermo-sensitive parameter is introduced. First results validate the concept.

Introduction

Accurate predictions on the lifetime of power semiconductors are crucial for economical converter designs. An early failure due to power cycling will lead to costly standstill periods. This is especially true for wind turbines, where precious yield is lost. To prevent this, the converter can easily be designed with a large safety margin in lifetime. The overdesign in lifetime is achieved by additional semiconductors, which consequently leads to additional investment costs.
In the following, a powercycling test bench is presented, which enables the testing of power semiconductors under an application-based superposition of different temperature ripples and loss sharing.
In the classical semiconductor power cycling test, the semiconductors are stressed with forward conduction losses. This is achieved by connecting a low voltage current source with the devices and changing the conducting device periodically. External switches switch the load current. To finish the test in a feasible time frame highly accelerated life test (HALT) are used. However, in the application a significant

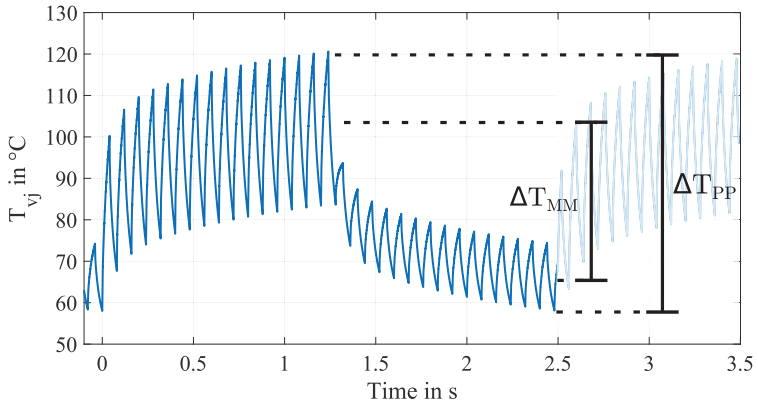


Fig. 1: Possible temperature pattern of innovative test bench

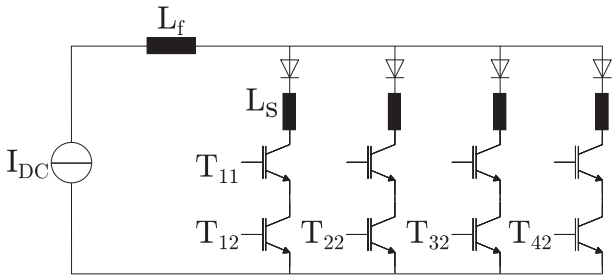


Fig. 2: Simplified electrical circuit diagram of the powercycling test bench

amount of losses are switching losses. A much higher forward current compared to the application has to be used to generate comparable temperature ripples with conduction losses only. The high forward current tends to stress the bondwire more due to self-heating. This problem intensifies with the need for highly accelerated tests.
Another mismatch from the application is how the semiconductor is stressed with different temperature swings. Recent publications on the linear cumulative damage theory show that a general addition of different temperature swings and their respective lifetime consumption is valid [1]-[3], as long as the same failure mechanism is stimulated. This concept, known as the Miners Rule [4], is limited to time serially events. However, in a complex mission profile, many different temperature ripples occur simultaneously. Different ripples with different period times superimpose upon each other. One single test for this has been done in [5], here the big and slower cycle was dominant for the failure. In lifetime calculations the superpositon is generally answered by a simulation with different time resolutions [6]-[7]. Often, a low resolution is used for load changes. Here, neither the frequency of the loadcurrent nor the thermal impedance can be rendered.
In [8], it is shown that the used resolution has an influence on the calculated lifetime. The large temperature ripple due to fluctuations in the wind can have a significant share of the overall calculated lifetime consumption [9]. However, this superposition of different temperature swings is not tested in standard power cycling test. A potential simulated temperature pattern of the test bench is shown in Figure 1. The pattern consists of two superimposed temperature ripples. A classical rainflow-algorithm will count the big ripple as the peak to peak value T_{pp}. Although, a calculation with a low resolution for slow temperature swings would calculate more like the middle to middle value T_{MM}. The question arises what the effective lifetime consuming temperature-ripple is and how the prevailing frequencies influence this.

Test Bench Design

A simplified electrical circuit diagram of the test bench is shown in Figure 2. The test bench consists of a low voltage current source (I_{DC}), a filter inductance (L_f), four switching inductances (exemplary L_s) and four IGBT half-bridge modules, with the lowside (LS) switches T_{12}-T_{42}. The concept of adding switching losses to power cycling tests with inductances was published and discussed by Herold and Lutz in [10] and [11]. These additional inductances cause voltage peaks at the turn-off of the IGBTs. The voltage peaks, in addition to the slopes in the current, lead to switching losses inside the devices. The current and voltage for one turn-off event during power cycling is depicted in Figure 3.

Three frequencies are used to control the test bench and create temperature patterns that consist of slow and fast ripples at the same time:

- Frequency of switching between any LS-Switch f_{sw}
- Frequency of load alternating between T1 and T2, or T3 and T4 with f_{fast}
- Frequency of varying the modulation index of each device f_{slow}

The usages of these frequencies are further explained in Figure 4. The shown pattern starts with an alternating switching between T_1 and T_2. This switching is done with f_{sw}. With this switching, the switching losses are introduced to the modules. T_1 is on 90% of the time, while T_2 is 10% of the time

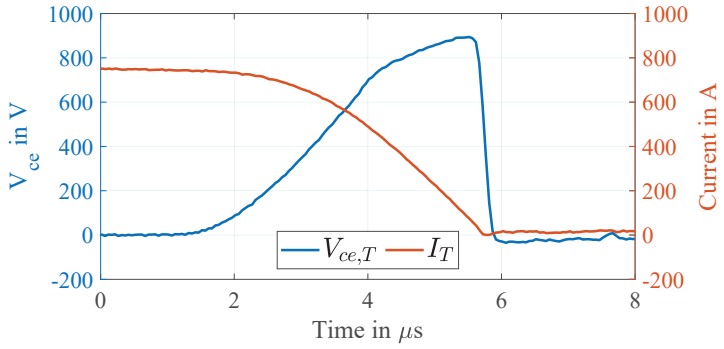


Fig. 3: Measurement: Voltage and Current during switching-event, $L_s \approx 1.3\,\mu H$

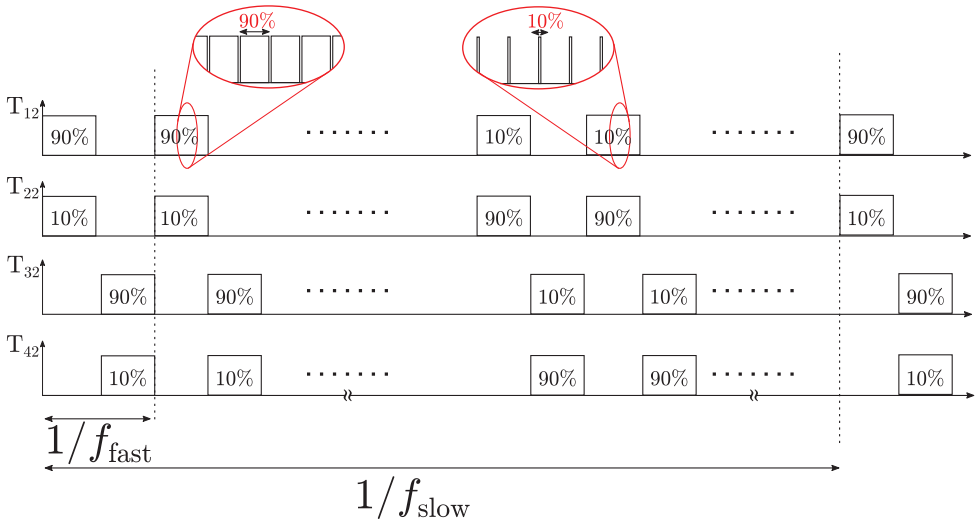


Fig. 4: Exemplary control Signals of LS-Switches

(the modulation indices of 90% and 10% are just an example to illustrate the functionality). After half of the fundamental period $1/f_{\text{fast}}$ the current is switched between T_3 and T_4. This continues until half of the period time of f_{slow} is reached. Here the modulation index is changed. So for example, T_1 is now on only 10% of the time. The change in the modulation index forms the large temperature ripple with f_{slow}. The alternation between switching the current and not switching forms the second temperature ripple with $1/f_{\text{fast}}$.
With these frequencies, a complex loadpattern can be reproduced. Hence, a rotor-side converter semiconductor of a windturbine can be reproduced, for example. With a change of f_{sw} a realistic loss distribution can be achieved. The second frequency f_{fast} can be set to the frequency of the nominal current. The third frequency f_{slow} can be adjusted to reproduce turbulent wind behavior. Additionally to the frequencies the value of the DC-Current (I_{DC}) and the modulation index (a) are degrees of freedom in the design of the testpattern. The test bench is not limited to four devices, the pattern can also be designed for six or more devices.

Additional Leakage Current Measurement

The leakage currents of power semiconductors are highly temperature-dependent. The positive feedback loop between power losses and temperature increase is known as thermal runaway, which affects high-voltage devices in the blocking state if the cooling is insufficient [12].
The physical principles for the temperature dependence will be briefly summarized in the following. The leakage current density j_r originates from charge carriers swept across the depletion region. It can be split into the diffusion current density, caused by the concentration difference of the PN Junction j_s and the drift current density, generated by the depletion region j_{DR}. As per [13], they can be described as:

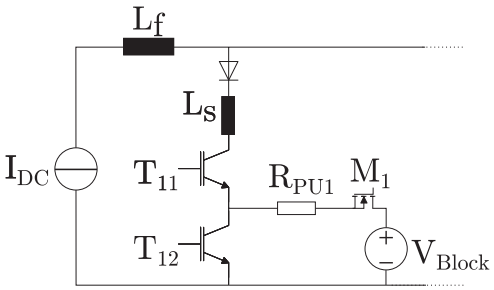


Fig. 5: Circuit Design to load T_{12} with V_{Block}

$$j_r = j_s + j_{\text{DR}} = \frac{q \cdot {n_i}^2}{N_D} \cdot \sqrt{\frac{D_p}{\tau_p}} + \frac{n_i \cdot q \cdot w_{\text{DR}}}{\tau_{sc}}, \tag{1}$$

where q represents the electron charge constant, n_i the intrinsic electron concentration, N_D the doping concentration, D_P the hole diffusion coefficient, τ_p the holes lifetime, τ_{sc} the carrier lifetime in the space charge region and w_{DR} is the width of the space charge region under the blocking voltage. The intrinsic carrier concentration of silicon can be stated as [14]:

$${n_i}^2(T_j) = C_1 \cdot T_{\text{j}}^3 \cdot \text{e}^{-\frac{C_2}{T_{\text{j}}}}. \tag{2}$$

Equation (1) and (2) show that the leakage current is strongly positively related to the junction temperature of the device. The strong dependence makes the leakage current a potent thermo-sensitive parameter (TSP). The $V_{\text{CE}}(T_j)$-method is very linear and provides a mean value over all chips. A minor degradation in the solder layers, which leads to a temperature enhancement of a small fraction of the whole chip area results therefore only in a relatively slight increase of the $V_{\text{CE}}(T_j)$. The leakage current, however increases over proportional with just a small hot spot.

The indirect measurement is shown in Figure 5. After the LS-Switch T_{12} is switched off, an additional DC-Voltage source (V_{Block}) is connected over the pull-up resistance R_{PU}. After some µs the MOSFET M_1 is switched off. Due to the leakage current the voltage over T_{12} decreases.
This behavior is shown for two temperatures in Figure 6 during power cycling. The figure shows the V_{CE} of T_{12} in the beginning of a temperature ripple at 90 °C (left) and in the end of the ripple at 130 °C (right). First the initial switch-off takes place, marked with the high voltage peak due to the switching inductances. After this the voltage rises to the voltage level of V_{Block}, subsequently the voltage source is disconnected and the voltage over the devices decreases. At the higher temperature the voltage decrease

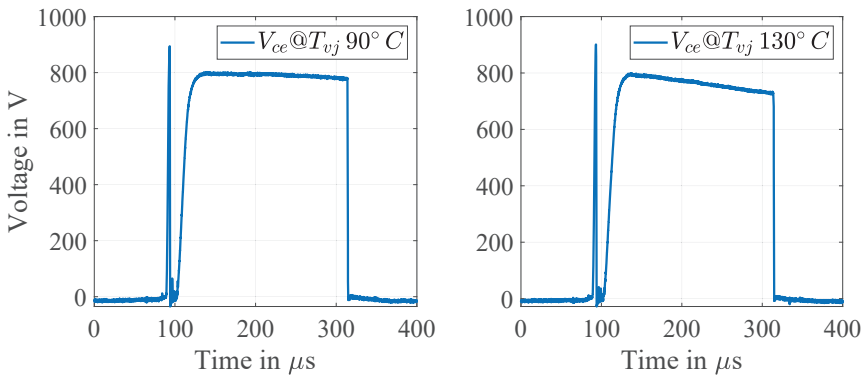


Fig. 6: Measurement: V_{CE} during powercycling, with $V_{\text{Block}} = 800\,\text{V}$, $f_{\text{sw}} = 2\,\text{kHz}$, left: beginning of temperature ripple with $T_j = 90\,°\text{C}$, right: end of temperature ripple with $T_j = 130\,°\text{C}$

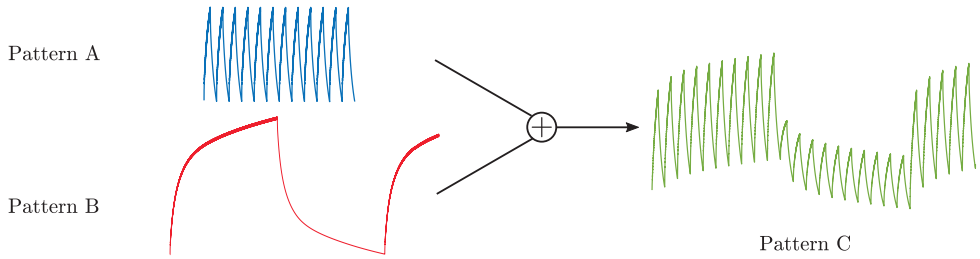


Fig. 7: Patterndesign: the simulataneous superposition of different temperature ripples

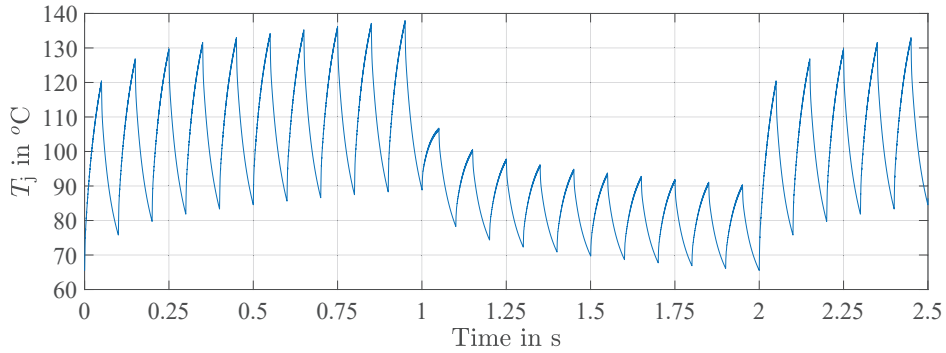


Fig. 8: Simulation: Target pattern **C**, from 0 s to 1 s a 50 K ripple is present, at 1 s the modulation index is changed, this change forms the big superimposed ripple with 72 K with f_{slow}

is much faster due to the increased leakage current.
For the power cycling periodically Z_{th}-Measurements are done with the $V_{\text{CE}}(T_j)$-Method. For this fast and potent clamping circuits and measurement-current sources were designed.

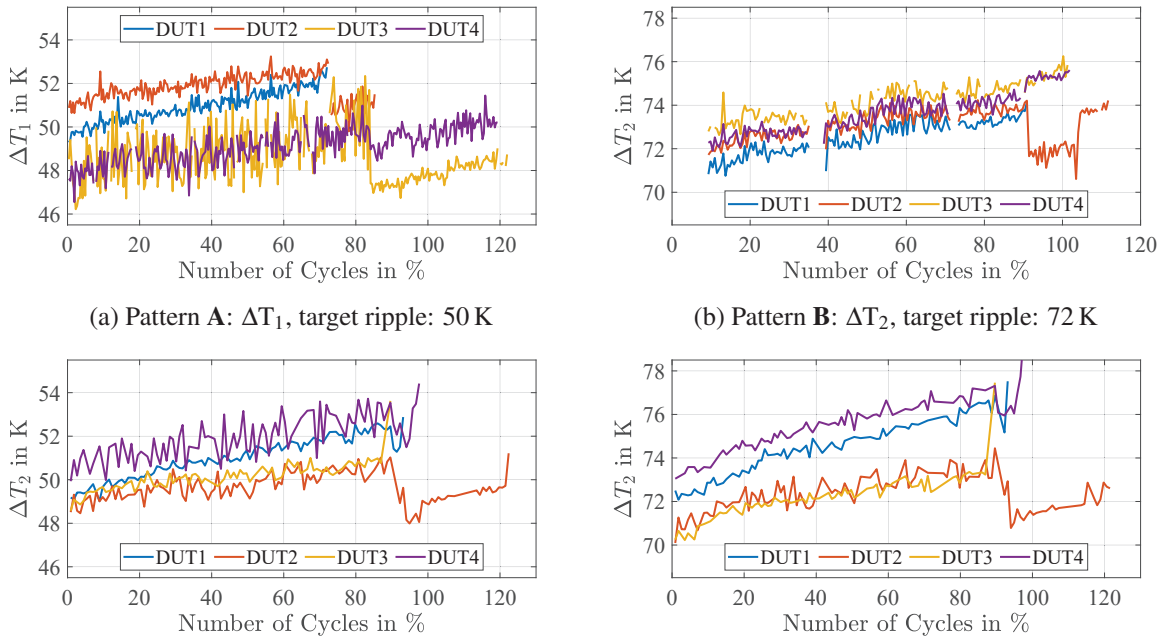
Patterndesign

For the first testruns, three different testpatterns have been designed. The first two patterns, pattern **A** and pattern **B**, are classic single-temperature-ripple powercycling patterns. The final pattern is a simultaneous superposition of the prior temperature ripples. In contrast to other tests, the new pattern is not a serial switching between pattern **A** and **B**, but rather a new pattern that includes both ripples simultaneously. Figure 7 illustrates this combination of the patterns. Table I summarizes the three patterns.

Table I: Temperature ripples and patterndesign

	ΔT_1 10 Hz $t_{\text{on}} = 0.05$ s	ΔT_2 0.5 Hz $t_{\text{on}} = 1$ s
Pattern **A**	50 K	-
Pattern **B**	-	72 K
Pattern **C**	50 K (only half of the time)	72 K

Pattern A only includes a 50 K ripple with a frequency of 10 Hz. Pattern **B** consist of a 72 K ripple with a frequency of 0.5 Hz. The final pattern, pattern **C**, superimposes these two ripples. The final pattern **C** is shown in Figure 8. The definition of the time t_{on} for the superposition of ripples is questionable. A rainflow algorithm, which is state-of-the-art in the lifetime calculation, does not differ if the ripples are superimposed or time serial, so the stated t_{on} time for pattern **C** is how a rainflow algorithm calculates the time.



(a) Pattern **A**: ΔT_1, target ripple: 50 K

(b) Pattern **B**: ΔT_2, target ripple: 72 K

(c) Pattern **C**: ΔT_1, target ripple: 50 K

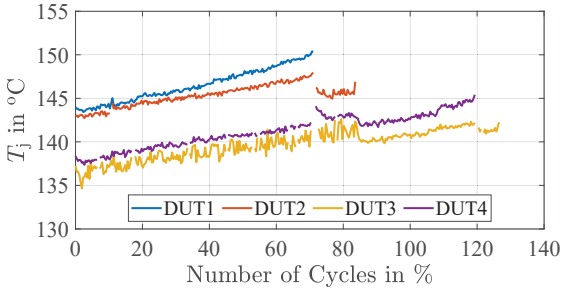
(d) Pattern **C**: ΔT_2, target ripple: 72 K

Fig. 9: Measurement: temperature ripples, ΔT_1 and ΔT_2 for pattern **A**, **B** & **C**

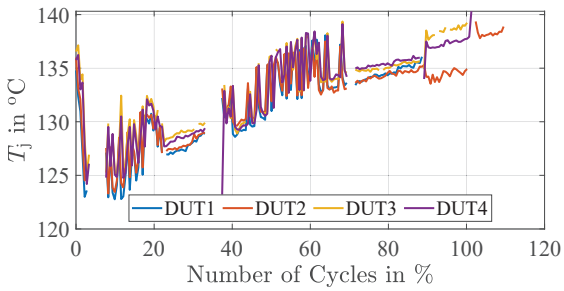
Powercycling Results

Each pattern has been tested with four devices, namely FF650R17 PrimePack modules. The results of the temperature ripple measurements are shown in Figure 9. Two particular findings have to be mentioned. In general, the temperatures tend to rise. However after one device has failed, the values of the remaining devices tend to jump to lower values. After one device has failed the test bench stops, and the particular device is changed manually with a dummy device. This dummy device has a higher power class, though. The exchange seems to influence the losses in the remaining switches. A relative small decrease in the switching inductances L_s can reduce the temperatures in the occurrent values. The lower temperatures result in a prolonged lifetime of the remaining devices.
Another finding is the difference in the absolute values between different devices. This is partly because of the inequality in the switching inductance L_s, small variations in the thermal coupling or simple device variations. The mean value of the measured ripple at the beginning of the test and the target ripples, however show a good agreement.

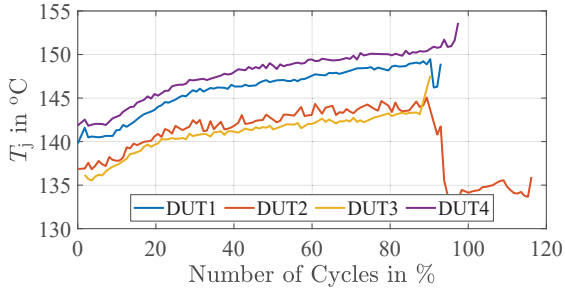
Similar behavior can also be seen in the maximum junction temperatures of the corresponding ripples. These temperatures are plotted in Figure 10. Again the jumps in the temperature after one device has been changed are visible. In theory, pattern **B** should have the same maximum temperatures as **A** and **C**. For this purpose, the cooling water temperature had to be increased from 15 °C to 45 °C. Unfortunately, the control of the cooling system could not keep this temperature constant, which resulted in a 5 K fluctuation in the cooling water temperature, this fluctuation is also visible in the maximum junction temperature.



(a) Pattern **A**: maximum junction temperature trend



(b) Pattern **B**: maximum junction temperature trend



(c) Pattern **C**: maximum junction temperature trend

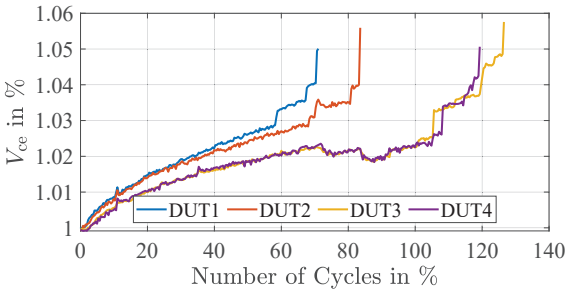
Fig. 10: Measurement: maximum junction temperature during powercycling for pattern **A**, **B** & **C**

The resulting V_{ce} trends are shown in Figure 11. The EoL (End-of-Life) is denoted as an increase of the forward voltage at load current by 5 %. Another failure criterion is an increase of 20 % of the thermal resistance. During all tests, all devices have reached the defined EoL due to the increase of the forward voltage. This failure mechanism is generally refered to a lift-off of the bondwires, while the degradation of solder layers mainly causes the increase of the thermal resistance. Also here a small voltage change after one device has reached its EoL is noticeable.

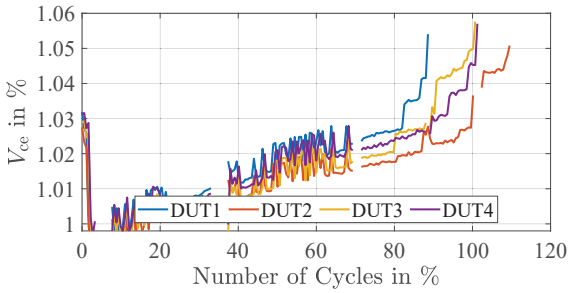
Figure 12 puts the results of all tests into perspective. The lifetimes are normalized to the mean lifetime of pattern **C** in realtime, not in cycles. The mean lifetime of pattern **A** was around factor 1.2 the lifetime of pattern **C**. The pattern B was about 0.8 times the lifetime of pattern **C**.
All devices of pattern **C** had lived longer than any device of pattern **B**. And this even with another lifetime relevant ripple (50 K) on top of the ripple of pattern **B** (72 K).
If a linear damage accumulation, in a way the rainflow-algorithm would count the ripples in pattern **C**, is assumed, a lower liftime would be expected. A simplified estimation of this expected lifetime ($L_{\mathrm{PC,expec.}}$) of pattern **C** is the inverse of the sum of the lifetimeconsumption of pattern **A** and **B**:

$$L_{\mathrm{PC,expec.}} = \left(0.5 \cdot \frac{1}{L_{\mathrm{PA}}} + \frac{1}{L_{\mathrm{PB}}}\right)^{-1} \approx 0.61 \cdot L_{\mathrm{PC}}\,. \tag{3}$$

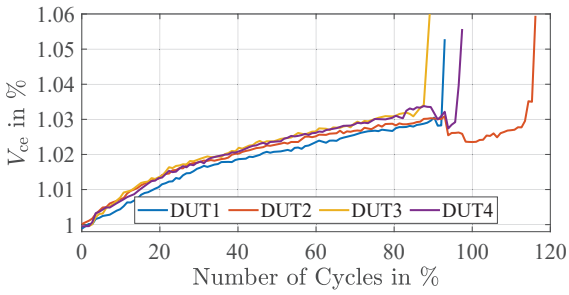
The factor 0.5 derives from the fact that $\Delta T_1 = 50\,\mathrm{K}$ only occurs half of the time in pattern **C**. The calculated value would be around factor 0.6 of the tested lifetime of pattern **C** L_{PC}, see also black stars in Fig. 12.



(a) Pattern **A**: V_{ce} trend of DUTs



(b) Pattern **B**: V_{ce} trend of DUTs



(c) DUT3

(d) Pattern **C**: V_{ce} trend of DUTs

Fig. 11: Measurement: V_{ce} trends of DUTs for pattern **A**, **B** & **C**

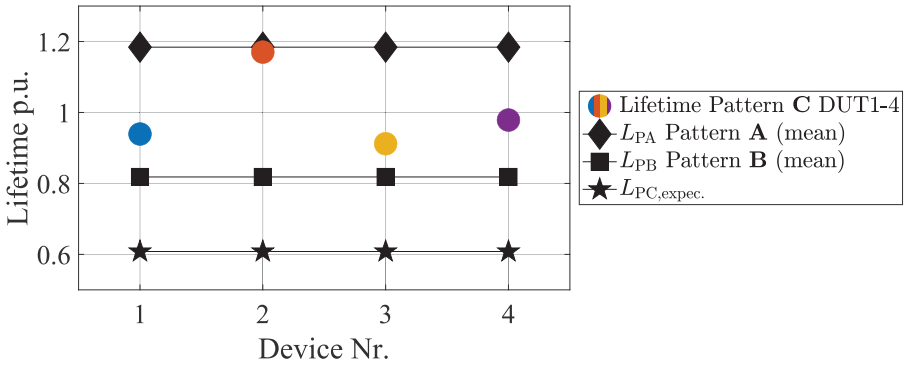
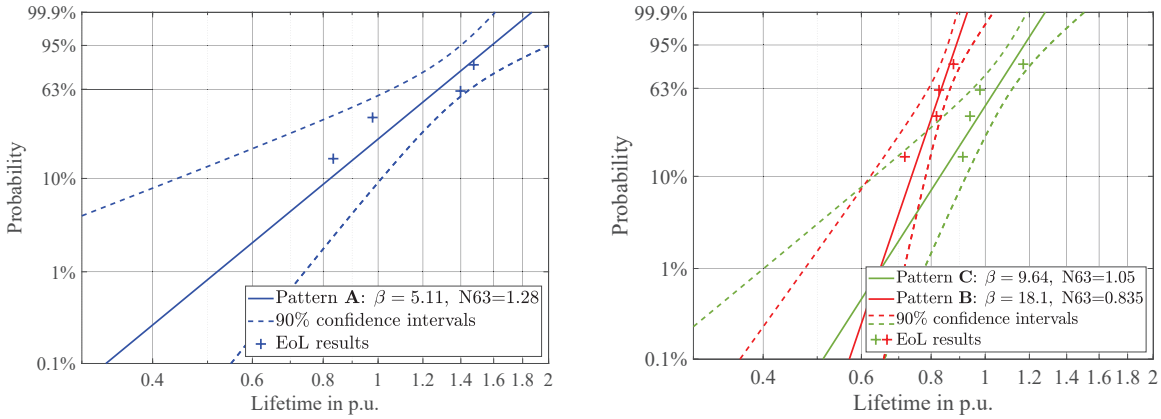


Fig. 12: Lifetimeresults of the different pattern, normalized to the mean Lifetime of pattern **C** in realtime (not cycles)

The results of the different patterns are also plotted in Weibull-Probability plots in Figure 13. Here the spread of the EoL-times for pattern **A** is clearly visible. This spread results in a relatively low β-factor, the slope in the probability plot. Hence also the range of the 90%-Confidence intervals is inflated in contrast to the other results.
For pattern **C** we see that all the EoL-Results are outside of the confidence intervals of pattern **B**, and this even with the additional temperature ripple of pattern **A**.

The final test bench is shown in Fig. 14. The left side is shown with the additional clamping circuits and necessary PCBs for the indirect leakage current measurement, while these PCBs are demounted on the right side to show the DUTs parts below.



(a) Weibull-Probability plot for pattern **A**

(b) Weibull-Probability plot for pattern **B** & **C**

Fig. 13: Weibull-Probability plots for pattern **A** and for pattern **B** & **C**

Conclusion

The presented powercycling test bench has been built up. First powercycling runs have been finished to validate the setup and the measurement systems. The actual measured patterns show a good match with the simulated target patterns.

Since all devices have failed due to bond-wire lift-off and not due to solder delamination, the analysis of the leakage current was unremarkable. To further evaluate the leakage current, different temperature patterns have to be used to address this failure mechanism specifically.

Of course, the results of these first runs must be taken with caution. Slight asymmetries in the switching inductances, especially after the exchange of one device influenced the results. Also the sample size is limited. Nevertheless, given the results the question arises if the linear damage accumulation for simultaneously occurring temperature ripples might be too conservative. Surely, a conservative design is always preferable to a risky variant, hence the results do not imply any risk to existing designs.

More investigations have to be done to further assess the error margin of the lifetime calculation with a state-of-the-art rainflow counting algorithm at mission-profiles with a valid number of superimposed temperature ripples. There might be a relevant lever to further reduce the semiconductor usage for these kind of applications. The presented test bench is capable of producing powercycling results to help answer this question more in detail.

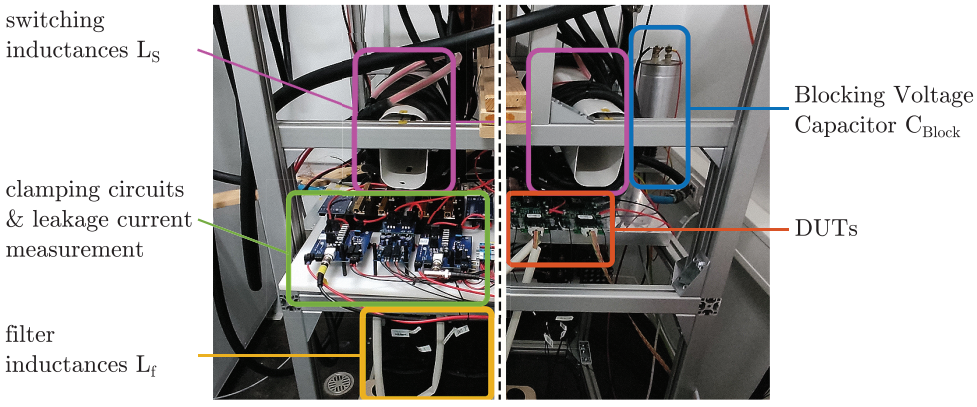


Fig. 14: Powercycling test bench, the image is split to show the uncovered DUTs

Acknowledgments

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