Design of A Second Harmonic Current Based High Step-down 48V-to-1V Resonant DC-DC Converter

Ziheng Liu[1], Jinyan Wang[1], Ju Gao[1], Jiayin He[1], Chengyu Huang[1], Xin Wang[1], Chen Wang[1], Bin Zhang[1], Yandong He[1] and Yong Xie[2]

[1] Peking University, Beijing, China

[2] Dongke Semiconductor (Auhui) Co., Ltd, Anhui, China

***Abstract*-- This paper presents an isolated DC-DC converter topology with a single ground-switch resonant inverter and a current driven rectifier. The inverter circuit oscillates the input voltage at a fundamental switching frequency and a series resonant tank is used to obtain the second harmonic current for power delivery. The circuit operates features constant current (CC) output, which means that the voltage gain never depends on the switching duty cycle. After the circuit's main waveforms are analyzed and the key parameters are optimized, a 5MHz prototype featuring 48V-to-1V transfer and up to 10A output current is verified by simulation with discrete ferrite transformer and GaN power switches.**

***Index Terms*—DC-DC Converter, Second Harmonic Current, 48V-to-1V, Resonant**

I. Introduction

High power density switch-mode power electronics are more and more demanded in modern industry. As the increasing of switching frequency, the switching loss occurs in the power switch will become larger due to the overlap of the drain-voltage and the drain-current waveforms. Single ground-switch resonant converter (SGSR) circuits have been proved to be able to operate efficiently at MHz level of switching frequency, such as Class-E topology [1] and Class-Φ_2 topology [2] (Class-Φ_2 circuits feature lower switching voltage stress than Class-E circuits). In these previous cases, the ground-connected power switch can achieve zero voltage switching (ZVS) during turning on/off state and thus the theorical switching loss becomes zero. Among the state-of-the-art switching topologies, although the buck type SGSR delivers power through the switching frequency resonant voltage/current, the voltage gain of this converter is always limited by the frequency response of the output resonator in the inverter stage [3] [4].

In a typical power distribution system as shown in Fig. 1(a), a number of low voltage microprocessors are supported with a 48V bus voltage, showing I^2R times lower power consumption than the solutions with intermediate voltage bus. To achieve a voltage step-down ratio as high as 48:1 with a low turn-ratio transformer, a second harmonic current based isolated SGSR circuits is proposed in this paper. Constant output second harmonic AC current is achieved at wide load range so that the load current is able to be linearly adjusted. The operating principle of the inverter and rectifier are introduced, the effect of the input resistance of the rectifier stage to the drain-to-source voltage (V_{DS}) waveform of the inverter stage is also analyzed. Finally, a 5MHz prototype with 48V input and 1V/1~10A output is built. Ferrite transformer and GaN power devices are used in simulation for verifying the proposed design procedure.

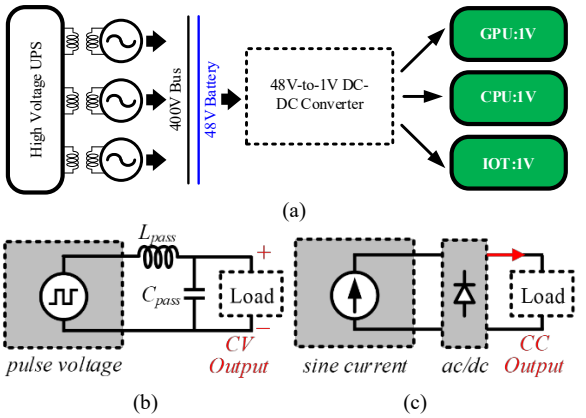


Fig. 1. (a) System architecture of data center's power supply. (GPU: Graphics Processing Unit; CPU: Central Processing Unit; IoT: Internets of Things) High step-down converter circuit diagrams with (b) CV output and (c) CC output.

This paper is organized as follows; Section II discusses and compares the design considerations of high step-down 48V-to-1Vconverter with constant voltage (CV) output topology and CC output topologies; Section III analyzes the operating principals and design equations of the proposed second harmonic current based SGSR circuit; Section IV shows the simulation results of the prototype; Section V concludes the paper.

II. High Step-Down Converter with CV or CC Output Topologies

A. Overview of 48V-to-1V Converter with CV Topology

High step-down converter with CV output includes switch-inductor circuit family, switch-capacitor-inductor family and bridge-transformer family.

1. The traditional buck converter is a typical switch-inductor circuit, the switching duty cycle should be designed as short as 1/48 to realize 48V-to-1V conversion, which strongly challenges the operating performance of the gate driver, especially

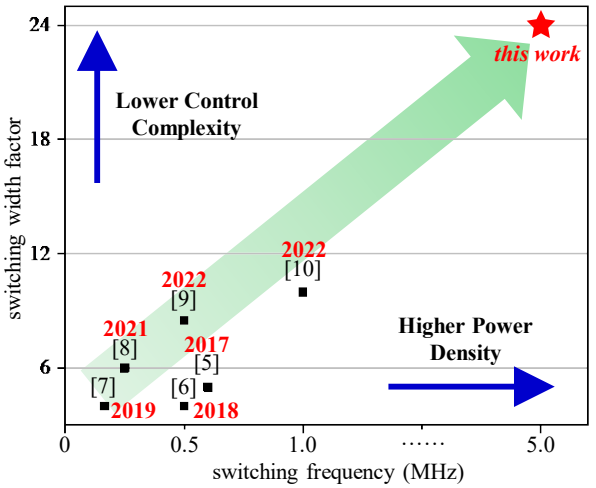


Fig. 2. Performance figure of recently typical designs of the directly 48V-to-1V DC-DC converter.

at high switching frequency. In addition to the duty cycle issue, the buck converter has poor light load efficiency due to hard switching.

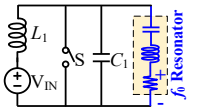
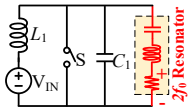
2. Switch-capacitor-inductor circuits (or call the hybrid circuits) introduce flying capacitors into the switch-inductor circuits, the voltage across the flying capacitors could be balanced to be stable level. The voltage conversion ratio is designed as positive function of the number of flying capacitors, indicating that high conversion ratio operation requires large number of power switch.
3. Bridge-transformer circuits, like LLC and Sigma topologies, comprising active inverter bridge, active rectifier bridge and high turn-ratio transformer. High conversion voltage ratio is obtained using high turn-ratio transformer; however, large leakage inductance limits the output power and operating frequency of the converter. In addition, active inverter and rectifier stages requires many independent power switches.

Based on the above three types of CV topologies, some applications of 48V-to-1V conversion have been designed and verified. Fig. 2 summarizes some of recent (2017 to 2022) reported board-level 48V-to-1V DC-DC converter, featuring different switching frequency and switching duty cycle. The switching width factor is defined to be a characteristic parameter related to the voltage gain and switching duty cycle of any a specific converter topology, expressed as follows:

$$\text{switching width factor} = D \Big/ \left(\frac{V_{OUT}}{V_{IN}} \right), \qquad (1)$$

where D refers to the switching duty cycle. It's noted that Fig. 2 shows that the switching width factor of any one previous design is lower than 12 (switching width factor = 24 means duty cycle = 50%), indicating that the duty cycle is lower than 0.25. For the same voltage conversion application, higher switching width factor results in lower complexity of controller circuit, benefiting higher switching frequency operation and better compatibility of classical fabrication process. As shown in Fig. 1(b), CV circuit inverts the input voltage into pulse waveform through the single/multi-level or single/multi-stage power switch networks. The passive elements L_{pass} and C_{pass} serve as low-pass filter, transferring the dc component of the pulse voltage to the load. Thus, the voltage gain and output power are determined with switching duty cycle.

TABLE I
PROPERTIES COMPARISONS OF CLASS-E AND CLASS-Φ_2 INVERTERS

Topology	Class-E	Class-Φ_2
Circuit Diagram*		
ZVS	Yes [1] [4]	Yes [2] [3]
Voltage stress of S as duty cycle is 0.5	4~6V_{IN}	**2~3V_{IN} (Suitable in high voltage application)**
How CV	Realized with voltage gain of about 1.59V_{IN} [4] [11]	Yes (Realized with voltage gain of about 1V_{IN} as duty cycle is 0.3 [11])
How CC	Realized by adding *LCL* compensation network to f_0 resonator [12] [13]	**None report**

* f_0 refers to the switching frequency of main switch S.

B. Proposed CC Topology

By avoiding the influence of the switching duty cycle on the converter's conversion performance, the switching width factor can be improved. A possible solution to this issue is to replace the pulse voltage source with a duty cycle-independent sine current source, as show in Fig. 1(c). It's has been reported that the Class-E and Class-Φ_2 inverters are able to achieve load-independent CV output performance, using finite or infinite input inductor, but the amplitude of the output voltage of the reported inverters are nearly 1.6V_{IN} and are unsuitable in high step-down applications. Table I lists some of the focused main properties of the Class-E and Class-Φ_2 inverters. Both of them only contain one power switch, operating under ZVS without any external control within load range of [0Ω, R_{opm}]. One of the important differences is that, Class-Φ_2 circuit only suffers 2~3V_{IN} on the main switch S, nearly 2 times lower than that of Class-E circuit, which makes Class-Φ_2 circuit more suitable for high voltage applications.

Load-independent CV output can be achieved in Class-E and Class-Φ_2 inverters by properly setting the resonant frequency and characteristic impedance of pairs "L_1-C_1" and "f_0/$2f_0$ resonator" [4] [11]. However, the voltage gains of 1~1.59 limits the topologies to be adopted in high conversion ratio power supply systems. Except of CV, CC

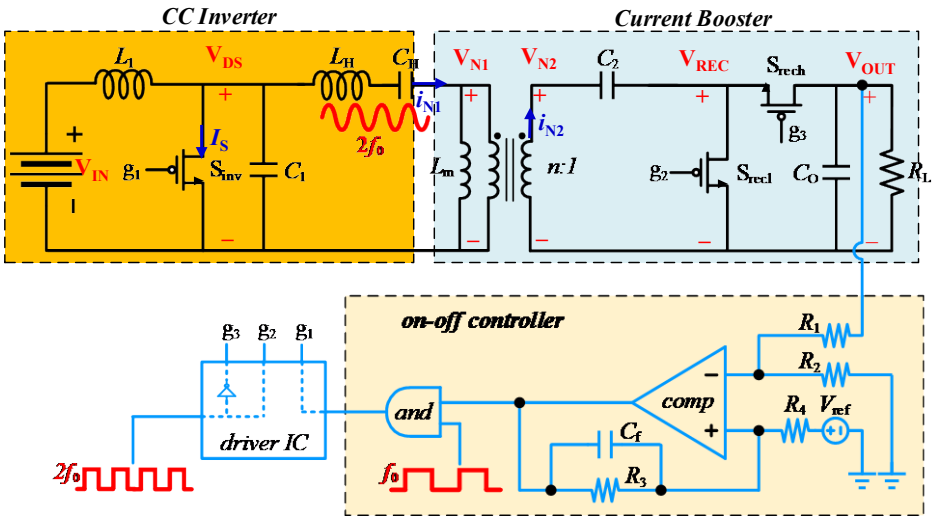


Fig. 3. Schematic of the proposed second harmonic current based 48V-to-1V step-down converter, including the power stage and the controller stage. (The power switches S_{inv}, S_{recl} and S_{rech} should be several parallel-connected devices at high output current applications.)

is another choice, it benefits safely battery charge and can merely be obtained with bridge-transformer circuits and SGSR circuits [14]. For Class-E circuit, the CC output is realized by adding a *LCL* compensation network in front of the load resistor, transferring the CV source to CC source.

As far as the authors know, there is little report about the CC realization in Class-Φ_2 converters. Actually, the Class-Φ_2 circuit itself can serve as a CC source of $2f_0$, the property can be maintained within a load range of [0Ω, R_{opm}]. In this study, as shown in Table I, the load resistor is considered as a part of the $2f_0$ resonator, then the second harmonic current is used to convert the power. Consequently, the converter always achieves CC output with switching width factor = 24 (D = 0.5), suffering lower voltage stress than Class-E CC converter on the main power switch.

III. Circuit Analysis and Parameter Design

Fig. 3 presents the circuit schematic of the proposed converter, including the power stage and the controller stage. The power stage consists of an inverter stage (including V_{IN}, power switch S_{inv}, L_1, C_1, L_H and C_H) and a rectifier stage (including a transformer, C_2, power switch S_{rec1}, S_{rec2}, C_O and R_L). A hysteresis on-off controller [2] [3] is adopted to form close-loop operation, so that the converter maintains CV as the V_{IN} value varying. Fig. 4 shows the key waveforms of the proposed circuit. For simplify, the following assumptions are adopted in the following analysis:

1. All the passive elements are ideal and could be descripted with linear equation.
2. The power switches are seen as ideal switch without conductance resistance and turning on/off delay.

A. Single Ground-Switch Resonant Inverter

The circuit diagram of the inverter stage circuit is shown

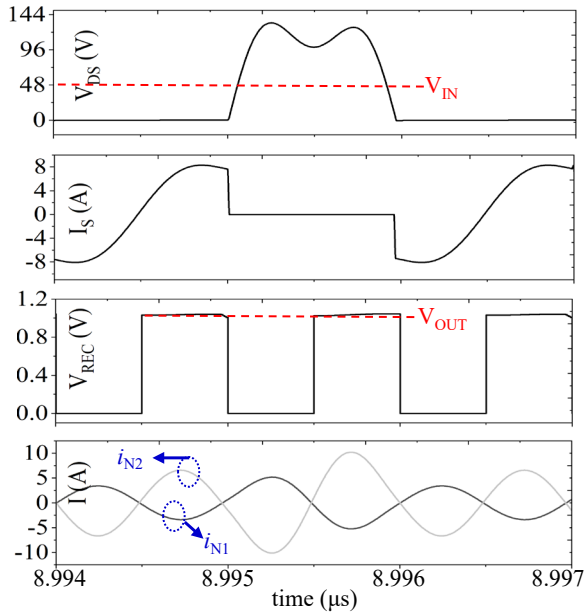
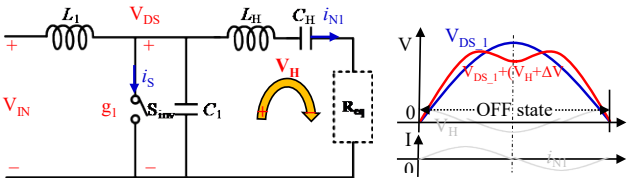


Fig. 4. Key waveforms of the proposed second harmonic current based high step-down DC-DC converter.

in Fig. 5(a), L_1 and C_1 serve as fundamental network that shaping the V_{DS} to near half-sine waveform with a frequency of switching frequency f_0. The L_H, C_H and R_{eq} forms a series connected resonant network resonating at $2f_0$, where R_{eq} is the input resistance of the rectifier stage.

The V_{DS} voltage in Fig. 3(a) is treated as a combination of $V_{DS\_1}+V_H+\Delta V$, where the V_{DS_1} is the switching frequency voltage on the drain of power switch that is generated by L_1 and C_1, V_H is the 2nd harmonic voltage shorted by the L_H and C_H branch, ΔV is the 3rd and 4th voltage components generated by the nonlinearity of the switching transients. The expressions of V_{DS_1} could be derived as follows:

$$L_1C_1\frac{dV_{DS\_1}^2}{dt^2}+V_{DS\_1}=V_{IN},V_{DS\_1}\big|_{t=0}=0$$
$$\frac{1}{2\pi}\int_0^{\pi}V_{DS\_1}d\varphi=V_{IN} \quad (1)$$



(a) (b)

Fig. 5. (a) Circuit diagram of the ground-switch resonant inverter stage. (b) Theoretical schematic of the voltage combination analysis.

$$\begin{cases} V_{DS\_1} = V_{IN}\left[\dfrac{\lambda_1\pi+\sin(\pi\lambda_1)}{1-\cos(\pi\lambda_1)}\sin(2\pi f_0\lambda_1 t)\right. \\ \qquad\qquad \left. -\cos(2\pi f_0\lambda_1 t)+1\right] \\ \lambda_1 = 1/2\pi f_0\sqrt{L_1C_1} \end{cases} \tag{2}$$

where the f_0 is the switching frequency. To generate the second harmonic current i_{N1} but do not short all second harmonic drain-source voltage component, the L_H and C_H should resonant at a bit larger at $2f_0$. Then the V_H is derived as follows:

$$i_{N1} = I_0\sin(2\pi f_0 t) \tag{3}$$

$$\frac{1}{2\pi\sqrt{L_HC_H}} = 2kf_0 \quad (1<k<1.1) \tag{4}$$

$$V_H = I_0\left(4\pi f_0L_H - 1/(4\pi f_0C_H)\right)\cos(2\pi f_0 t) \tag{5}$$

where the I_0 is a constant value related to the characteristic impedance of the L_H-C_H-R_{eq} branch. It's noted that the parameter k is nearly equal to 1 according to the traditional Class-Φ_2 design equations. The voltage across the input inductor L_1 should be zero in one switching period, so the average value of (V_H+ΔV) is zero. As shown in Fig. 5(b), a near-trapezoidal V_{DS} waveform is obtained by combining the V_{DS_1} and V_H, ΔV. The values of L_H and C_H determines the output current of the inverter and should be tuned together with rectifier stage. In (2), the power switch can exactly operate with ZVS if the value of λ_1 equals to around 1.29 [1], then the values of C_1 and L_1 can be selected by considering the L_H-C_H pair as one L_{eq} that is series-connected to L_1 and one C_{eq} that is parallel-connected to C_1, as follows:

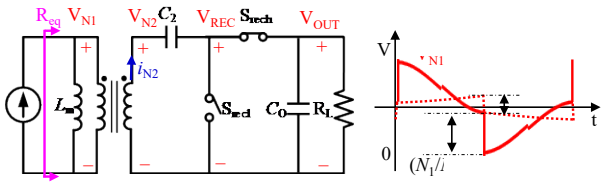
$$Z_{L_H-C_H} = j\omega_0L_H + \frac{1}{j\omega_0C_H} = j\omega_0L_{eq} = \frac{1}{j\omega_0C_{eq}} \tag{6}$$

$$L_{eq} = \left(1/(2\omega_0)^2 L_HC_H - 1\right)\Big/\left((2\omega_0)^2 C_H\right) \tag{7}$$

$$C_{eq} = C_H\Big/\left(1-1/(\omega_0)^2 L_HC_H\right) \tag{8}$$

$$1/2\pi\sqrt{(L_1+mL_{eq})(C_1+|C_{eq}|)} = 1.29f_0 \quad (where\ \omega_0 = 2\pi f_0, m>0) \tag{9}$$

In practical design, the parameter m is tuned to obtain ZVS and the value of m is often close to 1.



(a) (b)

Fig. 6 (a) Schematic of the current boosting rectifier, theorical waveforms of (b) V_{N1} and V_{N2}.

B. Current Boosting Rectifier

Fig. 6(a) shows the schematic of the isolated current boosting rectifier, where the turn ratio of the transformer is N_1:N_2. C_2 is a DC block capacitor, and the synchronous switches S_{recl}, S_{rech} turn on/off with a duty cycle of 50%, acting as a half-wave rectifier. In comparison with the diode rectifier, the MOSFET based synchronous rectifier avoids power loss caused by forward voltage during turning on of the diode. For very high output current design, additional series of power switches should be paralleled to S_{recl} and S_{rech}. The L_H-C_H pair in the inverter stage generates the input current and the rectifier deliveries a boosted current to the load. Fig. 6(b) give the theorical voltage waveforms.

The output voltage V_{OUT} and power P_{OUT}, as well as input resistance R_{eq} are given as follows:

$$\begin{aligned} i_{N2} &= -\frac{N_1}{N_2}i_{N1} = -I_{N2}\sin(4\pi f_0 t) \\ V_{OUT} &= \frac{I_{N2}}{\sqrt{2}}R_L, P_{OUT} = \frac{V_{OUT}^2}{R_L}, R_{eq} = \frac{2N_2^2}{\pi^2N_1^2}R_L \end{aligned} \tag{10}$$

According to (10), by carefully selecting N_1, N_2 and R_L, various output power is achieved at the same V_{OUT}. It's noted from Fig. 4 that the V_{REC} is square wave with a voltage swing of V_{OUT}, therefore, power devices with high current density but low rated voltage should be selected to realize a low output level application, such as 48V-to-1V. Because of the low V_{REC} swing, a ground-connected gate driver can directly drive the S_{rech} in the practical design.

It's obtained from (10) that the change of R_{eq} will be (N_1/N_2) times that of V_{OUT} with the turn ratio increasing, meaning that a larger R_{eq} is required to maintain a stable V_{OUT}. Thus, it's essential to analyze the inverter's performances at different R_{eq}. As shown in Fig. 7(a), the max voltage stress of V_{DS} increases with R_{eq} and exceeds $3V_{IN}$ at turn ratio of 16:1. However, Fig. 7(b) shows that the resonant current i_{N1} do not change with R_{eq}, indicating that the inverter works as a constant second harmonic current source.

IV. Prototype Verification

To verify the design procedure of the proposed high step-down SGSR, a 5MHz, 48V-to-1V prototype is built and simulated with commercial devices' spice models. A 200V rated GaN power device EPC2215 is selected as S_{inv}, while a pair of half-bridge power devices EPC2111Q1 and EPC2111Q2 are used as S_{recl} and S_{rech} respectively. The

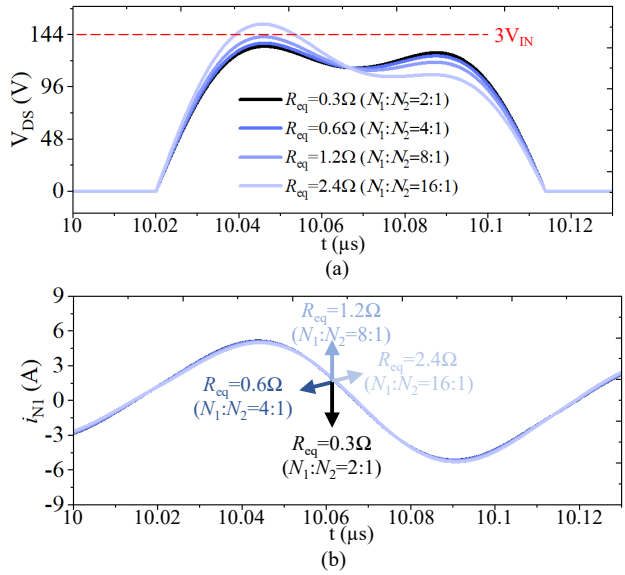


Fig. 7 (a) V_{DS} waveforms and (b) i_{N1} waveforms at different R_{eq} (different turn ratios), V_{IN}=48V and V_{OUT}=1V. The switching duty cycle is set as 0.5 for simulation.

TABLE II
SPECIFICATIONS OF CIRCUIT PARAMETERS USED IN PROTOTYPE

Circuit Parameters	Specifications
V_{IN}/V_{OUT}	48V/1V
I_{OUT}	2~10A
f_0 (S_{inv}/S_{recl}, S_{rech})	5MHz/10MHz
L_1, C_1	300nH, 470pF (m=1)
L_H, C_H	900nH, 250pF (k=1.06)
C_2	1μF
C_O	100μF
D	0.5

specifications of the circuit parameters used in the prototype are shown in Table II.

As observed in Fig. 8(a), the prototype under close-loop control perfectly achieves 1V output within 0.6ms, with a nominal voltage ripple of <20mV. The ripple decreases with larger output power. Thus, it's suitable for the proposed SGSR circuit to be applicated in special low-voltage modules.

Furthermore, the dynamic load performance is also demonstrated as presented in Fig. 8(b). Through on-off control clamps the average of the V_{OUT} by adjusting the V_{ref} (shown in Fig. 3), it is possible for the real load falls and the original V_{ref} drops to lower value. The V_{OUT} maintains 1V under on-off control, decreases at lighter load and rises back to 1V with 0.2ms. Fig. 9 shows the simulated conversion efficiency of the proposed 48V-to-1V converter under different transformer's turn ratios, it's seen from the data that the efficiency maintains over 80% as operating at wide output power.

V. CONCLUSIONS

This paper proposed a second harmonic current based high conversion ratio isolated step-down SRSG converter, featuring CC output operation and low voltage stress for power switch. The circuit parameters' selections and operation principle are discussed in detail using frequency-domain equations. To verify the proposed design procedure, a 5MHz, 48V-to-1V prototype is built with real spice models of GaN devices and ferrite transformer, 94% efficiency is achieved at 10A output. Therefore, the proposed SGSR is suitable for operating in MHz switching frequency and high output power applications.

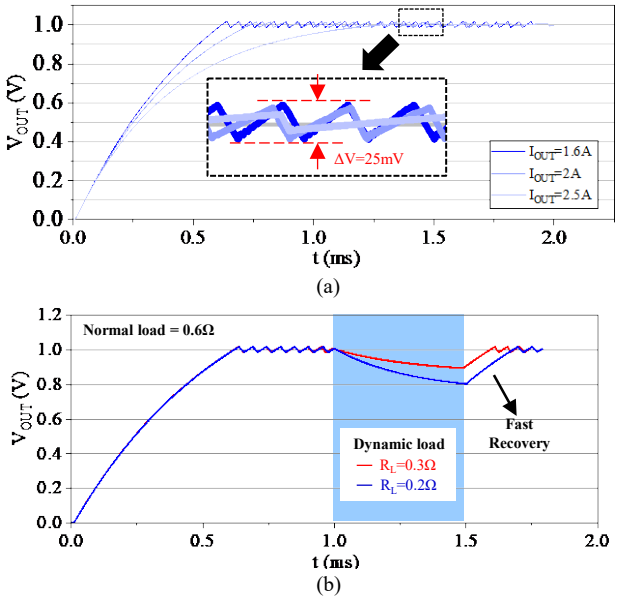


Fig. 8 (a) Output ripple of the V_{OUT} waveform. (b) Load variation implementation for the proposed prototype, presenting the V_{OUT} waveforms at loads of 0.6Ω (Nominal Load) and 0.3/0.2Ω (Lighter Load).

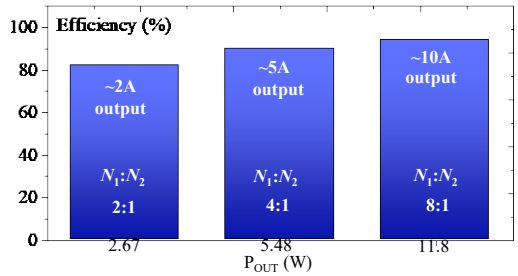


Fig. 9. Simulated conversion efficiency under different turn ratios.

ACKNOWLEDGMENT

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