Desaturated turn-off of low-saturation IGBTs with clamping method to reduce turn-off energy losses

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Keywords

«IGBT», «Smart Gate Drivers», «Driver Concepts», «Switching Devices»

Abstract

Investigations into the desaturated turn-off of low-saturation IGBTs with a novel hardware-based clamping approach are presented in this paper. Effects of the clamping voltage level and duration of desaturation on the reduction in turn-off energy losses are investigated. Turn-off measurement results with experimental low-saturation IGBT chips with the implemented clamping method demonstrate significant reduction in turn-off losses relative to the intrinsic turn-off of the device. Furthermore, TCAD based turn-off simulations with the clamping approach applied to different IGBT device models are presented with the objective of determining the potential of this method in reducing turn-off losses, as well as to obtain an insight into the necessary device on-state carrier concentration profile to obtain large reductions in turn-off energy losses for the advantageous application of this turn-off method.

Introduction

The Insulated Gate Bipolar Transistor (IGBT) finds itself in an increasingly large number of applications, such as in wind energy converters, VSC-HVDC applications, medium voltage drives among others. The rapid move towards green energy and energy efficient applications has propelled it to the status of being an indispensable device in medium to high voltage applications. With the goal of increasing the efficiency and decreasing the size of converters, recent research has focused on increasing the carrier concentration inside the device in an effort to reduce the on-state forward conduction voltage drop ($V_{CE,sat}$) [1] and thereby the conduction losses in the device. This is accomplished by increasing the front-end emitter-sided plasma concentration in the device during conduction by increasing the emitter efficiency [2]. Several methods have been proposed in literature and implemented in practice to increase the carrier concentration in the front-end emitter side of the device. The 'Injection-Enhancement effect' to increase the electron injection by suppressing the flow of hole current at the emitter side by reducing the trench-trench distance, also known as the mesa-width, was proposed in [3], which led to the device known as the IEGT. A further reduction of the mesa to sub-micron levels towards attaining the 'Silicon limit' for IGBTs was proposed in [4]. A n-doped layer below the p-base of the device between the trenches, which led to the device CSTBT, has been proposed [5] to further limit the hole current and lead to enhanced electron current in the MOS region. Recently, an attempt to further reduce the $V_{CE,sat}$ with carrier confinement and increased channel width has led to the MPT-IGBT concept with wide channels and low mesa-widths [6][7].

The result of increasing the front-end emitter sided-hence the device carrier concentration is a decreased $V_{CE,sat}$ but has the consequence of increased amount of carriers to be extracted from the device during turn-off, which could lead to higher turn-off energy losses necessitating more sophisticated turn-off methods. A desaturated turn-off of trench-fieldstop IGBTs was first shown to reduce the turn-off energy losses by about 17% in such devices

[8]. It has been further shown [9] through simulations, that such desaturated switching is especially beneficial in low-saturation IGBTs with increased front-end emitter sided carrier concentration compared to conventional IGBTs, which feature a higher back-end emitter sided plasma concentration.

Recently, turn-off measurements have been performed on a low-saturation 3.3kV IGBT chip [10] with a feed-forward based desaturation pulse based on the methodology introduced in [9]. This approach showed an optimistic 21% reduction in E_{OFF} compared to normal turn-off. However, investigations also revealed that the purely feed-forward-based approach also suffers from significant disadvantages in practical implementation. The outcome, it has been shown, is highly sensitive to control parameters such as the switching instants and also to the current carried by IGBT when it is switched off. It was also shown through TCAD simulations that a clamping-based approach to desaturated turn-off could potentially result in large reduction in turn-off energy losses and inherently being a feedback-based method, also helps avoid the disadvantages associated with the feed-forward-based approach.

The implementation of this method would require a sophisticated intelligent driver to time the activation of the clamping circuit based on feedback signals proportional to the collector to emitter voltage V_{CE} during turn-off. There has been a recent trend in research towards customized drivers equipped with fast FPGAs or microcontrollers to achieve particular objectives during device switching, for instance, to implement a gate voltage behavior-based distinction during turn-off of a reverse conducting IGBT [11] and in the implementation of a sophisticated turn-off of SiC mosfets [12]. Although not standard at the moment, it could be expected that application-specific drivers would eventually find commercial applications.

In the work presented in this paper, a previously implemented FPGA-based gate driver [10] is now supplemented with an additional active clamping circuit, the switching of which is also controlled by the FPGA as required to include the collector-gate clamping action during turn-off to implement the desaturation pulse. Scaled single chip turn-off measurement results with the desaturation pulse are presented with two different experimental low-saturation 3.3kV class IGBT chips to show the advantageous application of this method in terms of reduction of $E_{OFF.}$ Investigations to the effect of desaturation voltage level and duration on the reduction of E_{OFF} are presented. TCAD simulation results with different low-sat IGBT models are presented to obtain certain qualitative insight into the required device on-state plasma profile to gain maximum benefit from this turn-off method in terms of reduced E_{OFF}.

Collector-gate clamping based desaturation pulse – driver implementation and control

The relevant functional sections of the FPGA-based high voltage gate driver used to implement the collector-gate clamping (CG-Clamping) desaturation pulse are shown in Fig. 1. The push-pull actuator stage of the driver comprises of three different turn-off mosfet-$R_{G,off}$ combinations to enable the tuning of the turn-off dynamic during the initial fast intrinsic turn-off phase, the desaturation pulse phase and the final commutation phase. The logic signals required to switch these actuator mosfets are provided by the FPGA, which is programmed with a state machine algorithm to implement the turn-off method. This figure also shows the active clamping circuit used to implement the desaturation pulse. This circuit comprises of a TVS diode and a high voltage mosfet. The breakdown voltage of the TVS diode determines the clamping voltage level between the collector and gate and therefore between the collector and emitter ($V_{CE,clamp}$).

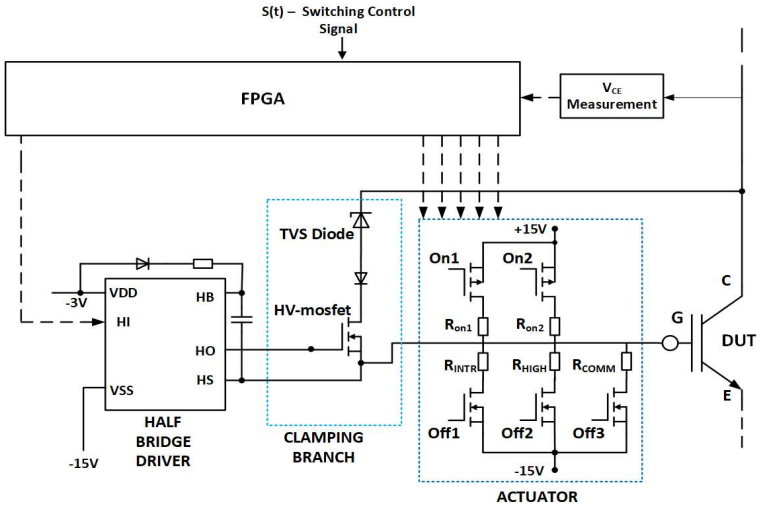

Fig. 1: Schematic representation of the FPGA-based HV gate driver with active clamping circuit

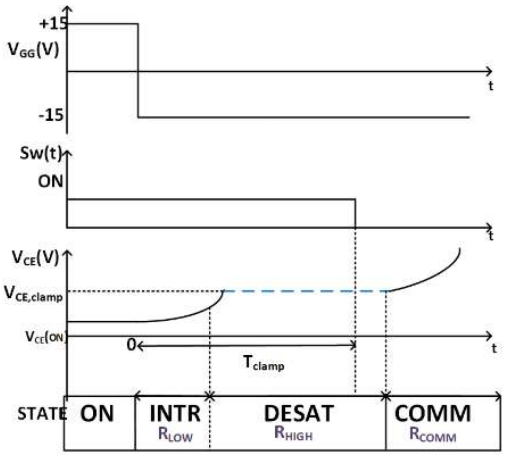

Fig. 2: Switching control diagram to implement the collector-gate clamping desaturation pulse-based turn-off

The high voltage mosfet, rated to block the full rated voltage of the DUT IGBT, is switched by the half bridge driver IC. The switching of this mosfet determines the clamping duration (t_{clamp}) during the desaturation pulse phase of the turn-off.

The control timing diagram to implement the desaturation pulse is shown in Fig. 2. The clamping HV- mosfet is turned-on (shown as Sw(t)) a few micro seconds after the turn-on of the DUT-IGBT. Following the turn-off signal at t=0, the IGBT turn-off initially progresses intrinsically with a turn-off gate resistance of R_{LOW} until shortly before the clamping voltage is attained. At this point, the gate is switched to a high resistance R_{HIGH} as the clamping action begins, to limit the current through the clamping circuit. The clamping action continues until the clamping mosfet is turned-off. The gate is now switched to R_{COMM} to lead to the completion of the turn-off process. The switching of the clamping mosfet is carried out in a feedforward manner by programming the FPGA.

Measurement Results with the Collector-gate clamping desaturation pulse-based turn-off

Turn-off measurement results with the desaturation pulse, performed on experimental low-saturation IGBT chips, are presented in this section. These experimental devices have a rated blocking voltage of 3.3kV and a nominal current ($I_{C,nom}$) of 106A. The stray inductance in the commutation circuit is scaled to correspond to the stray inductance seen in comparable IGBTs in an XHP module package. Normal turn-off is carried out with a turn-off resistance of 26Ω for $R_{G,COMM}$. For the implementation of the desaturation pulse, a R_{HIGH} of 5kΩ is used, and R_{COMM} of 23Ω is used during the final commutation phase of the turn-off.

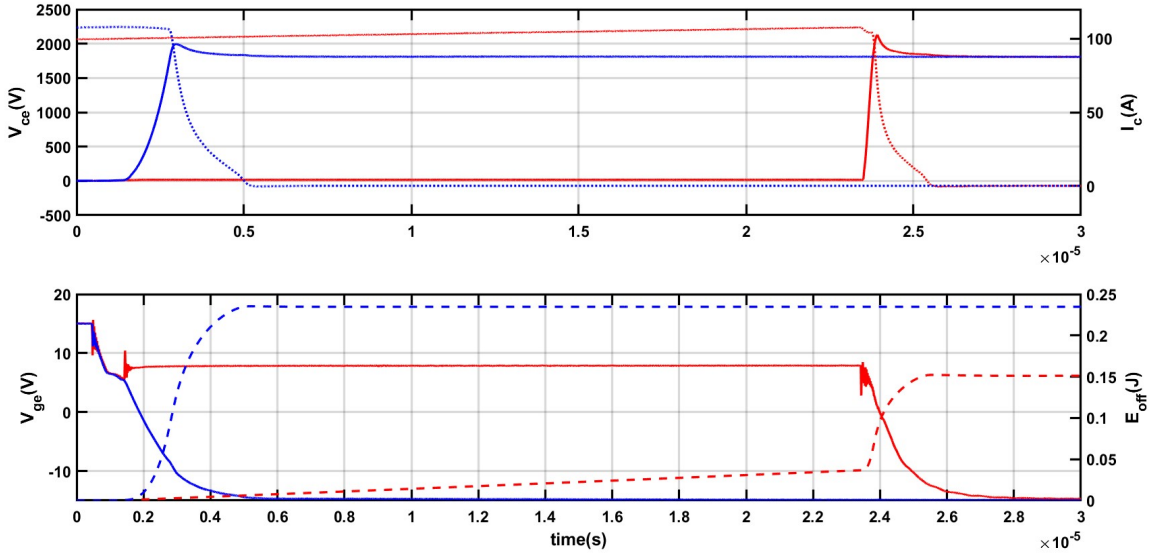

Fig. 3: Turn-off measurements for IGBT type W1
Top: V_{CE} and $I_{C,}$ bottom V_{GE} and E_{OFF}
Legend: Blue→ Normal Turn-off ($R_{G,off}$ = 25Ω), Red→ Desat pulse-based turn-off (5V TVS diode)

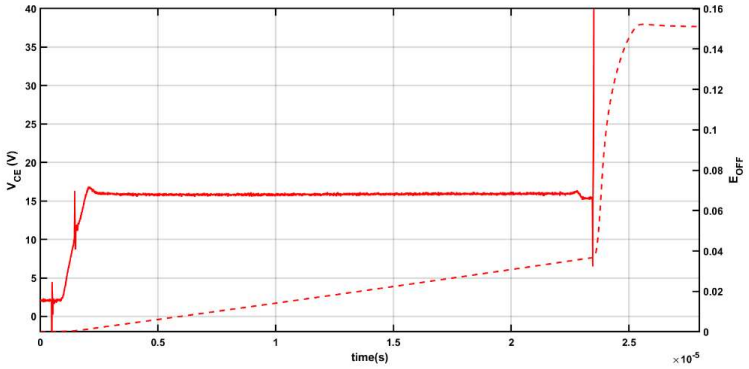

Fig. 4: V_{CE} during desaturation pulse corresponding to Fig. 3

Fig. 3 shows the comparison between normal and desaturation pulse-based turn-off measurements for one of the experimental low-saturation IGBT devices (W1), which has a $V_{CE,sat}$ of 1.75V at $I_{C,nom}$ and 125°C. Normal turn-off (shown in blue) results in a E_{OFF} of 0.237J. Desaturation pulse-based turn-off with a 5V TVS diode to set the CG-clamping voltage level, as described earlier, results in a E_{OFF} of 0.15J for a clamping duration (t_{clamp}) of 22µs, which is a significant reduction of 37% compared to the normal turn-off case. The clamped V_{CE} during the turn-off is shown magnified in Fig. 4. The V_{CE} remains more or less constant during the desaturation pulse. This indicates the adequacy of the driver implementation applied to drive the clamping mosfet.

Additional desaturation pulse-based turn-off measurements are performed on this IGBT chip to determine the optimal combination of collector-emitter clamping voltage $V_{CE,clamp}$ and duration t_{clamp} to obtain the minimum value for E_{OFF}. Fig. 5 shows the summary of these measurements. Here, the E_{OFF} normalized with respect to the intrinsic E_{OFF}, are plotted for different values of t_{clamp} and $V_{CE,clamp}$. A noticeable aspect from these results is that the E_{OFF} attains a local minimum for each value of clamped voltage and then starts increasing again. For this IGBT chip, it can be seen that a $V_{CE,clamp}$ of 16V and t_{clamp} of 22µs leads to the best outcome regarding reduction of E_{OFF}. It is to be noted that the turn-off energy losses during the turn-off with the desaturation pulse comprise of the additional on-state losses during the desaturation pulse E_{clamp} and the energy losses during final commutation E_{comm}. To further investigate the effect of the parameters $V_{CE,clamp}$ and t_{clamp}, the normalized E_{clamp} and E_{comm} corresponding to the turn-off measurement summary of Fig. 5 are shown in Fig. 6a and Fig. 6b respectively. It is seen from Fig. 6a that the E_{comm} decreases faster with respect to t_{clamp} at higher values of $V_{CE,clamp}$. It is also seen that the E_{comm} initially decreases rapidly with respect to t_{clamp} and rather sluggishly later. From Fig. 6b, it is immediately discernible that the losses during the desaturation pulse, E_{clamp} increases rather linearly with respect to t_{clamp} as expected, and is proportional to the $V_{CE,clamp}$. Therefore, although the E_{comm} decreases rapidly at larger values of $V_{CE,clamp}$, higher clamping voltages do not present an advantage because of the much larger amount of additional losses incurred in the device during the desaturation pulse phase of the turn-off due to larger on-state voltage across the device. It is noted from Fig. 6a however, that the normalized commutation losses for the chip W1 could potentially be decreased to 38% compared to the value 100% without the desaturation pulse, but at larger clamping voltages.

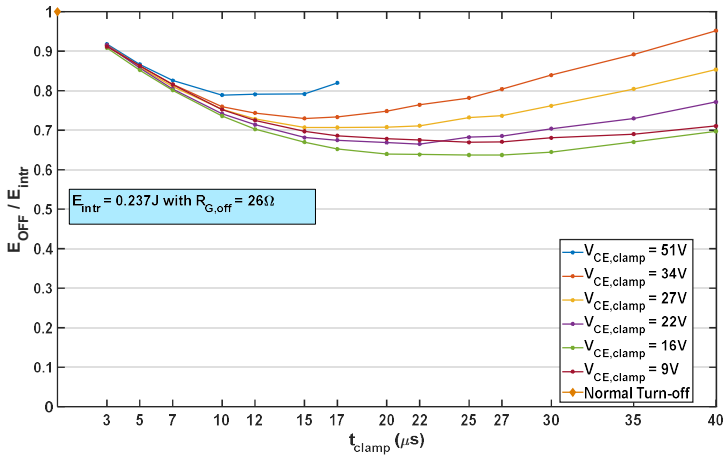

Fig. 5: Summary of Turn-off Measurements with desaturation pulse for low-sat IGBT chip W1

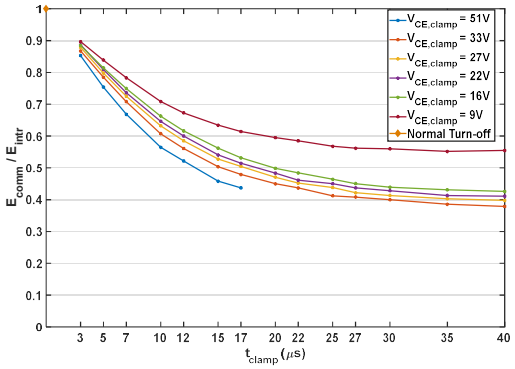

Fig. 6a: Normalized E_{comm} for W1

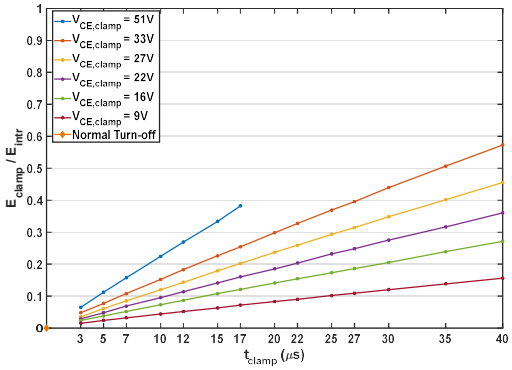

Fig. 6b: Normalized E_{clamp} for W1

Turn-off measurements have also been performed on a different experimental low-sat IGBT chip (W2), which has a $V_{CE,sat}$ of 2.4V at $I_{C,nom}$ and 125°C. This chip is known to have a much lower front-end emitter sided plasma concentration compared to chip W1. A summary of these measurements is shown in Fig. 7a. For this chip, it is seen that a lower $V_{CE,clamp}$ of 12V with a t_{clamp} of 22µs yields a maximum reduction of about 27% in E_{OFF}. The plot of normalized commutation losses corresponding to these measurements is shown if Fig. 7b. It is seen from these results that for comparable values of $V_{CE,clamp}$ and t_{clamp}, the chip W2 shows a smaller reduction in E_{OFF} and also in E_{comm} compared to the chip W1. A larger amount of carrier concentration in chip W1 in the on-state implies that not only the E_{OFF} is higher for this chip but also the potential to reduce the E_{OFF} due to removal of a larger amount of carriers during the desaturation pulse, which is an advantage for chip W1.

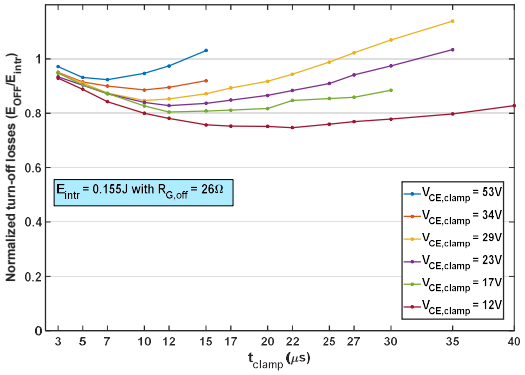

Fig. 7a: Normalized E_{OFF} for chip W2

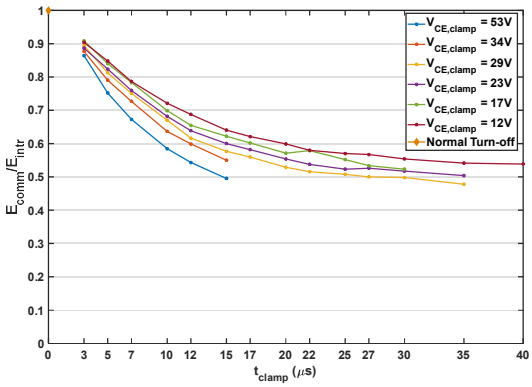

Fig. 7b: Normalized E_{comm} for chip W2

An advantageous application of this turn-off method requires a good performance at collector current values other than the nominal current. Turn-off measurements have been performed for the optimal combination of $V_{CE,clamp}$ and t_{clamp} determined for the nominal current case. Table I shows these results for chip W1. It can be seen that for a range of currents between 20% and 150% of the nominal current, this turn-off method yields a consistent reduction in E_{OFF} similar to the reduction seen in case of the nominal current. This table also shows a small but rather insignificant variation in V_{CE} as a function of the current through the device. This is in contrast to the large dependence of V_{CE} on I_C and various other control parameters from the results reported previously [10] with the feed-forward implementation of the desaturation pulse. Similar measurements for chip W2 have been made at

Table I: Desat-pulse based turn-off measurement results at different I_C for chip W1

I_C (A)	**E_{OFF} (intr) (J)**	**E_{OFF} with desat pulse (J) (5V TVS diode, t_{clamp} 22µs)**	**% Reduction in E_{OFF}**	**V_{CE} during desaturation pulse (V)**
159	0.316	0.22	30	17.3
120	0.256	0.166	35	16.6
90	0.204	0.132	35	15.8
75	0.175	0.113	36.5	15.3
53	0.133	0.085	36	14.8
21	0.059	0.039	33	14

Table II: Desat-pulse based turn-off measurement results at different I_C for chip W2

I_C (A)	E_{OFF} (intr) (J)	E_{OFF} with desat pulse (J) (No TVS diode, t_{clamp} 22µs)	% Reduction in E_{OFF}	V_{CE} during desaturation pulse (V)
159	0.158	0.116	21	12.8
120	0.175	0.134	23	12.2
90	0.143	0.103	28	10.9
75	0.122	0.09	26	10.3
53	0.095	0.068	29	9.5
21	0.043	0.032	25	8.8

its respective optimal combination of $V_{CE,clamp}$ and t_{clamp} determined for the nominal current case. These results are shown in table II. It can be seen again that this turn-off method shows consistent performance in terms of reduction in E_{OFF} in the entire range of currents considered in the measurement.

The measurements on W1 and W2 could be viewed comparatively in a trade-off diagram where the on-state voltage drop $V_{CE,sat}$ is plotted along the abscissa and the absolute turn-off energy loss E_{OFF} plotted along the ordinate. For each device, the normal turn-off is indicated in black whereas the result from the turn-off with desaturation pulse is shown in red. As could be expected, the result of a lesser $V_{CE,sat}$ for device W1 is an increased E_{OFF} compared to device W2. However, this diagram now brings out the advantage of the desaturation pulse-based turn-off. It can be seen that as a result of the desaturation pulse-based turn-off, the absolute reduction in E_{OFF} for device W1 is much larger than the corresponding reduction in device W2. Therefore, the E_{OFF} values for the devices are now closer to each other compared to the normal turn-off case. Obviously, the best result would have been if the E_{OFF} after the desaturation pulse were to be almost the same while W1 featured a much lower $V_{CE,sat}$ compared to W2.

Investigations in this direction are conveniently pursued with the TCAD simulations approach, which will be presented in the following section.

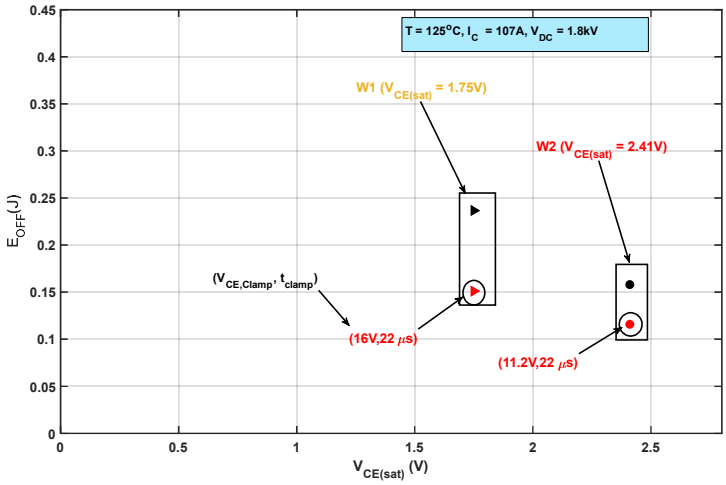

Fig. 8: Trade-off diagram comparing the devices W1 and W2
Legend: Black: Normal turn-off, Red: Turn-off with desaturation pulse

Collector-gate clamping based desaturation pulse – TCAD Simulation Results

TCAD turn-off simulations of the clamping-based desaturation pulse are carried out to further investigate the potential of this turn-off method to determine the extent of reduction in E_{OFF} as well as to obtain an insight into the required profile of the on-state carrier concentration in the device to achieve such a result. A trade-off between $V_{CE,sat}$ and E_{OFF} (normal turn-off) results when the plasma concentration is increased in the device. It will be investigated if along with a lower $V_{CE,sat}$ in such IGBTs, a lower E_{OFF} could also be achieved with the implementation of the desaturation pulse, which is desirable from the point of view of reduction of overall inverter losses. Previous work [10] presented simulation results with the clamping method with a low-saturation IGBT model, which promisingly showed up to 52% reduction in turn-off energy losses. In this section, further simulation results with different low-sat IGBT models are presented.

The turn-off simulation circuit is shown in Fig. 9. The breakdown voltage of diode D determines the collector-gate clamping voltage level. The duration for which the switch Sw is turned on determines the duration of the clamping desaturation pulse during the turn-off of the IGBT.

Fig. 10 shows the on-state plasma profiles of the simulated 3.3kV IGBT models at a nominal current of 450A corresponding to a XHP module. The model M1 features a moderate slope between the front-end emitter and the collector of the device, and resulted in 52% reduction in turn-off energy losses with the clamping-desaturation pulse-based turn-off method [10]. Model M2 has the same back-end emitter plasma concentration but features a higher front-end concentration compared to the model M1 whereas in model M5, the back-end concentration is increased while keeping the front-end concentration unchanged. Model M3 features a reduced back-end concentration compared to, and same front-end concentration as M2 and model M4 has a much higher front-end concentration and same back-end concentration as M3.

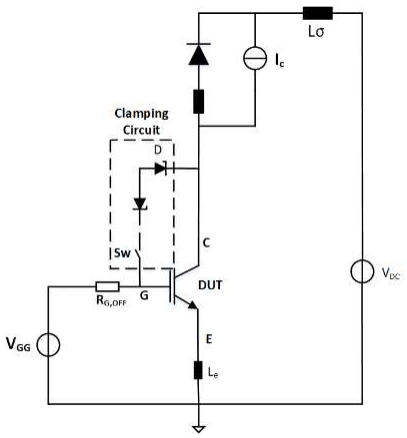

Fig. 9: Simulation Circuit for the clamping-based desaturation pulse

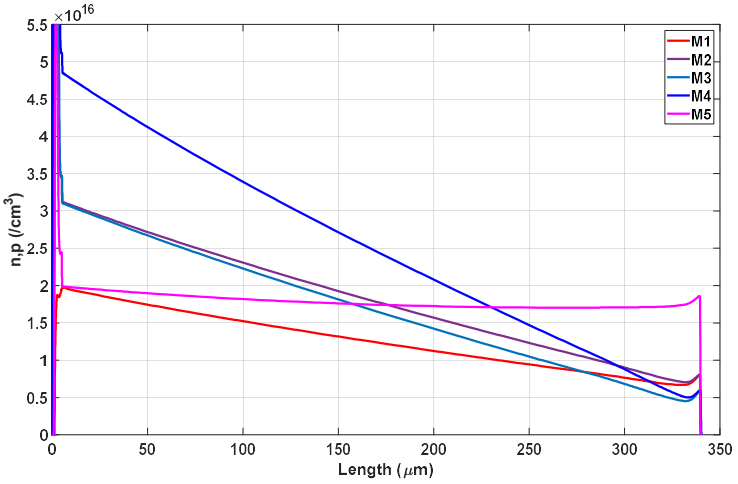

Fig. 10: On-state carrier concentration profiles of simulated models

Fig. 11 shows the summary of desaturation pulse-based turn-off simulations in a trade-off diagram similar to Fig. 9, where the $V_{CE,sat}$ is plotted along the x-axis and the E_{OFF} along the y-axis. The black markers show the points corresponding to normal turn-off whereas the red markers show optimal results from the desaturation pulse-based turn-off. As is evident, models M2, M3, M4 and M5 as expected, have a lower $V_{CE,sat}$ compared to model M1 as a result of higher plasma concentration in the device. Model M4, with the steepest plasma concentration profile between the emitter and collector has a $V_{CE,sat}$ of 1.29V at I_{nom} compared to $V_{CE,sat}$ of 1.96V seen in M1. With the desaturation pulse-based turn-off, the E_{OFF} in case of M4 is reduced from the intrinsic E_{OFF} of 1.031J to 0.42J, which is a significant reduction of about 60%. Therefore, the model M4 not only has a 35% reduced $V_{CE,sat}$ compared to model M1, but also an almost same value of E_{OFF} after the desaturation pulse. The device M4 therefore, offers both a large reduction in on-state conduction losses and with the desaturation pulse-based turn-off, also a higher absolute reduction in E_{OFF} bringing it to a value almost at par with the E_{OFF} of model M1

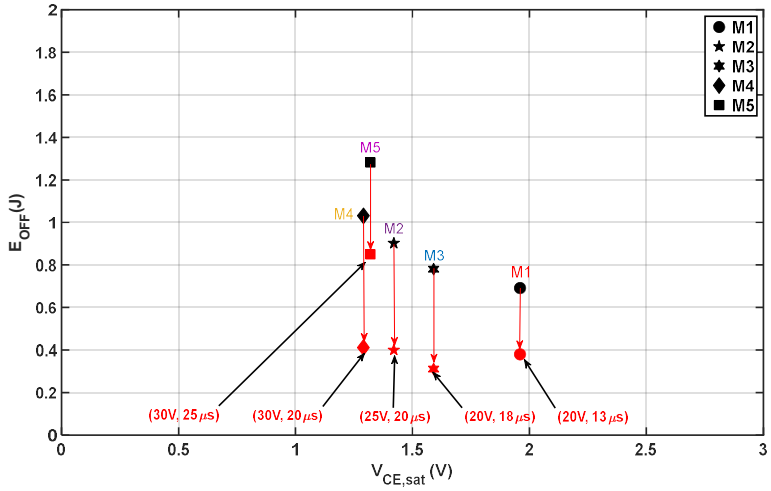

Fig. 11: Trade-off diagram from the desaturation-pulse based turn-off simulations
Legend: Black: Normal turn-off, Red: Turn-off with the desaturation pulse

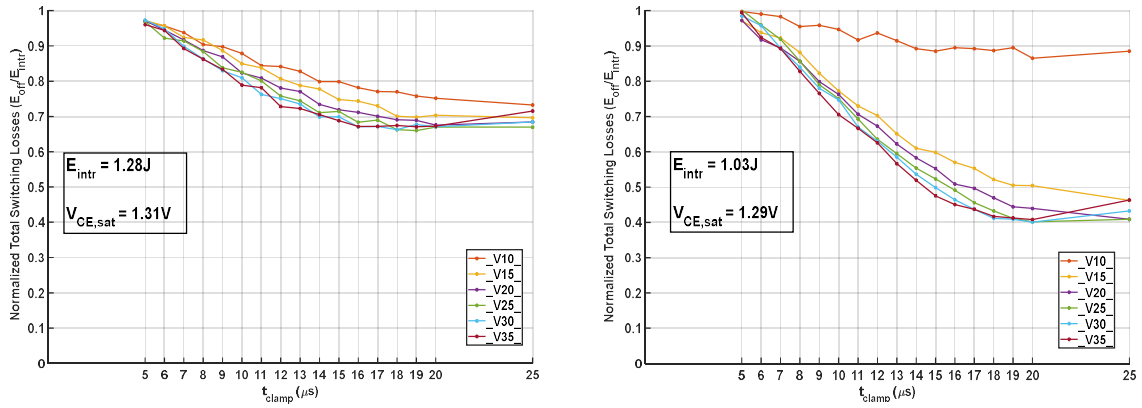

Fig. 12: Normalized E_{OFF} – Left: Model M5 and Right: Model M4

The turn-off energy losses with the desaturation pulse can be split into the conduction losses during the clamping duration and the losses during the final commutation. An analysis of the effect of the plasma profile on the switching and commutation losses provide insight into the desirable plasma profile from the point of view of possible further reduction in turn-off energy losses. The summary of turn-off simulation results for models M4 and M5 are presented in Fig.12, with the normalized E_{OFF} plotted for different collector-gate clamping voltages during the desaturation pulse ($V_{CG,clamp}$) and different values of t_{clamp}. It can be seen that the model M5, with higher collector-sided plasma concentration shows a maximum reduction of about 34% in E_{OFF} at the optimal combination of $V_{CG,clamp}$ = 25V and t_{clamp} = 20µs. However, the model M4 with a much higher front end plasma concentration and much lower back-end doping shows a significantly higher reduction of about 60% in E_{OFF} at the optimal combination of $V_{CG,clamp}$ = 30V and t_{clamp} = 20µs. It is noted, that both these models have almost the same $V_{CE,sat}$. The corresponding normalized commutation losses E_{comm} for both models are plotted in Fig. 13. The reason for a much larger reduction in E_{OFF} with desaturation pulse in case of model M4 is immediately evident from this figure. Model M4 shows a large reduction of about 85% in commutation losses at the determined minimum loss point whereas model M5 shows only about 58% at its respective minimum loss point. Therefore, it could be inferred that a steep on-state plasma profile is desirable from the loss reduction point of view after the desaturation pulse.

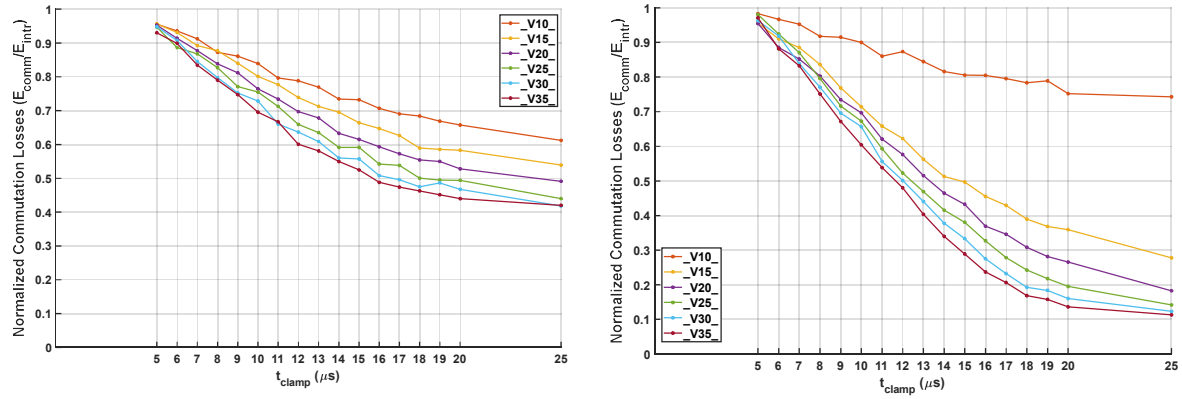

Fig. 13: Normalized E_{comm} – Left: Model M5 and Right: Model M4

The effect of the collector-sided plasma concentration on reduction in E_{OFF} and the necessary t_{clamp} are further investigated by plotting the normalized E_{OFF} and E_{comm} as a function of t_{clamp} at a particular level of $V_{CG,clamp}$ of 20V for the considered simulation models. From Fig. 14a, it is discernable that the model M1 shows the fastest reduction in E_{OFF} with respect to t_{clamp}, whereas the models with the higher device plasma concentration require increasingly larger values of t_{clamp} for a substantial reduction in E_{OFF}. Fig. 14b shows that the corresponding reductions in E_{comm} during the desaturation pulse appear to depend directly on the collector-sided plasma concentration in the device. This is evidenced by the fact that while model M5 shows the lowest reduction in E_{comm}, the models M3 and M4 show the largest reductions. An increase in the emitter sided concentration from M3 to M4 means that M4 requires a longer t_{clamp} to achieve this reduction but results in a better tradeoff between $V_{CE,sat}$ and E_{OFF} after the desaturation pulse as seen from the tradeoff diagram in Fig. 11.

The evolution of plasma inside the device during the progress of the desaturation pulse is shown in Fig. 15 for both the models, for a $V_{CG,clamp}$ of 20V. It can be seen from the figures that at the end of the desaturation pulse, model M5 still contains a large amount of plasma at the collector side as compared to model M4, which has desaturated substantially throughout the drift region of the device. This implies that a large reduction in losses

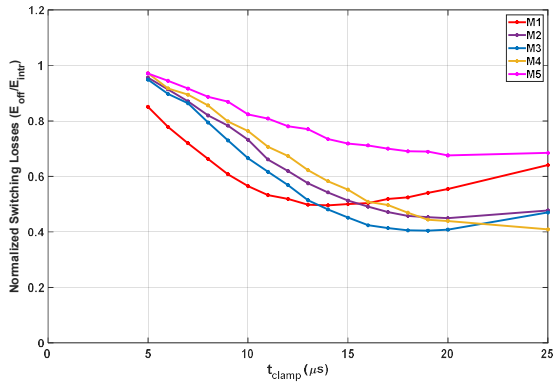

Fig. 14a: Normalized E_{OFF} for all models at $V_{CG,clamp=}$= 20V

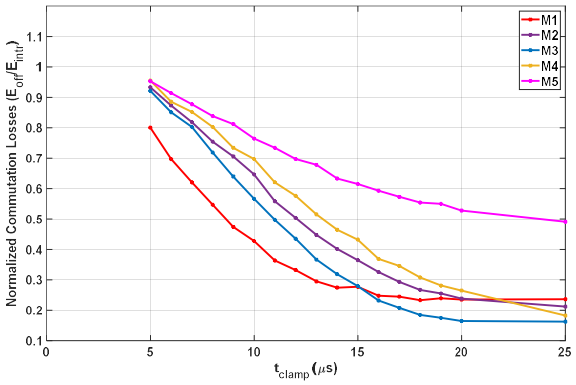

Fig. 14b: Normalized E_{comm} for all models at $V_{CG,clamp}$= 20V

during the final commutation is possible in case of model M4, thereby leading to a much better result from the desaturation pulse.

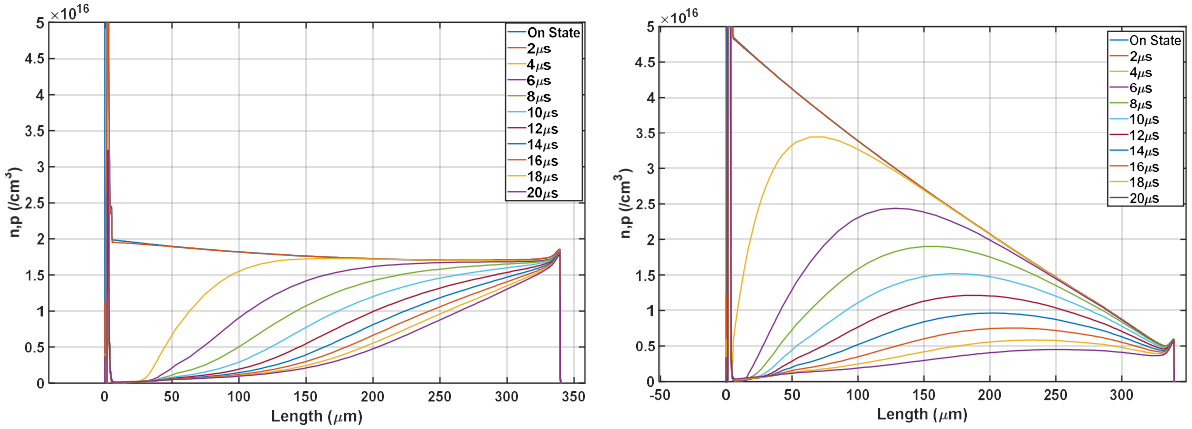

Fig. 15: Evolution of device plasma concentration during the desaturation pulse - Left: Model M5 and Right: Model M4

Conclusion

In this paper, further investigations into the turn-off of modern low-saturation type 3.3kV IGBT devices with the desaturation pulse have been presented. Turn-off measurements with the desaturation pulse based on a novel active-clamping based method applied on two different experimental 3.3kV IGBT chips have been presented. These measurements have shown up to 37% reduction in turn-off energy losses for one of the chips. Further measurements with that this method show a consistent reduction in turn-off energy losses over a range of currents carried by the device. TCAD based turn-off simulation results with desaturation pulse have been presented for different low-saturation IGBT models. These simulations have indicated the possibility of a device having not only a very low on-state collector-emitter voltage drop but also a potentially a much larger reduction of up to 60% in turn-off energy losses for a device with a steep gradient of the on-state carrier concentration profile.

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