Distribution transformer voltage control using a single-phase matrix converter

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Abstract

A new topology is proposed for fully-electronic tap changers in distribution transformers. In every single phase, the voltage is regulated by a 2×1 matrix converter, which can be extended using the concept of multilevel converters. The topology allows reaching the desired functionality with one single tap, which reduces the cost of the transformer.

Introduction

Medium-voltage (MV) to low-voltage (LV) distribution transformers are used to step down the MV grid voltage to a suitable level for residential consumers. LV side end-users shall receive a stable voltage with $\pm 10\%$ tolerance typically. However, users can receive different voltage levels due to the voltage drop across the line impedance. As a trend, residential load variations are increasing due to the growing penetration of electrical vehicles and heat pumps. Apart from these, the installation of solar panels can also cause bidirectional power flow, which roughly doubles the voltage swing at consumer side. As a result, voltage fluctuations become larger and happen more frequently.

To maintain a relatively stable LV side voltage, tap changers are used to vary the effective transformer turns ratio. In principle, tap changers can be placed at either MV or LV side of the transformer; the most common is at the MV side. Fig. 1 shows a simplified circuit of a distribution transformer with tap changers. The transformer is in Delta-Wye connection; it has $(n_{1a} + n_{1b})$ turns at the MV side and n_2 turns at the LV side. The tap winding is located at the MV side, in this example, it has n_{1b} turns in total and five tap positions. By switching to different positions, different voltage levels can be obtained at the LV side.

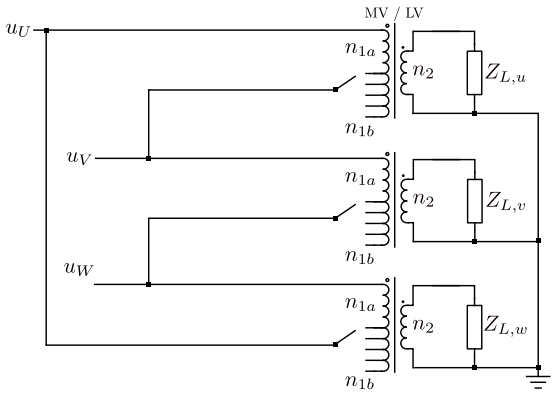


Fig. 1: Distribution transformer with mechanical tap changers at the MV side.

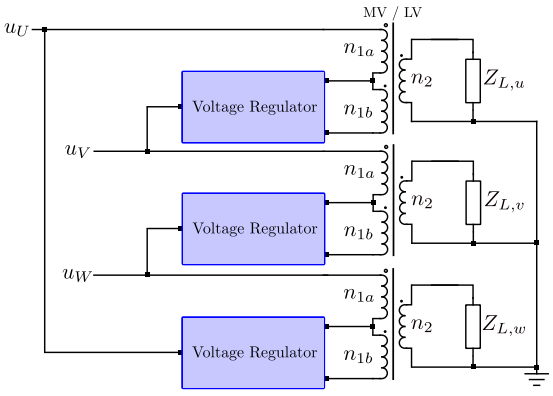


Fig. 2: Proposed voltage regulators for a distribution transformer.

Conventional tap changers use mechanical switches, which limit the speed of the tap-changing process. The resolution of the voltage regulation depends on the number of tap positions. The lifetime of mechanical switches is significantly impacted by arcs during switching. To reduce maintenance cost, electronically-assisted tap changers use both mechanical and semiconductor switches. Semiconductor switches are used in the process of switching between different tap position, which avoids arcing and thereby extends the lifetime of the mechanical switches. However, the time of the tap-changing process (between two taps) is still $100 \sim 200$ ms [1, 2, 3]; and jumping taps is not allowed as this would lead to large circulating current. Fully-electronic tap changers replace mechanical switches with semiconductor switches, which bring many advantages compared to mechanical switches [2]:

- Low maintenance cost: The arcs caused by mechanical switches disappear.
- Fast tap-changing process because of the high switching speed of semiconductor devices.
- Better controllability: The LV side voltage can be controlled continuously, which suggests that these tap changers can be used in power quality management.

Considering the switching and conduction losses, efficiencies of fully-electronic tap changers are lower than of their mechanical counterparts. Manufacturing and component costs are higher for fully-electronic tap changers; however, their maintenance costs will be significantly lower compared to designs using mechanical switches. Therefore, fully-electronic tap changers are very promising compared to conventional products.

Previous research proposed fully-electronic tap changers by inserting parallel half-bridge circuits between multiple tap positions [5, 6, 7]. In this paper, a new topology is proposed for fully-electronic tap changers as shown in Fig. 2. The tap changer requires only one tap connection. For simplicity, the following discussion will focus on the VR in one single phase of the distribution transformer as shown in Fig. 3. The transformer is assumed ideal; for brevity, the filter design will not be covered in this paper.

Voltage regulator

Fig. 4 provides an equivalent circuit of the VR. In this circuit, the VR is presented as three voltage sources u_x, u_z and u_y. According to coupling of the transformer:

$$u_y = u_z - u_{UV} + u_L \frac{n_{1a} + n_{1b}}{n_2} \tag{1}$$

u_y can be defined as a function of inputs u_x and u_z:

$$u_y = \frac{1}{2}\left((u_x + u_z) + K(u_x - u_z)\right) \tag{2}$$

where K is a control variable to realize different LV side voltages and $-1 \leqslant K \leqslant 1$. The effective MV side winding turns $n_{1,e}$ is defined as:

$$\frac{n_{1,e}}{n_2} = \frac{u_{UV}}{u_L} \tag{3}$$

By combining (1) and (2), $n_{1,e}$ can be obtained:

$$n_{1,e} = n_{1a} + \frac{1}{2}(1 - K)\, n_{1b} \tag{4}$$

For $K = 1$, the tap winding n_{1b} is open and only n_{1a} is used; for $K = -1$, the tap winding is fully connected and $(n_{1a} + n_{1b})$ winding turns are used at the MV side. The effective MV side turns can be controlled to any value in between n_{1a} and $(n_{1a} + n_{1b})$ by setting K.

For a conventional mechanical tap changer, the grid voltage is applied to the main transformer winding n_{1a} and part of the tap winding $\frac{1}{2}(1 - K)\, n_{1b}$; whereas the rest of the tap winding $\frac{1}{2}(1 + K)\, n_{1b}$ is open and there is no current flowing. However, for the electronic VR, a current i_z flows through the entire tap winding n_{1b}.

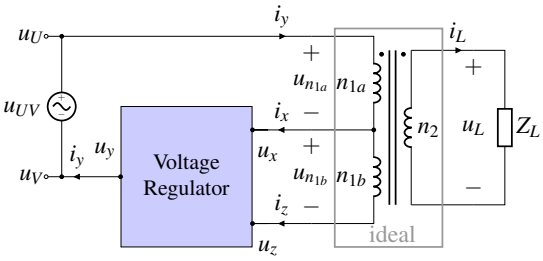


Fig. 3: Voltage regulator of one phase.

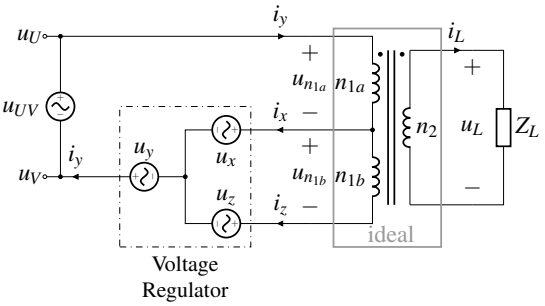


Fig. 4: Simplified single-phase circuit.

Fig. 5 and Fig. 6 show two basic topologies for the VR. For the half-bridge topology in Fig. 5, the VR is directly switching between the tap winding terminals. The average voltage of u_y can be set by the duty cycle of the pulse-width modulation. Bidirectional voltage-blocking switches are required due to the AC voltage. The advantage of this circuit is its simplicity. However, these bidirectional switches need to be controlled very accurately in the commutation process.

Fig. 6 shows a different solution using the matrix topology, it contains three switching legs X, Y, Z and a DC link capacitor C_{dc}. Phases X and Z are connected to the tap winding; they control the circulating current between the VR and the tap winding. The LV side voltage is determined by the duty cycle of phase Y. Because of the DC link, bidirectional voltage-blocking switches are unnecessary; standard IGBTs or MOSFETs with diodes can be used. As in the case of mechanical switches, the VR does not need to store energy. The DC link voltage is constant in the steady state; and as a consequence, the capacitor can be small in principle. This circuit needs two more switches compared to the AC half bridge. Thus, the matrix circuit has a higher manufacturing cost. However, the implementation of control is easier because bidirectional voltage-blocking switches are not required.

Considering MV applications, the high voltage is challenging for IGBTs/MOSFETs. For the half bridge circuit, a possible solution would be using series connected switches to reduce the voltage stress per switch. However, this requires a lot of efforts in hardware design. For the matrix converter, there are more multilevel solutions available, such as modular multilevel converters (MMC). This topic will be covered in future research.

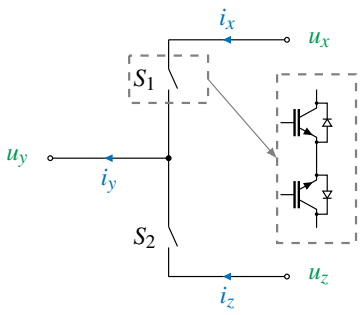


Fig. 5: Half bridge

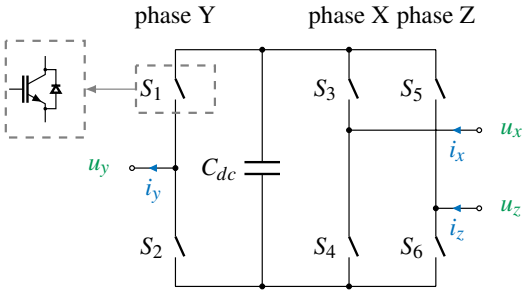


Fig. 6: Matrix converter

Matrix converter control

A cascade control strategy is used for the matrix circuit. The inner current loop controls the circulating current to guarantee the energy balance; and the voltage loop keeps the DC link voltage constant.

The current loop is shown in Fig. 8. The circulating current is defined as:

$$i^{\Delta} = i_x - i_z \tag{5}$$

The reference of circulating current is derived from the energy balance of the VR:

$$\int_{t_0}^{t_0+\frac{1}{f_0}} \left(i_x u_x + i_z u_z - i_y u_y\right) \mathrm{d}t = 0 \tag{6}$$

where f_0 is the fundamental frequency of the grid voltage. This equation can be simplified to:

$$\int_{t_0}^{t_0+\frac{1}{f_0}} \left(i^{\Delta} - K\, i_y\right) \left(u_x - u_z\right) \mathrm{d}t = 0 \tag{7}$$

According to (7), the circulating current reference $i^{\Delta}_{\mathrm{ref}}$ should be

$$i^{\Delta}_{\mathrm{ref}} = K\, i_y + i^{\Delta_\perp} \tag{8}$$

where the term $i^{\Delta_\perp}$ only contributes to reactive power. This orthogonal term $i^{\Delta_\perp}$ can have a 90° phase difference with respect to the voltage $(u_x - u_z)$. Alternatively, $i^{\Delta_\perp}$ can also contain harmonics at different frequencies; this will not be discussed in this paper. A proportional-resonant (PR) controller C_{i_Δ} is used in the current loop due to the sinusoidal current reference. In practice, an additional integrator (PIR) might be needed to prevent DC offset in the current.

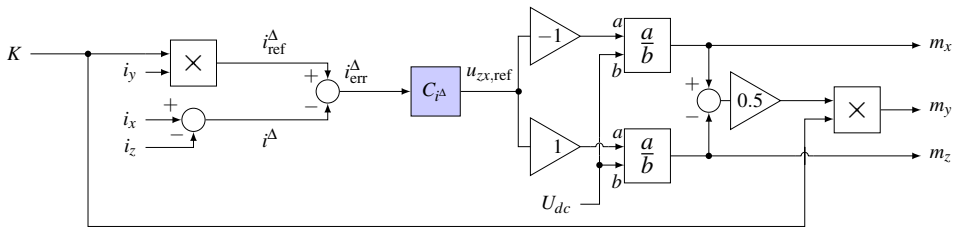


Fig. 7: Current loop control.

The control diagram including the voltage loop is shown in Fig. 8. A PI controller $C_{U_{dc}}$ is used to keep a constant DC link voltage. The output of the PI controller is multiplied by the signal $0.5(m_x - m_z)$, in order to obtain a sinusoidal reference $i^{\Delta}_{\mathrm{ref},2}$ to be added to the current loop.

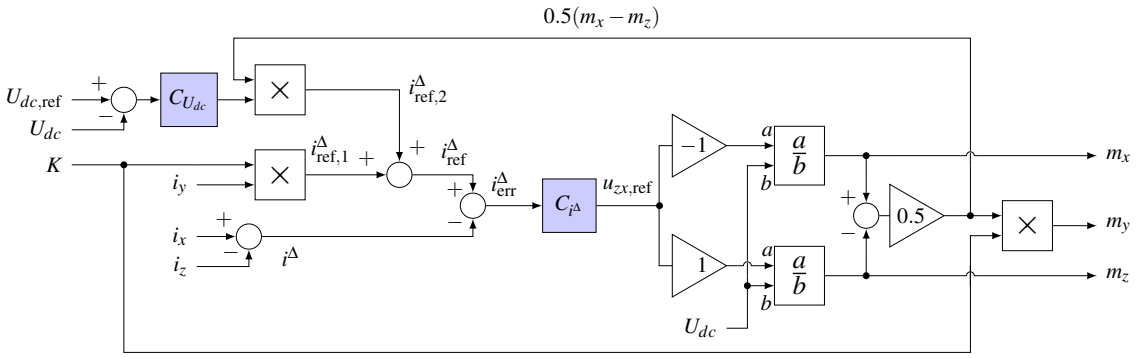


Fig. 8: Control diagram for the matrix baseline.

Scaled-down test

The purpose of this test is to verify the operating principle of the proposed matrix topology. Fig. 9 shows the lab setup; the schematic is shown in Fig. 10. The input voltage u_{in} is 240 Vrms, 50Hz. The VR circuit uses an existing 3-phase IGBT inverter with a 2.45 mF DC link capacitor. The IGBTs are switching at 20kHz with 2μs dead time. The high frequency components of the modulated voltages are eliminated by LC filters. The selected transformer (USTE 1000/2x115) has a rated power of 1 kVA and the turns ratio is $n_{1a} : n_{1b} : n_2 = 2.02 : 0.48 : 1$. The tap winding n_{1b} is arranged at the primary side. A 60Ω resistor R_L is placed at the secondary side as load.

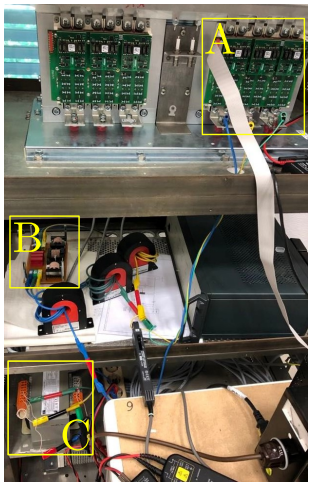


Fig. 9: Lab setup

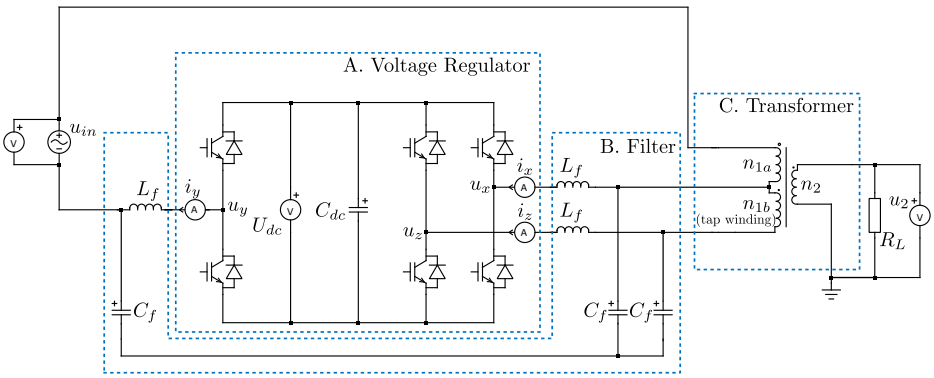


Fig. 10: Schematic of the test setup

The control is realized using a dSPACE MicrolabBox 1202/1302. The DC link voltage U_{dc} should be higher than the tap winding peak voltage in order to prevent over modulation. Initially, U_{dc} is controlled at 80V to just satisfy this requirement. In the current loop, the orthogonal term $i^{\Delta_\perp}$ is set to zero.

Results

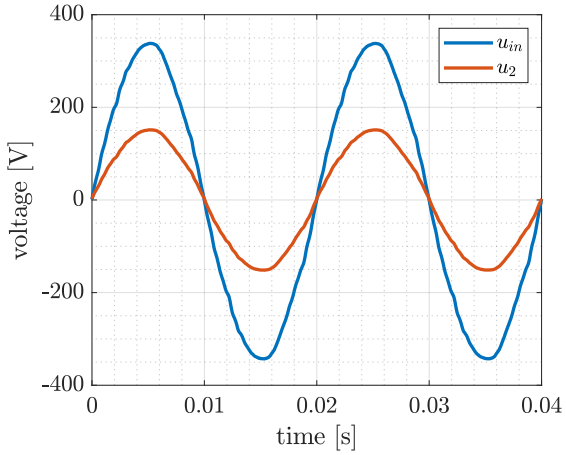
Fig. 11 shows the results of the operation when K equals 0.5. The input voltage u_{in} and regulated transformer secondary voltage u_2 are shown in Fig. 11a; and the resulting VR currents are shown in Fig. 11b. Fig. 11c shows the DC link voltage of the VR; u_{dc} was controlled at 80V with a very small ripple. In Fig. 11d, the circulating current i^{Δ} is tracking the reference. However, the actual current was slightly larger than its ideal reference (Ki_y). This difference could be related to the considerable dead time, which was not concerned in the ideal situation. The modulation errors caused by the dead time are nonlinear functions of currents. In the VR, currents in switching legs X, Z and Y have different amplitudes, which lead to different errors of u_x, u_z and u_y. As a result, the circulating current reference needs to be corrected to maintain the energy balance. Besides, the converter loss is also a concern. Especially the switching loss can be considerable due to the hard switching.

The current flow to the input voltage source i_y and also the load current i_2 were measured using an oscilloscope as shown in Fig. 12. Spikes appeared in the unfiltered waveform of i_y due to the hard switching of IGBTs. After filtering, harmonics at the switching frequency were mostly eliminated. In terms of the load current i_2, the amplitude of the ripple was less than 3%. The ripple and harmonic distortion can be further reduced by optimizing the filter design if necessary.

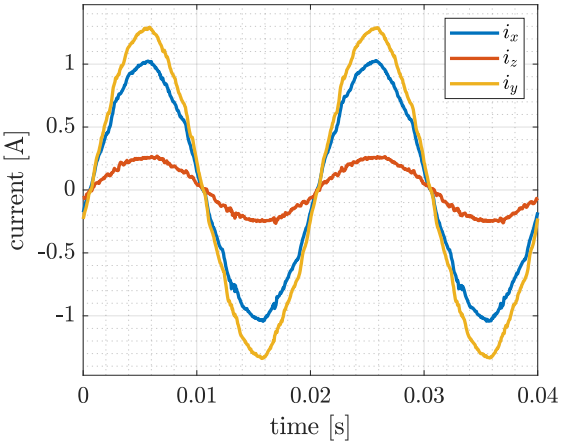
The dynamic performance was investigated by using step references for K. Results are shown in Fig. 13 and Fig. 14. In both test scenarios, the current loop immediately followed new references. Due to the disturbance in the current loop, the DC link voltage changed in the beginning and was gradually controlled back to its reference. Especially, in Fig. 14, the step of K happened when the input voltage was at its peak value. Though oscillations were observed initially, controllers regulated the system to the steady state in a short time.

According to (4), the effective number of turns n_{1e} at the primary side of the transformer can be more than $(n_{1a}+n_{1b})$ if $K<-1$, or less than n_{1a} if $K>1$. However, when K is set beyond the normal operation range of $-1 \leqslant K \leqslant 1$, the amplitude of the VR output voltage u_y will increase. Thus, a higher DC link voltage is required to prevent overmodulation. In Fig. 15, the DC link voltage was increased to 120V. In the normal operation, the waveform of u_2 was limited to the area between $u_2|_{K=-1}$ and $u_2|_{K=1}$. When K was set to +/-1.2, u_2 resulted in slightly larger/smaller amplitudes.

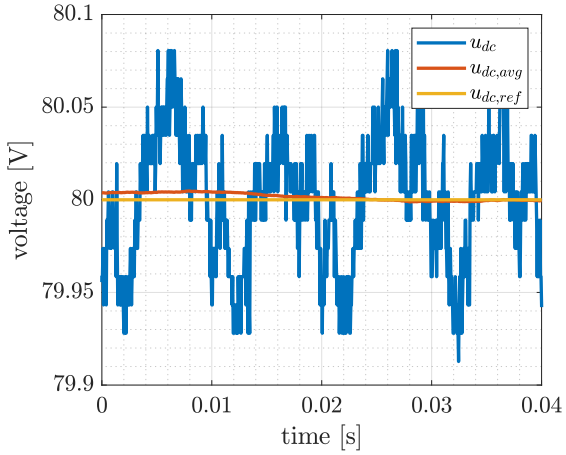
Fig. 16 summarizes the voltage regulation range as a function of the control variable K. The voltage base



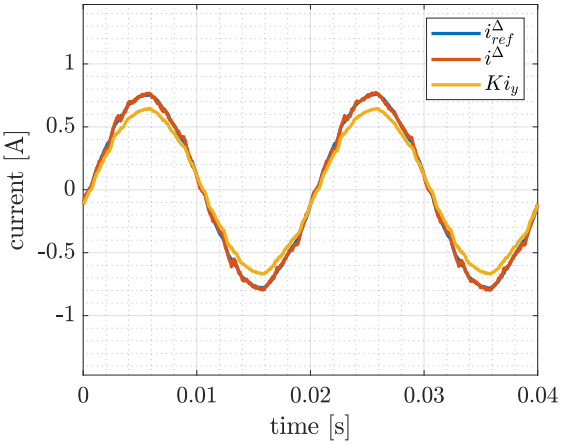
(a) voltage



(b) VR currents

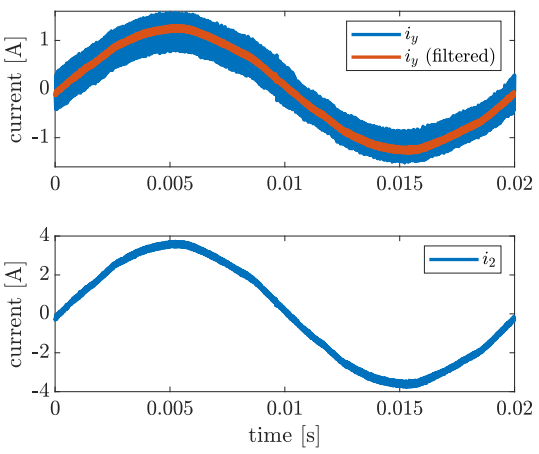


(c) DC link voltage ripple

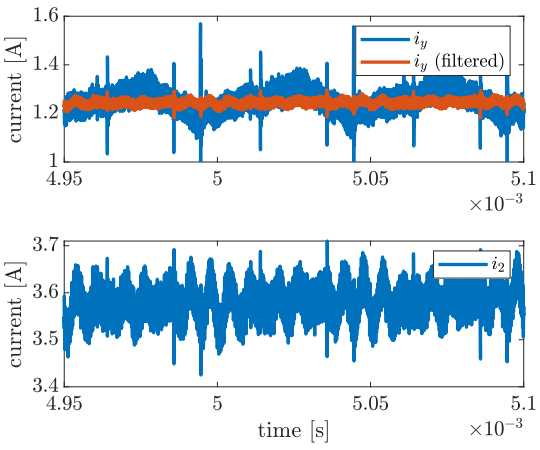


(d) circulating current

Fig. 11: Test results at $K = 0.5$.

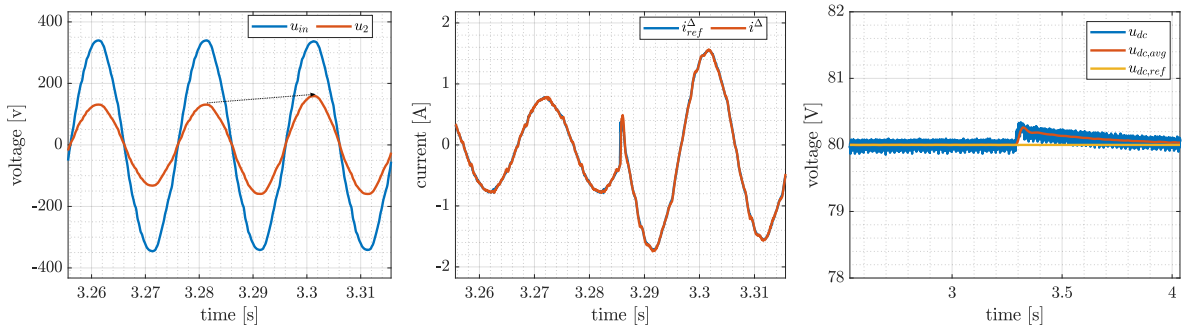


(a) One 50Hz cycle



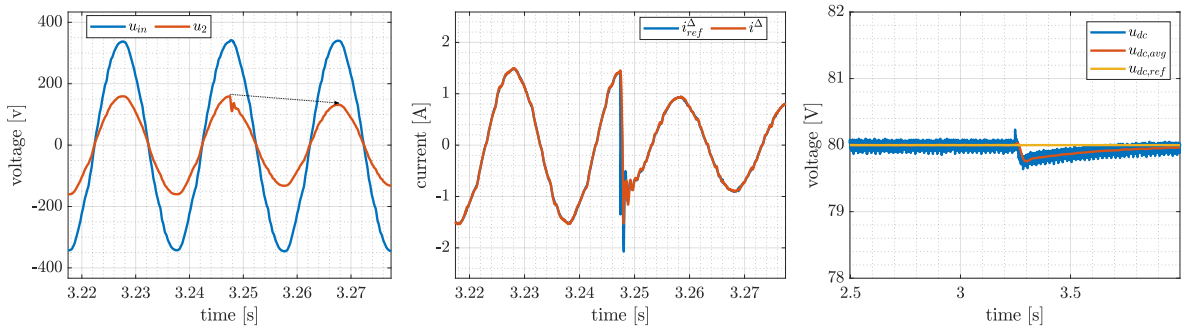
(b) ripples at peak currents

Fig. 12: Current i_y and i_2, measured by oscilloscope ($K = 0.5$).



(a) voltage (b) circulating current (c) DC link voltage

Fig. 13: Step response: K steps up from -1 to 1.



(a) voltage (b) circulating current (c) DC link voltage

Fig. 14: Step response: K steps down from 1 to -1.

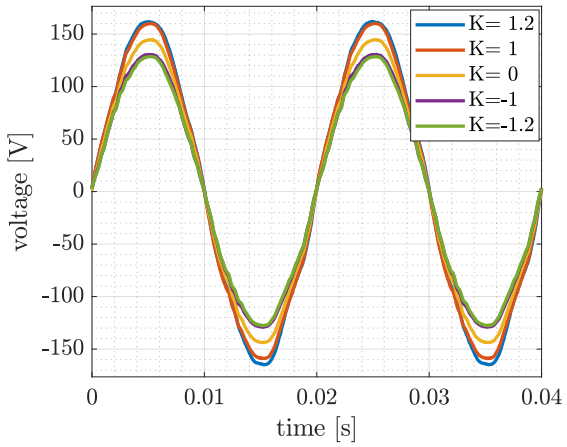


Fig. 15: u_2 wrt. K values, $U_{dc} = 120$V

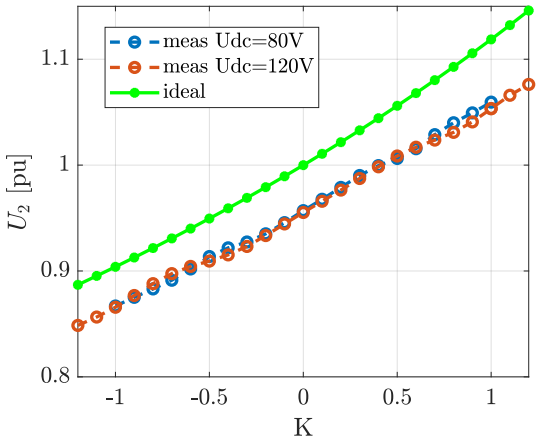


Fig. 16: Voltage regulation range

is chosen as the ideal voltage of U_2 when $K = 0$, and the input grid voltage is 240Vrms.

$$U_{base} = 240 \times \frac{n_2}{n_{1a} + \frac{1}{2} n_{1b}} = 106.2\,\mathrm{V}. \tag{9}$$

The ideal curve is estimated by:

$$U_2\,[pu] = \frac{240\,\mathrm{V}}{U_{base}} \times \frac{n_2}{n_{1a} + \frac{1}{2}(1-K)\, n_{1b}}. \tag{10}$$

During the test, u_2 was measured when a different DC link voltage U_{dc} was applied. In normal operation, U_2 did not show a dependency on U_{dc}. However, operation at $K < -1$ or $K > 1$ was not possible when U_{dc} was 80V. As shown in Fig. 16 , the measured secondary voltages were smaller than their ideal values. To explain this difference, aside from the dead time distortion as mentioned before, other reasons could be the impacts of the filter and also the leakage components of the transformer. This will be investigated in the future.

Conclusion and future work

In this paper, a new power-electronic tap changer (VR) is proposed for distribution transformers. The voltage regulation is realized by a single-phase matrix type converter. In previous research, the voltage regulation range was often limited by the length of the tap winding; whereas this proposed VR is capable to realize a wider range of effective turns coupled to the input voltage (with $K > 1$ and $K < -1$). The functionalities of the proposed matrix type circuit are verified in a scaled-down test. However, there were some mismatches between ideal estimations and measurements. Further study needs to include more details in modelling: for instance, the three-winding transformer model including leakage components and also considering the converter loss in the energy balance calculation.

The voltage of the MV grid is normally 10kV or 23kV in Europe. Thus, extending the proposed concept to multilevel/multi-cell topologies (e.g. modular multilevel converters) is needed. This will be addressed in future research.

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