On the reduction of output capacitance in two-level three phase PFC boost rectifier for pulsating loads.

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Keywords

«AC-DC converter», «Capacitors», «Converter control», «Pulse current charge/discharge», «Volume reduction».

Abstract

This work explores the dc-link capacitance reduction of a traditional three phase rectifier. A review of different methods for reducing the current across the dc-link capacitor, and consequently its size, is presented in this paper. In this work, the achievable capacitance reduction is explored by the action of a dual-loop control. A two-level power factor correction six-switch voltage source rectifier feeding a high demanding pulse load is analyzed. As a baseline, the output capacitor is designed from an energy storage perspective to achieve a specified maximum voltage ripple. The control design is performed in the frequency domain to get the best disturbance rejection under certain requirements and implementation constraints with the help of system time response evaluation. This work proposes a theoretical analysis that can be applied for the pursuit of converter weight reduction or other figures of merit such as volume or cost. The conclusions achieved with that theoretical study provide capacitance reduction ratios for the two-level power factor correction six-switch voltage source rectifier when implementing a classic dual-loop control algorithm.

Introduction

In power electronics, the use of capacitors acting as decouplers between supply and load is widespread. In that case, the capacitor must be designed to supply the load power demand during a certain time. Some examples can be found in dc-dc converters, Modular Multilevel Converters (MMC) or single-phase ac-dc converters [1]. In some of these cases, the capacitor is designed from an energy perspective, resulting in high capacitive values and consequently bulky capacitors. Furthermore, in some applications of three phase converters, the output capacitor has also to be sized for energy storage target. For instance, in Back-to-Back (BTB) converters, the robustness of the dc link is crucial and the capacitor should compensate any mismatch between the rectifier and the inverter [2].

The new paradigm of the electric mobility requires improvements in the specific power density of power converters. Transportation electrification is demanding higher power density power converters so the new electric solutions can substitute the original systems without increasing the total weight and volume of the propulsion system, which could derive into implementation problems and extra cost [2]– [4]. Reactive components are constantly under study in order to reduce their volume and weight because they are the highest contribution to power density of power converters. In the case of capacitor size reduction, an effective method is based on the minimization of current through the capacitor. The current through the capacitor is the sum of the current due to the instantaneous power imbalance between the power converter and the load, and the current harmonic content.

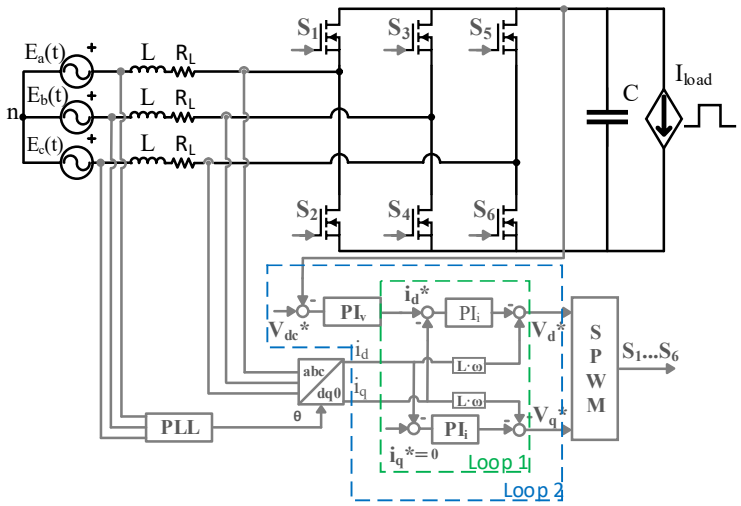


Fig. 1. Application scheme

Several methods to reduce either current type can be classified in three categories [5]: inverter topology modification [6], power balance control and innovative modulation schemes [7]. The power balance control method proposes different control schemes to improve the controller response speed, some of them can be found in [8], [9]. However, these control schemes add complexity to the control implementation. In [10], the BTB minimum capacitance is defined for different switching frequencies based on the linear relation between the inductance and the capacitance when the capacitor is purely selected and designed from an energy perspective. The main contribution of this work is a methodology to reduce the output capacitor by analysing the dynamics limit of a classic dual-loop control scheme, see Fig. 1, guaranteeing using the voltage ripple as a constraint.

The case under study consists of a two-level power factor correction six-switch voltage source rectifier (PFCVSR) supplying a pulsating high current load. The load of the converter can be considered as a pulsating current source connected to the output capacitor with a long period (i.e., on the order of milliseconds) when compared to the switching period of the power converter. In this work, the capacitance reduction is attained with the design of the control for the rectifier. The control design process includes the digital time delay introduced by digital implementation (Td). The analysis trades-off the control effort (i.e., control loop required bandwidth and phase margin), the switching frequency, the output voltage ripple and the required capacitance, yielding as a result a mapping of the minimum capacitive values required to achieve the desired performance.

The switching frequency range under study is limited for practical reasons (Table I). Although input filter design is not studied in this paper, the minimum switching frequency is fixed over 40 times the mains frequency not to penalize its design [11]. Although current power devices technology allows to manage high voltage (i.e. hundreds of volts) and medium current level (i.e. tens of amps) up to MHz range, switching frequency has been set 10 times lower to work in a more conservative range.

PFC rectifier control design

Table I shows the data of the system under study. It should be noted that the methodology procedure can be applied to other system specifications if the system is correctly modelled. For example, this is potentially useful for adapting the converter power rating, but if higher frequencies are considered parasitic elements may start playing an important role. The PFCVSR control design presented in this work is based on d-q synchronous reference frame converter average model assuming a sinusoidal PWM modulation [12]. A classic dual-loop control structure is used, where the outer control loop is responsible for maintaining a constant output capacitor voltage and the inner control loop is designed to control the boost inductor currents. Feedforward compensation is also implemented in the current control loop to eliminate the inherent d-q phases cross coupling, see Fig. 1. Therefore, the current control loop dynamics can be reduced to the input boost inductor, which can be simply modelled as a first order plant [13]. The stability requirements can be stablished in terms of phase margin (PM) by studying the control loop in the frequency domain. The minimum acceptable PM is set to 45° in both control loops. Mathematical expressions are derived from both current and voltage open loop gain (OL) to define the PI controller parameters as function of the phase margin (PM) and the crossover frequency (ω_c). At ω_c conditions (1) and (2) are imposed.

$$|OL(\omega_c)| = 1 \qquad (1)$$

$$\angle OL(\omega_c) = -180^0 + PM \quad (2)$$

Table I. Specifications of the case under test.

Variable	Value
Ac frequency	400-800 Hz
Nominal dc bus voltage (V_n)	430 V
Maximum voltage variation	10%
Minimum switching frequency	32 kHz
Maximum switching frequency	100 kHz
Pulse load amplitude (I_{load})	150 A
Pulse load period (T)	2 ms
Modulation index (M_p)	0.8962
T_d	T_{SW}

a) Current control loop design.

The current control loop, control loop 1 in Fig. 1, generates the PWM modulation index required to reproduce a sinusoidal input current in phase with the input voltage and with the required amplitude. The current OL expression is given by:

$$OL_i(s) = Kp_1 \frac{Ti_1 \cdot s + 1}{Ti_1 \cdot s} \cdot \frac{1}{T_d \cdot s + 1} \cdot \frac{1}{L \cdot s + R_L} \quad (3)$$

Although more complex and detailed approaches can be used to model the effect of T_d [14], the approach detailed in [13] is used to model it as a first-order system helping on reducing the complexity of the analysis.

Substituting the conditions defined by (1) and (2) in (3), the next mathematical expressions are yielded,

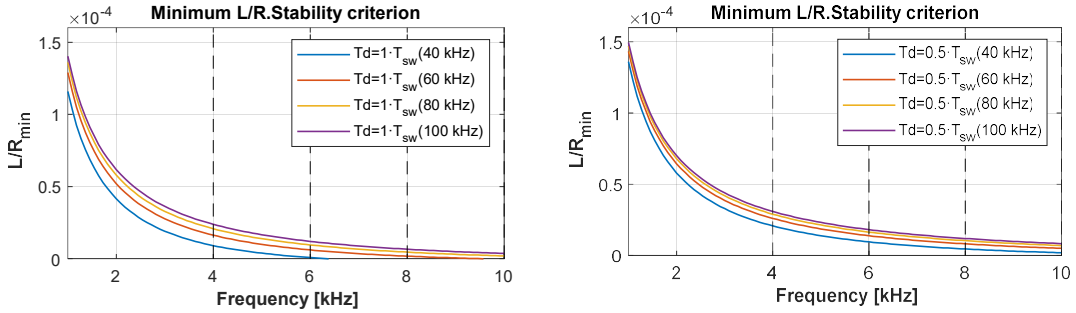
$$Ki_1 = \frac{1}{Ti_1} = \frac{\omega_c}{tan(-90° + PM + tan^{-1}(T_d \cdot \omega_c) + tan^{-1}\left({}^{L}/_{R_L} \cdot \omega_c\right))} \quad (4)$$

$$Kp_1 = \frac{Ti_i \cdot \omega_c}{\sqrt{(Ti_i \cdot \omega_c)^2 + 1}} \cdot \sqrt{(T_d \cdot \omega_c)^2 + 1}.R_L \cdot \sqrt{(L/R_L \cdot \omega_c)^2 + 1} \quad (5)$$

$$PI_i = Kp_1 \cdot \frac{s + Ki_1}{s} \quad (6)$$

, they determined the current controller parameters: Kp_1 that is the PI proportional gain and Ki_1, the PI integral action. They are defined in function of the design constraints, such as PM, ω_c, the inductor time constant defined by the ratio of L, the inductance value, and R_L, which is its series resistance, and T_d. Ti_1 represents the PI control time constant and it is the inverse of Ki_1 and the PI current controller is defined by a PI series form (PI_i). Note that the T_d and the inductor time constant (L/R_L) degrade the loop stability which will be compensated by the PI integral action.

Note that control loop stability can be studied by evaluating (4). The theoretical maximum for the crossover frequency ω_{clim} , can be obtained by equating Ti_1 to zero. T_d can be easily estimated by taking into account the sampling and updating rating [15]. It is normally expressed in terms of sampling periods, which in this case is related with the switching period. For example, T_d can be 1 or 0.5 sampling cycles. Evaluating (4) for $Ti_1 > 0$ the minimum L/R_L for different combinations of ω_c, switching frequency and PM are obtained, Fig.2. These limits indicate the dynamic constraint of the inductor design for a certain PM and ω_c. That is, there are L/R_L that will turn the system unstable and control compensation is not possible. Those limits are used to stablished constraints to the capacitance reduction study meaning that the attained solution will always be a feasible solution from a stability perspective.



(a) (b)

Fig. 2 Current control loop stability minimum boundaries when the PM is 45º and updating occurs at: (a) sampling time, (b) half the sampling time.

b) Voltage control loop.

The control loop 2, voltage control loop, in Fig. 1 is designed to regulate a constant voltage level. Load changes are seen as voltage disturbances by the control loop, so the design is focused on disturbance rejection. The effect of the control loop 1 dynamics has been approximated by a first order transfer function defined by this time constant response (T_{CL}). This can be done if the inner control loop, in this case control loop 1, dynamics are significantly higher than the outer control loop, the control loop 2 in this work. Voltage OL expression is given by,

$$OL_V(s) = Kp_2 \frac{Ti_2 \cdot s + 1}{Ti_2 \cdot s} \cdot \frac{1}{T_{CL} \cdot s + 1} \cdot \frac{3}{4} \cdot M_d \cdot \frac{ESR \cdot C \cdot s + 1}{C \cdot s} \quad (7)$$

Substituting the conditions (1) and (2) in (7) the following mathematical expressions are derived,

$$Ki_2 = \frac{1}{Ti_2} = \frac{\omega_c}{tan(PM + tan^{-1}(T_{CL} \cdot \omega_c) - tan^{-1}(C \cdot ESR.\omega_c))} \quad (8)$$

$$Kp_2 = \frac{Ti_2 \cdot \omega_c}{\sqrt{(Ti_2 \cdot \omega_c)^2 + 1}} \cdot \frac{\sqrt{(T_{CL} \cdot \omega_c)^2 + 1} \cdot C \cdot \omega_c}{\sqrt{(C \cdot ESR \cdot \omega_c)^2 + 1}} \cdot \frac{4}{3 \cdot M_d}. \quad (9)$$

$$PI_v = Kp_2 \cdot \frac{s + Ki_2}{s} \quad (10)$$

, they determined the current controller parameters: Kp_2 that is the PI proportional action and Ki_2,the PI integral action. The voltage controller is defined by a PI series (PI_v). As can be seen the OL gain depends on the modulation index (M_d), which decreases when load current increases. The voltage control loop is designed for the worst case, i.e. for the peak pulse amplitude. If the equivalent series resistance (ESR) of the output capacitor is expected to be big enough to change the design system plant [16], [17], it should be taken into account for the voltage control loop design.

In terms of zeros and poles, ESR adds a zero in the left s-plane side and in terms of frequency response it modifies OL gain and phase. From a time response perspective, it can be translated into slower response and initial voltage peak for high values of ESR. For simplicity, in the study presented in this work ESR effect has been neglected considering the expectation of very low ESR value. Nonetheless, it is important to take it into account otherwise.

PI controllers design criteria.

Fig. 3 illustrates the different design steps followed to determine the capacitance reduction. The solution with the best performance is selected based on (4)-(10) analysis. Best performance selection is evaluated with a performance factor (σ) that is defined in terms of the main close loop (CL(s)) time step response characteristics: the rise time (T_{rise}), the settling time ($T_{settling}$) and the overshoot percentage ($Overshoot(\%)$). For simplicity, in this work σ has been defined as the multiplication of all these characteristics:

$$\sigma = T_{settling} \cdot T_{rise} \cdot Overshoot(\%) \quad (11)$$

The best design is selected based on the minimum σ value, which is assumed to give a good trade off among the three parameters. In terms of control loop 1 the system response studied is focused on reference tracking improvement and in the case of the control loop 2 the system response studied is focused on the disturbance rejection improvement. Both control loop responses are analyzed independently under the same performance factor, although control loop 1 is studied first because it limits the theoretical maximum crossover frequency of control loop 2. In both cases, from a set of scenarios defined under constraints of minimum PM, a pre-defined switching frequency and a certain L/R_L, the case with the lowest σ is chosen as the best design.

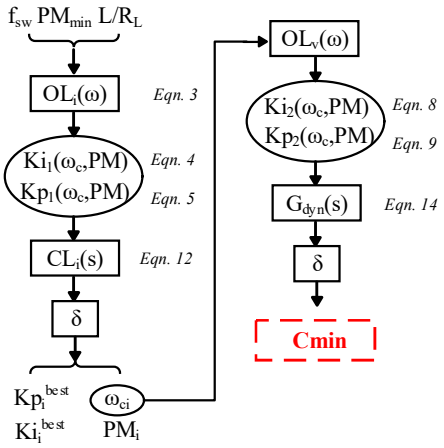


Fig. 3.Minimum capacitance calculation flowchart.

To perform the minimum capacitance identification, the equations that defined the loop control design has been made widespread. The control loop 1 and control loop 2 transfer function expressions that determines the reference tracking and disturbance rejection respectively have been rearranged to more general expressions,

$$\frac{id(s)}{idref(s)} = \frac{Kp_1{}' \cdot \frac{Ti_1 \cdot s + 1}{Ti_1 \cdot s} \cdot \frac{1}{Td \cdot s + 1} \cdot \frac{1}{L/_{R_L} \cdot s + 1}}{1 + Kp_1{}' \cdot \frac{Ti_1 \cdot s + 1}{Ti_1 \cdot s} \cdot \frac{1}{Td \cdot s + 1} \cdot \frac{1}{L/_{R_L} \cdot s + 1}} \tag{12}$$

$$\frac{Vo(s)}{io(s)} = \frac{1}{C} \cdot \frac{s \cdot (T_{CL} \cdot s + 1)}{T_{CL} \cdot s^3 + s^2 + Kp_2{}' \cdot s + \frac{Kp_2{}'}{Ti_v}} = \frac{1}{C} \cdot G_{dyn} \tag{13}$$

Where,

$$Kp_1{}' = \frac{Kp_1}{R_L} \tag{14}$$

$$Kp_2{}' = Kp_2 \cdot \frac{3 \cdot Md}{4 \cdot C} \tag{15}$$

It can be deduced from (14) that the value of the capacitor does not affect the dynamics (i.e., in terms of poles and zeros position). It only affects to the gain of the transfer function Therefore, analyzing G_{dyn} in terms of performance factor σ, the best disturbance rejection dynamics can be identified independently of the capacitance value and the operation point. The best disturbance rejection response that can be expected under f_{sw}, PM and $L/_{R_L}$ ratio constraints can be obtained for a normalized case where i_{load} and the nominal voltage are set to unity. This yields a normalized voltage variation, ΔV_{pu}.

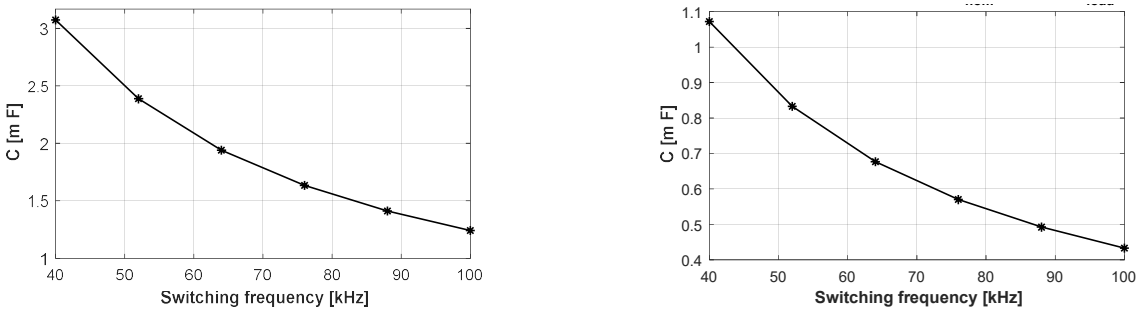
From ΔV_{pu}, the minimum capacitance for any voltage variation ($\Delta V_{required}$, expressed as an absolute value) and any certain current level demand (i_{load}) can be deduced with,

$$C_{min} = \Delta V_{pu} * \frac{i_{load}}{\Delta V_{required}} \tag{16}$$

Capacitance reduction evaluation

The main contribution of this work is the study of the limits of the output capacitance reduction by the action of the classic dual control loop. The capacitance reduction ratio in terms of the base case can be calculated. The base case has been set as energy storage capacitance design to limit a maximum voltage variation for a high current pulse demand of a duration of 2 ms. As mentioned in the introduction section, the obtained data can be also used for proving the effectiveness of more complex control algorithms proposed for capacitance reduction.

Table I specifications and an $L/_{R_L}$ ratio equal to $0.5 \cdot 10^3$ (i.e., as matter of example and based on a preliminary inductor design) have been used for the analysis presented in this paper. Fig. 4.a shows the results for an example in which i_{load} and $\Delta V_{required}$ are set to 1. The results shown in Fig. 4.b can be easily obtained from the case with i_{load} and $\Delta V_{required}$ set to 1, using (16).



(a) (b)

Fig. 4. Capacitance reduction study results. (a)Case where i_{load} and $\Delta V_{required}$ are set to 1 (b) Results particularization for a given operating point (Table I).

To validate the theoretical study results, a simulation has been performed. The simulation has been developed in MATLAB/Simulink software and a good approximation to the real control implementation in a DSP platform was achieved. Simulation and analytical results are compared with good agreement, Fig. 6.

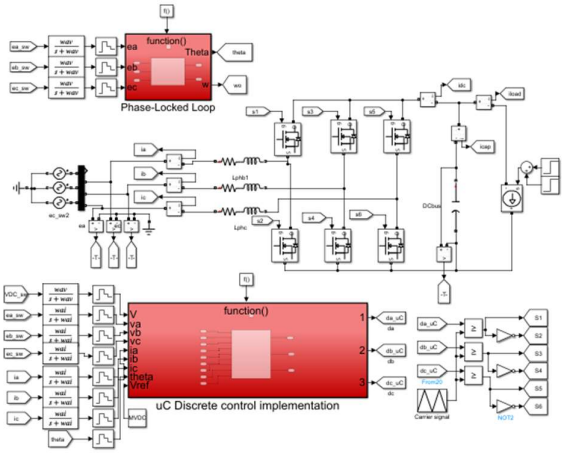
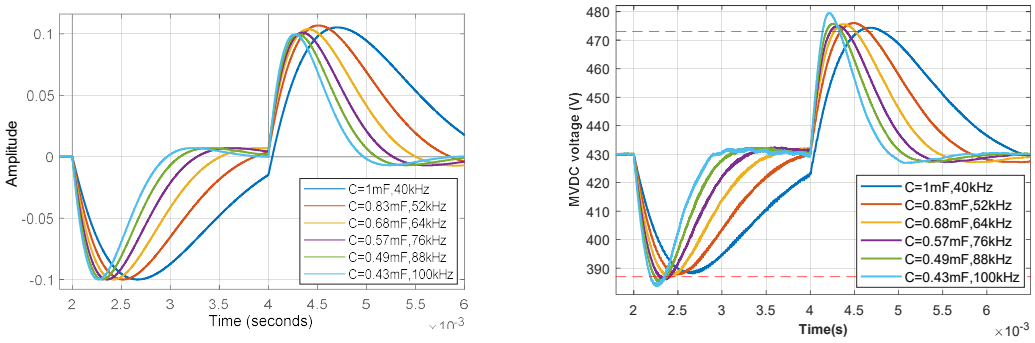


Fig. 5. MATLAB/Simulink discrete system simulation with C-code based control loop implementation.



(a) (b)

Fig. 6.Step response evaluation with the minimum capacitance calculated. Red dashed lines indicate the allowable voltage variation band (a) Theoretical time response, based on (7). (b) PFCVR switching model simulation implemented in MATLAB/Simulink.

Fig. 6.a shows the voltage variation of an equivalent linear system when a current of a unit pulse is demanded and Fig. 6.b displays the voltage variation of the switching model simulation of Fig. *5* for a 150 A pulse current. Finally, Table II illustrates the capacitor reduction ratios for different switching

frequencies when comparing with a purely based energy storage capacitor (C_{base}) under the specifications described in Table I.

Table II. Reduction ratio estimation.

f_{sw} [kHz]	C_{min} [mF] @430V,150A	Reduction ratio [%] (C_{base}= 6.7mF)
40	1.08	83.8
52	0.83	87.6
64	0.68	89.8
76	0.57	91.4
88	0.49	92.7
100	0.43	93.5

Conclusion

Optimization tools to help increase the power density of power converters are a need for the electric mobility market. In this work a methodology to estimate and reduce the size of output capacitor has been shown achieving reduction ratios as high as 93.5%.

The aim of this work is to present a useful methodology for power rectifier weight and volume optimization by identifying the reduction ratio of the output capacitor size by means of traditional control technique. In the case of study presented in this work, reduction ratios higher than 80% were achieved by improving the control dynamics of a three-phase ac-dc converter. As it can be seen in Fig. 4, the capacitance reduction is not linearly related with the switching frequency. The generated data is intended to be useful for evaluating more complex control algorithms focus on the capacitor reduction of PFCVR and voltage source converters in general. Additionally, a combination of these results with the study of the system losses can give a trade-off between losses and power density.

Finally, the proposed methodology for a PFCVR has been demonstrated in MATLAB/Simulink with a discrete model. This model is key in the future work to predict the operation of the prototype to be implemented.

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