# Active du/dt Filtering for Three Phase Motor Drive Applications

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***Abstract*— The performance of modern wide bandgap semiconductors cannot be fully exploited in inverters for motor drive applications, since faster switching is not possible due to the high du/dt causing overvoltages due to reflections on cables and EMI issues. Classical LC filters are also not suitable, as these limit power density. This situation calls for an active du/dt filter implementing intelligent switching transitions of the power semiconductors to ensure high efficiency and low du/dt at the output simultaneously. Theoretically, the modulation scheme can deliver ideal smooth transitions. However, in practical setups non-idealities cause severe oscillations of the resonant tank. This paper studies the origin of this oscillation and proposes a compensation method to successfully reduce the undesired oscillation.**

***Keywords*— *Active du/dt filter, GaN, Inverter, Non-idealities.***

## I. INTRODUCTION

As everyone knows, high efficiency is a standard requirement for most power electronics applications. Of course, this also applies to inverters. A lot of effort is spent in order to make inverters more efficient. One possibility is the implementation of triangular current mode (TCM) modulation that allows ZVS [1] [2]. An extension combines TCM with discontinuous pulse width modulation (DPWM) [3] schemes to reduce the detrimental current ripple required for ZVS [4] [5]. Also modulation methods using sectional constant switching frequencies to minimize the inductor current ripple are known [6].

Inverters using GaN power semiconductors call for adaptive dead time methods so minimize the losses resulting from reverse conduction, which [7] implements for a fixed switching frequency inverter with LC filter. [8] uses an adaptive dead time procedure with a GaN TCM ZVS inverter.

A recent survey publication [9] shows that not only inverter efficiency but also its EMI characteristics become more relevant. [10] gives a differential mode analysis in case of a TCM inverter. Furthermore, there are several methods to reduce the noise spectrum and du/dt present at the output of the inverter [11] [12]. Due to the wave traveling along the cable, which links inverter and motor, an overvoltage at the motor's clamps results when high du/dt is present at the inverter's output. Huge LC filters generating a sinusoidal voltage can be used, but worsen power density due to the large components required. Thus, other methods to tackle these problems are to be found. One possibility is to reduce the switching speed of the semiconductors by placing a gate resistor with high resistance slowing down the gate charging process. However, this contradicts the goal of high efficiency, as it drastically increases switching losses [13] [14].

Thus, du/dt filters represent an alternative solution [15]. Besides reduced peak amplitude at the motor's terminals, also lower high frequency common mode noise is to be expected [16].

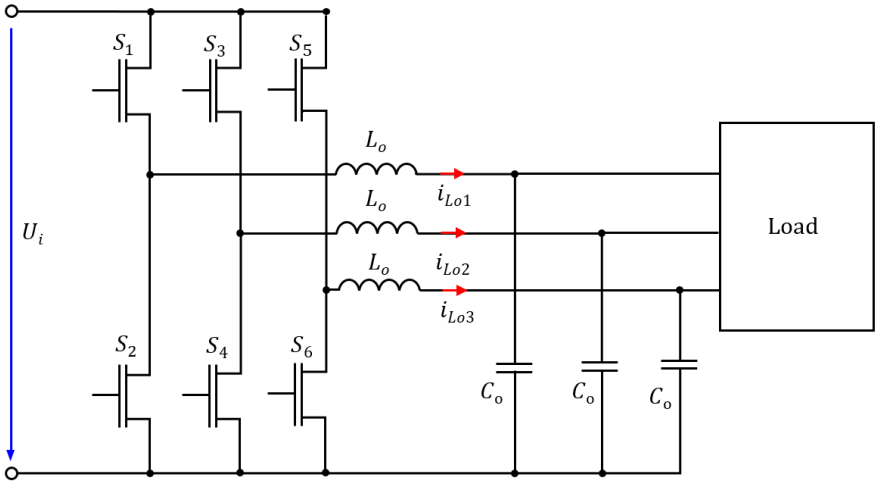


Fig. 1. Three-phase inverter with du/dt filter and load

Therefore, this paper takes up a modulation scheme [15] [17] [18] [19], which theoretically produces smooth output waveforms and principally arbitrary du/dt. It relies on a LC resonant tank and a proper active control of it to deliver piecewise sinusoidal voltage transitions at the inverter's output, where the resonant tank's components set the rise time. The authors identified some problems during practical implementation of this modulation scheme. This paper addresses these issues, analyzes the reasons, and suggests first measures for improvements.

## II. ACTIVE DU/DT FILTER

The active du/dt filter is applied to a three-phase inverter (see Fig. 1), but this paper uses only one half-bridge of a three-phase inverter to explain the modulation scheme. On leg of the inverter (see Fig. 2) comprises an input capacitor $C_i$, a half-bridge made of two GaN power semiconductors, a LC filter and a load. The load models the fundamental frequency impedance of e.g. electrical machines.

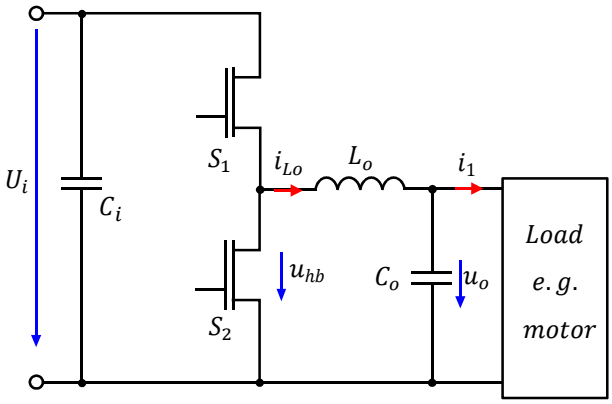


Fig. 2. Half-bridge with LC output filter and load

In order to minimize the high frequency content of the output voltage $u_o$ of the inverter as intended, a proper modulation scheme is required. It steers the LC filter's capacitor voltage in a smooth way to the intended voltage level. The fast switched half-bridge with its semiconductors is only capable of being in two states. In case the upper switch is on, $U_i$ is present at the half-bridge's midpoint. In the other case, the half-bridge voltage is 0. A proper filter component selection for the LC filter together with an active control of the LC filter by the modulation scheme leads to low du/dt at the output of the inverter ($u_o$). The idea of the active du/dt filter is to actively control the capacitor voltage due to a proper pulse train generated by the half-bridge to achieve smooth transitions from 0 to $U_i$ and vice versa.

The modulation method uses the fundamental principle of the LC resonant tank which is built by the filter. A steep voltage slope of the half-bridge voltage $u_{hb}$ causes a resonance in the filter ending in an overvoltage at the filter's output. The modulation method aims at interrupting this resonance to prevent this overvoltage and finally bring the filter's output to the intended value.

In order to analyze the circuit, some assumptions are made. A constant voltage source $U_i$ models the DC-link. Furthermore, the half-bridge is said to be ideal, thus, neglecting switching transitions and the half-bridge's dead time. The filter components are treated to be ideal inductors and capacitors. The load current does not affect the transitions, which is why it is done with $i_1 = 0$. Thus, the circuit is treated as an ideal (lossless) converter without load.

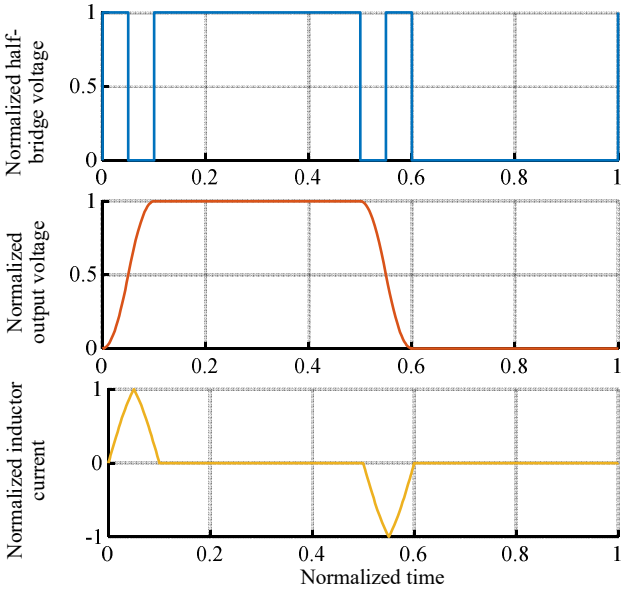


Fig. 3. Fundamental waveforms

The explanation of the modulation scheme refers to the rising edge of the output voltage. The transition begins when with the lower switch conducting. Then, the high side switch turns on, which means $U_i$ is present at the filter's input. The output voltage of the filter follows:

$$u_o = U_i \cdot \left(1 - \cos\frac{t}{\sqrt{L_o C_o}}\right) \qquad (1)$$

Thus, it exhibits a smooth sinusoidal shape. The voltage slope depends on the LC time constant of the circuit determined by $L_o$ and $C_o$. When the output voltage reaches half the input voltage, the upper switch turns off and the lower starts conducting. The corresponding time instant results from:

$$u_o(t_{1/2}) = \frac{U_i}{2} \quad \rightarrow \quad t_{1/2} = \frac{\pi}{3}\sqrt{L_o C_o} \qquad (2)$$

During the phase where the lower switch conducts, the output voltage of the inverter is given by (3).

$$u_o = U_i\left[\left(1 - \cos\frac{t}{\sqrt{L_o C_o}}\right) - \left(1 - \cos\frac{t - t_{1/2}}{\sqrt{L_o C_o}}\right)\right] \qquad (3)$$

At the time instant the output voltage reaches the DC-link voltage, the inductor current has discharged back to $i_{Lo} = 0$. Now, the upper switch turns on again and thus, the resonant tank is in steady-state without any oscillation. The conduction phase of the lower switch also depends on the time constant of the LC resonant tank and equals $t_{1/2}$. After this procedure, the rising edge of the output voltage is successfully completed. Fig. 3 depicts the half-bridge

voltage, the inverter's output voltage, and the inductor current in normalized form for a complete switching period. Fig. 3 also depicts the waveforms of the falling edge, which result from an analogous procedure (switching pattern).

From the theoretical analysis, the rise time of the output voltage is

$$t_r = \frac{2\pi}{3}\sqrt{L_o C_o} \tag{4}$$

and the duty cycle of the signal during rising edge equals $\delta_r = 0.5$. For the falling edge, the same applies.

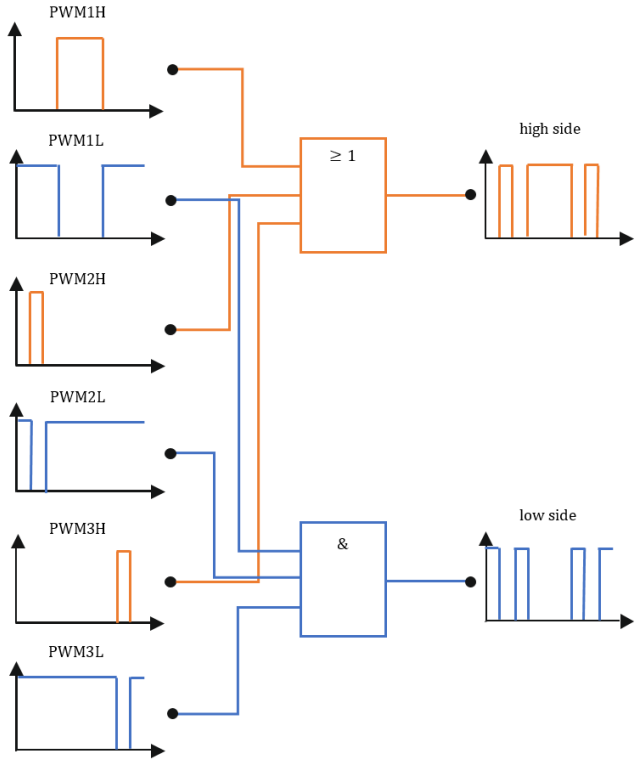


Fig. 4. Gate signal generation by logic gates

The required modulation signal for driving the power switches is a little bit more complicated than for conventional modulation. Fig. 4 visualizes the gate signal generation by using three pulsed signals for each of the power switches (each of the three signals for the high side switch can be used after inversion for the lower switch as well). The high side gate signal results from a three input 'or' gate. A 'and' gate with three inputs combines the signals to get the gate signal for the lower power semiconductor.

With this modulation scheme, theoretically, a smooth output voltage can be achieved.

## III. Experimental Setup

After the theoretical analysis of the modulation scheme, a practical test setup is built. Fig. 5 depicts the PCB of the test setup. The microcontroller generates the gate signals for the power switches. An evaluation board is placed on the power stage's PCB. 100 V GaN power FETs realize the half-bridge switches [20]. In order to avoid nonlinear effects caused by the filter capacitor $C_o$, C0G capacitors instead of X5R or X7R capacitors are used. The filter inductor utilizes a component that can be bought off the shelf.

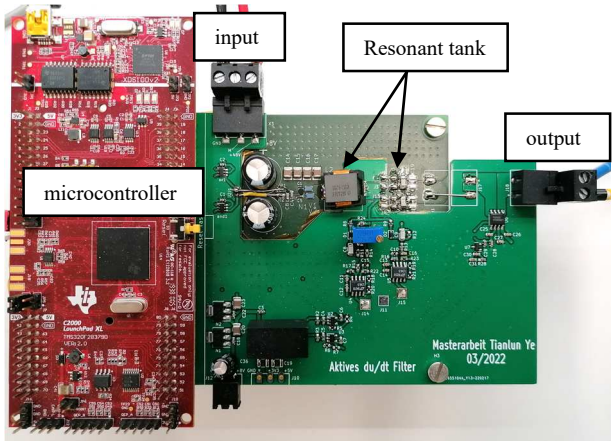


Fig. 5. Photo of the single-phase inverter

The test setup uses the operating parameters given in Table I. The switching frequency corresponds approximately to the switching frequency used with conventional IGBT inverters (10 kHz). During inverter operation, the duty-cycle varies over the sinusoidal period. Here, only one switching cycle and not the complete sinusoidal period is studied to easily analyze the inverter's behavior.

Table I: Operating parameters of the inverter

| Parameter | Value | Parameter | Value |
|---|---|---|---|
| $T_s$ | 100 µs | $\delta$ | 0.5 |
| $\delta_r$ | 0.5 | $t_r$ | ≈1 µs |
| $\delta_f$ | 0.5 | $t_f$ | ≈1 µs |
| $U_i$ | 48 V | $i_{Lo}$ | ≈ 2 A |
| $L_o$ | 2.3 µH | $C_o$ | 100 nF |

Putting the test setup into operation using the parameters mentioned above gives the waveforms shown in Fig. 6. Besides the correct switching pattern of the half-bridge, massive ringing of the output voltage $u_o$ is visible after the switching actions. This oscillation decays only slowly and is therefore still present before the next switching transition of the half-bridge. It is present for the complete conduction phase ($\approx \delta \cdot T_s$) of the upper switch. This oscillation is also visible in the waveform of the inductor current $i_{Lo}$. The resonance frequency present in both waveforms has an oscillating frequency of ≈330 kHz, which matches the resonance frequency of the LC resonant tank. To sum up, the experimental results do not match the expectations of smooth transitions without any ringing.

In order to understand the origin of this unexpected behavior of the experimental setup, we should have a closer look to the switching transitions. Thus, both transitions, the rising as well as falling edge are depicted separately in a zoomed diagram each (Fig. 7 and Fig. 8 respectively). The following explanations refer to the situation shown in Fig. 7, where the rising edge is displayed and the inductor current is exclusively positive. One can see (Fig. 7) that there are short phases (before the

first rising edge ($t_1$-$t_2$), after the first falling edge ($t_3$-$t_4$), and before the second rising edge ($t_5$-$t_6$) of the half-bridge voltage $u_{hb}$), where the half-bridge voltage is slightly negative (≈-2 V). These result from the necessary dead time of the half-bridge [7] [8]. During these short time intervals, the half-bridge voltage is generally not known, but depends on the direction of the inductor current [21]. At the beginning the lower switch conducts and the current flows in reverse direction through the power semiconductor. At the end of its conduction time it turns off. The current through the switch is still negative again forcing it to reverse conduction. Due to the GaN-device's characteristic, the voltage across the switch is ≈-2 V, which explains the negative half-bridge voltage [20]. After the dead time of the half-bridge the upper switch turns on and the half-bridge voltage is 48 V for the conduction phase of the upper switch. After the upper switch has turned off, the inductor current charges the output capacitances of the power semiconductor and the half-bridge voltage drops to zero. The lower power semiconductor conducts again in reverse direction, which leads to the negative voltage. The negative voltage slightly before the second rising edge results from the same origin as at the first edge.

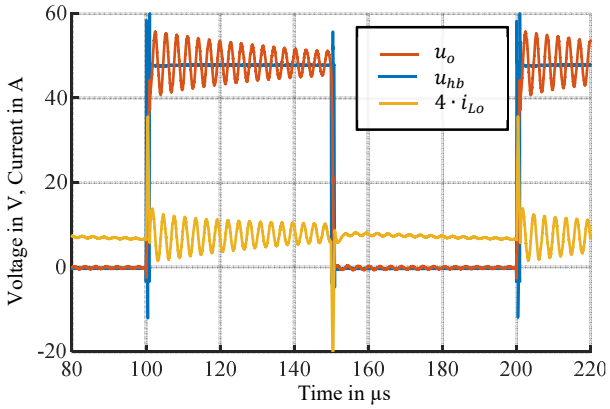


Fig. 6. Waveforms for one switching period gained by the test setup

Thus, if the current is positive, the lower switch is in reverse conduction phase during the dead time. Either this happens directly after the lower one turns off or after the output capacitances of the power semiconductors have been charged. For negative inductor current, the explanations are vice versa.

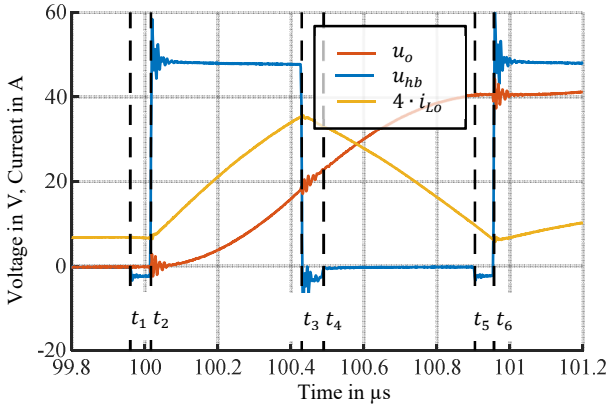


Fig. 7. Waveforms for the rising edge of $u_o$ gained by the test setup

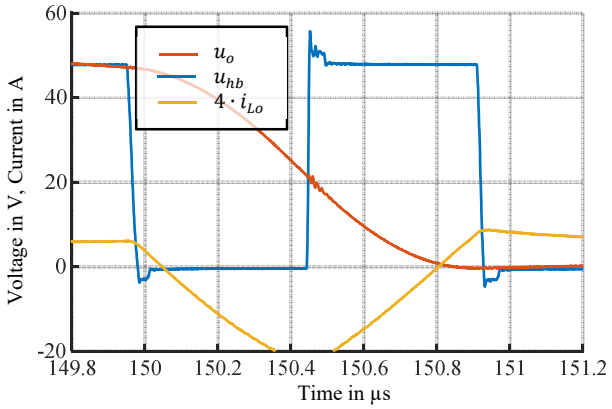


Fig. 8. Waveforms for the falling edge of $u_o$ gained by the test setup

The fact that the half-bridge voltage during dead time is defined by the inductor current's direction leads to the deviation of the half-bridge voltage from the intended waveform. Fig. 9 visualizes this effect schematically for exclusively positive inductor current in an idealized manner. In case of Fig. 7, the volt-second product of the half-bridge voltage pulse (≈100-100.4 µs) is not large enough to bring the inductor current to the intended value. As an result, the charge supplied by the inductor current is not sufficient to raise the capacitor's voltage (output voltage of the inverter) to the intended value of 48 V at the end of the switching pattern (≈101 µs). The resonant tank does not reach its steady state consequently triggering the oscillation visible in Fig. 6. In other words, one can say that the duty cycle present at the LC filter's input equals not the intended one, causing the oscillation.

The explanation for the oscillation after the falling edge of the inverter's output voltage in Fig. 8 is analogous. As Fig. 7 exhibits three phases where the voltage is negative, a huge oscillation results. In Fig. 8, the volt-second product is more balanced leading to a somewhat smaller oscillation amplitude than at the rising edge.

## IV. Optimized Modulation Scheme

Due to the non-ideal behavior of the half-bridge introduced by the dead time, the modulation scheme must be modified. As the non-ideal behavior affects the duty cycle present at the half-bridge voltage, a modified duty cycle must be found to reduce the oscillations within the

circuit. The procedure to gain the optimized duty cycle will be explained using the situation shown in Fig. 7, where the inductor current is positive at all three edges of the half-bridge voltage during the rising edge of the output voltage $u_o$. The procedure is analogous for all other cases of the inductor current. Furthermore, the explanations refer to the rising edge of the inverter's the output voltage, but the falling edge can be handled in the same manner.

For the analysis some assumptions must be made. The first one is that one of the power semiconductor is in reverse conduction state for the complete dead time interval. This assumes infinite steep slopes of the half-bridge voltage, thus neglects the hard switching transients and zero voltage switching transitions. Furthermore, the reverse conduction voltage of the half-bridge power semiconductors (in case of GaN at $u_{GS} = 0$ V it is $\approx$ 2 V [20]) is neglected and set to zero for the analysis. This assumption introduces an error of 2 V/48 V $\approx$ 4 %.

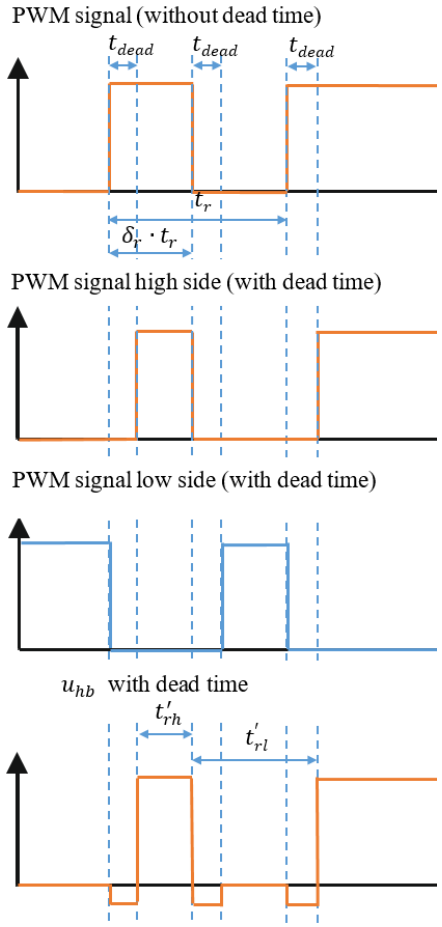


Fig. 9. Dead time insertion in half-bridge; $u_{hb}$ for exclusively positive inductor current

In the first step of the procedure, the voltage waveforms including the non-ideal behavior of the half-bridge must be analyzed. From Fig. 9 and Fig. 7 the duration where the half-bridge voltage exhibits high voltage (in this case equals the conduction phase of the upper switch) can be derived from the ideal duty cycle $\delta_r = 0.5$ and rise time $t_r$ using the dead time $t_{dead}$:

$$t'_{rh} = \delta_r \cdot t_r - t_{dead} = 0.5 \cdot t_r - t_{dead} \quad (5)$$

Fig. 9 demonstrates that $t'_{rh}$ is shortened by the dead time, which is now reflected in the 'high time'. In the same manner, the interval with low voltage including reverse conduction phases is:

$$t'_{rl} = t_r \cdot (1 - \delta_r) - t_{dead} + 2 \cdot t_{dead} \quad (6)$$

Compared to the ideal time interval, this time is now extended by the dead time. Setting $\delta_r = 0.5$ gives:

$$t'_{rl} = 0.5 \cdot t_r + t_{dead} \quad (7)$$

(8) gives the effective duty cycle, which results from the quotient of the effective 'high time' and the sum of the effective 'high time' and 'low time'.

$$\delta'_r = \frac{t'_{rh}}{t'_{rh} + t'_{rl}} = \frac{0.5 \cdot t_r - t_{dead}}{t_r} = 0.5 - \frac{t_{dead}}{t_r} \quad (8)$$

Subtracting the effective duty cycle $\delta'_r$ (resulting from the non-ideal behavior) from the ideal one $\delta_r$ gives the duty cycle error $\tilde{\delta}_r$:

$$\tilde{\delta}_r = \delta_r - \delta'_r = \frac{t_{dead}}{t_r} \quad (9)$$

In order to compensate the duty cycle error $\tilde{\delta}_r$ caused by the non-ideal behavior of the half-bridge, it is added to the intended duty-cycle:

$$\delta''_r = \delta_r + \tilde{\delta}_r = \frac{0.5 \cdot t_r + t_{dead}}{t_r} \quad (10)$$

Looking now at the other edge of the output voltage (Fig. 8), it becomes clear that at the falling edge of the output voltage, the current is positive (+) at the first edge of the half-bridge voltage, negative (-) at the second edge, and positive (+) at the third edge. This is why the short designation (+-+) results here. Thus, (11) is valid for the duty cycle of the falling edge $\delta''_f$.

$$\delta''_f = 0.5 \quad (11)$$

Now the equations for determining the optimized duty cycles $\delta''_r$ and $\delta''_f$ are ready to be implemented in the digital controller. Instead of using $\delta_r$ and $\delta_f$ for the implementation, now, (10) and (11) should be used.

The computational effort within the digital control circuit is a major criterion for modulation schemes. Of course, the calculation of the modified control parameters requires a higher computational effort, but this method will improve the quality of the output waveforms.

In order to verify this, the experimental setup is now operated with the modified parameters.

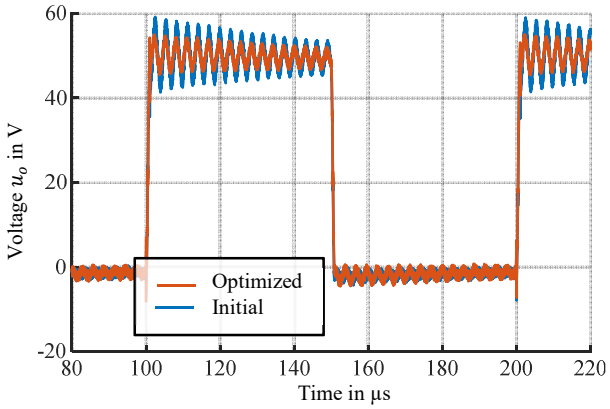


Fig. 10. Comparison of $u_o$ for the initial parameters and the optimized parameters for one switching period gained by the test setup

For the derived parameters ((10) and (11)) Fig. 10 depicts the resulting output voltage ('Optimized'). To evaluate the improvement by the modified modulation scheme, the waveform gained by the initial modulation scheme (section II) neglecting the non-ideal behavior is also depicted in Fig. 10 (denoted as 'Initial', copied from Fig. 6).

So far, only the case (+++) for the rising edge of the output voltage and the case (+-+) for the falling edge have been considered. All other combinations that may occur in a practical setup can be analyzed in the same way. Table II and Table III summarize the results for the corresponding cases, separated to the rising and falling edges of the output voltage.

Table II: Optimized duty cycle $\delta_r''$ for the rising edge

| $u_{hb}$ | | | | $\delta_r''$ |
|---|---|---|---|---|
| Sign of inductor current $i_{Lo}$ | + | + | + | $\frac{0.5 \cdot t_r + t_{dead}}{t_r}$ |
| | 0 | + | 0 | $\frac{0.5 \cdot t_r + t_{dead}}{t_r}$ |
| | - | + | - | 0.5 |
| | - | 0 | - | $\frac{0.5 \cdot t_r - t_{dead}}{t_r}$ |
| | - | - | - | $\frac{0.5 \cdot t_r - t_{dead}}{t_r}$ |

Table III: Optimized duty cycle $\delta_f''$ for the falling edge

| $u_{hb}$ | | | | $\delta_f''$ |
|---|---|---|---|---|
| Sign of inductor current $i_{Lo}$ | + | + | + | $\frac{0.5 \cdot t_f - t_{dead}}{t_f}$ |
| | + | 0 | + | $\frac{0.5 \cdot t_f - t_{dead}}{t_f}$ |
| | + | - | + | 0.5 |
| | 0 | - | 0 | $\frac{0.5 \cdot t_f + t_{dead}}{t_f}$ |
| | - | - | - | $\frac{0.5 \cdot t_f + t_{dead}}{t_f}$ |

Fig. 10 shows that the modified modulation scheme reduces the oscillations, but the output voltage is not as smooth as expected based on the theoretical analysis. The improved modulation scheme still exhibits oscillations, which stem from other non-idealities within the half-bridge circuit. This can be, for example, losses within the converter or switching transitions of the half-bridge.

## V. Discussion

The modulation method taken up here is a good possibility to reduce the harmonic content of the output voltage and reflections on the motor cable. Theoretically, it delivers smooth, oscillation free output waveforms, but measurements in a practical setup show, that non-idealities of the inverter worsen the results. Therefore, the next step is to compensate the negative effect of the dead time on the output voltage with this modulation scheme. This procedure (shown in section IV) reduces the filter resonance. However, oscillations still remain. To further reduce these, a control algorithm should be used to optimize both the duty cycle and the rise (fall) time. An algorithm like a maximum power point tracking (MPPT) algorithm in combination with a peak detector circuit for the output voltage can be used to find the control parameters which feature the lowest oscillations.

A few notes should be left regarding the losses within the inverter. Assuming a trapezoidal output voltage waveform with a given rise time $t_r$ (e.g. 1 µs), an inverter using a conventional modulation scheme needs to turn on the power semiconductors (e.g. IGBTs) relatively slow to ensure a low du/dt (long rise time) of the output voltage. The resulting turn-on energy is $E_{on} = 0.5 \cdot t_r U_i i_1$, which is the reference. In order to be able to use the modulation method presented here sensibly, the losses that occur must be lower than the reference just mentioned. The proposed modulation scheme in combination with GaN switches allow extremely fast voltage transitions ($< 10$ ns) and thus, lower losses than the reference. However, in the worst case, during the rising edge of the output voltage, two lossy switching actions occur using the modulation method discussed here (the third switching operation features ZVS). In addition losses occur in the inductor and the capacitor of the LC resonant tank. Thus, the sum of the semiconductor's losses and those occurring within the LC filter must be smaller than the losses of the power switches' of the reference design featuring slow turn-on transitions.

This method combines smooth output waveforms with low du/dt like those from classical IGBT inverters and fast switching GaN-devices by implementing a proper modulation scheme. Thus, the world outside the inverter sees only the slow edges (low du/dt) generated by the du/dt filter and the low switching frequency like known from conventional IGBT inverters. Nevertheless, the proposed inverter benefits from the low on-state resistance and low switching losses provided by GaN.

## VI. Conclusion

This paper takes up a modulation scheme using a properly designed LC resonant tank (filter) in combination with an active control of it to reduce the du/dt of the inverter's output voltage. The low switching losses associated with the use of GaN allow the beneficial implementation of this modulation scheme, which requires multiple switching operations to produce smooth output

voltage waveforms. The theoretical analysis using an ideal inverter promises smooth waveforms, but a prototype using the modulation scheme shows issues occurring in practical implementations, which result in oscillations of the output voltage. Compensating the impact of the dead time on the waveforms improves the results, but still oscillations remain. In future, a control algorithm (like MMPT) reducing the remaining oscillations should be implemented. Furthermore, a loss analysis and EMI evaluation should follow.

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