Investigation of an Interleaved Current-Fed Single Active Bridge DC-DC Converter for PV Applications

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Keywords

≪DC-DC converter≫, ≪Dual Active Bridge (DAB)≫, ≪Soft switching≫, ≪Design optimization≫, ≪Singel Active Bridge≫

Abstract

The increase in efficiency of photovoltaic inverters is the subject of many researches and in particular losses of semiconductors and magnetics have to be reduced. This topology follows the approach of a combined interleaved boost converter and a series resonant converter (SRC). In addition, it differs from the dual active bridge topology due to the non-synchronous rectification with less control effort.

Introduction

For the application of boosting a PV voltage level, a usual topology, which is composed of two stages, the interleaved boost converter, and the series resonant converter, is simplified to an interleaved current-fed single active bridge (CF-SAB). The amount of active components is significantly reduced by half while also reducing the overall conduction and switching losses in these elements. Also, a DC blocking capacitor is no longer necessary in the configuration due to the control approach. There are also many studies about similar topologies, such as the CF-DAB (current-fed dual active bridge). In [1]-[4], this topology and various operating points are discussed, comparing the results for different phase shifts between the two active bridges, as well as using different duty cycles in each bridge and mapping the power and zero voltage switching (ZVS) boundaries for every operating point. Different approaches to control these converters are presented in many studies, like using the voltage across the clamping capacitor [3], complex control systems [4], [5], or discrete-time modelling [6]. Related topologies were used to achieve DC-DC conversion in a similar way, like using additional switches and capacitors to avoid voltage spikes and to achieve ZVS [7], using double half-bridges [8], in which one leg is active and one is composed by only two capacitors as well as a three-port converter [9], using two active bridges of three legs each. This paper discusses the approach for loss reduction by combining the two full bridges of the boost converter and the series resonant converter into one shared full bridge. The differences are worked out and the advantages and disadvantages are discussed. A comprehensive analysis of the overall system is given in the following chapter and a first design of the prototype is presented afterwards.

Topology Description

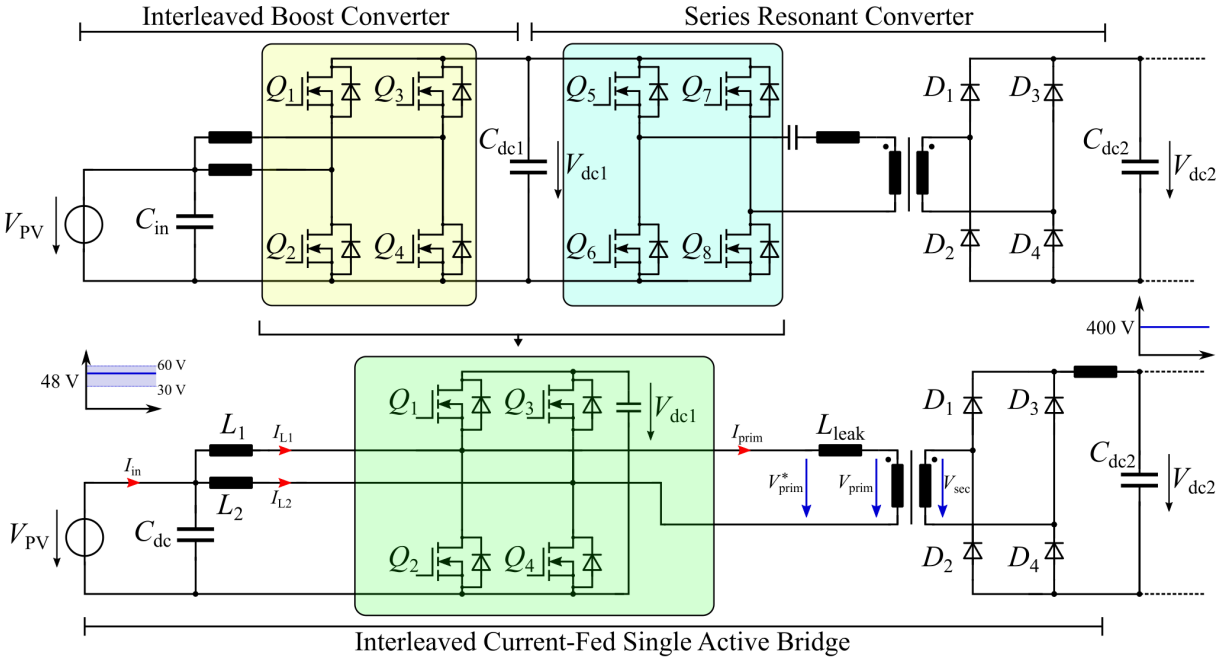


Fig. 1: Circuit description of the conventional two stage topology (top) in comparison to the combined interleaved current-fed single active bridge (bottom).

In Fig. 1 a comparison of the proposed topology to the conventional two stage topology is given. In this study, two operating points with the same output conditions are analyzed to show the degrees of freedom regarding the duty cycle and phase shift. First, a fixed phase shift of 180° is selected to reduce the input current ripple, followed by a phase shift of 120° to achieve a switching state where both low side switches are turned on at the same time which is initially not possible at a phase shift of 180°, since a duty cycle above 50 % would no longer meet the output requirements, even with the lowest input voltage of 30 V. For this research a constant input voltage of 48 V is selected, which is within the typical output voltage range of PV modules. The output voltage is set to 400 V at 1 kW output power and will be achieved by the boost characteristic of the proposed topology as well as the transformer winding ratio of $n = 8$. The resonant components can be eliminated since zero voltage switching (ZVS) can be achieved with the help of the boost inductors. In summary, the number of required MOSFETs is halved, switching and conduction losses are reduced and the more complex resonant component design is not required.

In Fig. 2 and Fig. 3 the main waveforms of the topology are shown. The switches Q_1 and Q_2 are complementary to each other as well as Q_3 and Q_4. It is possible to change the duty cycle D and the phase shift ϕ between the switching signal of the two legs, unlike previous studies [4], [5], in which the phase-shift is made between the active bridges of the primary and secondary side. The proposed converter has four possible switching states, however, which are not reached at every operating point within one period. The equivalent circuit diagram of each switching state is shown in Fig. 4 and only the active paths are highlighted. The four stages of operation are described as follows.

Stage I: Q_1 and Q_4 are active

Starting from the boost converter characteristic, the input voltage U_{PV} is applied to L_2 through the switched-on MOSFET Q_4, which increases the current I_{L2} through the inductor, and the energy will be stored in the magnetic field. Since the capacitor C_{dc1} is discharging, shown in Fig. 4 (a), the current I_{prim} of the primary side of the transformer is increasing. The voltage V^*_{prim} across the transformer is defined by the boost voltage V_{dc1}, which is in parallel during this state.

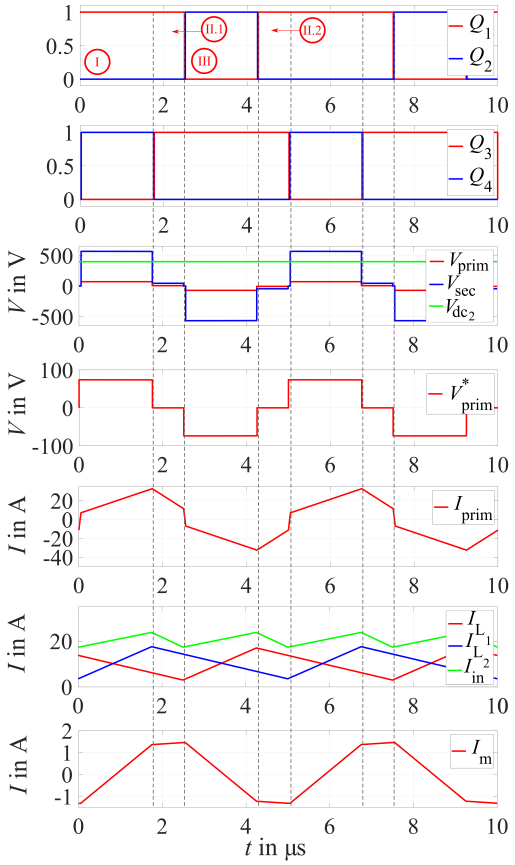


Fig. 2: Main waveforms of the proposed topology taken from the simulation @ $V_{PV} = 48\,V$, $V_{dc2} = 400\,V$, $P_{out} = 1\,kW$, $\phi = 180°$ and $D = 0.35$.

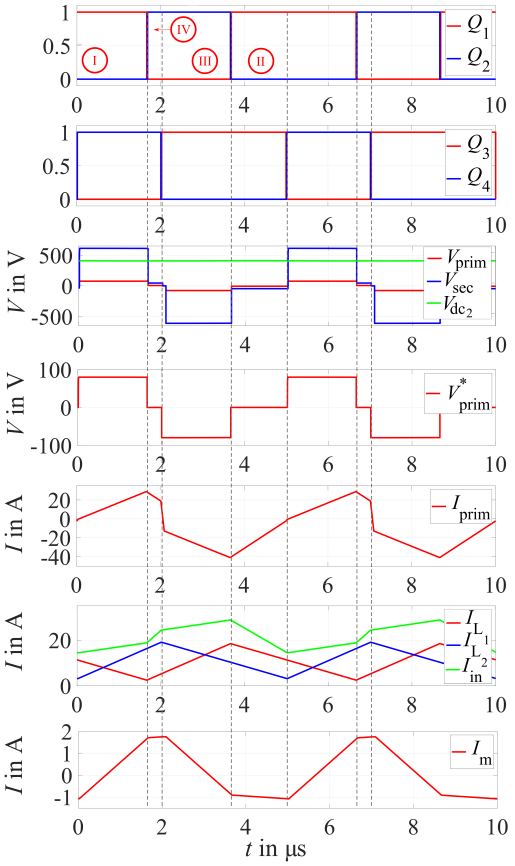


Fig. 3: Main waveforms of the proposed topology taken from the simulation @ $V_{PV} = 48\,V$, $V_{dc2} = 400\,V$, $P_{out} = 1\,kW$, $\phi = 120°$ and $D = 0.40$.

Stage II: Q_1 and Q_3 are active

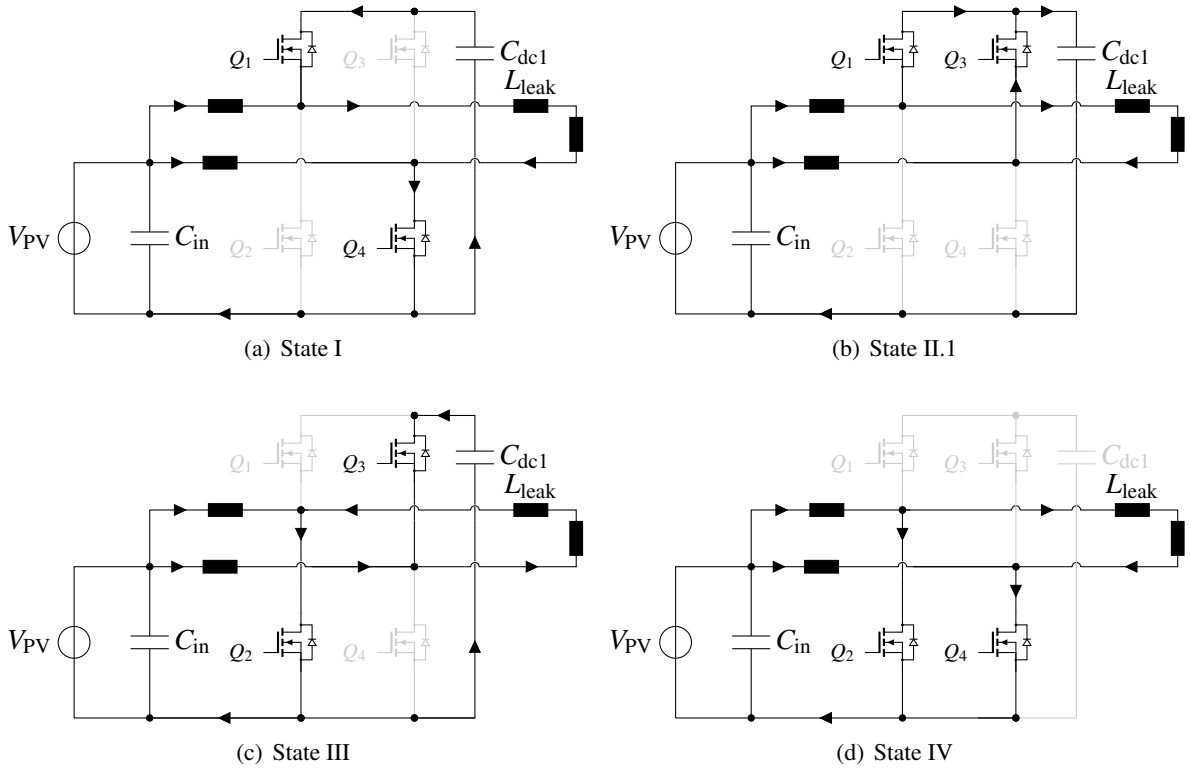
State II can be divided into states II.1 and II.2 depending on the current direction of I_{prim} which is in the first stage positive and due to the previous state of II.2 negative. Both inductors L_1 and L_2 maintain the current flow due to the previously stored energy and are decreasing over time which has the same effect on the primary side current. Since both winding endings are connected to V_{dc1} the voltage drop V^*_{prim} is zero as a result of which the magnetizing current remains nearly constant.

Stage III: Q_2 and Q_3 are active

State III corresponds to the inverted state II. The voltage at the transformer V^*_{prim} has reversed, causing the magnetic field to be excited in the negative direction by the magnetizing current. C_{dc1} is discharged again after being charged in the previous state. It can be observed that there exists a small voltage drop across the leakage inductance L_{leak}, which leads to a small plateau in the secondary-side voltage V_{sec}. Vice versa, the current and voltage characteristics of L_1 are comparable to the properties of a traditional boost converter.

Stage IV: Q_2 and Q_4 are active

State IV only appears if phase shift and duty cycle allow the two low side gate signals to overlap. However, this is the case with a phase shift from about 120° or less. In comparison to switching state II, the voltage at the transformer is also zero in this case. Because the magnetic field in the transformer is no longer symmetrical, there is an offset in the magnetizing current.



(a) State I (b) State II.1

(c) State III (d) State IV

Fig. 4: The various switching states of the converter.

Since it is possible to achieve the same initial conditions with different operating points, symmetrical loading of the components is recommended. The asymmetry observed in Fig. 3 leads to a DC current offset in the amount of 8 A. Likewise, the higher input current ripple leads to an additional load on the input capacitors and the associated shorter service life.

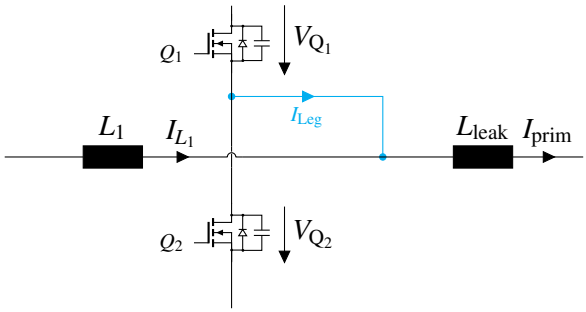
Zero Voltage Switching Analysis

Before analyzing the zero voltage switching possibilities of the presented topology, the soft switching conditions of the conventional topology from Fig. 1 will be analyzed. Here, soft switching for the respective stage must be differentiated.

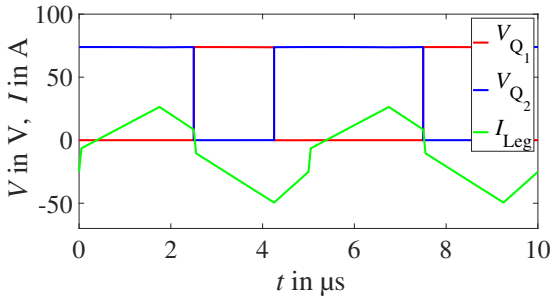
In the case of the boost converter, ZVS at turn-on without an additional network can only be realized by using a sufficiently low inductance value so that the current ripple reaches its negative value before switching on in order to discharge the output capacitor C_{OSS} of the low-side switches. The high-side switches are soft-switched by topology. Likewise, research on ZVS was carried out with the help of auxiliary circuits [10], [11], [12].

In resonant topologies like the SRC ZVS can be achieved by setting the switching frequency above or slightly below the resonant frequency [13]. In the first case, the transformer current is discharging C_{OSS} due to the lagging behavior of the current. In the second case, only the magnetizing current is present during the turn-on transition. The magnetizing inductance should be small enough to achieve a sufficiently high enough peak value of the magnetizing current to discharge C_{OSS} during the dead-time, resulting in a more complex transformer design even if the leakage inductance will be used as resonant inductance.

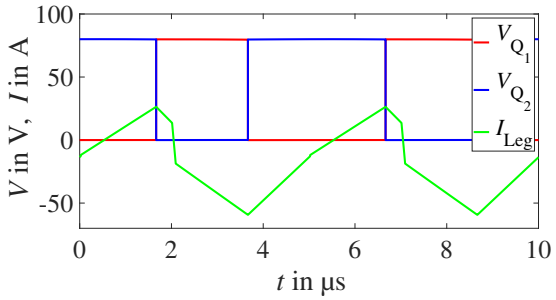
For visualizing the possibility of soft-switching, Fig. 5 is representing one leg of the converter as well as the voltage and current waveforms. In order to achieve ZVS, the antiparallel diode of the MOSFET must conduct at the moment the switch will be turned on so that only the forward voltage of the diode in the switching moment is present. That means, if the switch Q_1 is turned on, the current I_{Leg} must be lower than zero, respectively when Q_2 is turned on, the current needs to be higher than zero to realize ZVS. As



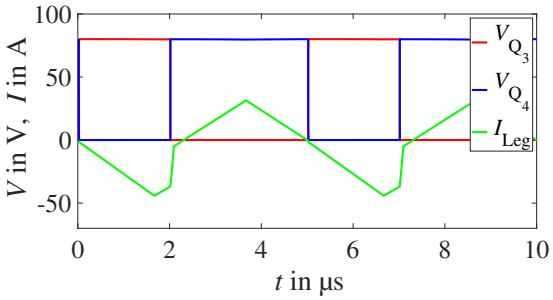
(a) Circuit diagram analysis of one half bridge.



(b) Waveforms analysis of the drain-source voltage drop and leg current with $D = 0.35$ and $\phi = 180°$. ZVS is achieved in all switches.



(c) Waveforms analysis of the drain-source voltage drop and leg current with $D = 0.40$ and $\phi = 120°$. ZVS is only achieved in Q_1, Q_2 and Q_3 (c).



(d) Waveforms analysis of the second leg, with its drain-source voltage drop and current, with $D = 0.40$ and $\phi = 120°$. ZVS is not achieved in Q_4.

Fig. 5: Depiction of soft switching analysis. ZVS in Q_2 is achieved when I_{Leg} is positive before the turn-on transition to discharge the output capacitor and same switching behavior for Q_1 vice versa.

long as the conditions in equation 1 and 2 are given for the respective switch, ZVS is achieved. Since switching state III preceeds the switch-on moment of the Q1 at a phase shift of 180°, the primary current I_{prim} in equation 1 has a negative polarity and the inductor current I_{L1} is at its maximum. Therefore, the switching operation of Q_1 is always soft-switching and Q_3 vice versa. Fig. 5 (d) shows an example in which the ZVS condition for Q_4 from equation 2 is not fulfilled, so that due to the phase shift the leg current I_{Leg} in the switching moment is zero.

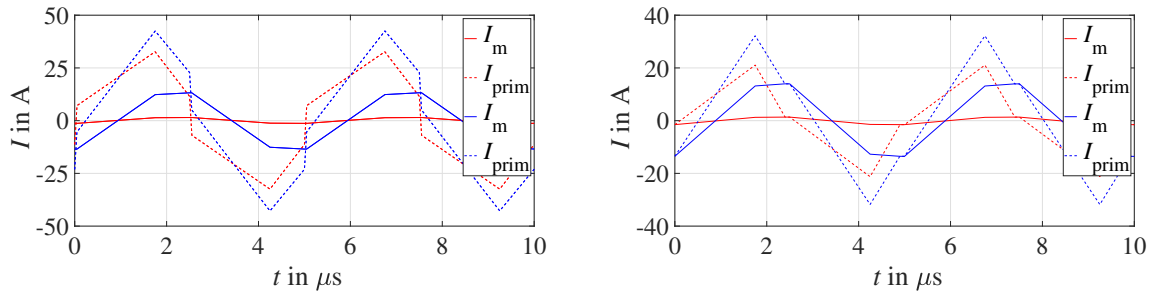
$$Q_1: \quad I_{\text{prim}} - I_{\text{L1}} < 0 \qquad Q_2: \quad I_{\text{prim}} - I_{\text{L1}} > 0 \tag{1}$$

$$Q_3: \quad -I_{\text{prim}} - I_{\text{L2}} < 0 \qquad Q_4: \quad -I_{\text{prim}} - I_{\text{L2}} > 0 \tag{2}$$

Transformer Design

For the design of the transformer, the influence of the magnetizing inductance on the primary current is investigated in Fig. 6 for full load and half load conditions to achieve discontinuous conduction mode (DCM). The plateau which occurs in DCM operation is mainly defined by the magnetizing current and can lead to increased DC losses in the circuit. To achieve ZVS in the SRC, the inductance would be chosen to be 4.5 µH to achieve a large enough magnetizing current to discharge C_{OSS} [13]. Since this criterion does not have to be fulfilled in the proposed topology, a significantly higher magnetising inductance can be chosen, which reduces the maximum amplitude of the primary current.

Based on the waveforms in Fig. 2 and Fig. 3 a transformer is designed by using the simulation software Frenetic, which artificial intelligence based algorithm offers several design recommendations. As a result, a PQ40 core with 3C97 ferrite material was chosen with overall losses of about 6.7 W. All parameters a given in Table I and the winding scheme is shown in Fig. 7. In order to reduce the winding



(a) Continuous conduction mode @ 1 kW output power

(b) Discontinuous conduction mode @ 500 W output power and $D_{Q2,4} = 0.35$

Fig. 6: Influence of the magnetizing inductance for a future design of the transformer. Red: $L_m = 45\,\mu H$, blue: $L_m = 4.5\,\mu H$.

Table I: Simulation results of the transformer design.

Core type	PQ 40	
Core material	Ferrite 3C97	
Air gap	0.64 mm	
Copper filling factor	78.1 %	
Number of turns	6 (prim.)	48 (sec.)
Winding type	Litz wire	
Winding geometry	512 x 0.05 mm	100 x 0.1 mm
Parallel windings	3 (prim.)	none (sec.)
Inductance	49 μH	
Core losses	0.55 W	
Winding losses	1.96 W (prim.)	4.17 W (sec.)
DC resistance @ 20 °C	3.3 mΩ (prim.)	129 mΩ (sec.)

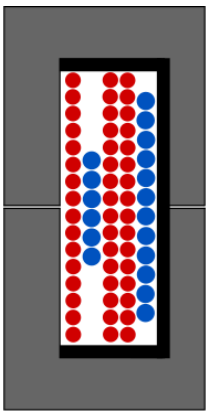


Fig. 7: Winding arrangement in one winding window of the transformer. The primary winding is marked in blue.

losses on the primary side, three primary windings are connected in parallel. Due to the lower current on the secondary side, this is not necessary. A small air gap is necessary to avoid saturation effects.

Component Specification and Hardware Setup

The hardware setup is shown in Fig. 8 and represents only the primary side of the overall prototype, which contain one half-bridge with boost inductor. For a compact design and at the same time easy exchange of the components or to measure different assembly options, each half bridge with its boost inductor is designed separately, so that two of the boards shown are necessary. The gate driver allows stand-alone operation but also enables control by a microcontroller. A sensing resistor prevents an unwanted high current rise within a half bridge as well as providing a symmetrical current distribution in each half bridge. A solder pad is provided for connecting one primary side winding end of the transformer. The secondary side of the transformer is connected to a common full-bridge diode rectifier, which is not shown here. Regarding the voltage ratings of the power semiconductors, 100 V Si MOSFETs from Infineon's OptiMOS series are selected and 650 V SiC Schottky diodes for the rectifier stage.

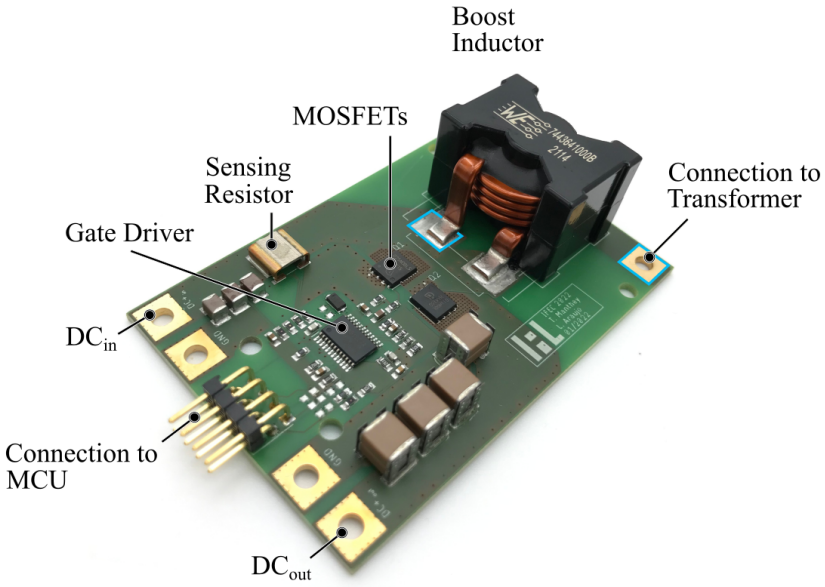


Fig. 8: Photograph of the hardware prototype. The two solder pads highlighted in blue are identical to the blue path of the current I_{Leg} marked in Figure 5 (a). Two of these PCBs form the overall system of the primary side.

Conclusion

This paper presents the investigation of a current-fed single active bridge as a combined topology of boost converter and series resonant converter at 1 kW output power and a boost operation from 48 V up to 400 V. The focus is on the analysis of different switching states and the possibilities for controlling the presented topology on the basis of two different operating points. In addition, a condition for soft-switching possibilities was developed and contrasted with the two stage topology.
Although no harmonics could be detected in the simulation model, oscillations occurred in the hardware setup, which spread to the transformer voltage, drain-source voltages as well as gate signals, it was not possible to show measurements of the operating points shown in this paper until the end of this work.

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