A Study of Non-Isolated Resonant Step-Down Converter with Peak Charge Control for High Power Density

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***Abstract*— Non-isolated resonant converter with peak charge control for high power density is studied in this paper. Step-down converter is required for system on chip (SoC) operation. Buck converter is mainly used, and many studies have been conducted to improve power density by reducing the size of converter. Increasing the switching frequency of converter can contribute to the size reduction. Therefore, class D/E resonant converter suitable for high-frequency operation due to zero voltage switching (ZVS) is chosen as a step-down converter instead of conventional hard switching buck converter. Furthermore, the output capacitor ripple current-based peak charge control and adaptive voltage position (AVP) are simultaneously applied to the class D/E resonant converter. Based on this control method, the size of passive components can be further minimized. The operation of converter with peak charge control and AVP is shown by simulation. Finally, comparison of passive component values according to topology and control method is provided.**

Index Terms*—Class D/E resonant converter, zero voltage switching (ZVS), adaptive voltage position (AVP), peak charge control.

I. INTRODUCTION

System on chip (SoC) refers to a system in which semiconductor devices are configured as one chip. As the functions of mobile devices such as portable device and laptop become more diverse, the use of SoC is expanding because various information can be processed in one chip. The increase in the degree of integration due to SoC has the advantage of contributing to the miniaturization of the system. Recently, the importance of SoC is emphasized in vehicles according to increasing need for processing numerous information due to development of autonomous driving technology.

Stable power supply is essential for proper operation of the SoC. Fig. 1 shows the general structure for SoC operation. The power required for SoC is mainly supplied from the low voltage (LV) battery. Since the LV battery voltage is higher than the voltage for operating SoC, step-down converter is required to lower the battery voltage. Generally, buck converter has been widely used due to the simplicity of design and control [1]-[4]. In order to meet the demand for miniaturization of the device according to high power density, the size of converter should be reduced. Increasing the switching frequency can lower the

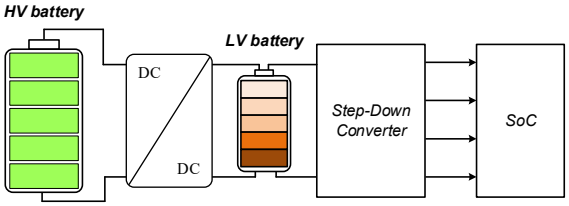

Fig. 1. General structure for SoC Operation.

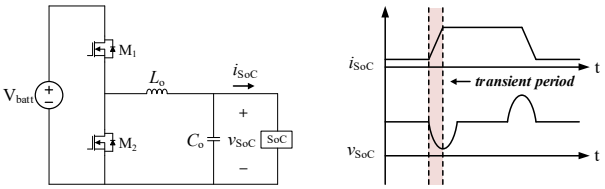

Fig. 2. (a) Conventional buck converter for SoC operation, (b) voltage and current waveforms of SoC.

overall values of passive components, which results in size reduction. However, there is a limit to increasing the switching frequency considering the loss caused by the hard switching of the switches consisting of the buck converter. Furthermore, there is a problem of increasing duty losses due to the turn-on and turn-off times of switch as the operation frequency increases. Therefore, another topology suitable for high frequency operation for size reduction is needed.

Fig. 2 shows conventional buck converter for SoC operation and key waveforms. Voltage spikes occur in the transient period where the SoC load current (i_{SoC}) changes rapidly, various control methods have been applied to handle this problem [2]-[7]. Adaptive voltage position (AVP) is to control the voltage (v_{SoC}) level according to the load current variation. This method can contribute to fewer output capacitors, which results in size reduction of buck converter [2]. V^2I_C control scheme is based on the peak current mode control of ripple current flowing through the output capacitor. Fast dynamic response under transient period can be achieved using this scheme [6]. Furthermore, the output capacitor value can be reduced, assuming the same voltage spike design under a change in load current.

In this paper, non-isolated resonant converter with high frequency operation is adopted for size reduction of

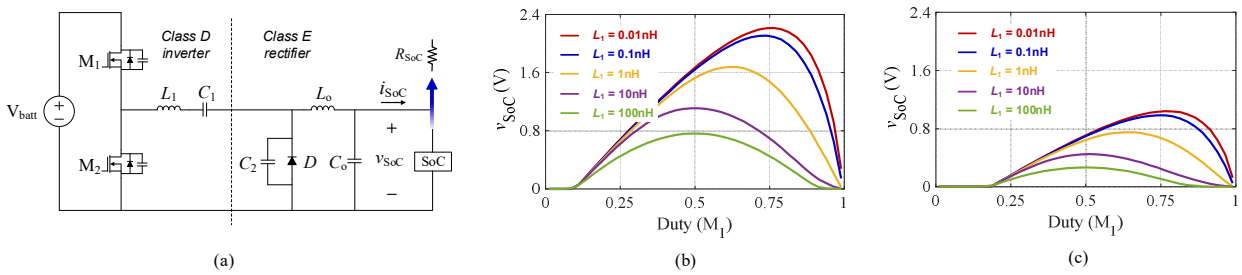

Fig. 3. (a) Class D/E resonant converter, (b) SoC voltage range according to L_1 value and duty variation at battery voltage of 5 V for fixed resonant frequency, (c) SoC voltage range according to L_1 value and duty variation at battery voltage of 2.7 V for fixed resonant frequency.

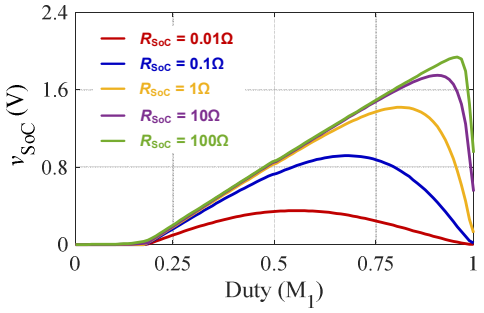

Fig. 4. SoC voltage range according to equivalent SoC resistance (R_{SoC}) value and duty variation at battery voltage of 5 V for fixed resonant frequency.

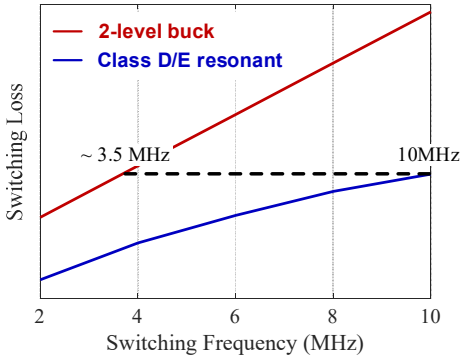

Fig. 5. Switching loss tendency comparison of buck converter and class D/E resonant converter depending on the switching frequency variation.

converter. Switching losses of resonant converter can be reduced due to ZVS [10], [11]. Therefore, high frequency design is possible compared to buck converter under the same switching losses. AVP and ripple current-based peak current control are simultaneously applied to non-isolated resonant converter. It can further minimize the output capacitor value. Difference in peak current control design between the buck converter and the resonant converter is provided. Peak current control for resonant converter is called peak charge control in this paper. Buck converter and resonant converter are designed for each switching frequency with the same switching loss. The values of passive components constituting two designed converters are compared. Also, the values constituting the resonant converter according to the control method based on the same SoC current and voltage during transient period are compared.

II. Non-Isolated Resonant Converter

Class D/E non-isolated resonant converter is chosen as a step-down converter in this paper. Class D/E resonant converter has a two-stage configuration which consists of class D inverter that converts DC battery power to AC power and class E rectifier that converts AC power to DC power required by SoC [8], [9]. In class D inverter, the resonant frequency (f_r) is defined as follows:

$$f_r = \frac{1}{2\pi\sqrt{L_1 C_1}}. \quad (1)$$

ZVS based on the inductive region operation can be implemented by designing the switching frequency of class D inverter higher than the resonant frequency. Therefore, the switching losses can be reduced by eliminating the turn-on loss with the help of ZVS. In other words, the class D/E resonant converter can be designed with higher switching frequency than buck converter with the same switching losses as shown in Fig. 5. The switching frequency of buck converter, which has the same switching loss as class D/E resonant converter operating at 10 MHz, is approximately 3.5 MHz. Thereby, the overall passive component values can be reduced by high frequency design.

Duty ratio of each switch is fixed in [8], [9]. However, a wide range of SoC voltage can be realized by the pulse width modulation (PWM) method under the assumption that the upper and lower switches are complementarily operated. Furthermore, the SoC voltage range varies depending on the change in the L_1 value constituting the class D inverter for the fixed resonant frequency. Therefore, optimal L_1 value can be designed based on the battery voltage and the SoC required voltage range. Fig. 4 shows the SoC voltage range according to the equivalent resistance (R_{SoC}) value and duty variation. Compared to buck converter, wider SoC voltage range cannot be designed. However, a small SoC voltage can be realized with a larger duty for the same battery voltage. Since the required SoC voltage is generally much lower than the battery voltage, class D/E resonant converter has an

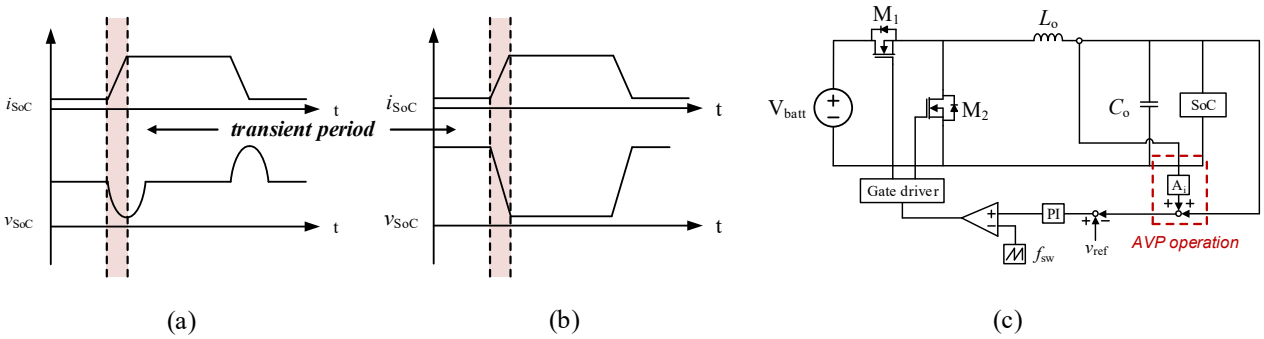

Fig. 6. Current and voltage waveforms of SoC (a) without AVP, (b) with AVP, (c) buck converter with AVP control method.

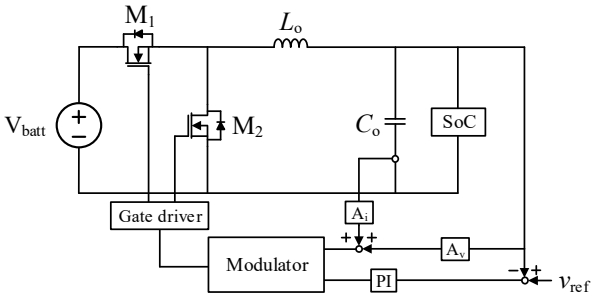

Fig. 7. V^2I_C applied buck converter.

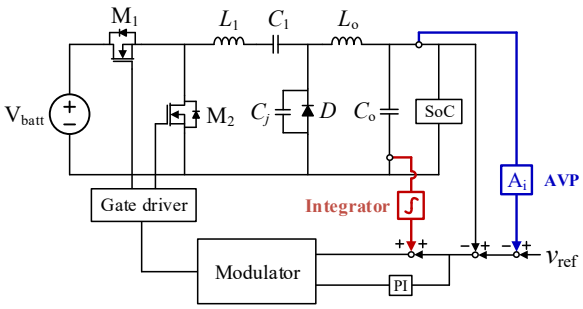

Fig. 8. Class D/E resonant converter with AVP and proposed integrator-based peak charge control.

advantage of reducing the effect of duty loss due to switch turn-on and turn-off time according to pulse width decrease in high frequency operation.

III. Control Method

In this section, not only conventional AVP method but also output capacitor ripple current-based peak current mode V^2I_C for buck converter is reviewed. Then, peak charge control for class D/E resonant converter is introduced. Finally, AVP and peak charge control are simultaneously applied to class D/E resonant converter.

A. Conventional AVP and V^2I_C for Buck Converter

The output voltage spike occurs in the transient period where the SoC load current changes rapidly. AVP control method designs a certain voltage range so that output voltage can be varied during transient period according to the changes in load current. Fig. 6(a)-(b) show the comparison of SoC current and voltage waveforms according to the application of AVP method. Based on AVP method, the width of voltage varied during transient period can increase compared to the same load current change, thereby reducing the value of the output capacitor. It can contribute to passive component size decrease. As shown in Fig. 6(c), AVP method can be implemented by designing the control loop so that the voltage reference changes according to the current flowing through the output inductor. There are two design guidelines to achieve AVP method based on output impedance analysis: current-mode control and active-droop control. In this paper, active-droop control is adopted [2].

V^2I_C control method uses ripple current of output capacitor for fast dynamic response [6], [7]. Due to the characteristics of current change in inductor, SoC load current change cannot be immediately reflected in output inductor current, and the difference between SoC current and inductor current flows through the output capacitor. Therefore, fast response speed can be achieved by using ripple current of output capacitor according to a load current change. As a result, voltage spike during transient period can be reduced. In other words, under the assumption of the same voltage spike, output capacitor with smaller value can be used by adopting the V^2I_C control. Accordingly, the size of passive components can be reduced.

Fig. 7 shows V^2I_C applied buck converter. Modulators of constant-on time and constant-off time for variable switching frequency can be configured. Furthermore, valley current and peak current modulator for fixed switching frequency can be used. Modulator used in this paper is based on peak current control for fixed frequency.

B. Proposed Peak Charge Control and AVP for Class D/E Resonant Converter

This paper provides class D/E resonant converter simultaneously applying AVP and proposed peak charge control. The concept illustrates in Fig. 8. The AVP and peak charge control methods for class D/E resonant converter are introduced, respectively.

Output capacitor ripple current-based peak current mode V^2I_C control method used in buck converter cannot be equally applied to the class D/E resonant converter. As shown in Fig. 10(a), peak value of the ripple current is

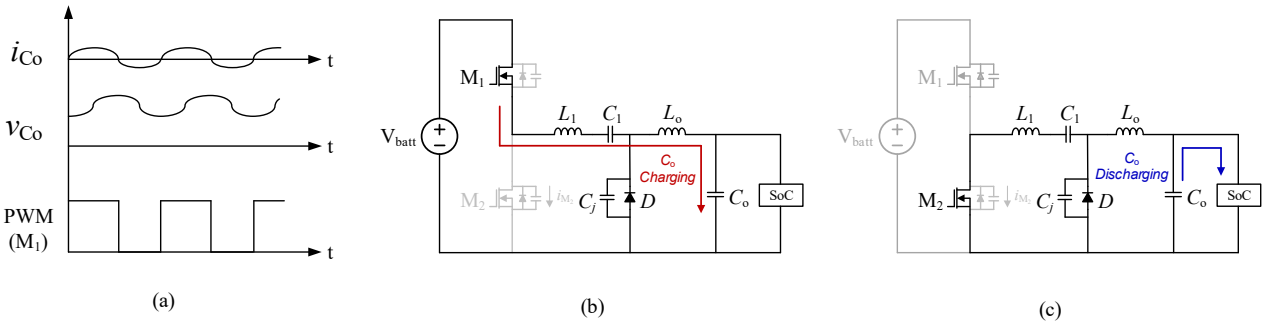

Fig. 9. (a) Ripple current and voltage waveforms according to upper switch operation, (b) operating mode when the upper switch is turning on. (c) operating mode when the lower switch is turning on. Complementary operation between the upper and lower switches is assumed.

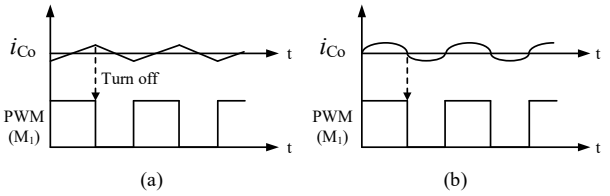

Fig. 10. Ripple current of output capacitor waveform and upper switch operation, (a) buck converter, (b) class D/E resonant converter.

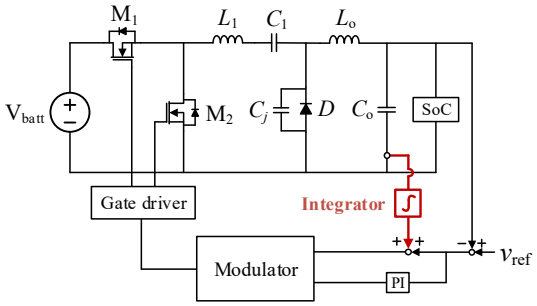

Fig. 11. Class D/E resonant converter with integrator-based peak charge control.

formed at the time when turn-off operation of the upper switch occurs. However, in case of class D/E resonant converter, peak value is realized while the upper switch is turning on. Therefore, the ripple current information cannot be used as it is, and additional solution is needed.

Fig. 9(a) shows the output capacitor ripple current and the voltage waveforms according to the upper switch operation. The voltage across the output capacitor is charged by the ripple current flowing through the output capacitor when the upper switch is turning on. Conversely, the voltage across the output capacitor is discharged when the lower switch is turning on. As a result, peak value of the voltage across the output capacitor is formed at the point where turn-off operation of the upper switch occurs. The voltage across the capacitor is the same as the output SoC voltage, so implementing peak control can be considered by replacing the output ripple current with the ripple voltage. However, designing a peak control with small ripple voltage is quite difficult because it is vulnerable to noise.

Therefore, the current and voltage characteristics of

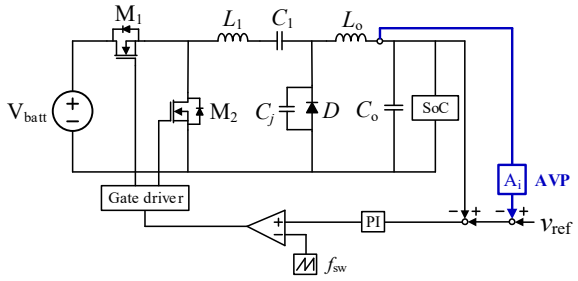

Fig. 12. Class D/E resonant converter with AVP design.

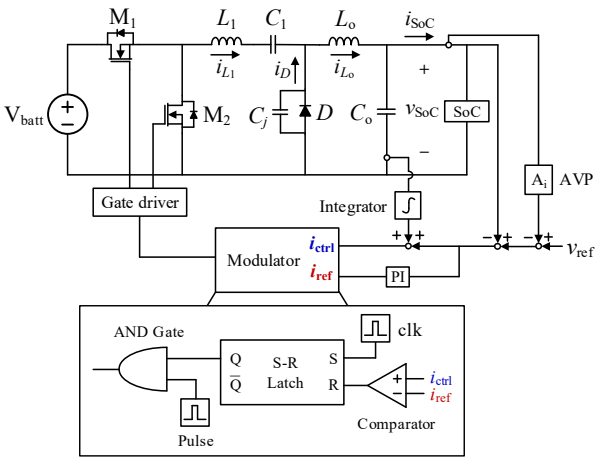

Fig. 13. Class D/E resonant circuit diagram with AVP and peak charge control for simulation

capacitor is used instead of ripple voltage. The voltage across capacitor is equal to the integral value of the current flowing through the capacitor. Therefore, the integrator can be designed for the output capacitor ripple current to realize the voltage across the capacitor as shown in Fig. 11. This proposed method is called integrator-based peak charge control in this paper. Proposed peak charge control has the same advantage as V^2I_C for buck converter. That is, fewer output capacitors can be used based on the same voltage spike design during transient period.

AVP design for class D/E resonant converter is not that different from buck converter. The L_o in class E rectifier serves as the same filter as the output inductor in the buck

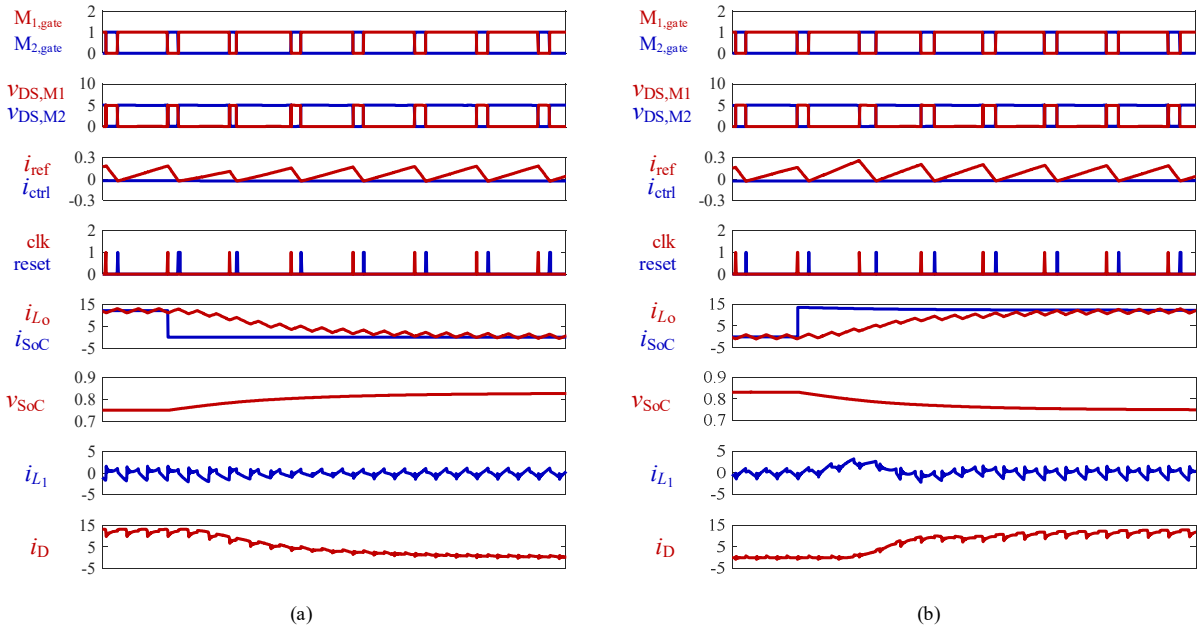

Fig. 14. Simulated waveforms of class D/E resonant converter with peak charge control and AVP at battery voltage (V_{batt}) of 5V. (a) i_{SoC} step-down operation. (b) i_{SoC} step-up operation.

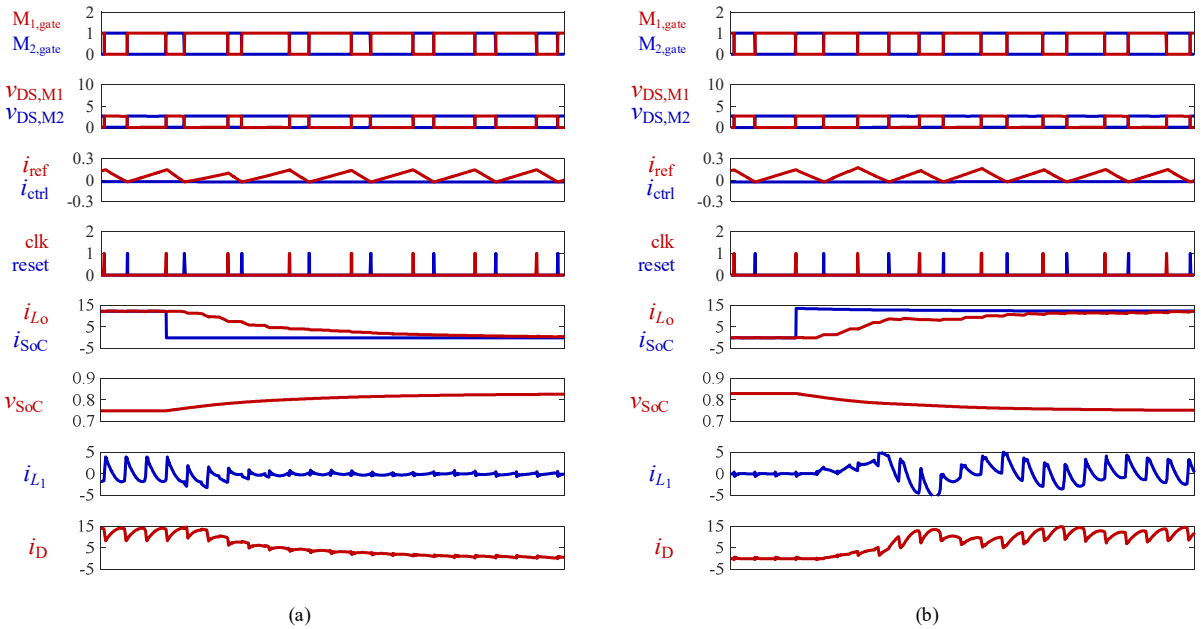

Fig. 15. Simulated waveforms of class D/E resonant converter with peak charge control and AVP at battery voltage (V_{batt}) of 2.7V. (a) i_{SoC} step-down operation. (b) i_{SoC} step-up operation.

converter. Therefore, the controller is designed to change the voltage reference within a certain range according to the load current variation based on the sensed L_o current. Fig. 12 shows the class D/E resonant converter with AVP design. The output capacitor value in class D/E resonant converter can be reduced as in buck converter by applying AVP method.

As a result, AVP and proposed peak charge control are simultaneously applied to the high frequency operation class D/E resonant converter. Overall passive component values are reduced compared to conventional buck converter due to high frequency design. Furthermore, value of output capacitor is minimized by applying AVP and peak charge control at the same time.

IV. Simulation and Comparison

A. Simulation Results

Fig. 13 shows the circuit diagram with control method for simulation. In class D/E resonant converter, there is a

TABLE I
Design Parameters of Buck Converter and Class D/E Resonant Converter

	2-level Buck Converter	Class D/E Resonant Converter		
Control Method	Fixed v_{ref}	Fixed v_{ref}	Peak charge	Peak charge & AVP
v_{ref}	0.79 V	0.79 V	0.79 V	0.75 V~0.83 V
v_{SoC}	0.75 V~0.83 V	0.75 V~0.83 V	0.75 V~0.83 V	0.75 V~0.83 V
i_{SoC}	0.05 A~12 A	0.05 A~12 A	0.05 A~12 A	0.05 A~12 A
f_{sw}	3.5 MHz	10 MHz	10 MHz	10 MHz
L_1	-	1.2 nH	1.2 nH	1.2 nH
L_o	55 nH	20 nH	20 nH	20 nH
C_1	-	0.28 uF	0.28 uF	0.28 uF
C_o	90 uF	32 uF	20.8 uF	14 uF

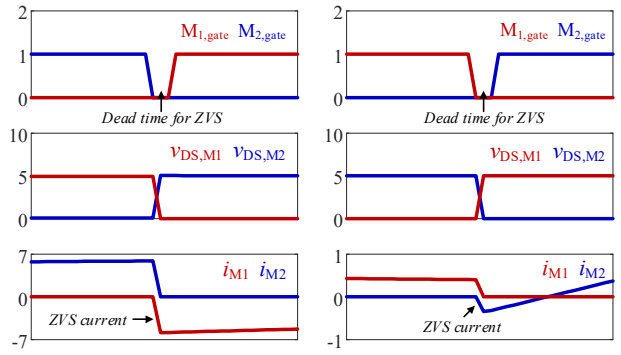

Fig. 16. ZVS waveforms of (a) upper switch M_1, (b) lower switch M_2.

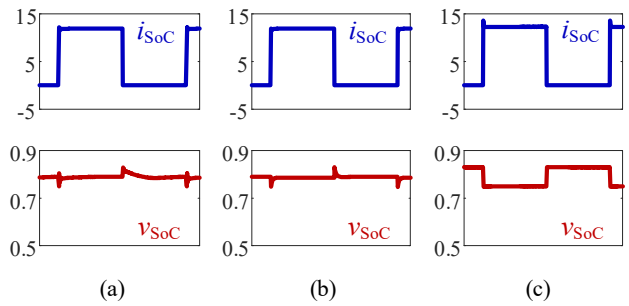

Fig. 17. SoC current and voltage waveforms of class D/E resonant converter according to control method. (a) Fixed v_{ref}. (b) Peak charge control. (c) Peak charge control and AVP. The ranges are equally implemented.

point where the tendency of SoC voltage variation according to duty ratio of the upper switch changes as shown in Fig. 3(b)-(c). The control loop is designed to increase the duty ratio if the SoC voltage is smaller than the reference voltage. Thus, the resonant converter should be operated in a duty ratio range smaller than a point where the tendency of voltage changes, and this is implemented by using an external signal with a constant pulse width and AND gate.

Fig. 14-15 show the simulated waveforms of the class D/E resonant converter with proposed peak charge control and AVP according to the battery voltage. The switching frequency of class D/E resonant converter is targeted at 10 MHz, and the designed parameters are summarized in

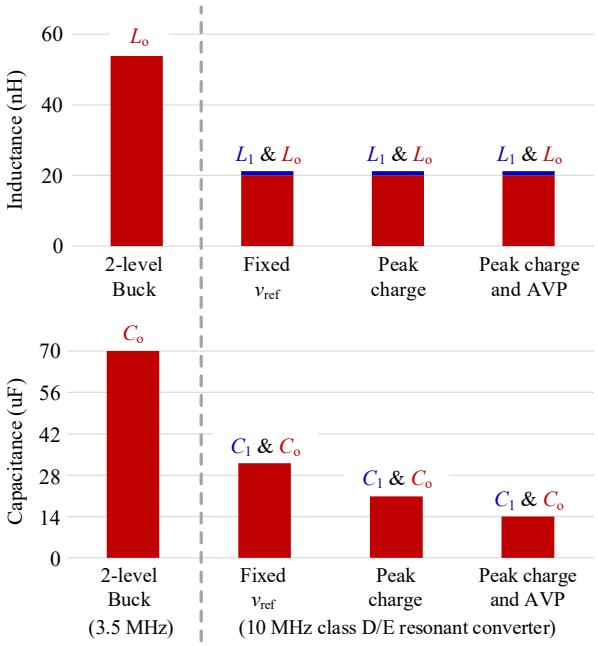

Fig. 18. Comparison of passive component values according to step-down topology and control method.

TABLE I. When the peak value of i_{ctrl} containing the integral value of the ripple current reaches i_{ref}, the comparator generates reset signal, which causes the upper switch to be turned off and the lower switch to be turned on after small dead time for ZVS. The upper switch (lower switch) is turned on (turned off) by external clk signal. That is, the switching frequency of class D/E resonant converter is determined by the frequency of clk. It can be seen that the L_o current change is slower than the SoC current change as mentioned earlier. That is, fast dynamic response during transient period can be achieved by adopting the proposed integrator-based peak charge control using ripple current of output capacitor. As a result, it can contribute to the size reduction of passive component. Furthermore, the AVP operation is verified by simulation results.

B. Value Comparison

As mentioned above, class D/E resonant operates at 10 MHz. Then, buck converter is designed to be 3.5 MHz,

which has the same switching loss with class D/E resonant converter as shown in Fig. 5. The voltage (v_{SoC}) and current (i_{SoC}) of SoC are set to have the same range regardless of the topology and control method. Also, the output inductance (L_o) is designed based on the same current ripple.

The number of passive components constituting the class D/E resonant converter is larger than that of the buck converter, but the overall value is reduced due to the high frequency design. Moreover, Fig. 18 shows that the passive component values are reduced by applying the peak charge control compared to when the fixed voltage control is applied, and finally, the values are further minimized by adopting the peak charge control and AVP simultaneously.

V. Conclusions

In this paper, class D/E non-isolated resonant converter is chosen as a step-down converter for high power density. Compared to conventional buck converter, class D/E resonant converter is suitable for high frequency operation due to ZVS. Therefore, it can be designed with the passive components with smaller values despite the increasing number of passive components. Accordingly, high power density can be achieved by reducing the size of the converter. Furthermore, selected converter has an advantage of minimizing the duty loss with wider duty ratio design. Finally, proposed integrator-based peak charge control and AVP are applied to the class D/E resonant converter at the same time. Thus, the passive component values further decrease. Consequently, the class D/E resonant converter with peak charge control and AVP can be a solution for small size step-down converter with high power density.

Acknowledgment

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