

```
Terminal
Serial COM4 (09/02/2025, 14:49)

////////////////////////////////////
// CONTROL MODULE for Convolutional Coalesced Tsetlin Machine (ConvCoTM) //
// image classification accelerator for 28x28 Boolean images.             //
// -- Xilinx ZCE104 FPGA Development Board ----- //
// ----- READY ----- //
////////////////////////////////////

DMA initialization succeeded

-----
Main Menu:
-----
1. Load model
2. TEST (10 k samples) in continuous mode
3. TEST (single sample)
4. TEST (long loop, for power measurement)
5. Reset image buffer
6. Reset FPGA accelerator
7. TEST (10 k samples) with singlemode operation
8. Enable or disable clock gating

Enter main menu selection:
Start loading model!

-----
ConvCoTM model loaded! :
* 272 TA action signals per clause (the configuration has 128 clauses).
* 10 sets of clause weights (one for each of the 10 classes).
* Each weight is 8 bits (two's complement format).
-----

-----
Main Menu:
-----
1. Load model
2. TEST (10 k samples) in continuous mode
3. TEST (single sample)
4. TEST (long loop, for power measurement)
5. Reset image buffer
6. Reset FPGA accelerator
7. TEST (10 k samples) with singlemode operation
8. Enable or disable clock gating

Enter main menu selection:
-----
Test results from ConvCoTM accelerator in continuous mode:
Test samples: 10000
TEST errors : 258
TEST accuracy : 97.42
-----
```

MNIST test accuracy results.