ECEN689: Special Topics in High-Speed Links Circuits and Systems
Spring 2012

Lecture 7: Equalization Introduction & TX FIR Eq

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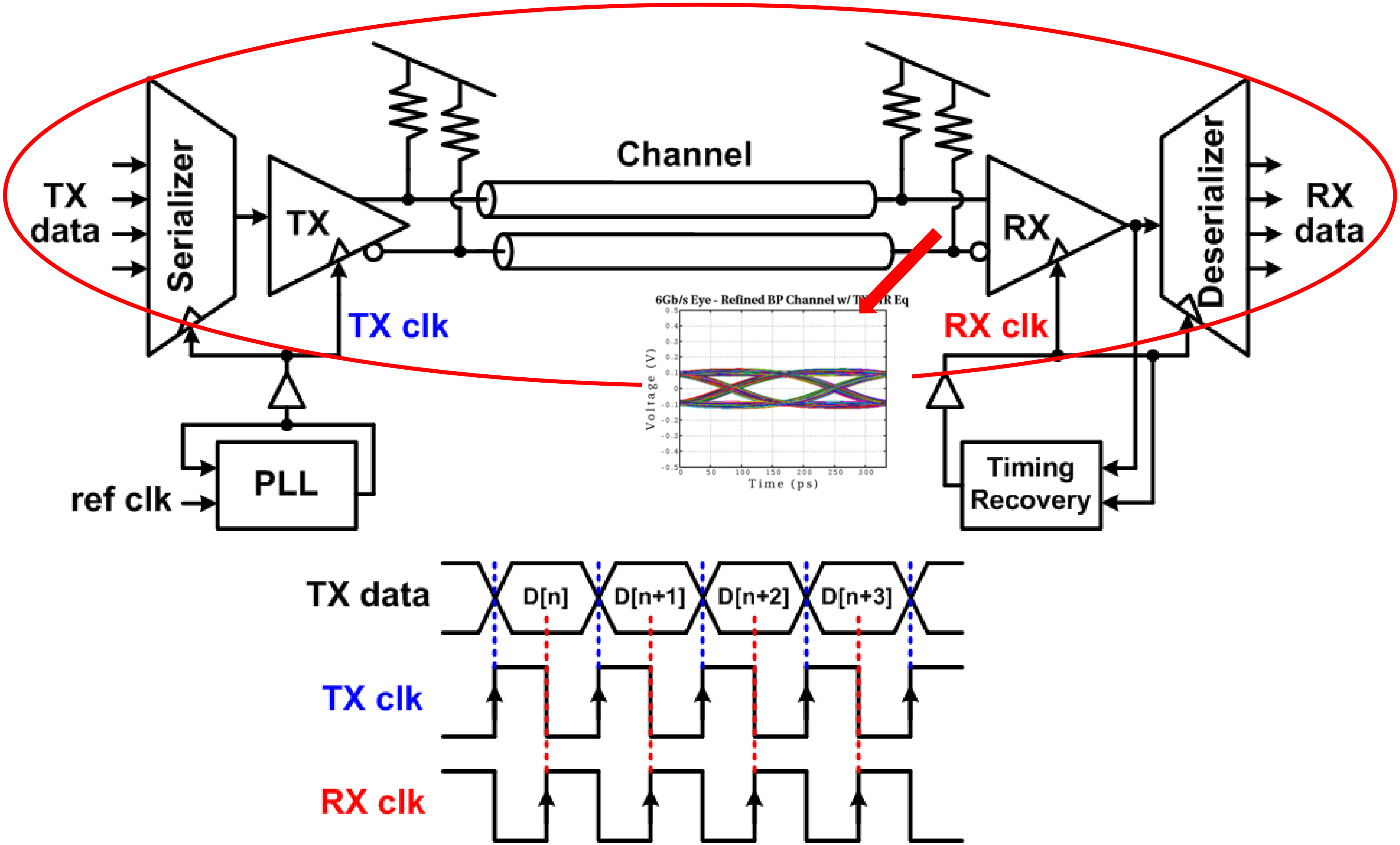
Announcements

- Exam 1 is March 7
  - 5:45-7:10PM (10 extra minutes)
  - Closed book w/ one standard note sheet
  - 8.5”x11” front & back
  - Bring your calculator
  - Covers material through lecture 6
  - Previous years’ exam 1s are posted on the website for reference

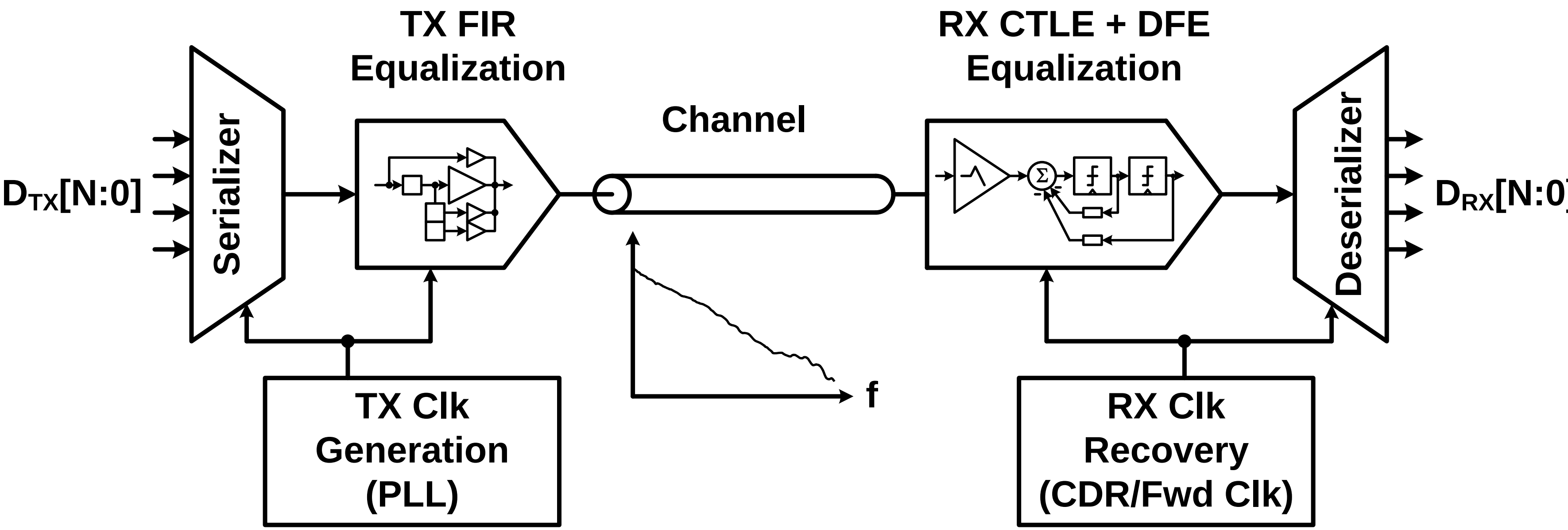
Agenda

- Equalization theory and circuits
  - Equalization overview
  - Equalization implementations
    - TX FIR
    - RX FIR
    - RX CTLE
    - RX DFE
- TX FIR Equalization
  - FIR filter in time and frequency domain
  - MMSE Coefficient Selection
  - Circuit Topologies
- Equalization overview paper posted on website

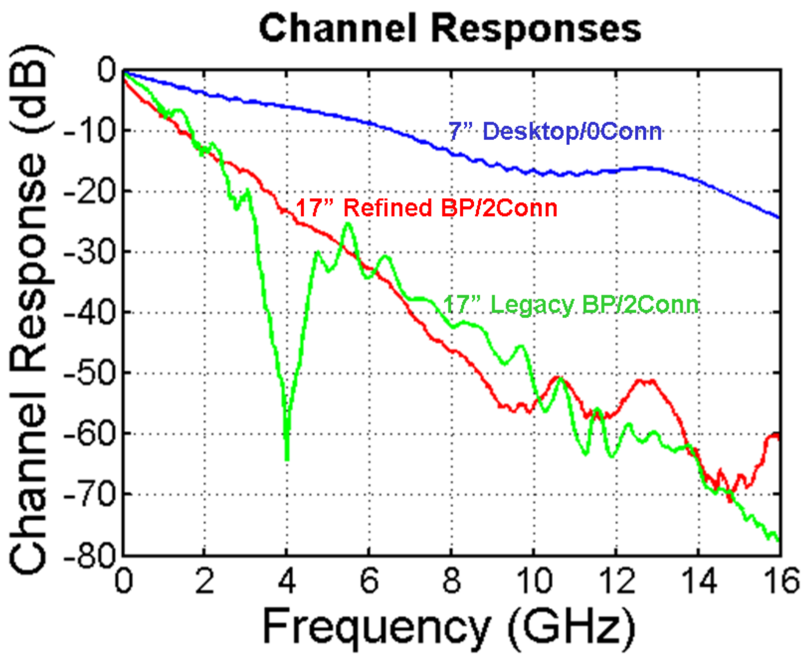
High-Speed Electrical Link System

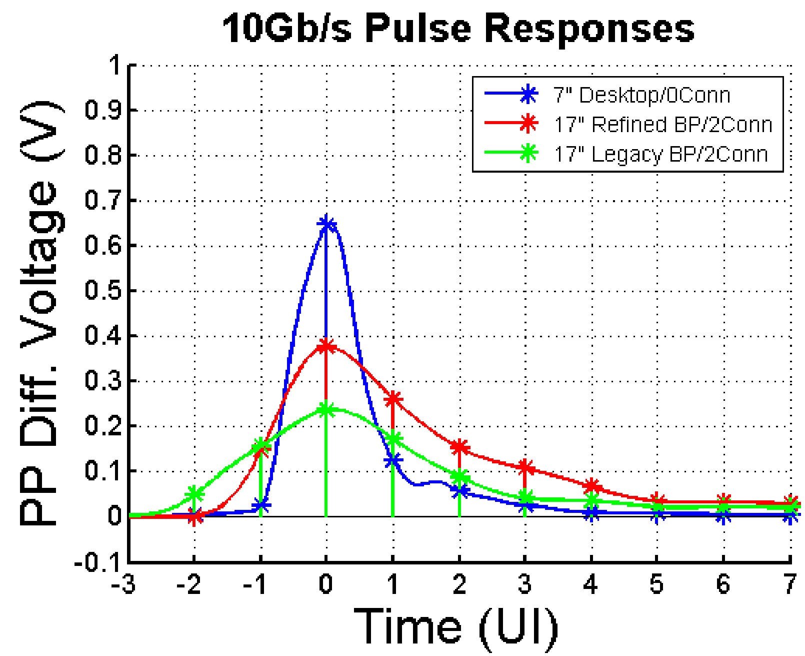


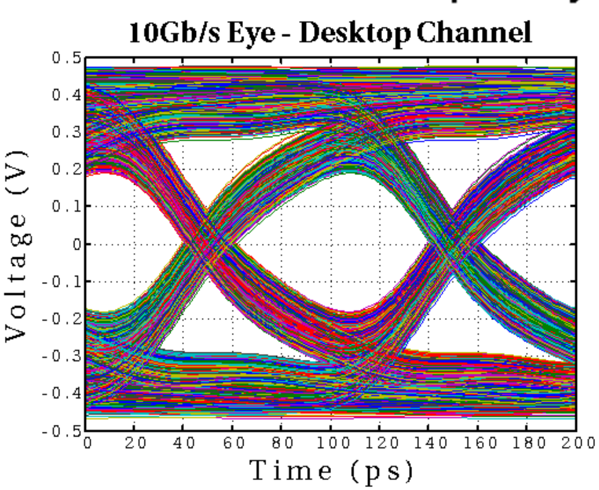
Link with Equalization

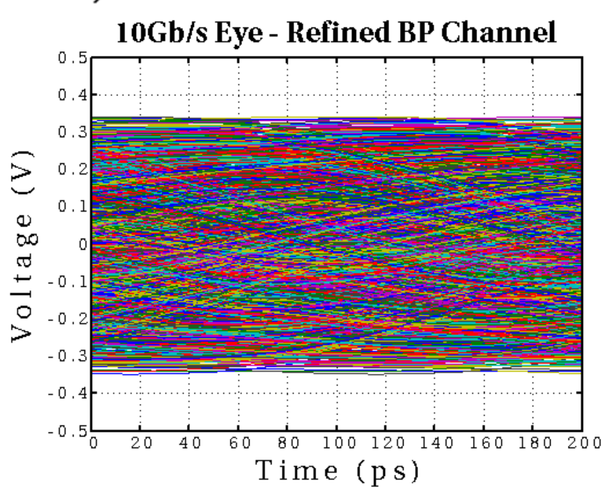


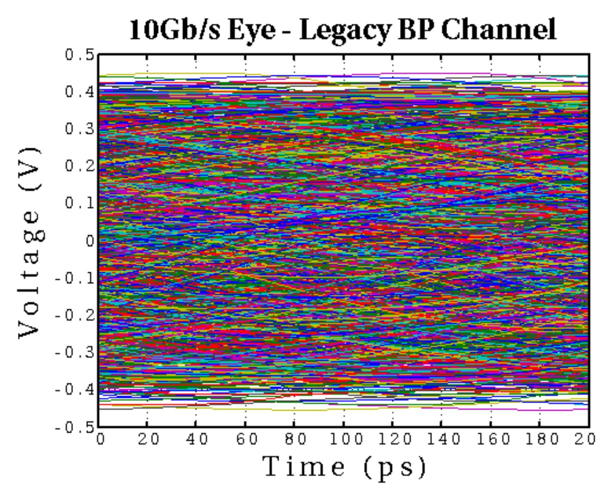
Channel Performance Impact



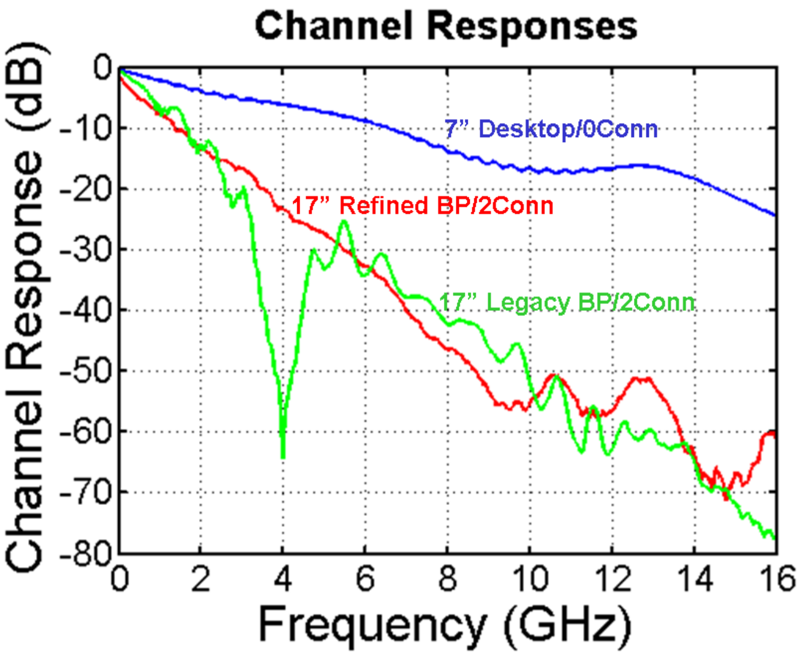


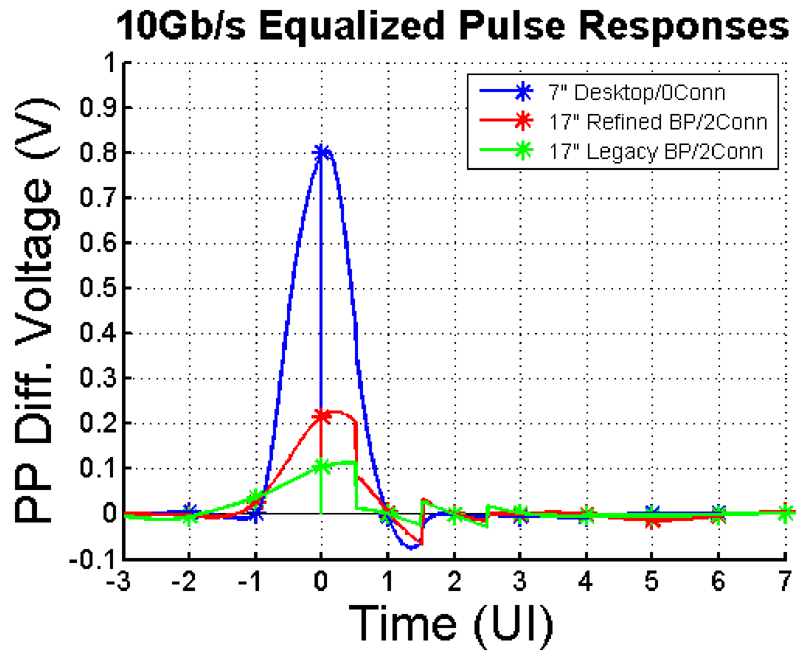


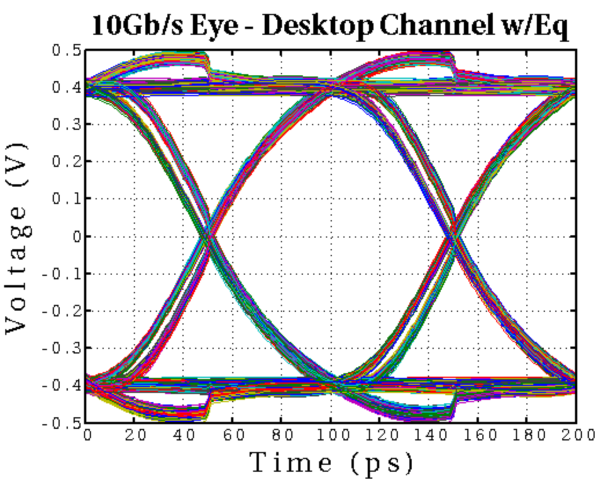


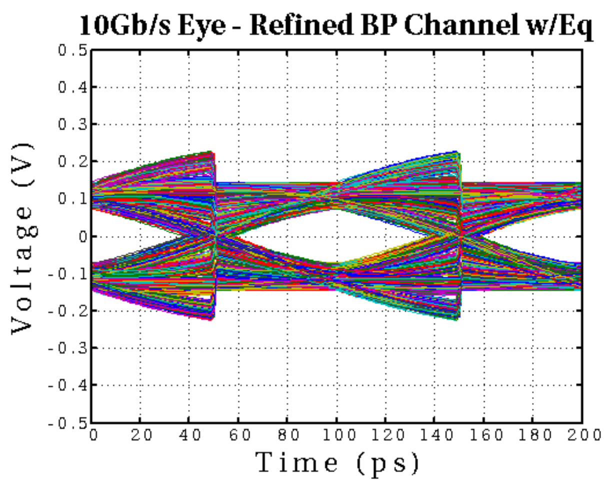


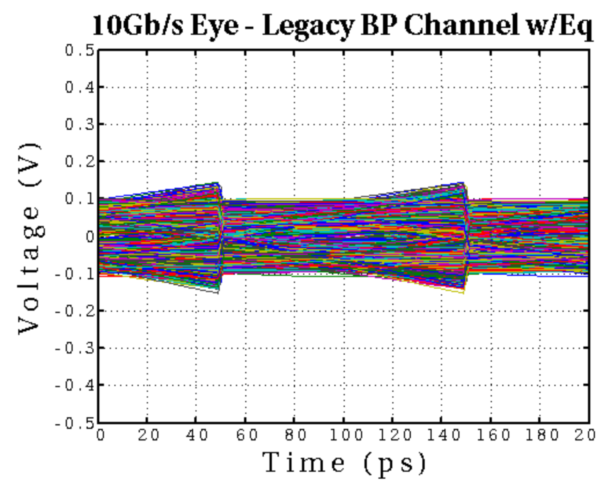
Channel Performance Impact





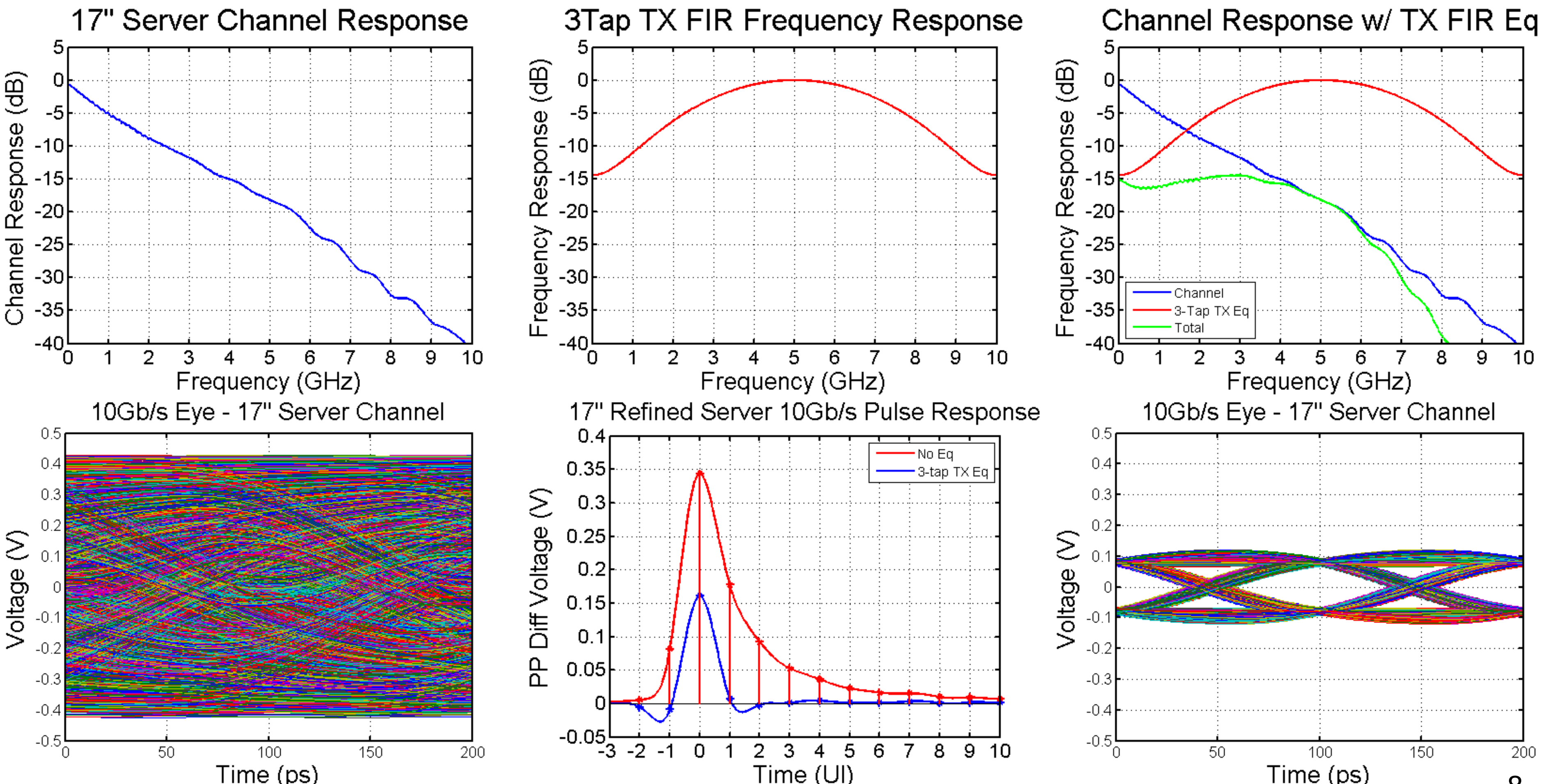






Channel Equalization

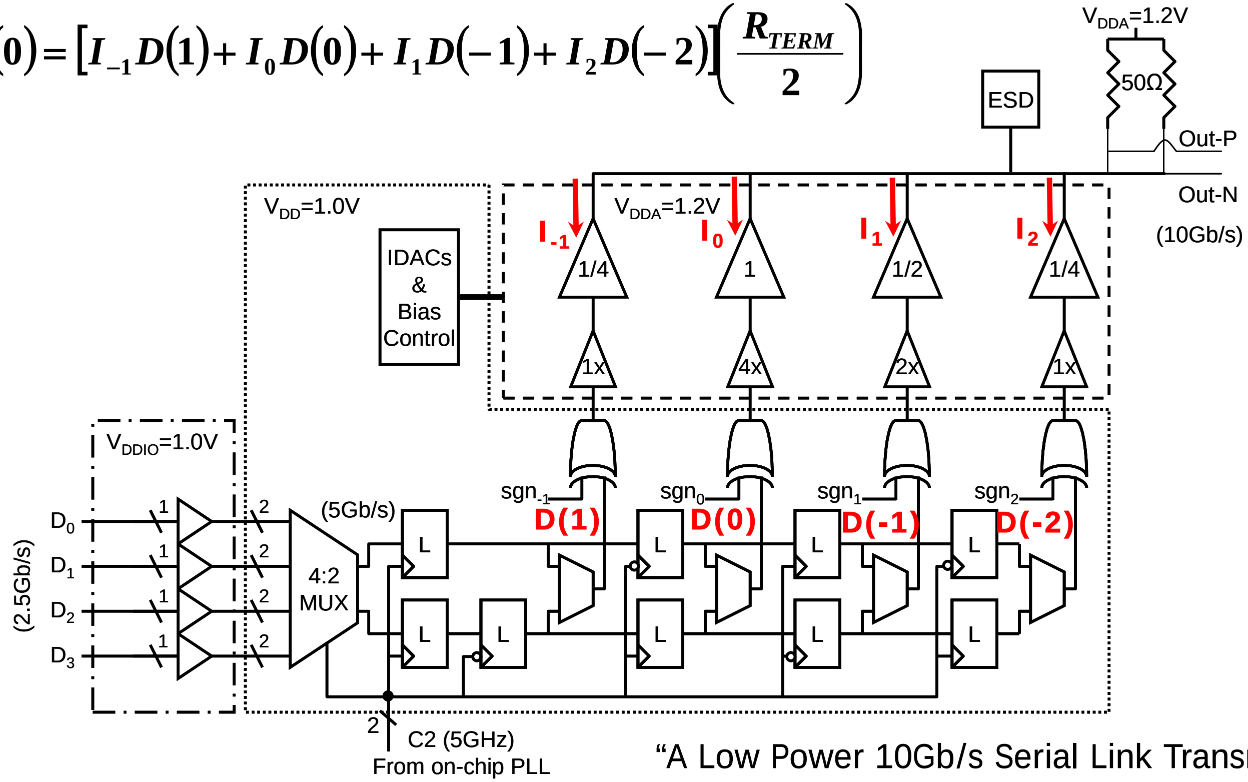
- Equalization goal is to flatten the frequency response out to the Nyquist Frequency and remove time-domain ISI



TX FIR Equalization

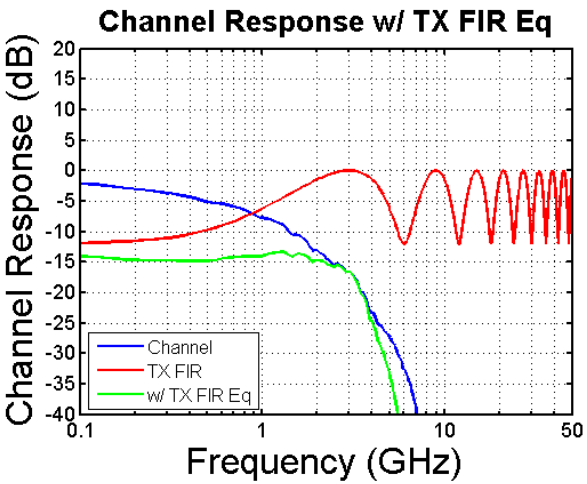
- TX FIR filter pre-distorts transmitted pulse in order to invert channel distortion at the cost of attenuated transmit signal (de-emphasis)

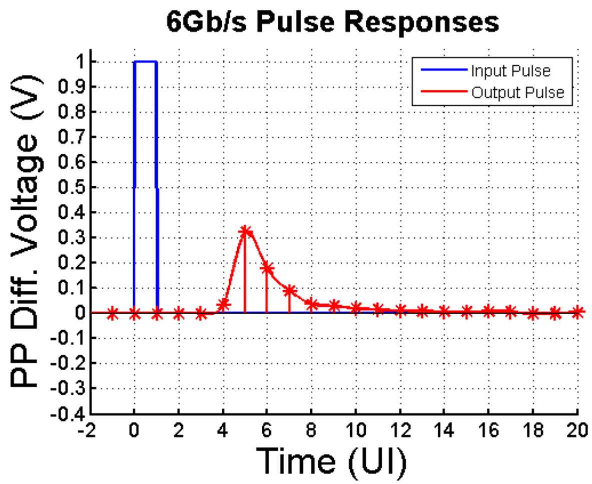
$$V_{out}(0) = \left[I_{-1}D(1) + I_0 D(0) + I_1 D(-1) + I_2 D(-2)\right]\left(\frac{R_{TERM}}{2}\right)$$

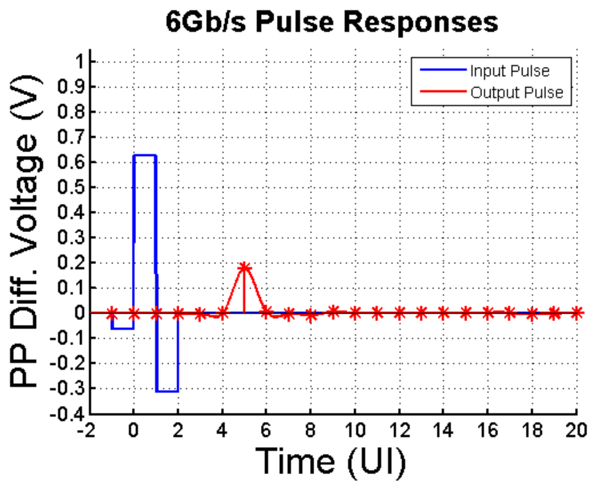


"A Low Power 10Gb/s Serial Link Transmitter in 90-nm CMOS," A. Rylyakov et al., CSICS 2005

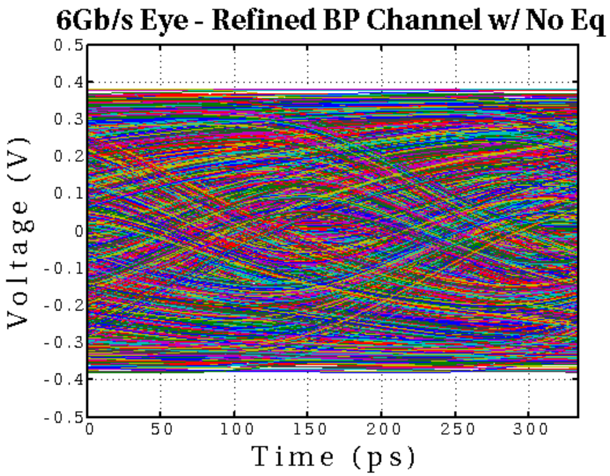
6Gb/s TX FIR Equalization Example

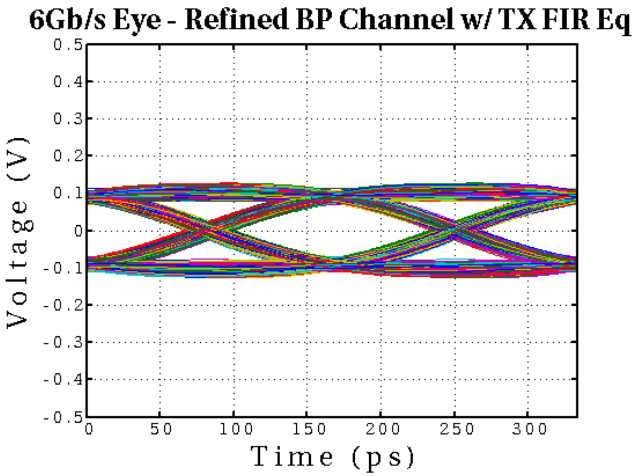




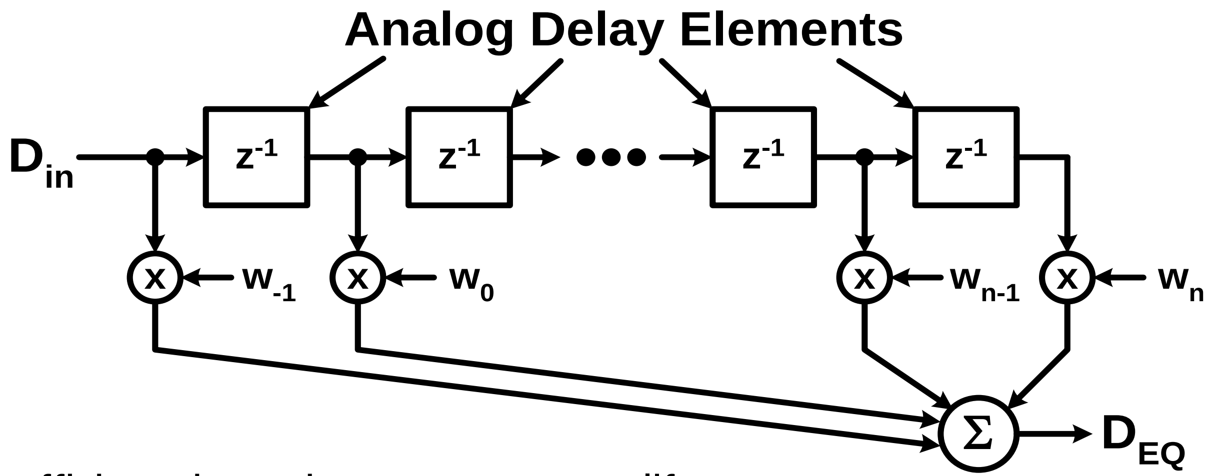


- Pros
  - Simple to implement
  - Can cancel ISI in pre-cursor and beyond filter span
  - Doesn't amplify noise
  - Can achieve 5-6bit resolution
- Cons
  - Attenuates low frequency content due to peak-power limitatior
  - Need a "back-channel" to tune filter taps



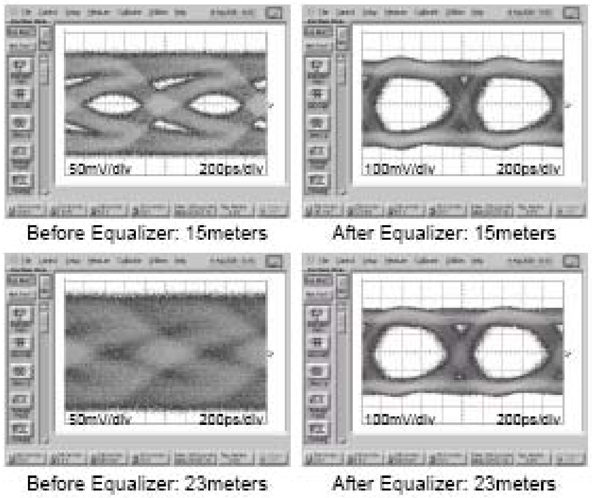


RX Equalization #1: RX FIR



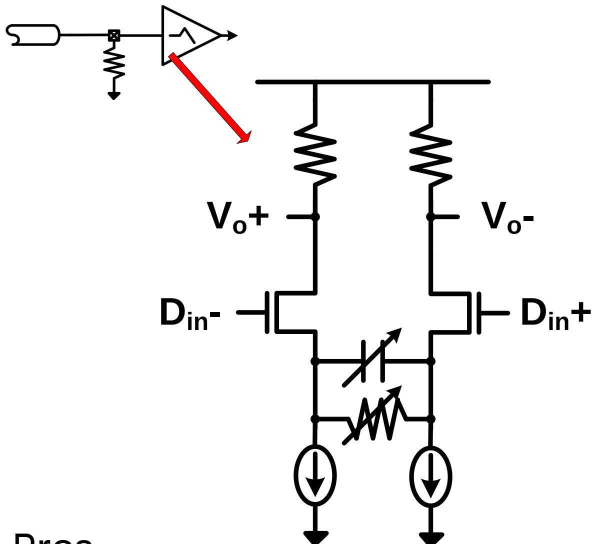
- Pros
  - With sufficient dynamic range, can amplify high frequency content (rather than attenuate low frequencies)
  - Can cancel ISI in pre-cursor and beyond filter span
  - Filter tap coefficients can be adaptively tuned without any back-channel
- Cons
  - Amplifies noise/crosstalk
  - Implementation of analog delays
  - Tap precision

Eye-Pattern Diagrams at 1Gb/s on CAT5e*

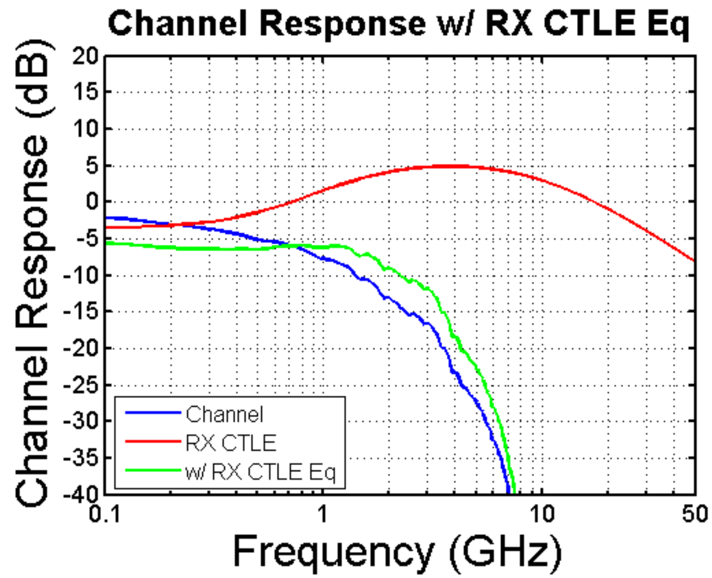


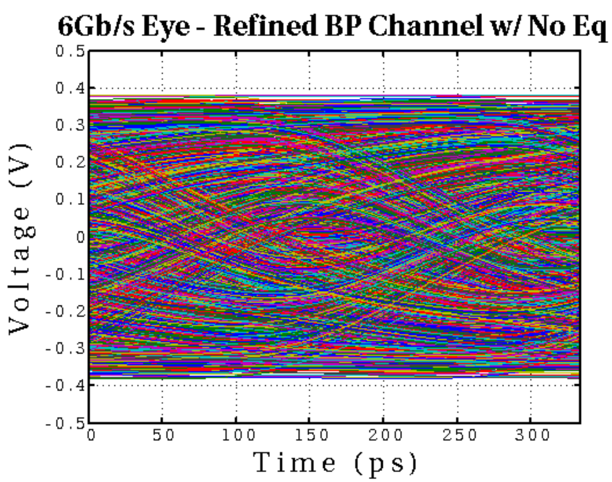
*D. Hernandez-Garduno and J. Silva-Martinez, "A CMOS 1Gb/s 5-Tap Transversal Equalizer based on 3rd-Order Delay Cells," ISSCC, 2007.

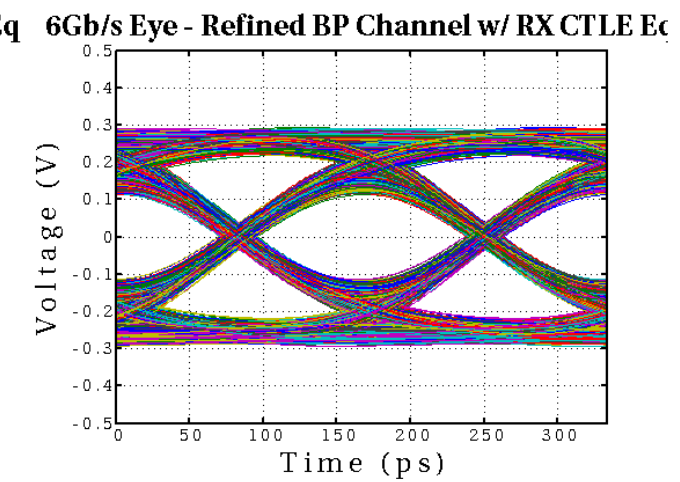
RX Equalization #2: RX CTLE



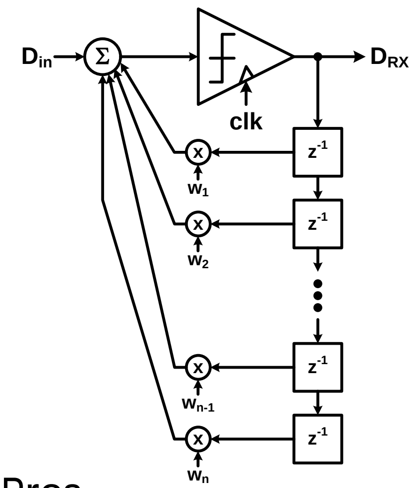
- Pros
  - Provides gain and equalization with low power and area overhead
  - Can cancel both pre-cursor and long-tail ISI
- Cons
  - Generally limited to 1st order compensation
  - Amplifies noise/crosstalk
  - PVT sensitivity
  - Can be hard to tune

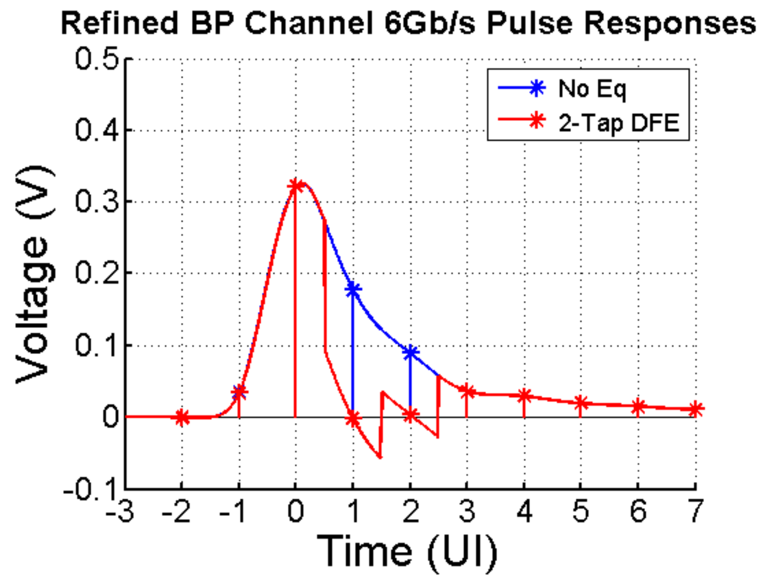




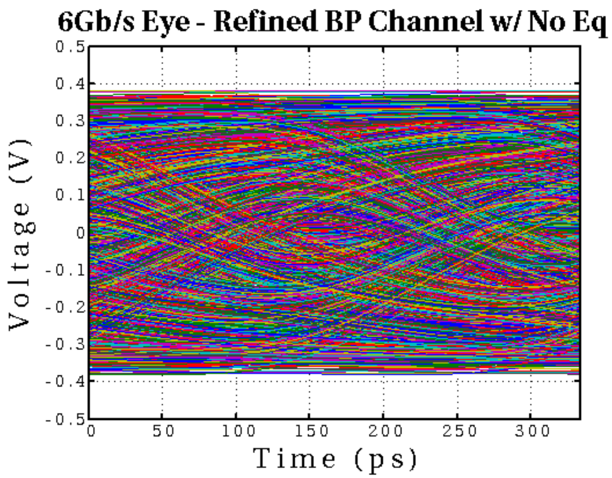


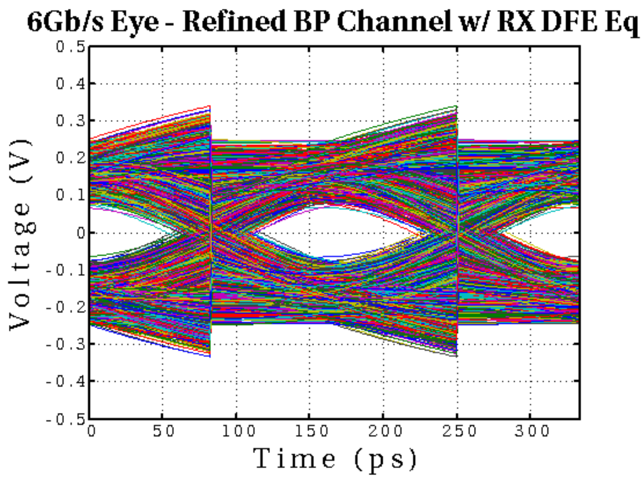
RX Equalization #3: RX DFE





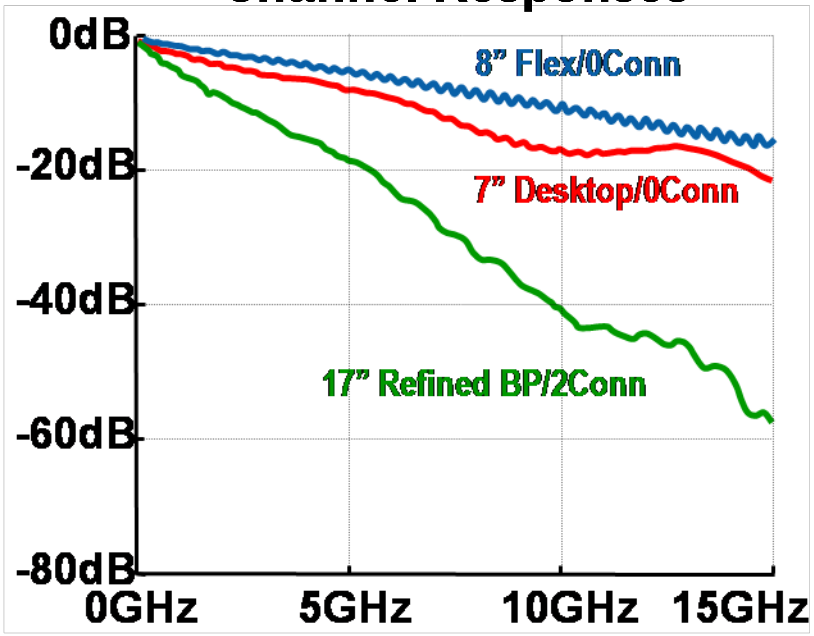
- Pros
  - No noise and crosstalk amplification
  - Filter tap coefficients can be adaptively tuned without any back-channel
- Cons
  - Cannot cancel pre-cursor ISI
  - Critical feedback timing path
  - Timing of ISI subtraction complicates CDR phase detection



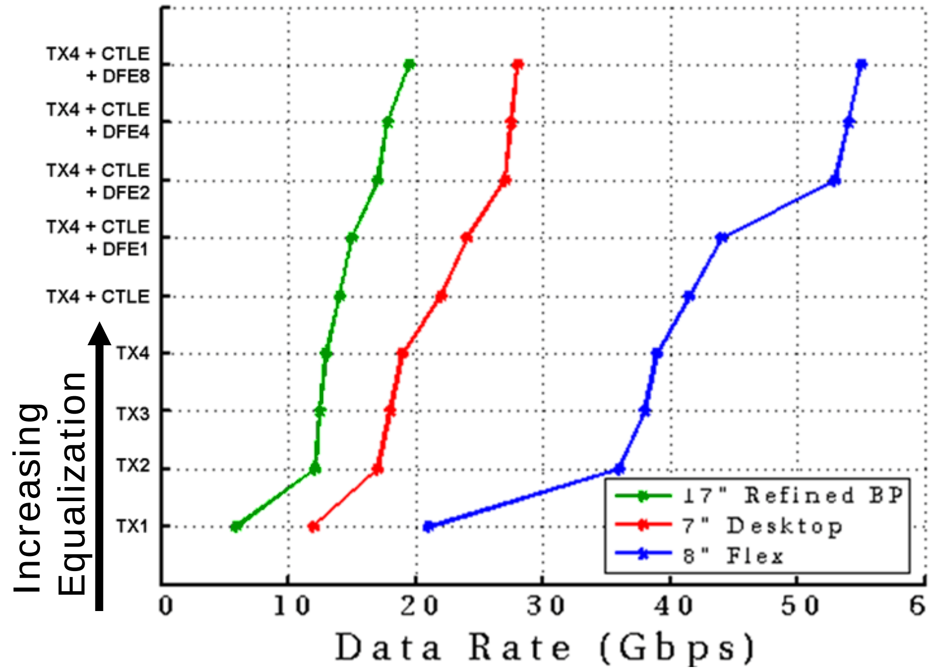


Equalization Effectiveness

Channel Responses

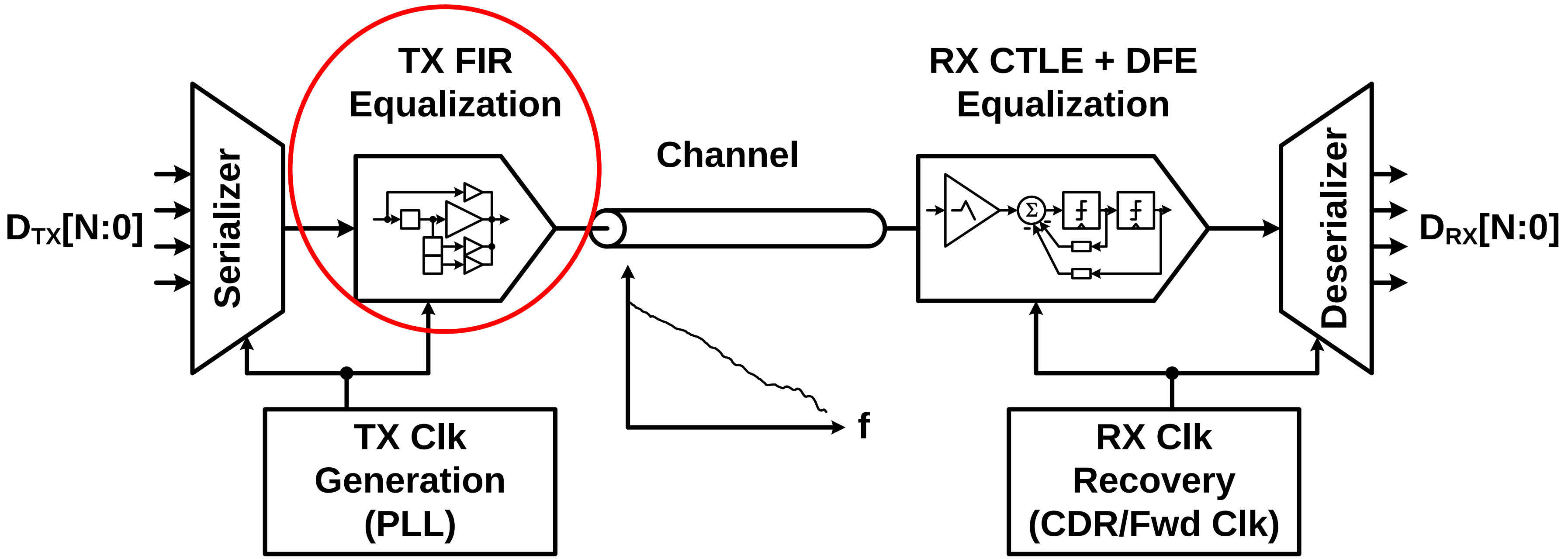


Eq. Complexity vs Max. Data Rate



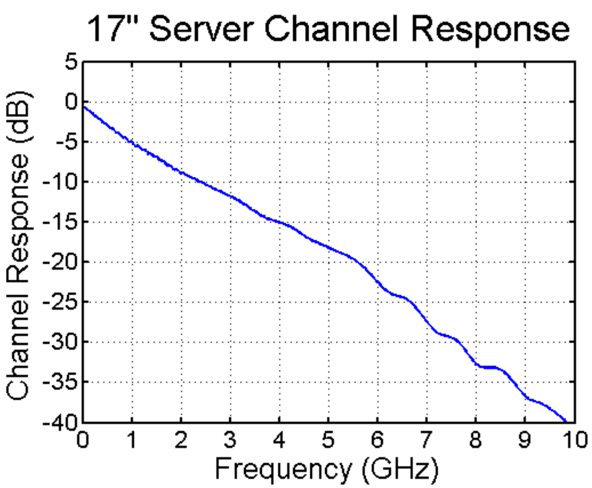
- Some observations:
  - Big initial performance boost with 2-tap TX eq.
  - With only TX eq., not much difference between 2 to 4-tap
  - RX equalization, particularly DFE, allows for further performance improvement
    - Caution – hard to build fast DFEs due to critical timing path

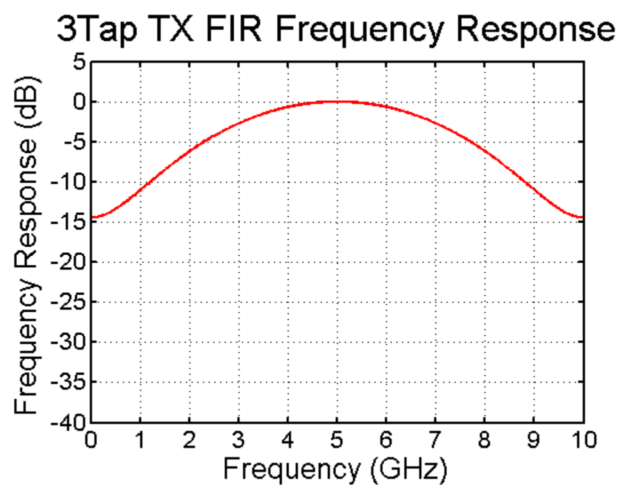
Link with Equalization

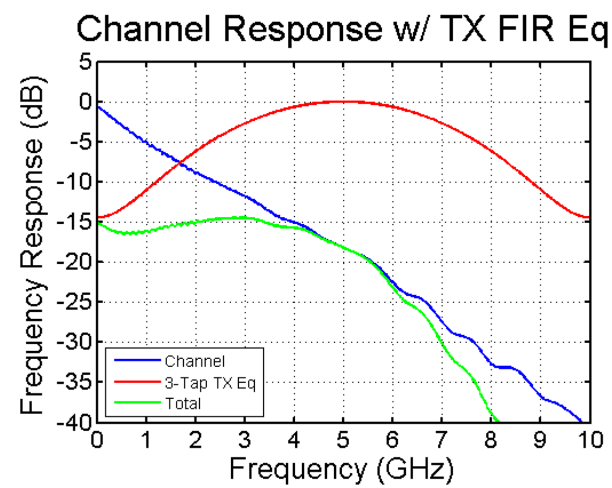


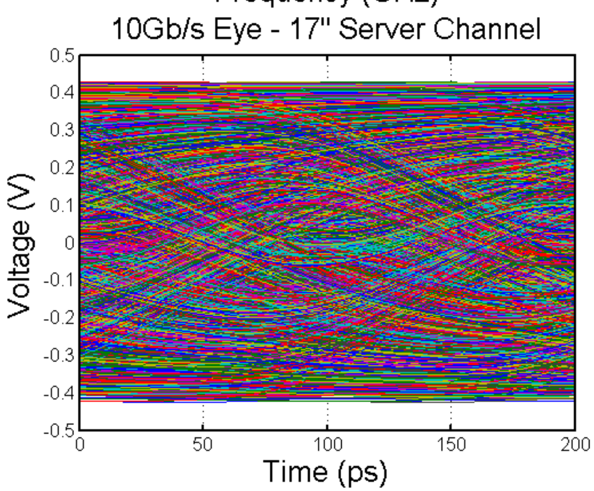
Channel Equalization

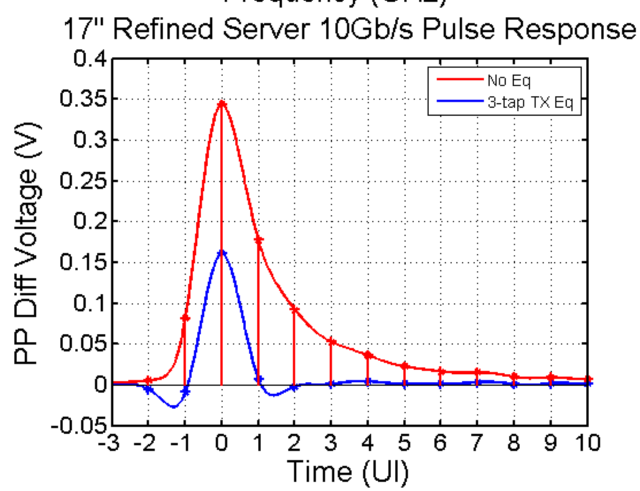
- Equalization goal is to flatten the frequency response out to the Nyquist Frequency and remove time-domain ISI

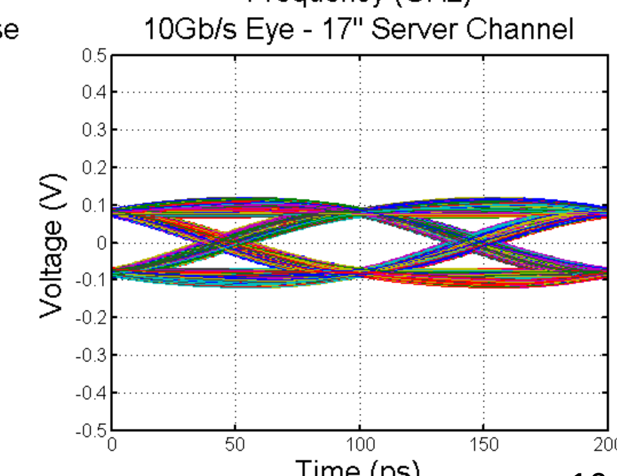






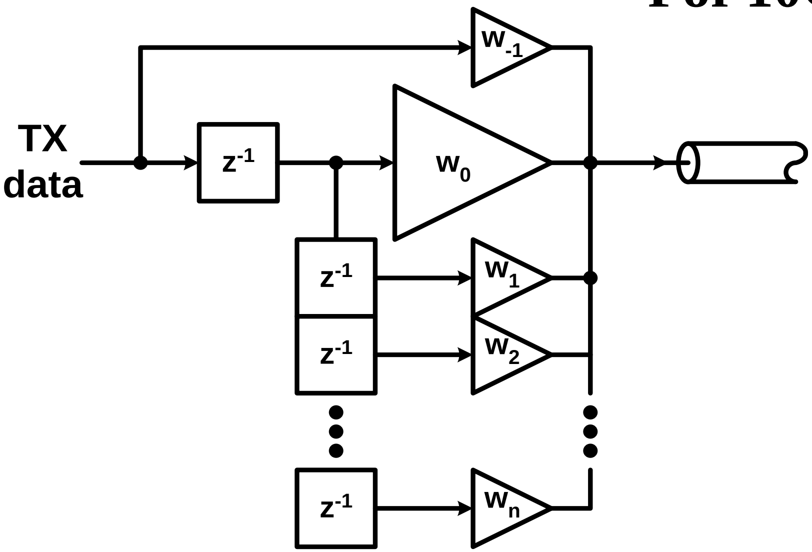


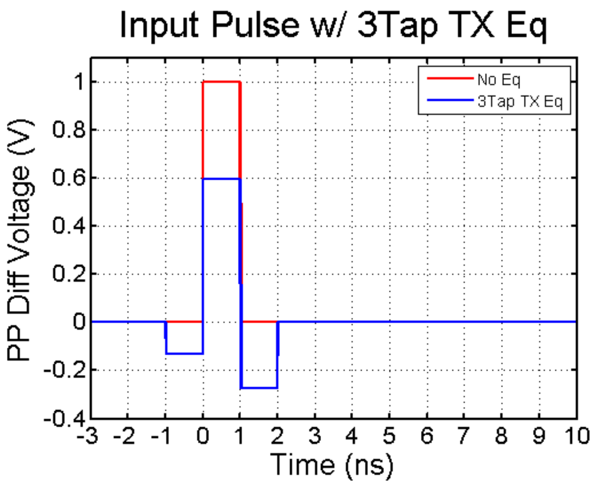


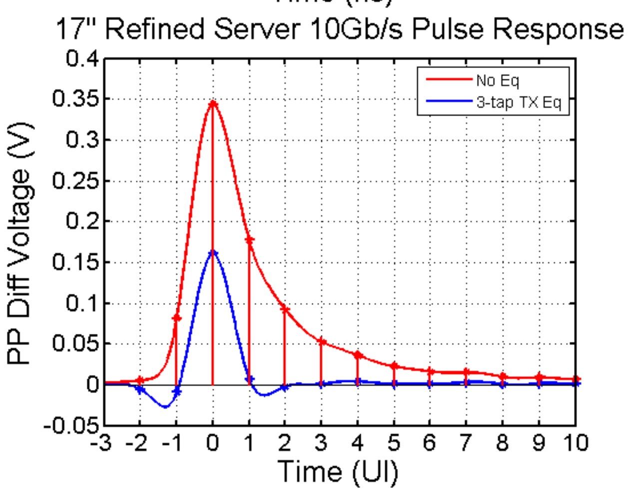


TX FIR Equalization – Time Domain

$$\textbf{For 10Gbps}: W(z) = -0.131 + 0.595z^{-1} - 0.274z^{-2}$$







$$\mathbf{W} = \begin{bmatrix} -0.131 & 0.595 & -0.274 \end{bmatrix}$$

Low Frequency Response (Sum Taps)

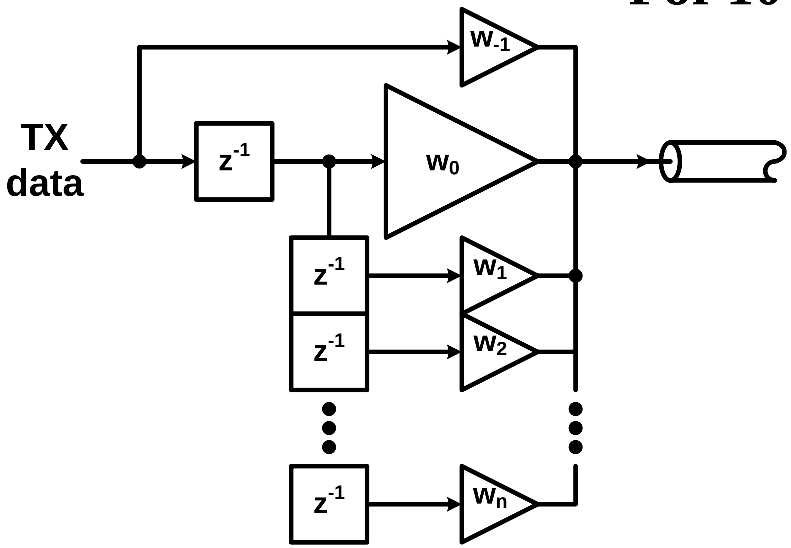
$$[\ldots \quad 1 \quad 1 \quad 1 \quad \ldots] * [-0.131 \quad 0.595 \quad -0.274] = [\ldots \quad 0.190 \quad 0.190 \quad 0.190 \quad \ldots]$$

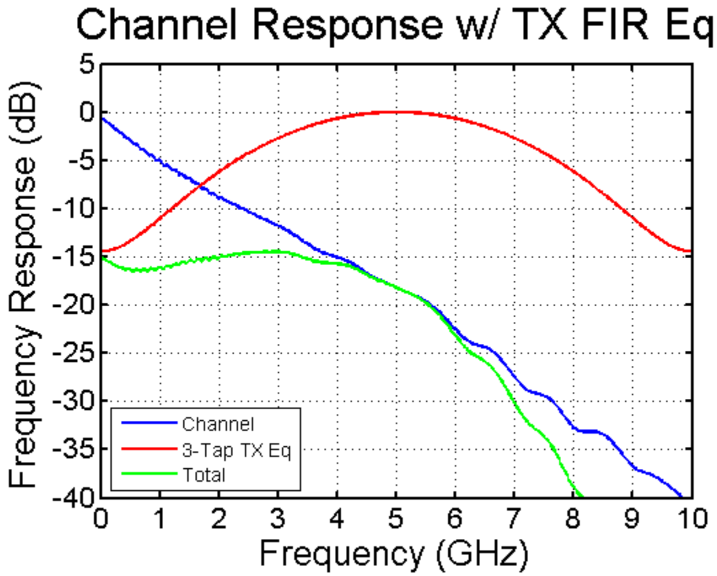
Nyquist Frequency Response (Sum Taps w/ Alternating Polarity)

$$[\ldots \quad -1 \quad 1 \quad -1 \quad \ldots] * [-0.131 \quad 0.595 \quad -0.274] = [\ldots \quad 1 \quad -1 \quad 1 \quad \ldots]$$

TX FIR Equalization – Freq. Domain

For 10Gbps : $W(z) = -0.131 + 0.595z^{-1} - 0.274z^{-2}$





$$W(z) = -0.131 + 0.595z^{-1} - 0.274z^{-2}$$

$$\text{w/} \quad z = e^{j2\pi f T_s} = \cos(2\pi f T_s) + j\sin(2\pi f T_s)$$

Low Frequency Response $(f = 0)$

$$z = \cos(0) + j\sin(0) = 1 \Rightarrow W(f = 0) = 0.190 \Rightarrow -14.4dB$$

Nyquist Frequency Response $\left(f = \frac{1}{2T_s}\right)$

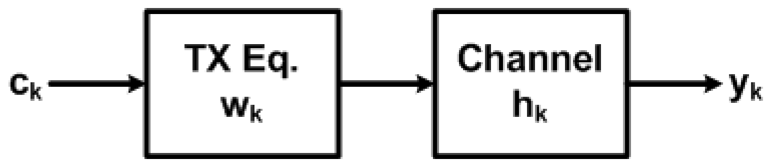
$$z = \cos(\pi) + j\sin(\pi) = -1 \Rightarrow W\left(f = \frac{1}{2T_s}\right) = -1 \Rightarrow 0dB$$

Note: Ts=Tb=100ps

- Equalizer has 14.4dB of frequency peaking
  - Attenuates DC at -14.4dB and passes Nyquist frequency at 0dB

TX FIR Coefficient Selection

- One approach to set the TX FIR coefficients is a Minimum Mean-Square Error (MMSE) Algorithm



channel output vector, y
Rows = k+n+ℓ-2
where k = channel pulse model length

TX Eq "w" Matrix
Rows = n+ℓ-1 where n = tap number
Columns = ℓ = input symbol number

$$\begin{bmatrix} y(0) \\ y(1) \\ \dots \\ y(l+n+k-3) \end{bmatrix} = \begin{bmatrix} h(0) & 0 & 0 & \dots & 0 & 0 \\ h(1) & h(0) & 0 & \dots & 0 & 0 \\ \dots & \dots & \dots & \dots & \dots & \dots \\ 0 & 0 & 0 & \dots & h(k-1) & h(k-2) \\ 0 & 0 & 0 & \dots & 0 & h(k-1) \end{bmatrix} \begin{bmatrix} w(0) & 0 & 0 & \dots & 0 & 0 \\ w(1) & w(0) & 0 & \dots & 0 & 0 \\ \dots & \dots & \dots & \dots & \dots & \dots \\ 0 & 0 & 0 & \dots & w(n-1) & w(n-2) \\ 0 & 0 & 0 & \dots & 0 & w(n-1) \end{bmatrix} \begin{bmatrix} c(0) \\ c(1) \\ \dots \\ c(l-1) \end{bmatrix}$$

Channel "h" Matrix
Rows = k+n+ℓ-2
Columns = n+ℓ-1

ℓ input symbols, c

TX FIR Coefficient Selection

- Total system

$$\begin{bmatrix} y(0) \\ y(1) \\ \dots \\ y(l+n+k-3) \end{bmatrix} = \begin{bmatrix} h(0) & 0 & 0 & \dots & 0 & 0 \\ h(1) & h(0) & 0 & \dots & 0 & 0 \\ \dots & \dots & \dots & \dots & \dots & \dots \\ 0 & 0 & 0 & \dots & h(k-1) & h(k-2) \\ 0 & 0 & 0 & \dots & 0 & h(k-1) \end{bmatrix} \begin{bmatrix} w(0) & 0 & 0 & \dots & 0 & 0 \\ w(1) & w(0) & 0 & \dots & 0 & 0 \\ \dots & \dots & \dots & \dots & \dots & \dots \\ 0 & 0 & 0 & \dots & w(n-1) & w(n-2) \\ 0 & 0 & 0 & \dots & 0 & w(n-1) \end{bmatrix} \begin{bmatrix} c(0) \\ c(1) \\ \dots \\ c(l-1) \end{bmatrix}$$

- Multiplying input symbols by TX Eq., wc=w*c

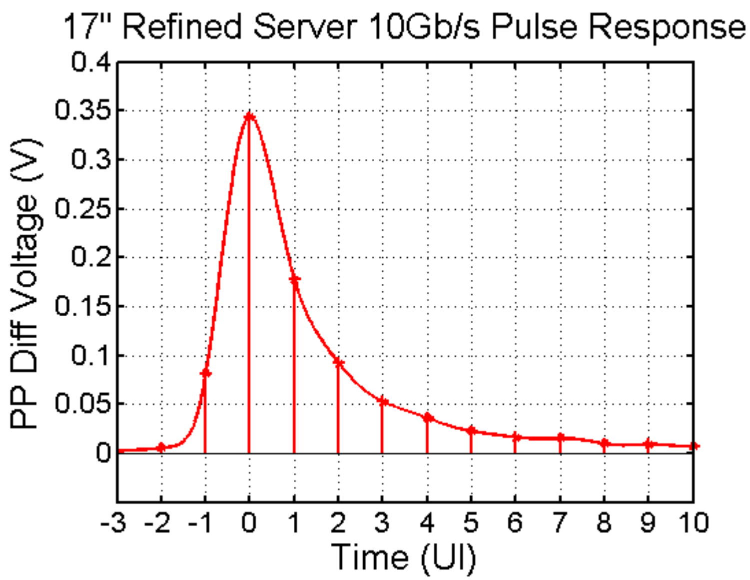
$$\begin{bmatrix} y(0) \\ y(1) \\ \dots \\ y(l+n+k-3) \end{bmatrix} = \begin{bmatrix} h(0) & 0 & 0 & \dots & 0 & 0 \\ h(1) & h(0) & 0 & \dots & 0 & 0 \\ \dots & \dots & \dots & \dots & \dots & \dots \\ 0 & 0 & 0 & \dots & h(k-1) & h(k-2) \\ 0 & 0 & 0 & \dots & 0 & h(k-1) \end{bmatrix} \begin{bmatrix} wc(0) \\ wc(1) \\ \dots \\ wc(n+l-1) \end{bmatrix}$$

- We desire the output vector, y, to be ISI free

$$y_{des} = \begin{cases} y_{des}(n) = 1, n = \textbf{Channel pre-cursor sample \# + Eq precursor tap \# + 1} \\ y_{des}(n) = 0, n \neq \textbf{Channel pre-cursor sample \# + Eq precursor tap \# + 1} \end{cases}$$

Lone-Pulse Equalization Example

- With lone-pulse equalization, ℓ=1 input symbols, i.e. c=[1]



Channel pre-cursor samples

$Y_{des}(5+1+1=7)=1$

Equalization pre-cursor taps

Channel pulse matrix H with 5 pre-cursor samples and 10 post-cursor samples, 3 columns for 3 eq taps

Y_{des}

$$
\begin{bmatrix} 0\\0\\0\\0\\0\\0\\1\\0\\0\\0\\0\\0\\0\\0\\0\\0\\0\\0 \end{bmatrix}
=
\begin{bmatrix}
0.0004 & 0 & 0\\
0.0010 & 0.0004 & 0\\
0.0023 & 0.0010 & 0.0004\\
0.0052 & 0.0023 & 0.0010\\
0.0812 & 0.0052 & 0.0023\\
0.3437 & 0.0812 & 0.0052\\
0.1775 & 0.3437 & 0.0812\\
0.0917 & 0.1775 & 0.3437\\
0.0526 & 0.0917 & 0.1775\\
0.0360 & 0.0526 & 0.0917\\
0.0224 & 0.0360 & 0.0526\\
0.0162 & 0.0224 & 0.0360\\
0.0152 & 0.0162 & 0.0224\\
0.0097 & 0.0152 & 0.0162\\
0.0090 & 0.0097 & 0.0152\\
0.0067 & 0.0090 & 0.0097\\
0 & 0.0067 & 0.0090\\
0 & 0 & 0.0067
\end{bmatrix}
\begin{bmatrix} w(0)\\ w(1)\\ w(2) \end{bmatrix}
\begin{bmatrix} 1 \end{bmatrix}
$$

3-tap Eq Matrix, W

Symbol Matrix, C for "Lone Pulse"

TX FIR Coefficient Selection

- We can calculate the error w.r.t. a desired output

$$E = Y - Y_{des} = HW_C - Y_{des} = HW - Y_{des} \textbf{ with pulse input}$$

- Computing the error matrix norm²

$$\|E\|^2 = W^T H^T HW - 2Y_{des}^T HW + Y_{des}^T Y_{des}$$

- Differentiating this w.r.t. tap matrix taps to find taps which yield minimum error norm²

$$\frac{d}{dW}\|E\|^2 = 2W^T H^T H - 2Y_{des}^T H = 0$$

$$W^T H^T H = Y_{des}^T H$$

- Solving for optimum TX Eq taps, W

$$\boxed{W_{ls} = \left(H^T H\right)^{-1} H^T Y_{des}}$$

- This will yield a W matrix to produce a value of "1" at the output cursor, i.e. an FIR filter with gain
  - Need to normalize by the total abs(tap) sum for TX FIR realization

$$\boxed{W_{lsnorm}(n) = \frac{W_{ls}(n)}{\sum_{i=1}^{n} \left|W_{ls}(n)\right|}}$$

TX FIR Tap Resolution

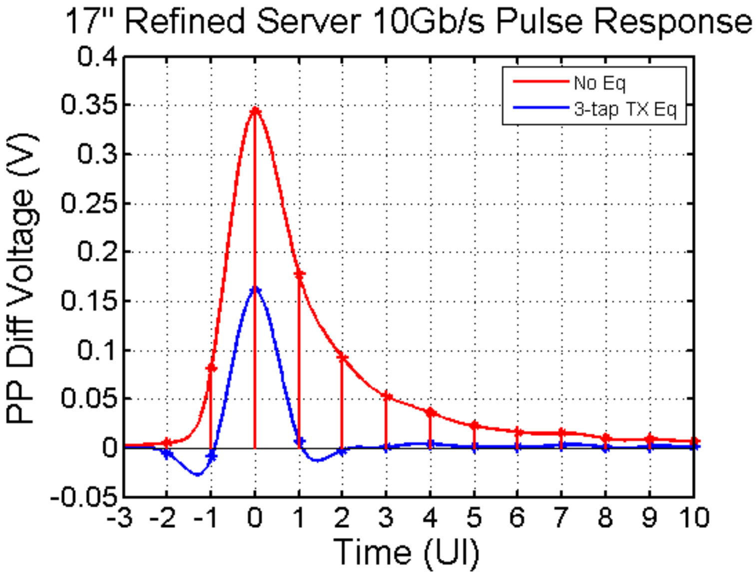
- Using the above MMSE algorithm for the Refined Server Channel at 10Gb/s

$$W_{ls} = \begin{bmatrix} -0.8180 \\ 3.7245 \\ -1.7184 \end{bmatrix} \overset{\text{normalizing by 6.2609}}{\Rightarrow} W_{lsnorm} = \begin{bmatrix} -0.1307 \\ 0.5949 \\ -0.2745 \end{bmatrix}$$

$$W(z) = -0.131 + 0.595z^{-1} - 0.274z^{-2}$$

$$\begin{bmatrix} 1pre & main & 1post \end{bmatrix}$$

$$\begin{bmatrix} -0.131 & 0.595 & -0.274 \end{bmatrix}$$

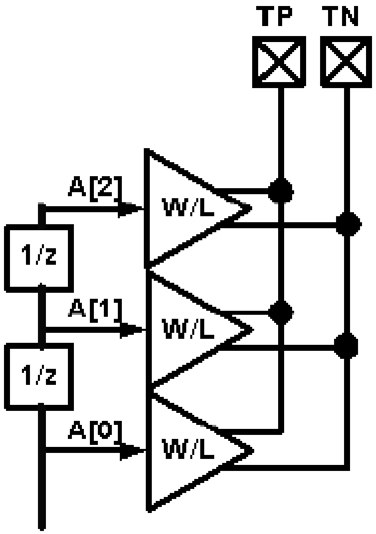


- Generally, TX DAC resolution is limited to between 4 to 6bits
- Mapping these equalization coefficients with this resolution may impact performance

TX FIR Circuit Architectures

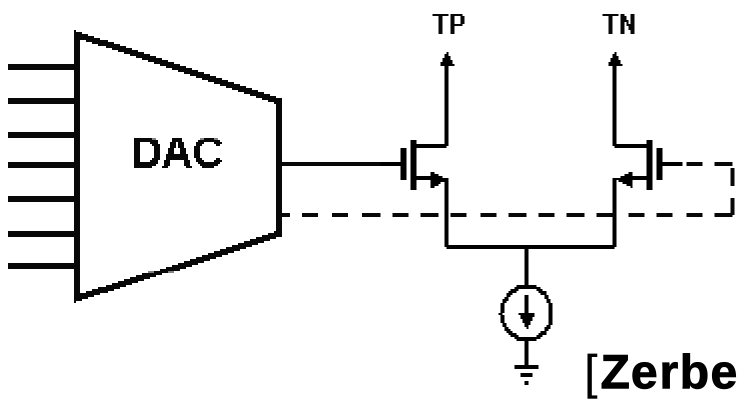
- Direct FIR vs Segmented DAC
- Direct FIR
  - Parallel output drivers for output taps
  - Each parallel driver must be sized to handle its potential maximum current
  - Lower power & complexity
  - Higher output capacitance
- Segmented DAC
  - Minimum sized output transistors to handle peak output current
  - Lowest output capacitance
  - Most power & complexity
    - Need mapping table (RAM)
    - Very flexible in equalization

Direct FIR



[Zerbe]

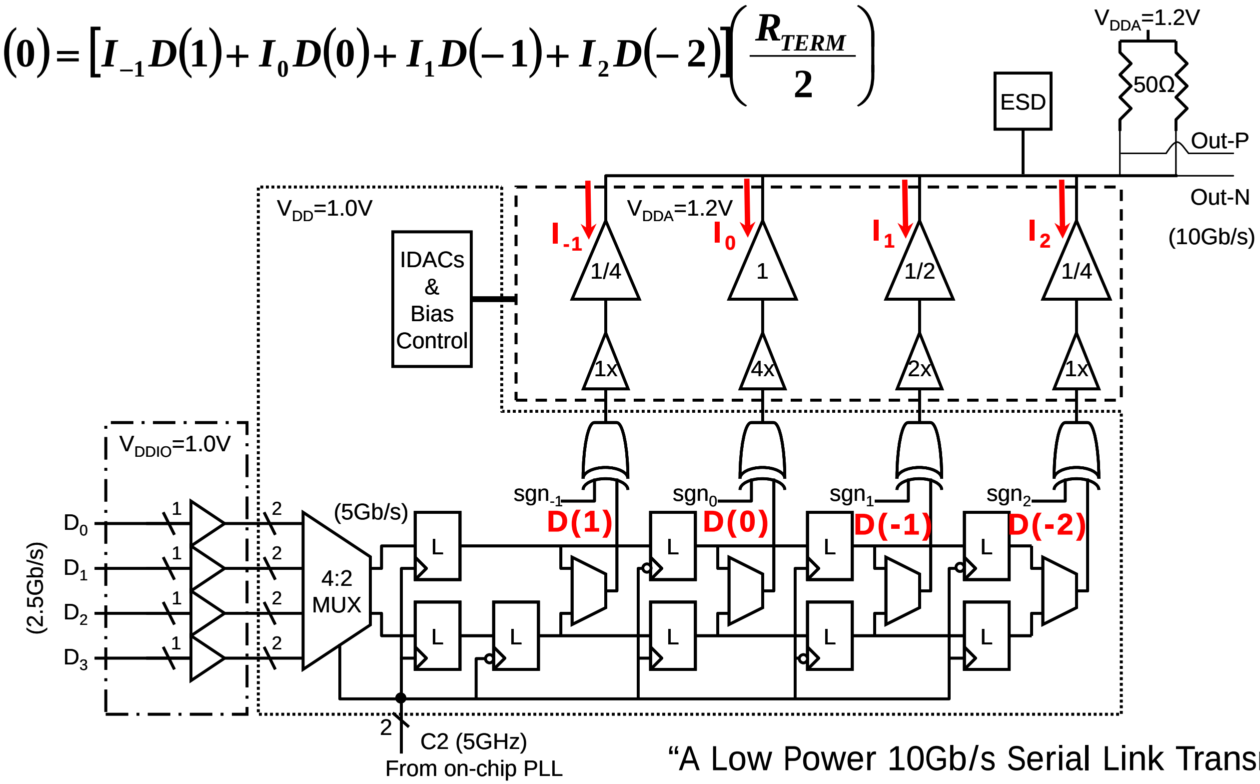
Segmented DAC



[Zerbe]

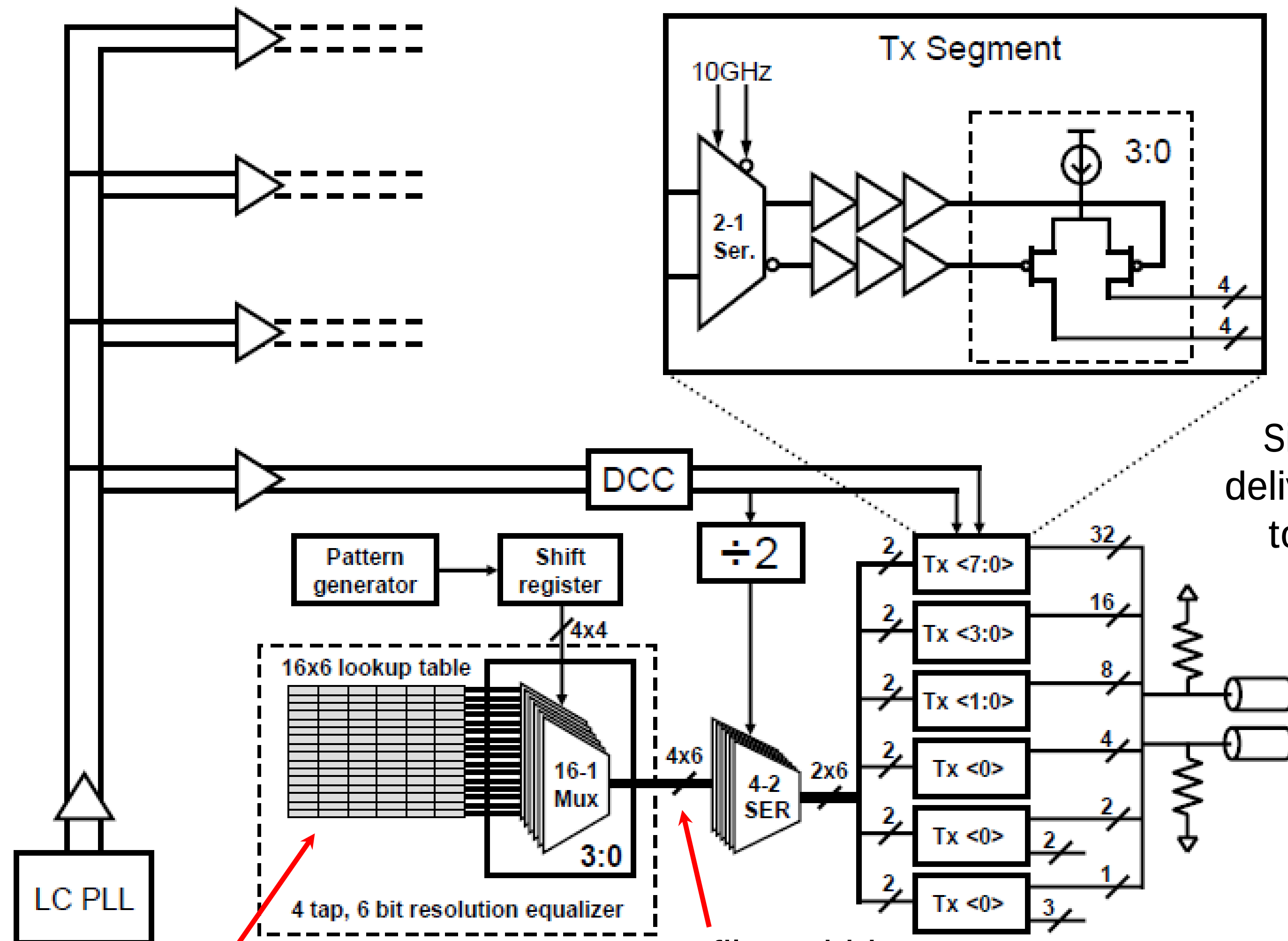
Direct FIR Equalization

$$V_{out}(0) = \left[I_{-1}D(1) + I_0 D(0) + I_1 D(-1) + I_2 D(-2)\right]\left(\frac{R_{TERM}}{2}\right)$$



"A Low Power 10Gb/s Serial Link Transmitter in 90-nm CMOS," A. Rylyakov et al., CSICS 2005

Segmented DAC Example



Sized only to deliver maximum total current

Row = 4-bit data pattern
Column = 6-bit weighting

4 filtered bits (parallel) at 6-bit resolution

[**Casper ISSCC 2006**]

Next Time

- RX FIR
- RX CTLE
- RX DFE
- Alternate/Future Approaches