A PAM3 Simultaneous Bidirectional Transceiver for Die-to-Die Links

As manufacturing costs rise for large monolithic integrated circuits at advanced technology nodes, and shrinking transistors face reliability issues such as electro-migration, aging, and quantum effects, heterogeneous integration has emerged as a practical solution [1-5]. In this approach, systems are partitioned into smaller chiplets, with only the most performance-critical functions implemented in advanced logic processes and then integrated into a system-in-package. This strategy improves yield, cost efficiency, and design flexibility. For compute-intensive domains such as artificial intelligence, high-performance computing, and networking, chiplets demand extremely high-bandwidth, power-efficient die-to-die (D2D) links to maintain system scalability [6].

Various signaling schemes have been explored to fulfill these requirements. While non-return-to-zero (NRZ) signaling is conceptually simple, it faces challenges at high data rates due to bandwidth limitations and increased power consumption in equalization and detection. Multi-level modulation schemes attempt to overcome these limitations by either doubling the throughput per symbol or reducing the Nyquist frequency while maintaining equivalent bandwidth. For instance, pulse-amplitude modulation with four levels (PAM4) transmits two bits per symbol, effectively doubling bandwidth efficiency over NRZ. However, PAM4 suffers from reduced noise margins—since each eye opening is only one-third the height of NRZ—as well as stringent linearity requirements to preserve four distinct levels without distortion [7]. An alternative that has been investigated is simultaneous bidirectional (SBD) signaling, in which NRZ data is transmitted in opposite directions over a single channel [8-11]. Hybrid circuits at each end isolate the incoming data while suppressing reflections of the outbound signal, thereby enabling bandwidth doubling without increasing modulation levels. Nevertheless, NRZ SBD still inherits the limited spectral efficiency of NRZ signaling.

To push beyond these limits, this thesis proposes combining PAM3 modulation with simultaneous bidirectional transmission. PAM3 provides a 50% increase in data rate over NRZ while maintaining larger noise margins than PAM4, making it a promising compromise between complexity and robustness [12]. By integrating PAM3 into an SBD architecture, the proposed transceiver can achieve higher data rates than NRZ SBD while avoiding the linearity requirements of PAM4.

System-level modeling will be performed in MATLAB and Python to characterize PAM3 SBD signaling over representative D2D channels. Comparisons of BER, eye diagrams, and spectral efficiency across NRZ, PAM3, and PAM4 will be used to quantify performance under noise and jitter conditions. Circuit-level design and simulation will be carried out in Cadence and LTspice, focusing on TX drivers, RX front ends, hybrid/echo cancellation circuits, and level detectors.

This work is expected to contribute a novel PAM3 SBD transceiver architecture tailored for die-to-die interconnects, a detailed analysis of tradeoffs between data rate, noise margin, and linearity across NRZ, PAM3, and PAM4 schemes, and circuit-level techniques for hybrid-based echo cancellation in multi-level bidirectional systems. The outcome will be a framework for evaluating PAM3 SBD as a scalable, power-efficient signaling solution for next-generation chiplet interconnects, with potential impact on the design of future AI and HPC systems.

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