Satvik Maurya

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Research Interests

Passionate and motivated about research in computer architecture, especially in the design of Domain Specific Accelerators.

Education

Delhi Technological University (DTU)

Bachelor in Technology, Electronics and Communications Engineering — *August 2014 – May 2018*
First Class with Distinction (Top 15 %) — *80.77 %*

Research Experience

Undergraduate Researcher

Digital System Architecture and Design (DSAD) Group, DTU — *August 2016 – May 2018*
Advisor: Prof. Neeta Pandey

- Worked on research and implementation of the system design of game solvers and AI accelerators using Xilinx's Zynq family of SoCs.
- More details on the work done can be found at: www.dsad.in.

Summer Research Intern

College of Engineering, Pune — *June 2017 – July 2017*
Advisor: Dr. Vaishali Ingale

- Conducted research on Elliptical Curve Cryptography (ECC) and other crypto-systems.
- Designed the entire architecture of a Scalar Point Multiplier for an elliptic curve crypto-processor.

Summer Research Intern

SWARATH, Indian Institute of Information Technology, Delhi — *June 2016 – July 2016*
Advisor: Dr. Sanjit Kaul

- Worked on the autonomous vehicle project-SWARATH of IIIT-Delhi.
- Primarily involved with obstacle detection using RADAR within the Robot Operating System (ROS) and in conjunction with the camera and LIDAR systems.

Publications

- Pranav Gangwar, **Satvik Maurya,** Shubham Garg, Sakshi Goyal, Aditya S. Kumar, Preyesh Dalmia, Neeta Pandey: "*Hardware/Software Co-Design of a High-Speed Othello Solver*", **IEEE 62nd International Midwest Symposium on Circuits & Systems (MWSCAS 2019), Dallas, Texas.**
- **Satvik Maurya,** Vaishali Ingale: "*FPGA Implementation of a Fast Scalar Point Multiplier for an Elliptic Curve Crypto-Processor*", **Lecture Notes in Networks and Systems, vol 38. Springer, Singapore.**
- **Satvik Maurya,** Pranav Gangwar, Neeta Pandey: "*Realization of Game Tree Search Algorithms on FPGA: A Comparative Study*", **2019 IEEE International Conference on Issues and Challenges in Intelligent Computing Techniques (ICICT 2019), Ghaziabad, India**.
- Jeebananda Panda, **Satvik Maurya**, Radhika Dang, Bhagya Lakshmi Narayanpuram: "*Analysis of robustness of an image watermarking algorithm using the Dual Tree Complex Wavelet Transform and Just Noticeable Difference*", **2016 IEEE International Conference on Signal Processing and Communication (ICSC 2016)**.

Work Experience

Synopsys Inc. — Noida, India

R&D Engineer, I — *June 2018 – May 2019*

R&D Engineer, II — *June 2019 – Present*

- Working on the Synopsys ZeBu emulation platform as a protocol transactor developer. Global R&D owner of the HDMI, DSI Host, UART, and I2C transactor solutions.
- Architected, implemented, and verified the entire microarchitecture of the HDMI Transmitter for the HDMI Protocol Specification version 2.1 consisting of the Fixed Rate Link (FRL) data path capable of handling video resolutions up to 8K.
- Architected, implemented, and verified the BFM of the Extended Audio Return Channel Transmitter as specified in the HDMI Protocol Specification version 2.1.
- Designing and integrating the Advanced Link Power Management (ALPM) feature for the Apple Low Power DisplayPort transactor solution.
- Conferred the *Standing Ovation* award thrice (Team and Individual) for contributions in the DSI Host transactor development, HDMI 2.1 transactor development, and UART transactor support and development.

Projects

An Accelerated Connect-6 Game Solver on Xilinx's Zynq SoC

- Decreased latency for move generation by computing the threat patterns of Connect-6 on the FPGA fabric of SoC.
- Currently working on improving the HW/SW communication latency by customizing the AXI Streaming IP that is being used for data transfer.
- Strength of the game solver increased by training the weights of the evaluation function using stochastic gradient descent.

Acceleration of a Twofish-Elliptical Curve Cryptography (ECC) Crypto-system using Xilinx's Zynq SoC

- This case study aimed to highlight the benefits of accelerated architecture of a crypto-system in terms of execution speed and development effort saved.
- A speedup of more than 3x was achieved by shifting the computationally intensive parts (previously profiled) of the Twofish-ECC crypto-system to the FPGA in the Zynq SoC.
- A gain of nearly 6 weeks in development time was also achieved over a pure hardware approach.

Technical Skills

Programming languages	C, C++, Perl, Python, MATLAB
HDLs and HVLs	Verilog, System Verilog
Tools	Xilinx ISE, Xilinx Vivado, Synopsys VCS, Synopsys Verdi, Synopsys Spyglass, Synopsys ZeBu, Icarus Verilog

Achievements

- Secured an All India rank of 1145 (99.74 percentile) in the Joint Entrance Exam (JEE) Mains, 2014.
- Secured an All India rank of 4851 in the Joint Entrance Exam (JEE) Advanced, 2014.
- Letter of Commendation from the Minister of Human Resource Development, Government of India for 100% score in Mathematics in the class XII All India Senior Secondary Certificate Examinations conducted by CBSE, 2014.
- Certificate of Merit for being among top 0.1 percent of successful candidates in Mathematics, All India Senior School Certificate Examination, CBSE, 2014.
- Completed volunteering assignments as a content developer for eVidyaLoka, an NGO focused on the education of underprivileged children in India (from June 2016 to July 2017).
- Completed the eYantra Robotics Competition 2015 which involved more than 3000 teams from all around the country.
- Received "Best Paper" award for the research paper titled "*Realization of Game Tree Search Algorithms on FPGA: A Comparative Study".*