Satvik Maurya

PhD Student · Electrical and Computer Engineering

University of Wisconsin-Madison

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Education

University of Wisconsin-Madison — *Madison, WI, USA*

PhD Electrical and Computer Engineering — *January 2021 - present*

- Advisor: Prof. Swamit Tannu

Delhi Technological University (formerly DCE) — *Delhi, India*

Bachelor of Technology Electronics and Communications Engineering — *August 2014 - May 2018*

- Undergraduate research advisor: Prof. Neeta Pandey

Professional Experience

AMD Research — *Austin, TX, USA*

Summer Intern — *May 2022 - August 2022*

- Worked on an heterogeneous workload framework for characterizing the power management firmware on the latest AMD EPYC server SoCs.
- Identified suboptimal behavior in the Dynamic Power Management algorithm using performance counters for phases where compute-bound and memory-bound workloads were running concurrently.
- Submitted a research paper to an internal AMD conference and an IDF during the internship.

Synopsys, Inc. — *Noida, UP, India*

R&D Engineer, II — *June 2018 - December 2020*

- Worked on the Synopsys ZeBu emulation platform as a protocol transactor developer. Global R&D owner of the HDMI, DSI Host, UART, and I2C transactor solutions.
- Responsible for designing and testing synthesizeable protocol IP using Verilog - Designed the HDMI 2.1 Tx, eARC, Video IPs.
- Also responsible for designing and testing the C++ interface for all transactors which included the partitioning of logic between hardware and software as well debugging complex, multi-threaded test cases.

Publications

Published

Satvik Maurya, Chaithanya Naik Mude, William D. Olliver, Benjamin Lienhard, Swamit Tannu: "Scaling Qubit Readout with Hardware Efficient Machine Learning Architectures", 50th International Symposium on Computer Architecture (**ISCA 2023**), Orlando, Florida, USA.

Satvik Maurya, Swamit Tannu: "COMPAQT: Compressed Waveform Memory Architecture for Scalable Qubit Control", 55th IEEE/ACM International Symposium on Microarchitecture (**MICRO 2022**), Chicago, Illinois, USA.

Satvik Maurya, Heather Hanson, Yasuko Eckert, Raj Desikan: "Making a Case for Heterogeneous Workload Tests for More Robust Dynamic Power Management", Annual AMD Global Technical Authors Conference 2022 (**GTAC'22**).

Pranav Gangwar, **Satvik Maurya**, Shubham Garg, Sakshi Goyal, Aditya S. Kumar, Preyesh Dalmia, Neeta Pandey: "Hardware/Software Co-Design of a High-Speed Othello Solver", IEEE 62nd International Midwest Symposium on Circuits and Systems (**MWSCAS 2019**), Dallas, Texas, USA.

Satvik Maurya, Vaishali Ingale: "FPGA Implementation of a Fast Scalar Point Multiplier for an Elliptic Curve Crypto-Processor", Lecture Notes in Networks and Systems, vol 38. Springer, Singapore.

Research Experience

University of Wisconsin-Madison *Madison, WI, USA*
Advisor: Prof. Swamit Tannu *January 2021 - Present*
- Scalable classical control architectures for quantum computers.

College of Engineering, Pune *Pune, MH, India*
Advisor: Prof. Vaishali Ingale *June 2017 - August 2017*
- High-performance encryption engine for Elliptical Curve Cryptography.

Delhi Technological University *Delhi, India*
Advisor: Prof. Neeta Pandey *2016-2018*
- HW/SW Co-Design architectures using Xilinx Zynq SoCs for AI and ML applications.

Projects

Load Value Predictor: Implemented the load value prediction unit for an out-of-order CPU and an in-order CPU in the Gem5 simulation environment.

Game Solver for Connect-4 using CUDA and OpenMP: Implemented a Connect-4 game solver using CUDA and OpenMP.

Graph Neural Network (GNN) Accelerator: Full ASIC design flow for a GNN accelerator – architecture, RTL design with Verilog, synthesis with Synopsys Design Compiler, timing with Synopsys PrimeTime.

Technical Skills

Proficient Python · Verilog · C/C++

Moderately proficient Perl · CUDA C++ · OpenMP · MATLAB

Familiar MPI (C++) · SystemVerilog

Tools Gem5 · Qiskit · Xilinx Vivado · Synopsys Spyglass · Synopsys VCS · Synopsys Design Compiler · Perforce · Git

Awards & Grants

2022 **MICRO 2022 Travel Grant**, MICRO 2022 Organizing Committee *$585*
2022 **Hiran Mayukh Award**, UW Computer Architecture

Service & Professional Development

Service

2022 **55th International Symposium on Microarchitecture (MICRO 2022)**, Artifact Evaluation Program Committee
2021-present **ECE Graduate Student Association**, Treasurer

Professional Memberships

Association of Computing Machinery (ACM)
American Physical Society (APS)