VIVADO: Performing synthesis
XILINX: Creating Schematic circuits

Lab Assignment 2

Title: Implementing Circuit of Assignment 1

Learning Objective:

Learn how to synthesize a circuit and implement it on BASYS-3 FPGA board.

Specification:

Implement the circuit designed in assignment 1 on BASYS-3 FPGA board, connecting the inputs to slide switches and outputs to LEDs.

Details:

Connections between inputs/outputs of logic circuits and physical resources of the FPGA board (such as switches and displays) are specified using a constraint file. The lift logic circuit of Assignment 1 has 16 inputs and 2 outputs. Associate the inputs to the 16 slide switches available on the BASYS-3 board and outputs to 2 of the 16 LEDs. This is to be done by suitably modifying "Basys-3-Master.xdc" file that has been posted on moodle.

After creating a constraint file, the circuit can be synthesized. For synthesis, it is required to convert the schematic diagram into a VHDL file. Instructions for this are given in file "VHDL Generation Tutorial". Instructions for performing synthesis are given in file "Vivado Tutorial". Synthesis results in creation of a configuration file for FPGA (bit file). Downloading this into the FPGA board implements the circuit.

Basys-3 reference manual has also been posted on moodle.