**Computer Architecture (COL 216)**

# II Semester 2019-2020

**Assignment 9:** Overcoming Data Hazards in a Pipelined Processor

Deadline: 11th April, 2020

The pipelined processor does not function efficiently if it is stalled on every hazard. Use the ideas discussed in class to overcome data hazards in your processor simulation. (Ignore branch hazards).

Compare the performance (in clock cycles) of the two processors simulated in Assignments 8 and 9.