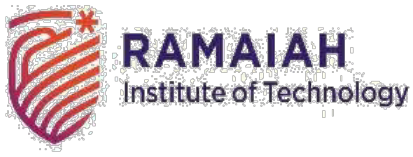

RAMAIAH INSTITUTE OF TECHNOLOGY

(Autonomous Institute affiliated to VTU),Banglore

Dept. of Electronics and Communication Engineering

MIXED SIGNAL IC DESIGN - ECE641

Report On

An Optimized Compensation Strategy for Two-Stage CMOS OP AMPS

Submitted to

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Contents

1 Introduction

- **Project Overview:** Designed a standard two-stage operational amplifier (opamp) and enhanced it using Miller compensation and a nulling resistor.
- **Design Platform:** Utilized Cadence Virtuoso for the entire design and simulation process.

1.1 Two-Stage Opamp Architecture

- **Differential Amplifier:** Offers high input impedance and good common-mode rejection ratio (CMRR).
- **Gain Stage:** Provides necessary amplification to achieve high open-loop gain.
- **Challenges:** Stability issues due to inherent poles introduced by each stage.

1.2 Miller Compensation

- **Purpose:** Address stability concerns.
- **Technique**: Added a Miller capacitor between the output of the gain stage and the inverting input of the differential stage.
- **Effects:** Shifts the dominant pole to a lower frequency.
  Introduces a left-half plane (LHP) zero, improving phase margin and stabilizing the opamp.

1.3 Nulling Resistor

- **Issue with Miller Capacitor:** Potential introduction of a right-half plane (RHP) zero, degrading phase margin.
- **Solution:** Introduced a nulling resistor in series with the Miller capacitor.
- **Effect:** Shifts the RHP zero back to the LHP, enhancing stability and overall performance.

2 Design of a simple Two Stage Op-amp

2.1 Circuit

- The basic structure of a two-stage opamp was designed, consisting of a differential amplifier followed by a gain stage.
- Three NMOS transistors were used at the bottom of the circuit as current mirrors to ensure constant current through the differential amplifier and gain stage.
- The following pins were defined and created: vin+ (non-inverting input), vin- (inverting input), chipvdd (positive power supply), chipgnd (ground), ibias (bias current input), and vout (output voltage).
- The width (W) and length (L) ratios for each transistor were specified. Multiple transistors were used in parallel for higher current capacity and other design requirements.
- A symbol representation of the opamp was generated from the completed cell view to simplify its use in larger designs.
- A new schematic was designed and the created opamp symbol was inserted into this schematic.
- The opamp was connected in a unity gain configuration by connecting the output (vout) to the inverting input (vin-). The non-inverting input (vin+) serves as the input to the buffer.
- Inductors were included in the circuit to nullify the effect of parasitic inductance developed in the design, ensuring better performance and stability.

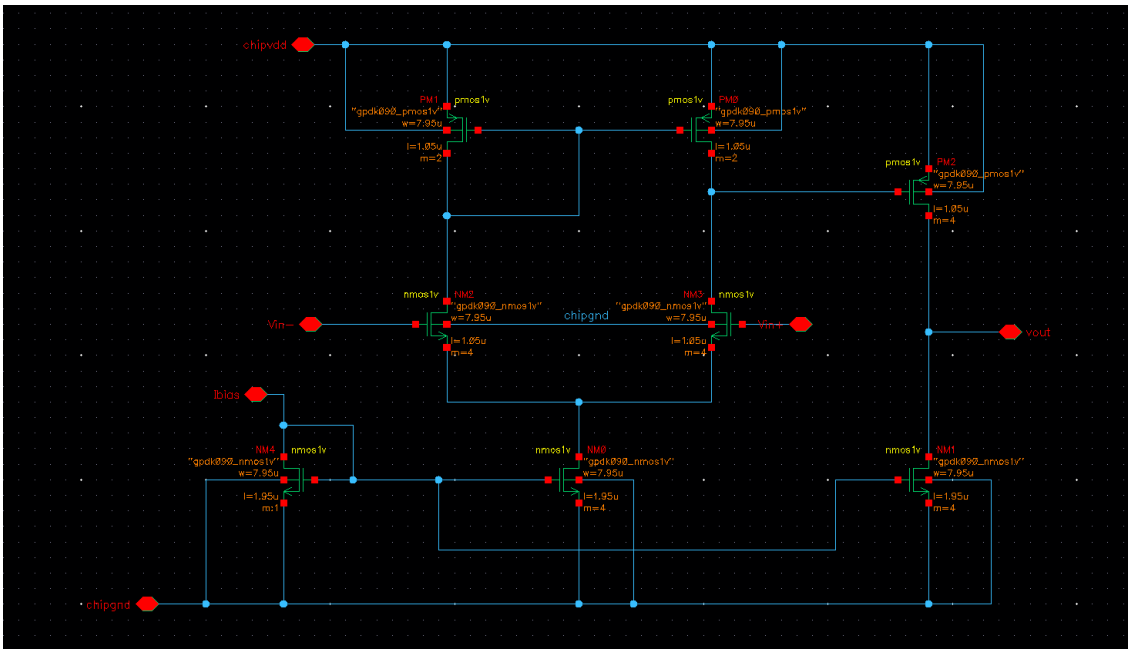

Figure 1: Two Stage Op-Amp circuit

M1, M2: W/L = 32 µm/1µm ≈ 7.95×4 µm /1.05 µm;
M3, M4: W/L = 16 µm/1µm ≈ 7.95×2 µm /1.05 µm;
M8: W/L = 32 µm/1µm ≈ 7.95×4 µm /1.05 µm;
M5: W/L = 32 µm/2µm ≈ 7.95×4 µm /1.95 µm;
M6: W/L = 8 µm/2µm ≈ 7.95×1 µm /1.95 µm;
M7: W/L = 32 µm/2µm ≈ 7.95×4 µm /1.95 µm;

Figure 2: Standard Transistor Sizes

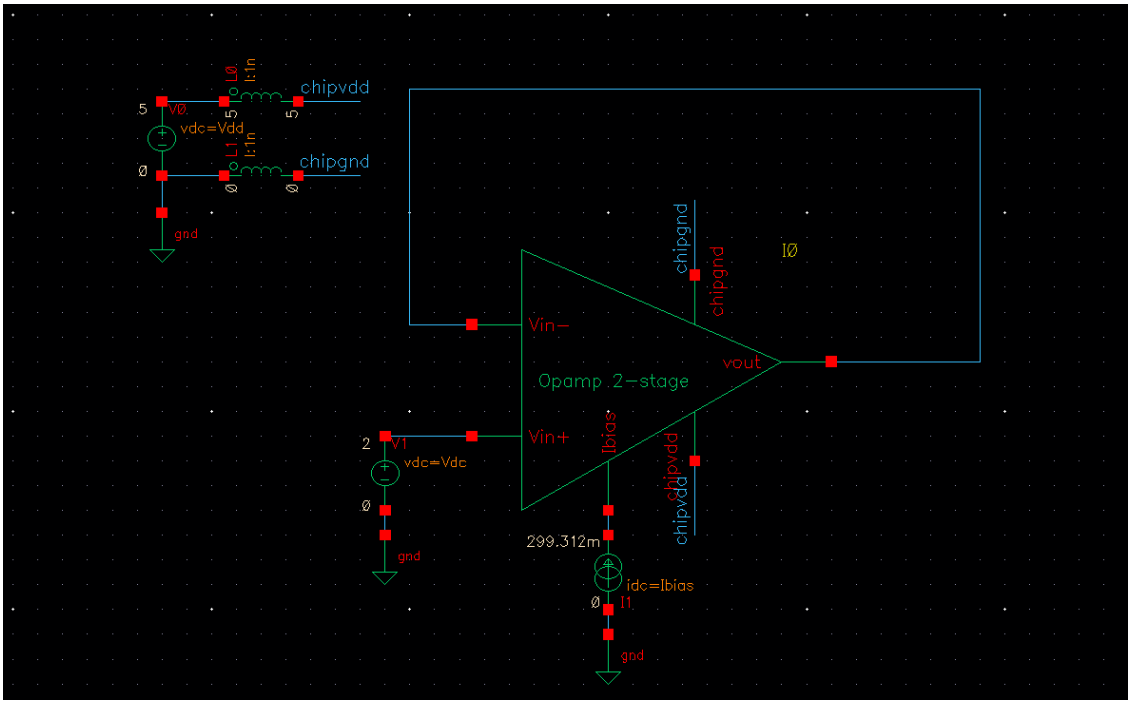

Figure 3: Two Stage Op-Amp Symbol

2.2 DC Analysis

- Conducted a DC analysis with the variables vdc, vdd, and ibias set to 2V, 5V, and 10uA respectively. Employed vdc as the sweep variable.
- Observed in the graph that initially, the input voltage matched the output voltage within the saturation region.
- As the analysis progressed, noted a divergence between the input and output voltages, indicating that they were no longer within the saturation region.
- This observation suggests that the circuit is operating correctly, with the input and output voltages behaving as expected within and outside the saturation region, respectively.

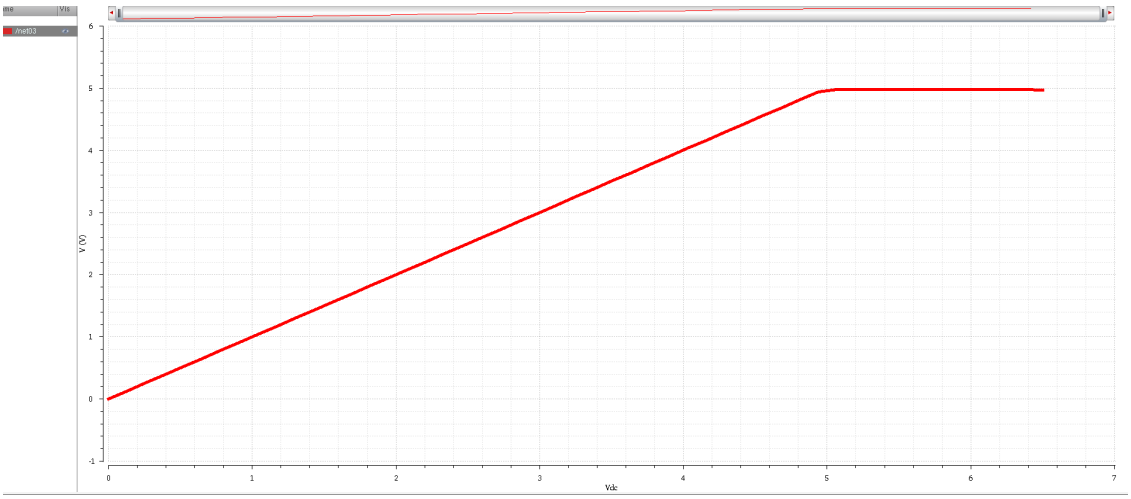

Figure 4: DC Analysis Plot of Two stage op-amp

2.3 Loop Gain using Stability Simulation

- Connected a DC voltage source with V=0 in series with the feedback path, effectively short-circuiting it.
- Performed a stability (STB) analysis and selected the probe instance as the DC voltage (vdc) in series.
- Plotted both the magnitude and phase of the loop gain.
- Observed a negative phase margin of -15.3 degrees and negative gain margin of -20.74 dB in the plot.
- This negative phase margin indicates instability in the system, necessitating the addition of Miller capacitance to stabilize the circuit.

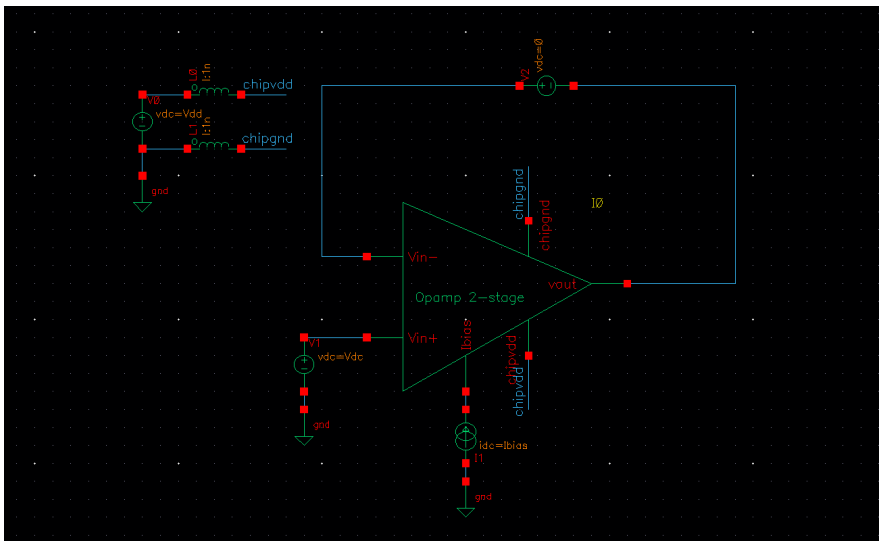

Figure 5: Circuit for STB Analysis

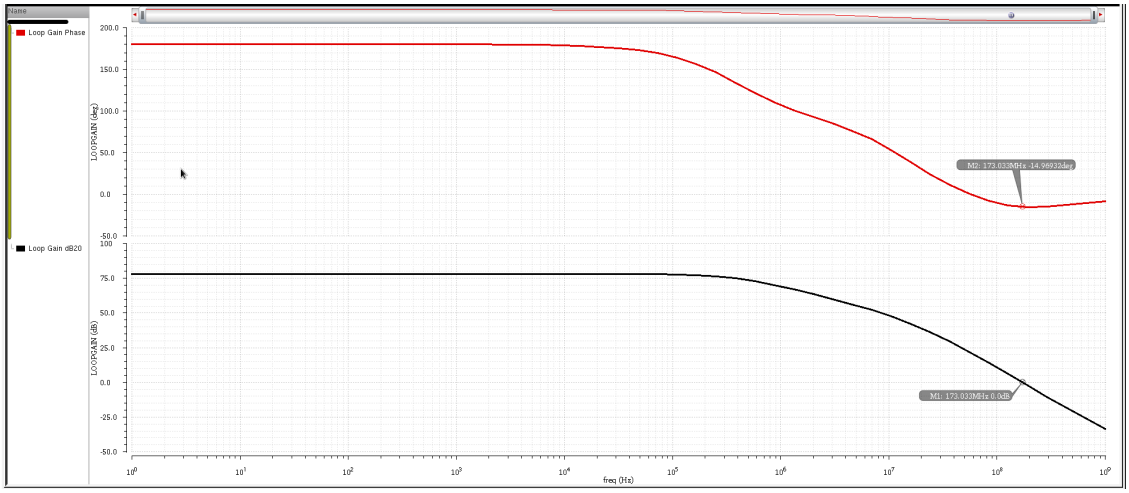

Figure 6: Magnitude and Phase Margin Plot for Gain

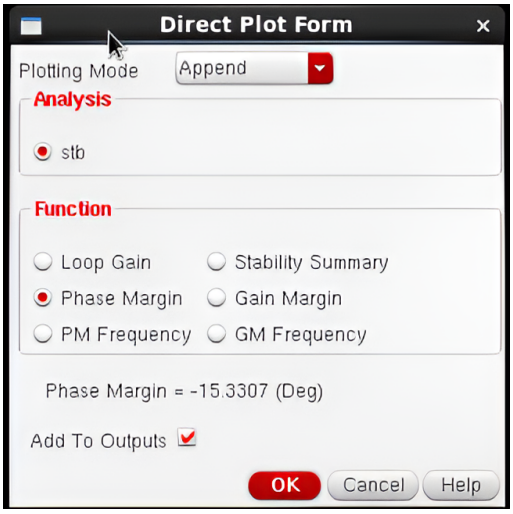

Figure 7: Phase Margin

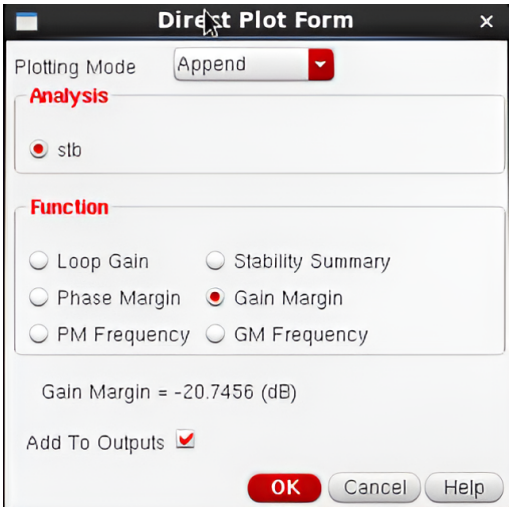

Figure 8: Gain Margin

3 Design of Miller Compensated Op-amp with nulling resistor

3.1 Circuit

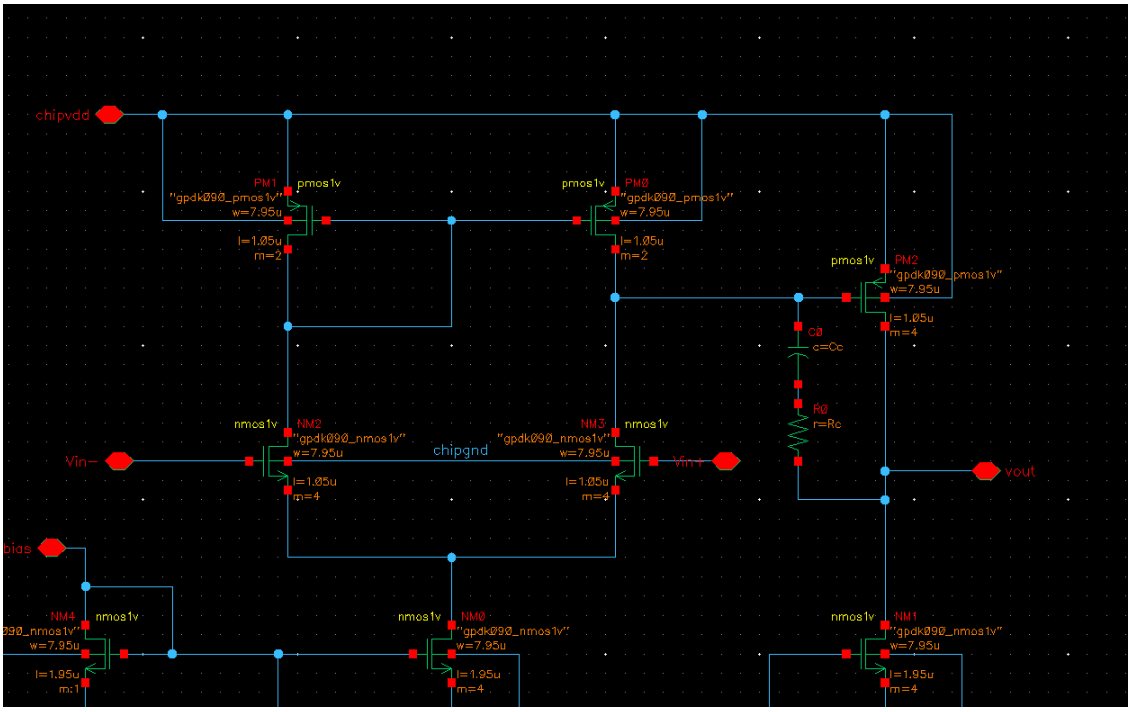

Figure 9: Two Stage Op-Amp in Millers Circuit

3.2 Parametric Analysis of Nulling Resistor and Miller's Capacitance

- Conducted a parametric analysis of Miller capacitance and nulling resistor to determine the best values.
- We observe in the graph that maximum phase margin is obtained at r= 4 kilo ohms
- Based on the graph, the optimal values are found to be:
  Miller capacitance (C) = 1 pF
  Nulling resistor (R) = 4 kilo ohms
- These values were identified as providing the most favorable performance characteristics for the circuit.

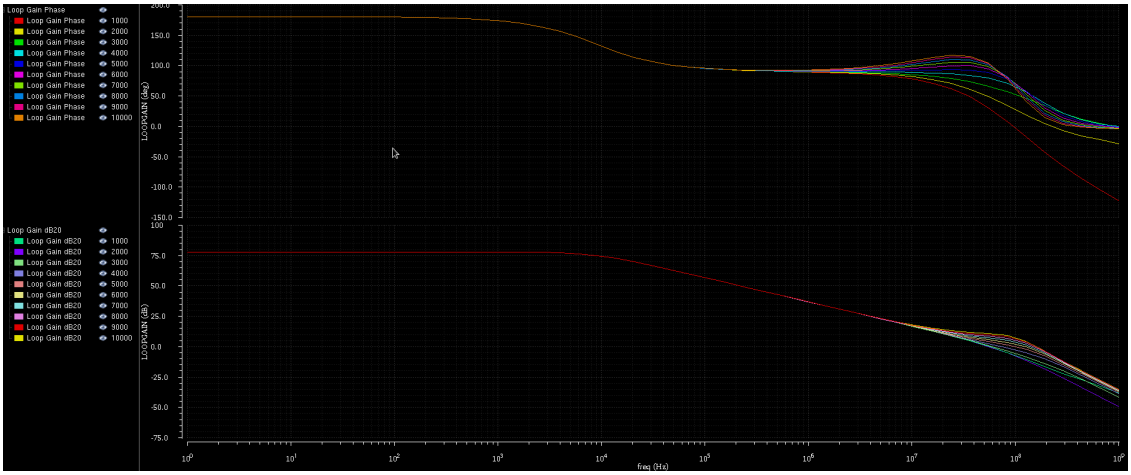

Figure 10: Parametric Analysis

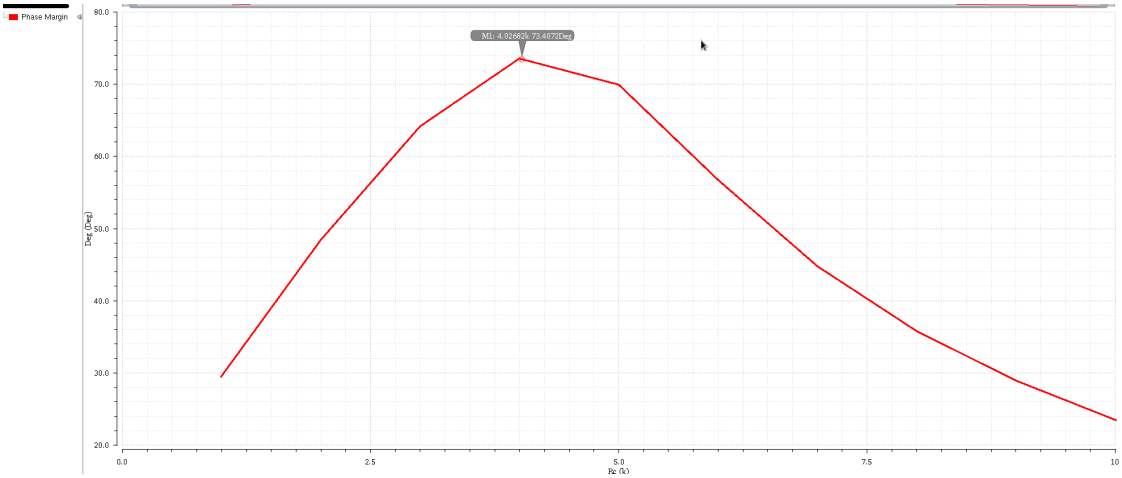

Figure 11: Phase Margin Variation with Resistance

3.3 AC Analysis

- By Setting the value of resistance as 4 kilo ohms, AC Analysis was conducted for 1Hz to 1GHz.
- We can observe in the graph, that the Phase Margin Achieved is 73 degrees and Gain Margin is 1.1dB which is more than two stage op-amp with no compensation.

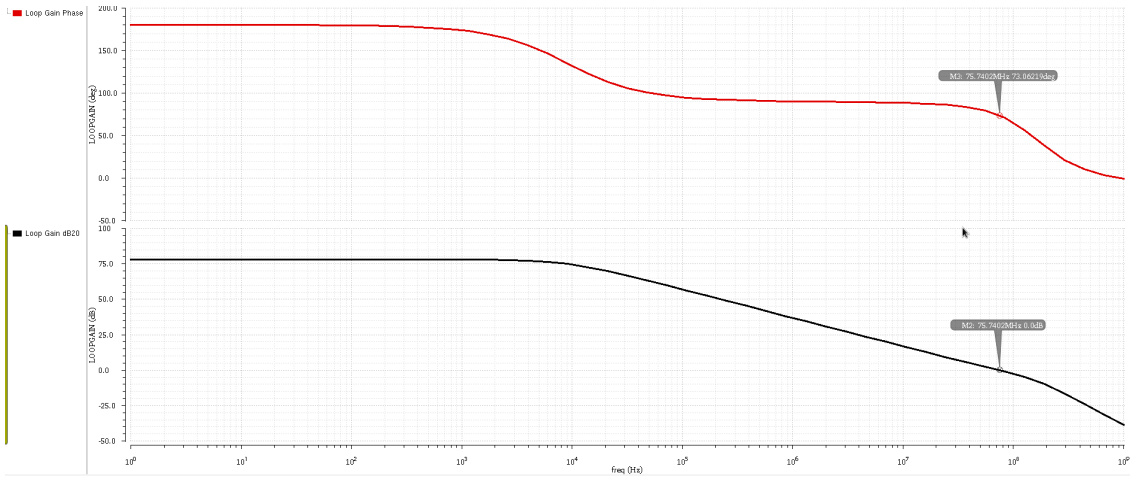

Figure 12: Phase Margin

3.4 Closed Loop Output Impedance Using XF Analysis

- **Setup for XF Analysis**:
  - Insert a current source with 0A in parallel to the output.
  - Perform an XF analysis with a frequency sweep from 1 Hz to 1 GHz.
- **Observation from Graph**:
  - At 127 MHz, the highest value of output impedance is observed to be 3.27 k ohms.

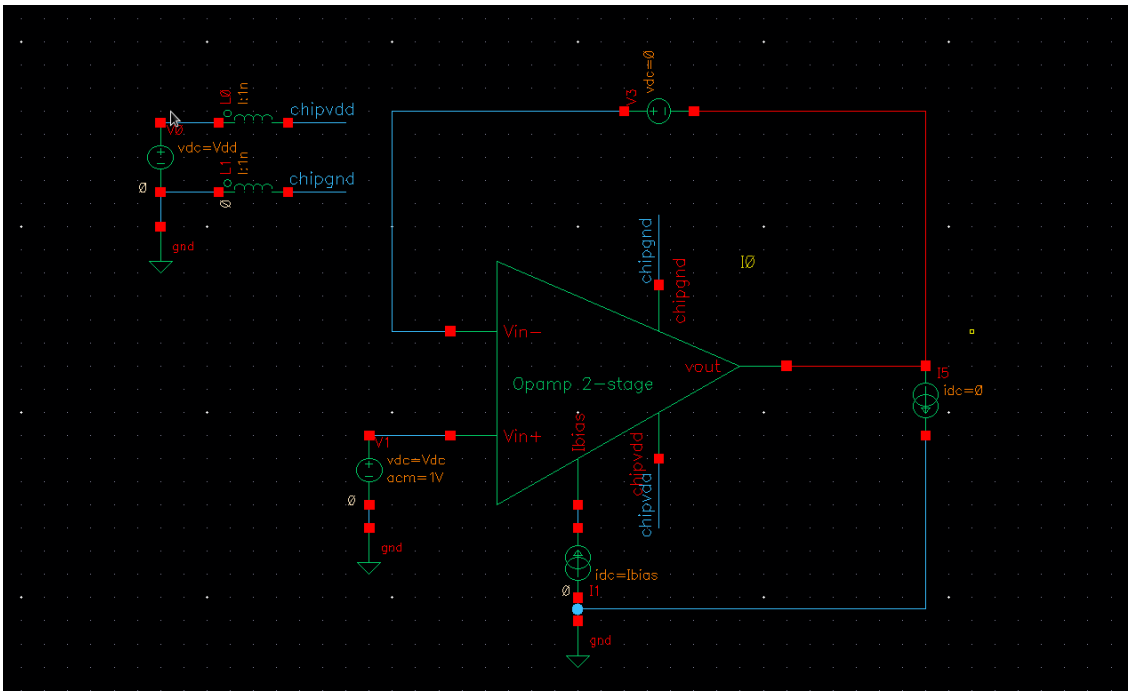

Figure 13: Phase Margin

3.5 Variation of Phase Margin with Temperature

From the Graph below, we can observe the the Phase Margin decreases with increase in temperature.

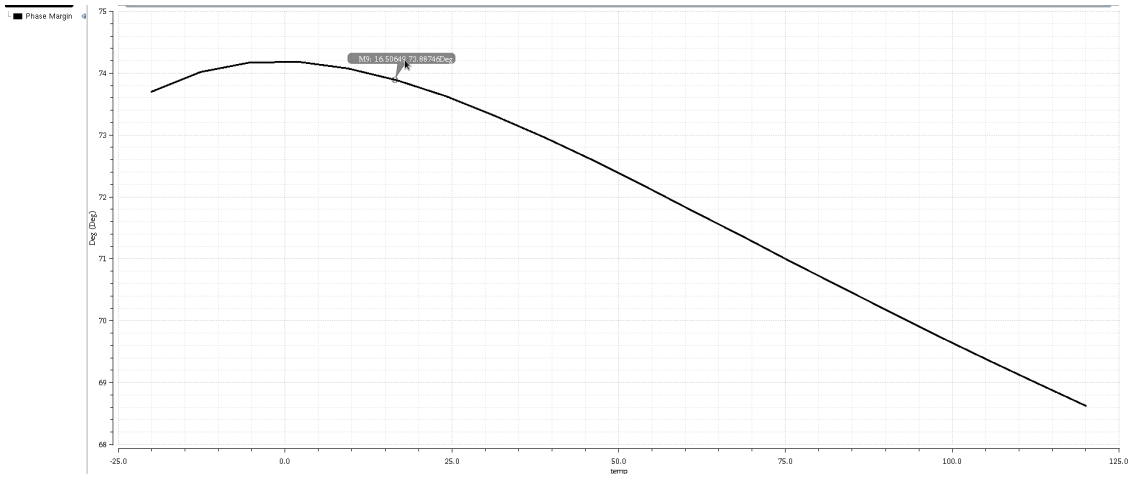

Figure 14: Variation of Phase Margin with Temperature

4 Applications

The designed two-stage operational amplifier with Miller compensation and a nulling resistor has several applications, including:

- **Signal Conditioning**: Used in various signal conditioning circuits to amplify and filter signals for further processing.
- **Analog Filters**: Utilized in the design of active analog filters, which are essential in communications and signal processing systems.
- **Sensor Interfaces**: Serves as an interface for sensors by amplifying low-level signals from sensors to usable levels.
- **Data Acquisition Systems**: Integral part of data acquisition systems where precise amplification of signals is required before digitization.
- **Voltage Followers**: Employed as a voltage follower (buffer) in circuits to provide high input impedance and low output impedance.
- **Comparators**: Used in comparator circuits to compare input voltages and produce a digital output based on the comparison.
- **Analog Computation**: Facilitates analog computation tasks such as integration, differentiation, summation, and subtraction in analog computers.
- **Feedback Control Systems**: Critical component in feedback control systems, ensuring stability and accurate control of system parameters.
- **Switched-Capacitor Circuits**: Applied in switched-capacitor circuits in analog-to-digital and digital-to-analog converters.
- **Audio Amplifiers**: Used in audio amplification systems to provide clear and distortion-free audio signals.

5 Conclusion

- **Optimal Values Identified**:
  - Miller capacitance: 1 pF
  - Nulling resistor: 4 kΩ
- **Improvements Achieved**:
  - **Gain Margin**:
    - Improved from -20 dB to 1.1 dB
  - **Phase Margin**:
    - Improved from -15.3 degrees to 73 degrees
- **Key Takeaway**:
  - Miller compensation significantly enhances the stability and performance of the two-stage operational amplifier, resulting in a more stable and reliable circuit.
  - From the XF analysis, the highest output impedance was observed to be 3.27 kΩ at 127 MHz.