External Gate Resistor Design Guide for Gate Drivers

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External gate drive resistors play a crucial part in limiting noise and ringing in the gate drive path. Parasitic inductances and capacitances, high dV/dt and di/dt, and body-diode reverse recovery can cause unwanted behavior without an appropriately sized gate resistor.

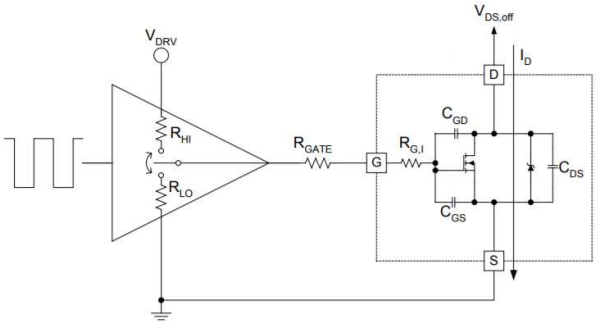

Figure 1. Gate Drive Elements

Figure 1 depicts common elements in the gate drive path: the internal resistance of the gate driver, external gate resistance, and internal gate resistance of the MOSFET or IGBT. R_{GATE} is the only component that tunes the gate drive waveform.

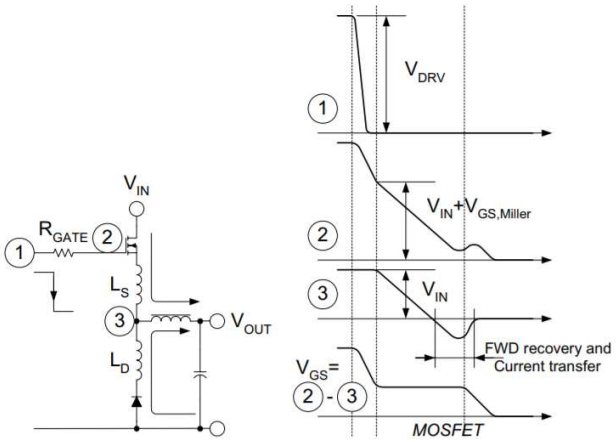

Figure 2. Switching Theory

Figure 2 shows the parasitic inductances and their effect on the gate drive waveform created by long trace length and poor PCB design.

These parasitics cause oscillations in the gate drive loop and are modeled by resonant circuits. Fortunately, the otherwise very high Q resonance between the input capacitance, C_{ISS} (C_{GD} + C_{GS}) and the source inductance, L_S can be damped by the series resistive components of the loop, R_G ($R_G = R_{HI\ or\ LO}+R_{GATE}+R_{G,I}$).

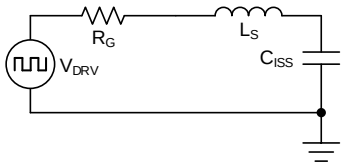

Figure 3. Resonant Circuits in Gate Drive Design

An optimum gate resistor selection is key for a high performance design. Without optimization, small resistor values will result in an overshoot in the gate drive voltage waveform but also result in faster turn-on speed. Also, higher resistor values will overdamp the oscillation and extend the switching times without offering much benefit for the gate drive design.

Select a gate resistor that will give your design a quality factor Q between 0.5 (critically damped) and 1 (under damped). A quality factor greater than 0.5 will give you faster turn-on and turn-off if needed. Start by recording the gate drive ring with no external resistance. This is your ring frequency f_R used in Equation 1. The MOSFET or IGBT's datasheet provides the input capacitance, C_{ISS}, which will help you calculate the source inductance L_S.

$$L_S = \frac{1}{C_{ISS}\left(2\pi f_R\right)^2} \quad (1)$$

Determine when the series resistance R_G is equal to or twice the inductor's reactance, for under damped or critically damped performance. The external gate resistor is then determined by subtracting the internal gate drive and transistor gate resistance from the total series resistance.

$$Q = \frac{X_L}{R_G} = \frac{\omega L_S}{R_G} \quad (2)$$

The above method is an iterative process starting with 0-Ω as the external gate resistance and calculating a new external gate resistor value based on ring frequency, source inductance, and input capacitance.

This TI TechNote uses two isolated single-channel gate drivers in a half-bridge configuration to provide proof of concept. In the following figures, two UCC5310MC driven from a 15-V supply are used to drive two 100V MOSFETs CSD19536KCS with a typical internal gate resistance, $R_{G,I}$ of 1.4-Ω.

The CSD19536KCS MOSFET was selected due to its relatively small internal gate resistance in order to show the effects of adding external gate resistors. External gate resistors may not be required if a MOSFET or IGBT's internal gate resistance is large enough.

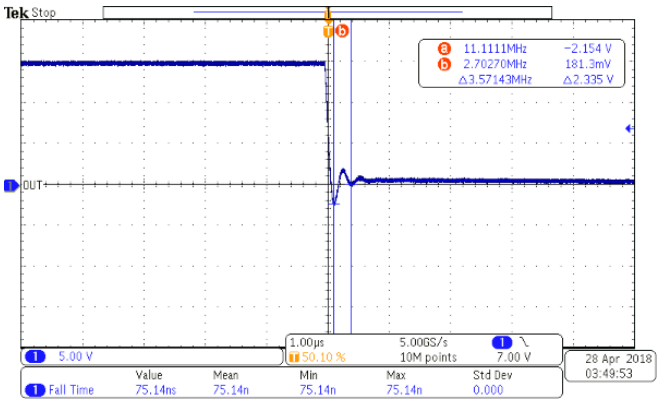

Figure 4. External Gate Resistor R_{GATE} = 0-Ω

At 0-Ω, there is unwanted ringing on the gate-source waveform. The internal gate resistance of the CSD19536KCS MOSFET is not enough to dampen the oscillations found in Figure 4.

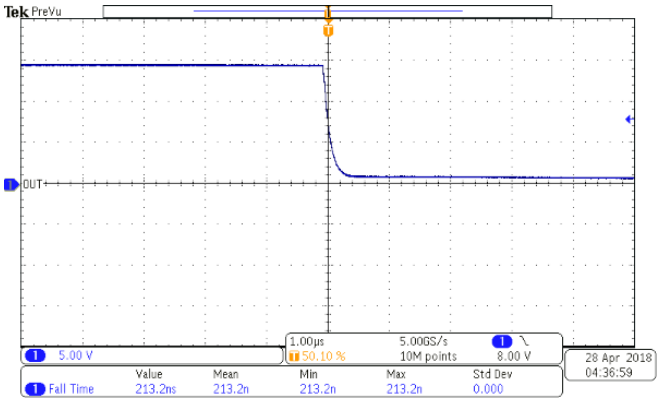

Figure 5. Critically Damped External Gate Resistor R_{GATE} = 7-Ω

Using 3.57MHz as the ring frequency and 9250-pF as the input capacitance, a critically damped resistor value is determined using Equation 1 and Equation 2. Don't forget to subtract the series resistive elements $R_{G,I}$ and $R_{HI\ or\ LO}$ from this calculated value. Figure 5 demonstrates the effects of adding a 7-Ω resistor to the gate drive path which makes the waveform critically damped.

The selection of the external gate resistor will affect three things: drive current, gate-driver power dissipation, and rise and fall times. Figure 4 and Figure 5 show the gate resistor's dampening effect and its effect on rise and fall times.

If the rise and fall times are too slow after adding an optimized gate resistor, another option is to calculate your gate resistor with a Q-factor set to 1. This will promote an under damped solution and caution should be used to prevent overshoot or undershoot. If this doesn't work, look at the source and sink current of your gate driver and find a device with greater peak currents to replace it with. This will charge and discharge your FET at a faster rate but will need a new optimized gate resistor to prevent overshooting.

Generally, another way to decrease the ringing from the series RLC circuit shown in Figure 3 is to minimize loop inductance between the source of the high-side transistor to the source of the low-side transistor. Confining the high peak currents that charge and discharge the transistor gates to a minimum physical area is essential. The gate driver must be placed as close as possible to the transistors to reduce these parasitics.

The trade-off between fast rise and fall times vs oscillations is why the external gate resistor element of the gate-drive design is so valuable.

Table 1. Alternative Device Recommendations

Device	Optimized Parameters	Performance Trade-Off
UCC5350MC	Miller Clamp Feature Available	Requires larger value gate resistor due to higher source/sink current
UCC5320SC	Split Output Feature Available	Need to design a method to prevent miller current induced turn-on
UCC5390EC	UVLO2 referenced to GND2 Feature Available	True UVLO2 monitoring at the expense of not having split output or Miller clamp
UCC21220	Configured as a half-bridge or two low-side drivers	Difficult to layout both transistors close to each output when using a dual channel

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