Faculty of Engineering and Technology			
Ramaiah University of Applied Sciences			
Department	Computer Science and Engineering	Programme	B. Tech. in CSE
Semester/Batch	03/2017		
Course Code	CSC203A	Course Title	Logic Design
Course Leader	Prof. A. Prabhakar, Mr. Deepak V. and Mr. Narasimha Murthy K. R.		

Assignment-2			
Reg.No.		**Name of Student**	

Sections	**Marking Scheme**		**Marks**		
			Max Marks	**First Examiner Marks**	**Moderator**
Part A					
	A.1.1	**Introduction**	**01**		
	A.1.2	**Complexity of ripple-carry and carry-lookahead adders**	**03**		
	A.1.3	**Stance and Justification**	**02**		
		Part-A Max Marks	**05**		
Part B.1					
	B.1.1	**Design and Analysis of Circuit**	**04**		
	B.1.2	**Truth Table**	**02**		
	B.1.3	**Implementation and Simulation**	**04**		
		B.1 Max Marks	**10**		
Part B.2					
	B.2.1	**Introduction**	**01**		
	B.2.2	**Design and Simulation**	**05**		
	B.2.3	**Issues involved in Bus Connections**	**02**		
	B.2.4	**Resolution of the Issues**	**02**		
		B.2 Max Marks	**10**		
		Total Assignment Marks	**50**		

Course Marks Tabulation				
Component-1 (B) Assignment	**First Examiner**	**Remarks**	**Moderator**	**Remarks**
A				
B.1				
B.2				
Marks (out of 25)				

Signature of First Examiner **Signature of Moderator**

Please note:

1. Documental evidence for all the components/parts of the assessment such as the reports, photographs, laboratory exam / tool tests are required to be attached to the assignment report in a proper order.
2. The First Examiner is required to mark the comments in RED ink and the Second Examiner's comments should be in GREEN ink.
3. The marks for all the questions of the assignment have to be written only in the **Component – CET B: Assignment** table.
4. If the variation between the marks awarded by the first examiner and the second examiner lies within +/- 3 marks, then the marks allotted by the first examiner is considered to be final. If the variation is more than +/- 3 marks then both the examiners should resolve the issue in consultation with the Chairman BoE.

Assignment 2

Term - 2

Instructions to students:

1. The assignment consists of **3** questions: Part A-**1** Question, Part B-**2** Questions.
2. Maximum marks is **25**.
3. The assignment has to be neatly word processed as per the prescribed format.
4. The maximum number of pages should be restricted to **10**.
5. Restrict your report for Part-A to 2 pages only.
6. Restrict your report for Part-B to a maximum of 7 pages.
7. The printed assignment must be submitted to the course leader.
8. **Submission Date: 22 October 2018**
9. **Submission after the due date is not permitted.**
10. **IMPORTANT**: It is essential that all the sources used in preparation of the assignment must be suitably referenced in the text.
11. Marks will be awarded only to the sections and subsections clearly indicated as per the problem statement/exercise/question

This course is intended to prepare students to design basic logic circuits and components used in a computer. Students are taught the principles and techniques of sequential and combinational logic circuits. Algorithms, digital logic elements and their optimization for design and implementation of digital logic circuits and their applications are covered. Students are trained to build, simulate and test digital circuits.

Part A **(05 Marks)**

CPUs implement addition using either ripple-carry adders or carry-lookahead adders. In ripple-carry adders, the carry traverses through all the adders. On the other hand, carry-lookahead adders use an additional logic circuit to predict the carry, thereby saving time.

Develop a debate on the topic **"A ripple-carry adder is faster than a carry-lookahead adder"**.

Your debate should emphasize on:

A.1.1 Introduction
A.1.2 Comparison of the complexity of ripple-carry adders and carry-lookahead adders
A.1.3 Stance and justification

Part B **(20 Marks)**

B.1 **(10 Marks)**

Design a combinational circuit block that can function both as 8:3 encoder and 8:1 multiplexer. There are fourteen inputs and three outputs to this block. One of the inputs is used to toggle between encoder and multiplexer operation.
Include the following in your report:

B.1.1 Design of the circuit and analysis of its shortcomings
B.1.2 Truth table for encoder and multiplexer
B.1.3 Implementation and simulation

B.2 **(10 Marks)**

The students are required to design and simulate an 8 bit Arithmetic and Logic Unit (ALU) using Logisim. The ALU should be able to perform arithmetic and logical operations.
Note: Contact the course leader for information about the arithmetic and logical operations that you have to design for.
The report should emphasize the following:

B.2.1 Introduction
B.2.2 Documentation of the design and simulation processes
B.2.3 Issues involving connecting four such ALUs to the CPU bus
B.2.4 Resolution of the issues identified above