

Laboratory 6**Combinational Circuits-II
Multiplexers and Demultiplexers****1. Introduction and Purpose of Experiment**

Students will learn to design, simulate and implement circuits using Multiplexers and Demultiplexers.

2. Aim and Objectives

Aim: To verify functionality of Mux and Demux and use Multiplexer to implement Boolean functions

Objectives: At the end of this lab, the student will be able to

- Verify the functionality of Mux and Demux
- Use Multiplexers to implement given Boolean Functions

3. Experimental Procedure**a. Write truth tables and block diagrams for**

- I. 4 to 1 Multiplexer
- II. 8 to 1 Multiplexer
- III. 1 to 4 Demultiplexer
- IV. 1 to 8 Demultiplexer

- b. Construct the circuits for 3 (a) (I) to 3 (a) (IV) above using appropriate ICs. Verify the functionality and show the output to the course leader
- c. Use Logisim to simulate the circuits designed above.
- d. Using an example, show how any Boolean Expression in SoP form can be implemented using a Multiplexer. Simulate the same using Logisim.

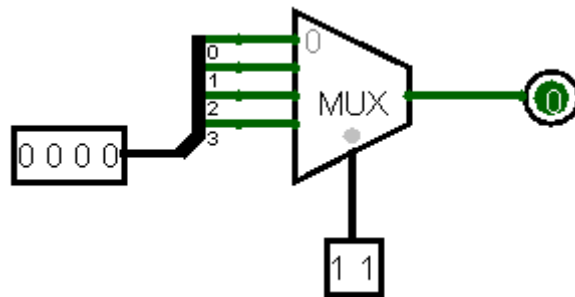
Your document should include:

- Handwritten truth tables and block diagrams for the circuits in 3(a).
- Logisim screenshots of all the Multiplexers and Demultiplexers.
- Answer to 3(d)
- Logisim screenshots for 3(d)

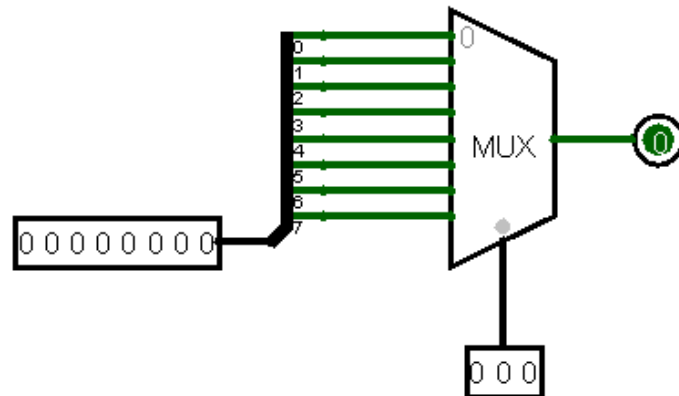
Name: SATYAJIT GHANA

Reg. No: 17ETCS002159

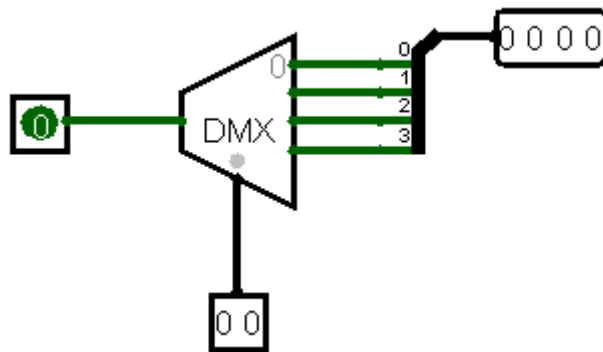
3.a.i



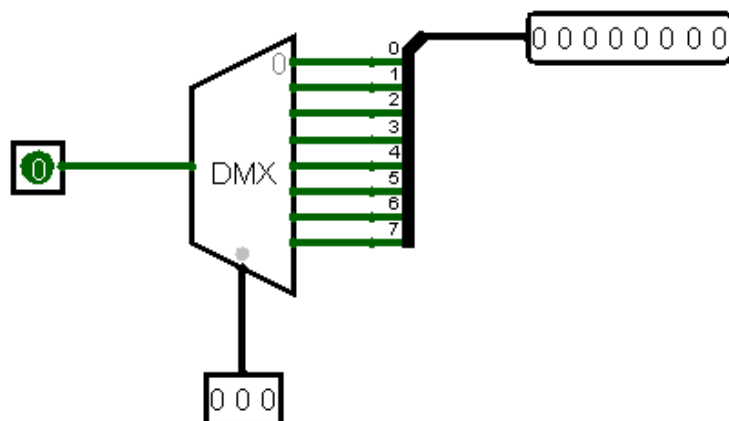
3.a.ii



3.a.iii



3.a.iv



3.d

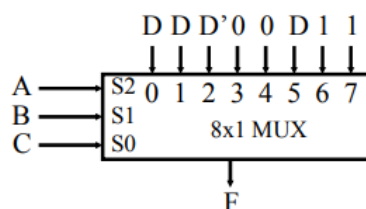
Let's consider a 4-Variable Boolean Expression that is to be implemented using a 8X1 MUX

The SOP form of the expression is given as:

$$F(A, B, C, D) = \sum m(1, 3, 4, 11, 12, 13, 14, 15)$$

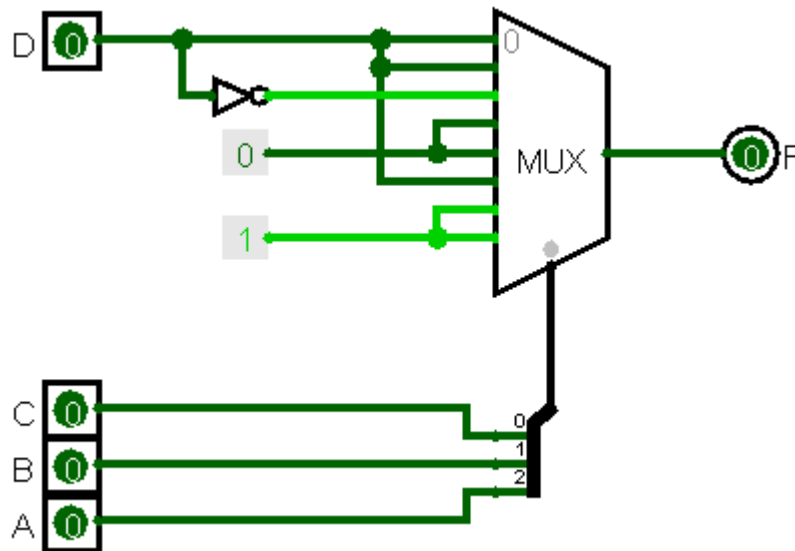
And the truth table can be constructed as follows, the first 3 variables are directly mapped to the Select lines of the multiplexer and the fourth variable is mapped to the input lines, but only as required, i.e. it depends on the Boolean expression, and according to that the fourth variable is mapped.

A	B	C	D	F	
0	0	0	0	0	F=D
0	0	0	1	1	
0	0	1	0	0	F=D
0	0	1	1	1	
0	1	0	0	1	F=~D
0	1	0	1	0	
0	1	1	0	0	F=0
0	1	1	1	0	
1	0	0	0	0	F=0
1	0	0	1	0	
1	0	1	0	0	F=D
1	0	1	1	1	
1	1	0	0	1	F=1
1	1	0	1	1	
1	1	1	0	1	F=1
1	1	1	1	1	



Name: SATYAJIT GHANA
Logisim:

Reg. No: 17ETCS002159



A	B	C	D	F
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1