

Faculty of Engineering and Technology			
Ramaiah University of Applied Sciences			
Department	Computer Science and Engineering	Programme	B. Tech
Semester/Batch	3 <sup>rd</sup> /2017		
Course Code	CSC208A	Course Title	Computer Organization and Architecture
Course Leader	Ms. Chaitra S, Naveeta Rani		

Assignment - 2					
Register No.		Name of the Student			
Sections		Marking Scheme	Marks		
			Max Marks	First Examiner Marks	Moderator
Part-A	A 1.1	Introduction to superscalar processor	01		
	A 1.2	Applications	03		
	A 1.3	Conclusion	01		
		Part-A Max Marks	05		
Part B 1	B 1.1	Pipelined mode of execution with a neat diagram	03		
	B 1.2	Compute the number of clock cycles	02		
		Part-B 1 Max Marks	05		
Part B 2	B2.1	Introduction to split stages	02		
	B2.2	Compute the number of clock cycles	06		
	B2.3	Analyze the performance of 5 stage and 7 stage processor	04		
	B2.4	Best design	02		
	B2.5	Conclusion	01		
		Part-B 2 Max Marks	15		
		Total Assignment Marks	25		

Course Marks Tabulation
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Component- CET B Assignment	First Examiner	Remarks	Second Examiner	Remarks
A				
B.1				
B.2				
Marks (out of 25 )				
<div>Signature of First Examiner</div> <div>Signature of Second Examiner</div>				

**Please note:**

1. Documental evidence for all the components/parts of the assessment such as the reports, photographs, laboratory exam / tool tests are required to be attached to the assignment report in a proper order.
2. The First Examiner is required to mark the comments in RED ink and the Second Examiner's comments should be in GREEN ink.
3. The marks for all the questions of the assignment have to be written only in the **Component – CET B: Assignment** table.
4. If the variation between the marks awarded by the first examiner and the second examiner lies within +/- 3 marks, then the marks allotted by the first examiner is considered to be final. If the variation is more than +/- 3 marks then both the examiners should resolve the issue in consultation with the Chairman BoE.

**Assignment -2**

**Term - 2**

**Instructions to students:**

1. The assignment consists of **3** questions: Part A – **1** Question, Part B- **2** Questions.
2. Maximum marks is **25**.
3. The assignment has to be neatly word processed as per the prescribed format.
4. The maximum number of pages should be restricted to **10**.
5. Restrict your report for Part-A to 1 page only.
6. Restrict your report for Part-B to a maximum of 9 pages.
7. The printed assignment must be submitted to the course leader.
8. **Submission Date: 22/10/2018**

9. **Submission after the due date is not permitted.**
10. **IMPORTANT:** It is essential that all the sources used in preparation of the assignment must be suitably referenced in the text.
11. Marks will be awarded only to the sections and subsections clearly indicated as per the problem statement/exercise/question

**Preamble:**

This course prepares the students to gain a thorough knowledge of the concepts and components of computer organisation and architecture. It introduces the architecture and operation of CPU, memory, Input / Output devices, pipelining and cache concepts. The students are also exposed to modern computing systems and their scope for engineering applications.

**PART – A**

**(5 Marks)**

Traditionally, processors have executed instructions sequentially. As processor architectures evolved, multiple sub-steps of sequential instructions are executed in parallel, leading to pipelined architectures. The next step of evolution involved executing multiple instructions in parallel. These architectures are known as superscalar architectures. Such architectures are susceptible to data dependencies. Hence dependencies need to be resolved before a processor can execute the instructions.

Develop an essay on the topic "***Applications of Superscalar Processors***".

Your essay should emphasize on:

- A1.1** Introduction to superscalar processors
- A1.2** Discussion on applications of superscalar processors
- A1.3** Conclusion

**PART – B**

**(20 Marks)**

**Specification:** An instruction pipeline has 5 stages namely Instruction Fetch (IF), Instruction Decode (ID), Execute (EXE), Memory (MEM) and Writeback (WB). IF stage reads instruction memory, ID stage reads the source register from the register file, EXE stage computes the effective memory address from the source register and the instruction's constant field, MEM stage involves reading the data memory from the address computed by the ALU and in WB stage, the memory value is stored into the destination register.

**B.1**

**10 Marks**

Consider a set of instructions and document relevant assumptions made. Your report should emphasize on:

**B1.1** Explanation of the pipelined mode of execution of the instructions using a suitable diagram depicting various instruction execution phases, for each instruction.

**B1.2** Computation of the number of clock cycles with stage delay as 1ns for 5 stage pipeline processor

**B.2**

Modify the same instruction set to a 7-stage pipeline processor by splitting second and third stages into two stages each i.e., ID stage is split into ID1 and ID2 stages; EXE is split into EXE1 and EXE2. Consider branch instructions. Your report should emphasize on:

**B2.1** Introduction to split stages

**B2.2** Compute the number of clock cycles with stage delay as 1ns including pipeline bubbles for 7 stage pipeline processor

**B2.3** Analyze the performance of 5 stage and 7 stage pipelined processor

**B2.4** Based on the analysis, recommend the best design for high performance computing applications

**B2.5** Conclusion

