Faculty of Engineering and Technology			
Ramaiah University of Applied Sciences			
Department	Computer Science and Engineering	Programme	B. Tech. in CSE
Semester/Batch	03/2017		
Course Code	CSC203A	Course Title	Logic Design
Course Leader	Prof. A. Prabhakar, Mr. Deepak V. and Mr. Narasimha Murthy K. R.		

Assignment-1			
Reg.No.		**Name of Student**	

Sections		**Marking Scheme**	**Marks**		
			Max Marks	**First Examiner Marks**	**Moderator**
Part A					
	A.1.1	**Introduction**	**01**		
	A.1.2	**Arithmetic Subtraction using BCD and Excess-3 Codes**	**03**		
	A.1.3	**Conclusion**	**01**		
		Part-A Max Marks	**05**		
Part B.1					
	B.1.1	**Truth Table**	**03**		
	B.1.2	**Expression in SoP Form**	**01**		
	B.1.3	**Minimization using K-Map**	**06**		
		B.1 Max Marks	**10**		
Part B.2					
	B.2.1	**Truth Table**	**02**		
	B.2.2	**Minimization using K-Map**	**05**		
	B.2.2	**Importance of Don't Care Condition**	**03**		
		B.2 Max Marks	**10**		
		Total Assignment Marks	**25**		

Course Marks Tabulation				
Component-1 (B) Assignment	**First Examiner**	**Remarks**	**Moderator**	**Remarks**
A				
B.1				
B.2				
Marks (out of 25)				

Signature of First Examiner **Signature of Moderator**

Please note:

1. Documental evidence for all the components/parts of the assessment such as the reports, photographs, laboratory exam / tool tests are required to be attached to the assignment report in a proper order.
2. The First Examiner is required to mark the comments in RED ink and the Second Examiner's comments should be in GREEN ink.
3. The marks for all the questions of the assignment have to be written only in the **Component – CET B: Assignment** table.
4. If the variation between the marks awarded by the first examiner and the second examiner lies within +/- 3 marks, then the marks allotted by the first examiner is considered to be final. If the variation is more than +/- 3 marks then both the examiners should resolve the issue in consultation with the Chairman BoE.

Assignment 1

Term - 1

Instructions to students:

1. The assignment consists of **3** questions: Part A-**1** Question, Part B-**2** Questions.
2. Maximum marks is **25**.
3. The assignment has to be neatly word processed as per the prescribed format.
4. The maximum number of pages should be restricted to **10**.
5. Restrict your report for Part-A to 2 pages only.
6. Restrict your report for Part-B to a maximum of 8 pages.
7. The printed assignment must be submitted to the course leader.
8. **Submission Date: 24 September 2018**
9. **Submission after the due date is not permitted.**
10. **IMPORTANT**: It is essential that all the sources used in preparation of the assignment must be suitably referenced in the text.
11. Marks will be awarded only to the sections and subsections clearly indicated as per the problem statement/exercise/question

This course is intended to prepare students to design basic logic circuits and components used in a computer. Students are taught the principles and techniques of sequential and combinational logic circuits. Algorithms, digital logic elements and their optimization for design and implementation of digital logic circuits and their applications are covered. Students are trained to build, simulate and test digital circuits.

Part A **(05 Marks)**

Most digital systems are implemented using circuit elements that have two distinct (binary) states: ON or OFF. This means that a binary number of n digits may be represented by n binary circuit elements, each having an output signal equivalent to 0 or 1. This concept is also utilized when information is encoded, applying binary codes. Some of the well-known binary codes are Binary Coded Decimal (BCD) code, Gray code, Excess-3 code and the 8421 code.

Develop an essay on the topic **"A comparison of Arithmetic Subtraction using BCD and Excess-3 codes"**.

Your essay should emphasize on:

A.1.1 Introduction

A.1.2 Arithmetic subtraction using BCD and Excess-3 codes

A.1.3 Conclusion

Part B **(20 Marks)**

B.1 **(10 Marks)**

Design a combinational circuit that outputs 1 when the restrictions given in the below scenario are met. The output will be 0 otherwise.

Consider a strong room at a university where question papers are stored. Entry to this room is restricted to specific employees of the university. The rules for entering the room are:

- Only the exam superintendent can enter alone
- Head of the department can enter only if he is accompanied by the exam superintendent
- Course leader can enter only if he is with the exam superintendent or head of the department
- Tutor can enter the room only if he is accompanied by the exam superintendent

B.1.1 Write the truth table for the combinational circuit described above.

B.1.2 Express the behaviour of the circuit in the canonical Sum of Product (SoP) form.

B.1.3 Reduce the above SoP expression to the minimized form using K-Map.

B.2 **(10 Marks)**

Design a combinational circuit that outputs 1 when the restrictions given in the below scenario are met. When the restrictions are not met, the output can be 0 or don't care.

Consider that a University has four courses A, B, C and D in a semester. The courses are of 2, 3, 4 and 5 credits respectively. The criteria for passing the semester is that a student has to obtain a minimum number of credits. There are no restrictions on the maximum number of courses a student can take.

Note: The number of credits required to pass the semester will be specified by the course leader.

B.2.1 Write the truth table for the combinational circuit described above.

B.2.2 Derive the minimized Product of Sum (PoS) expression using K-Map.

B.2.3 Analyse the importance of don't care conditions in the process of minimization