

Design of a Multi Port DC-DC Converter for energy storage systems

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Design of a Multiport DC-DC Converter for energy storage systems

by

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A thesis submitted in partial fulfillment for the
degree of Masters of Technology

in the
Department of Electrical Engineering

September 2018

Declaration of Authorship

I, SATYAKI MUKHERJEE, declare that this thesis titled, ‘Design of a Multiport DC-DC Converter for energy storage systems’ and the work presented in it are my own. I confirm that:

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- Where I have consulted the published work of others, this is always clearly attributed.
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Prof. Debaprasad Kastha:

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Abstract

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Multiport DC-DC converters have gained special interest lately due to it's attractive features of integrating renewable energy resources. Especially with bi-directional power flow abilities and suitable control strategies, a multiport converter achieves soft-switching as well as reduced device stresses over wide voltage range of operation. Several existing multiport topologies are discussed for there relative merits and demerits. A multiport isolated bi-directional dc-dc converter is presented, for hybrid battery and supercapacitor energy storage application. The converter topology and the operating principles are introduced. Detailed analysis of soft-switching of all switches is given. On the basis of theoretical analysis, the principle and method for parameter designing are provided. A 50 KHz experimental prototype was designed and built. Experimental results are in agreement with the theoretical modeling. Prototype converter was operated over a wide output power range in a bidirectional manner. Efficiency of the power stage was greater than 90% for a wide range of load variation. . . .

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Chapter 1

Introduction

With rapid proliferation of distributed renewable energy systems, [1–5] dc microgrids are gradually becoming the preferred interconnection standard for distributed generation application. [6, 7] As an essential part of the microgrid, an energy storage system is drawing wide attention. Battery is the most mature device for energy storage. It has advantages of high energy density, long lifespan, low initial cost, and disadvantages of low power density, slow dynamic response, which makes it unsuitable to satisfy the requirements of sudden change of load power. Meanwhile, a supercapacitor has short charging/discharging time and a longer cycle life. It is also easy to maintain. Therefore, a hybrid system combining the battery with the supercapacitor is often used to improve the performance of the energy storage system. Battery is used for long term energy storage, while the supercapacitor is used for transient energy storage and fast supplement. For dc/dc power conversion, the dual-active-bridge (DAB) converter has been proposed in [8]. It has attractive features such as low device stresses, bidirectional power flow, fixed-frequency operation, and utilization of the transformer leakage inductance as the energy transfer element. The main drawback of the DAB converter, however, is that it cannot handle a wide input voltage range (e.g., fuel cells and supercapacitors). In such a case the soft-switching region of operation will be significantly reduced. [8, 9] To enhance the ZVS range, an integrated magnetic structure three port converter is discussed in [10], which has the problem of increased conduction loss at no load to maintain constant current through the battery port of the converter. In [11] a novel resonant topology is discussed for achieving bidirectional power flow with wide ZVS range at a constant frequency of operation. This topology has several attractive features, such as phase shift control of the power flow from any port, bi-directional power flow between two ports even when one port is completely isolated. Finally, this work focuses on a multiport bidirectional converter presented in [12], which has several interesting features in terms of operation and control of the multiport system.

This thesis, after analyzing several multiport topologies, chooses a particular topology based on the specific application requirements. The phase shift controlled bi-directional converter is analyzed in terms of its operating principles and characteristics. A design methodology is introduced for soft switching operation. Relevant proof of concept hardware is developed along with essential gate driving circuitry and sensing arrangements. A Field Programmable Gate Array (FPGA) is utilized for 3 degrees of control, in open loop operation, in order to develop a suitable control strategy for the converter. Dedicated magnetics which involves a high frequency transformer along with several filter inductors, were handcrafted, and tested in the hardware prototype.

Keywords: Multiport DC-DC Conversion, Hybrid energy storage and bidirectional power flow, Zero Voltage Switching (ZVS), Dual Active Bridge (DAB), Control strategy.

1.1 Scope of Work

This work tries to adapt an existing converter topology for a particular application and design specification. In order to do that, the converter is theoretically analyzed to arrive at its design equations. Using which, for a particular specification, the converter is designed and simulated. Finally the aim is to verify the operation using a hardware prototype. Scope for this work can be summarized as to develop a high efficiency multiport DC-DC converter to interface a battery port a supercapacitor port and a DC Bus port. The converter should be able to achieve bidirectional power flow, along with soft switching over a wide range of operation, in order to maximize efficiency. The converter structure should be suitably chosen keeping in mind the transient responses of the energy storage devices. An ideal block diagram representation of the converter is shown in Fig. 1.1.

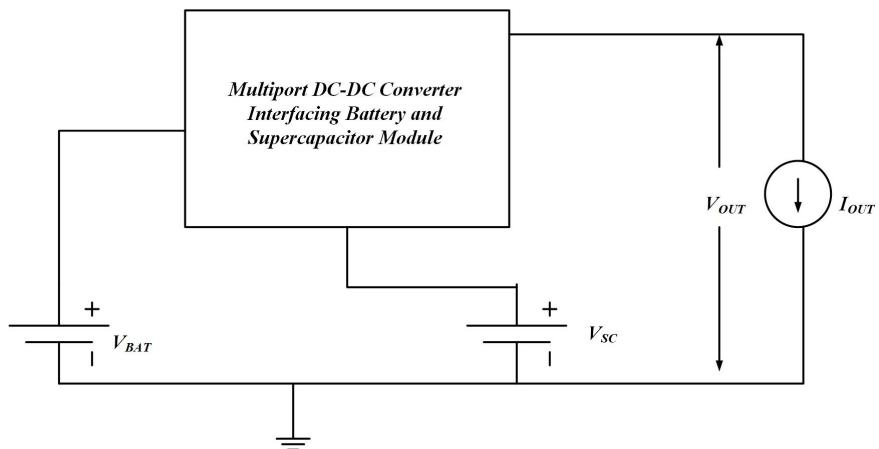


FIGURE 1.1: Block diagram representation of the multiport converter

We can infer the following system requirements from the scope defined above:

- The system needs current fed nature at the battery port in order to improve life expectancy of the device. Due to topological similarity, a similar current fed nature is adopted for the supercapacitor port as well.
- The system requires bi-directional power flow among all possible ports in the power stage. To realize this, MOSFETs have to be used to interface the associated ports in the converter.
- To maximize efficiency the devices are required to be soft switched. As majority carrier MOSFET devices are used (DC bus voltage is 200 volts in the design, hence MOSFETs are more feasible than IGBTs), Zero Voltage Switching (ZVS) is more important to achieve.

All the above mentioned criteria were kept in mind, during literature survey and the one presented in [12] is chosen, because of its inherent soft switching and bidirectional capabilities. Also, two of the ports were made current fed to interface the battery and the supercapacitor modules.

Chapter 2

Theoretical Analysis

In Fig. 2.1 the schematic of the converter topology is shown. It can be observed that, there is a Dual Active Bridge stage in between the source and load ports. Both the Battery and the Super Capacitor ports are interfaced with 2 inductors, to the transformer. This provides the advantage of having continuous current flowing through the battery, thus, increasing the lifetime of the battery. The converter is analyzed in detail for a

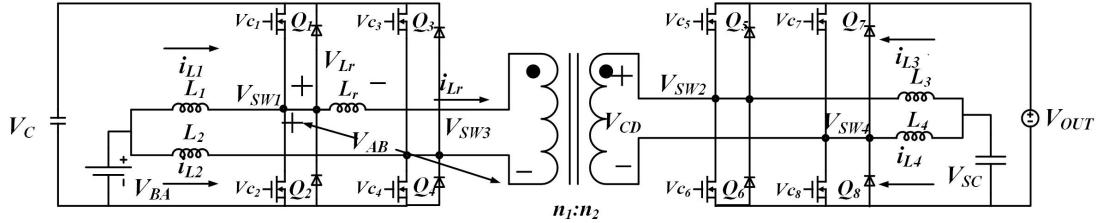


FIGURE 2.1: Schematic of the proposed bi-directional phase-shift controlled topology

particular mode of operation required for the desired hardware specification. The gate drive signals along with the predicted theoretical waveforms are shown in Fig. 2.2. The duty ratio of the switches in the top and bottom leg are defined in Fig. 2.2. Whereas the phase shift, which essentially controls the power flow from one side of the transformer to the other, is denoted by D_{phi} . Initially to operate the converter in a desired mode, $(D_2 + D_{phi}) < 0.5$ was maintained, so that the waveforms drawn are correct in that particular mode of operation. Due to boost operations of each switching leg, the Capacitor port voltage V_C and the load port voltage V_{OUT} can be written as:

$$V_C = \frac{V_{BAT}}{D_1} \quad (2.1)$$

$$V_{OUT} = \frac{V_{SC}}{D_2}$$

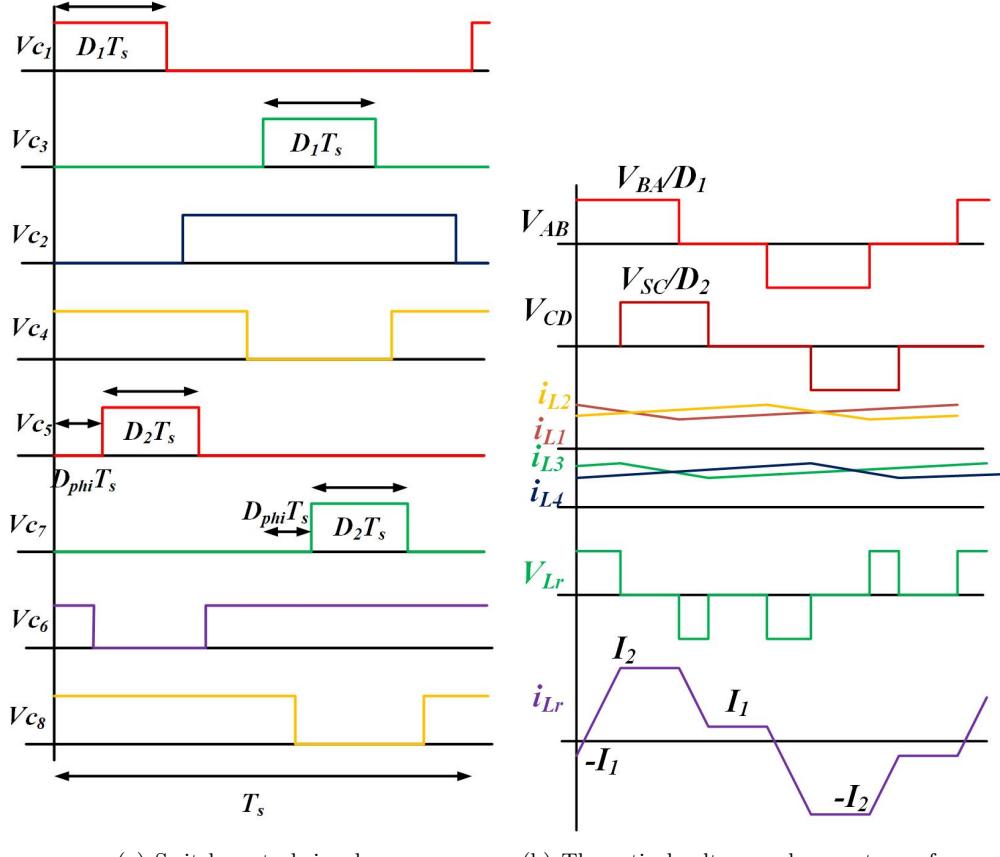


FIGURE 2.2: The converter is controlled by phase shift D_{phi} between the two full bridges

Now from the waveforms & the slope of the inductor current i_{lr} , it is clearly observed that

$$I_1 + I_2 = \frac{D_{phi}T_s V_c}{L_r} \quad (2.2)$$

$$I_2 - I_1 = \frac{(D_{phi} + D_2 - D_1)T_s V_{OUT}}{L_r} \quad (2.3)$$

Which, when solved simultaneously gives the current values of I_1 and I_2 as:

$$I_1 = \frac{T_s(V_c D_{phi} - (D_{phi} + D_2 - D_1)V_{OUT})}{2L_r} \quad (2.4)$$

$$I_2 = \frac{T_s(V_c D_{phi} + (D_{phi} + D_2 - D_1)V_{OUT})}{2L_r} \quad (2.5)$$

Now, this inductor current is rectified and drawn from the Battery. Since, the passive port will not draw any current, the battery port will deliver the average current through L_1 & L_2 during each $D_1 T_s$ period, **twice** (Due to 2 boost inductors) in one cycle. During $\frac{T_s}{2} - D_1 T_s$ period transformer primary is shorted through Q_2 & Q_4 and the current is just circulating through. There will be no average power delivered from battery port

during this time. So, the average battery current can be found out by:

$$\langle i_{BAT} \rangle = I_{BAT} = \frac{2 \int_0^{D_1 T_s} i_{Lr}(t) dt}{D_1 T_s} \quad (2.6)$$

Which Gives:

$$I_{BAT} = \frac{2(I_2(D_1 - 0.5D_{phi}) - 0.5 \times I_1 D_{phi})}{D_1} \quad (2.7)$$

Now, we arrive at the power flow equation, the average battery power output is the power processed through the transformer as the power delivered to the passive capacitor port V_C is zero. Which is given by:

$$\begin{aligned} P_{BAT} &= I_{BAT} V_{BAT} \\ &= \frac{V_{BAT} T_s (V_C D_{phi} (D_1 - D_{phi}) + V_{OUT} D_1 (D_2 - D_1 + D_{phi}))}{D_1 L_r} \end{aligned} \quad (2.8)$$

In order to achieve ZVS of the switches, the general requirement is that: $I_1 \& I_2 \geq 0$.

Also, to minimize the r.m.s. current flowing through the leakage inductor L_r , we need to adopt the voltage matching strategy, such that the inductor current waveform becomes flat topped, as described in [13]. Hence, another design constraint comes in terms of V_C & V_{OUT} :

$$V_C = \frac{n_1 V_{OUT}}{n_2} \quad (2.9)$$

2.1 Design Specifications

The design specification of the multiport converter is as follows:

$$\begin{aligned} 40 \text{ Volts} &\leq V_{BAT} \leq 60 \text{ Volts} \\ 22 \text{ Volts} &\leq V_{SC} \leq 56 \text{ Volts} \\ V_{OUT} &= 200 \text{ Volts} \\ P_{OUT} &\leq 1000 \text{ Watts (bidirectional)} \\ f_s &\geq 25 \text{ kHz (in RF band)} \end{aligned} \quad (2.10)$$

The main aim of the topology is to minimize stress on the battery. To do that, we always maintain a constant current flowing through the battery by closed loop phase shift control. Any variation in the load is maintained through the Super Capacitor. On the other hand the supercapacitor voltage is maintained through another closed loop control. If the voltage falls below 22 Volts, the battery is used to charge up the capacitor voltage. During this period the battery is used to supply the load and the capacitor charging power.

If the battery voltage falls below a certain threshold, the supercapacitor is used to charge up the battery. Since the load port can also be used to transfer power towards the source, due to its bi-directional capabilities, this topology is well suited for regenerative braking operation.

2.1.1 Design of Components

In order to simplify the design of the high frequency transformer the passive capacitor port voltage is designed to be equal to 200 Volts. This provides voltage matching with 1 : 1 transformer turns ratio for minimizing the r.m.s current through the leakage inductor. With this choice of V_C , we can directly arrive at the limiting values of D_1 & D_2 :

$$\begin{aligned} D_{1max} &= \frac{V_{BATmax}}{V_C} & D_{1min} &= \frac{V_{BATmin}}{V_C} \\ &= .3 & &= .2 \end{aligned} \quad (2.11)$$

$$\begin{aligned} D_{2max} &= \frac{V_{SCmax}}{V_{OUT}} & D_{2min} &= \frac{V_{SCmin}}{V_{OUT}} \\ &= .28 & &= .11 \end{aligned} \quad (2.12)$$

Switching frequency of the converter is selected to be equal to 50 Khz. The components are designed in order to satisfy the most stringent operating conditions. Also, to restrict the operation of the converter in the mode predicted in Fig. 2.2, we need to ensure:

$$\begin{aligned} D_{2max} + D_{phimax} &< .5 \\ D_{phimax} &< D_{1min} \\ D_{phimax} + D_{2min} &> D_{1max} \end{aligned} \quad (2.13)$$

Solving Eq. 2.13 we arrive at $D_{phimax} = .18$.

- **Operating Condition 1:** During this mode, the battery voltage is minimum as well as the supercapacitor voltage. Hence, the entire load power has to be transferred from the battery port. During this mode of operation, $D_1 = D_{1min} = .2$, $D_2 = D_{2min} = .11$ and $D_{phi} = D_{phimax} = .18$. Then the power input equation

can be formulated as:

$$\begin{aligned}
 P_{IN} &= 1000 \text{watts} \\
 &= \frac{V_{BAT}T_s(V_CD_{phi}(D_1 - D_{phi}) + V_{OUT}D_1(D_2 - D_1 + D_{phi}))}{D_1L_r} \\
 &= \frac{200 \times 40(0.18(0.2 - 0.18) + 0.2(0.11 - 0.2 + 0.18))}{5 \times 10^4 L_r 0.2}
 \end{aligned} \tag{2.14}$$

Solving Eq. 2.14 we get the value of the leakage inductance $L_r = 17.28 \times 10^{-6} H$.

- **Operating Condition 2:** During this mode, we verify that using the designed inductance value in Operating Condition 1 whether rated power can be delivered to the load port. At this operating point we have: $D_1 = .25$ & $D_2 = .195$, then using the maximum value of phase shift, $D_{phimax} = .18$ we get the power transmitted: $P_{IN} = 1650 \text{watts}$. Which is more than the maximum power required through load and the charging power for the supercapacitor. This confirms, with the designed value of leakage inductance, we can sustain the required power level at the nominal operating point.
- **Operating Condition 3:** Now, we test our design, for bidirectional power transfer. If the direction of power flow reverses, then the leakage inductor current waveforms would have to be seen from the load port and similar range of duty cycle will persist.

2.1.2 Zero Voltage Switching (ZVS) Conditions

As we can model the boost stages by two effective current sources, each carrying half the battery current, the equivalent circuit of a particular switching cell can be drawn as in Fig. 2.3. Now for ZVS analysis of SW_1 , we can formulate the KCL equation as Eq. 2.15. Prior to turning on the switch, the Inductor current i_{Lr} is maintained at a negative value of $-I_1$, so if power is delivered from battery, i.e. if $\frac{I_{BAT}}{2} \geq 0$, then $I_{SW1} < 0$. This ensures that there will be a negative current to discharge the output capacitor, leading to ZVS of the switch SW_1 .

$$\frac{I_{BAT}}{2} + I_{SW1} = i_{Lr} \tag{2.15}$$

$$\frac{I_{BAT}}{2} = I_{SW2} - i_{Lr} \tag{2.16}$$

For the bottom switch of the same leg, again applying KCL leads to Eq. 2.16. Prior to turning on of SW_2 , i_{Lr} is I_2 (refer Fig. 2.2). In order to make the switch current negative, we have to ensure that $I_2 \geq \frac{I_{BAT}}{2}$. Then only the bottom switch can undergo ZVS. This condition always holds, since $I_{BAT} \leq I_2$

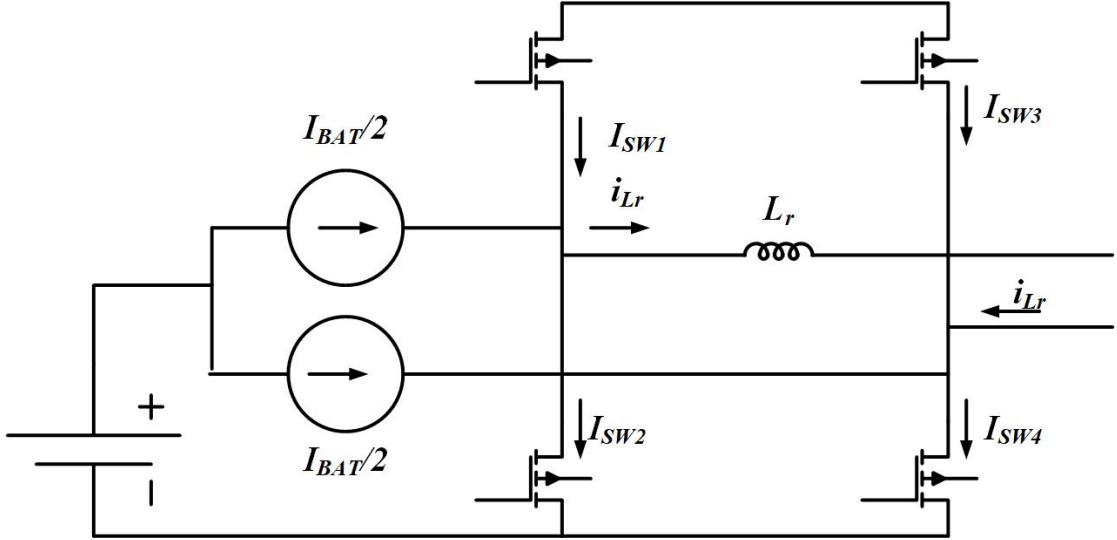


FIGURE 2.3: Effective equivalent circuit of a full bridge when Battery port is delivering Power

$$\frac{I_{BAT}}{2} + I_{SW3} + i_{Lr} = 0 \quad (2.17)$$

$$\frac{I_{BAT}}{2} + i_{Lr} = I_{SW4} \quad (2.18)$$

Similar kind of KCL equations are constructed for SW_3 & SW_4 in Eq . 2.17 & 2.18. One interesting point to note here is that prior to switching the devices of this leg, leakage inductor current reverses direction. So, in Eq. 2.17 $i_{Lr} = I_1 > 0$ & in Eq. 2.18 $i_{Lr} = -I_2 < \frac{I_{BAT}}{2}$. These conditions again ensure ZVS of all four switches, when the battery port is delivering power to the load.

The ZVS analysis for the power delivery port devices are done based on the equivalent circuit shown in Fig. 2.4. Here again ignoring the boost stage inductor current ripple, they are modeled as current sources, and the load port is also modeled as a current sink (The DC link capacitor will not draw any average current, hence it is ignored). Again the objective of ZVS is to make the switch currents negative at the point of turning on, so that the output capacitance can be discharged. In this case, for the top switches, achieving ZVS is pretty trivial, since, during transition of the top switches, $I_{SW1} = -I_{OUT}$, & $I_{SW3} = -I_{OUT}$. For the bottom switches however we need to apply KCL again.

$$\frac{I_{SC}}{2} + i_{Lr} = I_{SW2} \quad (2.19)$$

At this point, the leakage inductor current is simply $-I_1$, which imposes a limitation on the supecapacitor current for achieving ZVS. In Eq. 2.19 if $\frac{I_{SC}}{2} > I_1$ ZVS of this switch won't occur. Similar restrictions apply for SW_4 .

$$\frac{I_{SC}}{2} - i_{Lr} = I_{SW4} \quad (2.20)$$

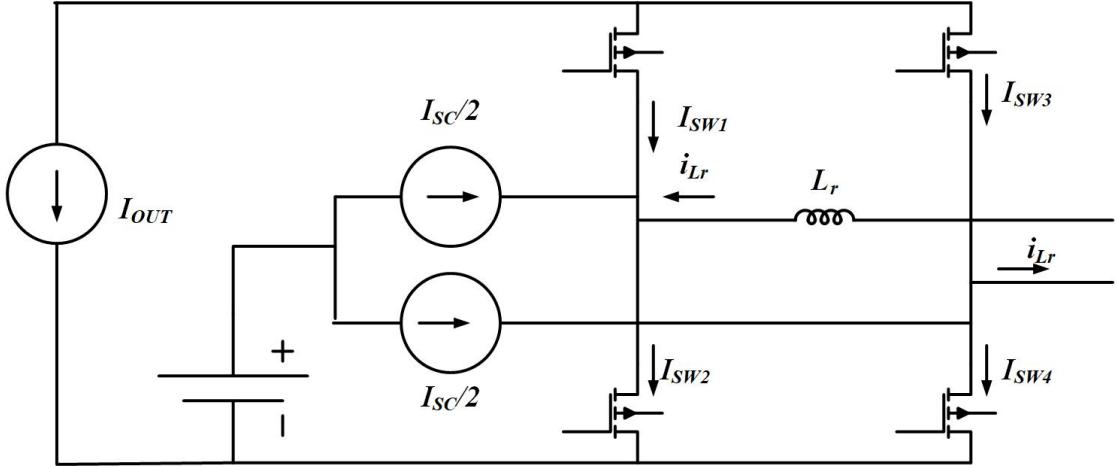
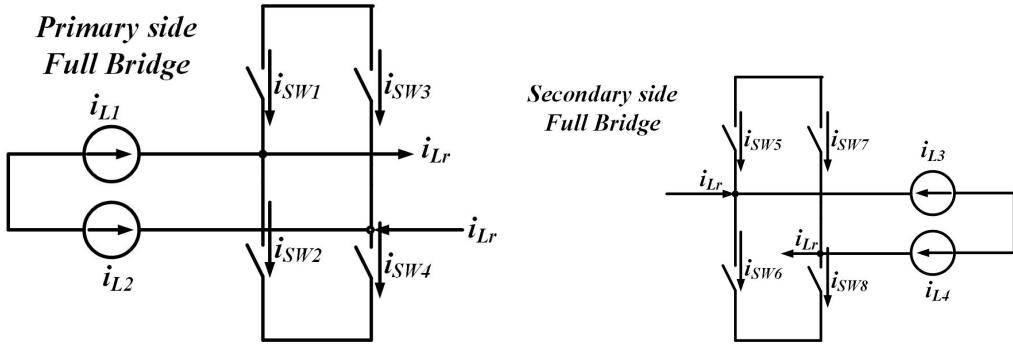


FIGURE 2.4: Effective equivalent circuit of a full bridge when Supercapacitor is delivering power and load port is receiving power



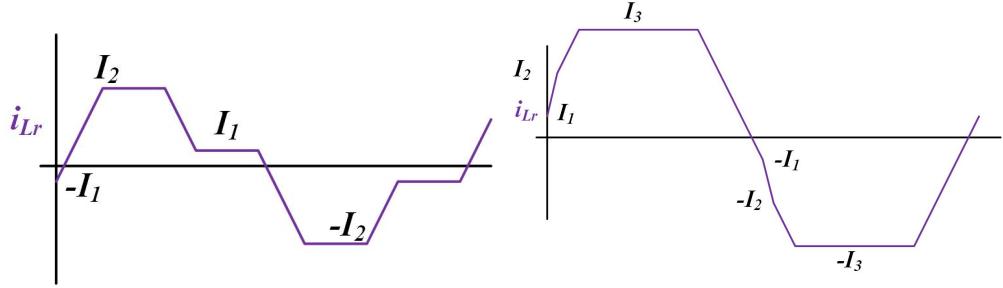
(a) Current through the switches of primary side full bridge (b) Switch currents of secondary side full bridge

FIGURE 2.5: ZVS analysis of 8 switches in terms of KCL equations

As predicted in Eq. 2.20, the inductor current during transition of this switch (I_2) should be larger than $\frac{I_{SC}}{2}$, to achieve ZVS of this switch.

2.1.2.1 Loss of ZVS at designed operating points

Achieving soft switching is a very important criterion to enhance efficiency of the converter. ZVS criteria of all 8 switches can be found, by applying KCL at the switch nodes in Fig. 2.5. For the designed converter operation and gate pulses depicted in Fig. 2.2 the leakage inductor current waveform is specifically shown in Fig. 2.6(a). From Fig. 2.5(a) using KCL, at the instants of switching we can write: (where inductor currents are sampled from Fig. 2.6(a))



(a) Current through leakage inductor at the de-signed value of $D_1 \& D_2$ (b) Current through leakage inductor at the modified design to ensure ZVS

FIGURE 2.6: Leakage inductor current waveforms at various operating conditions

$$\begin{aligned}
 I_{SW1} &= i_{Lr} - I_{L1max} \implies I_{SW1} = -I_1 - I_{L1max} \\
 I_{SW2} &= I_{L1min} - i_{Lr} \implies I_{SW2} = I_{L1min} - I_2 \\
 I_{SW3} &= -I_{L2max} - i_{Lr} \implies I_{SW3} = -I_{L2max} - I_1 \\
 I_{SW4} &= I_{L2min} + i_{Lr} \implies I_{SW4} = I_{L2min} - I_2
 \end{aligned} \tag{2.21}$$

Similarly for the ZVS condition of the secondary side full bridge, KCL equations at the switching instances, with sampled i_{lr} values reveal:

$$\begin{aligned}
 I_{SW5} &= -i_{Lr} - I_{L3max} \implies I_{SW5} = -I_2 - I_{L3max} \\
 I_{SW6} &= I_{L3min} + i_{Lr} \implies I_{SW6} = I_{L3min} + I_1 \\
 I_{SW7} &= -I_{L4max} + i_{Lr} \implies I_{SW7} = -I_{L4max} - I_2 \\
 I_{SW8} &= I_{L4min} - i_{Lr} \implies I_{SW8} = I_{L4min} + I_1
 \end{aligned} \tag{2.22}$$

Eq. 2.22 clearly shows that if the leakage inductor current level I_1 , shown in Fig. 2.6(a), is +ve, then I_{SW6} & I_{SW8} values are positive at the switching instances, which means they won't undergo ZVS. Eq. 2.4 suggests that $I_1 \leq 0$ is only satisfied when, $V_C D_{phi} \leq V_{OUT} (D_2 - D_1 + D_{phi})$, that is if the voltage levels are matched, i.e. $V_C = V_{OUT}$, then, $D_2 \geq D_1$ has to be satisfied to have ZVS transition of Q_6 & Q_8 . This imposes some serious limitations over the operation of the converter. That is why the duty ratios were changed to vary at different levels, to help achieve ZVS of all switches.

2.1.3 Modified design for achieving ZVS over wide operating range

In the modified design the duty ratios of both the half bridges were kept closer to 0.5. The relevant theoretical waveforms and gate signals are predicted in Fig. 2.7. The major

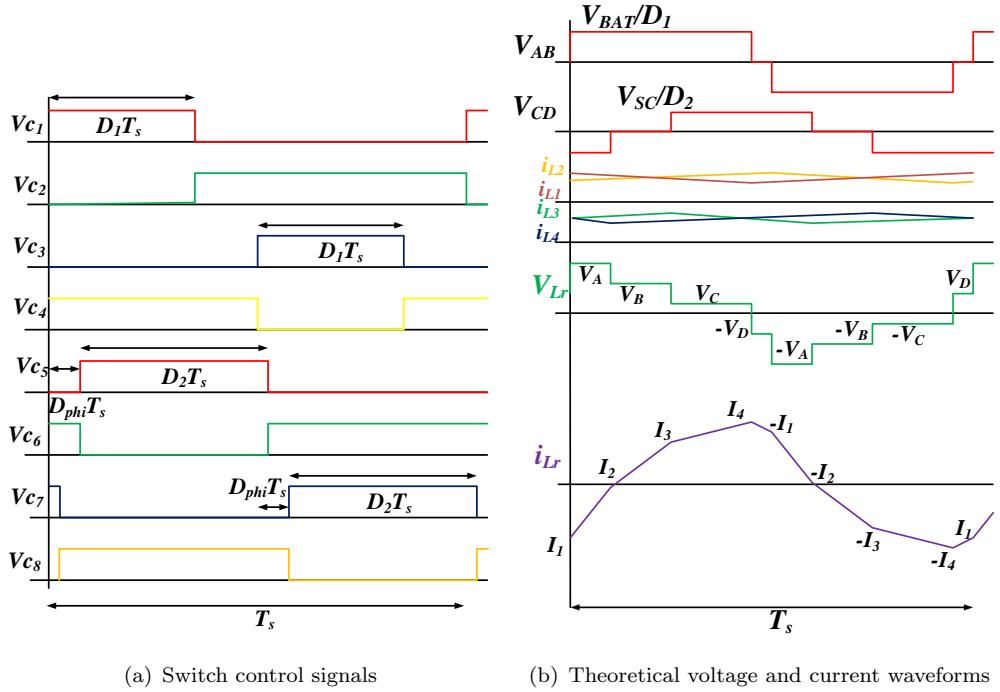


FIGURE 2.7: Modified switching strategy with increased values of D_1 & D_2 to achieve ZVS

change can be observed in the leakage inductor current, a magnified view of which is shown in Fig. 2.6(b). This current waveform now has 3 levels I_1, I_2, I_3 , where:

$$\begin{aligned}
 I_2 - I_1 &= \frac{(V_C + V_{OUT})(D_2 + D_{phi} - 0.5)T_s}{L_r} \\
 I_3 - I_2 &= \frac{V_C(0.5 - D_2)T_s}{L_r} \\
 I_4 - I_3 &= \frac{(V_C - V_{OUT})(D_1 - D_{phi})T_s}{L_r} \\
 I_4 + I_1 &= \frac{V_{OUT}(0.5 - D_1)T_s}{L_r}
 \end{aligned} \tag{2.23}$$

Solving the simultaneous equations of Eq. 2.23, we can arrive at the current values:

$$\begin{aligned} I_1 &= \frac{T_s[V_{OUT}(1 - D_2 - 2D_{phi}) - V_CD_1]}{2L_r}; \quad I_2 = \frac{[V_C[2D_2 + 2D_{phi} - D_1 - 1] + V_{OUT}D_2]T_s}{2L_r} \\ I_3 &= \frac{T_s[V_C[2D_{phi} - D_1] + V_{OUT}D_2]}{2L_r}; \quad I_4 = \frac{T_s[V_CD_1 + V_{OUT}[2D_{phi} - 2D_1 + D_2]]}{2L_r} \end{aligned} \quad (2.24)$$

Similar to Eq. 2.6, to find out the average battery current flowing out of the current fed port:

$$\langle i_{BAT} \rangle = I_{BAT} = \frac{2 \int_0^{D_1 T_s} i_{Lr}(t) dt}{D_1 T_s} \quad (2.25)$$

Eq. 2.25 gives the value of the average battery current I_{BAT} , which can also be used to find the average power output:

$$I_{BAT} = \frac{T_s V_{OUT} (D_{phi}(1 - 2D_2 + 2D_1 - 2D_{phi}) + D_2(1 + D_1 - D_2) - D_1^2 - 0.25)}{L_r D_1}$$

$$P_{BAT} = I_{BAT} \times V_{BAT} = \frac{V_{OUT}^2}{R_{load}}$$
(2.26)

Eq. 2.26 assumes that when the battery port is supplying power to the load port, supercapacitor port is disconnected, that is why the entire output power is supplied by the battery. Now, the motivation to move to this relatively complex mode of operation was, to have soft transition of the switches over wider range of operating points. Again, to find the ZVS conditions, in this design, KCL was applied to Fig. 2.5(a) and Fig. 2.5(b). The leakage inductor current waveform of Fig. 2.6(b) was sampled at the switching instants to find the transition currents through the switches.

$$\begin{aligned} I_{SW1} &= i_{Lr} - I_{L1max} \implies I_{SW1} = I_1 - I_{L1max} \\ I_{SW2} &= I_{L1min} - i_{Lr} \implies I_{SW2} = I_{L1min} - I_3 \\ I_{SW3} &= -I_{L2max} - i_{Lr} \implies I_{SW3} = -I_{L2max} + I_1 \\ I_{SW4} &= I_{L2min} + i_{Lr} \implies I_{SW4} = I_{L2min} - I_3 \end{aligned} \quad (2.27)$$

Eq. 2.27 gives us the ZVS transition currents for all 4 primary side switches. It should be observed that as I_1 magnitude is kept pretty low (if $V_C = V_{OUT}$, $I_1 = \frac{V_C T_s (1 - D_1 - D_2)}{2L_r}$ and as $D_1, D_2 \approx 0.5$, $1 - (D_1 + D_2) \approx 0$), hence, although I_1 opposes ZVS of Q_1 & Q_3 , the input filter inductor current is sufficient to overcome this.

$$\begin{aligned} I_{SW5} &= -i_{lr} - I_{L3max} \implies I_{SW5} = -I_3 - I_{L3max} \\ I_{SW6} &= I_{L3min} + i_{lr} \implies I_{SW6} = I_{L3min} - I_2 \\ I_{SW7} &= -I_{L4max} + i_{lr} \implies I_{SW7} = -I_{L4max} - I_3 \\ I_{SW8} &= I_{L4min} - i_{lr} \implies I_{SW8} = I_{L4min} - I_2 \end{aligned} \quad (2.28)$$

On the other hand at the secondary side, ZVS is aided by current I_2 . In the earlier operating condition, Eq. 2.22 depicts that if I_1 is positive there is no negative current to ensure ZVS of Q_6 & Q_8 , but in Eq. 2.28 for Q_6 & Q_8 the only opposing current in ZVS is the filter inductor currents. As, we will be anyway keeping the supercapacitor port open during power transfer from battery port, $I_{L2min} = I_{L4min} = \text{some -ve value}$. Hence, ZVS of all 8 switches are ensured during this modified mode of operation. It should be noted that, although all the derivations are done based on the assumption that the battery port is delivering the power, or V_{SW1} is leading V_{SW2} , the same analysis holds

true if supercapacitor port is delivering power to the passive port.

2.1.4 Filter Inductor Design

For the boost stage filter inductor design, the simple current ripple criterion is used. Allowing a maximum ripple of 2 A peak to peak on both battery and supercapacitor currents. This converter does not go into DCM, as all the switches can carry bidirectional current.

$$L = \frac{Vin(1 - D)_{max}T_s}{\Delta I} \quad (2.29)$$

Following Eq. 2.29 the filter inductors are designed as **350 μ H & 280 μ H**

Chapter 3

Simulation Results

The proposed topology, with the designed components is simulated in an LTSpice environment to evaluate the efficiency, verify ZVS of the switches, and check the effectiveness of the bi-directional power flow capability. Fig. 3.1 shows the simulation schematic. Variation in phase shift between the two full bridges, using the control variable D_{phi} is also done to check the control of power flow.

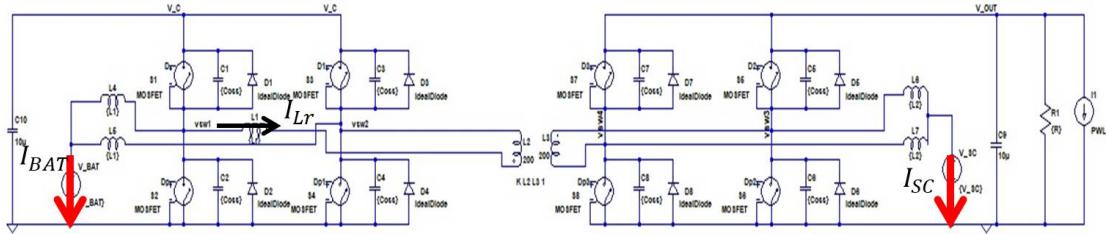


FIGURE 3.1: Simulation arrangement in LTSpice environment

Fig. 3.2 shows the simulated leakage inductor current waveform, which matches with the theoretically predicted waveform in Fig. 2.2. We can see that the Inductor current rises from a negative value, at the start of each switching instant.

Fig. 3.3 shows the operating point based on which the leakage inductor was designed. Both the Battery and the Super Capacitor voltages are at their respective minimum values, and the battery is supplying the entire load power. In this mode, the limiting value of D_{phi} is also used, to verify the theory. We can clearly see, that the converter is able to supply 1 kW of load power. Hence, the inductor design is verified. Now, to verify the Zero Voltage Switching of all the devices, the gate pulses given to the switches, along with the current flowing through them is plotted in Fig. 3.4. As the top devices are driven with a bootstrap kind of supply, the gate voltage is referred to the switch node voltage, and is around 200 Volts. The interesting phenomenon to note here is that,

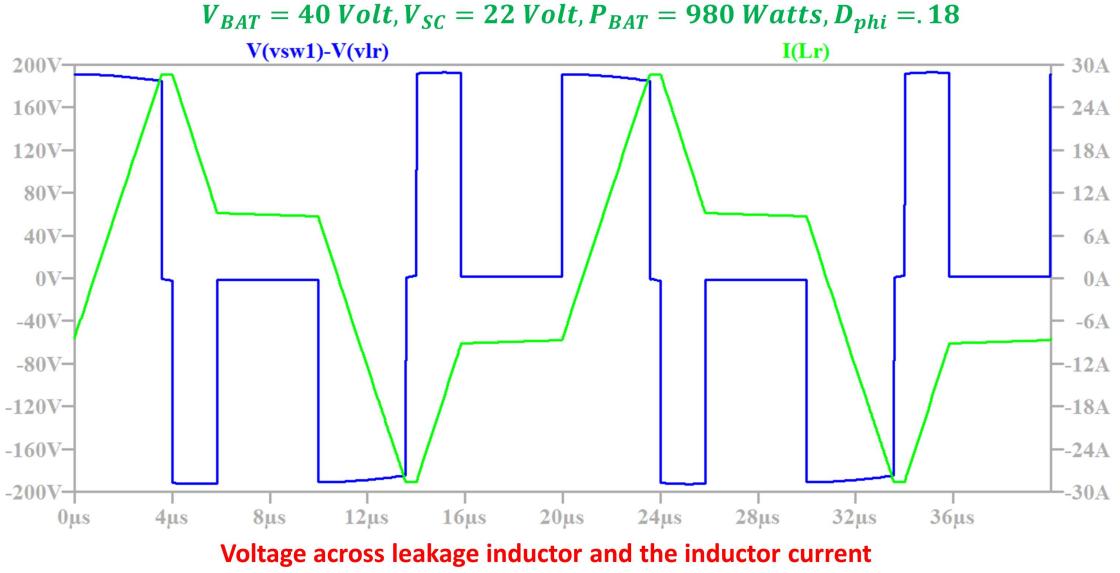


FIGURE 3.2: Leakage inductor current waveform along with the voltage across L_r with 1 KW power flow

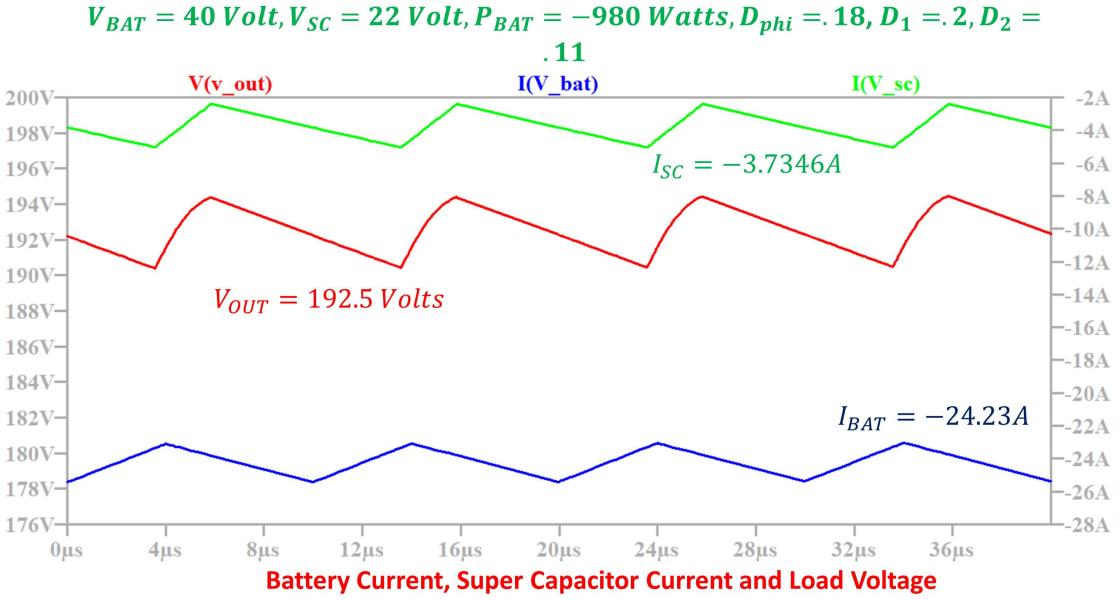


FIGURE 3.3: Verification of the operating point in Eq. 2.14, to verify the design of the leakage inductor

whenever a switch is driven with a gate pulse, the current flowing through the switch is negative. This ensures ZVS, as, if appropriate dead times are given, prior to turning on the devices, this negative current will help to discharge the output capacitances of the switches.

The bi-directional power flow capabilities of the converter is verified by making the phase shift D_{phi} negative. Now, the inductor current starts from a negative value. Still the primary side switches achieve ZVS, as the average current flowing in to the battery

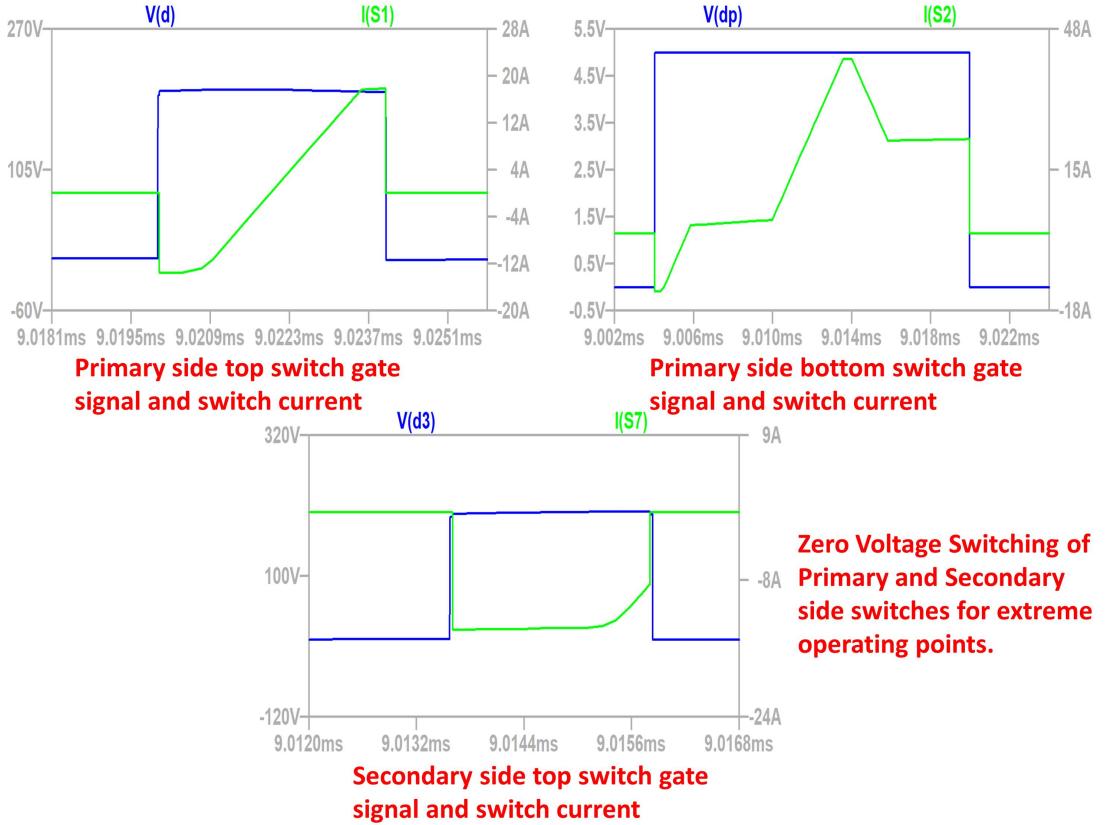


FIGURE 3.4: Zero Voltage Switching of both the top and bottom devices at a particular operating point

port has become positive. The effective inductor current waveforms along with the switching voltage is shown in Fig. 3.5. At this operating point effective phase shift D_{phi} is equal to .15, and the power coming into the battery port is equal to 870 Watts. Fig. 3.6 corresponds to the maximum power transfer from load port to the battery port. With a phase shift of $-.15$ we achieve a power flow of ≈ 1 kW from the load port to the battery port of the converter. Fig. 3.6 also shows that the excess power delivered from the load port is absorbed in the supercapacitor. Hence, this mode can be modeled as the charging mode of both the battery and supercapacitor port, from the power available through regenerative braking, at the load port. It should be noted here, that the bi-directional power flow is modeled in the simulation using a load current source at the load port.

Fig. 3.7 depicts operation of the converter at a nominal point. The converter is loaded with 1 kW power and the entire load is shared between the battery and supercapacitor. This is achieved again through phase shift control of the converter. The operating point shown, shares the load as $P_{BAT} = 450Watts$ and $P_{SC} = 550Watts$. These simulation results fully characterize all the major operational aspects of the converter including bidirectional power flow and Zero Voltage Switching of the devices.

$$V_{BAT} = 40 \text{ Volt}, V_{SC} = 22 \text{ Volt}, P_{IN} = 870 \text{ Watts}, D_{phi} = -.12$$

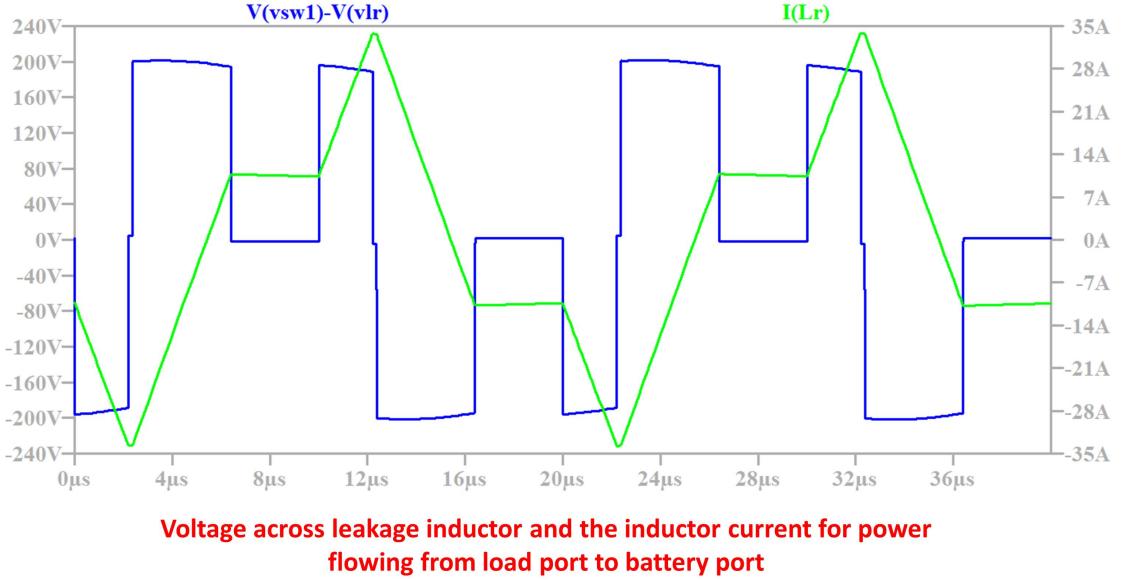


FIGURE 3.5: Leakage inductor current when Power is flowing from load port, to the battery port

$$V_{BAT} = 40 \text{ Volt}, V_{SC} = 22 \text{ Volt}, P_{IN_BAT} = -875 \text{ Watts}, D_{phi} = -.15, D_1 = .2, D_2 = .11$$

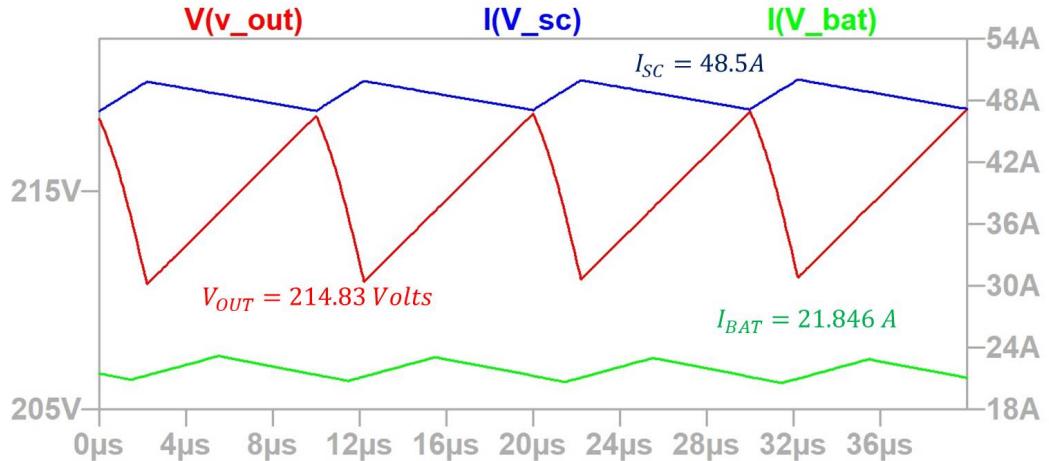


FIGURE 3.6: Effective Battery, Supercapacitor, load port current and voltages with bi-directional power flow

The control aspect of the converter is shown in Fig. 3.8. The converter is simulated at a nominal voltage of both battery and supercapacitor port for multiple values of the phase shift. It can be clearly seen that the power output from the battery port is directly proportional to the phase shift applied between the two ports of the converter. This also matches our theoretical analysis, which is derived in Eq. 2.8. This can very well be used

$$V_{BAT} = 50 \text{ Volt}, V_{SC} = 40 \text{ Volt}, P_{BAT} = 450 \text{ Watts}, D_{phi} = .05, D_1 = .25, D_2 = .2$$

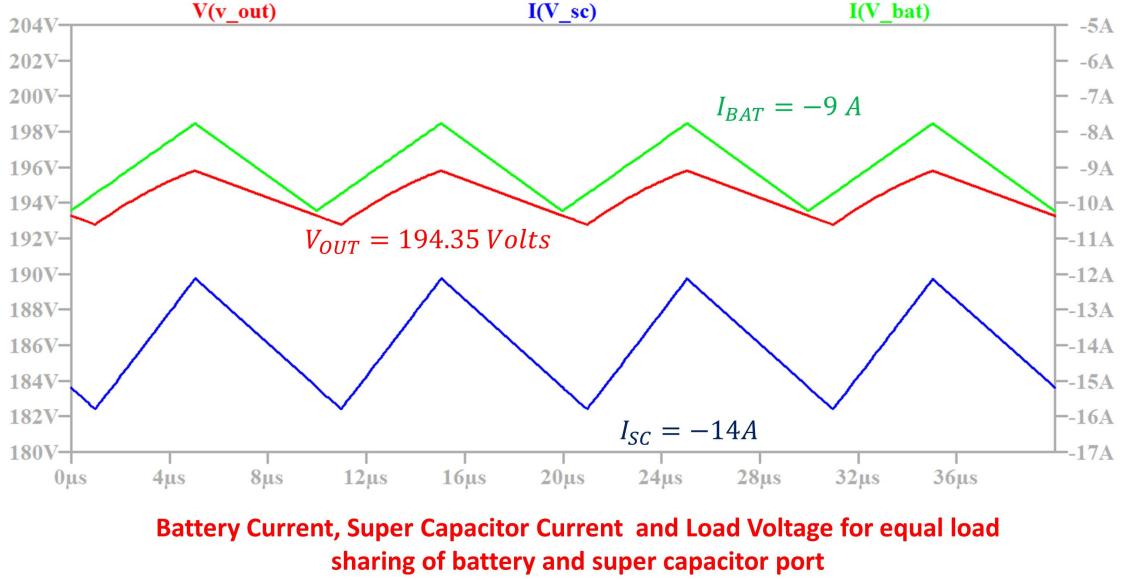


FIGURE 3.7: Load sharing between the battery port and supercapacitor port using phase shift control

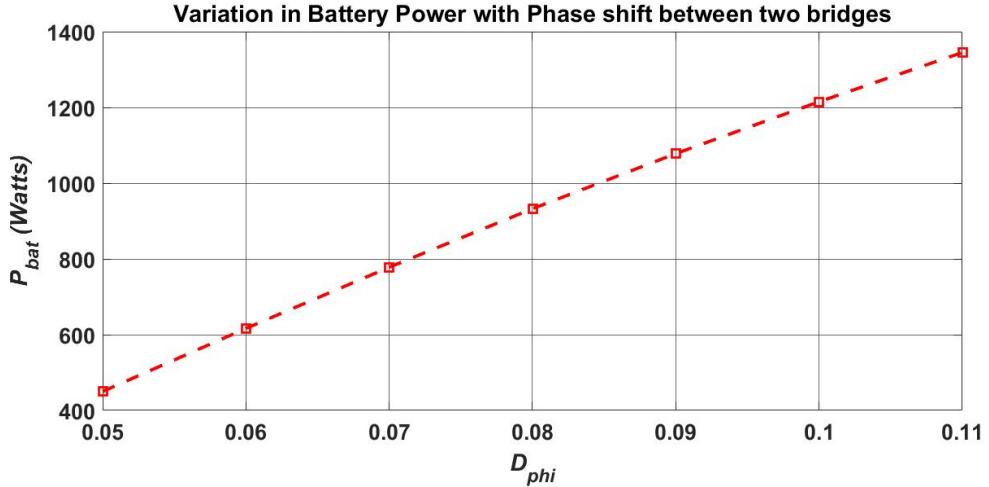


FIGURE 3.8: Battery Power output control using the control variable D_{phi} ($V_{BAT} = 50 \text{ Volts}, V_{SC} = 40 \text{ Volts}$)

to arrive at a closed loop control strategy to regulate the power flow from one port to the other.

Fig. 3.9 plots the simulated efficiency of the converter. As we keep on increasing the phase shift, more power is transferred through the transformer, and more losses occur in the converter power stage. As the boost stage is a direct converter topology [14], the efficiency of the power stage is more, if the load power is processed through the boost stage. However, we do observe that even when the battery is used to charge the supercapacitor the efficiency of the power stage does not fall below 90%.

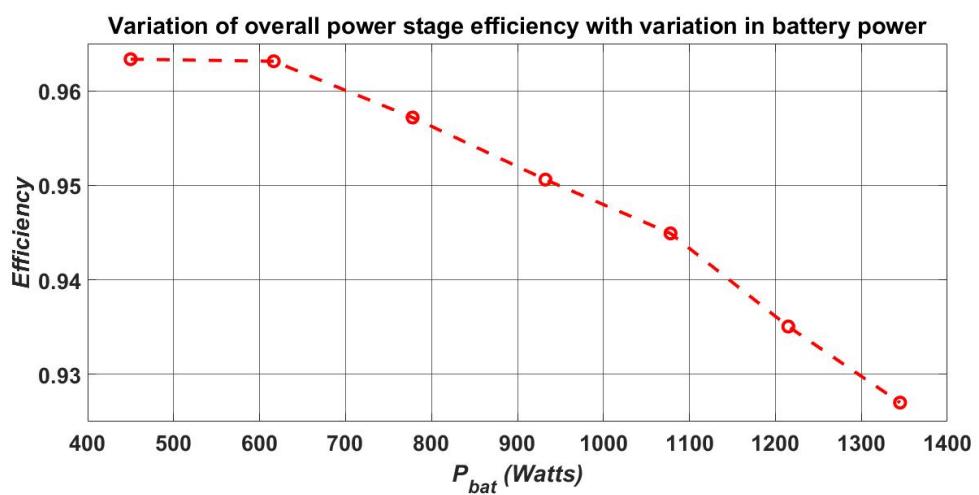


FIGURE 3.9: Plot of Efficiency vs. Power output from battery in the nominal operating point of $V_{BAT} = 50\text{Volts}$, $V_{SC} = 40\text{Volts}$

Chapter 4

Descriptions of the Experimental setup

This chapter discusses hand wound magnetics design, PWM signal generation, Power Stage Design, Sensing circuitry around the power stage. The FPGA control signals are capable of providing programmable duty ratio and phase shift to the primary and secondary side of the DAB. An isolated sensing board was developed in order to capture state variables like the inductor currents, supercapacitor voltage and DC bus voltage. Several customized circuits like isolated half bridge gate drivers, isolated voltage and current sensing methods were implemented for ease of controlling the converter. All the magnetics in the converter prototype were hand wound and customized. The core geometry design and wire gauge selection followed by a step by step design process for both the high frequency transformer and the filter inductors.

4.1 Transformer Design

One of the most important component for this converter topology is the high frequency transformer, which is to be designed to operate without saturation. A step by step design method is proposed in [14], following K_g method of designing magnetic elements. That is followed, with modifications, to arrive at the appropriate core geometry and magnetic material of the transformer. Fig. 4.1 depicts the ideal waveform of the voltage applied at the primary of the high frequency transformer assuming a 1:1 turns ratio as mentioned in Chapter2. The applied primary volt-seconds or flux linkage is given by:

$$\begin{aligned}
\lambda_1 &= \int_{\text{positive portion of cycle}} V_{CD}(t) dt \\
&= V_{OUT} D_{2max} T_s \\
&= 11.2 \times 10^{-4}
\end{aligned} \tag{4.1}$$

Next we need to choose the core material, in order to determine the material constants β & K_{fe} [14]. The core material was selected as 3C90, which according to the manufacturer's datasheet is suitable for 50 kHz high power applications. Fig. 4.2 shows the P_V vs B curve of the core material. In order to determine the Steinmetz parameters in the equation:

$$P_{fe} = K_{fe}(\Delta B)^\beta A_{clm} \tag{4.2}$$

the manufacturer provided core loss curve is fitted into a polynomial and the values of the constants are determined as:

$$K_{fe} = 33.81 \frac{W}{cm^3 T^\beta} \tag{4.3}$$

$$\beta = 2.661 \tag{4.4}$$

Now, after many iterations the core material ETD 44 is chosen for this application. Which has the following geometrical core constants: $A_c = 1.74 cm^2$, $W_A = 2.13 cm^2$, $MLT = 7.62 cm$, $l_m = 10.3 cm$, & $\Delta B = 400 mT$. Due to unavailability of Litz wire, SWG 17 was selected for this application after referring to the datasheet, which has a cross sectional area $A_w = 1.5 \times 10^{-5} cm^2$. With these material and core choice and a total allowable power loss of 10 Watts, we get the required geometric constant of the core

$$K_{gfe} \geq \frac{\rho \lambda_1^2 I_{rmsmax}^2 K_{fe}^{\frac{2}{\beta}}}{4 K_u P_{tot}^{\frac{2+\beta}{\beta}}} \times 10^8 = 0.02883 \tag{4.5}$$

where ρ is the resistivity of copper and P_{tot} is the maximum allowed loss in the transformer. (taken as 10 watts) As this value in Eq. 4.5 is greater than the geometrical constant value of ETD44 core (56.2×10^{-3}) we can use this core with less than 10 watts of loss. With the same design the peak value of flux density is given as:

$$\Delta B = \left(10^8 \frac{\rho \lambda_1^2 I_{rmsmax}^2 (MLT)}{2 K_u W_A A_c^3 l_m \beta K_{fe}} \right)^{\frac{1}{\beta+2}} = 100 mT \tag{4.6}$$

Again, this calculation in Eq. 4.6 shows that, with this operation, the peak flux density can reach the maximum value of 100 mT, which is much less than the saturation limit of the material used (400 mT), hence again this design should work.

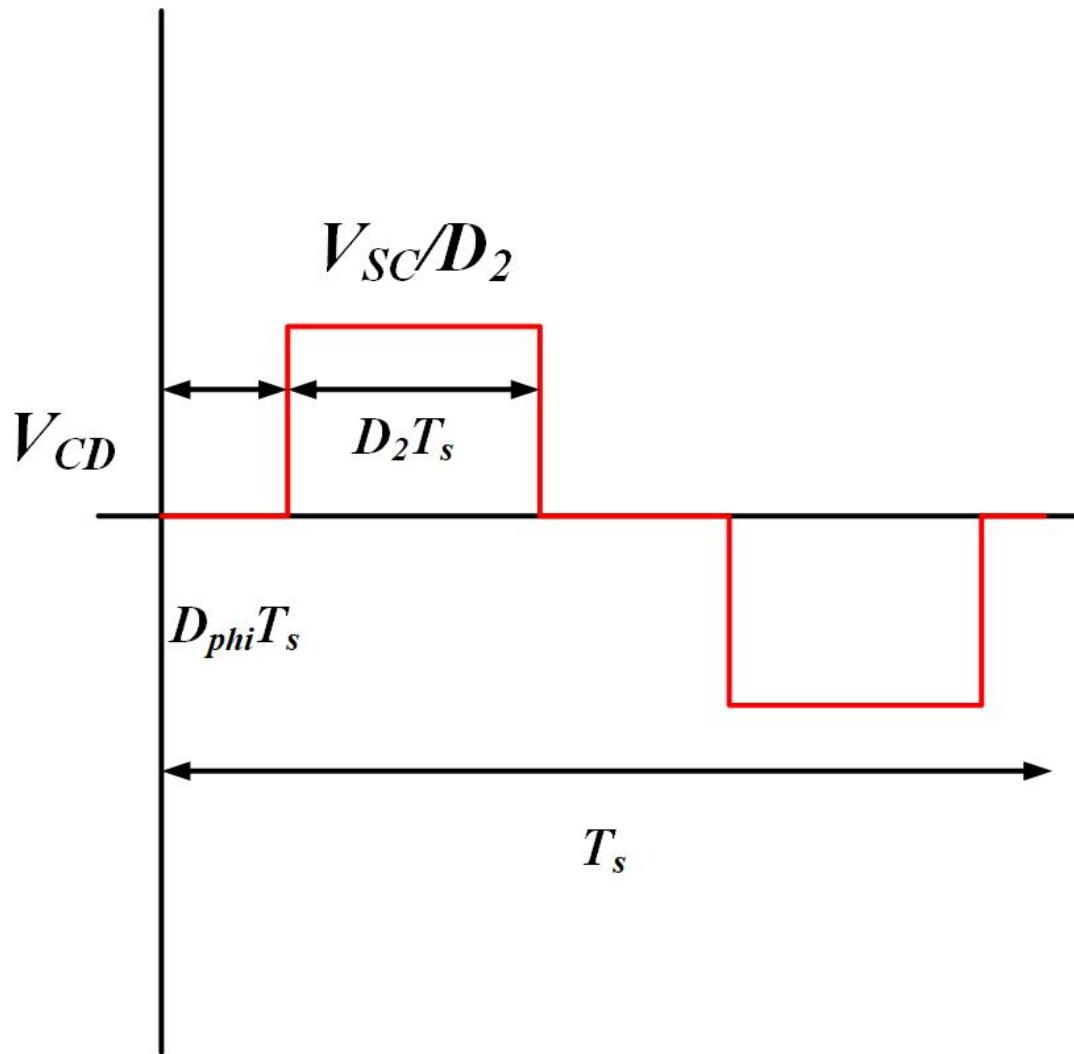


FIGURE 4.1: Primary voltage waveform across the primary of the transformer

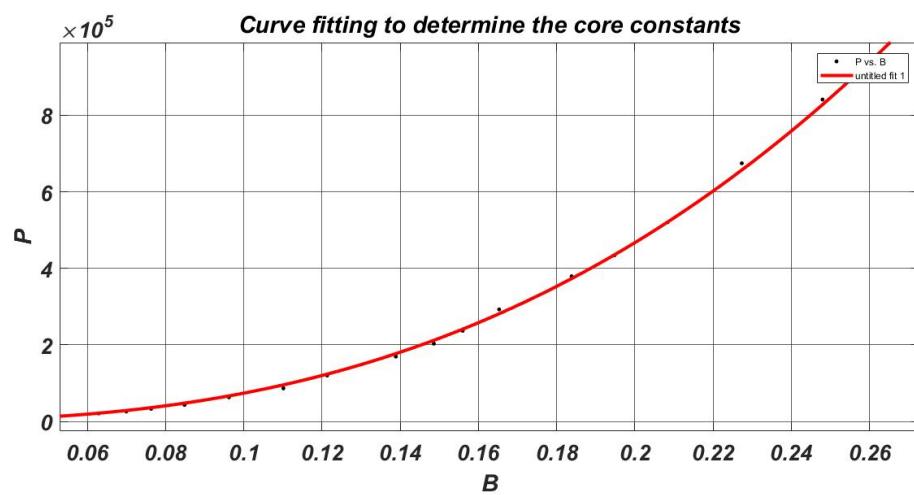


FIGURE 4.2: P Vs. B characteristics for 3C90 core material to determine the Steinmetz Parameters

Finally to evaluate the number of turns of the transformer we have

$$\Delta B = \frac{\lambda_1}{2n_1 A_c} \implies n_1 = \frac{\lambda_1}{2\Delta B A_c} \times 10^4 \approx 18 \quad (4.7)$$

Hence, we will require 18 turns at both primary and secondary, which again is quite feasible. So, **ETD44** core, **3C90** material, **SWG 17 wire** is used for the transformer.

TABLE 4.1: Summary of Transformer Design

Core Material	3C90 Ferrite Core
Core Geometry	ETD44 Planar E Core
Number of Primary & Secondary turns ($n_1 = n_2$)	18
Wire Gauge	SWG 17 Wire

4.2 Source Characteristics

- **Battery Port:** A maintenance free valve regulated Lead-Acid battery, with nominal capacity of 400 Ah at 10 C discharge rate is used. The battery has 50 cells, with a rated voltage of 100 Volts. Tapings at 25 cells are used to extract a voltage source of 50 Volts. Fig. 4.3 shows the series connected battery cells.
- **Super Capacitor Port:** 56 Volt rated Supercapacitor, with high power density and upto 14 years of DC life. Rated Capacitance of one pack is 130F, with ESR DC value of 8.1 mΩ. Fig. 4.4 shows the hardware setup.

These two sets of energy storage devices will be acting as primary sources supplying the ‘3+1’ port converter. The load port will typically be emulated by the DC grid. So that the load can sink power and during regeneration mode can also supply power to charge the energy storage devices.

4.3 Components for hardware development

The power stage of the board involves several components except the magnetic structures described in Sec. 4.1. A summary of the specifications and relevant hardwares are presented in Table .4.2. The most important part of the switching converter is the half bridge gate drivers and the signal conditioning circuit around it. The development of which is presented in the next section.



FIGURE 4.3: Series connected 100Volts battery packs

4.4 Phase Shifted PWM Gate Signal Generation

Nexys 2 Spartan-3E FPGA board was used as a controller board. It has an oscillator of 50 MHz, which makes the FPGA clock period $T_s = 20\text{ns}$. A reference for the FPGA manual was used from the available [Datasheet](#). Fig. 4.5(a) shows the FPGA board for gate signal generation.

4.4.1 Reference Carrier Generation

To generate the reference triangular carrier signal a simple MUX based logic was followed inside the FPGA. A 2 bit integrator was used at first, to generate a ramp signal which



FIGURE 4.4: 130F, 56 V supercapacitor packs

TABLE 4.2: Specifications and parameters for the 50 KHz ‘3+1’ port prototype converter

Switching Frequency f_s	50 kHz
Battery Voltage V_{BAT}	50V nominal, 40 – 60 V
Super Capacitor Voltage V_{SC}	22 V to 56 V
Load Voltage V_{OUT}	200V nominal
Total Power P_{max}	1 kW(components designed for 2 kW)
Transistors Q_1 to Q_8	Infenion SPW52N50C3
Gate Drivers	Texas instruments UCC21521
Inductors $L_1 \& L_2$	300 μ H
Inductors $L_3 \& L_4$	200 μ H
Leakage Inductor L_r	60 μ H

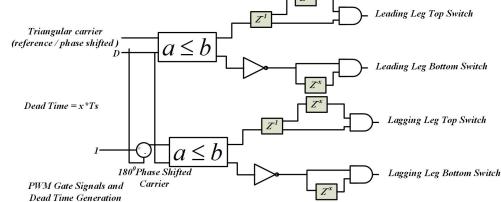
ramps up to the value of 4 at $2T$ time. ($T = 20^{-6} sec$)

$$\begin{aligned}
 y(t) &= x(t); 0 \leq x(t) \leq 1 \\
 &= 2 - x(t); 1 \leq x(t) \leq 2 \\
 &= x(t) - 2; 2 \leq x(t) \leq 3 \\
 &= 4 - x(t); 3 \leq x(t) \leq 4
 \end{aligned} \tag{4.8}$$

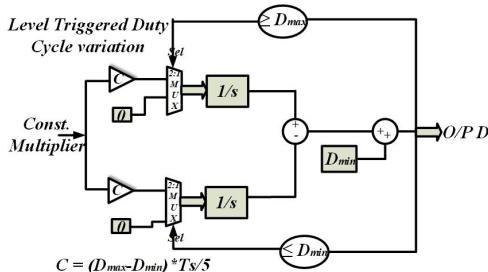
Using this logic, the generated signal $y(t)$ is a triangular carrier which goes from 0 to 1 in a switching time interval of $20\mu s$ (Since switching Frequency is 50 kHz). Fig. 4.5 summarizes the actual results from the FPGA after implementation of Eq. 4.8.



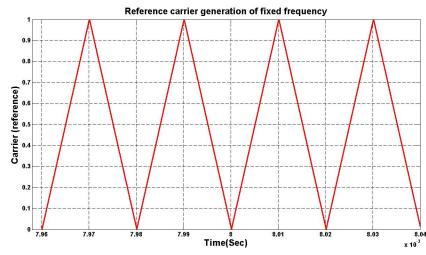
(a) Nexys 2 FPGA board used to generate Gate Pulses for the switching converter (b) Pulse Width Modulation along with dead time generation for 4 switches in any side of the transformer



(a) Nexys 2 FPGA board used to generate Gate Pulses for the switching converter (b) Pulse Width Modulation along with dead time generation for 4 switches in any side of the transformer



(c) FPGA Control scheme



(d) Triangular Reference Carrier

FIGURE 4.5: Fixed Frequency Reference Carrier Generation

4.4.2 Pulse Width Modulation and Dead Time implementation

The converter has a symmetric structure, where both the primary and the secondary side switches require 4 gate signals. In each leg, top and bottom switches get complimentary signals, whereas 2 legs in one side of the transformers are phase shifted by 180^0 . The complimentary signals need dead times inserted between them. The arrangement of dead time can be made in the Gate Driver of the power board also. But, for flexibility in the design, a variable dead time generation procedure is included in the FPGA. Simple Pulse Width Modulation strategy is followed to produce the required duty ratio of each leg. The Triangular carrier signal is compared with the duty cycle command:

$$s(t) = \begin{cases} 1 & \text{if } D \geq y(t) \\ 0 & \text{if } D < y(t) \end{cases} \quad (4.9)$$

Fig. 4.5(b) shows the scheme of Pulse generation for any 4 switches at any end of the transformer. A variable dead time strategy is implemented in the form of the variable

x. The dead time can be calculated as $T_d = x \times 20^{-9} \text{ sec}$

4.4.3 Dynamically Phase Shifted Triangular Carrier Generation for power flow

As discussed in Chapter 2, for controlling the power transferred through the Dual Active Bridge structure, we require a phase shift. The power is transferred from the leading bridge to the lagging bridge. In this way, bidirectional power flow can be achieved, if either of the two bridge is made lagging with respect to the other. Also Eq. 2.8 suggests that using D_{phi} as a control variable the power flow from the battery port can be controlled. To operate the converter in open loop condition, A variable phase shift generation capability was required from the FPGA. The toggle switches in the Nexys 2 board was used to discretize the maximum phase shift $D_{phimax} = 1.45\mu\text{sec}$ in 32 discrete steps.

$$D_{phi} = (\phi_1 \times 5 + \phi_2 \times .25 + \phi_3 \times .125 + \phi_4 \times .0625 + \phi_5 \times .03125) \times 1.5\mu\text{sec} \quad (4.10)$$

Fig. 4.6(b) shows that for a different duty ratio PWM signals if we want to generate a phase shift of T_{phi} for the lagging signal, equivalent phase shift required between the triangular carrier signals is given by $D_2 - D_1 + T_{phi}$. Using a similar analysis, we can show that for a leading signal with duty ratio D_2 , the equivalent phase shift by which the carrier needs to lead the reference carrier is given by $D_1 - D_2 + T_{phi}$. The implementation of this scheme is shown in Fig. 4.6(c). Finally the output of the phase shifted carrier block is used in the PWM block of Fig. 4.5(b). Fig. 4.7 shows the implementation of the phase shifted carriers in the Nexys 2 board. A phase shift of $1.45\mu\text{sec}$ was deemed adequate to transfer the rated power at rated voltages in the load port and passive port respectively.

4.4.4 Dynamically varying Duty ratio generation for open loop PWM Control of the Boost Function

Eq. 2.1 clearly suggest that the voltage level at each passive port and load port V_C & V_{OUT} depends on the respective duty ratios D_1 & D_2 . As this voltage levels also control the power flow across the transformer, controlling them is essential for the operation of the multiport converter. For open loop operation a Level Triggered Duty ratio control functionality was implemented in the FPGA board. 4 push button switches were used to either increment or decrement the duty ratio of the switches at both sides of the transformer. An anti windup mechanism was also followed, to ensure variation in duty

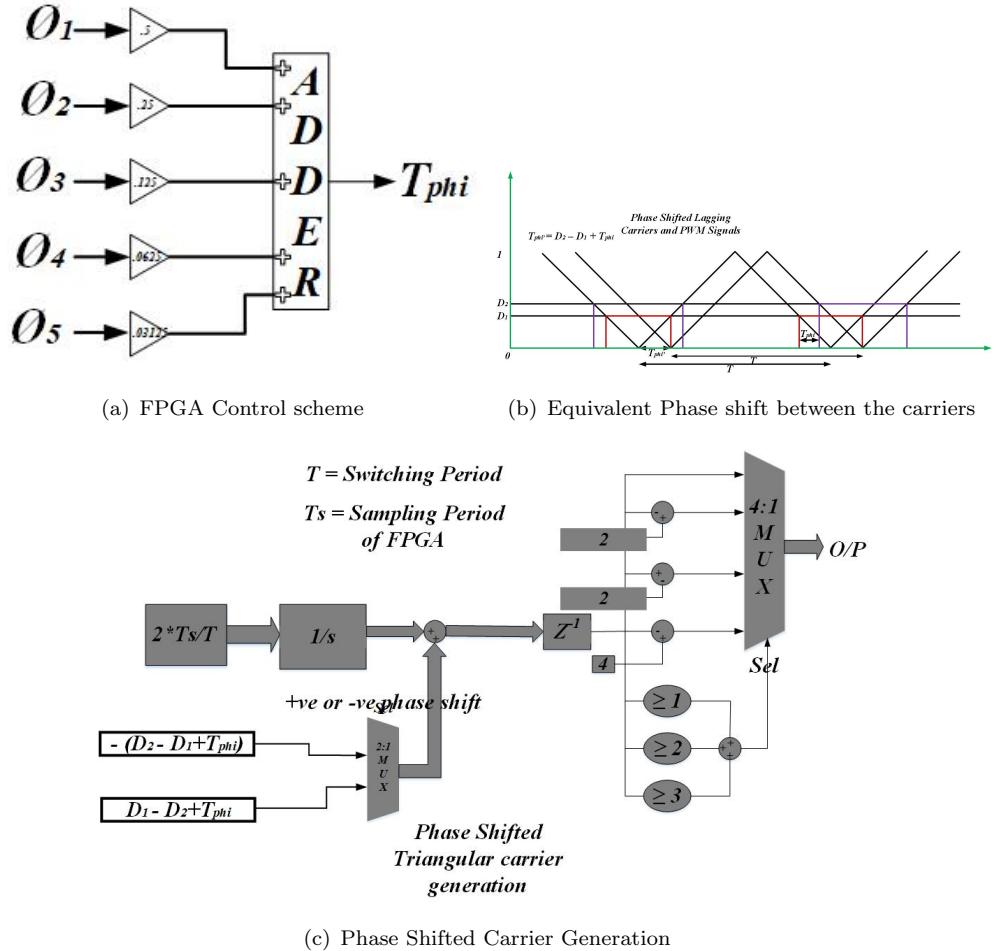


FIGURE 4.6: Fixed Frequency Phase Shifted Carrier Generation

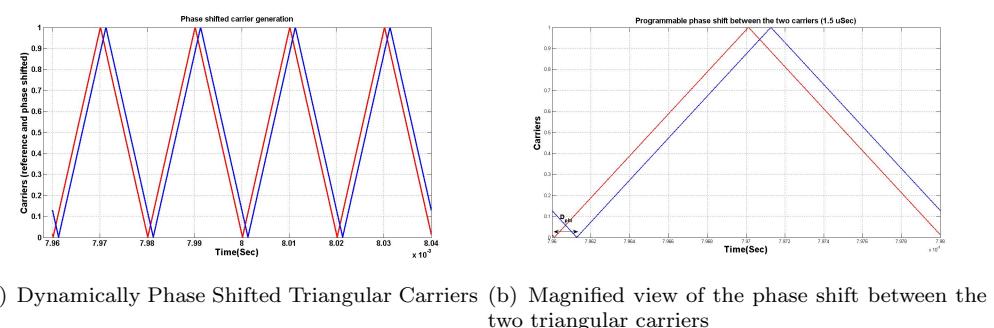
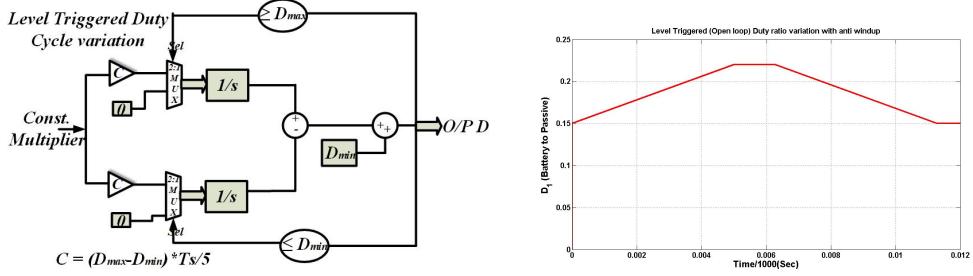


FIGURE 4.7: Phase shifted and reference carriers



(a) Level triggered variation of D between D_{min} & D_{max}
(b) Anti windup and smooth variation of Duty ratio between D_{min} & D_{max}

FIGURE 4.8: Level Triggered Duty Ratio variation

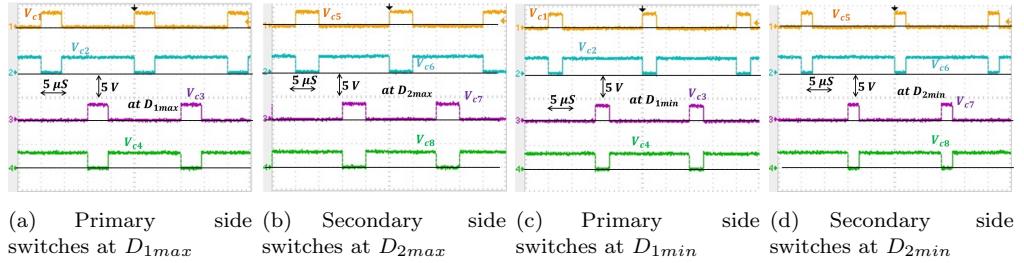


FIGURE 4.9: Complimentary and Phase shifted PWM signals with variable Duty

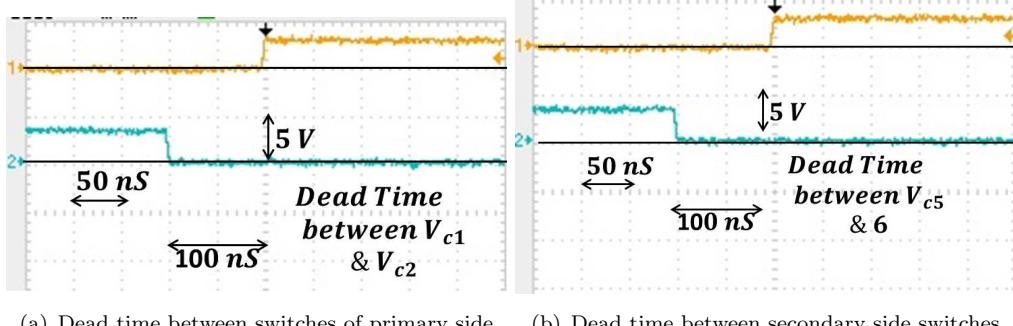
ratio, without saturation. The maximum and minimum possible values of the duty ratios were designed according to Eq. 2.11 & Eq. 2.12. Fig. 4.8 records the FPGA scheme and the result of the implementation. One may note, that the values of D_{max} & D_{min} are programmable.

4.4.5 Output Waveforms

To verify the FPGA outputs, experimental waveforms were obtained including the Receiver Transmitter Board. To ensure zero cross talking between the PWM signals, each signal was given a corresponding return current path along with the PWM signal.

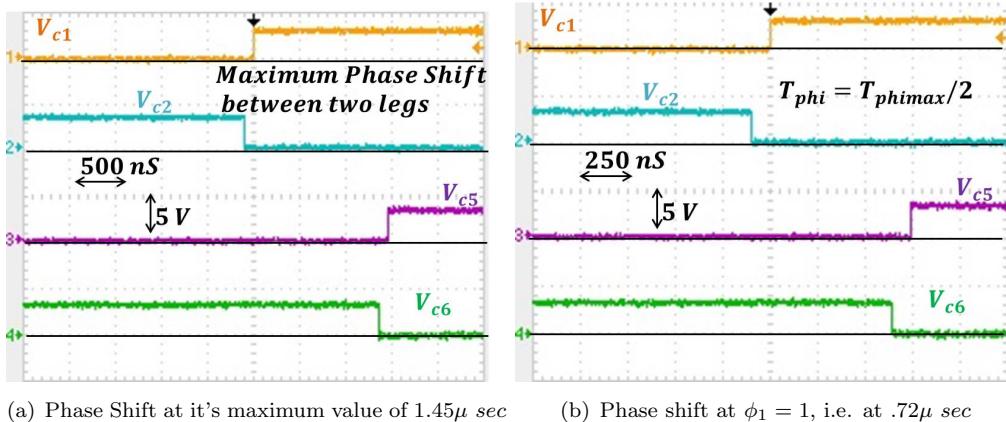
4.4.5.1 4 Gate pulses corresponding to one Full Bridge

In each side of the transformer there is a full bridge switching structure. The gate signals to the switches in the same leg are complimentary with some dead time, whereas the other legs gate pulses are 50% out of phase. As described in Sec. 4.4.4 the duty ratio control ensures that the Duty ratio of the top switches can be varied between the specified ranges. The Dead time implementation as discussed in Sec. 4.4.2 is also checked for complimentary signals of switches in the same leg. The variable x mentioned in Sec. 4.4.2 is taken as 5 in this case.



(a) Dead time between switches of primary side (b) Dead time between secondary side switches

FIGURE 4.10: Implementation of a 100ns dead time between top and bottom switches' PWM signals



(a) Phase Shift at it's maximum value of $1.45\mu \text{ sec}$ (b) Phase shift at $\phi_1 = 1$, i.e. at $.72\mu \text{ sec}$

FIGURE 4.11: Variation in Phase shift

4.4.5.2 Phase Shift Variation between two Full Bridge Structures

Fig. 4.11 shows the implementation of dynamically varying phase shift strategy described in Sec. 4.4.3. The PWM signals for the two phase shifted legs at the primary and the secondary sides are shown at maximum phase shift and at a medium phase shift. Similar 32 discrete values of phase shifts can be generated to control the power flow from the battery port to the load port.

4.4.5.3 Duty Cycle Variation of D₁ & D₂ with fixed phase shift

The variation in the phase shift and the duty ratio are independent of each other. Keeping the phase shift fixed, we can modify the duty ratio to change the DC bus voltage V_C & V_{OUT} , which in turn can also modify the power flow. Fig. 4.12 summarizes this operation. As we can see the phase shift is kept fixed while the duty ratio of all 8 switches are varied.

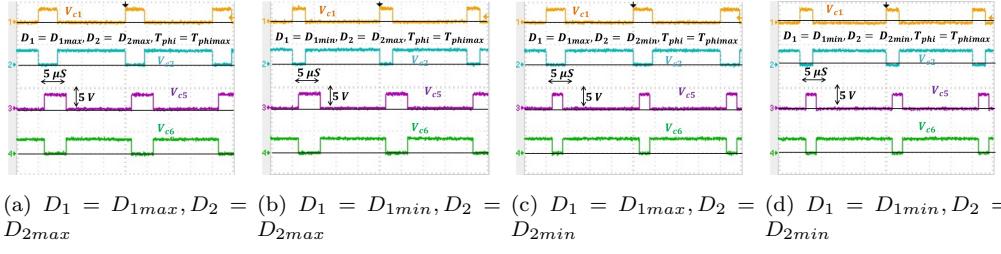


FIGURE 4.12: Variation in the Duty Ratio with fixed Phase shift of $T_{phi} = 1.5\mu s$

4.5 Isolated Half Bridge Gate Driver Design and Implementation

4 UCC21521 half bridge gate driver ICs were used to drive the 2 full bridge structures. This Gate Driver has isolation in itself and also gives bootstrap feature to drive the high side switches. But, in this case, isolated power supplies were used to drive the switches. Hence, the high side switch was driven by an isolated supply whose ground was referenced to the switch node.

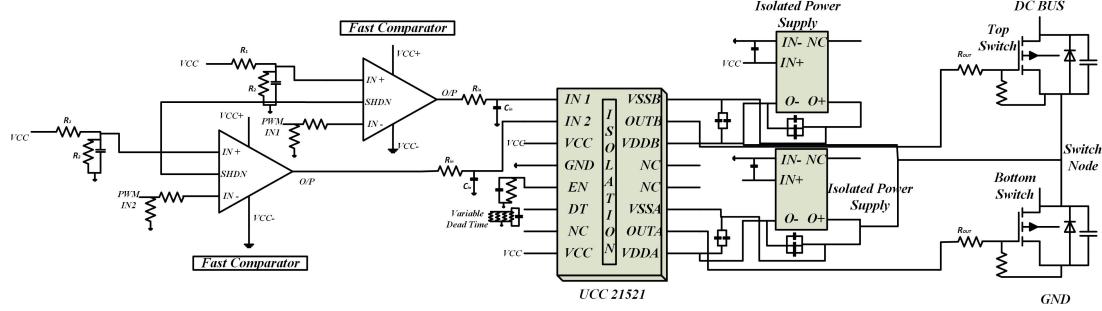
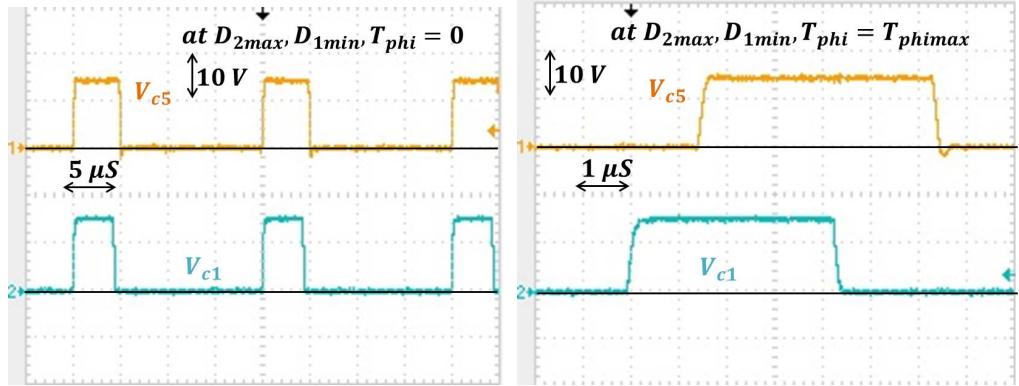


FIGURE 4.13: Isolated Gate Driver, with arrangements of shutdown, driving a set of half bridge power MOSFETs

4.5.1 Design of the Shutdown Feature

A Fast comparator IC was used with shutdown capabilities. At the $IN+$ terminal of the comparator, a R-C filter was implemented to make the voltage 1.5 Volts. $V_{IN+} = \frac{V_{CC} * R_2}{R_1 + R_2}$. Hence, at the input, resistances R_1 & R_2 were respectively chosen as $10k\Omega$ & $4.75k\Omega$ and as $V_{CC} = 5$ Volts, this voltage level was, $V_{IN+} = \frac{5 * 4.75}{14.75} = 1.61$ Volts. The FPGA output voltage is 3.3 Volts, when the gate signal is high. In this way, the comparator output is ensured to be high, when the FPGA gives a positive pulse. The shutdown pin is connected to a fault signal. If this fault signal is made high PWM signals won't reach the gate drive ICs and switching action will stop.



(a) Gate Driver output waveform with zero phase shift between primary and secondary side switches amount of phase shift between primary and secondary

FIGURE 4.14: Variation in Phase shift

4.5.2 Input Filter Design

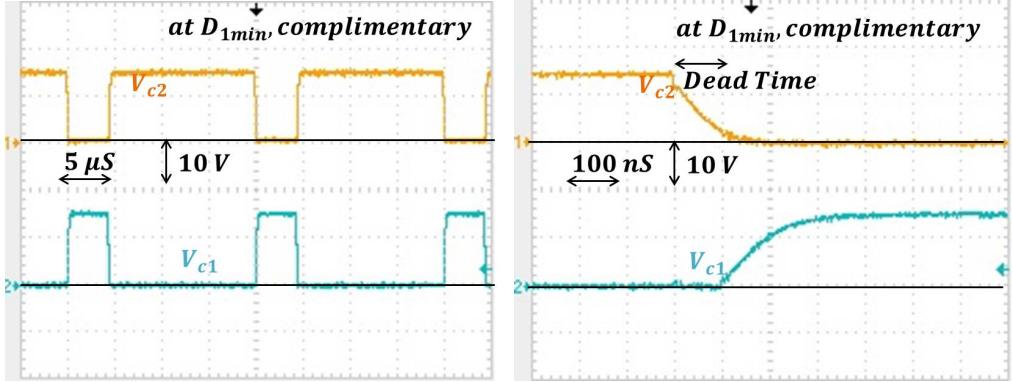
It is recommended in [UCC21521](#) that at the input pin of the gate driver ICs, a R-C filter with bandwidth close to 100MHz be used to avoid shaping of the signals. Hence, $R_{in} = 51\Omega$ & $C_{in} = 33pF$ was chosen for the input filter.

4.5.3 Gate Driver Output Resistor

To reduce EMI and to finetune the Gate Driver Delay, at the output of the Gate Driver a resistance is included to the gate of the switch. Fig. [4.13](#) shows this as R_{OUT} . A tunable 0806 pad was used, so that the value of the resistance can be modified if needed. During experiments a resistance of $R_{OUT} = 2.2\Omega$ was connected. Also, to reduce high $\frac{dV}{dt}$ noises, the ground node of the isolated gate driver outputs were tied to the source of the respective switches with a $100k\Omega$ resistance.

4.5.4 Hardware Results

The design of the gate drive circuitry was implemented in the PCB. Prior to powering up the board, the gate driver performance was verified. Fig. [4.14](#) shows the variation in D_{phi} . The gate driver is able to follow the phase shift command of the FPGA. [UCC21521](#) suggests that to have a programmable dead time, a variable resistance should be connected at the DT pin of the ic. $DT = R(\text{in k}\Omega) \times 10ns$. The hardware verification is done with a $10k\Omega$ resistance connected at the DT pin. This provides $100ns$ dead time on behalf of the gate driver. In addition to this, The FPGA implementation



(a) Complimentary gate pulses at the output of the gate driver for one switching leg
 (b) Dead time implementation at the output of the gate driver. ($DT = 100\text{ns}$)

FIGURE 4.15: Complimentary gate Drive Signals with Dead Time

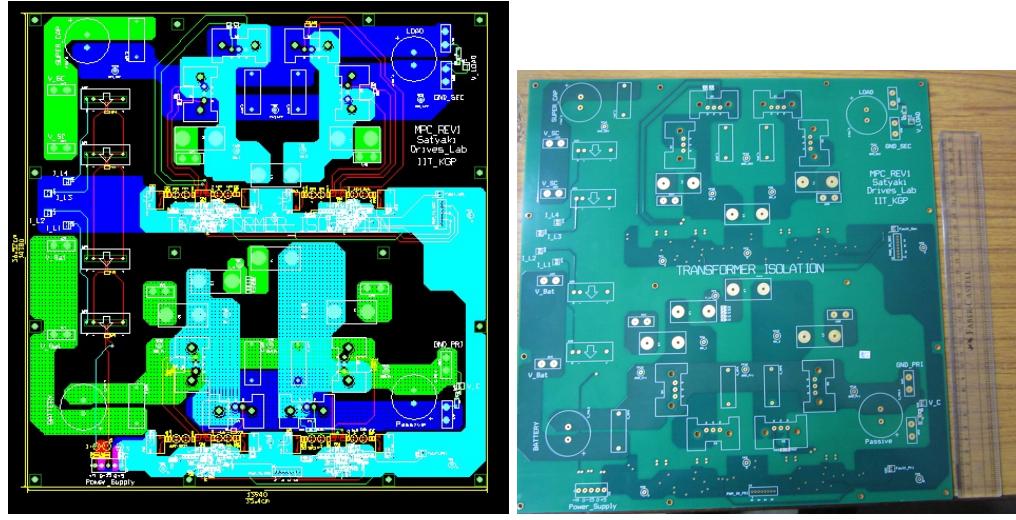
discussed in Sec. 4.4.2 gives an additiona control over the dead time. Fig. 4.15 shows the complimentary signals for one half bridge structure along with the dead time.

4.6 PCB Design and Sensing Circuits

The power board contains the 4 half bridge switching structures, with heat sink for each switch, along with the Isolated Gate Driver Circuits mentioned in Sec. 4.5. Film capacitors, with very low ESR values, are used to absorb the switching ripples of each leg. $1000\mu F$ electrolytic capacitors are mounted at each of the 4 ports to act as large filter capacitors. In addition to these, the power board also contains 4 LEM current sensors to measure the filter inductor currents at the current fed ports of the converter. Also, to sense the Passive DC bus voltage & the load port voltage, (V_C & V_{OUT}) scaling of the voltage level, to interface with the sensing card, is done in the power board itself.

4.6.1 Voltage Sensing Circuit

The potential divider arrangement for the DC bus voltages V_C & V_{OUT} are made in the power board itself. The buffer circuit, isolation circuit and an op-amp based gain circuit, essential to interface the measured signal with some form of controller is implemented in a separate 6 layer PCB. Fig. 4.17(c) shows this PCB. The schematic representation of the voltage sense scheme is depicted in Fig. 4.17(a). The value of the resistances in the potential divider circuit is kept at $200k\Omega$ & $1.5k\Omega$, such that at rated DC bus voltage (200 Volts), the output is close to 1.5 volts. The output of the sensing circuit is isolated

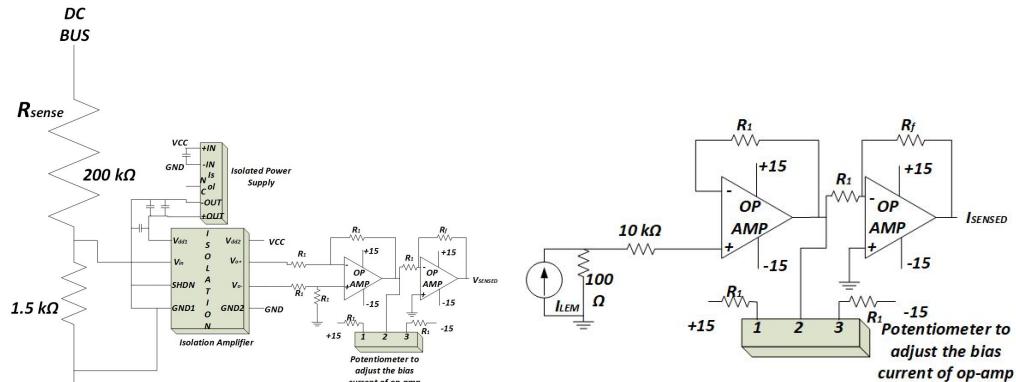


(a) Layout of the power board

(b) Fabricated Power Stage PCB

FIGURE 4.16: Power Stage PCB Design

and has a non-inverting gain of 7.5. Hence, the values of R_f & R_1 in Fig. 4.17(a) is chosen to be equal to $75k\Omega$ & $10k\Omega$ respectively.



(a) Schematic of the voltage sensing arrangement

(b) Schematic of the Current sensing arrangement



(c) Fabricated sensing PCB

FIGURE 4.17: Sensing circuitry and PCB

4.6.2 Current Sensing Circuit

As mentioned earlier, 4 LEM current sensors are included in the power board to measure the pulsating filter inductor currents of the boost configurations. The number of turns inside the LEM sensors are so adjusted that at rated condition the output of the LEM sensor acts like a current source with $I_{LEM} = 500mA$. A 100Ω resistance is used to convert this current to a voltage signal. Then, as shown in Fig. [4.17\(b\)](#) a similar isolation and gain circuitry is arranged to make this current signal compatible with the controller rating. In this case the required gain at rated condition is 3, hence the value of R_f was chosen to be equal to $30k\Omega$, keeping the value of R_1 same ($10k\Omega$). A protection circuit is also included in Fig. [4.17\(c\)](#), to trigger the fault signal of the power board. This protection circuit compares the DC bus voltages and the inductor currents to a pre-defined safety limit. If the sensed quantities crosses that threshold, the fault signal is made high and all switching action stops, stopping the converter.

Chapter 5

Experimental Results

Power stage open loop experimental waveforms and efficiency results for the multiport converter are discussed in this chapter. The hardware prototype does not have limitation in terms of operation. It is capable of running in all the 16 possible operating conditions mentioned in [12].

5.1 Testing & Evaluation of Power Stage

The power stage of the converter was used to carry out experiments with variable duty ratio and phase shifted gate signals generated through the FPGA, as mentioned in Sec. 4.4. Open loop operation, with manual variation of duty ratios D_1, D_2 & D_{phi} were checked to verify ZVS and bidirectional power flow properties of the converter topology. Finally experimentally obtained efficiency plots at different voltage levels and loads, is also presented in this section. This section is organized as follows. Sec. 5.1.1 describes the experimental setup used to emulate the bidirectional power flow and nature of the load. Sec. 5.1.2 shows the Zero Voltage Switching Transitions of the MOSFETs during power flow from Battery port to load port or, Supercapacitor port to Battery port. Bidirectional power flow and relevant PWM waveforms are discussed in Sec. 5.1.3. Finally the efficiency results are summarized in Sec. 5.1.4.

5.1.1 Description of the setup

To test and debug the power stage, we require isolated DC supplies which can act as the Battery port and the Supercapacitor ports. The only supply available in debugging the circuit is a single phase 220 volts AC supply. That is why a circuit arrangement shown in Fig. 5.1 was established.

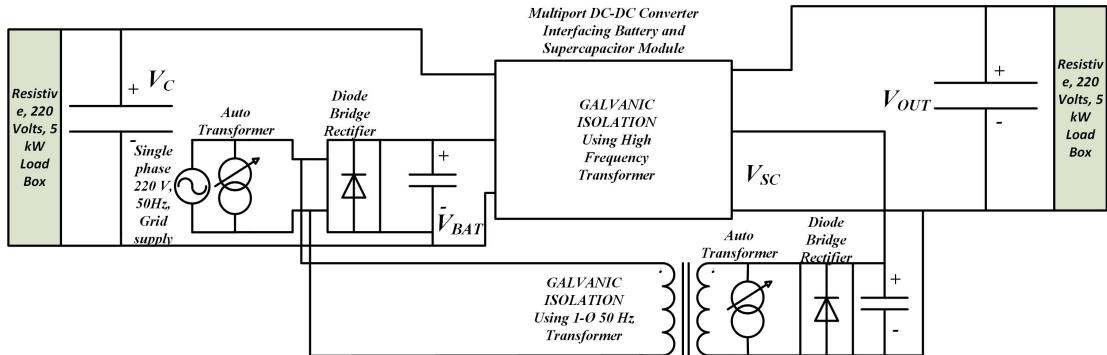
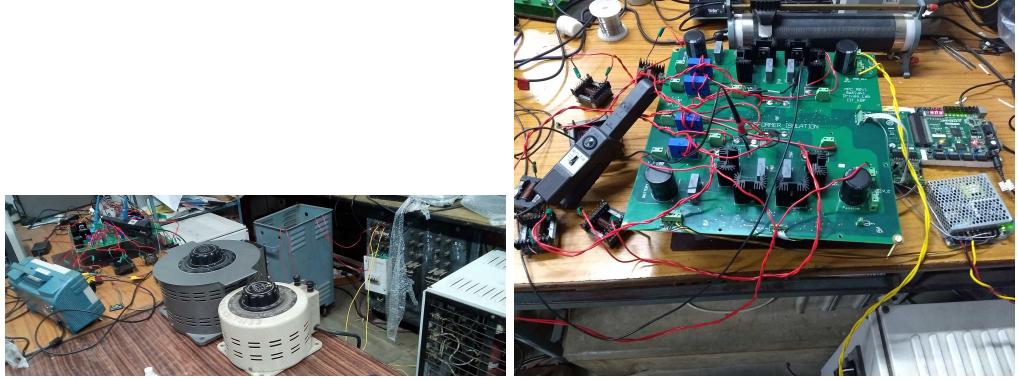


FIGURE 5.1: Schematic of the experimental setup for the power stage

- A diode rectifier is used to rectify the grid voltage and produce the Battery port DC voltage. To vary the DC output voltage of the diode bridge, an auto transformer is used to vary the single phase AC voltage supplied at the input of the diode bridge rectifier.
- To realize the supercapacitor port DC voltage a galvanic isolation is required. That's why a single phase 1:1 50 Hz AC transformer is used to isolate the grid voltage. The output of this isolation transformer is again fed to a diode bridge rectifier through an autotransformer to produce a variable DC supply at the supercapacitor port.
- It should be noted that none of this two DC sources will be able to sink power. Hence, the converter was never operated with both the sources connected. We need both DC voltages to build up the voltages at V_C and V_{OUT} ports. This voltages ensure the power transfer through the transformer. Hence, at the beginning we connect both the sources and start the converter. But, once the voltage is build up at the intended load port, we disconnect either the battery port or the supercapacitor port AC supply to see the nature of power transfer.
- To sink the power, load boxes of rating 220 Volts, 5kW were used at both V_C and V_{OUT} ports. To check bi-directional power flow capabilities of the converter, once the supercapacitor port was delivering power to the load box connected at the passive port, and then the battery port was used to deliver power to the load box connected at the load port.
- Operating modes where some power is coming across the transformer and some power is delivered through the boost action was also tested. During this mode, Battery port was delivering partial power to the load box connected at the load port, while the residual power was delivered from the supercapacitor port. This mode of operation is not very suitable for ZVS. The current fed port at the supercapacitor side will try to oppose the ZVS of the secondary side switches.



(a) Actual laboratory arrangement of the isolation
transformers and auto transformors

(b) Power board under testing

FIGURE 5.2: Experimental setup for the power stage

5.1.1.1 Issues with Current Sensing

The high frequency current, passing through the leakage inductor L_r in Fig. 2.1 is a very important state for the DAB power transfer phenomenon. This inductor eventually determines the power transferred through the high frequency transformer. Hence, capturing the current waveform was essential in the experimental process. Due to the unavailability of a high bandwidth isolated current probe, Tektronix' [A622 100 A AC/DC current probe](#) was used to capture the current waveforms. The bandwidth of this current probe is 100 kHz. Hence, the trapezoidal 50 kHz current signal captured through this probe will always be smoothed out, as if it is passing through a first order filter. A simulation exercise was carried out to characterize the behavior of the current probe. A high frequency trapezoidal current signal, similar to the one expected for i_{Lr} was smoothed through a single pole transfer function with $\omega_p = 2\pi \times 10^5$. The actual waveform and the filtered waveform are captured in Fig. 5.3. The filtered current is clearly smoothed out with some phase delay. This type of response is also expected in the actual sensed current waveforms from the hardware.

5.1.2 Zero Voltage Switching

Fig. 2.1 refers to the switching node voltages as V_{SW1} to V_{SW4} . Due to switching action of the MOSFETs these node voltages are supposed to pulsate between V_C or V_{OUT} to zero. If ZVS transition does not occur, we can see that during transition, switch node voltages will rise up to twice the DC bus voltage, due to discharging of output capacitance into the body of the device. Hence, the switch node voltages can very precisely predict whether we are achieving ZVS or not.

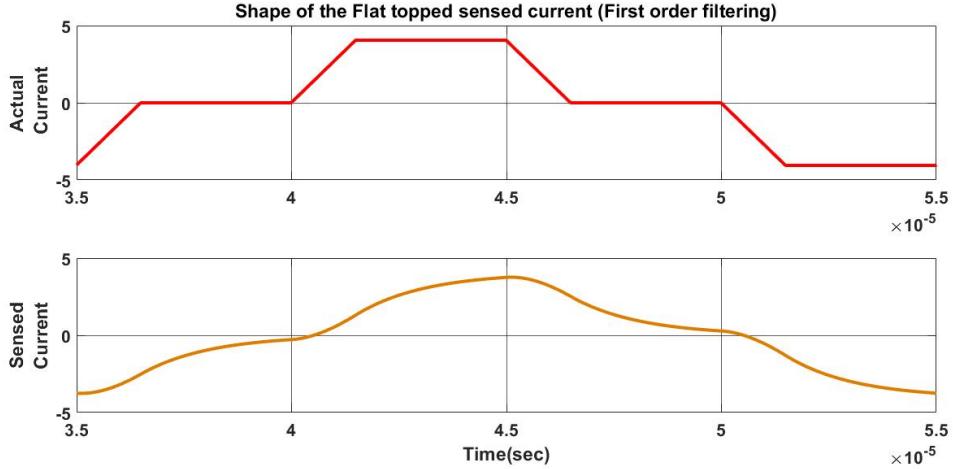


FIGURE 5.3: Actual current and expected Filtered current through A622 current probe

5.1.2.1 ZVS during power flow from Battery to load port:

According to the theoretical analysis, if power is transferred from the battery port to the load port, the leakage inductor current I_{lr} is always negative at the switching instants of all 4 switching legs. In Fig. 2.3

$$I_{SW1} = i_{Lr} - \frac{I_{BAT}}{2} \quad (5.1)$$

and

$$I_{SW2} = \frac{I_{BAT}}{2} - i_{Lr} \quad (5.2)$$

. So, for switching node 1, when V_{SW1} is rising from zero to V_C or the top device is turned on, according to Eq. 5.1 if i_{Lr} is negative then the switch current is also negative. (As power is flowing out of battery port, $I_{BAT} > 0$). Then we achieve ZVS of switch 1. Similarly during turn off of Q_1 and turn on of Q_2 , V_{SW1} is coming down to zero voltage from V_C . During this time Eq. 5.2 predicts that, $i_{Lr} > \frac{I_{BAT}}{2}$ to achieve ZVS of Q_2 . Assuming $V_C \geq V_{OUT}$ during D_1T_s period voltage across leakage inductor is always positive and at D_1T_s , I_{lr} reaches its peak value and hence, $I_{lr} > \frac{I_{BAT}}{2}$. That is why we achieve ZVS of Q_2 . Similar arguments holds true for switching node 3 as well. Hence, primary side ZVS is assured. On the secondary side however, ZVS of the bottom device of Switching leg 2 requires, the leakage inductor current going into the dot on primary side, or the current coming out of the primary side to be negative while we are switching the bottom device ON. Since the supercapacitor port is not giving any power, $\frac{I_{SC}}{2} = 0$ and hence, $I_{SW6} = i_{Lr}$. To make the inductor current come down to a negative value prior to switching on Q_6 we require sufficient V_{OUT} and D_2 , so that the negative voltage is sufficient across L_r . Top device's ZVS is always ensured, as when we turn ON Q_5 , $i_{Lr} = i_{Lrpeak} = I_1$ according to Fig. 2.1. As, $I_{SW5} = -i_{Lr}$, we will have ZVS of Q_5 .

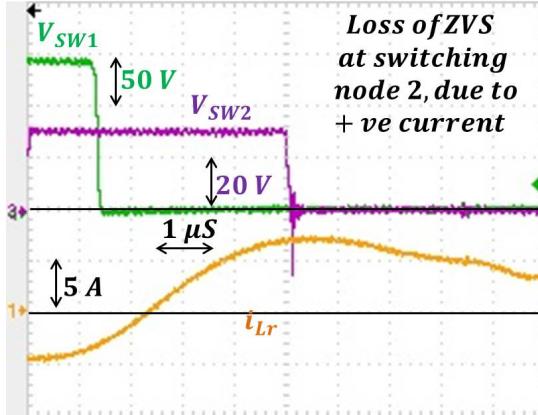
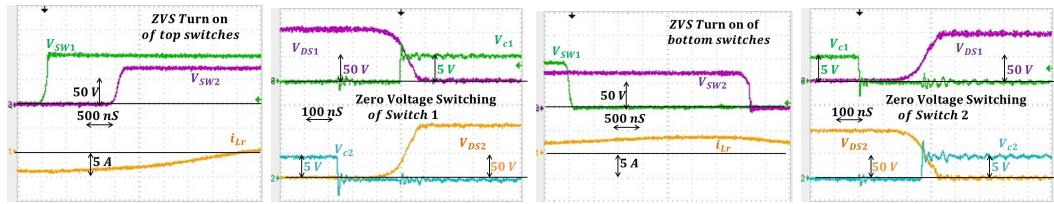


FIGURE 5.4: Loss of ZVS of bottom device



(a) Switch node voltage during turn on of the top Q_1 and bottom device in the half bridges
(b) V_{GS} & V_{DS} of Q_1 and Q_2 during Q_1 turn ON
(c) Switch node voltage during turn on of the bottom Q_2 during Q_2 turn ON
(d) V_{GS} & V_{DS} of Q_1 and bottom device in the half bridges

FIGURE 5.5: ZVS transitions during forward power flow

These transitions of V_{SW1} and V_{SW2} under ZVS is shown in Fig. 5.5. Soft transition of the top devices are shown in Fig. 5.5(a) and bottom devices are shown in Fig. 5.5(c). Now, if the supercapacitor port is also delivering some power along with the battery port, according to Fig. 2.4:

$$I_{SW5} = -i_{Lr} - \frac{I_{SC}}{2} \quad (5.3)$$

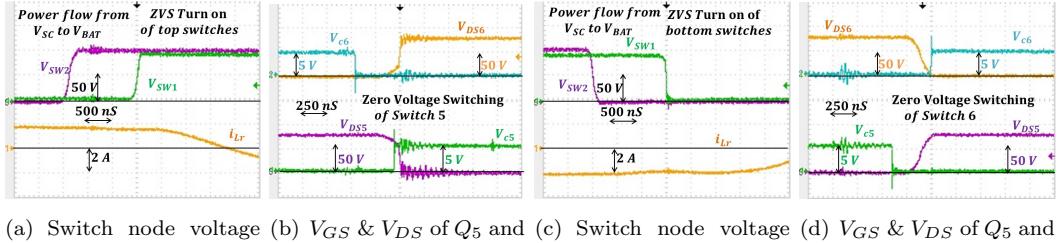
and

$$I_{SW6} = i_{Lr} + \frac{I_{SC}}{2} \quad (5.4)$$

It is clear from Eq. 5.3 and Eq. 5.4, that although Q_5 will have soft switching, but depending on I_{SC} , I_{SW6} might become positive during turn on of Q_6 . During this time Q_6 will not have soft turn ON. This situation is shown in Fig. 5.4

5.1.2.2 ZVS during power flow form supecapacitor to Passive port

Due to the topological symmetry of the converter (Fig. 2.1), all the arguments presented in Sec. 5.1.2.1 holds true for power flow from supercapacitor to the passive port. During this time switch node voltage V_{SW2} will lead V_{SW1} and the battery port current is made zero to achieve soft switching of Q_2 . Fig. 5.6 summarizes the hardware results during



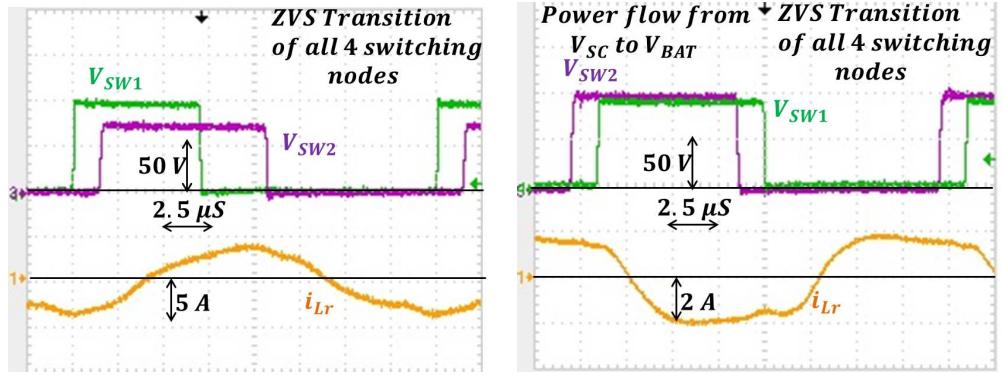
(a) Switch node voltage during turn on of the top switches
(b) V_{GS} & V_{DS} of Q_5 and Q_6 during Q_5 turn ON
(c) Switch node voltage during turn on of the bottom switches
(d) V_{GS} & V_{DS} of Q_5 and Q_6 during Q_6 turn ON
device in the half bridges

FIGURE 5.6: ZVS transitions during backward power flow

this mode of operation. Fig. 5.5 and Fig. 5.6 provides hardware verification of the soft switching capabilities of this topology during bi-directional power flow.

5.1.3 Bi-directional power flow

As mentioned in Sec. 5.1.1 to check the bi-directional power flow capabilities, arrangements were made to load the converter on both passive and the load port. The major difference between transferring power from battery to load port and from supercapacitor to passive port is the relative phase between the gate signals c_1 & c_5 . Fig. 2.2 shows the gate pulses with c_1 leading c_5 . Sec. 4.4.3 describes methods and implementation of making c_1 lag c_5 . When power is transferred from supercapacitor port to the capacitor port, effectively V_{SW2} leads V_{SW1} . Both forward power transfer and backward power transfer experiments were carried out on the experimental setup. Another feature to note is that, during the reverse power flow, direction of the leakage inductor current i_{LR} reverses. As, average power processed through the transformer is flowing from the secondary to primary in this case, the leakage inductor current going into the transformer will now be negative during the switching of $SW1$ & $SW2$ nodes. Fig. 5.7 shows the lead lag nature of the switch node voltages during both type of power transfer. One may note that, in Fig. 5.7(b) voltage levels V_C & V_{OUT} are almost same, which gives rise to a more flat-topped leakage inductor current, where as, in Fig. 5.7(a) due to unequal voltages, inductor current is not flat-topped and hence due to the filtering nature of the current probe, (refer Sec. 5.1.1.1) the inductor current is more smoothed out. The leakage inductor current and voltage profiles during forward and reverse power flow is captured in Fig. 5.8. These experimental results are in very good match with the theoretically predicted waveforms. Finally the DC link current along with the switch node voltages is shown in Fig. 5.9. It should be noted that, due to the voltage matching between V_C and V_{OUT} ports, with less amount of power transferred to the load port, all 4 switching nodes are achieving ZVS in Fig. 5.9(b). While describing the experimental setup in Sec. 5.1.1, it is mentioned that only one of the supercapacitor or the battery



(a) Switch node voltages and inductor current during forward power flow (b) Switch node voltages and inductor current during forward power flow

FIGURE 5.7: V_{SW1} leads V_{SW2} during forward power flow, and lags V_{SW2} during backward power flow

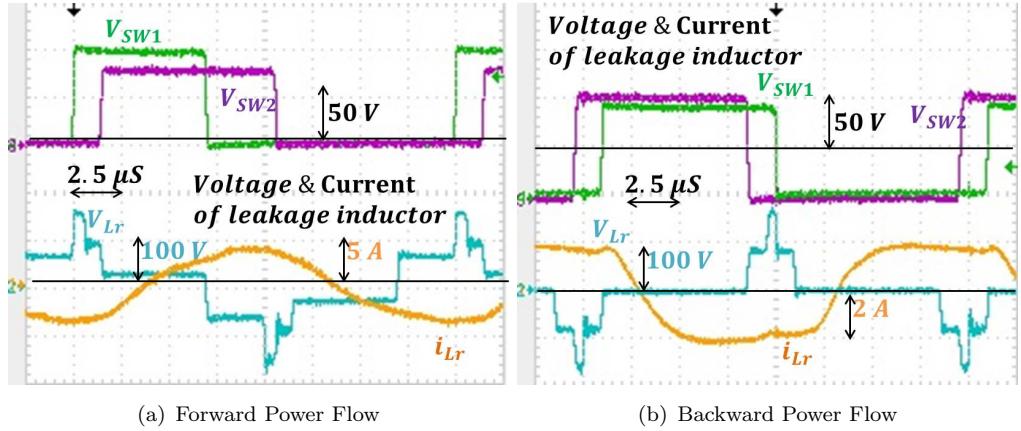


FIGURE 5.8: Leakage inductor voltage and current waveforms along with switch node voltages

port is used to transfer power, as there will be ZVS constraints if both current fed ports are operated simultaneously (refer Sec. 5.1.2). Hence, during forward power transfer the PWM current through inductor L_3 will oscillate around 0 and during backward power flow, as battery port is not supplying any power, I_{L1} will have an average value of 0. Fig. 5.10 shows the Filter inductor currents during forward power flow. The PWM current I_{L3} has an average value of 0 in Fig. 5.10(b). The battery port filter inductor is carrying an average current I_{L1} in fig. 5.10(a) to provide power at the load port. Fig. 5.11 shows the Filter inductor currents during reverse power flow. The PWM current I_{L3} here has an average value responsible for power transfer to the passive port, in Fig. 5.11(b). The battery port filter inductor is carrying an average current I_{L1} whose value is equal to 0, in Fig. 5.11(a) as there is no power source connected at the battery port. Voltages across the primary and secondary of the 1 : 1 high frequency transformer is shown in Fig. 5.12. For both forward and reverse power flows, the transformer acts

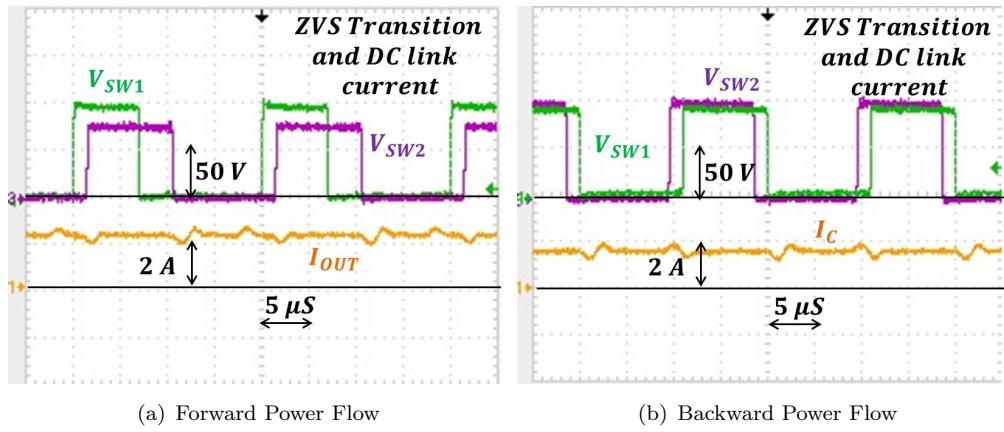


FIGURE 5.9: DC link current along with switch node voltages

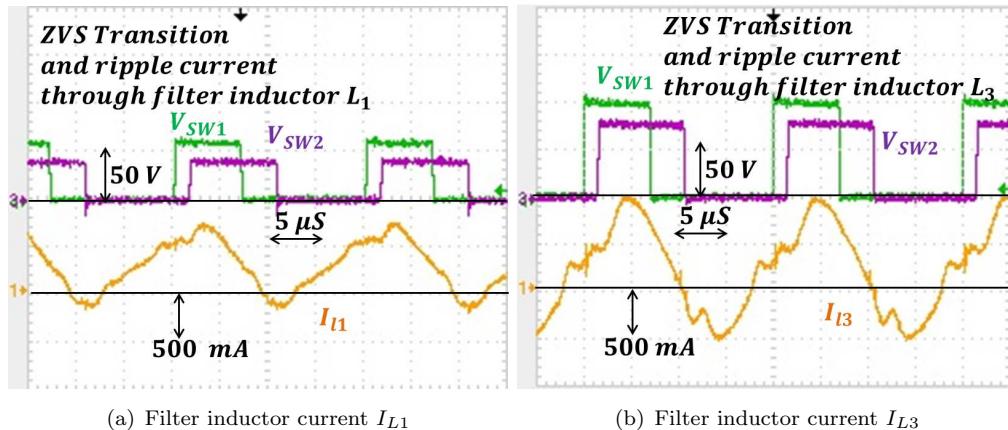


FIGURE 5.10: PWM current through filter inductors when battery port is supplying power to load port

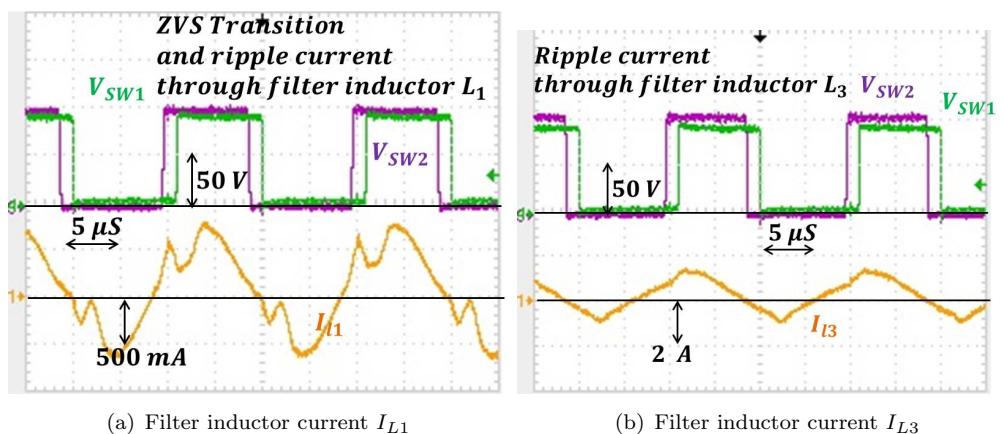


FIGURE 5.11: PWM current through filter inductors when supercapacitor port is supplying power to passive port

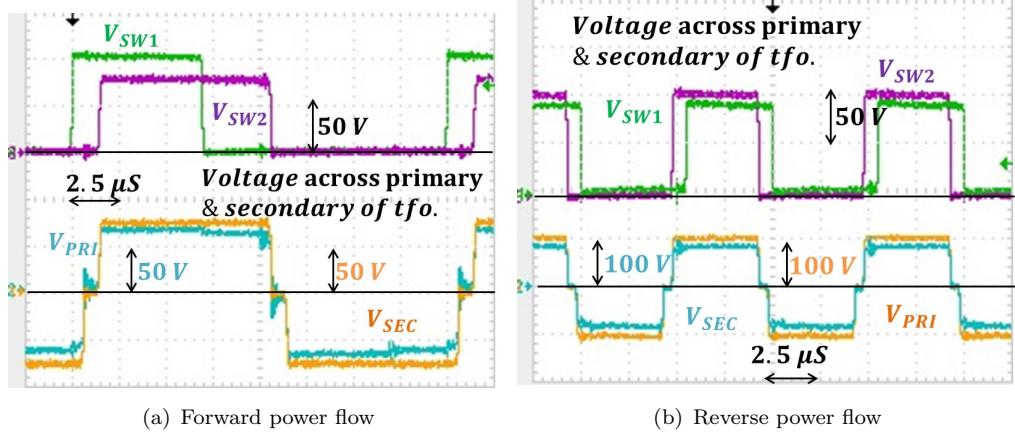


FIGURE 5.12: Voltages across the primary and secondary of the 1:1 transformer during forward and reverse power flow

perfectly well without any saturation issues. This shows that the hand wound magnetic structure design was up to the mark in terms of the converter operation.

5.1.4 Efficiency Results

At several operating points, the converter was operated for both forward and backward power transfer. In the hardware, operating conditions with discrete values of D_1, D_2 & D_{phi} were explored. As there were loss of ZVS at some points, the design was revisited and some stringent ZVS conditions were developed in Sec. 2.1.3. Using the strategy of Fig. 2.7, for ZVS over wider range of operations, the efficiency results are discussed in the following section.

5.1.4.1 Efficiency results during forward power flow

Fig. 5.13 shows the efficiency plot of the converter at three different V_{BAT} levels. The output power varies from 104 Watts to 720 Watts. The general trend of efficiency is observed. The efficiency peaks at 98%. relevant output power levels and V_{OUT} voltages are marked in Fig. 5.13. The experimental data for the forward power flow are summarized in Table 5.1. One important thing to observe from the experimental data is that, the efficiency of the converter is maximum when $V_C \approx V_{OUT}$. As load is increased the output port voltage drops, which increases conduction loss as inductor current does not remain flat-topped any more. At lighter loads efficiency drops due to switching loss. As inductor current may not be sufficient to discharge the output capacitances at light load, some switches might not undergo soft transitions. The efficiency plot in Fig. 5.13 shows typical efficiency trend. At some loading in between maximum and minimum the

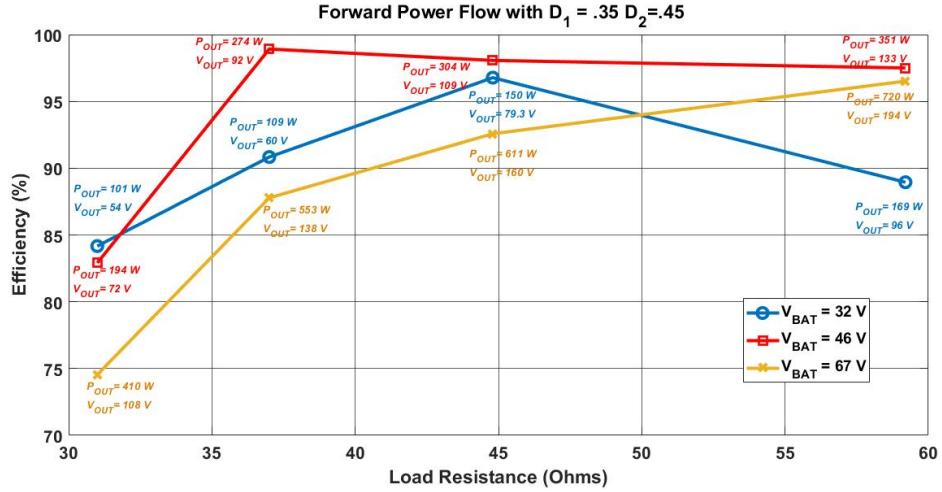


FIGURE 5.13: Efficiency Result with load variation when power flows from battery to load port

TABLE 5.1: Experimental results for forward power flow with $D_1 = .35$ & $D_2 = .45$

V_{BAT} (V)	P_{BAT} (W)	V_C (V)	V_{OUTexp} (V)	P_{OUT} (W)	Efficiency(%)	$R_{Load}(\Omega)$	V_{OUTthe} (V)
31	190	88.57	96	169	88.94	59.2	104.1
30.87	155	88.2	79.3	150	96.77	44.8	84.12
33.1	120	94.57	60	109	90.83	37	72.69
34	120	97.14	54	101	84.17	31	65.53
44	360	125.71	133	351	97.5	59.2	146.40
44.5	310	127.14	109	304	98.06	44.8	119.2
46.2	277	132	91.6	274	98.91	37	104.51
48	234	137.14	72.1	194	82.9	31	90.95
64.5	746	184.28	194	720	96.51	59.2	214.21
67	660	191.42	160	611	92.57	44.8	119.2
70	630	200	138	553	87.78	37	158.06
73	550	208.57	108	410	74.54	31	137.69

conduction and switching loss both are optimally minimum. Which increases the efficiency. Eq. 2.26 helps us to determine the load port voltage value theoretically as well. From, V_C , V_{BAT} , D_1 , D_2 , D_{phi} , T_s & L_r values, which are fixed at a particular operating point, the output power P_{BAT} can be evaluated according to Eq. 2.26. This power is dissipated at the load port. If the load resistance value is known then,

$$P_{BAT} = \frac{V_{OUT}^2}{R_{Load}} \quad (5.5)$$

Using Eq. 5.5 we can derive the value of V_{OUT} . Fig. 5.14 shows the theoretical and experimental values of V_{OUT} for forward power flow. One may observe that the experimental values have very close match with the theoretically obtained values.

5.1.4.2 Efficiency results during backward power flow

Similar experiments were carried out when the power is transferred from the supercapacitor port to the passive port. Fig. 5.15 summarizes the efficiency results. In table. 5.2 the experimental readings are tabulated. Similar trends, like forward power flow, are observed in the efficiency curve. As the relative degree of loading is quite less during backward power flow, (maximum loading of 570 Watts) efficiency is on the lower side.

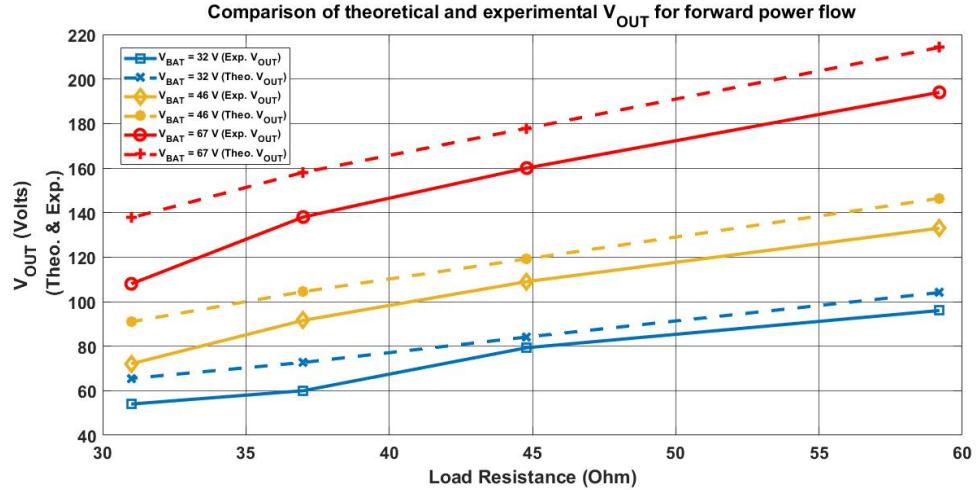


FIGURE 5.14: Theoretical and Experimental values of V_{OUT} for forward power flow

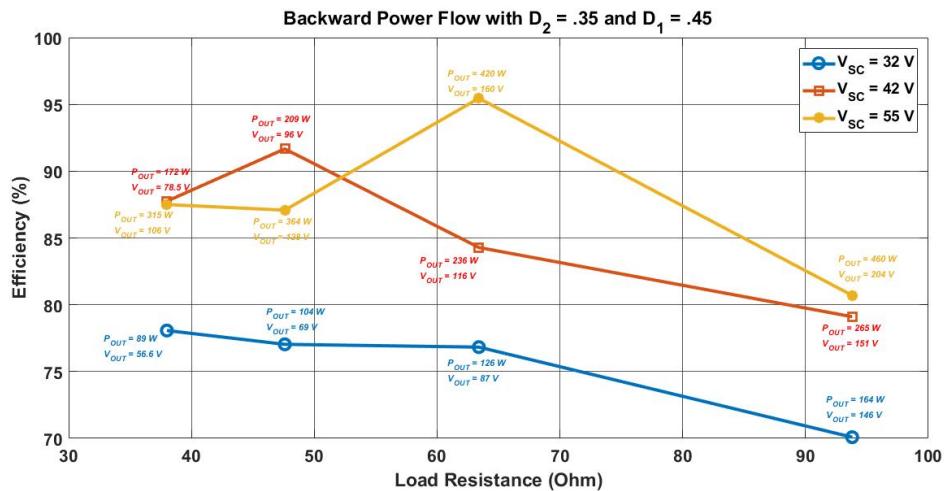


FIGURE 5.15: Efficiency Result with load variation when power flows from supercapacitor to passive port

Experimentally obtained values of V_C and the theoretically obtained values from Eq. 2.26 are plotted in Fig.5.16. Again the theoretical values are in very good agreement with the experimentally obtained results.

TABLE 5.2: Experimental results for backward power flow with $D_1 = .45$ & $D_2 = .35$

V_{SC} (V)	P_{SC} (W)	V_{OUT} (V)	V_{Cexp} (V)	P_C (W)	Efficiency(%)	$R_C(\Omega)$	V_{Cthe} (V)
27.5	234	78.57	146	164	70.08	93.8	144.42
31.2	164	89.14	87	126	76.83	63.4	104.23
32.9	135	94	69	104	77.03	47.6	86.04
34.2	114	97.71	56.6	89	78.07	38	73.93
38	335	108.57	151	265	79.104	93.8	177.08
41	280	117.14	116	236	84.28	63.4	137.71
43.2	228	123.42	96	209	91.67	47.6	115.25
45	196	128.57	78.5	172	87.75	38	98.92
51	570	145.71	204	460	80.70	93.8	238.2
55	440	157.14	160	420	95.45	63.4	186.67
57.6	418	164.57	128	364	87.08	47.6	153.67
60	360	171.42	106	315	87.5	38	132.43

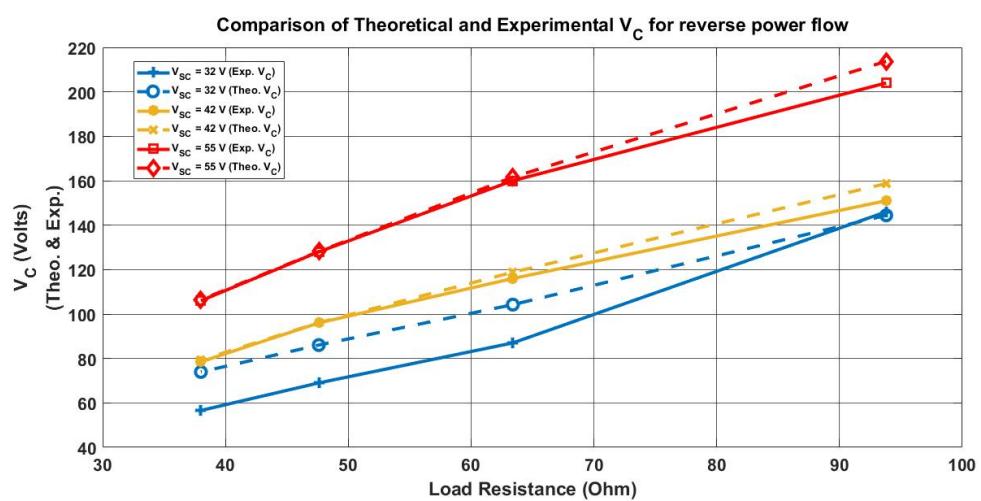


FIGURE 5.16: Theoretical and Experimental values of V_C for backward power flow

Chapter 6

Closed Loop Operation

Closed loop operation of the Multiport converter, along with small signal modeling of the plant and design of the controller is discussed in this chapter. Relevant ADC and DAC interfacing was done prior to this. Description of the modules and some experimental waveforms are also illustrated. Finally following simulation results, hardware verification of the control strategy summarizes this chapter.

6.1 Control Objectives & Small Signal Modelling:

The major control objectives of the proposed converter can be summarized as:

- The DC bus voltage should be tightly regulated at the reference value, independent of the load and energy variation in the storage devices
- For prolonged health of the battery, power flowing out of the battery port should be maintained constant, and the reference for the same, should be obtained from a Battery Management System (BMS), based on the State of Charge (SOC) estimate
- The control variables used for this plant are D_1, D_2 & D_{phi} . D_{phi} controls the power flow, D_2 regulates the load port voltage based on a boost converter dynamics and D_1 is used to do voltage matching of the DAB configuration, this maximizes converter efficiency

Depending on the control objectives, broadly the closed loop plant can be viewed as Fig. 6.1. Hence, the primary task to implement this control strategy was to derive the small signal transfer functions $G_{V_{OUT}D_2}$ & $G_{P_{BAT}D_{phi}}$

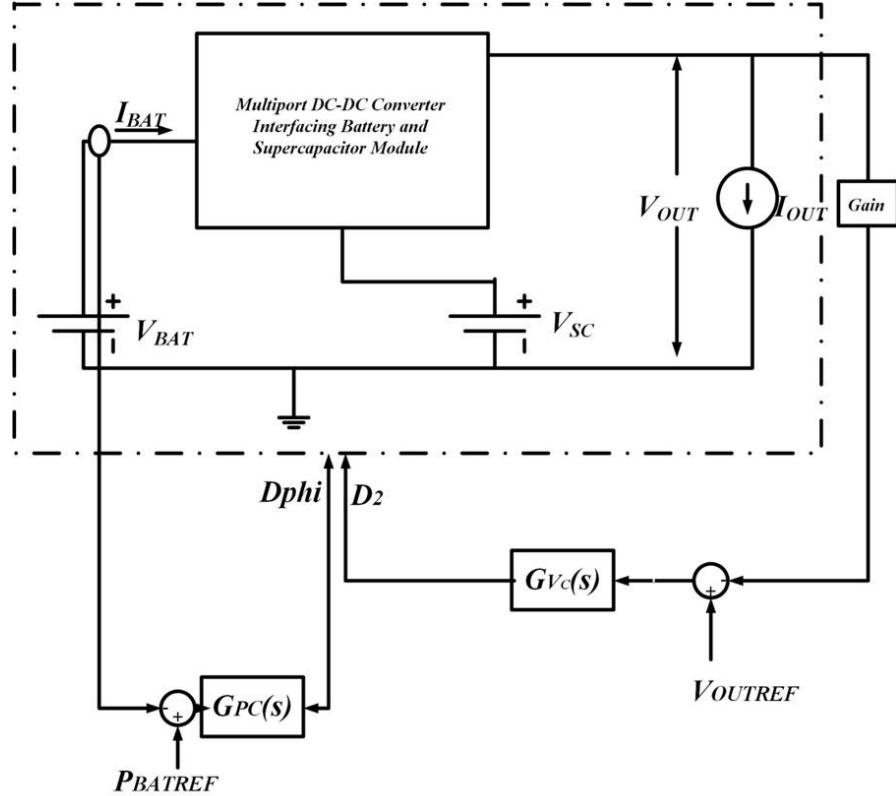


FIGURE 6.1: Controller structure of a Multi port converter

Small signal analysis of the converter was done, neglecting the dynamics of the leakage inductor and the transformer. Which gives the plant transfer functions:

$$G_{V_{OUT}D_2}(s) = \frac{\hat{v}_{OUT}(s)}{\hat{d}_2(s)} = \frac{-V_{OUT}(1 - \frac{s(L_3+L_4)}{R_{load}D_2^2})}{D_2(1 + \frac{s(L_3+L_4)}{R_{load}D_2^2} + \frac{s^2(L_3+L_4)C_{OUT}}{D_2^2})} \quad (6.1)$$

$$G_{P_{BAT}D_{phi}}(s) = \frac{\hat{p}_{BAT}(s)}{\hat{d}_{phi}(s)} = \frac{V_{SC}V_{BAT}(1 - 2D_2 + 2D_1 - 2D_p h_i)}{f_s L_r D_1 D_2}$$

To verify the theoretical findings, a plant characterization step was performed in MATLAB environment. Fig. 6.2 shows the response of the plant to a step change in the control variable D_2 . The salient features of the plant transfer function $G_{V_{OUT}D_2}$ are clear in the simulation result, which matches with the theoretically predicted small-signal model in Eq. 6.1. Similarly the other plant transfer function is predicted in Fig. 6.3.

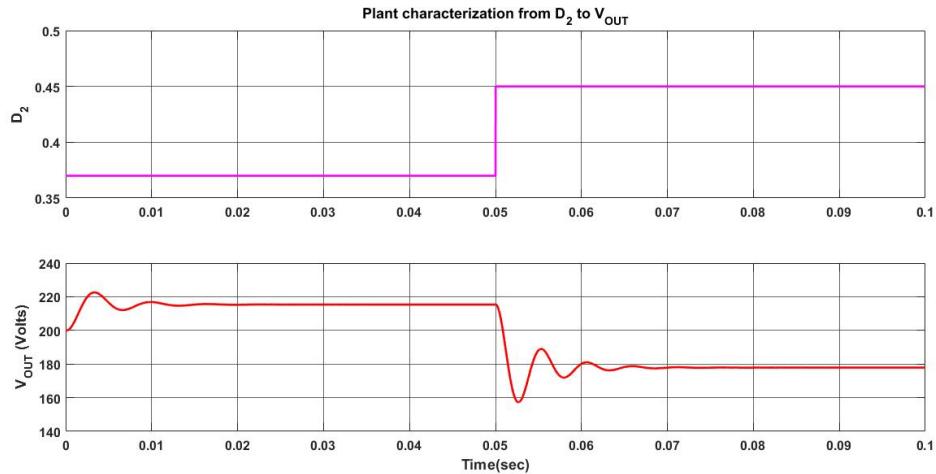


FIGURE 6.2: Step response for plant characterization form D_2 to V_{OUT}

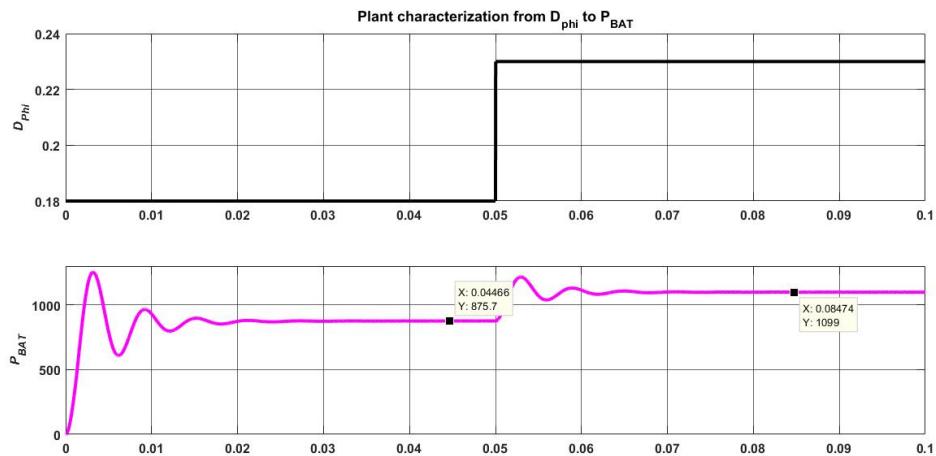


FIGURE 6.3: Step response for plant characterization form D_{phi} to P_{BAT}

6.2 Controller Design & Simulation results:

After the plant characterization, frequency domain based controller design tools (bode plots and phase margin tests) were deployed to design controllers of this MPC. A lead-lag compensator based voltage mode controller, with a crossover frequency of 2 kHz was designed, to regulate the output voltage, where as a P-I compensator, to regulate the battery power, was designed with a sufficiently smaller bandwidth was designed, so that the power loop does not see the voltage variation. The compensator structures can be described as:

$$\left\{ \begin{array}{l} G_{CV_{OUT}}(s) = \frac{G_{m1}(1+\frac{\omega_1}{s})(1+\frac{s}{\omega_z})}{1+\frac{s}{\omega_p}} \\ G_{CP_{BAT}}(s) = G_{m2}(1 + \frac{\omega_2}{s}) \end{array} \right. \quad (6.2)$$

With appropriate designs, using a nominal DC operating point, the compensator transfer functions came out to be:

$$\left\{ \begin{array}{l} G_{CVOUT}(s) = \frac{-30(s^2 + 2\pi \times 130s + 4\pi^2 \times 3000)}{80 \times (s^2 + 3000s)} \\ G_{CPBAT}(s) = \frac{1 + \frac{2\pi \times 50}{s}}{8000} \end{array} \right. \quad (6.3)$$

An additional high frequency pole was inserted in the lead-lag compensator to diminish the effects of switching noise. Fig. 6.4 represents a schematic description of the controller

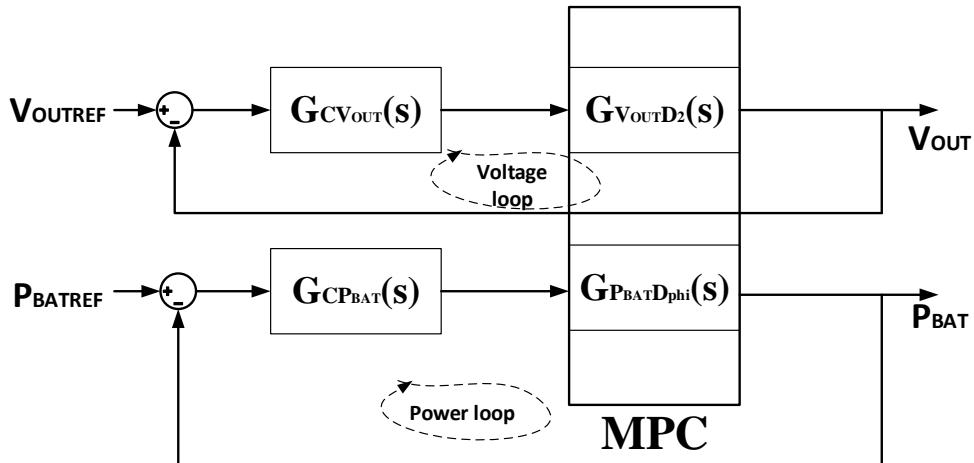
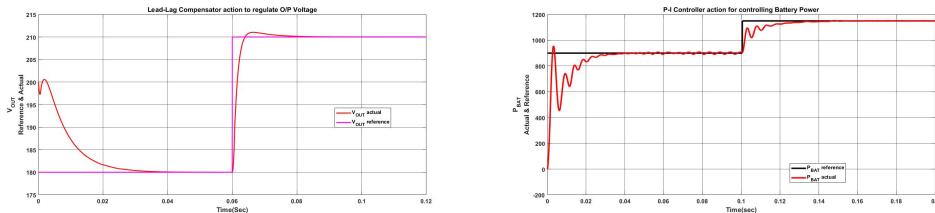


FIGURE 6.4: Nested Control loop structure of MPC

structure followed. Finally, the controllers were implemented in MATLAB and Fig. 6.5(a) shows the voltage controller action with a step change in the reference. Similarly Fig. 6.5(b) shows the controller action with a step change in the battey power reference. Fig. 6.6 finally shows the voltage controller performance, when the power is following a step change in reference. It clearly shows that the voltage remains nicely regulated during this mode. A complete mimic of the multi port converter system was realized using a variable current source at the load port. If the battery power reference and the output voltage reference do not change, both of them remains regulated under variable



(a) voltage compensator action under step change (b) Power compensator action under step change

FIGURE 6.5: Compensator performances under step change in reference

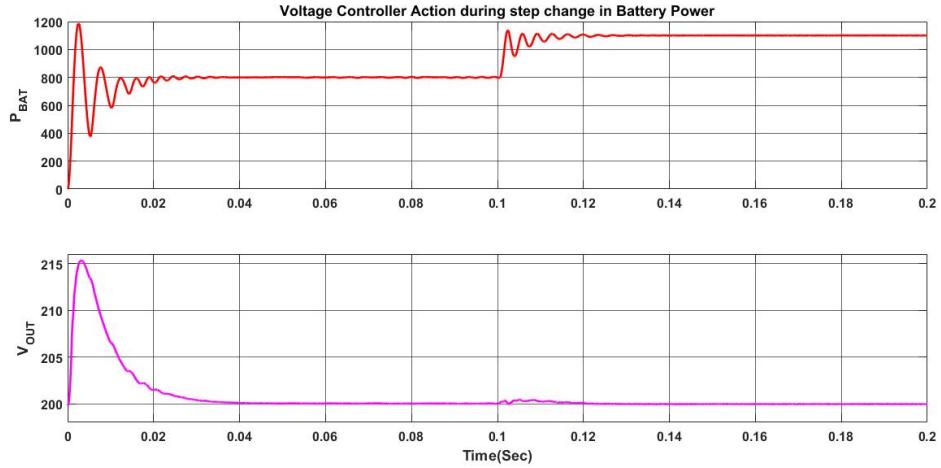


FIGURE 6.6: Voltage controller during change in power reference

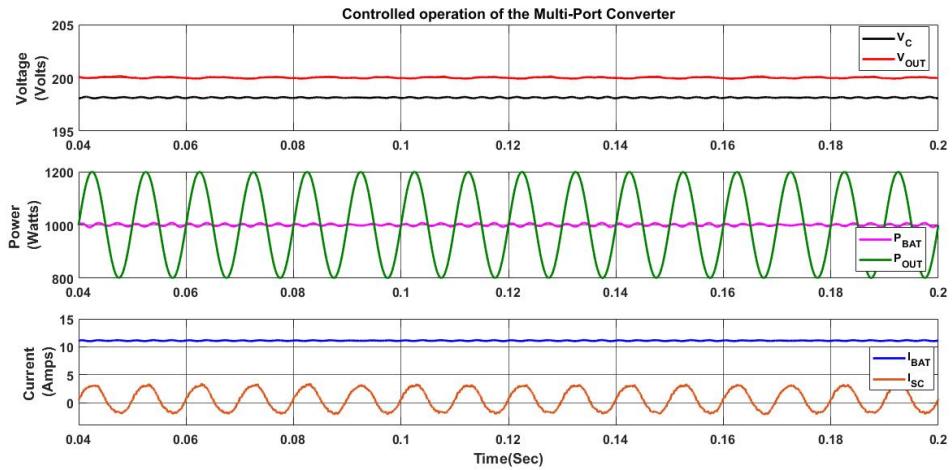


FIGURE 6.7: Simulated result of a functional MPC

load demand. The ripple power gets processed through the supercapacitor. Fig. 6.7 summarizes the simulation results.

6.3 Discrete time controller realization & ADC-DAC interfacing:

The controllers specified in Eq. 6.3 are realized using the Nexys 2 FPGA board in digital domain. The discrete time controller architecture shown in Fig. 6.8 is followed to realize both the lead-lag compensator and the P-I compensator. Digilent make 4 AD-1 modules (2 channel, 12 bits) were used as ADCs to digitize the sensed signals. To corroborate the ADC conversion, Digilent make 8 channel DA 4 DAC was used. All the modules were coded using Xilinx, with a sampling interval of $2.72 \mu\text{S}$. Fig. 6.9 shows the simultaneous

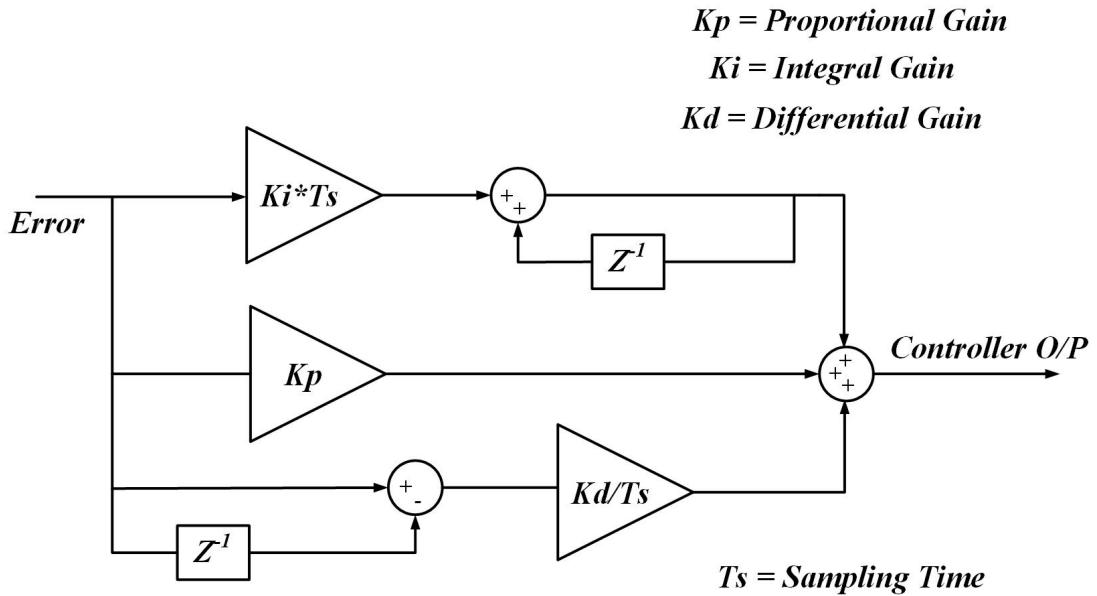


FIGURE 6.8: Discrete time P-I-D controller architecture

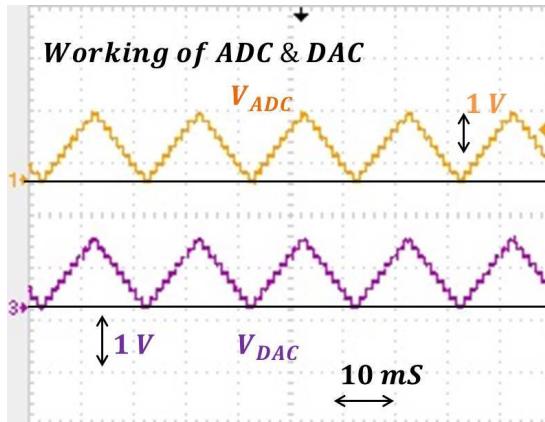


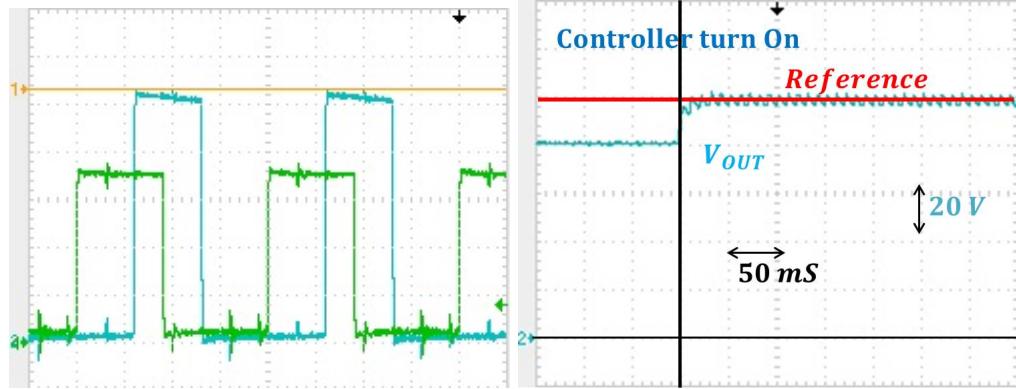
FIGURE 6.9: ADC-DAC Interfacing

waveforms from the i/p of ADC and the o/p of DAC, as they were a perfect match, the discrete time controller was reliable.

6.4 Hardware Results:

In this final section hardware verification of the proposed controllers are illustrated. The voltage mode controller was fully functional in the prototype, although, due to the high ripple content in the i/p current (As DC sources were realized using passive diode bridge rectifiers), the power controller was not implemented in hardware.

Fig. 6.10 shows the controlled operation of the MPC under a reference o/p voltage of 100 volts. Fig. 6.10(a) shows the switch node voltages under controlled operation.



(a) Switch node voltages (soft transitions) under controller action
(b) O/P voltage transition after controller turn ON

FIGURE 6.10: Hardware results of voltage controlled MPC

The o/p voltage matches the reference, while the transitions are smooth, indicating soft switching under controlled operation. Fig. 6.10(b) shows the transient waveform of the o/p voltage when the controller is turned on. One can observe that the settling time is sufficiently small in hardware implementation also.

Chapter 7

Conclusion & Future Scope

This chapter concludes the thesis and discusses a few future scopes based on the work done.

7.1 Conclusion

A ‘3+1’ multiport converter topology with bidirectional power flow capabilities is analyzed in detail in this project. Design of the converter for a particular specification is done at first theoretically. Simulation results are obtained for proof of concept and finally a prototype was build. Hardware results for the same are shown in detail. This topology ensures ZVS over wide operating range. Another important feature of the converter is 2 of its ports are current fed in nature. Efficiency results, ZVS boundary, Bi-directional power transfer and other important features were experimentally verified and results are concluded for open loop mode of operation. Further, small-signal modeling of the converter is done and a control strategy is discussed. Simulation results of the proposed control strategy is provided and partial hardware verification is also done in this thesis.

7.2 Future Scope

Some further improvements in the control strategy can still be explored

7.2.1 Control Strategy

The converter needs to be controlled at various modes of operation. The outline of the control strategy can be formulated as:

- If the battery and the supercapacitor voltage is above a particular reference voltage, then the load power will be entirely supplied by the supercapacitor. (In order to maximize efficiency)
- If the supercapacitor voltage falls below the threshold, the battery will be used to charge up the supercapacitor, as well as to supply the load.
- During regeneration, if the supercapacitor and the battery voltage, both are below a threshold value, the battery should be charged up first. (In order to increase the lifetime of the battery)
- If battery voltage is above the threshold, then both the regenerative power coming from load and battery delivered power is used to charge up the capacitor voltage.

Using these control strategies and the sensed signals coming from the power board, either a dual-loop or a cross-regulated controller has to be developed based on the control variables D_{phi} , D_1 & D_2

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