11. Bus lines can be repeated into ___ types
a. One
b. Two
c. Three
d. Four

12. Which of these is not a bus type dictated
a. Dedicated
b. Multiplexed
c. Non dictated
d. None of the above

13. ___ Dedication of buses offers high throughout
a. Functional
b. Physical
c. Both Physical and Function
d. None of the above

14. In physical dedication, there is ___ bus contention
a. High
b. Very high
c. Less
d. Very less

15. Multiplexed is also referred to as ___
a. Dedicated
b. Non- dedicated
c. Non-dictated
d. None of the above

16. The method of using the same bus for multiple purposes is known as ___
a. Frequency division multiplexing
b. Time multiplexing
c. Wave division multiplexing
d. None of the above

17. ALE stands for
a. Address latch enable
b. Address label enables
c. Address line enables
d. None of the above

18. Synchronous timing is
a. Simpler to implement
b. Simples to test

c. is less flexible
d. All of the above

19. What is the main cause of performance suffering in the device connected to the bus
a. The more devices attached to the bus, the greater is the bus length
b. The bus may become a bottleneck as the aggregate data transfer demand approaches the capacity of the bus
c. Both a& b
d. None of the above

20. MAB stands for
a. Memory address buffer
b. Memory address bus
c. Memory address batch
d. None of the above

21. DMA stands for
a. Direct memory access
b. Dedicated memory access
c. Direct managed access
d. None of the above

22. PPU stands for
a. Point to point unit
b. Peripheral Processor unit
c. Processors peripheral unit
d. Powered processor unit

23. ISA stands for
a. International standard Association
b. Industry-standard association
c. Industry-standard architecture
d. International standard architecture

24. Source and Result operands can be in
a. Main memory
b. CPU register
c. I/O device
d. All of the above

25. Each instruction is represented by a sequence of ___
a. Bits
b. Bytes
c. Words
d. Nibble

26. The ___ are written in symbolic represented of machine code using English like language called
a. Mini micros, Instructions
b. Instructions, Mnemonics
c. Program, Mnemonics
d. None of the above

27. Virtually all arithmetic and logic operations are
a. Unary
b. Binary
c. Either unary or Binary
d. Neither unary nor binary

28. ASCII stands for
a. Added source code to Instruction Index
b. American standard code for information and interchange
c. Argued standard code for information and Interrelate
d. None of the above

29. The general category of data is
a. Addresses,
b. Numbers
c. Characters
d. Logical data
e. All of the above

30. All machine language in ___ data type
a. Character
b. Logical
c. Numeric
d. Addresses

31. The numbers stored in the computer are___
a. limited
b. Unlimited
c. Zero
d. None of the above

32. Which type of numerical data is used in common computers
a. Integer or fixed point
b. Floating-point
c. Decimal
d. All of the above

33. IRA stands for
a. International Relocation address
b. Instruction Relocation address
c. International Reference alphabet
d. International Reference address

34. ASCIT is represented by ___ pattern
a. 6 bit
b. 7 bits
c. 8 bits
d. 16 bits

35. ASCII encoded characters are usually stored and transferred as ___ per characters
a. 6 bit
b. 7 bits
c. 8 bits
d. 16 bits

36. Signed integers are stored in ___ form
a. 1's complement
b. 2's complement
c. 3's complement
d. 9's complement

37. In VAX data types all data types are in terms of ___
a. bits
b. nibble
c. byte
d. Ward

38. Data transfer must specify
a. The location of the source and destination
b. Length of the data to be transferred
c. Mode of addressing for each operand
d. All of the above

39. Programmers use organizations called ___ to represent the data used in computations
a. Data types
b. Data storage
c. Data Structure
d. Data class

40. The different ways in which the location of an open and is specified in instruction are referred to go ___

a. Addressing mode
b. Instruction format
c. Memory I/O
d. Programmed I/O

41. Main memory stores ___ and ___.
a. Data, instructions
b. Data, address
c. Address, instructions
d. None of the above

42. I. For internal memory, the unit of transfer is equal to the number of data lines into and out of the memory module.
a. I is true
b. II is true
c. Both I and II True
d. Both are false

43. I. In volatile memory, Information once recorded remains without deterioration until deliberately changed.
II. In non-volatile memory, information decays naturally or is lost when electrical power is switched of.
a. I is true
b. II is true
c. Both are true
d. Both are false

44. How many transistors and capacitors does a DRAM cell need? SRAM cell?
a. DRAM: 0 Capacitor and 6 Transistor and SRAM: 1 Capacitor and 0 Transistors
b. DRAM: 1 Capacitor and 0 Transistor and SRAM: 6 Capacitors and 1 Transistor
c. DRAM: 1 Capacitor and 1 Transistor and SRAM: 0 Capacitors and 6 Transistors
d. DRAM: 0 Capacitor and 1 Transistor and SRAM: 1 Capacitor and 6 Transistors

45. Arrange the following in sequence the CPU must perform If one or both operands are in memory
A Determine whether the addressed item is in cache
B. Calculate the memory address based on the address mode
C. If not the issue command to the memory module
D. If the address refers to virtual memory, Translate from virtual to the actual memory address
a. A, B, C, D
b. D, B, C, A
c. B, C, D, A
d. B, D, A, C

46. Arrange in sequence operations performed by CPU.
A. I/o module transfers data from to CPU.
B I/o module gets data from the device
C. CPU ready, CPU requests data transfer
D. If ready, CPU requests data transfer
E. I/o module returns device status
a. A, B, C, D, E
b. E, D, C, B, A
c. C, E, D, A, B
d. B, C, D, A, B

47. Arrange in increasing order actions that take place with programmed I/o.
A) CPU may wait or come back
B) I/o module does not interrupt CPU
C) I/o module does not inform CPU directly
D) CPU checks status bits periodically
E) I/o module sets status bits
F) I/o module performs the operation
G) CPU requests I/o operation
a. G, F, E, D, C, B, A
b. A, B, C, D, E, F, G
c. B, C, E, D, A, F, G
d. D, A, B, C, F, G, E

48. Arrange the following in increasing order-
A. A memory read the control signal on the control bus.
B. Control signals to logic that adds 1 to the contents of the PC and stores the result back in the PC>
C. A control signal that opens the gate allowing the contents of the MAR on to the address bus.
D. A control signal that opens gates allowing the contents of the data bus to be stored in the MBR.
a. A, B, C, D
b. B. C. D. A
c. D, C, B, A
d. C, A, D, B

49. Arrange the following in increasing order-
A. Store a word of data from a CPU register in a given memory location.
B. Perform an arithmetic or logic operation and store the result in a CPU register.
C. Fetch the content of a given memory location and load them into a CPU register.
D. Transfer a word of data from one CPU register to ALU or another CPU register.
a. C, A, D, B
b. B, C, D, A

c. A, B, C, D
d. B, A, C, D

50. I. A signal applied to the word line by the address decoder selects the cell either for Read or Write operation.
II. Bit lines are used to transfer stored data and its complement between the cell and data drivers.
a. I is true
b. II is true
c. Both are true
d. Both are false

51. Let tc, h, and tm represent the cache access time, hit ratio, and the main memory access time respectively, Then the average access time can be determined by the eqn.
a. t = htc + (1-h) (tc+tm)
b. t = htc + h (tc+tm)
c. t = htc + (1+h) (tc+tm)
d. None of the above

52. Expression for the efficiency of a system that uses a cache can be delivered as :
a. = 1/[r(1-h)]
b. = 1/[1+r(1-h)]
c. = 1/[1-r(1-h)]
d. = 1/(1+1-h)

53. Peripheral often use different ___ and ___ than the computer system to which they're attached.
a. Data format, word length
b. Memory, size
c. Data format, memory
d. None of the above

54. Which statements are invalid in the case of RAID.
a. RAID is a set of physical disk drives viewed by the operating system as a single logical drive.
b. Data are distributed across the physical drives of an array.
c. Redundant disk capacity is used to store parity information, which guaranties data recoverability in case of a disk failure.
d. All are valid

55. Match the following
1. Direct addressing mode I. The effective address of the operand is the contents of a register specified the instrument
2. Indirect addressing mode II The effective address of the operand is generated by adding a constant value to the contents of a register

3. Index mode III. The effective address of the operand is the contents of the register or memory location whose address appears in the instructions
4. Autoincrement mode IV. The operand is the given memory location

a. 1:I, 2:II, 3:III, 4:IV
b. 1:IV, 2:III, 3:II, 4:I
c. 1:IV, 2:II, 3:III, 4:I
d. 1:II, 2:III, 3:I, 4:IV

56. Match the following :
A. Sequential I. Any location can be selected at random and directly accessed and addressed.
B. Direct II. Word is retrieved based on a portion of its contents rather than its address
C. Random III. Access is accomplished by direct access to reach a General vicinity, plus sequential searching, counting or Waiting to reach the final location.
D. Associative IV. Data is accessed sequentially, the records may be passed until the record that is searched is found.

a. A: IV, B:II. C:III, D:I
b. A: IV, B:III, C:II, D:I
c. A: IV, B:III, C:I, D:II
d. A: I, B:II, C:III, D:IV

57. Match the following :
A. Semiconductor I. Hard disks, Tape units
B. Magnetic II. Main Memory, Cache, RAM, ROM
C. Optical III. The optical laser is used.
D. Magneto-optical IV. CD-ROM, CD-RW

a. A:II, B:I, C:III, D:IV
b. A:II, B:I, C:IV, D:III
c. A:I, B:III, C:II, D:IV
d. A:IV, B:III, C:II, D:I

58. Match the following related to the Memory hierarchy.
A. Faster access time I. Greater capacity
B. Greater capacity II. Greater cost per bit
C. Slower access time III. Smaller cost per bit

a. A:I, B:II, C:III
b. C:I, B:II, A:III
c. A:II, B:III, C:I
d: A:III, B:I, C:II

59. Match the following:
A. PROM I. It can be programmed multiple times. The whole capacity needs to be erased by ultraviolet radiation before new programming activity. It cannot be partially programmed.
B. EPROM II. It is erased and programmed electrically. It can be partially Programmed.
C. EEPROM III. It can only be programmed once after its fabrication.

a. A:III, B:I, C:II
b. A:I, B:II, C:III
c. A:III, B:II, C:I
d. A:II, B:III, C:I

60. Match the following data rate of various devices.
A. Keyboard I. 100 bytes/sec
B. Mouse II. 7 KB/sec
C. USB III. 1.5 MB/sec
D. 56 Modem IV. 10 bytes/sec
a. A:IV, B:I, C:III, D:II
b. A:I, B:II, C:III, D:IV
c. A:III, B:I, C:IV, D:I
d. A:IV, B:III, C:II, D:I