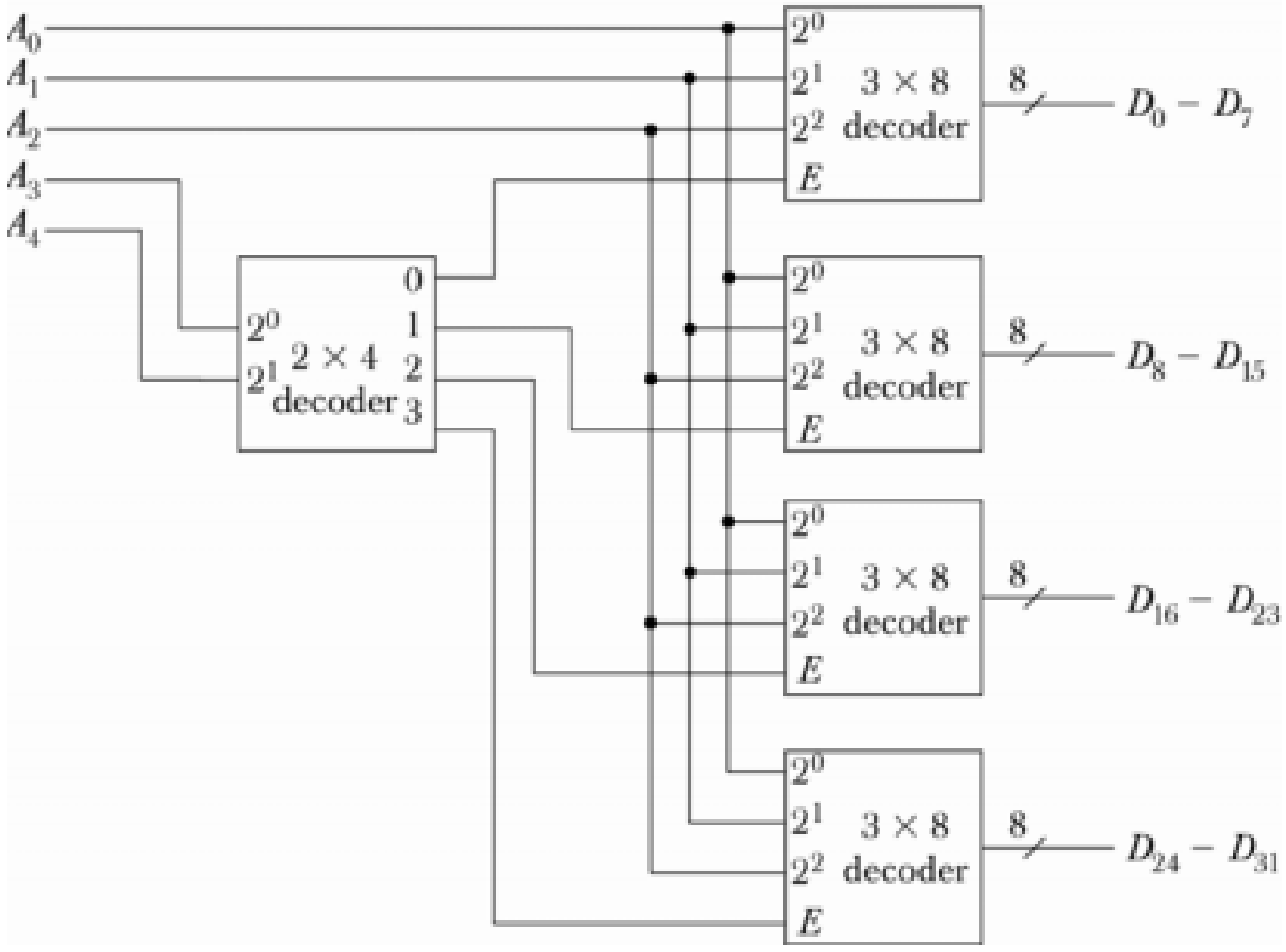
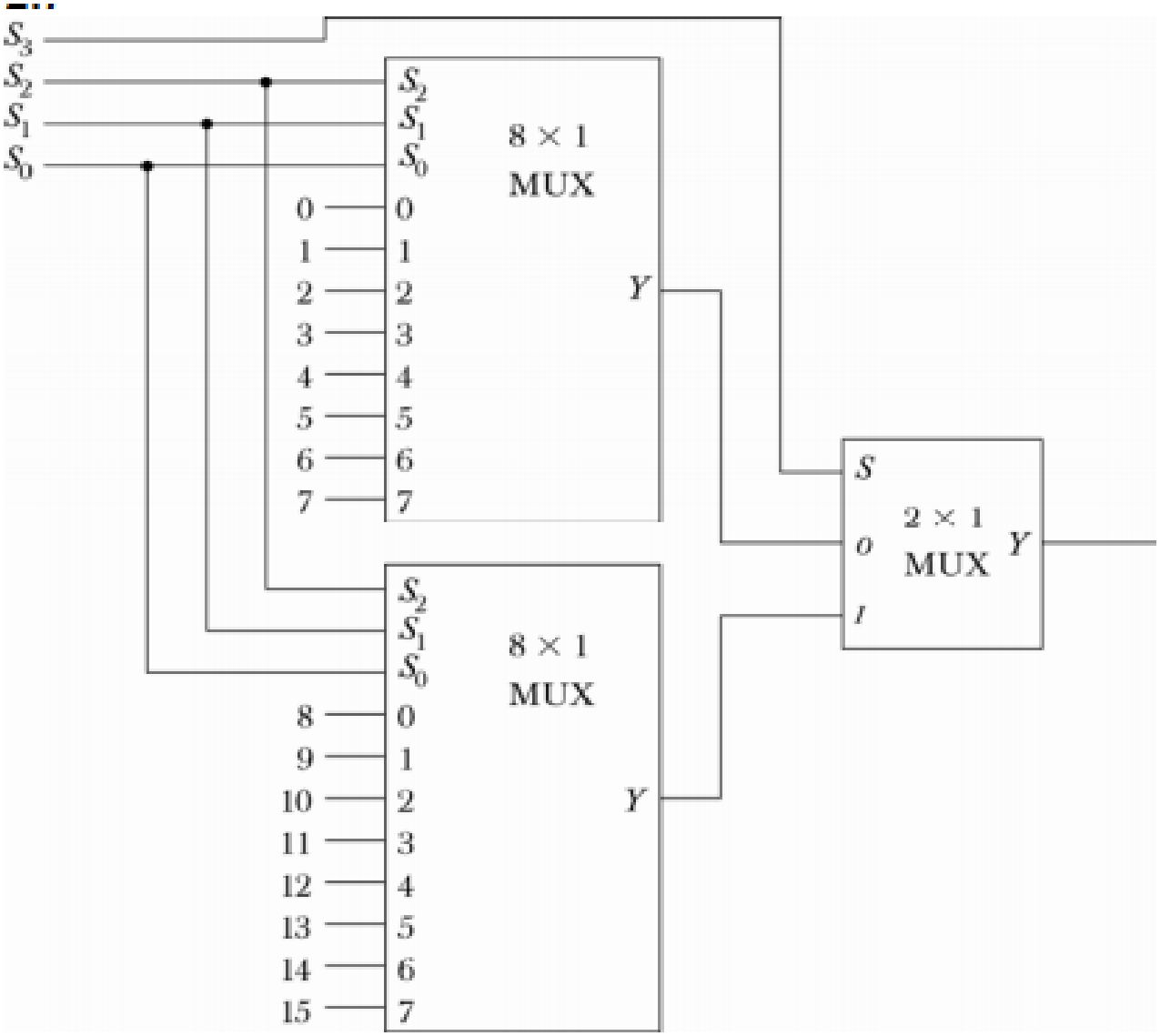
Practice Questions

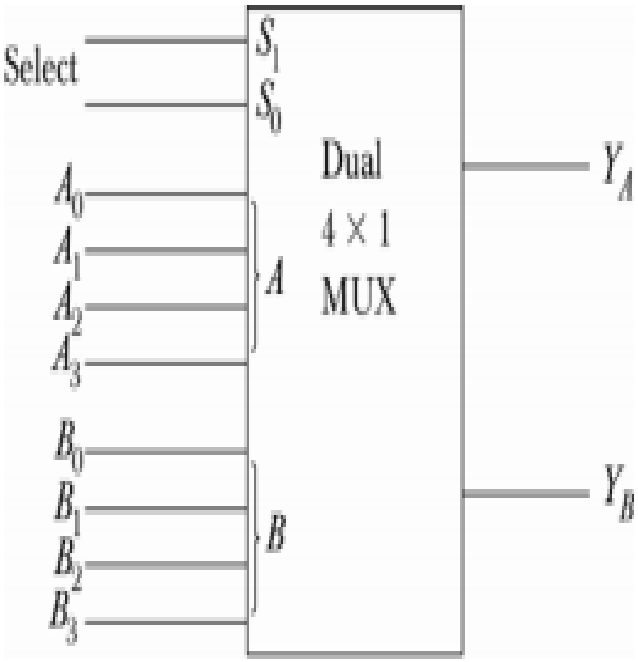
1. Construct a 5-to-32 line decoder with four 3-to-8 line decoders with enable and 2-to-4 line decoder.


A_0
A_1
A_2
A_3
A_4
2^0
2^1
2 × 4
decoder
0
1
2
3
2^0
2^1
2^2
E
3 × 8
decoder
8
$D_0 - D_7$
$D_8 - D_{15}$
$D_{16} - D_{23}$
$D_{24} - D_{31}$

2. Construct a 16-to-1 line multiplexer with two 8-to-1 line multiplexers and one 2-to-1 line multiplexer. Use block diagram for the three multiplexers.


S_3
S_2
S_1
S_0
S_2
S_1
S_0
8 × 1
MUX
0
1
2
3
4
5
6
7
0
1
2
3
4
5
6
7
Y
S
0
1
2 × 1
MUX
Y
S_2
S_1
S_0
8 × 1
MUX
8
9
10
11
12
13
14
15
0
1
2
3
4
5
6
7
Y

3. Draw the block diagram of a dual 4-to-1 line multiplexers and explain its operation by means of a function table.

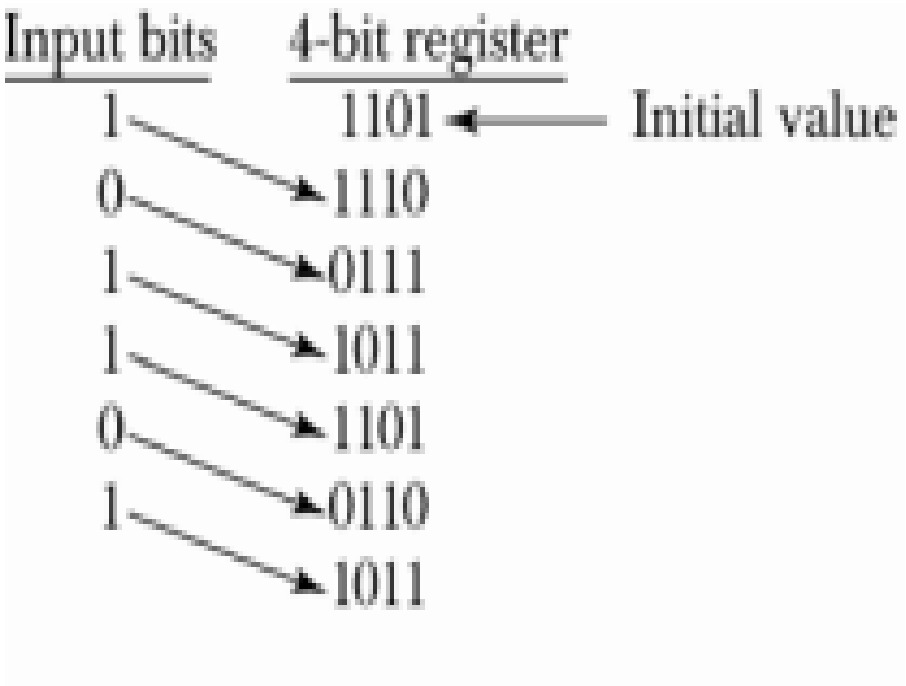


S_1S_0	Y_A Y_B
0 0	A_0 B_0
0 1	A_1 B_1
1 0	A_2 B_2
1 1	A_3 B_3

Function table

4. What is the purpose of buffer gate in the clock input of the register.

5. The content of a 4-bit register is initially 1101.The register is shifted six times to the right with the serial input being 101101. What is the content of the register after each shift.


Input bits
4-bit register
1
1101
Initial value
0
1110
1
0111
1
1011
0
1101
1
0110
1011