

DRONACHARYA

College of Engineering

Computer Architecture & Organization MCQ Questions:-

SEMESTER –IV

SUBJECT CODE- CSE-210 F

Branch-CSE/IT/CSIT/ECS

1. In a J-K Flip Flop the function $K=J'$ is used to realize

- ☒ A T-Flip-Flop
- ☐ B S-R Flip-Flop
- ☐ C D-Flip-Flop
- ☐ D M/S J-K Flip-Flop

2. Logic families of IC having dense packing density, simpler processing techniques and more economic operations are :

- ☐ A TTL
- ☐ B ECL
- ☒ C CMOS
- ☐ D None of the above

3. Using an additional NOT gate, a JK flip-flop can be converted into

- ☐ A T flip-flop
- ☐ B RS flip-flop
- ☒ C Master Slave flip-flop
- ☐ D D flip-flop

4. Which of the following logic families is well suited for high speed operations ?

- ☐ A TTL
- ☒ B ECL
- ☐ C MOS
- ☐ D CMOS

5. A Toggle Flip-Flop can be constructed using a J-K Flip-Flop by connecting the

- ☒ A Toggle input to J and inverted form of toggle input to K
- ☐ B The toggle input to J
- ☐ C Inverted form of toggle input to K

D None of the above

6. The half adder performs

A Decimal addition operation for 2 decimal inputs

B Binary addition operation for 2 binary inputs

☒ C Decimal addition operation for 2 binary inputs

D Binary addition operation for 2 decimal inputs

7. Which Logic circuit would you use for addressing memory ?

A Full adder

☒ B Multiplexer

☒ C Decoder

D Direct memory access circuit

8. One of the major difference between a combinational logic circuit such as a decoder and a storage circuit such as an RS latch is that

A The storage circuit requires a different class of gates.

☒ B The storage circuit requires a clock input.

C The storage circuit uses feedback

D The storage circuit has no propagation delay

9. A Flip-Flop circuit can be used for

☒ A Counting

B Scaling

C Rectification

D Demodulation

10. One bit full adder can be designed using

A Two half adders and one OR gate

☒ B Two half adders

C One Ex-OR and two NAND gates

D Two Ex-OR and four NAND gates

11. Which of the following shift operations divide a signed binary number by 2 ?

A Logical left shift

☒ Logical right shift

☐ C Arithmetic left shift

☐ D Arithmetic right shift

12. Normally digital computers are based on

☐ A AND and OR gates

☒ B NAND and NOR gates

☐ C NOT gate

☐ D None of the above

13. BCD stands for

☐ A Boolean code definition

☐ B Binary coded division

☐ C Binary coded decimal

☐ D None of the above

14. The basic circuit ECL supports the

☐ A NAND logic

☐ B NOR logic

☐ C EX-OR logic

☐ D OR-NOR logic

15. An adder-subtractor single unit can be designed using full adder and

☐ A OR gates

☐ B XOR gates

☒ C NOR gates

☐ D NAND gates

16. In register addressing mode operands are looked at

☐ A In cache

☐ B In secondary storage

☒ C In CPU

☐ D In primary memory

17. What can be used to store one or more bits of data, which can accept and/or transfer information serially ?

☐ A Parallel registers

☒ B Shift registers

C Counters

D None of these

18. The example of implied addressing is

☒ A Stack addressing

B Immediate addressing

C Indirect addressing

D None of the above

19. In the indirect address mode

A the effective address is equal to the address part of the instruction

☒ B the content of the program counter is added to address part of the instruction

C a memory is addressed by a register

D address in the instruction points to location of the effective address.

20. In an instruction the address part points to the address of actual data. The addressing mode is

A immediate addressing

☒ B direct addressing

C indirect addressing

D none of these

21 What is the minimal form of the Karnaugh map shown below? Assume that X denotes a don't care term.

gatecs2012Kmap

cd \ ab	00	01	11	10
00	1	x	x	1
01	x			1
11				
10	1			x

A $b'd'$

$$B b'd' + b'c'$$

$$C b'd' + a'b'c'd'$$

$$D b'd' + b'c' + c'd'$$

22. What is the minimal form of the Karnaugh map shown below? Assume that X denotes a don't care term.

cd \ ab	00	01	11	10
00	1	X	X	1
01	X			1
11				
10	1			X

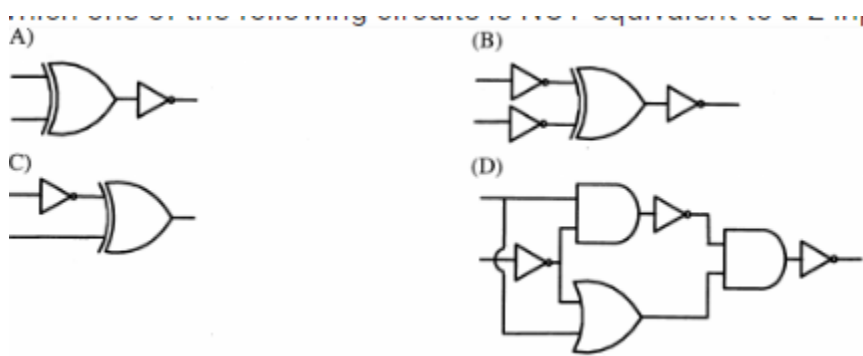
$$A b'd'$$

$$B b'd' + b'c'$$

$$C b'd' + a'b'c'd'$$

$$D b'd' + b'c' + c'd'$$

23. Which one of the following circuits is NOT equivalent to a 2-input XNOR (exclusive NOR) gate?



A A

B B

C C

D D

24. The simplified SOP (Sum Of Product) form of the boolean expression $(P + Q' + R') \cdot (P + Q' + R) \cdot (P + Q + R')$ is

A $(P' \cdot Q + R')$

B $(P + Q' \cdot R')$

C $(P' \cdot Q + R)$

D $(P \cdot Q + R)$

25. Consider the data given in previous question. If all the flip-flops were reset to 0 at power on, what is the total number of distinct outputs (states) represented by PQR generated by the counter?

A 3

B 4

C 5

D 6

26. The minterm expansion of $f(P, Q, R) = PQ + QR' + PR'$ is

A $m_2 + m_4 + m_6 + m_7$

B $m_0 + m_1 + m_3 + m_5$

C $m_0 + m_1 + m_6 + m_7$

D $m_2 + m_3 + m_4 + m_5$

27. In a k-way set associative cache, the cache is divided into v sets, each of which consists of k lines. The lines of a set are placed in sequence one after another. The lines in set s are sequenced before the lines in set (s+1). The main memory blocks are numbered 0 onwards. The main memory block numbered j must be mapped to any one of the cache lines from.

A $(j \bmod v) * k$ to $(j \bmod v) * k + (k-1)$

B $(j \bmod v)$ to $(j \bmod v) + (k-1)$

C $(j \bmod k)$ to $(j \bmod k) + (v-1)$

D $(j \bmod k) * v$ to $(j \bmod k) * v + (v-1)$

28. Consider the following sequence of micro-operations.

$MBR \leftarrow PC$

$MAR \leftarrow X$

$PC \leftarrow Y$

$Memory \leftarrow MBR$

29. Consider an instruction pipeline with five stages without any branch prediction: Fetch Instruction (FI), Decode Instruction (DI), Fetch Operand (FO), Execute Instruction (EI) and Write Operand (WO). The stage delays for FI, DI, FO, EI and WO are 5 ns, 7 ns, 10 ns, 8 ns and 6 ns, respectively. There are intermediate storage buffers after each stage and the delay of each buffer is 1 ns. A program consisting of 12 instructions I1, I2, I3, ..., I12 is executed in this pipelined processor. Instruction I4 is the only branch instruction and its branch target is I9. If the branch is taken during the execution of this program, the time (in ns) needed to complete the program is

- A 132
- B 165
- C 176
- D 328

30. The following code segment is executed on a processor which allows only register operands in its instructions. Each instruction can have at most two source operands and one destination operand. Assume that all variables are dead after this code segment.

```
c = a + b;
d = c * a;
e = c + a;
x = c * c;
if (x > a) {
    y = a * a;
}
else {
    d = d * d;
    e = e * e;
}
```

31. Suppose the instruction set architecture of the processor has only two registers. The only allowed compiler optimization is code motion, which moves statements from one place to another while preserving correctness. What is the minimum number of spills to memory in the compiled code?

- A 0
- B 1
- C 2
- D 3

31. Consider the same data as above question. What is the minimum number of registers needed in the instruction set architecture of the processor to compile this code segment without any spill to memory? Do not apply any optimization other than optimizing register allocation.

- A 3

B 4

C 5

D 6

32. The amount of ROM needed to implement a 4 bit multiplier is

A 64 bits

B 128 bits

C 1 Kbits

D 2 Kbits

33. Register renaming is done in pipelined processors

A as an alternative to register allocation at compile time

B for efficient access to function parameters and local variables

C to handle certain kinds of hazards

D as part of address translation

34. A computer has a 256 KByte, 4-way set associative, write back data cache with block size of 32 Bytes. The processor sends 32 bit addresses to the cache controller. Each cache tag directory entry contains, in addition to address tag, 2 valid bits, 1 modified bit and 1 replacement bit. The number of bits in the tag field of an address is

A 11

B 14

C 16

D 27

35. Consider the data given in previous question. The size of the cache tag directory is

A 160 Kbits

B 136 bits

C 40 Kbits

D 32 bits

36. Consider an instruction pipeline with four stages (S1, S2, S3 and S4) each with combinational circuit only. The pipeline registers are required between each stage and at the end of the last stage. Delays for the stages and for the pipeline registers. What is the approximate speed up of the pipeline in steady state under ideal conditions when compared to the corresponding non-pipeline implementation?

A 4.0

B 2.5

C 1.1

D 3.0

37. An 8KB direct-mapped write-back cache is organized as multiple blocks, each of size 32-bytes. The processor generates 32-bit addresses. The cache controller maintains the tag information for each cache block comprising of the following. 1 Valid bit 1 Modified bit As many bits as the minimum needed to identify the memory block mapped in the cache. What is the total size of memory needed at the cache controller to store meta-data (tags) for the cache?

A 4864 bits

B 6144 bits

C 6656 bits

D 5376 bits

38. A main memory unit with a capacity of 4 megabytes is built using $1M \times 1$ -bit DRAM chips. Each DRAM chip has 1K rows of cells with 1K cells in each row. The time taken for a single refresh operation is 100 nanoseconds. The time required to perform one refresh operation on all the cells in the memory unit is

A 100 nanoseconds

B 100×210 nanoseconds

C 100×220 nanoseconds

D 3200×220 nanoseconds

39. A 5-stage pipelined processor has Instruction Fetch(IF), Instruction Decode(ID), Operand Fetch(OF), Perform Operation(PO) and Write Operand(WO) stages. The IF, ID, OF and WO stages take 1 clock cycle each for any instruction. The PO stage takes 1 clock cycle for ADD and SUB instructions, 3 clock cycles for MUL instruction, and 6 clock cycles for DIV instruction respectively. Operand forwarding is used in the pipeline. What is the number of clock cycles needed to execute the following sequence of instructions?

Instruction	Meaning of instruction
-------------	------------------------

I0 : MUL R2 ,R0 ,R1	$R2 \leftarrow R0 * R1$
---------------------	-------------------------

I1 : DIV R5 ,R3 ,R4	$R5 \leftarrow R3 / R4$
---------------------	-------------------------

I2 : ADD R2 ,R5 ,R2	$R2 \leftarrow R5 + R2$
---------------------	-------------------------

I3 : SUB R5 ,R2 ,R6	$R5 \leftarrow R2 - R6$
---------------------	-------------------------

A 13

B 15

C 17

D 19

40. The program below uses six temporary variables a, b, c, d, e, f.

```

a = 1
b = 10
c = 20
d = a+b
e = c+d
f = c+e
b = c+e
e = b+f
d = 5+e
return d+f

```

Assuming that all operations take their operands from registers, what is the minimum number of registers needed to execute this program without spilling?

- A 2
- B 3
- C 4
- D 6

41. A computer system has an L1 cache, an L2 cache, and a main memory unit connected as shown below. The block size in L1 cache is 4 words. The block size in L2 cache is 16 words. The memory access times are 2 nanoseconds, 20 nanoseconds and 200 nanoseconds for L1 cache, L2 cache and main memory unit respectively. CSE_201048 When there is a miss in L1 cache and a hit in L2 cache, a block is transferred from L2 cache to L1 cache. What is the time taken for this transfer?

- A 2 nanoseconds
- B 20 nanoseconds
- C 22 nanoseconds
- D 88 nanoseconds

42. Consider the data from above question. When there is a miss in both L1 cache and L2 cache, first a block is transferred from main memory to L2 cache, and then a block is transferred from L2 cache to L1 cache. What is the total time taken for these transfers?

- A 222 nanoseconds
- B 888 nanoseconds
- C 902 nanoseconds
- D 968 nanoseconds

43. Which of the following addressing modes are suitable for program relocation at run time ?

- (i) Absolute addressing
- (ii) Based addressing
- (iii) Relative addressing
- (iv) Indirect addressing

☒ (i) and (iv)

B (i) and (ii)

C (ii) and (iii)

D (i), (ii) and (iv)

44. Direction for questions 63 to 64: Consider the following program segment for a hypothetical CPU having three user registers R1, R2 and R3.

Instruction	Operation	Instruction Size(in words)
MOV R1,5000;	R1 \leftarrow Memory[5000]	2
MOV R2, (R1);	R2 \leftarrow Memory[(R1)]	1
ADD R2, R3;	R2 \leftarrow R2 + R3	1
MOV 6000, R2;	Memory [6000] \leftarrow R2	2
HALT	Machine halts	1

Consider that the memory is byte addressable with size 32 bits, and the program has been loaded starting from memory location 1000 (decimal). If an interrupt occurs while the CPU has been halted after executing the HALT instruction, the return address (in decimal) saved in the stack will be

A 1007

B 1020

☒ C 1024

D 1028

45. Consider the following program segment for a hypothetical CPU having three user registers R1, R2 and R3.

Instruction	Operation	Instruction Size(in words)
MOV R1,5000;	R1 \leftarrow Memory[5000]	2
MOV R2, (R1);	R2 \leftarrow Memory[(R1)]	1
ADD R2, R3;	R2 \leftarrow R2 + R3	1
MOV 6000, R2;	Memory [6000] \leftarrow R2	2
HALT	Machine halts	1

Let the clock cycles required for various operations be as follows: Register to/ from memory transfer: 3 clock cycles ADD with both operands in register : 1 clock cycle Instruction fetch and decode : 2 clock cycles per word The total number of clock cycles required to execute the program is

A 29

B 24

C 23

D 20

46. The microinstructions stored in the control memory of a processor have a width of 26 bits. Each microinstruction is divided into three fields: a micro-operation field of 13 bits, a next address field (X), and a MUX select field (Y). There are 8 status bits in the inputs of the MUX. GATECS2004Q65 How many bits are there in the X and Y fields, and what is the size of the control memory in number of words?

A 10, 3, 1024

B 8, 5, 256

C 5, 8, 2048

D 10, 3, 512

47 Consider the following assembly language program for a hypothetical processor. A, B, and C are 8 bit registers. The meanings of various instructions are shown as comments.

MOV B, # 0 ; $B \leftarrow 0$

MOV C, # 8 ; $C \leftarrow 8$

Z : CMP C, # 0 ; compare C with 0

JZX ; jump to X if zero flag is set

SUB C, # 1 ; $C \leftarrow C - 1$

RRC A, # 1 ; right rotate A through carry by one bit. Thus:
; if the initial values of A and the carry flag are $a_7 \dots a_0$ and
; c_0 respectively, their values after the execution of this
; instruction will be $c_0 a_7 \dots a_1$ and a_0 respectively.

JC Y ; jump to Y if carry flag is set

JMP Z ; jump to Z

Y : ADD B, # 1 ; $B \leftarrow B + 1$

JMP Z ; jump to Z

X : Which of the following instructions when inserted at location X will ensure that the value of register A after program execution is the same as its initial value ?

A the number of 0 bits in A0

B the number of 1 bits in A0

C A0

D 8

48. Consider the following assembly language program for a hypothetical processor. A, B, and C are 8 bit registers. The meanings of various instructions are shown as comments.

```
MOV B, # 0      ;      B ← 0
MOV C, # 8      ;      C ← 8
Z :CMP C, # 0    ;      compare C with 0
JZX             ;      jump to X if zero flag is set
SUB C, # 1      ;      C ← C - 1
RRC A, # 1      ;      right rotate A through carry by one bit. Thus:
                ;      if the initial values of A and the carry flag are a7...a0 and
                ;      c0 respectively, their values after the execution of this
                ;      instruction will be c0a7...a1 and a0 respectively.
JC Y           ;      jump to Y if carry flag is set
JMP Z          ;      jump to Z
Y :ADD B, # 1    ;      B ← B + 1
JMP Z          ;      jump to Z
```

X :Which of the following instructions when inserted at location X will ensure that the value of register A after program execution is the same as its initial value ?

- A RRC A, #
- B NOP ; no operation
- C LRC A, # 1 ; left rotate A through carry flag by one bit
- D ADD A, # 1

49 A device employing INTR line for device interrupt puts the CALL instruction on the data bus while

- A) Active
- B) HOLD is active
- C) READY is active
- D) None of these

- A A
- B B
- C C
- D D

50. In 8085, which of the following modifies the program counter ?

- A Only PCHL instruction
- B Only ADD instructions

C Only JMP and CALL instructions

D All instructions