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Tutorial-7

Numerical Example

To show the differences between the various modes, we will show the effect of the addressing modes on the instruction defined in Fig. 8-7. The two-word instruction at address 200 and 201 is a "load to *AC*" instruction with an address field equal to 500. The first word of the instruction specifies the operation code and mode, and the second word specifies the address part. *PC* has the value 200 for fetching this instruction. The content of processor register *R*1 is 400, and the content of an index register *XR* is 100. *AC* receives the operand after the instruction is executed. The figure lists a few pertinent addresses and shows the memory content at each of these addresses.

TABLE 8-4 Tabular List of Numerical Example

Addressing Mode	Effective Address	Content of *AC*
Direct address	500	800
Immediate operand	201	500
Indirect address	800	300
Relative address	702	325
Indexed address	600	900
Register	—	400
Register indirect	400	700
Autoincrement	400	700
Autodecrement	399	450

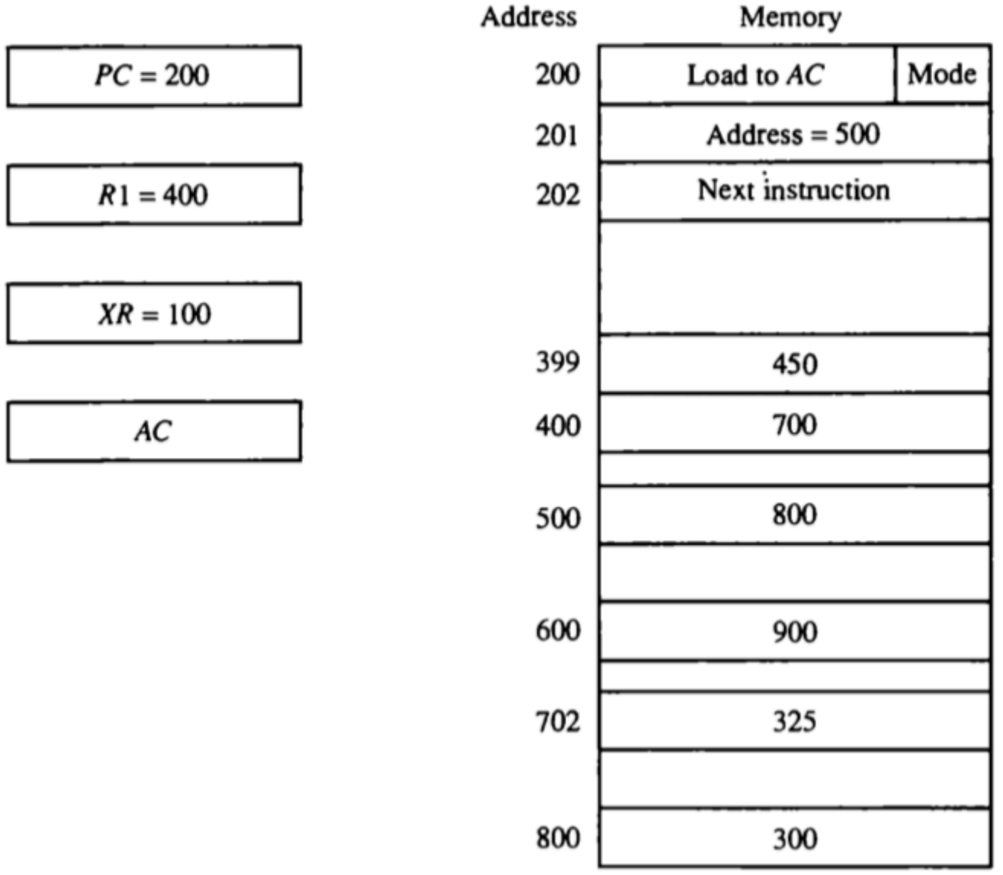


Figure 8-7 Numerical example for addressing modes.

The addressing mode/s, which uses the PC instead of a general purpose register is _____

a) Indexed with offset
b) Relative
c) Direct
d) Both Indexed with offset and direct

Q- A Load instruction is stored at location 200 with its address field value equal to 300. The address field 300 has value 500 and at location 500 operand (a+b) is stored. A processor register R1 contains value 250 which would also act as an Indexed register. Determine Effective Address and operand if possible in each of the following addressing modes .

A- Direct addressing mode
B- Indirect addressing mode
C- Auto-increment addressing mode
D- Auto- decrement addressing mode
E- Register addressing mode
F- Register indirect addressing mode
G- Relative addressing mode
H- Index addressing mode
I- Immediate addressing mode

Content of the program counter is added to the address part of the instruction in order to obtain the effective address is called.

(A) relative address mode.

(B) index addressing mode.

(C) register mode.

(D) Implied mode

Q- An 8-bits register R, determine the values of status bits C,S,Z,V after each of the following instructions . The initial value of register R in each case is hexadecimal 72. The number below are in hexadecimal .

A- ADD immediate operand C6 to R
B- Exclusive OR R with R
C- Subtract immediate operand 9A from R

- The 2s compliment form (Use 6 bit word) of the number 1010 is

- **(A)** 111100.
- **(B)** 110110.
- **(C)** 110111.
- **(D)** 1011.

Consider the two 8 bit numbers A= 01000001 B= 10000100

A-Give the decimal equivalent of each number assuming that

(i)Unsigned

(ii)Signed

B-Add the two binary numbers and interpret the sum assuming that

(i)Unsigned

(ii)Signed

C- Determine the values of C,Z,S,V status bits after the addition.

D- Write all Branch instructions possible

A two-word instruction is stored in memory at an address designated by the symbol W. The address field of the instruction (stored at W + 1) is designated by the symbol Y. The operand used during the execution of the instruction is stored at an address symbolized by Z. An index register contains the value X. State how Z is calculated from the other addresses if the addressing mode of the instruction is

a. direct

b. indirect

c. relative

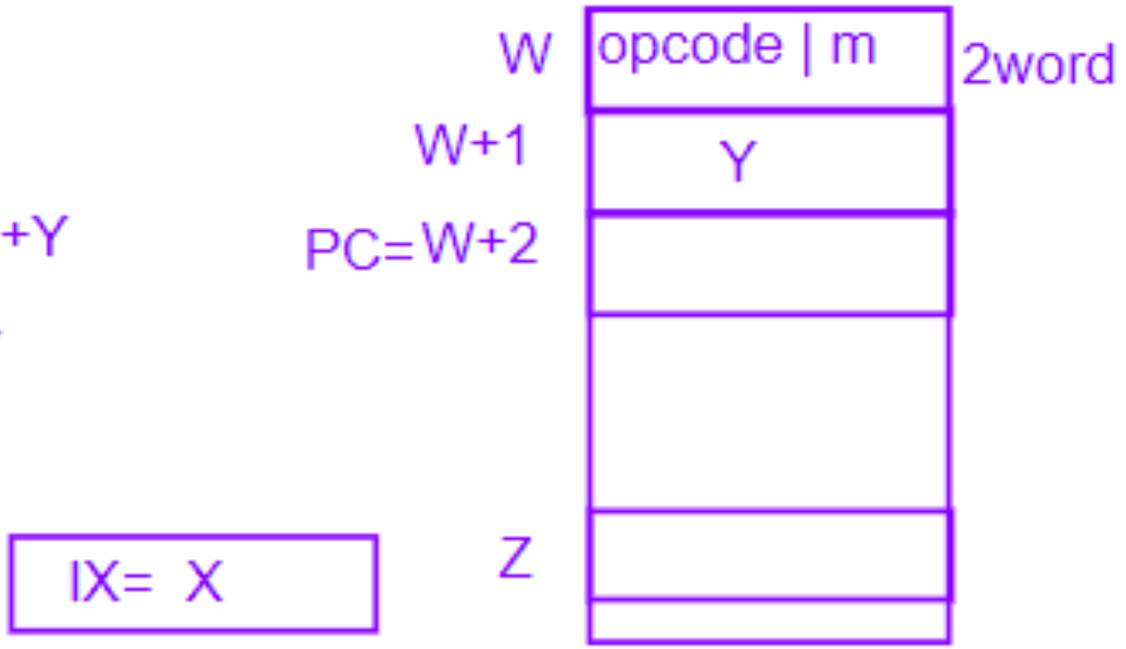
d. indexed

a. direct EA= Y

b. indirect EA= M[Y]

c. relative PC+addr= W+2+Y

d. indexed IX+addr= X+Y



Consider the two 8-bit numbers A=01000001 and B=10000100.

a. Give the decimal equivalent of each number assuming that (1) they are unsigned, and (2) they are signed.

b. Add the two binary numbers and interpret the sum assuming that the numbers are (1) unsigned, and (2) signed.

c. Determine the values of the C, Z, S, and V status bits after the addition.

	Unsigned	Signed
A = 01000001	65	+ 65
B = 10000100	132	– 124
A + B = 11000101	197	– 59

(c) C = 0 Z = 0 S = 1 V = 0

What is the content of Stack Pointer (SP)?

(A)Address of the current instruction

(B) Address of the next instruction

(C) Address of the top element of the stack

(D) Size of the stack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