UNIT-6

Sequential Logic Circuits Applications

Counter:

Asynchronous and Synchronous

What is Counter?

- A counter is a sequential circuit that goes through a prescribed sequence of states upon the application of input pulses.
- It is a cascade combination of multiple flip-flops to which the clock pulse is provided.
- Counters are generally used for the purpose of counting in digital circuits and the total number of counts represent the number of clock pulses arrived.

- Two types of counters:
  - synchronous (clocked /parallel) counters
  - asynchronous (ripple) counters

- Ripple counters allow some flip-flop outputs to be used as a source of clock for other flip-flops.
- Synchronous counters apply the same clock to all flip-flops.

Difference between synchronous and asynchronous

Synchronous	Asynchronous
All flip flips in a synchronous counter are triggered simultaneously by the same clock.	Various flip-flops are activated with different clocks rather than simultaneously in an asynchronous counter.
Operation speed of a synchronous counter is faster as compared to that of an asynchronous counter.	The operation speed of an asynchronous counter is comparatively slower than a synchronous counter
There is no propagation delay observed in case of Synchronous Counters	There is a subsequent propagation delay from one flip-flop to another.
A Synchronous counter can be operated in any desired count sequence, as it could get manipulated by changing the clock sequence.	An Asynchronous counter can operate only in a fixed count sequence, i.e., UP and DOWN
Examples of synchronized counters are Johnson and Ring counters.	Ripple UP counter and Ripple DOWN counter are two instances of asynchronous counters.

MCQ

Asynchronous counters are known as

(A) Ripple counters

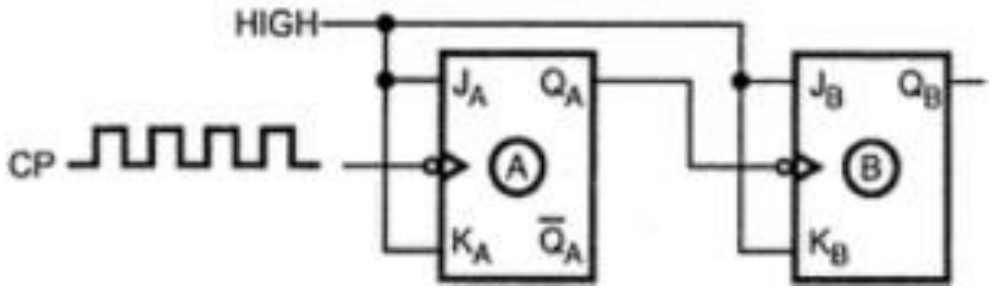
(B) Multiple clock counters

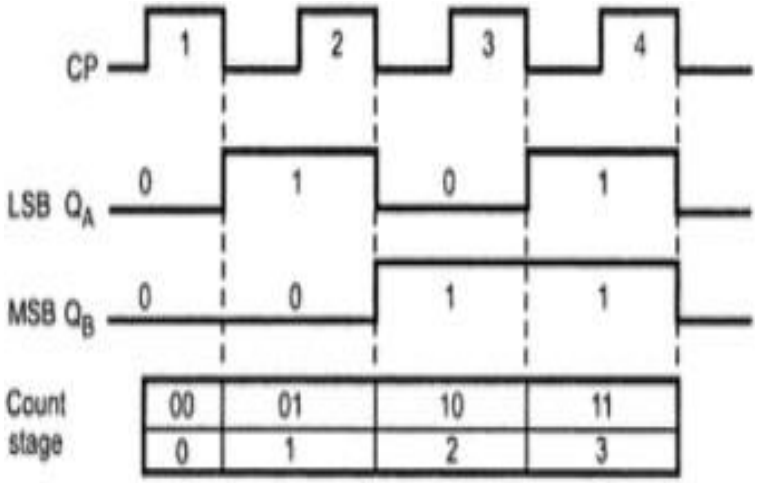
(c) Decade counters

(D) Modulus counter

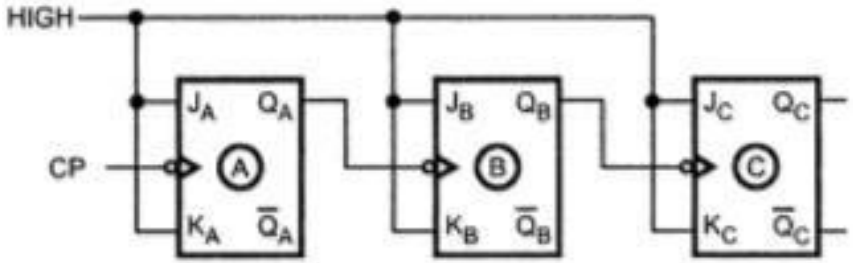
Asynchronous Counter

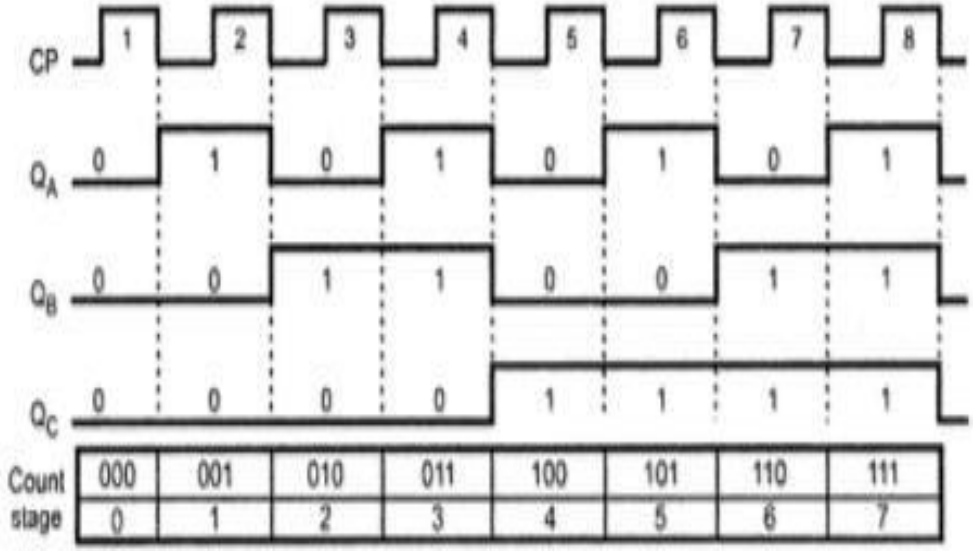
two-bit asynchronous binary counter



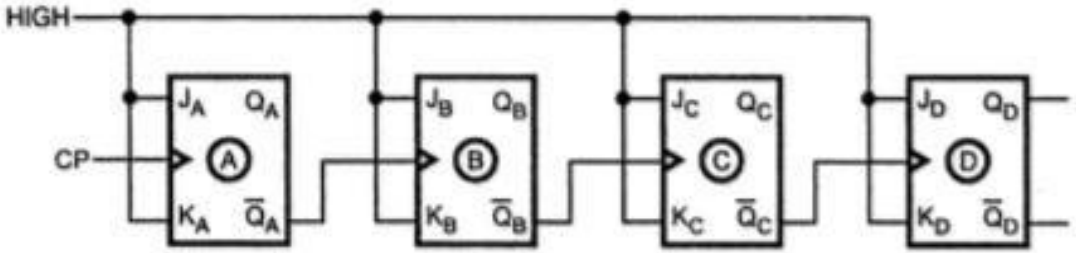


3-bit asynchronous counter





4-stage positive edge triggered ripple counter



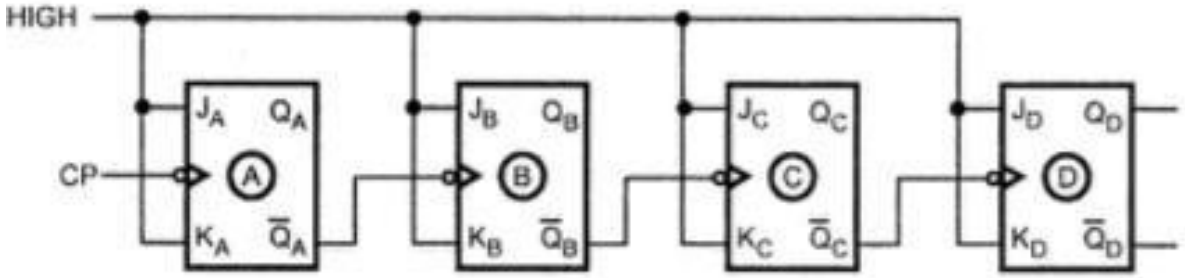
Frequency at output $Q_A = \frac{F_{CLK}}{2}$

Frequency at output $Q_B = \frac{Q_A}{2} = \frac{F_{CLK}}{4}$

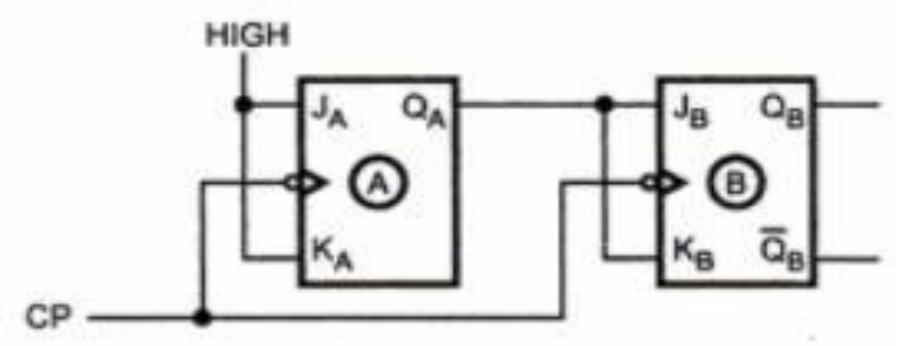
Frequency at output $Q_C = \frac{Q_B}{2} = \frac{Q_A}{4} = \frac{F_{CLK}}{8}$

Frequency at output $Q_D = \frac{Q_C}{2} = \frac{Q_B}{4} = \frac{Q_A}{8} = \frac{F_{CLK}}{16}$

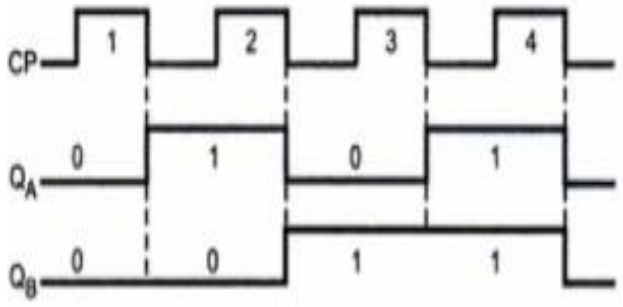
4-bit asynchronous down counter



Synchronous (clocked /parallel) counters

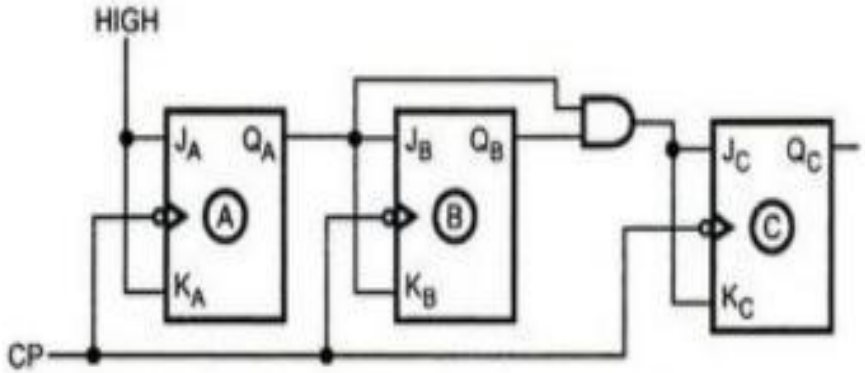


When negative edge of the first clock pulse is applied, flip-flop A will toggle because $J_A = K_A = 1$, whereas flip-flop B output will remain zero because $J_B = K_B = 0$. After first clock pulse $Q_A = 1$ and $Q_B = 0$. At negative going edge of the second clock pulse both flip-flops will toggle because they both have a toggle condition on their J and K inputs ($J_A = K_A = J_B = K_B = 1$). Thus after second clock pulse, $Q_A = 0$ and $Q_B = 1$. At negative going edge of the third clock pulse flip-flop A toggles making $Q_A = 1$, but flip-flop B remains set i.e. $Q_B = 1$. Finally, at the leading edge of the fourth clock pulse both flip-flops toggle as their JK inputs are at logic 1. This results $Q_A = Q_B = 0$ and counter recycled back to its original state. The timing details of

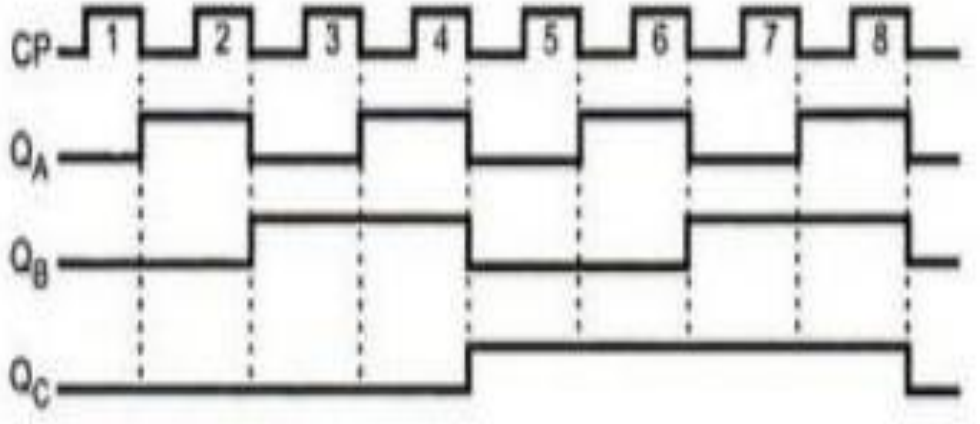


CP	Q_B	Q_A
0	0	0
1	0	1
2	1	0
3	1	1

3-bit Synchronous Binary Up Counter

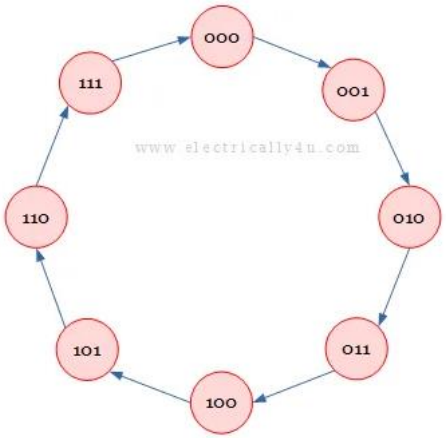


CP	Q_C	Q_B	Q_A
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

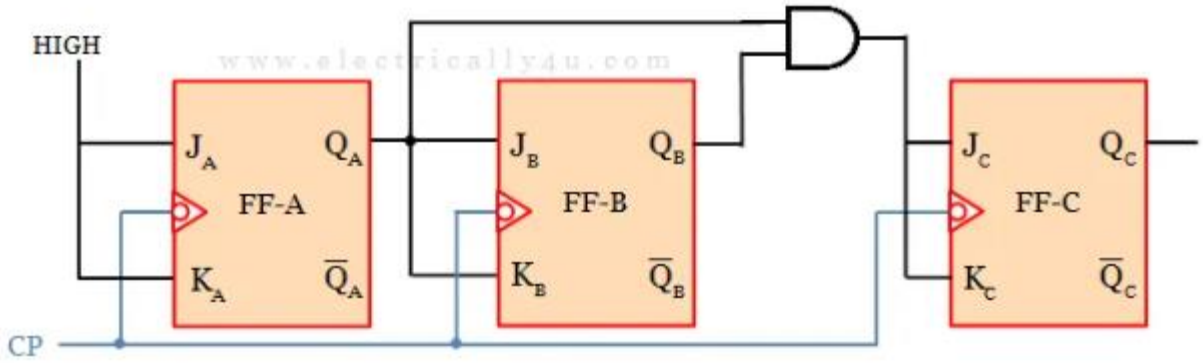


Design Steps of 3 bit Synchronous counter

Step 1: Find the number of flip flops.
Step 2: Choose the type of flip flop.
Step-3: Draw state diagram for the counter.
Step-4: Obtain excitation table for the counter.
Step 5: Derive the flip flop input functions (use K-Map)
Step-6: Draw the logic diagram of the counter.



Clock	Present State			Next State			Flip flop Inputs					
	Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	J_C	K_C	J_B	K_B	J_A	K_A
1	0	0	0	0	0	1	0	x	0	x	1	x
2	0	0	1	0	1	0	0	x	1	x	x	1
3	0	1	0	0	1	1	0	x	x	0	1	x
4	0	1	1	1	0	0	1	x	x	1	x	1
5	1	0	0	1	0	1	x	0	0	x	1	x
6	1	0	1	1	1	0	x	0	1	x	x	1
7	1	1	0	1	1	1	x	0	x	0	1	x
8	1	1	1	0	0	0	x	1	x	1	x	1



For J_C

Q_C \ Q_BQ_A	00	01	11	10
0	0	0	1	0
1	X	X	X	X

$J_C = Q_BQ_A$

For K_C

Q_C \ Q_BQ_A	00	01	11	10
0	X	X	X	X
1	0	0	1	0

$K_C = Q_BQ_A$

For J_B

Q_C \ Q_BQ_A	00	01	11	10
0	0	1	X	X
1	0	1	X	X

$J_B = Q_A$

For K_B

Q_C \ Q_BQ_A	00	01	11	10
0	X	X	1	0
1	X	X	1	0

$K_B = Q_A$

For J_A

Q_C \ Q_BQ_A	00	01	11	10
0	1	X	X	1
1	1	X	X	1

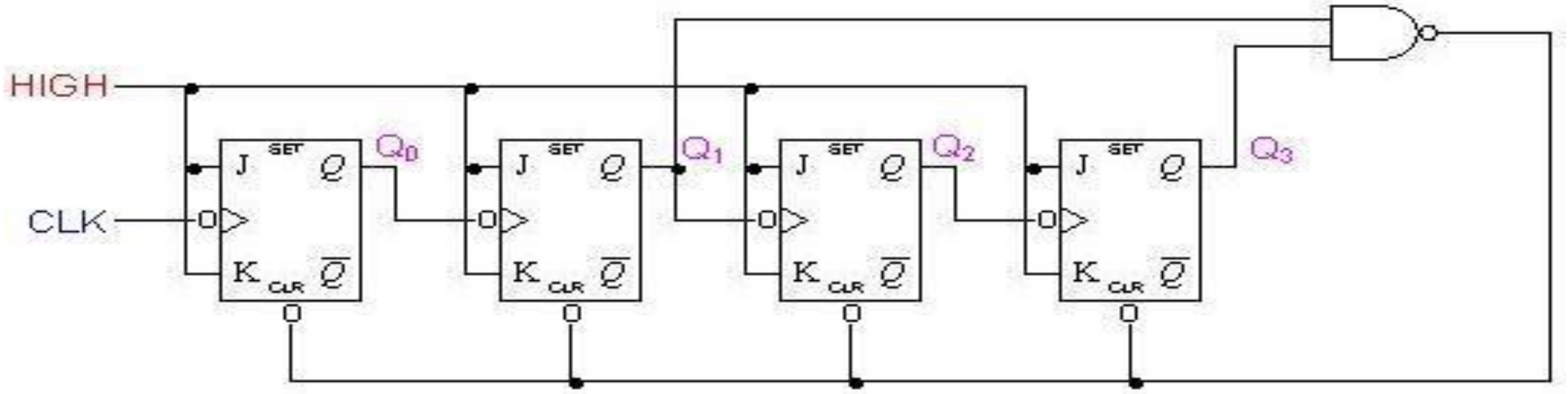
$J_A = 1$

For K_A

Q_C \ Q_BQ_A	00	01	11	10
0	X	1	1	X
1	X	1	1	X

$K_A = 1$

Decade Counter



Once the counter counts to ten (1010), all the flip-flops are being cleared.

Clock Pulse	Q3	Q2	Q1	Q0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1