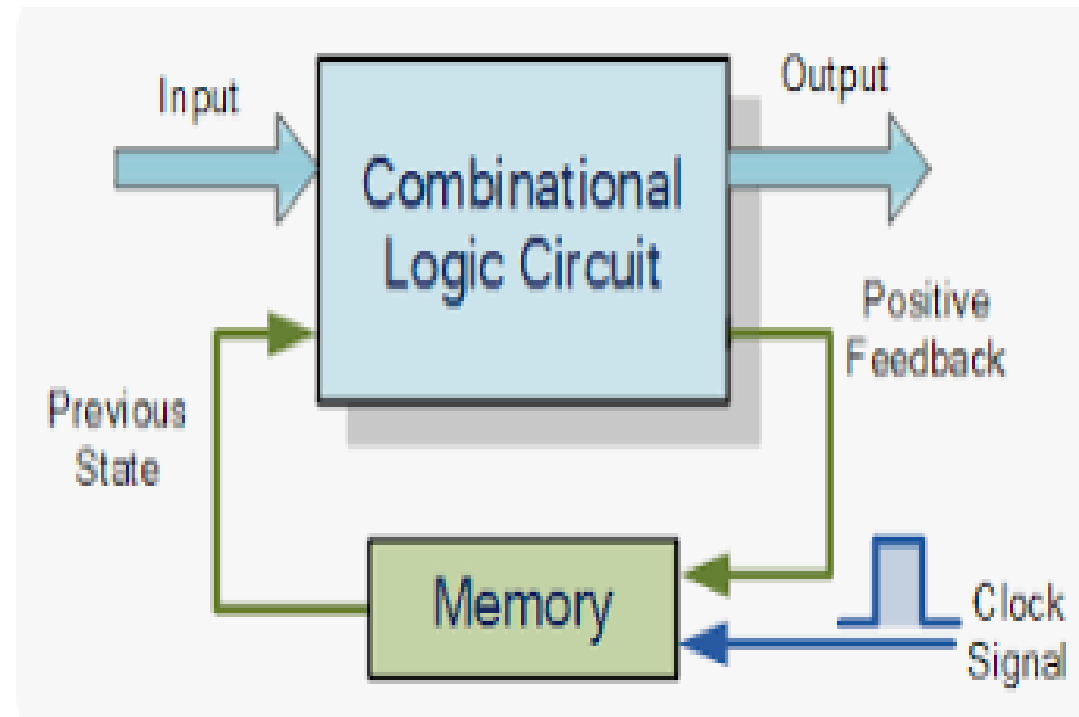


Unit-6:

Introduction to Sequential Logic Circuits

Sequential circuits are those which are dependent on clock cycles and depends on present as well as past inputs to generate any output.



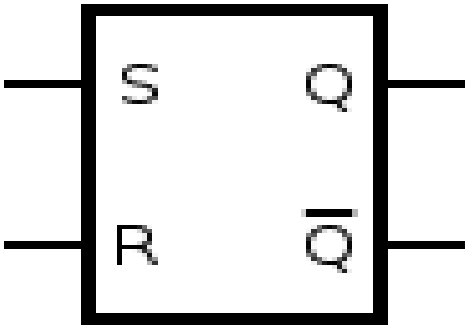
Contents

- Basic sequential circuits: SR-latch
- Types- SR flip-flop, JK flip-flop, D flip-flop, T flip-flop
- Master Slave JK flip flop
- Conversion of basic flip-flop
- Counters: Design of Asynchronous and Synchronous counters
- Ring counter and Johnson ring counter
- Registers: Operation of all basic Shift Registers

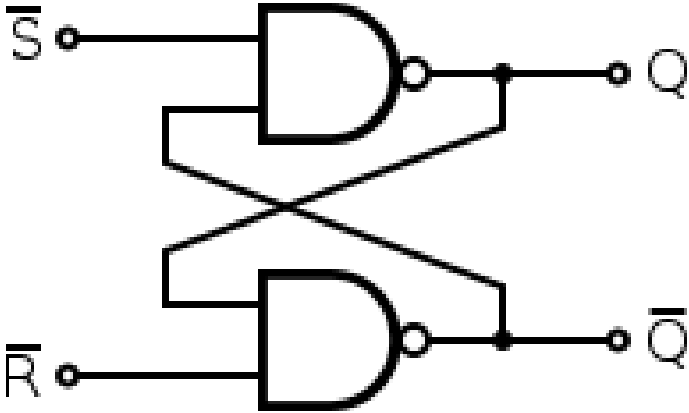
Latch

- A latch is an example of a bistable multivibrator
- Has two stable states (High-low)
- Has feedback path
- Latches can be memory devices,
- Store one bit of data for as long as the device is powered
- Asynchronous device

SR latch



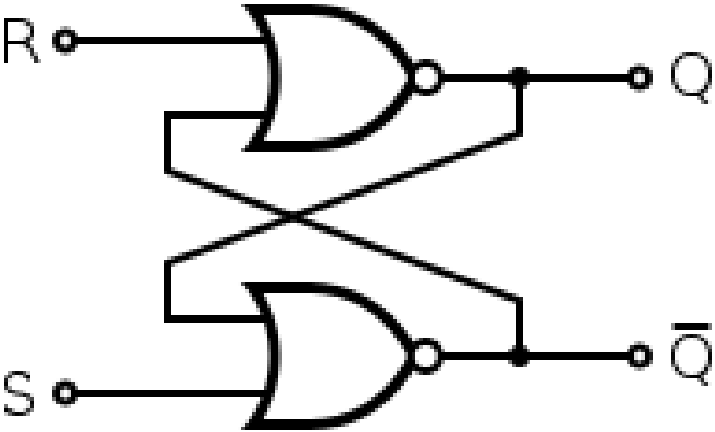
To maintain Uniformity
Input and swapped and Negated



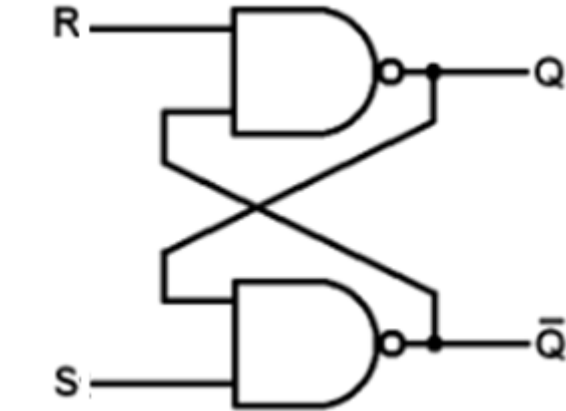
S	R	Q	\bar{Q}
0	0	No Change	
0	1	0	1
1	0	1	0
1	1	Invalid	

SR latch (Set/Reset)

can be created with two NOR/NAND gates have a cross-feedback loop.



S	R	Q	\bar{Q}
0	0	No Change	
0	1	0	1
1	0	1	0
1	1	Invalid	

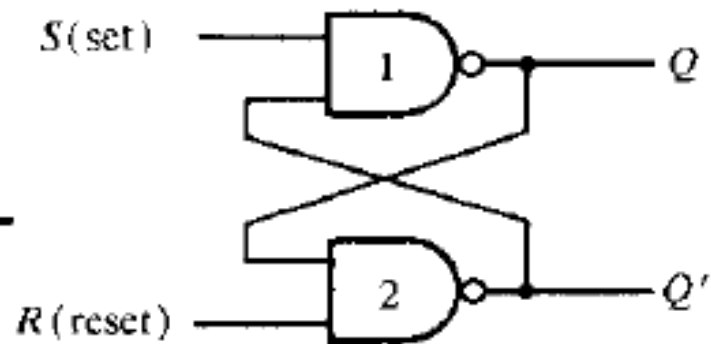


S	R	Q	\bar{Q}
0	0	Invalid	
0	1	0	1
1	0	1	0
1	1	No Change	

Difference between both....?

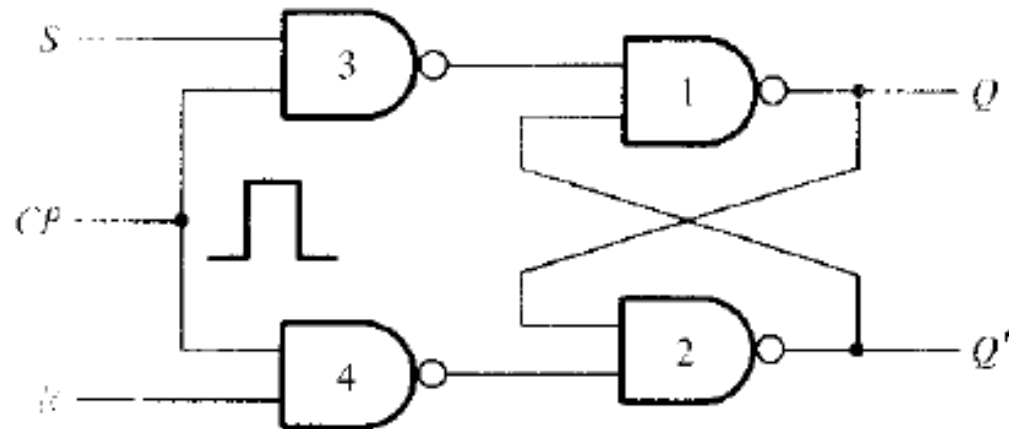
Latches..

- ❖ Both are same but there is a little difference between both.
- ❖ Latches are the building blocks of sequential circuits.
- ❖ latches can be built from gates.
- ❖ latch does not have a *clock signal*.



Flip Flop..

- ❖ flip-flops are also the building blocks of sequential circuits.
- ❖ Flip-flops can be built from latches.
- ❖ A flip-flop always has a *clock signal*



What is flip flops?

- A **flip-flop** is a circuit that has two stable states and can be used to store state information.
- A flip-flop is a bistable multivibrator.

The circuit can be made to change state by signals applied to one or more control inputs and will have one or two outputs.

- It is the basic storage element in sequential logic.
- Flip-flops maintain their state indefinitely until an input pulse called a trigger is received.

The flip-flop outputs change state according to defined rules and remain in those states until another trigger is received.

Uses of flip flops.

- ▶ Flip flop and latches are the circuits that can store and remember information.

They're the kind of circuits that are **used in computers to store program information** like RAM memory and Registers.

- ▶ Flip-flops can be used to design counter.

Types of flip flop..

- Clocked SR flip flop circuit
- D flip flop circuit
- Jk flip flop circuit
- T flip flop circuit

Clocked SR Circuit:

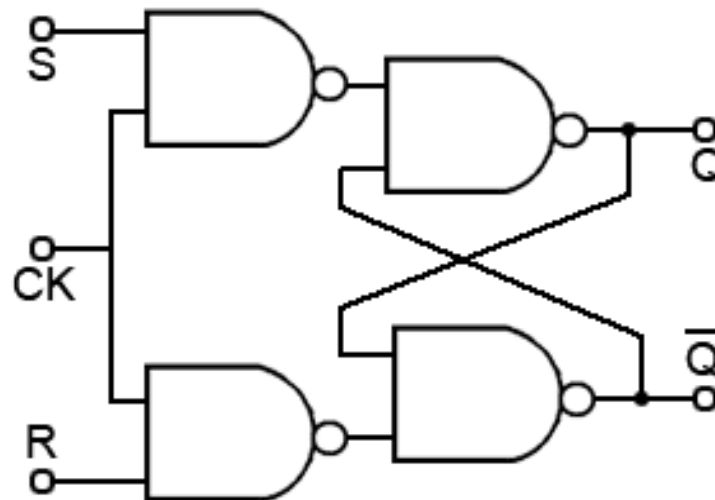
➤ DEFINITION:

“A circuit which is used to remain a memory stable by using “clock signals” is called clocked SR circuit.”

Clock Signal:

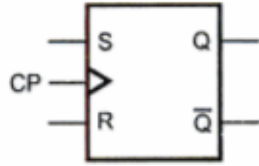
Basically clock signals are electrical pluses which are in the form of 1 or 0.

EXPLANATION OF Clocked SR Circuit:

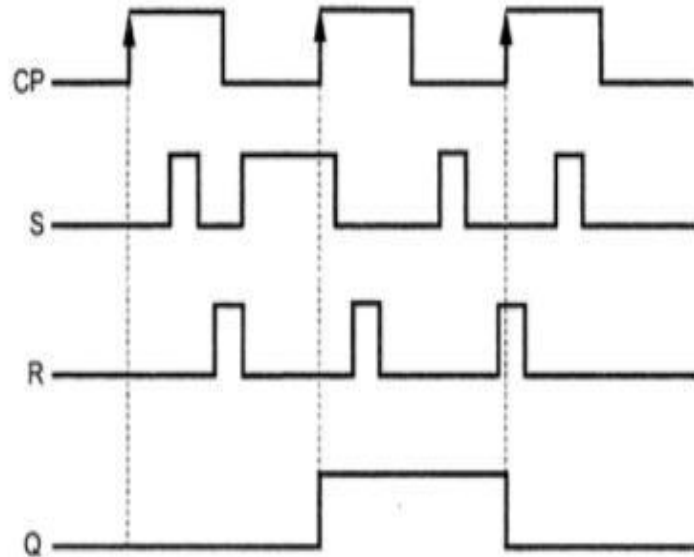


Logic Diagram:

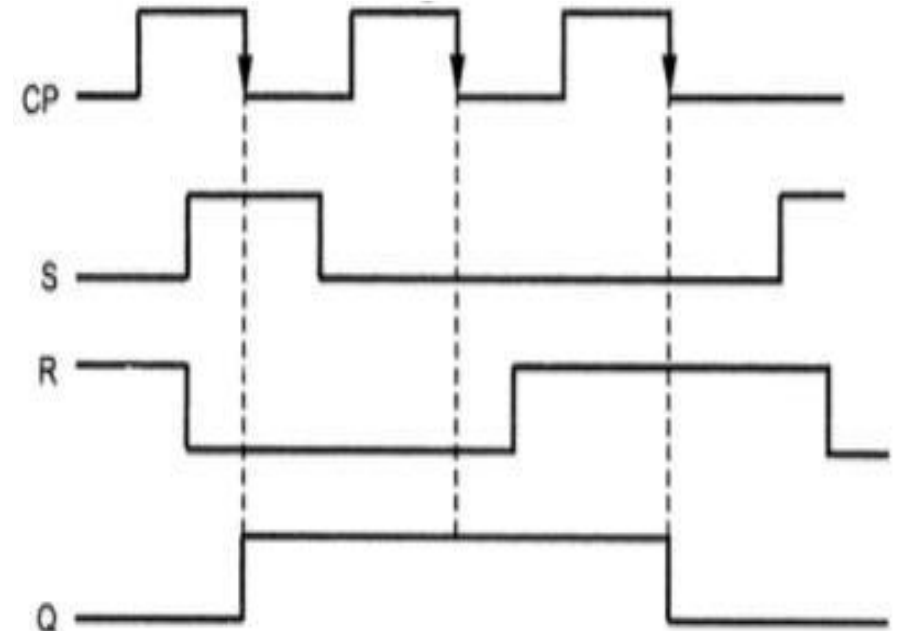
Clk	S	R	Q	Q'	
1	1	1	1	1	Not Allowed
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	0	0	Q	Q'	Memory state



Positive edge triggered SR flip-flop



Negative edge triggered SR flip-flop

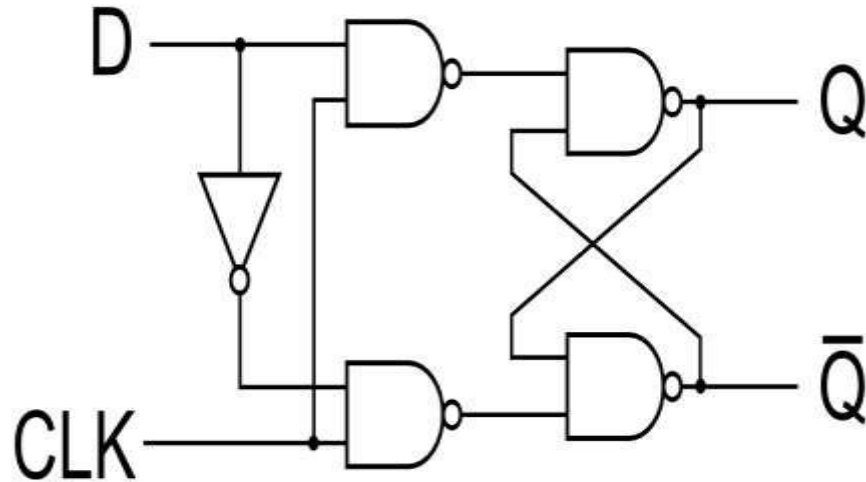


D Flip-Flop:

- A circuit which is used to remove Clocked SR Circuit's “**not allowed state**” more circuit's stability is called D flip flop.
- A circuit using Inverter is basically a SR circuit, which reduces the no. of inputs from two to one . It also called D-Latch.

➤ Uses of D Flip-Flop:

The D Flip-Flop receives the designation from its ability to transfer” **data**” into a flip-flop.

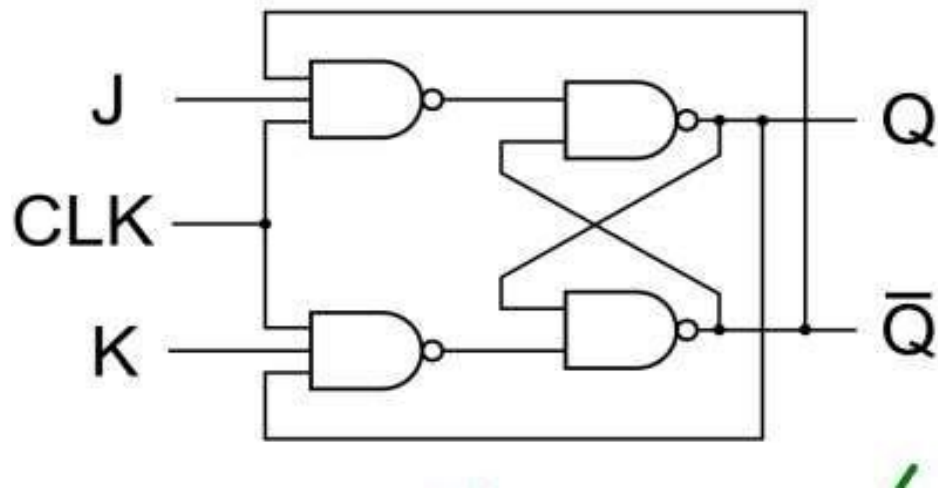


Cp	D	Q	Q'
0	0	Memory state	
1	1	Set state	
1	0	Reset state	

JK Flip-Flop:










- A JK flip-flop is a refinement of RS flip-flop circuit in that the determinate state of RS type is defined in the JK type.
- Means J and K behave like S and R to set and clear the flip-flop.”

Note: It is also used for removing not allowed state for memory state.



Circuit Diagram:

Truth Table:

Trigger	Inputs		Output				Inference
			Present State		Next State		
CLK	J	K	Q	Q'	Q	Q'	
	x	x	-		-		Latched
	0	0	0	1	0	1	No Change
			1	0	1	0	
	0	1	0	1	0	1	Reset
			1	0	0	1	
	1	0	0	1	1	0	Set
			1	0	1	0	
	1	1	0	1	1	0	Toggles
			1	0	0	1	

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	Q_n'

J K Flip-Flop:

Memory state:

When $\text{Clk}=0$ and J and K=don't care conditions then memory stays stable.

ALSO:

When $\text{Clk}=1$ and both J and K are 0, then memory also stays stable.

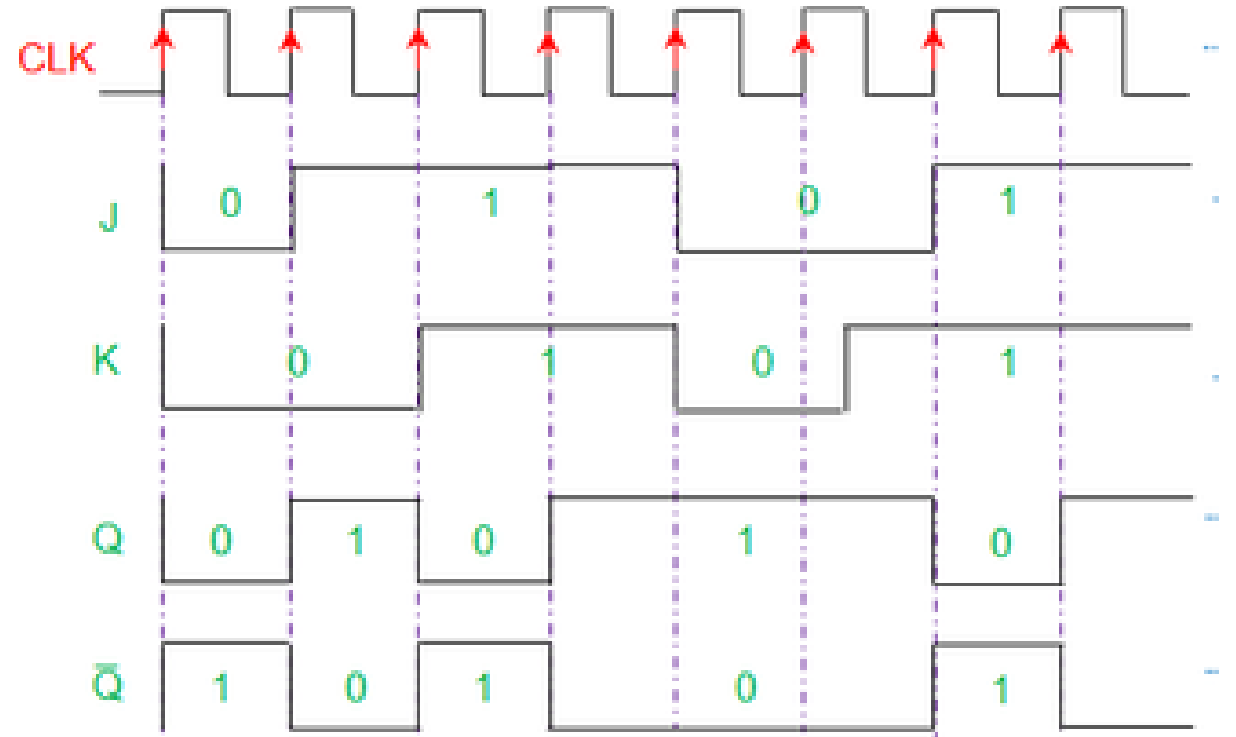
Set state:

When inputs are given as $\text{Clk}=1$ and $J=1$ and $K=0$, then the output comes $Q=1$ AND $Q'=0$. (“WHEN Q comes 1 this state is called SET state”)

ReSet state:

When inputs are given as $\text{Clk}=1$ and $J=0$ and $K=1$, then the output comes $Q=0$ and $Q'=1$. (“WHEN Q' comes 1 this state is called RESET state”)

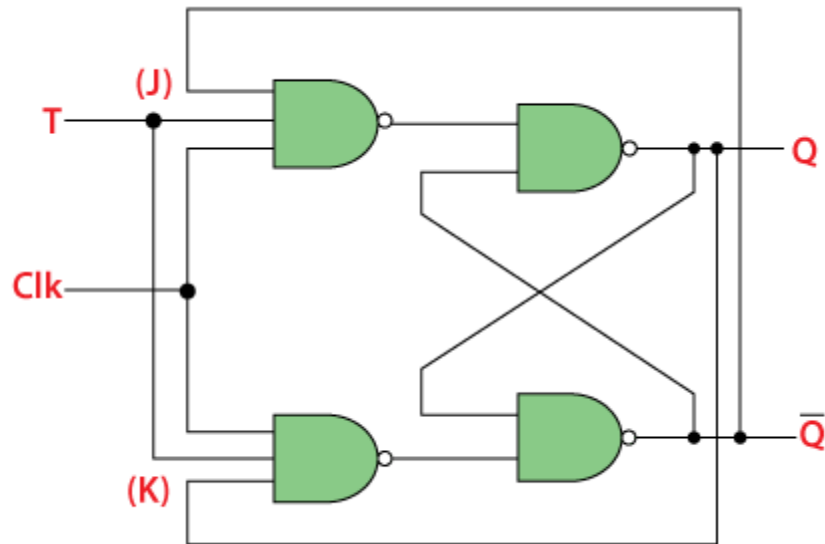
Timing Diagram



T-Flip Flops

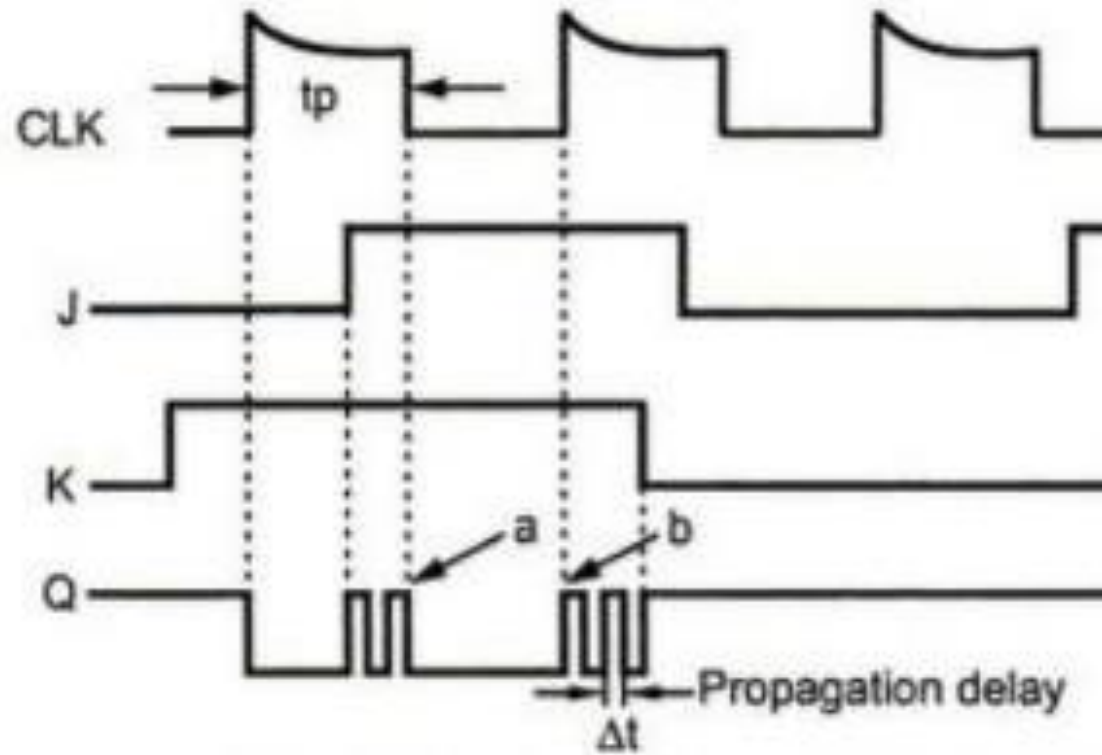
- T or "toggle" flip-flop changes its output on each clock edge, giving an output which is half the frequency of the signal to the T input.
- It is useful for constructing binary counters, and frequency dividers.
- It can be made from a J-K flip-flop.

Circuit Diagram:



T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Race Around Condition?



Master-Slave Flip Flop?

Two JK FFs by connecting in series.

One of these FFs, one FF works as the master as well as other FF works as a slave.

