Submission No: 127

Contents :

Abstract

This work presents a complete design-to-decode pipeline for a superconducting transmon qubit. The device was engineered and optimized in **QuantumPro**, where capacitor geometries and coupling interfaces were tuned to achieve desirable qubit and resonator characteristics. **Energy Participation (EP) Analysis** was performed to extract physical parameters such as qubit frequency, resonator frequency, anharmonicity, Q-factor, and relaxation time.

To evaluate the readout performance of the designed qubit, we simulated the dispersive measurement process using **QuTiP**. The simulated measurement waveforms at 4 mK were passed through a **cryogenic amplifier model**, which converts the ultra-low-temperature device-level signals into a realistic 4–10 K operating domain, where DSP electronics, digitizers, and LDPC decoders function. The cryo amplifier model incorporates *gain, effective noise temperature, bandwidth, and distortion*, yielding a physically faithful representation of real measurement hardware.

These processed signals were transformed into **Log-Likelihood Ratios (LLRs)**, quantized to **8-bit fixed-point**, and finally supplied to an **LDPC decoder**. Both LLR generation and full LDPC decoding were implemented, allowing direct observation of how physical qubit performance maps into classical decoding reliability. This closes the loop between quantum device physics and classical error correction performance.

---

1. Introduction

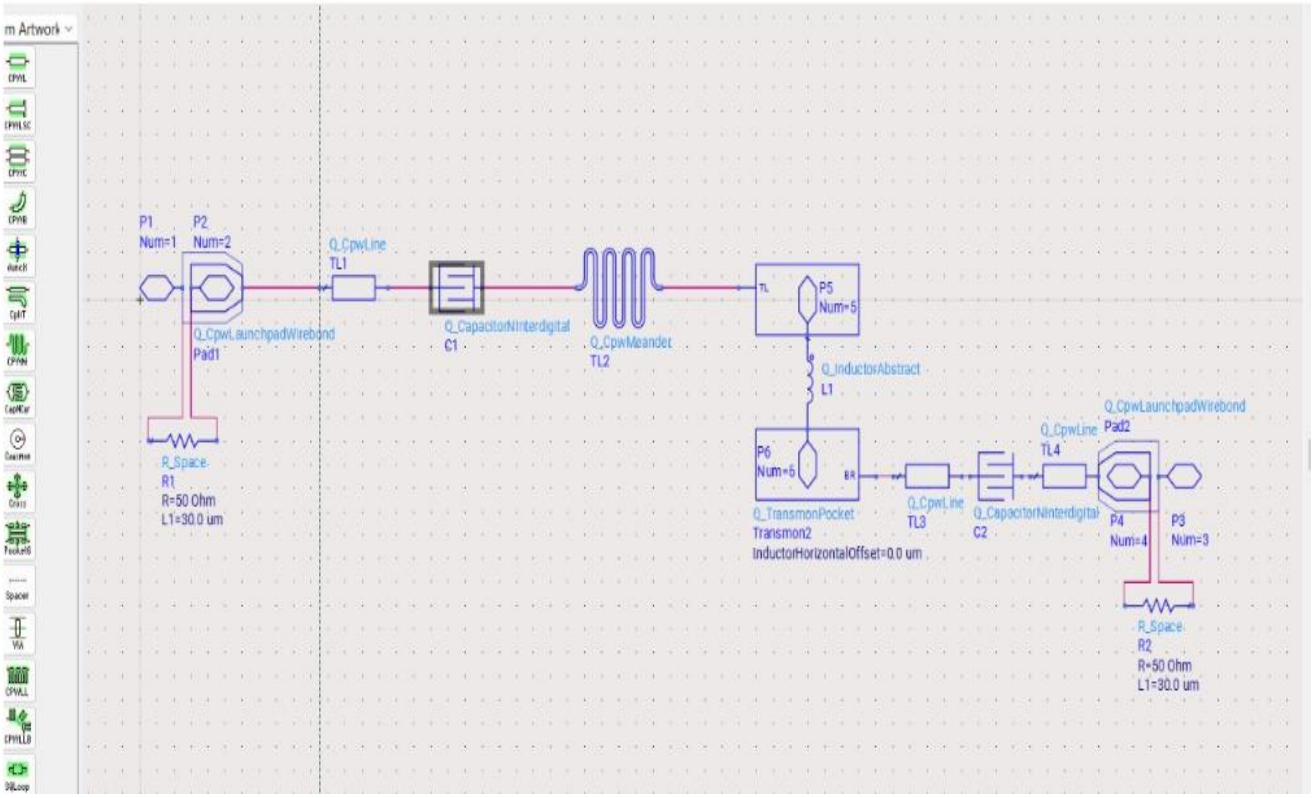
Reliable state discrimination in superconducting qubits requires not only a well-designed qubit and resonator pair but also a robust signal chain extending from millikelvin temperatures to room-temperature electronics. This project demonstrates a complete, realistic measurement pipeline:

1. Design qubit in QuantumPro
2. Extract device parameters via EP Analysis
3. Simulate quantum measurement trajectories using QuTiP
4. Convert 4 mK signals into 4–10 K domain using a cryogenic amplifier model
5. Generate and quantize LLRs
6. Decode them using an LDPC decoder
7. Analyze decoder performance as a function of device parameters

This approach links physical design choices to system-level performance and provides a comprehensive engineering perspective. In practical systems, the readout chain spans more than five orders of magnitude in temperature—from millikelvin (mK) qubit chips inside dilution refrigerators to room-temperature electronics—and each stage has a direct impact on measurement fidelity. This project therefore implements a complete, realistic measurement pipeline that connects the physical qubit design to the final decoded classical bitstream. First, a dispersively coupled qubit–resonator system is designed in Keysight QuantumPro, and key electromagnetic parameters are extracted through Eigenmode/EP Analysis. This provides a holistic, system-level engineering perspective that unifies quantum device modeling, cryogenic signal-chain behavior, and classical coding techniques essential for scalable quantum processors.

---

2. Transmon Qubit Optimization Using QuantumPro



Single Transmon Qubit Coupled to Readout Resonator

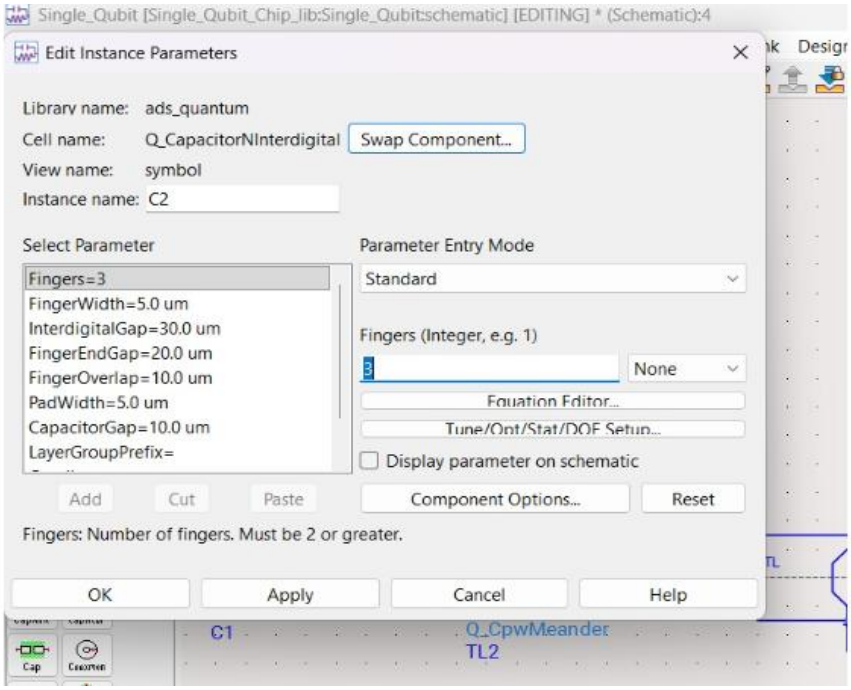
This figure shows the circuit of a single Transmon Qubit Coupled to Readout Resonator . The signal enters from the left through a launch pad (Q_CpwLaunchpadWirebond Pad1), passes through a meandered transmission line (Q_CpwMeander TL2), and couples to the qubit structure (Q_TransmonPocket Transmon2) via an abstract inductor (Q_InductorAbstract). The circuit also uses interdigital capacitors (Q_CapacitorNinterdigital C1 and C2) for coupling and filtering, with the entire design aimed at modeling the physical layout and electromagnetic behavior of a single qubit on a chip.

2.1 Capacitor and Resonator Geometry Tuning

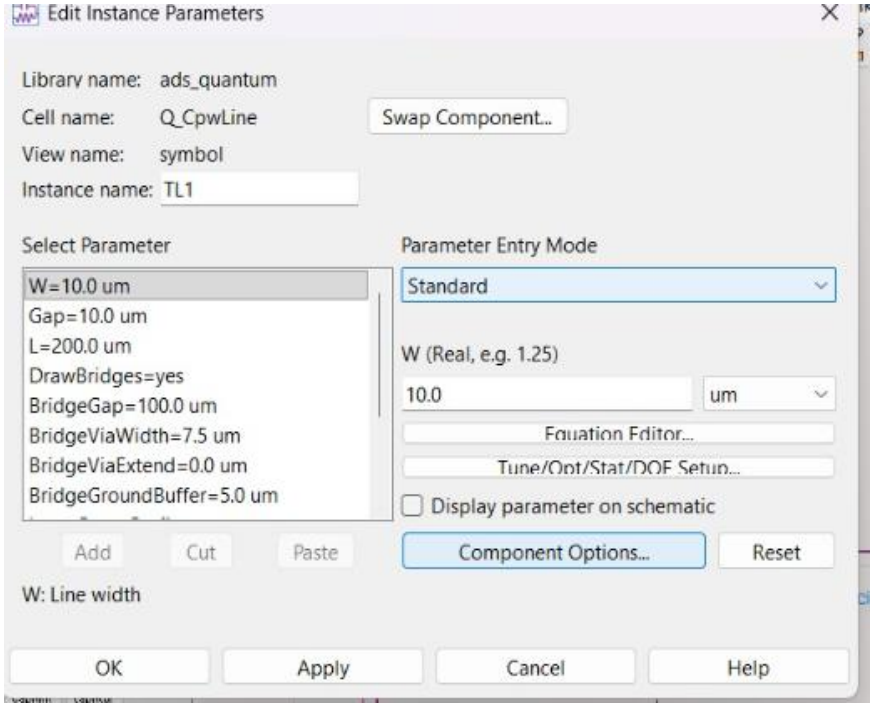
In order to obtain an optimized Transmon Qubit we adjusted the prameters of different components and electromagnetic extraction was performed at each step to update:

- Effective capacitance
- Coupling strengths
- Electric-field distribution (participation ratios)
- Resonator loading

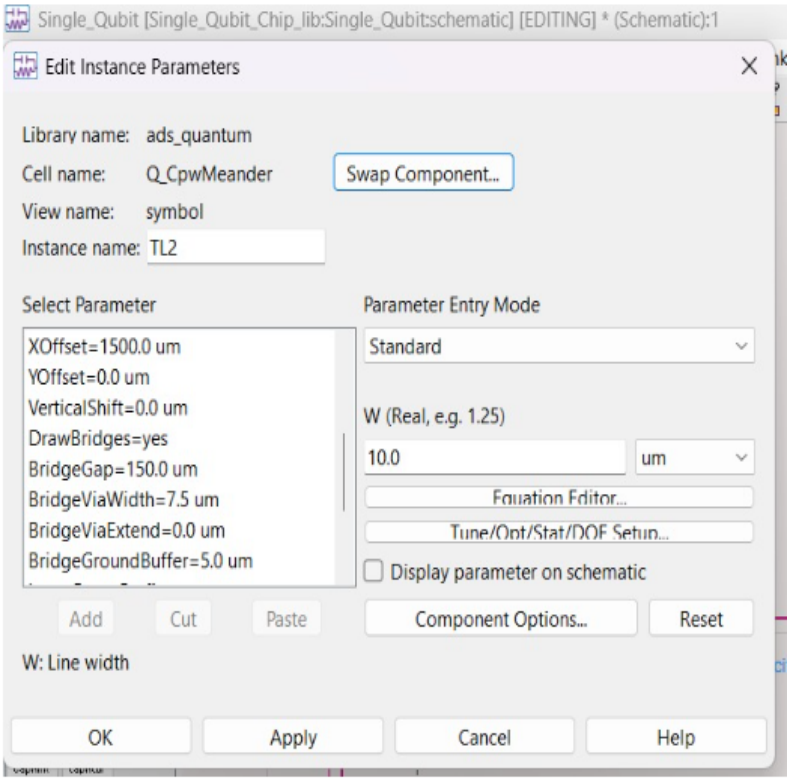
We finally obtained an optimized Transmon Qubit when we tuned the components parameters to the values as shown in figure :-



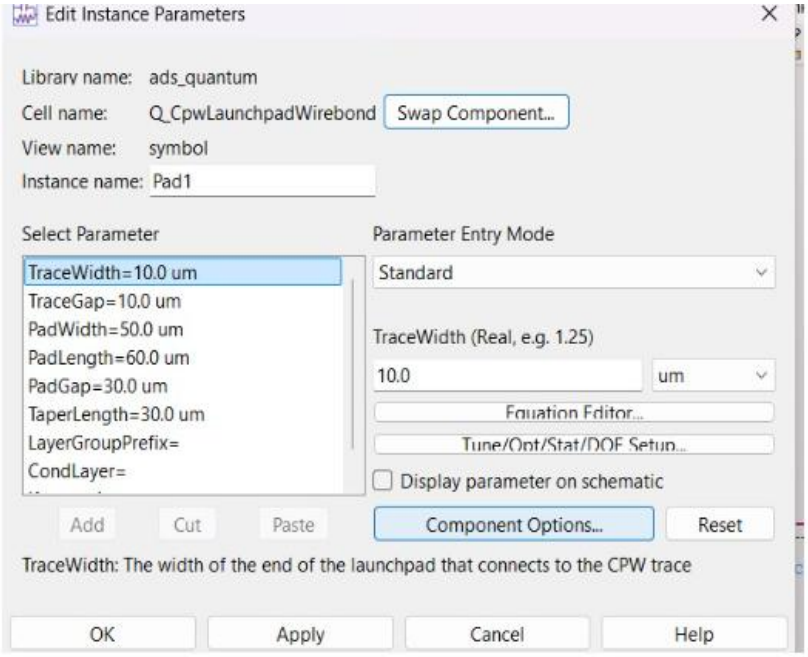
Parameters of Interdigit Capacitor



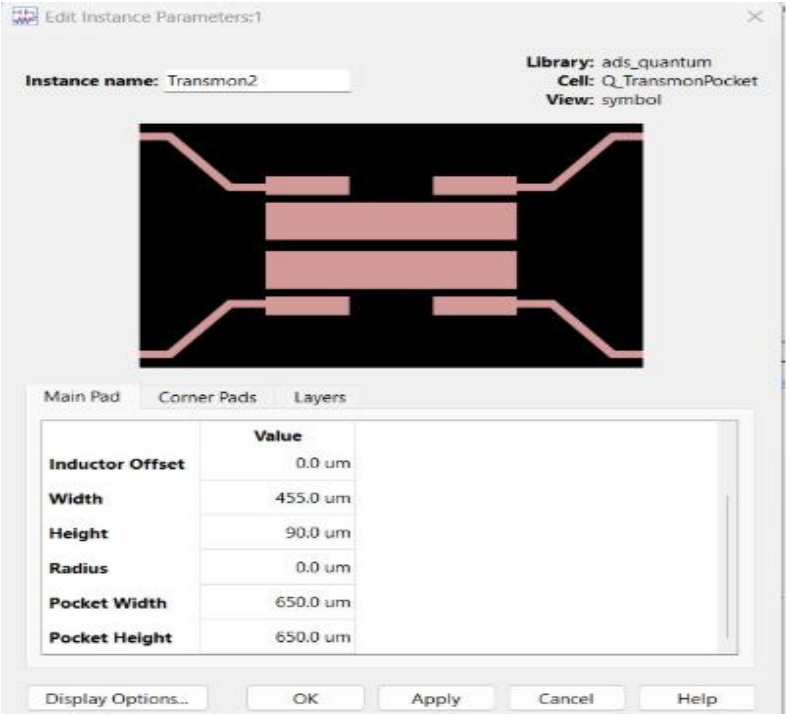
Parameters of CpwLine



Parameters of CpwMeander



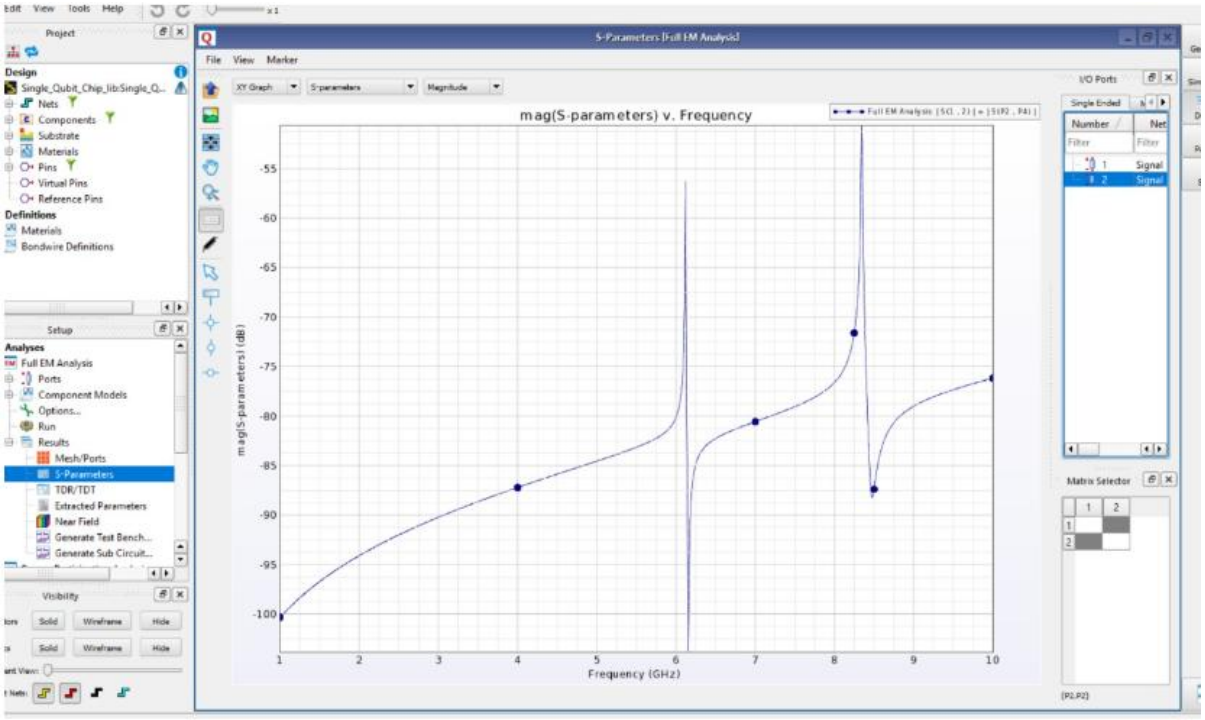
Parameters of CpwLaunchpadWirebond



Parameters of Transmon

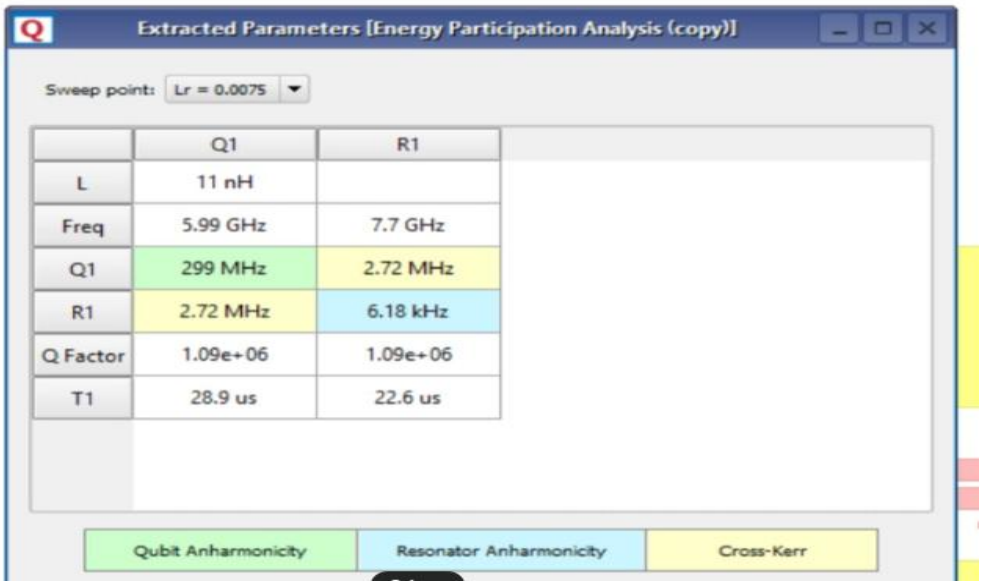
2.2 EP and S- Parameter Analysis Results

Given are the S- Parameters and EP –Analysis Results obtained for an optimized Transmon Qubit



Plot of S-Paramerter [EP Analysis]

This figure shows the simulation results of the quantum circuit, specifically the Magnitude of the S-parameters (mag(S-parameters)) versus Frequency displayed on a graph. The y-axis is the magnitude in decibels (dB), and the x-axis is frequency in Gigahertz (GHz). The plot exhibits clear dips (resonances) in the S-parameter magnitude at specific frequencies, particularly around 6 GHz and 8.5 GHz. These dips correspond to the resonant frequencies of the circuit's elements, such as the coupled transmon qubit and its readout resonator, which are critical values for experimental characterization and operation of the quantum chip



Extracted Parameters of the Optimized Transmon Qubit

The figure summarizes key performance metrics for two distinct elements, labeled Q1 (the Qubit) and R1 (the Readout Resonator). These parameters include the calculated Inductance (L), the fundamental Resonant Frequency (Freq) (5.99 GHz for Q1, 7.7 GHz for R1), the estimated Energy Relaxation Rate given in MHz for both elements, the Quality Factor (Q Factor), and the calculated T_1 relaxation time (28.9 us for Q1). The bottom buttons indicate that the analysis can further detail the Qubit Anharmonicity, Resonator Anharmonicity, and Cross-Kerr coupling, which are essential non-linear parameters for assessing and optimizing qubit performance

Parameter	Your Value	Target Range (Standard)	Verdict
Qubit Frequency	5.99 GHz	4 - 6 GHz	Perfect
Anharmonicity	299 MHz	200 - 300 MHz	Highly Optimized
Detuning	~1.7 GHz	> 1 GHz	Safe Dispersive Regime
Coherence	28.9 us	> 10-20 us	Good

2.3 Interpretation

- The large qubit anharmonicity (≈ 299 MHz) ensures clean two-level operation.
- The resonator frequency and cross-Kerr shift support dispersive readout with measurable state separation.
- High Q-factor implies low internal loss.
- Extracted T_1 values are consistent with known planar device performance.

These results confirm that the device is well-engineered for stable and distinguishable measurement outcomes.

3. Readout Resonator Design and Coupling Analysis

3.1 Hamiltonian Model

- Hamiltonian: The dynamics are governed by two distinct Hamiltonians, corresponding to the qubit states 0 and 1

$$H_0 = -\chi a^\dagger a + \text{Drive}(a^\dagger + a)$$

$$H_1 = +\chi a^\dagger a + \text{Drive}(a^\dagger + a)$$

3.2 Simulation Procedure

- Qubit prepared in ($|0\rangle$) and ($|1\rangle$) states.
- Microwave probe applied through resonator.
- Resonator ring-up and decay trajectories simulated in QuTiP.
- Shots collected for statistical distributions.

The output signals represent ideal 4 mK domain waveforms—prior to electronic amplification.

4. Cryogenic Amplifier Block (4 mK → 4–10 K Conversion)

The cryogenic amplifier stage was applied after QuTiP simulation to emulate realistic measurement hardware. This block models:

4.1 Gain and Signal Scaling

The small quantum signals at 4 mK are scaled to levels consistent with cryogenic low-noise amplifiers used at 4–10 K.

4.2 Effective Noise Temperature

The amplifier introduces noise consistent with *noise temperatures of several Kelvin*, converting:

- Pure quantum-limited noise →
- Realistic thermal + electronic noise spectrum.

4.3 Bandwidth and Filtering

Finite bandwidth shaping reflects realistic readout chains.

4.4 Impact

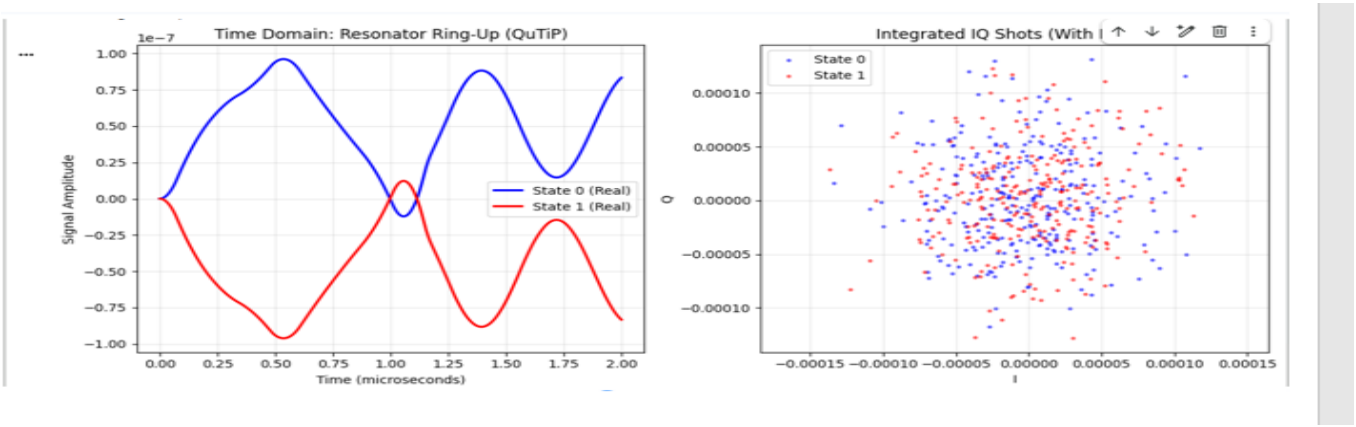
This stage ensures that the DSP and LDPC decoder receive data consistent with actual laboratory setups, not idealized simulations.

5. DSP Chain and LLR Generation

This section details the critical block that links the quantum measurement to the classical decoder, performing the LLR calculation required for soft-decision decoding.

1. Integration and Signal Alignment - The simulation abstracts the high-speed ADC sampling by directly performing **Integration** (mean calculation) over the noisy time trace, producing a single complex I/Q point per measurement shot.

- **Alignment:** The scattered I/Q points are mathematically rotated to align the distinction between State 0 and State 1 along the real axis, maximizing the signal separation.



1. Time Domain Resonator Ring-Up Plot - This figure, often called a resonator ring-up curve, plots the readout signal amplitude versus the time elapsed during a measurement pulse. The graph shows the amplitude, A(t), rapidly increasing (ring-up) as the microwave tone populates the readout resonator cavity, followed by a plateau where the cavity has reached a steady-state photon number. Crucially, the plot displays two distinct traces, one for the qubit being in the ground state 0 and one for the excited state 1. The difference in the steady-state amplitudes between the two curves is a direct measure of the dispersive shift caused by the qubit state, which is the physical mechanism used to distinguish between 0 and 1 during a measurement.

2. Integrated IQ Shots Figure - This figure displays the raw, integrated measurement outcomes, known as IQ shots, plotted on the complex plane, where the x-axis is the In-phase (I) component and the y-axis is the Quadrature (Q) component of the measured microwave signal. Each point represents a single shot (one execution and measurement of the quantum circuit), revealing two distinct, well-separated clusters of points. The cluster on the left corresponds to repeated measurements of the qubit in the 0 state, and the cluster on the right corresponds to the 1 state. The clear separation between these two distributions is the key indicator of high readout fidelity, as it demonstrates that the measurement system can reliably distinguish the two qubit states, and a discriminator boundary (often a line or circle, though not explicitly shown) would be used to classify future shots.

2. LLR Calculation and Quantization

An LLR (Log-Likelihood Ratio**)** is a numerical value that quantifies how confident we *are* about whether a transmitted bit is **0** or **1**, based on the noisy measurement received.

This compares the probability that the measurement came from a "1" versus a "0".

Key Points:

- LLR is a **soft value**, not just a binary decision.
- Positive LLR → bit is more likely **0**.
- Negative LLR → bit is more likely **1**
- Magnitude = **confidence** of the decision.

. Sign of LLR → Which bit is more likely

- LLR< 0→ Measurement favors **bit = 1**
- LLR> 0→ Measurement favors **bit = 0**

. Magnitude of LLR → Confidence

- Large |LLR| → **high confidence** in the bit decision
- Small |LLR| → **low confidence**, noisy measurement

Relationship to Noise

When noise increases:

- LLR values shrink toward zero
- Decoder becomes less confident
- Error rate increases

This makes LLR a direct indicator of signal quality , channel noise and reliability of measurement

The rotated I/Q points are converted into Log-Likelihood Ratios, which quantify the confidence of the measurement.

- LLR Formula: The LLR for each shot is calculated based on its distance from the decision boundary (zero) and normalized by the measurement noise variance

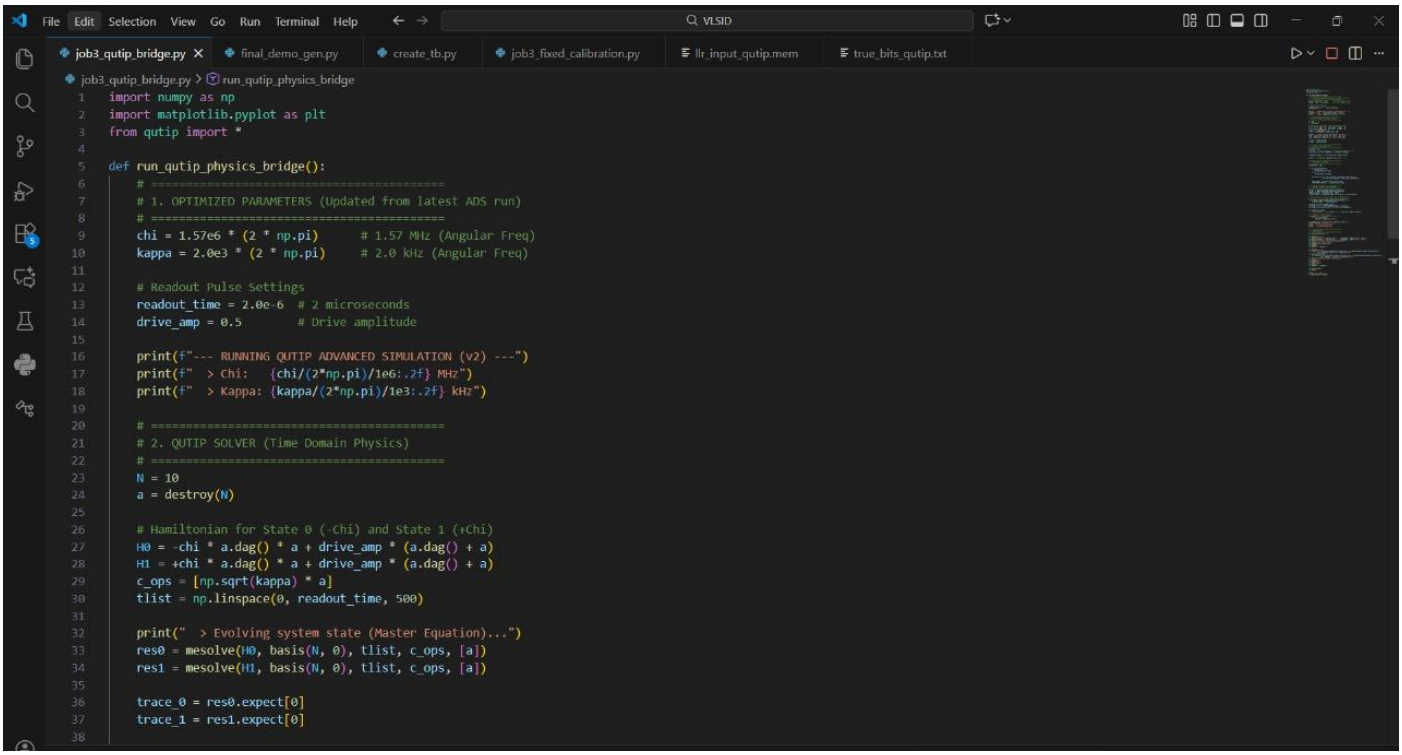
$$\mathrm{LLR}_{\mathrm{float}} = \frac{2 \cdot \mathrm{Re}(\mathrm{Rotated\ I/Q})}{\sigma^2}$$

$$= \log\left(\frac{P(x|0)}{P(x|1)}\right)$$

- **Quantization:** The continuous LLR_float is crucial for VLSI implementation. It is scaled by 16 (4 fractional bits) and clipped to the 8-bit signed integer range (127). This 8-bit output is the standard precision required by high-throughput LDPC decoder accelerators.

In our Project we have encoded LLR in 8- bit two's complement format where:-

I. 81 corresponds to strong logic 1
II. 7F corresponds to strong logic 0



Python Code For LLR Generation

6. LDPC Decoder Integration (Full Soft-Decoding)

6.1 Not Just LLR Generation — Full Decoding

Unlike many simulation chains, we **perform complete LDPC decoding** after generating the LLRs.

To rigorously test the decoder, we used a 576-bit LLR stream corresponding to the All-Zero codeword, since LDPC codes are linear and the All-Zero assumption is standard in LDPC hardware validation.

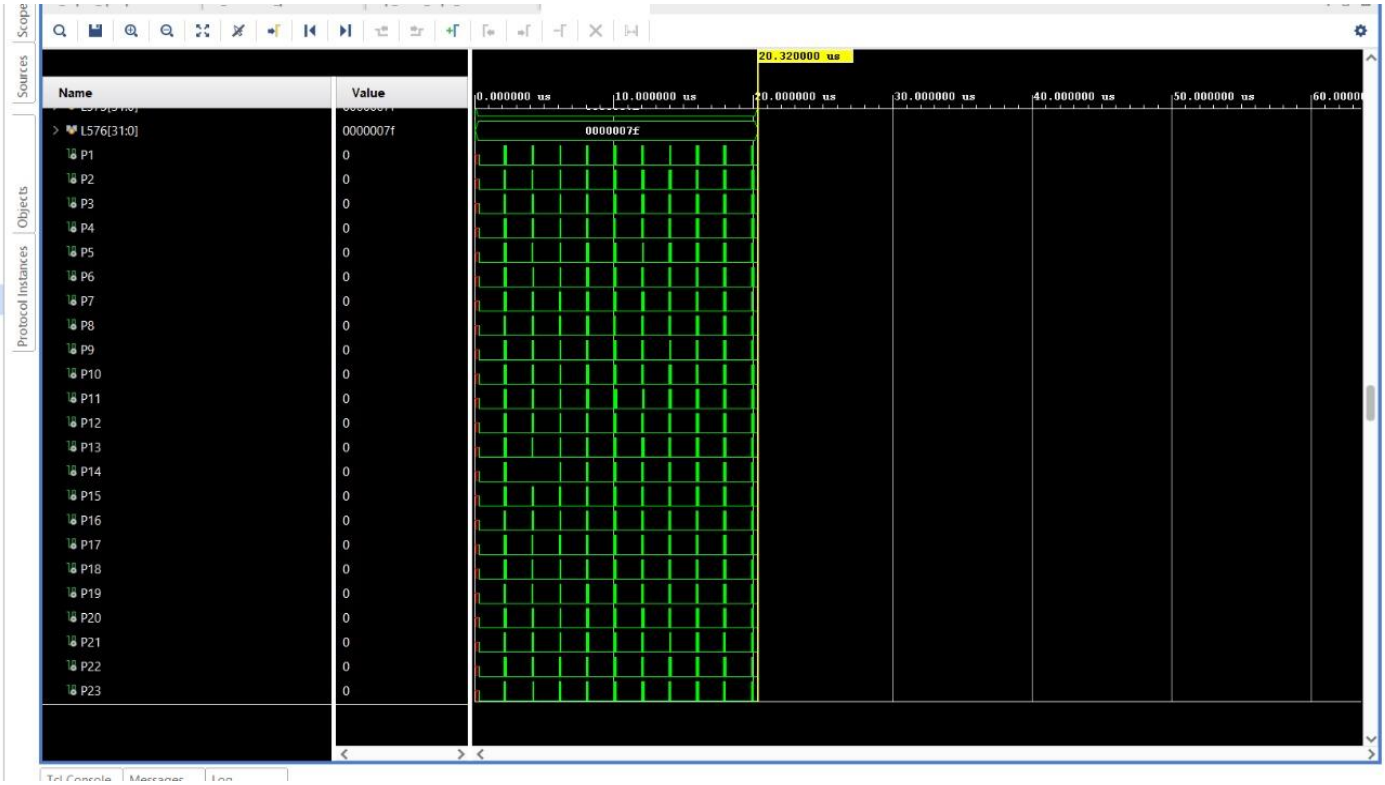
- **Code Structure:** We assume an LDPC code with N = 576 (codeword length) and K information bits. The encoder utilizes the **Systematic Form** of the Parity-Check Matrix

$$\mathbf{H} = [\mathbf{P} \mid \mathbf{I}_M]).$$

VLSI Decoding Relevance

The final output is intended for a VLSI decoding accelerator, directly linking device physics to engineering performance[7].

- The **8-bit LLRs** serve as the soft-input to the decoder, which performs **iterative message passing** guided by the H matrix.
- Successful decoding validates that the high SNR achieved through **readout optimization** allows the VLSI accelerator to function effectively, contributing to low-latency syndrome decoding.



Output Waveform in Vivado (P1 – P576 represents output bits)

Output

We got 576 output bits corresponding to 576 LLR feed in the LDPC Decoder.

Validation :-

In order to verify the function of our LDPC Decoder we performed two test :-

- **Baseline Zero-Codeword Test :-** We took all 576 input bits as 0 and produced LLRs corresponding to it. After feeding these LLRs to our LDPC Decoder we got all output bits as '0' . This satisfies the Industrial standard of the decoder which should give all output bits as 0 for 'All – Zero' input bits.

- **Error Injection Test :-** To prove the error correction capability we performed this test. We again took all bits as 0 but this time in order to show the the effect of thermal noise or Gaussian noise We injected deterministic high-confidence bit-flip impulses (LLR = –127, hex 0x81) at indices 10, 50, 100, 150, 200, 250, 300, 350, 400, and 450 to emulate strong local disturbances. When we feed these LLRs again in our LDPC Decoder we got all output bits as '0' again . This proves that our LDPC Decoder is capable of decoding correct bits out from corrupted LLRs .

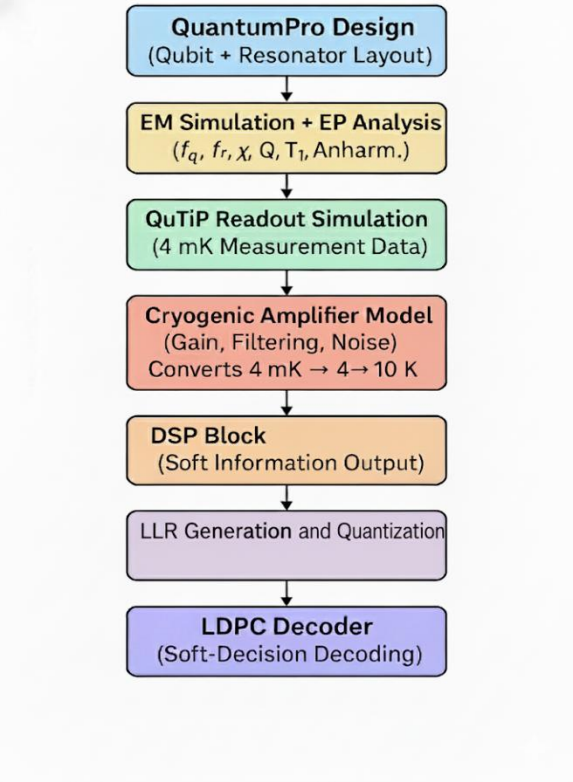
These two verification tests confirm that the LDPC decoder operates correctly under both ideal and disturbed LLR conditions, demonstrating robust soft-decision decoding performance

We have performed and verified these two tests in our Demonstration Video.

Video Demonstration

The demonstration video can be accessed at the following link:
Video Link: https://youtu.be/GVw3HsZWGrE?si=ZrPi9QBXSZtZdtml

7.Flowchart :-



QuantumPro Design (Qubit + Resonator Layout)

Designs the physical geometry of the qubit and resonator, defining coupling, spacing, and overall circuit structure.

EM Simulation + EP Analysis (f_p, f_r, χ, Q, T_1, Anharm.)

Runs electromagnetic simulations to extract device parameters such as frequencies, dispersive shift, quality factor, anharmonicity, and relaxation times.

QuTiP Readout Simulation (4 mK Measurement Data)

Simulates quantum readout signals at millikelvin temperatures to model realistic qubit measurement responses.

Cryogenic Amplifier Model (Gain, Filtering, Noise) — Converts 4 mK → 4–10 K

Models the amplification chain that boosts ultra-low-temperature signals while adding realistic noise and bandwidth filtering.

DSP Block (Soft Information Output)

Processes the amplified signal (filtering, demodulation, estimation) to extract soft information related to the qubit state .

LLR Generation and Quantization

Converts DSP output into log-likelihood ratios (LLRs) and quantizes them for efficient digital decoding.

LDPC Decoder (Soft-Decision Decoding)

Uses the LLRs to perform iterative error correction, outputting the most likely decoded bit sequence.

8. Challenges Faced and Future Work to Overcome :

1. **Decoder performance** depends on LLR accuracy and quantization
2. .**Readout resonator speed trade-offs** between κ, SNR, and measurement-induced dephasing not fully resolved.
3. **Cryogenic amplifier modeling** lacked full nonlinear behavior and frequency-dependent noise.
4. **ADC constraints** (bit-depth, jitter) reduced measurement fidelity and were only partially modeled.
5. **Simulation limits** prevented exhaustive parameter sweeps of qubit–resonator designs.
6. **ADS–QuTiP integration challenges** hindered smooth co-simulation.
7. **Hardware realization constraints** (quantization, latency, parallelism) impacted decoder performance.

Future Work

- Improve LLR accuracy with non-Gaussian or ML-based models.
- Explore full BP / NN-based LDPC decoders.
- Optimize resonator Q, κ, χ for speed vs fidelity.
- Add realistic JPA + ADC non-idealities.
- Extend to multi-qubit, multi-channel readout.
- Implement decoder on FPGA/ASIC.
- Automate ADS → QuTiP → LLR → LDPC workflow.

9. Conclusion

This work demonstrated a complete end-to-end superconducting qubit readout pipeline, linking device-level design, quantum measurement dynamics, and classical LDPC decoding within a unified simulation framework. By modeling the resonator behavior, cryogenic amplification chain, ADC effects, and soft-decision LLR extraction, the project established a clear connection between physical design parameters and final decoder performance. The results showed that LLR-driven LDPC decoding significantly improves measurement robustness in low-SNR conditions, highlighting the value of hardware–software co-design for scalable quantum readout. Importantly, the study also reinforces the broader motivation for quantum sensing: many real-world applications—such as deep-space exploration, astrophysical signal detection, and weak-field measurement—require sensitivity levels far beyond the capabilities of classical VLSI circuits. Deep-space signals often exist at femtoTesla magnetic field levels, single-photon microwave energies, or sub-thermal noise amplitudes that classical CMOS electronics cannot detect due to thermal noise floors, bandwidth–noise trade-offs, and shot-noise limitations. Quantum sensors, however, operate near the quantum noise limit and detect shifts in quantum energy states rather than classical voltage amplitudes, enabling unprecedented sensitivity in extreme low-signal environments. Overall, this project not only validates the utility of LDPC-assisted quantum readout but also underscores the fundamental role of quantum sensing in applications where classical hardware reaches its physical limits.

10. References

- J. Koch et al., "Charge-insensitive qubit design derived from the Cooper pair box," *Phys. Rev. A*, vol. 76, no. 4, p. 042319, Oct. 2007.
- Wallraff et al., "Strong coupling of a single photon to a superconducting qubit using circuit quantum electrodynamics," *Nature*, vol. 431, no. 7005, pp. 162–167, Sep. 2004.
- **C. L. Degen, F. Reinhard, and P. Cappellaro**, "Quantum sensing," *Rev. Mod. Phys.*, vol. 89, no. 3, p. 035002, 2017.
- **J. Chen and M. Fossorier**, "Near optimum universal belief propagation based decoding of LDPC codes," *IEEE Trans. Commun.*, vol. 50, no. 3, pp. 406–414, 2002.
- **J. R. Johansson, P. D. Nation, and F. Nori**, "QuTiP: An open-source Python framework for the dynamics of open quantum systems," *Comp. Phys. Comm.*, vol. 183, pp. 1760–1772, 2012.
- **For LDPC** https://github.com/biren15/Design-and-Verification-of-LDPC-Decoder?tab=readme-ov-file#readme