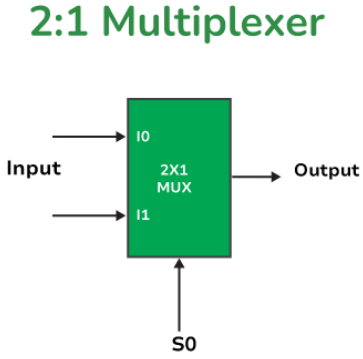
Day 9

2x1 and 4x1 Multiplexer in Verilog

1) 2x1 MUX



Truth Table

S_0	I_0	I_1	Y
0	0	X	0
0	1	X	1
1	X	0	0
1	X	1	1

🔧 **Verilog Code**

A) Dataflow modeling

```
1  module mux_2x1 (I0,I1,sel,out);
2      input I0;
3      input I1;
4      input sel;
5      output wire out;
6      assign out = sel ? I1 : I0;
7  endmodule
8
```

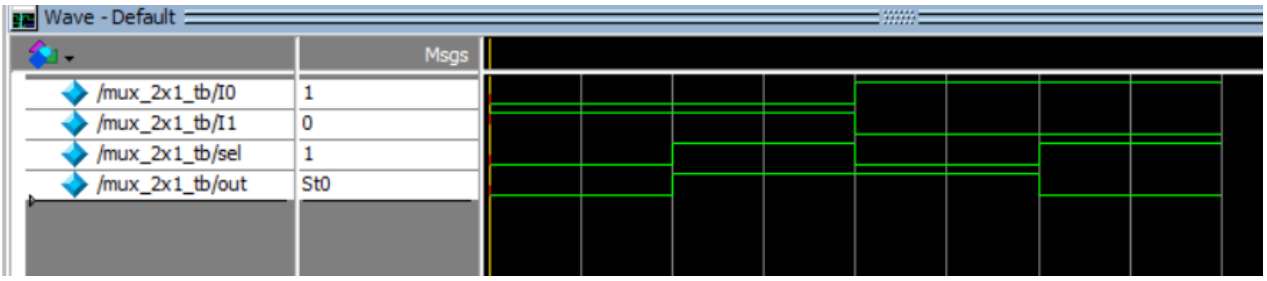
B) Behavioral modeling

```
 1  module mux_2x1(I0,I1,sel,out);
 2  input I0,I1,sel;
 3  output reg out;
 4
 5  always @(*)begin
 6      if(sel)
 7      out=I1;
 8      else
 9      out=I0;
10  end
11  endmodule
12
```

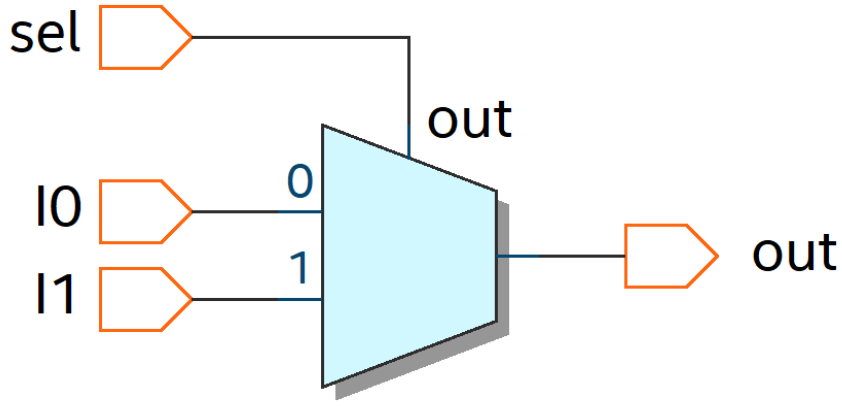
Testbench Code

```
 1  module mux_2x1_tb;
 2      reg I0, I1, sel;
 3      wire out;
 4
 5      mux_2x1 dut (I0,I1,sel,out);
 6
 7      initial begin
 8          $monitor("I0=%b I1=%b sel=%b -> out=%b", I0, I1, sel, out);
 9          I0=0; I1=1; sel=0; #10;
10          I0=0; I1=1; sel=1; #10;
11          I0=1; I1=0; sel=0; #10;
12          I0=1; I1=0; sel=1; #10;
13          $finish;
14      end
15  endmodule
```

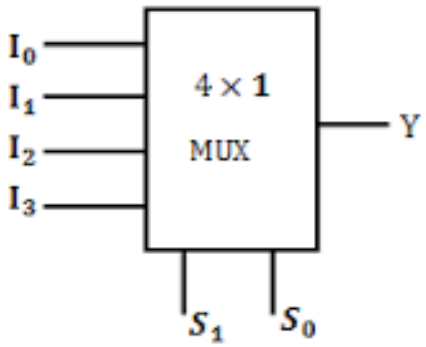
Waveform



📐 Schematic



2) 4x1 MUX



Truth table

S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

🔧 Verilog Code

A) Dataflow modeling

```
module mux_4x1(I,sel,out);
input [3:0]I;
input [2:0]sel;
output out;
assign out = I[sel];
endmodule
```

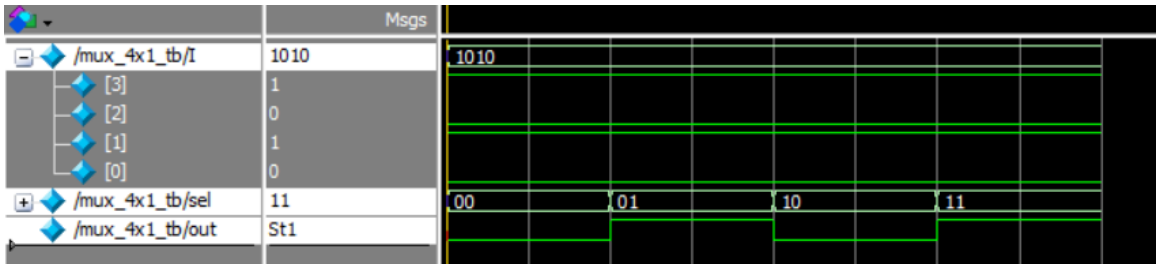
B) Behavioral modeling

```
module mux_4x1 (I,sel,out);
    input [3:0] I;
    input [1:0] sel;
    output reg out;
    always @(*) begin
        case (sel)
            2'b00: out = I[0];
            2'b01: out = I[1];
            2'b10: out = I[2];
            2'b11: out = I[3];
        endcase
    end
endmodule
```

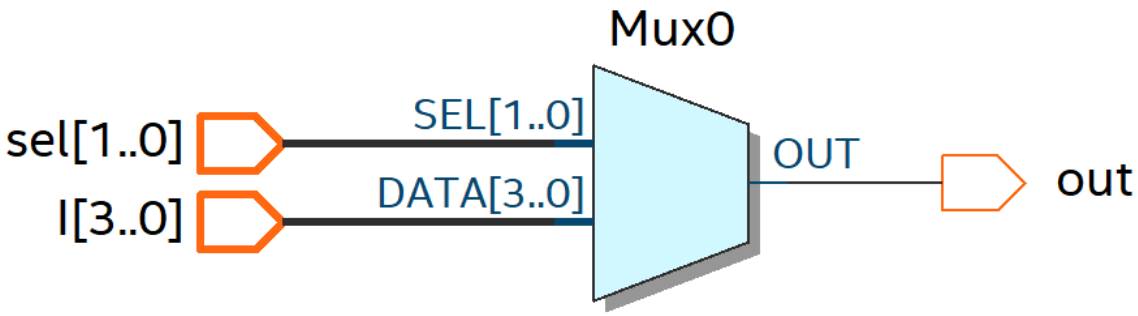
Testbench Code

```
module mux_4x1_tb;
    reg [3:0] I;
    reg [1:0] sel;
    wire out;
    mux_4x1 dut(I,sel,out);
    initial begin
        I = 4'b1010;
        $display("I[0]=%b I[1]=%b I[2]=%b I[3]=%b ",I[0],I[1],I[2],I[3]);
        sel = 2'b00; #10;
        sel = 2'b01; #10;
        sel = 2'b10; #10;
        sel = 2'b11; #10;
        $finish;
    end
endmodule
```

Waveform



📐 Schematic



🛠️ EDA Tools Used

- IntelQuartusPrime
- ModelSim