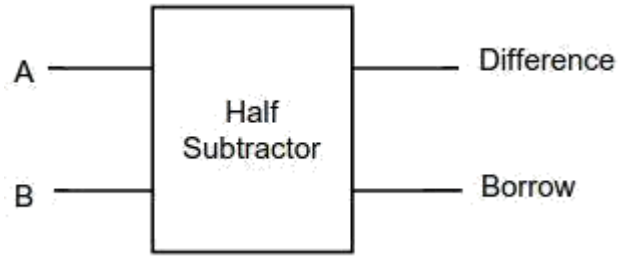
Day 06

Half Subtractor & Full Subtractor in Verilog

1) HALF SUBTRACTOR



Inputs		Outputs	
A	B	Difference	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

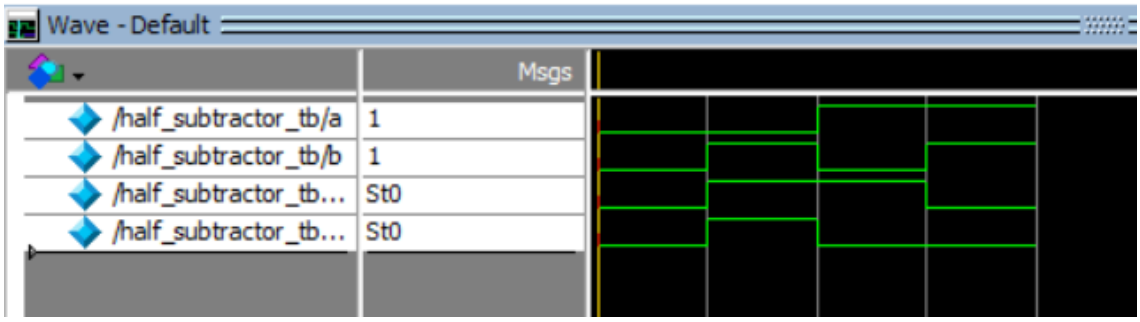
Verilog Code

```
1  module half_subtractor(a, b,diff, borrow);
2      input a, b;
3      output diff, borrow;
4
5      assign diff = a ^ b;
6      assign borrow = ~a & b;
7
8  endmodule
9
```

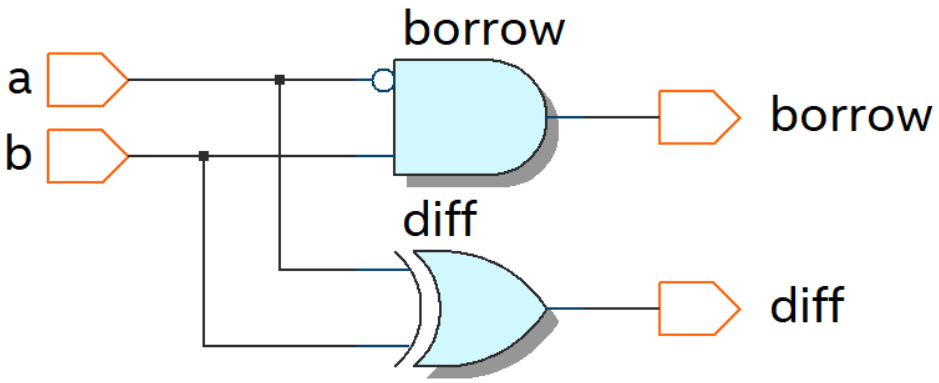
Testbench Code

```
1  module half_subtractor_tb;
2      reg a, b;
3      wire diff, borrow;
4      half_subtractor DUT (a,b,diff,borrow);
5
6      initial begin
7          $monitor($time,"a=%b b=%b => diff=%b borrow=%b", a, b, diff, borrow);
8          a = 0; b = 0; #10;
9          a = 0; b = 1; #10;
10         a = 1; b = 0; #10;
11         a = 1; b = 1; #10;
12         $finish;
13     end
14 endmodule
15
```

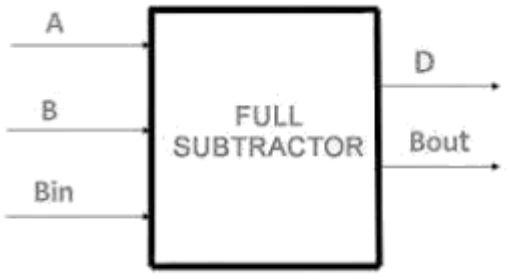
Waveform



Schematic



2) FULL SUBTRACTOR



A	B	B_{in}	D	B_{out}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

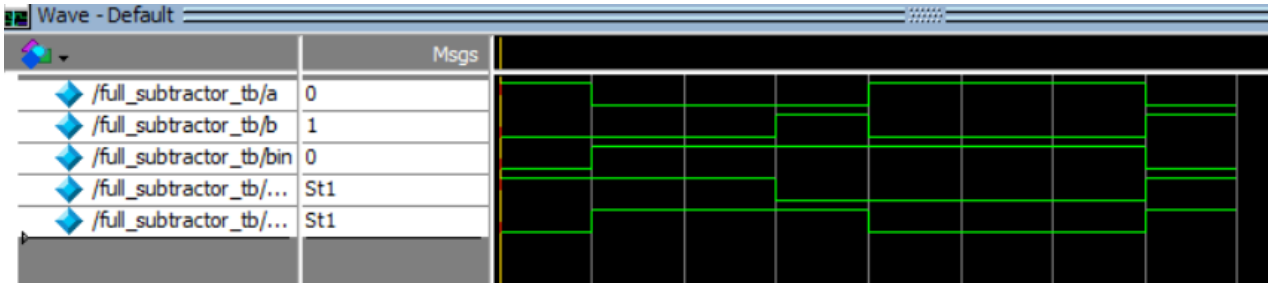
Verilog Code

```
1  module full_subtractor(a, b, bin, diff, borrow);
2      input a, b, bin;
3      output diff,borrow;
4      assign diff =a ^ b ^ bin;
5      assign borrow =(~a & bin)|(~a & b)|(b & bin);
6  endmodule
7
```

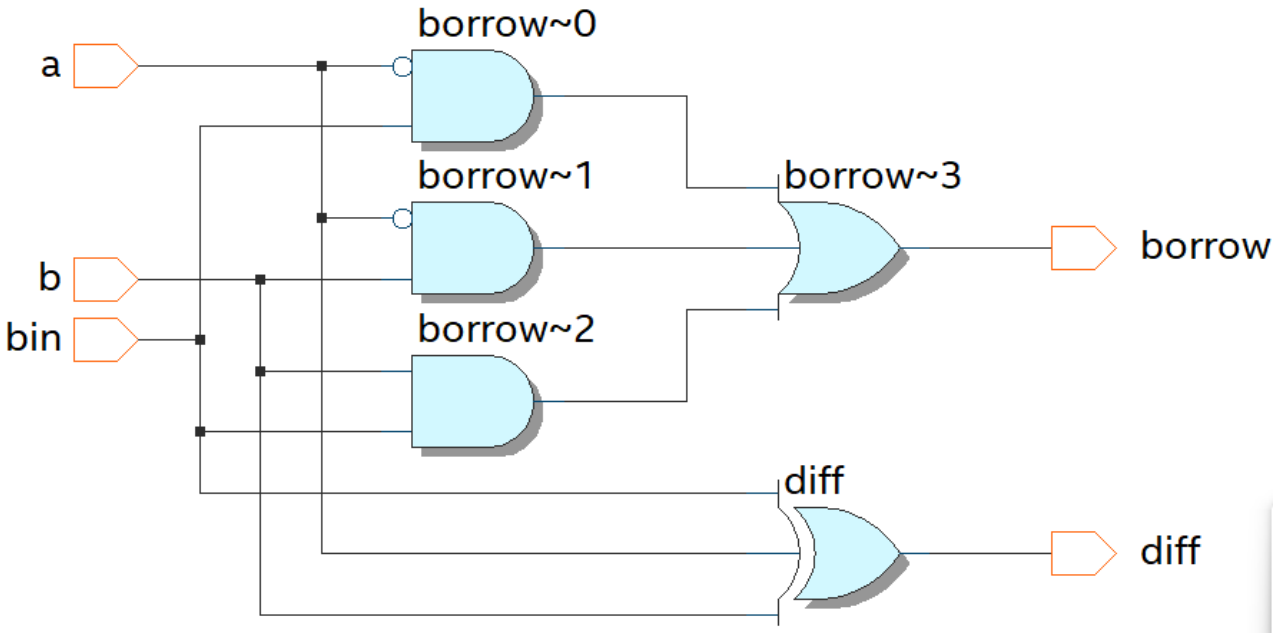
Testbench Code

```
1  module full_subtractor_tb;
2      reg a, b, bin;
3      wire diff, borrow;
4      full_subtractor DUT (a,b,bin,diff,borrow);
5
6      initial begin
7          $monitor("a=%b b=%b bin=%b | diff=%b borrow=%b", a, b, bin, diff, borrow);
8          repeat(8) begin
9              {a, b, bin} = $random;
10             #10;
11         end
12         $finish;
13     end
14 endmodule
```

Waveform



📐 Schematic



🛠️ EDA Tools Used

- IntelQuartusPrime
- ModelSim