Day 08

8-bit ALU in Verilog

8-bit ALU in Verilog

🔧 Verilog Code

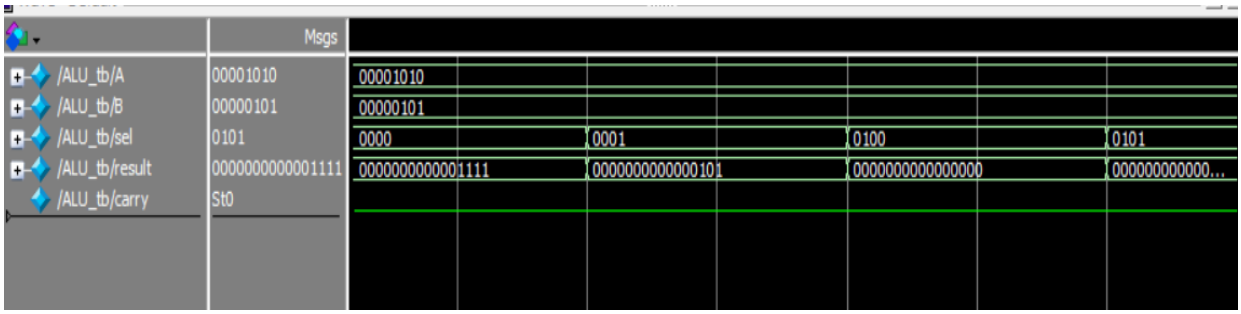
```
1   module ALU(A,B,sel,result,carry);
2   input [7:0]A,B;
3   input [3:0]sel;
4   output reg [15:0]result;
5   output reg carry;
6   always @(*)begin
7
8   result = 0;
9   carry = 0;
10
11  case(sel)
12
13  4'b0000: begin // Addition
14  {carry, result} = A + B;
15  end
16
17  4'b0001: begin // Subtraction
18  {carry, result} = A - B;
19  end
20
21  4'b0010: begin // Multiplication
22  result = A * B;
23  end
24
25  4'b0011: begin // Division
26  if (B != 0) begin
27  result = A / B;
28  end
29  else begin
30  result = 16'hXXXX;
31  end
32  end
33
34  4'b0100: begin // AND
35  result = A & B;
36  end
```

```
4'b0101: begin // OR
result = A | B;
end

4'b0110: begin // XOR
result = A ^ B;
end

4'b0111: begin // NOT A
result = ~A;
end

4'b1000: begin // Left Shift
result = A << 1;
end

4'b1001: begin // Right Shift
result = A >> 1;
end
default: begin
result = 0;
carry = 0;
end
endcase
end

endmodule
```

Testbench Code

```
module ALU_tb;

  reg [7:0] A, B;
  reg [3:0] sel;
  wire [15:0] result;
  wire carry;
  ALU dut(A,B,sel,result,carry);
  initial begin

    A = 8'd10; B = 8'd5; sel = 4'b0000; #10;// Test Addition

    sel = 4'b0001; #10;// Test Subtraction

    sel = 4'b0100; #10;// Test AND

    sel = 4'b0101; #10;// Test OR

    sel = 4'b1000; #10;// Test Left Shift
    $finish;
  end

endmodule
```

Waveform



Schematic

Refer github

EDA Tools Used

- IntelQuartusPrime
- ModelSim