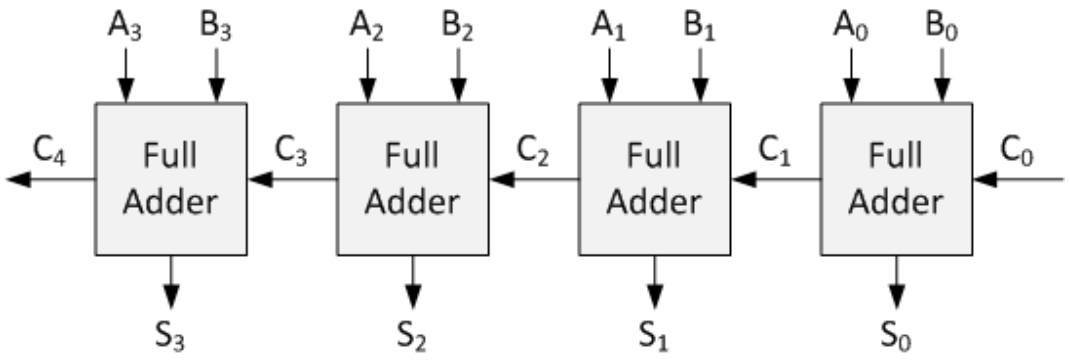
Day 07

4-bit Ripple Carry Adder in Verilog

4-bit Ripple Carry Adder



🔧 Verilog Code

1) Using Structural Modeling

```
1  module full_adder(a,b,cin,sum,cout);
2  input a,b,cin;
3  output sum,cout;
4
5     assign sum = a^b^cin;
6     assign cout = (a&b)| (a&cin) | (b&cin);
7  endmodule
8
9  module ripple_adder(A,B,cin,sum,cout);
10     input [3:0]A,B;
11     input cin;
12     output [3:0]sum;
13     output cout;
14     wire c1,c2,c3;
15
16     full_adder A0 (A[0], B[0], cin,  sum[0], c1);
17     full_adder A1 (A[1], B[1], c1,   sum[1], c2);
18     full_adder A2 (A[2], B[2], c2,   sum[2], c3);
19     full_adder A3 (A[3], B[3], c3,   sum[3], cout);
20 endmodule
21
```

1) Using Dataflow Modeling

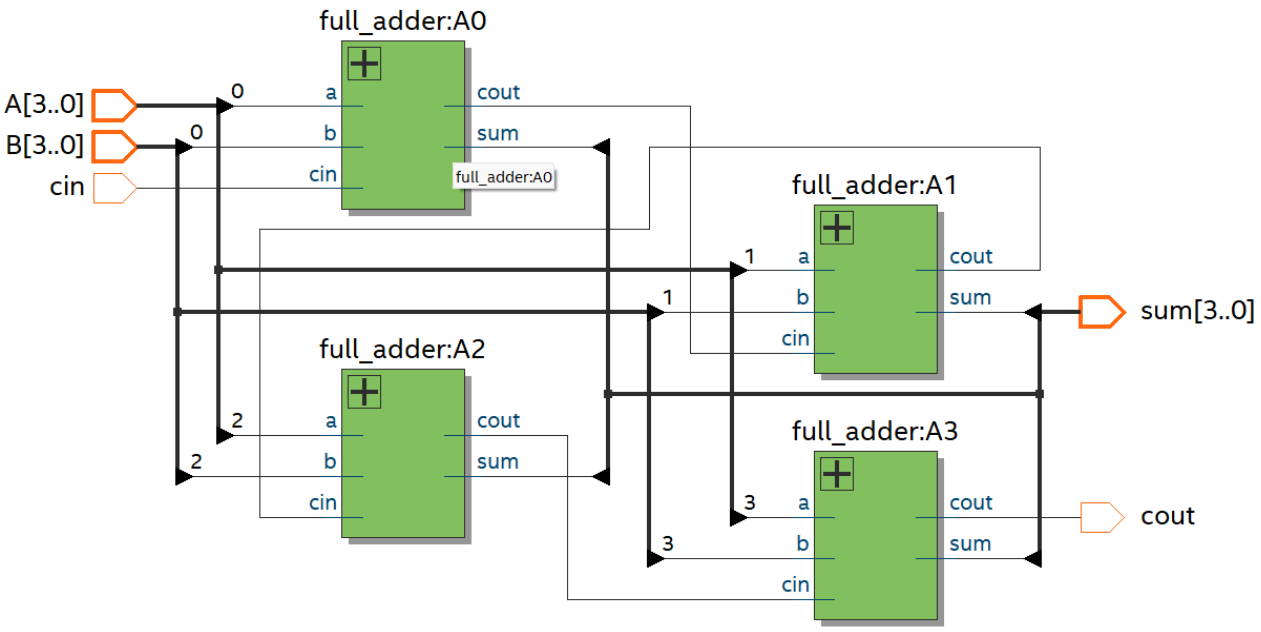
```
1  module ripple_adder(A,B,cin,sum,cout);
2      input [3:0]A,B;
3      input cin;
4      output [3:0]sum;
5      output cout;
6      assign {cout, sum} = A + B + cin;
7  endmodule
```

🧪 Testbench Code

```
1  module ripple_adder_tb;
2      reg [3:0] A, B;
3      reg cin;
4      wire [3:0] sum;
5      wire cout;
6      ripple_adder dut(A,B,cin,sum,cout);
7
8      initial begin
9          $monitor($time," A=%b, B=%b, Cin=%b => Sum=%b, Cout=%b",
10                     A, B, cin, sum, cout);
11         A = 4'b0101; B = 4'b0011; cin = 1; #10;
12         A = 4'b1111; B = 4'b0001; cin = 0; #10;
13         A = 4'b1010; B = 4'b0101; cin = 1; #10;
14         $finish;
15     end
16 endmodule
```

📈 Waveform

Schematic



EDA Tools Used

- IntelQuartusPrime
- ModelSim