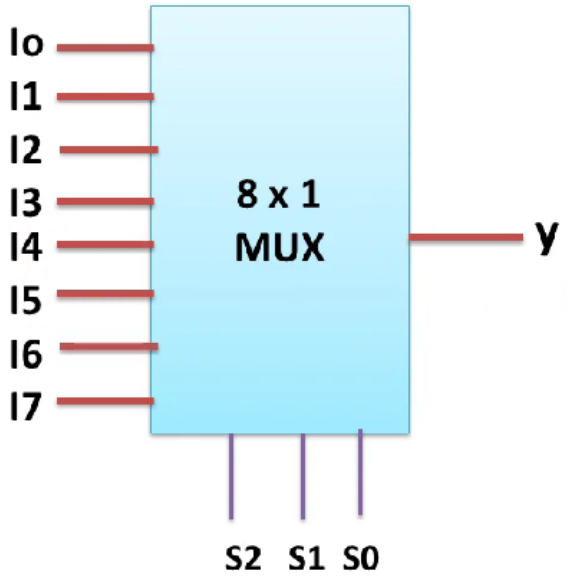
Day 10

8x1 Multiplexer in Verilog

8x1 MUX



S2	S1	S0	Y
0	0	0	I0
0	0	1	I1
0	1	0	I2
0	1	1	I3
1	0	0	I4
1	0	1	I5
1	1	0	I6
1	1	1	I7

Verilog Code

A) Dataflow modeling

```
1  module mux_8x1(I,sel,out);
2      input [7:0] I;
3      input [2:0] sel;
4      output out;
5      assign out = I[sel];
6  endmodule
7
```

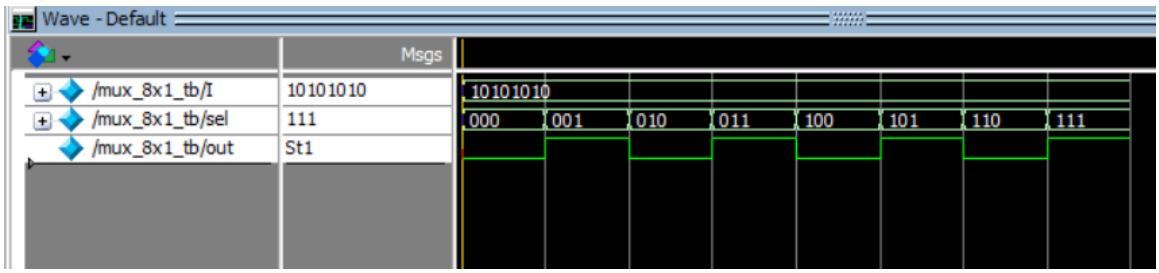
B) Behavioral modeling

```
 1  module mux_8x1(I,sel,out);
 2   input [7:0]I;
 3   input [2:0]sel;
 4   output reg out;
 5   always @(*) begin
 6       case (sel)
 7           3'b000: out = I[0];
 8           3'b001: out = I[1];
 9           3'b010: out = I[2];
10           3'b011: out = I[3];
11           3'b100: out = I[4];
12           3'b101: out = I[5];
13           3'b110: out = I[6];
14           3'b111: out = I[7];
15       endcase
16   end
17  endmodule
```

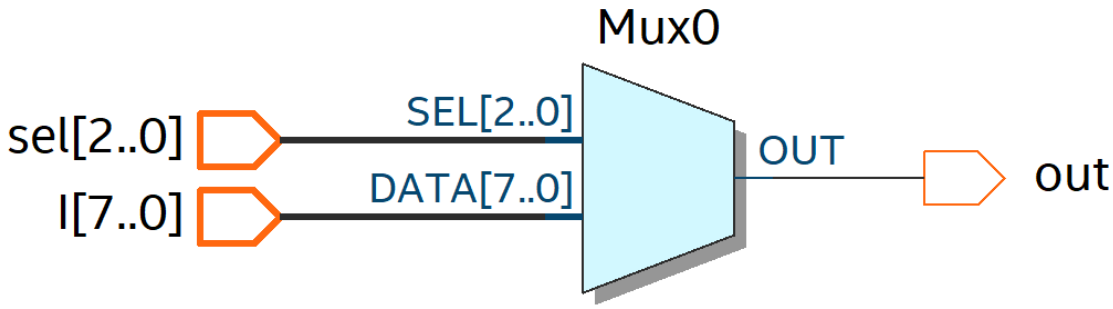
Testbench Code

```
 1  module mux_8x1_tb;
 2  reg [7:0] I;
 3  reg [2:0] sel;
 4  wire out;
 5     mux_8x1 dut(I,sel,out);
 6     initial begin
 7       I = 8'b10101010;
 8       sel = 3'b000; #10;
 9       sel = 3'b001; #10;
10       sel = 3'b010; #10;
11       sel = 3'b011; #10;
12       sel = 3'b100; #10;
13       sel = 3'b101; #10;
14       sel = 3'b110; #10;
15       sel = 3'b111; #10;
16       $finish;
17     end
18  endmodule
```

Waveform



Schematic



EDA Tools Used

- IntelQuartusPrime
- ModelSim