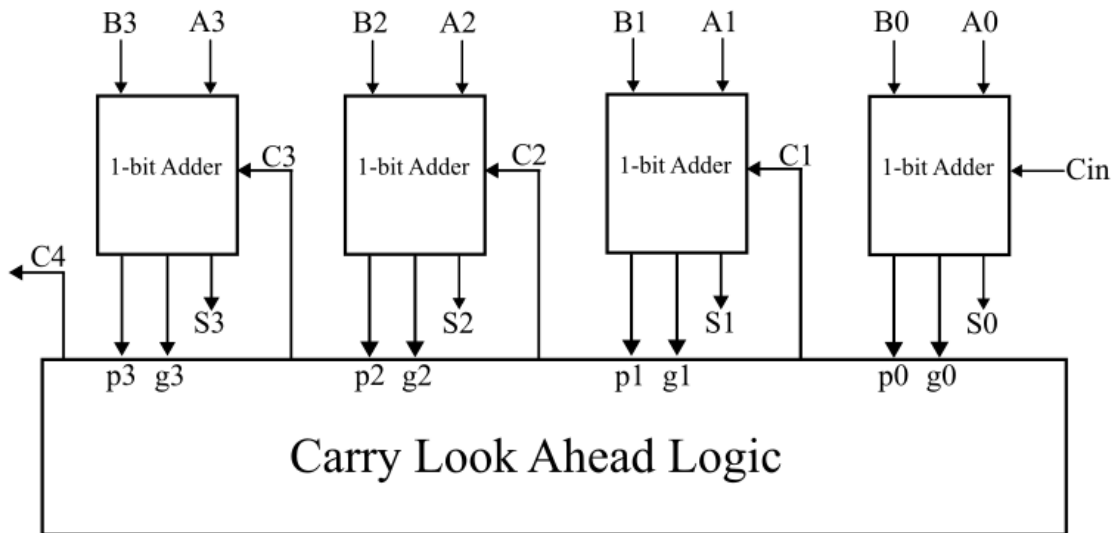


Day 12

4-bit Carry Look-Ahead Adder (CLA) in Verilog

Circuit Diagram :



Verilog Code

```
1 module carryLook_ahead(A,B,Cin,Sum,Cout);
2   input [3:0]A, B;
3   input Cin;
4   output [3:0]Sum;
5   output Cout;
6   wire [3:0]G, P;
7   wire [4:0]C;
8
9   assign G = A & B;
10  assign P = A ^ B;
11
12  assign C[0] = Cin;
13  assign C[1] = G[0] | (P[0] & C[0]);
14  assign C[2] = G[1] | (P[1] & G[0]) | (P[1] & P[0] & C[0]);
15  assign C[3] = G[2] | (P[2] & G[1]) | (P[2] & P[1] & G[0]) | (P[2] & P[1] & P[0] & C[0]);
16  assign C[4] = G[3] | (P[3] & G[2]) | (P[3] & P[2] & G[1]) | (P[3] & P[2] & P[1] & G[0]) | (P[3] & P[2] & P[1] & P[0] & C[0]);
17  assign Cout = C[4];
18  assign Sum = P ^ C;
19
20 endmodule
```

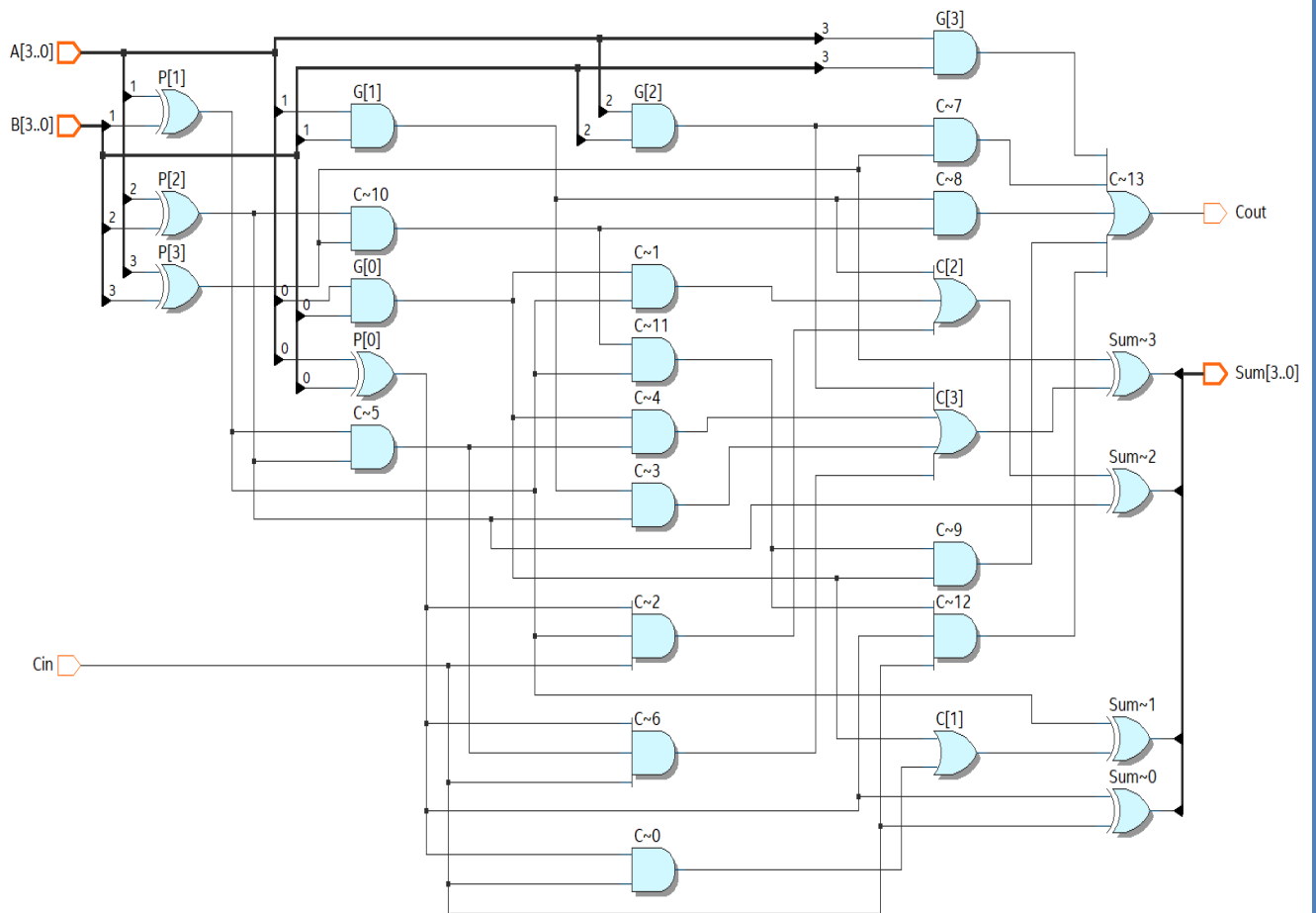
Testbench Code

```
1 module tb_carryLook_ahead;
2     reg [3:0] A, B;
3     reg Cin;
4     wire [3:0] Sum;
5     wire Cout;
6
7     carryLook_ahead dut (A,B,Cin,Sum,Cout);
8
9     initial begin
10         A = 4'b0001; B = 4'b0010; Cin = 0; #10;
11         A = 4'b0101; B = 4'b0011; Cin = 1; #10;
12         A = 4'b1111; B = 4'b0001; Cin = 0; #10;
13         A = 4'b1010; B = 4'b0101; Cin = 1; #10;
14         A = 4'b1111; B = 4'b1111; Cin = 1; #10;
15     end
16 endmodule
17
```

Waveform

Wave - Default									
		Msgs							
+	/tb_carryLook_ahe...	-No Data-	0001	0101	1111	1010	1111		
	/tb_carryLook_ahe...	-No Data-	0010	0011	0001	0101	1111		
	/tb_carryLook_ahe...	-No Data-							
	/tb_carryLook_ahe...	-No Data-	0011	1001	0000	0000	1111		
	/tb_carryLook_ahe...	-No Data-							

Schematic



EDA Tools Used

- IntelQuartusPrime
- ModelSim

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