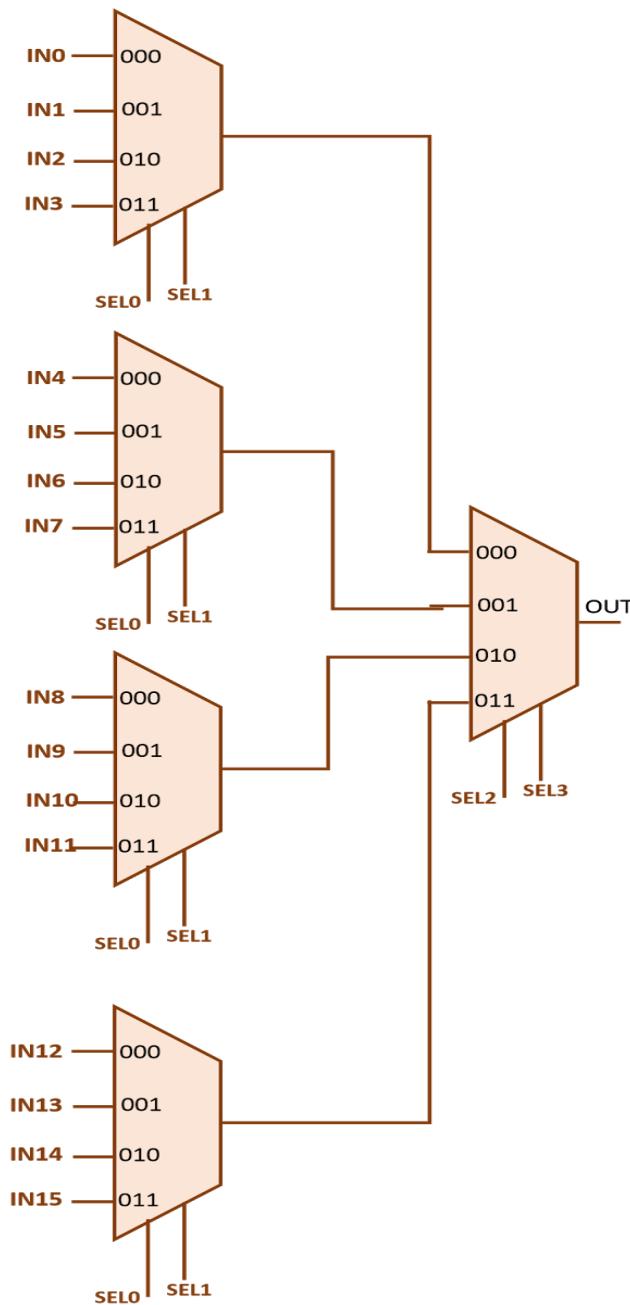


Day 11

16x1 Multiplexer using 4x1 MUX in Verilog

16x1 MUX



 [Verilog Code](#)

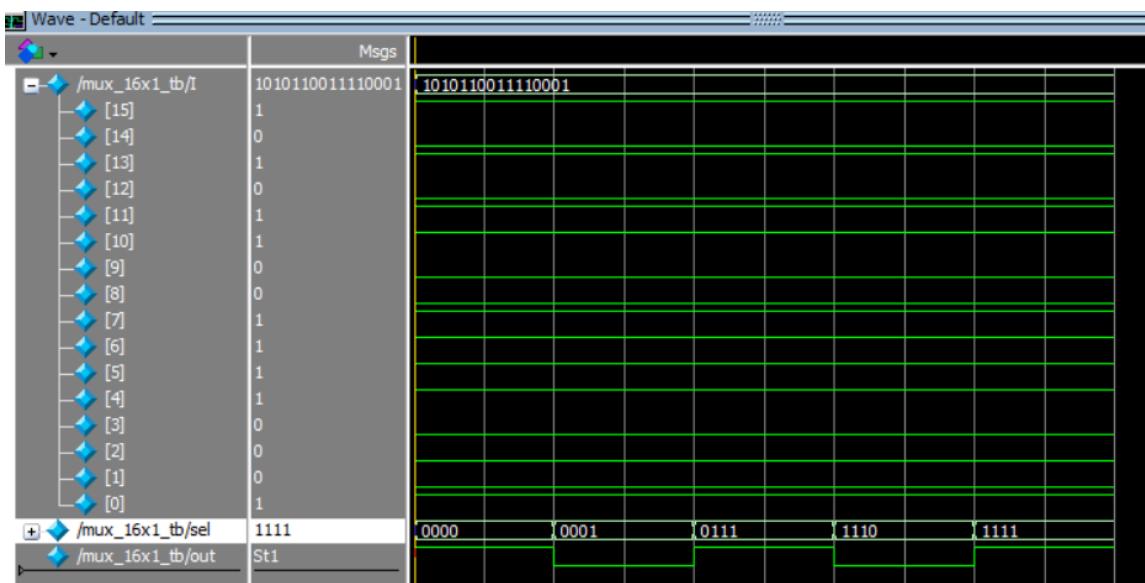
Using 4x1 MUX Modules

```
1 module mux_4x1(I,sel,out);
2   input [3:0]I;
3   input [1:0]sel;
4   output reg out;
5   always @(*) begin
6     case(sel)
7       2'b00: out=I[0];
8       2'b01: out=I[1];
9       2'b10: out=I[2];
10      2'b11: out=I[3];
11    endcase
12  end
13 endmodule
14
15 module mux_16x1(I,sel,out);
16   input [15:0]I;
17   input [3:0]sel;
18   output out;
19   wire [3:0]w;
20   mux_4x1 m0(I[3:0],sel[1:0],w[0]);
21   mux_4x1 m1(I[7:4],sel[1:0],w[1]);
22   mux_4x1 m2(I[11:8],sel[1:0],w[2]);
23   mux_4x1 m3(I[15:12],sel[1:0],w[3]);
24   mux_4x1 m4(w[3:0],sel[3:2],out);
25 endmodule
26
```

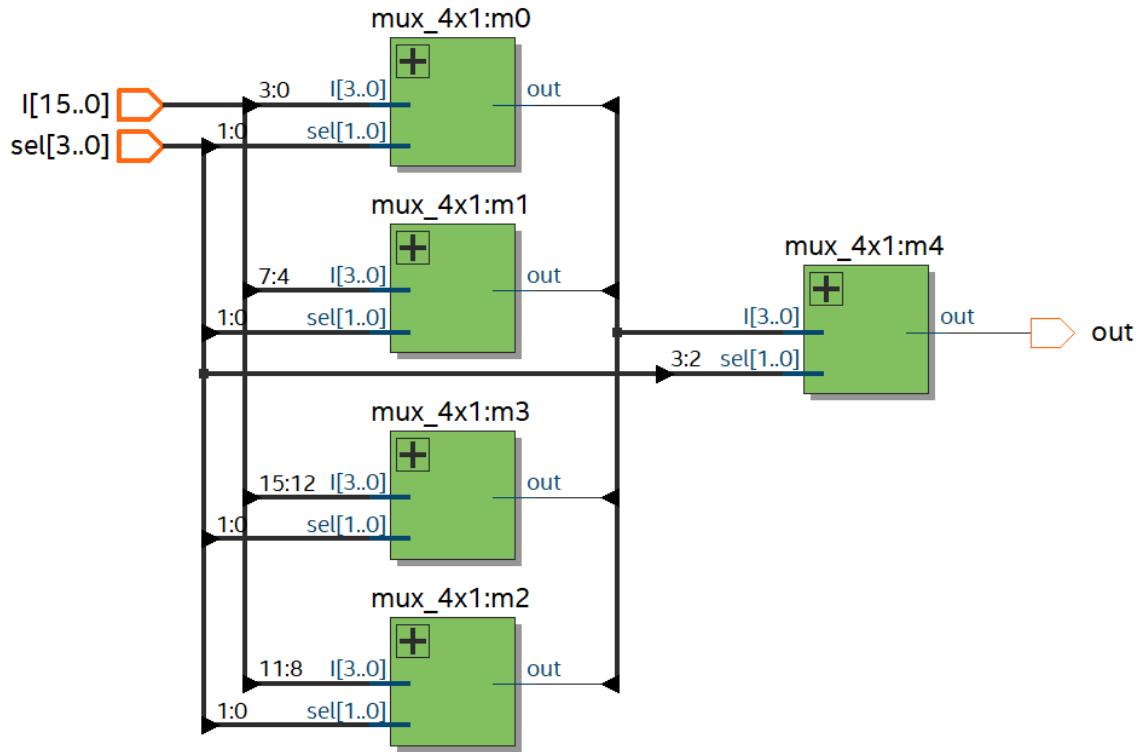
Testbench Code

```
1 module mux_16x1_tb;
2 reg [15:0] I;
3 reg [3:0] sel;
4 wire out;
5
6 mux_16x1 DUT (I,sel,out);
7
8 initial begin
9   $monitor($time," sel=%b out=%b", sel, out);
10  I = 16'b1010_1100_1111_0001;
11  sel = 4'b0000; #10; //for i0
12  sel = 4'b0001; #10; //for i1
13  sel = 4'b0111; #10; //for i7
14  sel = 4'b1110; #10; //for i14
15  sel = 4'b1111; #10; //for i15
16  $finish;
17 end
18 endmodule
19
```

Waveform



Schematic



EDA Tools Used

- IntelQuartusPrime
- ModelSim