ROSH

NPTEL COA ANSWERS OF WEEK-1

1. Instruction fetch → Instruction decode → Operand fetch → Execute → Result store {OPTION - C}

2. The least significant byte is stored at the smallest address. {OPTION – A}

3. It contains the address of the next instruction to be fetched {OPTION -B}

4. Increase in the average number of cycles per instruction {OPTION -D}

5. 15 bits {OPTION -D}

6. 16 {OPTION – B}

7. 2.4

8. 1.714 {ACCURACY HAI BAAKI PIC DEKH LO}

JOIN GROUP FOR NEXT WEEK ASSIGNMENT ANSWERS

https://chat.whatsapp.com/JEWbyHw5ZXC4ssZ3aycaHh

CONTACT FOR ISSUE = 8595613178

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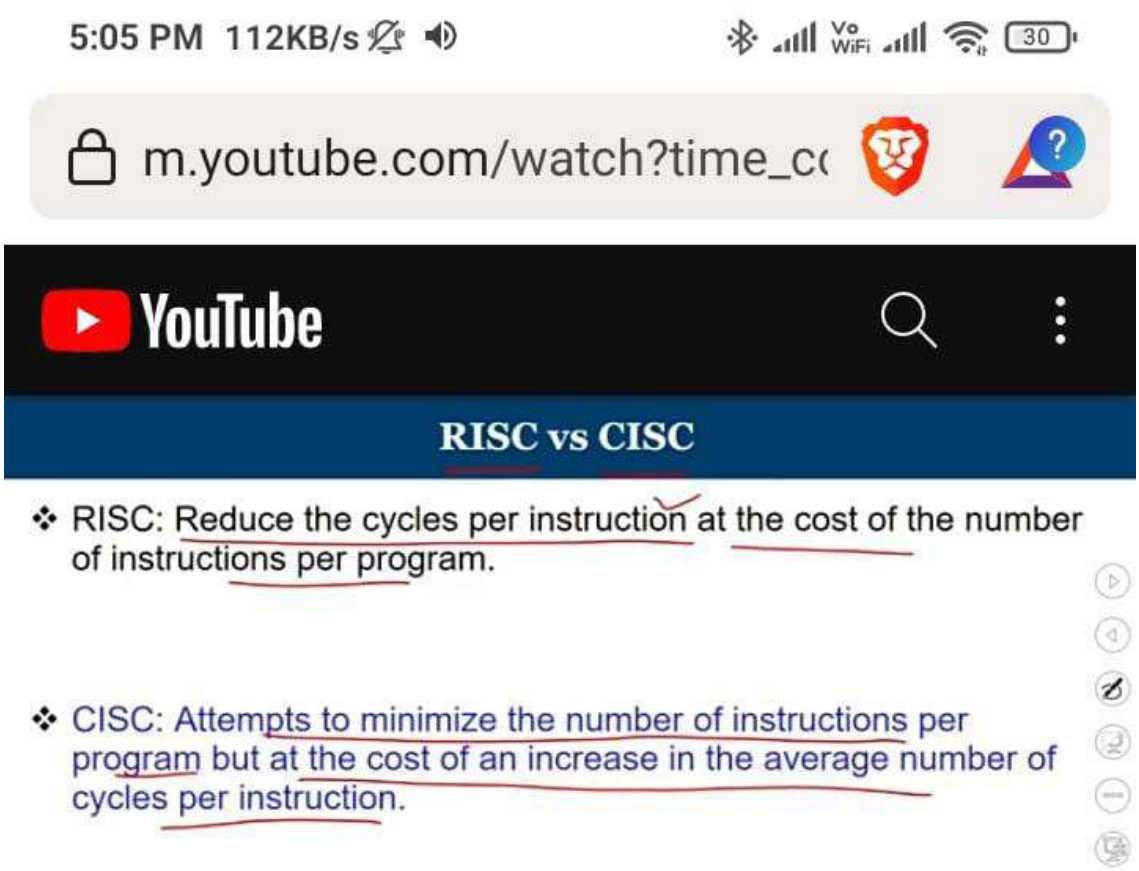
5:05 PM 112KB/s
m.youtube.com/watch?time_c
YouTube
RISC vs CISC
RISC: Reduce the cycles per instruction at the cost of the number of instructions per program.
CISC: Attempts to minimize the number of instructions per program but at the cost of an increase in the average number of cycles per instruction.

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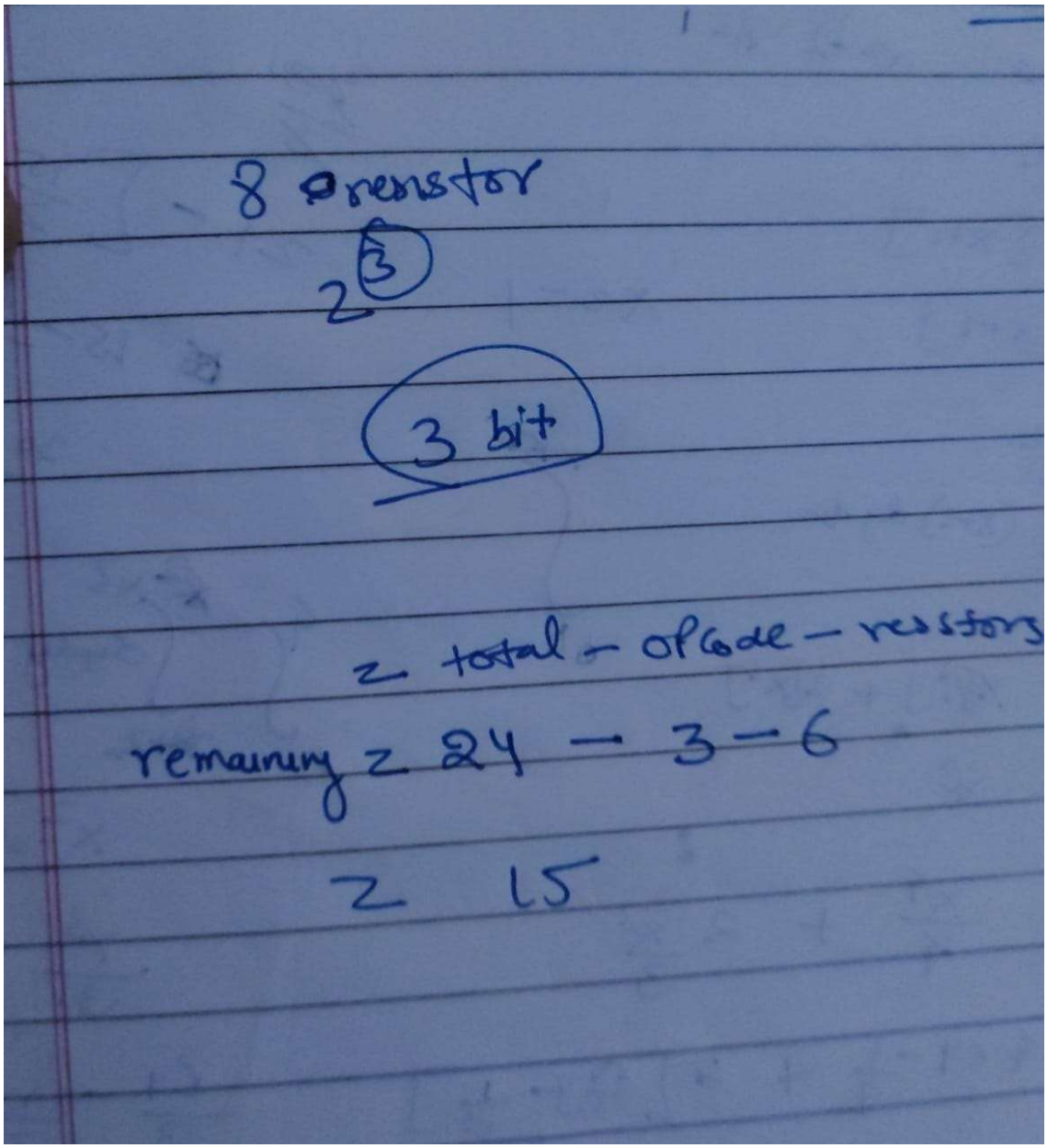

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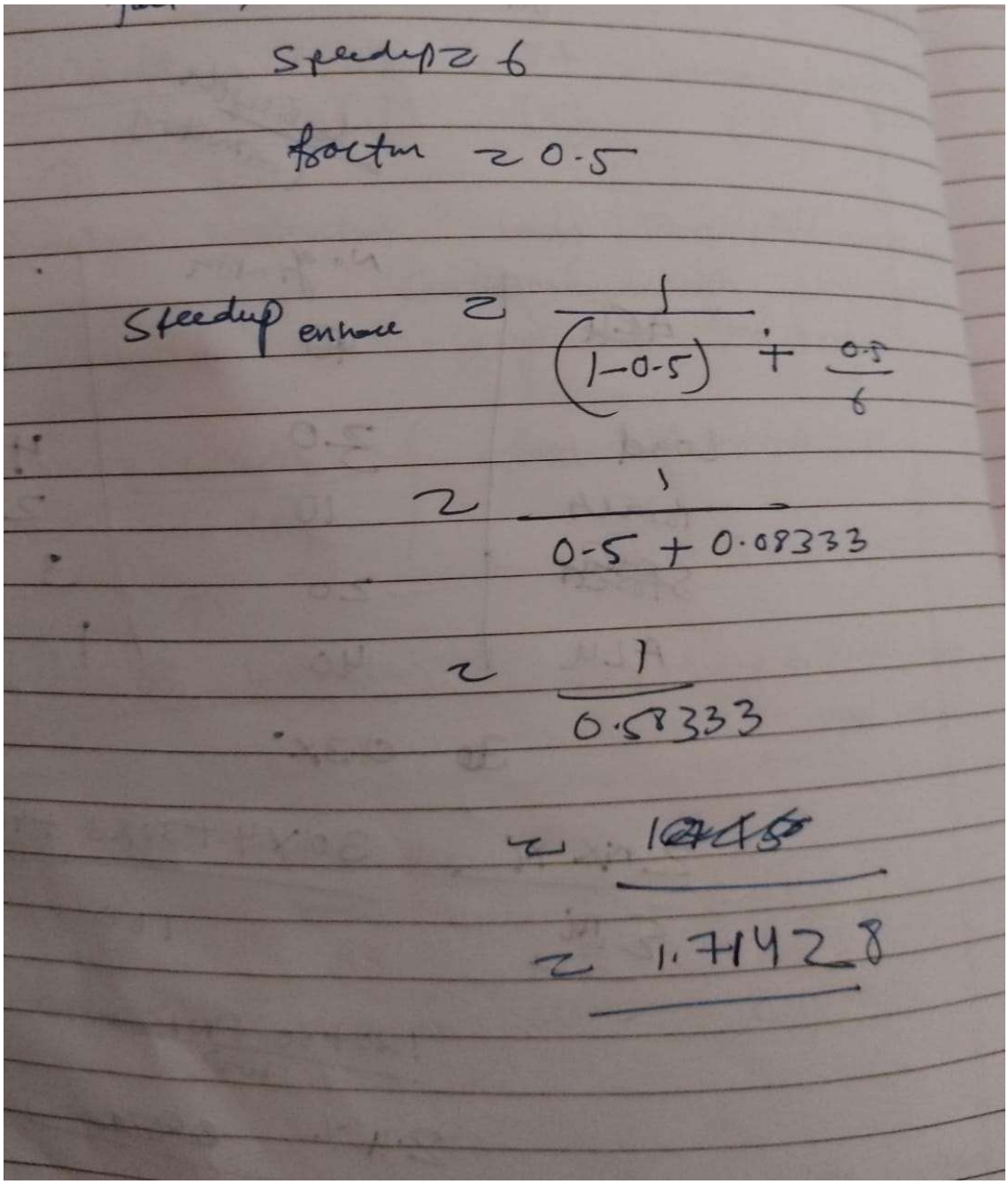
Speedup = 6
fractn = 0.5
Speedup enhance = 1 / ((1-0.5) + 0.5/6)
= 1 / 0.5 + 0.08333
= 1 / 0.58333
= 1.71428

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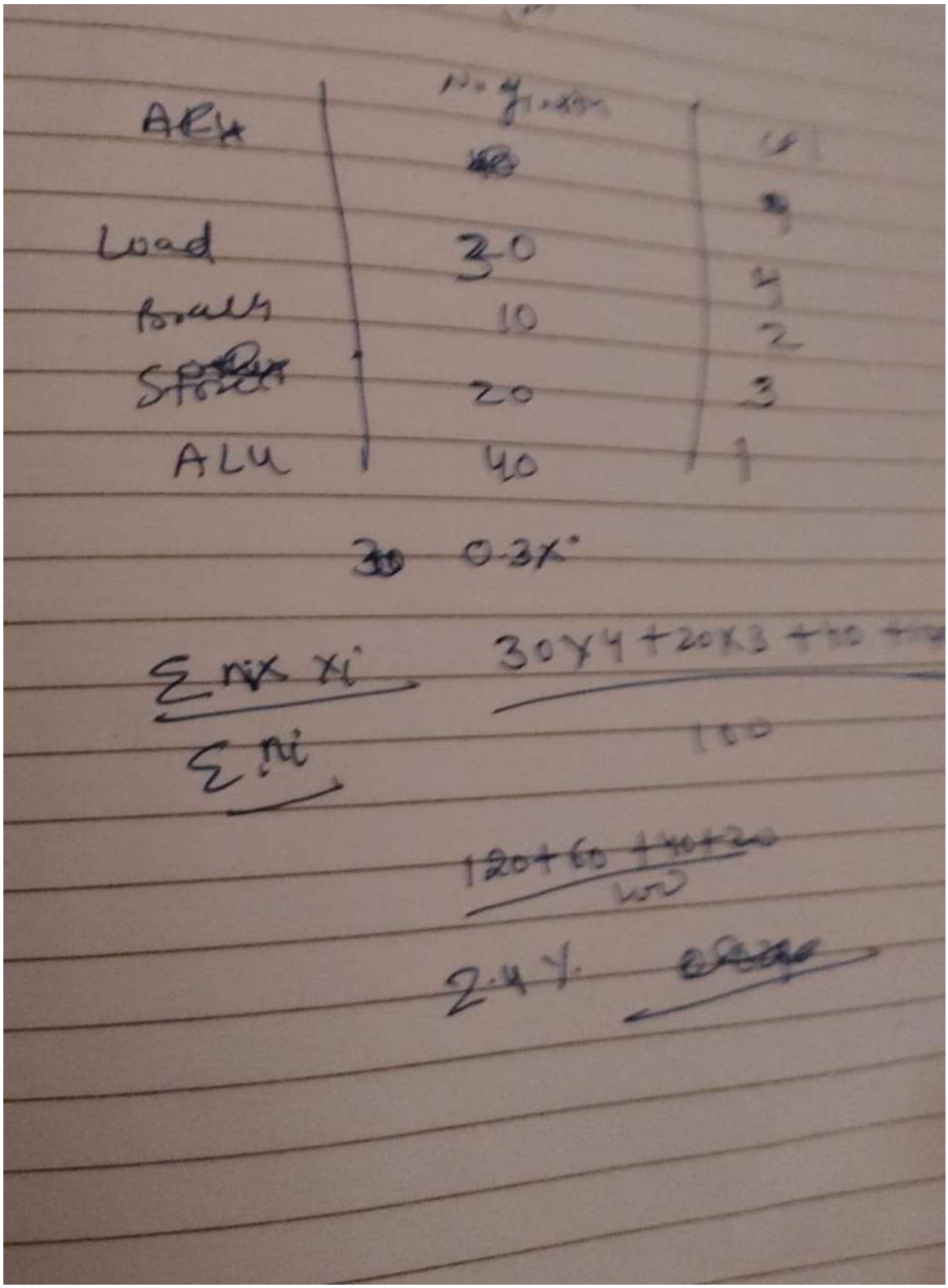
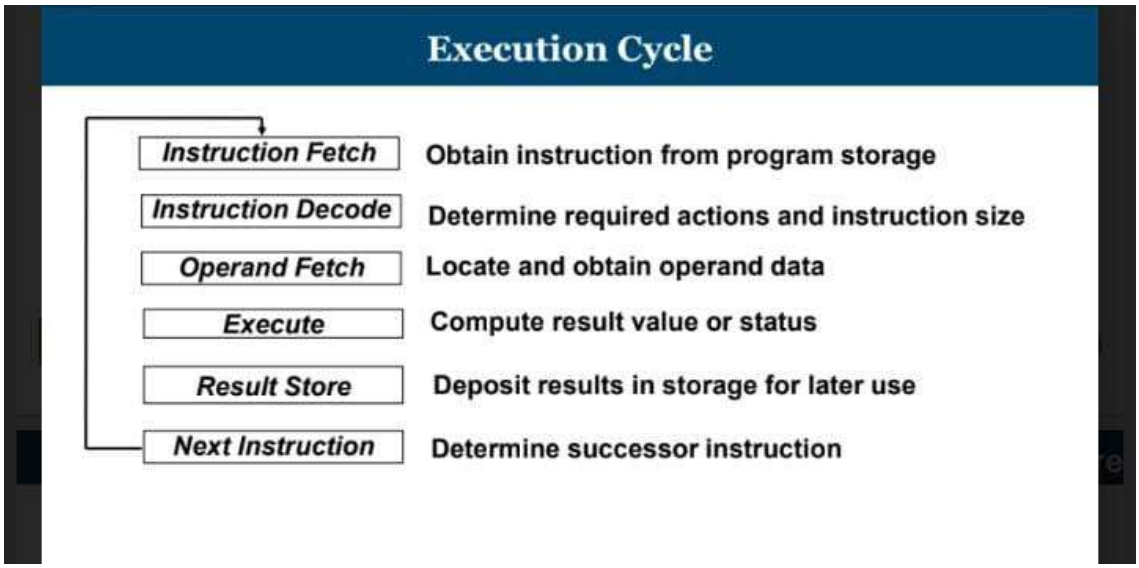


ROSH


Execution Cycle
Instruction Fetch
Obtain instruction from program storage
Instruction Decode
Determine required actions and instruction size
Operand Fetch
Locate and obtain operand data
Execute
Compute result value or status
Result Store
Deposit results in storage for later use
Next Instruction
Determine successor instruction