Printed Pages: 02 University Roll No | | | | | | | | |

End Term Examination Session 2016-17
B.Tech. I Year, I Semester
Electronics Engineering (ECE-1001)

Time –2 ½ hours **Max Marks: 40**

SECTION- A

Note: Attempt all questions **(1x16)**

I. Write mass action law?
II. Write the equation for diffusion current in a semiconductor.
III. Write the expression for a current in pn junction diode.
IV. Draw the V-I characteristic of a Zener diode and show in which region it works as a voltage regulator?
V. Define PIV? Write PIVs for a full wave center tap rectifier.
VI. What is a function of a clamper? What different electrical components do you require for a implementing a clamper circuit?
VII. If a BJT has α=0.98. Determine the value of β.
VIII. Write any two applications of a transistor?
IX. Draw the circuit diagram of a npn BJT in common base configuration for forward active operation.
X. Why FET is called a voltage controlled device?
XI. Define trans-conductance of FET?
XII. Sketch the construction of an n channel enhancement type MOSFET. Indicate clearly drain, gate and source regions.
XIII. Write truth table of EX-OR Gate.
XIV. Subtract using 2's complement method
$(1011)_2$- $(0101)_2$
XV. Write the expression for voltage gain in an inverting amplifier?
XVI. What should be the ideal values of input resistance and output resistance for an OP-AMP?

SECTION- B

Note: Attempt any four questions **3x4=12**

I. Sketch the circuit diagram of am non-inverting OP-AMP amplifier.Dervie the expression for its gain.

II. Discuss the concept of virtual short in an OP-AMP with a neat sketch.

III. Implement AND, OR and NOT gate using NAND Gates only.

IV. Express the following as sum of minterms.

$F(A,B,C,D) = \bar{B}D + \bar{A}D + BD$

V. Simplify the given boolean expression : $xy + x\bar{y} + \bar{x}y$

SECTION- C

Note: Attempt any three questions **4x3=12**

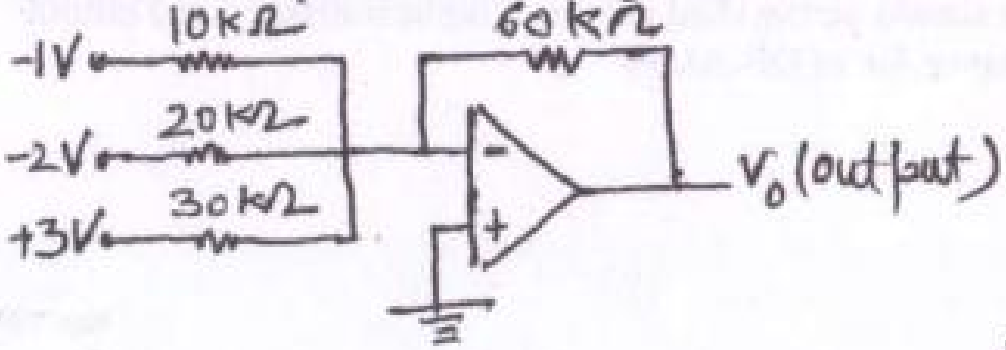
I. Draw the circuit of OP-AMP based integrator. Derive the expression for its output. What will be the output of integrator if it is subject to a square input?

II. State and prove Demorgan's theorem.

III. Simplify the given Boolean expression using k-map and implement the simplified expression with basic gates:

$F(x,y,z) = \sum(0,2,3,6,7)$

IV. Calculate the output of the following circuit.



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End Term Examination, Even Semester 2016-17

B. Tech., I-Year, II-Semester

ECE 1001: Electronics Engineering

Time: 2½ Hours **Max. Marks: 40**

Section-A

Note: Attempt All Questions. **(1x16=16)**

I. Draw energy band diagrams for n-type and p-type semiconductor materials.

II. Define mass-action law.

III. Determine the diode current at 20 ^{0}C for a Si diode with reverse saturation current (I_S) of 50 nA and an applied forward bias of 0.6 V.

IV. Draw I-V characteristics for Zener diode.

V. What does temperature effect on reverse saturation current?

VI. Draw circuit network of Centre-tapped full wave rectifier with input-output waveforms.

VII. Differentiate between BJT and MOSFET.

VIII. Arrange emitter, base and collector of BJT in descending order with respect to:

(a) Doping and (b) Size

IX. Determine the stability factor $S(V_{BE})$ andΔI_C;due to change in temperature from 25 ^{0}C to 100 ^{0}C in a BJT for the fixed bias arrangement with R_B=240 KΩ and β = 100. (given: V_{BE1} = 0.65V at 25 ^{0}C andV_{BE2} = 0.98V at 100 ^{0}C)

X. Briefly explain voltage divider bias for BJT.

XI. Define Pinch-off in FET devices.

XII. If $I_D = I_{DSS}/4$, find V_{GS} at $V_P = -4$ V.

XIII. What is virtual ground in Op-Amp?

XIV. Define slew rate.

XV. Convert $(2AC5.D)_{16}$ to Octal.

XVI. Perform the subtraction using 2's complement:

(a) 11010 – 1101 (b) 100 – 101100

Section-B

Note: Attempt Any Four Questions. **(3x4=12)**

I. Reduce the following Boolean expressions using Boolean postulates:

(a) $\overline{[(\overline{C.D}) + A]} + A + C.D + A.B$

(b) $A.B.C + \bar{A}.\bar{B}.C + \bar{A}.B.C + A.B.\bar{C} + \bar{A}.\bar{B}.\bar{C}$

II. Define CMRR in Op-Amp. Determine the output voltage of an Op-Amp for input voltages of $V_{i1} = 210\ \mu V$ and $V_{i2} = 150\ \mu V$. The amplifier has a differential gain of $A_d = 5000$ and the value of CMRR is: (a) 300 and (b) 2×10^5.

III. Explain Op-Amp as inverting amplifier. Also derive respective expressions.

IV. Simplify the functions T_1 and T_2 to a minimum no. of literals for the given inputs A, B and C as shown in Table 1.

Table 1

Input	A	0	0	0	0	1	1	1	1
	B	0	0	1	1	0	0	1	1
	C	0	1	0	1	0	1	0	1
Output	T_1	1	1	1	0	0	0	0	0
	T_2	0	0	0	1	1	1	1	1

V. Draw and explain the block diagram of operational amplifier with its characteristics.

Section-C

Note: Attempt Any Three Questions. **(4x3=12)**

I. Explain Op-Amp as subtractor amplifier. Calculate the output voltage of an Op-Amp summing amplifier for the following sets of voltages and resistors considering the feedback resistance of 2 MΩ for each set.

(a) $V_1 = +1$ V, $V_2 = +2$ V, $V_3 = +3$ V, $R_1 = 500$ KΩ, $R_2 = 1$ MΩ, $R_3 = 1.5$ MΩ

(b) $V_1 = +3$ V, $V_2 = -1.5$ V, $V_3 = +2$ V, $R_1 = 250$ KΩ, $R_2 = 800$ KΩ, $R_3 = 2.5$ MΩ

II. What is input bias current in Op-Amp? Calculate V_o in the circuit as shown in Fig. 1:

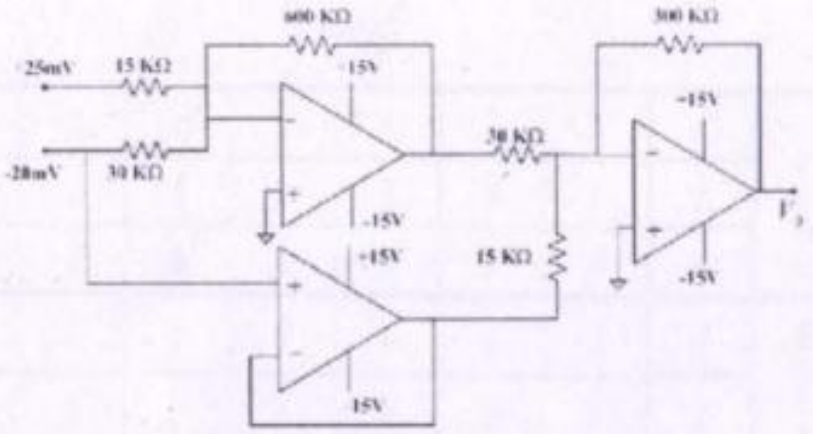

Fig. 1

III. (a) Why are NAND and NOR gates called universal gates? Design Ex-OR using NAND gates only.

(b) Simplify the following Boolean function using K-map.

F(w,x,y,z) = (1, 3, 4, 7, 11, 12, 15) and don't care conditions: d(w,x,y,z) = (0, 2, 6)

IV. (a) Simplify the following Boolean expressionin canonical forms(SOP and POS):

$$\bar{w}.y.\bar{z} + v.\bar{w}.\bar{z} + v.\bar{w}.x + \bar{v}.w.z + \bar{v}.\bar{w}.\bar{y}.\bar{z}$$

(b) Implement the following function with NOR and NAND gates:

$$A.\bar{B} + \bar{C}.\bar{D} + \bar{A}.C.\bar{D} + D.\bar{C}.(A.B + \bar{A}.\bar{B}) + D.B.(A.\bar{C} + \bar{A}.C)$$

End-Term Examination

Odd-Semester, 2017-18

Program: B.Tech **Year:** I

Subject: Electronics Engineering **Subject Code:** ECE-1001

Time: 3 Hrs **Maximum Marks:** 50

Section-A

Note: Attempt ALL questions. **35 marks**

Q1) If a sample of intrinsic Si at 300 K is doped with acceptor impurity such that hole concentration becomes 2×10^{20} /m^3, calculate

(a) Concentration of electrons in extrinsic Si

(b) Conductivity of extrinsic Si.

What is the type of extrinsic Si? (5)

Q2) Define PIV for a rectifier circuit. Find and compare the PIV of half wave, full wave and bridge rectifier circuits (5)

Q3) (a) An FET is called voltage controlled device. Justify the statement? (3)

(b) When an FET is said to be in the saturation region? (2)

Q4) Draw the circuit of emitter bias arrangement. What is the main advantage of the emitter bias arrangement over fixed bias arrangement? (5)

Q5) (a) Convert the hexadecimal $(8F6)_{16}$ to a decimal number (2)

(b) Find $(11010110)_2 - (01000101)_2$ using 2's complement (2)

(c) Write the truth table of XOR Gate (1)

Q6) (a) List the ideal characteristics of an OPAMP (2)

(b) Explain the virtual ground concept in OPAMP (3)

Q7) Implement AND, OR and NOT gate using NOR gates only (5)

Section-B

'Note: Attempt ALL questions. **15 marks**

Q1) State and Prove De-Morgan's law for two variables using truth table method (2)

Q2) Define CMRR. What should be its ideal value? What is its significance? (2)

Q3) Simplify $Y = A\bar{B}C + ABC$ and draw the logic circuit for simplified expression using basic gates (2)

Q4) Draw the circuit of OPAMP as an integrator and derive the expression for its output (3)

Q5) Express f in canonical SOP form.

$$f = AB + A\bar{C} + C + AD + A\bar{B}C + ABC \quad (3)$$

Q6) Minimize the following expression using K-map.

$$f(A,B,C,D) = \sum m(0, 3, 5, 6, 9, 10, 12, 15) \quad (3)$$

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End Term Examination, Odd Semester, 2018-19

B. Tech., First Year, First Semester

BECG 0001: Electronics Engineering

Time: 3 Hour | Max Marks: 50

SECTION- A

Note: Attempt all questions **35 Marks**

I. (a) Draw the block diagram of regulated power supply. (2)

(b) Draw the p-n junction diode characteristics. Determine the diode current at 25°C for a silicon diode with Is=50nA and an applied forward bias of 0.6 V. (3)

II. (a) Classify the types of resistances present in diode? Derive their expression. (3)

(b) In a Full wave rectifier using four diodes the load resistance is 7500Ω, the input voltage available has a maximum value of 20V. Find the average and rms value of output voltage. (2)

III. Explain the working of n-channel JFET by drawing the drain and transfer characteristics. (5)

IV. Determine I_B, I_C, V_{CE}, V_C and V_E for the circuit shown in Fig 1(β=50).

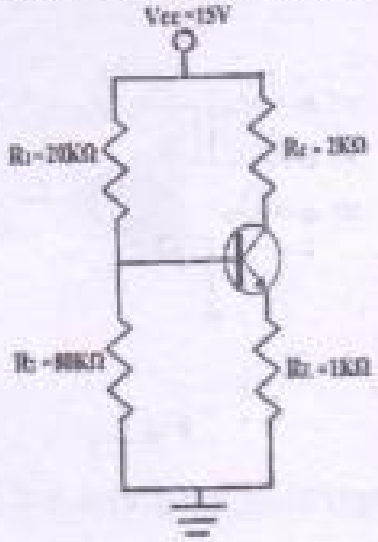


Fig 1. (5)

V. (a) List the ideal characteristics of op-amp. (3)

(b) Explain virtual ground concept in OPAMP (2)

VI. Simplify the following function using Boolean algebra. Implement the simplified function using basic gates and only NAND gate.
$F(A, B,C)=A'B+BC'+BC+AB'C'$ (5)

VII. Simplify the following function using K-amp and implement the simplified function using only NOR gate.
$f=\Sigma(0,1,3,5,9,12)+\Sigma d(2,4,6,7)$ (5)

SECTION- B

Note: Attempt all questions **15 Marks**

I. Find the maxterms and minterms for the following function
$F=(A+B)(B+C)$ (2)

II. Solve the following $(85.36)_{10}+(A9.2)_{16}+(25.64)_8=(?)_2$ (3)

III. Find the output voltage for the circuit shown in Fig. 2? (3)
Given R1=5KΩ, R2=15KΩ, R3=10KΩ, Rf=20KΩ, V1=1mV, V2=3mV and V3=5mV

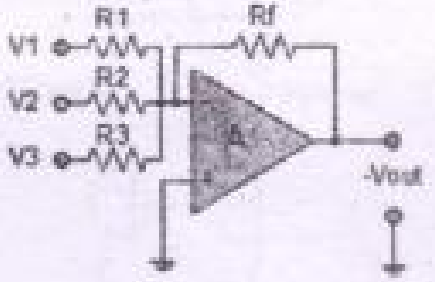


Fig 2

IV. Draw the circuit diagram of Integrator and derive its output expression. (3)

V. Draw the circuit diagram of non-inverting amplifier and derive the expression for its output voltage. (2)

VI. Draw the symbol and truth table of universal gates. (2)

University Roll No:.....

End Term Examination, Even Semester 2018-19

B.Tech, I[st] Year, II[nd] Semester

BECG0001, Electronics Engineering

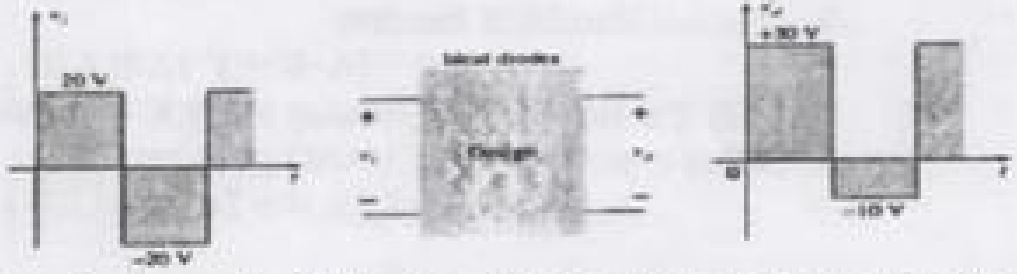
Time: 3 Hrs. **Max. Marks: 50**

Section-A

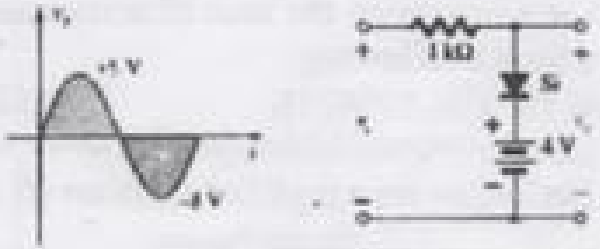
Note: Attempt All questions. *7x5=35 marks*

I. Explain the working of center-tapped full wave rectifier with circuit diagram and input-output waveform. Define ripple factor and rectifier efficiency.

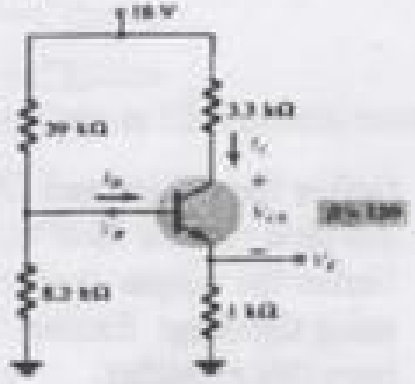
II. a) Design a clamper circuit to perform the function indicated below:



b) Analyze the following clipper circuit and sketch the output waveform.



III. Determine I_B, V_{CE}, V_C, V_E and Stability factor(S) for the given BJT network. Assume(V_{BE}=0.7v)



IV. Explain the construction and working of n-channel JFET with transfer and drain characteristics.

University Roll No:.....

OR

Explain the construction and working of n-channel Enhancement MOSFET with transfer and drain characteristics.

V. Design the circuit of 3-input adder using operational amplifier. Derive its output expression. For the following sets of voltages and resistances determine the output of adder circuit.

V_1=3v, V_2=-5v, V_3=-8v

R_1=2KΩ, R_2= 13KΩ, R_3=15KΩ, R_f=20KΩ.

VI. a) Perform the $(f)_2=(35)_{10}-(54)_{10}$ using 2's complement method.

b) Simplify the given function using Boolean algebra. Also Determine the minimum number of basic gates required to implement the obtained simplified function.

$$f=A'B'C+(A+B+C)'+A'B'C'D$$

VII. Simplify the following expression using K-Map and implement the simplified expression using NAND gates only.

$$y=\Sigma(0,1,2,3,7,9,10)+\Sigma d(8,11,12,14)$$

Section-B

15 marks

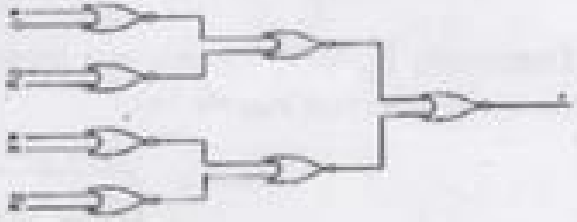
Note: Attempt All questions. *3x2=6 marks*

I. Let x represents the base of the number system, then find the value of x for the following:

a) $(D9B)_{16}=(6633)_x$ b) $(4123)_x=(538)_{10}$

II. List the characteristics (atleast 6) of ideal operational amplifier.

III. Determine the simplified function (f) for the given logic circuit.



Note: Attempt All questions. *3x3=9 marks*

I. Define Slew Rate and CMRR. What should be the values of CMRR and slew rate for ideal Operational amplifier?

II. Derive the output expression for closed loop Non-Inverting amplifier using Op-Amp. Explain how a unity gain amplifier can be obtained from this amplifier.

III. Convert the following function into its canonical form and find the minterms and maxterms.

$$F(x,y,z)=(x+y')(x+z')(y+z)$$

University Roll No: .....

End Term Examination, Odd Semester, 2019-20

B.Tech, I–Year, I–Semester

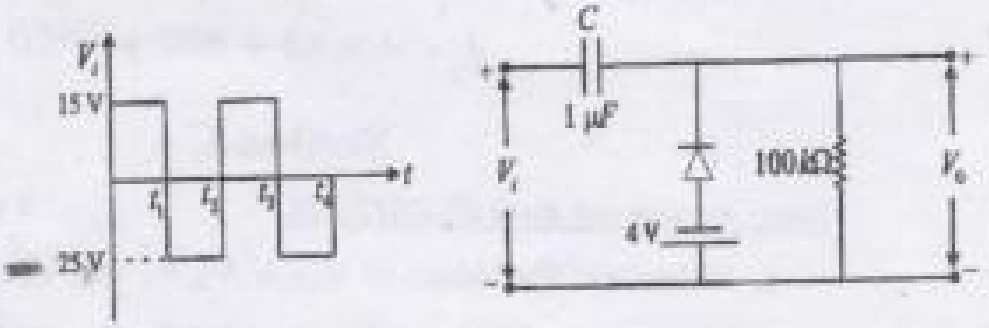
BECG 0001: Electronics Engineering

Time: 3 Hour **Maximum Marks: 50**

Section-A

Note: Attempt AnyFive QUESTIONS. **5 × 4 =20 Marks**

1. Explain the working of centre tapped full wave rectifier with circuit diagram. If input signal applied to FWR has frequency of 50Hz then determine the frequency of output signal of FWR.
2. Draw and analyze the output waveform for the circuit shown below considering ideal ~~op-amp~~ diode.



3. Explain the working operation of npn BJT with the help of suitable diagram. Derive the relation between α and β.
4. Draw the circuit diagram of op-amp integrator and derive the output expression.
5. Implement X-OR and X-NOR gate using NAND gate only.
6. (a) Perform the following operation using 2's complement method.
   $(101010111)_2 - (101010)_2 = (?)_2$
   (b) Solve the following using binary addition.
   $(A6)_{16} + (732)_8 = (?)_2$

Section-B

Note: Attempt ALL QUESTIONS. **5 x 3 =15 Marks**

1. Simplify the given Boolean function using K-map.

   $$f(A,B,C,D) = \Pi M(0,1,3,4,9,11,14).d(5,10,12,15)$$

2. Write the characteristics of an ideal op-amp.
3. Calculate I_D and g_m for n-channel JFET if I_{DSS}=8mA, V_P=-5V and V_{GS}=-3V.
4. Convert the given function into canonical form and find it's maxterm and minterms.

   $$f(w,x,y,z) = \bar{w}xy + x\bar{y}z + wz$$

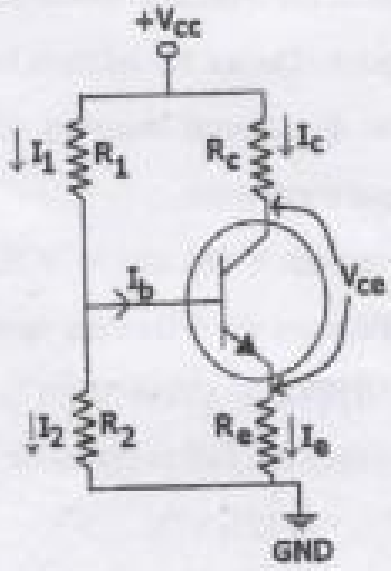
5. Simplify the Boolean function using boolean algebra

   $$f = A + AB + ABC + \overline{ABCD}$$

Section-C

Note: Attempt any three QUESTIONS. **3 x 5 = 15 Marks**

1. Determine the values of V_{CE}, I_C, V_B, V_C and V_E for the given circuit where V_{CC} = 18V, β = 50, R_1 = 82KΩ, R_2 = 22KΩ, R_C = 5.6 KΩ, R_E = 1.2KΩ, V_{BE} = 0.7V.



2. Simplify the following function using K-map and implement the simplified function using basic gates only.

$$f(A,B,C,D) = \sum m(0,1,2,8,9,10,11,12,14,15)$$

3. Draw the circuit diagram of 2 input adder using op-amp. Calculate the output voltage for the given values of 2 input adder.
   V_1=0.2V, V_2=-0.5V, R_1=10KΩ, R_2=15KΩ and R_f=20KΩ.
4. Explain the working of D-MOSFET by drawing the drain characteristics.

Course Name: Electronics Engineering

Course Outcome

CO1: Understand the basics of semiconductors and PN junction diodes with its characteristics.

CO2: Apply the basics of diodes to analyze rectifiers, clippers, clampers and voltage regulator circuits.

CO3: Understand the basic concepts of Bipolar Junction Transistor, Field Effect Transistor and MOSFET's with their characteristics.

CO4: Apply the basics of transistor to design and analyze DC biasing amplifier circuits.

CO5: Understand operations amplifier and its parameters. Design different application circuits such as adder, subtract or, integrator and differentiator.

CO6: Identify and understand different types of Number systems, theorems, postulates of Boolean algebra and logic gates. Apply theorems of Boolean algebra for minimization of Boolean expression. Apply basics of logic gates to draw logic circuits for any Boolean function.

Printed Pages:3 **University Roll No. .....**

End Term Examination, Odd Semester 2022-23

Program: B.Tech (All Branch), I Year, I Semester

Code: BECG0001 **Subject- Electronics Engineering**

Time: 3 Hours **Maximum Marks: 50**

Section – A

Attempt All Questions 4 X 5 = 20 Marks

No	Detail of Question	Marks	CO	BL	KL
1	Define static and dynamic resistance. Derive the formula for dynamic resistance.	4	1	R	F
2	A Half wave rectifier has R_L=1000Ω, R_f=50Ω. Input voltage applied to this rectifier is V_m=200 sin 314t. Determine: (a) Maximum value of current (b) average or dc value of current (c) the rms value of current (d) ripple factor.	4	2	A	C
3	Draw and discuss the input and output characteristics of Common Base BJT configuration.	4	3	U	F
4	Write the ideal characteristics of op-amp.	4	5	R	F
5	Draw and explain the drain & transfer characteristics of n-channel JFET. OR Draw and explain the drain & transfer characteristics of n-channel Depletion MOSFET.	4	3	U	F

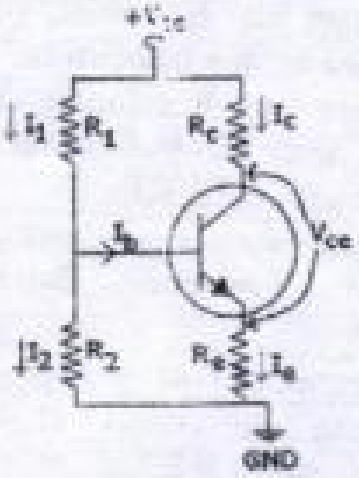
Section – B

Attempt All Questions 3 X 5 = 15 Marks

No.	Detail of Question	Marks	CO	BL	KL
6	Write the minterms of the following function. F(A,B,C)=A'+B'C+AB	3	6	A	C
7	Give the differences between BJT and FET.	3	3	U	F
8	Simplify the following function using Boolean algebra. F(A,B,C)=AB+(AC)'+AB'C(AB+C)	3	6	A	C
9	Perform the following operations (a) Solve $(11010101)_2 - (10001011)_2$ using 2's complement. (b) Convert $(89.26)_{10}=(?)_2=(?)_8$	3	6	U	C
10	Draw the symbol, boolean function and truth table of XOR & XNOR logic gates.	3	6	R	F

Section – C

Attempt All Questions 5 X 3 = 15 Marks

No	Detail of Question	Marks	CO	BL	KL
11	Determine the values of I_B, I_C, V_B, V_{CE} and V_E for the given circuit where V_{CC} = 20V, β = 51, R_1 = 700KΩ, R_2 = 100KΩ, R_C = 1.2 KΩ, R_E = 1.1 KΩ, V_{BE} = 0.7V. 	5	4	A	P
12	Simplify the following function using K-map and implement the simplified function using basic gates	5	6	U	C

	only. $f(A,B,C,D) = \sum m(0,1,2,9,11,15) + \sum d(8,10,14)$				
13	Explain the inverting and non-inverting operational amplifier and drive their output voltage.	5	5	R	F

Course Name: **Electronics Engineering**

Course Outcome

CO1: Understand semiconductor and transport mechanism of charge carrier in semiconductor material, PN junction diodes with its V-I characteristics

CO2: Apply the diodes in rectifiers, clippers, clampers and voltage regulator circuits.

CO3: Understand the basic concepts of Bipolar Junction Transistor, Field Effect Transistor and MOSFET's with their characteristics.

CO4: Design DC biasing amplifier circuits using transistors.

CO5: Understand operational amplifier and its applications in the circuits such as adder, subtractor, integrator and differentiator.

CO6: Understand Number systems, theorems and postulates of Boolean algebra, K-Map.

Printed Pages: 04 **University Roll No. .....**

End Term Examination, Even Semester 2022-23

Program: B. Tech (Common to All Branch), Ist Year, IInd Semester

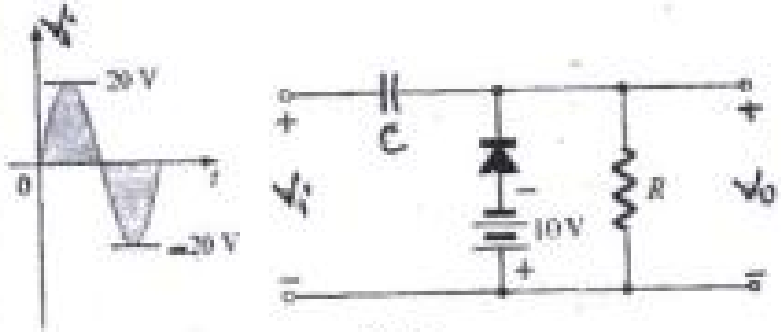
Subject Code: BECG 0001

Subject Name- Electronics Engineering

Time: 3 Hours **Maximum Marks: 50**

Section – A

Attempt All Questions 4 X 5 = 20 Marks

No.	Detail of Question	Marks	CO	BL	KL
1	(i) Draw the V-I characteristics of pn-junction diode. (ii) Enlist the differences between the Avalanche breakdown and Zener breakdown.	4	1	U	P
2	Analyse the output waveform of given electronic circuit as shown in Fig. 1. Also, depict its output waveform.  Fig. 1	4	2	A	P
3	An experiment is carried out where BJT is connected in Common Emitter configuration. Show the observations of input and output characteristics if micro-ammeter is connected in the input side whereas milli-ammeter is connected in the output side.	4	3	A	P
4	Enlist any four ideal characteristics of an	4	5	R	F

	Operational Amplifier.				
5	Represent following Boolean functions such that minimum logic gates are required for digital implementation. (i) AB+AC+ABC(AB+C) (ii) C(B+C)(A+B+C) ***OR*** Subtract the following terms using 2's complement (i) $(110101)_2 - (10011)_2$ (ii) $(01101011)_2 - (11011001)_2$	4	6	A	P

Section – B

Attempt All Questions 3 X 5 = 15 Marks

No	Detail of Question	Marks	CO	BL	KL
6	(i) In a transistor experiment, following parameters are recorded. Emitter current is 8 mA and base current is (1/100) of collector current. Determine the values of base current and collector current. (ii) Determine α and I_{CBO} if I_E=2.8mA, I_C=2.75mA and I_{CBO}=0.1μA.	3	4	A	P
7	Enlist any three valid differences between the BJT and FET on the basis of their characteristics. ***OR*** Demonstrate DC load line analysis for the output characteristics of a Bipolar Junction Transistor connected in fixed biased configuration.	3	3	R	F
8	Tabulate the input output relation of two bit NOR gate. Also, implement AND gate using NOR gate.	3	6	U	P
9	Convert the number systems as instructed: (i) $(5746.65)_8 = (?)_2 = (?)_{16} = (?)_{10}$ (ii) $(4467)_8 + (110010101100)_2 = (?)_{10}$ ***OR*** Convert given expression into canonical sum of product form. Also, find the minterms for the same expression as given below: $F = A\bar{B} + \bar{B}C + C + \bar{A}\bar{B}C$	3	6	A	P
10	Calculate the output voltage for the circuit depicted	3	5	A	P

in Fig. 2:

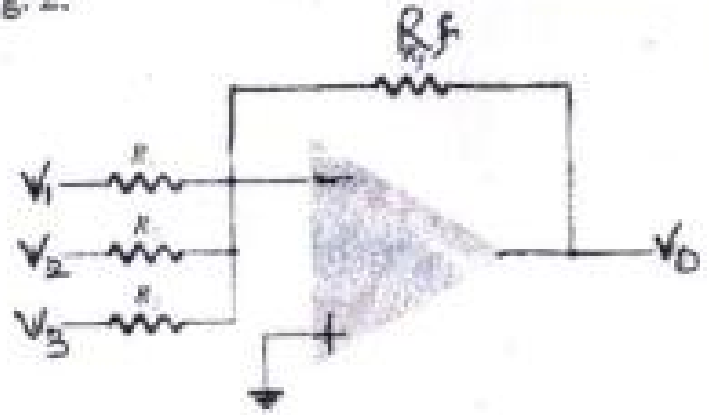


Fig. 2

Where, $R_1=R_2=R_3=10K\Omega$, $R_f=40K\Omega$, $V_1=4V$, $V_2=-6V$ and $V_3=10V$.

Section – C

Attempt All Questions 5 X 3 = 15 Marks

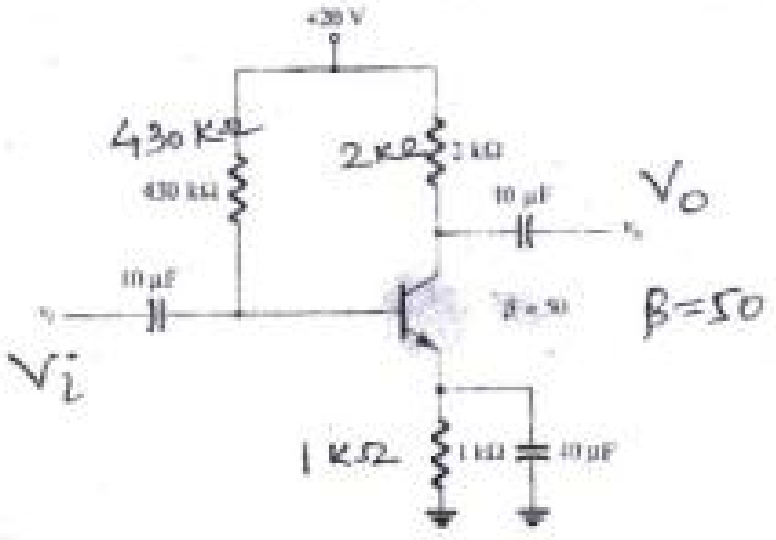
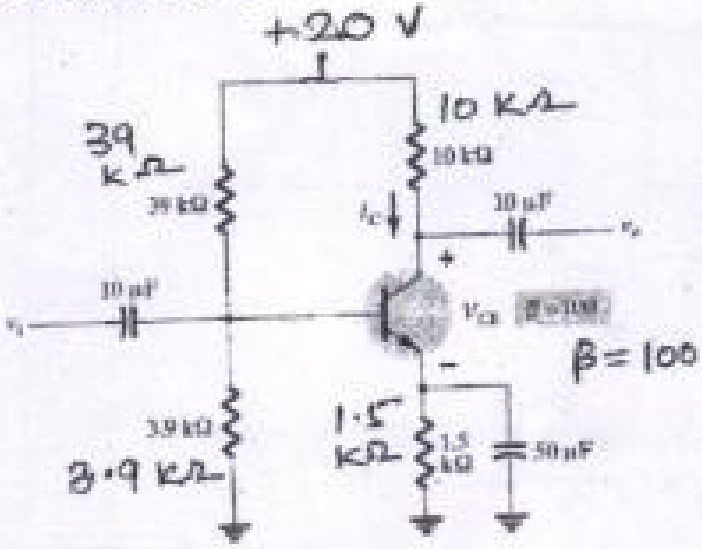
No.	Detail of Question	Marks	CO	BL	KL
11	Minimize given Expression using 4 variable K-Map: $f(A,B,C,D) = \sum m(0,1,2,3,6,7,14,15) + d(8,10,11)$	5	6	U	P
12	In the Emitter bias network as shown in Fig. 3, Determine I_B, I_C, I_E, V_{CE} and V_B.  Fig. 3 ***OR*** For the Voltage Divider bias network as depicted in	5	4	A	P

	Fig. 4, determine I_B, I_C and V_{CE}.  Fig. 4				
13	Draw the circuit of Differentiator and Integrator using Op-amp and derive the expression for their output voltages.	5	5	U	P