**HW#01: Register File, Arithmetic Logic Unit, and Multiplier**

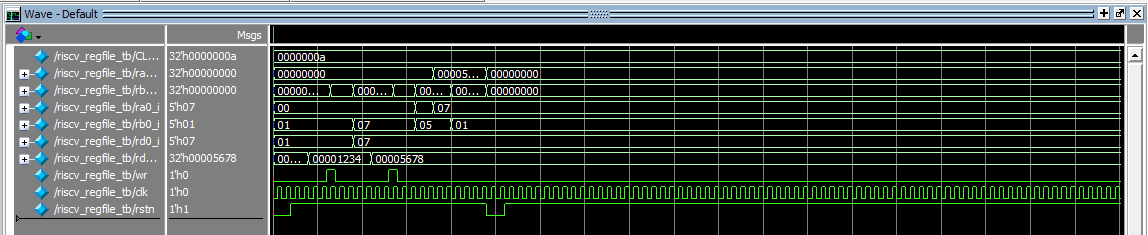
**Satyam (2023-81784)**

**Problem 1 (15p): Register File**

Files:

1. **Lab02/ex1\_regfile/riscv\_regfile.v**
2. **Lab02/ex1\_regfile/riscv\_regfile\_tb.v**

Waveform -

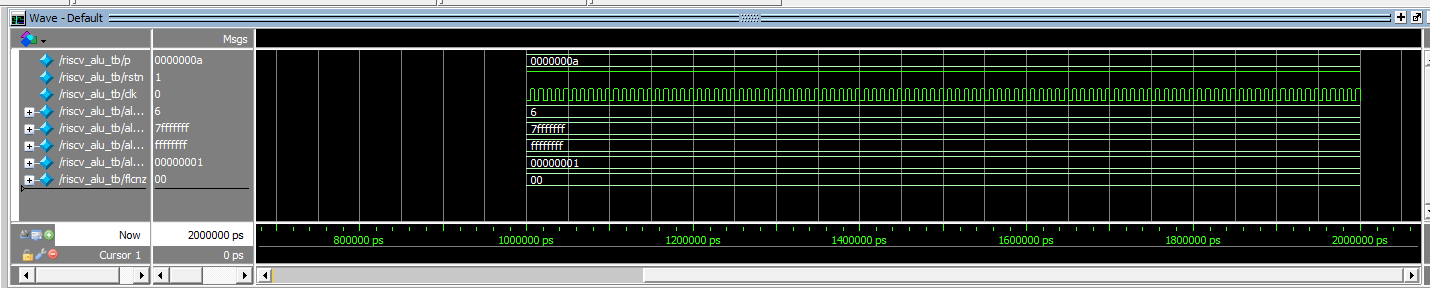


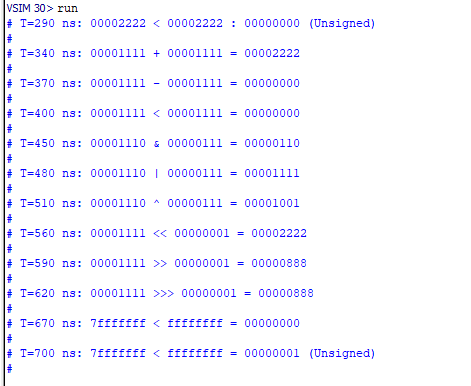
**Problem 2 (15p): Arithmetic Logic Unit (ALU)**

Files -

1. **Lab02/ex2\_alu/riscv\_alu.v**
2. **Lab02/ex2\_alu/riscv\_alu\_tb.v**

Waveform & Result -

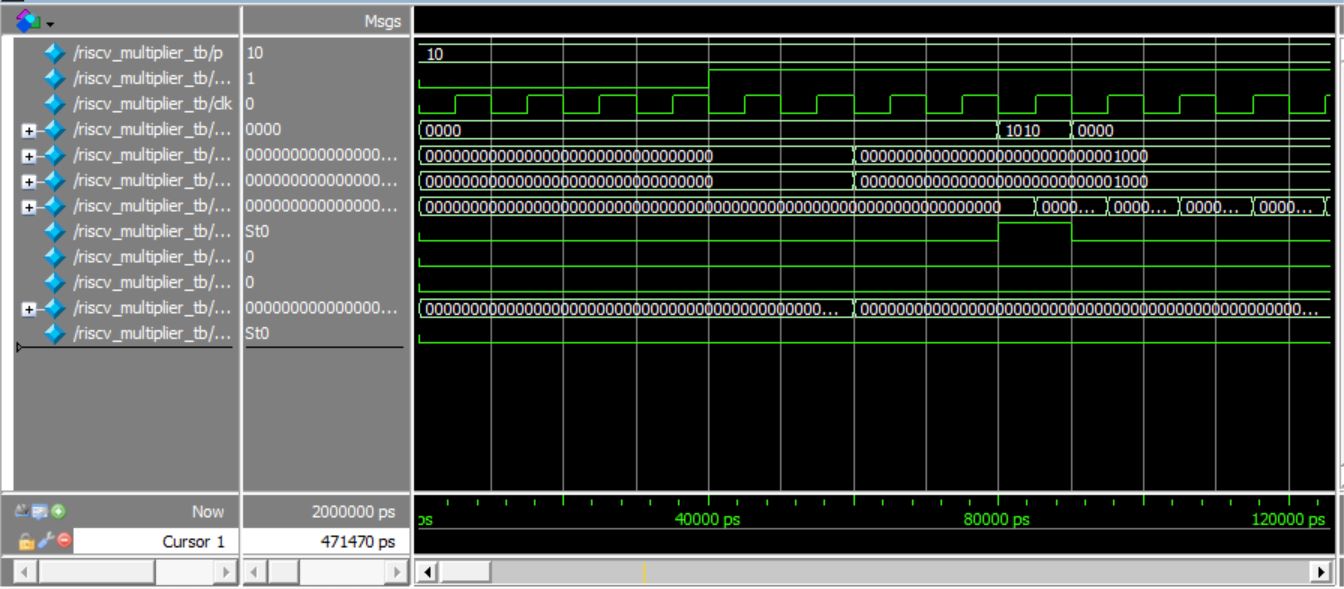
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**Problem 3 (5p): Multiplier**

Files -

1. **Lab02/ex3\_multiplier/riscv\_multiplier.v**
2. **Lab02/ex3\_multiplier/riscv\_multiplier\_tb.v**

Waveform -

**Problem 4 (3p): (Optional) Bonus**

1. (1p) Assume that each operation in ALU is described in a block. Draw a block diagram of ALU.
2. (2p) In problem 3, a slow sequential multiplier completes a 32-bit multiplication in 32 cycles. Is a computation result correct if the input is changed during computation? Modify the code to make the computation result correct even though input is changed during computation. Show the test cases and the waveform corresponding to both the baseline code and a modified code.