About this Document

In this document, I am presenting the error analysis of Schematic and PCB design of the KiCAD assesment file. I have included the following datasheets and documents that I used as a reference to analyze the errors and make recommendations:

1. Antenna Datasheet: Datasheet for 916 MHz USP410 Antenna.
2. AN5407 STM32WL5x: Application Notes regarding optimization of RF board Layout for STM32WL5x/Ex MCUs
3. RAK3172 Datasheet: Datasheet for the RAK3172 RF Module.
4. SHTC3 Datasheet: Datasheet for SHTC3 temperature sensor.
5. SHTXX Design Guide: A design guide for SHTC3 module.

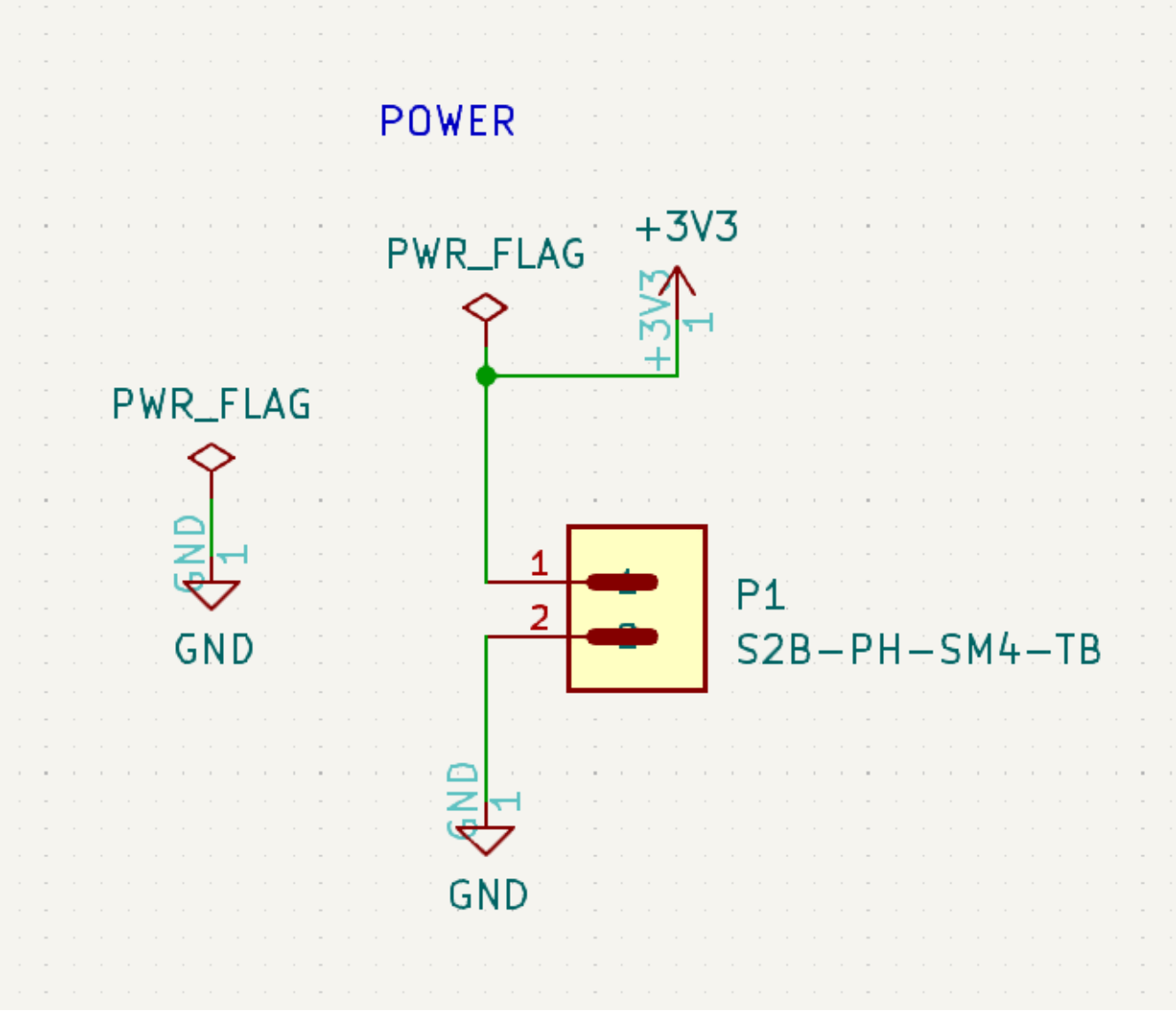
All the analysis presented in the document are based on my current knowledge, experiences and short study about RF design during the period of the assessment submission.

Schematic Section

This section highlights the analysis of the schematic section of the KiCAD assessment file.

Power Section:

For optimum and smooth power delivery to the system, a capacitor between the power supply terminals can be added which is not present in this case.



Antenna Section:

The schematic regarding antenna section consists of the USP410 916 MHz antenna along with the impedance matching filtering circuit.

Impedance matching and filtering circuit:

Looking at the antenna Datasheet, Linx specifies that the antenna is design to operated without any impedance matching circuit. However, the device has a high possibility of being subjected to a highly rough environment imposing various kinds of proximity effects, for which, matching may improve the end-product antenna performance. For matching network, Lnix recommends at least a 3-element surface mount matching pi network with two parallel capacitor and one serial inductor as shown in figure below:

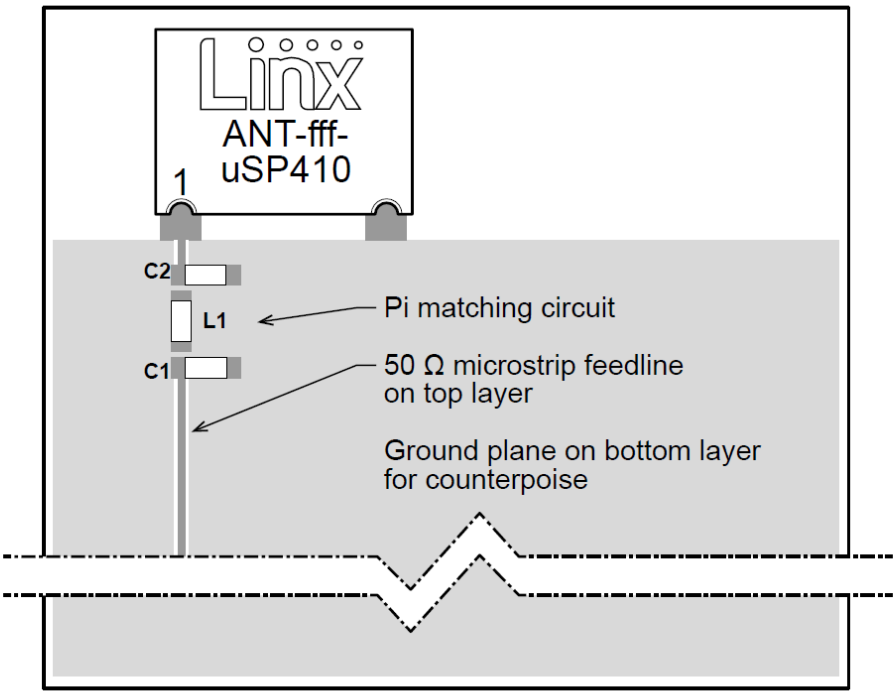


Figure 9. Linx uSP410 Series Recommended Layout.

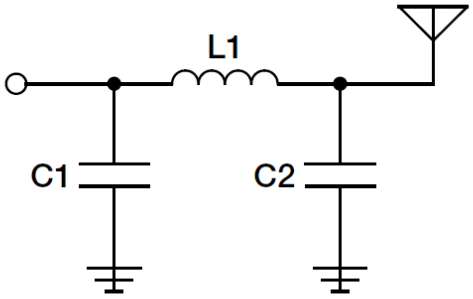
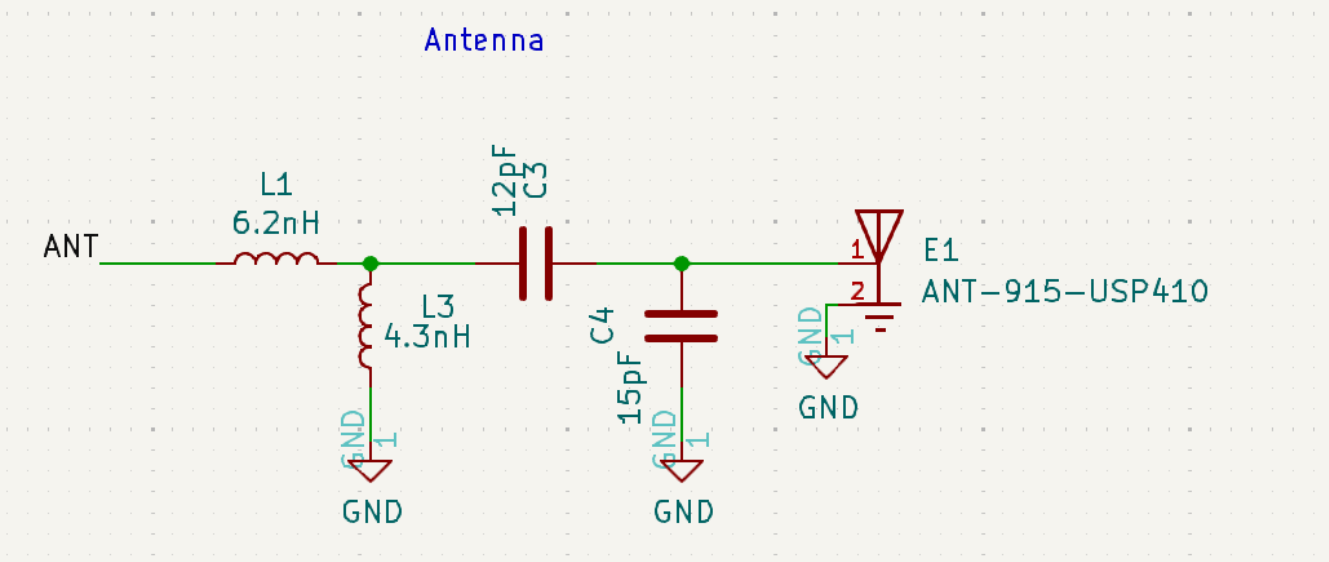
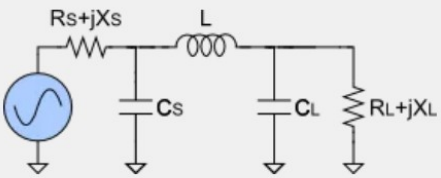


Figure 10. Matching Network Recommendation

In the existing design, another type of network is used as shown below.



I would like to align with the recommendation provided by Linx datasheet with the following calculation for the values of inductors and capacitors that yields the presented frequency response in the figure below:



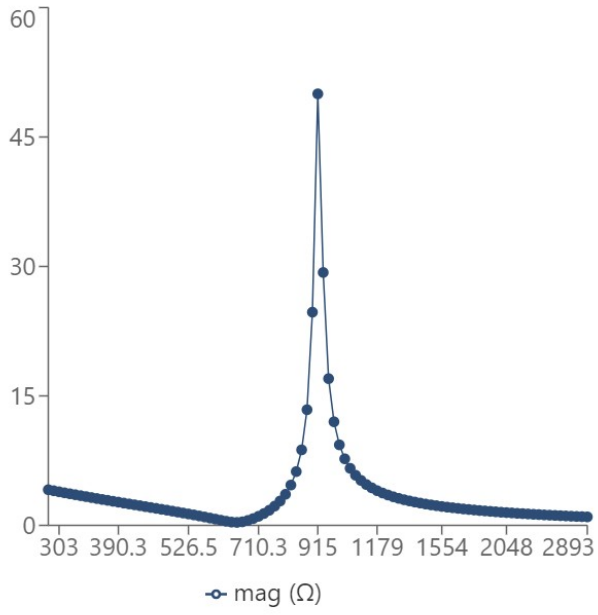
Frequency (F)	915 MHz
Source resistance (RS)	50 Ω
Source reactance (XS)	0 Ω
Load resistance (RL)	50 Ω
Load reactance (XL)	0 Ω
Q factor	17
Circuit DC current	Pass DC Current

Results

Inductance (L)	1.0196 nH
Source capacitance (CS)	0.05914 nF
Load capacitance (CL)	0.05914 nF

Charts

Show plot? Mag

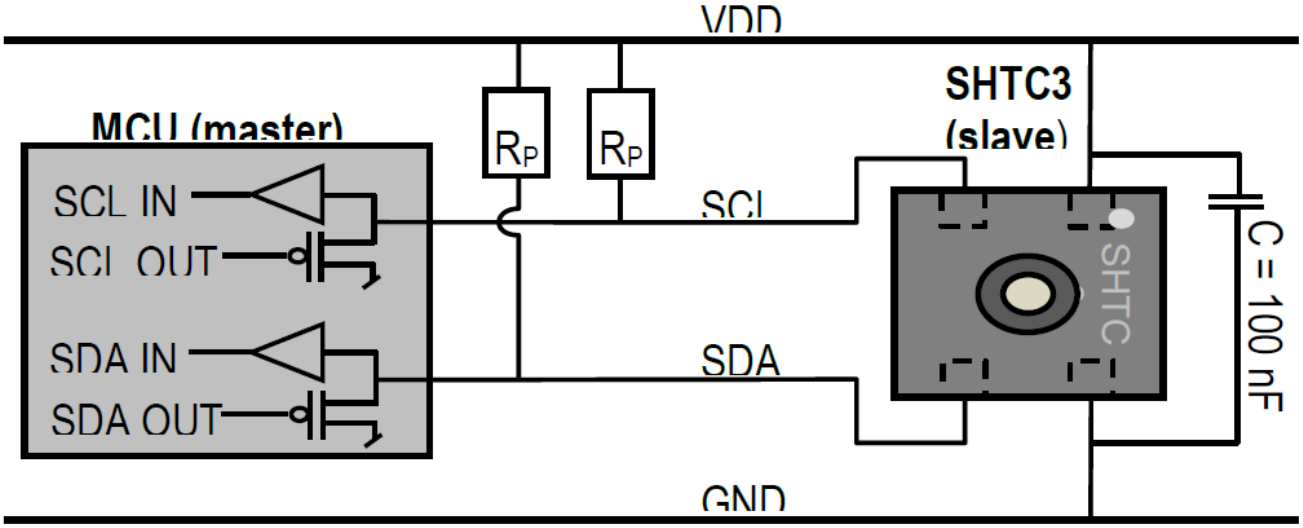


For the selection of components, first of all, the inductor availability was inspected (as it has availability for limited number of values only than compared to capacitor) for various Q factor values with appropriate frequency response, the resulting value was searched in the web application of electronic supplier (mouser electronics in this case) considering the package size of 0402 (priority given for this case) or 0603 and comparing various parameters, the following components for the matching network is selected:

Component	Quantity	Value	Link
Inductor	1	1 nH	https://www.mouser.ca/ProductDetail/KYOCERA-AVX/HLQ021R0BTTR?qs=RNZK%252BTbvcGGezGJ%2FSnTp8A%3D%3D
Capacitor	2	56 pF	https://www.mouser.ca/ProductDetail/KYOCERA-AVX/0402ZK560FBWTR?qs=HoCaDK9Nz5c0Kbb2clqWWw%3D%3D

Sensor Section:

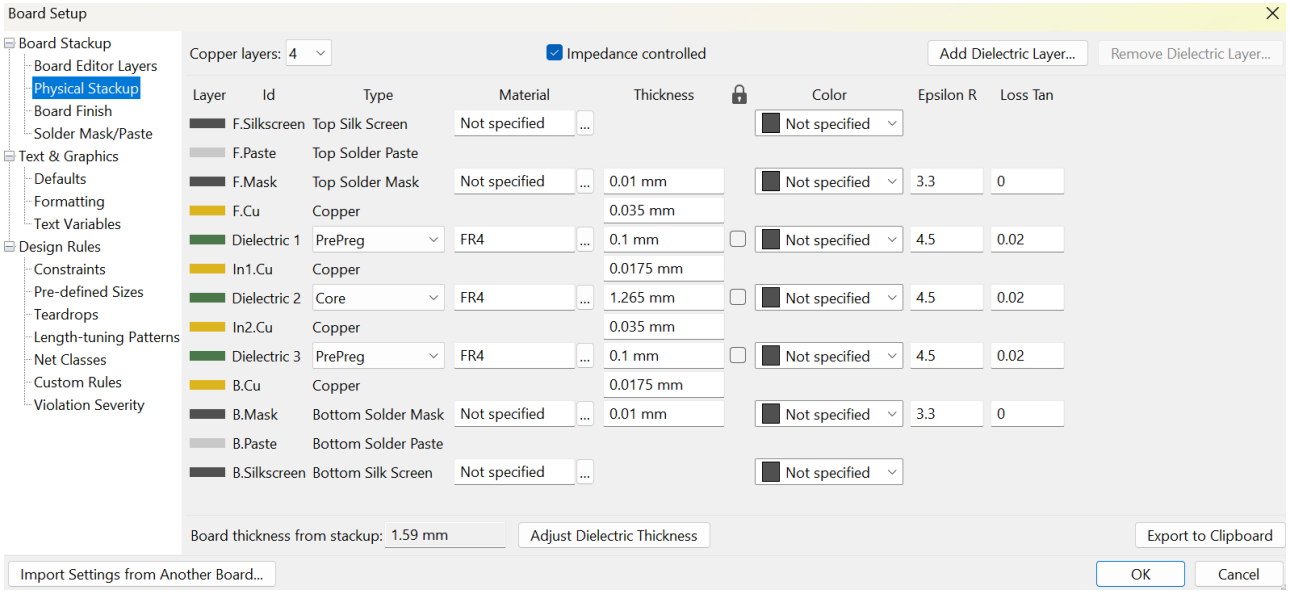
The sensor section consists of direct connection between the MCU's and Sensor's I2C interface. According to I2C standard, it is an open-drain NMOS(mostly) interface and requires a pull up resistor connected for each SCL and SDA line. Furthermore, the datasheet of the temperature sensor also recommends external pull-up resistors having the value of 10K on the lines.



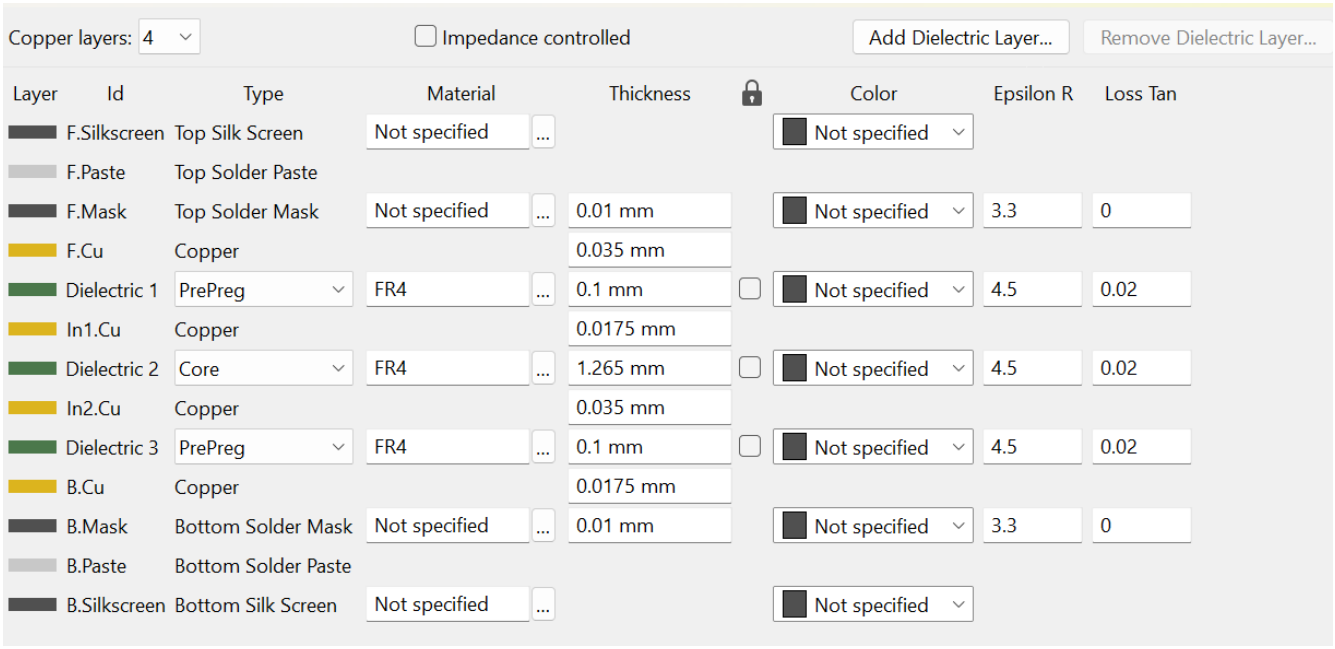
PCB Section:

This section highlights the analysis of the PCB section of the KiCAD assessment file. The following analysis were made:

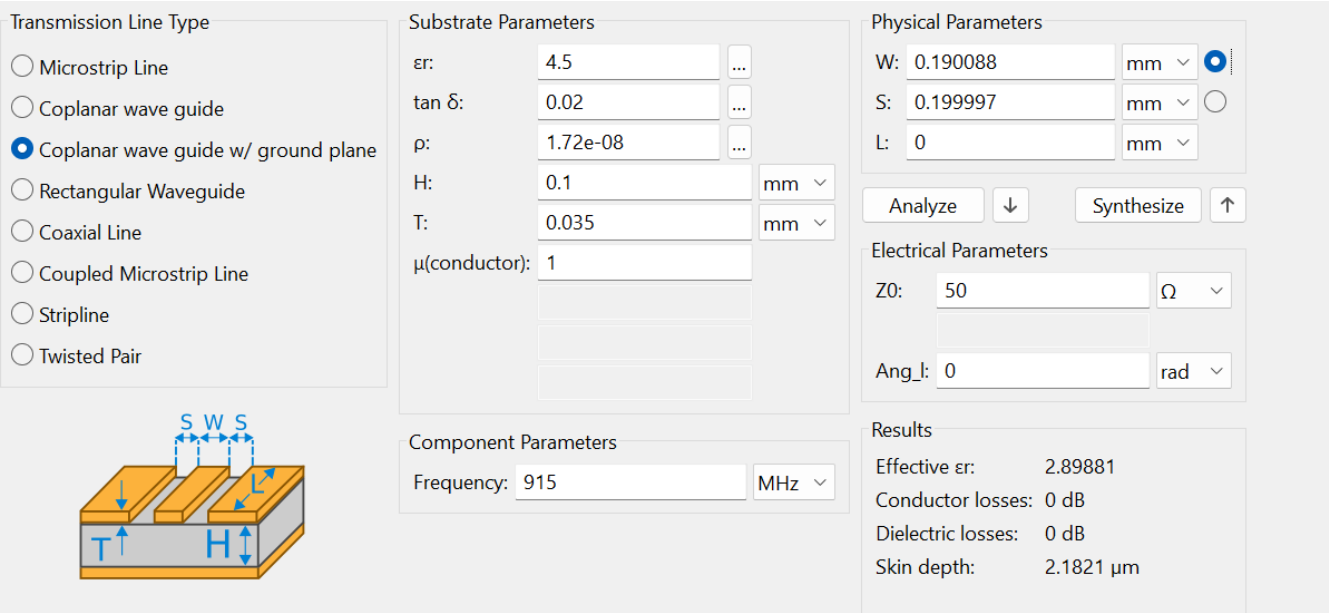
1. In the board setup options, i.e.: Board Setup -> Physical Stackup, the Impedance Controlled option was not checked. Checking this option before designing for RF design will ensure the Loss Tangent and relative dielectric constant (ε_r) will be added to the constraints. This will help in Trace Geometry Adjustments and Design Rule Enforcement.



2. Since there is no particular manufacturer specified, referencing to the following available pre-configured Physical Stackup:



The trace width of the RF microstrip wave guide in the grounded co-planar wave guide configuration is calculated as under using the KiCAD calculator:



Based on the above calculation, the width(W) of the microstrip should not cross 0.19mm, however, in the current design, the width is 0.25mm. However, the spacing between the microstrip and copper planes (S) for optimum performance must be around three times the height of dielectric (3*0.1mm = 0.3mm being 0.19 minimum from above calculation) which seems to be satisfied in the design (exactly 0.3mm).

3. The Average Critical Length of the microstrip for maintaining the impedance of 50Ω is calculated by using the following expression:

   $L_c = \lambda/12 = C/(f*\sqrt{\varepsilon_{eff}})*12)$ m

   Where,

   $C = 3x10^8$ m/s

   $f = 915*10^6$ Hz

   $\varepsilon_{eff} = 2.9$ (from above calculation)

   So the expression for the critical length yields: 0.016044 m = 16.044 mm ~= 16mm.

   In the design, the overall route length of the above 32mm which directly leads to the failure to maintain 50Ω impedance.

4. The maximum allowable distance between two vias in the via stitching is given by expression:

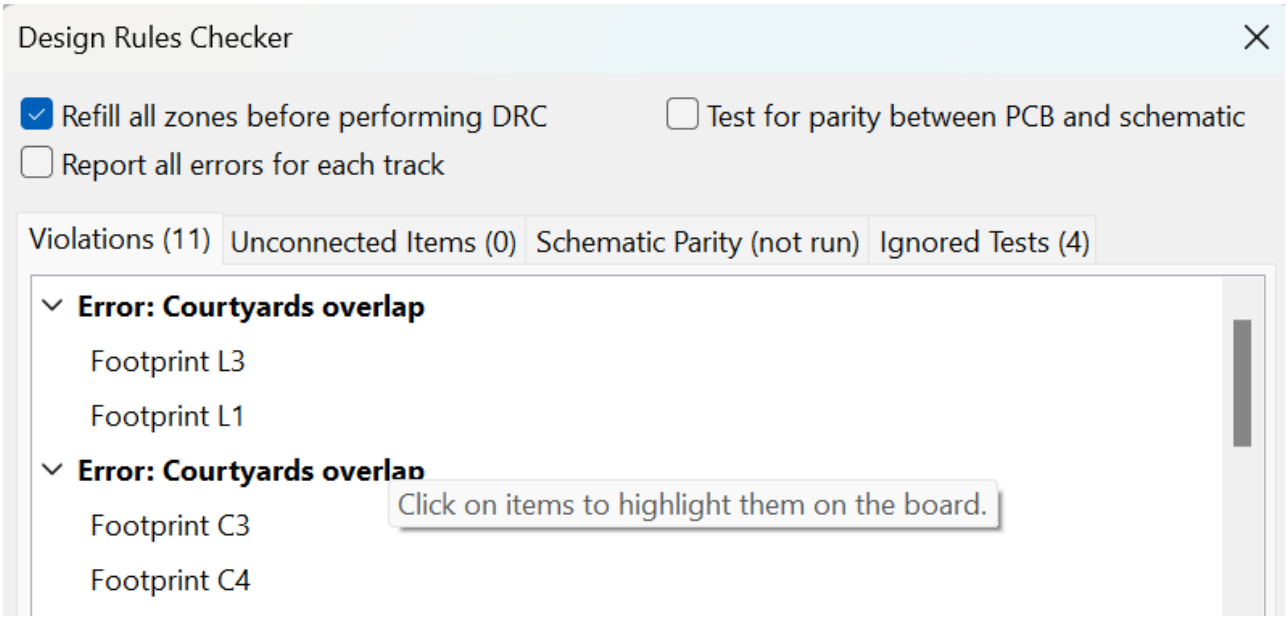
   $V_L = \lambda/20 = C/(f*\sqrt{\varepsilon_{eff}})*20)$ m

   Referencing the symbolic parameters with the same values as above, the calculation yields:

   $V_L = 0.00983$ m = 9.832 mm ~= 10 mm.

The spacing between the vias seems to be fine, but, they are spaced irregularly. In my opinion, stitches spaced regularly all across the board may provide a better easy return path and improves the impedance and RF performance of a board in most of the cases. Also, increasing the spacing slightly to an allowed range can help in providing more spaces for routing signals, improves copper filled-zone area and some thermal improvements.

5. The datasheet for Linx antenna recommends no ground plane or traces under any layer of the antenna, where as, in the provided design, all the four layer has copper filled zones including ground planes and power planes. This can be solved by using Keepout zone in the KiCAD or shrinking copper filled-zone areas in all layers towards the left side until it crosses the end of the pad of the antenna.
6. The design rules checker prompts two most obvious errors in the placement of RF components near the antenna as their pads are overlapping each other.



The three components L3, C3 and C4 can be placed little towards the right side of the current positions and routed accordingly keeping the connection straight.

7. The Application Note AN5407 recommends a straight RF transmission microstrip is ideal which is possible to implement in this case by proper placement of the microcontroller module, Antenna Module and other components.

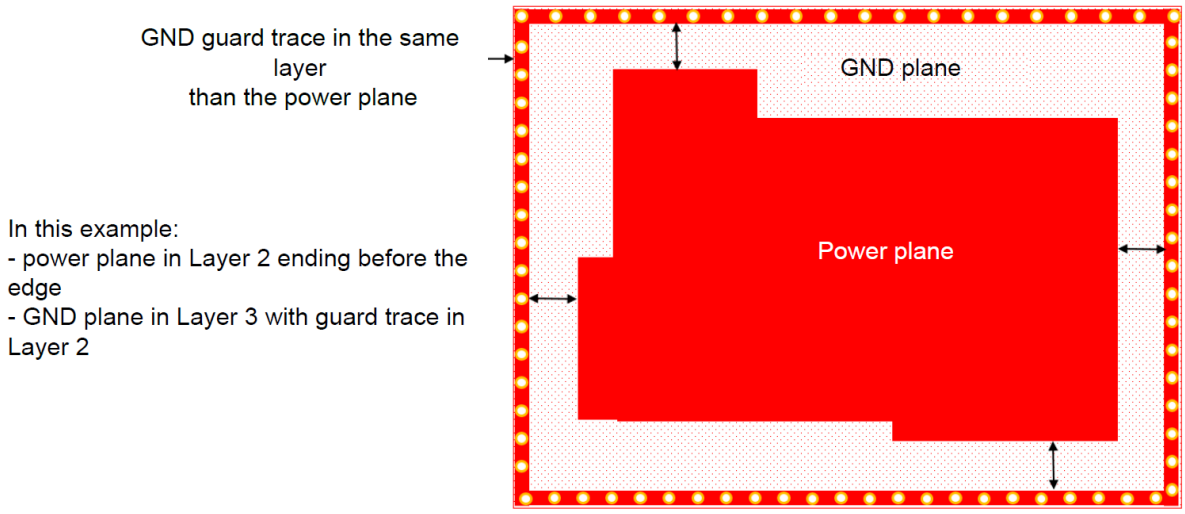
The ideal case is a straight line with a constant width as shown below.

Figure 21. Ideal case: straight line

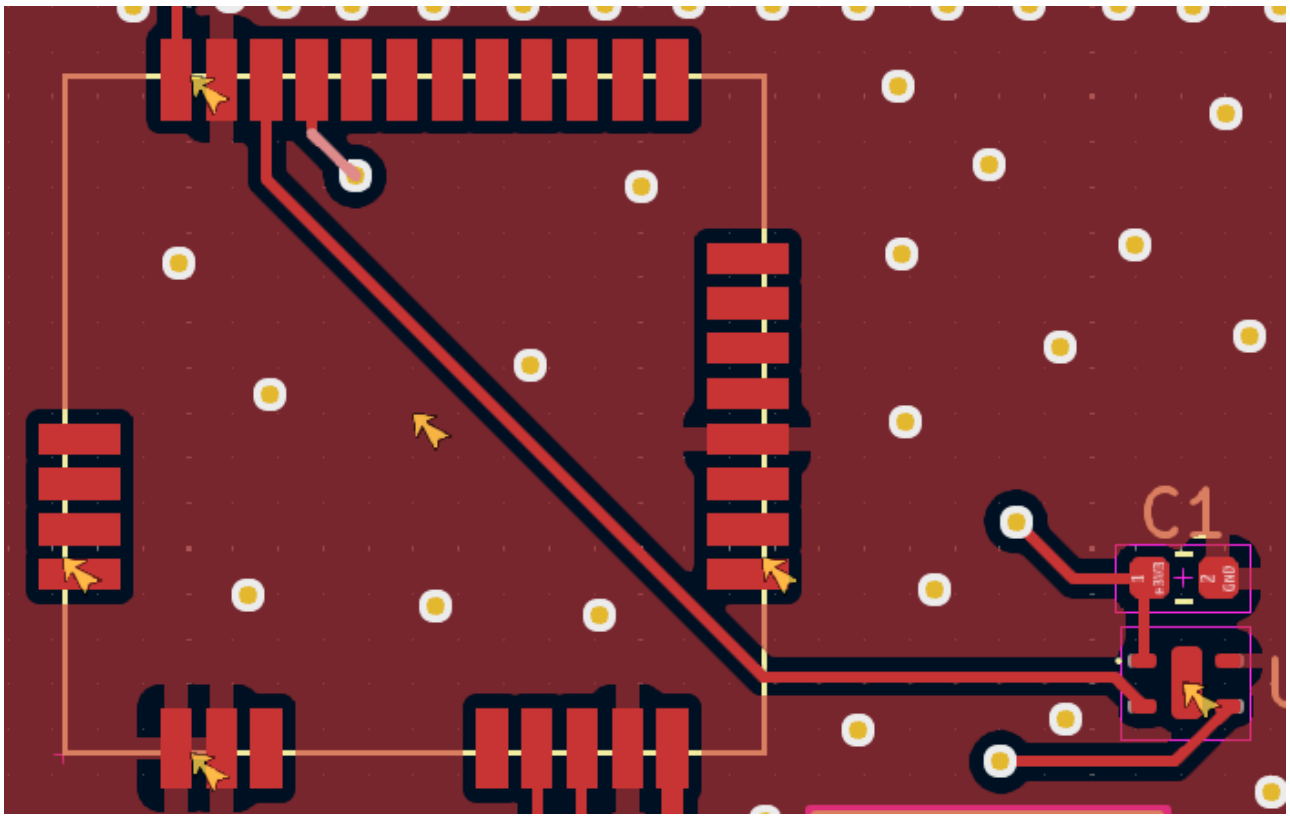
Performance	Bend type
Recommended	
Better	
Better	
Not good	

Even the curves with the continuous width (only if required) would be better than bending the RF microstrip wave guide at any angles.

8. The third layer from the top is the power plane. The Application Note AN5407 recommends power plane not to be routed at the edge of the board to avoid the unintentional electromagnetic radiations due to fringe fields. Ground plane must be put in all layers around the board and must be connected.



9. The filled copper zone at the bottom side of the RAK 3172 module acts as a thermal release as it is obvious that the microcontroller gets heated during its operation. Routing any traces that carries signal may cause signal loss or bit misrepresentation due to the temperature effect on the signal trace. To avoid routing the signal with net label I2C_SCL, the proper layout and arrangement of components along with the RAK 3172 module will be sufficient.



There is a similar case with routing for the signal trace with net label I2C_SDA, but, in this case the signal is transmitted to the bottom layer and again brought back to the top layer which may

not be required in this case as there is a plenty space for routing a signal with proper arrangements of all of the components. The use of via as in this case is unreasonable because via is used only when it is impossible to route a signal from top layer because the unavailability of a proper routing path from the source to the destination. Furthermore, this also violates the best practices for PCB design implementing I2C protocol which includes:

- For best performance, route the I2C traces on the same plane and above a reference plane (GND, Ideally or plane that has the same voltage as I2C interface), don't cross splits.
- Keep distance between the traces (SCL and SDA must be around 3 times the height of the dielectric)
- Keep traces as short as possible.

Furthermore in such tracks, the heat from the microcontroller is easily conducted to the temperature sensor causing the measurement with errors.

10. The placement of the temperature and humidity sensor at the center of the board is not optimum in my opinion as the copper plane acting as a thermal release near the microcontroller module can introduce extra heat causing measured temperature to be slightly higher than actual value. It should be placed near the edge of the board with a fair amount of clearance from the filled copper zone where it is free to sense the surrounding temperature. As the design guide also suggests this.

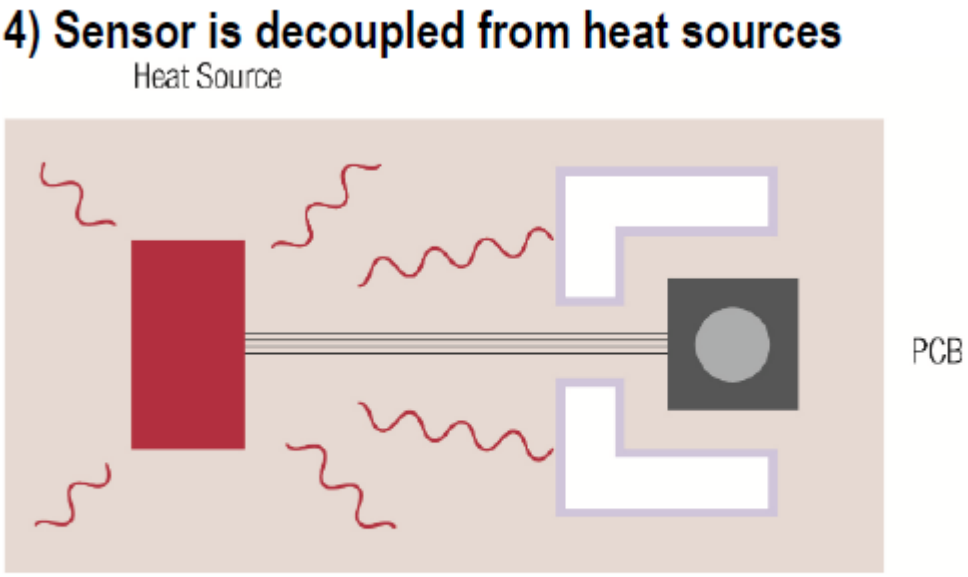


Figure 4: Decoupling of the sensor from heat sources in the PCB minimizes the influence of internal heating on the sensor.

Even the width of the traces connecting to the sensor must also be as thin as possible. In short, the design guidelines recommended by the sensor manufacturer should be followed as much as possible as shown below:

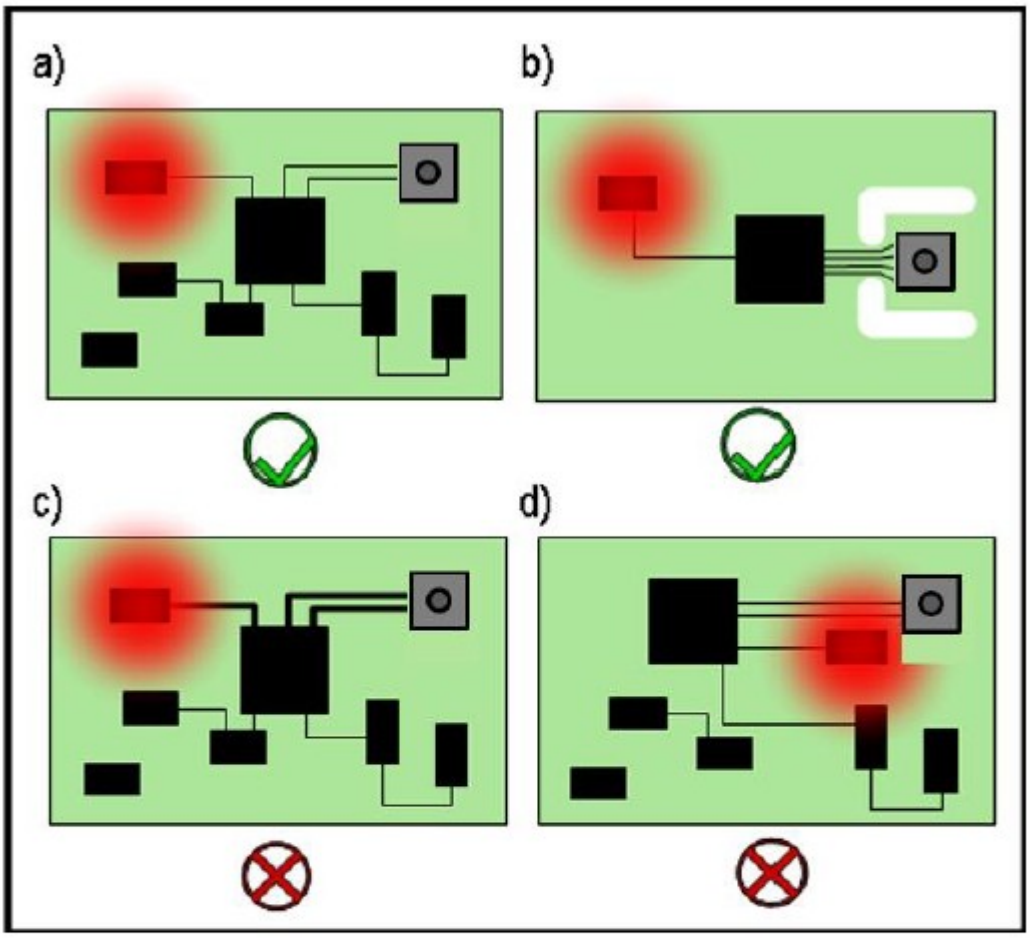


Figure 6: a) Thin metal connections and sufficient distance to the heat source helps to avoid heat conduction. Please note to remove unnecessary metal on the PCB around the sensor. b) The milled slits (white lines) around the sensor decrease the thermal conduction through the PCB. c) Unnecessary metal, such as thick metal connections will increase heat transfer from the heat source to the sensor. d) Heat sources in close proximity will heat the sensor

In order to get a good decoupling of the sensor and the housing / PCB the heat conduction needs to be reduced as described in the heating section above (see *Figure 10*).

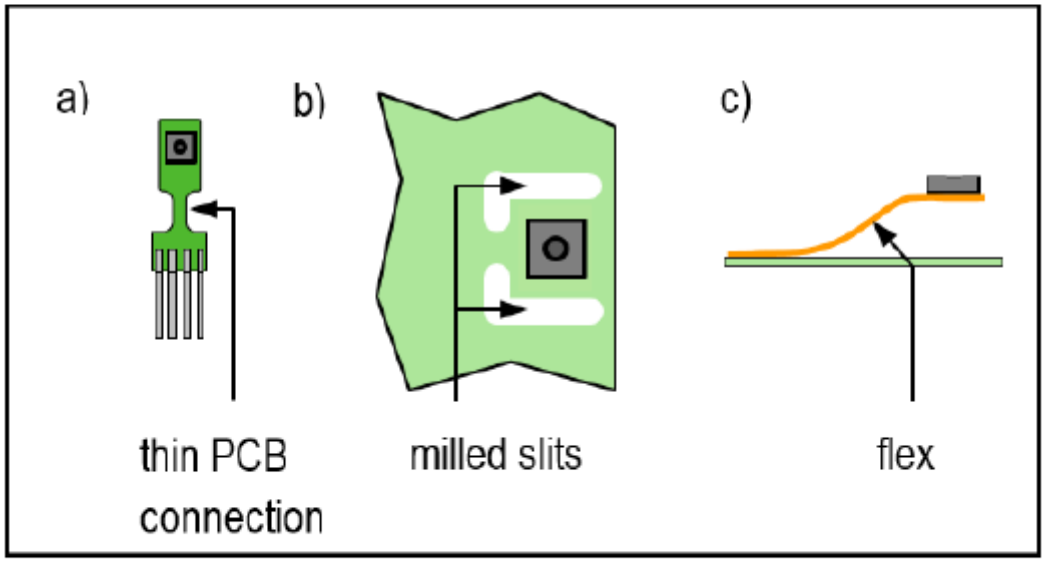


Figure 10: The sensor may be thermally decoupled from the PCB by small PCB connections or with a flex.

11. Also I can not find a proper reason to connect the ground of the ground of the power connector to a stitching via, as both of them are already connected to the copper filled-zone on all of the ground plane layers and the connected trace however is in the 3D view of the board, the trace is not visible as the trace and copper filled-zone are both copper.