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Design Rule Specification

XH018 - 0.18 µm Modular Mixed

Signal HV CMOS

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1. Introduction

1.1 Related documents

Note: The specification documents listed in the table below do not contain information which is additional to that available in the SpecXplorer.

Description	Document number
Process and Device Specification XH018 - 0.18 µm Modular Mixed Signal HV CMOS	PDS_018_03
PCM Acceptance Specification XH018 - 0.18 µm Modular Mixed Signal HV CMOS	PAS_018_03
Process Reliability Specification XH018 - 0.18 µm Modular Mixed Signal HV CMOS	PR_018_03

Note: Additional available specifications:

Design Rule Specification 0.18µm MIM Antenna Rules [DR_018_10](#)

Note: Note that additional documents and application notes related to this process family can be found in the relevant document container at "my X-FAB", under "[Process Selection Documents](#)" and "[Technical Documents](#)"

Note: Users may also wish to use the RelXplorer interactive application. This can provide information about device and layer reliability according to application specific mission profiles. For access to this see <http://relxplorer.xfab.com>

1.2 General notes

It is strongly advised that all reported DRC errors are removed.

In addition to the rules for mask making, this document also contains the rules for design support layers which:

- aid chip construction
- aid scribe lane construction
- enable LVS extraction of components
- control automatic pattern fill

Scaling of these rules for application to or from the other processes is NOT guaranteed.

All data represent the drawn dimensions. Graphical illustrations are not to scale.

Predefined layout must not be changed.

Modified devices are not supported.

This specification is valid excluding a process specific area around the wafer edge of 5mm width. In the affected area, the function, parameters and reliability of the structures are not guaranteed.

1.3 Support

Technical questions should be directed to:

X-FAB Semiconductor Foundries

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1.4 SpecXplorer

All of the data in this specification document is also available online via the SpecXplorer website. For access to this, see <http://specxplorer.xfab.com>.

2. General

2. General

2.1 Process modules

For this process family, one main module exists. This main module must be chosen. This can then be combined with one or more additional modules. Please also refer to the tables showing the required and forbidden modules, because:

- some modules are only available in combination with other modules,
- some modules are not available in combination with other modules.

For a complete list of available metal layer combinations, refer to the table below:

Metal Options

number of metals	Available Metal Layer Combinations	Module names
4	MET1-MET2-MET3-METTP	LPMOS+MET3+METMID
5	MET1-MET2-MET3-MET4-METTP	LPMOS+MET3+MET4+METMID
5	MET1-MET2-MET3-METTP-METTPL	LPMOS+MET3+METMID+METTHK
6	MET1-MET2-MET3-MET4-MET5-METTP	LPMOS+MET3+MET4+MET5+METMID
6	MET1-MET2-MET3-MET4-METTP-METTPL	LPMOS+MET3+MET4+METMID+METTHK

2.1.1 Main modules

Name	No. of masks	Description	Typical devices, applications
LPMOS	19	1.8V / 3.3V low power CMOS module, single polysilicon, metal 1, metal 2	1.8V low power NMOS/ PMOS, 3.3V low power NMOS/ PMOS, PNP, well, polysilicon and metal resistors

Module restrictions for main modules

Name	Required modules	Forbidden modules
LPMOS	MET3 and METMID	-

2.1.2 Additional modules for LPMOS main module

Name	No. of masks	Description	Typical devices, applications
MET3	2	3-metal module, additional via2/metal 3 layers	more complex wiring
MET4	2	4-metal module, additional via3/metal 4 layers	more complex wiring
MET5	2	5-metal module, additional via4/metal 5 layers	more complex wiring
METMID	2	top metal module, additional top metal & via layers	more complex wiring
METTHK	2	thick metal module, additional thick metal and thick via layers	power distribution
CPOD	1	Polysilicon over diffusion capacitor	1.8V POD capacitor
CPODHV	2	High voltage polysilicon over diffusion capacitor	high voltage POD capacitor
	Note: If the CPODHV module is selected in combination with the HVMOS or HVNMOS or HVPMOS or ESDPNP module, the combined additional mask count is 0.		
MRPOLY	1	medium resistance polysilicon module	lightly P-doped POLY1 resistor
ISOMOS	1	triple well isolated CMOS module	isolated 1.8V or 3.3V CMOS in DNWELLMV
ISOMOS2	1	triple well isolated CMOS module	isolated 1.8V or 3.3V CMOS in DNWELL



2. General → 2.1 Process modules→ 2.1.2 Additional modules f...

Name	No. of masks	Description	Typical devices, applications
HIGHTEMP	0	High temperature module	operating conditions up to +175 °C
LVT	2	1.8V low Vt module additional NWELL and PWELL	1.8V low Vt NMOS and PMOS 1.8V isolated low Vt NMOS and PMOS
SVT	2	1.8V medium Vt module, additional NWELL and PWELL	1.8V medium Vt NMOS and PMOS 1.8V isolated
LNPMOS3	1	3.3V low noise PMOS module, additional NWELL4	3.3V low noise PMOS, 3.3V isolated low noise PMOS
ULN	1	Low noise CMOS module, additional ULN	1.8V & 3.3V low noise CMOS, 1.8V & 3.3V isolated low noise CMOS
DEPL	1	depletion module, depletion well implant	3.3V depletion NMOS, NPN
HVDEPL	1	High voltage depletion module, depletion well implant	32V depletion NMOS
DMOS	1	DMOS module, DMOS drift implant	40V / 45V NDMOS, 35V PDMOS
HVMOS	5	high voltage module, additional gate oxide, high voltage N-well and P-well	15V HV CMOS
	Note: If the ISOMOS module or ISOMOS2 module is selected in combination with the HVMOS module, the combined additional mask count is 5.		
HVN莫斯	3	HVNmos module, thick gate oxide	6V NMOS with thick gate oxide
	Note: 1.If the HVNMOS module is selected in combination with the HVMOS module, the combined additional mask count is 5. 2.If the HVNMOS module is selected in combination with the HVPMOS module, the combined additional mask count is 6. 3.If the HVNMOS module is selected in combination with the HVPMOS + NHVE module, the combined additional mask count is 6.		
NHVE	1	high voltage extension module, shallow N-well	10 / 15 / 45V HVNMOS
HVPMOS	6	HVPMOS module, thick gate oxide and high voltage N-well	6V PMOS with thick gate oxide
	Note: 1.If the HVPMOS module is selected in combination with the HVMOS module, the combined additional mask count is 7. 2.If the HVPMOS module is selected in combination with the HVNMOS + PHVE module, the combined additional mask count is 7.		
PHVE	1	high voltage extension module, shallow P-well	20 / 45V HVPMOS
SCHOTTKY	2	Schottky module	Schottky diode
	Note: 1.If the Schottky module is selected in combination with the HVMOS module, the combined additional mask count is 6. 2.If the Schottky module is selected in combination with the HVNMOS module, the combined additional mask count is 4. 3.If the Schottky module is selected in combination with the HVPMOS module, the combined additional mask count is 6.		
MIM	1	MIM capacitor module	MIM capacitor between metal top and metal layer underneath
MIM23	1	MIM capacitor module	MIM capacitor between metal 2 and metal 3
MIM34	1	MIM capacitor module	MIM capacitor between metal 3 and metal 4
DMIM	1	double MIM capacitor module	double MIM capacitor
TMIM	1	triple MIM capacitor module	triple MIM capacitor
MIMH	1	single high capacitance MIM capacitor module	single high capacitance MIM capacitor
MIMH23	1	high capacitance MIM capacitor module	MIM capacitor between metal 2 and metal 3
MIMH34	1	high capacitance MIM capacitor module	MIM capacitor between metal 3 and metal 4
DMIMH	1	double high capacitance MIM capacitor module	double high capacitance MIM capacitor
TMIMH	1	triple high capacitance MIM capacitor module	triple high capacitance MIM capacitor

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2. General → 2.1 Process modules → 2.1.2 Additional modules f... → Module restrictions ...

Name	No. of masks	Description	Typical devices, applications
NVM	2	non volatile memory module (SONOS based)	ready-to-use NVRAM memory blocks
		Note: For ready-to-use memory blocks, refer to the memory block specification regarding the process module combination which is required for the specific block.	
FLASH	0	Flash module	ready-to-use Flash memory blocks
		Note: For ready-to-use memory blocks, refer to the memory block specification regarding the process module combination which is required for the specific block.	
OTP3	0	One-Time Programmable memory module	ready to use OTP memory blocks
		Note: For ready-to-use memory blocks, refer to the memory block specification regarding the process module combination which is required for the specific block.	
ANODOP	1	UV diode module - anode implant	Photodiode
CATDOP	1	CATDOP module - cathode implant	Photodiode
UVWINDOW	0	UV diode module - opens UV sensitive window	Photodiode
AVLA	1	Avalanche photodiode module - avalanche multiplication implant	Avalanche photodiode
BIPESD	3	ESD module	ESD protected HV PNP transistor
		Note: 1.The BIPESD module must be selected for device qpvhbscr only. 2.If the BIPESD module is selected in combination with the HVMOS module, the combined additional mask count is 7.	
ESDPNP	5	ESD module	ESD protected HV PNP transistor
		Note: 1.The ESDPNP module must be selected for device qpvhbscr only. 2.If the ESDPNP module is selected in combination with the HVMOS module, the combined additional mask count is 6.	
FLATPV	0	Flat passivation	Flat passivation, post process
SFLATPV	0	Sensor Flat passivation	Flat passivation for microlens or colour filtering, post process
PIMIDE	1	polyimide module, resilient barrier layer on top of passivation	wafer overcoat for stress relief and passivation protection
PHOTODIO	0	Photodiode module	Photodiode
		Note: This module requires the addition of other modules or may not be used in combination with other modules, as listed in the table "Restrictions for Module Combinations".	
HALL	3	Hall sensor module	Hall sensor
		Note: If the HALL module is selected in combination with the HVMOS module or the modules HVMOS AND DMOS, the combined additional mask count is 6.	

Module restrictions for LPMOS main module

Name	Required modules	Forbidden modules
MET3	-	-
MET4	MET3	ANODOP or UVWINDOW
MET5	MET4	METTHK
METMID	-	-
METTHK	METMID	MET5 or FLATPV or ANODOP or CATDOP or UVWINDOW or SFLATPV or AVLA
CPOD	-	-
CPODHV	CPOD	-
MRPOLY	-	-
ISOMOS	-	-
ISOMOS2	ISOMOS	-
HIGHTEMP	-	PHOTODIO or HALL or ANODOP



2. General → 2.1 Process modules → 2.1.2 Additional modules f... → Module restrictions ...

Name	Required modules	Forbidden modules
LVT	-	-
SVT	-	-
LNPMOS3	-	-
ULN	-	-
DEPL	-	-
HVDEPL	NHVE	-
DMOS	HVMOS	-
HVMOS	-	-
HVNOMOS	-	-
NHVE	HVNOMOS	-
HVPMOS	-	-
PHVE	HVPMOS	-
SCHOTTKY	-	-
MIM	METMID	DMIM or DMIMH or MIMH or TMIM or TMIMH or MIM23 or MIM34 or MIMH23 or MIMH34
MIM23	MET3	MIM34 or MIMH23 or MIMH34 or MIM or DMIM or TMIM or MIMH or DMIMH or TMIMH
MIM34	MET4	MIM23 or MIMH23 or MIMH34 or MIM or DMIM or TMIM or MIMH or DMIMH or TMIMH
DMIM	MET3	MIM or TMIM or MIMH or DMIMH or TMIMH or MIM23 or MIM34 or MIMH23 or MIMH34
TMIM	MET4	MIM or DMIM or DMIMH or MIMH or TMIMH or MIM23 or MIM34 or MIMH23 or MIMH34
MIMH	METMID	MIM or MIM23 or MIM34 or DMIM or TMIM or MIMH23 or MIMH34 or DMIMH or TMIMH
MIMH23	MET3	MIM23 or MIM34 or MIMH34 or MIM or DMIM or TMIM or MIMH or DMIMH or TMIMH
MIMH34	MET4	MIM23 or MIM34 or MIMH23 or MIM or DMIM or TMIM or MIMH or DMIMH or TMIMH
DMIMH	MET3	MIM or DMIM or MIMH or TMIM or TMIMH or MIM23 or MIM34 or MIMH23 or MIMH34
TMIMH	MET4	MIM23 or MIM34 or MIMH23 or MIMH34 or MIM or DMIM or TMIM or MIMH or DMIMH
NVM	ISOMOS	-
FLASH	NVM	-
OTP3	-	-
ANODOP	UVWINDOW	MET4 or METTHK or HIGHEMP
CATDOP	-	METTHK
UVWINDOW	MET3 and METMID	MET4 or METTHK
	Note: It is recommended to select either ANODOP or CATDOP module when the UVWINDOW module was selected. For any other use of UVWINDOW module, please contact X-FAB hotline.	
AVLA	CATDOP	PIMIDE or METTHK
BIPESD	-	-
ESDPNP	-	-
FLATPV	METMID	METTHK or SFLATPV
SFLATPV	METMID	METTHK or FLATPV
PIMIDE	-	AVLA

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2. General → 2.1 Process modules → 2.1.2 Additional modules f... → Module restrictions ...

Name	Required modules	Forbidden modules
PHOTODIO	ISOMOS	HIGHTEMP
HALL	-	HIGHTEMP

2. General → 2.2 Design layers

2.2 Design layers

The designer is responsible for the creation of all Design Layers needed by the targeted process module(s). They are necessary for mask layer generation and/or design tools, e.g. design rule check. Some of the layers defined may be optional dependent upon the design style being used: these are described in the text.

Design Layers may be used directly, or combined with other Design Layers, or sized to create the Mask Layers.

The order of the design layers in the table does not infer any process sequence.

Design layers with GDS numbers 480 to 499 are reserved for exclusive customer use. Any data for these layers will be ignored by X-FAB.

2.2.1 LPMOS main module

Name	Description	Code	GDS#	Data type	Purpose	Comments
NWELL	N-well	NW	2	0	DRAWING	
				5	VERIFICATION	defined as NW_VERIFY
PWBLK	P-well Block	PB	10	0	DRAWING	blocks 1.8V / 3.3V P-well generation
DIFF	Active Area	DF	3	0	DRAWING	
				1	DUMMY	defined as DIFFDUMMY
				14	NOBLK	not allowed for customer use
MV	3.3V Gate Oxide	MV	4	0	DRAWING	
POLY1	Poly 1	P1	13	0	DRAWING	
				1	DUMMY	defined as P1DUMMY
				3	TEXT	defines top level nets
				4	DMYBLK	blocks dummy generation, Design related guidelines must be considered
				5	VERIFICATION	defined as POLY1_VERIFY
				14	NOBLK	not allowed for customer use
				15	VLABEL	defines voltage classes
HRES	High resistive Poly 1	HR	65	0	DRAWING	
SBLK	Silicide Block	SB	34	0	DRAWING	
NIMP	N+ Implant	IN	8	0	DRAWING	
PIMP	P+ Implant	IP	7	0	DRAWING	
CONT	Contact	CT	15	0	DRAWING	
MET1	Metal 1	M1	16	0	DRAWING	
				1	DUMMY	defined as M1DUMMY
				2	SLOT	defined as M1SLOT
				3	TEXT	defines top level nets
				4	DMYBLK	blocks dummy generation, Design related guidelines must be considered
				5	VERIFICATION	defined as M1VERIFY
				9	net	defines net shapes
				10	boundary	
				15	VLABEL	defines voltage classes
VIA1	Via 1	V1	17	0	DRAWING	
				5	VERIFICATION	



2. General → 2.2 Design layers→ 2.2.1 LPMOS main module

Name	Description	Code	GDS#	Data type	Purpose	Comments
MET2	Metal 2	M2	18	0	DRAWING	
				1	DUMMY	defined as M2DUMMY
				2	SLOT	defined as M2SLOT
				3	TEXT	defines top level nets
				4	DMYBLK	blocks dummy generation, Design related guidelines must be considered
				5	VERIFICATION	defined as M2VERIFY
				9	net	defines net shapes
				10	boundary	
				15	VLABEL	defines voltage classes
				0	DRAWING	
PAD	Passivation	PA	19	5	VERIFICATION	
LOCKED	IP core definition	LOCK	20	10	boundary	
				19	ALL	
				20	LOCKED1	
				24	LOCKED2	
LOCKED1	IP core definition	LOCK	73	10	boundary	
LOCKED2	IP core definition	LOCK	74	10	boundary	
LOCKED3	IP core definition	LOCK	40	10	boundary	
LOCKED4	IP core definition	LOCK	41	10	boundary	
CAPDEF	Capacitor Definition	CDEF	78	5	VERIFICATION	
DIODEF	Diode Definition		56	5	VERIFICATION	
PHODEF	Photodiode Definition	D1	102	3	TEXT	defines top level light power net
				5	VERIFICATION	
XFLAY	Reserved		1			not allowed for customer use
SUBCUT	Splitting the substrate for LVS	SU	191	5	VERIFICATION	
BLKALL	Dummy Block	BA	83	4	DMYBLK	blocks all dummy generation, Design related guidelines must be considered
CORNER	Chip Corner box Definition	CB	330	5	VERIFICATION	
DEVLBL	Device Label		100	5	VERIFICATION	
FAMARK	Failure Analysis Marker		64	0	DRAWING	
PRBNDRY	Place & Route Boundary		190	0	DRAWING	
				10	boundary	
SUBDEV	for Substrate-Extractor- Tool PNAAware XSUB		197	3	TEXT	
				5	VERIFICATION	
SUBEXT	for Substrate-Extractor- Tool PNAAware XSUB		195	5	VERIFICATION	
DONOTUSE	Should not be used by customers		380	5	VERIFICATION	
TEXT	Optional Information		230	0	DRAWING	

2. General → 2.2 Design layers→ 2.2.2 MET3 module

2.2.2 MET3 module

Name	Description	Code	GDS#	Data type	Purpose	Comments
VIA2	Via 2	V2	27	0	DRAWING	
				5	VERIFICATION	
MET3	Metal 3	M3	28	0	DRAWING	
				1	DUMMY	defined as M3DUMMY
				2	SLOT	defined as M3SLOT
				3	TEXT	defines top level nets
				4	DMYBLK	blocks dummy generation, Design related guidelines must be considered
				5	VERIFICATION	defined as M3VERIFY
				9	net	defines net shapes
				10	boundary	
				15	VLABEL	defines voltage classes

2.2.3 MET4 module

Name	Description	Code	GDS#	Data type	Purpose	Comments
VIA3	Via 3	V3	29	0	DRAWING	
				5	VERIFICATION	
MET4	Metal 4	M4	31	0	DRAWING	
				1	DUMMY	defined as M4DUMMY
				2	SLOT	defined as M4SLOT
				3	TEXT	defines top level nets
				4	DMYBLK	blocks dummy generation, Design related guidelines must be considered
				5	VERIFICATION	defined as M4VERIFY
				9	net	defines net shapes
				10	boundary	
				15	VLABEL	defines voltage classes

2.2.4 MET5 module

Name	Description	Code	GDS#	Data type	Purpose	Comments
VIA4	Via 4	V4	32	0	DRAWING	
				5	VERIFICATION	

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2. General → 2.2 Design layers→ 2.2.4 MET5 module

Name	Description	Code	GDS#	Data type	Purpose	Comments
MET5	Metal 5	M5	50	0	DRAWING	
				1	DUMMY	defined as M5DUMMY
				2	SLOT	defined as M5SLOT
				3	TEXT	defines top level nets
				4	DMYBLK	blocks dummy generation, Design related guidelines must be considered
				5	VERIFICATION	defined as M5VERIFY
				9	net	defines net shapes
				10	boundary	
				15	VLABEL	defines voltage classes

2.2.5 METMID module

Name	Description	Code	GDS#	Data type	Purpose	Comments
VIATP	Top Via	VT	51	0	DRAWING	
				5	VERIFICATION	
METTP	Top Metal	MT	33	0	DRAWING	
				1	DUMMY	defined as MTPDUMMY
				2	SLOT	defined as MTPSLOT
				3	TEXT	defines top level nets
				4	DMYBLK	blocks dummy generation, Design related guidelines must be considered
				5	VERIFICATION	defined as MTPVERIFY
				9	net	defines net shapes
				10	boundary	
				15	VLABEL	defines voltage classes

2.2.6 METTHK module

Name	Description	Code	GDS#	Data type	Purpose	Comments
VIATPL	Thick Via	VL	36	0	DRAWING	
				0	DRAWING	
METTPL	Thick Metal	ML	35	1	DUMMY	defined as MTPLDUMMY
				3	TEXT	defines top level nets
				4	DMYBLK	blocks dummy generation, Design related guidelines must be considered
				5	VERIFICATION	defined as MLVERIFY
				9	net	defines net shapes
				10	boundary	
				15	VLABEL	defines voltage classes

2. General → 2.2 Design layers → 2.2.7 CPOD module

2.2.7 CPOD module

Name	Description	Code	GDS#	Data type	Purpose	Comments
BNIMP	CPOD N+ implant	NU	207	0	DRAWING	

2.2.8 CPODHV module

Name	Description	Code	GDS#	Data type	Purpose	Comments
HVGDX	Thick Gate Oxide	GH	85	0	DRAWING	

2.2.9 MRPOLY module

Name	Description	Code	GDS#	Data type	Purpose	Comments
MRES	lightly P+ Poly Implant	MR	42	0	DRAWING	

2.2.10 ISOMOS module

Name	Description	Code	GDS#	Data type	Purpose	Comments
DNWELLMV	Deep N-well (middle Volt)	WM	96	0	DRAWING	Deep N-well with reduced well edge design rules for middle volt applications
ISOPW				5	VERIFICATION	defined as DNWMV_VERIFY
ISOPW	Isolated P-well	PI	95	0	DRAWING	

2.2.11 ISOMOS2 module

Name	Description	Code	GDS#	Data type	Purpose	Comments
DNWELL	Deep N-well	WD	68	0	DRAWING	
HVPWELL	High Voltage Pwell	HP	86	0	DRAWING	

2.2.12 LVT module

Name	Description	Code	GDS#	Data type	Purpose	Comments
LVT	LVT Implant	LV	39	0	DRAWING	

2.2.13 SVT module

Name	Description	Code	GDS#	Data type	Purpose	Comments
SVT	SVT Implant	SV	309	0	DRAWING	

2.2.14 LNPMOS3 module

Name	Description	Code	GDS#	Data type	Purpose	Comments
LNDEV	Low Noise Device	LD	44	0	DRAWING	

2.2.15 ULN module

Name	Description	Code	GDS#	Data type	Purpose	Comments
ULN	Low Noise CMOS	UL	298	0	DRAWING	

2. General → 2.2 Design layers → 2.2.16 DEPL module

2.2.16 DEPL module

Name	Description	Code	GDS#	Data type	Purpose	Comments
DEPL	Depletion	DL	92	0	DRAWING	

2.2.17 HVDEPL module

Name	Description	Code	GDS#	Data type	Purpose	Comments
HVDEPL	high voltage depletion	HL	114	0	DRAWING	

2.2.18 DMOS module

Name	Description	Code	GDS#	Data type	Purpose	Comments
PDD	DMOS Drift implant	PT	89	0	DRAWING	not allowed for customer use. Layer for predefined devices in the modules DMOS and HALL only.

2.2.19 HVMOS module

Name	Description	Code	GDS#	Data type	Purpose	Comments
DNWELL	Deep N-well	WD	68	0	DRAWING	
DNWELLMV	Deep N-well (middle Volt)	WM	96	0	DRAWING	Deep N-well with reduced well edge design rules for middle volt applications
				5	VERIFICATION	defined as DNWMV_VERIFY
HVGOX	Thick Gate Oxide	GH	85	0	DRAWING	
HVNWELL	High Voltage Nwell	HN	87	0	DRAWING	
HVPWELL	High Voltage Pwell	HP	86	0	DRAWING	

2.2.20 HVNMOS module

Name	Description	Code	GDS#	Data type	Purpose	Comments
HVGOX	Thick Gate Oxide	GH	85	0	DRAWING	
HVPWELL	High Voltage Pwell	HP	86	0	DRAWING	

2.2.21 NHVE module

Name	Description	Code	GDS#	Data type	Purpose	Comments
NDF	N drift implant	ND	146	0	DRAWING	

2.2.22 HVPMOS module

Name	Description	Code	GDS#	Data type	Purpose	Comments
HNW	Diffused HV N-well (high voltage)	HW	145	0	DRAWING	
HVGOX	Thick Gate Oxide	GH	85	0	DRAWING	
HVNWELL	High Voltage Nwell	HN	87	0	DRAWING	
HVPWELL	High Voltage Pwell	HP	86	0	DRAWING	

2. General → 2.2 Design layers→ 2.2.22 HVMOS module

Name	Description	Code	GDS#	Data type	Purpose	Comments
NDF	N drift implant	ND	146	0	DRAWING	

2.2.23 PHVE module

Name	Description	Code	GDS#	Data type	Purpose	Comments
PDF	P Drift Implant	PD	147	0	DRAWING	

2.2.24 SCHOTTKY module

Name	Description	Code	GDS#	Data type	Purpose	Comments
DNC	Deep N-contact	NC	132	0	DRAWING	not allowed for customer use. Layer for predefined devices in the modules SCHOTTKY and HALL only.
HNW	Diffused HV N-well (high voltage)	HW	145	0	DRAWING	
HVPWELL	High Voltage Pwell	HP	86	0	DRAWING	

2.2.25 MIM module

Name	Description	Code	GDS#	Data type	Purpose	Comments
CAPM	Single MIM Top Plate Metal	CM	47	0	DRAWING	

2.2.26 MIM23 module

Name	Description	Code	GDS#	Data type	Purpose	Comments
CAPM23F	Single MIM Top Plate Metal	C3	115	0	DRAWING	

2.2.27 MIM34 module

Name	Description	Code	GDS#	Data type	Purpose	Comments
CAPM34F	Single MIM Top Plate Metal	C4	117	0	DRAWING	

2.2.28 DMIM module

Name	Description	Code	GDS#	Data type	Purpose	Comments
CAPM2	Double MIM Capacitor Metal	DM	37	0	DRAWING	

2.2.29 TMIM module

Name	Description	Code	GDS#	Data type	Purpose	Comments
CAPM3	Triple MIM Capacitor Metal	TM	38	0	DRAWING	

2. General → 2.2 Design layers→ 2.2.30 MIMH module

2.2.30 MIMH module

Name	Description	Code	GDS#	Data type	Purpose	Comments
CAPMH	Single High Capacitance MIM Top Plate Metal	CH	173	0	DRAWING	

2.2.31 MIMH23 module

Name	Description	Code	GDS#	Data type	Purpose	Comments
CAPMH23F	Single High Capacitance MIM Top Plate Metal	H3	116	0	DRAWING	

2.2.32 MIMH34 module

Name	Description	Code	GDS#	Data type	Purpose	Comments
CAPMH34F	Single High Capacitance MIM Top Plate Metal	H4	118	0	DRAWING	

2.2.33 DMIMH module

Name	Description	Code	GDS#	Data type	Purpose	Comments
CAPMH2	Double High Capacitance MIM Top Plate Metal	DH	174	0	DRAWING	

2.2.34 TMIMH module

Name	Description	Code	GDS#	Data type	Purpose	Comments
CAPMH3	Triple High Capacitance MIM Top Plate Metal	TH	175	0	DRAWING	

2.2.35 NVM module

Name	Description	Code	GDS#	Data type	Purpose	Comments
SCI	SONOS channel implant	SC	90	0	DRAWING	not allowed for customer use

2.2.36 ANODOP module

Name	Description	Code	GDS#	Data type	Purpose	Comments
ANODOP	UV Anode	OA	126	0	DRAWING	

2.2.37 CATDOP module

Name	Description	Code	GDS#	Data type	Purpose	Comments
CATDOP	Cathode Implant	OC	127	0	DRAWING	

2.2.38 UVWINDOW module

Name	Description	Code	GDS#	Data type	Purpose	Comments
UVWIN	UV Window	UV	125	0	DRAWING	

2. General → 2.2 Design layers→ 2.2.39 AVLA module

2.2.39 AVLA module

Name	Description	Code	GDS#	Data type	Purpose	Comments
AML	Avalanche multiplication implant	AM	45	0	DRAWING	

2.2.40 BIPESD module

Name	Description	Code	GDS#	Data type	Purpose	Comments
HNW	Diffused HV N-well (high voltage)	HW	145	0	DRAWING	
HVPWELL	High Voltage Pwell	HP	86	0	DRAWING	
PDF	P Drift Implant	PD	147	0	DRAWING	

2.2.41 ESDPNP module

Name	Description	Code	GDS#	Data type	Purpose	Comments
HNW	Diffused HV N-well (high voltage)	HW	145	0	DRAWING	
HVGOX	Thick Gate Oxide	GH	85	0	DRAWING	
HVNWELL	High Voltage Nwell	HN	87	0	DRAWING	
HVPWELL	High Voltage Pwell	HP	86	0	DRAWING	

2.2.42 PIMIDE module

Name	Description	Code	GDS#	Data type	Purpose	Comments
NOPIM	No Polyimide	IB	46	0	DRAWING	

2.2.43 HALL module

Name	Description	Code	GDS#	Data type	Purpose	Comments
DNC	Deep N-contact	NC	132	0	DRAWING	not allowed for customer use. Layer for predefined devices in the modules SCHOTTKY and HALL only.
DPC	Deep P-contact	PC	134	0	DRAWING	not allowed for customer use. Layer for predefined devices in the module HALL only.
HVNWELL	High Voltage Nwell	HN	87	0	DRAWING	
HVPWELL	High Voltage Pwell	HP	86	0	DRAWING	
PDD	DMOS Drift implant	PT	89	0	DRAWING	not allowed for customer use. Layer for predefined devices in the modules DMOS and HALL only.

2. General → 2.3 Mask layers

2.3 Mask layers

The layout rules are defined in microns and bear some physical relationship to the finished on-silicon dimensions. Changes and biases will be generated during the process of mask making / Pattern Generation (under control of the X-FAB Semiconductor Foundries) to produce the declared electrical feature sizes which are the only maintained parameters.

The Mask Layers are produced from the Design Layers by manipulation during the mask data preparation activity.

Sizing values used for process mask manufacturing have not been included here.

According to the mask generation and mask sizing procedure, change to data on a design layer could result in more than one mask layer being affected. Additionally, some details of the mask data preparation are factory specific.

The order of the process layers in the table does not infer any process sequence.

2.3.1 LPMOS main module

Name	Mask ID	GDS#	Generated from drawn design layers
CONT	CON	15	= CONT
DIFF	ACT	3	= DIFF (DRAWING OR DUMMY)
LDN	LDN	61	derived from SPECIAL1, NIMP, ISOPW, MV, and HRES
LDP	LDP	54	derived from PIMP, NWELL, and MV
LNM	LNM	94	derived from SPECIAL2, NIMP, NWELL, HVNWELL, DNWELL, DNWELLMV, ISOPW, DEPL, SCI, MV, and HRES
LPM	LPM	93	derived from SPECIAL3, PIMP, NW, MV, HVNWELL, DEPL
MET1	M1	16	= MET1 (((DRAWING OR net) AND NOT SLOT) OR DUMMY)
MET2	M2	18	= MET2 (((DRAWING OR net) AND NOT SLOT) OR DUMMY)
MV	MV	4	= MV OR HVGOX OR SPECIAL6
NIMP	NP	8	= NIMP
NWELL1	NW1	79	derived from NWELL, MV, DNC and SVT
NWELL2	NW2	81	derived from NWELL, MV, DNC and LNDEV
PAD	PAD	19	= PAD or UVWIN
PIMP	PP	7	= PIMP
POLY1	GP	13	= POLY1 (DRAWING OR DUMMY)
PWELL1	PW1	80	derived from SPECIAL1, ISOPW , MV, DPC and SVT
PWELL2	PW2	82	derived from SPECIAL1, ISOPW, MV and DPC
SBLK	SAB	34	= SBLK
VIA1	V1	17	= VIA1

2.3.2 MET3 module

Name	Mask ID	GDS#	Generated from drawn design layers
MET3	M3	28	= MET3 (((DRAWING OR net) AND NOT SLOT) OR DUMMY)
VIA2	V2	27	= VIA2

2.3.3 MET4 module

Name	Mask ID	GDS#	Generated from drawn design layers
MET4	M4	31	= MET4 (((DRAWING OR net) AND NOT SLOT) OR DUMMY)
VIA3	V3	29	= VIA3

2. General → 2.3 Mask layers → 2.3.4 MET5 module

2.3.4 MET5 module

Name	Mask ID	GDS#	Generated from drawn design layers
MET5	M5	50	= MET5 (((DRAWING OR net) AND NOT SLOT) OR DUMMY)
VIA4	V4	32	= VIA4

2.3.5 METMID module

Name	Mask ID	GDS#	Generated from drawn design layers
METTP	MTP	33	= METTP (((DRAWING OR net) AND NOT SLOT) OR DUMMY)
VIATP	VTP	51	= VIATP

2.3.6 METTHK module

Name	Mask ID	GDS#	Generated from drawn design layers
METTPL	MPL	35	= METTPL ((DRAWING OR net) OR DUMMY)
VIATPL	VPL	36	= VIATPL

2.3.7 CPOD module

Name	Mask ID	GDS#	Generated from drawn design layers
CPOD	CPD	207	= BNIMP

2.3.8 CPODHV module

Name	Mask ID	GDS#	Generated from drawn design layers
HVGOX	GXH	85	= HVGOX
SSD	SSD	91	derived from HVGOX, DIFF, and POLY1

2.3.9 MRPOLY module

Name	Mask ID	GDS#	Generated from drawn design layers
MRPOLY	LPP	42	= MRES

2.3.10 ISOMOS module

Name	Mask ID	GDS#	Generated from drawn design layers
DNWELL	DNW	68	= DNWELL OR DNWELLMV

2.3.11 ISOMOS2 module

Name	Mask ID	GDS#	Generated from drawn design layers
HVPWELL	PBD	86	= HVPWELL

2.3.12 LVT module

Name	Mask ID	GDS#	Generated from drawn design layers
NWELL3	NW3	30	derived from NWELL, MV, DNC, LVT and SVT

2. General → 2.3 Mask layers→ 2.3.12 LVT module

Name	Mask ID	GDS#	Generated from drawn design layers
PWELL3	PW3	49	derived from SPECIAL1, ISOPW, MV, DPC, LVT and SVT

2.3.13 SVT module

Name	Mask ID	GDS#	Generated from drawn design layers
NWELL5	NW5	307	derived from NWELL, MV, DNC, and SVT
PWELL5	PW5	308	derived from SPECIAL1, ISOPW, MV, DPC, and SVT

2.3.14 LNPMOS3 module

Name	Mask ID	GDS#	Generated from drawn design layers
NWELL4	NW4	103	derived from NWELL, MV and LNDEV

2.3.15 ULN module

Name	Mask ID	GDS#	Generated from drawn design layers
ULN	ULN	298	= ULN

2.3.16 DEPL module

Name	Mask ID	GDS#	Generated from drawn design layers
DEPL	DPL	92	= DEPL

2.3.17 HVDEPL module

Name	Mask ID	GDS#	Generated from drawn design layers
HVDEPL	HPL	114	= HVDEPL

2.3.18 DMOS module

Name	Mask ID	GDS#	Generated from drawn design layers
PDD	PDD	89	= PDD

2.3.19 HVMOS module

Name	Mask ID	GDS#	Generated from drawn design layers
DNWELL	DNW	68	= DNWELL OR DNWELLMV
HVGDX	GXH	85	= HVGDX
HVNWELL	NBD	87	= HVNWELL
HVPWELL	PBD	86	= HVPWELL
SSD	SSD	91	derived from HVGDX, DIFF, and POLY1

2.3.20 HVNMOS module

Name	Mask ID	GDS#	Generated from drawn design layers
HVGDX	GXH	85	= HVGDX
HVPWELL	PBD	86	= HVPWELL

2. General → 2.3 Mask layers→ 2.3.20 HVNMOS module

Name	Mask ID	GDS#	Generated from drawn design layers
SSD	SSD	91	derived from HVGOX, DIFF, and POLY1

2.3.21 NHVE module

Name	Mask ID	GDS#	Generated from drawn design layers
NDF	NDF	146	= NDF

2.3.22 HVP MOS module

Name	Mask ID	GDS#	Generated from drawn design layers
HNW	HNW	145	= HNW
HVGOX	GXH	85	= HVGOX
HVN WELL	NBD	87	= HVN WELL
HVP WELL	PBD	86	= HVP WELL
NDF	NDF	146	= NDF
SSD	SSD	91	derived from HVGOX, DIFF, and POLY1

2.3.23 PHVE module

Name	Mask ID	GDS#	Generated from drawn design layers
PDF	PDF	147	= PDF

2.3.24 SCHOTTKY module

Name	Mask ID	GDS#	Generated from drawn design layers
HNW	HNW	145	= HNW
HVP WELL	PBD	86	= HVP WELL

2.3.25 MIM module

Name	Mask ID	GDS#	Generated from drawn design layers
CAPM	CM	47	= CAPM

2.3.26 MIM23 module

Name	Mask ID	GDS#	Generated from drawn design layers
CAPM	CM	47	= CAPM23F

2.3.27 MIM34 module

Name	Mask ID	GDS#	Generated from drawn design layers
CAPM	CM	47	= CAPM34F

2.3.28 DMIM module

Name	Mask ID	GDS#	Generated from drawn design layers
CAPM	CM	47	= CAPM2

2. General → 2.3 Mask layers→ 2.3.29 TMIM module

2.3.29 TMIM module

Name	Mask ID	GDS#	Generated from drawn design layers
CAPM	CM	47	= CAPM3

2.3.30 MIMH module

Name	Mask ID	GDS#	Generated from drawn design layers
CAPMH	CMH	173	= CAPMH

2.3.31 MIMH23 module

Name	Mask ID	GDS#	Generated from drawn design layers
CAPMH	CMH	173	= CAPMH23F

2.3.32 MIMH34 module

Name	Mask ID	GDS#	Generated from drawn design layers
CAPMH	CMH	173	= CAPMH34F

2.3.33 DMIMH module

Name	Mask ID	GDS#	Generated from drawn design layers
CAPMH	CMH	173	= CAPMH2

2.3.34 TMIMH module

Name	Mask ID	GDS#	Generated from drawn design layers
CAPMH	CMH	173	= CAPMH3

2.3.35 NVM module

Name	Mask ID	GDS#	Generated from drawn design layers
SCI	SCI	90	= SCI
SOC	SOC	97	derived from SCI and DIFF

2.3.36 ANODOP module

Name	Mask ID	GDS#	Generated from drawn design layers
ANODOP	OA	126	= ANODOP

2.3.37 CATDOP module

Name	Mask ID	GDS#	Generated from drawn design layers
CATDOP	OC	127	= CATDOP

2. General → 2.3 Mask layers→ 2.3.38 AVLA module

2.3.38 AVLA module

Name	Mask ID	GDS#	Generated from drawn design layers
AML	AML	45	= AML

2.3.39 BIPESD module

Name	Mask ID	GDS#	Generated from drawn design layers
HNW	HNW	145	= HNW
HVPWELL	PBD	86	= HVPWELL
PDF	PDF	147	= PDF

2.3.40 ESDPNP module

Name	Mask ID	GDS#	Generated from drawn design layers
HNW	HNW	145	= HNW
HVGOX	GXH	85	= HVGOX
HVNWELL	NBD	87	= HVNWELL
HVPWELL	PBD	86	= HVPWELL
SSD	SSD	91	derived from HVGOX, DIFF, and POLY1

2.3.41 PIMIDE module

Name	Mask ID	GDS#	Generated from drawn design layers
PIMIDE	PIB	46	= NOPIM OR (PAD + sizing)

2.3.42 HALL module

Name	Mask ID	GDS#	Generated from drawn design layers
HVNWELL	NBD	87	= HVNWELL
HVPWELL	PBD	86	= HVPWELL
PDD	PDD	89	= PDD

2. General → 2.4 Definitions

2.4 Definitions

The 2-character code is intended for rule codes. The rule codes are used for short design rule check error messages.

Name	Code	Logical
BM	BM	single MIM bottom metal layer (differs with the selected metal option) see also "Table for BM and VIA assignment"
BNDIFF		Buried N+ diffusion (BNIMP AND DIFF)
CATDIFF	DC	DIFF and CATDOP
DIFFCON	CT	diffusion contact (DIFF AND CONT)
DIFFDUMMY	YD	DIFF purpose DUMMY
DNWMV_VERIFY		DNWELLMV purpose VERIFICATION
DNW_VERIFY		DNWELL purpose VERIFICATION
EXTENT		least enclosing rectangle of the database
GATE	GA	gate area (POLY1 AND DIFF)
GUARD RING		ring shaped DIFF area for well contacts
ISOWELL	IW	Isolated wells ((ISOPW or DEPL or SCI) and (DNWELL or DNWELLMV))
M1DUMMY	Y1	MET1 purpose DUMMY
M1SLOT		MET1 purpose SLOT
M1VERIFY		MET1 purpose VERIFICATION
M2DUMMY	Y2	MET2 purpose DUMMY
M2SLOT		MET2 purpose SLOT
M2VERIFY		MET2 purpose VERIFICATION
M3DUMMY	Y3	MET3 purpose DUMMY
M3SLOT		MET3 purpose SLOT
M3VERIFY		MET3 purpose VERIFICATION
M4DUMMY	Y4	MET4 purpose DUMMY
M4SLOT		MET4 purpose SLOT
M4VERIFY		MET4 purpose VERIFICATION
M5DUMMY	Y5	MET5 purpose DUMMY
M5SLOT		MET5 purpose SLOT
M5VERIFY		MET5 purpose VERIFICATION
MET1HV		high voltage MET1: MET1 over NTYPE_WELL OR PTYPE_WELL OR PWBLK, if VMET1-VWELL > 35V
MET2HV		high voltage MET2: MET2 over HNW, if VMET2-VWELL > 35V
MLVERIFY		METTPL purpose VERIFICATION
MTPDUMMY	YT	METTP purpose DUMMY
MTPLDUMMY	YL	METTPL purpose DUMMY
MTPSLOT		METTP purpose SLOT
MTPVERIFY		METTP purpose VERIFICATION
NDIFF	DN	N+ diffusion (DIFF AND NIMP)
NTYPE1_WELL		NTYPE_WELL AND NOT PTYPE_WELL
NTYPE_WELL		n-doped well (NWELL OR HVNWELL OR DNWELLMV OR DNWELL OR HNW OR NDF OR DNC)
NW4DMY	NW	= NWELL OR HVNWELL OR DNC OR NDF
NWELL1	W1	1.8V N-well (((NWELL AND NOT MV) AND NOT LVT) AND NOT SVT) OR DNC)
NWELL2	W3	3.3V N-well (((MV AND NWELL) OR DNC) AND NOT LNDEV)



2. General → 2.4 Definitions

Name	Code	Logical
NWELL3	W5	1.8V N-well (((NWELL AND NOT MV) OR DNC) AND LVT)
NWELL4	W7	3.3V N-well ((MV AND NWELL) AND LNDEV)
NWELL5	W9	1.8V N-well ((NWELL AND NOT MV) AND SVT)
NW_VERIFY		NWELL purpose VERIFICATION
OPTOVIA1	V1	VIA1 stripes AND (VIA1 purpose VERIFICATION)
OPTOVIA2	V2	VIA2 stripes AND (VIA2 purpose VERIFICATION)
OPTOVIA3	V3	VIA3 stripes AND (VIA3 purpose VERIFICATION)
OPTOVIA4	V4	VIA4 stripes AND (VIA4 purpose VERIFICATION)
OPTOVIATP	VT	VIATP stripes AND (VIATP purpose VERIFICATION)
P1DUMMY	YP	POLY1 purpose DUMMY
PDIFF	DP	P+ diffusion (DIFF AND PIMP)
PHODIO	D1	PHODEF AND DIODEF
POLY1HV		high voltage POLY1: POLY1 over NTYPE_WELL OR PTYPE_WELL OR PWBLK, if VPOLY1-VWELL > 4 V
POLY1_VERIFY		POLY1 purpose VERIFICATION
PSUB		p-Epi layer in p- substrate
PTYPE_WELL		p-doped well (PWELL OR ISOPW OR HVPWELL OR DEPL OR SCI OR PDD OR PDF OR DPC)
PW4DMY	PI	= ISOPW OR HVPWELL OR PDD OR PDF OR DEPL OR SCI OR DPC
PWELL1	W2	1.8V P-well (((((NOT (NTYPE_WELL OR HVPWELL OR DEPL OR SCI OR PDD) AND NOT MV) AND NOT PWBLK) OR (ISOPW AND NOT MV)) AND NOT LVT) AND NOT SVT) OR DPC)
PWELL2	W4	3.3V P-well (((MV AND NOT (NTYPE_WELL OR DEPL OR SCI OR PWBLK OR HVPWELL OR PDD) OR (ISOPW AND MV)) OR DPC)
PWELL3	W6	1.8V P-well (((((NOT (NTYPE_WELL OR HVPWELL OR DEPL OR SCI OR PDD) AND NOT MV) AND NOT PWBLK) OR (ISOPW AND NOT MV) OR DPC) AND LVT)
PWELL5	W10	1.8V P-well (((((NOT (NTYPE_WELL OR HVPWELL OR DEPL OR SCI OR PDD) AND NOT MV) AND NOT PWBLK) OR (ISOPW AND NOT MV) AND SVT)
SPECIAL1		= DNWELL OR DNWELLMV OR NWELL OR HVNWELL OR HVPWELL OR PDD OR SCI OR DEPL OR PWBLK OR HNW OR NDF OR PDF OR DNC
SPECIAL2		= (HVPWELL OR PDF) AND NIMP AND HVGOX
SPECIAL3		= (HVNWELL OR NDF) AND PIMP AND HVGOX
SPECIAL6		= ((DNWELL OR DNWELLMV) AND NOT (NWELL OR ISOPW OR DEPL)) OR HVNWELL OR HVPWELL OR SCI
VIA _n	VN	VIA (except VIATP) to connect the single MIM bottom layer (differs with the selected metal option) see also "Table for BM and VIA _n assignment"
WIDE_MET1		MET1 width and length > 10 µm
		Note: The wide metal definition includes all extensions from the wide metal which extend by 1.0µm or less from the wide piece.
WIDE_MET2		MET2 width and length > 10 µm
		Note: The wide metal definition includes all extensions from the wide metal which extend by 1.0µm or less from the wide piece.
WIDE_MET3		MET3 width and length > 10 µm
		Note: The wide metal definition includes all extensions from the wide metal which extend by 1.0µm or less from the wide piece.
WIDE_MET4		MET4 width and length > 10 µm
		Note: The wide metal definition includes all extensions from the wide metal which extend by 1.0µm or less from the wide piece.



2. General → 2.4 Definitions

Name	Code	Logical
WIDE_MET5		MET5 width and length > 10 µm
		Note: The wide metal definition includes all extensions from the wide metal which extend by 1.0µm or less from the wide piece.
WIDE_METTP		METTP width and length > 10 µm
		Note: The wide metal definition includes all extensions from the wide metal which extend by 1.0µm or less from the wide piece.
cpod#		cpod, cpodhv
davla#		dapda, dapda0, dspada, dspada0
dphoc#		dphoc, dphoc0, dphocfp
dphod#		dphod, dphod0, dphodfp
dsb#		dsb, dsba
ned#		nedi, nedia
nh#		nhhv, nhv, nhhvd, nhvd
nm#		nmmc, nmc, nmmd
ped#		ped, ped2
ph#		phhv, phv
pm#		pmmc, pmc
rnp1#		rnp1, rnp1_3
rnp1h#		rnp1h, rnp1h_3
rpp1#		rpp1, rpp1_3
rpp1k1#		rpp1k1, rpp1k1_3
rpp1s#		rpp1s, rpp1s_3

2. General → 2.5 Primitive devices

2.5 Primitive devices

The primitive device list does not include all the required module combinations for the stated modules. Refer also to the Module restrictions tables.

In addition to the capacitors stated in the primitive device list, it is also possible to use the capacitors built by the different gate oxides. These capacitors can be simulated by using the model of a transistor which has the respective oxide: for instance the ne and pe models in case of the 1.8V gate oxide. The operating conditions of the relating transistors are valid as well for these capacitors.

Minor changes of the simulation models might be generated due to continuous improvement of device and circuit simulation. Minor changes of models are described within the actual model data files. Please refer to further information within the current model path.

The qualification status of single devices can be checked in the Application Note "[Primitive device release status](#)" available at "my X-FAB"

The following devices are available for design:

2.5.1 LPMOS main module

MOS transistors

Name	Description	Required modules	Model rev.
ne	1.8V low power NMOS	-	4.0
pe	1.8V low power PMOS 4 terminals	-	4.0
pe_5 ⁽¹⁾	1.8V low power PMOS 5 terminals	-	5.0
nel	1.8V low VT NMOS	LVT	6.0
pel	1.8V low VT PMOS 4 terminals	LVT	6.0
pel_5 ⁽¹⁾	1.8V low VT PMOS 5 terminals	LVT	6.0
nei ⁽²⁾	isolated 1.8V low power NMOS 4 terminals	ISOMOS	4.0
nei_6 ⁽¹⁾	isolated 1.8V low power NMOS in DNWELL 6 terminals	ISOMOS2 or (ISOMOS and HVMOS)	4.0
nei_m_6 ⁽¹⁾	isolated 1.8V low power NMOS in DNWELLMV 6 terminals	ISOMOS	4.0
pei ⁽²⁾	isolated 1.8V low power PMOS 4 terminals	ISOMOS	4.0
pei_5 ⁽¹⁾	isolated 1.8V low power PMOS in DNWELL 5 terminals	ISOMOS2 or (ISOMOS and HVMOS)	5.0
pei_m_5 ⁽¹⁾	isolated 1.8V low power PMOS in DNWELLMV 5 terminals	ISOMOS	5.0
neli ⁽²⁾	isolated 1.8V low VT NMOS 4 terminals	LVT and ISOMOS	6.0
neli_6 ⁽¹⁾	isolated 1.8V low VT NMOS in DNWELL 6 terminals	LVT and (ISOMOS2 or (ISOMOS and HVMOS))	6.0
neli_m_6 ⁽¹⁾	isolated 1.8V low VT NMOS in DNWELLMV 6 terminals	LVT and ISOMOS	6.0
peli ⁽²⁾	isolated 1.8V low VT PMOS 4 terminals	LVT and ISOMOS	6.0
peli_5 ⁽¹⁾	isolated 1.8V low VT PMOS in DNWELL 5 terminals	LVT and (ISOMOS2 or (ISOMOS and HVMOS))	6.0
peli_m_5 ⁽¹⁾	isolated 1.8V low VT PMOS in DNWELLMV 5 terminals	LVT and ISOMOS	6.0
nesvt	1.8V medium VT NMOS	SVT	7.0
nesvti ⁽²⁾	isolated 1.8V medium VT NMOS 4 terminals	SVT and ISOMOS	7.0
nesvti_6 ⁽¹⁾	isolated 1.8V medium VT NMOS in DNWELL 6 terminals	SVT and (ISOMOS2 or (ISOMOS and HVMOS))	7.0
nesvti_m_6 ⁽¹⁾	isolated 1.8V medium VT NMOS in DNWELLMV 6 terminals	SVT and ISOMOS	7.0

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2. General → 2.5 Primitive devices→ 2.5.1 LPMOS main module→ MOS transistors

Name	Description	Required modules	Model rev.
pesvt	1.8V medium VT PMOS 4 terminals	SVT	7.0
pesvt_5 ⁽¹⁾	1.8V medium VT PMOS 5 terminals	SVT	7.0
pesvti ⁽²⁾	isolated 1.8V medium VT PMOS 4 terminals	SVT and ISOMOS	7.0
pesvti_5 ⁽¹⁾	isolated 1.8V medium VT PMOS in DNWELL 5 terminals	SVT and (ISOMOS2 or (ISOMOS and HVMOS))	7.0
pesvti_m_5 ⁽¹⁾	isolated 1.8V medium VT PMOS in DNWELLMV 5 terminals	SVT and ISOMOS	7.0
nelna	1.8V low noise NMOS	ULN	7.0
nelnai ⁽²⁾	isolated 1.8V low noise NMOS 4 terminals	ULN and ISOMOS	7.0
nelnai_6 ⁽¹⁾	isolated 1.8V low noise NMOS in DNWELL 6 terminals	ULN and (ISOMOS2 or (ISOMOS and HVMOS))	7.0
nelnai_m_6 ⁽¹⁾	isolated 1.8V low noise NMOS in DNWELLMV 6 terminals	ULN and ISOMOS	7.0
nn3	3.3V native Vt NMOS	-	7.1
ne3	3.3V low power NMOS	-	4.1
pe3	3.3V low power PMOS 4 terminals	-	4.1
pe3_5 ⁽¹⁾	3.3V low power PMOS 5 terminals	-	5.0
ne3i ⁽²⁾	isolated 3.3V low power NMOS 4 terminals	ISOMOS	4.1
ne3i_6 ⁽¹⁾	isolated 3.3V low power NMOS in DNWELL 6 terminals	ISOMOS2 or (ISOMOS and HVMOS)	4.1
ne3i_m_6 ⁽¹⁾	isolated 3.3V low power NMOS in DNWELLMV 6 terminals	ISOMOS	4.1
pe3i ⁽²⁾	isolated 3.3V low power PMOS 4 terminals	ISOMOS	4.1
pe3i_5 ⁽¹⁾	isolated 3.3V low power PMOS in DNWELL 5 terminals	ISOMOS2 or (ISOMOS and HVMOS)	5.0
pe3i_m_5 ⁽¹⁾	isolated 3.3V low power PMOS in DNWELLMV 5 terminals	ISOMOS	5.0
ne3lna	3.3V low noise NMOS	ULN	7.0
ne3lnai ⁽²⁾	isolated 3.3V low noise NMOS 4 terminals	ULN and ISOMOS	7.0
ne3lnai_6 ⁽¹⁾	isolated 3.3V low noise NMOS in DNWELL 6 terminals	ULN and (ISOMOS2 or (ISOMOS and HVMOS))	7.0
ne3lnai_m_6 ⁽¹⁾	isolated 3.3V low noise NMOS in DNWELLMV 6 terminals	ULN and ISOMOS	7.0
pe3lna	3.3V low noise PMOS 4 terminals	ULN	7.0
pe3lna_5 ⁽¹⁾	3.3V low noise PMOS 5 terminals	ULN	7.0
pe3lnai ⁽²⁾	isolated 3.3V low noise PMOS 4 terminals	ULN and ISOMOS	7.0
pe3lnai_5 ⁽¹⁾	isolated 3.3V low noise PMOS in DNWELL 5 terminals	ULN and (ISOMOS2 or (ISOMOS and HVMOS))	7.0
pe3lnai_m_5 ⁽¹⁾	isolated 3.3V low noise PMOS in DNWELLMV 5 terminals	ULN and ISOMOS	7.0
pe3ln	3.3V low noise PMOS 4 terminals	LNPMOS3	6.1
pe3ln_5 ⁽¹⁾	3.3V low noise PMOS 5 terminals	LNPMOS3	6.1
pe3lni ⁽²⁾	isolated 3.3V low noise PMOS 4 terminals	LNPMOS3 and ISOMOS	6.1
pe3lni_5 ⁽¹⁾	isolated 3.3V low noise PMOS in DNWELL 5 terminals	LNPMOS3 and (ISOMOS2 or (ISOMOS and HVMOS))	6.1

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2. General → 2.5 Primitive devices→ 2.5.1 LPMOS main module→ MOS transistors

Name	Description	Required modules	Model rev.
pe3lni_m_5 ⁽¹⁾	isolated 3.3V low noise PMOS in DNWELLMV 5 terminals	LNPMOS3 and ISOMOS	6.1
nd3	3.3V depletion NMOS	DEPL	4.0
nd3i ⁽²⁾	isolated 3.3V depletion NMOS 4 terminals	(DEPL and ISOMOS) or (DEPL and HVMOS)	4.0
nd3i_6 ⁽¹⁾	isolated 3.3V depletion NMOS in DNWELL 6 terminals	DEPL and HVMOS	4.0
nd3i_m_6 ⁽¹⁾	isolated 3.3V depletion NMOS in DNWELLMV 6 terminals	DEPL and ISOMOS	4.0
nmma	10V HV NMOS	HVMOS	7.0
nmma_bjt ⁽³⁾	nmma with additional parasitic bjt model	HVMOS	7.0
pmma	15V HV PMOS	HVMOS	7.0
pmma_bjt ⁽³⁾	pmma with additional parasitic bjt model	HVMOS	7.0
nedi ⁽⁴⁾ ⁽⁵⁾	isolated 40V lateral n-DMOS	DMOS	7.0
nedi_bjt ⁽³⁾ ⁽⁴⁾ ⁽⁵⁾	nedi with additional parasitic bjt model	DMOS	7.0
nedia ⁽⁵⁾	isolated 45V lateral n-DMOS	DMOS	6.1
nedia_bjt ⁽³⁾ ⁽⁵⁾	nedia with additional parasitic bjt model	DMOS	6.1
ped2	35V lateral p-DMOS	DMOS	6.1
ped2_bjt ⁽³⁾	ped2 with additional parasitic bjt model	DMOS	6.1
ped	45V lateral p-DMOS	DMOS	6.1
ped_bjt ⁽³⁾	ped with additional parasitic bjt model	DMOS	6.1
nhv	45V asymmetrical HV NMOS	NHVE	7.0
nhv_bjt ⁽³⁾	nhv with additional parasitic bjt model	NHVE	7.0
nhhv	45V symmetrical HV NMOS	NHVE	7.0
nhhv_bjt ⁽³⁾	nhhv with additional parasitic bjt model	NHVE	7.0
nmc	10V asymmetrical HV NMOS	NHVE	7.0
nmc_bjt ⁽³⁾	nmc with additional parasitic bjt model	NHVE	7.0
nmmc	15V symmetrical HV NMOS	NHVE	7.0
nmmc_bjt ⁽³⁾	nmmc with additional parasitic bjt model	NHVE	7.0
nmmdd	15V symmetrical HV NMOS	NHVE	7.0
nmmdd_bjt ⁽³⁾	nmmdd with additional parasitic bjt model	NHVE	7.0
nma	6V NMOS with thick gate oxide	HVN莫斯	7.0
nma_bjt ⁽³⁾	nma with additional parasitic bjt model	HVN莫斯	7.0
nhvd	32V asymmetrical HV depletion NMOS	HVDEPL	5.0
nhvd_bjt ⁽³⁾	nhvd with additional parasitic bjt model	HVDEPL	6.3
nhhvd	32V symmetrical HV depletion NMOS	HVDEPL	5.0
nhhvd_bjt ⁽³⁾	nhhvd with additional parasitic bjt model	HVDEPL	6.3
phv	45V asymmetrical HV PMOS	PHVE	7.0
phv_bjt ⁽³⁾	phv with additional parasitic bjt model	PHVE	7.0
phhv	45V symmetrical HV PMOS	PHVE	7.0
phhv_bjt ⁽³⁾	phhv with additional parasitic bjt model	PHVE	7.0
pmc	20V asymmetrical HV PMOS	PHVE	7.0

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2. General → 2.5 Primitive devices → 2.5.1 LPMOS main module → MOS transistors

Name	Description	Required modules	Model rev.
pmc_bjt ⁽³⁾	pmc with additional parasitic bjt model	PHVE	7.0
pmmc	20V symmetrical HV PMOS	PHVE	7.0
pmmc_bjt ⁽³⁾	pmmc with additional parasitic bjt model	PHVE	7.0
pma	6V PMOS with thick gate oxide	HVPMOS	7.0
pma_bjt ⁽³⁾	pma with additional parasitic bjt model	HVPMOS	7.0

Note 1 These devices are variants of the corresponding basic device with underlying wells. Parameters of these devices are identical to the corresponding basic device.

Note 2 The ISOMOS2 or HVMOS module is needed, if isolated MOS transistors are placed in DNWELL instead of DNWELLMV.

Note 3 Parameters of these devices are identical to the corresponding basic device.

Note 4 This device has been superseded by 'nedia'.

Note 5 'nedia' is a more robust device with a higher on-state drain-source breakdown voltage than 'nedi'.

Bipolar transistors

Name	Description	Required modules	Model rev.
qpva	1.8V vertical PNP bipolar transistor; emitter area = 2µm x 2µm	-	4.0
qpvb	1.8V vertical PNP bipolar transistor; emitter area = 5µm x 5µm	-	4.0
qpvc	1.8V vertical PNP bipolar transistor; emitter area = 10µm x 10µm	-	4.0
qpva3	3.3V vertical PNP bipolar transistor; emitter area = 2µm x 2µm	-	4.0
qpvb3	3.3V vertical PNP bipolar transistor; emitter area = 5µm x 5µm	-	4.0
qpvc3	3.3V vertical PNP bipolar transistor; emitter area = 10µm x 10µm	-	4.0
qnva	vertical NPN bipolar transistor	DEPL and HVMOS	1.0
qnvb	vertical NPN bipolar transistor	(DEPL and ISOMOS) or (DEPL and HVMOS)	3.0
qnvc	vertical NPN bipolar transistor	ISOMOS	7.0

Resistors

Name	Description	Required modules	Model rev.
rdn	1.8V NDIFF / PWELL1 resistor (non salicided)	-	6.3
rdp	1.8V PDIFF / NWELL1 resistor (non salicided)	-	6.3
rnw	1.8V NWELL1 / PSUB resistor (STI terminated)	-	6.3
rdn3	3.3V NDIFF / PWELL2 resistor (non salicided)	-	6.3
rdp3	3.3V PDIFF / NWELL2 resistor (non salicided)	-	6.3
rnw3	3.3V NWELL2 / PSUB resistor (STI terminated)	-	6.3
rdnwmv	5V DNWELLMV / PSUB resistor (STI terminated)	ISOMOS or HVMOS	6.3
rnp1	N-doped POLY1 resistor (non salicided), 2 terminals	-	6.3

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2. General → 2.5 Primitive devices→ 2.5.1 LPMOS main module→ Resistors

Name	Description	Required modules	Model rev.
rnp1_3 ⁽¹⁾	N-doped POLY1 resistor (non-salicided), 3 terminals	-	6.3
rpp1	P-doped POLY1 resistor (non-salicided), 2 terminals	-	6.3
rpp1_3 ⁽¹⁾	P-doped POLY1 resistor (non-salicided), 3 terminals	-	6.3
rpp1s	salicided P-doped POLY1 resistor, 2 terminals	-	6.3
rpp1s_3 ⁽¹⁾	salicided P-doped POLY1 resistor, 3 terminals	-	6.3
rnp1h	high-ohmic N-doped POLY1 resistor (non salicided), 2 terminals	-	6.3
rnp1h_3 ⁽¹⁾	high-ohmic N-doped POLY1 resistor (non salicided), 3 terminals	-	6.3
rpp1k1	lightly P-doped POLY1 resistor (non salicided), 2 terminals	MRPOLY	6.3
rpp1k1_3 ⁽¹⁾	lightly P-doped POLY1 resistor (non salicided), 3 terminals	MRPOLY	6.3
rm1	metal 1 resistor	-	7.0
rm2	metal 2 resistor	-	7.0
rm3	metal 3 resistor	MET3	7.0
rm4	metal 4 resistor	MET4	7.0
rm5	metal 5 resistor	MET5	7.0
rmtp	top metal resistor	METMID	7.0
rmtpl	thick metal resistor	METTHK	7.0

Note 1 These devices are variants of the corresponding basic device with an underlying well, but not crossing a well boundary. The models realise an improved description of bulk voltage dependency. Parameters of these devices are identical to the corresponding basic device.

Capacitors

Name	Description	Required modules	Forbidden modules	Model rev.
mosvc	1.8V N-type varactor	-	-	6.3
mosvc3	3.3V N-type varactor	-	-	6.3
mosvc3i	3.3V P-type varactor in DNWELL	ISOMOS2 or (ISOMOS and HVMOS)	-	6.3
mosvc3i_m	3.3V P-type varactor in DNWELLMV	ISOMOS	-	6.3
mosvci	1.8V P-type varactor in DNWELL	ISOMOS2 or (ISOMOS and HVMOS)	-	6.3
mosvci_m	1.8V P-type varactor in DNWELLMV	ISOMOS	-	6.3
cpod	1.8V POD capacitor	CPOD	-	7.0
cpodhv	POD capacitor (high voltage)	CPODHV or (CPOD and (HVMOS or HVNMOS or HVPMOS or ESDPNP))	-	7.0
csandwt3	POLY1 / metal1/ metal2/ metal3 capacitor	MET3	-	7.0
csandwt4	POLY1 / metal1/ metal2/ metal3/ metal4 capacitor	MET4	-	7.0
csandwt5	POLY1 / metal1/ metal2/ metal3/ metal4/ metal5 capacitor	MET5	-	7.0

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2. General → 2.5 Primitive devices→ 2.5.1 LPMOS main module→ Capacitors

Name	Description	Required modules	Forbidden modules	Model rev.
csf2p	POLY1/metal1/metal2 fringe capacitor	-	-	7.0
csf3p	POLY1/metal1/metal2/metal3 fringe capacitor	MET3	-	7.0
csf3	10V metal1/metal2/metal3 fringe capacitor	MET3	-	7.0
csf3a	45V metal1/metal2/metal3 fringe capacitor	MET3	-	7.0
csf4	10V metal1/metal2/metal3/metal4 fringe capacitor	MET4	-	7.0
csf4a	45V metal1/metal2/metal3/metal4 fringe capacitor	MET4	-	7.0
csf5	10V metal1/metal2/metal3/metal4/metal5 fringe capacitor	MET5	-	7.0
csf5a	45V metal1/metal2/metal3/metal4/metal5 fringe capacitor	MET5	-	7.0
csft4	10V metal1/metal2/metal3/metaltop fringe capacitor	MET3 and METMID	MET4	7.0
csft4a	45V metal1/metal2/metal3/metaltop fringe capacitor	MET3 and METMID	MET4	7.0
csft5	10V metal1/metal2/metal3/metal4/metaltop fringe capacitor	MET4 and METMID	MET5	7.0
csft5a	45V metal1/metal2/metal3/metal4/metaltop fringe capacitor	MET4 and METMID	MET5	7.0
csft6	10V metal1/metal2/metal3/metal4/metal5/metaltop fringe capacitor	MET5 and METMID	-	7.0
csft6a	45V metal1/metal2/metal3/metal4/metal5/metaltop fringe capacitor	MET5 and METMID	-	7.0
cmm3	single MIM capacitor between metal2 and metal3	MIM23	-	7.0
cmm4	single MIM capacitor between metal3 and metal4	MIM34	-	7.0
cmm4t	single MIM capacitor between metal3 and metaltop	MIM and MET3 and METMID	MET4	7.0
cmm5t	single MIM capacitor between metal4 and metaltop	MIM and MET4 and METMID	MET5	7.0
cmm6t	single MIM capacitor between metal5 and metaltop	MIM and MET5 and METMID	-	7.0
cmmh3	single MIM capacitor (high capacitance) between metal2 and metal3	MIMH23	-	7.0
cmmh4	single MIM capacitor (high capacitance) between metal3 and metal4	MIMH34	-	7.0
cmmh4t	single MIM capacitor (high capacitance) between metal3 and metaltop	MIMH and MET3 and METMID	MET4	7.0
cmmh5t	single MIM capacitor (high capacitance) between metal4 and metaltop	MIMH and MET4 and METMID	MET5	7.0
cmmh6t	single MIM capacitor (high capacitance) between metal5 and metaltop	MIMH and MET5 and METMID	-	7.0
cdmm4	double MIM capacitor between metal2, metal3 and metal4	MET4 and DMIM	-	7.0
cdmm4t	double MIM capacitor between metal2, metal3 and metaltop	DMIM and MET3 and METMID	MET4	7.0

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2. General → 2.5 Primitive devices → 2.5.1 LPMOS main module → Capacitors

Name	Description	Required modules	Forbidden modules	Model rev.
cdmmh4	double MIM capacitor (high capacitance) between metal2, metal3 and metal4	MET4 and DMIMH	-	7.0
cdmmh4t	double MIM capacitor (high capacitance) between metal2, metal3 and metaltop	DMIMH and MET3 and METMID	MET4	7.0
ctmm5	triple MIM capacitor between metal2, metal3, metal4 and metal5	MET5 and TMIM	-	7.0
ctmm5t	triple MIM capacitor between metal2, metal3, metal4 and metaltop	TMIM and MET4 and METMID	MET5	7.0
ctmmh5	triple MIM capacitor (high capacitance) between metal2, metal3, metal4 and metal5	MET5 and TMIMH	-	7.0
ctmmh5t	triple MIM capacitor (high capacitance) between metal2, metal3, metal4 and metaltop	(MET4 and METMID) and TMIMH	MET5	7.0

Diodes

Name	Description	Required modules	Model rev.
dn	diode NDIFF / PWELL1,3,5 (1.8V)	-	7.0
dp	diode PDIFF / NWELL1,3,5 (1.8V)	-	7.0
dnw	diode NWELL1,3,5 / PSUB (1.8V)	-	7.0
dn3	diode NDIFF / PWELL2 (3.3V)	-	7.0
dp3	diode PDIFF / NWELL2,4 (3.3V)	-	7.0
d nw3	diode NWELL2,4 / PSUB (3.3V)	-	7.0
d nn3 ⁽¹⁾	diode NDIFF/ PSUB (3.3V)	-	7.0
ddnwmv	diode DNWELLMV / PSUB	ISOMOS or HVMOS	7.0
dpdnwmv	diode PDIFF / DNWELLMV	ISOMOS or HVMOS	7.0
dipdnwmv	diode PWELL1,2 / DNWELLMV	ISOMOS or HVMOS	7.0
ddnw	diode DNWELL / PSUB	ISOMOS2 or HVMOS	7.0
dpdnw	diode PDIFF / DNWELL	ISOMOS2 or HVMOS	7.0
dipdnw	diode PWELL1,2 / DNWELL	ISOMOS2 or (HVMOS and ISOMOS)	7.0
dnhpw	diode NDIFF / HVPWELL	HVMOS	7.0
dphnw	diode PDIFF / HVNWELL	HVMOS	7.0
dhpw	diode HVPWELL / DNWELL	ISOMOS2 or HVMOS	7.0
d hn w	diode HVNWELL / PSUB	HVMOS	7.0
dndf	diode NDF / PSUB	NHVE	7.0
dpdwhn	diode PDF / HNW	PHVE	7.0
d whn	diode HNW / PSUB	HVPMOS	7.0
dpwhn	diode PDIFF / HNW	HVPMOS	7.0
p_dn3dpl	parasitic junction diode NDIFF / DEPL (3.3V)	DEPL	7.0
p_ddpldnw	parasitic junction diode DEPL / DNWELL	DEPL and (HVMOS or ISOMOS or ISOMOS2)	7.0
p_dpddd nw	parasitic junction diode PDD / DNWELL	DMOS	7.0
p_dpndf	parasitic junction diode PDIFF / NDF	NHVE or HVPMOS	7.0

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2. General → 2.5 Primitive devices→ 2.5.1 LPMOS main module→ Diodes

Name	Description	Required modules	Model rev.
p_dbn	parasitic junction diode CPOD n+ / PSUB	CPOD	7.0
dsba	18V Schottky diode	SCHOTTKY	7.1
dsb ⁽²⁾	18V Schottky diode	SCHOTTKY	7.1
dpol	polysilicon diode	-	7.0
dnp20	20V N-type protection diode	NHVE	3.0
dpp20	20V P-type protection diode	HVMOS	3.0
dphoa	Photodiode for visible and infrared light detection	PHOTODIO	7.0
dphob	Photodiode for infrared light detection	PHOTODIO	7.0
dphoc	Photodiode for ultraviolet, visible and infrared light detection	CATDOP and UVWINDOW	6.0
dphoco	Blind (metal covered) reference photodiode for ultraviolet, visible and infrared light detection	CATDOP and UVWINDOW	6.0
dphocfp	Blind (poly covered) reference photodiode for ultraviolet, visible and infrared light detection	CATDOP and UVWINDOW	6.0
dphod	Photodiode for ultraviolet, visible and infrared light detection	ANODOP and UVWINDOW	6.0
dphodo	Blind (metal covered) reference photodiode for ultraviolet, visible and infrared light detection	ANODOP and UVWINDOW	6.0
dphodfp	Blind (poly covered) reference photodiode for ultraviolet, visible and infrared light detection	ANODOP and UVWINDOW	6.0
dapda ⁽³⁾	Avalanche photodiode with breakdown voltage < 20V	CATDOP and AVLA	8.0
dapda0 ⁽³⁾	Blind (metal covered) reference avalanche photodiode with breakdown voltage < 20V	CATDOP and AVLA	8.0
dspada ⁽³⁾	Single-photon avalanche diode for low light levels with breakdown voltage < 20V	CATDOP and AVLA	8.0
dspada0 ⁽³⁾	Single-photon avalanche diode for high light levels (metal covered) with breakdown voltage < 20V	CATDOP and AVLA	8.0

Note 1 This diode is only available along with the corresponding transistor where it is used as source/drain.

Note 2 The device dsb is superseded by dsba.

Note 3 Please refer to the documentation on "my X-FAB":
["Application Note - Avalanche Photodiodes"](#)

Memories

Name	Description	Required modules	Model rev.
pfuse	polysilicon fuse	-	6.3

Sensors

Name	Description	Required modules	Model rev.
hall1	Hall sensor (available on request)	HALL	2.2

2. General → 2.5 Primitive devices → 2.5.1 LPMOS main module → Virtual devices

Virtual devices

Name	Description	Required modules	Model rev.
tag_25v ⁽¹⁾	defines voltage class for net with $\leq 25V$ related to PSUB	-	7.0
tag_60v ⁽¹⁾	defines voltage class for net with $> 25V \leq 60V$ related to PSUB	-	7.0

Note 1 These devices are not fabricated on silicon; they are available for DRC and LVS voltage class checks only. For further information, please refer to the design related guideline "Voltage class definitions".

ESD devices

Name	Description	Required modules	Model rev.
qpvhbscr	ESD protected HV PNP bipolar transistor	ESDPNP	6.1
qpvascr ⁽¹⁾	HVPWELL in DNWELL isolated scr	HVMOS	4.0
rdp_io ⁽¹⁾	PDIFF drain ballast resistor of pmb (Pdiff in HVNWELL in DNW)	HVMOS	4.0
rdn_esd ⁽¹⁾	NDIFF drain ballast resistor of ESD nma (Ndif in HVPWELL)	HVN莫斯	4.0
rdp_esd ⁽¹⁾	PDIFF drain ballast resistor of ESD pma (Pdiff in HVNWELL in HNW)	HVPMOS	4.0
rnw_scr ⁽¹⁾	1.8V LV NMOS triggered SCR dio/res network resistor	-	4.0
rnw3_scr ⁽¹⁾	3.3V LV NMOS triggered SCR dio/res network resistor	-	4.0
qpvhscr	ESD protected HV PNP bipolar transistor	BIPESD	7.0
pmb ⁽¹⁾	5V ESD PMOS	HVMOS	7.0

Note 1 These devices are only allowed to be used for ESD protection. Please refer to the ESD documentation on "my X-FAB":
["Basic ESD Guidelines"](#)
["XH018 ESD Protection Device and Latch-up Guidelines"](#)
["XH018 MOS TLP I-V Characteristics"](#)
["XH018 TLP I-V Characteristics"](#)

2. General → 2.6 Geometric relations and rule code

2.6 Geometric relations and rule code

The rule codes, in general, use the description of the geometric relation (e.g. "S" for spacing) and also the design layer/definition code (e.g. "M1" for Metal 1). Rule codes are intended for short design rule check error messages.

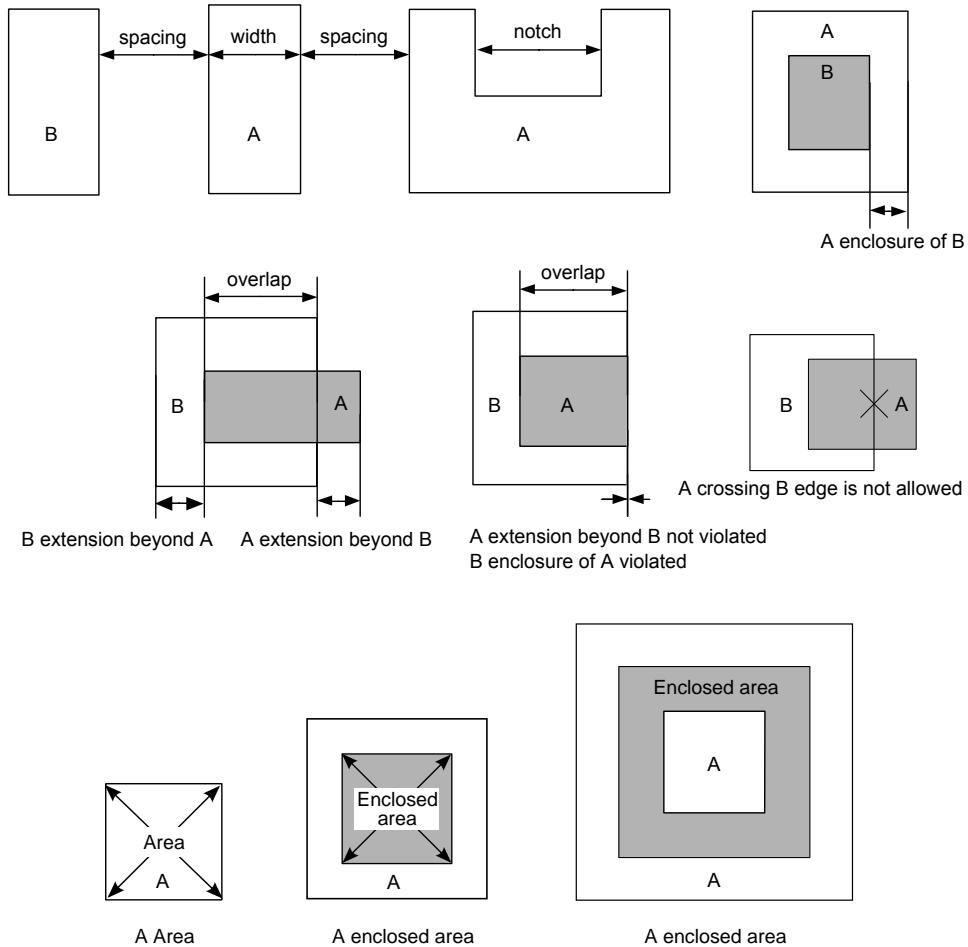
Design rules that are not checked by DRC are indicated by printing the rule code in red underlined italics. The designer must ensure manually that these rules are adhered to.

'QnA(B)' - Query/ warning based rules are not considered to be DRC failures.

The rule types M_A, N_A, G_A are used to check that predefined devices adhere to the following statement: "The layout of the device is predefined and must not be changed". Please note, that for these devices, it is a requirement that the layout is not to be changed (except for the described conditions). The checks related to the rule codes M_A, N_A, G_A are a supporting tool to achieve this requirement. These rules are available for viewing only via the SpecXplorer website.

Rule text	Description	Rule code
(arbitrary text)	Illegal construct	BnA(B)
A crossing B edge is not allowed	Not allowed for layer A polygon to have portions both inside and outside layer B	BnA
A width	Distance inside_A - inside_A	WnA
A size	(Distance inside_A - inside_A) x (Distance inside_A - inside_A)	WnA
A spacing / notch	Distance outside_A - outside_A	SnA
A spacing to B	Distance outside_A - outside_B	SnAB or SnBA
A enclosure of B	Distance inside_A - outside_B (A contains B)	EnAB or EnBA
A extension beyond B	Distance inside_A - outside_B (A must intersect B)	EnAB or EnBA
A overlap of B	Distance inside_A - inside_B	OnAB or OnBA
A area	Area	AnA
A enclosed area	Area enclosed by A	AnA
ratio of A to B	Ratio	RnAB
(arbitrary text)	Recommend investigation (query or warning)	QnA(B)
curvature	Curvature	CnA
Predefined area must have A	Area restriction	M_A
Predefined area must not have A	Area restriction	N_A
Predefined geometry of A violated	Area restriction	G_A

2. General → 2.6 Geometric relations and rule code

**Figure 2.1** Geometric relations

2. General → 2.7 General requirements

2.7 General requirements

Grid	0.005 µm
Recommended working grid	0.01 µm
Corners	90°, 135°
Data extrema including Peripheral Ring and Scribe Lane Note: Data extrema requirements cover demands of the mask generation procedure and the wafer manufacturing process only.	multiple of 1 µm

It is **MANDATORY** that all layout data, including path edges (centre line & width defined), lie on the minimum grid. Designers are recommended to work with a 0.01µm grid because the data edges can be 0.005µm when 0.01µm is used for the centre line of 'paths'.

45 degree data must not be used for:

- minimum width lines;
- minimum spaced lines;
- or for components with a critical tolerance;

since 'snapping to grid' can occur at mask generation.

Self intersecting polygons must be avoided.

Off-grid data points are **NOT** checked by the standard DRC; they are checked by XFAB at GDS tape in and any errors found, by XFAB, may delay mask making and manufacture.

3. Layer and Device rules

3. Layer and Device rules

3.1 LPMOS main module

3.1.1 Layer rules

NWELL

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
W1NW	Minimum NWELL width (except nedia)	0.86	μm
S1NW	Minimum NWELL spacing/notch	0.6	μm
S2NW	Minimum NWELL spacing (different net)	1.4	μm
S3NW	Minimum NWELL spacing (different net) Note: Valid if one NWELL to PSUB voltage is less than 1 V.	2.0	μm

Note: It is not recommended to take 'spurs' of device N-Wells to make resistors.

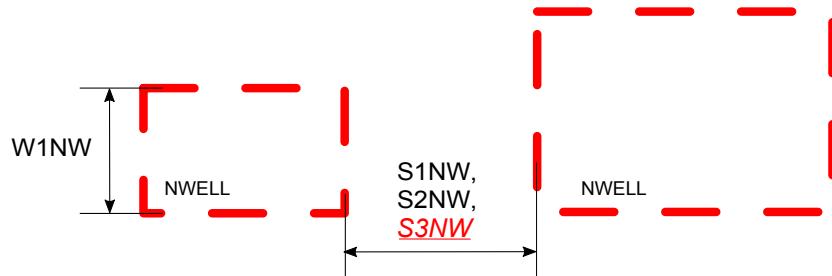


Figure 3.1 NWELL

3. Layer and Device rules → 3.1 LPMOS main module→ 3.1.1 Layer rules→ NWELL1, NWELL2, NWEL...

NWELL1, NWELL2, NWELL3, NWELL4, NWELL5, PWELL1, PWELL2, PWELL3, PWELL5

These rules are related to a combination of design layers (refer to section "2.4 Definitions").

Name	Description	Value	Unit
W1W1	Minimum NWELL1 width (except nedia)	0.86	µm
W1W2	Minimum PWELL1 width	0.6	µm
W1W3	Minimum NWELL2 width	0.86	µm
W1W4	Minimum PWELL2 width	0.6	µm
W1W5	Minimum NWELL3 width	0.86	µm
W1W6	Minimum PWELL3 width	0.6	µm
W1W7	Minimum NWELL4 width	0.86	µm
W1W9	Minimum NWELL5 width	0.86	µm
W1W10	Minimum PWELL5 width	0.6	µm

3. Layer and Device rules → 3.1 LPMOS main module → 3.1.1 Layer rules → NWELL1, NWELL2, NWELL4, PWELL1, PWELL2, PWELL3, PWELL4, PWELL5, LNDEV, MV, W1W1, W1W2, W1W3, W1W4, W1W5, W1W6, W1W7, W1W8, W1W9, W1W10, LVT, SVT

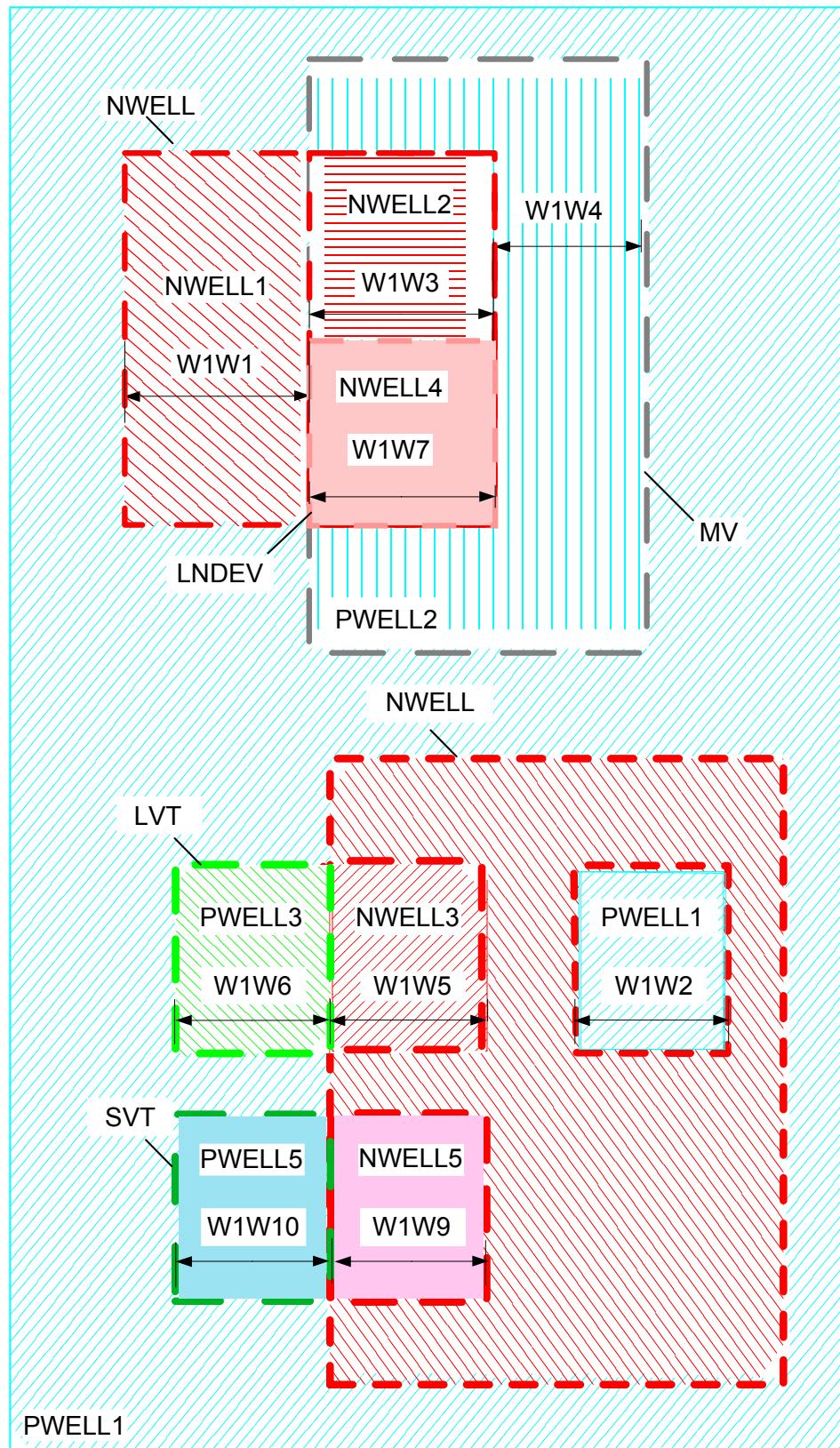


Figure 3.2 NWELL1, PWELL1, NWELL2, PWELL2, NWELL3, PWELL3, NWELL4, NWELL5, PWELL5

3. Layer and Device rules → 3.1 LPMOS main module→ 3.1.1 Layer rules→ PWBLK

PWBLK

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B3PB	PWBLK overlap of PDIFF is not allowed Note: Valid outside wells	-	-
B5PB	PWBLK overlap of NDIFF without MV or BNIMP is not allowed Note: Valid outside wells	-	-
B6PB	Only a single rectangular NDIFF inside PWBLK is allowed (except nmma, nh#, nmmd, dphoc#) Note: Valid outside wells	-	-
B4PB	DIFF crossing PWBLK edge is not allowed (except nmma, nh#, nmmd) Note: Valid outside wells	-	-
W1PB	Minimum PWBLK width	0.6	μm
S1PB	Minimum PWBLK spacing/notch	0.86	μm
S1PBDN	Minimum PWBLK spacing to NDIFF Note: Valid outside wells	0.12	μm
S1PBNW	Minimum PWBLK spacing to NWELL (except dphod#) Note: Valid outside wells	0.86	μm
S1PBWM	Minimum PWBLK spacing to DNWELLMV Note: Valid outside wells	0.86	μm
E1PBDN	Fixed PWBLK enclosure of NDIFF (except nmma, nh#, nmmd, dphoc#, cpod#) Note: Valid outside wells	0.12	μm

3. Layer and Device rules → 3.1 LPMOS main module → 3.1.1 Layer rules → PWBLK

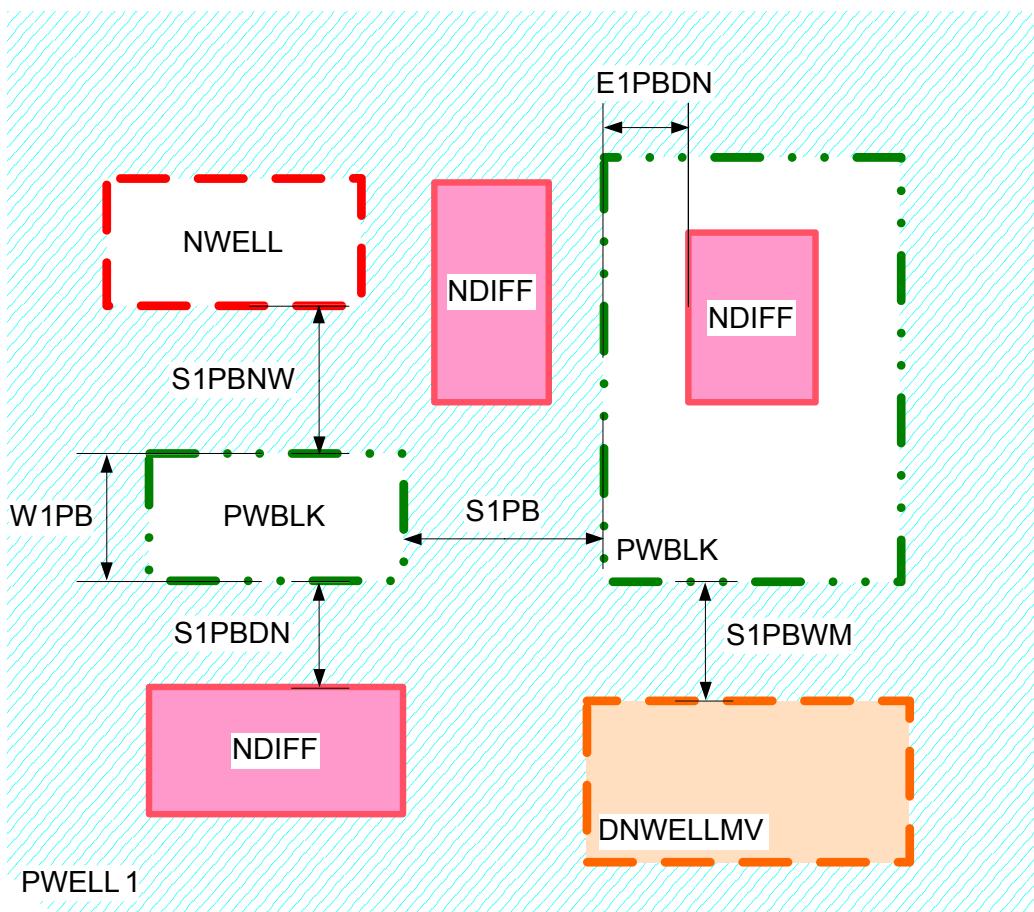


Figure 3.3 PWBLK

3. Layer and Device rules → 3.1 LPMOS main module→ 3.1.1 Layer rules→ DIFF

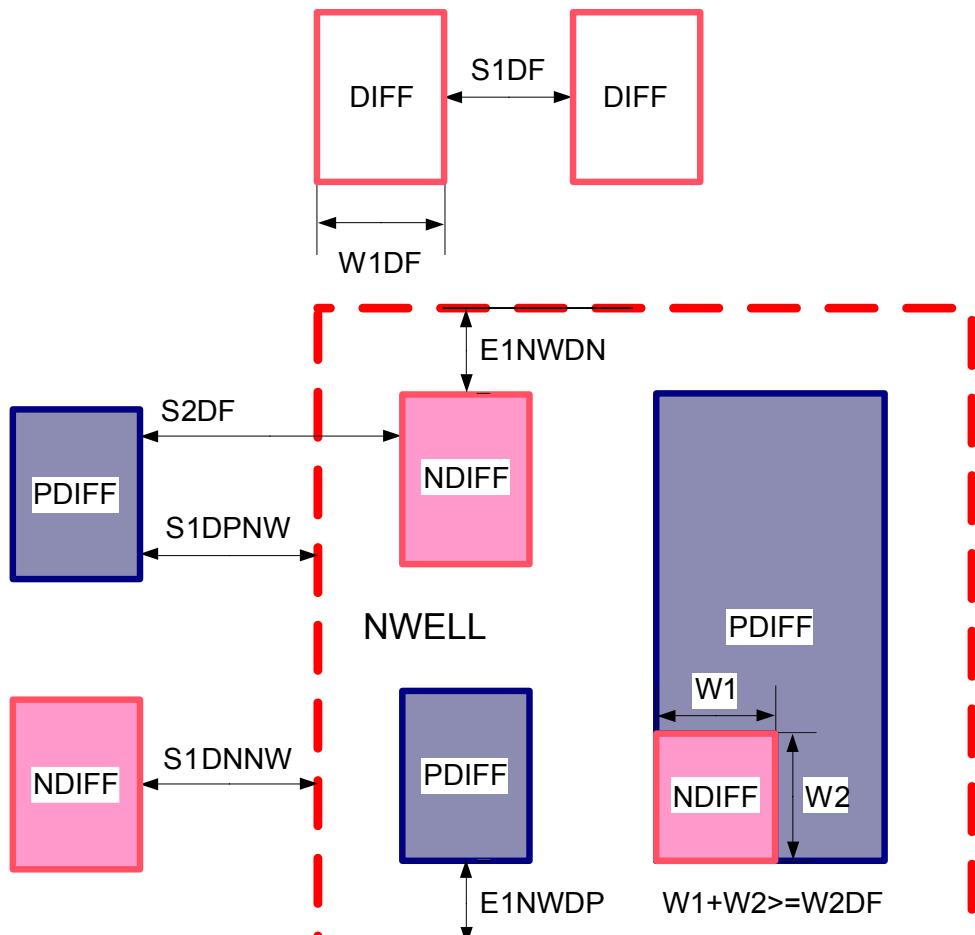
DIFF

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit	
B1DF	DIFF without NIMP or PIMP is not allowed (except qnva, qnvb, qnvc, nedia, dsb#, dphoa, dphob, dphoc#, dphod# or PHODIO)	-	-	
	Note: Not valid for DIFFDUMMY.			
B2DF	Not allowed to be used by customers	-	-	
	Note: Only valid for DIFF purpose NOBLK. Reserved layer.			
B3DF	DIFF crossing NTYPE_WELL or PTYPE_WELL edge is not allowed (except PHODIO)	-	-	
W1DF	Minimum DIFF width	0.22	μm	
W2DF	Minimum length of coincident NDIFF/PDIFF path edge	0.42	μm	
S1DF	Minimum DIFF spacing/notch	0.28	μm	
S3DF	Minimum PDIFF spacing	0.56	μm	
	Note: Valid inside DNWELLMV/DNWELL/HNW and NOT other wells only.			
S1DNNW	Minimum NDIFF spacing to NWELL	0.43	μm	
S1DPNW	Minimum PDIFF spacing to NWELL	0.12	μm	
S2DF	Minimum NDIFF in NWELL spacing to PDIFF in PWELL	0.36	μm	
E1NWDN	Minimum NWELL enclosure of NDIFF (except nedia)	0.12	μm	
E1NWDP	Minimum NWELL enclosure of PDIFF	0.43	μm	
A1DF	Minimum DIFF area	0.202	μm ²	
	Minimum local DIFF density	15.0	%	
<i>R1DF</i>	Note: Valid in any 200μm x 200μm window, step size 100μm.			
	Note: Not checked with standard DRC, option for check is available.			

Note: DIFF dimension greater than 200 μm x 200 μm must not be used (except PHODEF or UVWIN).

3. Layer and Device rules → 3.1 LPMOS main module → 3.1.1 Layer rules → DIFF

**Figure 3.4** DIFF

3. Layer and Device rules → 3.1 LPMOS main module→ 3.1.1 Layer rules→ DIFFDUMMY

DIFFDUMMY

It is recommended to use X-FAB's dummy pattern generation option (DUMMY_FILL included in the DRC for preview) to create dummy pattern. If the generated dummy pattern is not sufficient to meet the minimum requirements for pattern density, customers can draw additional dummy pattern following the dummy design rules (DIFFDUMMY, P1DUMMY, M1DUMMY, M2DUMMY, M3DUMMY, M4DUMMY, M5DUMMY, MTPDUMMY and MTPLDUMMY). For further information, refer to the design related guideline "Dummy Pattern Generation".

Name	Description	Value	Unit
B1YD	DIFFDUMMY overlap of DIFF is not allowed	-	-
B2YD	DIFFDUMMY overlap of NIMP or PIMP is not allowed	-	-
B3YD	DIFFDUMMY overlap of CONT is not allowed	-	-
B5YD	DIFFDUMMY overlap of SBLK is not allowed	-	-
B6YD	DIFFDUMMY overlap of HVDEPL is not allowed	-	-
B7YD	DIFFDUMMY overlap of PHODEF is not allowed	-	-
W1YD	Minimum DIFFDUMMY width	0.4	μm
S1YD	Minimum DIFFDUMMY spacing/notch	0.5	μm
S10YD	Minimum DIFFDUMMY spacing to LOCKED	3.6	μm
S11YD	Minimum DIFFDUMMY spacing to LOCKED1	3.6	μm
S12YD	Minimum DIFFDUMMY spacing to LOCKED2	3.6	μm
S13YD	Minimum DIFFDUMMY spacing to LOCKED3	3.6	μm
S14YD	Minimum DIFFDUMMY spacing to LOCKED4	3.6	μm
S1YDDF	Minimum DIFFDUMMY spacing to DIFF	3.0	μm
S1YDHL	Minimum DIFFDUMMY spacing to HVDEPL	5.0	μm
S1YDHW	Minimum DIFFDUMMY spacing to HNW	10.0	μm
S1YDIN	Minimum DIFFDUMMY spacing to NIMP	0.3	μm
S1YDIP	Minimum DIFFDUMMY spacing to PIMP	0.3	μm
S1YDNW	Minimum DIFFDUMMY spacing to NW4DMY	5.0	μm
S1YDP1	Minimum DIFFDUMMY spacing to POLY1	3.0	μm
S1YDPI	Minimum DIFFDUMMY spacing to PW4DMY	5.0	μm
S1YDSB	Minimum DIFFDUMMY spacing to SBLK	3.0	μm
S1YDWD	Minimum DIFFDUMMY spacing to DNWELL	10.0	μm
S1YDWM	Minimum DIFFDUMMY spacing to DNWELLMV	5.0	μm
	Note: Valid if DNWELLMV is outside DNWELL.		
E1YDHW	Minimum HNW enclosure of DIFFDUMMY	10.0	μm
E1YDNW	Minimum NW4DMY enclosure of DIFFDUMMY	5.0	μm
E1YDPI	Minimum PW4DMY enclosure of DIFFDUMMY	5.0	μm
E1YDWD	Minimum DNWELL enclosure of DIFFDUMMY	10.0	μm
E1YDWM	Minimum DNWELLMV enclosure of DIFFDUMMY	5.0	μm
	Note: Valid if DNWELLMV is outside DNWELL.		
A1YD	Minimum DIFFDUMMY area	1.2	μm ²

3. Layer and Device rules → 3.1 LPMOS main module → 3.1.1 Layer rules → DIFFDUMMY

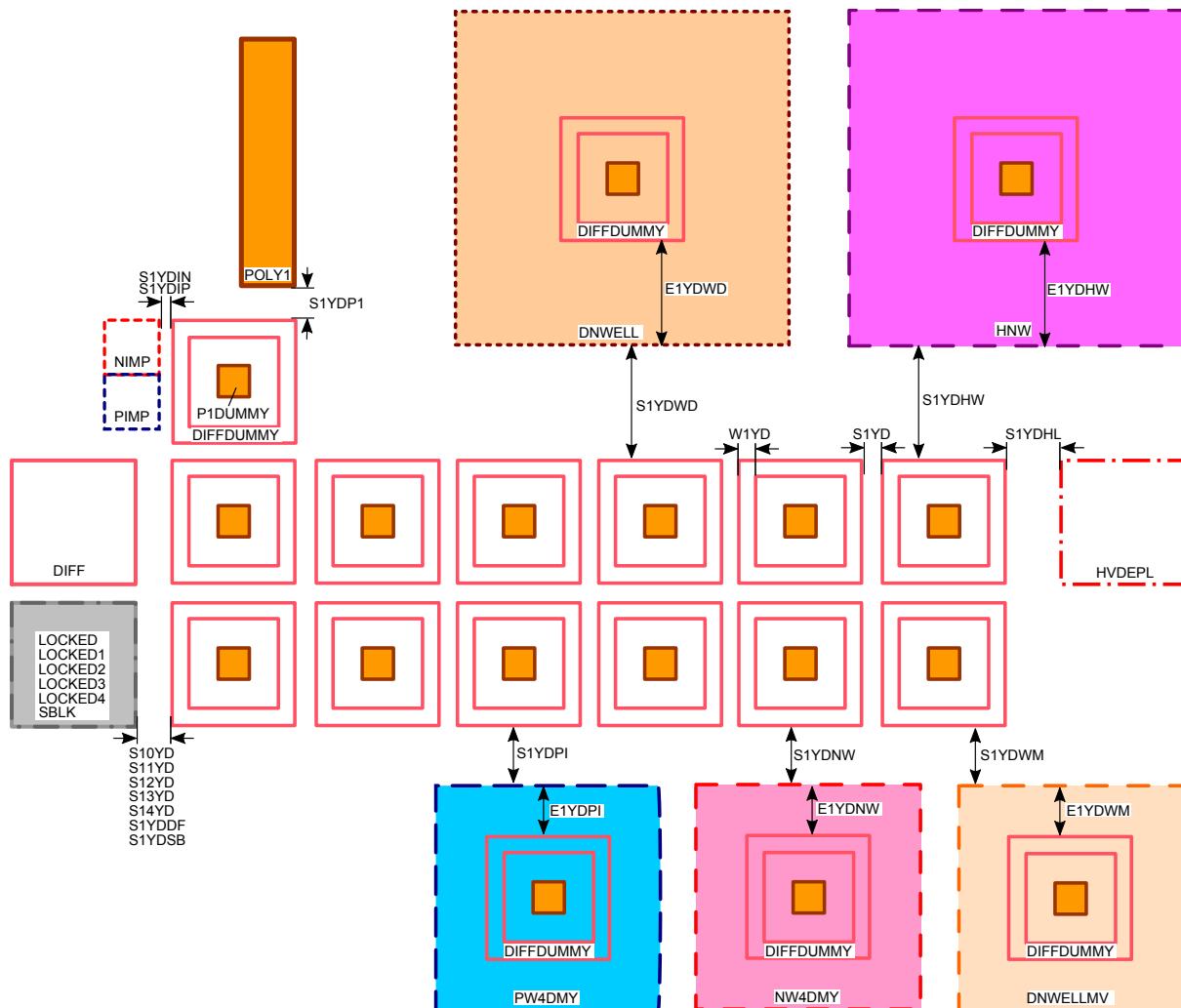


Figure 3.5 DIFFDUMMY

3. Layer and Device rules → 3.1 LPMOS main module → 3.1.1 Layer rules → MV

MV

Name	Description	Value	Unit
B3MV	MV overlap of HVPWELL, HVNWELL, PDD is not allowed	-	-
B1MV	DIFF crossing MV edge is not allowed Note: Not valid for DIFFDUMMY.	-	-
B2MV	NW_VERIFY crossing MV edge is not allowed	-	-
W1MV	Minimum MV width	0.6	μm
S1MV	Minimum MV spacing/notch	0.45	μm
S1MVDF	Minimum MV spacing to DIFF Note: Not valid for DIFFDUMMY.	0.32	μm
S1MVGA	Minimum MV spacing to GATE	0.4	μm
E1MVDF	Minimum MV enclosure of DIFF Note: Not valid for DIFFDUMMY.	0.32	μm
E1MVGA	Minimum MV enclosure of GATE	0.4	μm

Note: In many cases MV width and MV spacing are also determined by NWELL1, PWELL1, NWELL2, PWELL2, NWELL3, PWELL3, NWELL4 rules.

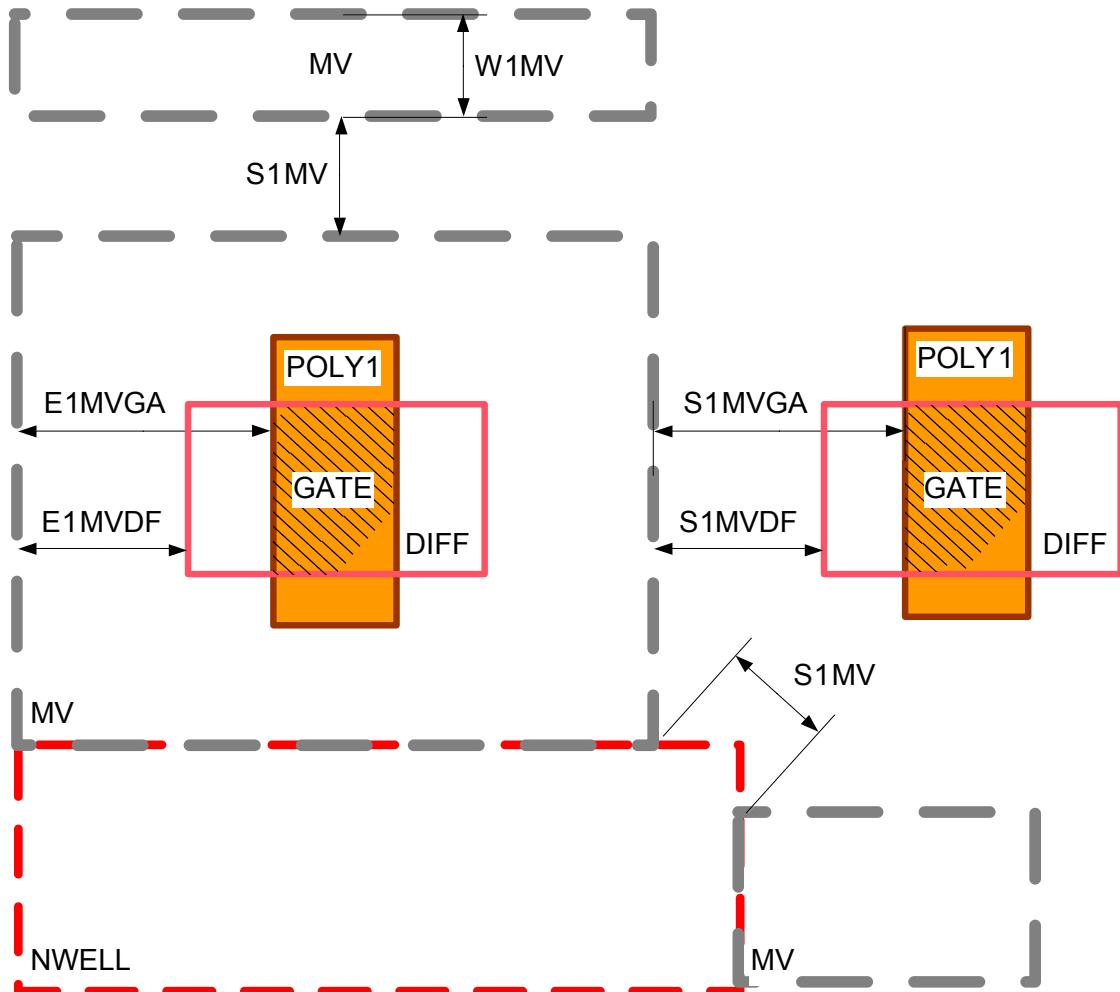


Figure 3.6 MV

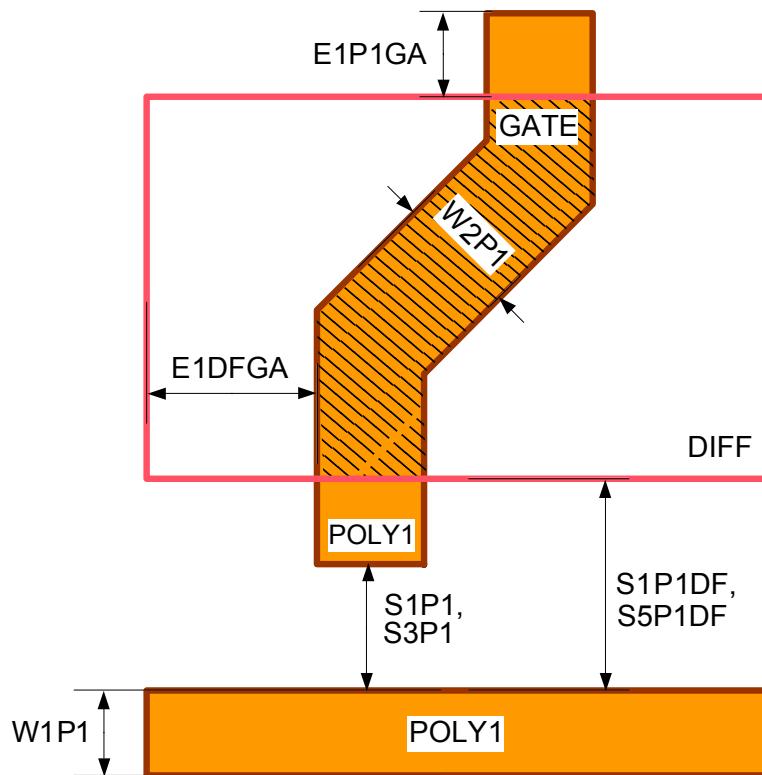
3. Layer and Device rules → 3.1 LPMOS main module→ 3.1.1 Layer rules→ POLY1

POLY1

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1GA	90 degree bent GATE is not allowed Note: Only valid for POLY1 over DIFF or for DIFF over POLY1 structures with > 4 vertices.	-	-
B1P1	(POLY1 and SBLK and not (HRES or MRES)) without NIMP or PIMP is not allowed (except dpol, davla#) Note: NIMP touching PIMP under (POLY1 and SBLK and not (HRES or MRES)) is not allowed.	-	-
B2GA	Illegal GATE construct Note: GATE region has been identified as having no association with supported devices.	-	-
BDP1	Not allowed to be used by customers Note: Only valid for POLY1 purpose NOBLK. Reserved layer.	-	-
W1P1	Minimum POLY1 width	0.18	μm
W2P1	Minimum POLY1 width (for 45 degree bent GATE)	0.21	μm
S1P1	Minimum POLY1 spacing/notch	0.25	μm
S3P1	Minimum POLY1 spacing (different net, tag_60v) Note: Valid for spacing of all POLY1 shapes with label tag_60v to all POLY1 shapes having lower voltage classes. Refer to the design related guideline "Voltage class definitions".	0.5	μm
S1P1DF	Minimum POLY1 spacing to DIFF	0.1	μm
S5P1DF	Minimum POLY1 spacing to DIFF (different net, tag_60v) Note: Valid for spacing of all POLY1/DIFF shapes with label tag_60v to all DIFF/POLY1 shapes having lower voltage classes. Refer to the design related guideline "Voltage class definitions".	0.5	μm
E1DFGA	Minimum DIFF extension beyond GATE (except davla#)	0.32	μm
E1P1GA	Minimum POLY1 extension beyond GATE (except davla#)	0.22	μm
A1P1	Minimum POLY1 area	0.118	μm ²
<u>R1P1</u>	Minimum ratio of POLY1 area to EXTENT area Note: Not checked with standard DRC, option for check is available.	14.0	%
R2P1	Maximum ratio of POLY1 area to connected GATE area Note: Refer to section "Antenna Rule definitions" as well.	200.0	-
Q1P1	Resistor terminal net without VLABEL Note: Resistor having VLABEL at one terminal only is not allowed. Refer to the design related guideline "Voltage class definitions".	-	-

3. Layer and Device rules → 3.1 LPMOS main module → 3.1.1 Layer rules → POLY1

**Figure 3.7** POLY1

3. Layer and Device rules → 3.1 LPMOS main module→ 3.1.1 Layer rules→ P1DUMMY

P1DUMMY

It is recommended to use X-FAB's dummy pattern generation option (DUMMY_FILL included in the DRC for preview) to create dummy pattern. If the generated dummy pattern is not sufficient to meet the minimum requirements for pattern density, customers can draw additional dummy pattern following the dummy design rules (DIFFDUMMY, P1DUMMY, M1DUMMY, M2DUMMY, M3DUMMY, M4DUMMY, M5DUMMY, MTPDUMMY and MTPLDUMMY). For further information, refer to the design related guideline "Dummy Pattern Generation".

Name	Description	Value	Unit
B1YP	Only rectangular P1DUMMY is allowed	-	-
B2YP	P1DUMMY overlap of POLY1 is not allowed	-	-
B3YP	P1DUMMY overlap of CONT is not allowed	-	-
B5YP	P1DUMMY overlap of SBLK is not allowed	-	-
B6YP	P1DUMMY overlap of MRES or HRES is not allowed	-	-
B7YP	P1DUMMY overlap of HVDEPL is not allowed	-	-
B8YP	P1DUMMY overlap of PHODEF is not allowed	-	-
W1YP	Minimum P1DUMMY width	1.0	μm
S1YP	Minimum P1DUMMY spacing	1.0	μm
S10YP	Minimum P1DUMMY spacing to LOCKED	3.6	μm
S11YP	Minimum P1DUMMY spacing to LOCKED1	3.6	μm
S12YP	Minimum P1DUMMY spacing to LOCKED2	3.6	μm
S13YP	Minimum P1DUMMY spacing to LOCKED3	3.6	μm
S14YP	Minimum P1DUMMY spacing to LOCKED4	3.6	μm
S1YPDF	Minimum P1DUMMY spacing to DIFF	3.0	μm
S1YPHL	Minimum P1DUMMY spacing to HVDEPL	5.0	μm
S1YPHW	Minimum P1DUMMY spacing to HNW	10.0	μm
S1YPNW	Minimum P1DUMMY spacing to NW4DMY	5.0	μm
S1YPP1	Minimum P1DUMMY spacing to POLY1	3.0	μm
S1YPP1	Minimum P1DUMMY spacing to PW4DMY	5.0	μm
S1YPSB	Minimum P1DUMMY spacing to SBLK	3.0	μm
S1YPWD	Minimum P1DUMMY spacing to DNWELL	10.0	μm
S1YPWM	Minimum P1DUMMY spacing to DNWELLMV	5.0	μm
	Note: Valid if DNWELLMV is outside DNWELL.		
S1YPYD	Minimum P1DUMMY spacing to DIFFDUMMY	0.4	μm
E1YPHW	Minimum HNW enclosure of P1DUMMY	10.0	μm
E1YPNW	Minimum NW4DMY enclosure of P1DUMMY	5.0	μm
E1YPP1	Minimum PW4DMY enclosure of P1DUMMY	5.0	μm
E1YPWD	Minimum DNWELL enclosure of P1DUMMY	10.0	μm
E1YPWM	Minimum DNWELLMV enclosure of P1DUMMY	5.0	μm
	Note: Valid if DNWELLMV is outside DNWELL.		

3. Layer and Device rules → 3.1 LPMOS main module → 3.1.1 Layer rules → P1DUMMY

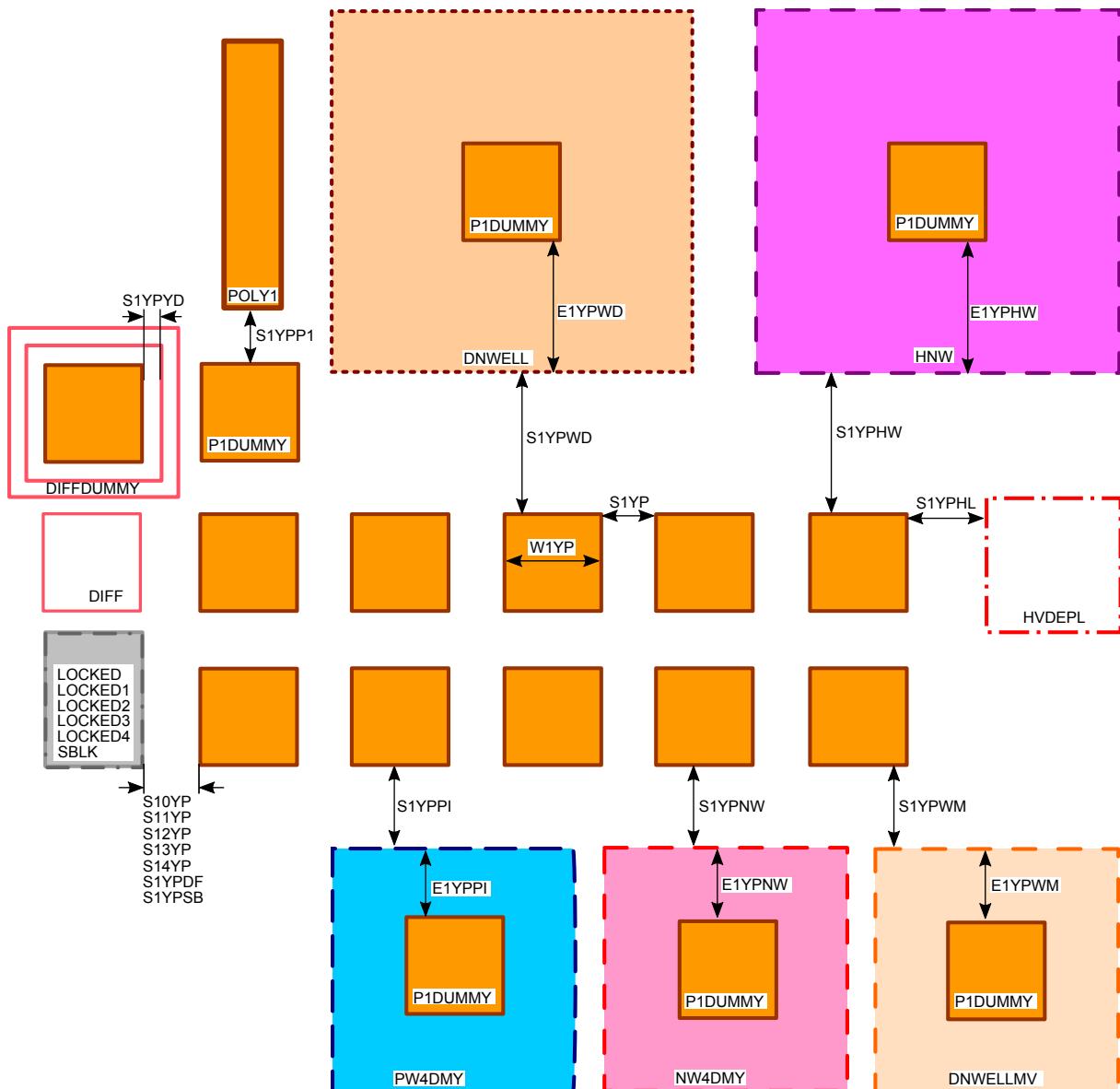


Figure 3.8 P1DUMMY

3. Layer and Device rules → 3.1 LPMOS main module→ 3.1.1 Layer rules→ HRES

HRES

Name	Description	Value	Unit
B1HR	HRES overlap of DIFF is not allowed	-	-
B3HR	PIMP overlap of HRES is not allowed	-	-
B4HR	POLY1 crossing HRES edge is not allowed	-	-
B6HR	NIMP crossing HRES edge is not allowed	-	-
W1HR	Minimum HRES width	0.44	μm
S1HR	Minimum HRES spacing/notch	0.44	μm
S1HRDF	Minimum HRES spacing to DIFF	0.32	μm
S1HRIN	Minimum HRES spacing to NIMP	0.44	μm
S1HRIP	Minimum HRES spacing to PIMP	0.44	μm
S1HRP1	Minimum HRES spacing to POLY1	0.32	μm
E1HRP1	Minimum HRES enclosure of POLY1	0.18	μm

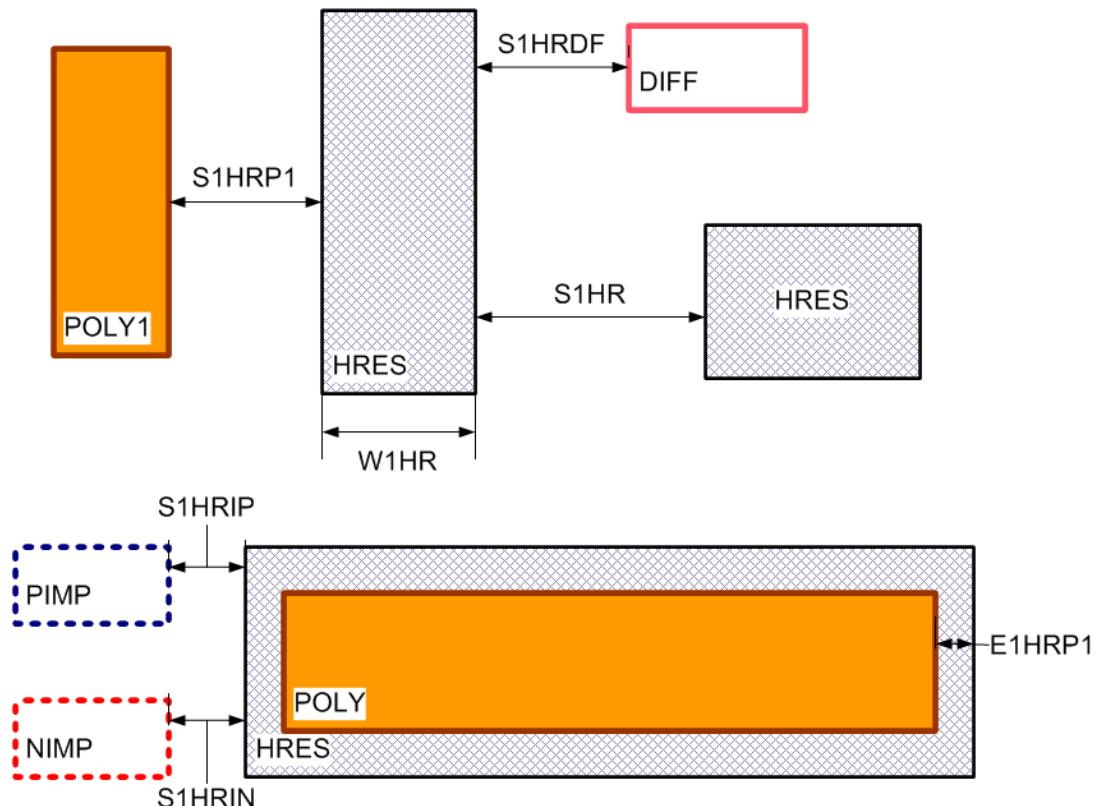


Figure 3.9 HRES

3. Layer and Device rules → 3.1 LPMOS main module → 3.1.1 Layer rules → SBLK

SBLK

SBLK is only allowed for primitive devices.

Name	Description	Value	Unit
W1SB	Minimum SBLK width	0.43	μm
S1SB	Minimum SBLK spacing/notch	0.43	μm
S1SBCT	Minimum SBLK spacing to CONT	0.22	μm
S1SBDF	Minimum SBLK spacing to DIFF	0.22	μm
S1SBGA	Minimum SBLK spacing to GATE	0.45	μm
S1SBP1	Minimum SBLK spacing to POLY1	0.3	μm
E1DFSB	Minimum DIFF extension beyond SBLK	0.22	μm
E1SBDF	Minimum SBLK extension beyond DIFF	0.22	μm
E1SBP1	Minimum SBLK extension beyond POLY1	0.22	μm
O1SBGA	Minimum SBLK overlap of GATE	0.05	μm
Note: It is recommended to use SBLK over GATE only for IO blocks and ESD protection.			
A1SB	Minimum SBLK area	2.0	μm ²

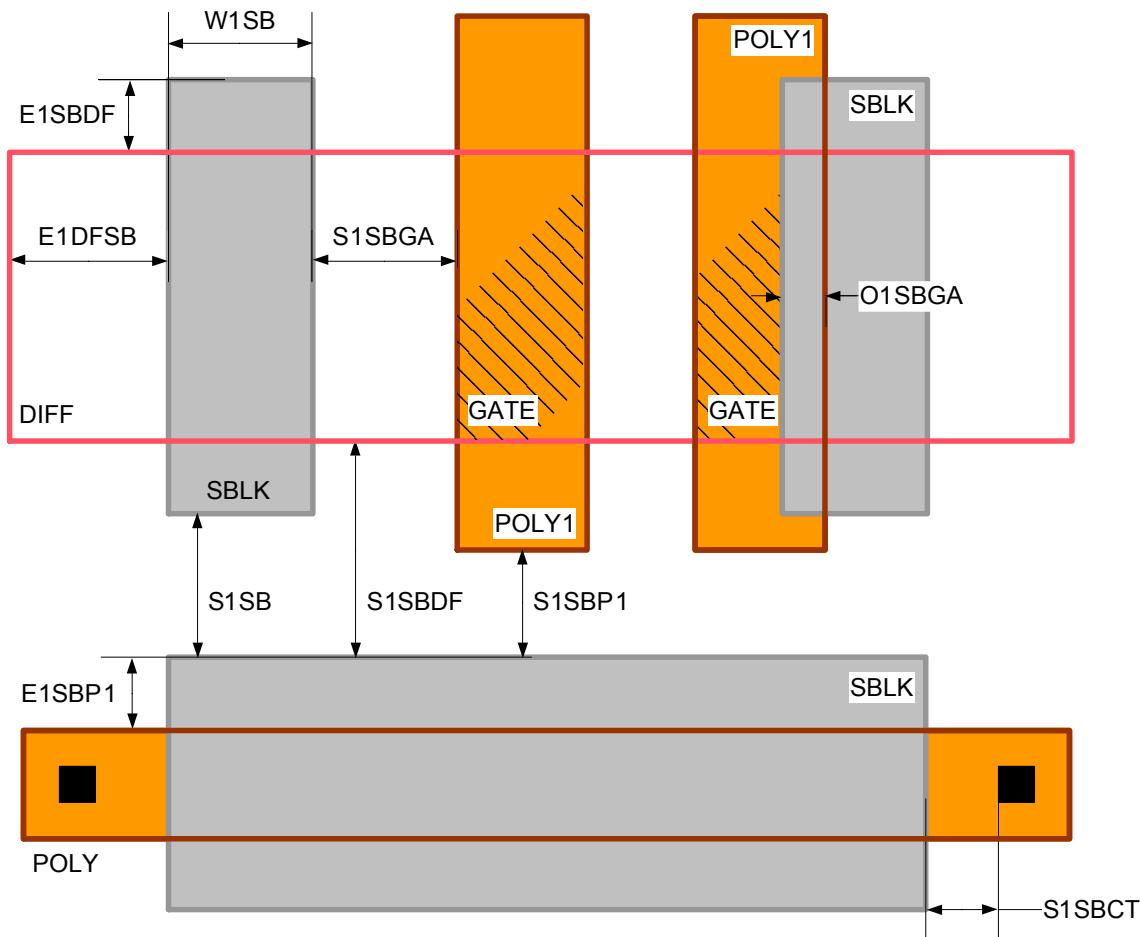


Figure 3.10 SBLK

3. Layer and Device rules → 3.1 LPMOS main module→ 3.1.1 Layer rules→ NIMP

NIMP

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
W1IN	Minimum NIMP width	0.44	μm
S1IN	Minimum NIMP spacing/notch	0.44	μm
S1INDP	Minimum NIMP spacing to PDIFF	0.1	μm
S2INDP	Minimum NIMP spacing to PDIFF (in NTYPE1_WELL)	0.26	μm
S3INDP	Minimum NIMP spacing to PDIFF (if PDIFF to NTYPE1_WELL spacing is <0.43μm)	0.18	μm
E1DNP1	Minimum NDIFF extension beyond POLY1	0.32	μm
E1INDF	Minimum NIMP extension beyond DIFF	0.18	μm
E1INDN	Minimum NIMP extension beyond POLY1/NDIFF in direction of POLY1	0.35	μm
E2INDF	Minimum NIMP extension beyond DIFF (in NTYPE1_WELL) (if NTYPE1_WELL enclosure of NDIFF is >=0.43μm)	0.02	μm
O1INDF	Minimum DIFF overlap of NIMP	0.23	μm
A1IN	Minimum NIMP area	0.3844	μm ²

3. Layer and Device rules → 3.1 LPMOS main module → 3.1.1 Layer rules → NIMP

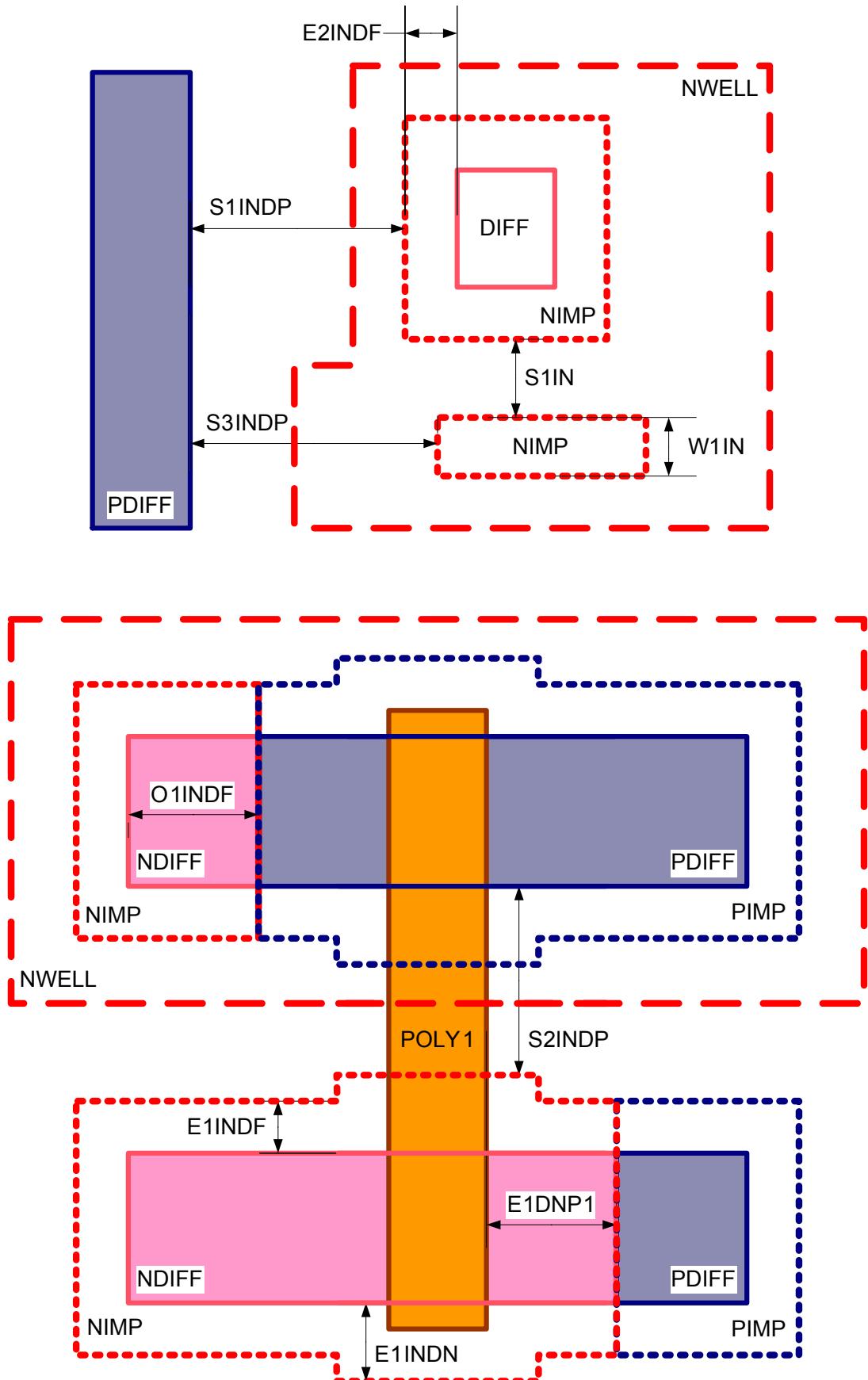


Figure 3.11 NIMP

3. Layer and Device rules → 3.1 LPMOS main module→ 3.1.1 Layer rules→ PIMP

PIMP

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1IPIN	PIMP overlap of NIMP is not allowed	-	-
W1IP	Minimum PIMP width	0.44	μm
S1IP	Minimum PIMP spacing/notch	0.44	μm
S1IPDN	Minimum PIMP spacing to NDIFF (outside NTYPE1_WELL)	0.26	μm
S2IPDN	Minimum PIMP spacing to NDIFF (in NTYPE1_WELL) (if NTYPE1_WELL enclosure of NDIFF is >=0.43μm)	0.1	μm
S3IPDN	Minimum PIMP spacing to NDIFF (in NTYPE1_WELL) (if NTYPE1_WELL enclosure of NDIFF is <0.43μm)	0.18	μm
E1DPP1	Minimum PDIFF extension beyond POLY1 (except dsb#)	0.32	μm
E1IPDF	Minimum PIMP extension beyond DIFF	0.18	μm
E1IPDP	Minimum PIMP extension beyond POLY1/PDIFF in direction of POLY1	0.35	μm
E2IPDF	Minimum PIMP extension beyond DIFF (outside NTYPE1_WELL) (if NTYPE1_WELL spacing to PDIFF is >=0.43μm)	0.02	μm
O1IPDF	Minimum DIFF overlap of PIMP	0.23	μm
A1IP	Minimum PIMP area	0.3844	μm ²

3. Layer and Device rules → 3.1 LPMOS main module → 3.1.1 Layer rules → PIMP

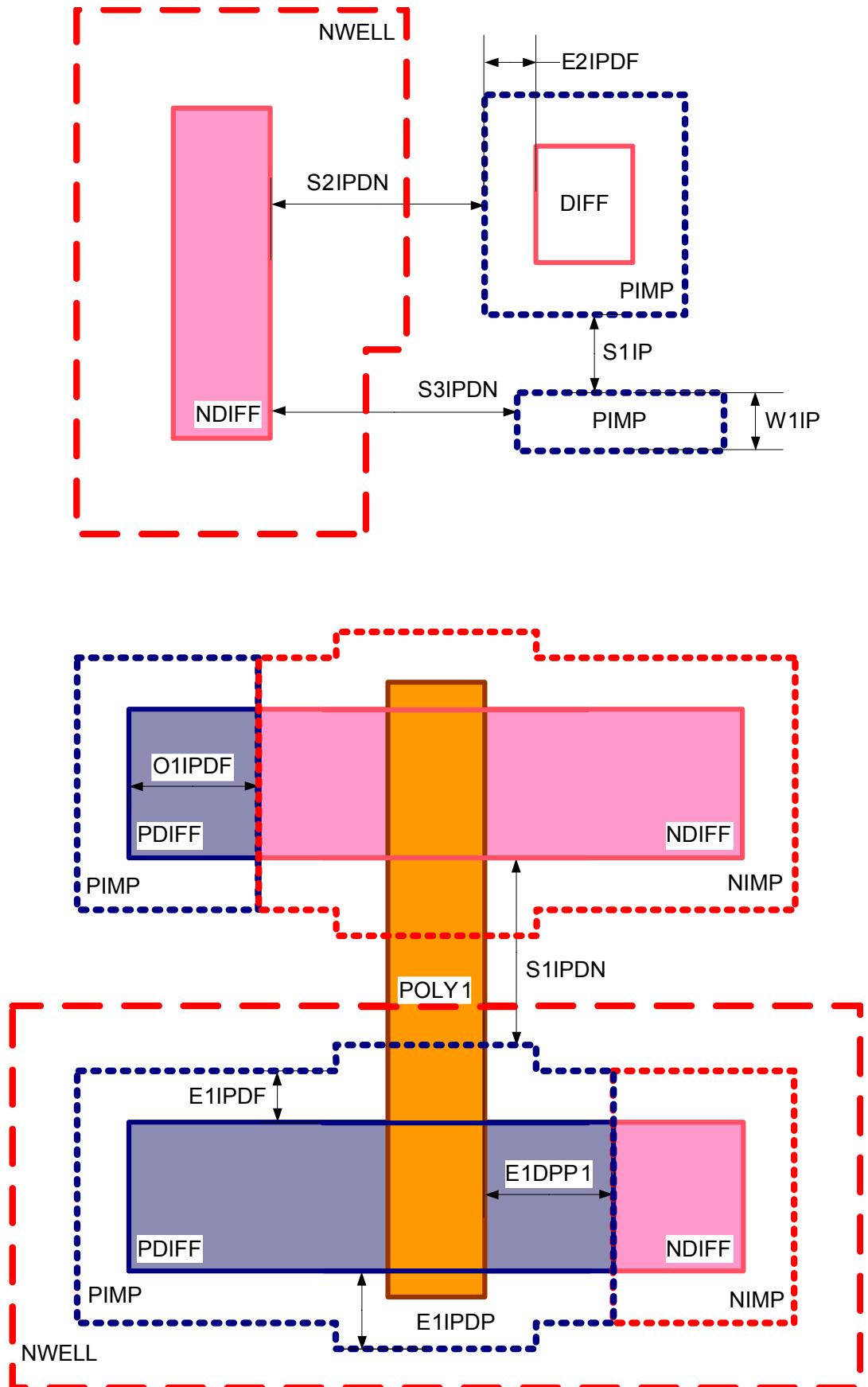


Figure 3.12 PIMP

3. Layer and Device rules → 3.1 LPMOS main module→ 3.1.1 Layer rules→ CONT

CONT

Name	Description	Value	Unit
B1CT	CONT without NDIFF or PDIFF or POLY1 is not allowed (except dsb#)	-	-
B1CTGA	CONT overlap of GATE is not allowed (except davla#)	-	-
B1CTSB	CONT overlap of SBLK is not allowed	-	-
B3CT	CONT stripes are only allowed to bend at 135 degrees	-	-
W2CT	Fixed CONT stripe width Note: Stripes are only allowed for use with photodiodes or other optical purposes.	0.22	μm
W1CT	Fixed CONT size (except dphoc#, dphod#, DIFF within PHODIO)	0.22 x 0.22	μm x μm
S1CT	Minimum CONT spacing	0.25	μm
S2CT	Minimum CONT spacing (for contact arrays containing more than 4x4 elements) Note: Two contact regions within 0.3 μm spacing are considered to be in the same array.	0.28	μm
S3CT	Minimum CONT stripe to CONT spacing	0.39	μm
S4CT	Minimum CONT stripe spacing/notch	0.67	μm
S1CTDF	Minimum CONT spacing to DIFF	0.2	μm
S1CTP1	Minimum CONT spacing to POLY1 (except davla#)	0.16	μm
E1CTIN	Minimum NIMP enclosure of DIFFCON	0.12	μm
E1CTIP	Minimum PIMP enclosure of DIFFCON	0.12	μm
E1DFCT	Minimum DIFF enclosure of CONT	0.1	μm
E1P1CT	Minimum POLY1 enclosure of CONT (except davla#)	0.1	μm
R1CT	Maximum ratio of CONT area to connected GATE area	10.0	-

3. Layer and Device rules → 3.1 LPMOS main module → 3.1.1 Layer rules → CONT

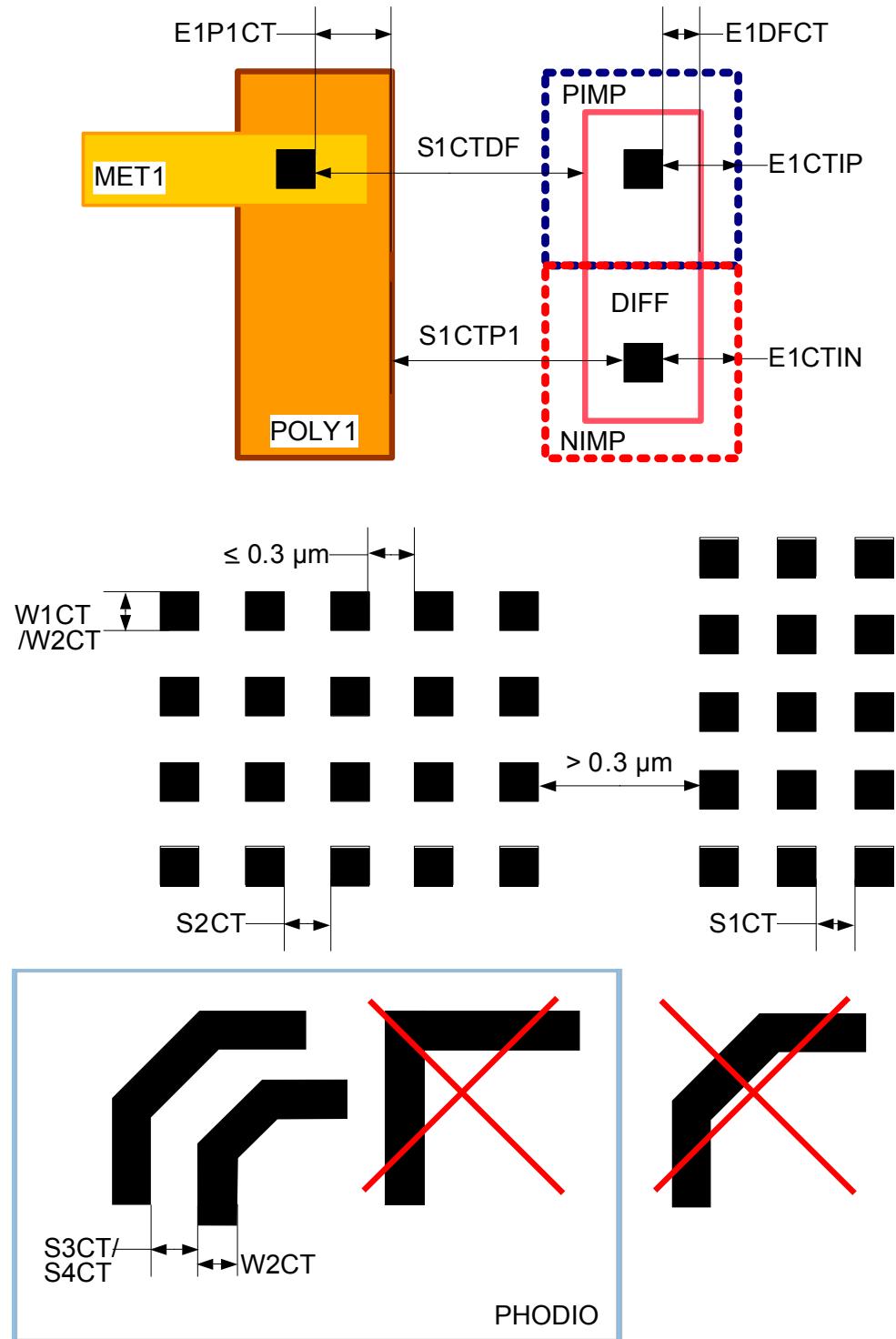


Figure 3.13 CONT

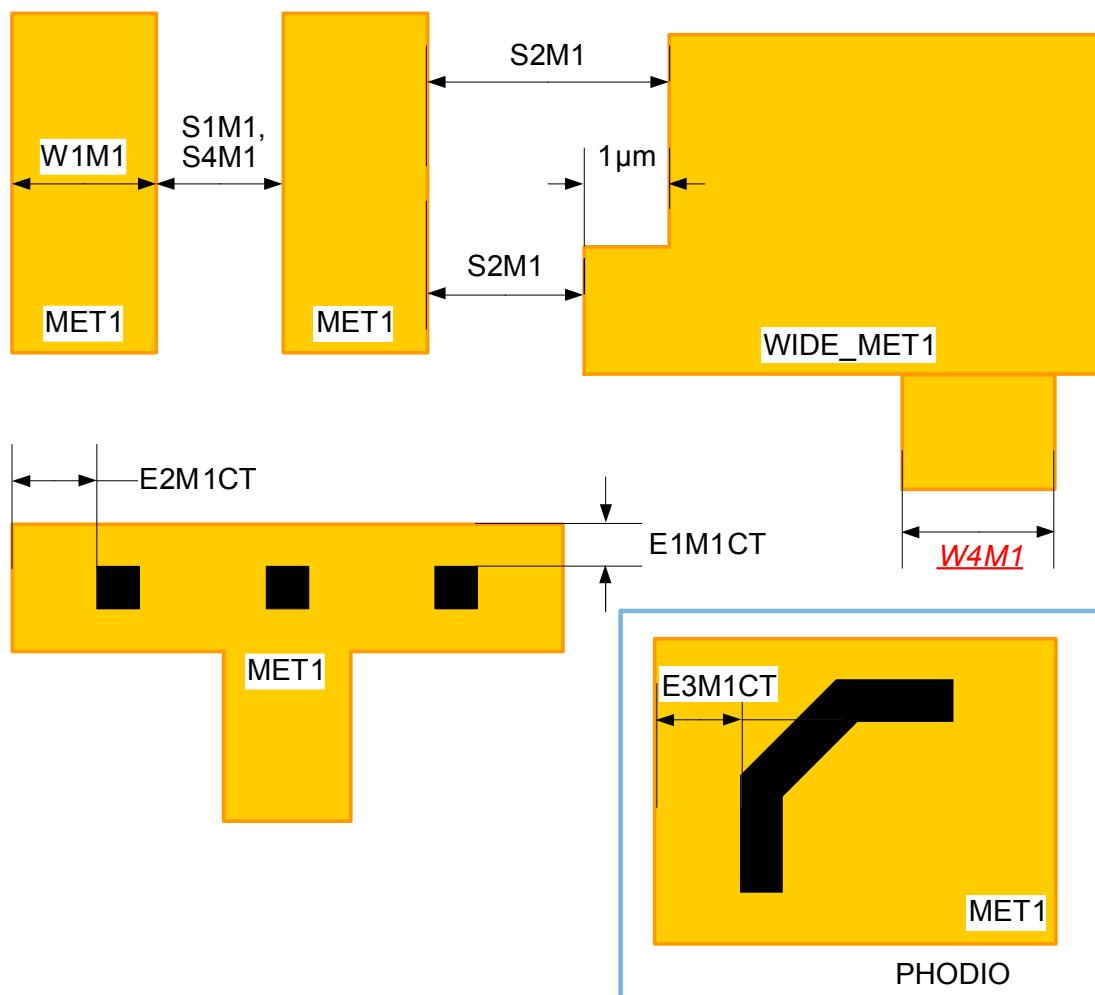
3. Layer and Device rules → 3.1 LPMOS main module→ 3.1.1 Layer rules→ MET1

MET1

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1CTM1	CONT must be covered by MET1	-	-
B1M1	All MET1 tracks > 35µm wide to be slotted (except Pads)	-	-
W1M1	Minimum MET1 width	0.23	µm
<i>W4M1</i>	Minimum MET1 width joining wide MET1 track (> 35 µm)	10.0	µm
	Note: No slot is allowed opposite the join. It is recommended to maintain this width for at least 1 µm from the main track prior to narrowing it.		
<i>W5M1</i>	Maximum MET1 region size	17.0 x 17.0	µm x µm
	Note: Not checked with standard DRC, option for check is available. Note: MET1 regions are defined as MET1 shapes (single MET1 shapes or a bundle of MET1 shapes, with width > 2.0µm, inclusive of the spacing if the spacing is <= 1.0µm) without any other metal layer above. For further information and design guidelines, please refer to the application note about IMD popping on "my X-FAB".		
S1M1	Minimum MET1 spacing/notch	0.23	µm
S4M1	Minimum MET1 spacing (different net, tag_60v)	0.38	µm
	Note: Valid for spacing of all MET1 shapes with label tag_60v to all MET1 shapes having lower voltage classes. Refer to the design related guideline "Voltage class definitions".		
S2M1	Minimum MET1 spacing to WIDE_MET1	0.6	µm
E1M1CT	Minimum MET1 enclosure of CONT	0.005	µm
E2M1CT	Minimum MET1 enclosure of CONT (in one direction of CONT corner)	0.06	µm
E3M1CT	Minimum MET1 enclosure of CONT stripe	0.07	µm
A1M1	Minimum MET1 area	0.202	µm ²
<i>R1M1</i>	Minimum ratio of MET1 area to EXTENT area	30.0	%
	Note: Not checked with standard DRC, option for check is available.		
<i>R2M1</i>	Maximum ratio of MET1 area to EXTENT area	65.0	%
	Note: Not checked with standard DRC, option for check is available.		
R1M1P1	Maximum ratio of MET1 area to connected GATE area	400.0	-
	Note: Refer to section "Antenna Rule definitions" as well.		
R2M1P1	Maximum ratio of MET1 area to connected GATE area	400.0	-
	Note: Refer to section "Antenna Rule definitions" as well.		
Q1M1	Resistor terminal net without VLABEL	-	-
	Note: Resistor having VLABEL at one terminal only is not allowed. Refer to the design related guideline "Voltage class definitions".		

3. Layer and Device rules → 3.1 LPMOS main module → 3.1.1 Layer rules → MET1

**Figure 3.14** MET1

3. Layer and Device rules → 3.1 LPMOS main module→ 3.1.1 Layer rules→ M1SLOT

M1SLOT

Name	Description	Value	Unit
W2M1	Minimum M1SLOT width	0.6	μm
	Minimum M1SLOT length	20.0	μm
W3M1	Note: If this rule cannot be adhered to, it is suggested that the track in question is drawn as two narrow parallel tracks.		
S3M1	Minimum M1SLOT spacing/notch	10.0	μm
E1M1M1	Minimum MET1 enclosure of M1SLOT Note: M1SLOT without MET1 is not allowed.	10.0	μm

Note: Insert M1SLOTS in direction of current flow.

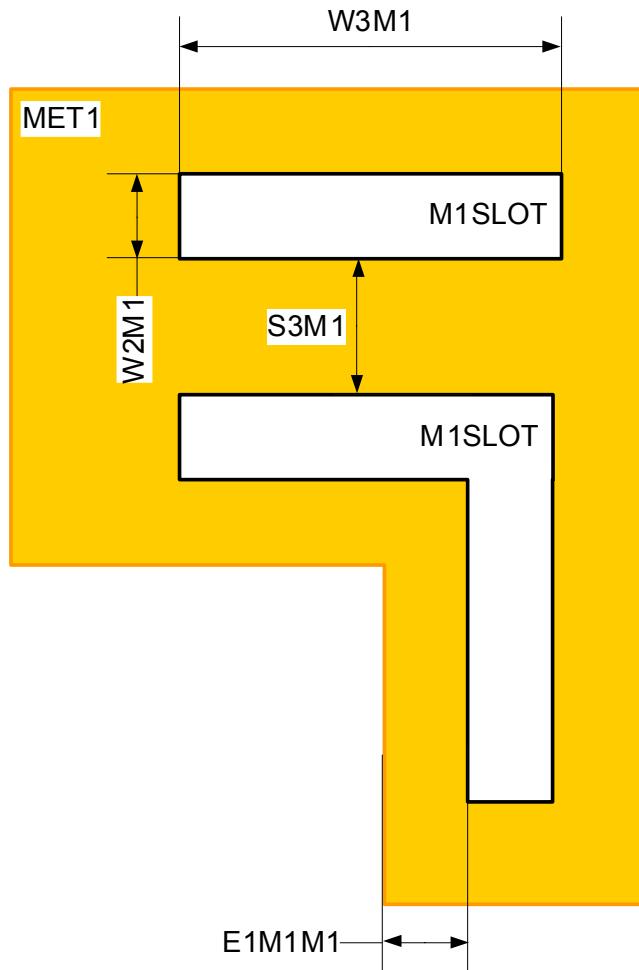


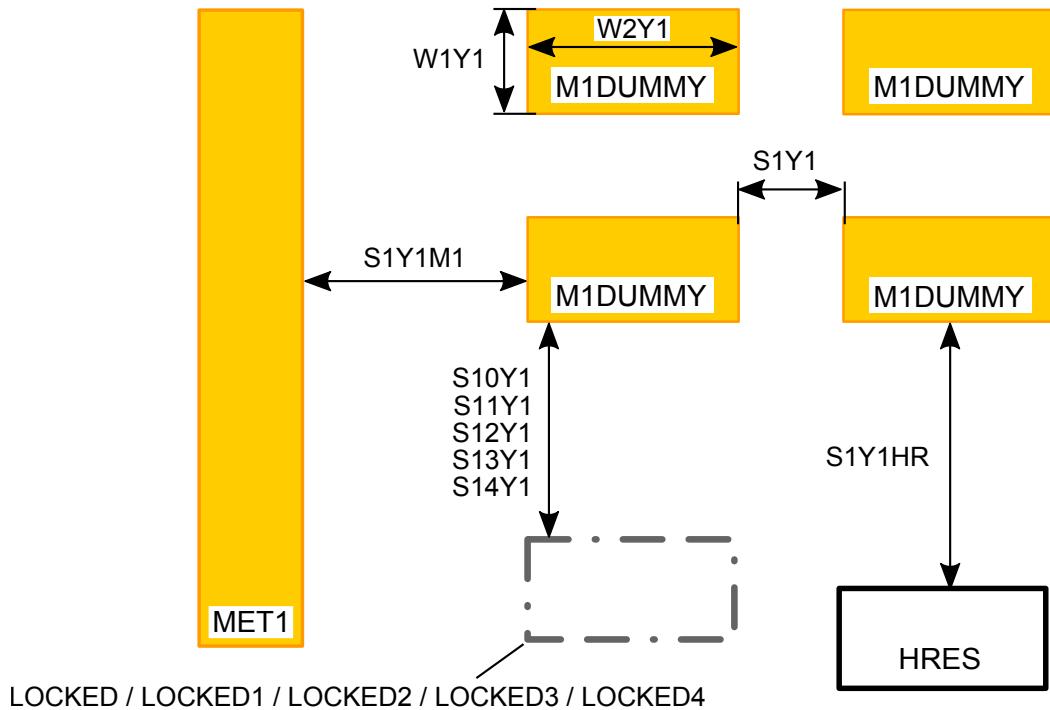
Figure 3.15 M1SLOT

3. Layer and Device rules → 3.1 LPMOS main module→ 3.1.1 Layer rules→ M1DUMMY

M1DUMMY

It is recommended to use X-FAB's dummy pattern generation option (DUMMY_FILL included in the DRC for preview) to create dummy pattern. If the generated dummy pattern is not sufficient to meet the minimum requirements for pattern density, customers can draw additional dummy pattern following the dummy design rules (DIFFDUMMY, P1DUMMY, M1DUMMY, M2DUMMY, M3DUMMY, M4DUMMY, M5DUMMY, MTPDUMMY and MTPLDUMMY). For further information, refer to the design related guideline "Dummy Pattern Generation".

Name	Description	Value	Unit
B1Y1	Only rectangular M1DUMMY is allowed	-	-
B2Y1	M1DUMMY overlap of MET1 is not allowed	-	-
B3Y1	M1DUMMY overlap of CONT or VIA1 is not allowed	-	-
B4Y1	M1DUMMY overlap of HRES is not allowed	-	-
W1Y1	Minimum M1DUMMY width	2.0	μm
W2Y1	Maximum M1DUMMY edge length	20.0	μm
S1Y1	Minimum M1DUMMY spacing	2.0	μm
S10Y1	Minimum M1DUMMY spacing to LOCKED	4.0	μm
S11Y1	Minimum M1DUMMY spacing to LOCKED1	4.0	μm
S12Y1	Minimum M1DUMMY spacing to LOCKED2	4.0	μm
S13Y1	Minimum M1DUMMY spacing to LOCKED3	4.0	μm
S14Y1	Minimum M1DUMMY spacing to LOCKED4	4.0	μm
S1Y1HR	Minimum M1DUMMY spacing to HRES	5.0	μm
S1Y1M1	Minimum M1DUMMY spacing to MET1	4.0	μm

**Figure 3.16 M1DUMMY**

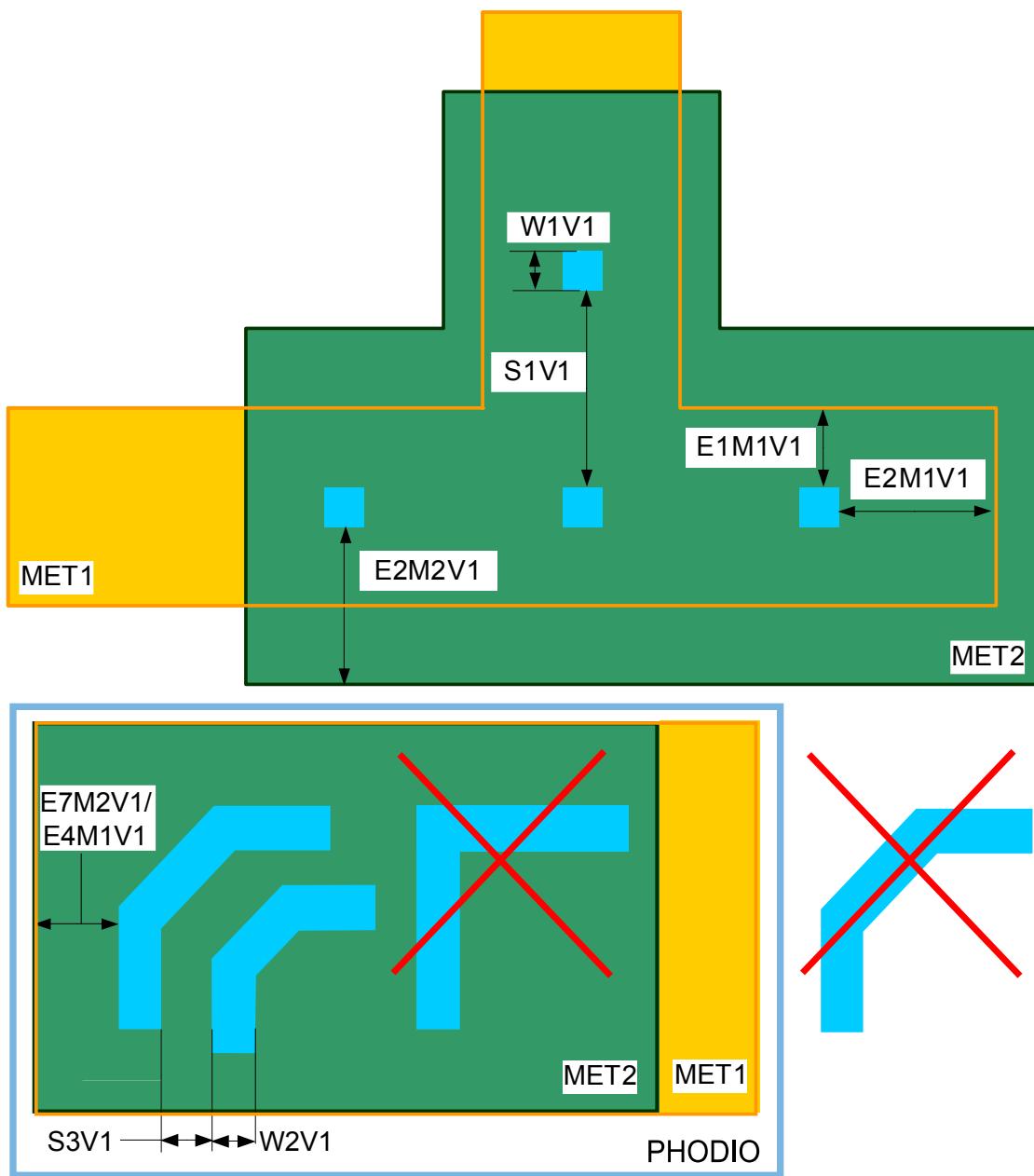
3. Layer and Device rules → 3.1 LPMOS main module→ 3.1.1 Layer rules→ VIA1

VIA1

Name	Description	Value	Unit
B1V1	VIA1 must be covered by MET1 and MET2	-	-
B2V1	VIA1 stripes are only allowed to bend at 135 degrees	-	-
W2V1	Fixed VIA1 stripe width Note: Stripes are only allowed for use with photodiodes or other optical purposes.	0.26	µm
W1V1	Fixed VIA1 size (except dphoc#, dphod#, PHODIO, OPTOVIA1)	0.26 x 0.26	µm x µm
S1V1	Minimum VIA1 spacing	0.26	µm
S3V1	Minimum VIA1 stripe to VIA1 spacing	1.0	µm
E1M1V1	Minimum MET1 enclosure of VIA1	0.01	µm
E1M2V1	Minimum MET2 enclosure of VIA1	0.01	µm
E2M1V1	Minimum MET1 enclosure of VIA1 (in one direction of VIA1 corner)	0.06	µm
E2M2V1	Minimum MET2 enclosure of VIA1 (in one direction of VIA1 corner)	0.06	µm
E4M1V1	Minimum MET1 enclosure of VIA1 stripe	0.1	µm
E7M2V1	Minimum MET2 enclosure of VIA1 stripe	0.1	µm
R1V1	Maximum ratio of VIA1 area to connected GATE area	20.0	-
Q20V1	Check for the right usage of OPTOVIA1 Note: VIA1 stripes must only be used for light shielding purpose.	-	-

Note: Bond pads require interconnecting vias between the metal layers. See section "Bond Pad".

3. Layer and Device rules → 3.1 LPMOS main module → 3.1.1 Layer rules → VIA1

**Figure 3.17 VIA1**

3. Layer and Device rules → 3.1 LPMOS main module→ 3.1.1 Layer rules→ MET2

MET2

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1M2	All MET2 tracks > 35µm wide to be slotted (except Pads, dphoc0, dphod0)	-	-
W1M2	Minimum MET2 width	0.28	µm
<i>W4M2</i>	Minimum MET2 width joining wide MET2 track (> 35 µm)	10.0	µm
	Note: No slot is allowed opposite the join. It is recommended to maintain this width for at least 1 µm from the main track prior to narrowing it.		
<i>W5M2</i>	Maximum MET2 region size	17.0 x 17.0	µm x µm
	Note: Not checked with standard DRC, option for check is available.		
	Note: MET2 regions are defined as MET2 shapes (single MET2 shapes or a bundle of MET2 shapes, with width > 2.0µm, inclusive of the spacing if the spacing is <= 1.0µm) without any other metal layer above. For further information and design guidelines, please refer to the application note about IMD popping on "my X-FAB".		
S1M2	Minimum MET2 spacing/notch	0.28	µm
S4M2	Minimum MET2 spacing (different net, tag_60v)	0.4	µm
	Note: Valid for spacing of all MET2 shapes with label tag_60v to all MET2 shapes having lower voltage classes. Refer to the design related guideline "Voltage class definitions".		
S2M2	Minimum MET2 spacing to WIDE_MET2	0.6	µm
A1M2	Minimum MET2 area	0.202	µm ²
<i>R1M2</i>	Minimum ratio of MET2 area to EXTENT area	30.0	%
	Note: Not checked with standard DRC, option for check is available.		
<i>R2M2</i>	Maximum ratio of MET2 area to EXTENT area	65.0	%
	Note: Not checked with standard DRC, option for check is available.		
R1M2P1	Maximum ratio of MET2 area to connected GATE area	400.0	-
	Note: Refer to section "Antenna Rule definitions" as well.		
R2M2P1	Maximum ratio of MET2 area to connected GATE area	400.0	-
	Note: Refer to section "Antenna Rule definitions" as well.		
Q1M2	Resistor terminal net without VLABEL	-	-
	Note: Resistor having VLABEL at one terminal only is not allowed. Refer to the design related guideline "Voltage class definitions".		

3. Layer and Device rules → 3.1 LPMOS main module→ 3.1.1 Layer rules→ MET2

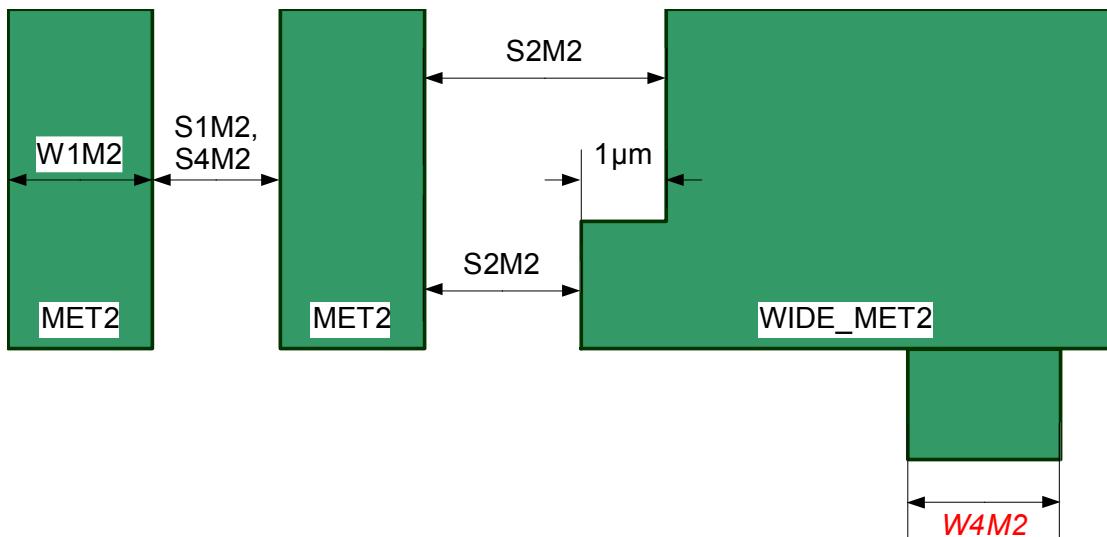


Figure 3.18 MET2

3. Layer and Device rules → 3.1 LPMOS main module → 3.1.1 Layer rules → M2SLOT

M2SLOT

Name	Description	Value	Unit
W2M2	Minimum M2SLOT width	0.6	μm
W3M2	Minimum M2SLOT length	20.0	μm
	Note: If this rule cannot be adhered to, it is suggested that the track in question is drawn as two narrow parallel tracks.		
S3M2	Minimum M2SLOT spacing/notch	10.0	μm
S1M2M1	Minimum M2SLOT spacing to M1SLOT	2.0	μm
	Note: M2SLOT is not allowed over M1SLOT.		
E1M2M2	Minimum MET2 enclosure of M2SLOT	10.0	μm
	Note: M2SLOT without MET2 is not allowed		

Note: Insert M2SLOTS in direction of current flow.

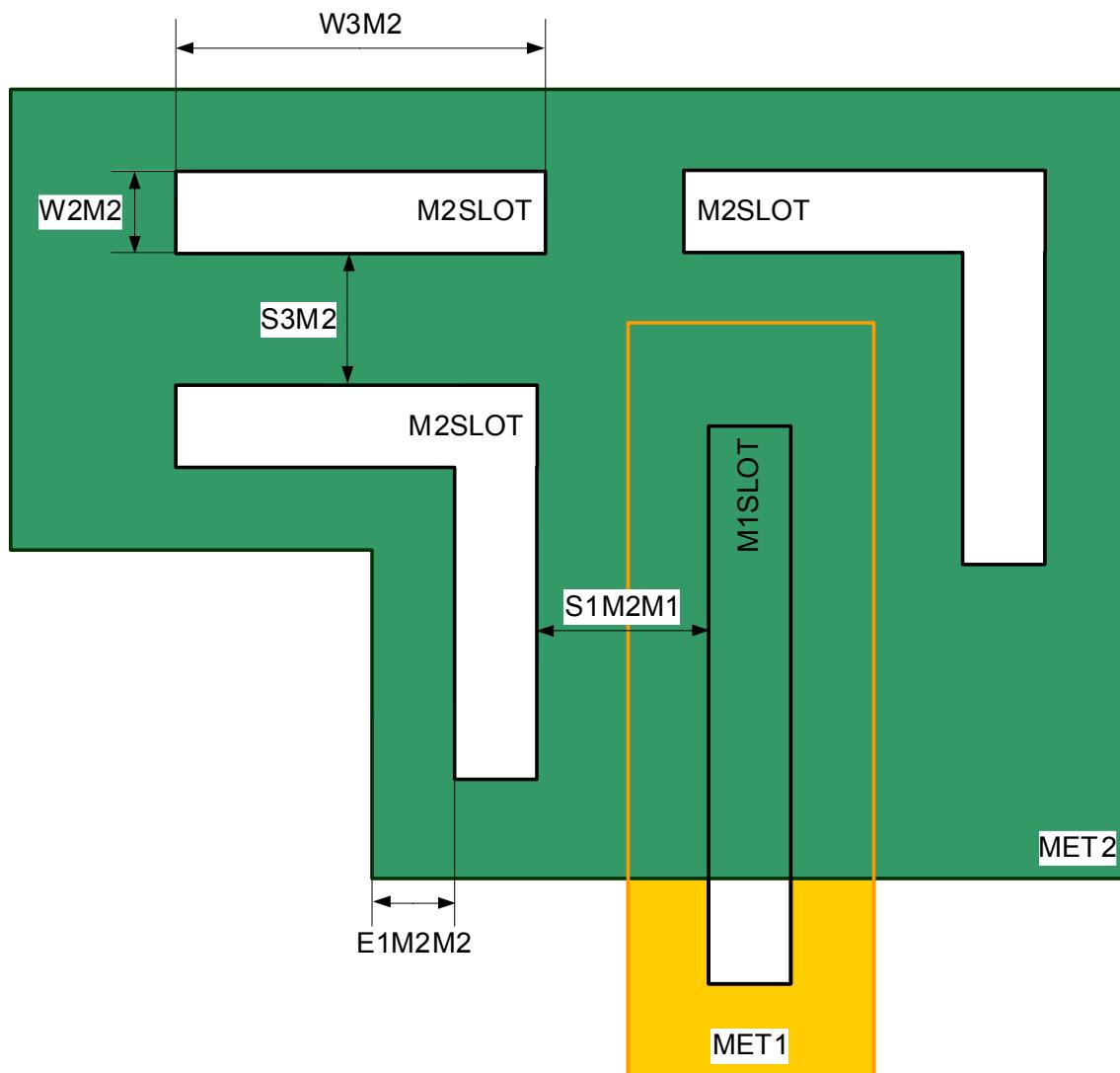


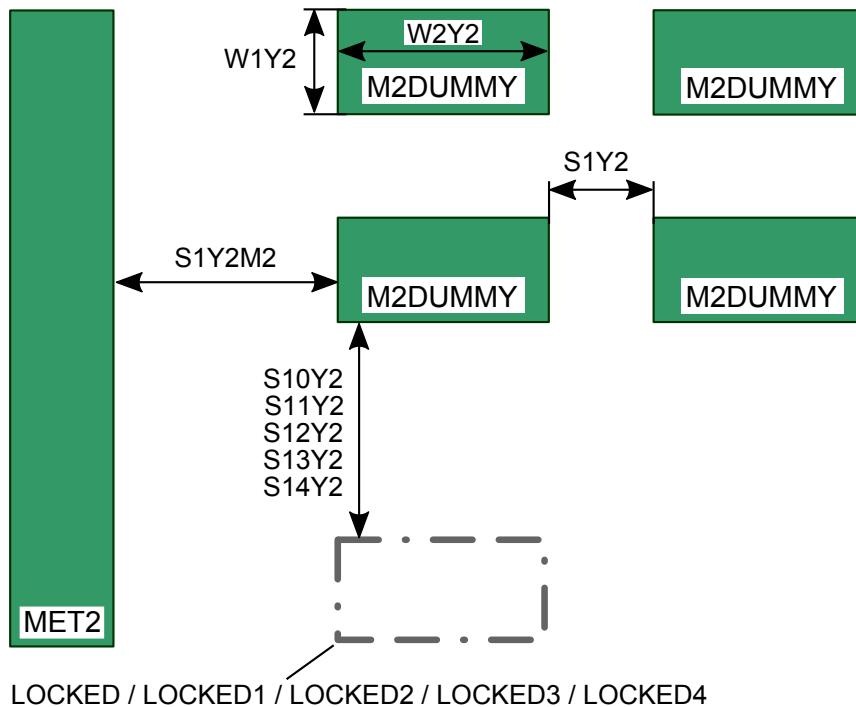
Figure 3.19 M2SLOT

3. Layer and Device rules → 3.1 LPMOS main module → 3.1.1 Layer rules → M2DUMMY

M2DUMMY

It is recommended to use X-FAB's dummy pattern generation option (DUMMY_FILL included in the DRC for preview) to create dummy pattern. If the generated dummy pattern is not sufficient to meet the minimum requirements for pattern density, customers can draw additional dummy pattern following the dummy design rules (DIFFDUMMY, P1DUMMY, M1DUMMY, M2DUMMY, M3DUMMY, M4DUMMY, M5DUMMY, MTPDUMMY and MTPLDUMMY). For further information, refer to the design related guideline "Dummy Pattern Generation".

Name	Description	Value	Unit
B1Y2	Only rectangular M2DUMMY is allowed	-	-
B2Y2	M2DUMMY overlap of MET2 is not allowed	-	-
B3Y2V1	M2DUMMY overlap of VIA1 is not allowed	-	-
B3Y2V2	M2DUMMY overlap of VIA2 is not allowed	-	-
B3Y2VT	M2DUMMY overlap of VIATP is not allowed	-	-
Note: Only valid if module MET3 is not selected.			
W1Y2	Minimum M2DUMMY width	2.0	μm
W2Y2	Maximum M2DUMMY edge length	20.0	μm
S1Y2	Minimum M2DUMMY spacing	2.0	μm
S10Y2	Minimum M2DUMMY spacing to LOCKED	4.0	μm
S11Y2	Minimum M2DUMMY spacing to LOCKED1	4.0	μm
S12Y2	Minimum M2DUMMY spacing to LOCKED2	4.0	μm
S13Y2	Minimum M2DUMMY spacing to LOCKED3	4.0	μm
S14Y2	Minimum M2DUMMY spacing to LOCKED4	4.0	μm
S1Y2M2	Minimum M2DUMMY spacing to MET2	4.0	μm

**Figure 3.20 M2DUMMY****LOCKED, LOCKED1, LOCKED2**

This layer protects the IP core against routing (of specific layers) and is used to increase the safety of designs during IP replacement. LOCKED* layers are part of the X-FAB provided IP LEF file.

3. Layer and Device rules → 3.1 LPMOS main module→ 3.1.1 Layer rules→ LOCKED, LOCKED1, LOC...

Name	Description	Value	Unit
BDLOCK	Any structure over LOCKED (ALL) or LOCKED (boundary) is not allowed	-	-
B1LOCK	Any structure over LOCKED (LOCKED1) or LOCKED1 (boundary) is not allowed Note: Except: - METTPL if (MET4 and METMID) modules are selected or MET5 module is selected - METTP if MET5 module is selected	-	-
B2LOCK	Any structure over LOCKED (LOCKED2) or LOCKED2 (boundary) is not allowed Note: Except: - METTPL if (MET3 and METMID) modules are selected or MET4 module is selected - METTP if MET4 module is selected - MET5	-	-

LOCKED3

This layer protects the IP core against routing (of specific layers) and is used to increase the safety of designs during IP replacement. LOCKED* layers are part of the X-FAB provided IP LEF file.

Name	Description	Value	Unit
	Any structure over LOCKED3 is not allowed	-	-
B3LOCK	Note: Except: - METTPL if METMID module is selected or MET3 module is selected - METTP if MET3 module is selected - MET5 - MET4		

LOCKED4

This layer protects the IP core against routing (of specific layers) and is used to increase the safety of designs during IP replacement. LOCKED* layers are part of the X-FAB provided IP LEF file.

Name	Description	Value	Unit
	Any structure over LOCKED4 is not allowed	-	-
B4LOCK	Note: Except: - METTPL, METTP, MET5, MET4, MET3		

CAPDEF

This layer is only used to define certain capacitors.

DIODEF

This layer is used to define diodes that are to be extracted into the netlist. All diodes without DIODEF are extracted as parasitic components. DIODEF must encompass the entire P/N junction forming the diode.

3. Layer and Device rules → 3.1 LPMOS main module → 3.1.1 Layer rules → PHODEF

PHODEF

Important note: PHODEF is necessary to identify photodiodes derived from the basic diode constructions. Please make sure to draw it only for the light sensitive area. It must only be used for this purpose.

Name	Description	Value	Unit
B1D1	PHODEF without DIODEF is not allowed (except dphoa, dphob)	-	-
B1D1DF	PHODEF and DIFF without NIMP or PIMP or SBLK is not allowed (except dphoa, dphob)	-	-
B2D1	PHODEF without BLKALL is not allowed (except davla#)	-	-
B3D1	PHODEF and DIFF without SBLK is not allowed (except DIFFCON sized by 0.5µm, davla#)	-	-
W1DFD1	Maximum (DIFF overlap of PHODEF) bounding box size Note: The bounding box is the generated minimum rectangle enclosing the polygon.	502.0 x 502.0	µm x µm
O1SBIN	Minimum PHODEF and SBLK overlap of NIMP (except davla#)	0.22	µm
O1SBIP	Minimum PHODEF and SBLK overlap of PIMP	0.22	µm
Q1D1	Check for the right usage of the layer PHODEF	-	-

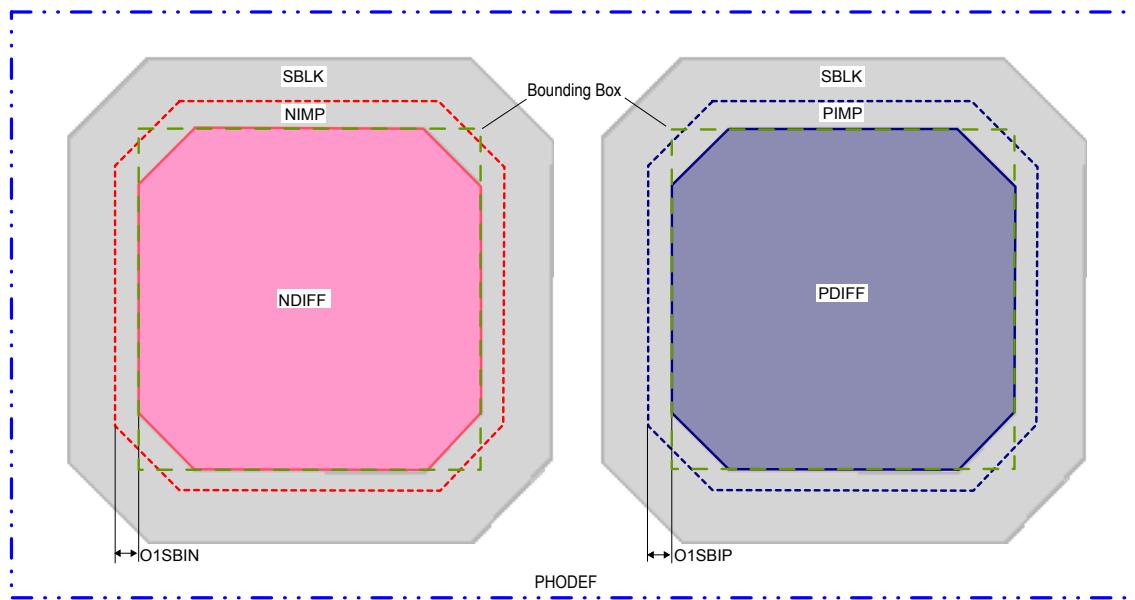


Figure 3.21 PHODEF

XFLAY

This layer is a reserved layer.

Name	Description	Value	Unit
BDXF	Not allowed to be used by customers	-	-

SUBCUT

Refer to the corresponding [application note](#) available on "my X-FAB" for information about this layer.

Name	Description	Value	Unit
B1SU	DIFF or *WELL crossing SUBCUT edge is not allowed Note: Not valid for DIFFDUMMY.	-	-

⇒

3. Layer and Device rules → 3.1 LPMOS main module→ 3.1.1 Layer rules→ SUBCUT

Name	Description	Value	Unit
Q1SU	Check for the right usage of the layer SUBCUT	-	-

3. Layer and Device rules → 3.1 LPMOS main module → 3.1.2 Device rules → ne, pe

3.1.2 Device rules

ne, pe

Name	Description	Value	Unit
W3DF	Minimum GATE width	0.22	μm
	Note: The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) having smaller GATE width than 0.22μm.		
W4P1	Minimum GATE length	0.18	μm
	Note: The design rule check error message W4P1 is also used generally for GATE areas (of any devices or shapes) being smaller than 0.18μm at any dimension.		

Note: For more extensive LVS, it is recommended to use the related 5 or 6 terminal device.

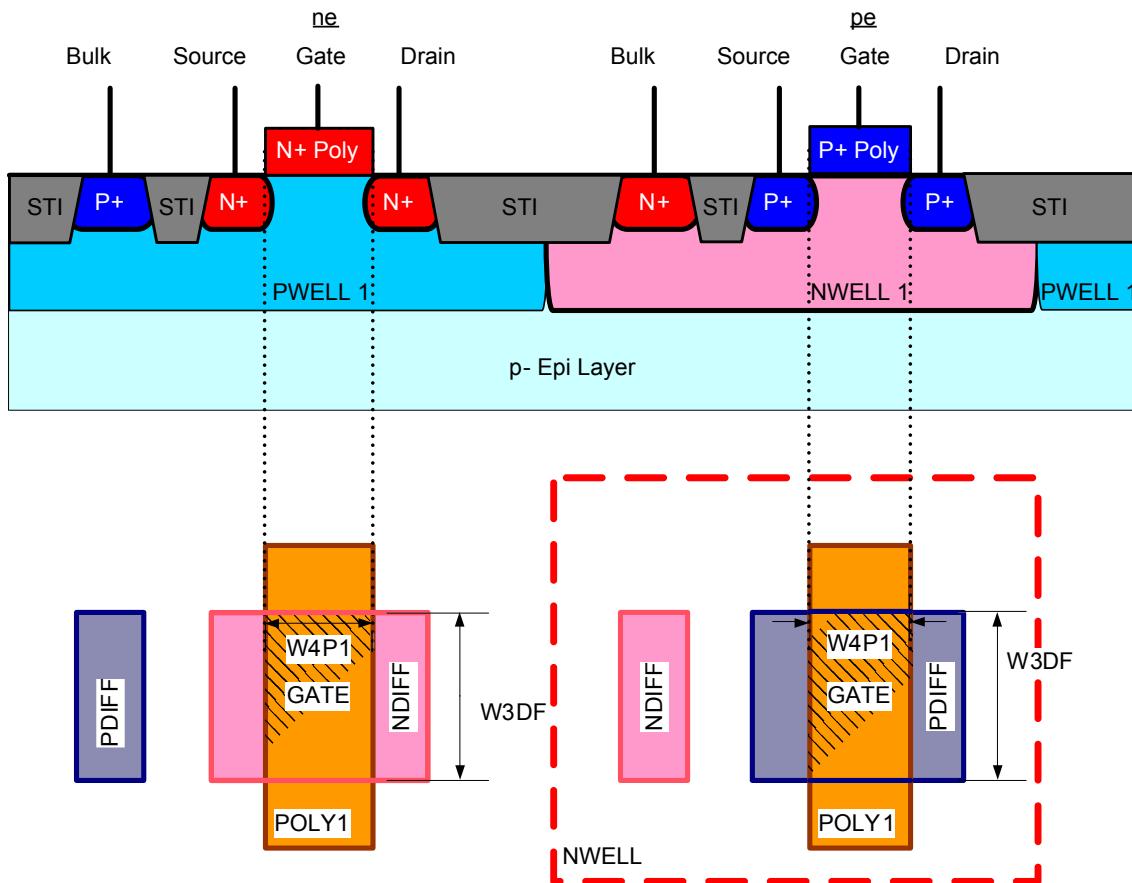


Figure 3.22 ne, pe

3. Layer and Device rules → 3.1 LPMOS main module → 3.1.2 Device rules → pe_5

pe_5

Name	Description	Value	Unit
W3DF	Minimum GATE width	0.22	μm
	Note: The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) having smaller GATE width than 0.22μm.		
W4P1	Minimum GATE length	0.18	μm
	Note: The design rule check error message W4P1 is also used generally for GATE areas (of any devices or shapes) being smaller than 0.18μm at any dimension.		

Note: pe_5 device must be labeled “5T” using POLY1 (VERIFICATION) layer over the GATE.

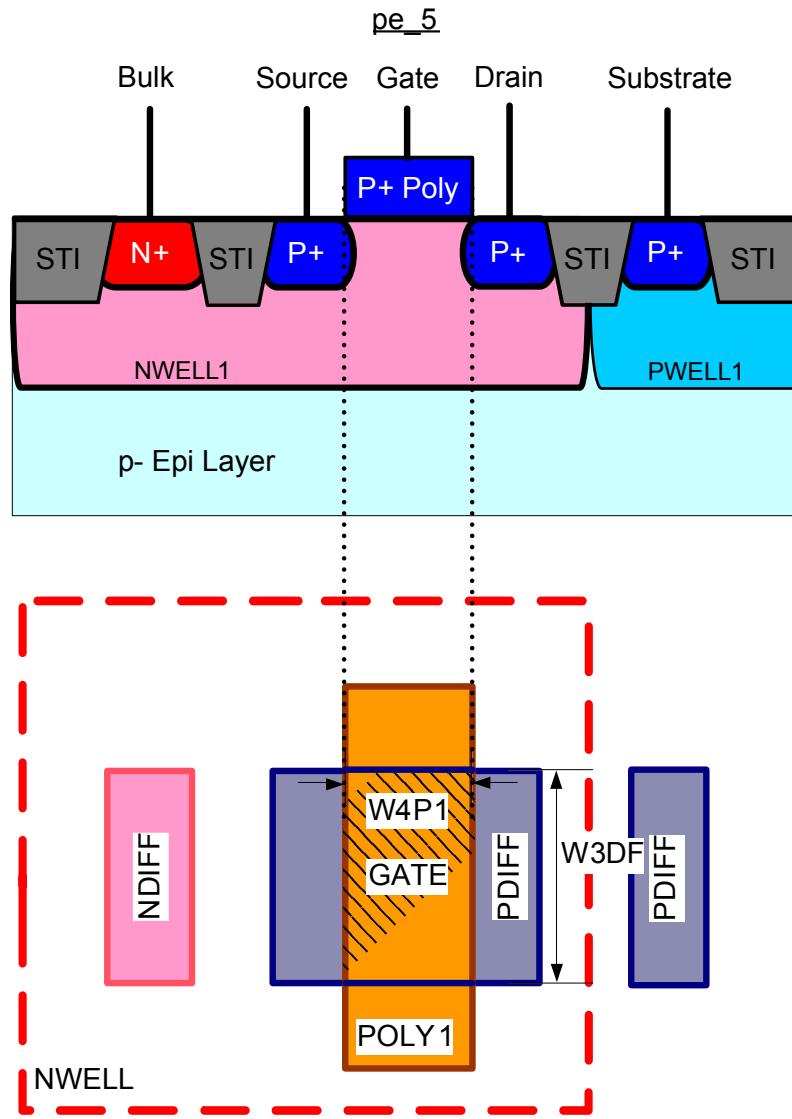


Figure 3.23 pe_5

3. Layer and Device rules → 3.1 LPMOS main module → 3.1.2 Device rules → nn3

nn3

Name	Description	Value	Unit
B3GA	Only rectangular GATE inside PWBLK is allowed	-	-
W4DF	Minimum GATE width	1.0	μm
W5P1	Minimum GATE length	1.0	μm

Note: MV is necessary for nn3.

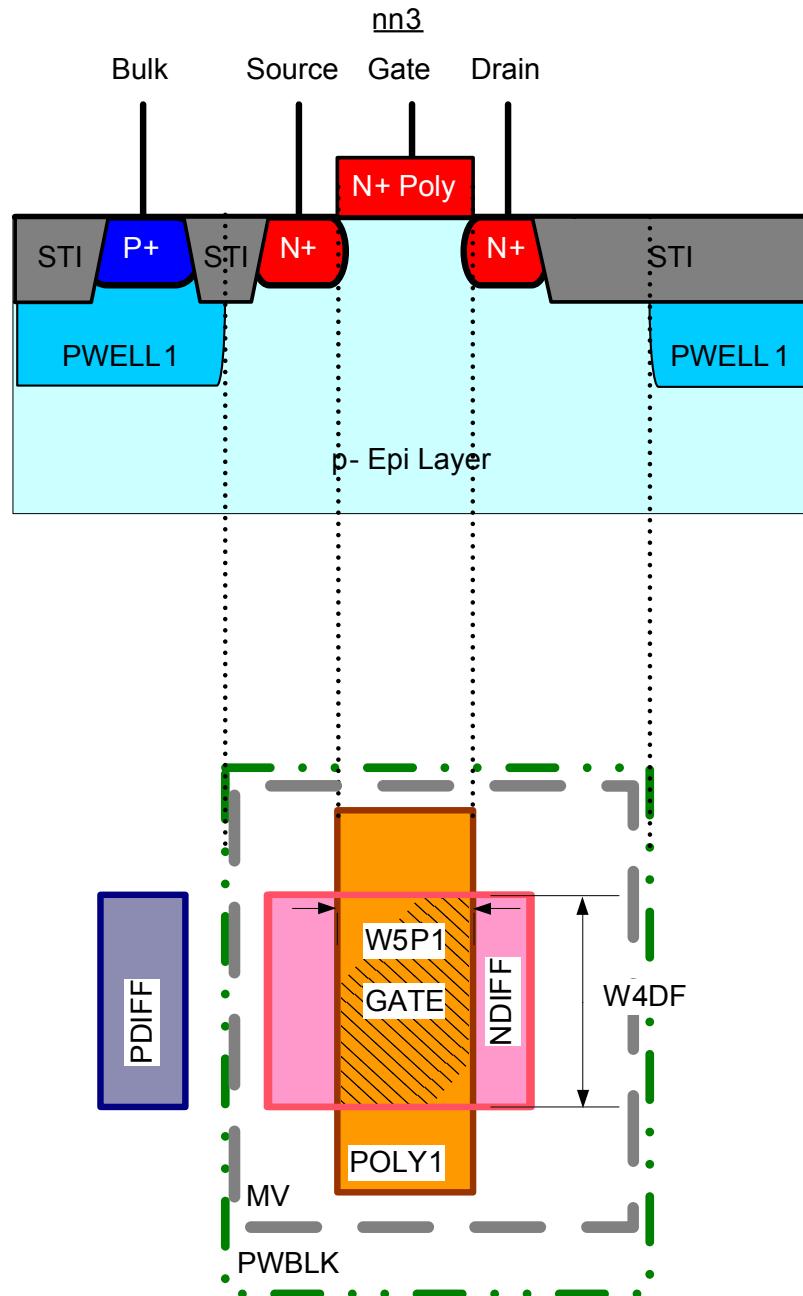


Figure 3.24 nn3

3. Layer and Device rules → 3.1 LPMOS main module → 3.1.2 Device rules → ne3, pe3

ne3, pe3

Name	Description	Value	Unit
W3DF	Minimum GATE width	0.22	μm
	Note: The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) having smaller GATE width than 0.22μm.		
W6P1	Minimum GATE length	0.35	μm
W7P1	Minimum GATE length	0.3	μm

Note: MV is necessary for ne3 and pe3.

Note: For more extensive LVS, it is recommended to use the related 5 or 6 terminal device.

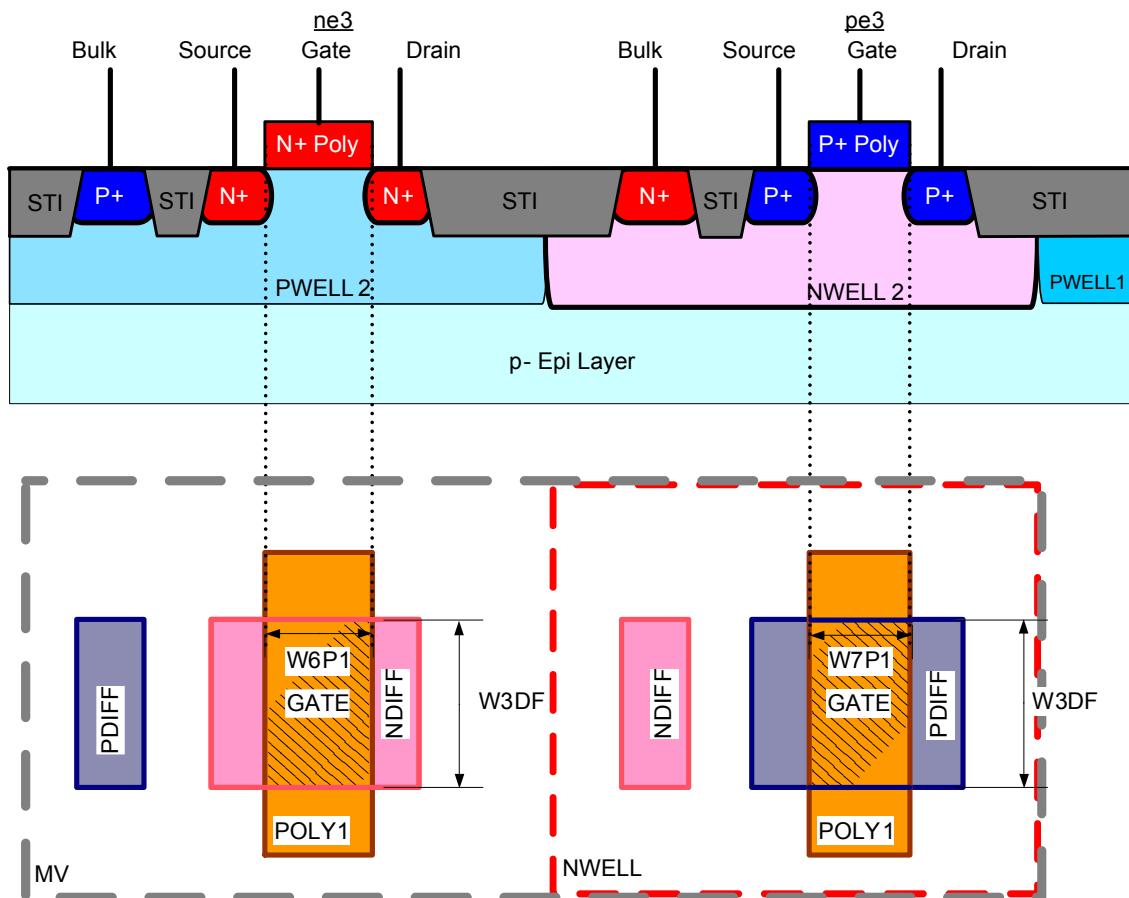


Figure 3.25 ne3, pe3

3. Layer and Device rules → 3.1 LPMOS main module → 3.1.2 Device rules → pe3_5

pe3_5

Name	Description	Value	Unit
W3DF	Minimum GATE width	0.22	μm
	Note: The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) having smaller GATE width than 0.22μm.		
W7P1	Minimum GATE length	0.3	μm

Note: pe3_5 device must be labeled "5T" using POLY1 (VERIFICATION) layer over the GATE.

Note: MV is necessary for pe3_5.

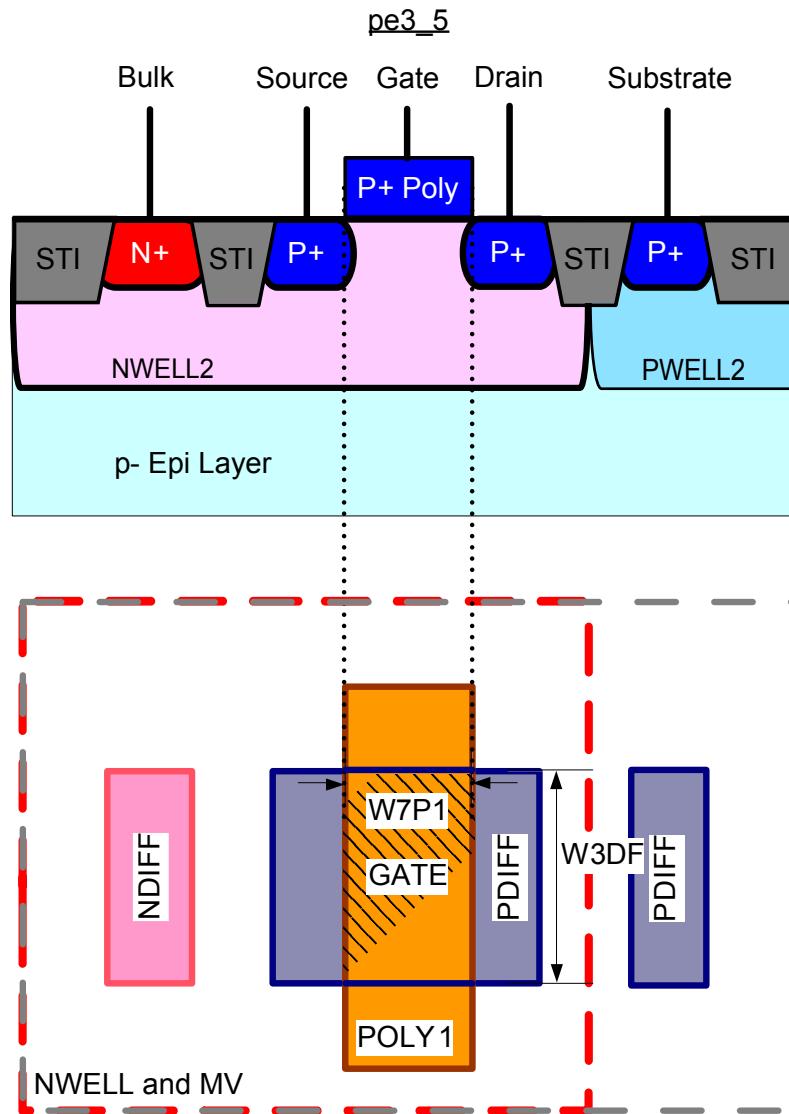


Figure 3.26 pe3_5

3. Layer and Device rules → 3.1 LPMOS main module→ 3.1.2 Device rules→ qpva, qpvb, qpvc

qpva, qpvb, qpvc

The devices qpva, qpvb and qpvc use PDIFF as emitter, NWELL as base and PWELL as collector. The layouts of qpva, qpvb and qpvc are predefined. They must not be changed.

qpva

NDIFF base surrounding PDIFF emitter contact, emitter area: $2 \times 2 \mu\text{m}^2$

qpvb

NDIFF base surrounding PDIFF emitter contact, emitter area: $5 \times 5 \mu\text{m}^2$

qpvc

NDIFF base surrounding PDIFF emitter contact, emitter area: $10 \times 10 \mu\text{m}^2$

Note: qpva, qpvb and qpvc must not be drawn inside DNWELL, DNWELLMV, HVNWELL, HVPWELL, DEPL or HVGOX.

3. Layer and Device rules → 3.1 LPMOS main module → 3.1.2 Device rules → qpva, qpvb, qpvc

qpva, qpvb, qpvc

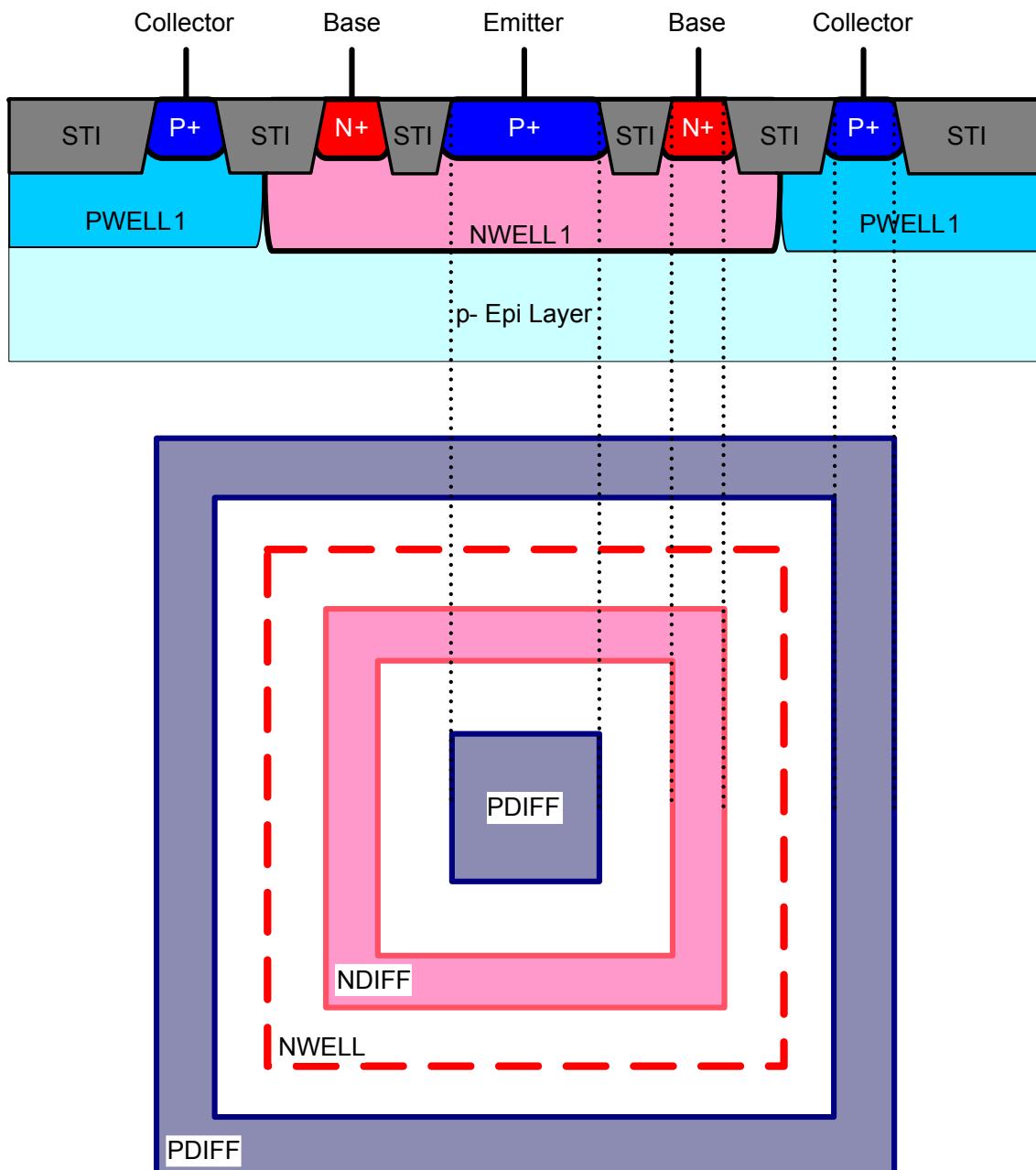


Figure 3.27 qpva, qpvb, qpvc

3. Layer and Device rules → 3.1 LPMOS main module→ 3.1.2 Device rules→ qpva3, qpvb3, qpvc3

qpva3, qpvb3, qpvc3

This section describes the vertical PNP transistors qpva3, qpvb3 and qpvc3.

These transistors use PDIFF as emitter, NWELL2 as base and PWELL2 as collector. Their layouts are predefined. They must not be changed.

qpva3

NDIFF base surrounding PDIFF emitter contact, emitter area: $2 \times 2 \mu\text{m}^2$

qpvb3

NDIFF base surrounding PDIFF emitter contact, emitter area: $5 \times 5 \mu\text{m}^2$

qpvc3

NDIFF base surrounding PDIFF emitter contact, emitter area: $10 \times 10 \mu\text{m}^2$

Note: MV is necessary for qpva3, qpvb3 and qpvc3.

Note: qpva3, qpvb3 and qpvc3 must not be drawn inside DNWELL, DNWELLMV, HVNWELL, HVPWELL, or DEPL.

3. Layer and Device rules → 3.1 LPMOS main module → 3.1.2 Device rules → qpva3, qpvb3, qpvc3

qpva3, qpvb3, qpvc3

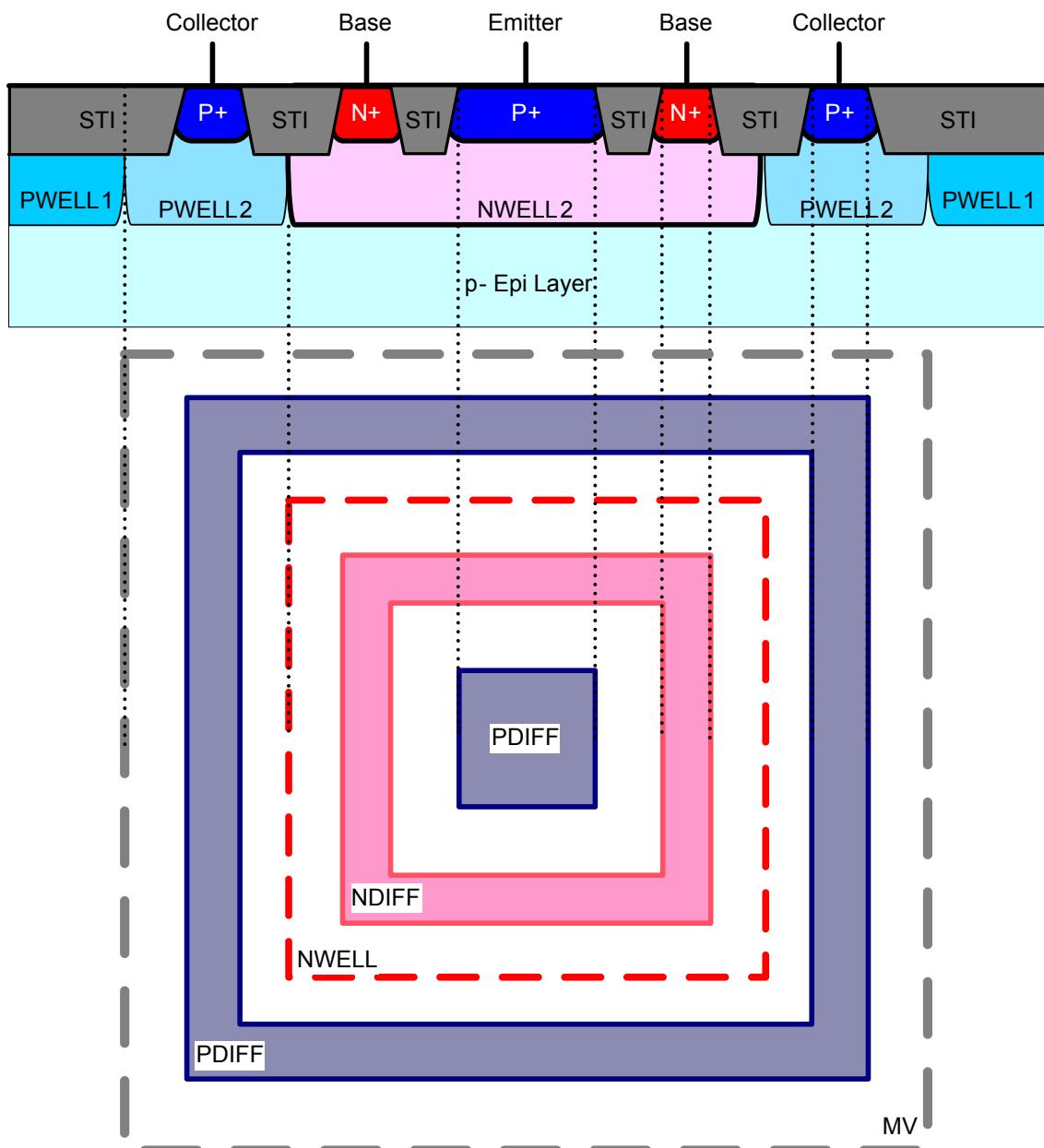


Figure 3.28 qpva3, qpvb3, qpvc3

3. Layer and Device rules → 3.1 LPMOS main module → 3.1.2 Device rules → rdn, rdp, rdn3, rdp3

rdn, rdp, rdn3, rdp3

Name	Description	Value	Unit
B1DN	rdn/rdn3 inside ISOPW, DEPL, SCI, HVPWELL, PDD or PDF is not allowed Note: rdn, rdn3 are only allowed in ISOPW in case on Gate in IO blocks and ESD.	-	-
B2GH	HVGOX overlap of rdn or rdp is not allowed	-	-
W5DF	Minimum rdn/rdn3, rdp/rdp3 width	0.42	μm

Note: Recommended minimum number of squares is $L/W \geq 5$.

Note: rdn, rdn3 resistor definition: SBLK and PTYPE_WELL and NDIFF (except GATE, PHODIO).

Note: rdp, rdp3 resistor definition: SBLK and NWELL and PDIFF (except GATE, PHODIO).

Note: MV is necessary for rdn3 and rdp3.

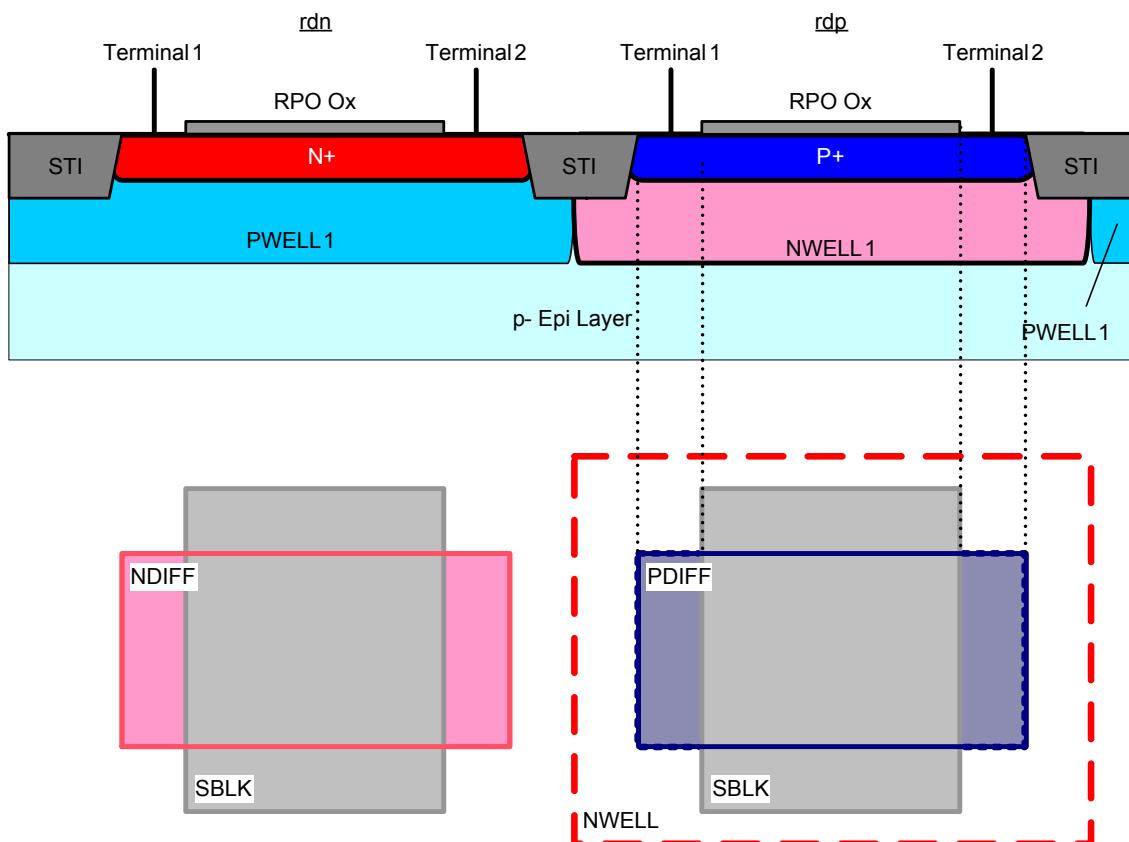


Figure 3.29 rdn, rdp, rdn3, rdp3

3. Layer and Device rules → 3.1 LPMOS main module→ 3.1.2 Device rules→ rnw, rnw3

rnw, rnw3

Name	Description	Value	Unit
B1NW	NW_VERIFY overlap of DIFF is not allowed	-	-
	Note: NW_VERIFY edge must touch rnw/rnw3 NDIFF-contact edge.		
B2NW	NW_VERIFY overlap of DNWELL or DNWELLMV is not allowed	-	-
B3GH	HVGDX overlap of rnw is not allowed	-	-
W2NW	Minimum rnw, rnw3 width	2.0	μm

Note: Recommended minimum number of squares is $L/W \geq 5$.

Note: It is recommended to place DIFF stripes close to resistor.

Note: rnw and rnw3 resistor definition: NWELL and NW_VERIFY.

Note: Recommended maximum width is 10μm.

Note: MV is necessary for rnw3.

3. Layer and Device rules → 3.1 LPMOS main module → 3.1.2 Device rules → rnw, rnw3

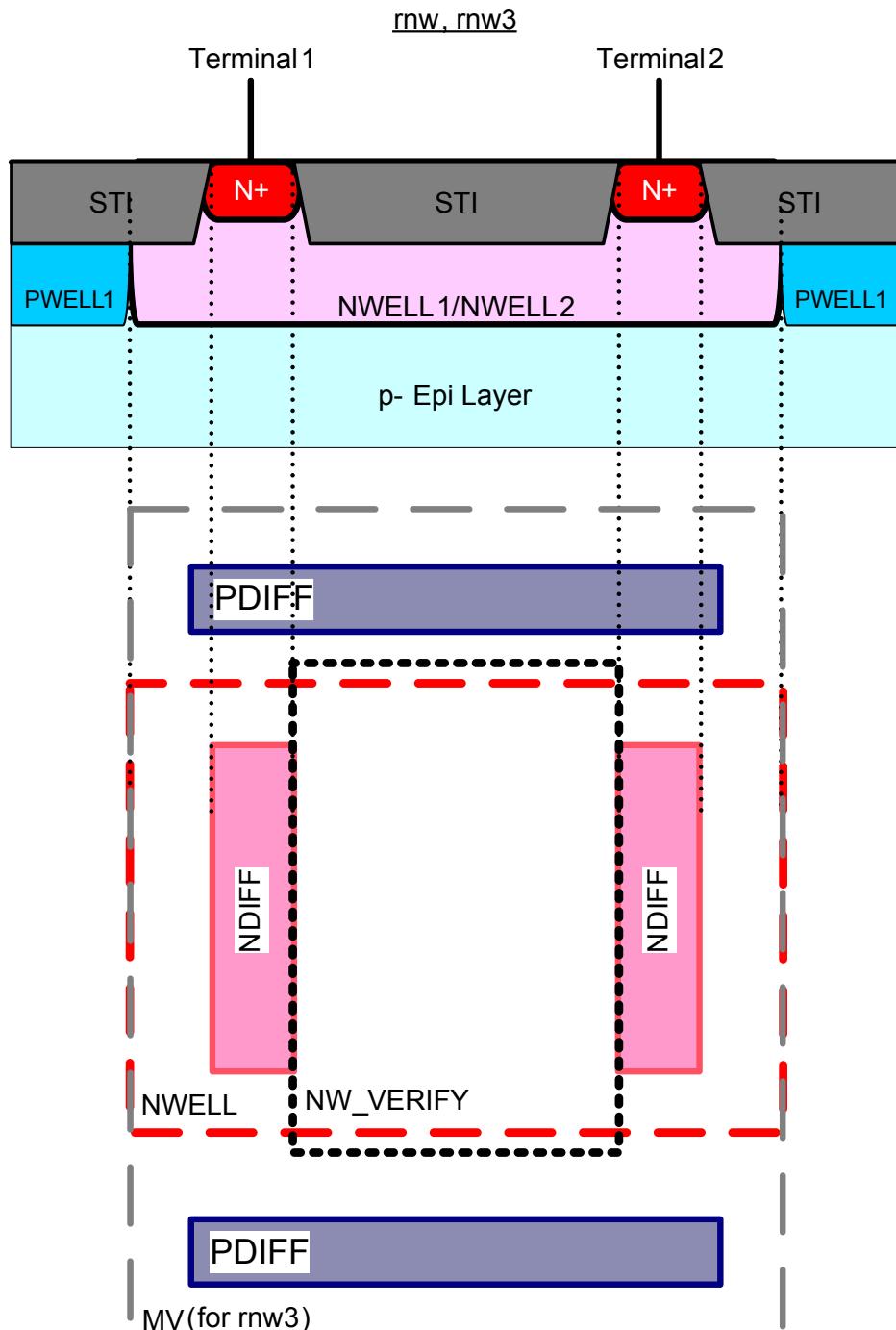


Figure 3.30 rnw, rnw3

3. Layer and Device rules → 3.1 LPMOS main module → 3.1.2 Device rules → rnp1, rnp1_3, rpp1, ...

rnp1, rnp1_3, rpp1, rpp1_3, rpp1s, rpp1s_3

Name	Description	Value	Unit
B10P1	rpp1s_3 overlap rnw/rnw3/rdnwmv is not allowed	-	-
B2CT	CONT is not allowed within rpp1s#	-	-
B6P1	rnp1_3 overlap rnw/rnw3/rdnwmv is not allowed	-	-
B8P1	rpp1_3 overlap rnw/rnw3/rdnwmv is not allowed	-	-
B5P1	rnp1_3 crossing NTYPE_WELL or PTYPE_WELL or SUBCUT edge is not allowed	-	-
B7P1	rpp1_3 crossing NTYPE_WELL or PTYPE_WELL or SUBCUT edge is not allowed	-	-
B9P1	rpp1s_3 crossing NTYPE_WELL or PTYPE_WELL or SUBCUT edge is not allowed	-	-
W3P1	Minimum rnp1#, rpp1# width	0.42	μm
S1INP1	Minimum NIMP spacing to rpp1# or rpp1s#	0.26	μm
S1IPP1	Minimum PIMP spacing to rnp1#	0.26	μm
E1INP1	Minimum NIMP extension beyond rnp1#	0.18	μm
E1IPP1	Minimum PIMP extension beyond rpp1# or rpp1s#	0.18	μm

Note: CONT array for POLY1 resistor should be a single column.

Note: Recommended minimum number of squares is L/W ≥ 5.

Note: rnp1# resistor definition: POLY1 and SBLK and NIMP. (except GATE oversized by 0.22μm)

Note: Do not use dog-bone at the end of POLY1 resistor for CONT pickup.

Note: rnp1_3 device must be labeled "rnp1_3" using POLY1 (VERIFICATION) layer.

Note: rpp1# resistor definition: POLY1 and SBLK and PIMP. (except GATE oversized by 0.22μm)

Note: rpp1_3 device must be labeled "rpp1_3" using POLY1 (VERIFICATION) layer.

Note: rpp1s# resistor definition: POLY1 and POLY1_VERIFY and PIMP. (except rpp1 oversized by 0.22 μm and not GATE)

Note: rpp1s_3 device must be labeled "rpp1s_3" using POLY1 (VERIFICATION) layer.

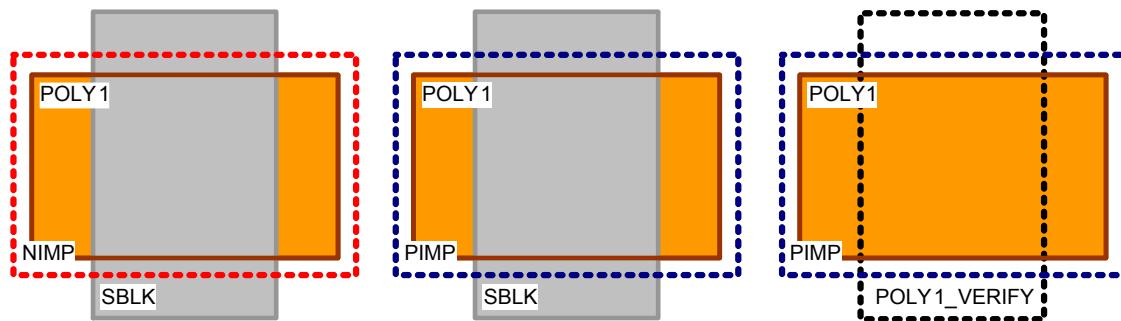
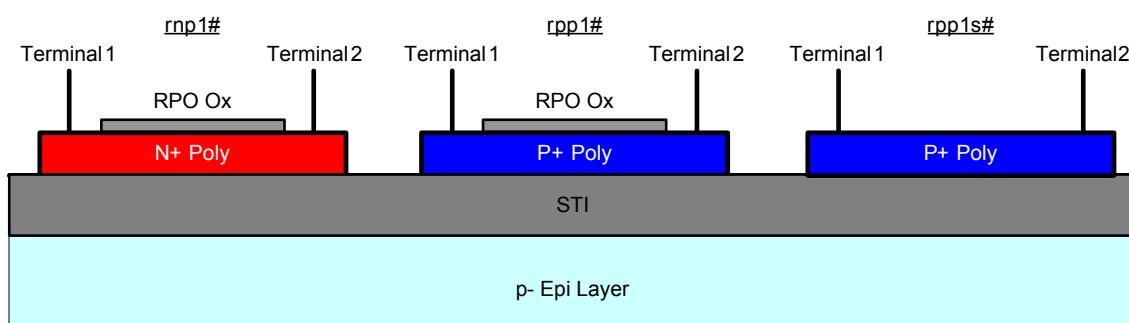


Figure 3.31 rnp1#, rpp1#, rpp1s#

3. Layer and Device rules → 3.1 LPMOS main module→ 3.1.2 Device rules→ rnp1h, rnp1h_3

rnp1h, rnp1h_3

Name	Description	Value	Unit
B11HR	rnp1h_3 overlap rnw/rnw3/rdnwmv is not allowed	-	-
B2HR	NIMP overlap of rnp1h# (resistor body) is not allowed	-	-
B5HR	rnp1h# terminal without NIMP is not allowed	-	-
B7HR	MET1 overlap of rnp1h# (resistor body) is not allowed	-	-
B10HR	rnp1h_3 crossing NTYPE_WELL or PTYPE_WELL or SUBCUT edge is not allowed	-	-
W2HR	Minimum rnp1h# width	0.42	μm
W3HR	Minimum rnp1h# length	5.0	μm
S2INP1	Minimum NIMP (in SBLK) spacing to rnp1h#	0.18	μm
E2INP1	Minimum NIMP extension beyond POLY1	0.18	μm

Note: CONT array for POLY1 resistor should be a single column.

Note: Recommended minimum number of squares is $L/W \geq 5$.

Note: rnp1h# resistor definition: POLY1 and SBLK and HRES.

Note: Do not use dog-bone at the end of POLY1 resistor for CONT pickup.

Note: For good matching or precise resistance value it is strongly recommended to use larger HRES extension beyond POLY1 in resistor width direction ($\geq 0.5\mu m$).

Note: rnp1h_3 device must be labeled “rnp1h_3” using POLY1 (VERIFICATION) layer.

3. Layer and Device rules → 3.1 LPMOS main module → 3.1.2 Device rules → rnp1h, rnp1h_3

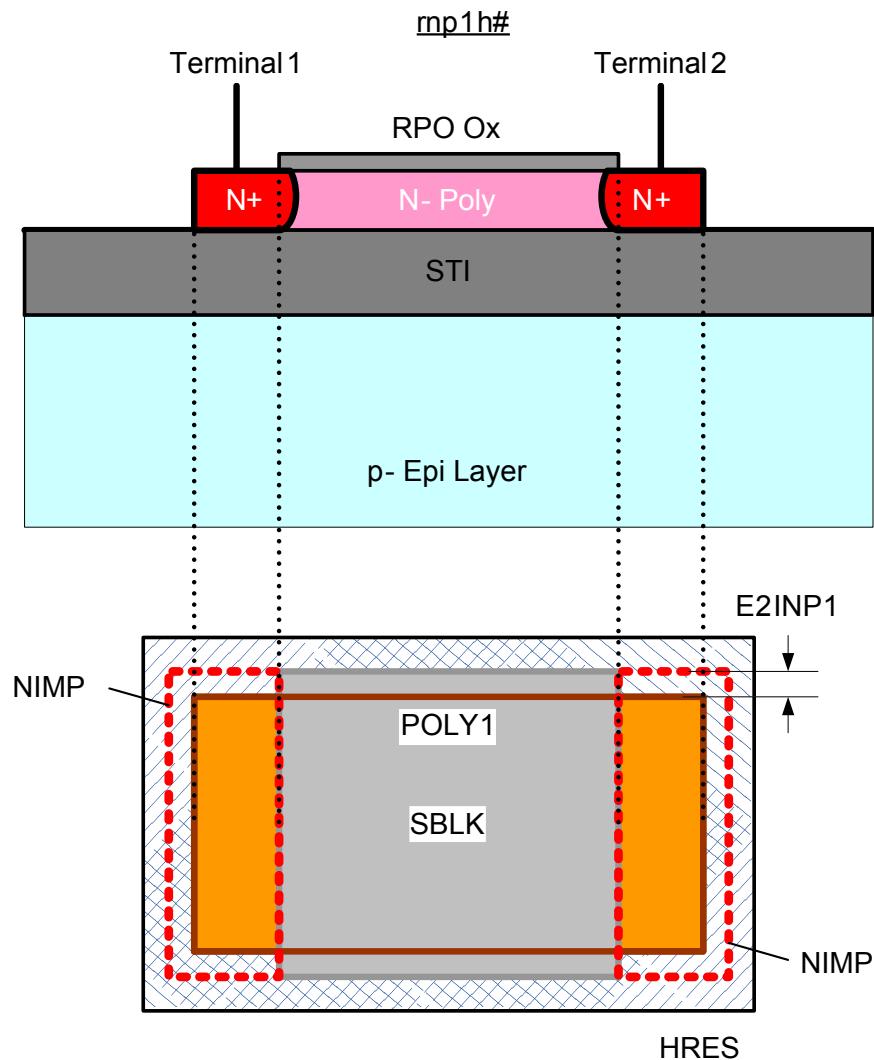


Figure 3.32 rnp1h#

3. Layer and Device rules → 3.1 LPMOS main module→ 3.1.2 Device rules→ rm1, rm2

rm1, rm2

Name	Description	Value	Unit
B2M1	CONT or VIA1 is not allowed within rm1	-	-
B2M2	VIA1 is not allowed within rm2	-	-
B4M2	VIA2 is not allowed within rm2	-	-
Note: Valid if MET3 module is selected.			

Note: rm1 resistor definition: MET1 and M1VERIFY.

Note: rm2 resistor definition: MET2 and M2VERIFY.



Figure 3.33 rm1, rm2

3. Layer and Device rules → 3.1 LPMOS main module → 3.1.2 Device rules → mosvc

mosvc

Name	Description	Value	Unit
B4GA	Only rectangular GATE is allowed	-	-
W38GA	Minimum GATE length	2.0	μm
W39GA	Minimum GATE width	2.0	μm

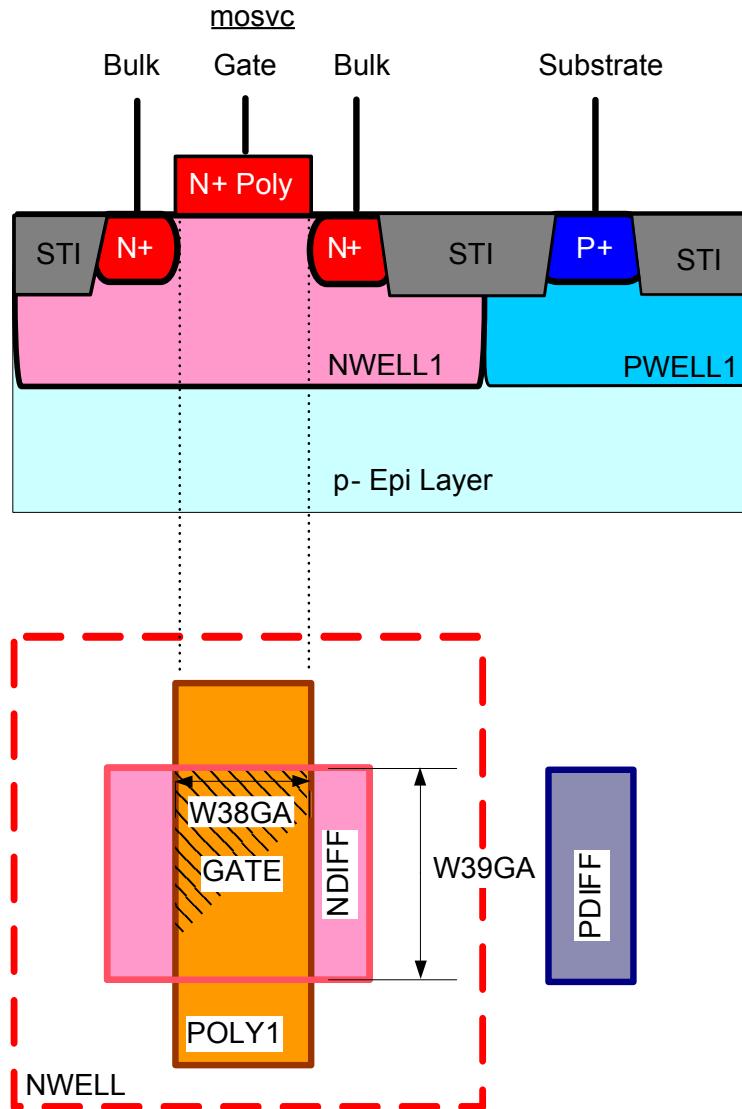


Figure 3.34 mosvc

3. Layer and Device rules → 3.1 LPMOS main module → 3.1.2 Device rules → mosvc3

mosvc3

Name	Description	Value	Unit
B4GA	Only rectangular GATE is allowed	-	-
W38GA	Minimum GATE length	2.0	μm
W39GA	Minimum GATE width	2.0	μm

Note: MV is necessary for mosvc3.

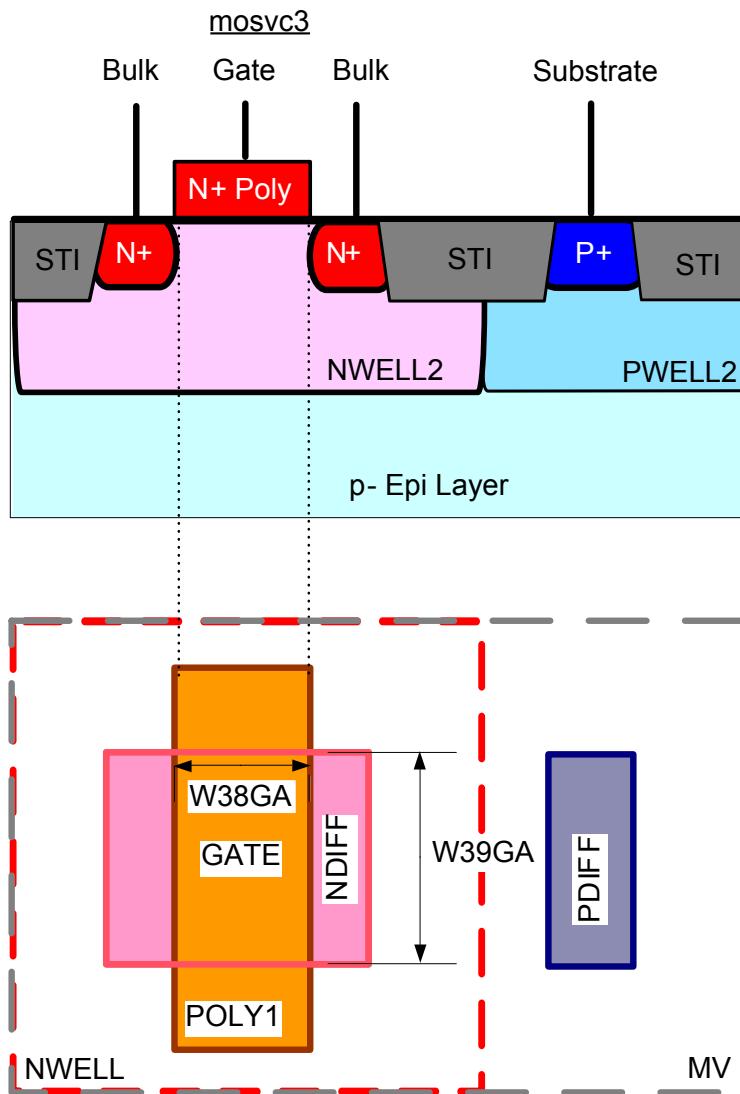


Figure 3.35 mosvc3

csf2p

The layout of the device csf2p is fixed and must not be changed. A single cell instance has an area of 4.48 μm × 10.80 μm.

Note: CAPDEF is necessary for csf2p.

Note: Higher values may be achieved by the formation of arrays.

3. Layer and Device rules → 3.1 LPMOS main module → 3.1.2 Device rules → dn, dp, dnw

dn, dp, dnw

Note: The drawing is only for NWELL1 and PWELL1 respectively.

Note: The layer DIODEF must enclose the pn junction, crossing the pn junction is not allowed.

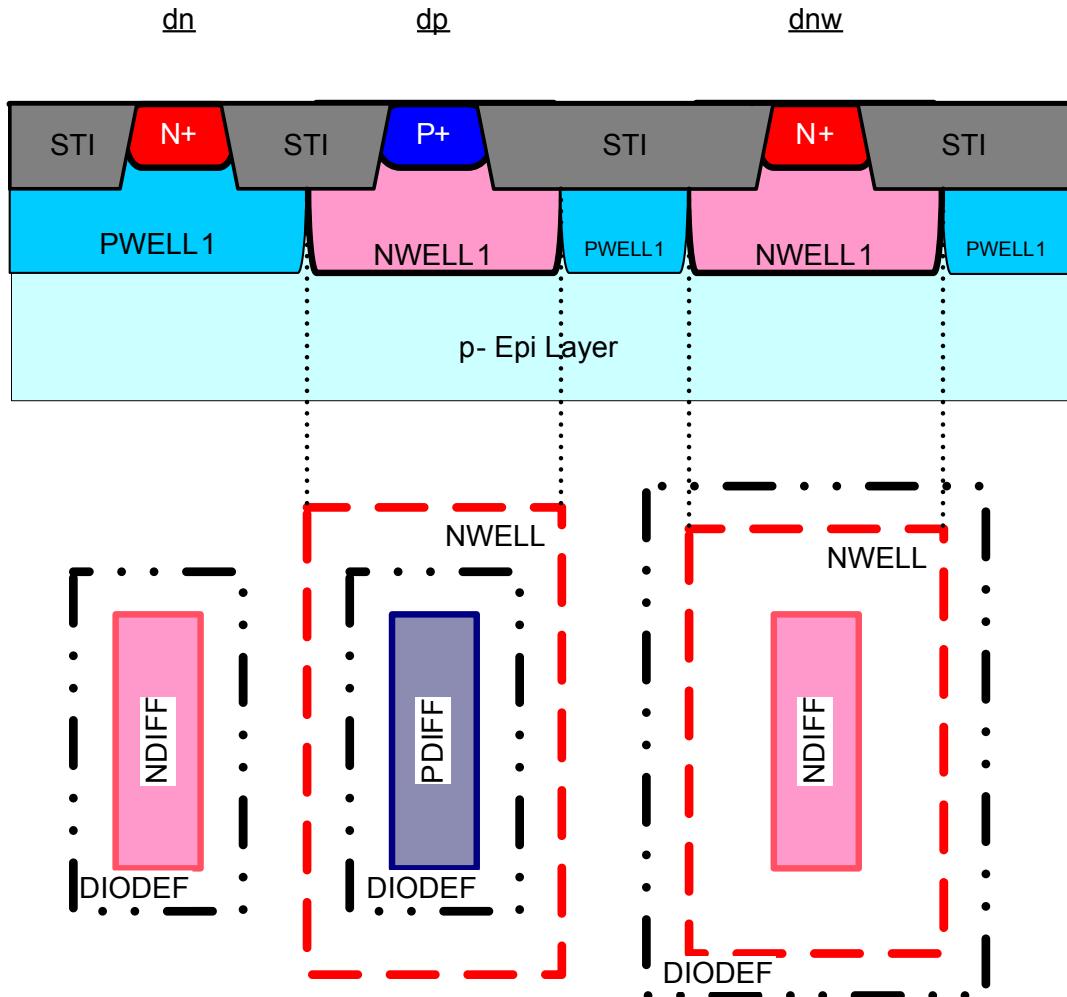


Figure 3.36 dn, dp, dnw

3. Layer and Device rules → 3.1 LPMOS main module → 3.1.2 Device rules → dn3, dp3, dnw3

dn3, dp3, dnw3

Note: MV is necessary for dn3, dp3 and dnw3.

Note: The layer DIODEF must enclose the pn junction, crossing the pn junction is not allowed.

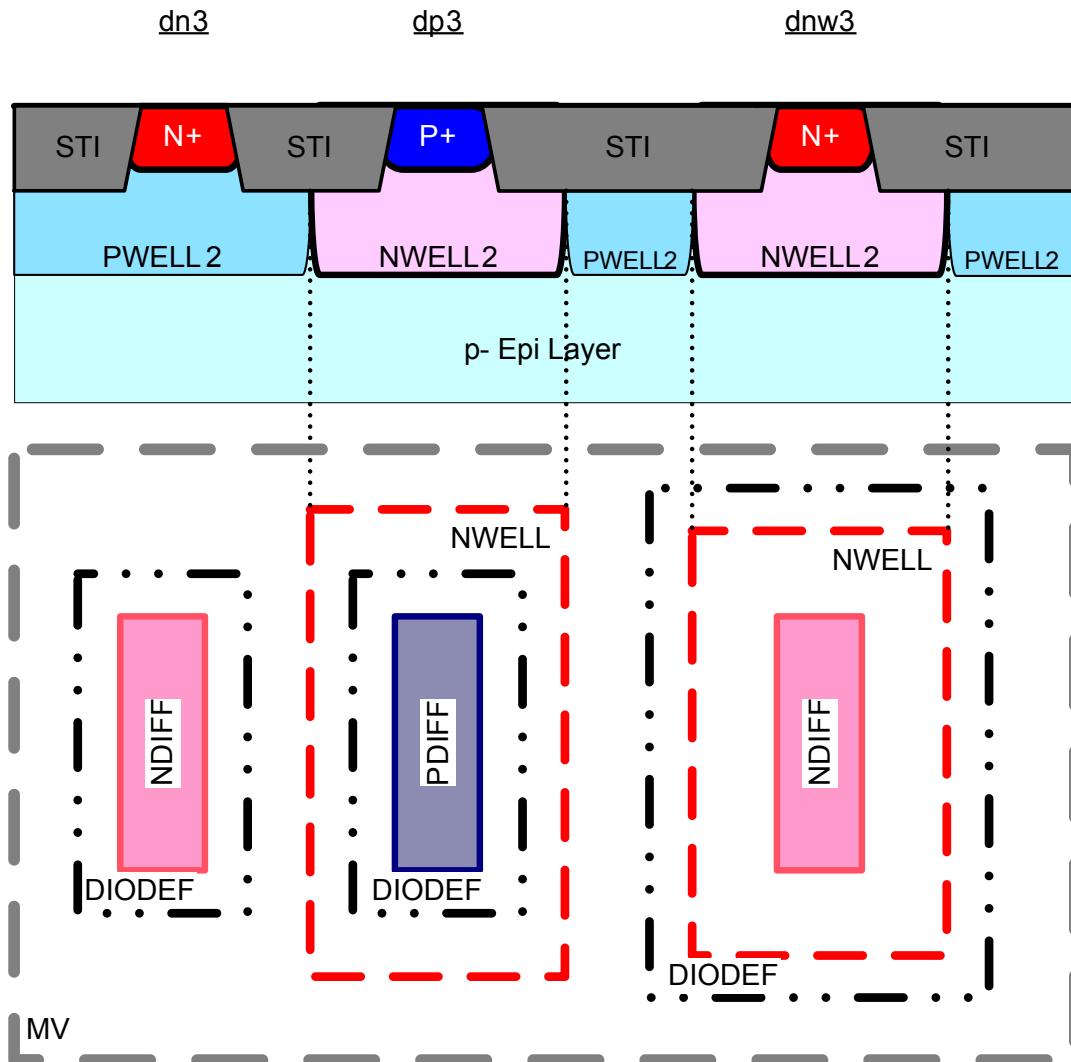


Figure 3.37 dn3, dp3, dnw3

3. Layer and Device rules → 3.1 LPMOS main module → 3.1.2 Device rules → dnn3

dnn3

Note: MV is necessary for dnn3.

Note: The layer DIODEF must enclose the pn junction, crossing the pn junction is not allowed.

dnn3

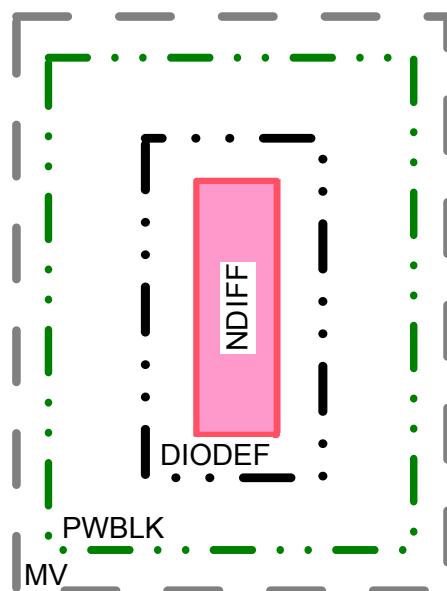
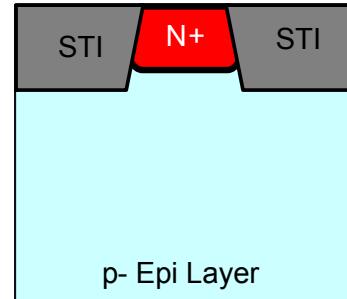


Figure 3.38 dnn3

3. Layer and Device rules → 3.1 LPMOS main module→ 3.1.2 Device rules→ dpol

dpol

The layout of dpol is predefined and scalable concerning device width only. All other dimensions must not be changed.

Name	Description	Value	Unit
B11P1	Only rectangular dpol body is allowed	-	-
B12P1	dpol body (oversized by 1.5 µm) overlap of DIFF is not allowed	-	-
B13P1	dpol body (oversized by 1.0 µm) overlap of MET1, MET2, MET3, MET4, MET5, METTP or METTPL is not allowed	-	-
B14P1	dpol body (oversized by 1.0 µm) without BLKALL is not allowed	-	-
W12P1	Minimum dpol width	1.0	µm
W13P1	Maximum dpol width	200.0	µm
W14P1	Fixed dpol body length	0.85	µm
E3IPP1	Minimum PIMP extension beyond POLY1	0.18	µm
E4INP1	Minimum NIMP extension beyond POLY1	0.18	µm
O1INSB	Fixed SBLK overlap of (POLY and NIMP)	1.0	µm
O1IPSB	Fixed SBLK overlap of (POLY1 and PIMP)	1.0	µm

Note: dpol body is defined as (POLY and SBLK) and not (NIMP or PIMP).

Note: The layer DIODEF must enclose the pn junction, crossing the pn junction is not allowed.

3. Layer and Device rules → 3.1 LPMOS main module → 3.1.2 Device rules → dpol

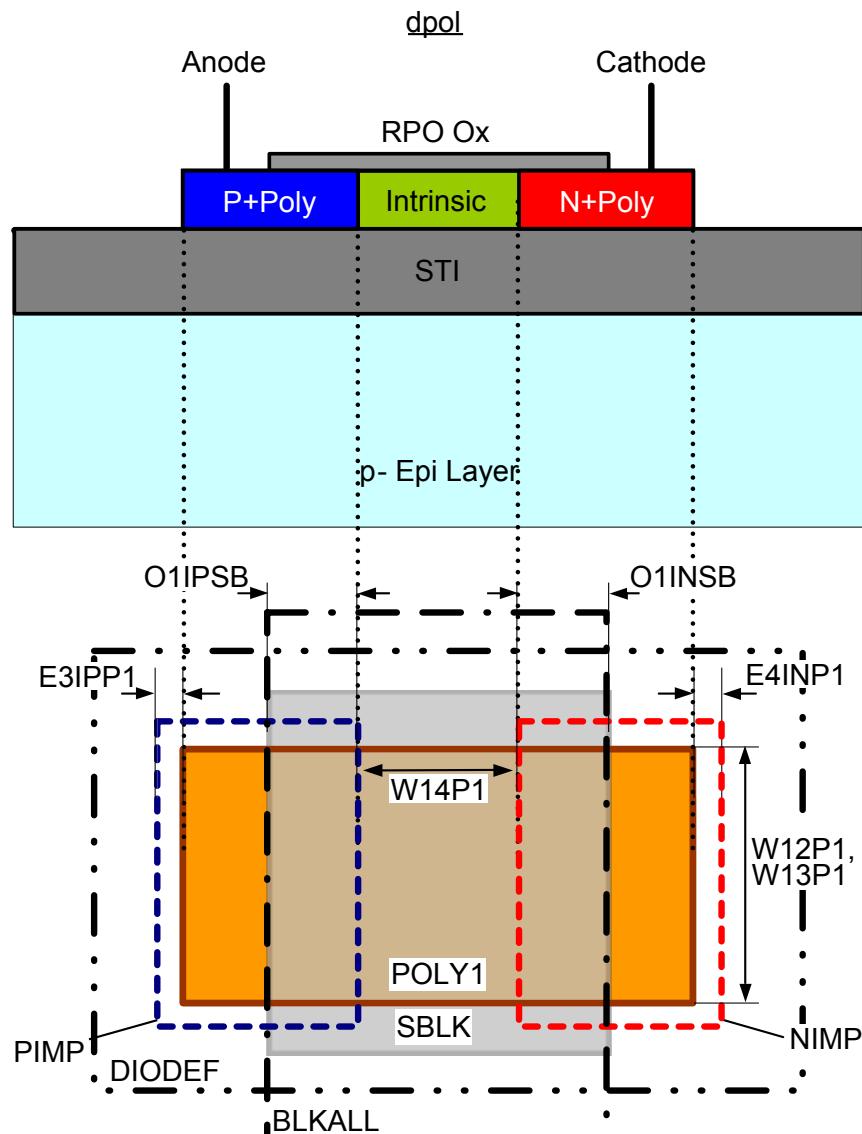


Figure 3.39 dpol

3. Layer and Device rules → 3.1 LPMOS main module→ 3.1.2 Device rules→ pfuse

pfuse

Name	Description	Value	Unit
B2P1	pfuse overlap of MET1, MET2, MET3, MET4, MET5, METTP or METTPL is not allowed	-	-
B3P1	pfuse overlap of SBLK or DIFF is not allowed	-	-
B4P1	pfuse without NIMP and BLKALL is not allowed	-	-
S1DFP1	Minimum DIFF spacing to pfuse Note: Valid in pfuse width direction only.	2.0	μm
S1M1P1	Minimum MET1 spacing to pfuse Note: Valid in pfuse width direction only.	0.8	μm
S1M2P1	Minimum MET2 spacing to pfuse Note: Valid in pfuse width direction only.	0.8	μm
S1M3P1	Minimum MET3 spacing to pfuse Note: Valid in pfuse width direction only.	1.7	μm
S1M4P1	Minimum MET4 spacing to pfuse Note: Valid in pfuse width direction only.	1.7	μm
S1M5P1	Minimum MET5 spacing to pfuse Note: Valid in pfuse width direction only.	1.7	μm
S1MLP1	Minimum METTPL spacing to pfuse Note: Valid in pfuse width direction only.	1.7	μm
S1MTP1	Minimum METTP spacing to pfuse Note: Valid in pfuse width direction only.	1.7	μm
S2P1	Minimum POLY1 spacing to pfuse Note: Valid in pfuse width direction only.	2.0	μm
S2SBP1	Minimum SBLK spacing to pfuse Note: Valid in pfuse width direction only.	2.0	μm
E1BAP1	Minimum BLKALL enclosure of pfuse	1.7	μm
E1NWP1	Fixed NWELL enclosure of pfuse Note: NWELL is an electrically floating area without any connections.	1.7	μm
E3INP1	Minimum NIMP enclosure of POLY1	0.3	μm

Note: pfuse device must be labeled "PFUSE" using POLY1 (VERIFICATION) layer.

Note: pfuse device must have POLY1 (VERIFICATION) layer.

Note: The layout of pfuse is predefined. It must not be changed. The other rules support the fixed dimensions of the layout or describe the relation to adjacent structures.

3. Layer and Device rules → 3.1 LPMOS main module → 3.1.2 Device rules → pfuse

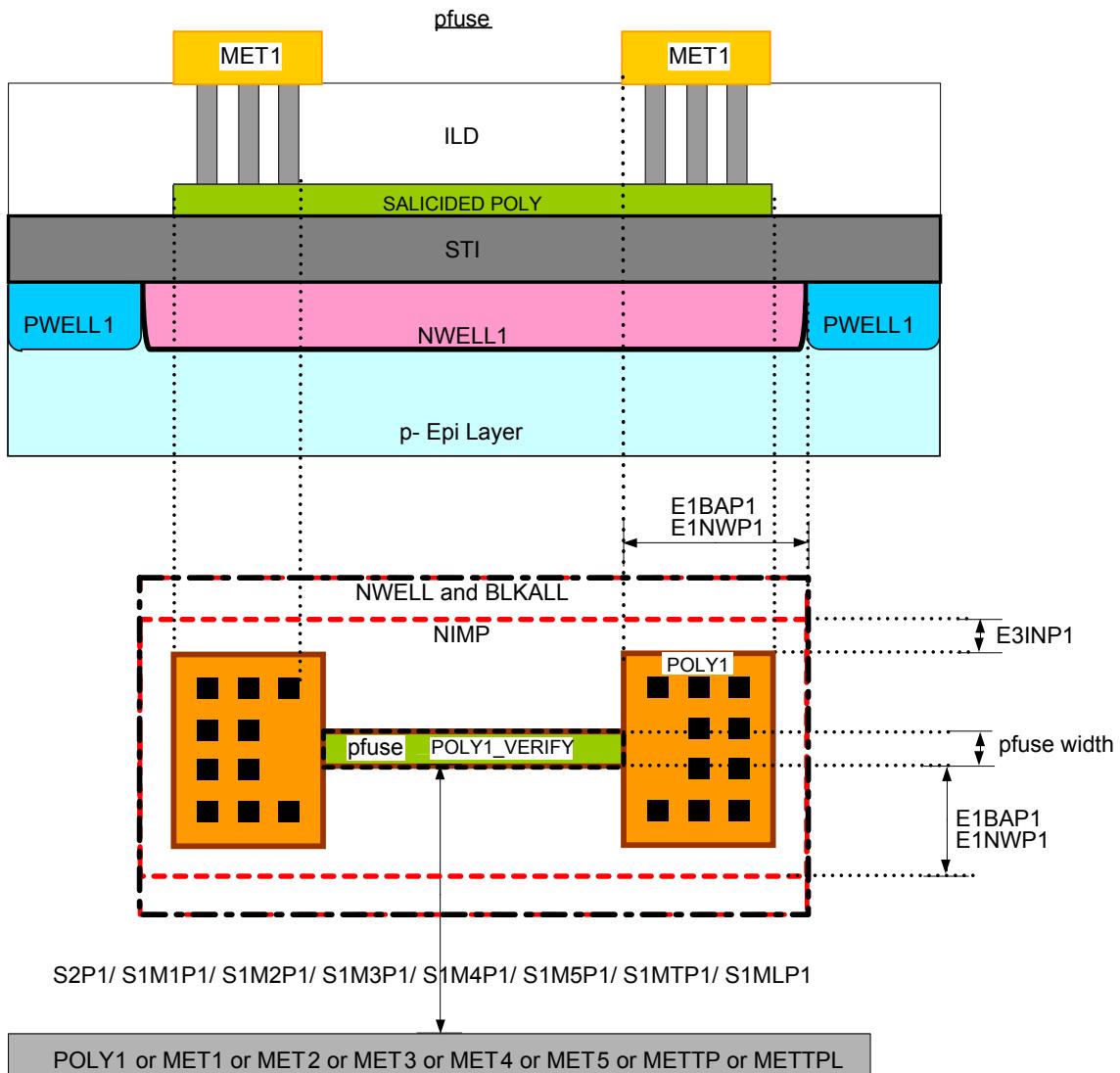


Figure 3.40 pfuse

3. Layer and Device rules → 3.2 MET3 module

3.2 MET3 module

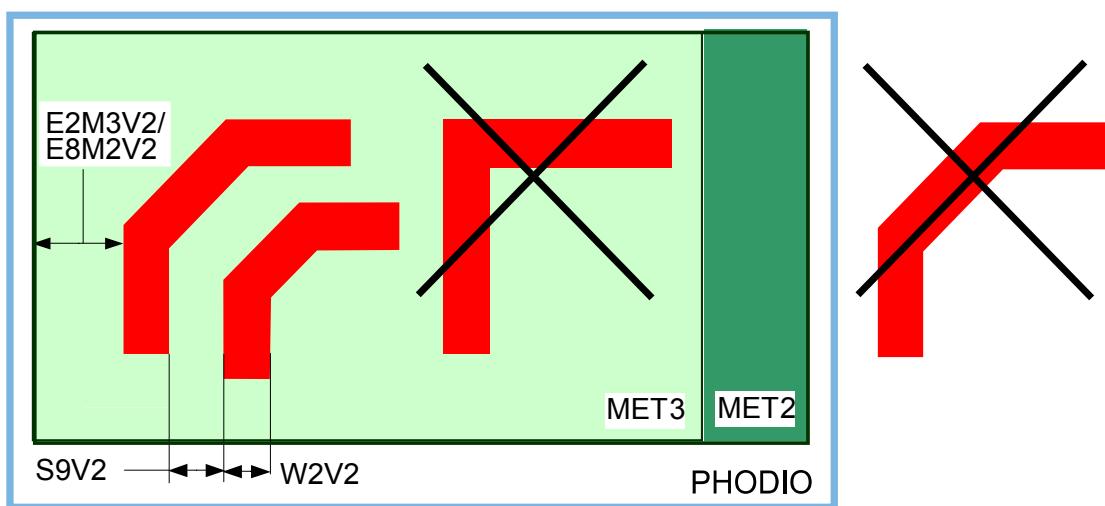
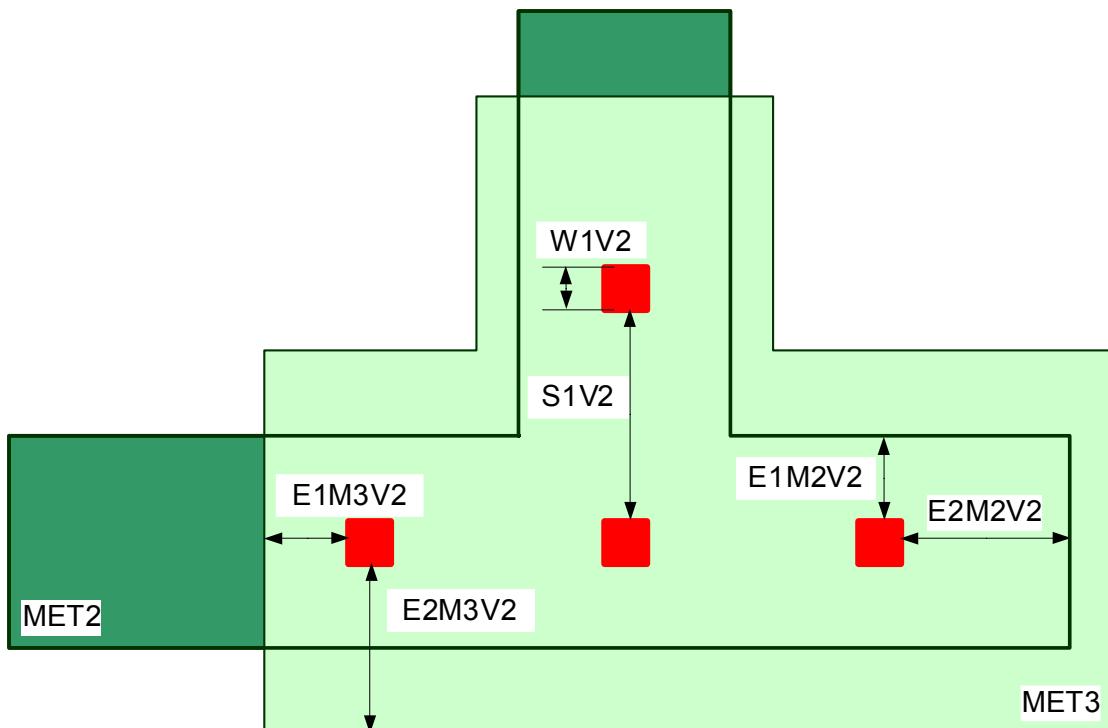
3.2.1 Layer rules

VIA2

Name	Description	Value	Unit
B1V2	VIA2 must be covered by MET2 and MET3	-	-
B2V2	VIA2 stripes are only allowed to bend at 135 degrees	-	-
W2V2	Fixed VIA2 stripe width Note: Stripes are only allowed for use with photodiodes or other optical purposes.	0.26	µm
W1V2	Fixed VIA2 size (except dphoc#, dphod#, PHODIO, OPTOVIA2)	0.26 x 0.26	µm x µm
S1V2	Minimum VIA2 spacing	0.26	µm
S9V2	Minimum VIA2 stripe to VIA2 spacing	1.0	µm
E1M2V2	Minimum MET2 enclosure of VIA2	0.01	µm
E1M3V2	Minimum MET3 enclosure of VIA2	0.01	µm
E2M2V2	Minimum MET2 enclosure of VIA2 (in one direction of VIA2 corner)	0.06	µm
E2M3V2	Minimum MET3 enclosure of VIA2 (in one direction of VIA2 corner)	0.06	µm
E3M3V2	Minimum MET3 enclosure of VIA2 stripe	0.1	µm
E8M2V2	Minimum MET2 enclosure of VIA2 stripe	0.1	µm
R1V2	Maximum ratio of VIA2 area to connected GATE area	20.0	-
Q20V2	Check for the right usage of OPTOVIA2 Note: VIA2 stripes must only be used for light shielding purpose.	-	-

Note: Bond pads require interconnecting vias between the metal layers. See section "Bond Pad".

3. Layer and Device rules → 3.2 MET3 module → 3.2.1 Layer rules → VIA2

**Figure 3.41** VIA2

3. Layer and Device rules → 3.2 MET3 module → 3.2.1 Layer rules → MET3

MET3

Name	Description	Value	Unit
B1M3	All MET3 tracks > 35µm wide to be slotted (except Pads)	-	-
W1M3	Minimum MET3 width	0.28	µm
<i>W4M3</i>	Minimum MET3 width joining wide MET3 track (> 35 µm)	10.0	µm
	Note: No slot is allowed opposite the join. It is recommended to maintain this width for at least 1 µm from the main track prior to narrowing it.		
<i>W5M3</i>	Maximum MET3 region size	17.0 x 17.0	µm x µm
	Note: Not checked with standard DRC, option for check is available.		
	Note: MET3 regions are defined as MET3 shapes (single MET3 shapes or a bundle of MET3 shapes, with width > 2.0µm, inclusive of the spacing if the spacing is <= 1.0µm) without any other metal layer above. For further information and design guidelines, please refer to the application note about IMD popping on "my X-FAB".		
S1M3	Minimum MET3 spacing/notch	0.28	µm
<i>S4M3</i>	Minimum MET3 spacing (different net, tag_60v)	0.4	µm
	Note: Valid for spacing of all MET3 shapes with label tag_60v to all MET3 shapes having lower voltage classes. Refer to the design related guideline "Voltage class definitions".		
S2M3	Minimum MET3 spacing to WIDE_MET3	0.6	µm
A1M3	Minimum MET3 area	0.202	µm ²
<i>R1M3</i>	Minimum ratio of MET3 area to EXTENT area	30.0	%
	Note: Not checked with standard DRC, option for check is available.		
<i>R2M3</i>	Maximum ratio of MET3 area to EXTENT area	65.0	%
	Note: Not checked with standard DRC, option for check is available.		
R1M3P1	Maximum ratio of MET3 area to connected GATE area	400.0	-
	Note: Refer to section "Antenna Rule definitions" as well.		
<i>R2M3P1</i>	Maximum ratio of MET3 area to connected GATE area	400.0	-
	Note: Refer to section "Antenna Rule definitions" as well.		
Q1M3	Resistor terminal net without VLABEL	-	-
	Note: Resistor having VLABEL at one terminal only is not allowed. Refer to the design related guideline "Voltage class definitions".		

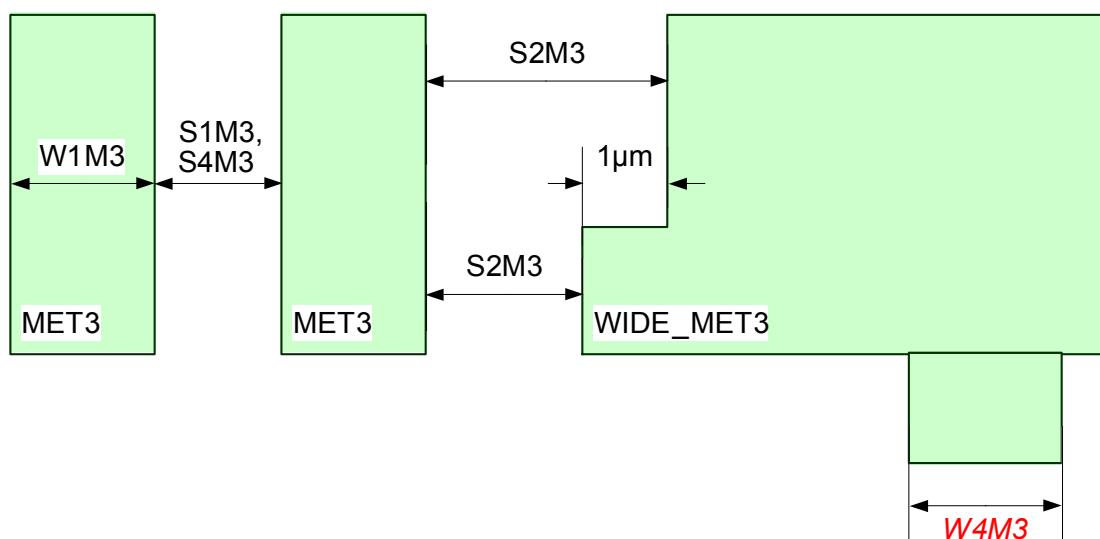


Figure 3.42 MET3

3. Layer and Device rules → 3.2 MET3 module→ 3.2.1 Layer rules→ M3SLOT

M3SLOT

Name	Description	Value	Unit
W2M3	Minimum M3SLOT width	0.6	μm
W3M3	Minimum M3SLOT length	20.0	μm
	Note: If this rule cannot be adhered to, it is suggested that the track in question is drawn as two narrow parallel tracks.		
S3M3	Minimum M3SLOT spacing/notch	10.0	μm
S1M3M2	Minimum M3SLOT spacing to M2SLOT	2.0	μm
	Note: M3SLOT is not allowed over M2SLOT.		
E1M3M3	Minimum MET3 enclosure of M3SLOT	10.0	μm
	Note: M3SLOT without MET3 is not allowed.		

Note: Insert M3SLOTS in direction of current flow.

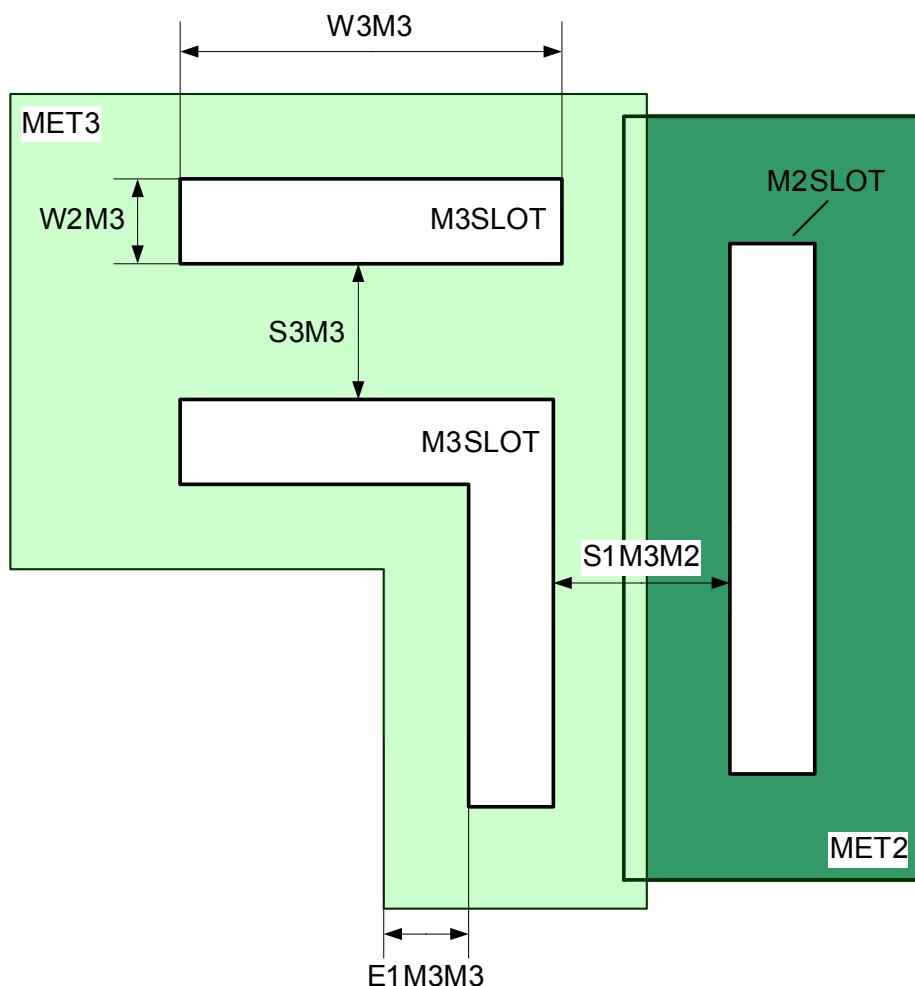


Figure 3.43 M3SLOT

3. Layer and Device rules → 3.2 MET3 module → 3.2.1 Layer rules → M3DUMMY

M3DUMMY

It is recommended to use X-FAB's dummy pattern generation option (DUMMY_FILL included in the DRC for preview) to create dummy pattern. If the generated dummy pattern is not sufficient to meet the minimum requirements for pattern density, customers can draw additional dummy pattern following the dummy design rules (DIFFDUMMY, P1DUMMY, M1DUMMY, M2DUMMY, M3DUMMY, M4DUMMY, M5DUMMY, MTPDUMMY and MTPLDUMMY). For further information, refer to the design related guideline "Dummy Pattern Generation".

Name	Description	Value	Unit
B1Y3	Only rectangular M3DUMMY is allowed	-	-
B2Y3	M3DUMMY overlap of MET3 is not allowed	-	-
B3Y3V2	M3DUMMY overlap of VIA2 is not allowed	-	-
B3Y3V3	M3DUMMY overlap of VIA3 is not allowed	-	-
B3Y3VT	M3DUMMY overlap of VIATP is not allowed Note: Only valid if module MET4 is not selected.	-	-
W1Y3	Minimum M3DUMMY width	2.0	μm
W2Y3	Maximum M3DUMMY edge length	20.0	μm
S1Y3	Minimum M3DUMMY spacing	2.0	μm
S10Y3	Minimum M3DUMMY spacing to LOCKED	4.0	μm
S11Y3	Minimum M3DUMMY spacing to LOCKED1	4.0	μm
S12Y3	Minimum M3DUMMY spacing to LOCKED2	4.0	μm
S13Y3	Minimum M3DUMMY spacing to LOCKED3	4.0	μm
S1Y3M3	Minimum M3DUMMY spacing to MET3	4.0	μm

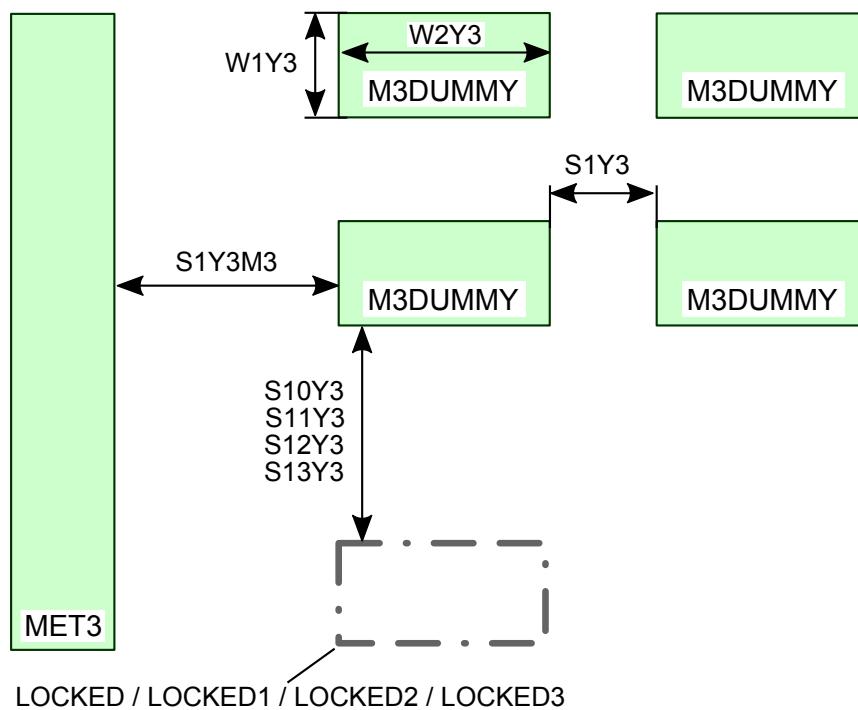


Figure 3.44 M3DUMMY

3. Layer and Device rules → 3.2 MET3 module → 3.2.2 Device rules → rm3

3.2.2 Device rules

rm3

Name	Description	Value	Unit
B2M3	VIA2 is not allowed within rm3	-	-
B3M3	VIATP is not allowed within rm3 Note: Valid if MET4 module is not selected.	-	-
B4M3	VIA3 is not allowed within rm3 Note: Valid if MET4 module is selected.	-	-

Note: rm3 resistor definition: MET3 and M3VERIFY.

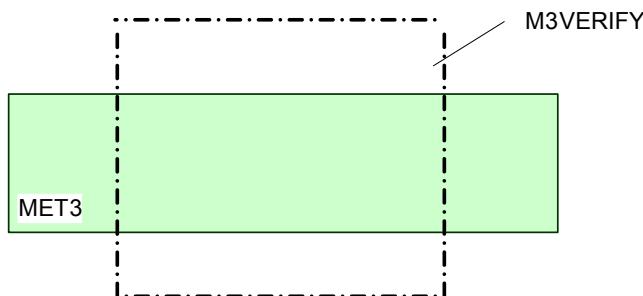


Figure 3.45 rm3

3. Layer and Device rules → 3.2 MET3 module → 3.2.2 Device rules → csandwt3

csandwt3

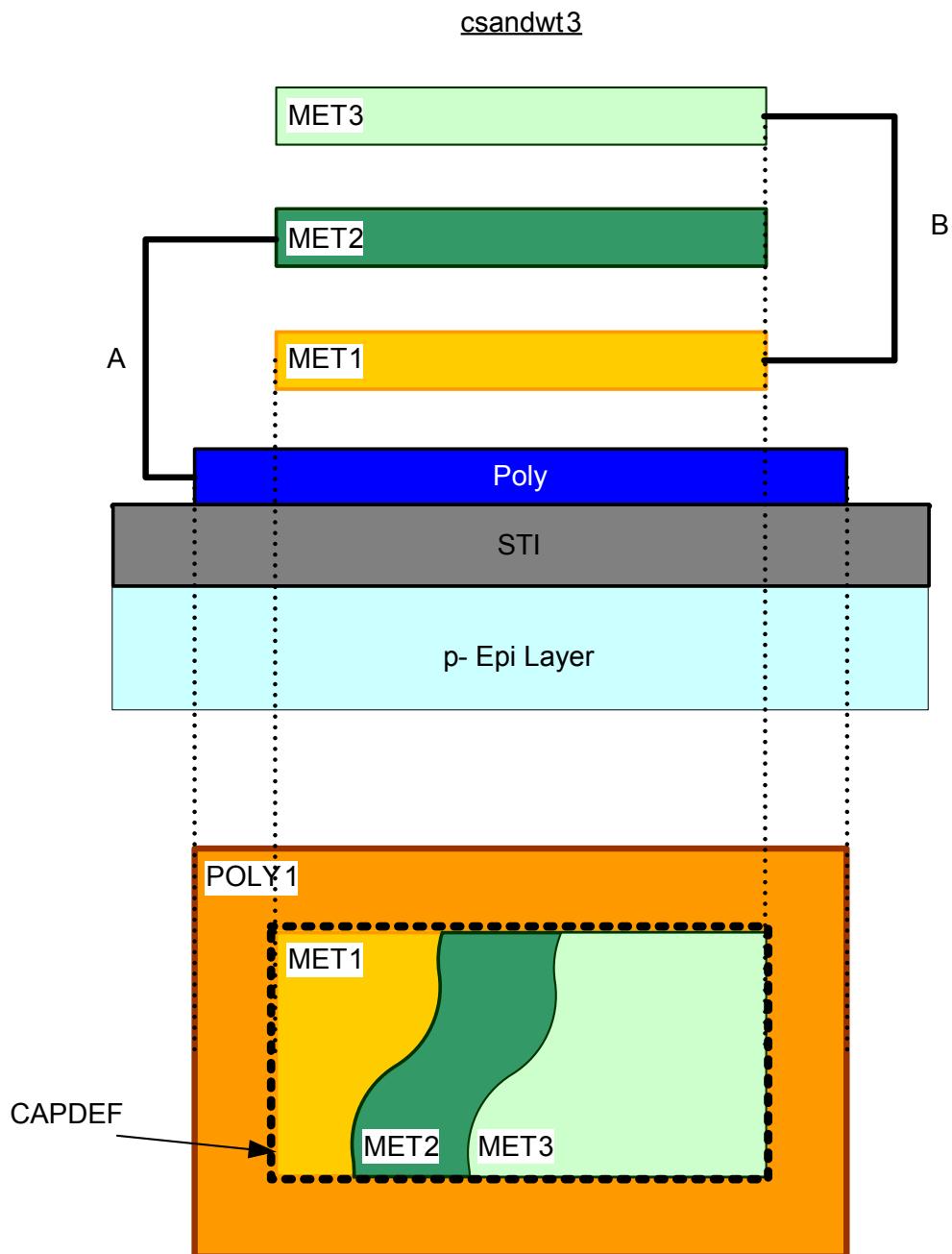


Figure 3.46 csandwt3

csf3p, csf3, csf3a

The layouts of the devices csf3p, csf3 and csf3a are fixed and must not be changed. For csf3p and csf3, a single cell instance has an area of 4.48 µm x 10.80 µm. For csf3a, a single cell instance has an area of 5.76 µm x 11.10 µm.

Note: Higher values may be achieved by the formation of arrays.

Note: CAPDEF is necessary for csf3p, csf3 and csf3a.

3. Layer and Device rules → 3.3 MET4 module

3.3 MET4 module

3.3.1 Layer rules

VIA3

Name	Description	Value	Unit
B1V3	VIA3 must be covered by MET3 and MET4	-	-
B2V3	VIA3 stripes are only allowed to bend at 135 degrees	-	-
W2V3	Fixed VIA3 stripe width Note: Stripes are only allowed for use with photodiodes or other optical purposes.	0.26	µm
W1V3	Fixed VIA3 size (except dphoc#, dphod#, PHODIO, OPTOVIA3)	0.26 x 0.26	µm x µm
S1V3	Minimum VIA3 spacing	0.26	µm
S9V3	Minimum VIA3 stripe to VIA3 spacing	1.0	µm
E1M3V3	Minimum MET3 enclosure of VIA3	0.01	µm
E1M4V3	Minimum MET4 enclosure of VIA3	0.01	µm
E2M3V3	Minimum MET3 enclosure of VIA3 (in one direction of VIA3 corner)	0.06	µm
E2M4V3	Minimum MET4 enclosure of VIA3 (in one direction of VIA3 corner)	0.06	µm
E4M4V3	Minimum MET4 enclosure of VIA3 stripe	0.1	µm
E8M3V3	Minimum MET3 enclosure of VIA3 stripe	0.1	µm
R1V3	Maximum ratio of VIA3 area to connected GATE area	20.0	-
Q20V3	Check for the right usage of OPTOVIA3 Note: VIA3 stripes must only be used for light shielding purpose.	-	-

Note: Bond pads require interconnecting vias between the metal layers. See section "Bond Pad".

3. Layer and Device rules → 3.3 MET4 module → 3.3.1 Layer rules → VIA3

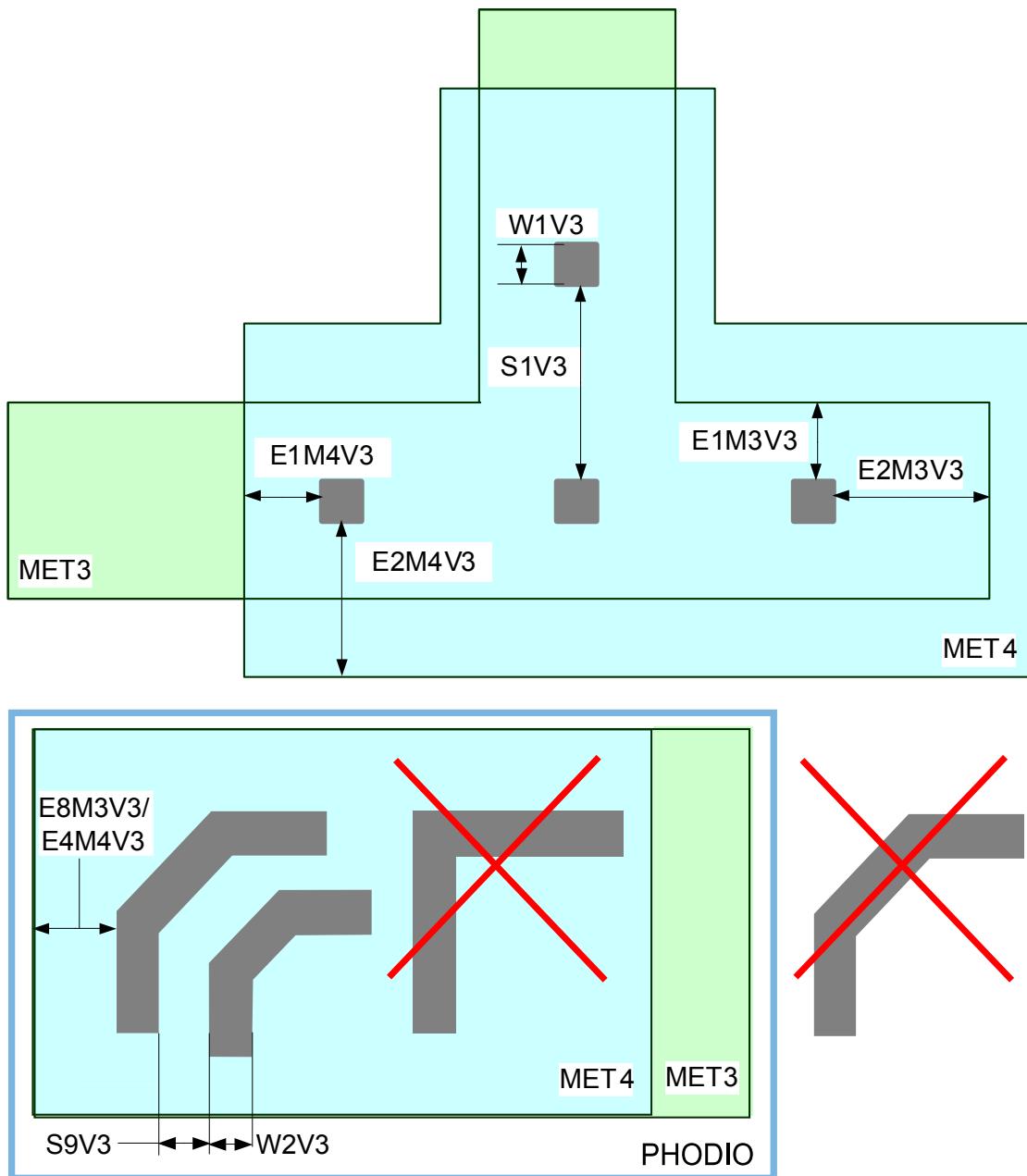


Figure 3.47 VIA3

3. Layer and Device rules → 3.3 MET4 module → 3.3.1 Layer rules → MET4

MET4

Name	Description	Value	Unit
B1M4	All MET4 tracks > 35µm wide to be slotted (except Pads)	-	-
W1M4	Minimum MET4 width	0.28	µm
W4M4	Minimum MET4 width joining wide MET4 track (> 35 µm)	10.0	µm
	Note: No slot is allowed opposite the join. It is recommended to maintain this width for at least 1 µm from the main track prior to narrowing it.		
W5M4	Maximum MET4 region size	17.0 x 17.0	µm x µm
	Note: Not checked with standard DRC, option for check is available.		
	Note: MET4 regions are defined as MET4 shapes (single MET4 shapes or a bundle of ME4 shapes, with width > 2.0µm, inclusive of the spacing if the spacing is <= 1.0µm) without any other metal layer above. For further information and design guidelines, please refer to the application note about IMD popping on "my X-FAB".		
S1M4	Minimum MET4 spacing/notch	0.28	µm
S4M4	Minimum MET4 spacing (different net, tag_60v)	0.4	µm
	Note: Valid for spacing of all MET4 shapes with label tag_60v to all MET4 shapes having lower voltage classes. Refer to the design related guideline "Voltage class definitions".		
S2M4	Minimum MET4 spacing to WIDE_MET4	0.6	µm
A1M4	Minimum MET4 area	0.202	µm ²
R1M4	Minimum ratio of MET4 area to EXTENT area	30.0	%
	Note: Not checked with standard DRC, option for check is available.		
R2M4	Maximum ratio of MET4 area to EXTENT area	65.0	%
	Note: Not checked with standard DRC, option for check is available.		
R1M4P1	Maximum ratio of MET4 area to connected GATE area	400.0	-
	Note: Refer to section "Antenna Rule definitions" as well.		
R2M4P1	Maximum ratio of MET4 area to connected GATE area	400.0	-
	Note: Refer to section "Antenna Rule definitions" as well.		
Q1M4	Resistor terminal net without VLABEL	-	-
	Note: Resistor having VLABEL at one terminal only is not allowed. Refer to the design related guideline "Voltage class definitions".		

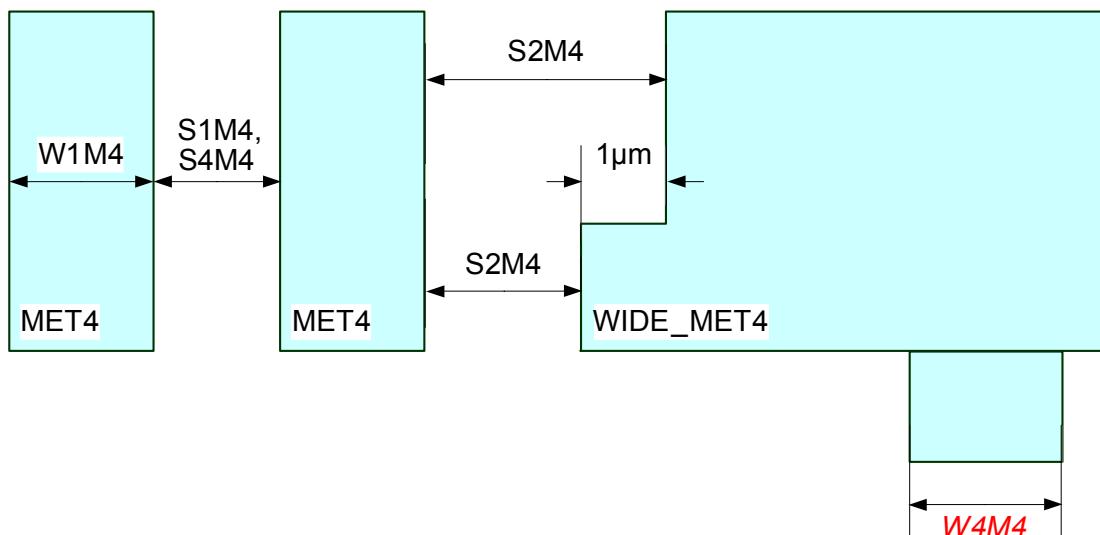


Figure 3.48 MET4

3. Layer and Device rules → 3.3 MET4 module → 3.3.1 Layer rules → M4SLOT

M4SLOT

Name	Description	Value	Unit
W2M4	Minimum M4SLOT width	0.6	μm
	Minimum M4SLOT length	20.0	μm
W3M4	Note: If this rule cannot be adhered to, it is suggested that the track in question is drawn as two narrow parallel tracks.		
S3M4	Minimum M4SLOT spacing/notch	10.0	μm
S1M4M3	Minimum M4SLOT spacing to M3SLOT Note: M4SLOT is not allowed over M3SLOT.	2.0	μm
E1M4M4	Minimum MET4 enclosure of M4SLOT Note: M4SLOT without MET4 is not allowed.	10.0	μm

Note: Insert M4SLOTS in direction of current flow.

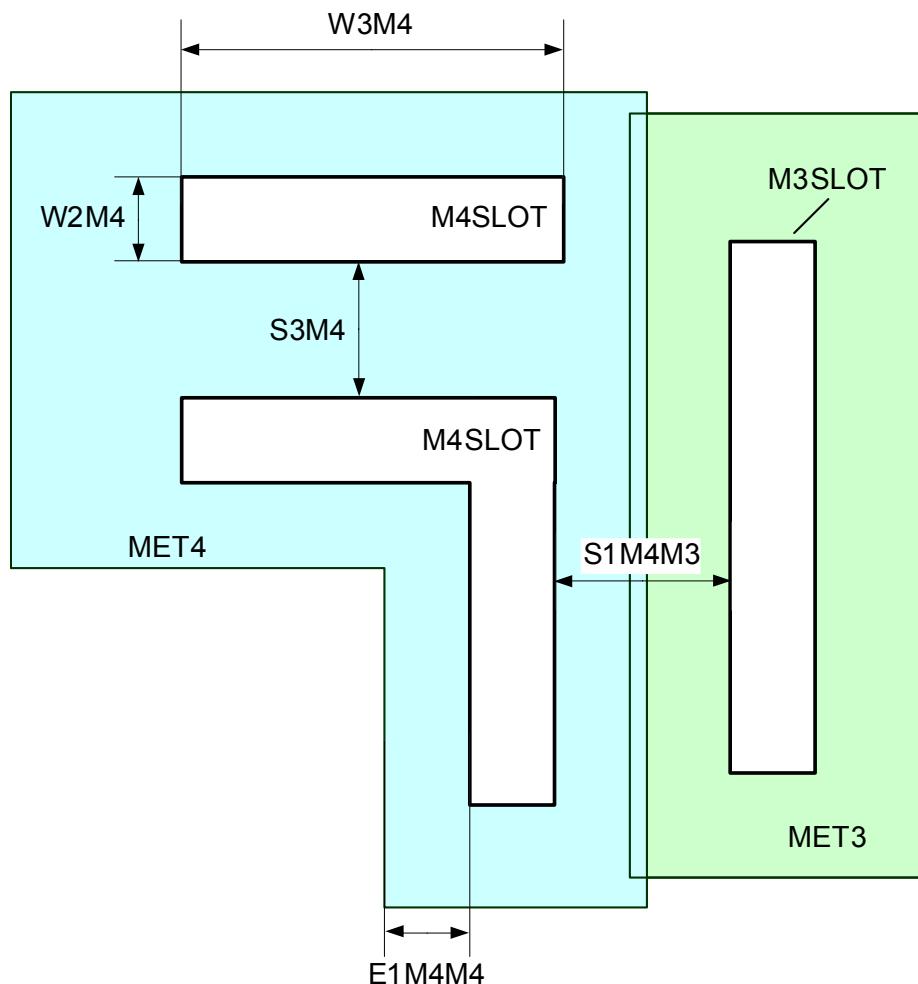


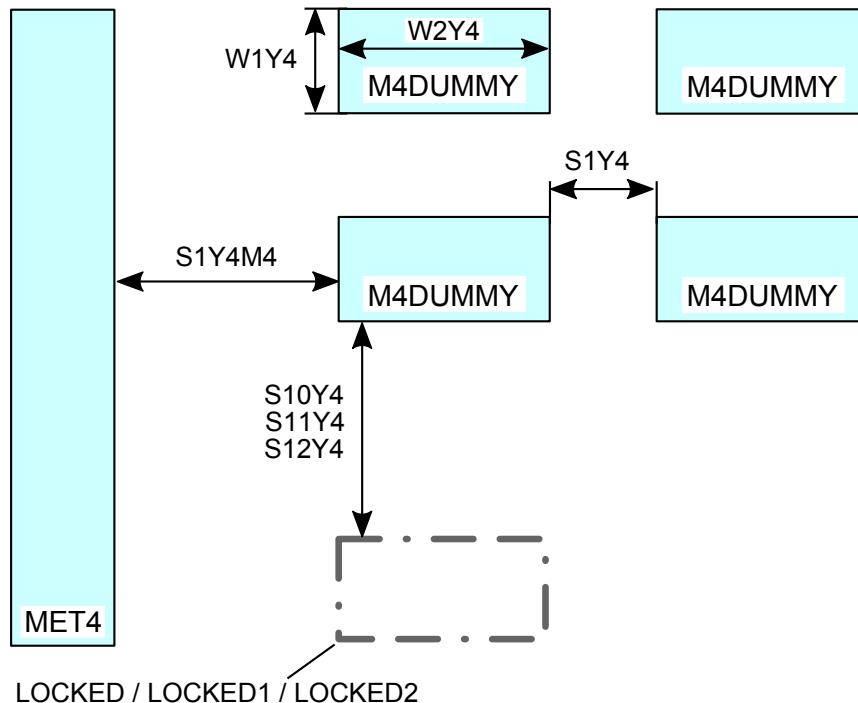
Figure 3.49 M4SLOT

3. Layer and Device rules → 3.3 MET4 module → 3.3.1 Layer rules → M4DUMMY

M4DUMMY

It is recommended to use X-FAB's dummy pattern generation option (DUMMY_FILL included in the DRC for preview) to create dummy pattern. If the generated dummy pattern is not sufficient to meet the minimum requirements for pattern density, customers can draw additional dummy pattern following the dummy design rules (DIFFDUMMY, P1DUMMY, M1DUMMY, M2DUMMY, M3DUMMY, M4DUMMY, M5DUMMY, MTPDUMMY and MTPLDUMMY). For further information, refer to the design related guideline "Dummy Pattern Generation".

Name	Description	Value	Unit
B1Y4	Only rectangular M4DUMMY is allowed	-	-
B2Y4	M4DUMMY overlap of MET4 is not allowed	-	-
B3Y4V3	M4DUMMY overlap of VIA3 is not allowed	-	-
B3Y4V4	M4DUMMY overlap of VIA4 is not allowed	-	-
B3Y4VT	M4DUMMY overlap of VIATP is not allowed Note: Only valid if module MET5 is not selected.	-	-
W1Y4	Minimum M4DUMMY width	2.0	μm
W2Y4	Maximum M4DUMMY edge length	20.0	μm
S1Y4	Minimum M4DUMMY spacing	2.0	μm
S10Y4	Minimum M4DUMMY spacing to LOCKED	4.0	μm
S11Y4	Minimum M4DUMMY spacing to LOCKED1	4.0	μm
S12Y4	Minimum M4DUMMY spacing to LOCKED2	4.0	μm
S1Y4M4	Minimum M4DUMMY spacing to MET4	4.0	μm

**Figure 3.50 M4DUMMY**

3. Layer and Device rules → 3.3 MET4 module → 3.3.2 Device rules → rm4

3.3.2 Device rules

rm4

Name	Description	Value	Unit
B2M4	VIA3 is not allowed within rm4	-	-
B3M4	VIATP is not allowed within rm4 Note: Valid if module METMID is selected and not MET5	-	-
B4M4	VIA4 is not allowed within rm4 Note: Valid if MET5 module is selected.	-	-

Note: rm4 resistor definition: MET4 and M4VERIFY.



Figure 3.51 rm4

3. Layer and Device rules → 3.3 MET4 module → 3.3.2 Device rules → csandwt4

csandwt4

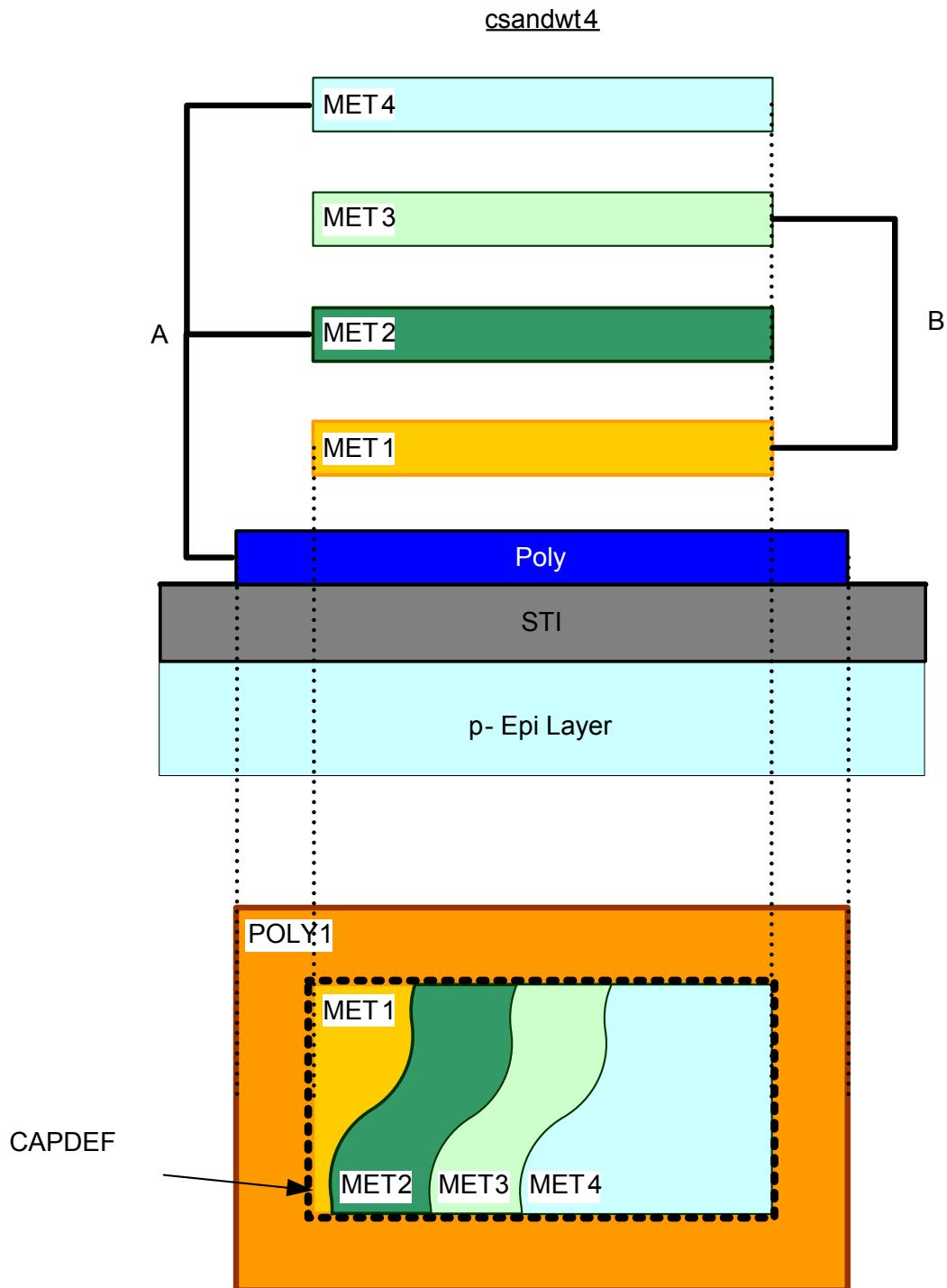


Figure 3.52 csandwt4

csf4, csf4a

The layouts of the devices csf4 and csf4a are fixed and must not be changed. For csf4, a single cell instance has an area of $4.48 \mu\text{m} \times 10.80 \mu\text{m}$. For csf4a, a single cell instance has an area of $5.76 \mu\text{m} \times 11.10 \mu\text{m}$.

Note: Higher values may be achieved by the formation of arrays.

Note: CAPDEF is necessary for csf4 and csf4a.

3. Layer and Device rules → 3.4 MET5 module

3.4 MET5 module

3.4.1 Layer rules

VIA4

Name	Description	Value	Unit
B1V4	VIA4 must be covered by MET4 and MET5	-	-
B2V4	VIA4 stripes are only allowed to bend at 135 degrees	-	-
W2V4	Fixed VIA4 stripe width Note: Stripes are only allowed for use with photodiodes or other optical purposes.	0.26	µm
W1V4	Fixed VIA4 size (except dphoc#, dphod#, PHODIO, OPTOVIA4)	0.26 x 0.26	µm x µm
S1V4	Minimum VIA4 spacing	0.26	µm
S5V4	Minimum VIA4 stripe to VIA4 spacing	1.0	µm
E1M4V4	Minimum MET4 enclosure of VIA4	0.01	µm
E1M5V4	Minimum MET5 enclosure of VIA4	0.01	µm
E2M4V4	Minimum MET4 enclosure of VIA4 (in one direction of VIA4 corner)	0.06	µm
E2M5V4	Minimum MET5 enclosure of VIA4 (in one direction of VIA4 corner)	0.06	µm
E3M5V4	Minimum MET5 enclosure of VIA4 stripe	0.1	µm
E5M4V4	Minimum MET4 enclosure of VIA4 stripe	0.1	µm
R1V4	Maximum ratio of VIA4 area to connected GATE area	20.0	-
Q20V4	Check for the right usage of OPTOVIA4 Note: VIA4 stripes must only be used for light shielding purpose.	-	-

Note: Bond pads require interconnecting vias between the metal layers. See section "Bond Pad".

3. Layer and Device rules → 3.4 MET5 module → 3.4.1 Layer rules → VIA4

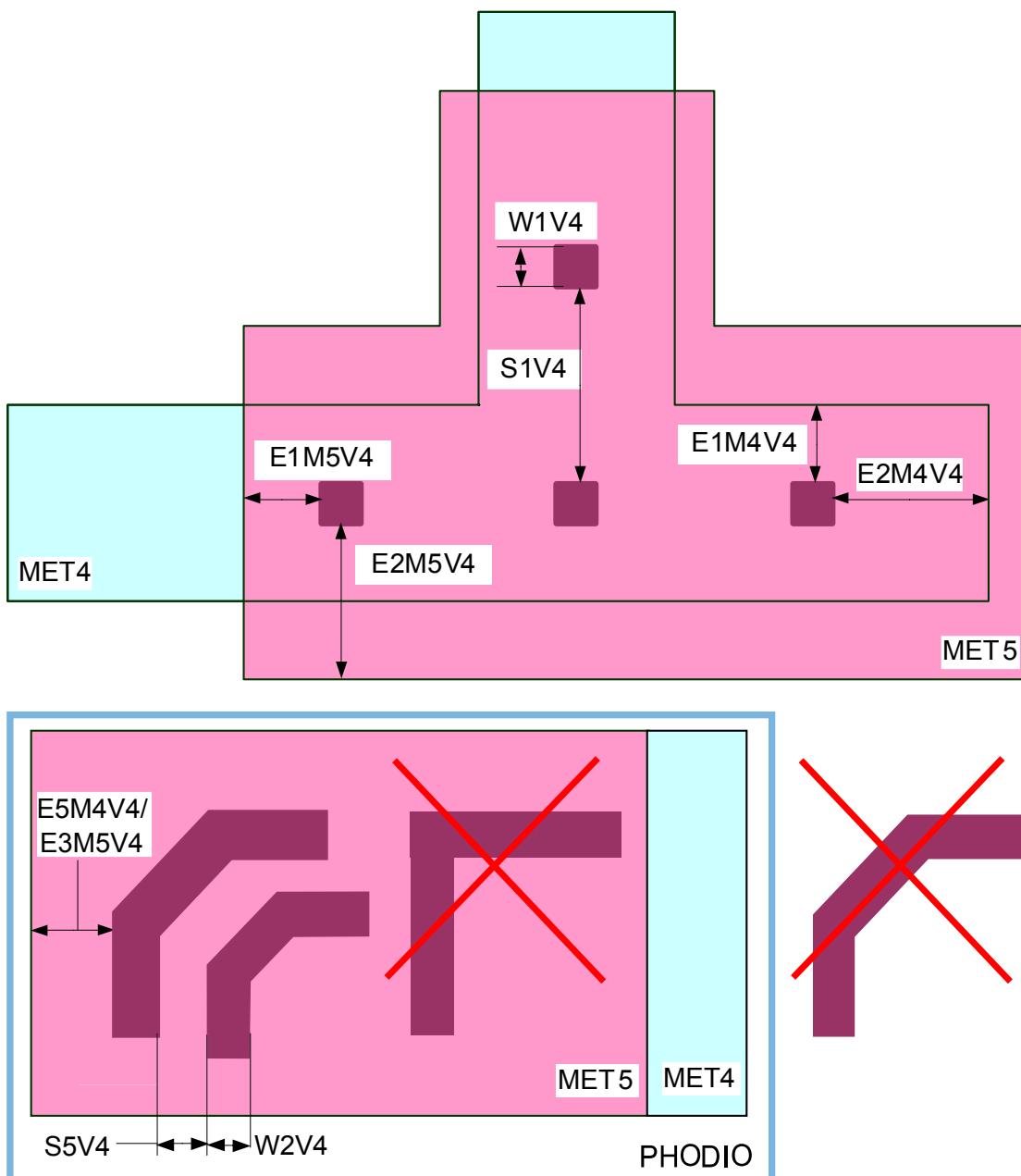


Figure 3.53 VIA4

3. Layer and Device rules → 3.4 MET5 module → 3.4.1 Layer rules → MET5

MET5

Name	Description	Value	Unit
B1M5	All MET5 tracks > 35µm wide to be slotted (except Pads)	-	-
W1M5	Minimum MET5 width	0.28	µm
<i>W4M5</i>	Minimum MET5 width joining wide MET5 track (> 35 µm)	10.0	µm
	Note: No slot is allowed opposite the join. It is recommended to maintain this width for at least 1 µm from the main track prior to narrowing it.		
<i>W5M5</i>	Maximum MET5 region size	17.0 x 17.0	µm x µm
	Note: Not checked with standard DRC, option for check is available.		
	Note: MET5 regions are defined as MET5 shapes (single MET5 shapes or a bundle of MET5 shapes, with width > 2.0µm, inclusive of the spacing if the spacing is <= 1.0µm) without any other metal layer above. For further information and design guidelines, please refer to the application note about IMD popping on "my X-FAB".		
S1M5	Minimum MET5 spacing/notch	0.28	µm
<i>S4M5</i>	Minimum MET5 spacing (different net, tag_60v)	0.4	µm
	Note: Valid for spacing of all MET5 shapes with label tag_60v to all MET5 shapes having lower voltage classes. Refer to the design related guideline "Voltage class definitions".		
S2M5	Minimum MET5 spacing to WIDE_MET5	0.6	µm
A1M5	Minimum MET5 area	0.202	µm ²
<i>R1M5</i>	Minimum ratio of MET5 area to EXTENT area	30.0	%
	Note: Not checked with standard DRC, option for check is available.		
<i>R2M5</i>	Maximum ratio of MET5 area to EXTENT area	65.0	%
	Note: Not checked with standard DRC, option for check is available.		
R1M5P1	Maximum ratio of MET5 area to connected GATE area	400.0	-
	Note: Refer to section "Antenna Rule definitions" as well.		
<i>R2M5P1</i>	Maximum ratio of MET5 area to connected GATE area	400.0	-
	Note: Refer to section "Antenna Rule definitions" as well.		
Q1M5	Resistor terminal net without VLABEL	-	-
	Note: Resistor having VLABEL at one terminal only is not allowed. Refer to the design related guideline "Voltage class definitions".		

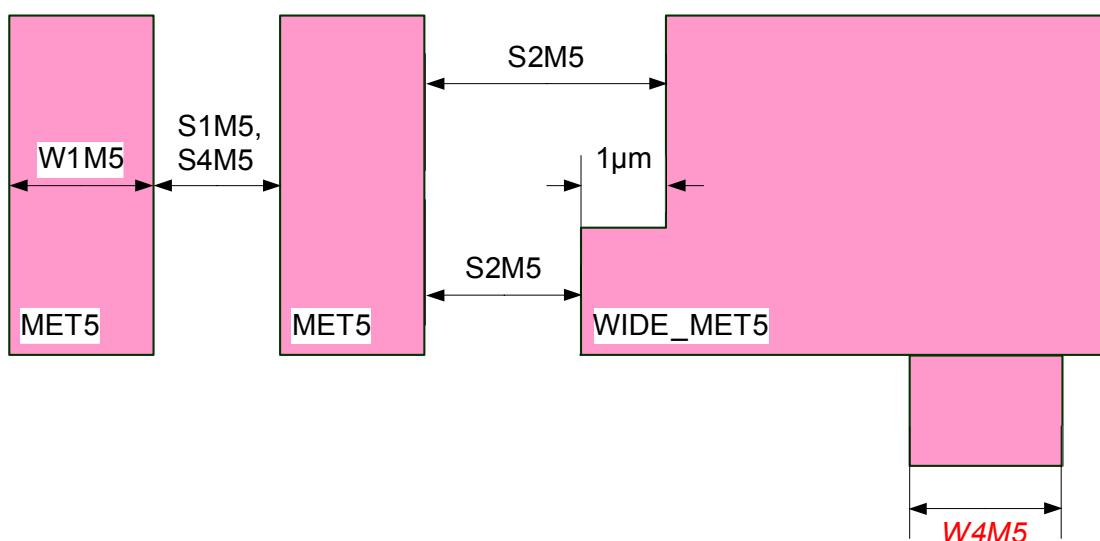


Figure 3.54 MET5

3. Layer and Device rules → 3.4 MET5 module→ 3.4.1 Layer rules→ M5SLOT

M5SLOT

Name	Description	Value	Unit
W2M5	Minimum M5SLOT width	0.6	μm
W3M5	Minimum M5SLOT length	20.0	μm
	Note: If this rule cannot be adhered to, it is suggested that the track in question is drawn as two narrow parallel tracks.		
S3M5	Minimum M5SLOT spacing/notch	10.0	μm
S1M5M4	Minimum M5SLOT spacing to M4SLOT	2.0	μm
	Note: M5SLOT is not allowed over M4SLOT.		
E1M5M5	Minimum MET5 enclosure of M5SLOT	10.0	μm
	Note: M5SLOT without MET5 is not allowed.		

Note: Insert M5SLOTS in direction of current flow.

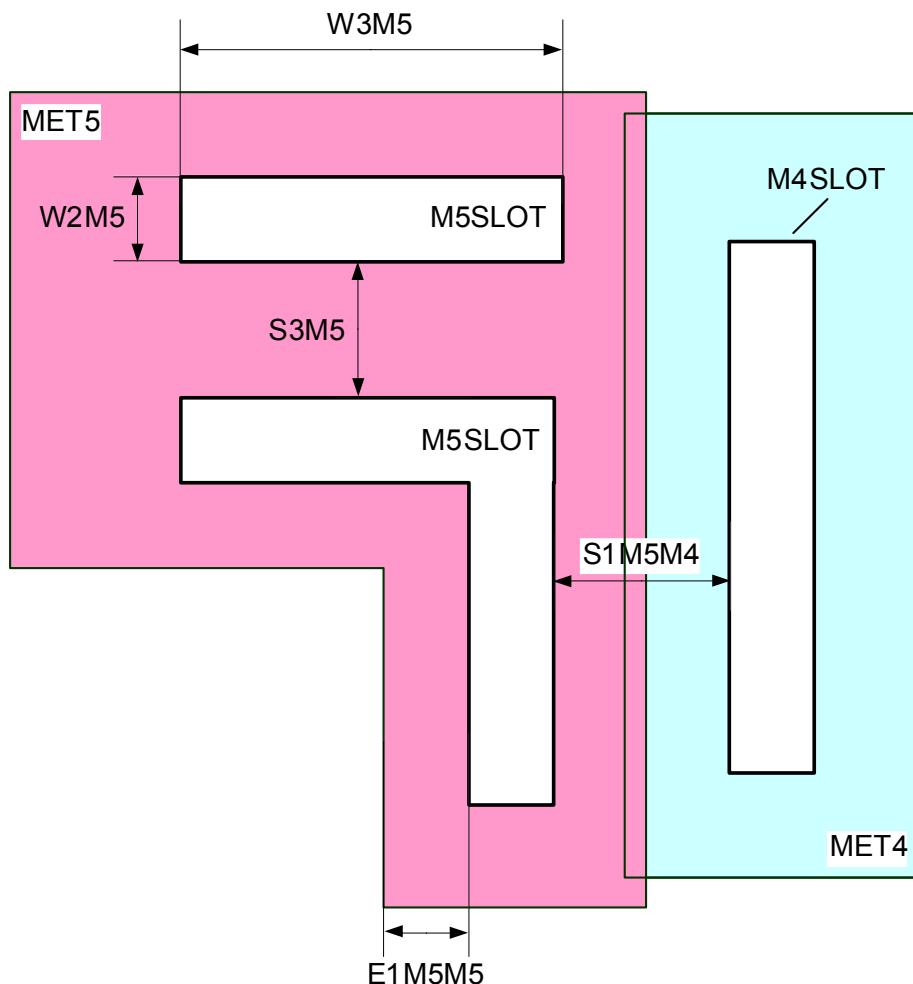


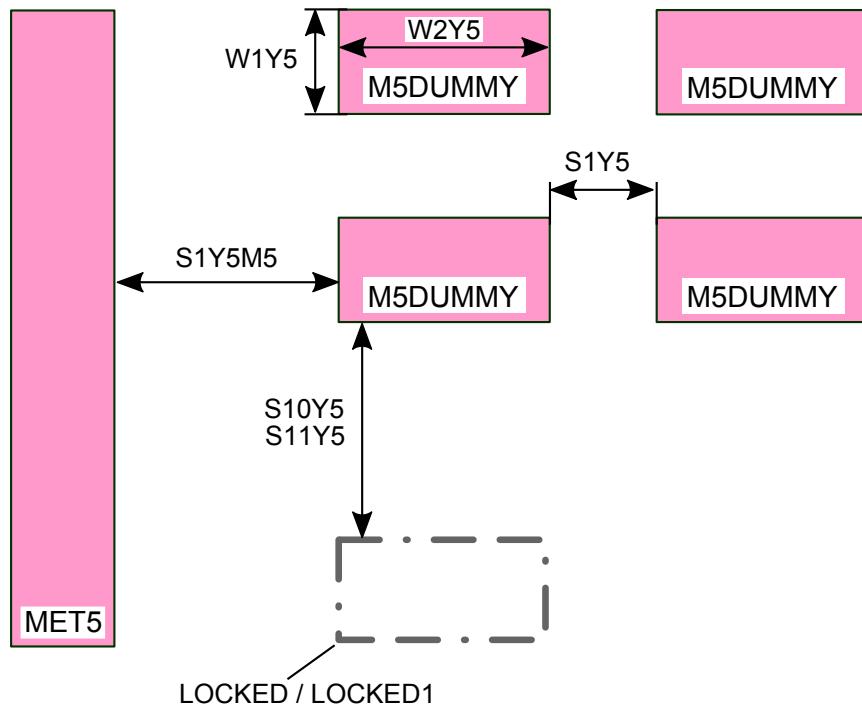
Figure 3.55 M5SLOT

3. Layer and Device rules → 3.4 MET5 module → 3.4.1 Layer rules → M5DUMMY

M5DUMMY

It is recommended to use X-FAB's dummy pattern generation option (DUMMY_FILL included in the DRC for preview) to create dummy pattern. If the generated dummy pattern is not sufficient to meet the minimum requirements for pattern density, customers can draw additional dummy pattern following the dummy design rules (DIFFDUMMY, P1DUMMY, M1DUMMY, M2DUMMY, M3DUMMY, M4DUMMY, M5DUMMY, MTPDUMMY and MTPLDUMMY). For further information, refer to the design related guideline "Dummy Pattern Generation".

Name	Description	Value	Unit
B1Y5	Only rectangular M5DUMMY is allowed	-	-
B2Y5	M5DUMMY overlap of MET5 is not allowed	-	-
B3Y5V4	M5DUMMY overlap of VIA4 is not allowed	-	-
B3Y5VT	M5DUMMY overlap of VIATP is not allowed	-	-
W1Y5	Minimum M5DUMMY width	2.0	μm
W2Y5	Maximum M5DUMMY edge length	20.0	μm
S1Y5	Minimum M5DUMMY spacing	2.0	μm
S10Y5	Minimum M5DUMMY spacing to LOCKED	4.0	μm
S11Y5	Minimum M5DUMMY spacing to LOCKED1	4.0	μm
S1Y5M5	Minimum M5DUMMY spacing to MET5	4.0	μm

**Figure 3.56 M5DUMMY**

3. Layer and Device rules → 3.4 MET5 module → 3.4.2 Device rules → rm5

3.4.2 Device rules

rm5

Name	Description	Value	Unit
B2M5	VIA4 is not allowed within rm5	-	-
B3M5	VIATP is not allowed within rm5	-	-

Note: rm5 resistor definition: MET5 and M5VERIFY.

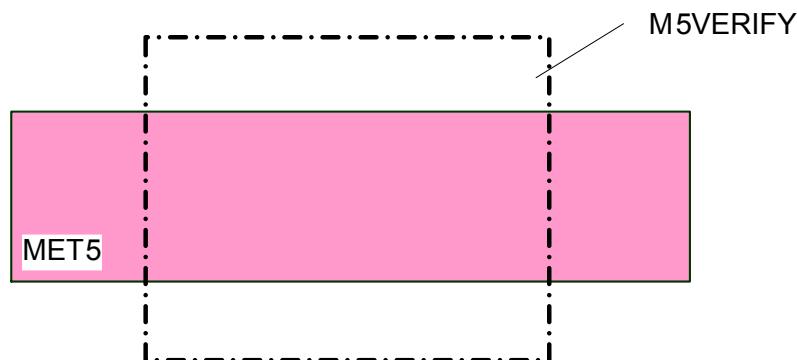


Figure 3.57 rm5

3. Layer and Device rules → 3.4 MET5 module → 3.4.2 Device rules → csandwt5

csandwt5

Note: CAPDEF is necessary for csandwt5.

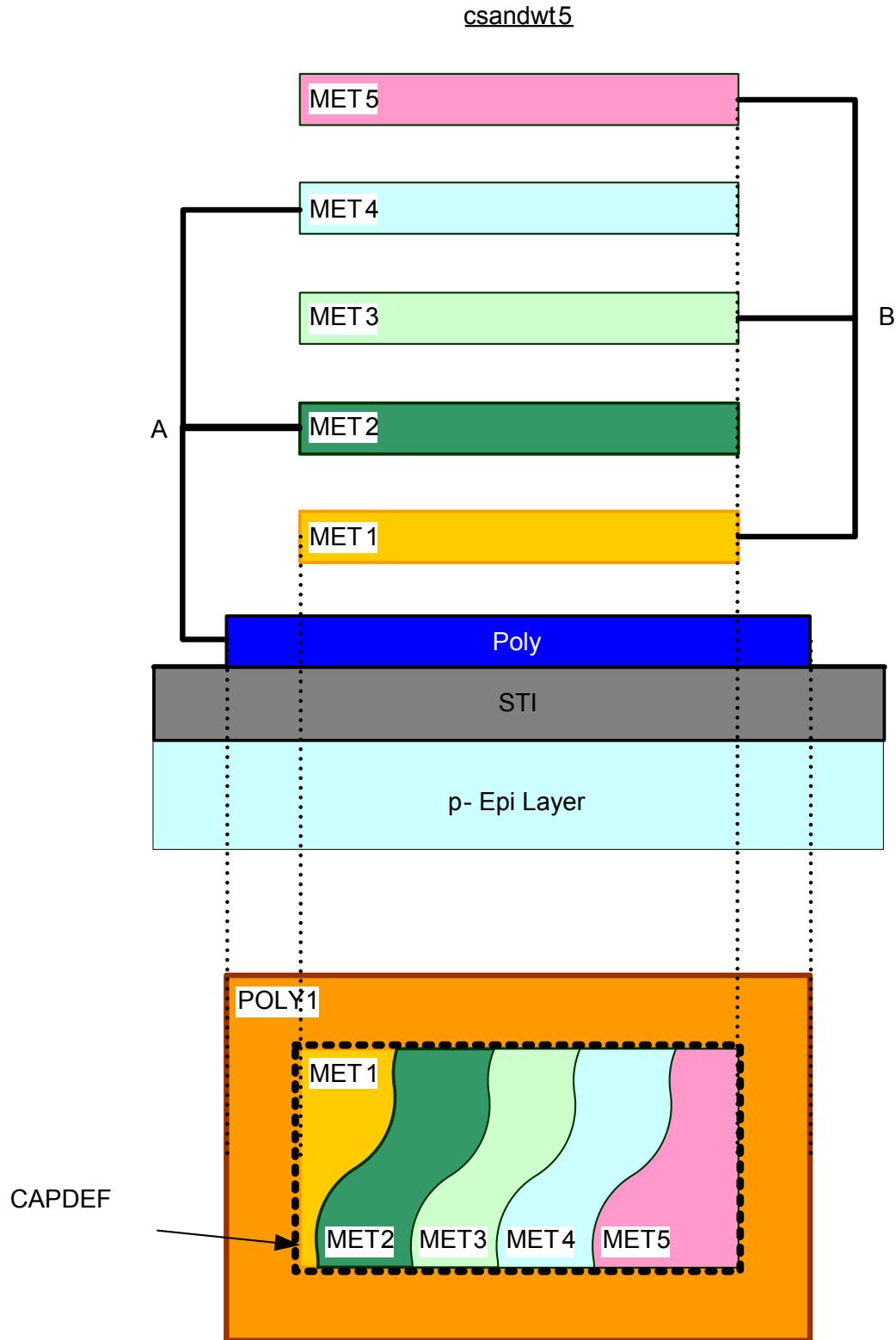


Figure 3.58 csandwt5

csf5, csf5a

The layout of the devices csf5 and csf5a are fixed and must not be changed. For csf5, a single cell instance has an area of $4.48 \mu\text{m} \times 10.80 \mu\text{m}$. For csf5a, a single cell instance has an area of $5.76 \mu\text{m} \times 11.10 \mu\text{m}$.



3. Layer and Device rules → 3.4 MET5 module→ 3.4.2 Device rules→ csf5, csf5a

Note: Higher values may be achieved by the formation of arrays.

Note: CAPDEF is necessary for csf5 and csf5a.

3. Layer and Device rules → 3.5 METMID module

3.5 METMID module

3.5.1 Layer rules

VIATP

Name	Description	Value	Unit
B1VT	VIATP must be covered by METTP	-	-
B1VTM3	VIATP must be covered by MET3 Note: Valid if MET4 module is not selected	-	-
B1VTM4	VIATP must be covered by MET4 Note: Valid if MET4 module is selected and MET5 module is not selected.	-	-
B1VTM5	VIATP must be covered by MET5 Note: Valid if MET5 module is selected	-	-
B2VT	VIATP stripes are only allowed to bend at 135 degrees	-	-
W2VT	Fixed VIATP stripe width Note: Stripes are only allowed for use with photodiodes or other optical purposes.	0.36	μm
W1VT	Fixed VIATP size (except dphoc#, dphod#, PHODIO, OPTOVIATP)	0.36 x 0.36	μm x μm
S1VT	Minimum VIATP spacing	0.35	μm
S9VT	Minimum VIATP stripe to VIATP spacing	1.0	μm
E1M3VT	Minimum MET3 enclosure of VIATP Note: Valid if MET4 module is not selected	0.01	μm
E1M4VT	Minimum MET4 enclosure of VIATP Note: Valid if MET4 module is selected and MET5 module is not selected.	0.01	μm
E1M5VT	Minimum MET5 enclosure of VIATP Note: Valid if MET5 module is selected	0.01	μm
E1MTVT	Minimum METTP enclosure of VIATP	0.09	μm
E2M3VT	Minimum MET3 enclosure of VIATP (in one direction of VIATP corner) Note: Valid if MET4 module is not selected	0.06	μm
E2M4VT	Minimum MET4 enclosure of VIATP (in one direction of VIATP corner) Note: Valid if MET4 module is selected and MET5 module is not selected.	0.06	μm
E2M5VT	Minimum MET5 enclosure of VIATP (in one direction of VIATP corner) Note: Valid if MET5 module is selected	0.06	μm
E3MTVT	Minimum METTP enclosure of VIATP stripe	0.2	μm
E4M5VT	Minimum MET5 enclosure of VIATP stripe Note: Valid if MET5 module is selected	0.2	μm
E5M3VT	Minimum MET3 enclosure of VIATP stripe Note: Valid if MET4 module is not selected	0.2	μm
E5M4VT	Minimum MET4 enclosure of VIATP stripe Note: Valid if MET4 module is selected and MET5 module is not selected.	0.2	μm
R1VT	Maximum ratio of VIATP area to connected GATE area	20.0	-
Q20VT	Check for the right usage of OPTOVIATP Note: VIATP stripes must only be used for light shielding purpose.	-	-

Note: Bond pads require interconnecting vias between the metal layers. See section "Bond Pad".

3. Layer and Device rules → 3.5 METMID module → 3.5.1 Layer rules → VIATP

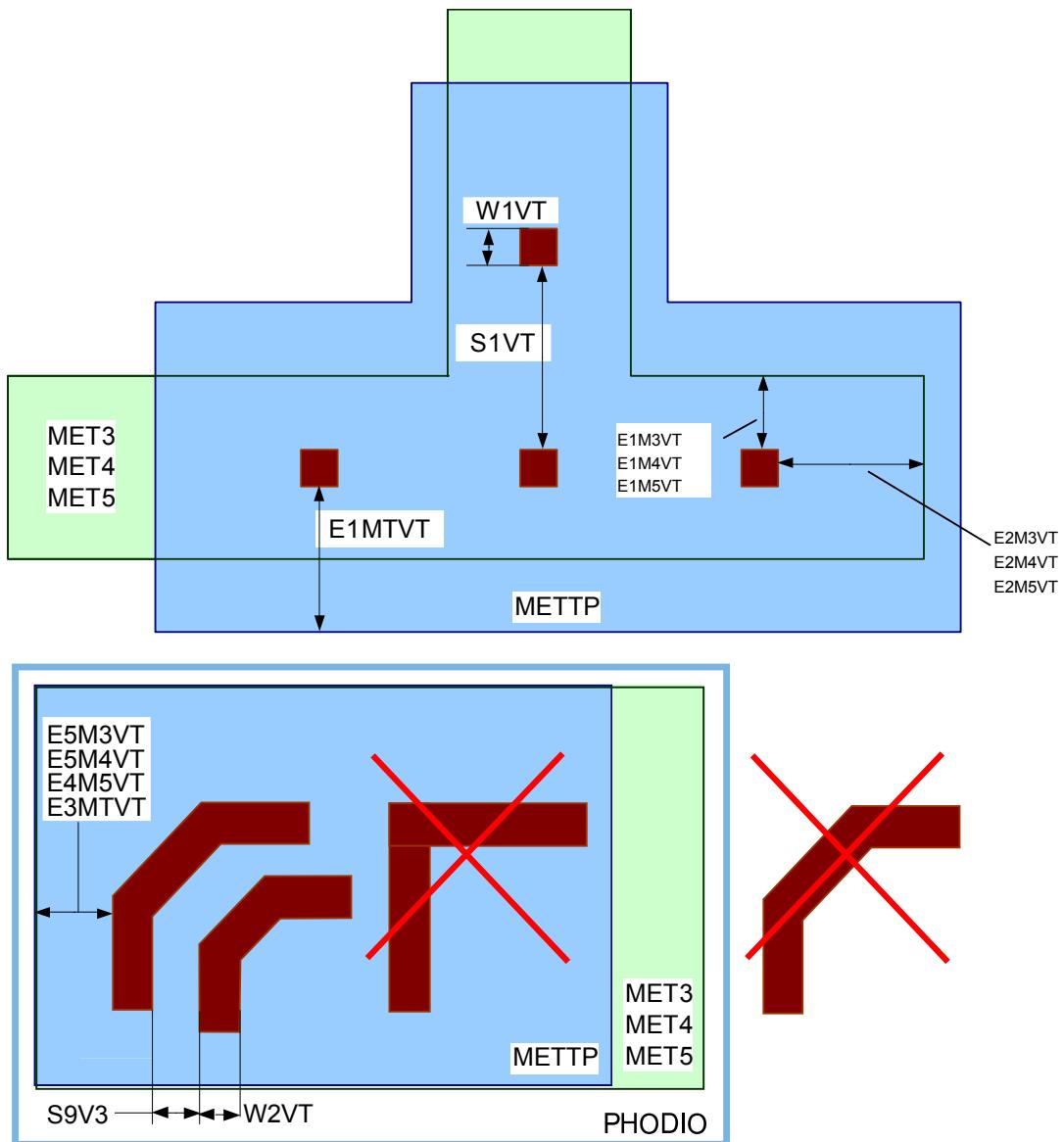


Figure 3.59 VIATP

3. Layer and Device rules → 3.5 METMID module→ 3.5.1 Layer rules→ METTP

METTP

Name	Description	Value	Unit
B1MT	All METTP tracks > 35µm wide to be slotted (except Pads)	-	-
W1MT	Minimum METTP width	0.44	µm
W4MT	Minimum METTP width joining wide METTP track (> 35 µm)	10.0	µm
	Note: No slot is allowed opposite the join. It is recommended to maintain this width for at least 1 µm from the main track prior to narrowing.		
W5MT	Maximum METTP region size	17.0 x 17.0	µm x µm
	Note: Not checked with standard DRC, option for check is available.		
	Note: METTP regions are defined as METTP shapes (single METTP shapes or a bundle of METTP shapes, with width > 2.0µm inclusive of the spacing if the spacing is <= 1.0µm) without any other metal layer above. For further information and design guidelines, please refer to the application note about IMD popping on "my X-FAB".		
S1MT	Minimum METTP spacing/notch	0.46	µm
S4MT	Minimum METTP spacing (different net, tag_60v)	0.5	µm
	Note: Valid for spacing of all METTP shapes with label tag_60v to all METTP shapes having lower voltage classes. Refer to the design related guideline "Voltage class definitions".		
S2MT	Minimum METTP spacing to WIDE_METTP	0.6	µm
A1MT	Minimum METTP area	0.562	µm ²
R1MT	Minimum ratio of METTP area to EXTENT area	30.0	%
	Note: Not checked with standard DRC, option for check is available.		
R2MT	Maximum ratio of METTP area to EXTENT area	65.0	%
	Note: Not checked with standard DRC, option for check is available.		
R1MTP1	Maximum ratio of METTP area to connected GATE area	400.0	-
	Note: Refer to section "Antenna Rule definitions" as well.		
R2MTP1	Maximum ratio of METTP area to connected GATE area	400.0	-
	Note: Refer to section "Antenna Rule definitions" as well.		
Q1MT	Resistor terminal net without VLABEL	-	-
	Note: Resistor having VLABEL at one terminal only is not allowed. Refer to the design related guideline "Voltage class definitions".		

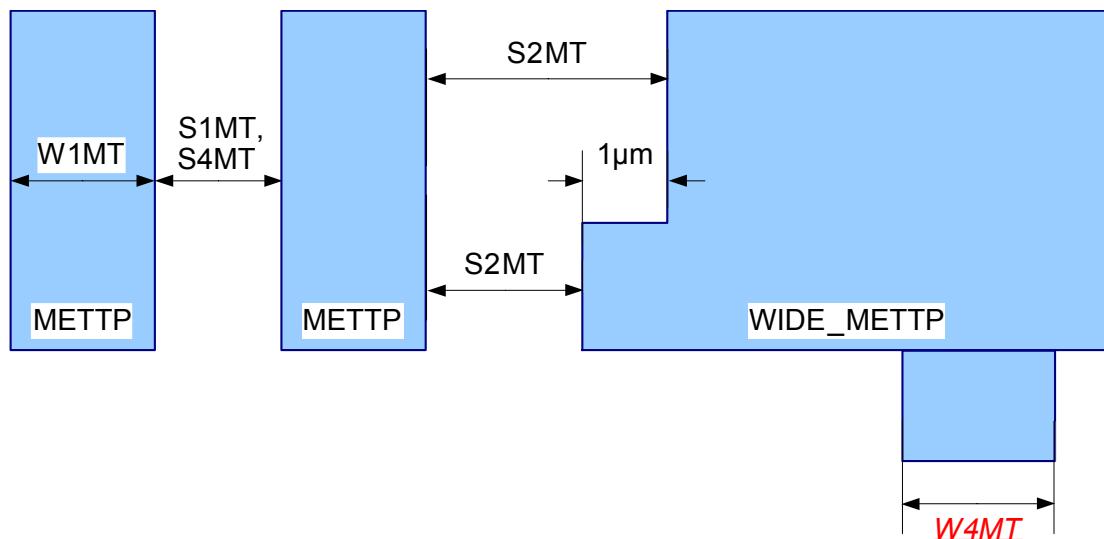


Figure 3.60 METTP

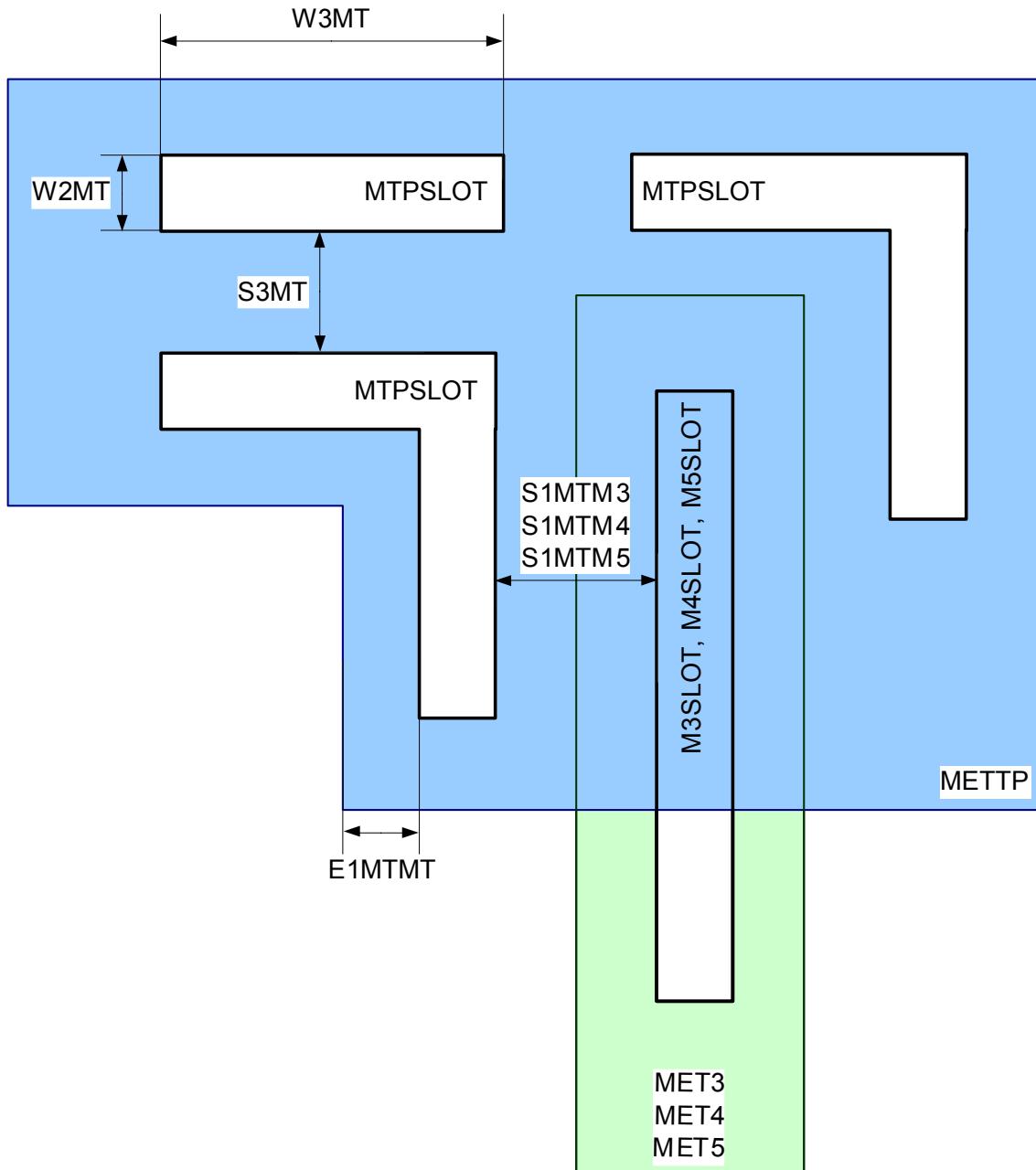
3. Layer and Device rules → 3.5 METMID module→ 3.5.1 Layer rules→ MTPSLOT

MTPSLOT

Name	Description	Value	Unit
W2MT	Minimum MTPSLOT width	0.6	µm
W3MT	Minimum MTPSLOT length Note: If this rule cannot be adhered to, it is suggested that the track in question is drawn as two narrow parallel tracks.	20.0	µm
S3MT	Minimum MTPSLOT spacing/notch	10.0	µm
S1MTM3	Minimum MTPSLOT spacing to M3SLOT Note: MTPSLOT is not allowed over M3SLOT. Note: Valid if module MET4 is not selected	2.0	µm
S1MTM4	Minimum MTPSLOT spacing to M4SLOT Note: Valid if module MET4 is selected and not MET5 Note: MTPSLOT is not allowed over M4SLOT.	2.0	µm
S1MTM5	Minimum MTPSLOT spacing to M5SLOT Note: Valid if module MET5 is selected Note: MTPSLOT is not allowed over M5SLOT.	2.0	µm
E1MTMT	Minimum METTP enclosure of MTPSLOT Note: MTPSLOT without METTP is not allowed.	10.0	µm

Note: Insert MTPSLOTs in direction of current flow.

3. Layer and Device rules → 3.5 METMID module → 3.5.1 Layer rules→ MTPSLOT

**Figure 3.61** MTPSLOT

3. Layer and Device rules → 3.5 METMID module → 3.5.1 Layer rules → MTPDUMMY

MTPDUMMY

It is recommended to use X-FAB's dummy pattern generation option (DUMMY_FILL included in the DRC for preview) to create dummy pattern. If the generated dummy pattern is not sufficient to meet the minimum requirements for pattern density, customers can draw additional dummy pattern following the dummy design rules (DIFFDUMMY, P1DUMMY, M1DUMMY, M2DUMMY, M3DUMMY, M4DUMMY, M5DUMMY, MTPDUMMY and MTPLDUMMY). For further information, refer to the design related guideline "Dummy Pattern Generation".

Name	Description	Value	Unit
B1YT	Only rectangular MTPDUMMY is allowed	-	-
B2YT	MTPDUMMY overlap of METTP is not allowed	-	-
B3YTVL	MTPDUMMY overlap of VIATPL is not allowed	-	-
B3YTVT	MTPDUMMY overlap of VIATP is not allowed	-	-
W1YT	Minimum MTPDUMMY width	2.0	μm
W2YT	Maximum MTPDUMMY edge length	20.0	μm
S1YT	Minimum MTPDUMMY spacing	2.0	μm
S1YTMT	Minimum MTPDUMMY spacing to METTP	2.0	μm
S10YT	Minimum MTPDUMMY spacing to LOCKED	2.0	μm
S11YT	Minimum MTPDUMMY spacing to LOCKED1	2.0	μm
	Note: Only valid if module MET5 is not selected.		
S12YT	Minimum MTPDUMMY spacing to LOCKED2	2.0	μm
	Note: Only valid if module MET4 is not selected.		
S1YTPA	Minimum MTPDUMMY spacing to PAD	5.0	μm

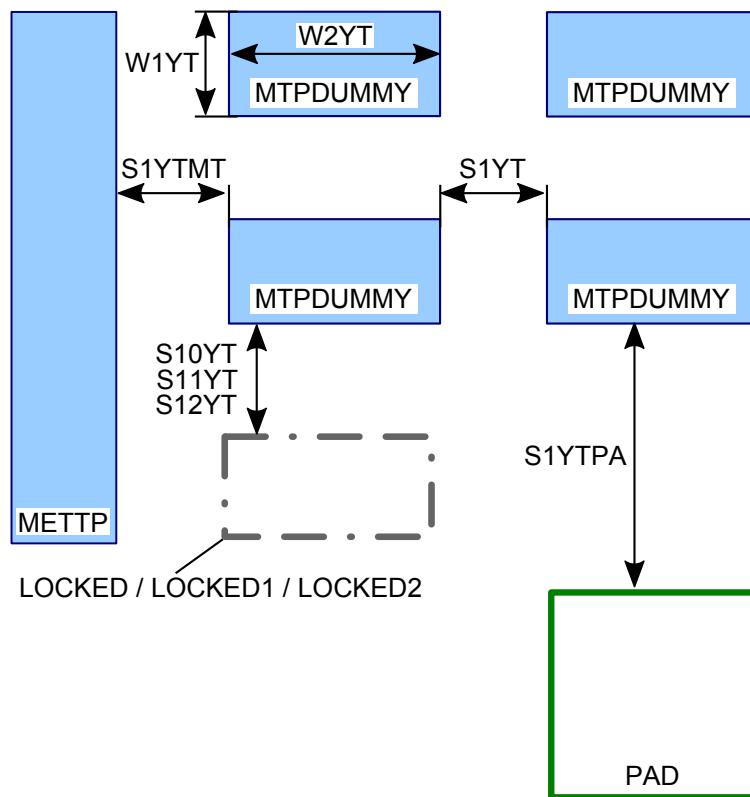


Figure 3.62 MTPDUMMY

3. Layer and Device rules → 3.5 METMID module → 3.5.2 Device rules → rmtp

3.5.2 Device rules

rmtp

Name	Description	Value	Unit
B2MT	VIATP is not allowed within rmtp	-	-
B3MT	VIATPL is not allowed within rmtp	-	-
Note: Valid if METTHK is selected.			

Note: rmtp resistor definition: METTP and MTPVERIFY.

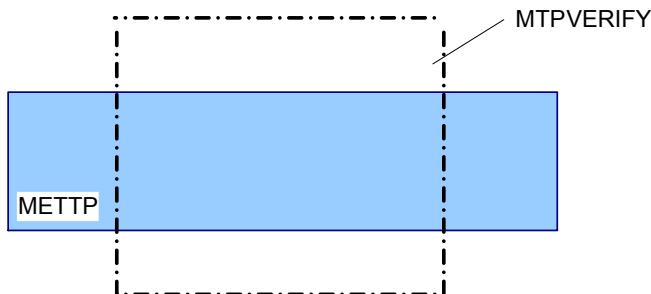


Figure 3.63 rmtp

csft4, csft4a, csft5, csft5a, csft6, csft6a

The layouts of the devices csft4, csft4a, csft5, csft5a, csft6 and csft6a are fixed and must not be changed. For csft4, csft5 and csft6, a single cell instance has an area of 4.48 µm x 10.80 µm. For csft4a, csft5a and csft6a, a single cell instance has an area of 5.76 µm x 11.10 µm.

Note: Higher values may be achieved by the formation of arrays.

Note: CAPDEF is necessary for csft4, csft4a, csft5, csft5a, csft6 and csft6a.

3. Layer and Device rules → 3.6 METTHK module

3.6 METTHK module

3.6.1 Layer rules

VIATPL

Name	Description	Value	Unit
B1VL	VIATPL must be covered by METTPL	-	-
B1VLMT	VIATPL must be covered by METTP	-	-
Note: Valid if METMID module is selected.			
W1VL	Fixed VIATPL size	0.50 x 0.50	μm x μm
S1VL	Minimum VIATPL spacing	0.45	μm
E1MLVL	Minimum METTPL enclosure of VIATPL	0.5	μm
E1MTVL	Minimum METTP enclosure of VIATPL	0.5	μm
R1VL	Maximum ratio of VIATPL area to connected GATE area	20.0	-

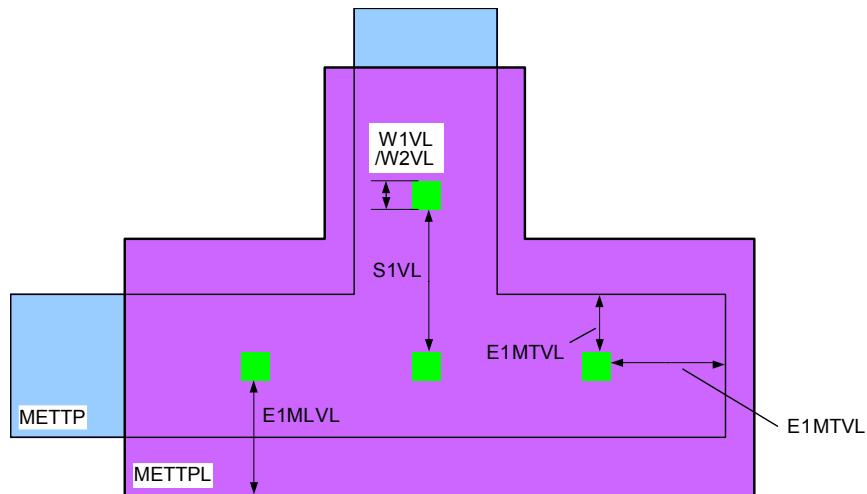


Figure 3.64 VIATPL

3. Layer and Device rules → 3.6 METTHK module→ 3.6.1 Layer rules→ METTPL

METTPL

Name	Description	Value	Unit
B1ML	METTPL tracks >35.0µm are not allowed (except Pads) Note: dimensions greater than the limit above should be divided into parallel tracks.	-	-
W1ML	Minimum METTPL width	3.0	µm
S1ML	Minimum METTPL spacing/notch	2.5	µm
A1ML	Minimum METTPL area	10.0	µm ²
A2ML	Minimum METTPL enclosed area	18.0	µm ²
<i>R1ML</i>	Minimum ratio of METTPL area to EXTENT area Note: Not checked with standard DRC, option for check is available.	30.0	%
<i>R2ML</i>	Maximum ratio of METTPL area to EXTENT area Note: Not checked with standard DRC, option for check is available.	65.0	%
R1MLP1	Maximum ratio of METTPL area to connected GATE area Note: Refer to section "Antenna Rule definitions" as well.	200.0	-
R2MLP1	Maximum ratio of METTPL area to connected GATE area Note: Refer to section "Antenna Rule definitions" as well.	200.0	-
Q1ML	Resistor terminal net without VLABEL Note: Resistor having VLABEL at one terminal only is not allowed. Refer to the design related guideline "Voltage class definitions".	-	-

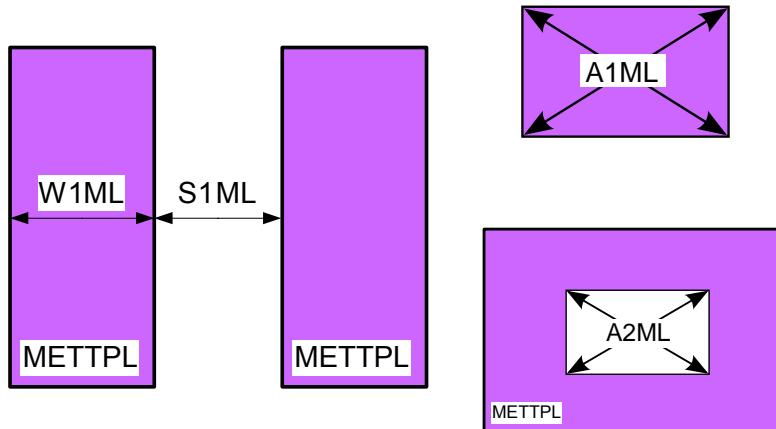


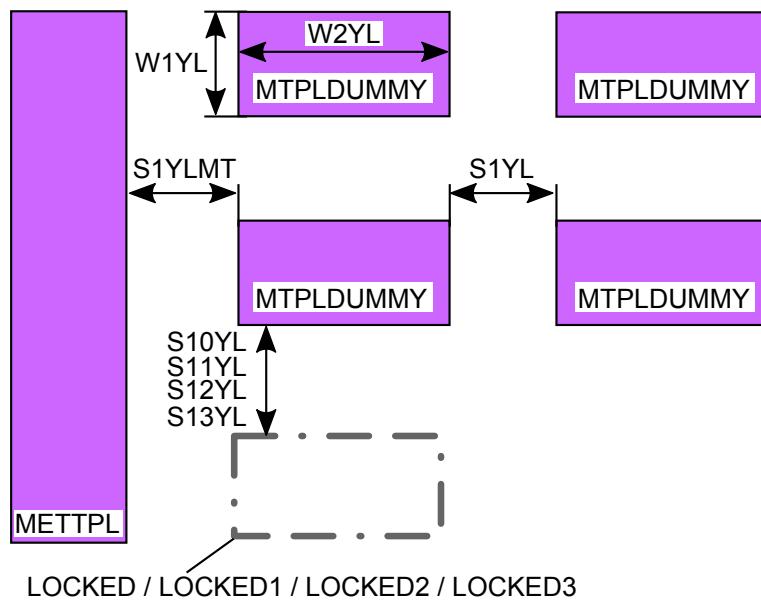
Figure 3.65 METTPL

3. Layer and Device rules → 3.6 METTHK module→ 3.6.1 Layer rules→ MTPLDUMMY

MTPLDUMMY

It is recommended to use X-FAB's dummy pattern generation option (DUMMY_FILL included in the DRC for preview) to create dummy pattern. If the generated dummy pattern is not sufficient to meet the minimum requirements for pattern density, customers can draw additional dummy pattern following the dummy design rules (DIFFDUMMY, P1DUMMY, M1DUMMY, M2DUMMY, M3DUMMY, M4DUMMY, M5DUMMY, MTPDUMMY and MTPLDUMMY). For further information, refer to the design related guideline "Dummy Pattern Generation".

Name	Description	Value	Unit
B1YL	Only rectangular MTPLDUMMY is allowed	-	-
B2YL	MTPLDUMMY overlap of METTPL is not allowed	-	-
B3YLVL	MTPLDUMMY overlap of VIATPL is not allowed	-	-
W1YL	Minimum MTPLDUMMY width	5.0	μm
W2YL	Maximum MTPLDUMMY edge length	20.0	μm
S1YL	Minimum MTPLDUMMY spacing	5.0	μm
S10YL	Minimum MTPLDUMMY spacing to LOCKED	5.0	μm
S11YL	Minimum MTPLDUMMY spacing to LOCKED1	5.0	μm
Note: Not valid if (MET4 and METMID) modules are selected or MET5 module is selected.			
S1YML	Minimum MTPLDUMMY spacing to METTPL	5.0	μm

**Figure 3.66** MTPLDUMMY

3. Layer and Device rules → 3.6 METTHK module→ 3.6.2 Device rules→ rmtpl

3.6.2 Device rules

rmtpl

Name	Description	Value	Unit
B2ML	VIATPL is not allowed within rmtpl	-	-

Note: rmtpl resistor definition: METTPL and MLVERIFY.

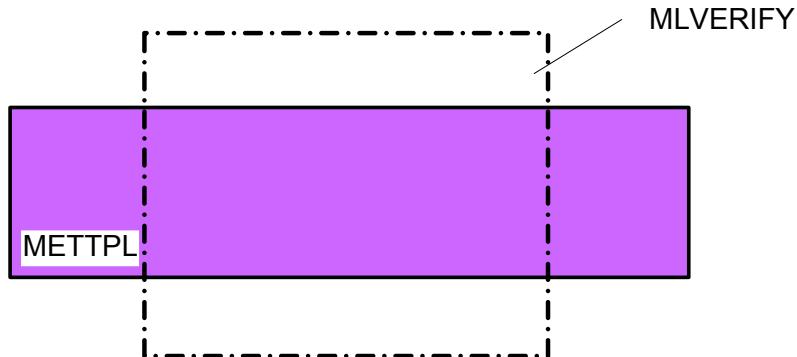


Figure 3.67 rmtpl

3. Layer and Device rules → 3.7 CPOD module

3.7 CPOD module

3.7.1 Layer rules

BNIMP

Name	Description	Value	Unit
B1NU	BNIMP overlap of LVT, SVT, DEPL, HVDEPL, PDD, LNDEV or ULN is not allowed	-	-
B2NU	BNIMP overlap of NTYPE_WELL is not allowed	-	-
B3NU	BNIMP overlap of HVPWELL is not allowed	-	-
B4NU	(BNIMP and DIFF) without NIMP is not allowed	-	-
W1NU	Minimum BNIMP width	0.6	μm
S1NU	Minimum BNIMP spacing/notch	0.6	μm
S1NUDF	Minimum BNIMP spacing to DIFF	0.35	μm
	Note: Not valid for DIFFDUMMY.		
S1NUGA	Minimum BNIMP spacing to GATE	0.45	μm
E1NUGA	Minimum BNIMP enclosure of GATE	0.25	μm
E1NUDN	Minimum BNIMP extension beyond NDIFF	0.25	μm

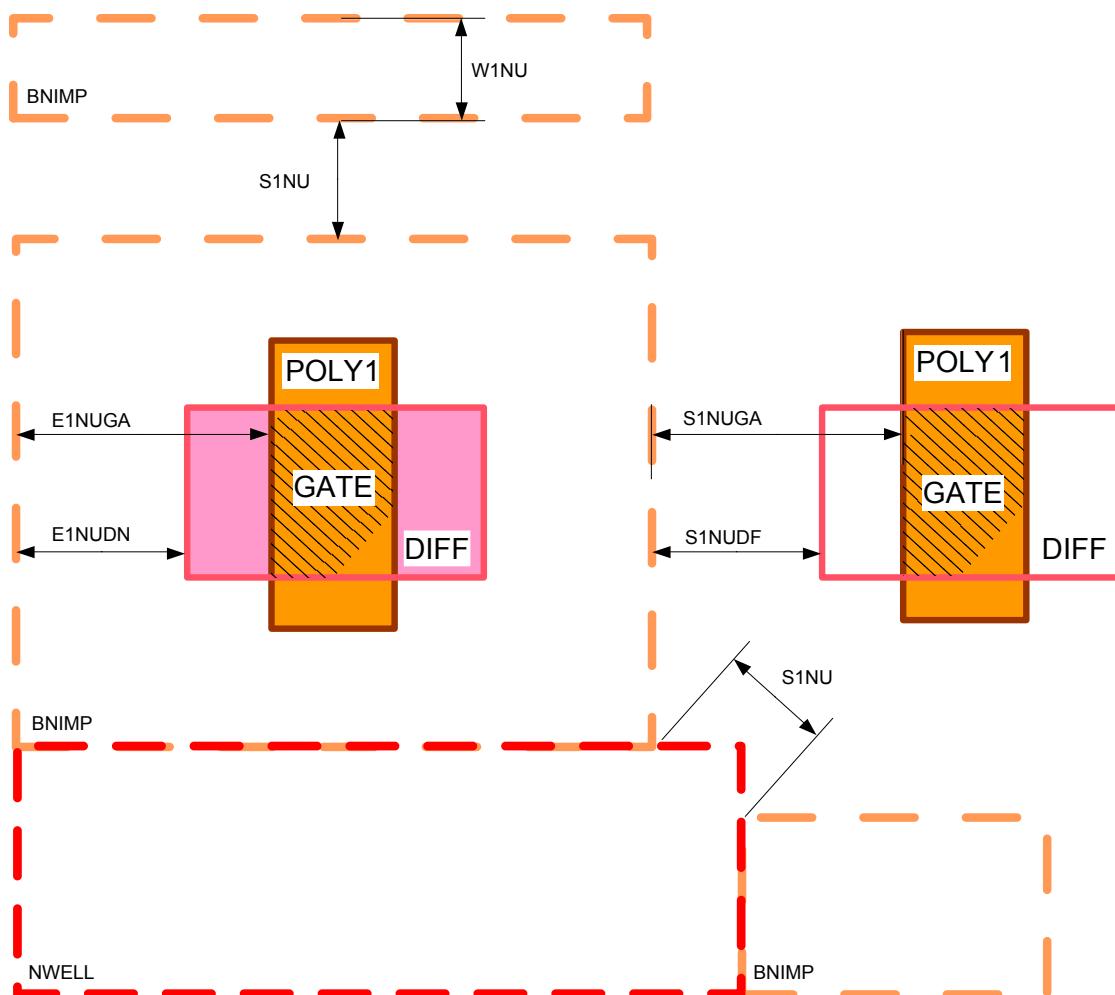


Figure 3.68 BNIMP

3. Layer and Device rules → 3.7 CPOD module → 3.7.2 Device rules → cpod

3.7.2 Device rules

cpod

Name	Description	Value	Unit
B5NU	BNIMP without PWBLK is not allowed	-	-
W2NU	Minimum cpod# width	2.0	μm
E2PBDN	Fixed PWBLK enclosure of NDIFF	1.2	μm

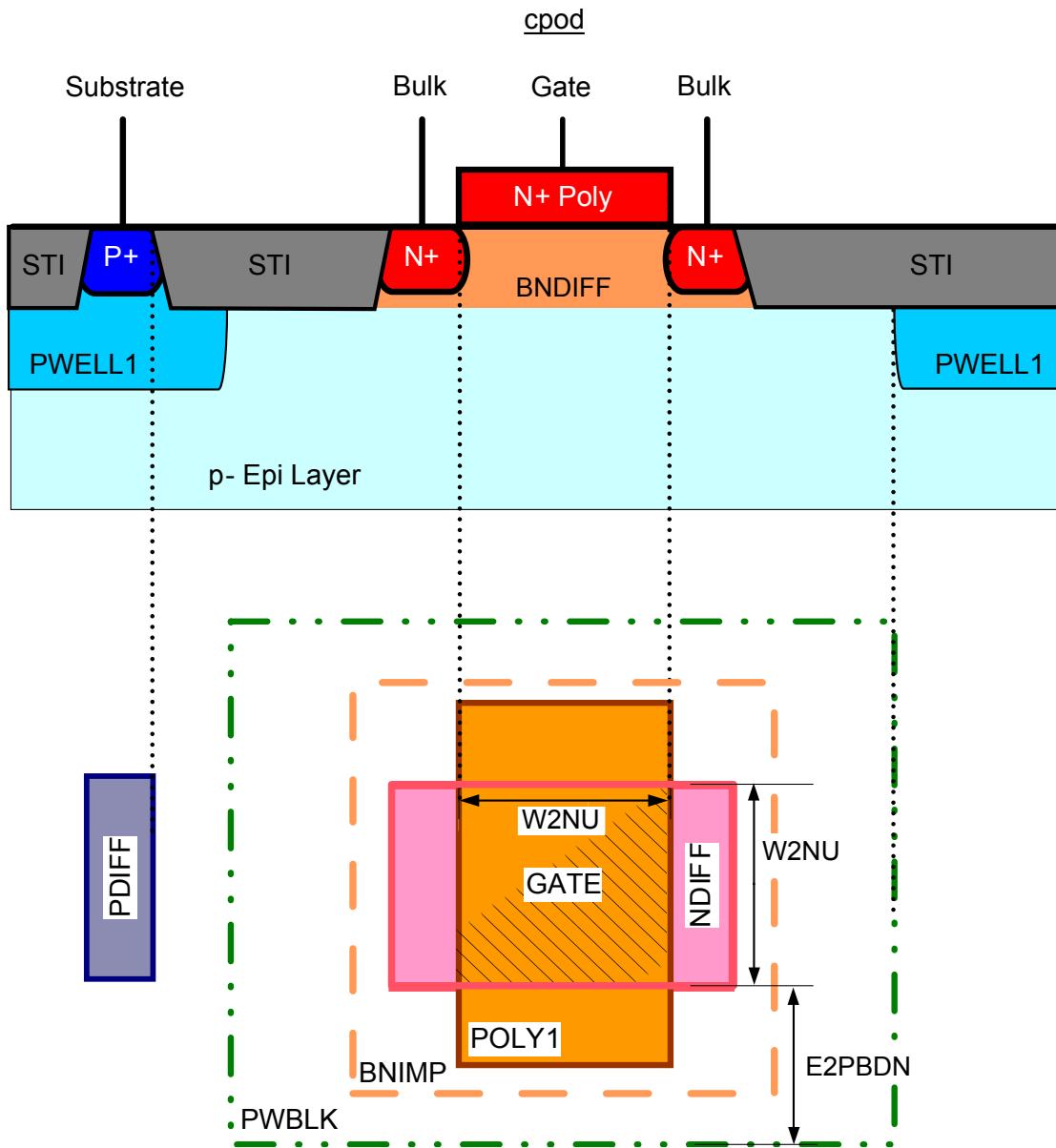


Figure 3.69 cpod

3. Layer and Device rules → 3.8 CPODHV module

3.8 CPODHV module

3.8.1 Layer rules

HVGDX

Name	Description	Value	Unit
B1GHMV	HVGDX overlap of MV is not allowed	-	-
B1GH	DIFF crossing HVGDX edge is not allowed	-	-
W1GH	Minimum HVGDX width	0.6	μm
S1GH	Minimum HVGDX spacing/notch	1.0	μm
S1GHDF	Minimum HVGDX spacing to DIFF	0.2	μm
E1GHDF	Minimum HVGDX enclosure of DIFF	0.2	μm

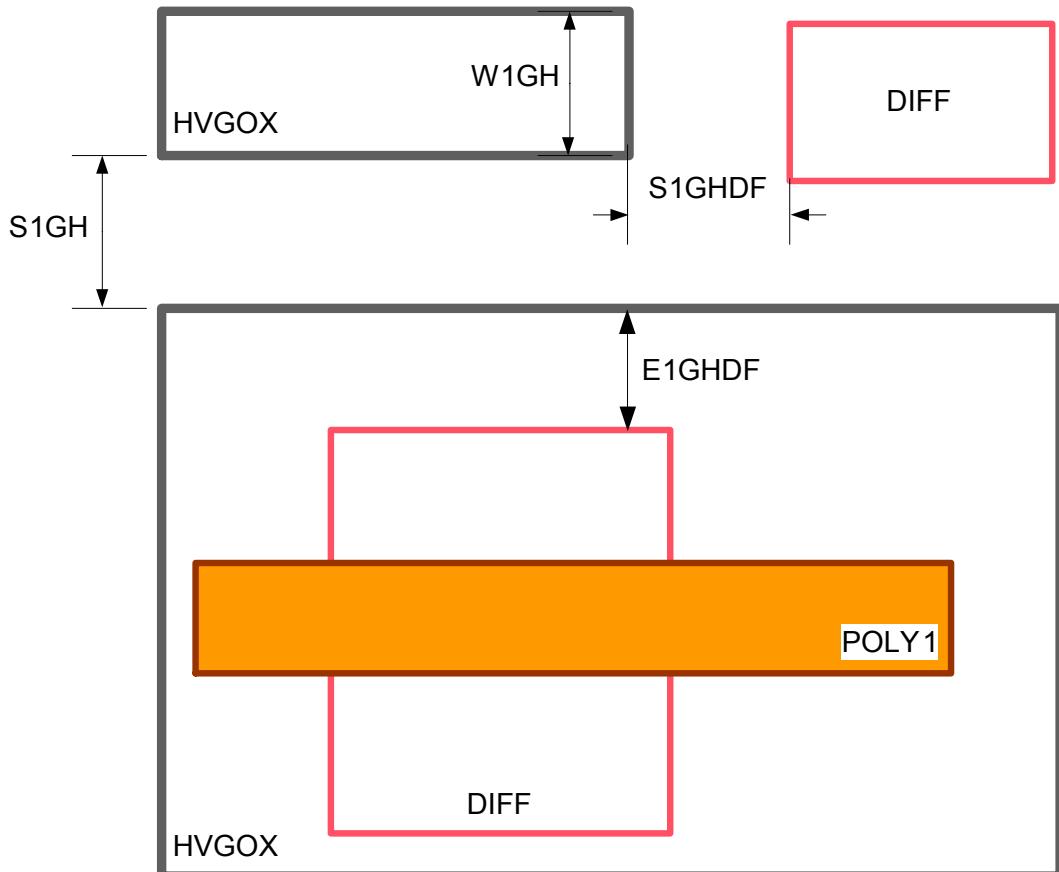


Figure 3.70 HVGDX

3. Layer and Device rules → 3.8 CPODHV module→ 3.8.2 Device rules→ cpodhv

3.8.2 Device rules

cpodhv

Name	Description	Value	Unit
B5NU	BNIMP without PWBLK is not allowed	-	-
W2NU	Minimum cpod# width	2.0	μm
E2PBDN	Fixed PWBLK enclosure of NDIFF	1.2	μm

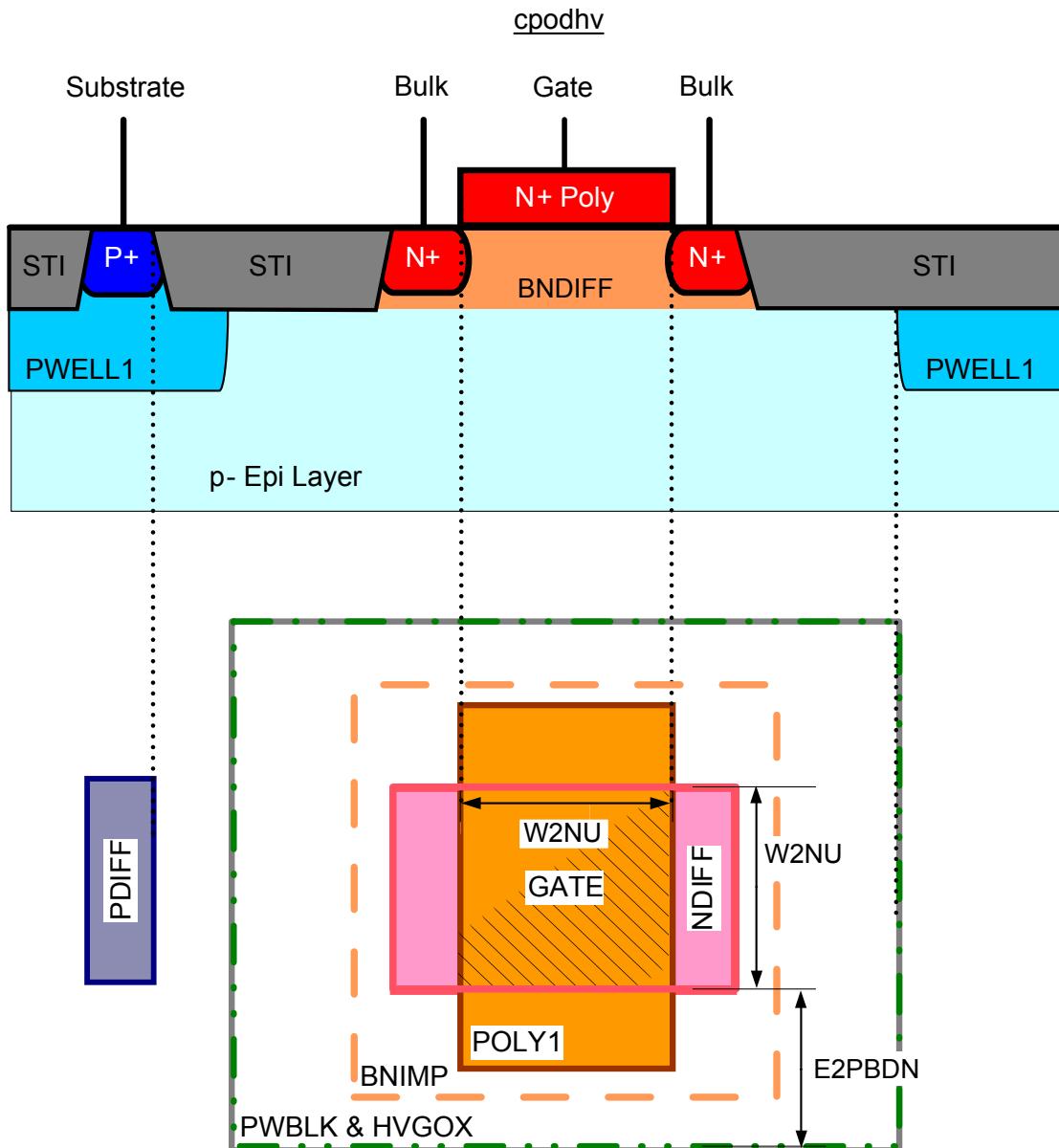


Figure 3.71 cpodhv

3. Layer and Device rules → 3.9 MRPOLY module

3.9 MRPOLY module

3.9.1 Layer rules

MRES

Name	Description	Value	Unit
B1MR	MRES overlap of DIFF is not allowed	-	-
B2MR	MRES without SBLK is not allowed	-	-
B3MR	MRES overlap of NIMP or PIMP is not allowed	-	-
B4MR	HRES overlap of MRES is not allowed	-	-
W1MR	Minimum MRES width	0.44	µm
S1MR	Minimum MRES spacing / notch	0.44	µm
S1MRDF	Minimum MRES spacing to DIFF	0.32	µm
S1MRP1	Minimum MRES spacing to POLY1	0.32	µm

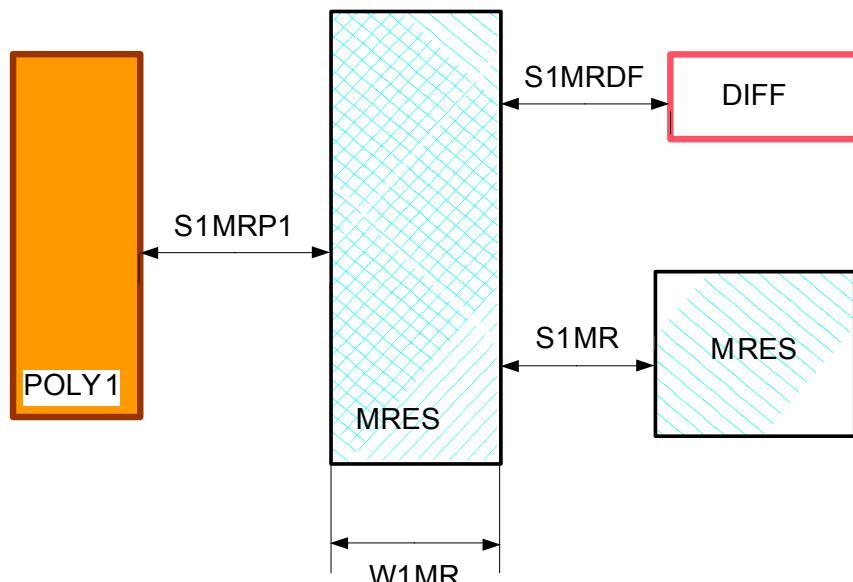


Figure 3.72 MRES

3. Layer and Device rules → 3.9 MRPOLY module → 3.9.2 Device rules → rpp1k1, rpp1k1_3

3.9.2 Device rules

rpp1k1, rpp1k1_3

Name	Description	Value	Unit
B7MR	rpp1k1_3 overlap of rnw/rnw3/rdnwmv is not allowed	-	-
B6MR	rpp1k1_3 crossing NTYPE_WELL or PTYPE_WELL or SUBCUT edge is not allowed	-	-
W16P1	Minimum rpp1k1# width	0.42	μm
S3INP1	Minimum NIMP spacing to rpp1k1# or rpp1k1_ext Note: The rpp1k1_ext area is defined as the (POLY1 and SBLK) area outside the resistor at the resistor terminals (see rpp1k1# drawing).	0.26	μm
E1MRP1	Minimum MRES extension beyond rpp1k1#	0.18	μm
E1SBMR	Fixed SBLK extension beyond MRES in direction of POLY1	0.22	μm
E2IPP1	Minimum PIMP extension beyond rpp1k1_ext Note: The rpp1k1_ext area is defined as the (POLY1 and SBLK) area outside the resistor at the resistor terminals (see rpp1k1# drawing).	0.18	μm

Note: CONT array for rpp1k1 and rpp1k1_3 resistors should be a single column.

Note: Do not use dog-bone at the end of rpp1k1 and rpp1k1_3 resistors for CONT pickup.

Note: Recommended minimum number of squares is L/W ≥ 5.

Note: rpp1k1# resistor definition: POLY1 and MRES.

Note: rpp1k1_3 device must be labeled “rpp1k1_3” using POLY1 (VERIFICATION) layer.

3. Layer and Device rules → 3.9 MRPOLY module→ 3.9.2 Device rules→ rpp1k1, rpp1k1_3

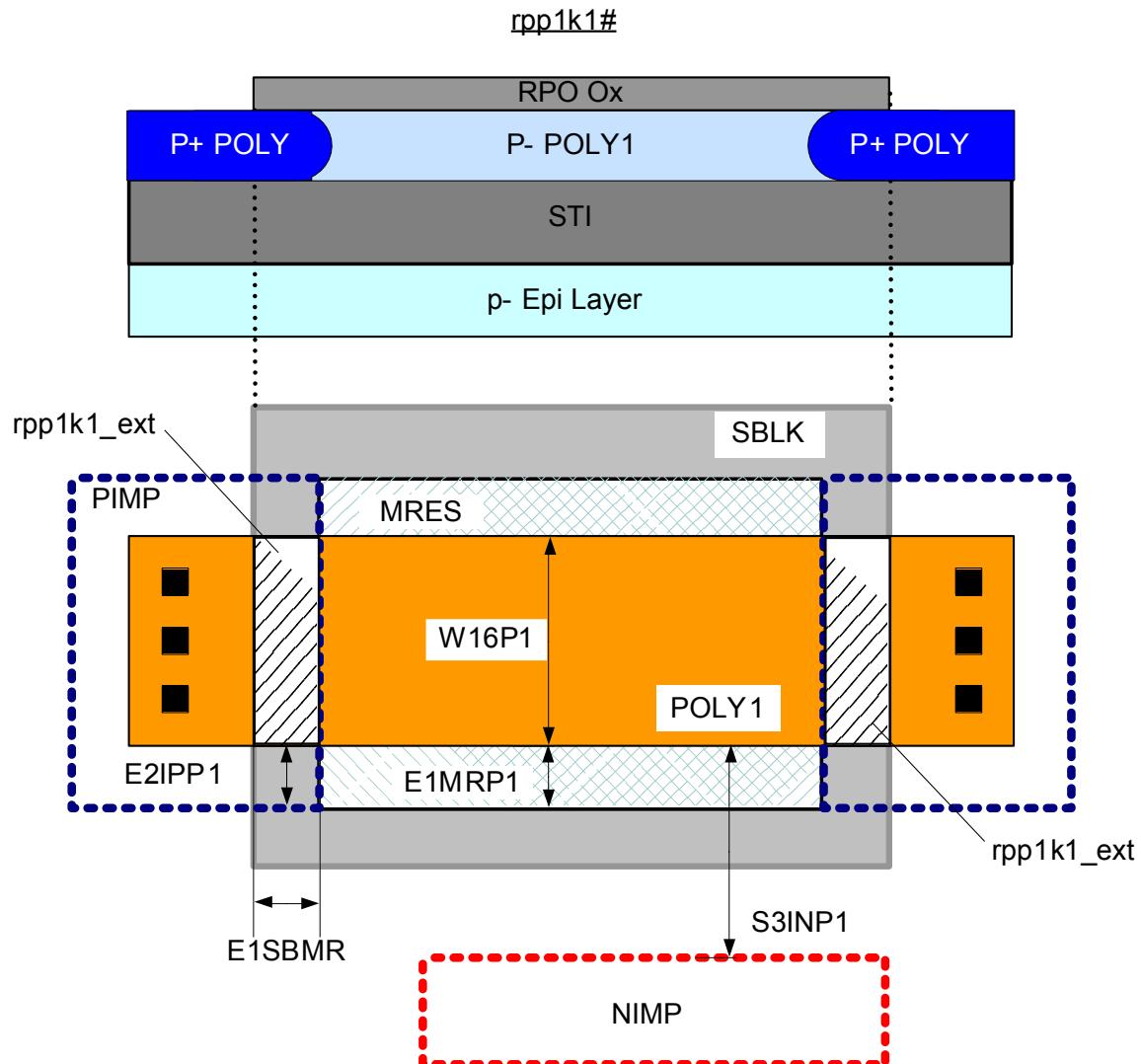


Figure 3.73 rpp1k1#

3. Layer and Device rules → 3.10 ISOMOS module

3.10 ISOMOS module

3.10.1 Layer rules

DNWELLMV

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1WM	DNWELLMV crossing DNWELL edge is not allowed	-	-
B2WM	NWELL crossing DNWELLMV edge is not allowed Note: Valid if DNWELLMV is outside DNWELL.	-	-
B6WM	HVPWELL crossing DNWELLMV edge is not allowed	-	-
B7WM	HVNWELL crossing DNWELLMV edge is not allowed	-	-
B8WM	POLY1 crossing DNWELLMV edge is not allowed Note: Valid if DNWELLMV is outside DNWELL.	-	-
W1WM	Minimum DNWELLMV width	1.6	μm
S1WM	Minimum DNWELLMV spacing/notch Note: Valid if DNWELLMV is outside DNWELL.	1.6	μm
S2WM	Minimum DNWELLMV spacing (different net) Note: Valid if DNWELLMV is outside DNWELL.	5.0	μm
S1WMDN	Minimum DNWELLMV spacing to NDIFF Note: Valid if DNWELLMV and NOT NWELL are outside DNWELL.	0.43	μm
S1WMDP	Minimum DNWELLMV spacing to PDIFF Note: Valid if DNWELLMV and NOT NWELL are outside DNWELL.	0.43	μm
S1WMHN	Minimum DNWELLMV spacing to HVNWELL Note: Valid if DNWELLMV is outside DNWELL.	8.0	μm
S1WMHP	Minimum DNWELLMV spacing to HVPWELL	3.0	μm
S1WMNW	Minimum DNWELLMV spacing to NWELL Note: Valid if DNWELLMV is outside DNWELL.	3.5	μm
S1WMP1	Minimum DNWELLMV spacing to POLY1 Note: Valid if DNWELLMV is outside DNWELL.	2.0	μm
S1WMWD	Minimum DNWELLMV spacing to DNWELL Note: Valid if DNWELLMV is outside DNWELL.	10.0	μm
E1WMDN	Minimum DNWELLMV enclosure of NDIFF Note: Valid if DNWELLMV and NOT NWELL are outside DNWELL.	0.43	μm
E1WMDP	Minimum DNWELLMV enclosure of PDIFF Note: Valid if DNWELLMV and NOT NWELL are outside DNWELL.	0.86	μm
E1WMHN	Minimum DNWELLMV enclosure of HVNWELL Note: Valid if DNWELLMV is outside DNWELL.	1.0	μm
E1WMHP	Minimum DNWELLMV enclosure of HVPWELL	2.0	μm
E1WMP1	Minimum DNWELLMV enclosure of POLY1 Note: Valid if DNWELLMV is outside DNWELL.	2.0	μm

3. Layer and Device rules → 3.10 ISOMOS module → 3.10.1 Layer rules → DNWELLMV

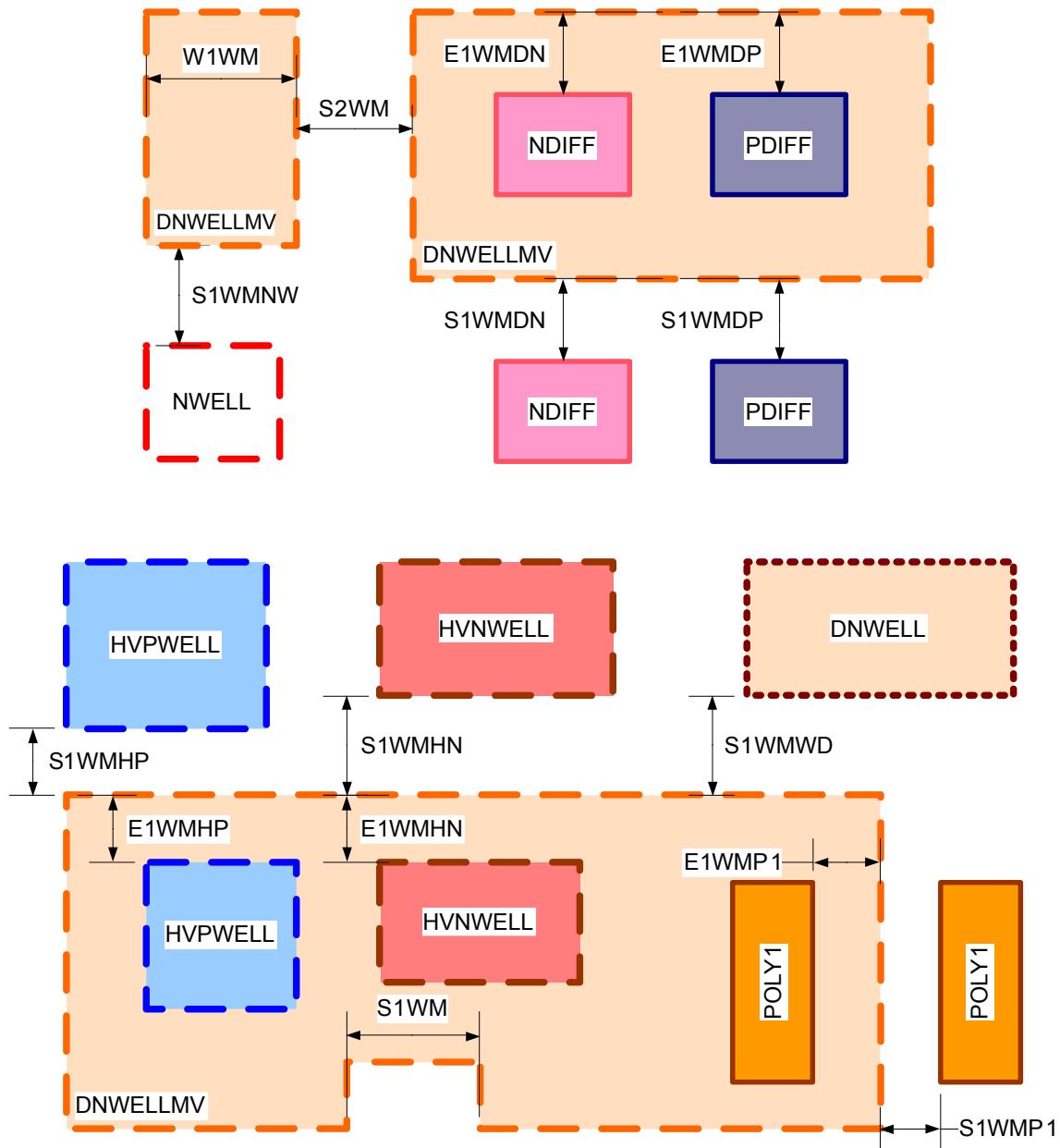


Figure 3.74 DNWELLMV

3. Layer and Device rules → 3.10 ISOMOS module→ 3.10.1 Layer rules→ ISOPW

ISOPW

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1PI	ISOPW outside DNWELLMV/DNWELL is not allowed (except qvhscr)	-	-
W1PI	Minimum ISOPW width	0.6	μm
S1PI	Minimum ISOPW spacing/notch	0.6	μm

Note: ISOPW may be drawn coincident with MV / LVT edge or with minimum spacing / enclosure defined by the NWELL1, PWELL1, NWELL2, PWELL2, NWELL3, PWELL3 rules.

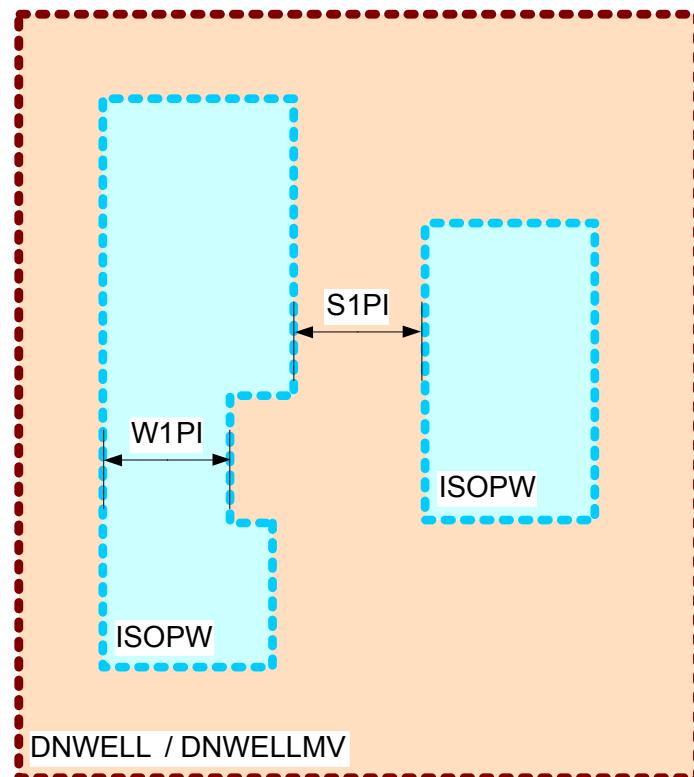


Figure 3.75 ISOPW

3. Layer and Device rules → 3.10 ISOMOS module→ 3.10.1 Layer rules→ ISOWELL

ISOWELL

Name	Description	Value	Unit
B1IW	ISOWELL overlap of NWELL, HVNWELL, HVPWELL or PDD is not allowed Note: Valid except on predefined devices nedia, qnva or qnvb.	-	-
B2IW	ISOWELL crossing DNWELLMV edge is not allowed	-	-
S1IW	Minimum ISOWELL spacing/notch	0.6	µm
S2IW	Minimum ISOWELL spacing (different net)	3.0	µm
S1IWDN	Minimum ISOWELL spacing to NDIFF Note: Valid except on predefined devices nedia or qnva.	0.43	µm
S1IWDP	Minimum ISOWELL spacing to PDIFF Note: Valid except on predefined devices nedia or qnva.	0.43	µm
S1IWHN	Minimum ISOWELL spacing to HVNWELL	0.8	µm
S1IWHP	Minimum ISOWELL spacing to HVPWELL	7.4	µm
S1IWPT	Minimum ISOWELL spacing to PDD Note: Valid except on predefined devices nedia or qnva.	8.0	µm
S2IWDN	Minimum ISOWELL spacing to NDIFF Note: Valid except on predefined devices nedia or qnva. Note: Valid outside DNWELLMV.	3.0	µm
S2IWDP	Minimum ISOWELL spacing to PDIFF Note: Valid except on predefined devices nedia or qnva. Note: Valid outside DNWELLMV.	3.0	µm
S2IWHN	Minimum ISOWELL spacing to HVNWELL Note: Valid outside DNWELLMV.	3.0	µm
E1IWDN	Minimum ISOWELL enclosure of NDIFF Note: Valid except on predefined devices nedia or qnva.	0.43	µm
E1IWDP	Minimum ISOWELL enclosure of PDIFF Note: Valid except on predefined devices nedia or qnva.	0.43	µm
E1WMIW	Minimum DNWELLMV enclosure of ISOWELL Note: Valid outside DNWELL.	2.0	µm
E2IWDN	Minimum ISOWELL enclosure of NDIFF Note: Valid except on predefined devices nedia or qnva. Note: Valid outside DNWELLMV.	3.5	µm
E2IWDP	Fixed ISOWELL enclosure of PDIFF Note: Valid except on predefined devices nedia or qnva. Note: Valid outside DNWELLMV.	3.0	µm
Q1IW	ISOWELL should be contacted by PDIFF	-	-

Note: ISOWELL may be drawn coincident with MV / LVT edge or with minimum spacing / enclosure defined by the NWELL1, PWELL1, NWELL2, PWELL2, NWELL3, PWELL3 rules.

3. Layer and Device rules → 3.10 ISOMOS module → 3.10.1 Layer rules → ISOWELL

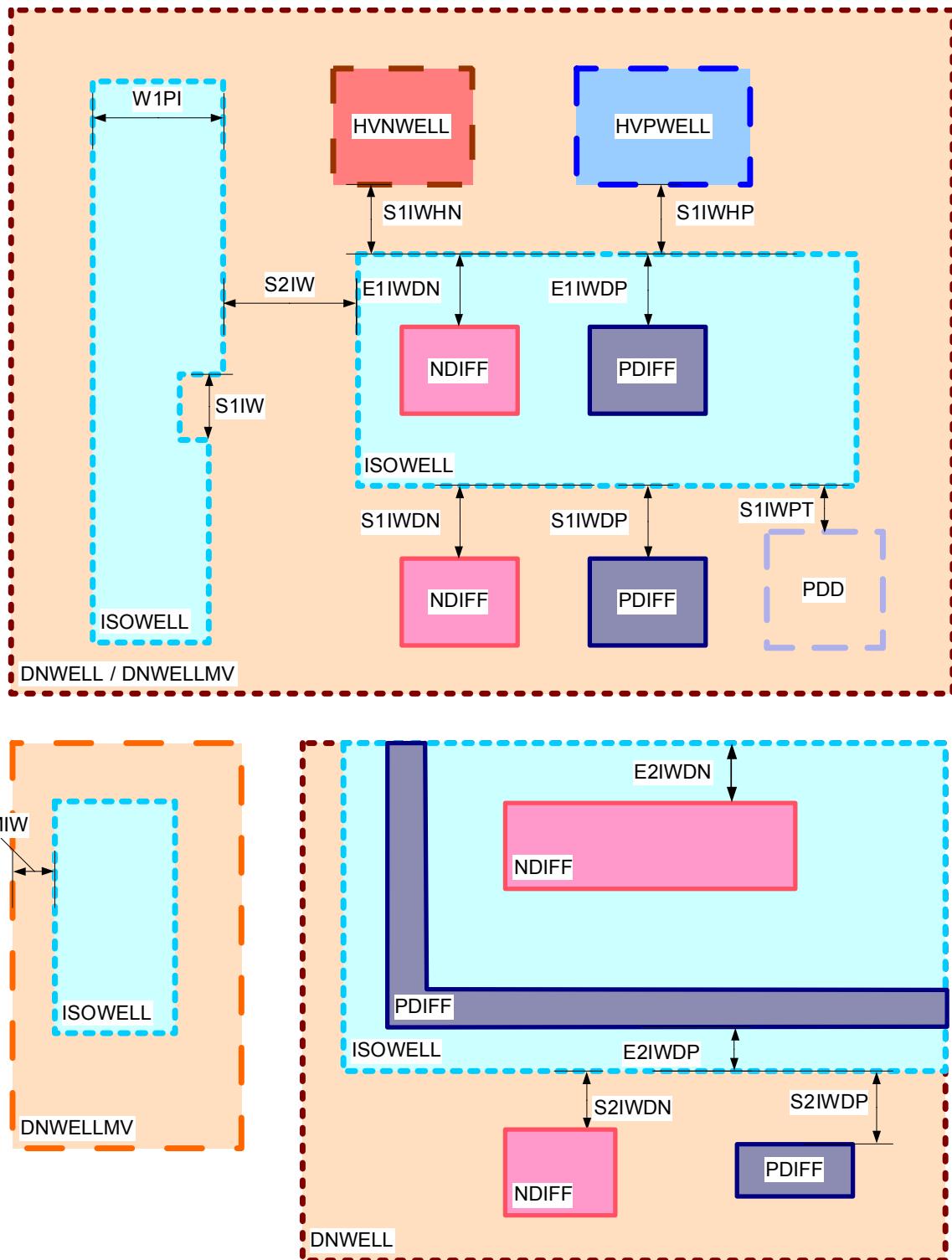


Figure 3.76 ISOWELL

3. Layer and Device rules → 3.10 ISOMOS module→ 3.10.2 Device rules→ nei, pei

3.10.2 Device rules

nei, pei

Name	Description	Value	Unit
W3DF	Minimum GATE width	0.22	μm
	Note: The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) having smaller GATE width than 0.22μm.		
W4P1	Minimum GATE length	0.18	μm
	Note: The design rule check error message W4P1 is also used generally for GATE areas (of any devices or shapes) being smaller than 0.18μm at any dimension.		

Note: For more extensive LVS, it is recommended to use the related 5 or 6 terminal device.

Note: nei and pei may be placed in DNWELLMV or DNWELL. Please take care of the different well edge design rules for both cases. For DNWELL the ISOMOS2 or HVMOS Module is needed. (Drawing on this page is only for nei and pei in DNWELLMV)

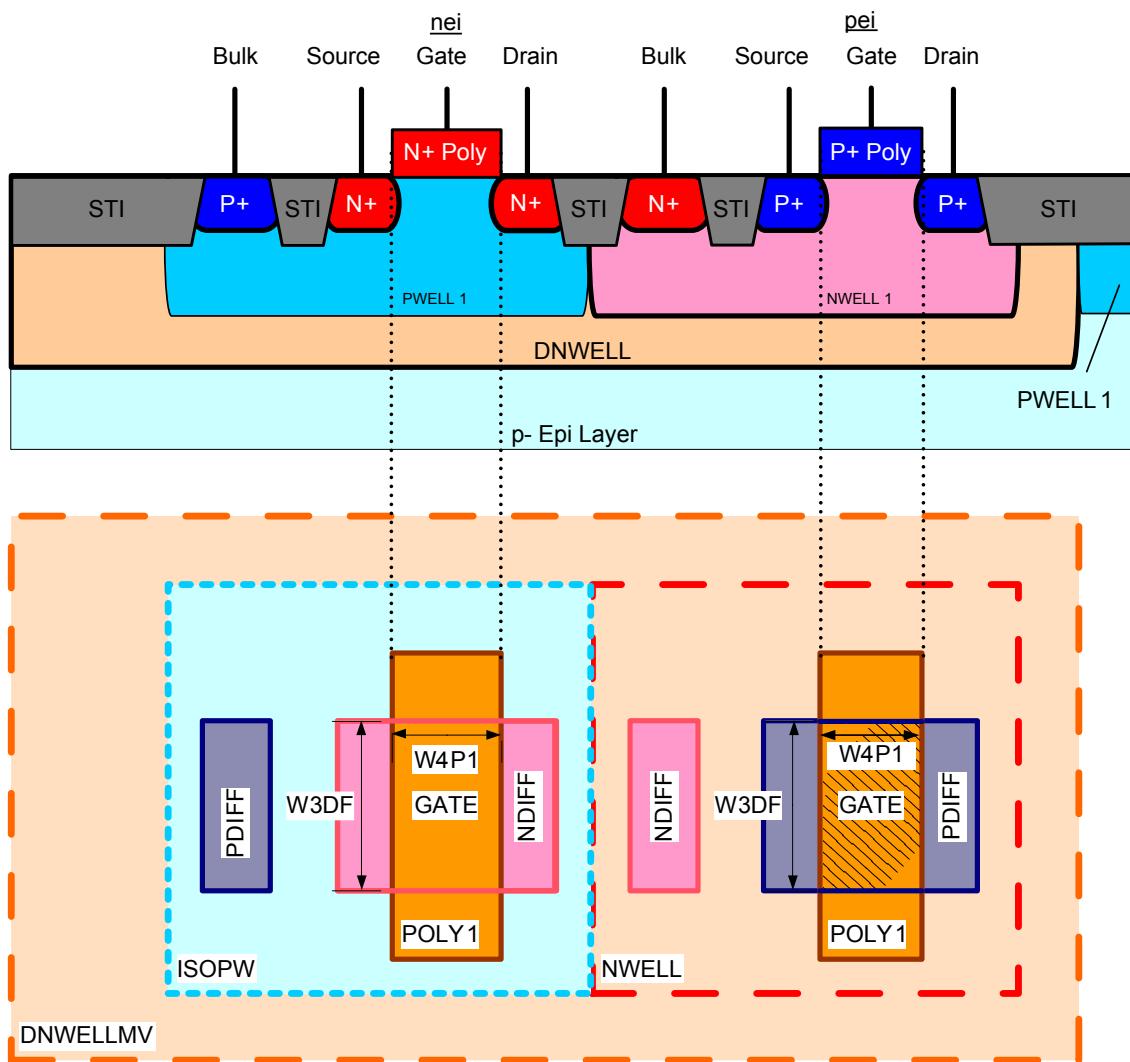


Figure 3.77 nei, pei

3. Layer and Device rules → 3.10 ISOMOS module→ 3.10.2 Device rules→ nei_m_6

nei_m_6

Name	Description	Value	Unit
W3DF	Minimum GATE width	0.22	μm
	Note: The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) having smaller GATE width than 0.22μm.		
W4P1	Minimum GATE length	0.18	μm
	Note: The design rule check error message W4P1 is also used generally for GATE areas (of any devices or shapes) being smaller than 0.18μm at any dimension.		

Note: nei_m_6 device must be labeled “6T” using POLY1 (VERIFICATION) layer over the GATE.

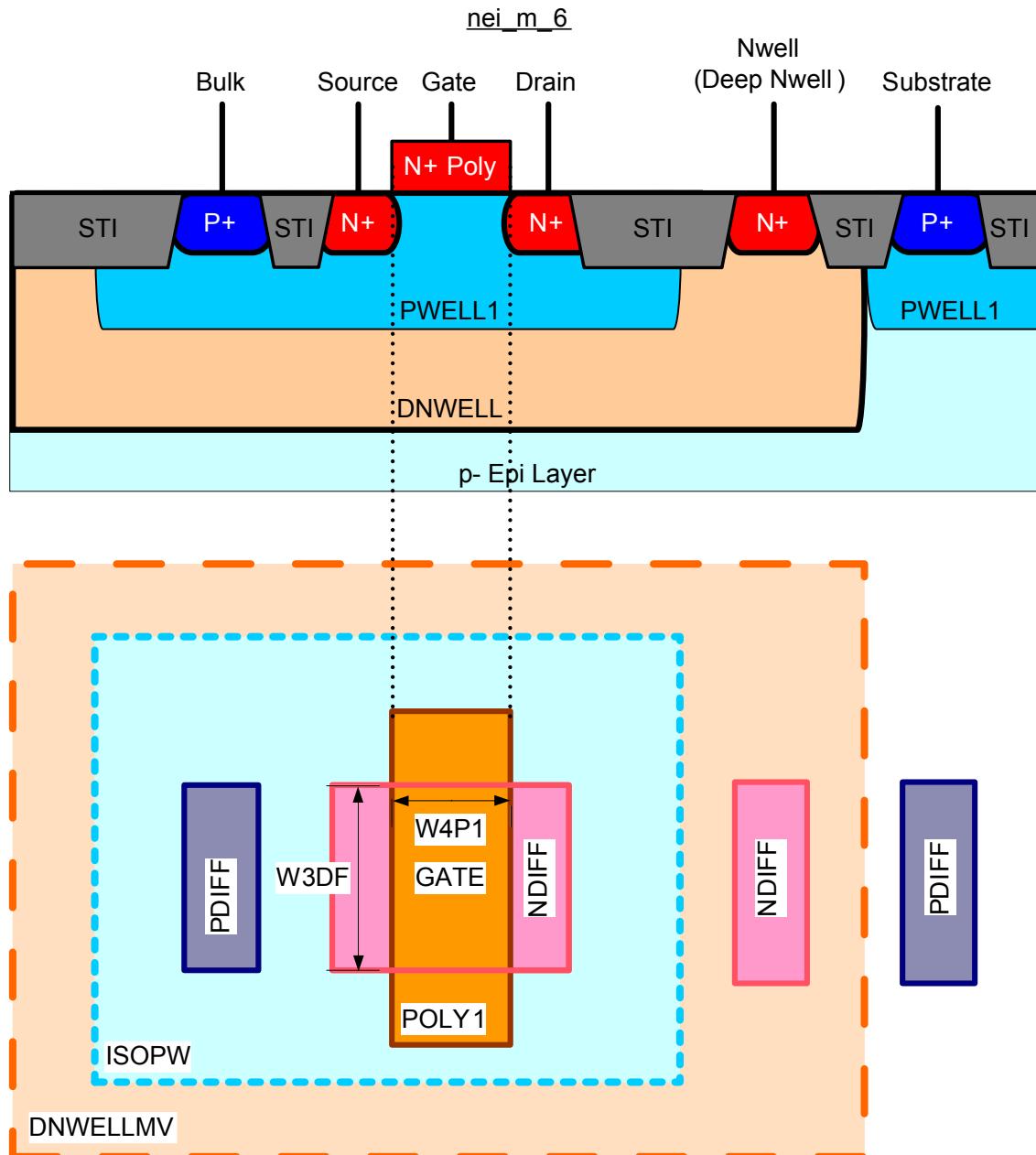


Figure 3.78 nei_m_6

3. Layer and Device rules → 3.10 ISOMOS module→ 3.10.2 Device rules→ pei_m_5

pei_m_5

Name	Description	Value	Unit
W3DF	Minimum GATE width	0.22	μm
	Note: The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) having smaller GATE width than 0.22μm.		
W4P1	Minimum GATE length	0.18	μm
	Note: The design rule check error message W4P1 is also used generally for GATE areas (of any devices or shapes) being smaller than 0.18μm at any dimension.		

Note: pei_m_5 device must be labeled “5T” using POLY1 (VERIFICATION) layer over the GATE.

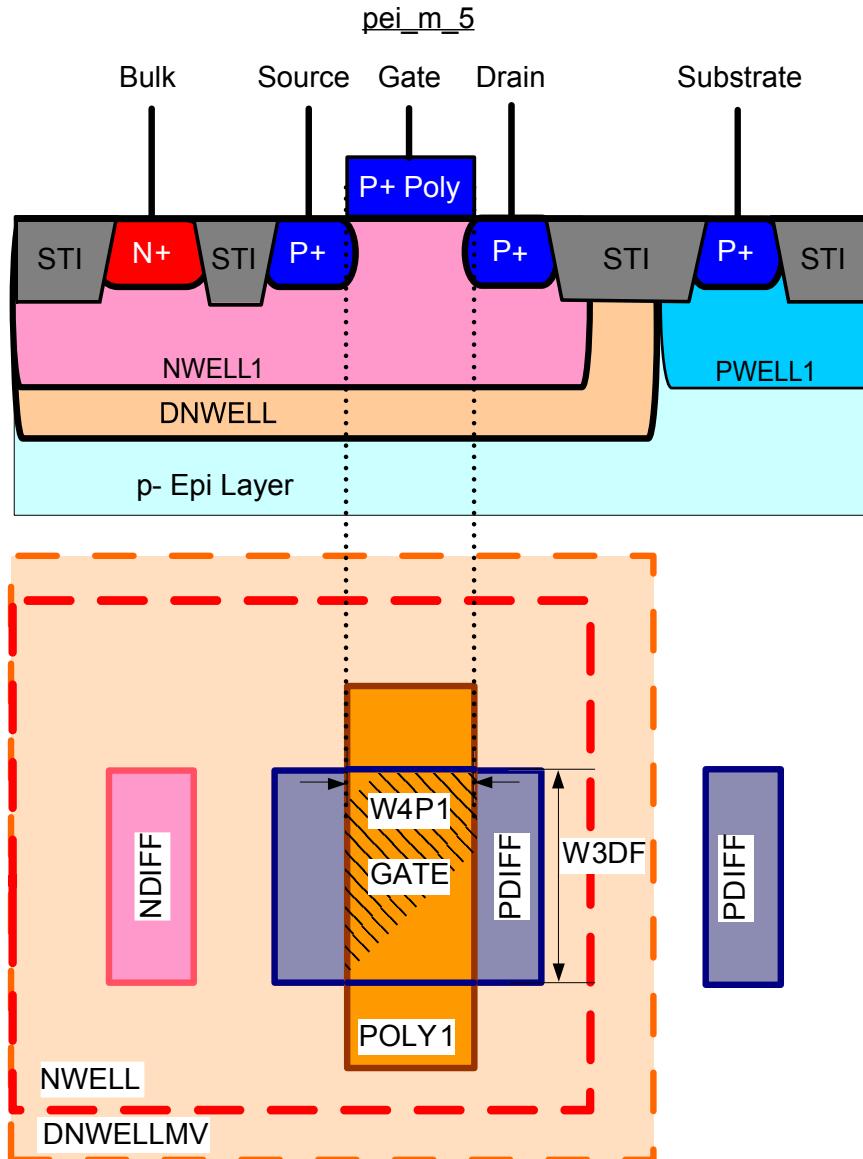


Figure 3.79 pei_m_5

3. Layer and Device rules → 3.10 ISOMOS module→ 3.10.2 Device rules→ ne3i, pe3i

ne3i, pe3i

Name	Description	Value	Unit
W3DF	Minimum GATE width	0.22	μm
	Note: The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) having smaller GATE width than 0.22μm.		
W6P1	Minimum GATE length	0.35	μm
W7P1	Minimum GATE length	0.3	μm

Note: MV is necessary for ne3i and pe3i.

Note: ne3i and pe3i may be placed in DNWELLMV or DNWELL. Please take care of the different well edge design rules for both cases. For DNWELL the HVMOS Module is needed. (Drawing on this page is only for ne3i and pe3i in DNWELLMV)

Note: For more extensive LVS, it is recommended to use the related 5 or 6 terminal device.

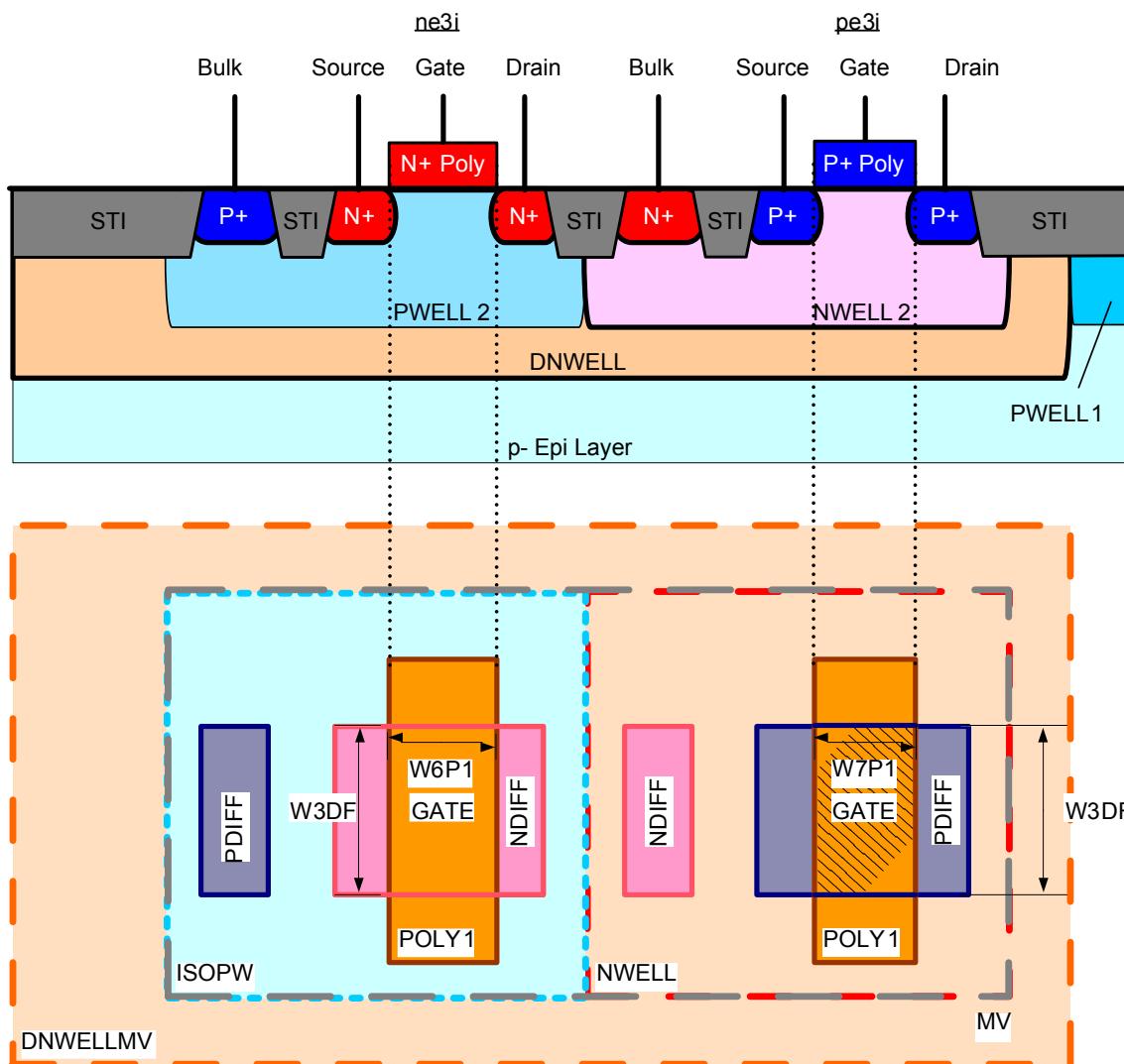


Figure 3.80 ne3i, pe3i

3. Layer and Device rules → 3.10 ISOMOS module→ 3.10.2 Device rules→ ne3i_m_6

ne3i_m_6

Name	Description	Value	Unit
W3DF	Minimum GATE width	0.22	μm
	Note: The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) having smaller GATE width than 0.22μm.		
W6P1	Minimum GATE length	0.35	μm

Note: MV is necessary for ne3i_m_6.

Note: ne3i_m_6 devices must be labeled “6T” using POLY1 (VERIFICATION) layer over the GATE.

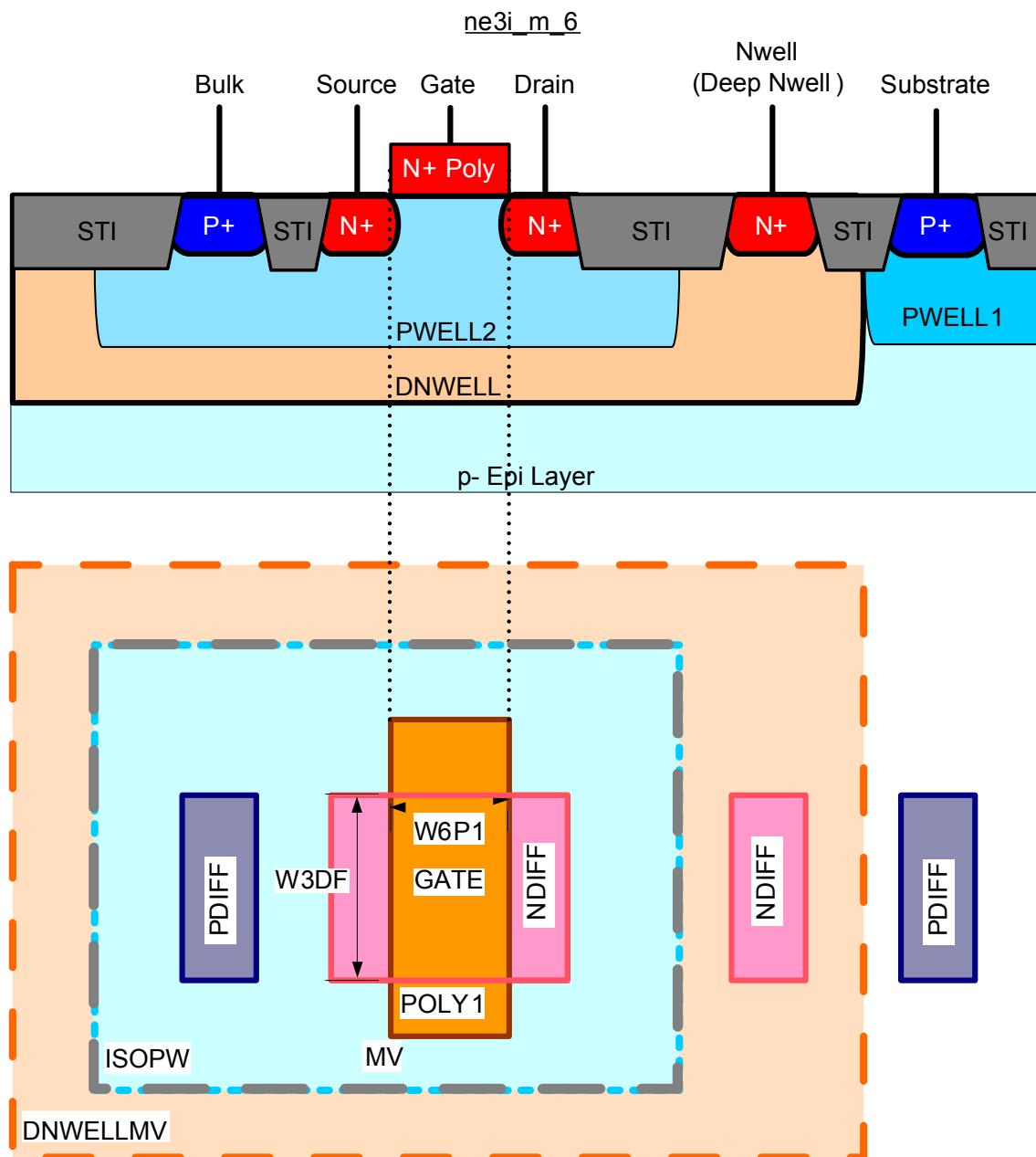


Figure 3.81 ne3i_m_6

3. Layer and Device rules → 3.10 ISOMOS module→ 3.10.2 Device rules→ pe3i_m_5

pe3i_m_5

Name	Description	Value	Unit
W3DF	Minimum GATE width	0.22	μm
	Note: The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) having smaller GATE width than 0.22μm.		
W7P1	Minimum GATE length	0.3	μm

Note: pe3i_m_5 device must be labeled “5T” using POLY1 (VERIFICATION) layer over the GATE.

Note: MV is necessary for pe3i_m_5.

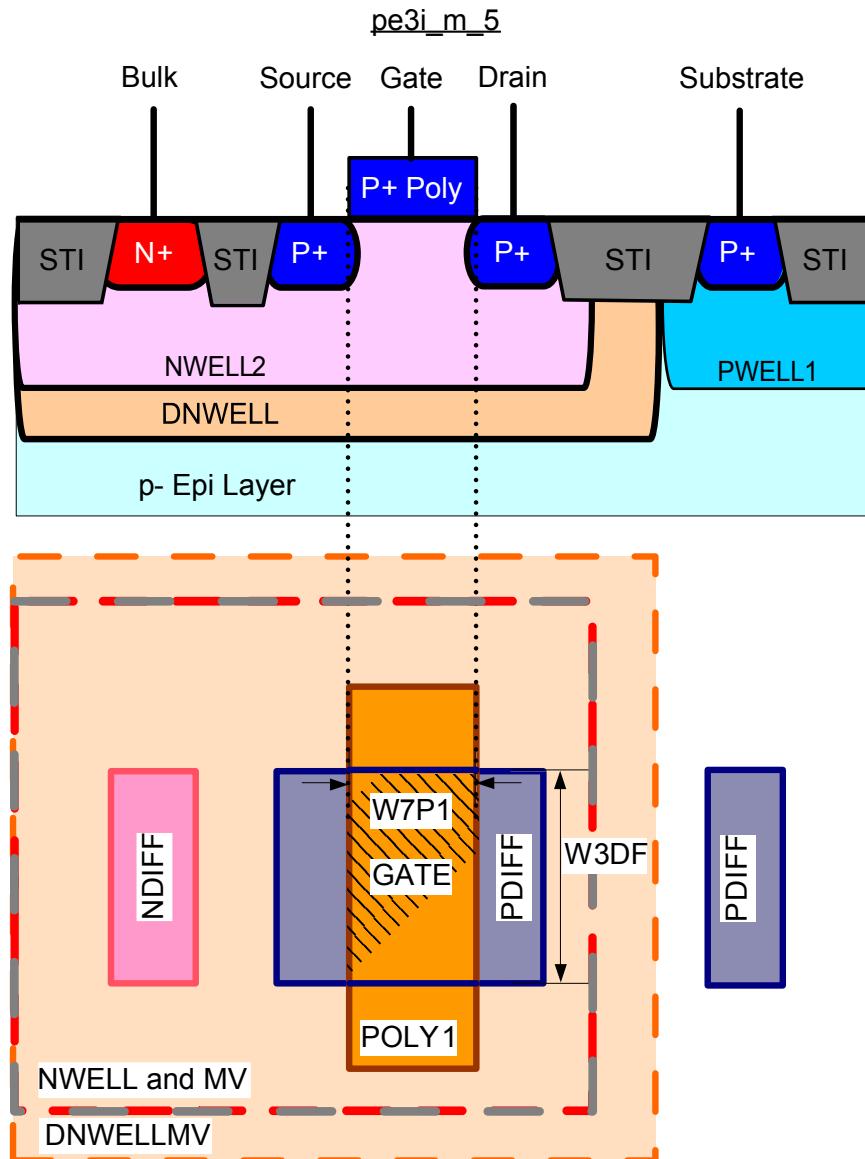


Figure 3.82 pe3i_m_5

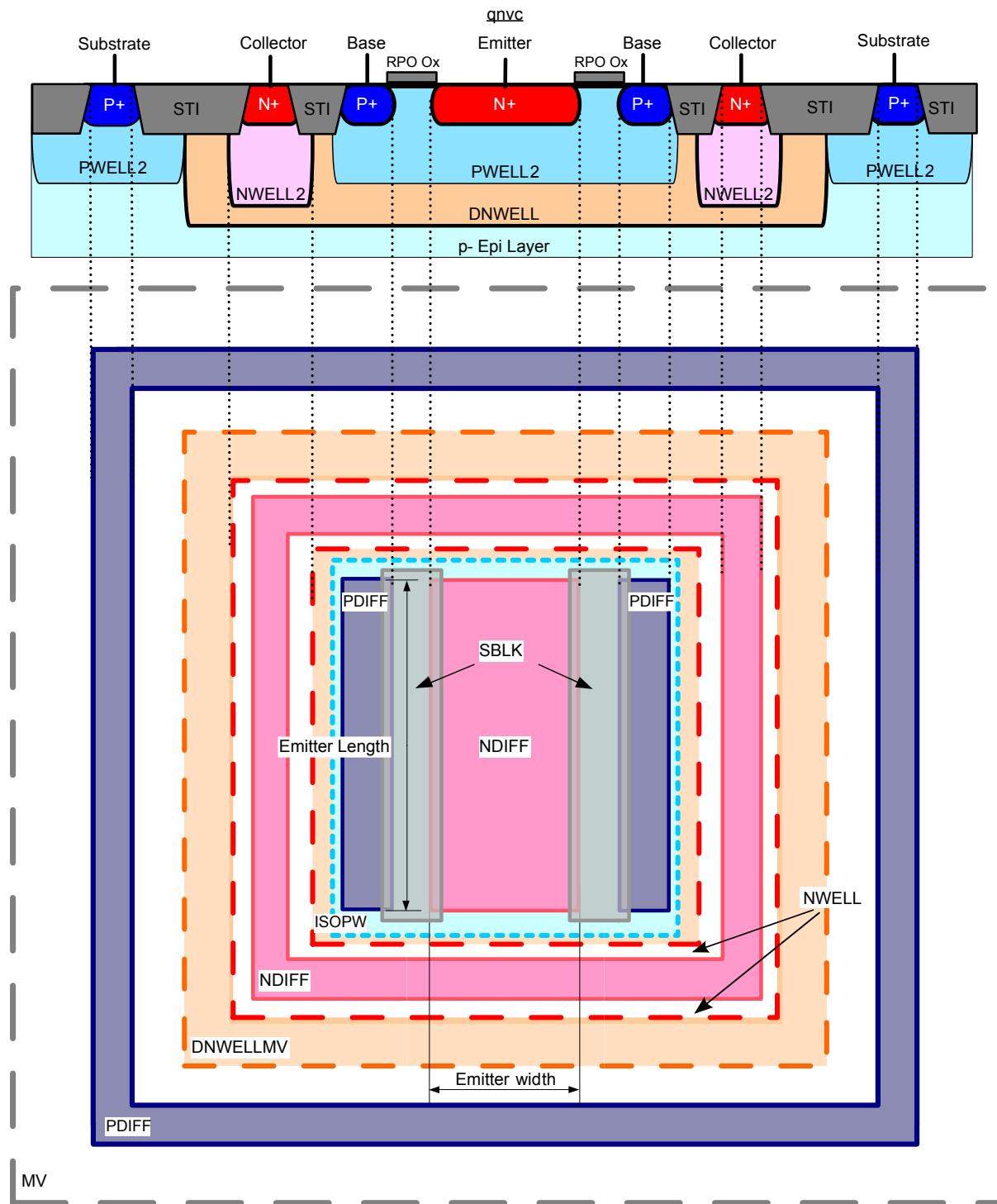
3. Layer and Device rules → 3.10 ISOMOS module→ 3.10.2 Device rules→ qnvc

qnvc

Name	Description	Value	Unit
B7WD	qnvc inside DNWELL is not allowed	-	-
E1MVWM	Minimum MV enclosure of DNWELLMV	0.6	μm

Note: The layout of the qnvc vertical bipolar NPN transistor is pre-defined and only the emitter length can be changed in the range of 3μm to 50μm. The drawing below is a basic sketch only and does not give all details.

Note: MV is necessary for qnvc.

**Figure 3.83 qnvc**

3. Layer and Device rules → 3.10 ISOMOS module→ 3.10.2 Device rules→ rdnwmv

rdnwmv

Name	Description	Value	Unit
B4GH	HVGDX overlap of rdnwmv is not allowed	-	-
B4WM	DNWMV_VERIFY overlap of NWELL, DNWELL or HVNWELL is not allowed	-	-
B5WM	DNWMV_VERIFY overlap of DIFF is not allowed	-	-
	Note: DNWMV_VERIFY edge must touch rdnwmv NDIFF-contact edge.		
B9WM	DNWMV_VERIFY overlap of ISOPW, DEPL, SCI, HVPWELL, PDF or PDD is not allowed	-	-
W2WM	Minimum rdnwmv width	2.0	μm

Note: Recommended minimum number of squares is L/W ≥ 5.

Note: rdnwmv resistor definition: DNWELLMV and DNWMV_VERIFY.

Note: It is recommended to place DIFF stripes close to resistor.

Note: Recommended maximum width is 10μm.

3. Layer and Device rules → 3.10 ISOMOS module → 3.10.2 Device rules → rdnwmv

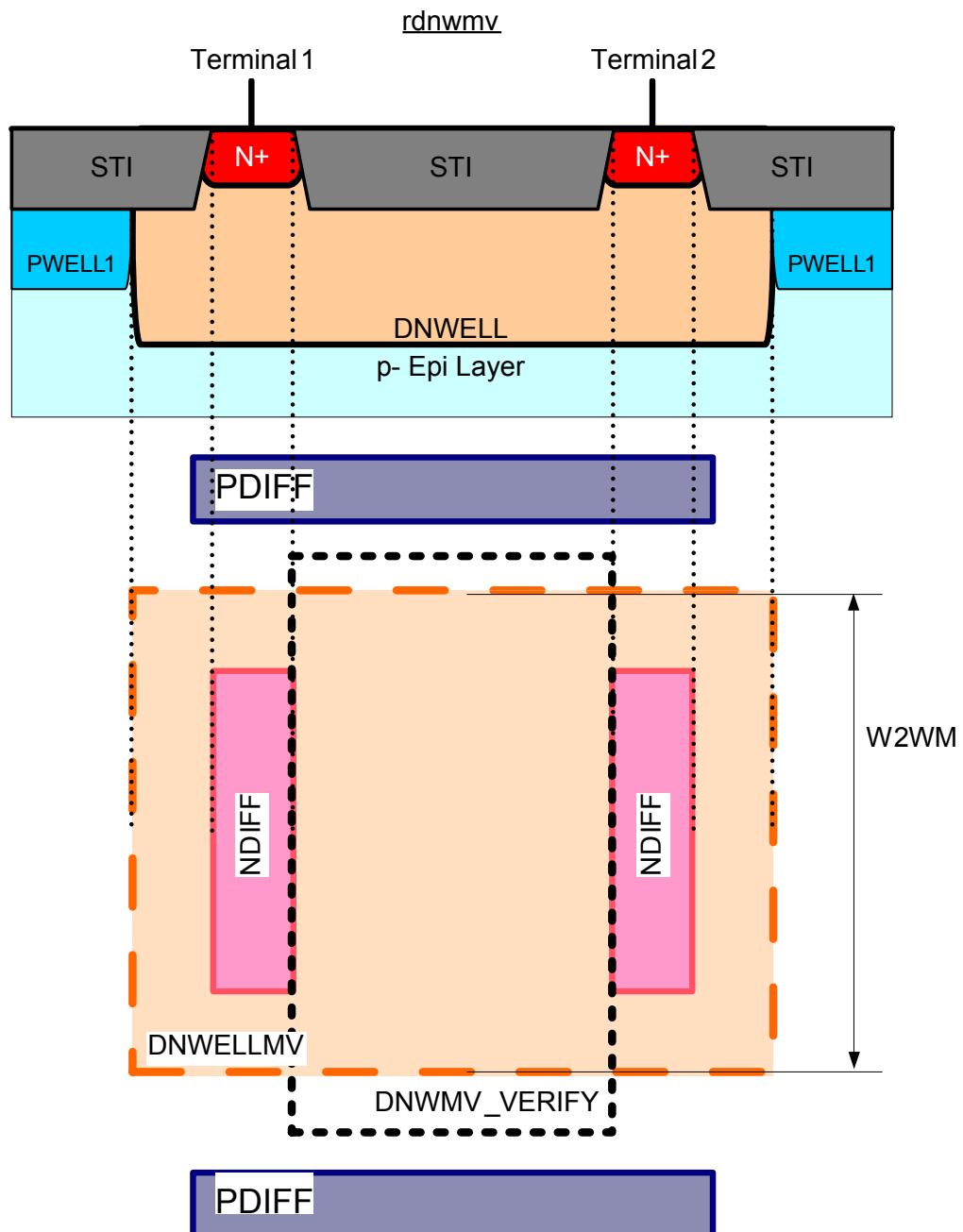


Figure 3.84 rdnwmv

3. Layer and Device rules → 3.10 ISOMOS module→ 3.10.2 Device rules→ mosvc3i_m

mosvc3i_m

Name	Description	Value	Unit
B4GA	Only rectangular GATE is allowed	-	-
W38GA	Minimum GATE length	2.0	μm
W39GA	Minimum GATE width	2.0	μm

Note: MV is necessary for mosvc3i_m.

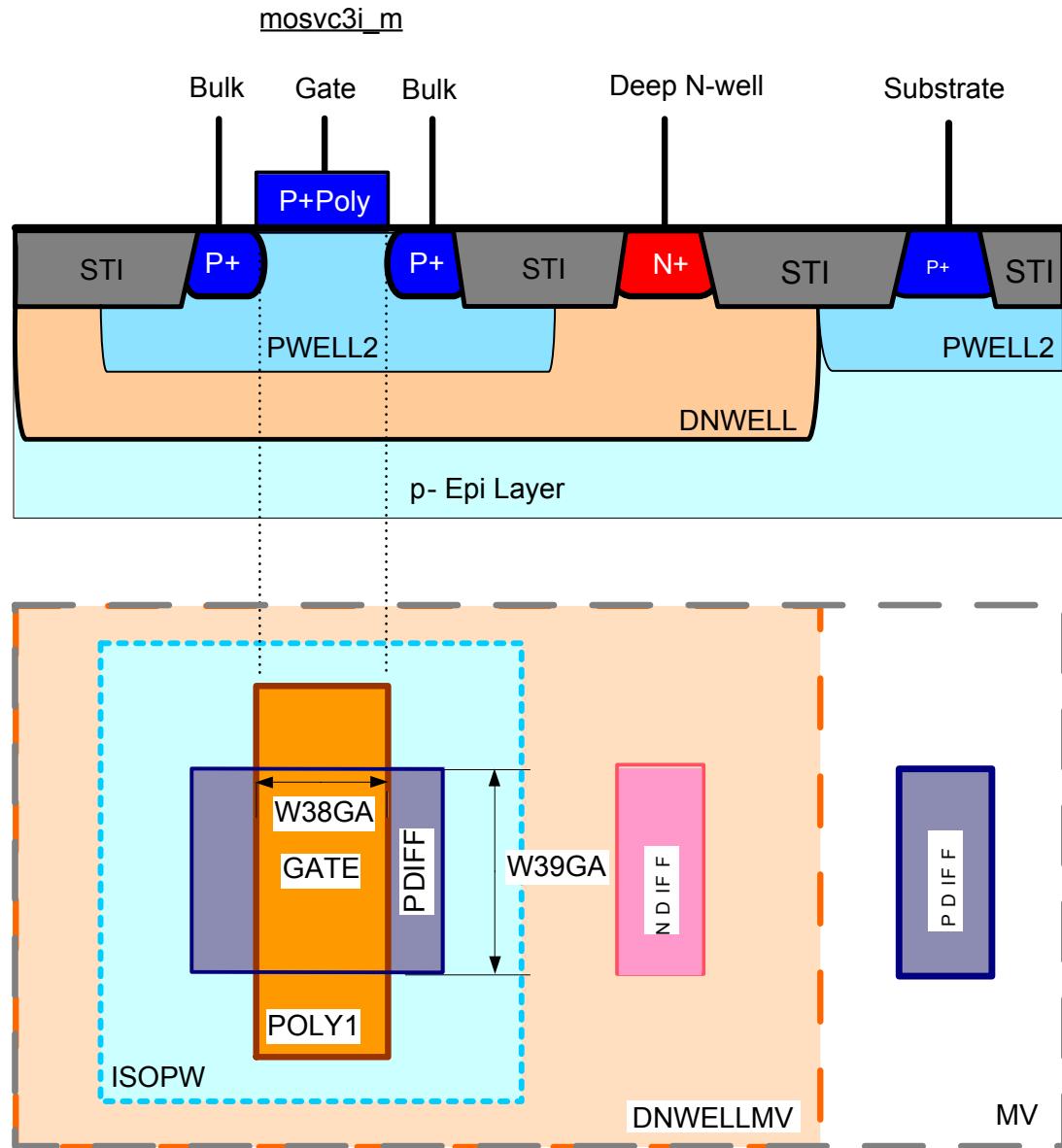


Figure 3.85 mosvc3i_m

3. Layer and Device rules → 3.10 ISOMOS module→ 3.10.2 Device rules→ mosvci_m

mosvci_m

Name	Description	Value	Unit
B4GA	Only rectangular GATE is allowed	-	-
W38GA	Minimum GATE length	2.0	μm
W39GA	Minimum GATE width	2.0	μm

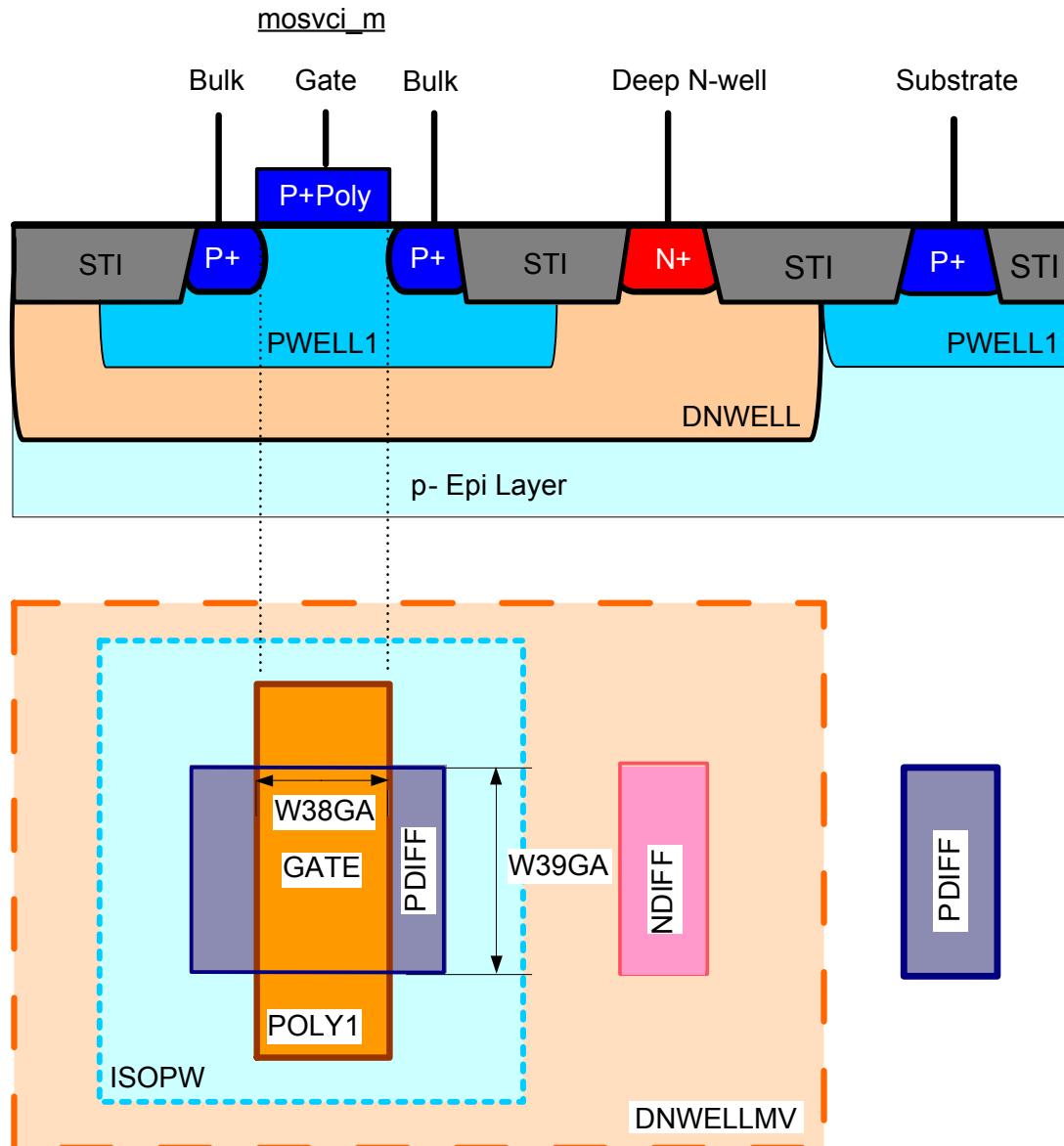


Figure 3.86 mosvci_m

3. Layer and Device rules → 3.10 ISOMOS module→ 3.10.2 Device rules→ ddnwmv, dpdnwmv, dip...

ddnwmv, dpdnwmv, dipdnwmv

Note: The layer DIODEF must enclose the pn junction, crossing the pn junction is not allowed.

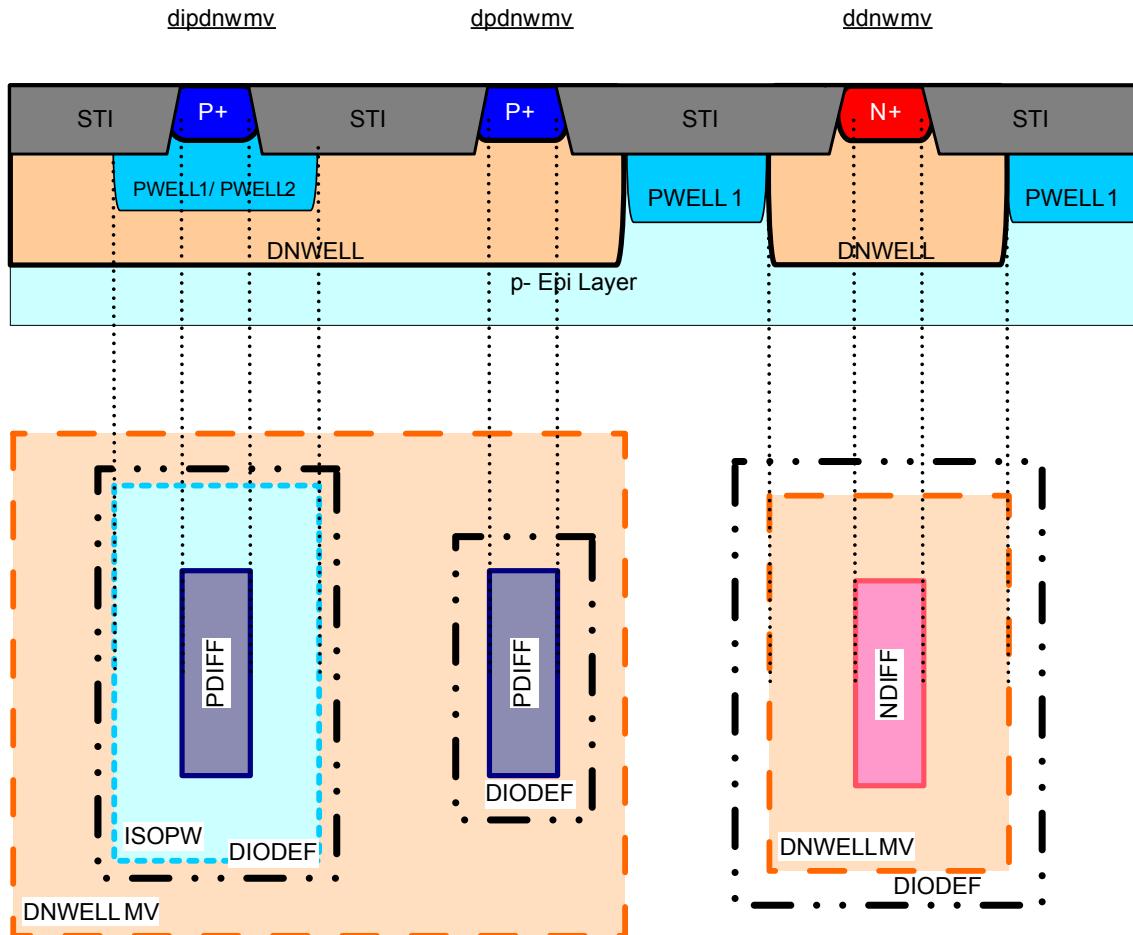


Figure 3.87 ddnwmv, dpdnwmv, dipdnwmv

3. Layer and Device rules → 3.11 ISOMOS2 module

3.11 ISOMOS2 module

3.11.1 Layer rules

DNWELL

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1WD	DNWELL must be surrounded by a GUARD RING consisting of PDIFF and HVPWELL	-	-
B3WD	NWELL crossing DNWELL edge is not allowed	-	-
W1WD	Minimum DNWELL width	6.44	µm
S1WD	Minimum DNWELL spacing/notch	10.0	µm
S1P1WD	Minimum POLY1 spacing to DNWELL	5.35	µm
S1WDDN	Minimum DNWELL spacing to NDIFF	4.23	µm
S1WDDP	Fixed DNWELL spacing to PDIFF	4.0	µm
S1WDHN	Minimum DNWELL spacing to HVNWELL	10.0	µm
S1WDHP	Minimum DNWELL spacing to HVPWELL	3.75	µm
S1WDNW	Minimum DNWELL spacing to NWELL	10.0	µm
E1PBWD	Fixed PWBLK enclosure of DNWELL (min. spacing DNWELL to generated Pwells)	4.0	µm
E1WDDN	Fixed DNWELL enclosure of NDIFF (except ned#, ped#)	3.0	µm
Note: NDIFF must be the DNWELL contact.			
E1WDDP	Minimum DNWELL enclosure of PDIFF	3.5	µm
E1WDHN	Minimum DNWELL enclosure of HVNWELL (except pmma, qpvascr)	3.65	µm
E1WDNW	Minimum DNWELL enclosure of NWELL	3.65	µm
E1WDP1	Minimum DNWELL enclosure of POLY1	3.95	µm
E1WDWM	Minimum DNWELL enclosure of DNWELLMV	3.0	µm
E2WDHN	Minimum DNWELL enclosure of HVNWELL	2.76	µm

Note: Rules for DNWELLMV layer are described under DNWELLMV section.

3. Layer and Device rules → 3.11 ISOMOS2 module → 3.11.1 Layer rules → DNWELL

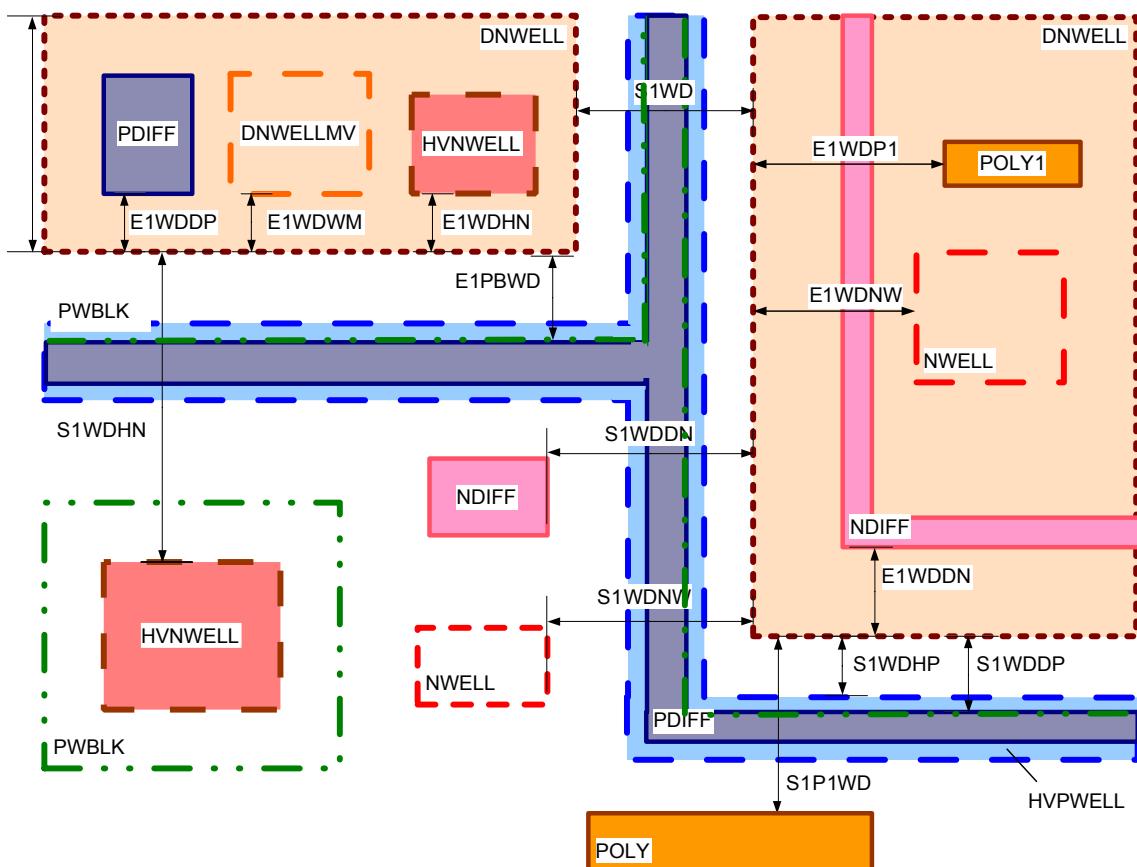


Figure 3.88 DNWELL

3. Layer and Device rules → 3.11 ISOMOS2 module→ 3.11.1 Layer rules→ HVPWELL

HVPWELL

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1HP	HVPWELL must be contacted by PDIFF	-	-
B3HP	HVPWELL overlap of NWELL is not allowed	-	-
B5HP	HVPWELL overlap of DNWELL is not allowed Note: Valid inside DNWELLMV.	-	-
B2HP	DIFF crossing HVPWELL edge is not allowed (except ped, ned#, nm#, nh#, pmma, nmma)	-	-
B4HP	HVPWELL crossing DNWELL edge is not allowed	-	-
W1HP	Minimum HVPWELL width	0.9	μm
S1HP	Minimum HVPWELL spacing/notch	0.6	μm
S2HP	Minimum HVPWELL spacing (different net) Note: Not valid for channel region of pmma GATE (oversized by 0.43 μm).	3.0	μm
S1HPDN	Minimum HVPWELL spacing to NDIFF (except ned#)	0.43	μm
S1HPDP	Minimum HVPWELL spacing to PDIFF	0.43	μm
S1HPNW	Minimum HVPWELL spacing to NWELL Note: Valid inside DNWELLMV.	0.8	μm
S2HPDN	Fixed HVPWELL spacing to NDIFF (except ned#, ped#, qpvascr) Note: Valid inside DNWELL and NOT DNWELLMV.	3.0	μm
S2HPNW	Minimum HVPWELL spacing to NWELL Note: Valid inside DNWELL and NOT DNWELLMV.	3.0	μm
E1HPDN	Minimum HVPWELL enclosure of NDIFF	0.43	μm
E1HPDP	Minimum HVPWELL enclosure of PDIFF (except ped#, pmma, nmma) Note: Valid inside DNWELLMV/DNWELL.	0.43	μm

3. Layer and Device rules → 3.11 ISOMOS2 module → 3.11.1 Layer rules→ HVPWELL

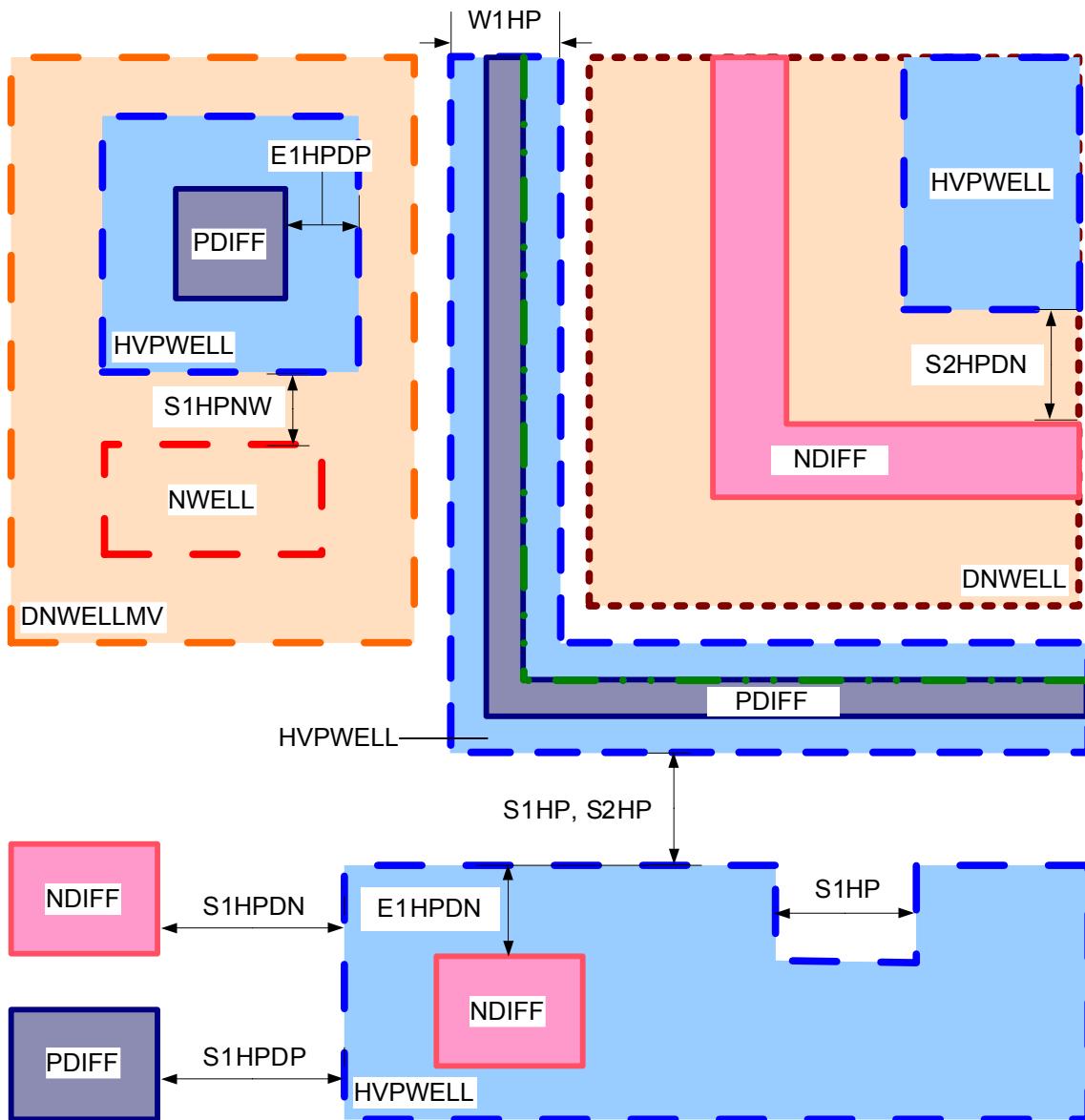


Figure 3.89 HVPWELL

3. Layer and Device rules → 3.11 ISOMOS2 module → 3.11.2 Device rules → nei_6

3.11.2 Device rules

nei_6

Name	Description	Value	Unit
W3DF	Minimum GATE width	0.22	μm
	Note: The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) having smaller GATE width than 0.22μm.		
W4P1	Minimum GATE length	0.18	μm
	Note: The design rule check error message W4P1 is also used generally for GATE areas (of any devices or shapes) being smaller than 0.18μm at any dimension.		

Note: nei_6 device must be labeled “6T” using POLY1 (VERIFICATION) layer over the GATE.

Note: nei_6 is placed in DNWELLMV and DNWELL. Please take care of the well edge design rules.

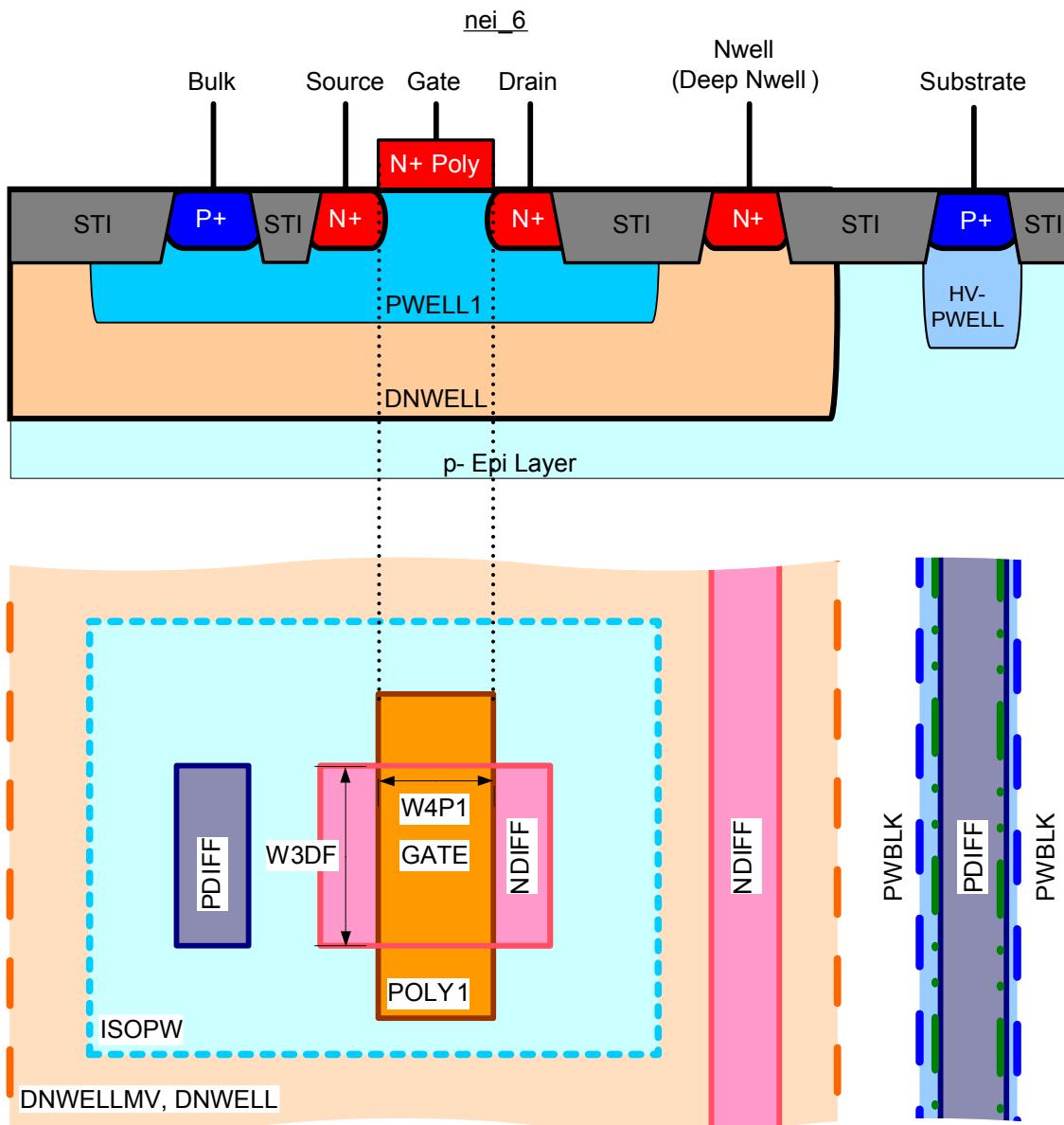


Figure 3.90 nei_6

3. Layer and Device rules → 3.11 ISOMOS2 module→ 3.11.2 Device rules→ pei_5

pei_5

Name	Description	Value	Unit
W3DF	Minimum GATE width	0.22	μm
	Note: The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) having smaller GATE width than 0.22μm.		
W4P1	Minimum GATE length	0.18	μm
	Note: The design rule check error message W4P1 is also used generally for GATE areas (of any devices or shapes) being smaller than 0.18μm at any dimension.		

Note: pei_5 and pei_m_5 devices must be labeled "5T" using POLY1 (VERIFICATION) layer over the GATE.

Note: pei_5 is placed in DNWELLMV and DNWELL. Please take care of the well edge design rules.

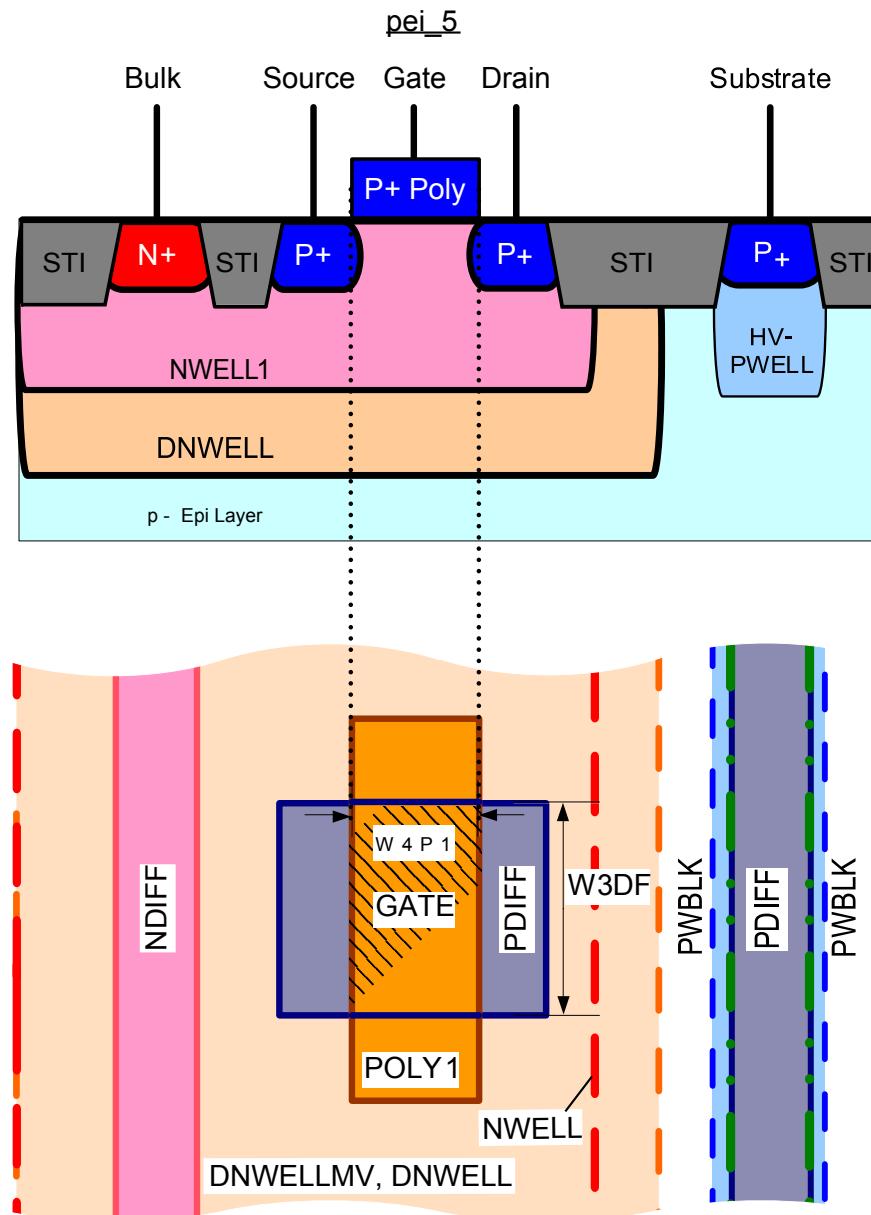


Figure 3.91 pei_5

3. Layer and Device rules → 3.11 ISOMOS2 module→ 3.11.2 Device rules→ ne3i_6

ne3i_6

Name	Description	Value	Unit
W3DF	Minimum GATE width	0.22	μm
	Note: The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) having smaller GATE width than 0.22μm.		
W6P1	Minimum GATE length	0.35	μm

Note: ne3i_6 is placed in DNWELLMV and DNWELL. Please take care of the well edge design rules.

Note: MV is necessary for ne3i_6.

Note: ne3i_6 device must be labeled “6T” using POLY1 (VERIFICATION) layer over the GATE.

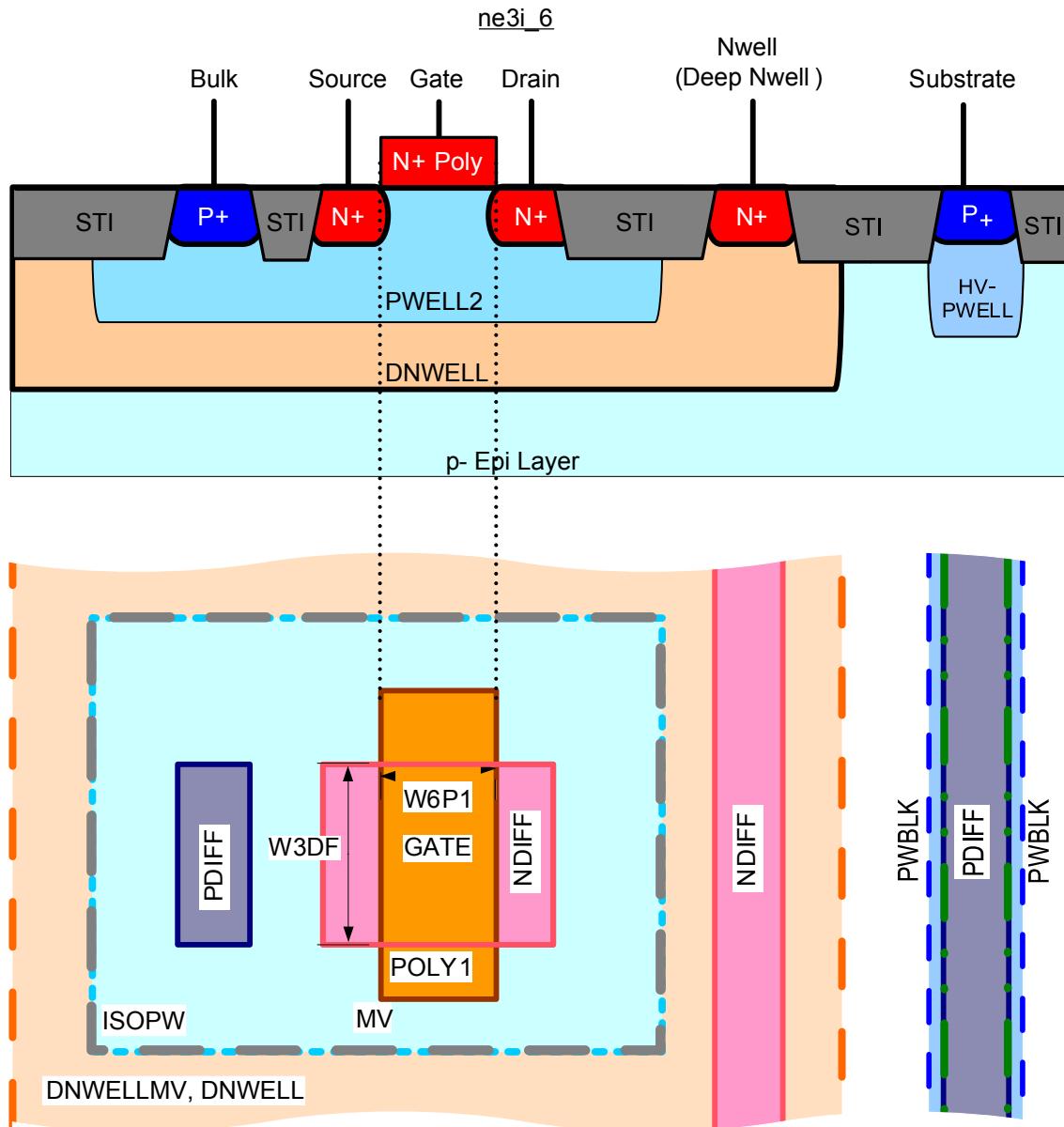


Figure 3.92 ne3i_6

3. Layer and Device rules → 3.11 ISOMOS2 module→ 3.11.2 Device rules→ pe3i_5

pe3i_5

Name	Description	Value	Unit
W3DF	Minimum GATE width	0.22	μm
	Note: The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) having smaller GATE width than 0.22μm.		
W7P1	Minimum GATE length	0.3	μm

Note: pe3i_5 device must be labeled “5T” using POLY1 (VERIFICATION) layer over the GATE.

Note: MV is necessary for pe3i_5.

Note: pe3i_5 is placed in DNWELLMV and DNWELL. Please take care of the well edge design rules.

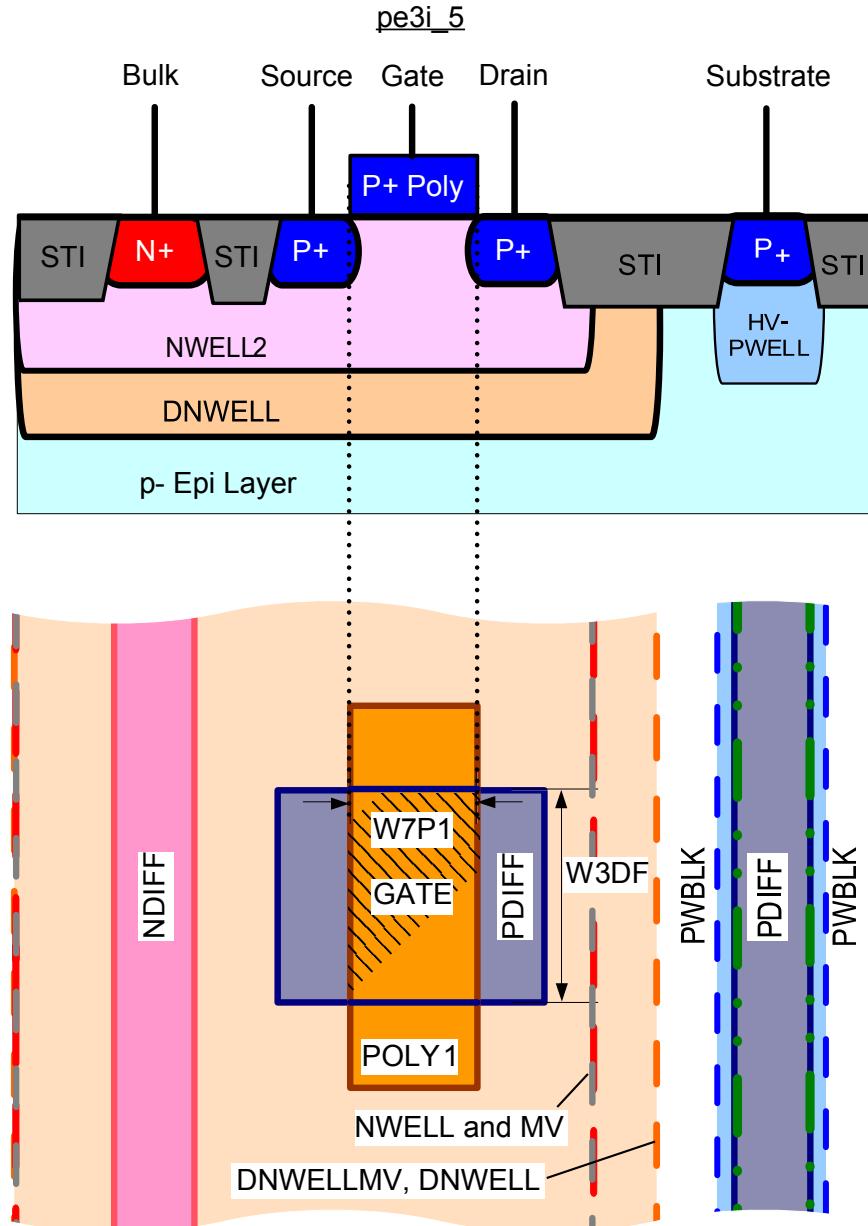


Figure 3.93 pe3i_5

3. Layer and Device rules → 3.11 ISOMOS2 module → 3.11.2 Device rules → mosvc3i

mosvc3i

Name	Description	Value	Unit
B4GA	Only rectangular GATE is allowed	-	-
W38GA	Minimum GATE length	2.0	μm
W39GA	Minimum GATE width	2.0	μm

Note: mosvc3i is placed in DNWELLMV and DNWELL. Please take care of the well edge design rules.

Note: MV is necessary for mosvc3i.

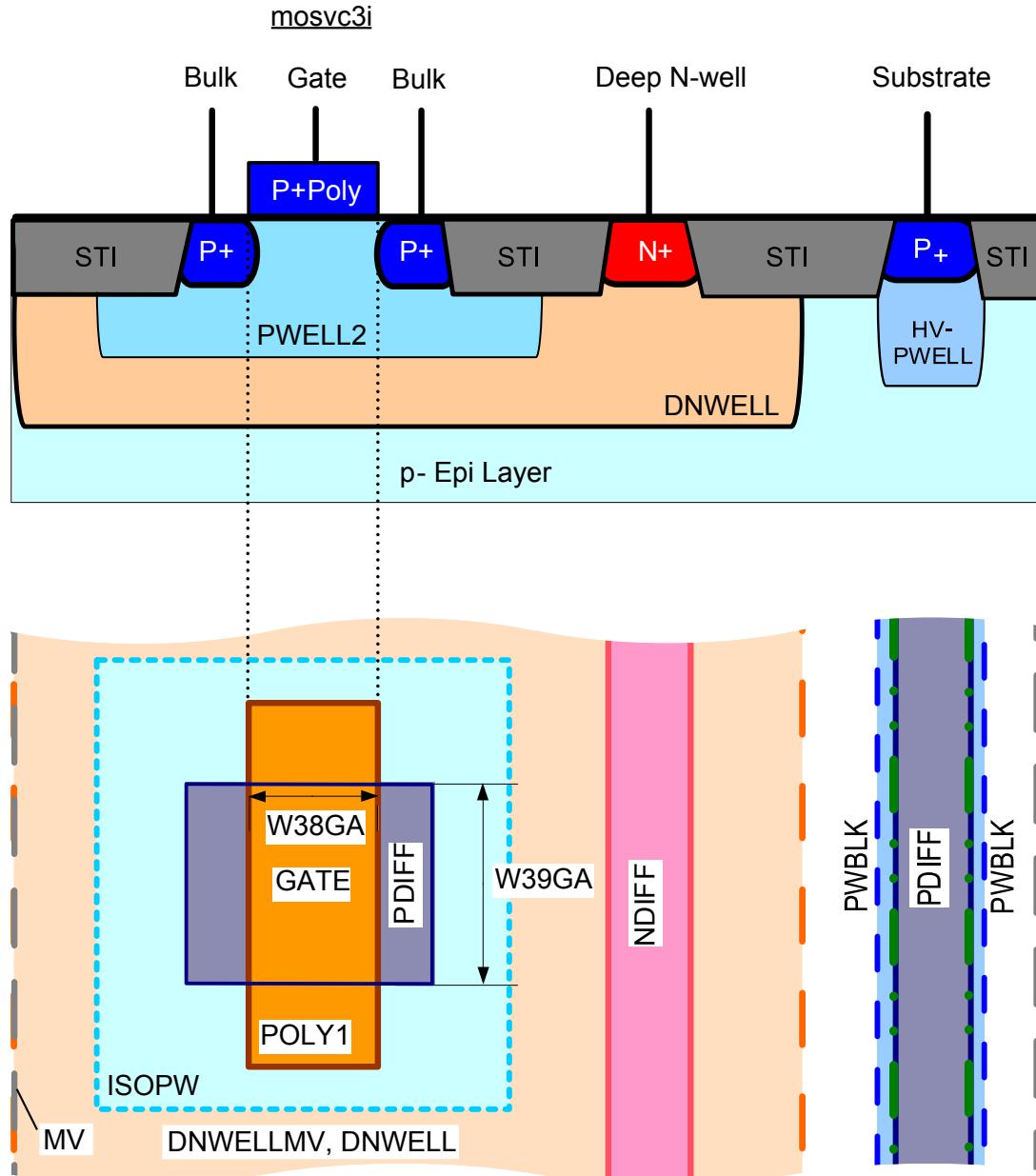


Figure 3.94 mosvc3i

3. Layer and Device rules → 3.11 ISOMOS2 module → 3.11.2 Device rules → mosvci

mosvci

Name	Description	Value	Unit
B4GA	Only rectangular GATE is allowed	-	-
W38GA	Minimum GATE length	2.0	μm
W39GA	Minimum GATE width	2.0	μm

Note: mosvci is placed in DNWELLMV and DNWELL. Please take care of the well edge design rules.

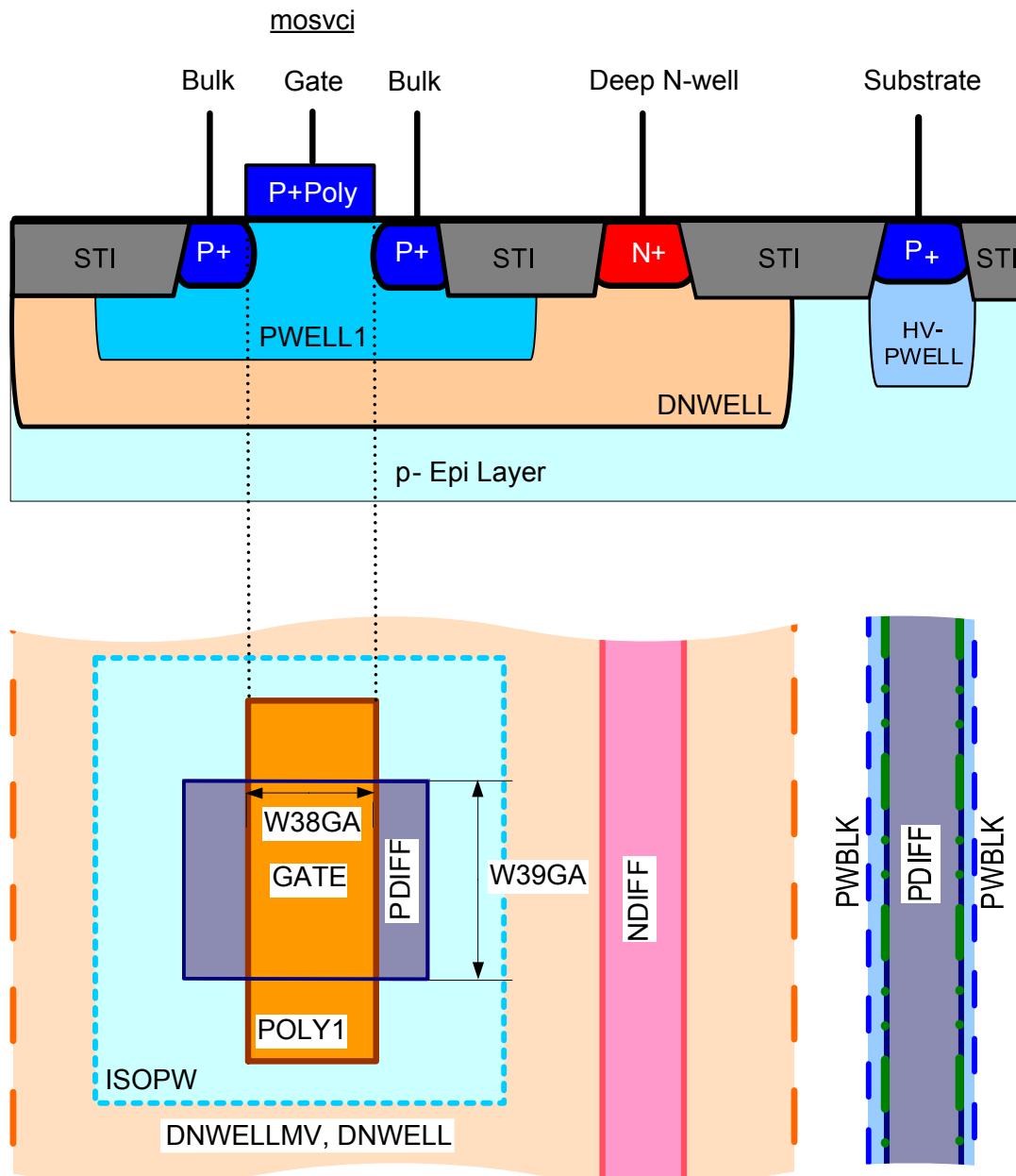


Figure 3.95 mosvci

3. Layer and Device rules → 3.12 HIGHTEMP module

3.12 HIGHTEMP module

This module must be selected for IC designs operating at junction temperatures above 125°C (operating conditions). The module qualification status for temperature range -40°C...+175°C may differ from that at -40°C...+125°C.

For all design rules, please refer to those sections of “3. Layer and Device Rules” describing the relevant rules.

3. Layer and Device rules → 3.13 LVT module

3.13 LVT module

3.13.1 Layer rules

LVT

Name	Description	Value	Unit
B1LV	LVT overlap of PWBLK, MV, HVGOX, HVNWELL, HVPWELL, HNW, DNC, DPC, PDD, SCI or DEPL is not allowed	-	-
B2LV	LVT overlap of rnw, rdn, rdp, qpva, qpvb, qpvc or qnvb is not allowed	-	-
S1LVGA	Minimum LVT spacing to GATE	0.35	µm
S1LVHN	Minimum LVT spacing to HVNWELL	3.0	µm
S1LVHP	Minimum LVT spacing to HVPWELL	3.0	µm
S1LVHW	Minimum LVT spacing to HNW	10.0	µm
S1LVND	Minimum LVT spacing to NDF	10.0	µm
S1LVWD	Minimum LVT spacing to DNWELL	10.0	µm
S1LVWM	Minimum LVT spacing to DNWELLMV	3.5	µm
	Note: Only valid if DNWELLMV is outside DNWELL.		
S2LVGA	Minimum LVT spacing to GATE (in GATE length direction)	0.46	µm
E1LVGA	Minimum LVT enclosure of GATE	0.35	µm
E2LVGA	Minimum LVT enclosure of GATE (in GATE length direction)	0.46	µm

Note: Because of the well proximity effect it is not recommended to use the minimum design rules E1LVGA, E2LVGA, S1LVGA and S2LVGA for critical and precise designs. Please refer to the corresponding [application note](#) on "my X-FAB".

3. Layer and Device rules → 3.13 LVT module → 3.13.1 Layer rules→ LVT

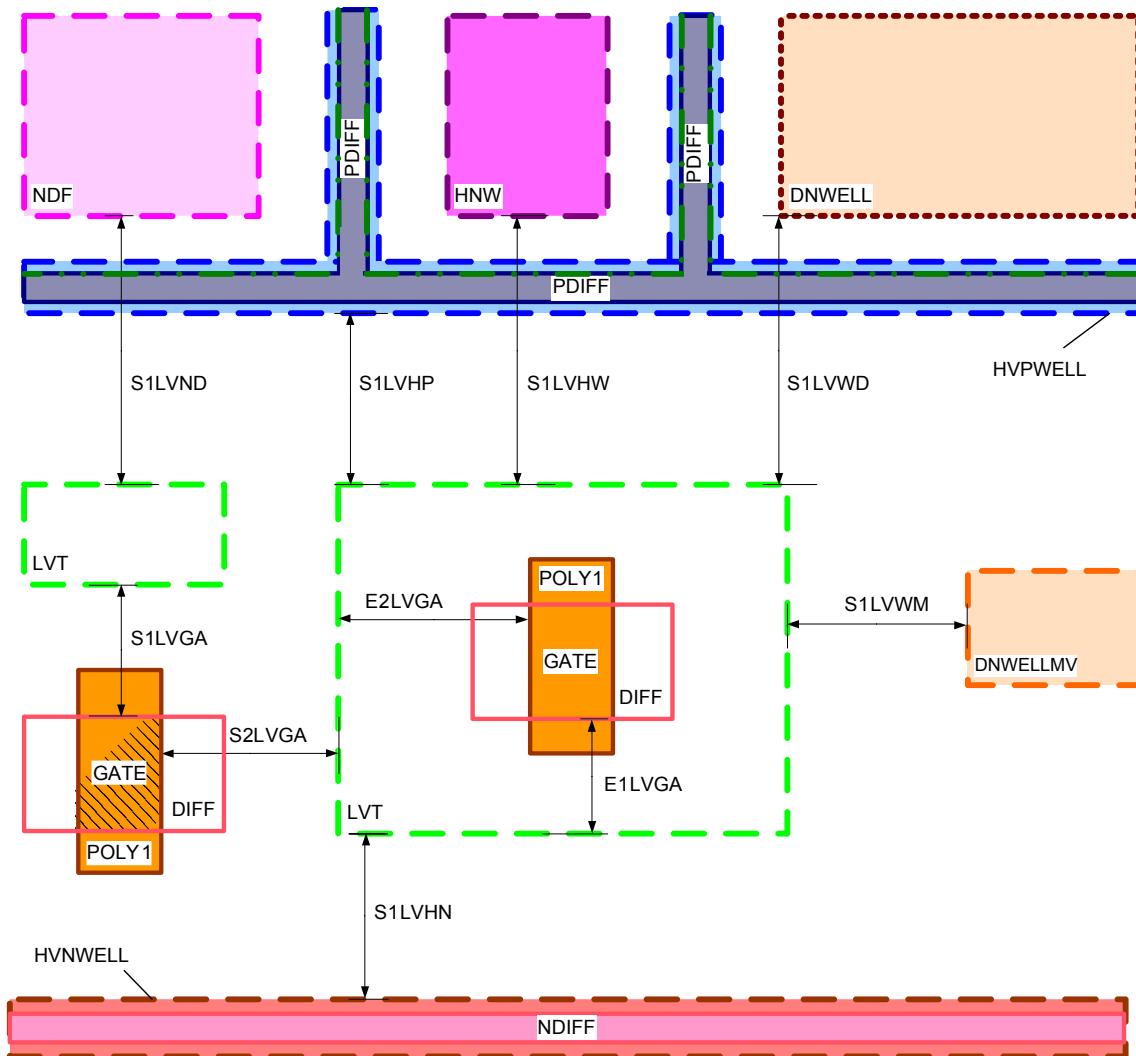


Figure 3.96 LVT

3. Layer and Device rules → 3.13 LVT module → 3.13.2 Device rules → nel, pel

3.13.2 Device rules

nel, pel

Name	Description	Value	Unit
W3DF	Minimum GATE width Note: The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) having smaller GATE width than 0.22µm.	0.22	µm
W4P1	Minimum GATE length Note: The design rule check error message W4P1 is also used generally for GATE areas (of any devices or shapes) being smaller than 0.18µm at any dimension.	0.18	µm

Note: For more extensive LVS, it is recommended to use the related 5 or 6 terminal device.

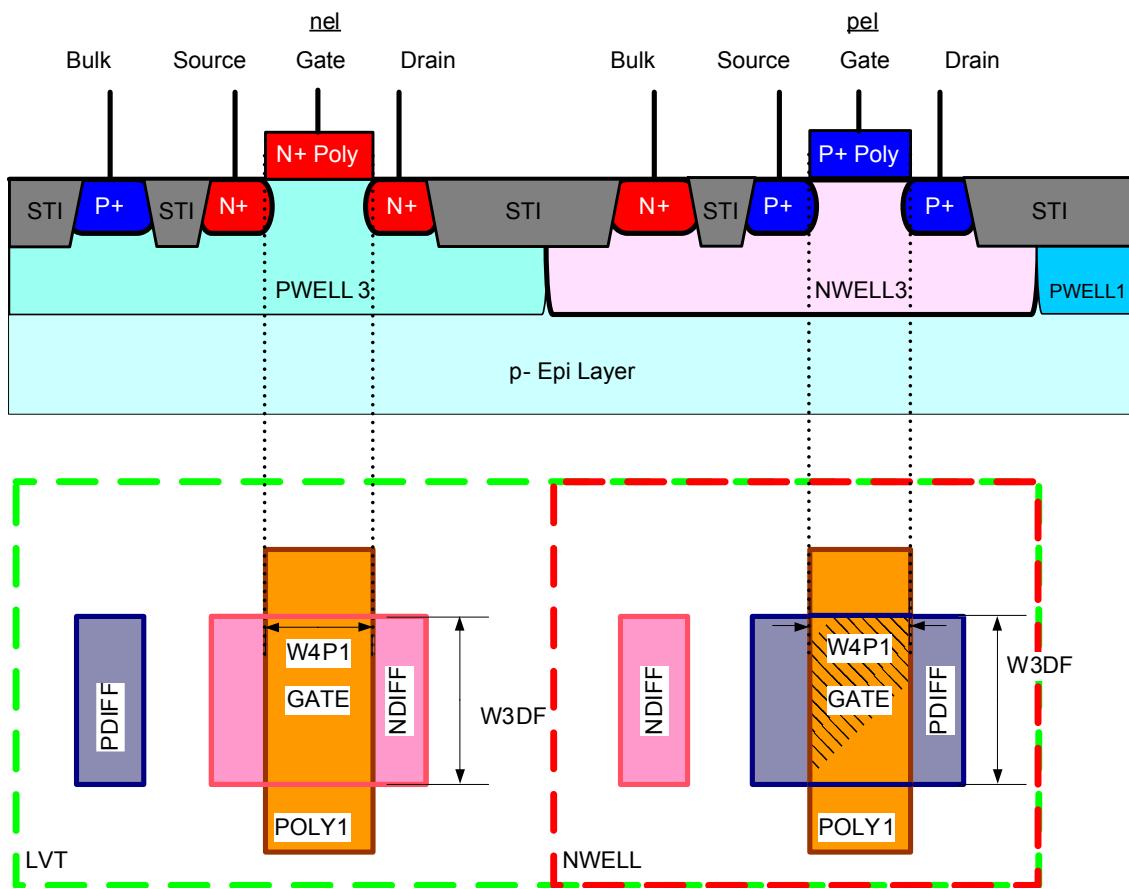


Figure 3.97 nel, pel

3. Layer and Device rules → 3.13 LVT module→ 3.13.2 Device rules→ pel_5

pel_5

Name	Description	Value	Unit
W3DF	Minimum GATE width	0.22	μm
	Note: The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) having smaller GATE width than 0.22μm.		
W4P1	Minimum GATE length	0.18	μm
	Note: The design rule check error message W4P1 is also used generally for GATE areas (of any devices or shapes) being smaller than 0.18μm at any dimension.		

Note: pel_5 device must be labeled “5T” using POLY1 (VERIFICATION) layer over the GATE.

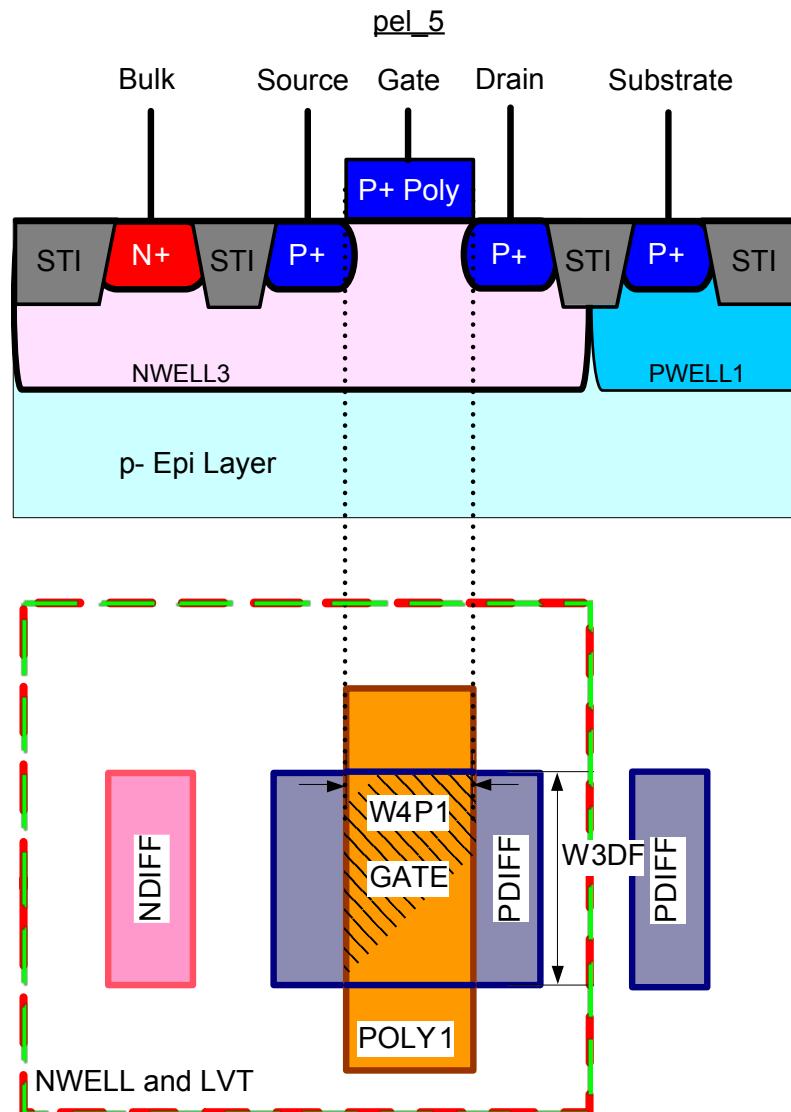


Figure 3.98 pel_5

3. Layer and Device rules → 3.13 LVT module→ 3.13.2 Device rules→ neli, peli

neli, peli

Name	Description	Value	Unit
W3DF	Minimum GATE width	0.22	μm
	Note: The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) having smaller GATE width than 0.22μm.		
W4P1	Minimum GATE length	0.18	μm
	Note: The design rule check error message W4P1 is also used generally for GATE areas (of any devices or shapes) being smaller than 0.18μm at any dimension.		

Note: neli and peli may be placed in DNWELLMV or DNWELL. Please take care of the different well edge design rules for both cases. For DNWELL the HVMOS Module is needed. (Drawing on this page is only for neli and peli in DNWELLMV)

Note: For more extensive LVS, it is recommended to use the related 5 or 6 terminal device.

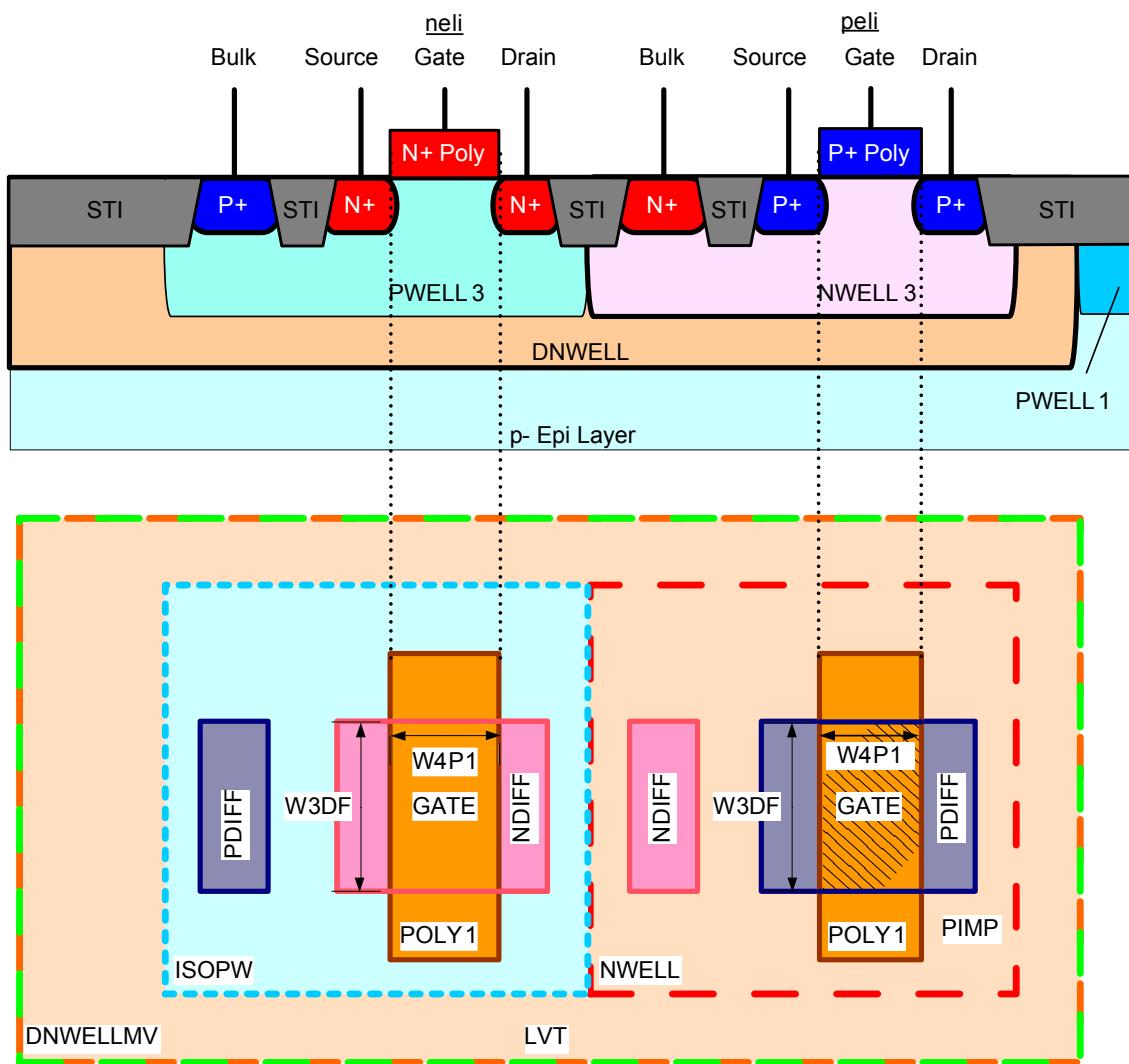


Figure 3.99 neli, peli

3. Layer and Device rules → 3.13 LVT module → 3.13.2 Device rules → neli_6

neli_6

Name	Description	Value	Unit
W3DF	Minimum GATE width	0.22	μm
	Note: The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) having smaller GATE width than 0.22μm.		
W4P1	Minimum GATE length	0.18	μm
	Note: The design rule check error message W4P1 is also used generally for GATE areas (of any devices or shapes) being smaller than 0.18μm at any dimension.		

Note: neli_6 is placed in DNWELLMV and DNWELL. Please take care of the well edge design rules.

Note: neli_6 device must be labeled "6T" using POLY1 (VERIFICATION) layer over the GATE.

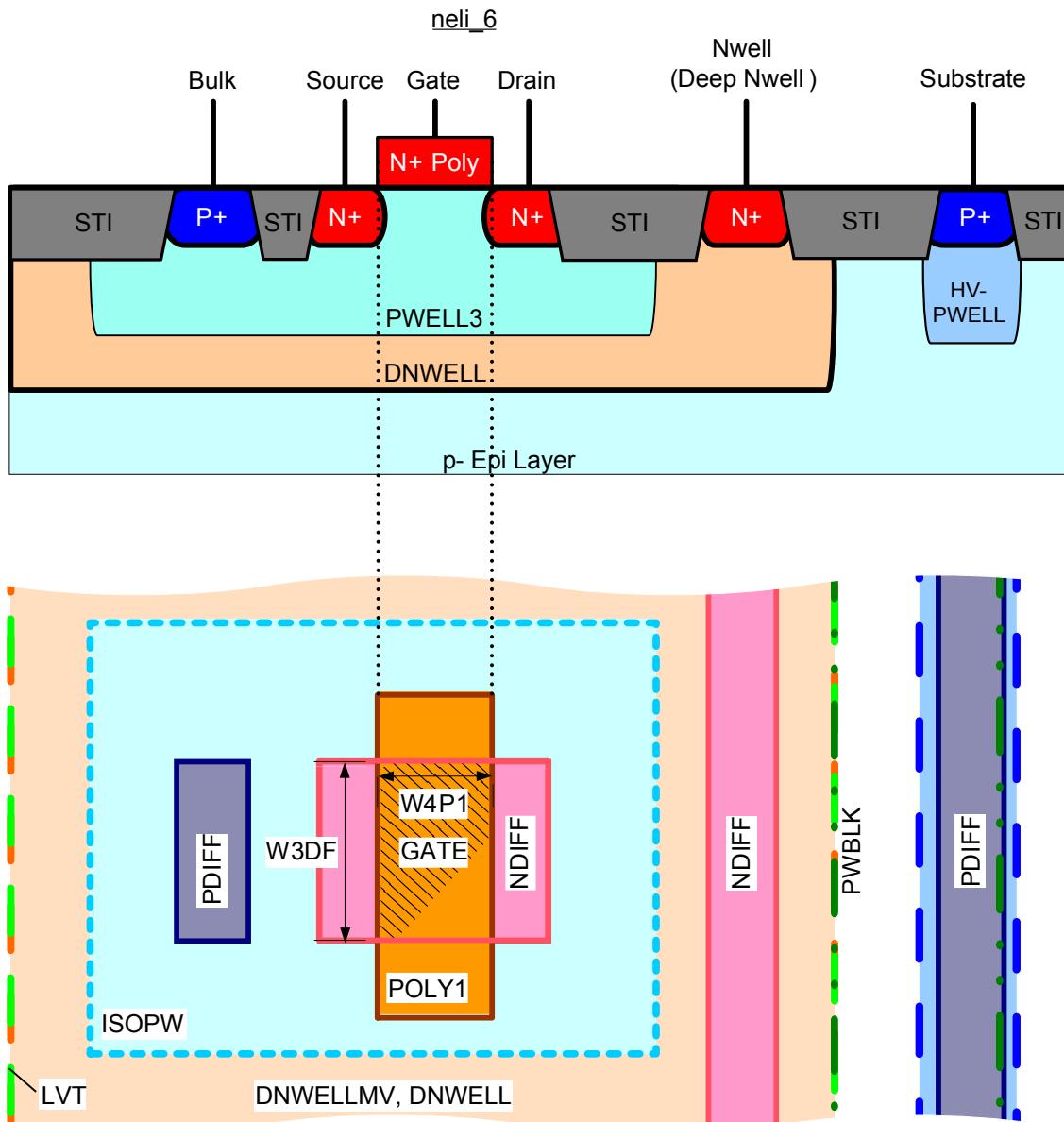


Figure 3.100 neli_6

3. Layer and Device rules → 3.13 LVT module → 3.13.2 Device rules → neli_m_6

neli_m_6

Name	Description	Value	Unit
W3DF	Minimum GATE width	0.22	μm
	Note: The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) having smaller GATE width than 0.22μm.		
W4P1	Minimum GATE length	0.18	μm
	Note: The design rule check error message W4P1 is also used generally for GATE areas (of any devices or shapes) being smaller than 0.18μm at any dimension.		

Note: neli_m_6 device must be labeled "6T" using POLY1 (VERIFICATION) layer over the GATE.

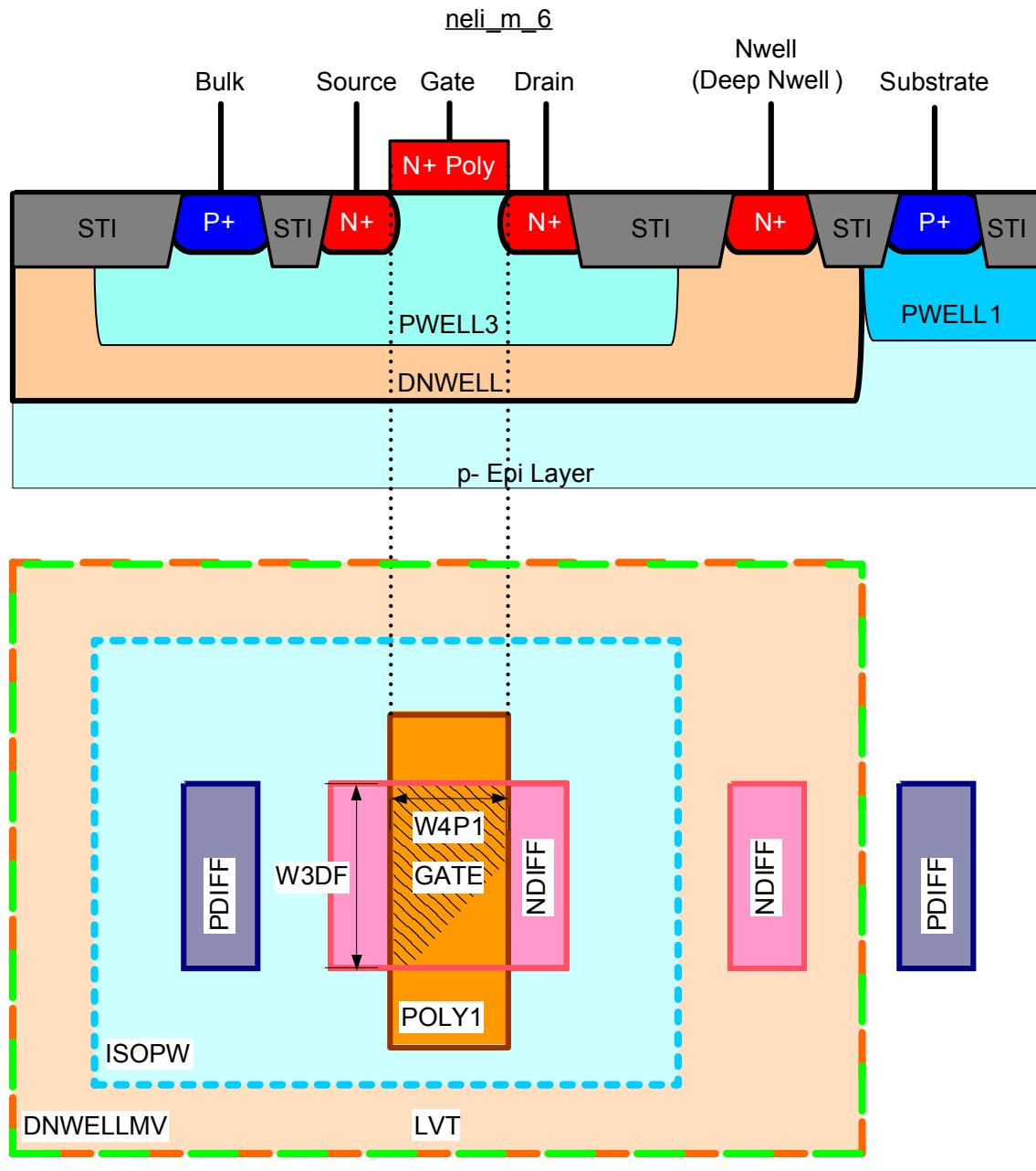


Figure 3.101 neli_m_6

3. Layer and Device rules → 3.13 LVT module→ 3.13.2 Device rules→ peli_5

peli_5

Name	Description	Value	Unit
W3DF	Minimum GATE width	0.22	μm
	Note: The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) having smaller GATE width than 0.22μm.		
W4P1	Minimum GATE length	0.18	μm
	Note: The design rule check error message W4P1 is also used generally for GATE areas (of any devices or shapes) being smaller than 0.18μm at any dimension.		

Note: peli_5 is placed in DNWELLMV and DNWELL. Please take care of the well edge design rules.

Note: peli_5 device must be labeled "5T" using POLY1 (VERIFICATION) layer over the GATE.

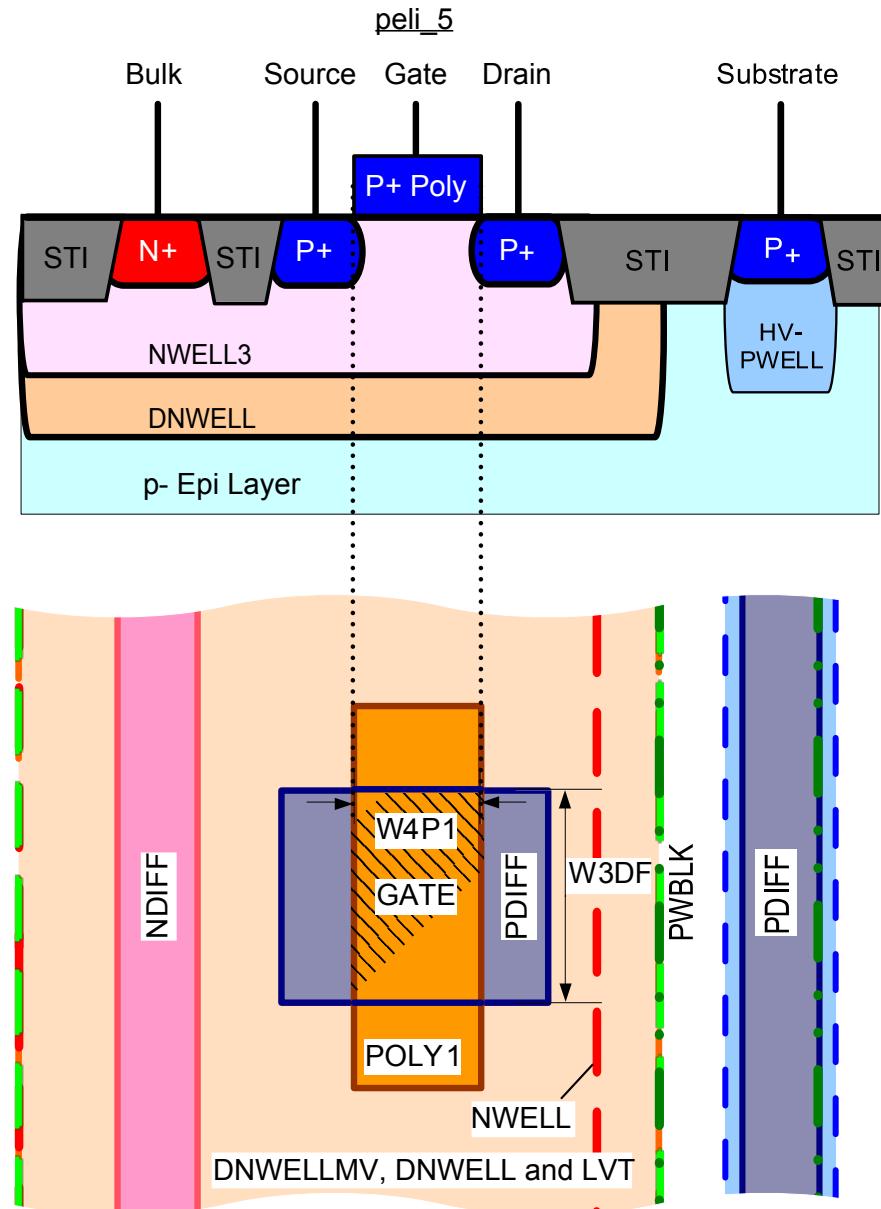


Figure 3.102 peli_5

3. Layer and Device rules → 3.13 LVT module → 3.13.2 Device rules → peli_m_5

peli_m_5

Name	Description	Value	Unit
W3DF	Minimum GATE width	0.22	μm
	Note: The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) having smaller GATE width than 0.22μm.		
W4P1	Minimum GATE length	0.18	μm
	Note: The design rule check error message W4P1 is also used generally for GATE areas (of any devices or shapes) being smaller than 0.18μm at any dimension.		

Note: peli_m_5 device must be labeled "5T" using POLY1 (VERIFICATION) layer over the GATE.

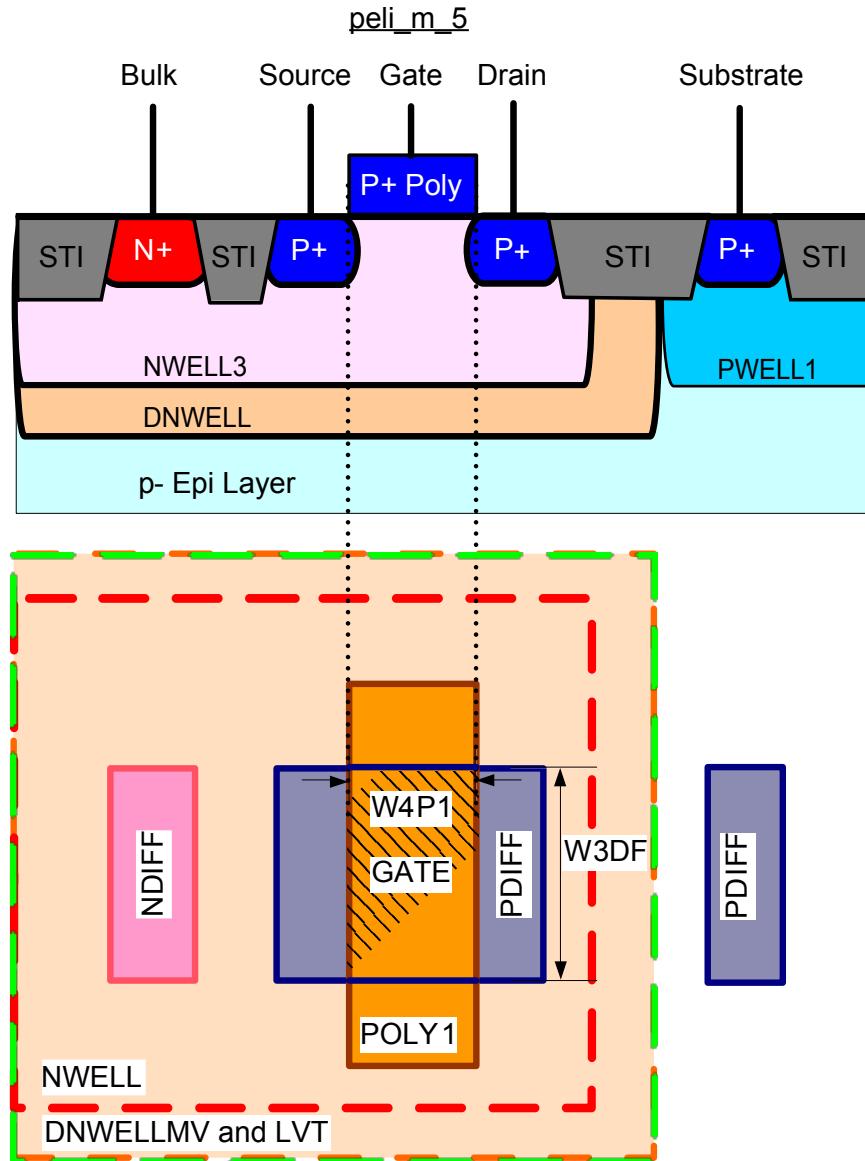


Figure 3.103 peli_m_5

3. Layer and Device rules → 3.14 SVT module

3.14 SVT module

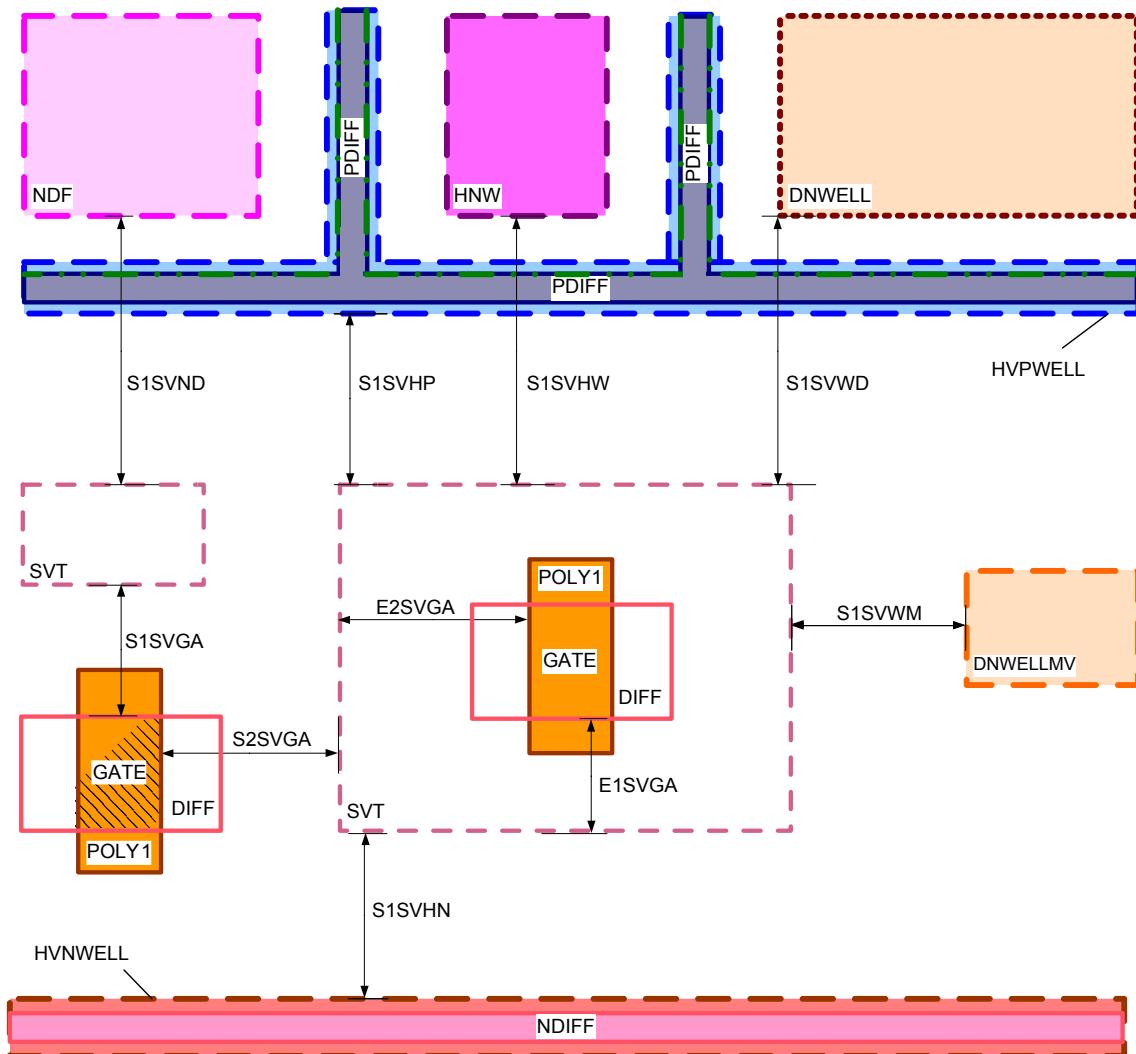
3.14.1 Layer rules

SVT

Name	Description	Value	Unit
B1SV	SVT overlap of PWBLK, MV, HVGOX, HVNWELL, HVPWELL, HNW, DNC, DPC, PDD, LVT, SCI or DEPL is not allowed	-	-
B2SV	SVT overlap of rnw, rdn, rdp, qpva, qpvb, qpvc or qnvb is not allowed	-	-
S1SVGA	Minimum SVT spacing to GATE	0.35	μm
S1SVHN	Minimum SVT spacing to HVNWELL	3.0	μm
S1SVHP	Minimum SVT spacing to HVPWELL	3.0	μm
S1SVHW	Minimum SVT spacing to HNW	10.0	μm
S1SVND	Minimum SVT spacing to NDF	10.0	μm
S1SVWD	Minimum SVT spacing to DNWELL	10.0	μm
S1SVWM	Minimum SVT spacing to DNWELLMV	3.5	μm
	Note: Only valid if DNWELLMV is outside DNWELL.		
S2SVGA	Minimum SVT spacing to GATE (in GATE length direction)	0.46	μm
E1SVGA	Minimum SVT enclosure of GATE	0.35	μm
E2SVGA	Minimum SVT enclosure of GATE (in GATE length direction)	0.46	μm

Note: Because of the well proximity effect it is not recommended to use the minimum design rules E1SVGA, E2SVGA, S1SVGA and S2SVGA for critical and precise designs.

3. Layer and Device rules → 3.14 SVT module → 3.14.1 Layer rules→ SVT

**Figure 3.104** SVT

3. Layer and Device rules → 3.14 SVT module→ 3.14.2 Device rules→ nesvt

3.14.2 Device rules

nesvt

Name	Description	Value	Unit
W3DF	Minimum GATE width	0.22	μm
	Note: The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) having smaller GATE width than 0.22μm.		
W4P1	Minimum GATE length	0.18	μm
	Note: The design rule check error message W4P1 is also used generally for GATE areas (of any devices or shapes) being smaller than 0.18μm at any dimension.		

Note: For more extensive LVS, it is recommended to use the related 5 or 6 terminal device.

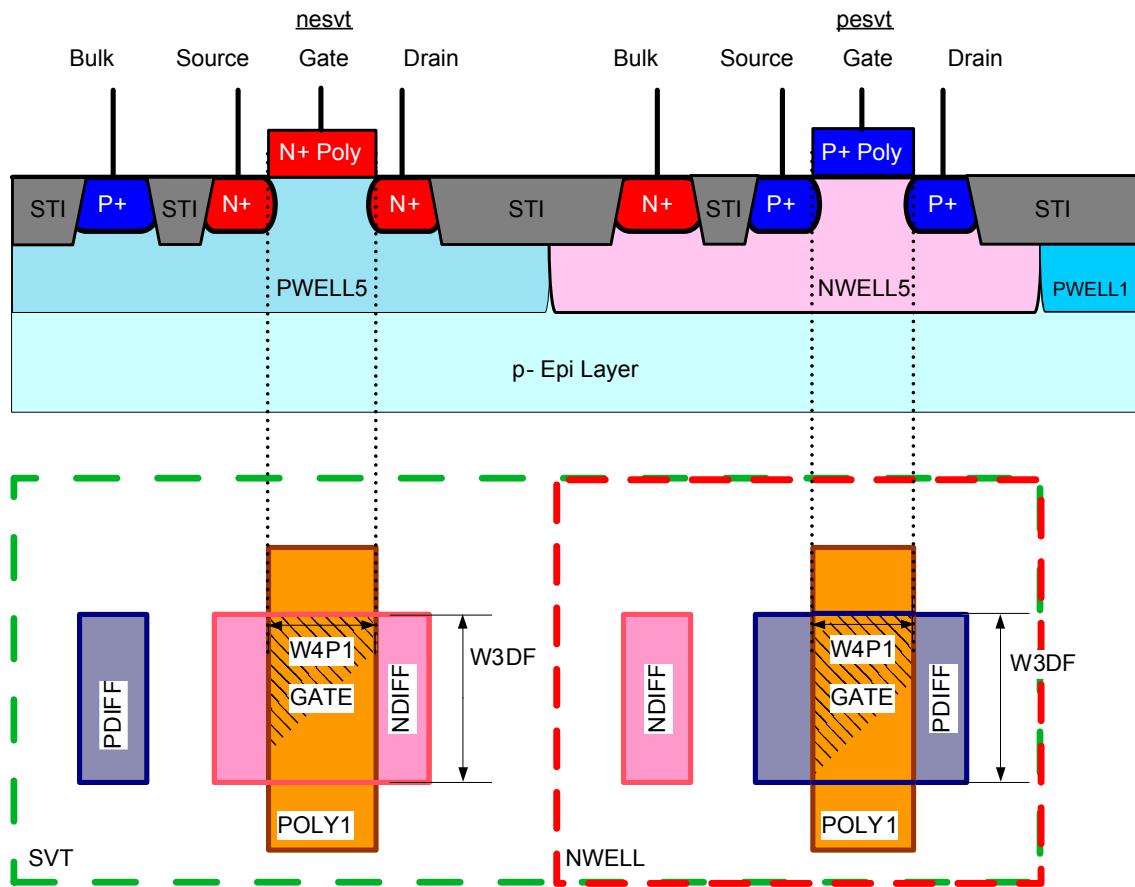


Figure 3.105 nesvt, pesvt

3. Layer and Device rules → 3.14 SVT module→ 3.14.2 Device rules→ nesvti

nesvti

Name	Description	Value	Unit
W3DF	Minimum GATE width	0.22	μm
	Note: The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) having smaller GATE width than 0.22μm.		
W4P1	Minimum GATE length	0.18	μm
	Note: The design rule check error message W4P1 is also used generally for GATE areas (of any devices or shapes) being smaller than 0.18μm at any dimension.		

Note: For more extensive LVS, it is recommended to use the related 5 or 6 terminal device.

Note: nesvti and pesvti may be placed in DNWELLMV or DNWELL. Please take care of the different well edge design rules for both cases. For DNWELL the HVMOS Module is needed. (Drawing on this page is only for neli and peli in DNWELLMV)

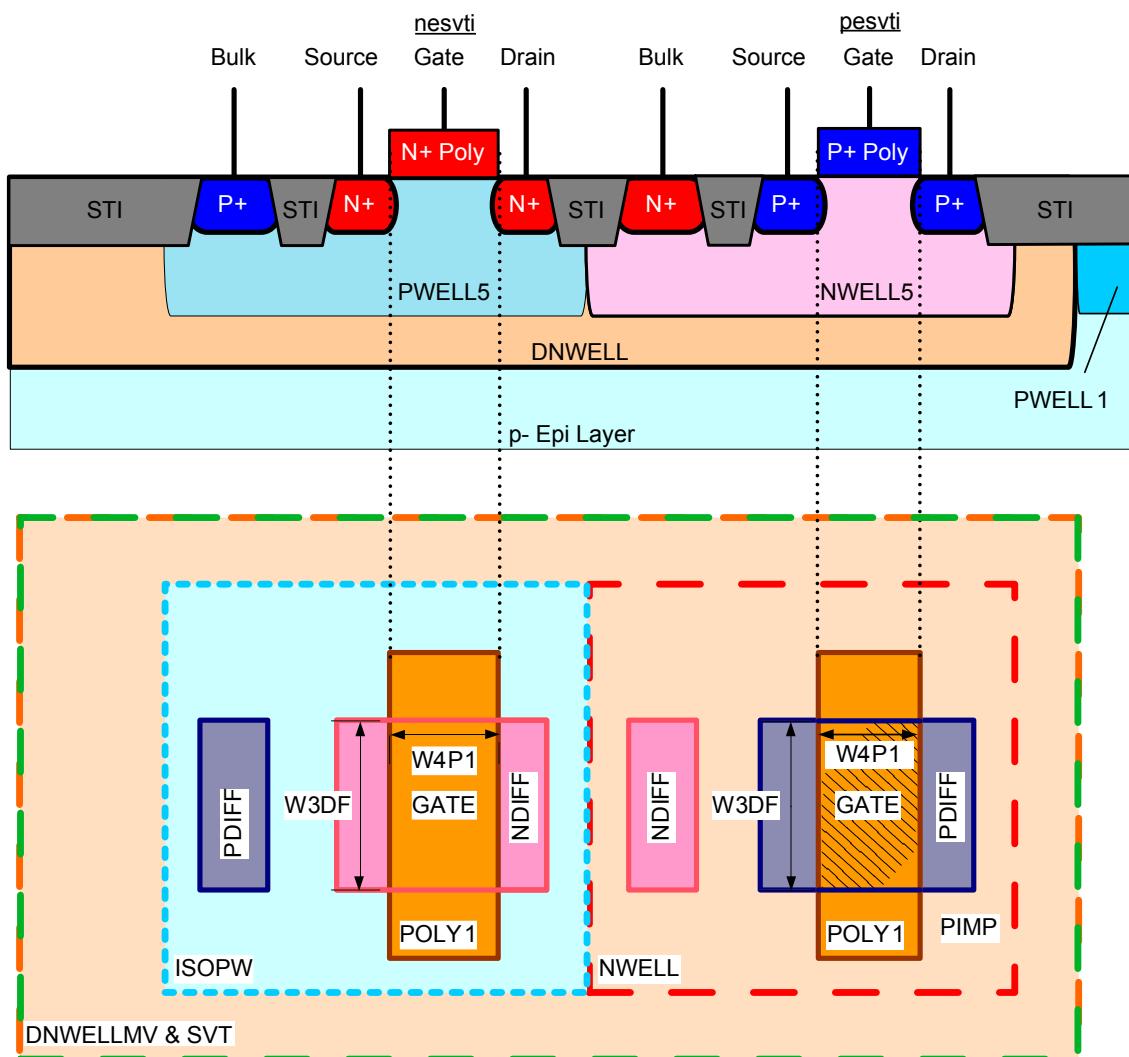


Figure 3.106 nesvti, pesvti

3. Layer and Device rules → 3.14 SVT module→ 3.14.2 Device rules→ nesvti_6

nesvti_6

Name	Description	Value	Unit
W3DF	Minimum GATE width	0.22	μm
	Note: The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) having smaller GATE width than 0.22μm.		
W4P1	Minimum GATE length	0.18	μm
	Note: The design rule check error message W4P1 is also used generally for GATE areas (of any devices or shapes) being smaller than 0.18μm at any dimension.		

Note: nesvti_6 is placed in DNWELLMV and DNWELL. Please take care of the well edge design rules.

Note: nesvti_6 device must be labeled "6T" using POLY1 (VERIFICATION) layer over the GATE.

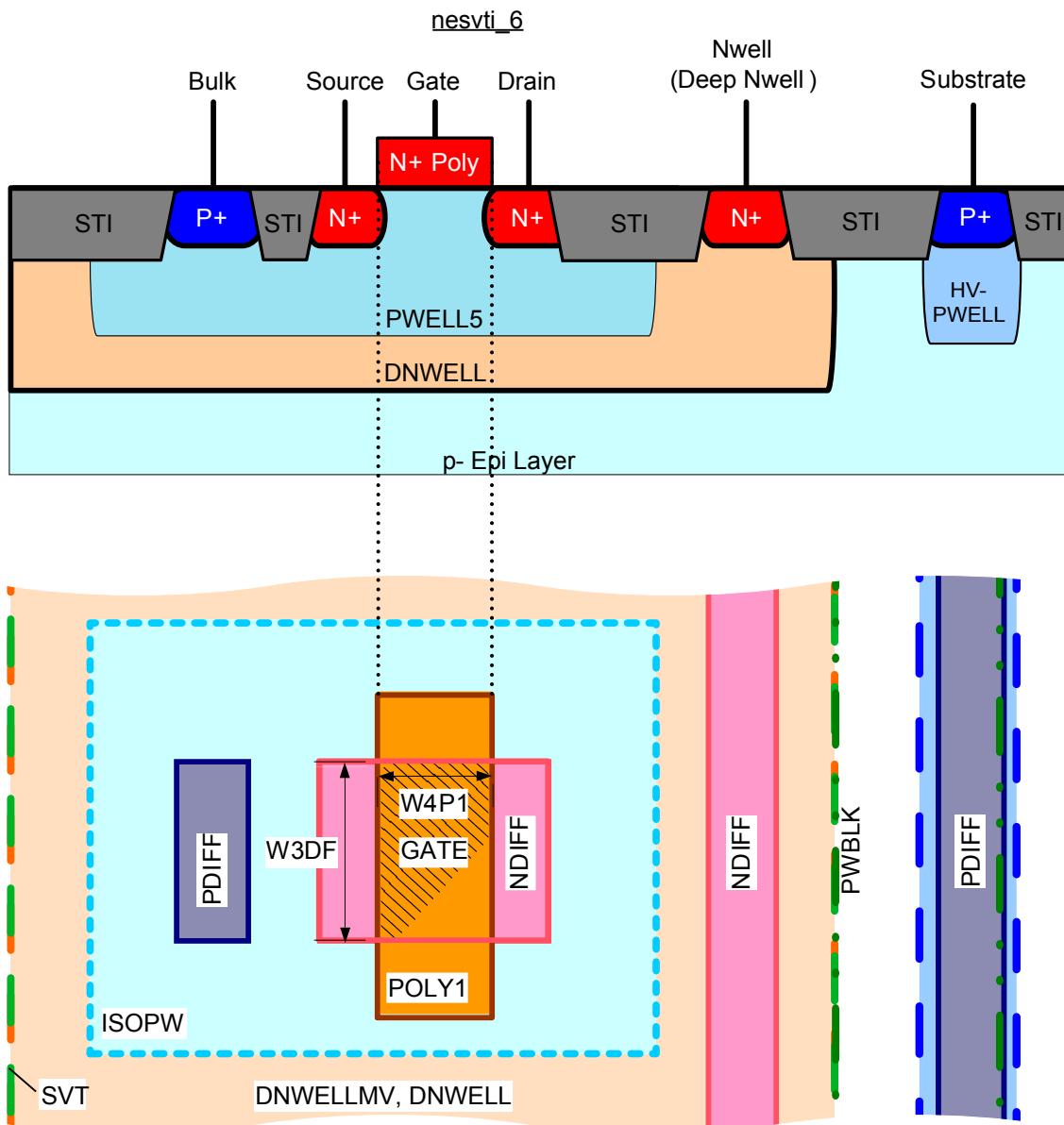


Figure 3.107 nesvti_6

3. Layer and Device rules → 3.14 SVT module→ 3.14.2 Device rules→ nesvti_m_6

nesvti_m_6

Name	Description	Value	Unit
W3DF	Minimum GATE width	0.22	μm
	Note: The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) having smaller GATE width than 0.22μm.		
W4P1	Minimum GATE length	0.18	μm
	Note: The design rule check error message W4P1 is also used generally for GATE areas (of any devices or shapes) being smaller than 0.18μm at any dimension.		

Note: nesvti_m_6 device must be labeled “6T” using POLY1 (VERIFICATION) layer over the GATE.

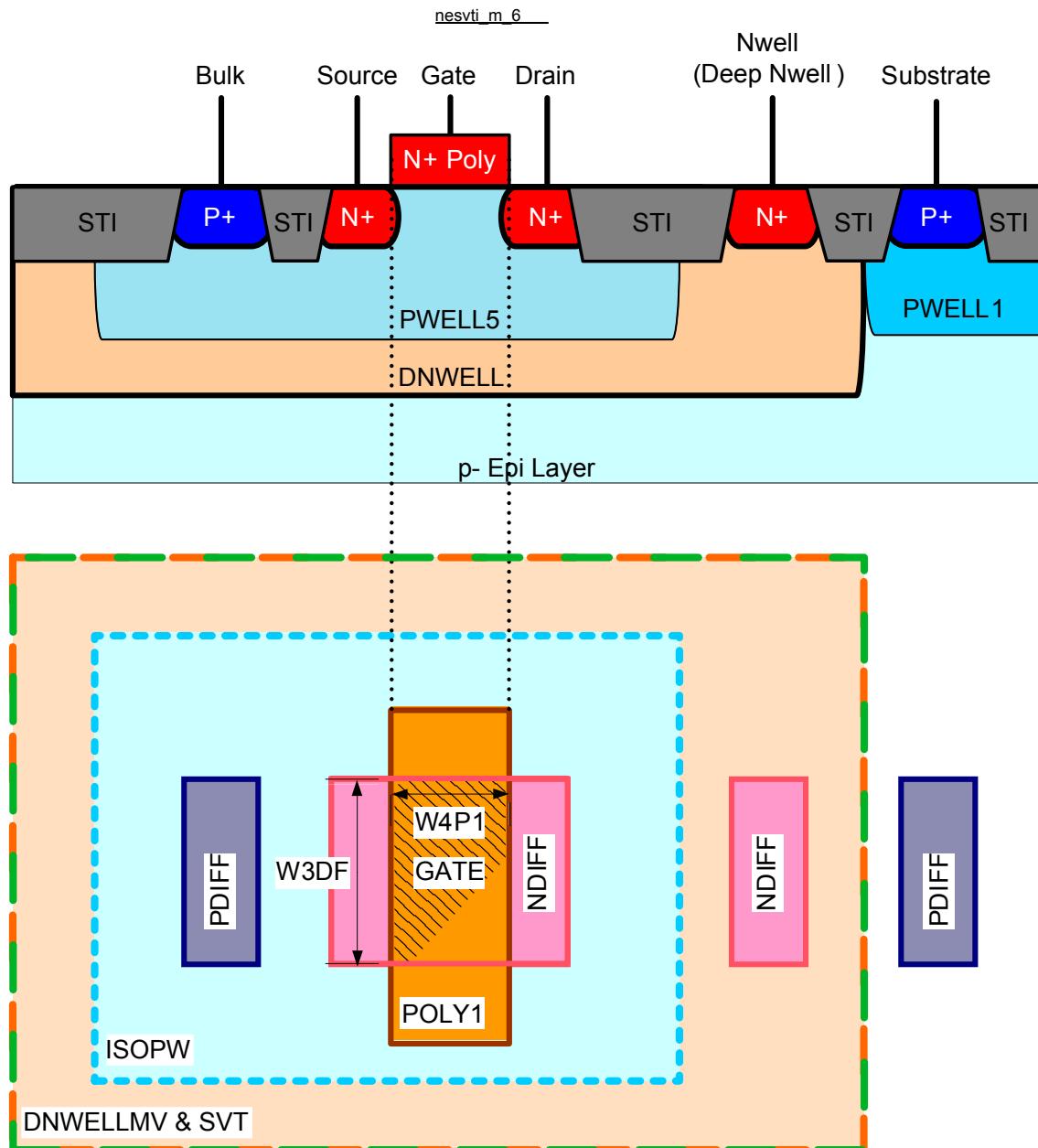


Figure 3.108 nesvti_m_6

3. Layer and Device rules → 3.14 SVT module→ 3.14.2 Device rules→ pesvt

pesvt

Name	Description	Value	Unit
W3DF	Minimum GATE width	0.22	μm
	Note: The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) having smaller GATE width than 0.22μm.		
W4P1	Minimum GATE length	0.18	μm
	Note: The design rule check error message W4P1 is also used generally for GATE areas (of any devices or shapes) being smaller than 0.18μm at any dimension.		

Note: For more extensive LVS, it is recommended to use the related 5 or 6 terminal device.

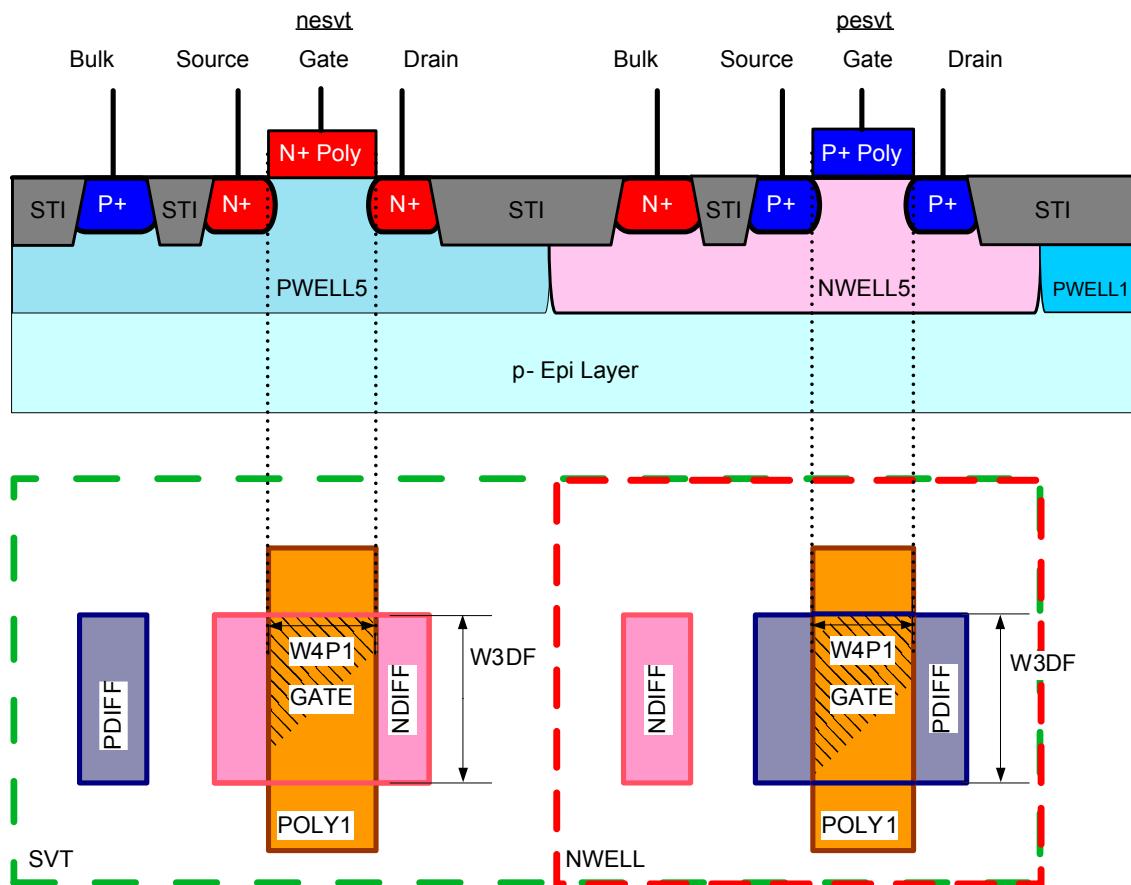


Figure 3.109 nesvt, pesvt

3. Layer and Device rules → 3.14 SVT module→ 3.14.2 Device rules→ pesvt_5

pesvt_5

Name	Description	Value	Unit
W3DF	Minimum GATE width	0.22	μm
	Note: The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) having smaller GATE width than 0.22μm.		
W4P1	Minimum GATE length	0.18	μm
	Note: The design rule check error message W4P1 is also used generally for GATE areas (of any devices or shapes) being smaller than 0.18μm at any dimension.		

Note: pesvt_5 is placed in DNWELLMV and DNWELL. Please take care of the well edge design rules.

Note: pesvt_5 device must be labeled "5T" using POLY1 (VERIFICATION) layer over the GATE.

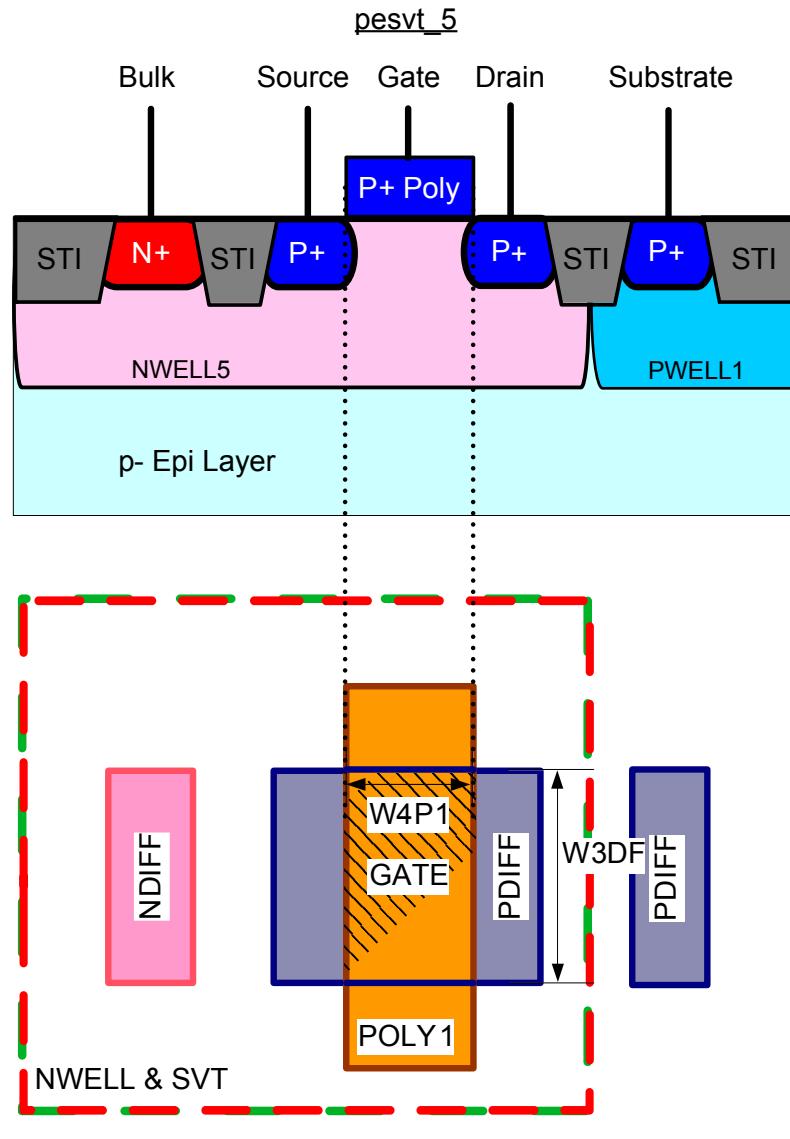


Figure 3.110 pesvt

3. Layer and Device rules → 3.14 SVT module→ 3.14.2 Device rules→ pesvti

pesvti

Name	Description	Value	Unit
W3DF	Minimum GATE width	0.22	μm
	Note: The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) having smaller GATE width than 0.22μm.		
W4P1	Minimum GATE length	0.18	μm
	Note: The design rule check error message W4P1 is also used generally for GATE areas (of any devices or shapes) being smaller than 0.18μm at any dimension.		

Note: For more extensive LVS, it is recommended to use the related 5 or 6 terminal device.

Note: nesvti and pesvti may be placed in DNWELLMV or DNWELL. Please take care of the different well edge design rules for both cases. For DNWELL the HVMOS Module is needed. (Drawing on this page is only for neli and peli in DNWELLMV)

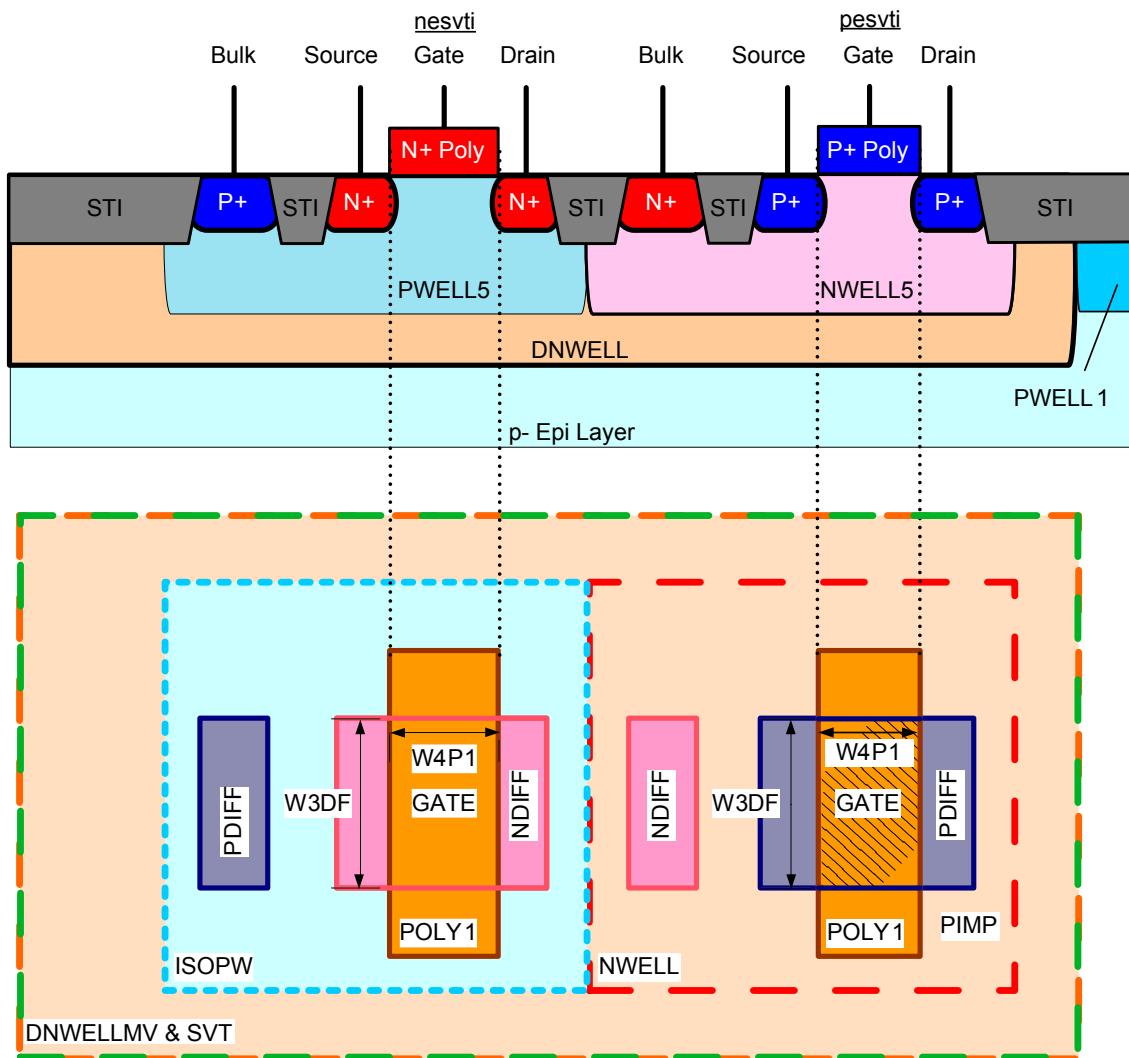


Figure 3.111 nesvti, pesvti

3. Layer and Device rules → 3.14 SVT module→ 3.14.2 Device rules→ pesvti_5

pesvti_5

Name	Description	Value	Unit
W3DF	Minimum GATE width	0.22	μm
	Note: The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) having smaller GATE width than 0.22μm.		
W4P1	Minimum GATE length	0.18	μm
	Note: The design rule check error message W4P1 is also used generally for GATE areas (of any devices or shapes) being smaller than 0.18μm at any dimension.		

Note: pesvti_5 device must be labeled "5T" using POLY1 (VERIFICATION) layer over the GATE.

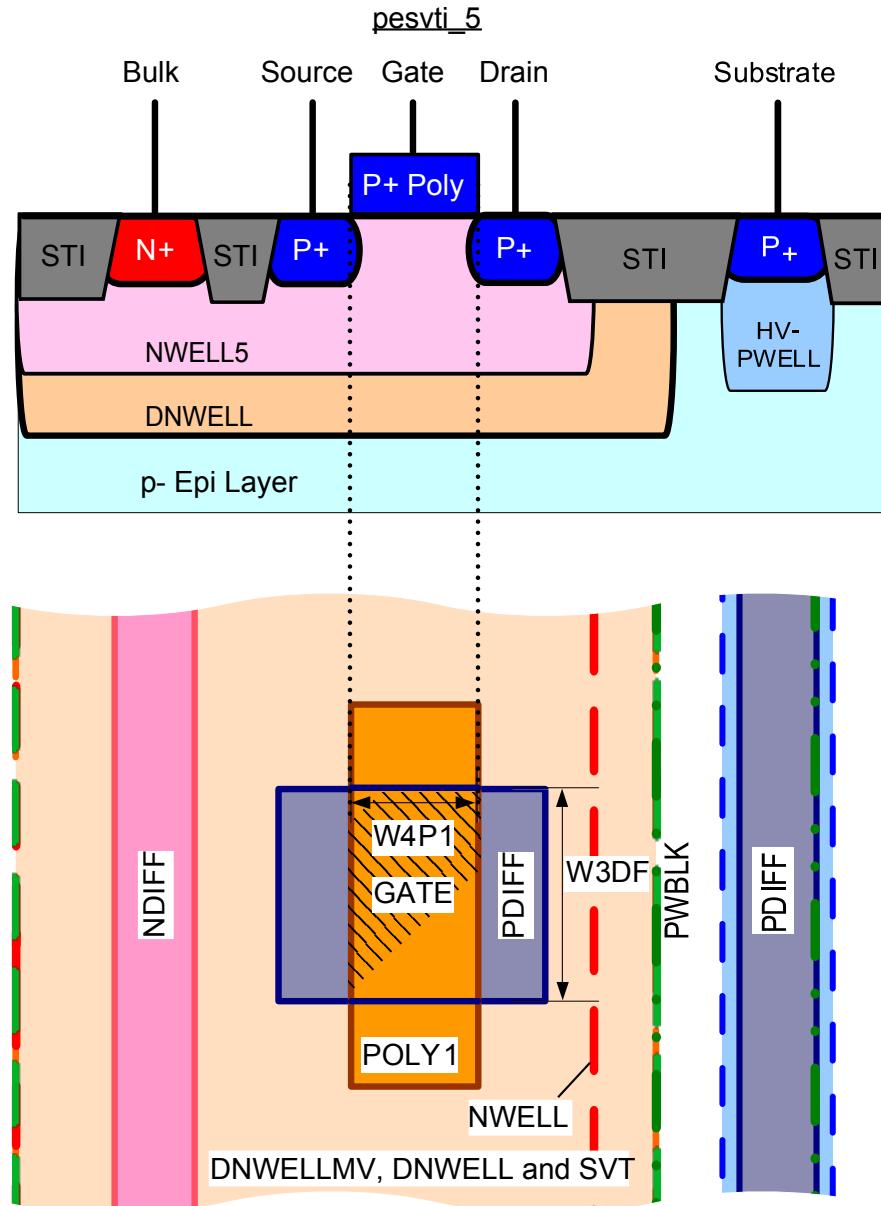


Figure 3.112 pesvti_5

3. Layer and Device rules → 3.14 SVT module→ 3.14.2 Device rules→ pesvti_m_5

pesvti_m_5

Name	Description	Value	Unit
W3DF	Minimum GATE width	0.22	μm
	Note: The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) having smaller GATE width than 0.22μm.		
W4P1	Minimum GATE length	0.18	μm
	Note: The design rule check error message W4P1 is also used generally for GATE areas (of any devices or shapes) being smaller than 0.18μm at any dimension.		

Note: pesvti_m_5 device must be labeled "5T" using POLY1 (VERIFICATION) layer over the GATE.

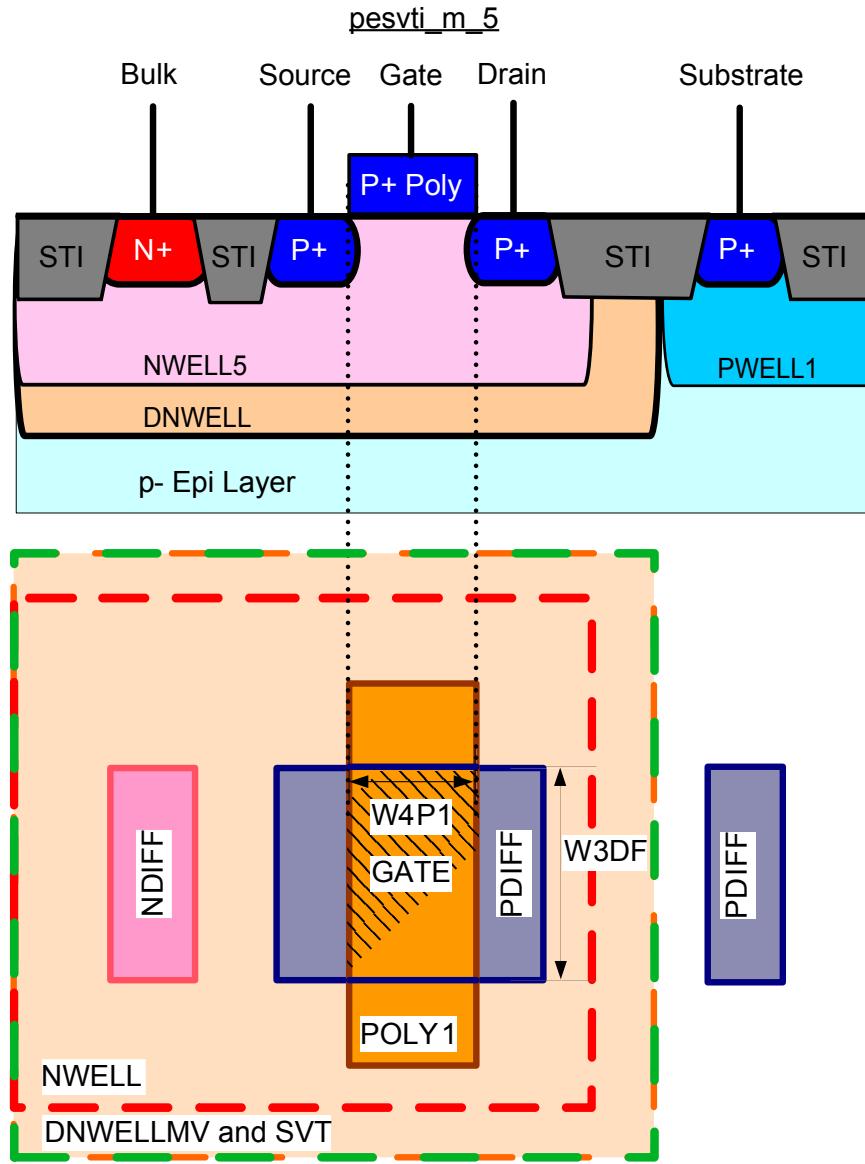


Figure 3.113 pesvti_m_5

3. Layer and Device rules → 3.15 LNPMOS3 module

3.15 LNPMOS3 module

3.15.1 Layer rules

LNDEV

Name	Description	Value	Unit
B1LD	LNDEV overlap of HVGOX, HVNWELL, HVPWELL, HNW, DNC, DPC, PDD, SCI or DEPL is not allowed	-	-
B2LD	LNDEV overlap of rnw3, rdn3, rdp3, qpva3, qpvb3 or qpvc3 is not allowed	-	-
B3LD	LNDEV overlap of LVT or SVT is not allowed	-	-
S1LDGA	Minimum LNDEV spacing to GATE	0.35	µm
S1LDHN	Minimum LNDEV spacing to HVNWELL	3.0	µm
S1LDHP	Minimum LNDEV spacing to HVPWELL	3.0	µm
S1LDHW	Minimum LNDEV spacing to HNW	10.0	µm
S1LDND	Minimum LNDEV spacing to NDF	10.0	µm
S1LDWD	Minimum LNDEV spacing to DNWELL	10.0	µm
S1LDWM	Minimum LNDEV spacing to DNWELLMV	3.5	µm
	Note: Only valid if DNWELLMV is outside DNWELL.		
S2LDGA	Minimum LNDEV spacing to GATE (in GATE length direction)	0.46	µm
E1LDGA	Minimum LNDEV enclosure of GATE	0.35	µm
E2LDGA	Minimum LNDEV enclosure of GATE (in GATE length direction)	0.46	µm

3. Layer and Device rules → 3.15 LNPMOS3 module → 3.15.1 Layer rules → LNDEV

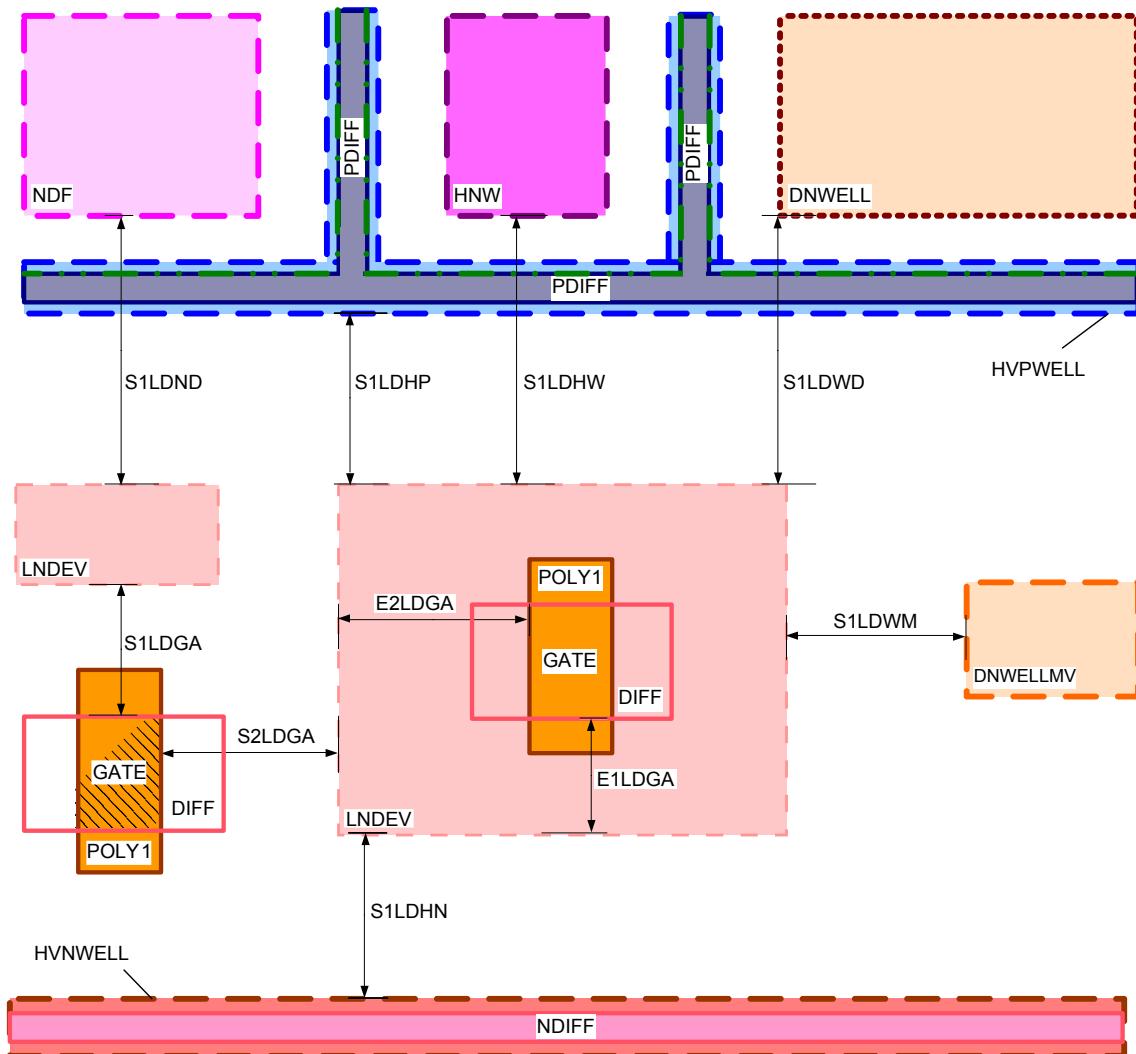


Figure 3.114 LNDEV

3. Layer and Device rules → 3.15 LNPMOS3 module → 3.15.2 Device rules → pe3In

3.15.2 Device rules

pe3In

Name	Description	Value	Unit
W3DF	Minimum GATE width	0.22	μm
	Note: The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) having smaller GATE width than 0.22μm.		
W9P1	Minimum GATE length	0.5	μm

Note: MV is necessary for pe3In.

Note: For more extensive LVS, it is recommended to use the related 5 terminal device.

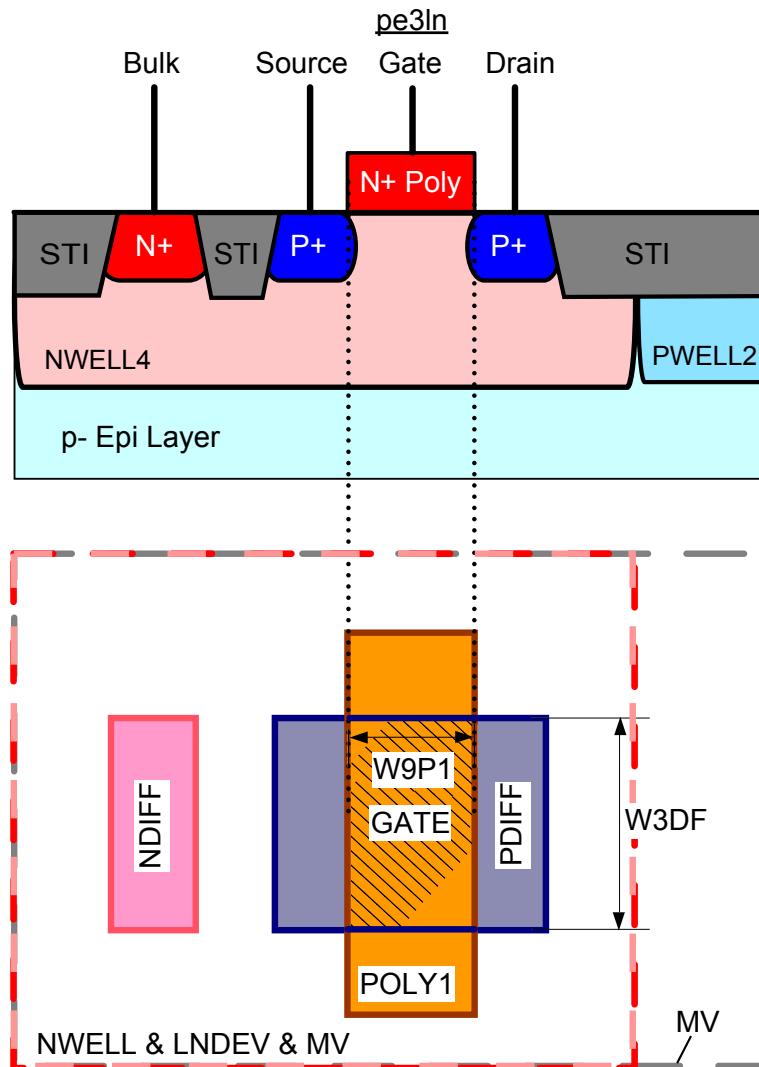


Figure 3.115 pe3In

3. Layer and Device rules → 3.15 LNPMOS3 module → 3.15.2 Device rules → pe3In_5

pe3In_5

Name	Description	Value	Unit
W3DF	Minimum GATE width	0.22	μm
	Note: The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) having smaller GATE width than 0.22μm.		
W9P1	Minimum GATE length	0.5	μm

Note: pe3In_5 device must be labeled "5T" using POLY1 (VERIFICATION) layer over the GATE.

Note: MV is necessary for pe3In_5.

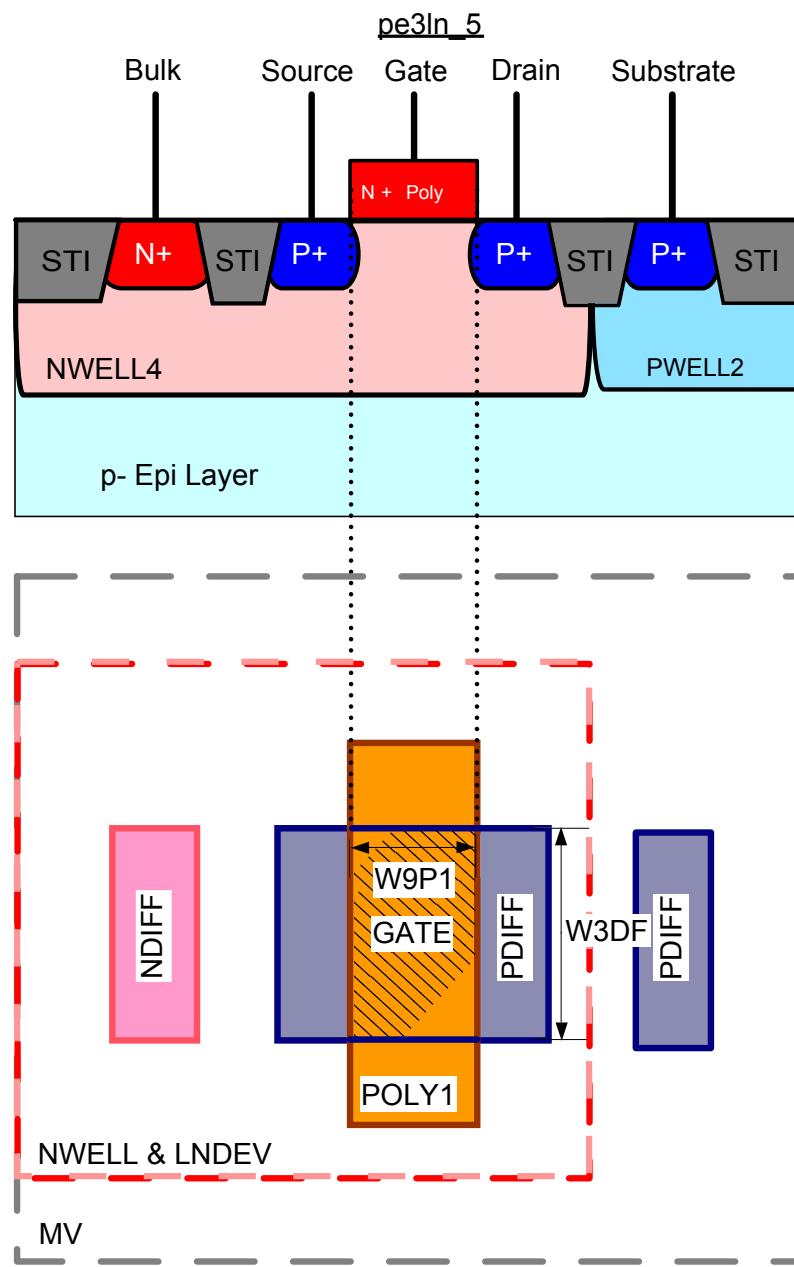


Figure 3.116 pe3In_5

3. Layer and Device rules → 3.15 LNPMOS3 module → 3.15.2 Device rules → pe3lni

pe3lni

Name	Description	Value	Unit
W3DF	Minimum GATE width	0.22	μm
	Note: The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) having smaller GATE width than 0.22μm.		
W9P1	Minimum GATE length	0.5	μm

Note: MV is necessary for pe3lni.

Note: pe3lni may be placed in DNWELLMV or DNWELL. Please take care of the different well edge design rules for both cases. For DNWELL the HVMOS Module is needed. (Drawing on this page is only for pe3lni in DNWELLMV)

Note: For more extensive LVS, it is recommended to use the related 5 terminal device.

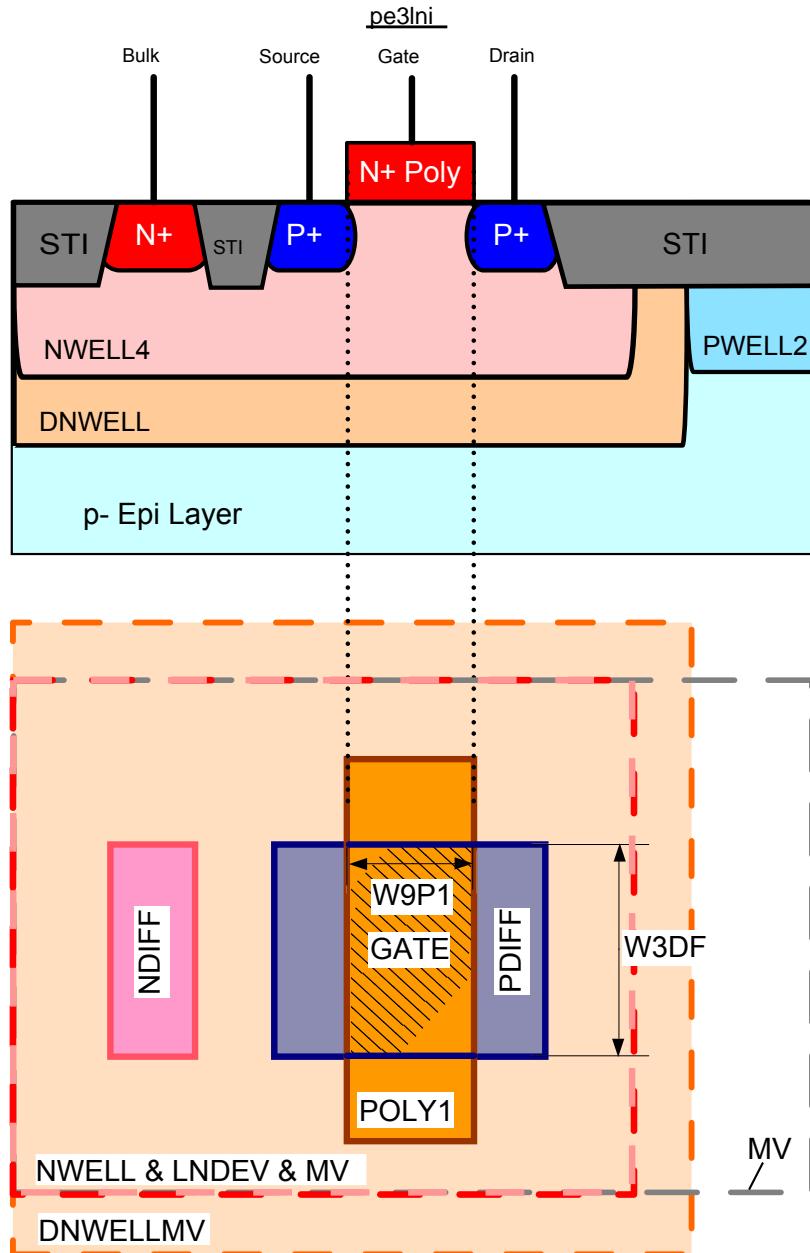


Figure 3.117 pe3lni

3. Layer and Device rules → 3.15 LNPMOS3 module → 3.15.2 Device rules → pe3Ini_5

pe3Ini_5

Name	Description	Value	Unit
W3DF	Minimum GATE width	0.22	μm
	Note: The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) having smaller GATE width than 0.22μm.		
W9P1	Minimum GATE length	0.5	μm

Note: pe3Ini_5 device must be labeled "5T" using POLY1 (VERIFICATION) layer over the GATE.

Note: MV is necessary for pe3Ini_5.

Note: pe3Ini_5 is placed in DNWELLMV and DNWELL. Please take care of the well edge design rules.

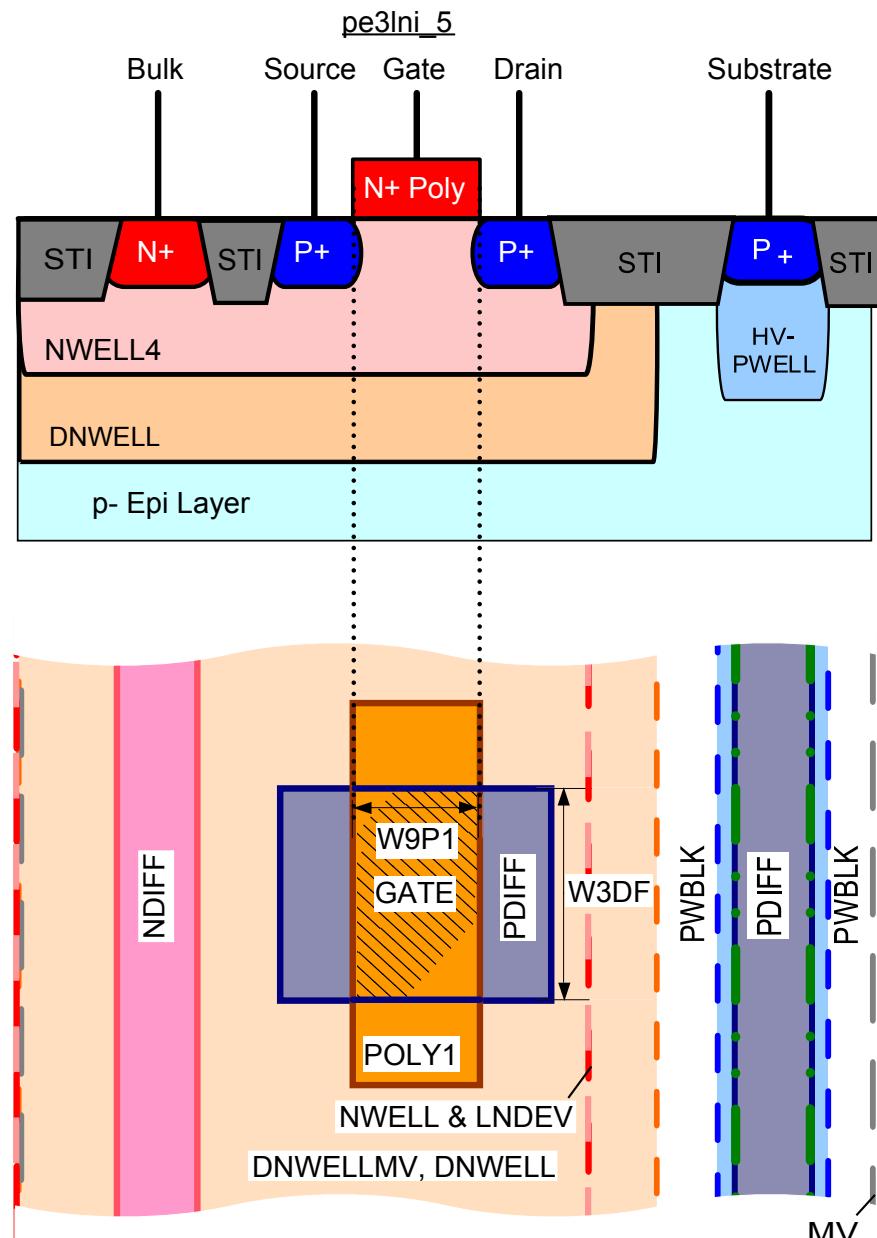


Figure 3.118 pe3Ini_5

3. Layer and Device rules → 3.15 LNPMOS3 module → 3.15.2 Device rules → pe3Ini_m_5

pe3Ini_m_5

Name	Description	Value	Unit
W3DF	Minimum GATE width	0.22	μm
	Note: The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) having smaller GATE width than 0.22μm.		
W9P1	Minimum GATE length	0.5	μm

Note: pe3Ini_m_5 device must be labeled "5T" using POLY1 (VERIFICATION) layer over the GATE.

Note: MV is necessary for pe3Ini_m_5.

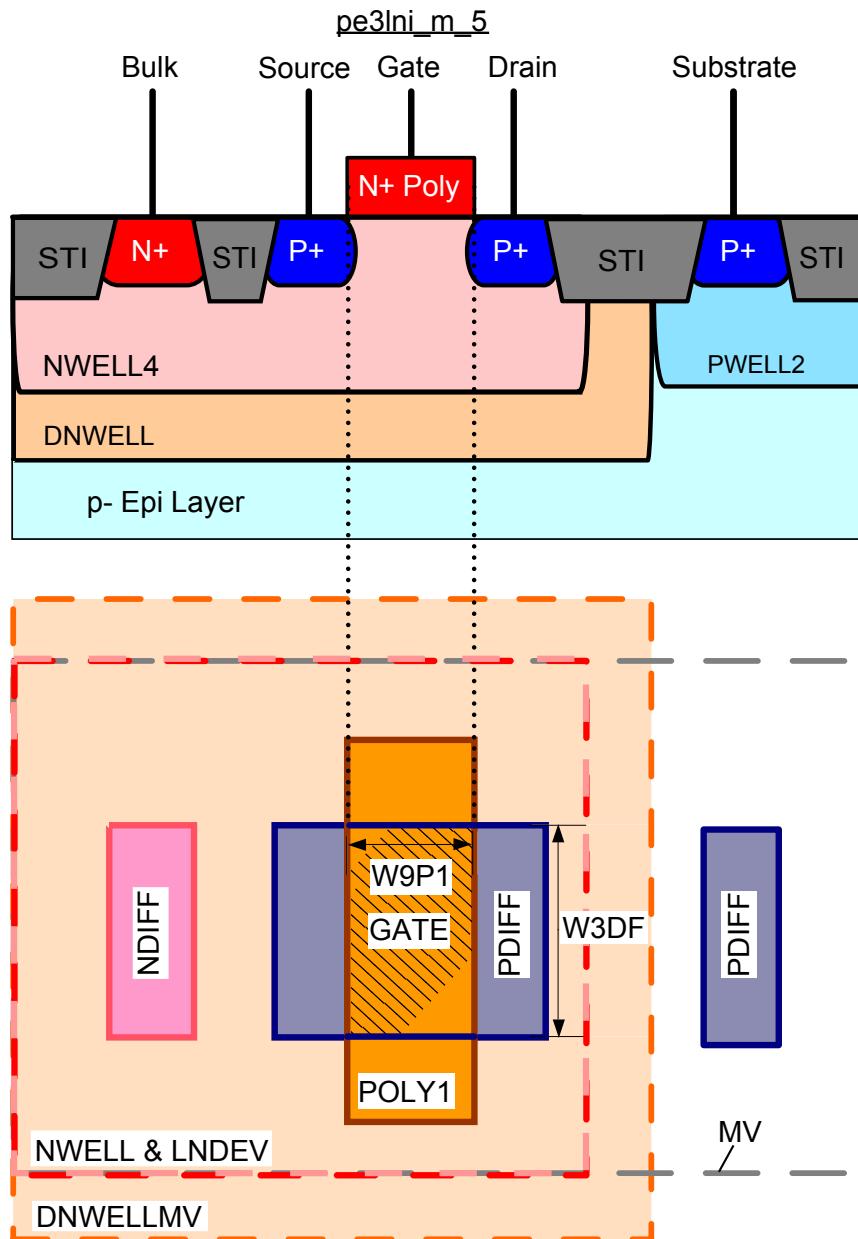


Figure 3.119 pe3Ini_m_5

3. Layer and Device rules → 3.16 ULN module

3.16 ULN module

3.16.1 Layer rules

ULN

Name	Description	Value	Unit
B1UL	ULN overlap of PWBLK, HVGOX, HVNWELL, HVPWELL, HNW, DNC, DPC, PDD, SCI, DEPL, LVT, SVT, LNDEV, CATDOP or ANODOP is not allowed	-	-
B1ULSB	ULN overlap of SBLK is not allowed	-	-
B2UL	ULN overlap of rpp1#, rnp1#, rpp1s#, MRES or HRES is not allowed	-	-
W1UL	Minimum ULN width	0.44	μm
S1UL	Minimum ULN spacing / notch	0.44	μm
S1ULGA	Minimum ULN spacing to GATE	0.35	μm
S1ULSB	Minimum ULN spacing to SBLK	0.35	μm
E1ULGA	Minimum ULN enclosure of GATE	0.35	μm

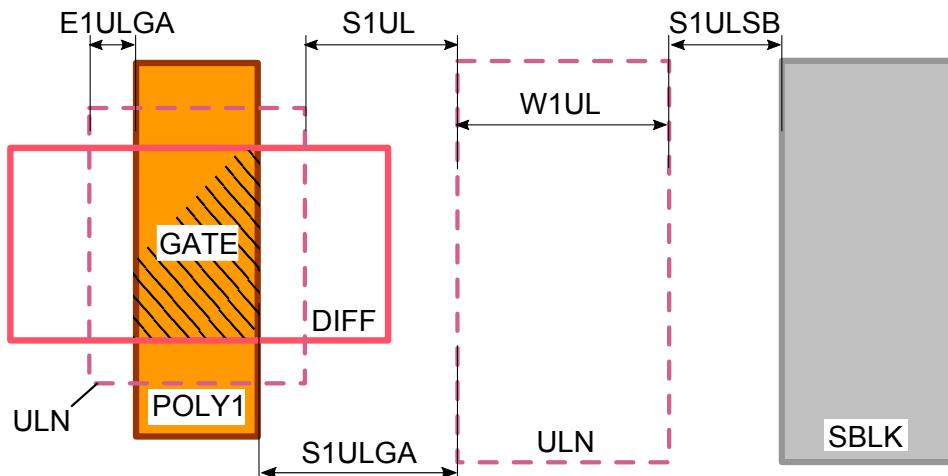


Figure 3.120 ULN

3. Layer and Device rules → 3.16 ULN module→ 3.16.2 Device rules→ nelna

3.16.2 Device rules

nelna

Name	Description	Value	Unit
W3DF	Minimum GATE width	0.22	μm
	Note: The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) having smaller GATE width than 0.22μm.		
W4P1	Minimum GATE length	0.18	μm
	Note: The design rule check error message W4P1 is also used generally for GATE areas (of any devices or shapes) being smaller than 0.18μm at any dimension.		

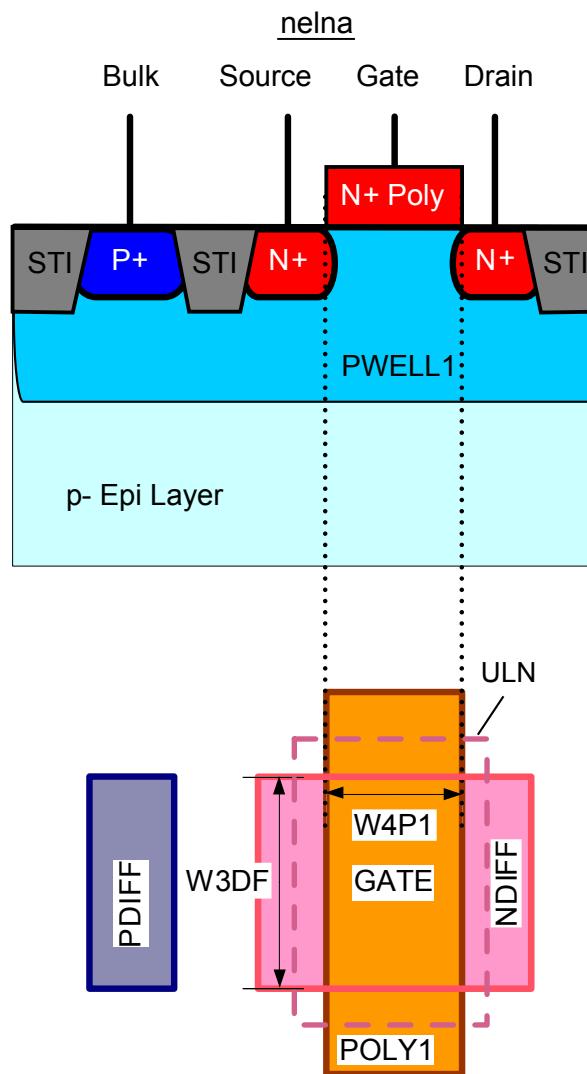


Figure 3.121 nelna

3. Layer and Device rules → 3.16 ULN module→ 3.16.2 Device rules→ nelnai

nelnai

Name	Description	Value	Unit
W3DF	Minimum GATE width	0.22	μm
	Note: The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) having smaller GATE width than 0.22μm.		
W4P1	Minimum GATE length	0.18	μm
	Note: The design rule check error message W4P1 is also used generally for GATE areas (of any devices or shapes) being smaller than 0.18μm at any dimension.		

Note: For more extensive LVS, it is recommended to use the related 6 terminal device.

Note: nelnai may be placed in either DNWELLMV or DNWELL. Please take care of the different well edge design rules for both cases. For DNWELL the HVMOS Module is needed.

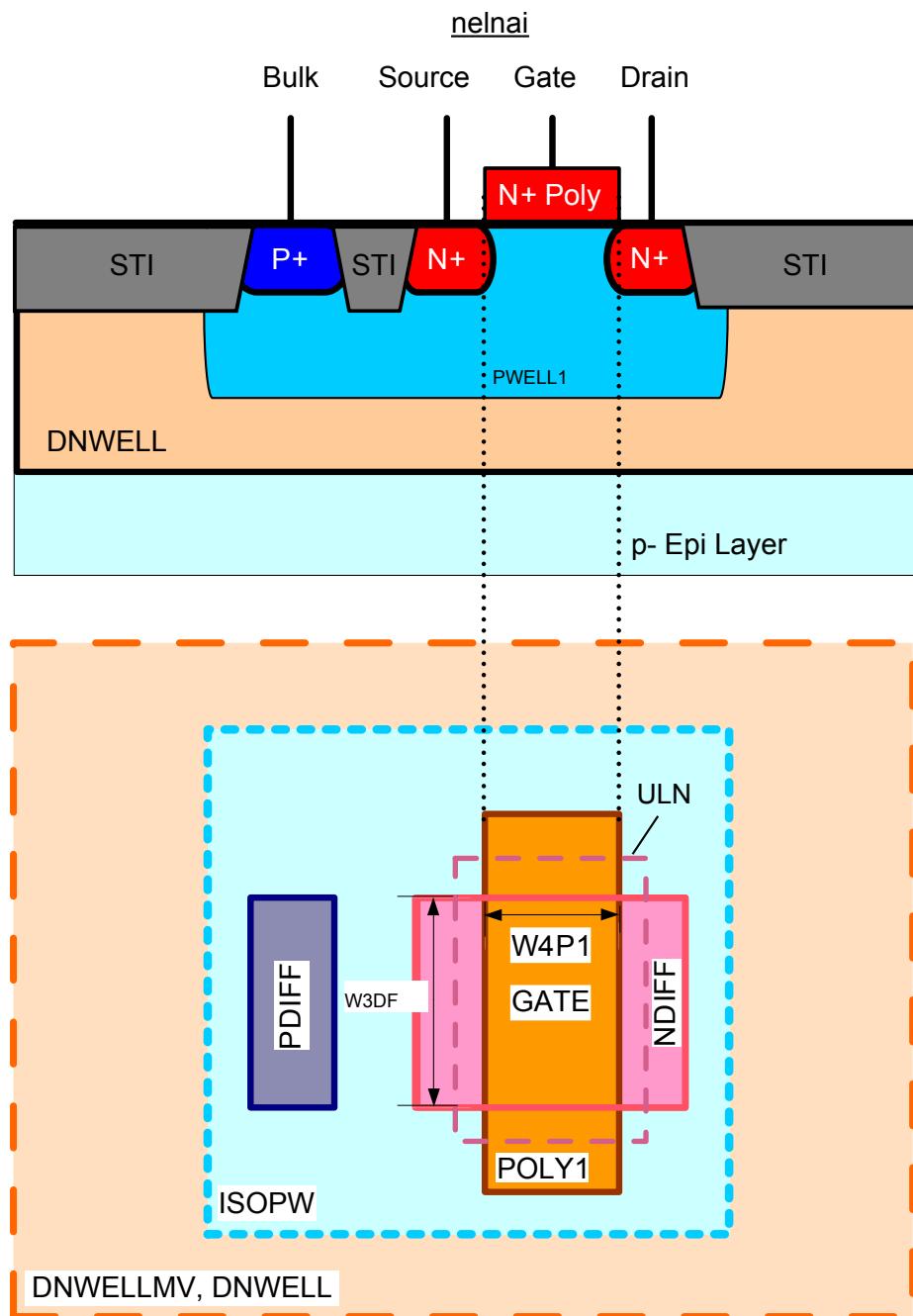


Figure 3.122 nelnai

3. Layer and Device rules → 3.16 ULN module→ 3.16.2 Device rules→ nelnai_6

nelnai_6

Name	Description	Value	Unit
W3DF	Minimum GATE width	0.22	μm
	Note: The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) having smaller GATE width than 0.22μm.		
W4P1	Minimum GATE length	0.18	μm
	Note: The design rule check error message W4P1 is also used generally for GATE areas (of any devices or shapes) being smaller than 0.18μm at any dimension.		

Note: nelnai_6 is placed in DNWELLMV and DNWELL. Please take care of the well edge design rules.

Note: nelnai_6 device must be labeled "6T" using POLY1 (VERIFICATION) layer over the GATE.

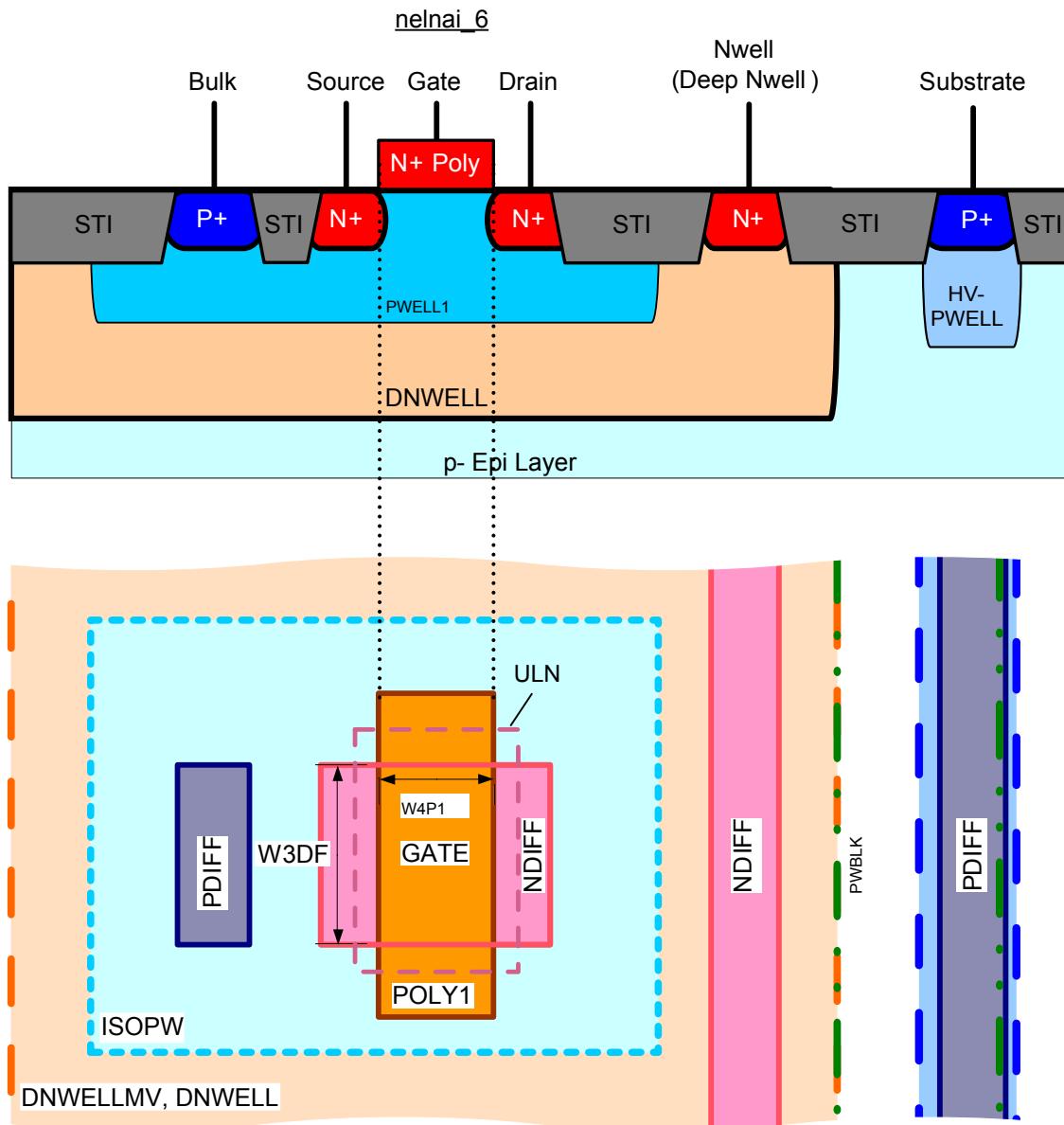


Figure 3.123 nelnai_6

3. Layer and Device rules → 3.16 ULN module→ 3.16.2 Device rules→ nelnai_m_6

nelnai_m_6

Name	Description	Value	Unit
W3DF	Minimum GATE width	0.22	μm
	Note: The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) having smaller GATE width than 0.22μm.		
W4P1	Minimum GATE length	0.18	μm
	Note: The design rule check error message W4P1 is also used generally for GATE areas (of any devices or shapes) being smaller than 0.18μm at any dimension.		

Note: nelnai_m_6 device must be labeled “6T” using POLY1 (VERIFICATION) layer over the GATE.

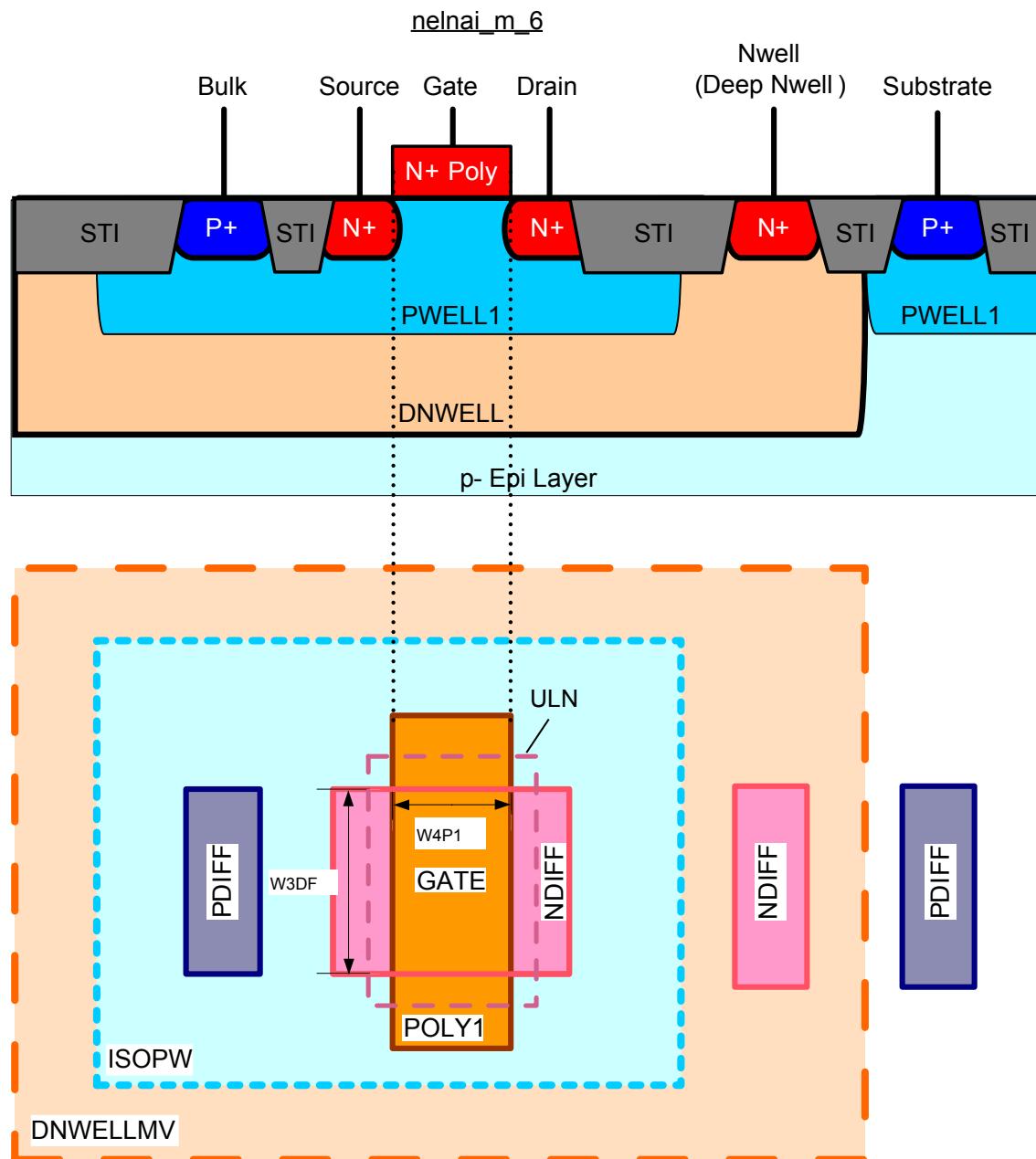


Figure 3.124 nelnai_m_6

3. Layer and Device rules → 3.16 ULN module→ 3.16.2 Device rules→ ne3lna

ne3lna

Name	Description	Value	Unit
W10P1	Minimum GATE length	0.35	μm
W3DF	Minimum GATE width	0.22	μm
Note: The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) having smaller GATE width than 0.22μm.			

Note: MV is necessary for ne3lna.

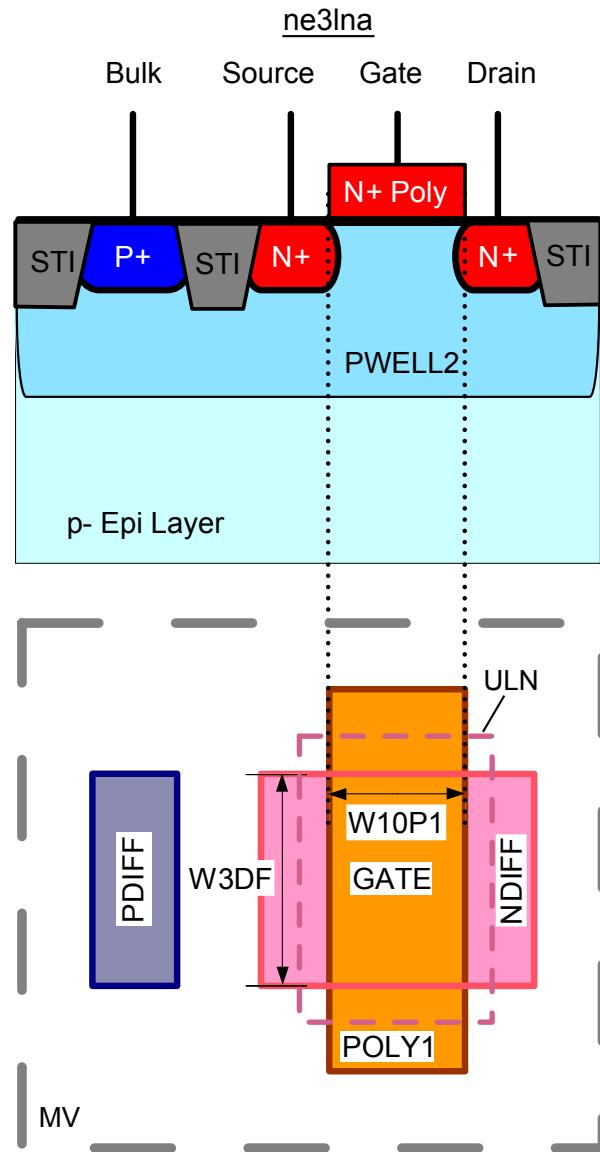


Figure 3.125 ne3lna

3. Layer and Device rules → 3.16 ULN module→ 3.16.2 Device rules→ ne3lnai, pe3lnai

ne3lnai, pe3lnai

Name	Description	Value	Unit
W10P1	Minimum GATE length	0.35	μm
W11P1	Minimum GATE length	0.3	μm
W3DF	Minimum GATE width	0.22	μm
Note: The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) having smaller GATE width than 0.22μm.			

Note: For more extensive LVS, it is recommended to use the related 5 or 6 terminal device.

Note: MV is necessary for ne3lnai and pe3lnai.

Note: ne3lnai and pe3lnai may be placed in DNWELLMV or DNWELL. Please take care of the different well edge design rules for both cases. For DNWELL the HVMOS Module is needed. (Drawing on this page is only for ne3lnai and pe3lnai in DNWELLMV)

Note: MV is necessary for pe3lnai.

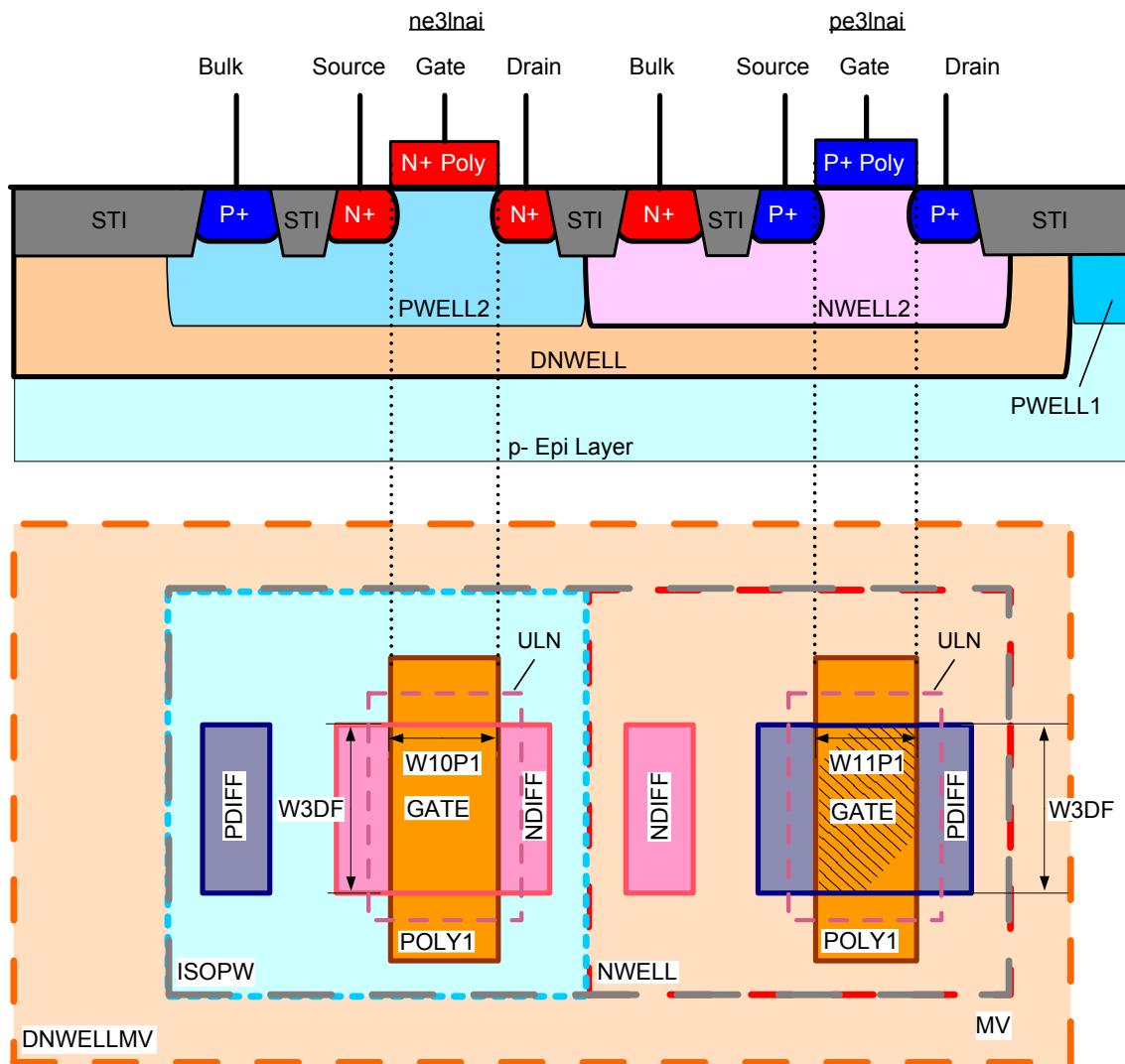


Figure 3.126 ne3lnai, pe3lnai

3. Layer and Device rules → 3.16 ULN module→ 3.16.2 Device rules→ ne3lnai_6

ne3lnai_6

Name	Description	Value	Unit
W10P1	Minimum GATE length	0.35	μm
W3DF	Minimum GATE width	0.22	μm
Note: The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) having smaller GATE width than 0.22μm.			

Note: MV is necessary for ne3lnai_6.

Note: ne3lnai_6 is placed in DNWELLMV and DNWELL. Please take care of the well edge design rules.

Note: ne3lnai_6 device must be labeled "6T" using POLY1 (VERIFICATION) layer over the GATE.

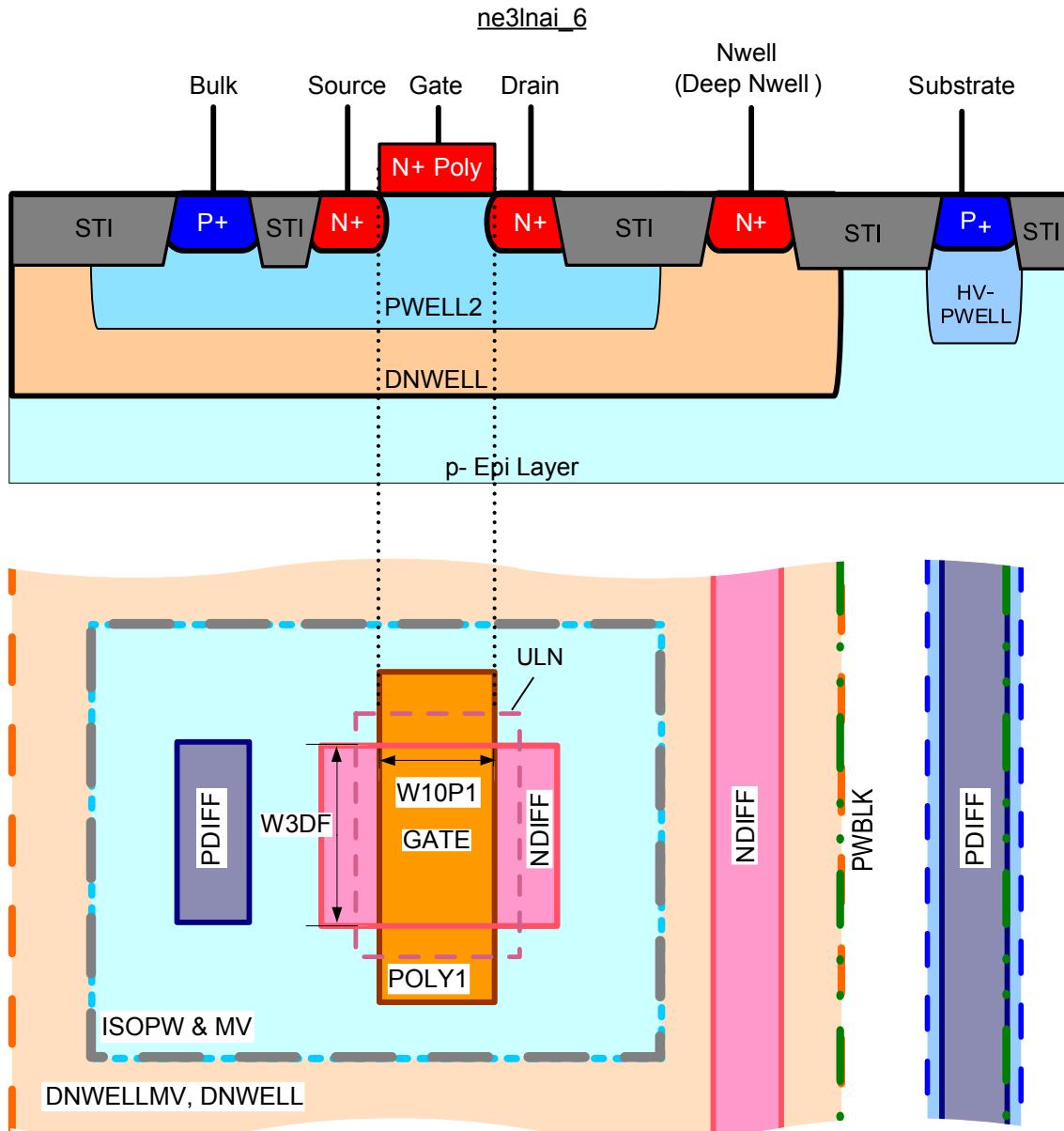


Figure 3.127 ne3lnai_6

3. Layer and Device rules → 3.16 ULN module → 3.16.2 Device rules → ne3lnai_m_6

ne3lnai_m_6

Name	Description	Value	Unit
W10P1	Minimum GATE length	0.35	μm
W3DF	Minimum GATE width	0.22	μm
Note: The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) having smaller GATE width than 0.22μm.			

Note: MV is necessary for ne3lnai_m_6.

Note: ne3lnai_m_6 device must be labeled "6T" using POLY1 (VERIFICATION) layer over the GATE.

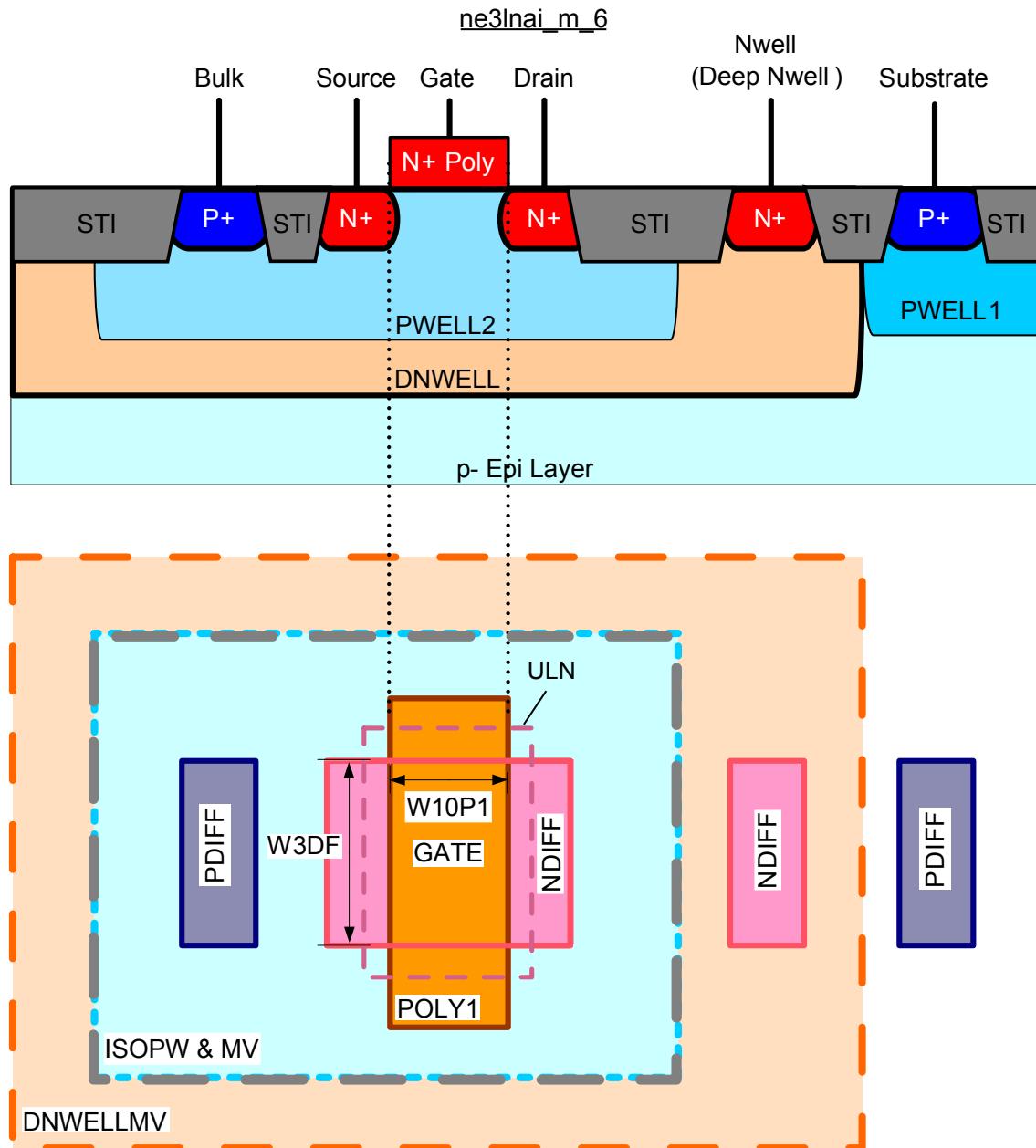


Figure 3.128 ne3lnai_m_6

3. Layer and Device rules → 3.16 ULN module→ 3.16.2 Device rules→ pe3lna

pe3lna

Name	Description	Value	Unit
W11P1	Minimum GATE length	0.3	μm
W3DF	Minimum GATE width	0.22	μm
Note: The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) having smaller GATE width than 0.22μm.			

Note: MV is necessary for pe3lna.

Note: For more extensive LVS, it is recommended to use the related 5 or 6 terminal device.

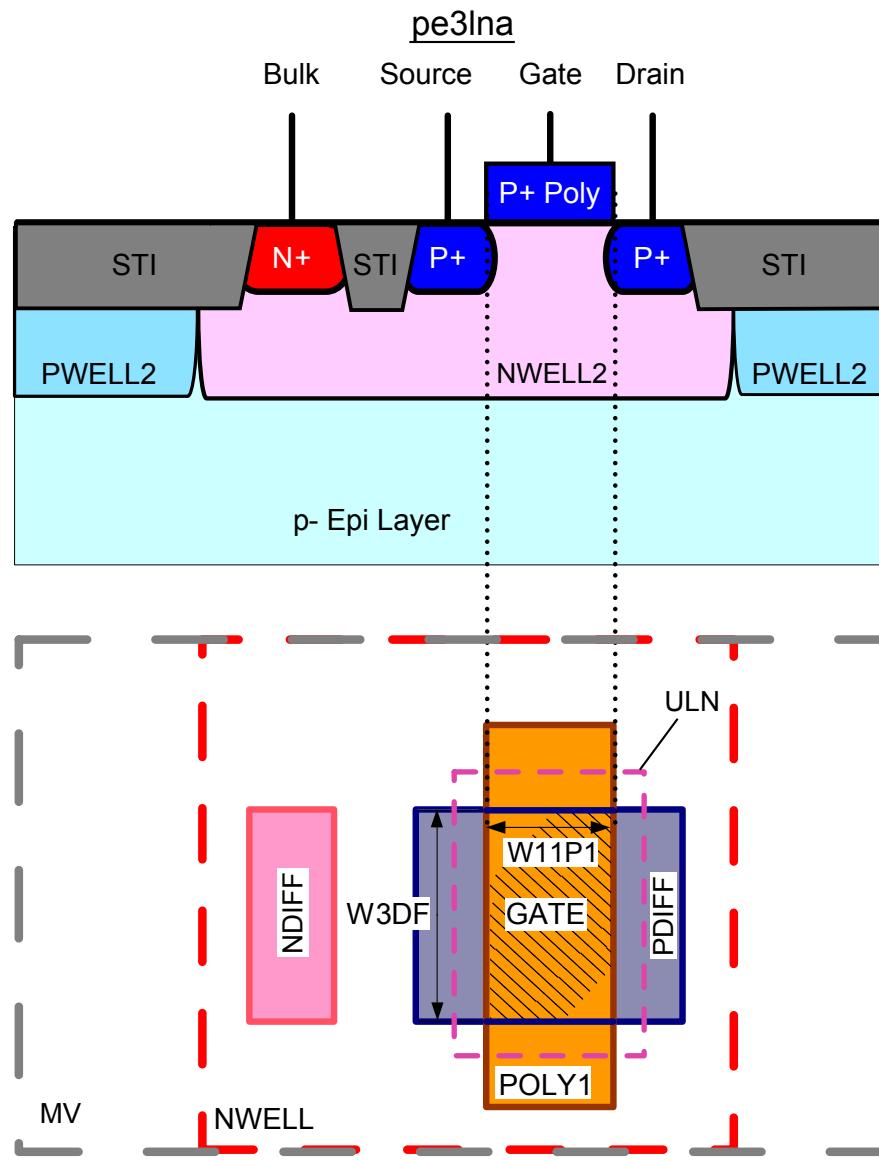


Figure 3.129 pe3lna

3. Layer and Device rules → 3.16 ULN module→ 3.16.2 Device rules→ pe3lna_5

pe3lna_5

Name	Description	Value	Unit
W11P1	Minimum GATE length	0.3	μm
W3DF	Minimum GATE width	0.22	μm
Note: The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) having smaller GATE width than 0.22μm.			

Note: MV is necessary for pe3lna_5.

Note: pe3lna_5 device must be labeled "5T" using POLY1 (VERIFICATION) layer over the GATE.

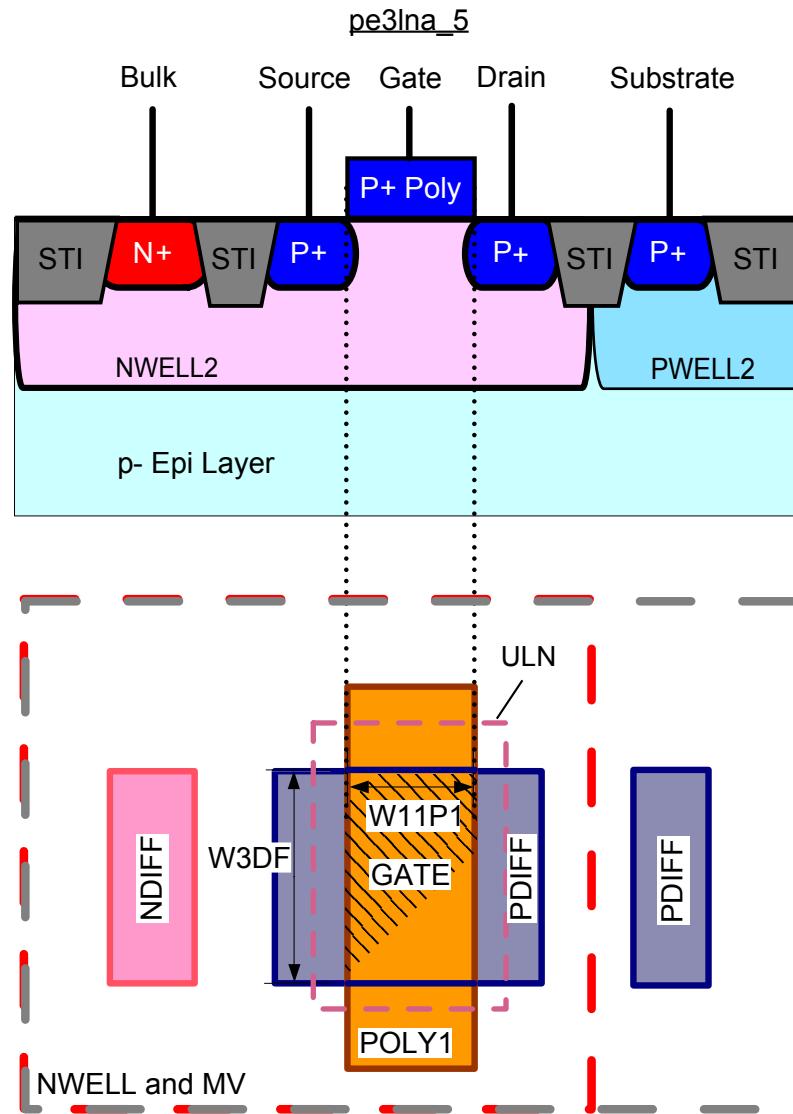


Figure 3.130 pe3lna_5

3. Layer and Device rules → 3.16 ULN module→ 3.16.2 Device rules→ pe3lnai_5

pe3lnai_5

Name	Description	Value	Unit
W11P1	Minimum GATE length	0.3	μm
W3DF	Minimum GATE width	0.22	μm
Note: The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) having smaller GATE width than 0.22μm.			

Note: MV is necessary for pe3lnai_5.

Note: pe3lnai_5 device must be labeled "5T" using POLY1 (VERIFICATION) layer over the GATE.

Note: pe3lnai_5 is placed in DNWELLMV and DNWELL. Please take care of the well edge design rules.

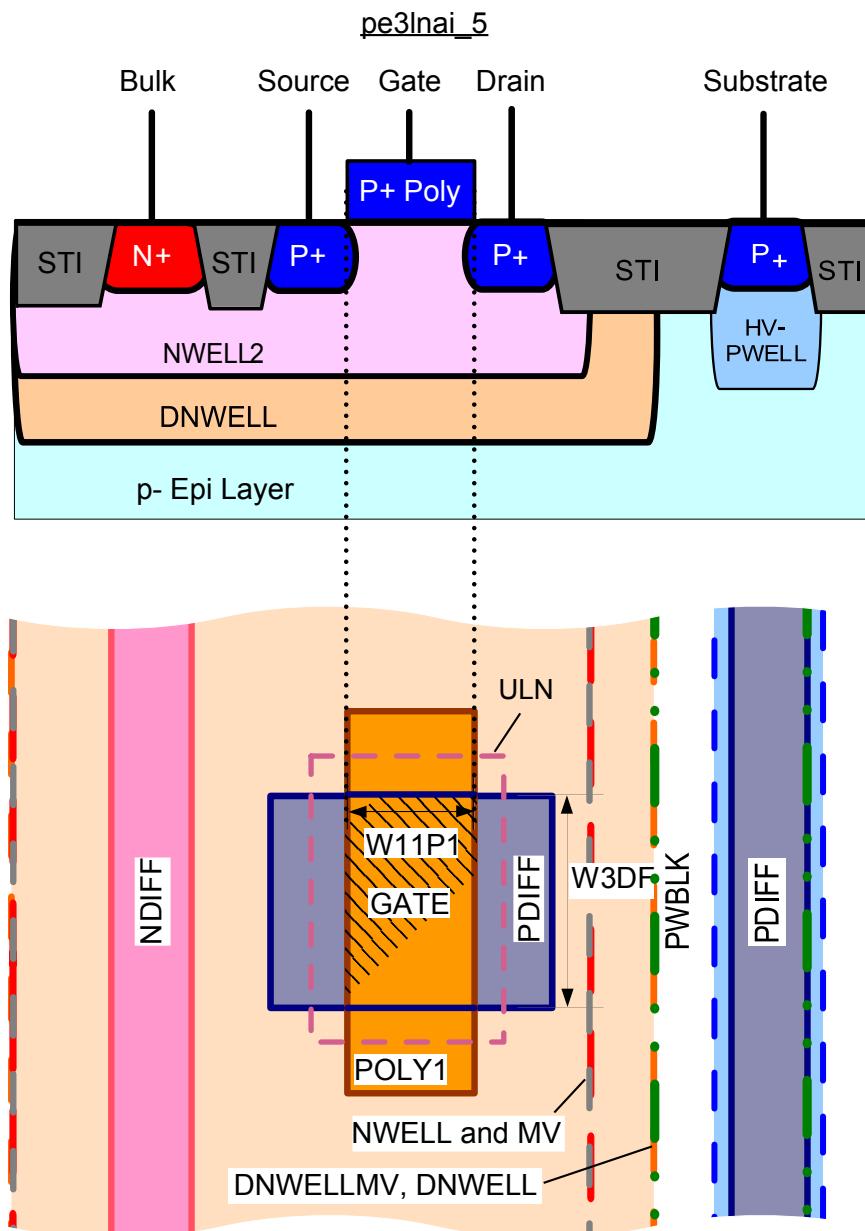


Figure 3.131 pe3lnai_5

3. Layer and Device rules → 3.16 ULN module→ 3.16.2 Device rules→ pe3lnai_m_5

pe3lnai_m_5

Name	Description	Value	Unit
W11P1	Minimum GATE length	0.3	μm
W3DF	Minimum GATE width	0.22	μm
Note: The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) having smaller GATE width than 0.22μm.			

Note: MV is necessary for pe3lnai_m_5.

Note: pe3lnai_m_5 device must be labeled “5T” using POLY1 (VERIFICATION) layer over the GATE.

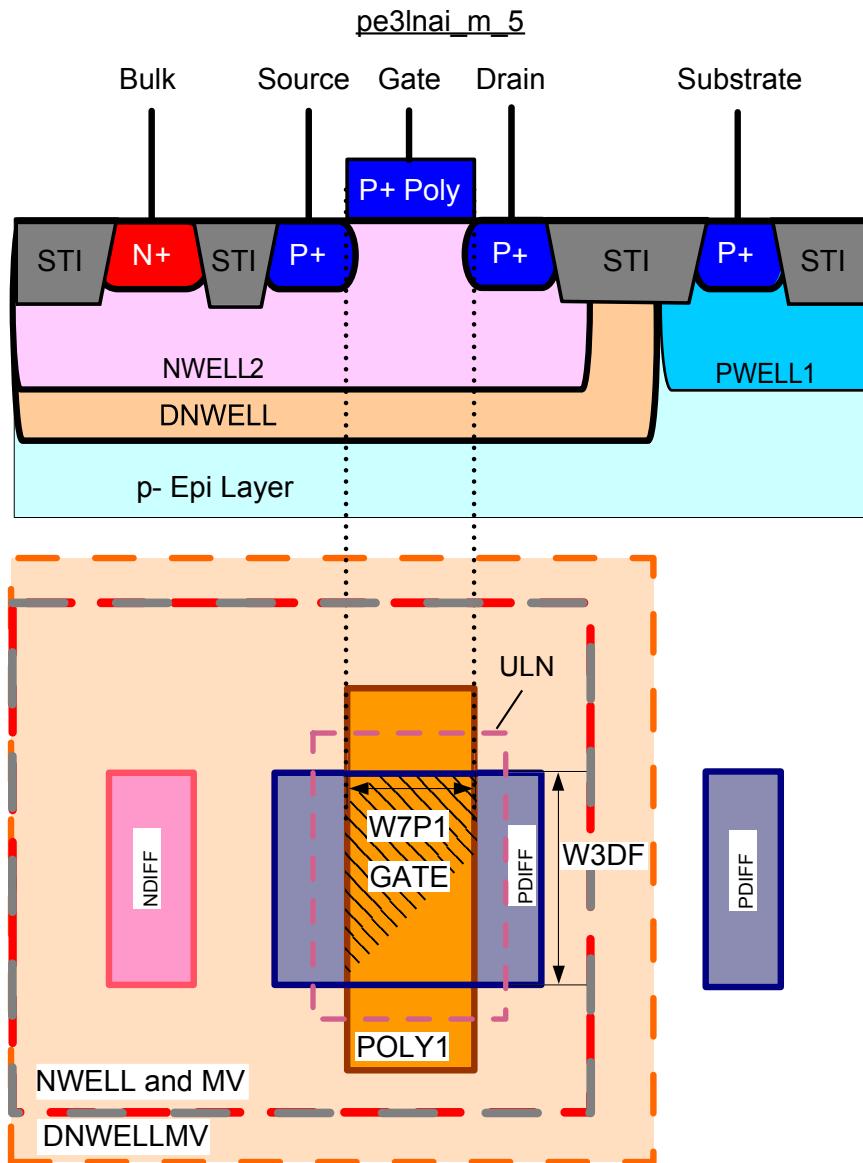


Figure 3.132 pe3lnai_m_5

3. Layer and Device rules → 3.17 DEPL module

3.17 DEPL module

3.17.1 Layer rules

DEPL

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1DL	DEPL overlap of HVGOX, NWELL, HVNWELL or HVPWELL is not allowed (except qnva, qnvb)	-	-
B3DL	DEPL NMOS transistor without MV is not allowed	-	-
B2DL	DEPL crossing DNWELLMV / DNWELL edge is not allowed	-	-
W1DL	Minimum DEPL width	1.0	μm
S1DL	Minimum DEPL spacing/notch	0.6	μm
S1DLGA	Minimum DEPL spacing to GATE	0.7	μm
S1DLHN	Minimum DEPL spacing to HVNWELL	3.0	μm
E1DLGA	Minimum DEPL extension beyond GATE	0.7	μm
O1DLPI	Fixed DEPL overlap of ISOPW (same potential)	0.05	μm

Note: Please refer to ISOWELL section for related DEPL in DNWELL and DEPL in DNWELLMV rules.

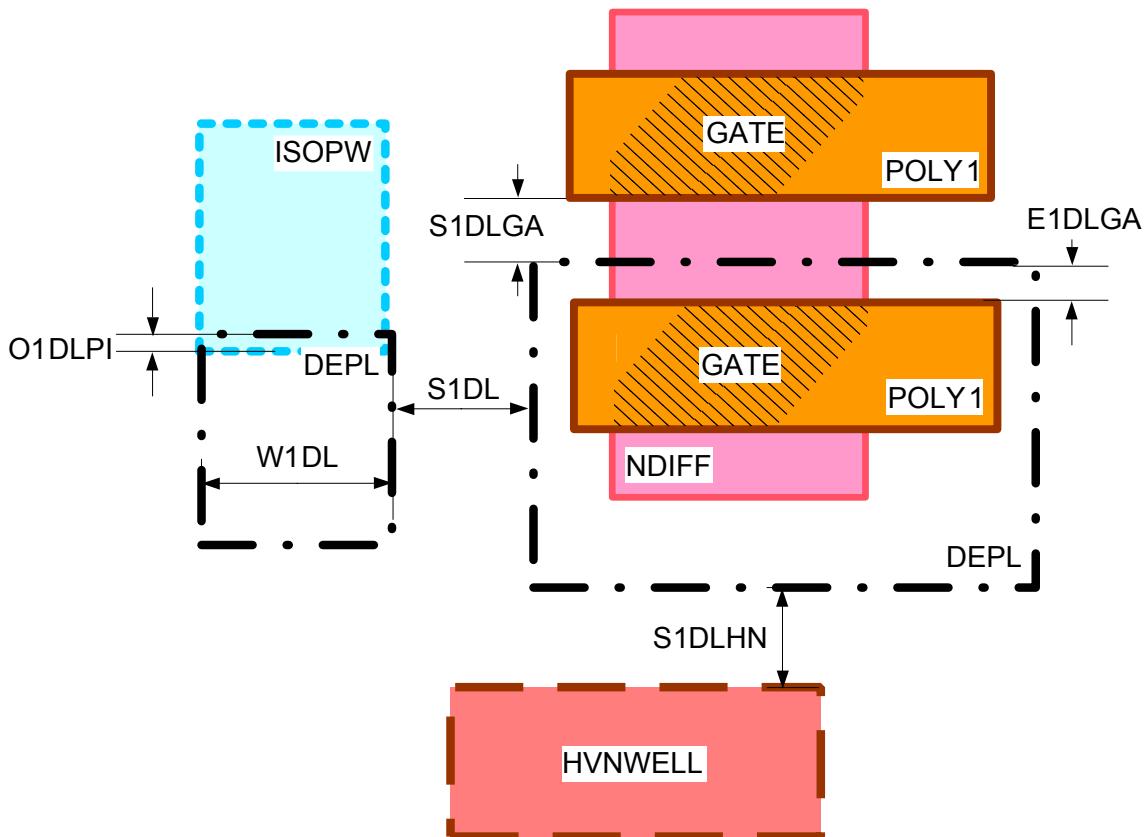


Figure 3.133 DEPL

3. Layer and Device rules → 3.17 DEPL module→ 3.17.2 Device rules→ nd3

3.17.2 Device rules

nd3

Name	Description	Value	Unit
W1GA	Minimum GATE length	0.7	μm
W2GA	Minimum GATE width	0.44	μm

Note: MV is necessary for nd3.

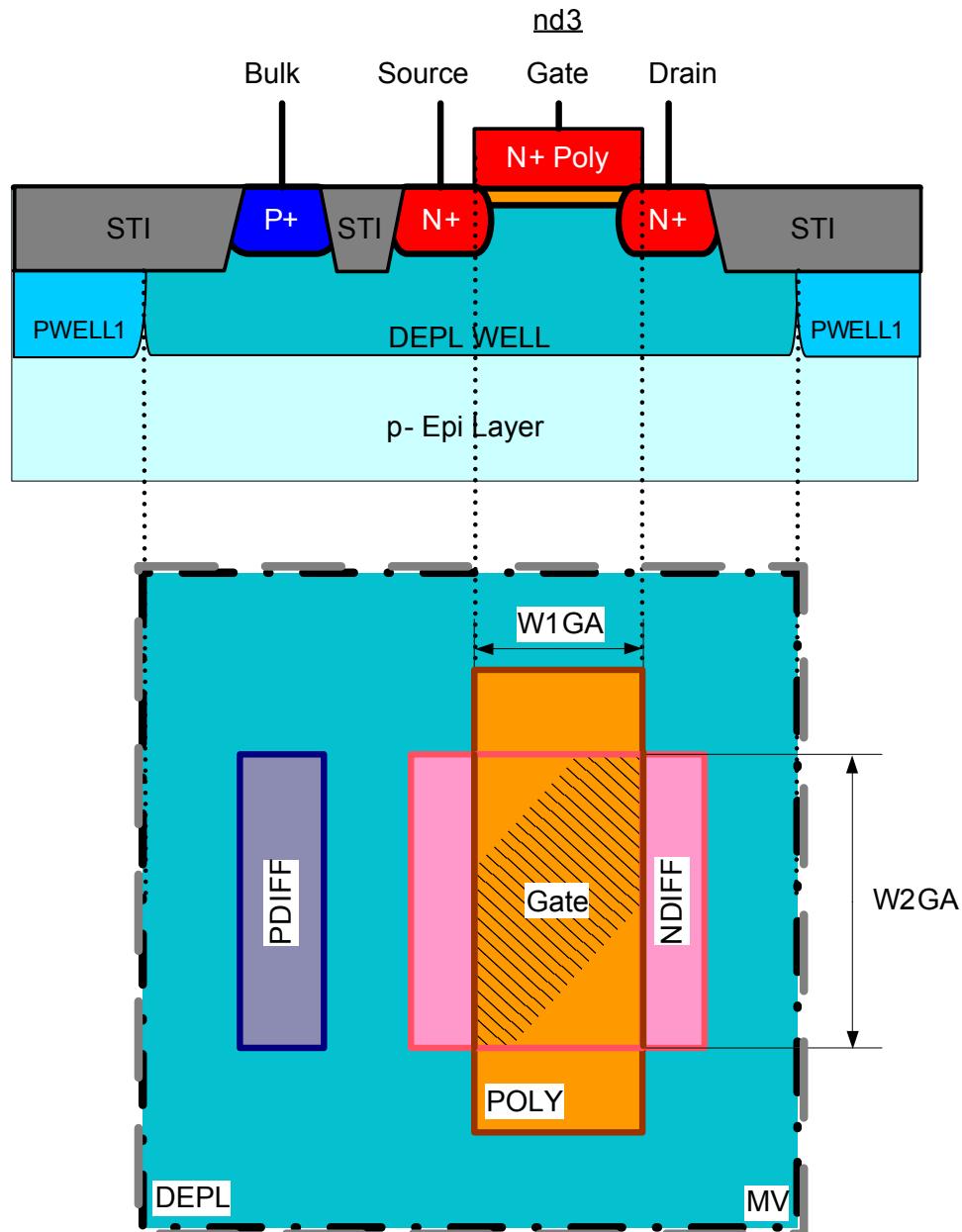


Figure 3.134 nd3

3. Layer and Device rules → 3.17 DEPL module→ 3.17.2 Device rules→ nd3i

nd3i

Name	Description	Value	Unit
W1GA	Minimum GATE length	0.7	μm
W2GA	Minimum GATE width	0.44	μm

Note: MV is necessary for nd3i.

Note: nd3i may be placed in either DNWELLMV or DNWELL. Please take care of the different well edge design rules for both cases. For DNWELL the HVMOS Module is needed. (Drawing on this page is only for nd3i in DNWELLMV)

Note: For more extensive LVS, it is recommended to use the related 6 terminal device.

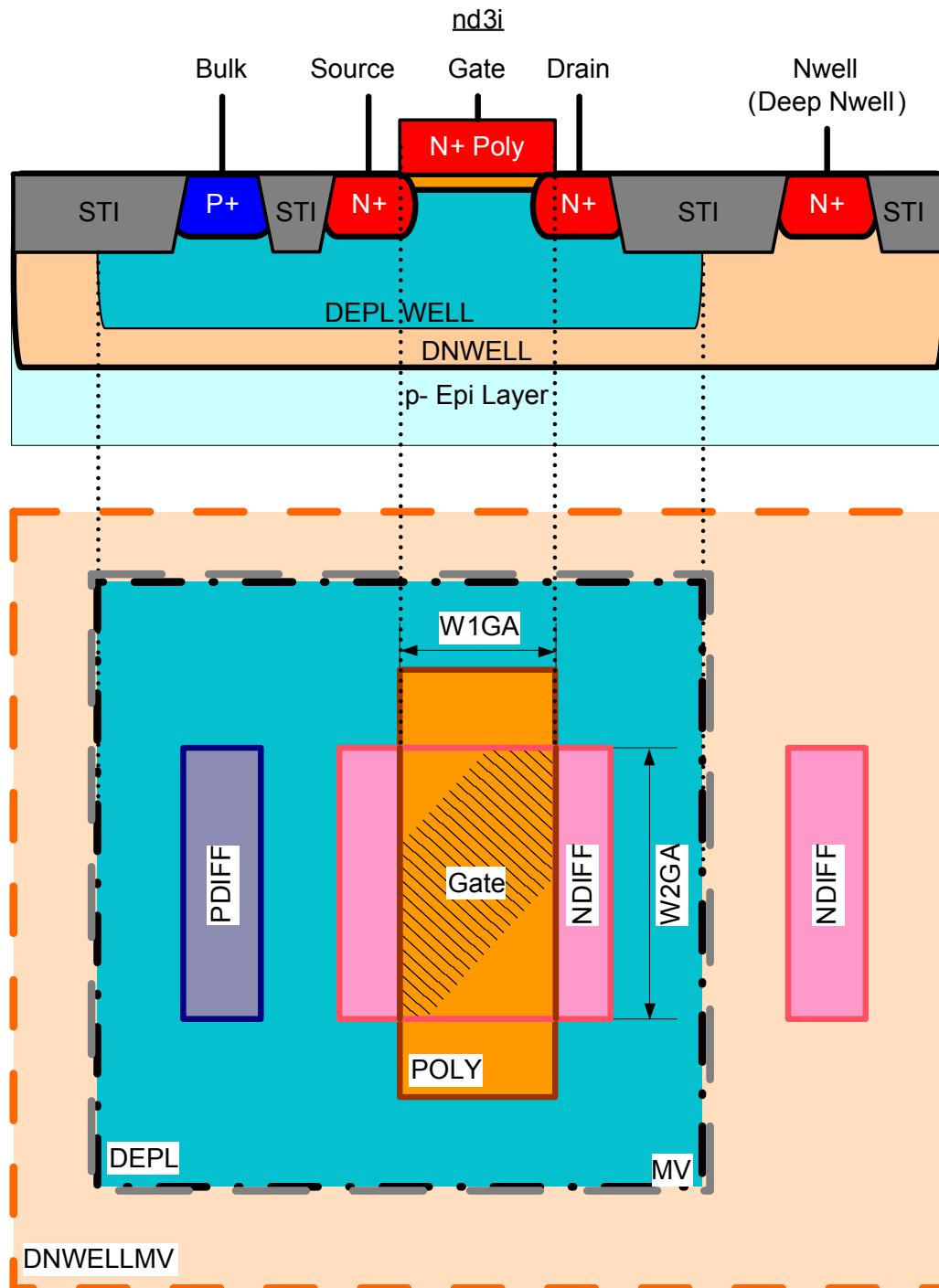


Figure 3.135 nd3i

3. Layer and Device rules → 3.17 DEPL module→ 3.17.2 Device rules→ nd3i_6

nd3i_6

Name	Description	Value	Unit
W1GA	Minimum GATE length	0.7	μm
W2GA	Minimum GATE width	0.44	μm

Note: MV is necessary for nd3i_6.

Note: nd3i_6 are placed in DNWELLMV and DNWELL. Please take care of the well edge design rules.

Note: nd3i_6 devices must be labeled "6T" using POLY1 (VERIFICATION) layer over the GATE.

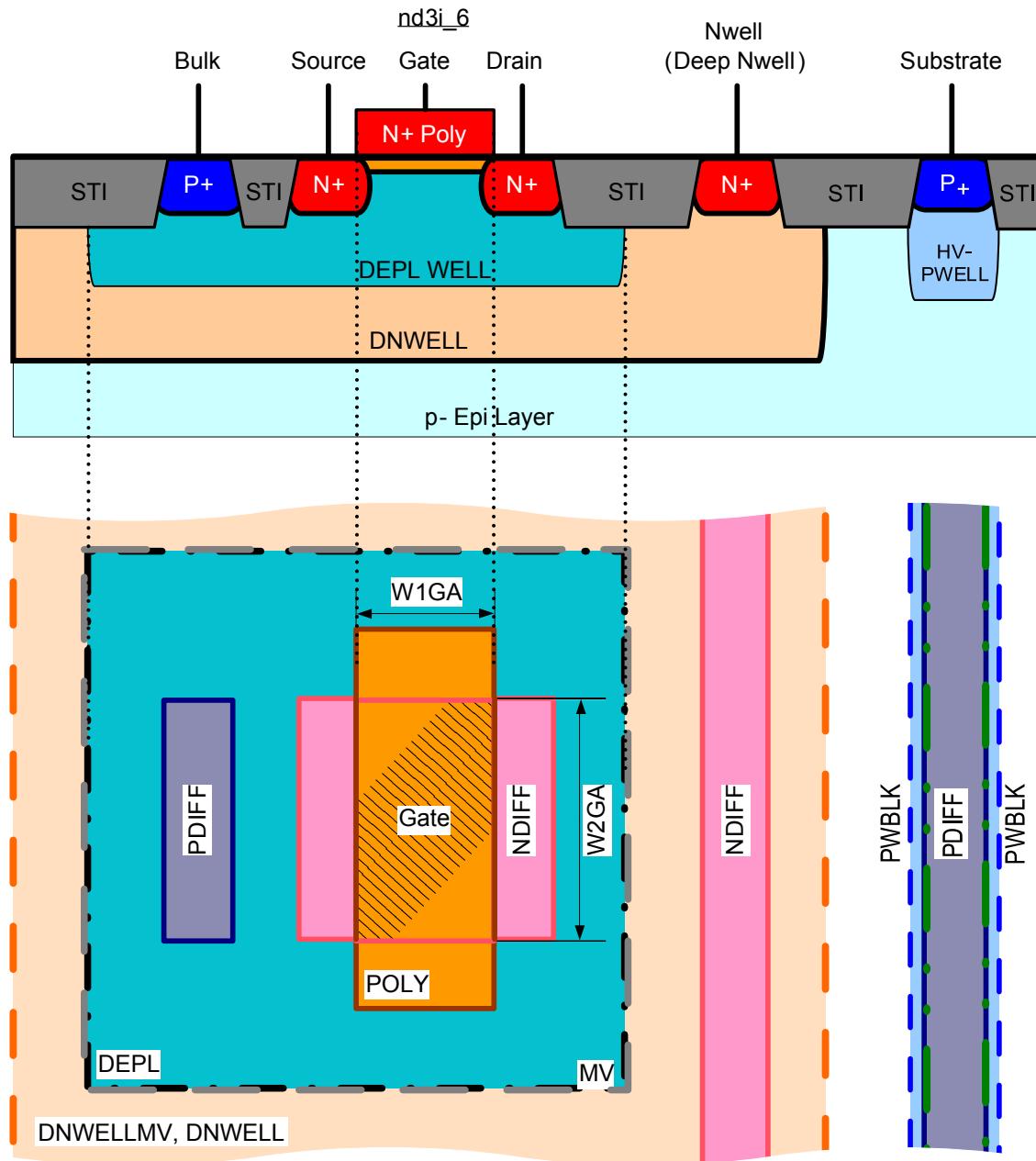


Figure 3.136 nd3i_6

3. Layer and Device rules → 3.17 DEPL module→ 3.17.2 Device rules→ nd3i_m_6

nd3i_m_6

Name	Description	Value	Unit
W1GA	Minimum GATE length	0.7	μm
W2GA	Minimum GATE width	0.44	μm

Note: MV is necessary for nd3i_m_6.

Note: nd3i_m_6 devices must be labeled “6T” using POLY1 (VERIFICATION) layer over the GATE.

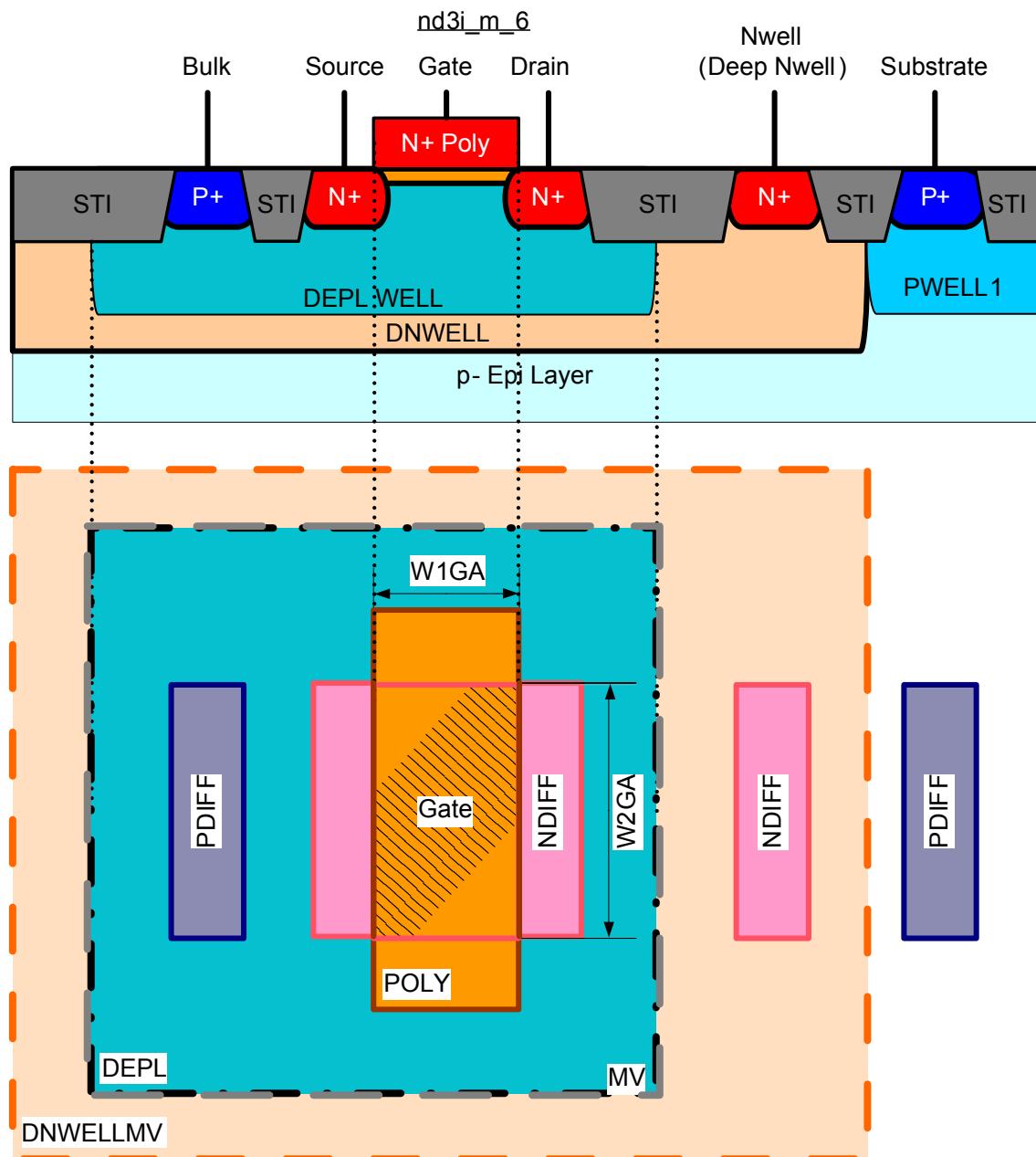


Figure 3.137 nd3i_m_6

3. Layer and Device rules → 3.17 DEPL module→ 3.17.2 Device rules→ qnva

qnva

Name	Description	Value	Unit
B4MV	MV overlap of qnva is not allowed	-	-
B5WD	qnva inside DNWELL is not allowed	-	-

Note: The layout of the qnva vertical bipolar NPN transistor is pre-defined and only the emitter length can be changed in the range of 2µm to 50µm. The drawing below is a basic sketch only and does not give all details.

Note: DEPL overlap of HVNWELL is only allowed for the qnva.

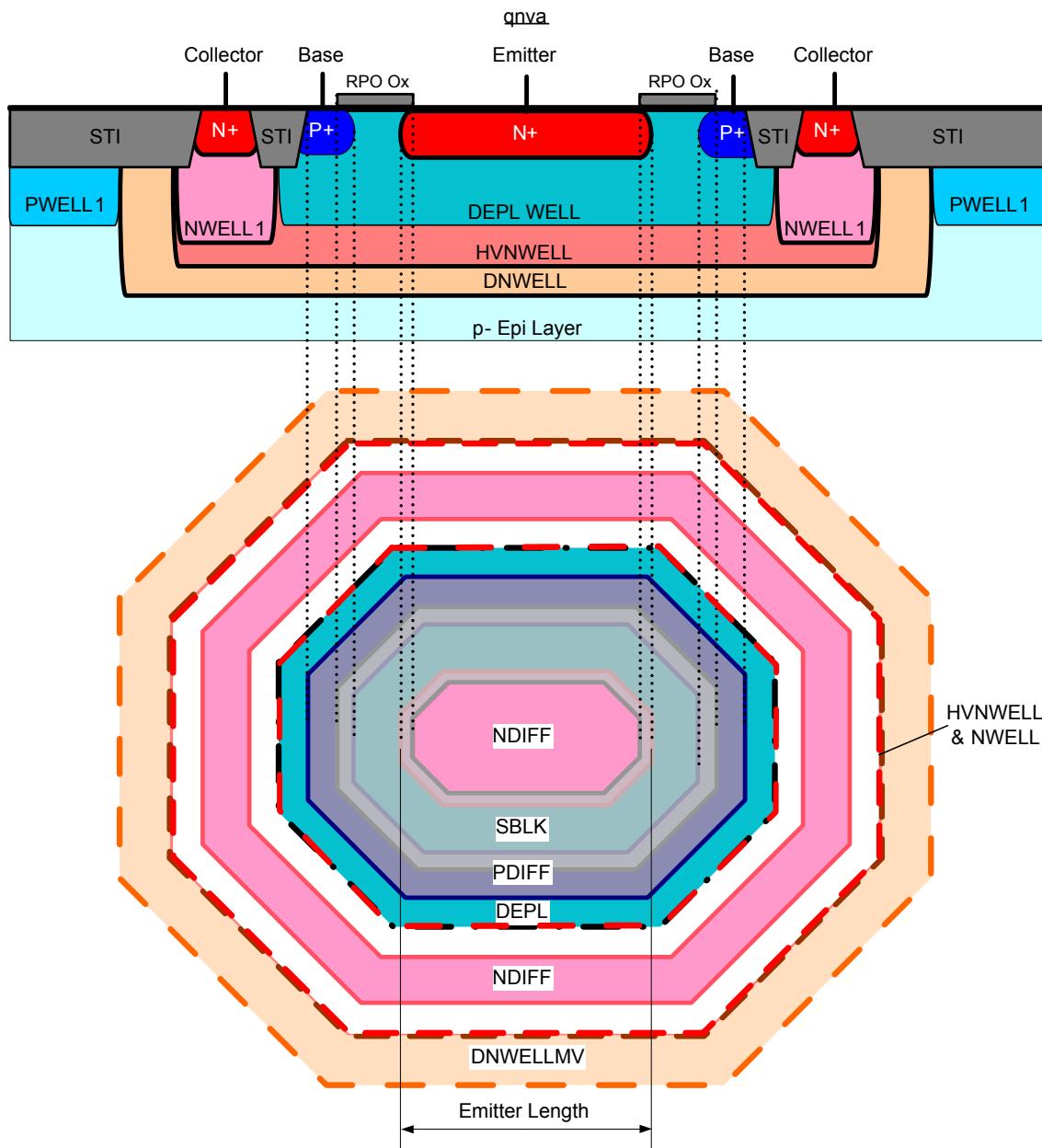


Figure 3.138 qnva

3. Layer and Device rules → 3.17 DEPL module→ 3.17.2 Device rules→ qnvb

qnvb

Name	Description	Value	Unit
B5MV	MV overlap of qnvb is not allowed	-	-
B6WD	qnvb inside DNWELL is not allowed	-	-

Note: The layout of the qnvb vertical bipolar NPN transistor is pre-defined and only the emitter length can be changed in the range of 3µm to 50µm. The drawing below is a basic sketch only and does not give all details.

Note: DEPL overlap of NWELL is only allowed for the qnvb.

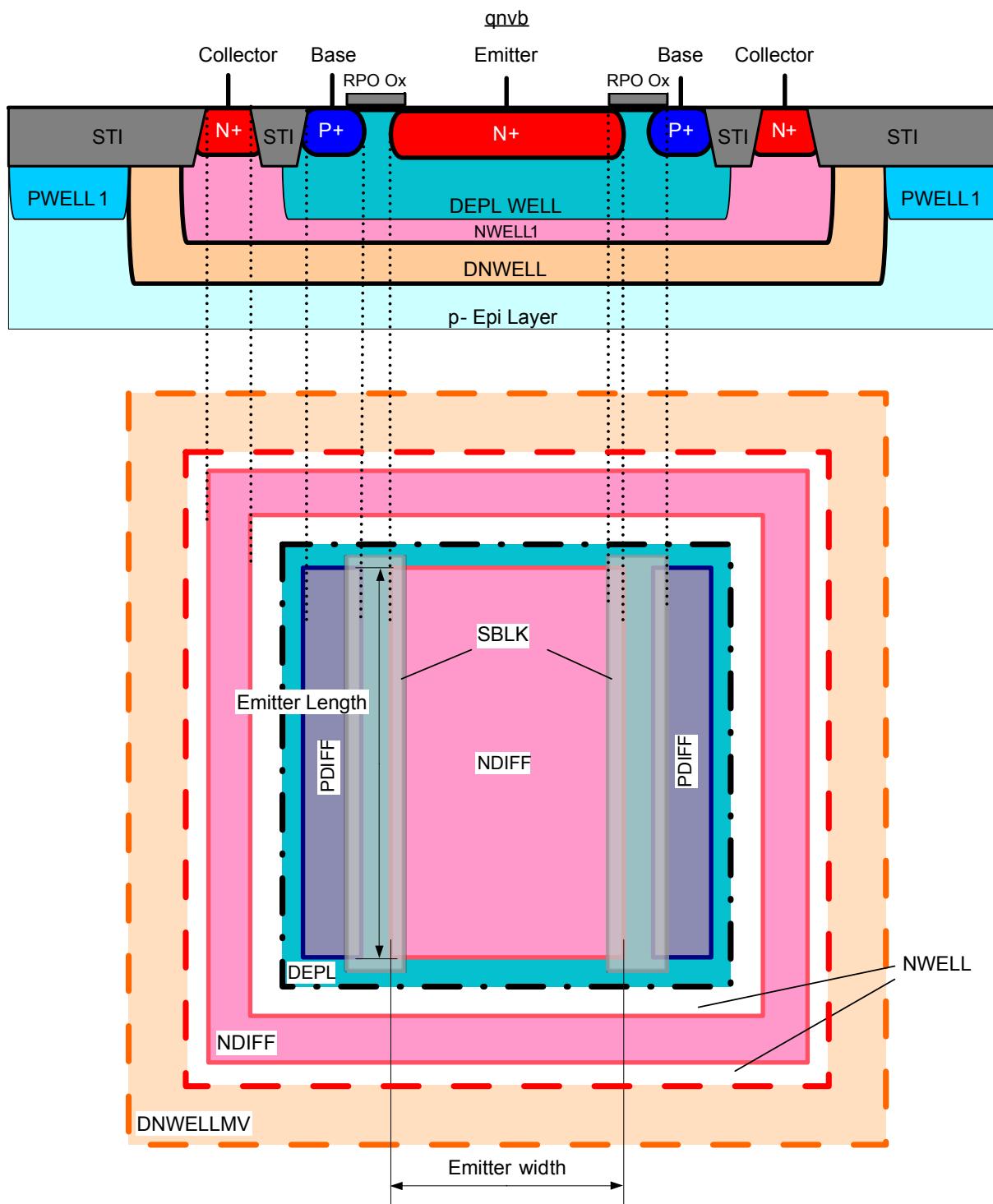


Figure 3.139 qnvb

3. Layer and Device rules → 3.18 HVDEPL module

3.18 HVDEPL module

3.18.1 Layer rules

HVDEPL

Name	Description	Value	Unit
B1HL	HVDEPL is only allowed for nhvd and nhhvd	-	-
W1HL	Minimum HVDEPL width	4.5	μm
S1HL	Minimum HVDEPL spacing / notch	0.6	μm
S1HLGA	Minimum HVDEPL spacing to GATE	0.7	μm

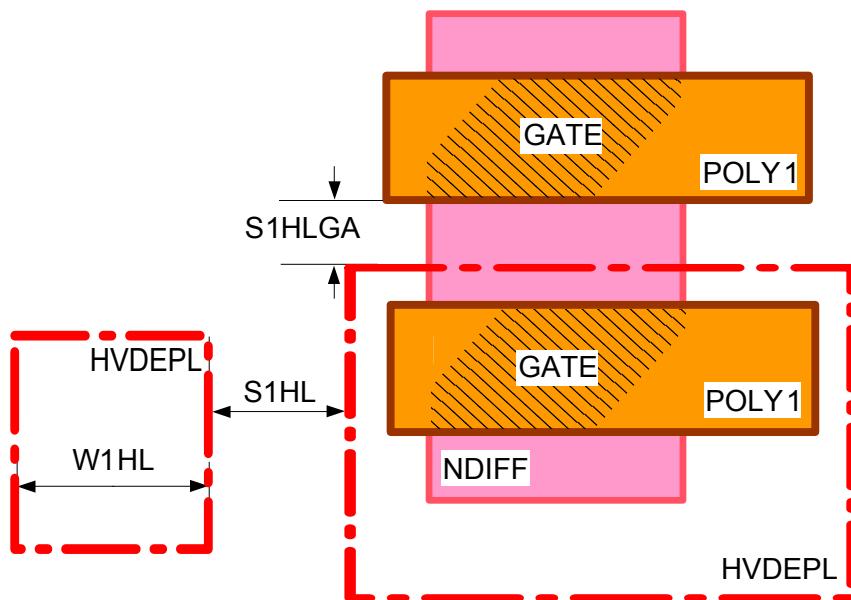


Figure 3.140 HVDEPL

3. Layer and Device rules → 3.18 HVDEPL module → 3.18.2 Device rules → nhvd, nhvd_bjt

3.18.2 Device rules

nhvd, nhvd_bjt

Name	Description	Value	Unit
B1P1GA	Only a rectangular POLY1 over GATE is allowed	-	-
W28GA	Minimum GATE length	3.0	µm
W29GA	Minimum GATE width	4.0	µm
S12DF	Fixed DRAIN-EDGE-STI length	3.0	µm
S2NDDP	Fixed NDF spacing to PDIFF	4.0	µm
S2NDHP	Fixed NDF spacing to HVPWELL (in channel region)	0.5	µm
S2NWGA	Minimum NWELL spacing to GATE	2.78	µm
S5P1DN	Minimum POLY1 spacing to DRAIN NDIFF	2.4	µm
S7NDHP	Fixed NDF spacing to HVPWELL (except channel region)	3.76	µm
E2HLGA	Fixed HVDEPL enclosure of GATE	0.75	µm
E2M1DN	Fixed MET1 enclosure of DRAIN NDIFF	1.0	µm
E3NDNW	Minimum NDF enclosure of NWELL	0.78	µm
E3NWDN	Minimum NWELL enclosure of NDIFF	0.22	µm
E4PBND	Fixed PWBLK enclosure of NDF (except channel region)	4.0	µm
E3P1DN	Minimum POLY1 extension beyond NDIFF	0.6	µm
E5P1GA	Fixed POLY1 extension beyond GATE (in GATE width direction)	1.2	µm
O2NDGA	Fixed NDF overlap of GATE	0.9	µm

Note: The layout of nhvd and nhvd_bjt is predefined and scalable concerning device width and length only. The other rules support the fixed dimensions of the layout or describe the relation to adjacent structures.

Note: nhvd_bjt device must be labeled "bjt" using POLY1 (VERIFICATION) layer over the GATE.

3. Layer and Device rules → 3.18 HVDEPL module → 3.18.2 Device rules→ nhvd, nhvd_bjt

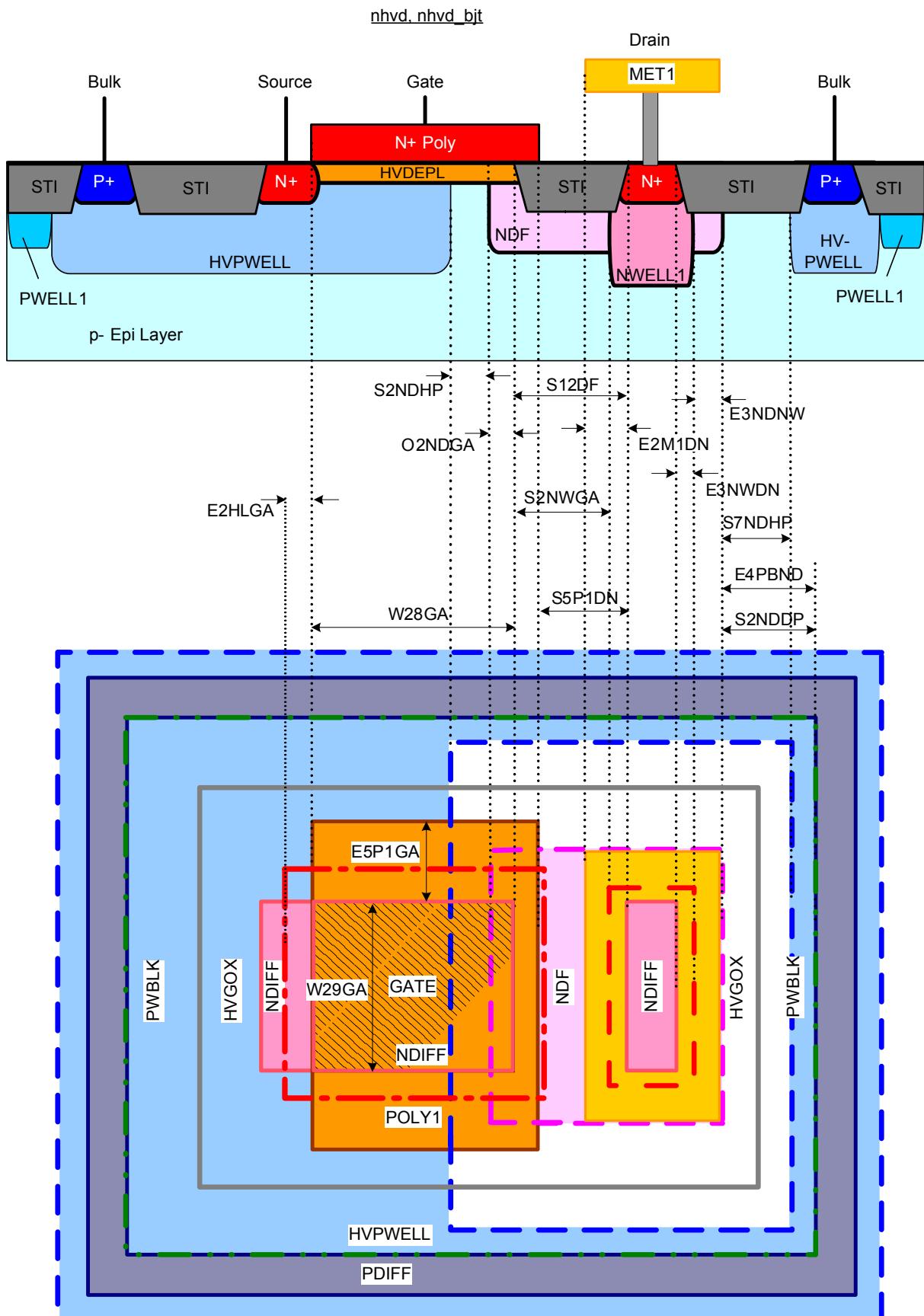


Figure 3.141 nhvd, nhvd_bjt

3. Layer and Device rules → 3.18 HVDEPL module → 3.18.2 Device rules → nhhvd, nhhvd_bjt

nhhvd, nhhvd_bjt

Name	Description	Value	Unit
B1P1GA	Only a rectangular POLY1 over GATE is allowed	-	-
W16GA	Minimum GATE length	5.0	µm
W17GA	Minimum GATE width	4.0	µm
S7DF	Fixed SOURCE/DRAIN-EDGE-STI length	3.0	µm
S2NDDP	Fixed NDF spacing to PDIFF	4.0	µm
S2NDHP	Fixed NDF spacing to HVPWELL (in channel region)	0.5	µm
S2NWGA	Minimum NWELL spacing to GATE	2.78	µm
S3P1DN	Minimum POLY1 spacing to SOURCE / DRAIN NDIFF	2.4	µm
S7NDHP	Fixed NDF spacing to HVPWELL (except channel region)	3.76	µm
E1HLGA	Fixed HVDEPL enclosure of GATE	0.75	µm
E1M1DN	Fixed MET1 enclosure of SOURCE / DRAIN NDIFF	1.0	µm
E3NDNW	Minimum NDF enclosure of NWELL	0.78	µm
E3NWDN	Minimum NWELL enclosure of NDIFF	0.22	µm
E4PBND	Fixed PWBLK enclosure of NDF (except channel region)	4.0	µm
E3P1GA	Minimum POLY1 extension beyond GATE	0.6	µm
E5P1GA	Fixed POLY1 extension beyond GATE (in GATE width direction)	1.2	µm
O2NDGA	Fixed NDF overlap of GATE	0.9	µm

Note: The layout of nhhvd and nhhvd_bjt is predefined and scalable concerning device width and length only. The other rules support the fixed dimensions of the layout or describe the relation to adjacent structures.

Note: nhhvd_bjt device must be labeled "bjt" using POLY1 (VERIFICATION) layer over the GATE.

3. Layer and Device rules → 3.18 HVDEPL module → 3.18.2 Device rules→ nhhvd, nhhvd_bjt

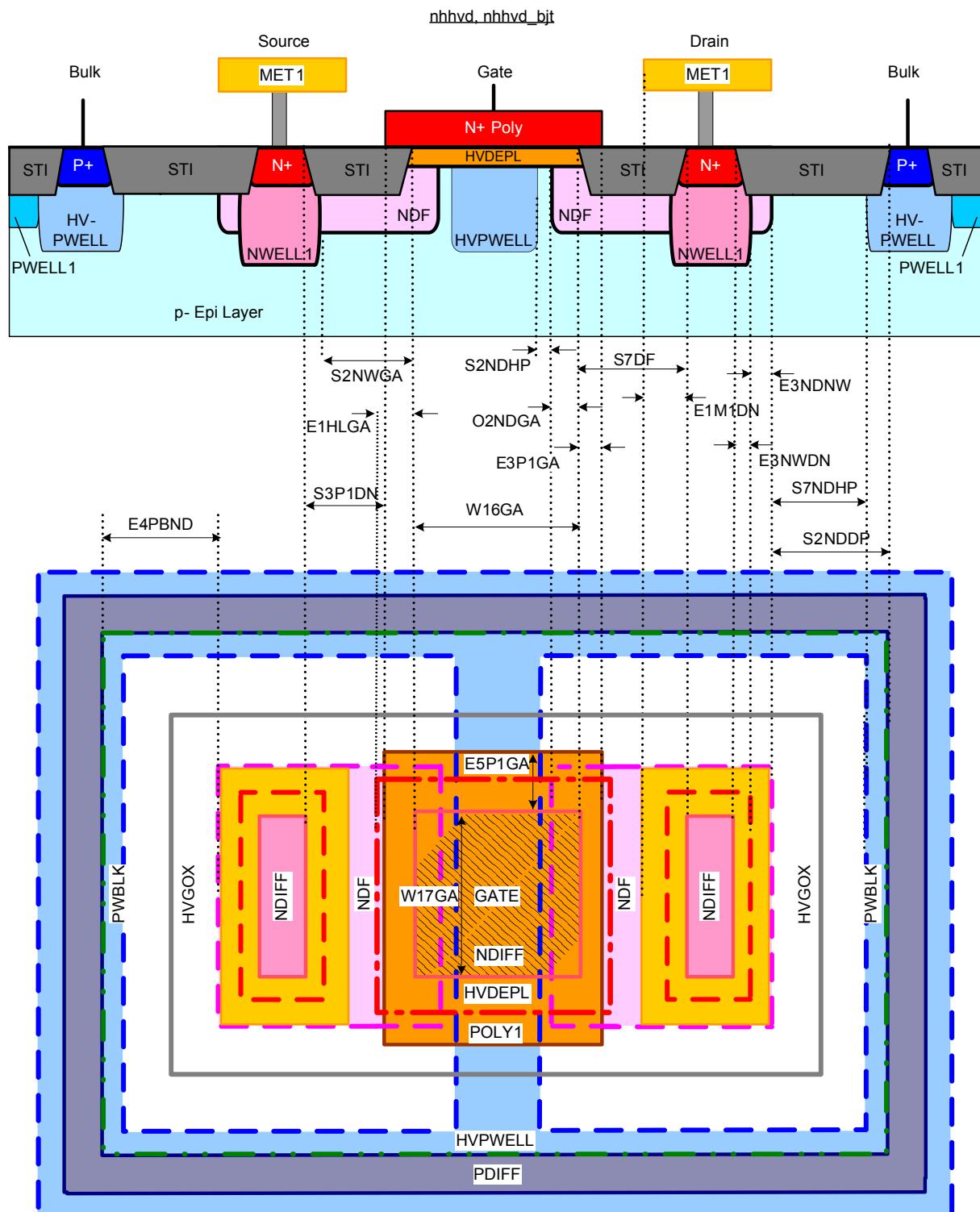


Figure 3.142 nhhvd, nhhvd_bjt

3. Layer and Device rules → 3.19 DMOS module

3.19 DMOS module

3.19.1 Layer rules

PDD

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1PT	PDD is only allowed for ned#, ped#	-	-
W1PT	Minimum PDD width	1.0	μm
S1PT	Minimum PDD spacing / notch	0.86	μm
A1PT	Minimum PDD area	6.0	μm ²
A2PT	Minimum PDD enclosed area	12.0	μm ²

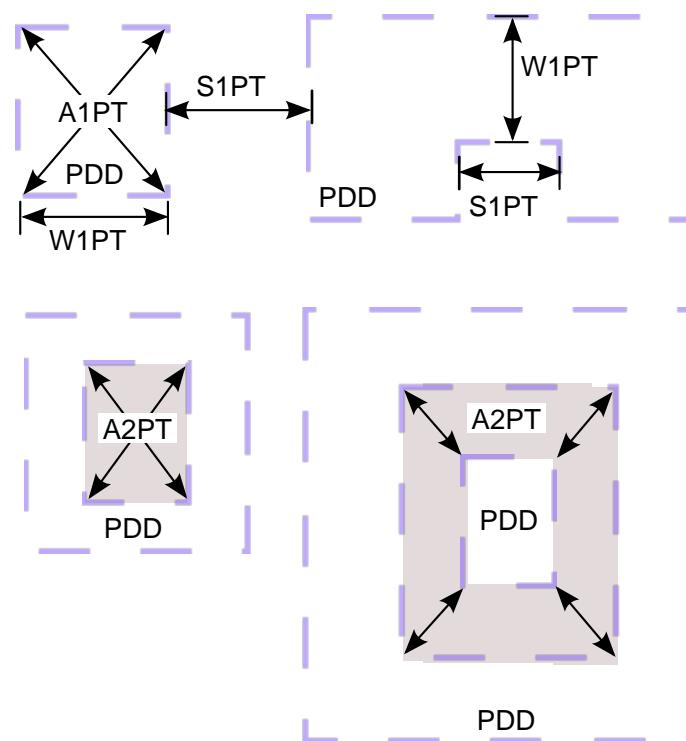


Figure 3.143 PDD

3. Layer and Device rules → 3.19 DMOS module→ 3.19.2 Device rules→ ned_i, ned_i_bjt

3.19.2 Device rules

ned_i, ned_i_bjt

Name	Description	Value	Unit
W7GA	Fixed CHANNEL length	0.65	μm
W8GA	Minimum linear cell width	5.0	μm
Note: CHANNEL width is defined as 2 * linear cell width.			

Note: CHANNEL for ned_i is defined as GATE and HVPWELL.

Note: Cross section and layout sketch are valid in the length direction of the device only. Device termination perpendicular to the length direction is predefined by ready to use cell elements. Thus it is not described by additional ned_i rules.

Note: The layout of ned_i and ned_i_bjt is predefined and scalable concerning device width only. All other dimensions must not be changed.

Note: ned_i_bjt device must be labeled "bjt" using POLY1 (VERIFICATION) layer over the GATE.

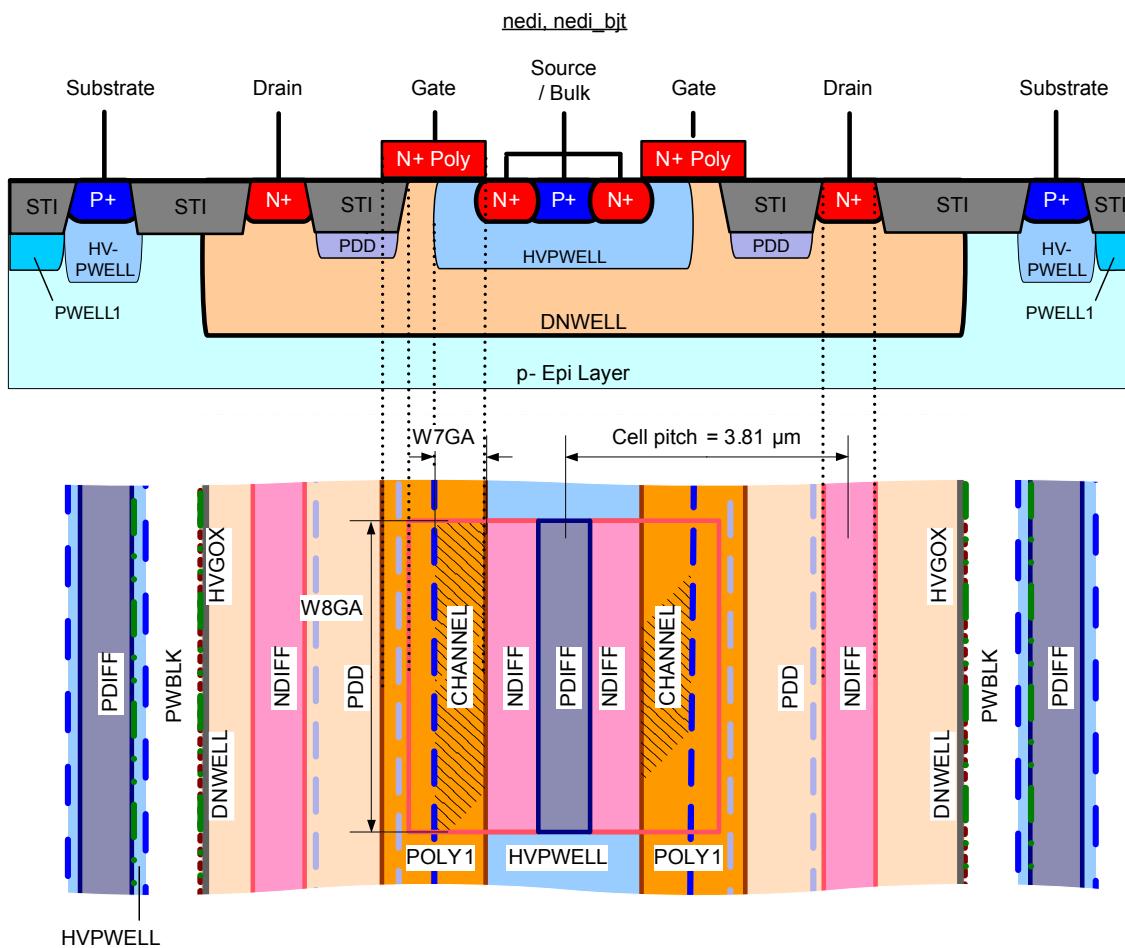


Figure 3.144 ned_i, ned_i_bjt

3. Layer and Device rules → 3.19 DMOS module→ 3.19.2 Device rules→ nedia, nedia_bjt

nesia, nedia_bjt

Name	Description	Value	Unit
W11GA	Fixed CHANNEL length	1.25	μm
W8GA	Minimum linear cell width	5.0	μm
Note: CHANNEL width is defined as 2 * linear cell width.			

Note: CHANNEL for nedia is defined as GATE and HVPWELL.

Note: Cross section and layout sketch are valid in the length direction of the device only. Device termination perpendicular to the length direction is predefined by ready to use cell elements. Thus it is not described by additional nedia rules.

Note: The layout of nedia and nedia_bjt is predefined and scalable concerning device width only. All other dimensions must not be changed.

Note: nedia_bjt device must be labeled "bjt" using POLY1 (VERIFICATION) layer over the GATE.

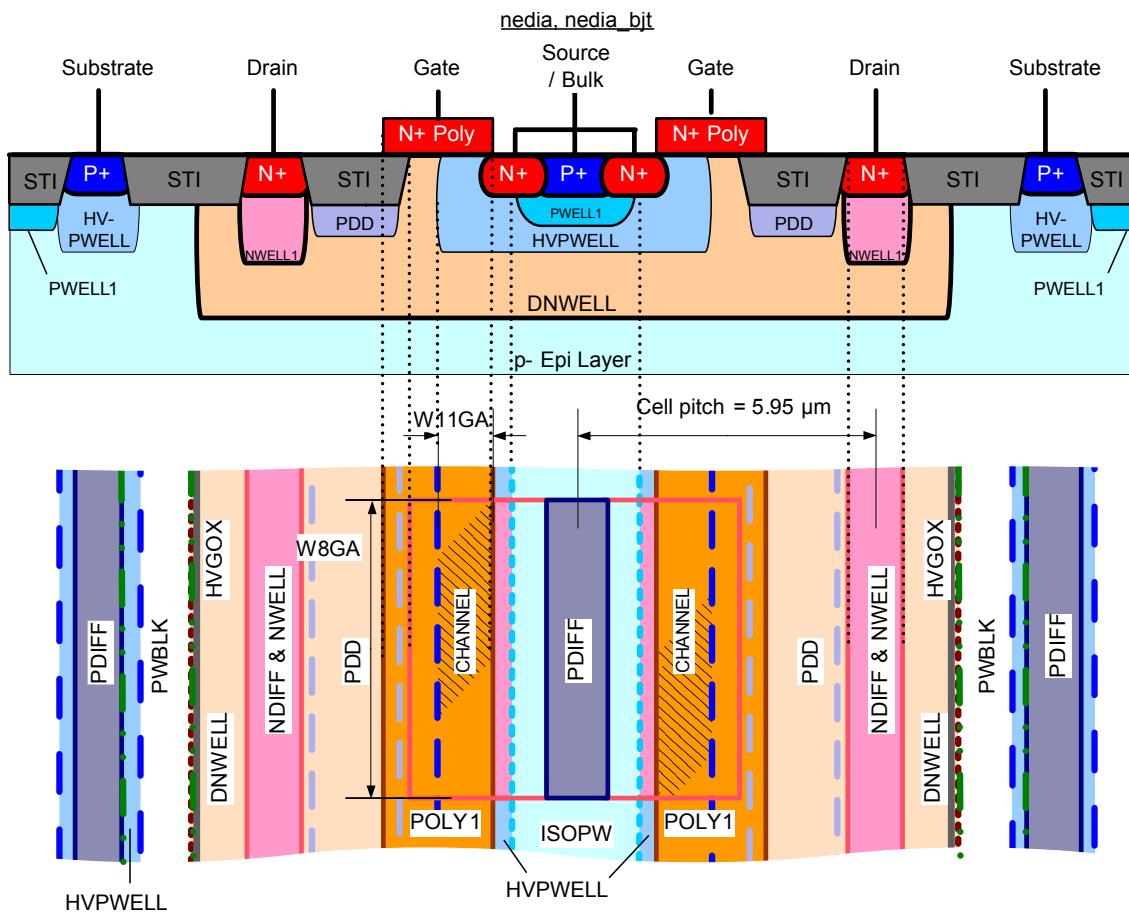


Figure 3.145 nedia, nedia_bjt

3. Layer and Device rules → 3.19 DMOS module→ 3.19.2 Device rules→ ped2, ped2_bjt

ped2, ped2_bjt

Name	Description	Value	Unit
W10GA	Minimum linear cell width	5.0	μm
	Note: CHANNEL width is defined as 2 * linear cell width.		
W9GA	Fixed CHANNEL length	0.94	μm

Note: CHANNEL for ped2 is defined as GATE and not PDD.

Note: Cross section and layout sketch are valid in the length direction of the device only. Device termination perpendicular to the length direction is predefined by ready to use cell elements. Thus it is not described by additional ped2 rules.

Note: The layout of ped2 and ped2_bjt is predefined and scalable concerning device width only. All other dimensions must not be changed.

Note: ped2_bjt device must be labeled "bjt" using POLY1 (VERIFICATION) layer over the GATE.

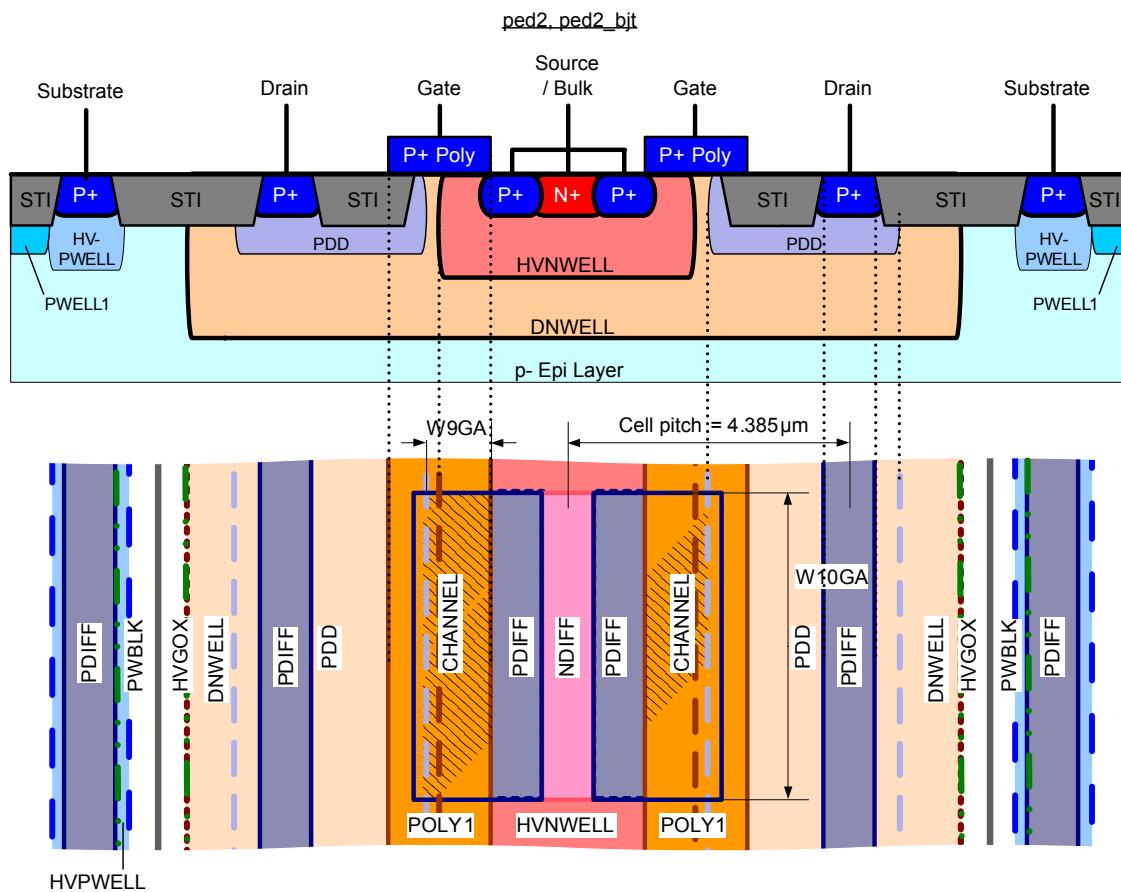


Figure 3.146 ped2, ped2_bjt

3. Layer and Device rules → 3.19 DMOS module→ 3.19.2 Device rules→ ped, ped_bjt

ped, ped_bjt

Name	Description	Value	Unit
W10GA	Minimum linear cell width	5.0	μm
	Note: CHANNEL width is defined as 2 * linear cell width.		
W9GA	Fixed CHANNEL length	0.94	μm

Note: CHANNEL for ped is defined as GATE and not PDD.

Note: Cross section and layout sketch are valid in the length direction of the device only. Device termination perpendicular to the length direction is predefined by ready to use cell elements. Thus it is not described by additional ped rules.

Note: The layout of ped and ped_bjt is predefined and scalable concerning device width only. All other dimensions must not be changed.

Note: ped_bjt device must be labeled "bjt" using POLY1 (VERIFICATION) layer over the GATE.

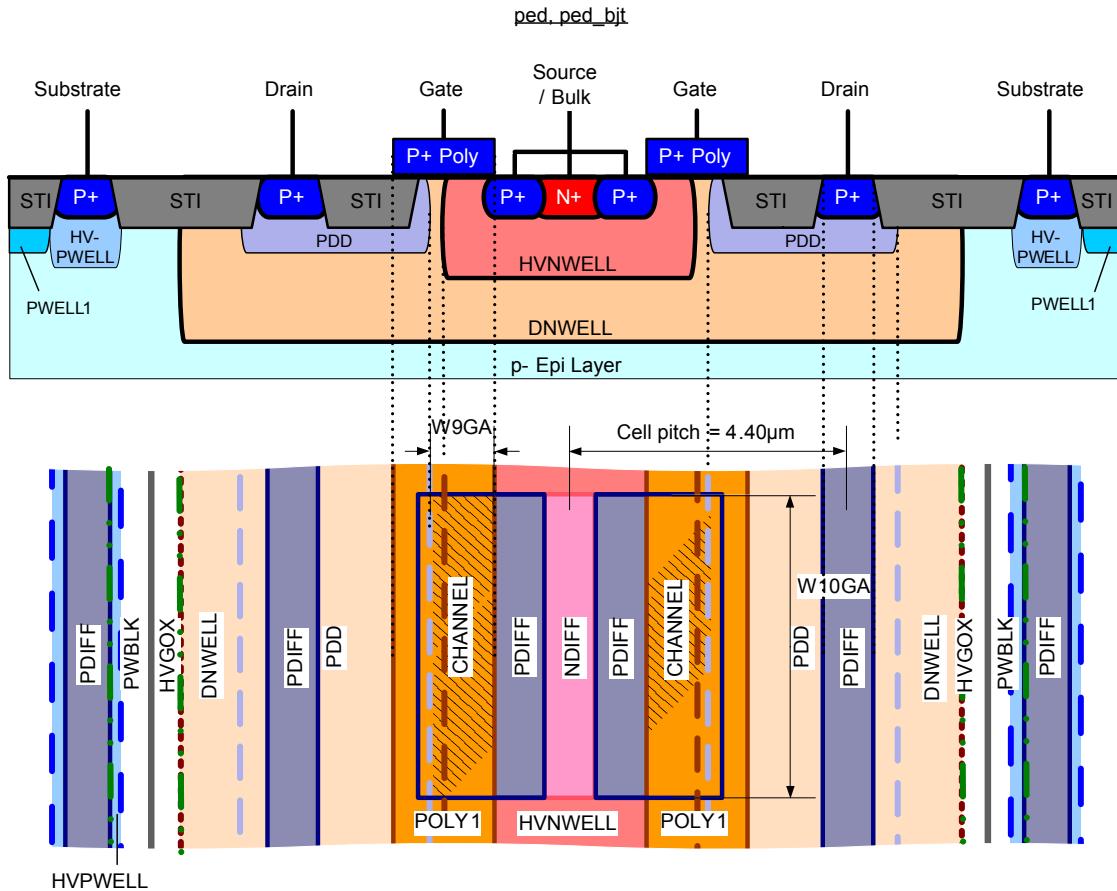


Figure 3.147 ped, ped_bjt

3. Layer and Device rules → 3.20 HVMOS module

3.20 HVMOS module

3.20.1 Layer rules

DNWELL

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1WD	DNWELL must be surrounded by a GUARD RING consisting of PDIFF and HVPWELL	-	-
B3WD	NWELL crossing DNWELL edge is not allowed	-	-
W1WD	Minimum DNWELL width	6.44	µm
S1WD	Minimum DNWELL spacing/notch	10.0	µm
S1P1WD	Minimum POLY1 spacing to DNWELL	5.35	µm
S1WDDN	Minimum DNWELL spacing to NDIFF	4.23	µm
S1WDDP	Fixed DNWELL spacing to PDIFF	4.0	µm
S1WDHN	Minimum DNWELL spacing to HVNWELL	10.0	µm
S1WDHP	Minimum DNWELL spacing to HVPWELL	3.75	µm
S1WDNW	Minimum DNWELL spacing to NWELL	10.0	µm
E1PBWD	Fixed PWBLK enclosure of DNWELL (min. spacing DNWELL to generated Pwells)	4.0	µm
E1WDDN	Fixed DNWELL enclosure of NDIFF (except ned#, ped#)	3.0	µm
Note: NDIFF must be the DNWELL contact.			
E1WDDP	Minimum DNWELL enclosure of PDIFF	3.5	µm
E1WDHN	Minimum DNWELL enclosure of HVNWELL (except pmma, qpvascr)	3.65	µm
E1WDNW	Minimum DNWELL enclosure of NWELL	3.65	µm
E1WDP1	Minimum DNWELL enclosure of POLY1	3.95	µm
E1WDWM	Minimum DNWELL enclosure of DNWELLMV	3.0	µm
E2WDHN	Minimum DNWELL enclosure of HVNWELL	2.76	µm

Note: Rules for DNWELLMV layer are described under DNWELLMV section.

3. Layer and Device rules → 3.20 HVMOS module→ 3.20.1 Layer rules→ DNWELL

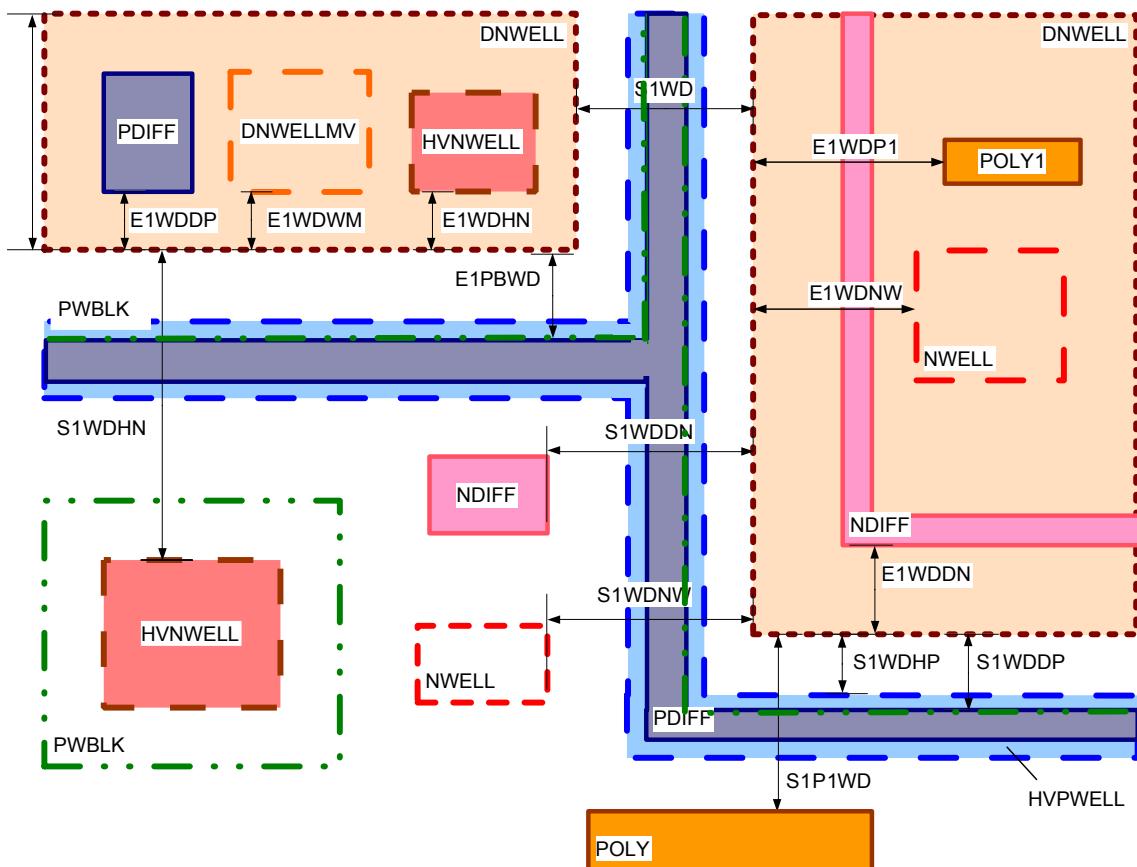


Figure 3.148 DNWELL

3. Layer and Device rules → 3.20 HVMOS module→ 3.20.1 Layer rules→ DNWELLMV

DNWELLMV

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1WM	DNWELLMV crossing DNWELL edge is not allowed	-	-
B2WM	NWELL crossing DNWELLMV edge is not allowed	-	-
Note: Valid if DNWELLMV is outside DNWELL.			
B6WM	HVPWELL crossing DNWELLMV edge is not allowed	-	-
B7WM	HVNWELL crossing DNWELLMV edge is not allowed	-	-
B8WM	POLY1 crossing DNWELLMV edge is not allowed	-	-
Note: Valid if DNWELLMV is outside DNWELL.			
W1WM	Minimum DNWELLMV width	1.6	μm
S1WM	Minimum DNWELLMV spacing/notch	1.6	μm
Note: Valid if DNWELLMV is outside DNWELL.			
S2WM	Minimum DNWELLMV spacing (different net)	5.0	μm
Note: Valid if DNWELLMV is outside DNWELL.			
S1WMDN	Minimum DNWELLMV spacing to NDIFF	0.43	μm
Note: Valid if DNWELLMV and NOT NWELL are outside DNWELL.			
S1WMDP	Minimum DNWELLMV spacing to PDIFF	0.43	μm
Note: Valid if DNWELLMV and NOT NWELL are outside DNWELL.			
S1WMHN	Minimum DNWELLMV spacing to HVNWELL	8.0	μm
Note: Valid if DNWELLMV is outside DNWELL.			
S1WMHP	Minimum DNWELLMV spacing to HVPWELL	3.0	μm
S1WMNW	Minimum DNWELLMV spacing to NWELL	3.5	μm
Note: Valid if DNWELLMV is outside DNWELL.			
S1WMP1	Minimum DNWELLMV spacing to POLY1	2.0	μm
Note: Valid if DNWELLMV is outside DNWELL.			
S1WMWD	Minimum DNWELLMV spacing to DNWELL	10.0	μm
Note: Valid if DNWELLMV is outside DNWELL.			
E1WMDN	Minimum DNWELLMV enclosure of NDIFF	0.43	μm
Note: Valid if DNWELLMV and NOT NWELL are outside DNWELL.			
E1WMDP	Minimum DNWELLMV enclosure of PDIFF	0.86	μm
Note: Valid if DNWELLMV and NOT NWELL are outside DNWELL.			
E1WMHN	Minimum DNWELLMV enclosure of HVNWELL	1.0	μm
Note: Valid if DNWELLMV is outside DNWELL.			
E1WMHP	Minimum DNWELLMV enclosure of HVPWELL	2.0	μm
E1WMP1	Minimum DNWELLMV enclosure of POLY1	2.0	μm
Note: Valid if DNWELLMV is outside DNWELL.			

3. Layer and Device rules → 3.20 HVMOS module → 3.20.1 Layer rules → DNWELLMV

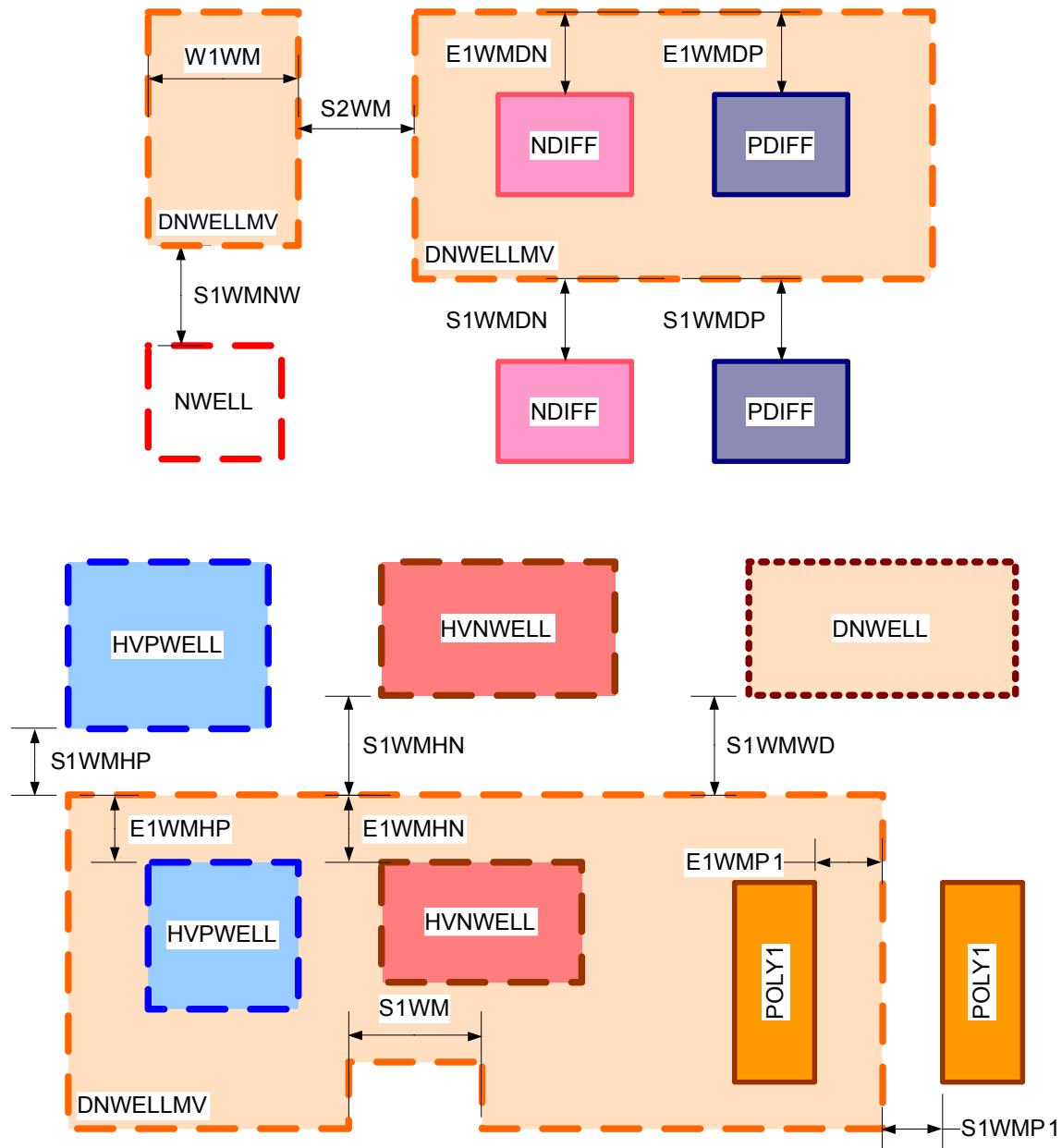


Figure 3.149 DNWELLMV

3. Layer and Device rules → 3.20 HVMOS module→ 3.20.1 Layer rules→ HVGOX

HVGOX

Name	Description	Value	Unit
B1GHMV	HVGOX overlap of MV is not allowed	-	-
B1GH	DIFF crossing HVGOX edge is not allowed	-	-
W1GH	Minimum HVGOX width	0.6	μm
S1GH	Minimum HVGOX spacing/notch	1.0	μm
S1GHDF	Minimum HVGOX spacing to DIFF	0.2	μm
E1GHDF	Minimum HVGOX enclosure of DIFF	0.2	μm

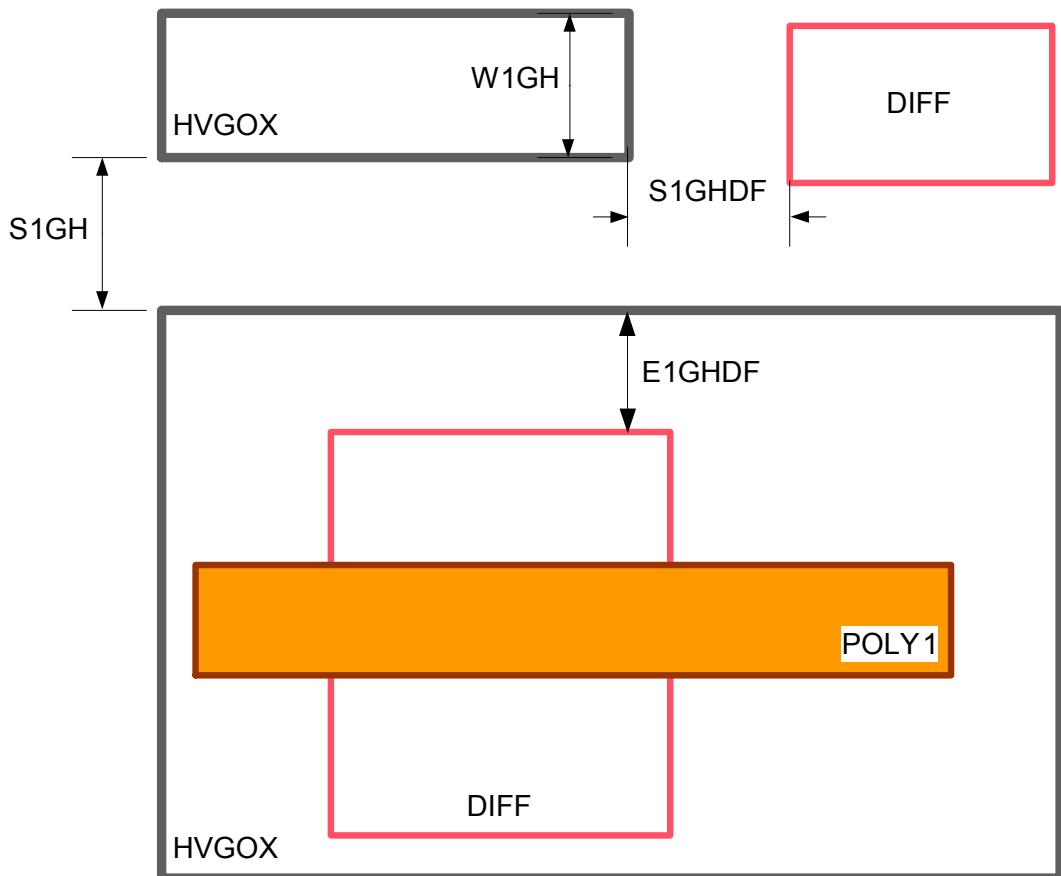


Figure 3.150 HVGOX

3. Layer and Device rules → 3.20 HVMOS module→ 3.20.1 Layer rules→ HVNWELL

HVNWELL

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1HN	HVNWELL must be contacted by NDIFF	-	-
B2HN	HVNWELL overlap of HVPWELL or PDD is not allowed	-	-
B3HN	HVNWELL overlap of NWELL is not allowed (except qnva)	-	-
B5HN	HVNWELL without PWBLK is not allowed Note: Valid outside DNWELL/DNWELLMV/HNW.	-	-
B7HN	HVNWELL overlap of DNWELL is not allowed Note: Valid inside DNWELLMV.	-	-
B4HN	DIFF crossing HVNWELL edge is not allowed (except ped#, pmma, nmma, pm#, ph#, pma)	-	-
B6HN	HVNWELL crossing DNWELL edge is not allowed	-	-
W1HN	Minimum HVNWELL width	0.9	μm
S1HN	Minimum HVNWELL spacing/notch	0.6	μm
S2HN	Minimum HVNWELL spacing (different net) Note: Valid outside DNWELL/DNWELLMV/HNW.	7.0	μm
S1HNDN	Minimum HVNWELL spacing to NDIFF	0.43	μm
S1HNHP	Minimum HVNWELL spacing to HVPWELL (except ped#, pmma, nmma, qpvascr, qpvhbscr) Note: Valid outside of DNWELLMV.	3.0	μm
S1HNNW	Minimum HVNWELL spacing to NWELL	3.0	μm
S2HNDN	Minimum HVNWELL spacing to NDIFF Note: Valid outside DNWELL/DNWELLMV/HNW.	3.43	μm
S2HNHP	Minimum HVNWELL spacing to HVPWELL Note: Valid inside DNWELLMV.	0.8	μm
E1HNDN	Minimum HVNWELL enclosure of NDIFF (except qnva)	0.12	μm
E1HNDP	Minimum HVNWELL enclosure of PDIFF	0.43	μm
E1PBHN	Fixed PWBLK enclosure of HVNWELL (except nmma) Note: Valid outside DNWELL/DNWELLMV/HNW.	3.0	μm
E2HNDN	Minimum HVNWELL enclosure of NDIFF Note: Valid outside DNWELL/DNWELLMV/HNW.	0.43	μm

3. Layer and Device rules → 3.20 HVMOS module→ 3.20.1 Layer rules→ HVNWELL

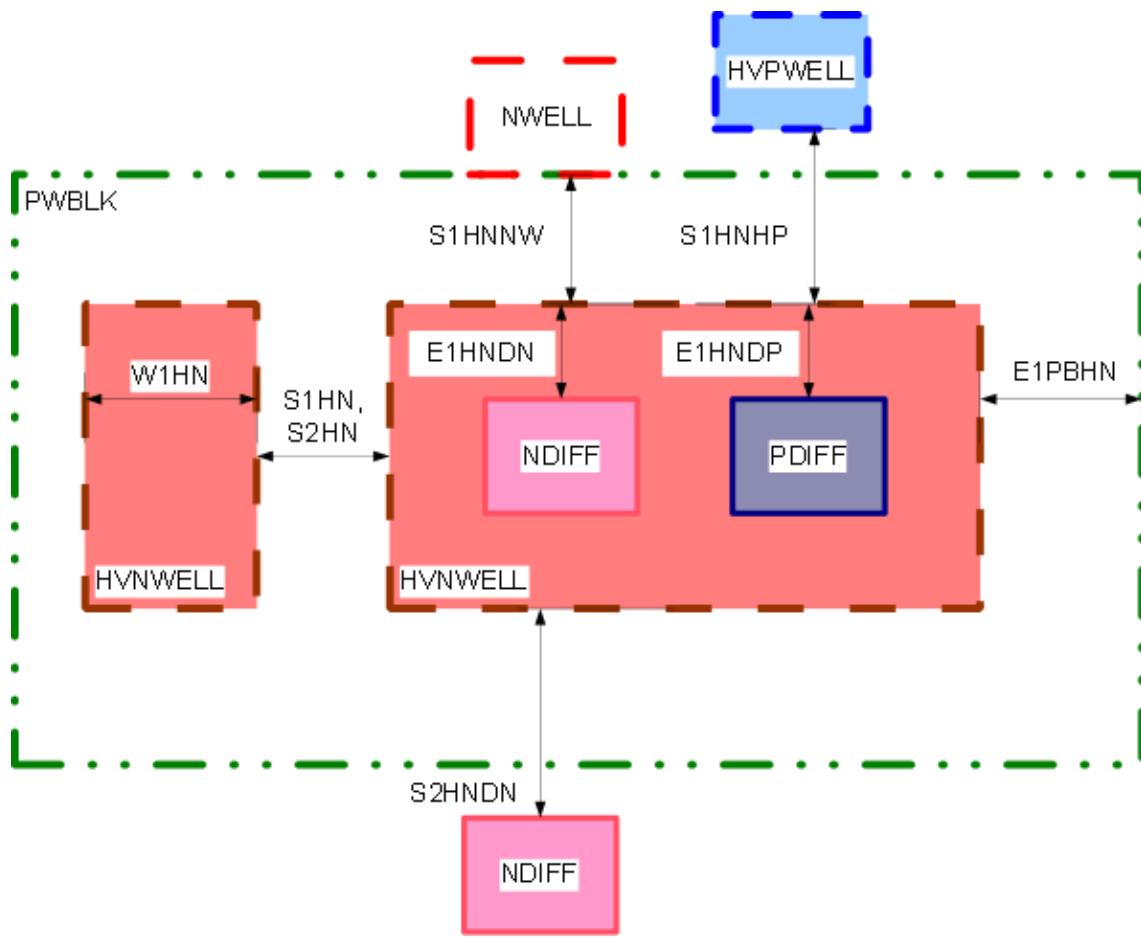


Figure 3.151 HVNWELL

3. Layer and Device rules → 3.20 HVMOS module→ 3.20.1 Layer rules→ HVPWELL

HVPWELL

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1HP	HVPWELL must be contacted by PDIFF	-	-
B3HP	HVPWELL overlap of NWELL is not allowed	-	-
B5HP	HVPWELL overlap of DNWELL is not allowed Note: Valid inside DNWELLMV.	-	-
B2HP	DIFF crossing HVPWELL edge is not allowed (except ped, ned#, nm#, nh#, pmma, nmma)	-	-
B4HP	HVPWELL crossing DNWELL edge is not allowed	-	-
W1HP	Minimum HVPWELL width	0.9	μm
S1HP	Minimum HVPWELL spacing/notch	0.6	μm
S2HP	Minimum HVPWELL spacing (different net) Note: Not valid for channel region of pmma GATE (oversized by 0.43 μm).	3.0	μm
S1HPDN	Minimum HVPWELL spacing to NDIFF (except ned#)	0.43	μm
S1HPDP	Minimum HVPWELL spacing to PDIFF	0.43	μm
S1HPNW	Minimum HVPWELL spacing to NWELL Note: Valid inside DNWELLMV.	0.8	μm
S2HPDN	Fixed HVPWELL spacing to NDIFF (except ned#, ped#, qpvascr) Note: Valid inside DNWELL and NOT DNWELLMV.	3.0	μm
S2HPNW	Minimum HVPWELL spacing to NWELL Note: Valid inside DNWELL and NOT DNWELLMV.	3.0	μm
E1HPDN	Minimum HVPWELL enclosure of NDIFF	0.43	μm
E1HPDP	Minimum HVPWELL enclosure of PDIFF (except ped#, pmma, nmma) Note: Valid inside DNWELLMV/DNWELL.	0.43	μm

3. Layer and Device rules → 3.20 HVMOS module → 3.20.1 Layer rules → HVPWELL

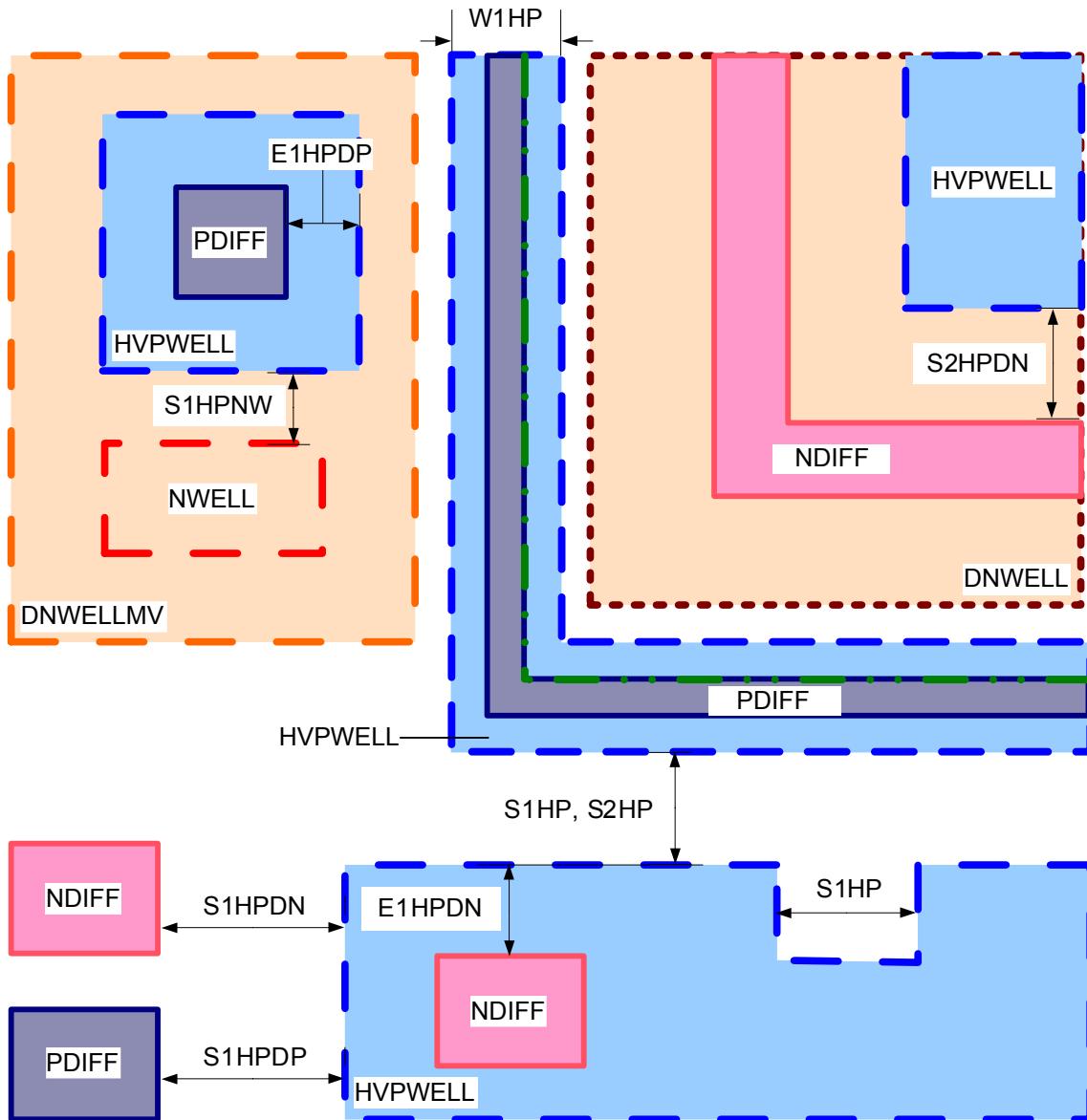


Figure 3.152 HVPWELL

3. Layer and Device rules → 3.20 HVMOS module→ 3.20.2 Device rules→ nmma, nmma_bjt

3.20.2 Device rules

nmma, nmma_bjt

Name	Description	Value	Unit
B1DNGH	NDIFF without HVGOX is not allowed	-	-
W5GA	Minimum GATE length	2.9	µm
W6GA	Minimum GATE width	2.5	µm
S4DF	Fixed SOURCE / DRAIN-EDGE-STI length	0.6	µm
S1DPGA	Maximum PDIFF spacing to GATE (at channel end) Note: PDIFF must be the HVPWELL contact.	2.6	µm
S1P1DN	Minimum POLY1 spacing to SOURCE / DRAIN NDIFF	0.3	µm
S3HNHP	Fixed HVNWELL spacing to HVPWELL of GATE	0.5	µm
S4HNHP	Fixed HVNWELL spacing to HVPWELL (except channel region)	1.75	µm
E2PBHN	Minimum PWBLK enclosure of HVNWELL	1.75	µm
E1P1DN	Minimum POLY1 extension beyond GATE	0.3	µm
O1HNGA	Fixed HVNWELL overlap of GATE	0.2	µm

Note: The layout of nmma and nmma_bjt is predefined and scalable concerning device width and length only. The other rules support the fixed dimensions of the layout or describe the relation to adjacent structures.

Note: nmma_bjt device must be labeled "bjt" using POLY1 (VERIFICATION) layer over the GATE.

3. Layer and Device rules → 3.20 HVMOS module → 3.20.2 Device rules → nmma, nmma_bjt

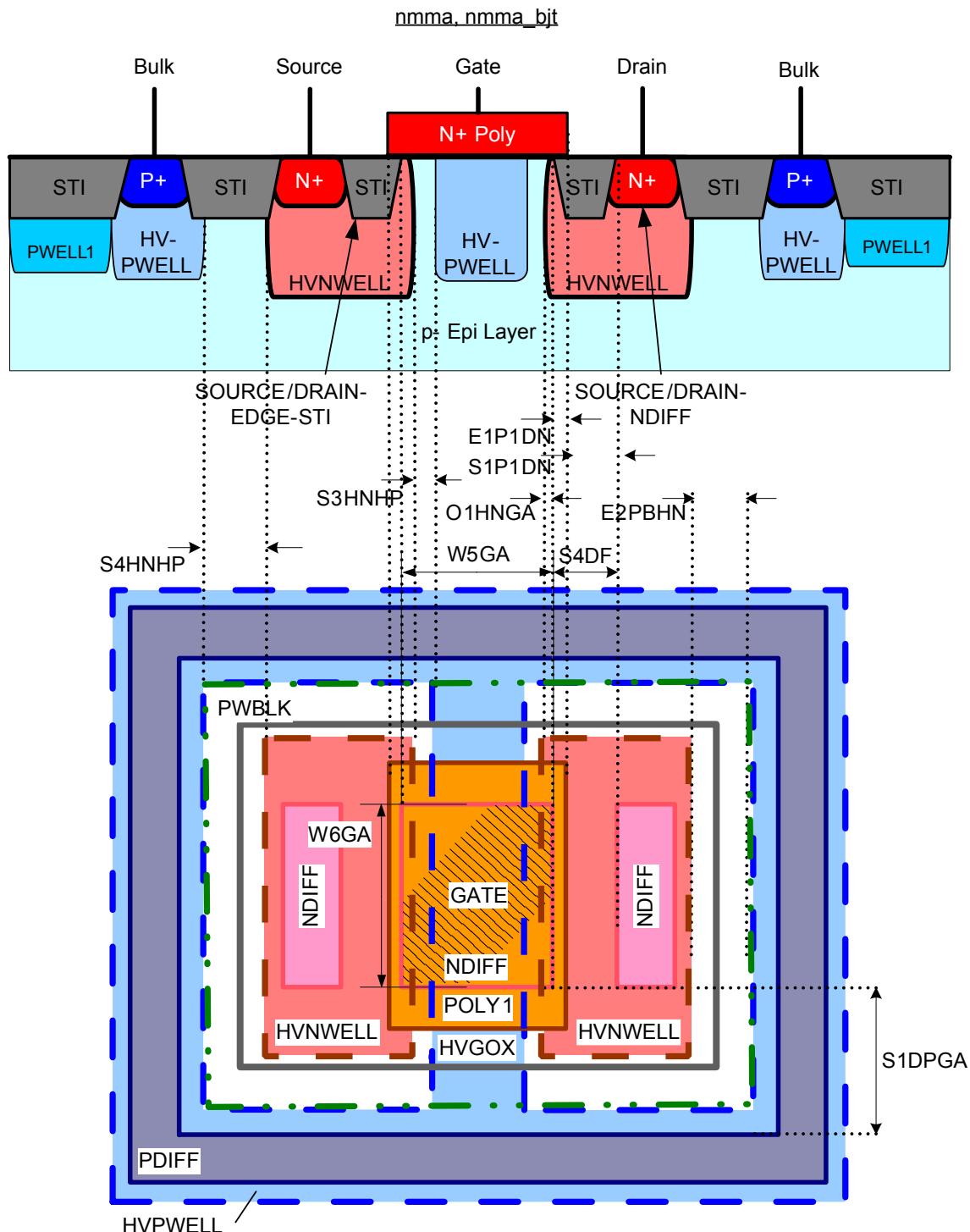


Figure 3.153 nmma, nmma_bjt

3. Layer and Device rules → 3.20 HVMOS module→ 3.20.2 Device rules→ pmma, pmma_bjt

pmma, pmma_bjt

Name	Description	Value	Unit
B1DPGH	PDIFF without HVGOX is not allowed	-	-
B3WM	pmma inside DNWELLMV is not allowed	-	-
W5GA	Minimum GATE length	2.9	µm
W6GA	Minimum GATE width	2.5	µm
S5DF	Fixed SOURCE / DRAIN-EDGE-STI length	0.6	µm
S1DNGA	Maximum NDIFF spacing to GATE (at channel end)	3.3	µm
	Note: NDIFF must be the HVNWELL contact.		
S1P1DP	Minimum POLY1 spacing to SOURCE / DRAIN PDIFF	0.3	µm
S2HPHN	Fixed HVPWELL spacing to HVNWELL of GATE	0.8	µm
S3HPDN	Minimum SOURCE/DRAIN HVPWELL spacing to NDIFF	2.6	µm
S3HPHN	Minimum HVPWELL spacing to HVNWELL (except channel region)	2.6	µm
E1HNGA	Minimum HVNWELL extension beyond GATE (at channel end)	2.7	µm
E1P1DP	Minimum POLY1 extension beyond GATE	0.3	µm
O1HPGA	Fixed HVPWELL overlap of GATE	0.2	µm

Note: The layout of pmma and pmma_bjt is predefined and scalable concerning device width and length only. The other rules support the fixed dimensions of the layout or describe the relation to adjacent structures.

Note: pmma_bjt device must be labeled "bjt" using POLY1 (VERIFICATION) layer over the GATE.

3. Layer and Device rules → 3.20 HVMOS module→ 3.20.2 Device rules→ pmma, pmma_bjt

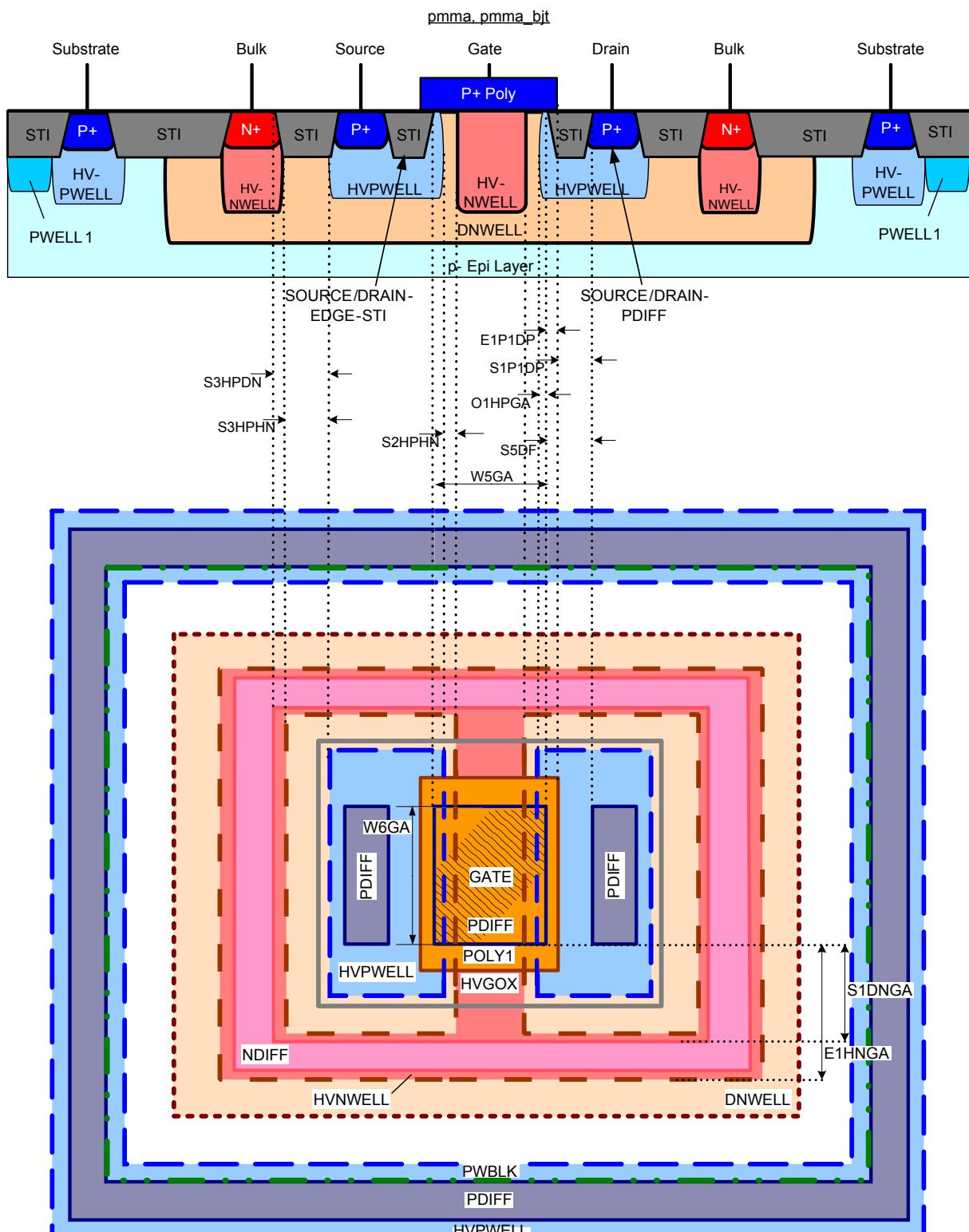


Figure 3.154 pmma, pmma_bjt

3. Layer and Device rules → 3.20 HVMOS module→ 3.20.2 Device rules→ qpvascr

qpvascr

Note: The layout of the qpvascr vertical bipolar PNP transistor is pre-defined and only the emitter length can be changed in the range of 10μm to 150μm. Device qpvascr has a fixed emitter width of 10.59um. The drawing below is a basic sketch only and does not show all details.

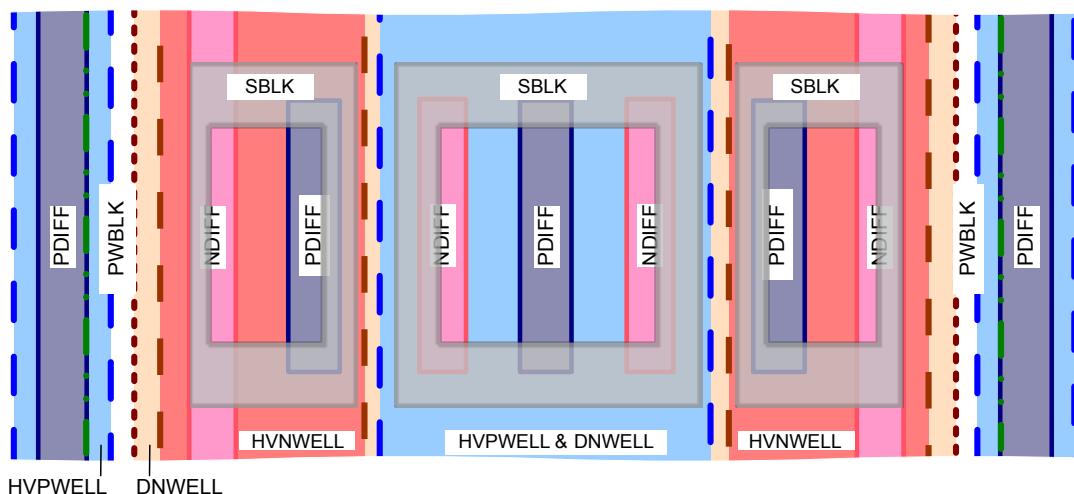
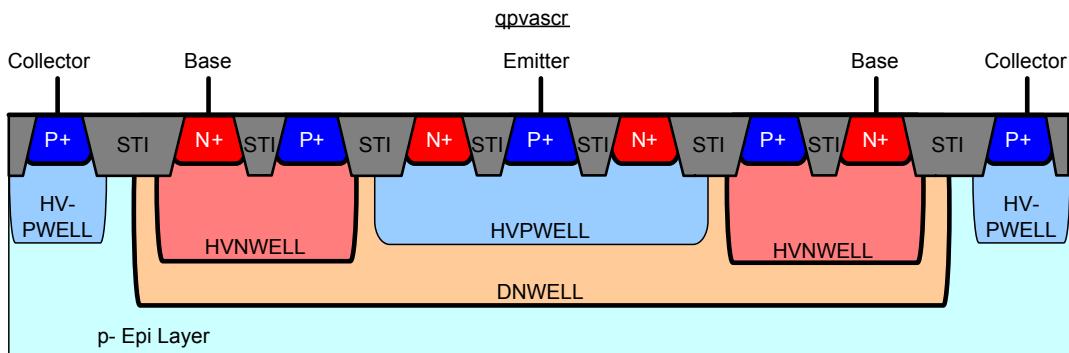


Figure 3.155 qpvascr

3. Layer and Device rules → 3.20 HVMOS module→ 3.20.2 Device rules→ rdnwmv

rdnwmv

Name	Description	Value	Unit
B4GH	HVGDX overlap of rdnwmv is not allowed	-	-
B4WM	DNWMV_VERIFY overlap of NWELL, DNWELL or HVNWELL is not allowed	-	-
B5WM	DNWMV_VERIFY overlap of DIFF is not allowed	-	-
	Note: DNWMV_VERIFY edge must touch rdnwmv NDIFF-contact edge.		
B9WM	DNWMV_VERIFY overlap of ISOPW, DEPL, SCI, HVPWELL, PDF or PDD is not allowed	-	-
W2WM	Minimum rdnwmv width	2.0	μm

Note: Recommended minimum number of squares is L/W ≥ 5.

Note: rdnwmv resistor definition: DNWELLMV and DNWMV_VERIFY.

Note: It is recommended to place DIFF stripes close to resistor.

Note: Recommended maximum width is 10μm.

3. Layer and Device rules → 3.20 HVMOS module→ 3.20.2 Device rules→ rdnwmv

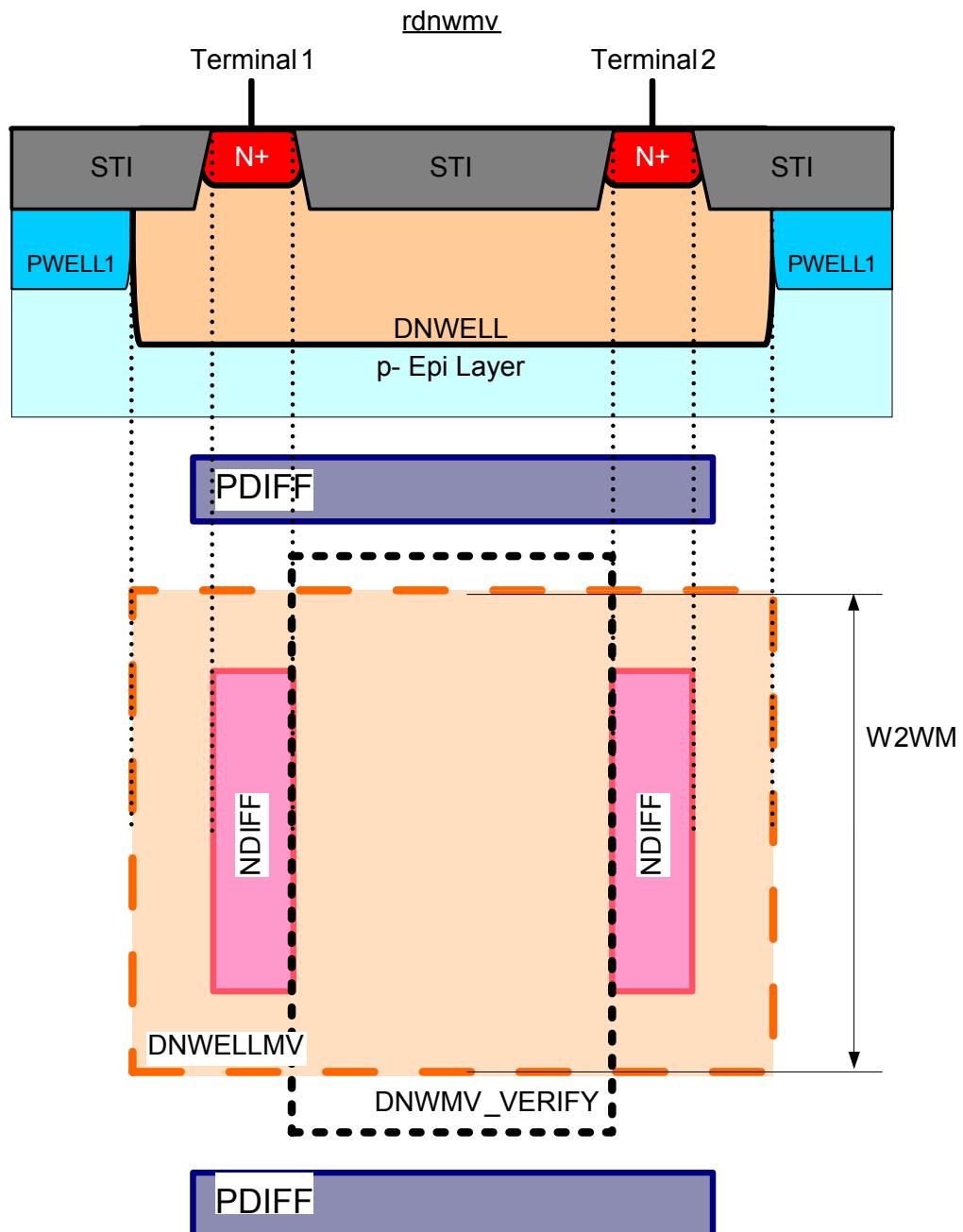


Figure 3.156 rdnwmv

3. Layer and Device rules → 3.20 HVMOS module→ 3.20.2 Device rules→ ddnwmv, dpdnwmv, dip...

ddnwmv, dpdnwmv, dipdnwmv

Note: The layer DIODEF must enclose the pn junction, crossing the pn junction is not allowed.

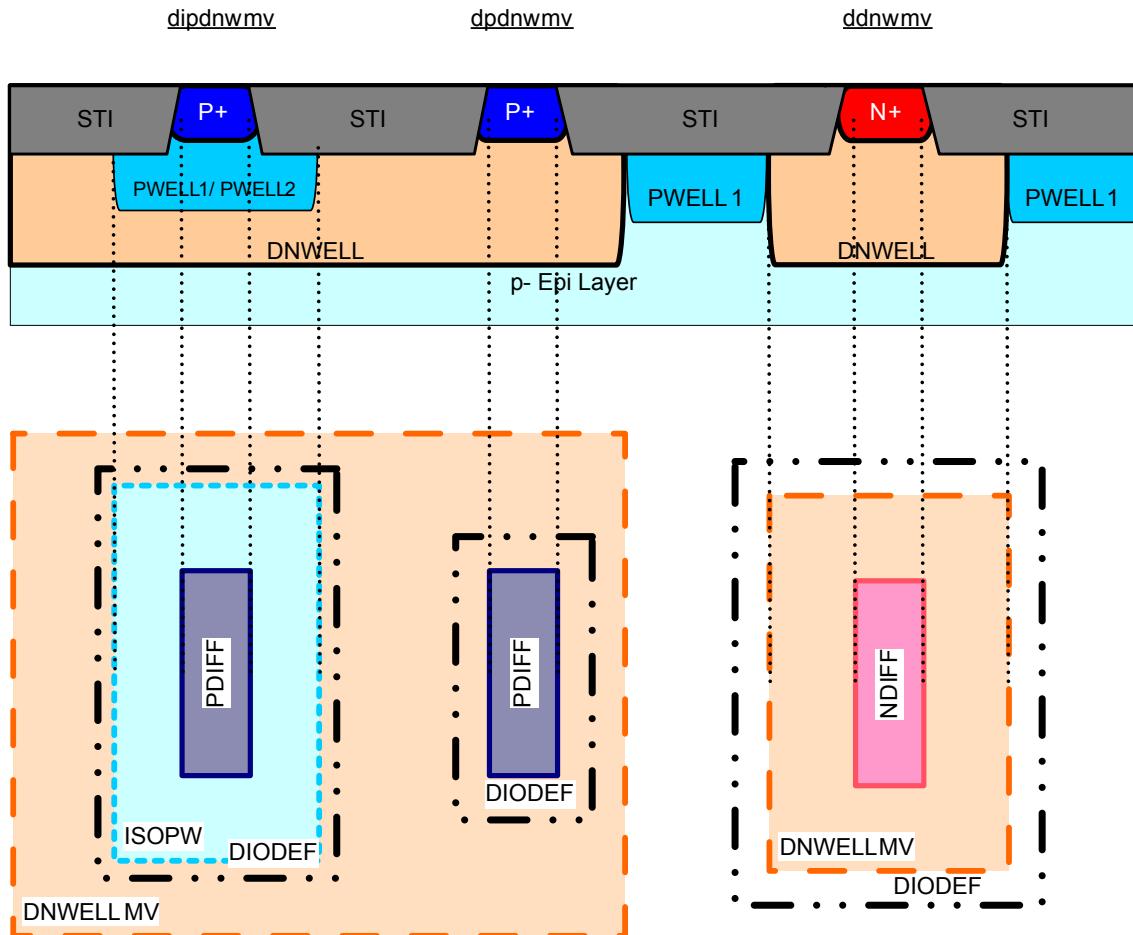


Figure 3.157 ddnwmv, dpdnwmv, dipdnwmv

3. Layer and Device rules → 3.20 HVMOS module→ 3.20.2 Device rules→ ddnw, dpdnw, dipdnw

ddnw, dpdnw, dipdnw

Note: The device dpdnw is allowed in predefined ESD protection structures only.

Note: The layer DIODEF must enclose the pn junction, crossing the pn junction is not allowed.

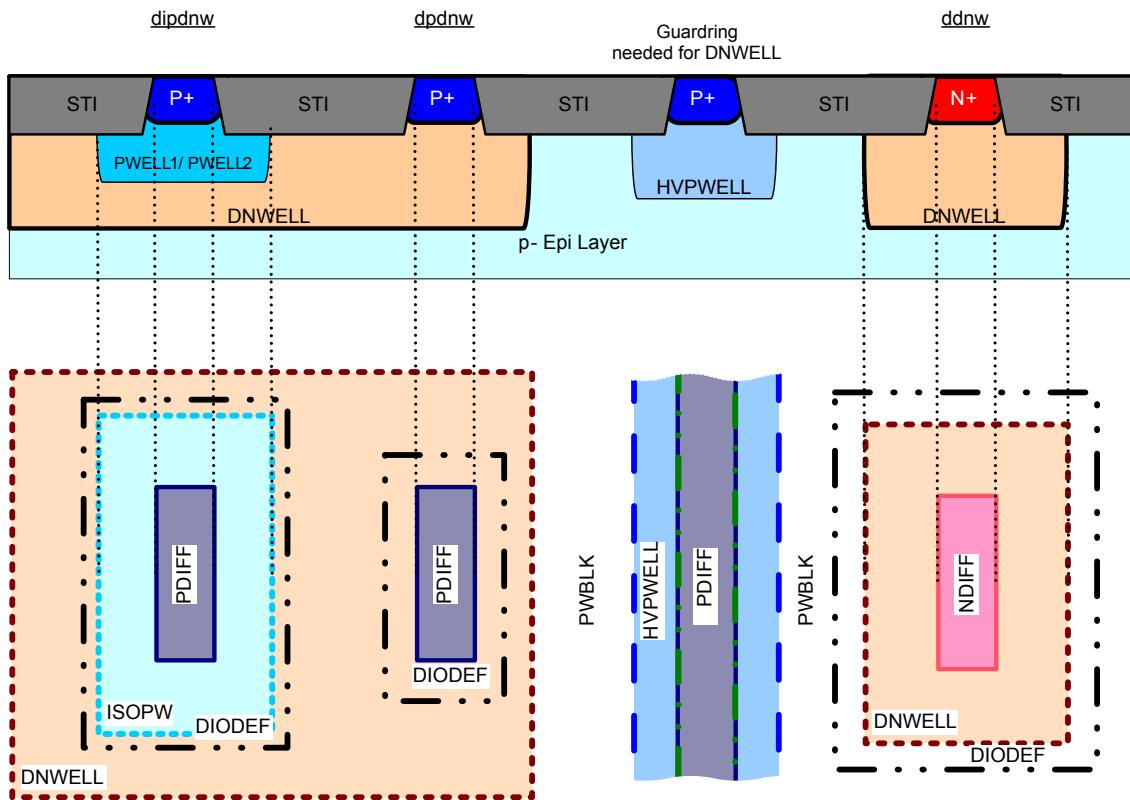


Figure 3.158 ddnw, dpdnw, dipdnw

3. Layer and Device rules → 3.20 HVMOS module→ 3.20.2 Device rules→ dnhpw, dphnw, dhpw, ...

dnhpw, dphnw, dhpw, dhnw

Note: The layer DIODEF must enclose the pn junction, crossing the pn junction is not allowed.

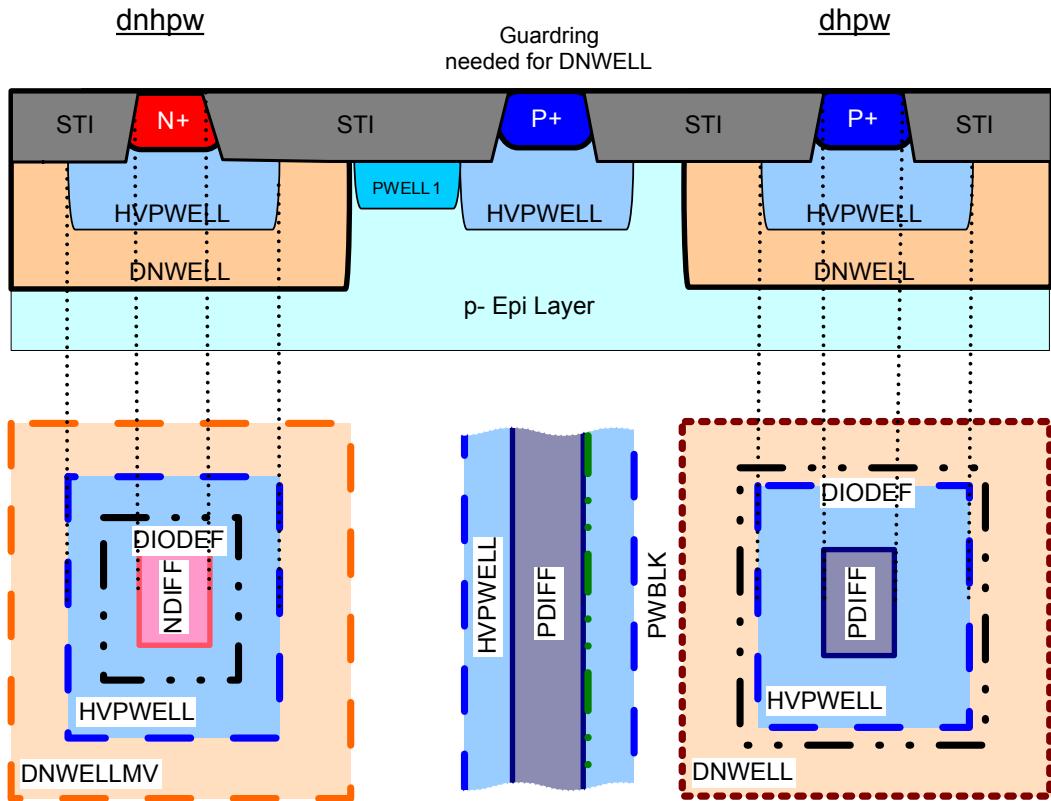


Figure 3.159 dnhpw, dhpw

3. Layer and Device rules → 3.20 HVMOS module→ 3.20.2 Device rules→ dhnw, dphnw, dhpw, ...

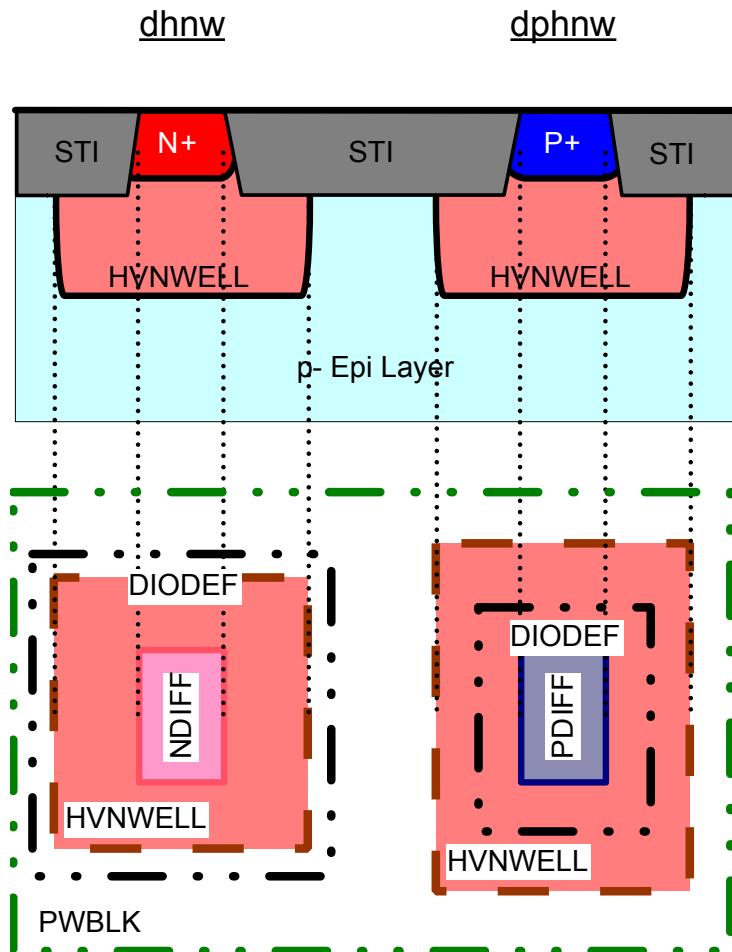


Figure 3.160 dhnw, dphnw

3. Layer and Device rules → 3.20 HVMOS module→ 3.20.2 Device rules→ dpp20

dpp20

Note: The device must be labeled "dpp20" using DIODEF layer.

Note: The layout of the dpp20 protection diode is predefined and only the HVPWELL width (anode) can be changed in the range of 20 μ m to 100 μ m. Fixed HVPWELL length (anode) is 5 μ m. The drawing below is a basic sketch only and does not give all details.

Note: The layer DIODEF must enclose the pn junction, crossing the pn junction is not allowed.

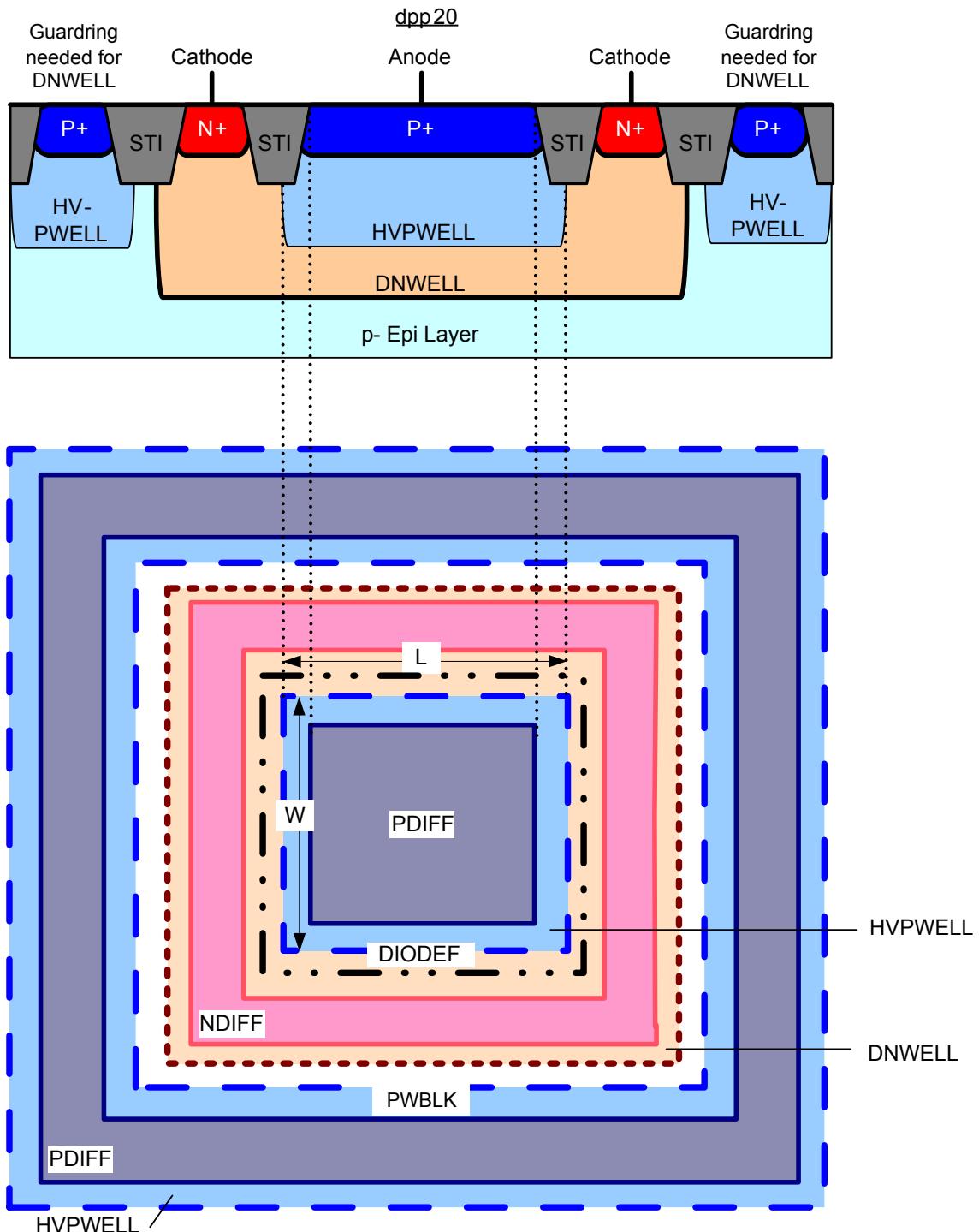


Figure 3.161 dpp20

3. Layer and Device rules → 3.21 HVNMOS module

3.21 HVNMOS module

3.21.1 Layer rules

HVGDX

Name	Description	Value	Unit
B1GHMV	HVGDX overlap of MV is not allowed	-	-
B1GH	DIFF crossing HVGDX edge is not allowed	-	-
W1GH	Minimum HVGDX width	0.6	μm
S1GH	Minimum HVGDX spacing/notch	1.0	μm
S1GHDF	Minimum HVGDX spacing to DIFF	0.2	μm
E1GHDF	Minimum HVGDX enclosure of DIFF	0.2	μm

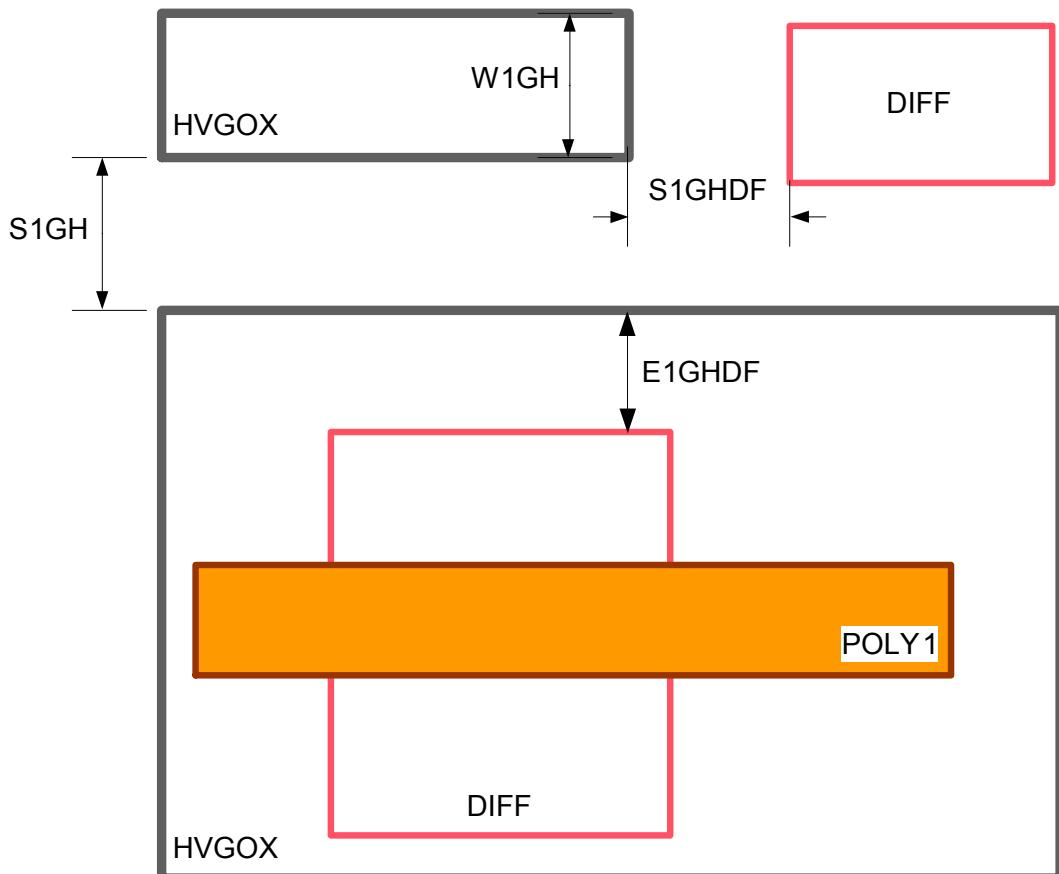


Figure 3.162 HVGOX

3. Layer and Device rules → 3.21 HVNMOS module→ 3.21.1 Layer rules→ HVPWELL

HVPWELL

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1HP	HVPWELL must be contacted by PDIFF	-	-
B3HP	HVPWELL overlap of NWELL is not allowed	-	-
B5HP	HVPWELL overlap of DNWELL is not allowed Note: Valid inside DNWELLMV.	-	-
B2HP	DIFF crossing HVPWELL edge is not allowed (except ped, ned#, nm#, nh#, pmma, nmma)	-	-
B4HP	HVPWELL crossing DNWELL edge is not allowed	-	-
W1HP	Minimum HVPWELL width	0.9	μm
S1HP	Minimum HVPWELL spacing/notch	0.6	μm
S2HP	Minimum HVPWELL spacing (different net) Note: Not valid for channel region of pmma GATE (oversized by 0.43 μm).	3.0	μm
S1HPDN	Minimum HVPWELL spacing to NDIFF (except ned#)	0.43	μm
S1HPDP	Minimum HVPWELL spacing to PDIFF	0.43	μm
S1HPNW	Minimum HVPWELL spacing to NWELL Note: Valid inside DNWELLMV.	0.8	μm
S2HPDN	Fixed HVPWELL spacing to NDIFF (except ned#, ped#, qpvascr) Note: Valid inside DNWELL and NOT DNWELLMV.	3.0	μm
S2HPNW	Minimum HVPWELL spacing to NWELL Note: Valid inside DNWELL and NOT DNWELLMV.	3.0	μm
E1HPDN	Minimum HVPWELL enclosure of NDIFF	0.43	μm
E1HPDP	Minimum HVPWELL enclosure of PDIFF (except ped#, pmma, nmma) Note: Valid inside DNWELLMV/DNWELL.	0.43	μm

3. Layer and Device rules → 3.21 HVN MOS module → 3.21.1 Layer rules → HVPWELL

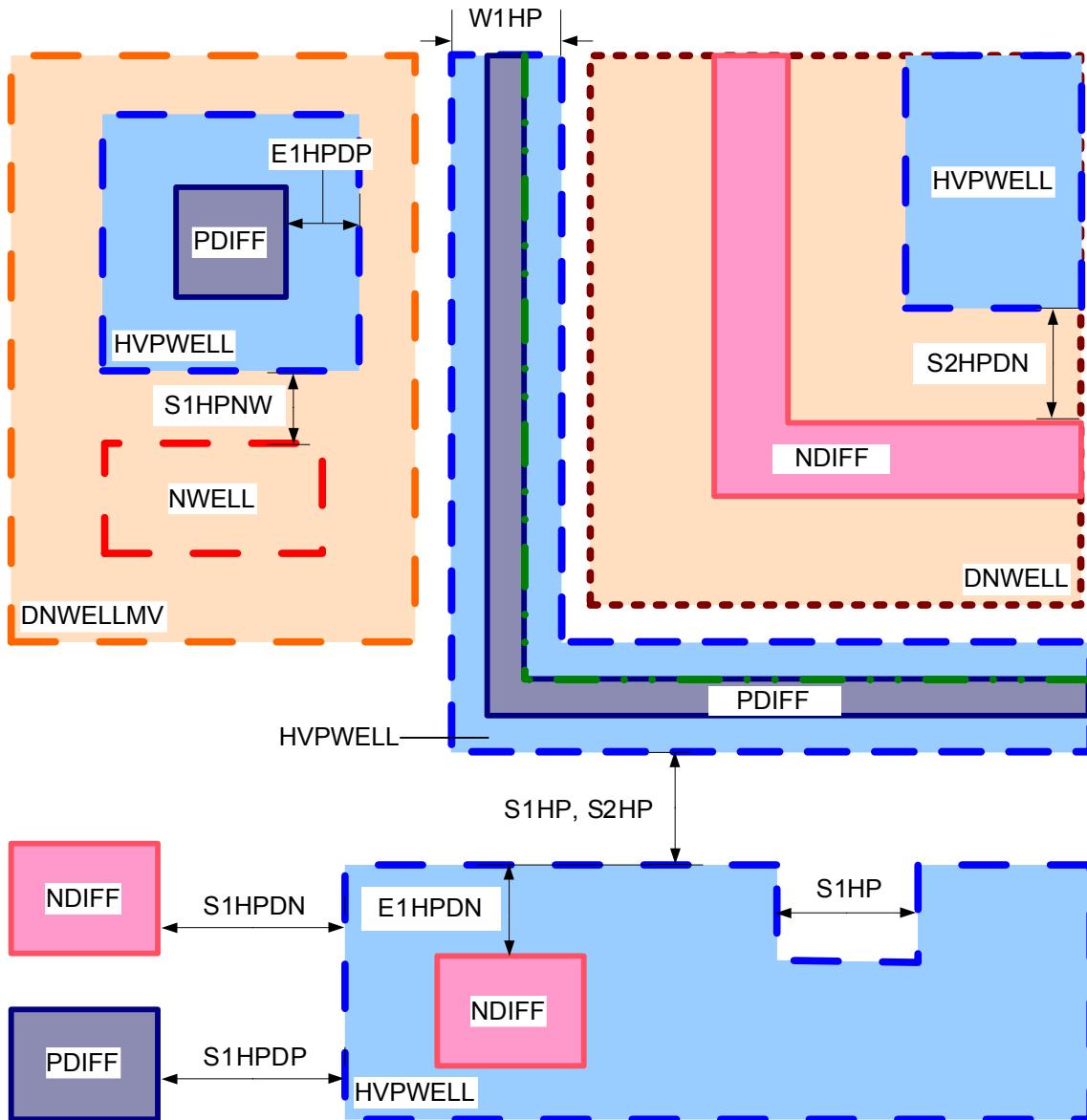


Figure 3.163 HVPWELL

3. Layer and Device rules → 3.21 HVNMOS module → 3.21.2 Device rules → nma, nma_bjt

3.21.2 Device rules

nma, nma_bjt

Name	Description	Value	Unit
W20GA	Minimum GATE length	1.0	μm
W21GA	Minimum GATE width	2.5	μm

Note: nma_bjt device must be labeled "bjt" using POLY1 (VERIFICATION) layer over the GATE.

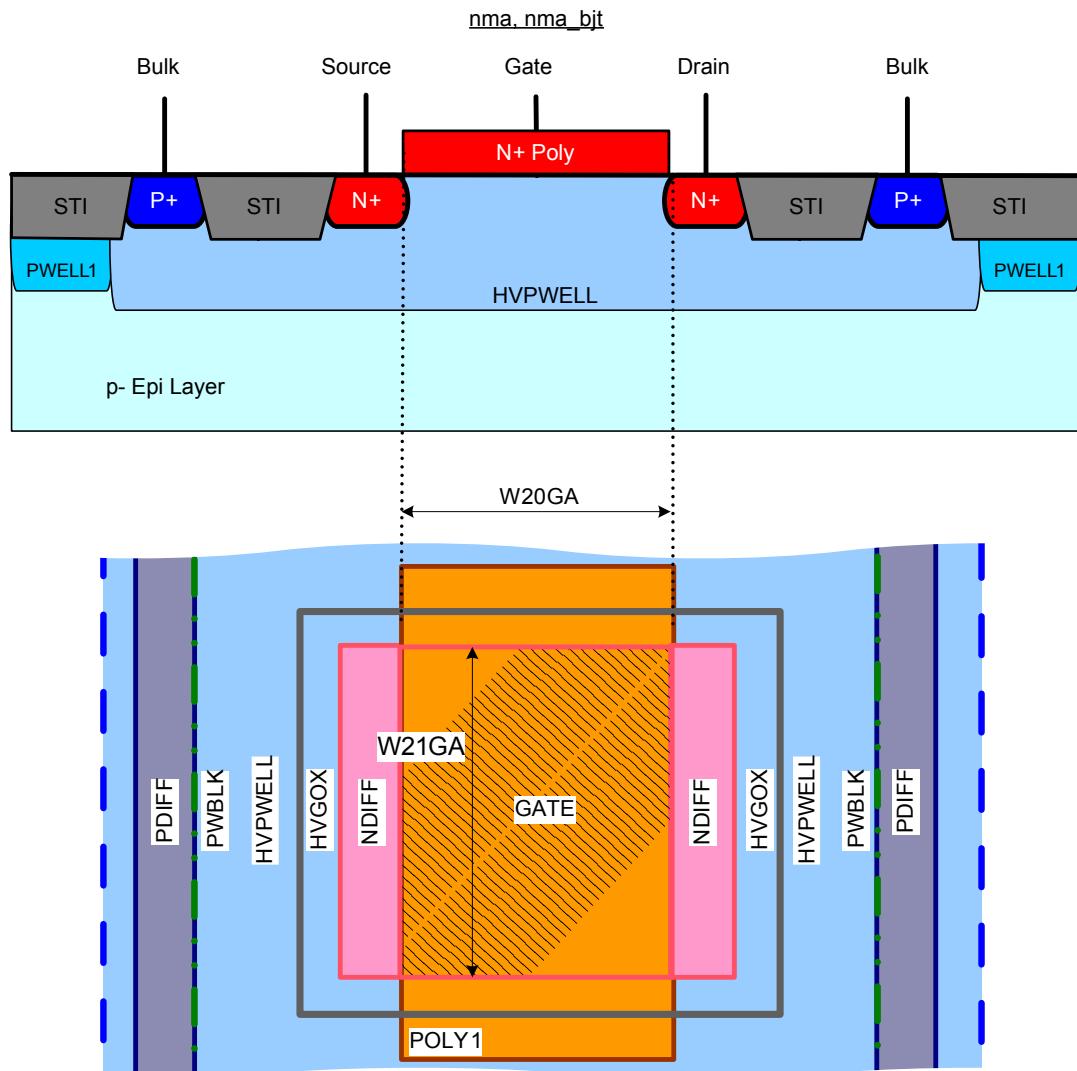


Figure 3.164 nma, nma_bjt

3. Layer and Device rules → 3.22 NHVE module

3.22 NHVE module

3.22.1 Layer rules

NDF

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B10ND	NDF must be surrounded by a GUARD RING consisting of PDIFF and HVPWELL Note: Valid outside HNW.	-	-
B11ND	POLY1 overlap of NDF is not allowed (except nh#, nm#) Note: Valid outside HNW.	-	-
B12ND	NDIFF overlap of NDF is not allowed Note: Valid inside HNW.	-	-
B13ND	NWELL overlap of NDF is not allowed (except nh#, nm#)	-	-
B1ND	NDF without HVGOX and PWBLK is not allowed. (except PWBLK for dnp20)	-	-
B2ND	NDF overlap of DNWELL, DNWELLMV, HVPWELL, ISOPW, SCI, DEPL or PDD is not allowed	-	-
B4ND	PDIFF overlap of NDF is not allowed	-	-
B5ND	NDF overlap of HVNWELL is not allowed Note: Valid outside HNW.	-	-
B6ND	NDF without HVNWELL is not allowed Note: Valid inside HNW.	-	-
B7ND	NDF overlap of rpp1#, rnp1#, rpp1s#, HRES or MRES is not allowed	-	-
B9ND	NW_VERIFY overlap of NDF is not allowed	-	-
B3ND	NDF crossing HNW edge is not allowed	-	-
B8ND	NWELL crossing NDF edge is not allowed	-	-
W1ND	Minimum NDF width	0.8	µm
W2ND	Minimum NDF width (except nm#) Note: Valid outside HNW.	5.32	µm
S1ND	Minimum NDF spacing/notch	0.54	µm
S2ND	Minimum NDF spacing (different net, except nhhv, nhvvd, nm#) Note: Valid outside HNW.	8.42	µm
S1NDDN	Minimum NDF spacing to NDIFF (except NDF of nm#) Note: Valid outside HNW.	4.5	µm
S1NDPP	Fixed NDF spacing to PDIFF (except nh#, nm#, dnp20) Note: Valid outside HNW.	4.0	µm
S1NDHN	Minimum NDF spacing to HVNWELL Note: Valid outside HNW.	10.0	µm
S1NDHP	Minimum NDF spacing to HVPWELL (except nh#, nm#) Note: Valid outside HNW.	3.76	µm
S1NDNW	Minimum NDF spacing to NWELL Note: Valid outside HNW.	10.0	µm
S1NDWD	Minimum NDF spacing to DNWELL Note: Valid outside HNW.	10.0	µm

3. Layer and Device rules → 3.22 NHVE module→ 3.22.1 Layer rules→ NDF

Name	Description	Value	Unit
S1NDWM	Minimum NDF spacing to DNWELLMV	10.0	μm
	Note: Valid outside HNW.		
E1GHND	Minimum HVGOX enclosure of NDF	0.5	μm
	Note: Valid outside HNW.		
E1NDDN	Fixed NDF enclosure of NDIFF (except dnp20, channel region of nh#, nm#)	1.0	μm
	Note: Valid outside HNW.		
E1PBND	Fixed PWBLK enclosure of NDF (except nh#, nm#, dnp20)	4.0	μm
	Note: Valid outside HNW.		

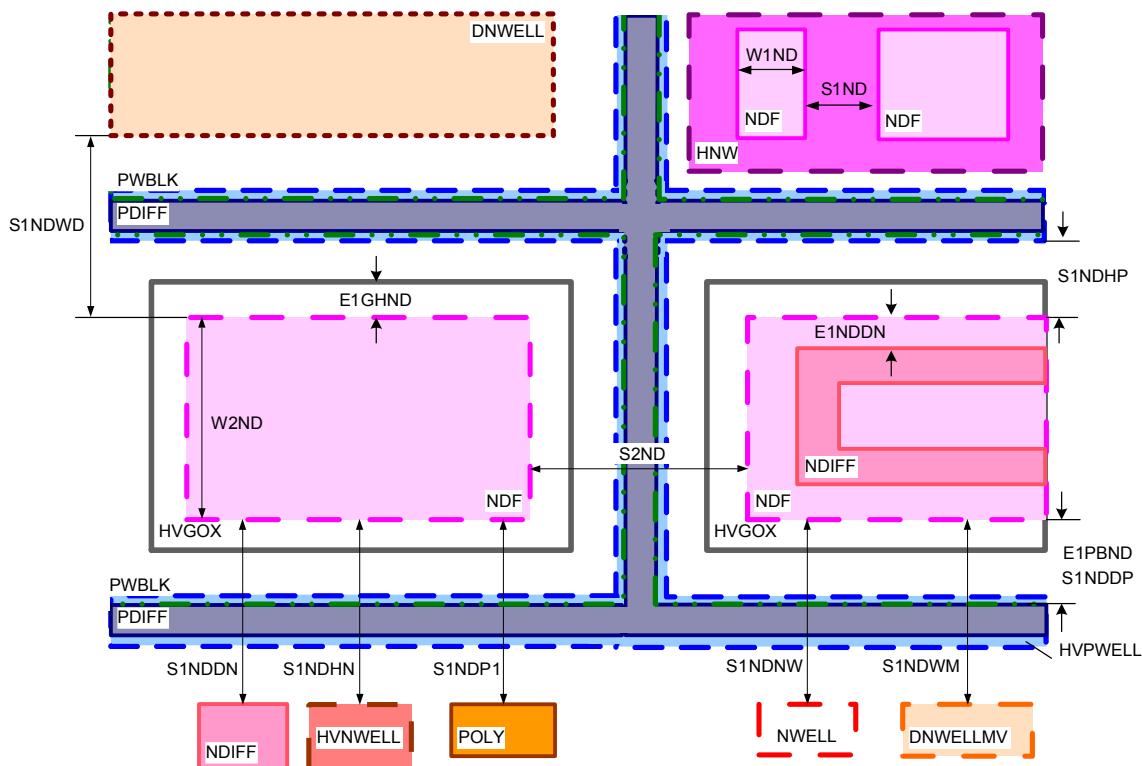


Figure 3.165 NDF

3. Layer and Device rules → 3.22 NHVE module→ 3.22.2 Device rules→ nhv, nhv_bjt

3.22.2 Device rules

nhv, nhv_bjt

Name	Description	Value	Unit
B1P1GA	Only a rectangular POLY1 over GATE is allowed	-	-
W28GA	Minimum GATE length	3.0	µm
W29GA	Minimum GATE width	4.0	µm
S12DF	Fixed DRAIN-EDGE-STI length	3.0	µm
S2NDDP	Fixed NDF spacing to PDIFF	4.0	µm
S2NDHP	Fixed NDF spacing to HVPWELL (in channel region)	0.5	µm
S2NWGA	Minimum NWELL spacing to GATE	2.78	µm
S5P1DN	Minimum POLY1 spacing to DRAIN NDIFF	2.4	µm
S7NDHP	Fixed NDF spacing to HVPWELL (except channel region)	3.76	µm
E2M1DN	Fixed MET1 enclosure of DRAIN NDIFF	1.0	µm
E3NDNW	Minimum NDF enclosure of NWELL	0.78	µm
E3NWDN	Minimum NWELL enclosure of NDIFF	0.22	µm
E4PBND	Fixed PWBLK enclosure of NDF (except channel region)	4.0	µm
E3P1DN	Minimum POLY1 extension beyond NDIFF	0.6	µm
E5P1GA	Fixed POLY1 extension beyond GATE (in GATE width direction)	1.2	µm
O2NDGA	Fixed NDF overlap of GATE	0.9	µm

Note: The layout of nhv and nhv_bjt is predefined and scalable concerning device width and length only. The other rules support the fixed dimensions of the layout or describe the relation to adjacent structures.

Note: nhv_bjt device must be labeled "bjt" using POLY1 (VERIFICATION) layer over the GATE.

3. Layer and Device rules → 3.22 NHVE module → 3.22.2 Device rules → nhv, nhv_bjt

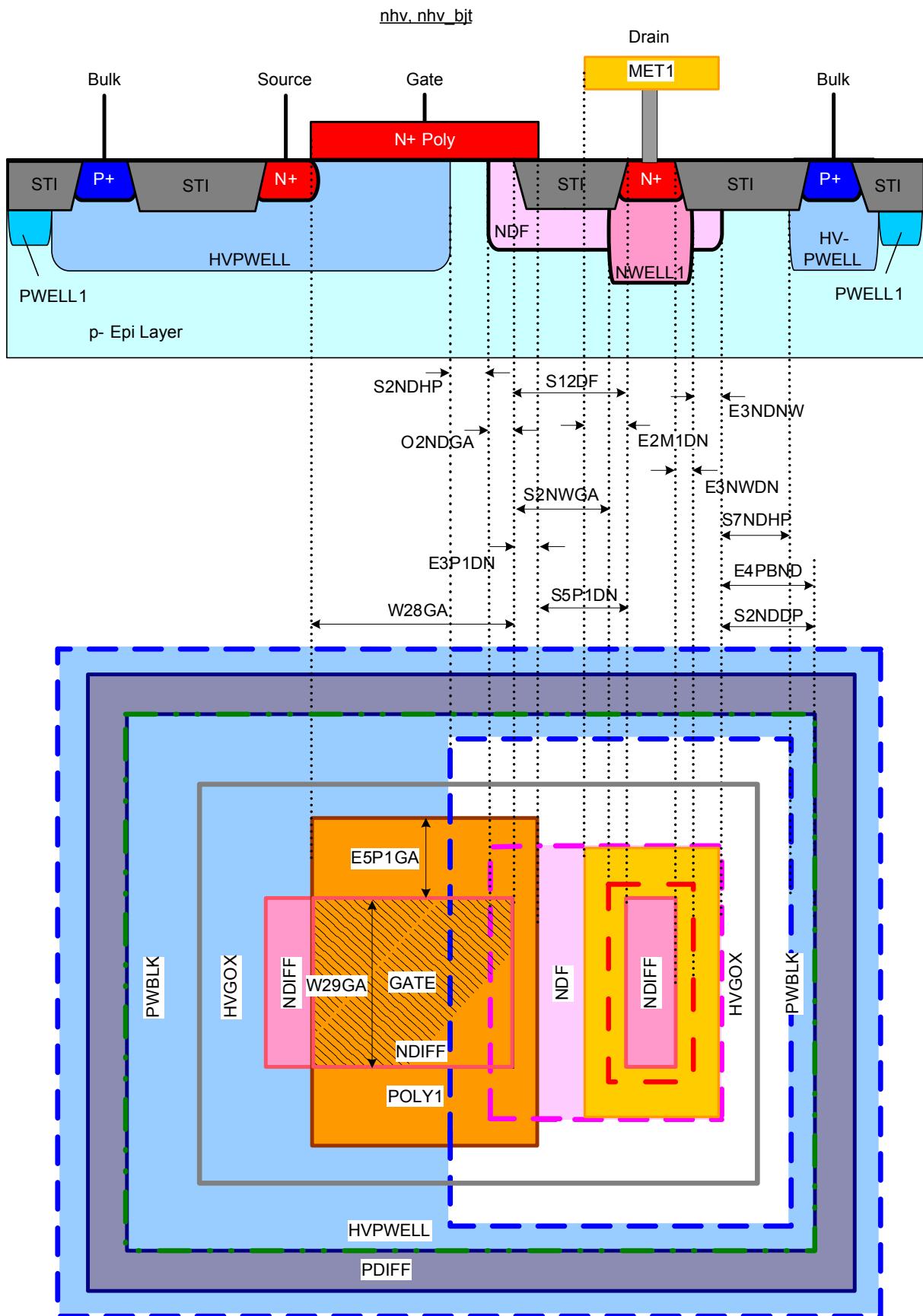


Figure 3.166 nhv, nhv_bjt

3. Layer and Device rules → 3.22 NHVE module→ 3.22.2 Device rules→ nhhv, nhhv_bjt

nhhv, nhhv_bjt

Name	Description	Value	Unit
B1P1GA	Only a rectangular POLY1 over GATE is allowed	-	-
W16GA	Minimum GATE length	5.0	µm
W17GA	Minimum GATE width	4.0	µm
S7DF	Fixed SOURCE/DRAIN-EDGE-STI length	3.0	µm
S2NDDP	Fixed NDF spacing to PDIFF	4.0	µm
S2NDHP	Fixed NDF spacing to HVPWELL (in channel region)	0.5	µm
S2NWGA	Minimum NWELL spacing to GATE	2.78	µm
S3P1DN	Minimum POLY1 spacing to SOURCE / DRAIN NDIFF	2.4	µm
S7NDHP	Fixed NDF spacing to HVPWELL (except channel region)	3.76	µm
E1M1DN	Fixed MET1 enclosure of SOURCE / DRAIN NDIFF	1.0	µm
E3NDNW	Minimum NDF enclosure of NWELL	0.78	µm
E3NWDN	Minimum NWELL enclosure of NDIFF	0.22	µm
E4PBND	Fixed PWBLK enclosure of NDF (except channel region)	4.0	µm
E3P1GA	Minimum POLY1 extension beyond GATE	0.6	µm
E5P1GA	Fixed POLY1 extension beyond GATE (in GATE width direction)	1.2	µm
O2NDGA	Fixed NDF overlap of GATE	0.9	µm

Note: The layout of nhhv and nhhv_bjt is predefined and scalable concerning device width and length only. The other rules support the fixed dimensions of the layout or describe the relation to adjacent structures.

Note: nhhv_bjt device must be labeled "bjt" using POLY1 (VERIFICATION) layer over the GATE.

3. Layer and Device rules → 3.22 NHVE module→ 3.22.2 Device rules→ nhhv, nhhv_bjt

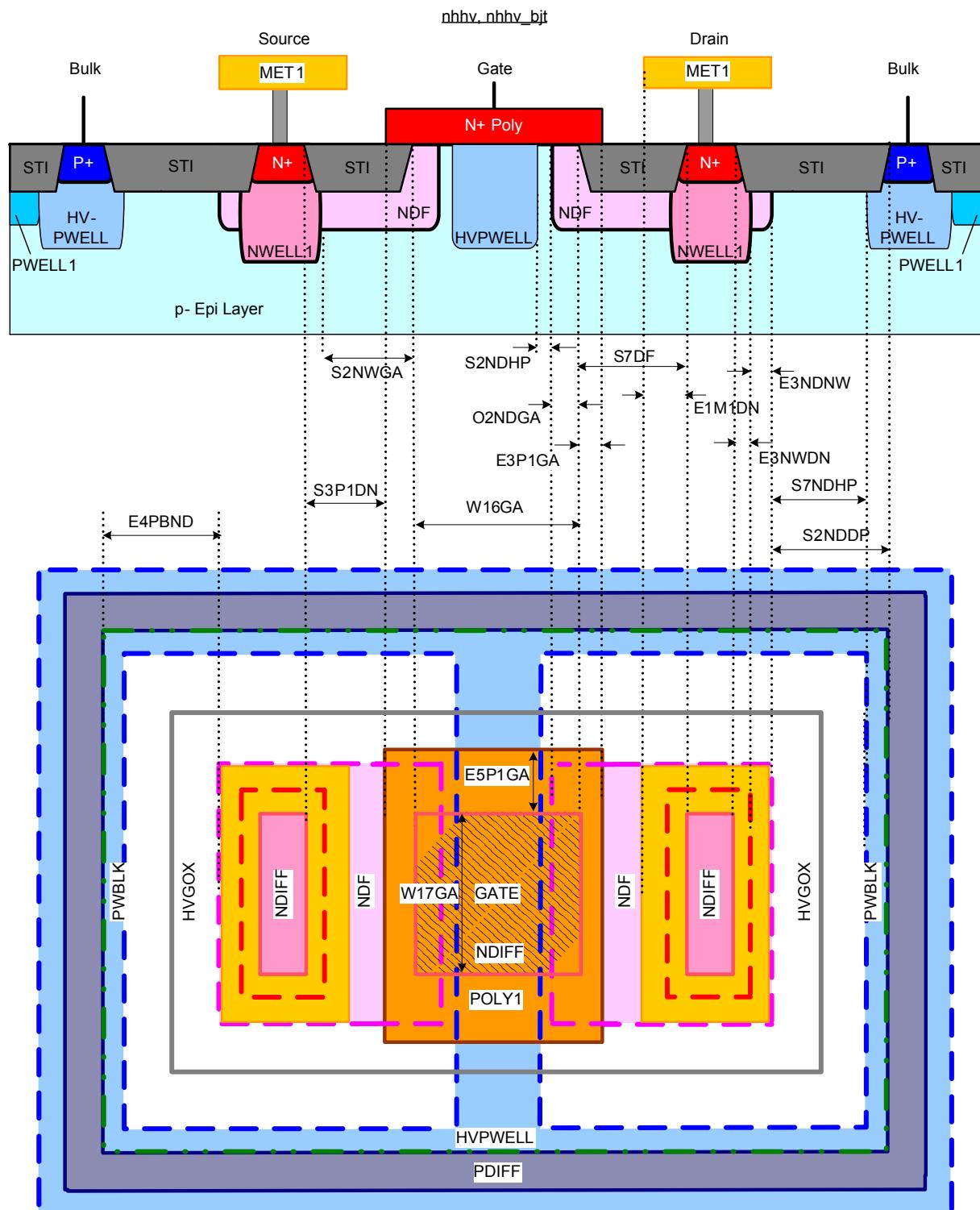


Figure 3.167 nhhv, nhhv_bjt

3. Layer and Device rules → 3.22 NHVE module→ 3.22.2 Device rules→ nmc, nmc_bjt

nmc, nmc_bjt

Name	Description	Value	Unit
W24GA	Minimum GATE length	1.5	µm
W25GA	Minimum GATE width	3.0	µm
W4ND	Minimum NDF width	2.82	µm
S9DF	Fixed DRAIN-EDGE-STI length	1.0	µm
S2NDDN	Minimum NDF spacing to NDIFF	3.0	µm
S3NDDP	Fixed NDF spacing to PDIFF	2.0	µm
S3NWGA	Minimum NWELL spacing to GATE	0.78	µm
S4NDHP	Fixed NDF spacing to HVPWELL (in channel region)	0.0	µm
S4P1DN	Minimum POLY1 spacing to DRAIN NDIFF	0.5	µm
S6NDHP	Fixed NDF spacing to HVPWELL (except channel region)	1.76	µm
E2NDNW	Minimum NDF enclosure of NWELL	0.78	µm
E2PBND	Fixed PWBLK enclosure of NDF (except channel region)	2.0	µm
E4NWDN	Minimum NWELL enclosure of NDIFF	0.22	µm
E2P1DN	Minimum POLY1 extension beyond NDIFF	0.5	µm
O3NDGA	Fixed NDF overlap of GATE	0.4	µm

Note: The layout of nmc and nmc_bjt is predefined and scalable concerning device width and length only. The other rules support the fixed dimensions of the layout or describe the relation to adjacent structures.

Note: nmc_bjt device must be labeled "bjt" using POLY1 (VERIFICATION) layer over the GATE.

3. Layer and Device rules → 3.22 NHVE module → 3.22.2 Device rules → nmc, nmc_bjt

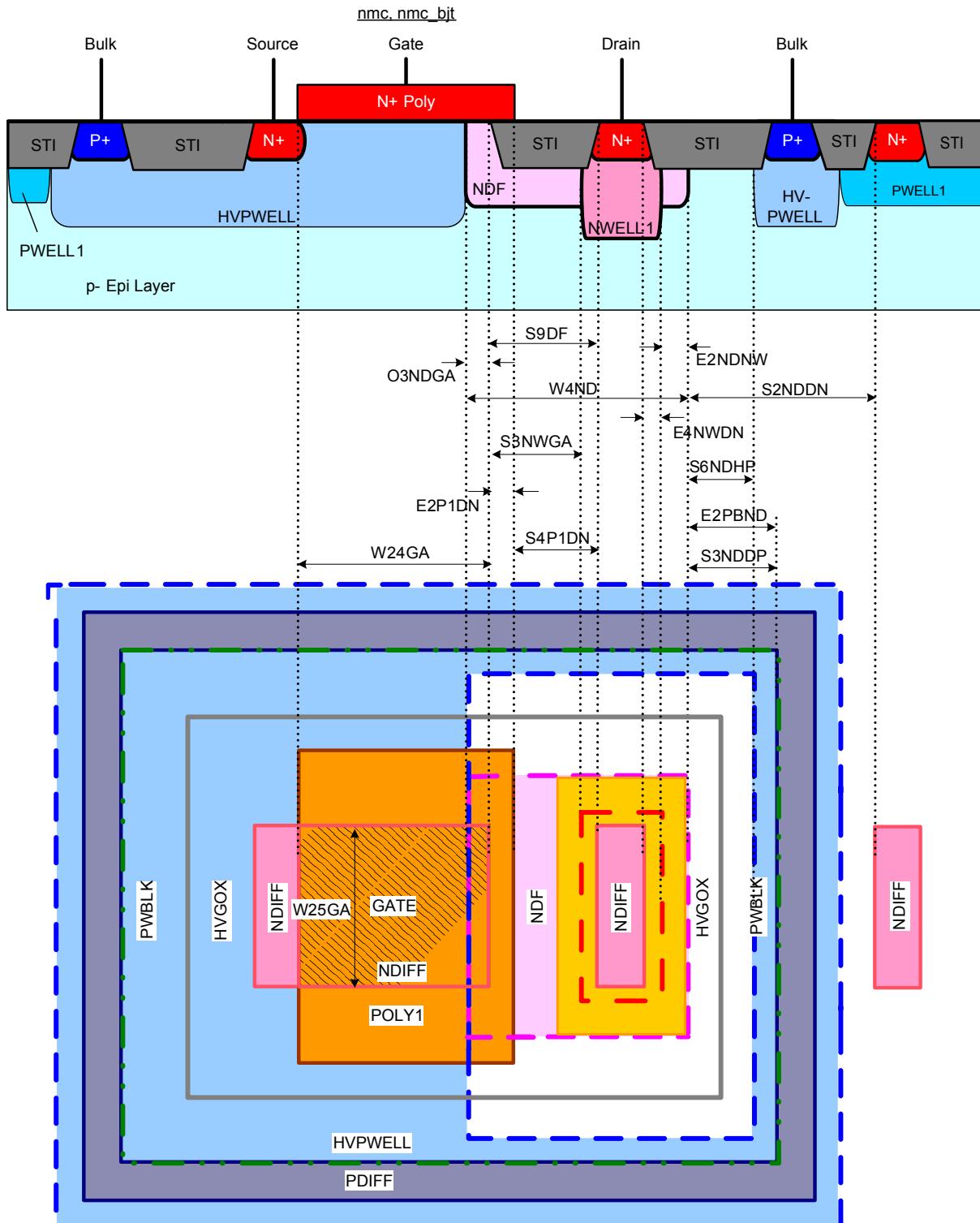


Figure 3.168 nmc, nmc_bjt

3. Layer and Device rules → 3.22 NHVE module→ 3.22.2 Device rules→ nmmc, nmmc_bjt

nmmc, nmmc_bjt

Name	Description	Value	Unit
W12GA	Minimum GATE length	2.0	µm
W13GA	Minimum GATE width	3.0	µm
W3ND	Minimum NDF width	2.82	µm
S6DF	Fixed SOURCE/DRAIN-EDGE-STI length	1.0	µm
S1NWGA	Minimum NWELL spacing to GATE	0.78	µm
S2NDDN	Minimum NDF spacing to NDIFF	3.0	µm
S2P1DN	Minimum POLY1 spacing to SOURCE / DRAIN NDIFF	0.5	µm
S3NDDP	Fixed NDF spacing to PDIFF	2.0	µm
S3NDHP	Fixed NDF spacing to HVPWELL (in channel region)	0.0	µm
S5NDHP	Fixed NDF spacing to HVPWELL (except channel region)	1.76	µm
E1NDNW	Minimum NDF enclosure of NWELL	0.78	µm
E2NWDN	Minimum NWELL enclosure of NDIFF	0.22	µm
E2PBND	Fixed PWBLK enclosure of NDF (except channel region)	2.0	µm
E2P1GA	Minimum POLY1 extension beyond GATE	0.5	µm
O1NDGA	Fixed NDF overlap of GATE	0.4	µm

Note: The layout of nmmc and nmmc_bjt is predefined and scalable concerning device width and length only. The other rules support the fixed dimensions of the layout or describe the relation to adjacent structures.

Note: nmmc_bjt device must be labeled "bjt" using POLY1 (VERIFICATION) layer over the GATE.

3. Layer and Device rules → 3.22 NHVE module → 3.22.2 Device rules → nmmc, nmmc_bjt

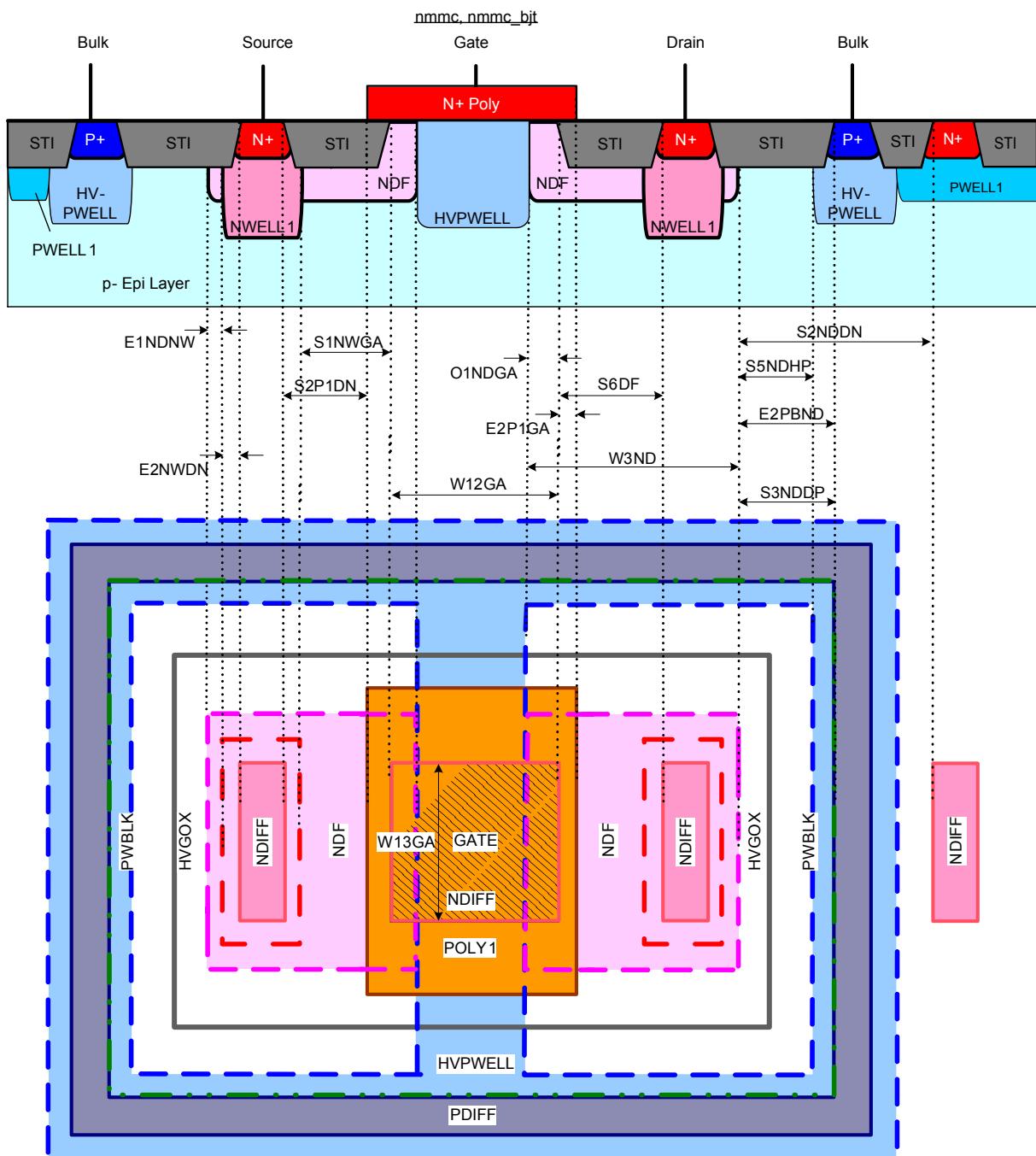


Figure 3.169 nmmc, nmmc_bjt

3. Layer and Device rules → 3.22 NHVE module→ 3.22.2 Device rules→ nmmd, nmmd_bjt

nmmd, nmmd_bjt

Name	Description	Value	Unit
W30GA	Fixed GATE length	3.2	µm
W31GA	Minimum GATE width	3.0	µm
W5ND	Minimum NDF width	2.82	µm
S13DF	Fixed SOURCE/DRAIN-EDGE-STI length	1.0	µm
S2NDDN	Minimum NDF spacing to NDIFF	3.0	µm
S4NDDP	Fixed NDF spacing to PDIFF	2.0	µm
S4NWGA	Minimum NWELL spacing to GATE	0.78	µm
S6P1DN	Minimum POLY1 spacing to SOURCE / DRAIN NDIFF	0.5	µm
S8NDHP	Fixed NDF spacing to HVPWELL (in channel region)	0.3	µm
S9NDHP	Fixed NDF spacing to HVPWELL (except channel region)	1.76	µm
E3PBND	Fixed PWBLK enclosure of NDF (except channel region)	2.0	µm
E4NDNW	Minimum NDF enclosure of NWELL	0.78	µm
E5NWDN	Minimum NWELL enclosure of NDIFF	0.22	µm
E7P1GA	Minimum POLY1 extension beyond GATE	0.5	µm
O4NDGA	Fixed NDF overlap of GATE	0.9	µm

Note: nmmd and nmmd_bjt devices must be labeled "nmmd" using POLY1 (VERIFICATION) layer over the GATE.

Note: The layout of nmmd and nmmd_bjt is predefined and scalable concerning device width and length only. The other rules support the fixed dimensions of the layout or describe the relation to adjacent structures.

Note: nmmd_bjt device must be labeled "bjt" using POLY1 (VERIFICATION) layer over the GATE.

3. Layer and Device rules → 3.22 NHVE module→ 3.22.2 Device rules→ nmmd, nmmd_bjt

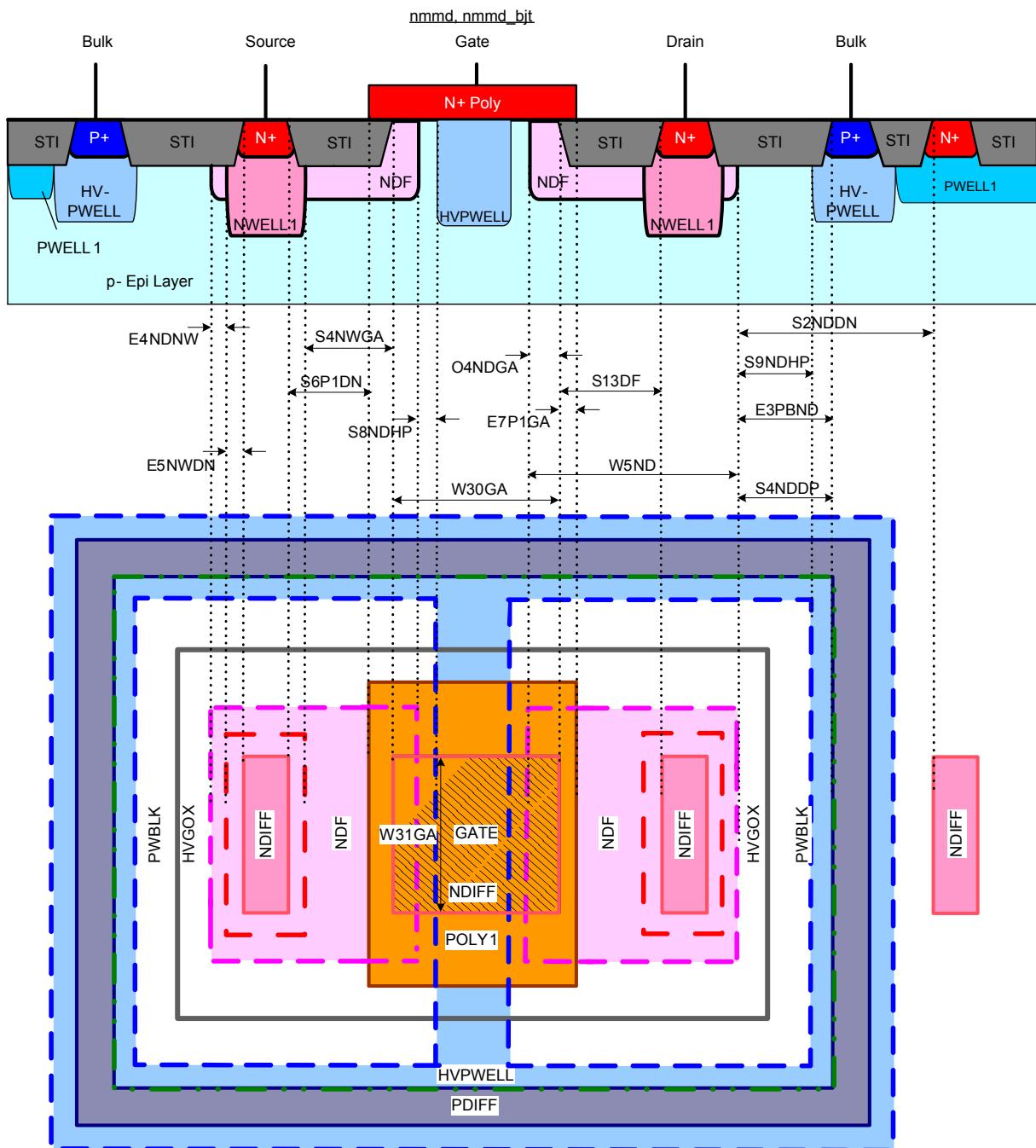


Figure 3.170 nmmd, nmmd_bjt

3. Layer and Device rules → 3.22 NHVE module → 3.22.2 Device rules → dndf

dndf

Note: The layer DIODEF must enclose the pn junction, crossing the pn junction is not allowed.

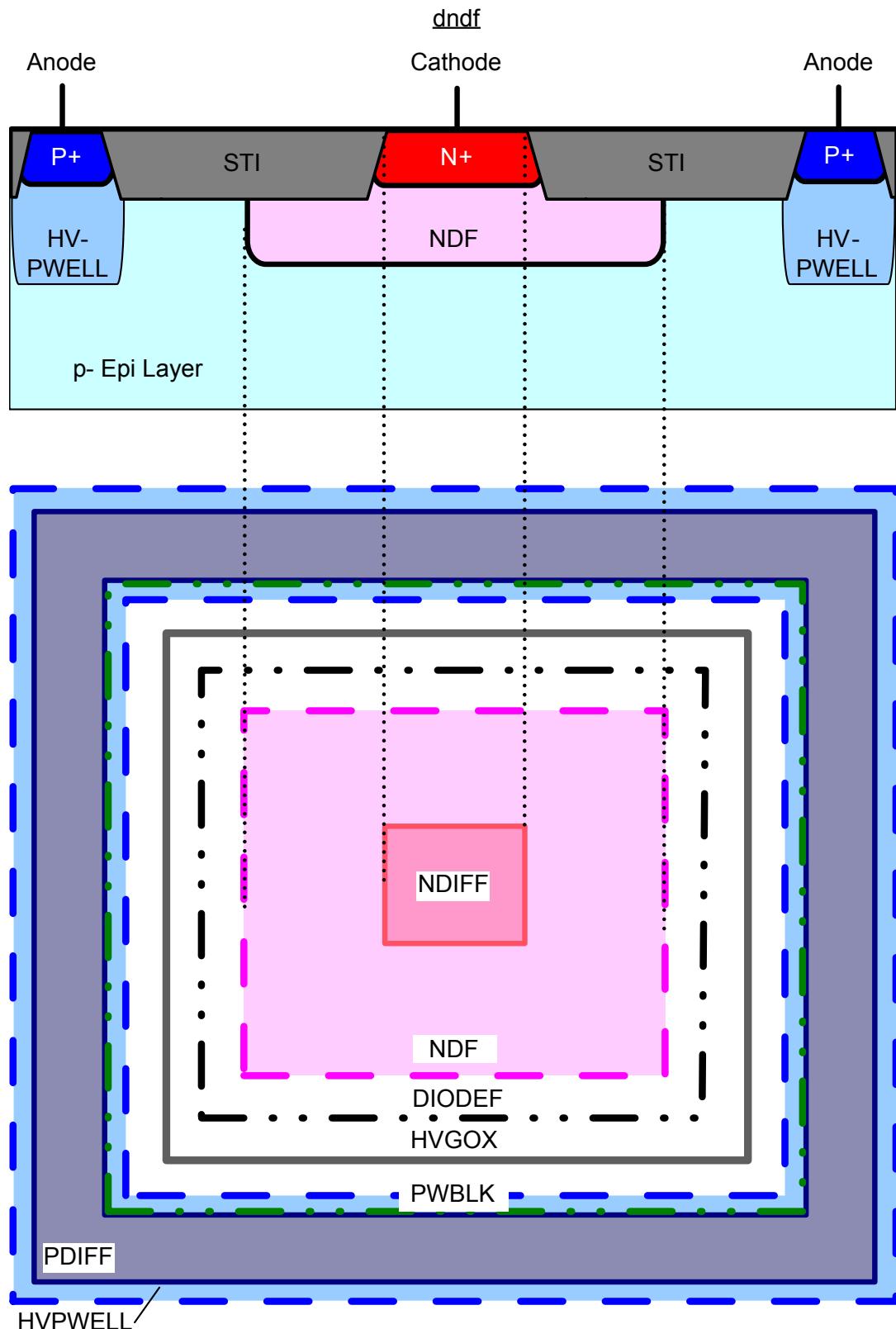


Figure 3.171 dndf

3. Layer and Device rules → 3.22 NHVE module→ 3.22.2 Device rules→ dnp20

dnp20

Note: The layout of the dnp20 protection diode is predefined and only the NDF width (cathode) can be changed in the range of 20 µm to 100 µm. Fixed NDF length (cathode) is 6 µm. The drawing below is a basic sketch only and does not give all details.

Note: The layer DIODEF must enclose the pn junction, crossing the pn junction is not allowed.

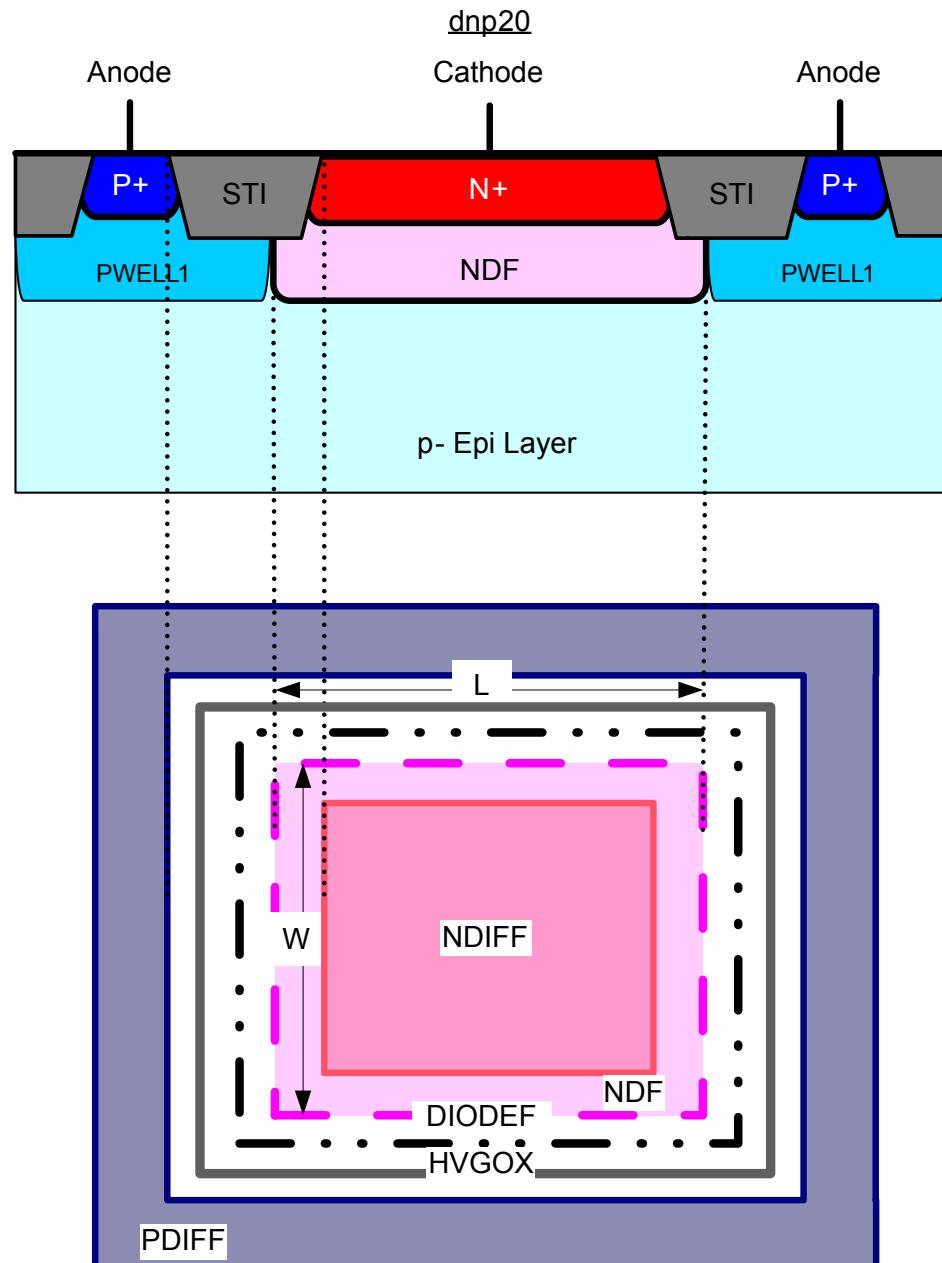


Figure 3.172 dnp20

3. Layer and Device rules → 3.23 HVMOS module

3.23 HVMOS module

3.23.1 Layer rules

HNW

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1HW	HNW without HVGOX and PWBLK is not allowed (except qpvhscr, dsb#)	-	-
B2HW	HNW must be surrounded by a GUARD RING consisting of PDIFF and HVPWELL	-	-
B3HW	HNW overlap of DNWELL, DNWELLMV, NWELL, HVPWELL, ISOPW, SCI, DEPL or PDD is not allowed. (except ISOPW and NWELL for qpvhscr, HVPWELL for qpvhbscr)	-	-
B5HW	HNW overlap of rpp1#, rnp1#, rpp1s#, MRES or HRES is not allowed	-	-
B4HW	HVNWELL crossing HNW edge is not allowed	-	-
W1HW	Minimum HNW width	8.0	µm
S1HW	Minimum HNW spacing/notch	10.0	µm
S1HWDN	Minimum HNW spacing to NDIF	4.5	µm
S1HWDP	Fixed HNW spacing to PDIFF	4.0	µm
S1HWHN	Minimum HNW spacing to HVNWELL	10.0	µm
S1HWHP	Minimum HNW spacing to HVPWELL	3.76	µm
S1HWND	Minimum HNW spacing to NDF	10.0	µm
S1HWNW	Minimum HNW spacing to NWELL	10.0	µm
S1HWP1	Minimum HNW spacing to POLY1	5.35	µm
S1HWWD	Minimum HNW spacing to DNWELL	10.0	µm
S1HWWM	Minimum HNW spacing to DNWELLMV	10.0	µm
E1GHHW	Minimum HVGOX enclosure of HNW	0.5	µm
E1HWDN	Fixed HNW enclosure of NDIF (except qpvhscr, qpvhbscr, dsb#)	2.0	µm
E1HWDP	Minimum HNW enclosure of PDIFF	2.86	µm
E1HWHN	Minimum HNW enclosure of HVNWELL	1.76	µm
E1HWP1	Minimum HNW enclosure of POLY1	2.95	µm
E1PBHW	Fixed PWBLK enclosure of HNW	4.0	µm

3. Layer and Device rules → 3.23 HVMOS module → 3.23.1 Layer rules → HNW

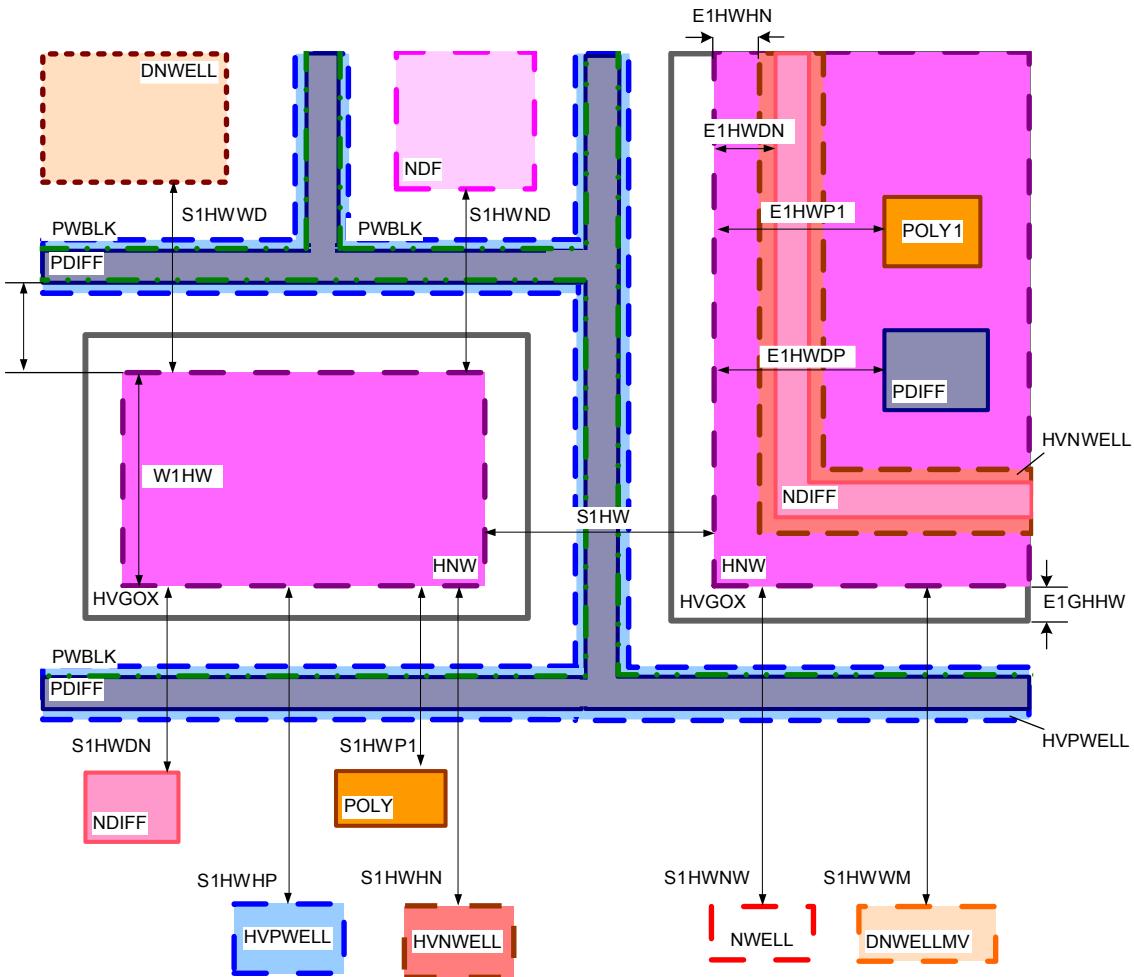


Figure 3.173 HNW

3. Layer and Device rules → 3.23 HVPMOS module→ 3.23.1 Layer rules→ HVGOX

HVGOX

Name	Description	Value	Unit
B1GHMV	HVGOX overlap of MV is not allowed	-	-
B1GH	DIFF crossing HVGOX edge is not allowed	-	-
W1GH	Minimum HVGOX width	0.6	μm
S1GH	Minimum HVGOX spacing/notch	1.0	μm
S1GHDF	Minimum HVGOX spacing to DIFF	0.2	μm
E1GHDF	Minimum HVGOX enclosure of DIFF	0.2	μm

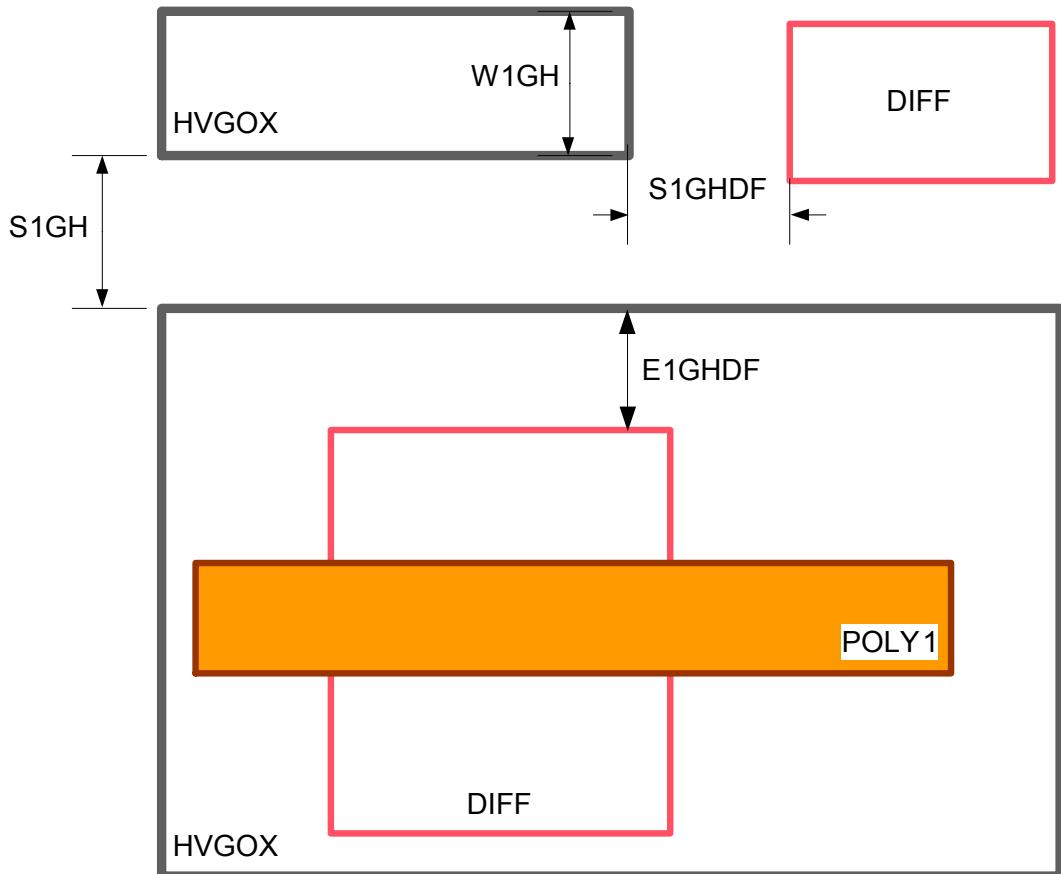


Figure 3.174 HVGOX

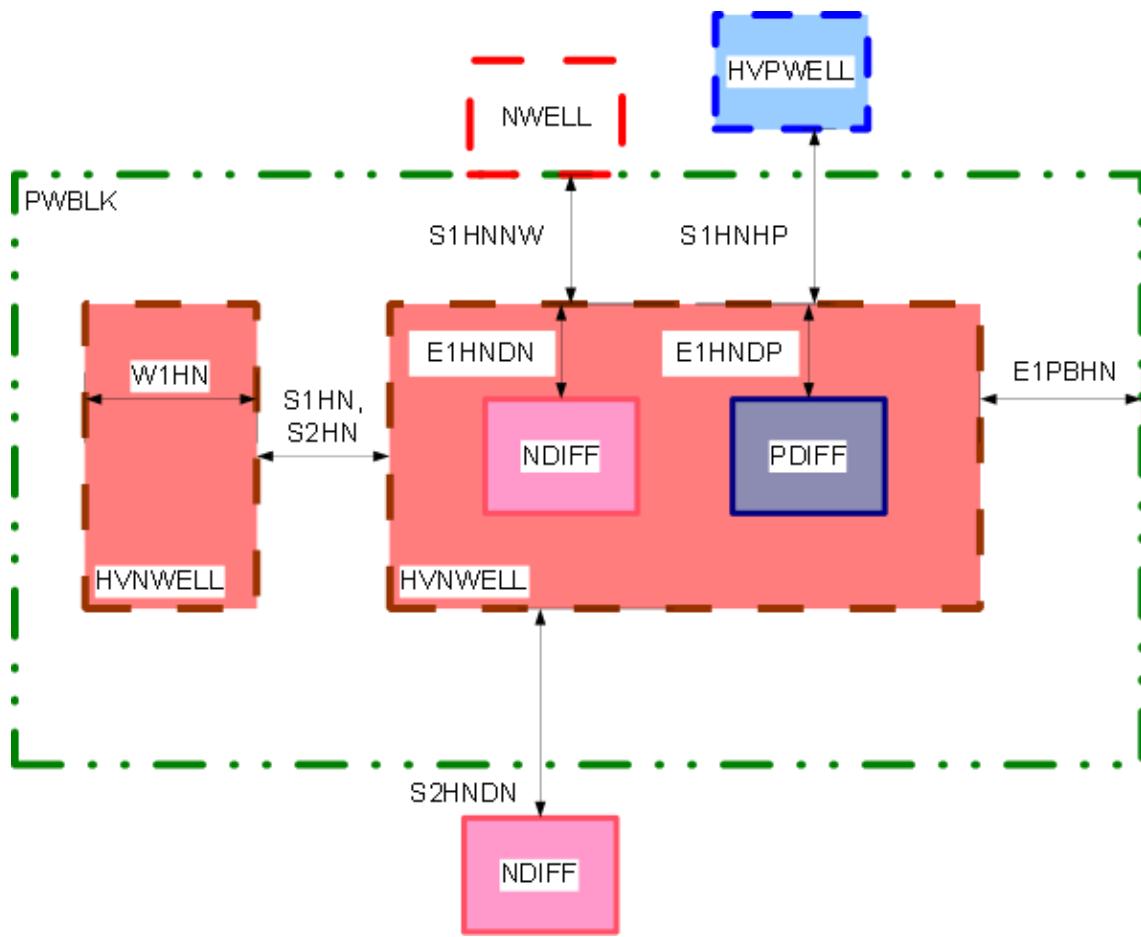
3. Layer and Device rules → 3.23 HVPMOS module→ 3.23.1 Layer rules→ HVNWELL

HVNWELL

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1HN	HVNWELL must be contacted by NDIFF	-	-
B2HN	HVNWELL overlap of HVPWELL or PDD is not allowed	-	-
B3HN	HVNWELL overlap of NWELL is not allowed (except qnva)	-	-
B5HN	HVNWELL without PWBLK is not allowed Note: Valid outside DNWELL/DNWELLMV/HNW.	-	-
B7HN	HVNWELL overlap of DNWELL is not allowed Note: Valid inside DNWELLMV.	-	-
B4HN	DIFF crossing HVNWELL edge is not allowed (except ped#, pmma, nmma, pm#, ph#, pma)	-	-
B6HN	HVNWELL crossing DNWELL edge is not allowed	-	-
W1HN	Minimum HVNWELL width	0.9	μm
S1HN	Minimum HVNWELL spacing/notch	0.6	μm
S2HN	Minimum HVNWELL spacing (different net) Note: Valid outside DNWELL/DNWELLMV/HNW.	7.0	μm
S1HNDN	Minimum HVNWELL spacing to NDIFF	0.43	μm
S1HNHP	Minimum HVNWELL spacing to HVPWELL (except ped#, pmma, nmma, qpvascr, qpvhbscr) Note: Valid outside of DNWELLMV.	3.0	μm
S1HNNW	Minimum HVNWELL spacing to NWELL	3.0	μm
S2HNDN	Minimum HVNWELL spacing to NDIFF Note: Valid outside DNWELL/DNWELLMV/HNW.	3.43	μm
S2HNHP	Minimum HVNWELL spacing to HVPWELL Note: Valid inside DNWELLMV.	0.8	μm
E1HNDN	Minimum HVNWELL enclosure of NDIFF (except qnva)	0.12	μm
E1HNDP	Minimum HVNWELL enclosure of PDIFF	0.43	μm
E1PBHN	Fixed PWBLK enclosure of HVNWELL (except nmma) Note: Valid outside DNWELL/DNWELLMV/HNW.	3.0	μm
E2HNDN	Minimum HVNWELL enclosure of NDIFF Note: Valid outside DNWELL/DNWELLMV/HNW.	0.43	μm

3. Layer and Device rules → 3.23 HVPMOS module → 3.23.1 Layer rules → HVNWELL

**Figure 3.175 HVNWELL**

3. Layer and Device rules → 3.23 HVMOS module→ 3.23.1 Layer rules→ HVPWELL

HVPWELL

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1HP	HVPWELL must be contacted by PDIFF	-	-
B3HP	HVPWELL overlap of NWELL is not allowed	-	-
B5HP	HVPWELL overlap of DNWELL is not allowed Note: Valid inside DNWELLMV.	-	-
B2HP	DIFF crossing HVPWELL edge is not allowed (except ped, ned#, nm#, nh#, pmma, nmma)	-	-
B4HP	HVPWELL crossing DNWELL edge is not allowed	-	-
W1HP	Minimum HVPWELL width	0.9	μm
S1HP	Minimum HVPWELL spacing/notch	0.6	μm
S2HP	Minimum HVPWELL spacing (different net) Note: Not valid for channel region of pmma GATE (oversized by 0.43 μm).	3.0	μm
S1HPDN	Minimum HVPWELL spacing to NDIFF (except ned#)	0.43	μm
S1HPDP	Minimum HVPWELL spacing to PDIFF	0.43	μm
S1HPNW	Minimum HVPWELL spacing to NWELL Note: Valid inside DNWELLMV.	0.8	μm
S2HPDN	Fixed HVPWELL spacing to NDIFF (except ned#, ped#, qpvascr) Note: Valid inside DNWELL and NOT DNWELLMV.	3.0	μm
S2HPNW	Minimum HVPWELL spacing to NWELL Note: Valid inside DNWELL and NOT DNWELLMV.	3.0	μm
E1HPDN	Minimum HVPWELL enclosure of NDIFF	0.43	μm
E1HPDP	Minimum HVPWELL enclosure of PDIFF (except ped#, pmma, nmma) Note: Valid inside DNWELLMV/DNWELL.	0.43	μm

3. Layer and Device rules → 3.23 HVMOS module → 3.23.1 Layer rules → HVPWELL

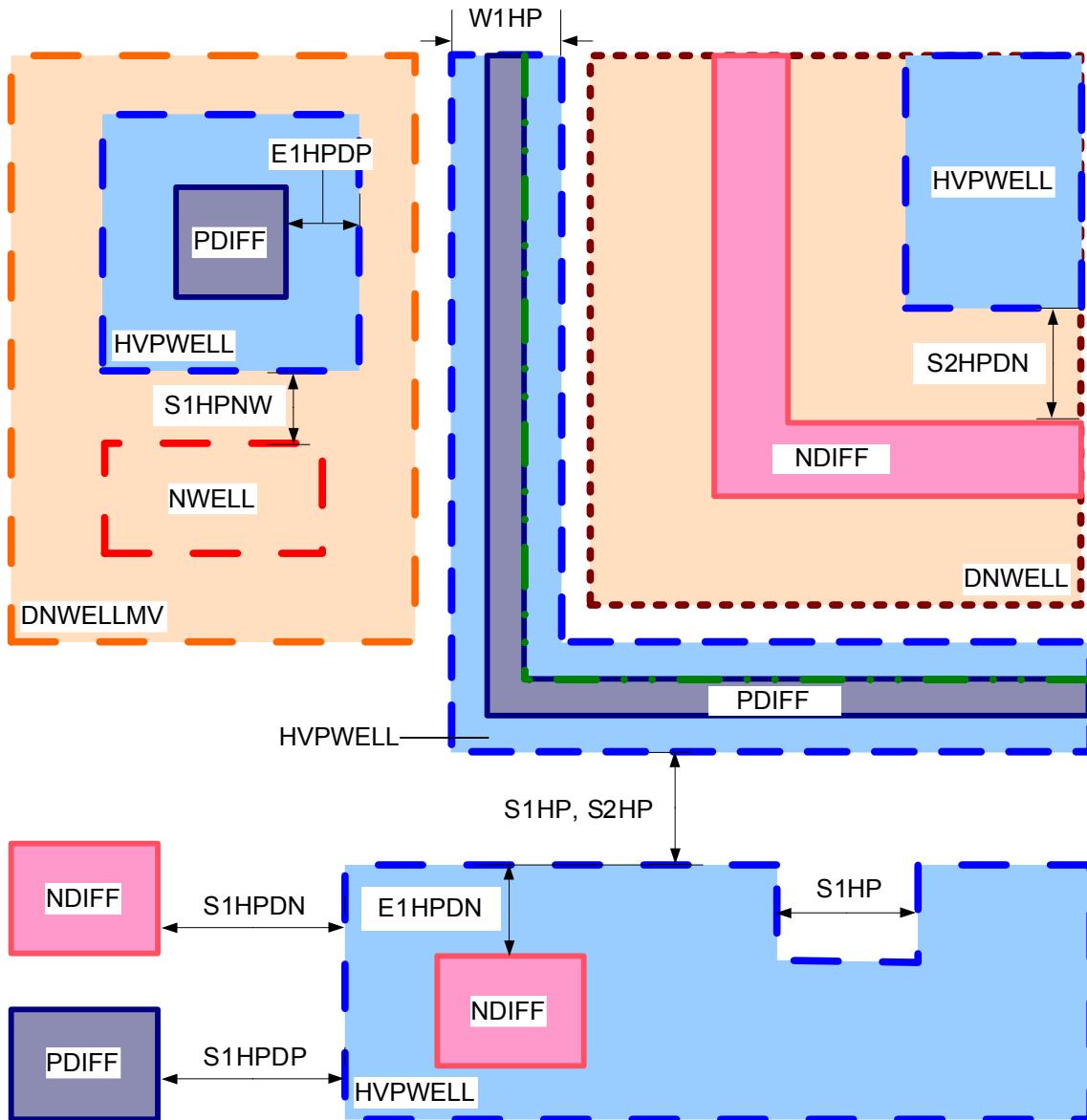


Figure 3.176 HVPWELL

3. Layer and Device rules → 3.23 HVPMOS module→ 3.23.1 Layer rules→ NDF

NDF

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B10ND	NDF must be surrounded by a GUARD RING consisting of PDIFF and HVPWELL Note: Valid outside HNW.	-	-
B11ND	POLY1 overlap of NDF is not allowed (except nh#, nm#) Note: Valid outside HNW.	-	-
B12ND	NDIFF overlap of NDF is not allowed Note: Valid inside HNW.	-	-
B13ND	NWELL overlap of NDF is not allowed (except nh#, nm#)	-	-
B1ND	NDF without HVGOX and PWBLK is not allowed. (except PWBLK for dnp20)	-	-
B2ND	NDF overlap of DNWELL, DNWELLMV, HVPWELL, ISOPW, SCI, DEPL or PDD is not allowed	-	-
B4ND	PDIFF overlap of NDF is not allowed	-	-
B5ND	NDF overlap of HVNWELL is not allowed Note: Valid outside HNW.	-	-
B6ND	NDF without HVNWELL is not allowed Note: Valid inside HNW.	-	-
B7ND	NDF overlap of rpp1#, rnp1#, rpp1s#, HRES or MRES is not allowed	-	-
B9ND	NW_VERIFY overlap of NDF is not allowed	-	-
B3ND	NDF crossing HNW edge is not allowed	-	-
B8ND	NWELL crossing NDF edge is not allowed	-	-
W1ND	Minimum NDF width	0.8	μm
W2ND	Minimum NDF width (except nm#) Note: Valid outside HNW.	5.32	μm
S1ND	Minimum NDF spacing/notch	0.54	μm
S2ND	Minimum NDF spacing (different net, except nhhv, nhhvd, nm#) Note: Valid outside HNW.	8.42	μm
S1NDDN	Minimum NDF spacing to NDIFF (except NDF of nm#) Note: Valid outside HNW.	4.5	μm
S1NDPP	Fixed NDF spacing to PDIFF (except nh#, nm#, dnp20) Note: Valid outside HNW.	4.0	μm
S1NDHN	Minimum NDF spacing to HVNWELL Note: Valid outside HNW.	10.0	μm
S1NDHP	Minimum NDF spacing to HVPWELL (except nh#, nm#) Note: Valid outside HNW.	3.76	μm
S1NDNW	Minimum NDF spacing to NWELL Note: Valid outside HNW.	10.0	μm
S1NDWD	Minimum NDF spacing to DNWELL Note: Valid outside HNW.	10.0	μm
S1NDWM	Minimum NDF spacing to DNWELLMV Note: Valid outside HNW.	10.0	μm
E1GHND	Minimum HVGOX enclosure of NDF Note: Valid outside HNW.	0.5	μm

3. Layer and Device rules → 3.23 HVPMOS module → 3.23.1 Layer rules → NDF

Name	Description	Value	Unit
E1NDDN	Fixed NDF enclosure of NDIFF (except dnp20, channel region of nh#, nm#)	1.0	μm
Note:	Valid outside HNW.		
E1PBND	Fixed PWBLK enclosure of NDF (except nh#, nm#, dnp20)	4.0	μm
Note:	Valid outside HNW.		

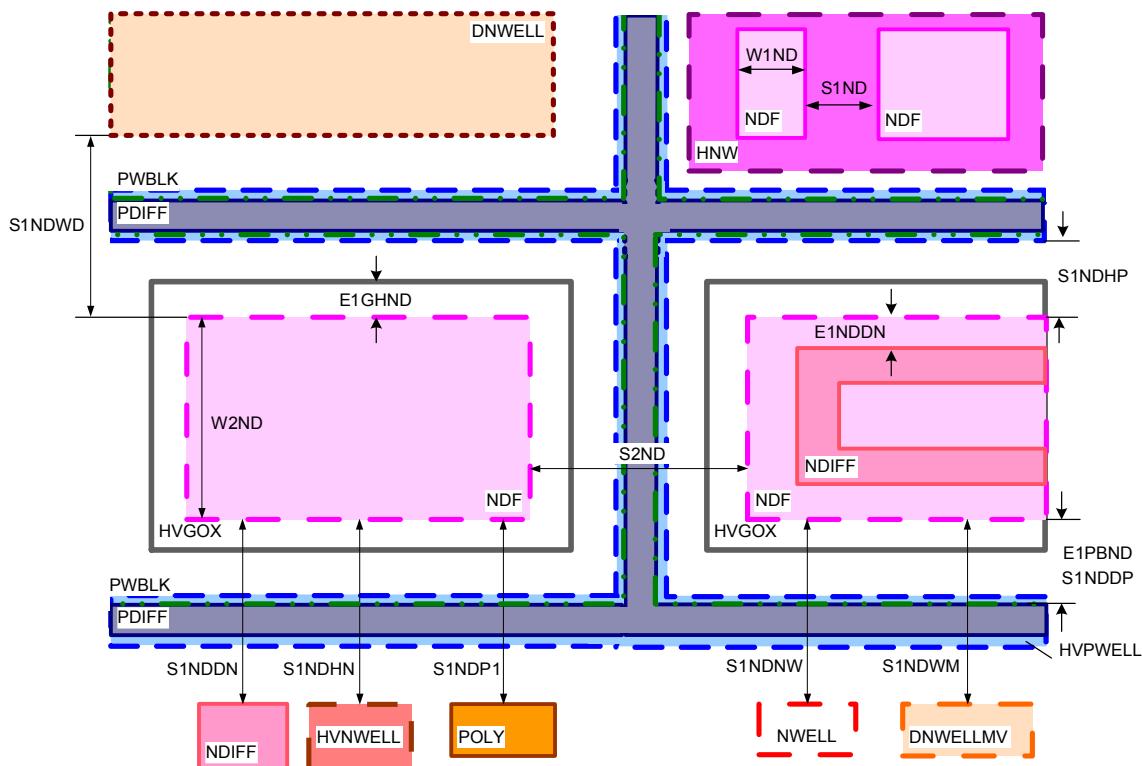


Figure 3.177 NDF

3. Layer and Device rules → 3.23 HVMOS module → 3.23.2 Device rules → pma, pma_bjt

3.23.2 Device rules

pma, pma_bjt

Name	Description	Value	Unit
W22GA	Minimum GATE length	1.0	μm
W23GA	Minimum GATE width	2.5	μm

Note: The layout of pma and pma_bjt is predefined and scalable concerning device width and length only. The other rules support the fixed dimensions of the layout or describe the relation to adjacent structures.

Note: pma_bjt device must be labeled “bjt” using POLY1 (VERIFICATION) layer over the GATE.

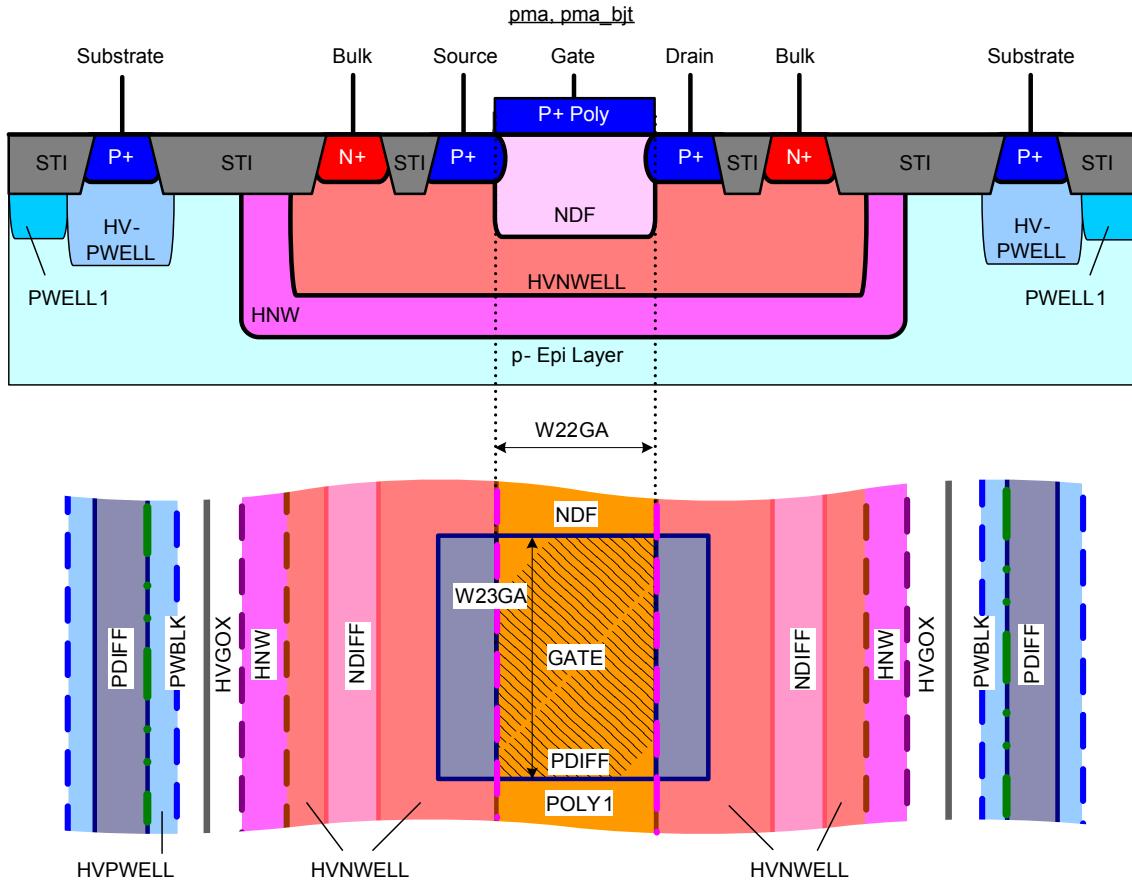


Figure 3.178 pma, pma_bjt

3. Layer and Device rules → 3.23 HVPMOS module → 3.23.2 Device rules → dwhn

dwhn

Note: The layer DIODEF must enclose the pn junction, crossing the pn junction is not allowed.

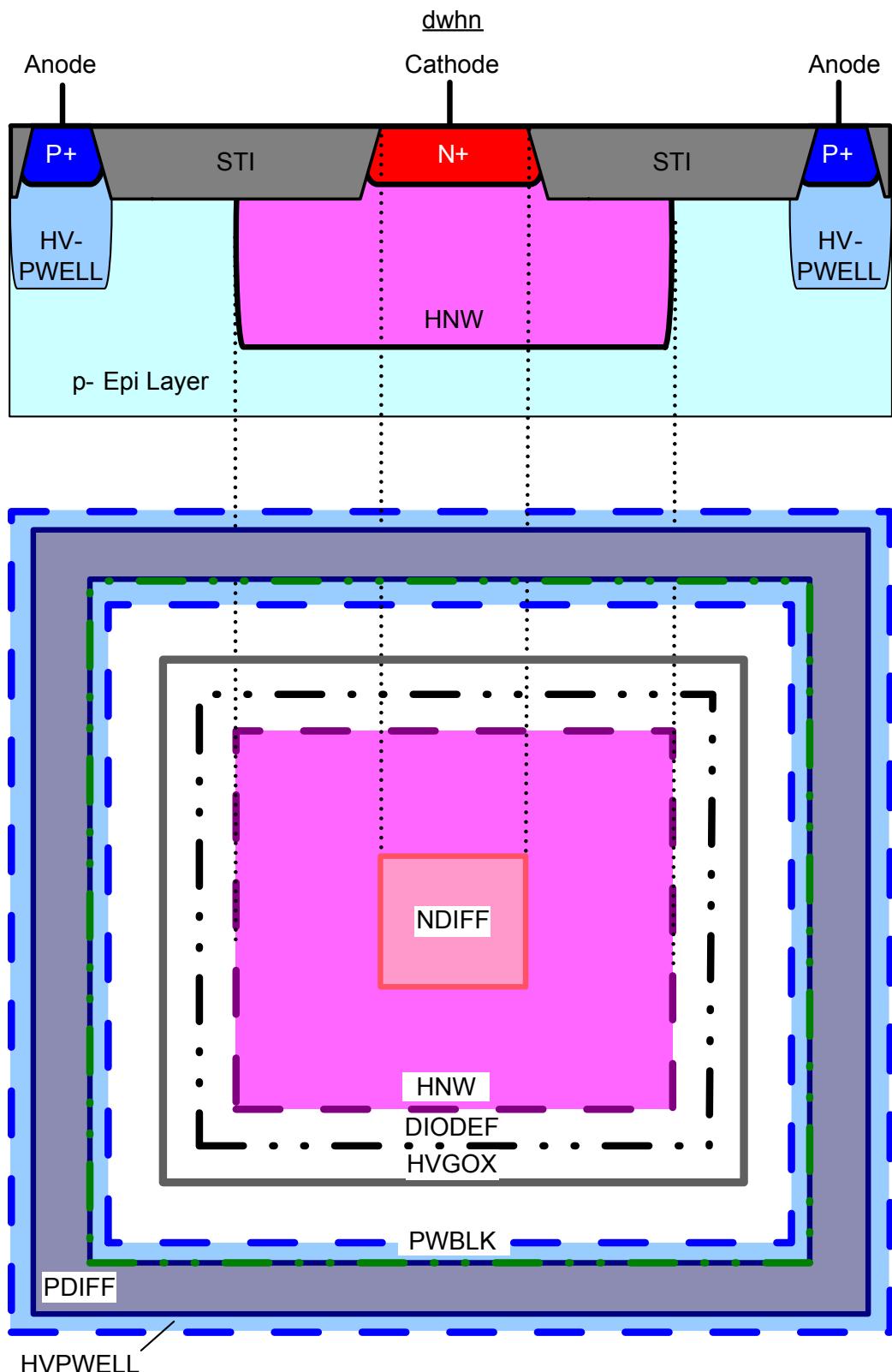


Figure 3.179 dwhn

3. Layer and Device rules → 3.23 HVPMOS module → 3.23.2 Device rules → dpwhn

dpwhn

Note: The layer DIODEF must enclose the pn junction, crossing the pn junction is not allowed.

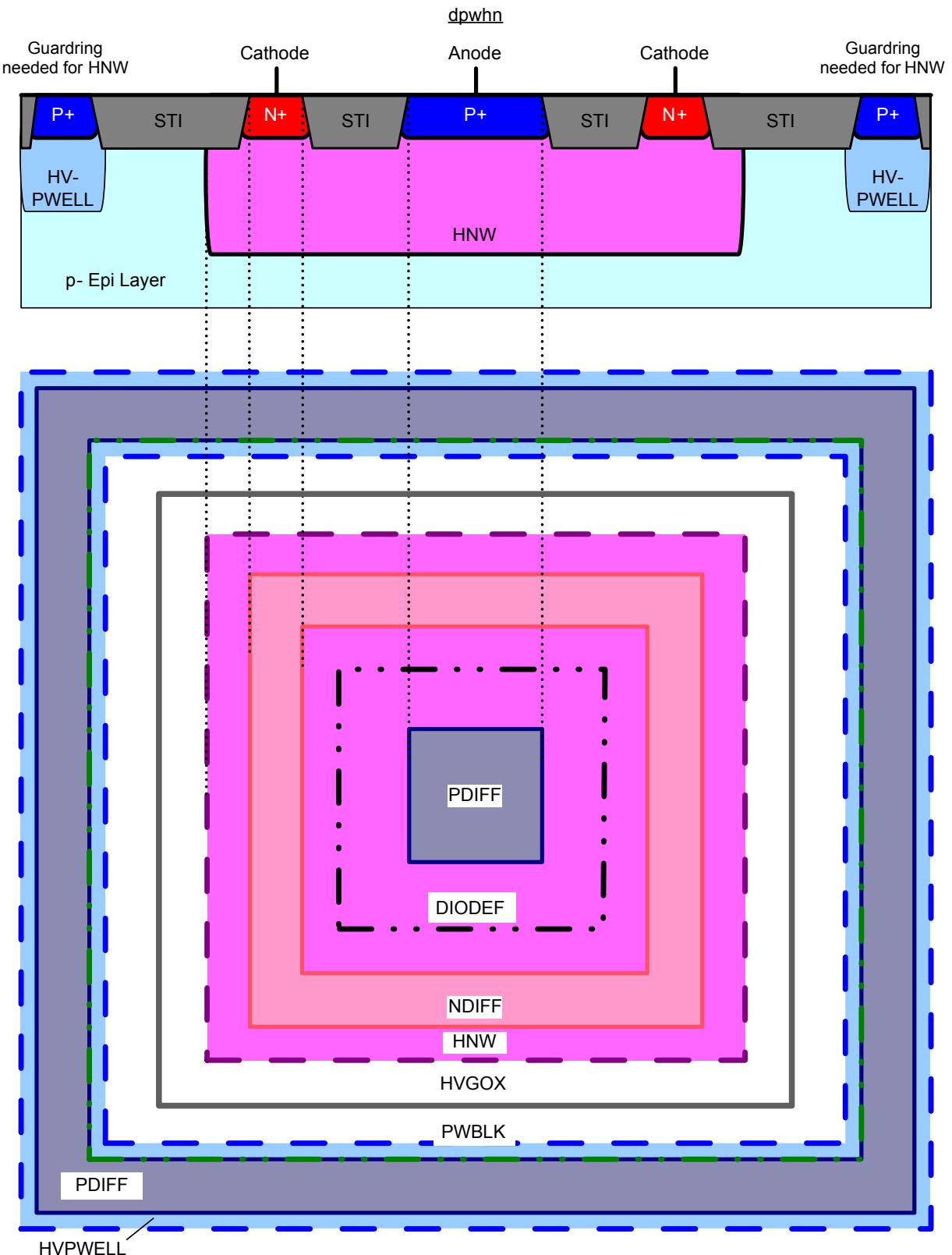


Figure 3.180 dpwhn

3. Layer and Device rules → 3.24 PHVE module

3.24 PHVE module

3.24.1 Layer rules

PDF

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1PD	PDF without HNW is not allowed	-	-
B2PD	NDIFF overlap of PDF is not allowed (except qpvhscr)	-	-
B3PD	PDF overlap of HVNWELL is not allowed	-	-
W1DP	Fixed PDIFF stripe width (except channel region of ph#, pm#)	0.42	µm
W1PD	Minimum PDF width (except phhv, pm#)	5.0	µm
S1PD	Minimum PDF spacing/notch (except channel region of pmmc)	2.2	µm
S2PD	Minimum PDF spacing (different net) (except channel region of phhv, pmmc)	5.0	µm
S1PDDN	Minimum PDF spacing to NDIFF (except qpvhscr)	3.0	µm
S1PDDP	Minimum PDF spacing to PDIFF (except qpvhscr)	4.0	µm
	Note: Valid for PDIFF outside PDF.		
S1PDHN	Minimum PDF spacing to HVNWELL (except channel region of ph#, pm#)	2.76	µm
E1HWPD	Minimum HNW enclosure of PDF	5.0	µm
E1PDDP	Minimum PDF enclosure of PDIFF (except channel region of ph#, pm#, qpvhscr)	3.0	µm

3. Layer and Device rules → 3.24 PHVE module→ 3.24.1 Layer rules→ PDF

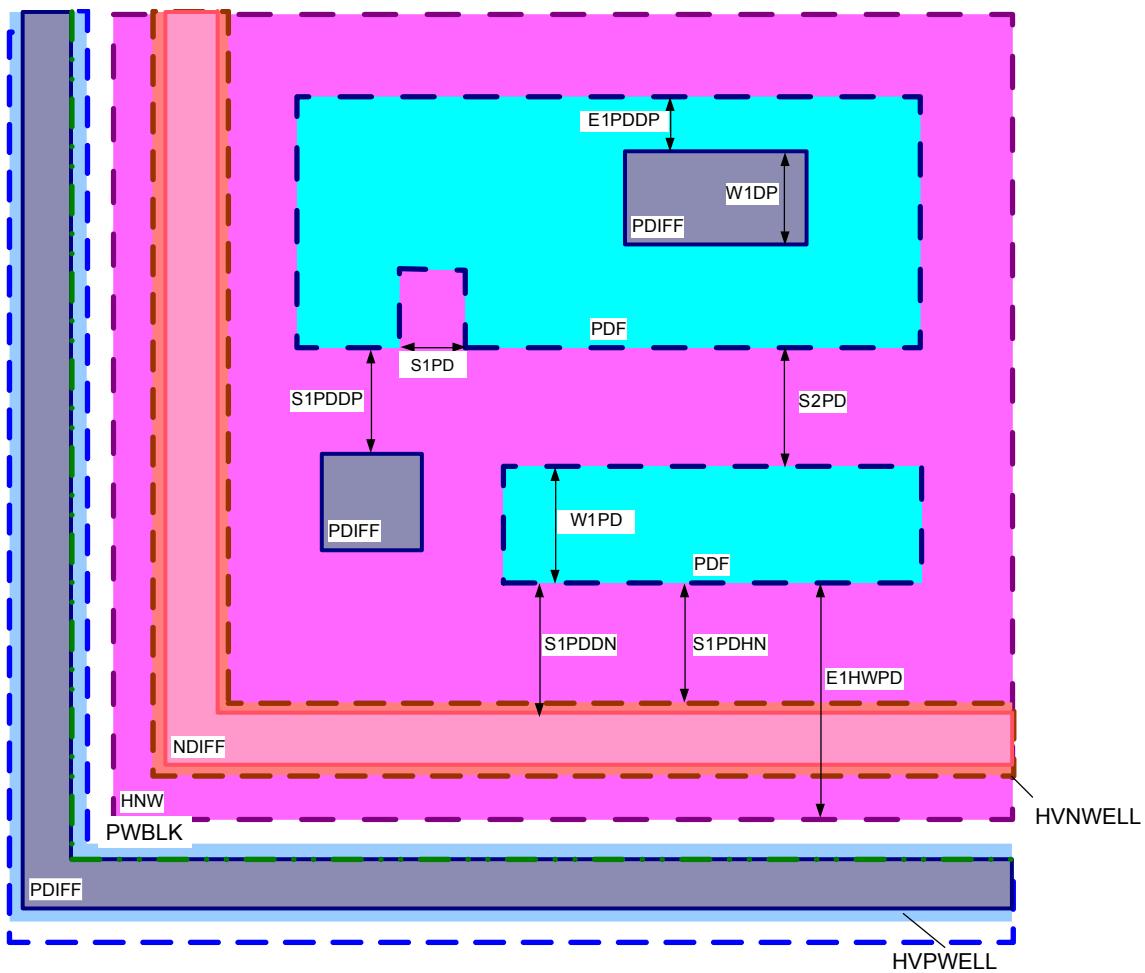


Figure 3.181 PDF

3. Layer and Device rules → 3.24 PHVE module→ 3.24.2 Device rules→ phv, phv_bjt

3.24.2 Device rules

phv, phv_bjt

Name	Description	Value	Unit
W32GA	Minimum GATE length	2.0	µm
W33GA	Minimum GATE width	4.0	µm
S14DF	Fixed DRAIN-EDGE-STI length	2.5	µm
S3PDND	Fixed PDF spacing to NDF (in channel region)	0.0	µm
S5P1DP	Minimum POLY1 spacing to DRAIN PDIFF	1.25	µm
E3P1DP	Minimum POLY1 extension beyond PDIFF	1.25	µm
O2PDGA	Fixed PDF overlap of GATE	0.5	µm

Note: phv and phv_bjt devices must be labeled “phv” using POLY1 (VERIFICATION) layer over the GATE.

Note: The layout of phv and phv_bjt is predefined and scalable concerning device width and length only. The other rules support the fixed dimensions of the layout or describe the relation to adjacent structures.

Note: phv_bjt device must be labeled “bjt” using POLY1 (VERIFICATION) layer over the GATE.

3. Layer and Device rules → 3.24 PHVE module → 3.24.2 Device rules → phv, phv_bjt

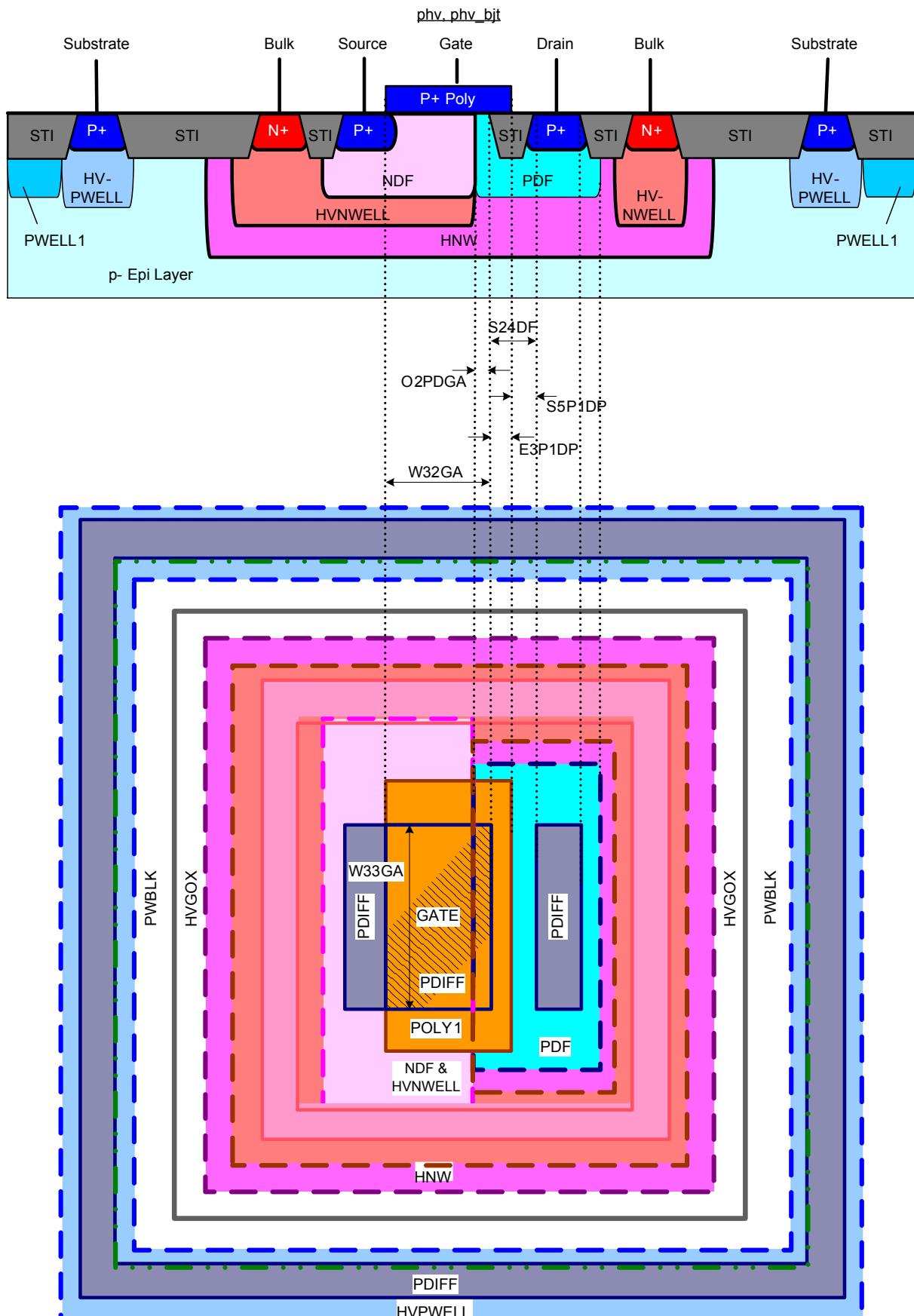


Figure 3.182 phv, phv_bjt

3. Layer and Device rules → 3.24 PHVE module→ 3.24.2 Device rules→ phhv, phhv_bjt

phhv, phhv_bjt

Name	Description	Value	Unit
W18GA	Minimum GATE length	3.5	µm
W19GA	Minimum GATE width	4.0	µm
S4PD	Minimum PDF spacing (in channel region)	2.5	µm
S8DF	Fixed SOURCE/DRAIN-EDGE-STI length	2.5	µm
S3P1DP	Minimum POLY1 spacing to SOURCE / DRAIN PDIFF	1.25	µm
S3PDND	Fixed PDF spacing to NDF (in channel region)	0.0	µm
E4P1GA	Minimum POLY1 extension beyond GATE	1.25	µm
O2PDGA	Fixed PDF overlap of GATE	0.5	µm

Note: phhv and phhv_bjt devices must be labeled “phhv” using POLY1 (VERIFICATION) layer over the GATE.

Note: The layout of phhv and phhv_bjt is predefined and scalable concerning device width and length only. The other rules support the fixed dimensions of the layout or describe the relation to adjacent structures.

Note: phhv_bjt device must be labeled “bjt” using POLY1 (VERIFICATION) layer over the GATE.

3. Layer and Device rules → 3.24 PHVE module→ 3.24.2 Device rules→ phhv, phhv_bjt

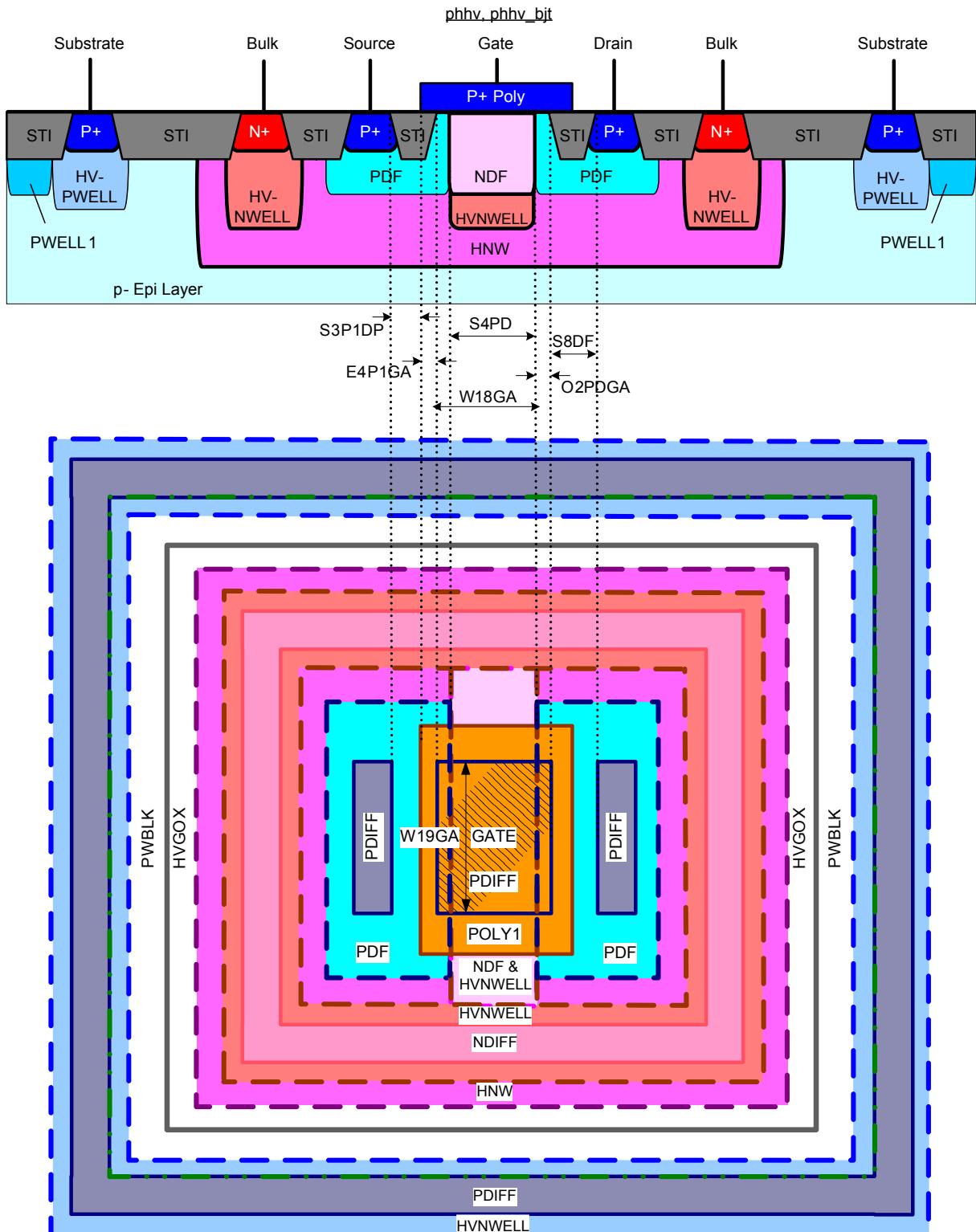


Figure 3.183 phhv, phhv_bjt

3. Layer and Device rules → 3.24 PHVE module→ 3.24.2 Device rules→ pmc, pmc_bjt

pmc, pmc_bjt

Name	Description	Value	Unit
W26GA	Minimum GATE length	1.3	µm
W27GA	Minimum GATE width	3.0	µm
W3PD	Minimum PDF width	3.02	µm
S10DF	Fixed DRAIN-EDGE-STI length	1.0	µm
S2PDND	Fixed PDF spacing to NDF (in channel region)	0.0	µm
S4P1DP	Minimum POLY1 spacing to DRAIN PDIFF	0.5	µm
E3PDDP	Minimum PDF enclosure of PDIFF	1.1	µm
E2P1DP	Minimum POLY1 extension beyond PDIFF	0.5	µm
O3PDGA	Fixed PDF overlap of GATE	0.5	µm

Note: The layout of pmc and pmc_bjt is predefined and scalable concerning device width and length only. The other rules support the fixed dimensions of the layout or describe the relation to adjacent structures.

Note: pmc_bjt device must be labeled “bjt” using POLY1 (VERIFICATION) layer over the GATE.

3. Layer and Device rules → 3.24 PHVE module→ 3.24.2 Device rules→ pmc, pmc_bjt

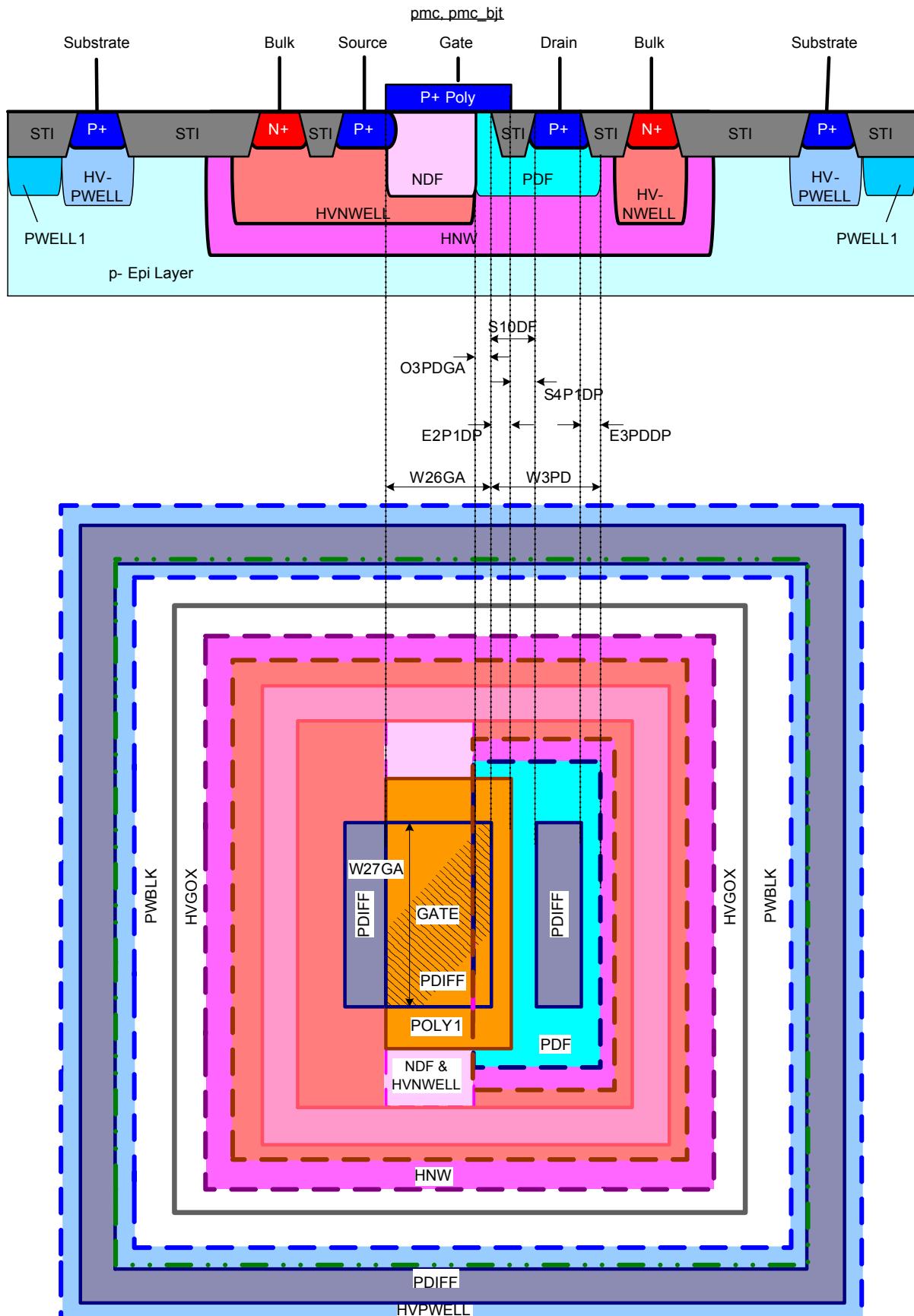


Figure 3.184 pmc, pmc_bjt

3. Layer and Device rules → 3.24 PHVE module→ 3.24.2 Device rules→ pmmc, pmmc_bjt

pmmc, pmmc_bjt

Name	Description	Value	Unit
W14GA	Minimum GATE length	1.8	µm
W15GA	Minimum GATE width	3.0	µm
W2PD	Minimum PDF width	3.02	µm
S11DF	Fixed SOURCE/DRAIN-EDGE-STI length	1.0	µm
S1PDND	Fixed PDF spacing to NDF (in channel region)	0.0	µm
S3PD	Minimum PDF spacing (in channel region)	0.8	µm
S2P1DP	Minimum POLY1 spacing to SOURCE / DRAIN PDIFF	0.5	µm
E2PDDP	Minimum PDF enclosure of PDIFF	1.1	µm
E6P1GA	Minimum POLY1 extension beyond GATE	0.5	µm
O1PDGA	Fixed PDF overlap of GATE	0.5	µm

Note: The layout of pmmc and pmmc_bjt is predefined and scalable concerning device width and length only. The other rules support the fixed dimensions of the layout or describe the relation to adjacent structures.

Note: pmmc_bjt device must be labeled “bjt” using POLY1 (VERIFICATION) layer over the GATE

3. Layer and Device rules → 3.24 PHVE module→ 3.24.2 Device rules→ pmmc, pmmc_bjt

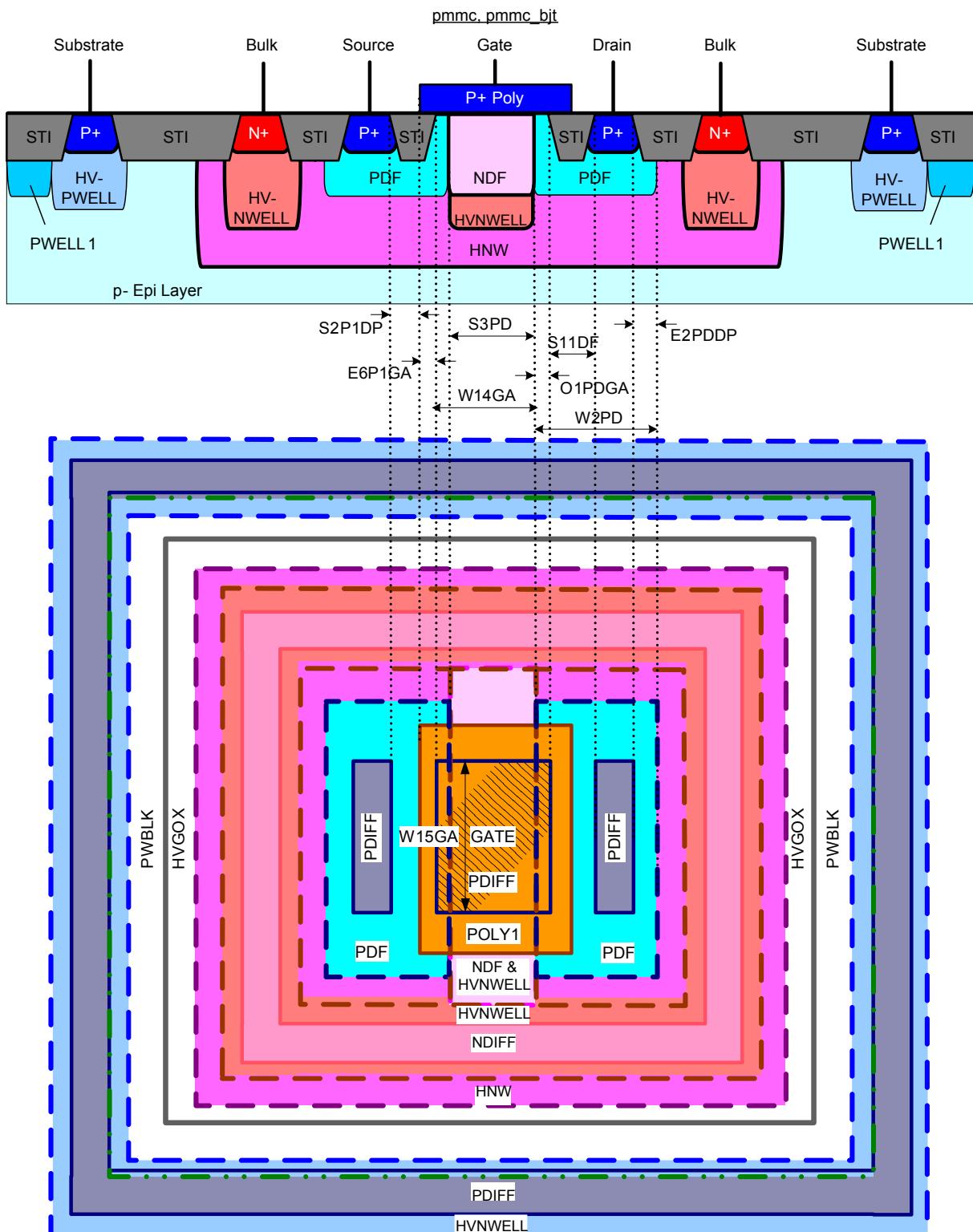


Figure 3.185 pmmc, pmmc_bjt

3. Layer and Device rules → 3.24 PHVE module→ 3.24.2 Device rules→ dpdwhn

dpdwhn

Note: The layer DIODEF must enclose the pn junction, crossing the pn junction is not allowed.

3. Layer and Device rules → 3.24 PHVE module → 3.24.2 Device rules → dpdwhn

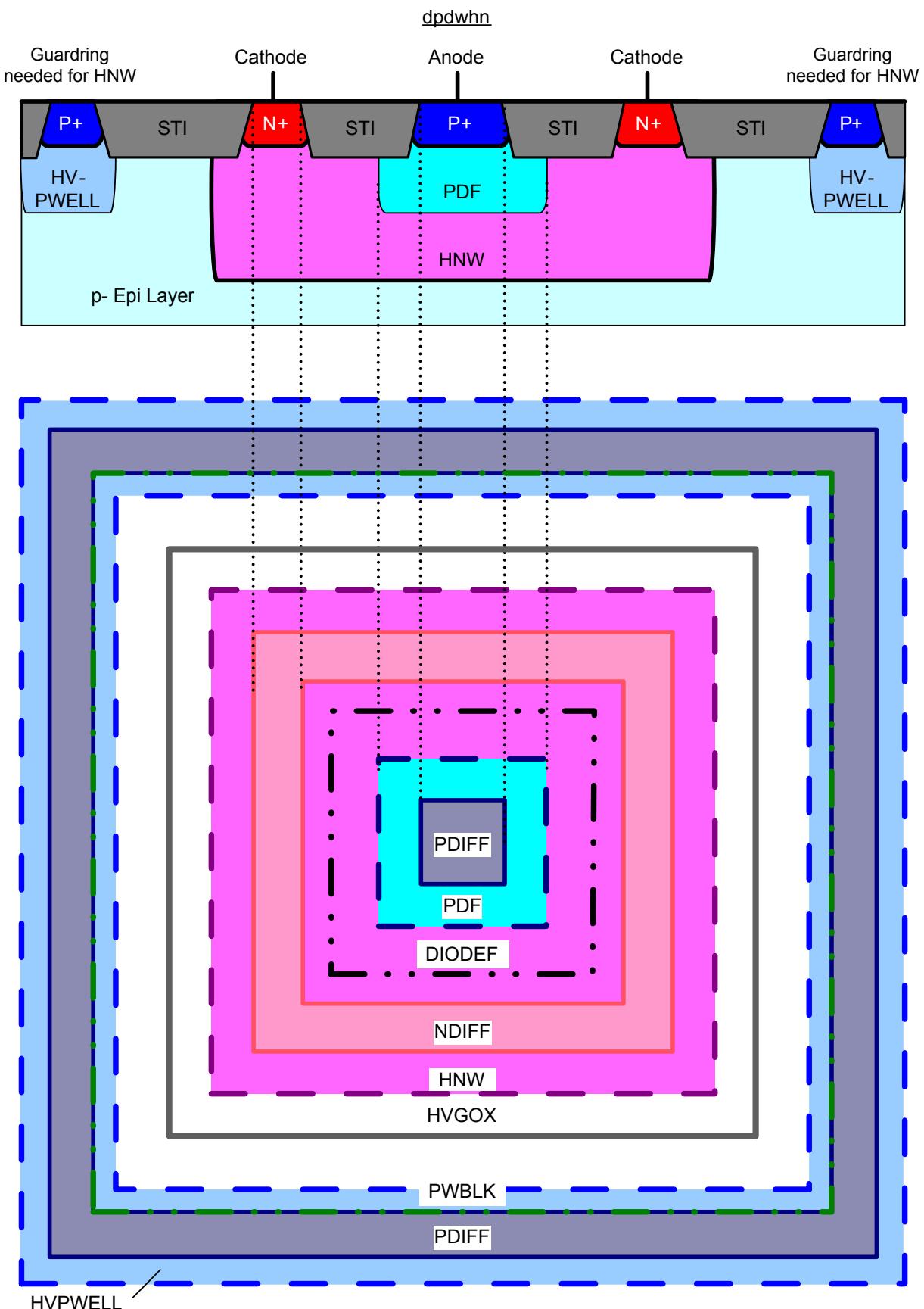


Figure 3.186 dpdwhn

3. Layer and Device rules → 3.25 SCHOTTKY module

3.25 SCHOTTKY module

3.25.1 Layer rules

DNC

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
BDNC	Not allowed to be used by customers Note: Except for predefined devices. Reserved layer.	-	-

3. Layer and Device rules → 3.25 SCHOTTKY module→ 3.25.1 Layer rules→ HNW

HNW

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1HW	HNW without HVGOX and PWBLK is not allowed (except qpvhscr, dsb#)	-	-
B2HW	HNW must be surrounded by a GUARD RING consisting of PDIF and HVPWELL	-	-
B3HW	HNW overlap of DNWELL, DNWELLMV, NWELL, HVPWELL, ISOPW, SCI, DEPL or PDD is not allowed. (except ISOPW and NWELL for qpvhscr, HVPWELL for qpvhbscr)	-	-
B5HW	HNW overlap of rpp1#, rnp1#, rpp1s#, MRES or HRES is not allowed	-	-
B4HW	HVNWELL crossing HNW edge is not allowed	-	-
W1HW	Minimum HNW width	8.0	μm
S1HW	Minimum HNW spacing/notch	10.0	μm
S1HWDN	Minimum HNW spacing to NDIF	4.5	μm
S1HWDP	Fixed HNW spacing to PDIF	4.0	μm
S1HWHN	Minimum HNW spacing to HVNWELL	10.0	μm
S1HWHP	Minimum HNW spacing to HVPWELL	3.76	μm
S1HWND	Minimum HNW spacing to NDF	10.0	μm
S1HWNW	Minimum HNW spacing to NWELL	10.0	μm
S1HWP1	Minimum HNW spacing to POLY1	5.35	μm
S1HWWD	Minimum HNW spacing to DNWELL	10.0	μm
S1HWWM	Minimum HNW spacing to DNWELLMV	10.0	μm
E1GHHW	Minimum HVGOX enclosure of HNW	0.5	μm
E1HWDN	Fixed HNW enclosure of NDIF (except qpvhscr, qpvhbscr, dsb#)	2.0	μm
E1HWDP	Minimum HNW enclosure of PDIF	2.86	μm
E1HWHN	Minimum HNW enclosure of HVNWELL	1.76	μm
E1HWP1	Minimum HNW enclosure of POLY1	2.95	μm
E1PBHW	Fixed PWBLK enclosure of HNW	4.0	μm

3. Layer and Device rules → 3.25 SCHOTTKY module→ 3.25.1 Layer rules→ HNW

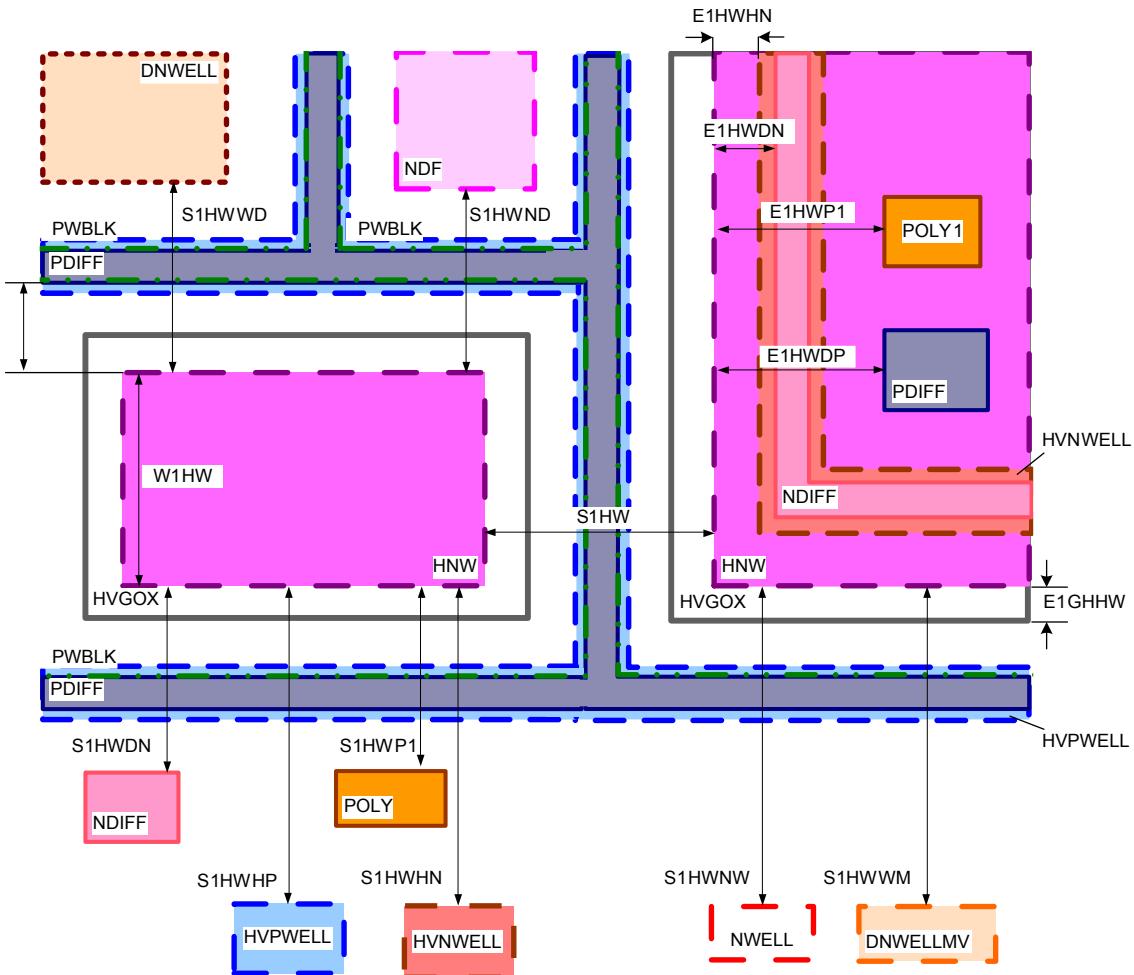


Figure 3.187 HNW

3. Layer and Device rules → 3.25 SCHOTTKY module→ 3.25.1 Layer rules→ HVPWELL

HVPWELL

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1HP	HVPWELL must be contacted by PDIFF	-	-
B3HP	HVPWELL overlap of NWELL is not allowed	-	-
B5HP	HVPWELL overlap of DNWELL is not allowed Note: Valid inside DNWELLMV.	-	-
B2HP	DIFF crossing HVPWELL edge is not allowed (except ped, ned#, nm#, nh#, pmma, nmma)	-	-
B4HP	HVPWELL crossing DNWELL edge is not allowed	-	-
W1HP	Minimum HVPWELL width	0.9	μm
S1HP	Minimum HVPWELL spacing/notch	0.6	μm
S2HP	Minimum HVPWELL spacing (different net) Note: Not valid for channel region of pmma GATE (oversized by 0.43 μm).	3.0	μm
S1HPDN	Minimum HVPWELL spacing to NDIFF (except ned#)	0.43	μm
S1HPDP	Minimum HVPWELL spacing to PDIFF	0.43	μm
S1HPNW	Minimum HVPWELL spacing to NWELL Note: Valid inside DNWELLMV.	0.8	μm
S2HPDN	Fixed HVPWELL spacing to NDIFF (except ned#, ped#, qpvascr) Note: Valid inside DNWELL and NOT DNWELLMV.	3.0	μm
S2HPNW	Minimum HVPWELL spacing to NWELL Note: Valid inside DNWELL and NOT DNWELLMV.	3.0	μm
E1HPDN	Minimum HVPWELL enclosure of NDIFF	0.43	μm
E1HPDP	Minimum HVPWELL enclosure of PDIFF (except ped#, pmma, nmma) Note: Valid inside DNWELLMV/DNWELL.	0.43	μm

3. Layer and Device rules → 3.25 SCHOTTKY module→ 3.25.1 Layer rules→ HVPWELL

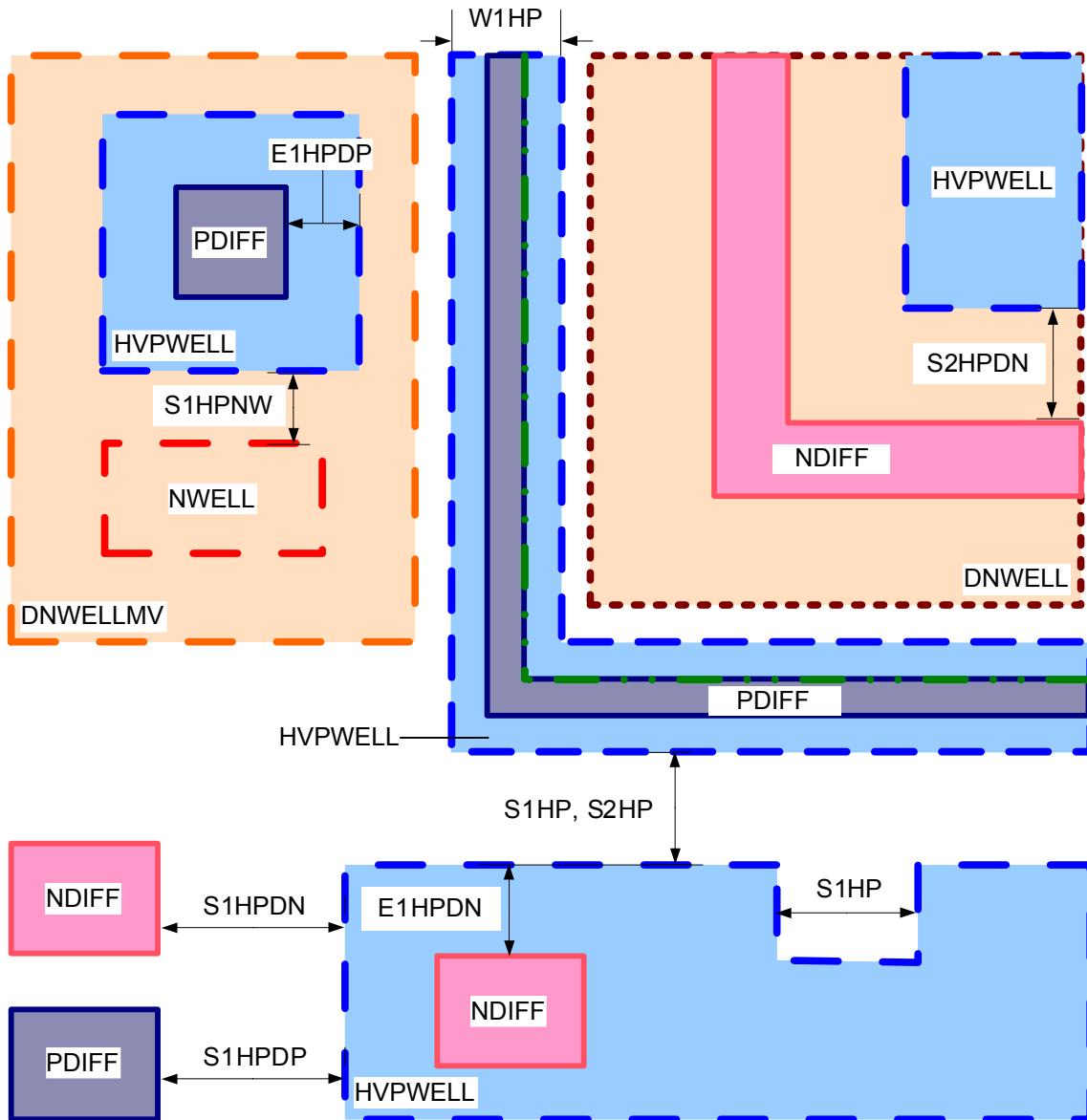


Figure 3.188 HVPWELL

3. Layer and Device rules → 3.25 SCHOTTKY module→ 3.25.2 Device rules→ dsba, dsb

3.25.2 Device rules

dsba, dsb

The layout of the Schottky diodes is pre-defined and only the width can be changed in the range of 2.4 µm up to 50 µm. Fixed length is 0.94 µm.

Name	Description	Value	Unit
B4DF	Check for dsb usage Note: The device dsb is superseded by dsba. It is strongly recommended to use dsba, in particular for diode leakage sensitive designs.	-	-

Note: The drawing is a basic sketch only and does not give all details.

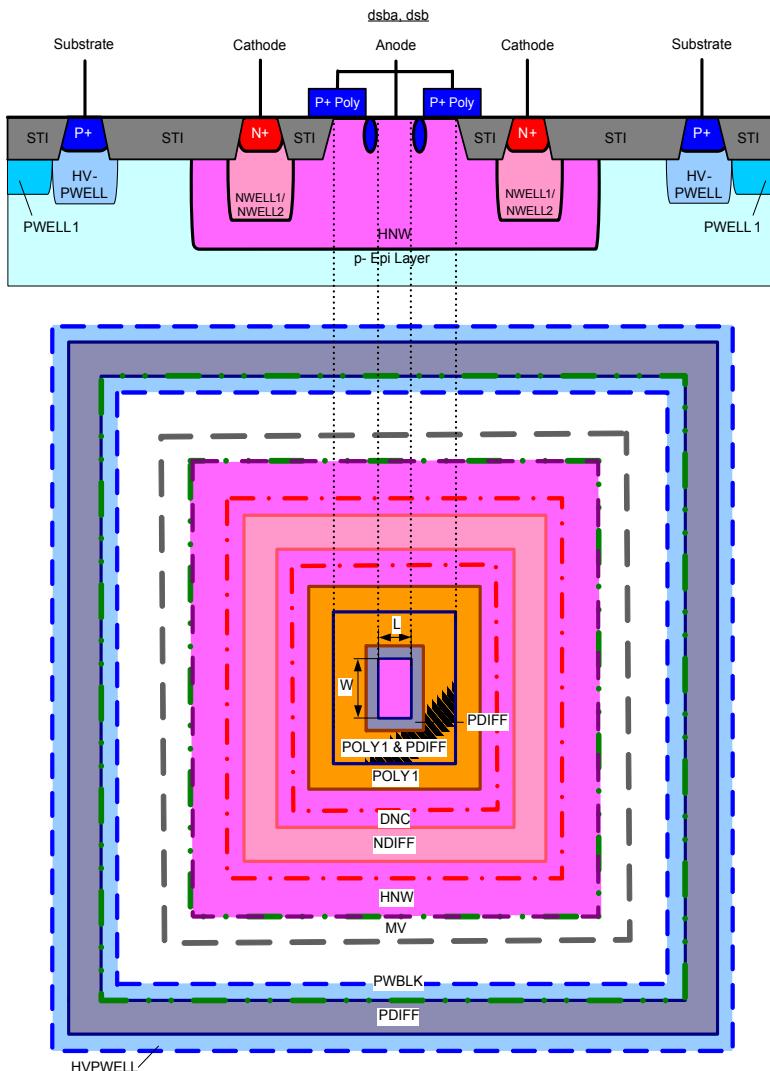


Figure 3.189 dsba, dsb

3. Layer and Device rules → 3.26 MIM module

3.26 MIM module

3.26.1 Layer rules

CAPM

Name	Description	Value	Unit
B1CM	CAPM without BM is not allowed	-	-
B2CM	CAPM overlap of VIA or PAD is not allowed	-	-
B3CM	CAPM is not allowed when CAPM23F, CAPM34F, CAPMH, CAPMH23F, CAPMH34F, CAPM2, CAPMH2, CAPM3 or CAPMH3 is present	-	-
B4CM	CAPM without module METMID is not allowed	-	-
W1CM	Minimum CAPM width	2.0	μm
W2CM	Maximum CAPM bounding box size	30.0 x 30.0	μm x μm
	Note: The bounding box is the generated minimum rectangle enclosing the polygon.		
S1CM	Minimum CAPM spacing/notch	1.5	μm
S3VT	Minimum VIATP spacing on CAPM	2.0	μm
S1CMPA	Minimum CAPM spacing to PAD	10.0	μm
S1CMVN	Minimum CAPM spacing to VIA	0.5	μm
S1CMVT	Minimum CAPM spacing to VIATP	0.5	μm
E1BMCM	Minimum BM enclosure of CAPM	0.5	μm
E1BMVN	Minimum BM enclosure of VIA	0.15	μm
	Note: This rule is related to all VIAs inside CAPM regions extended by 2.5μm.		
E1BMVT	Minimum BM enclosure of VIATP	0.15	μm
	Note: This rule is related to all VIAs inside CAPM regions extended by 2.5μm.		
E1CMVT	Minimum CAPM enclosure of VIATP	0.3	μm
Q1VT	Recommended minimum ratio of VIATP to CAPM area	1.0	%

Note: The Single MIM Capacitor is located between the top metal and the metal layer underneath top metal. The table below shows the assignment of the MIM bottom layer BM and the via layer VIA to the physical metal and via layers for the different metal module options.

Table for BM and VIA assignment

module combination	bottom MIM metal (BM)	device	VIA
LPMOS and not MET4	MET3	cmm4t	VIA2
MET4 and not MET5	MET4	cmm5t	VIA3
MET5	MET5	cmm6t	VIA4

3. Layer and Device rules → 3.26 MIM module→ 3.26.1 Layer rules→ CAPM

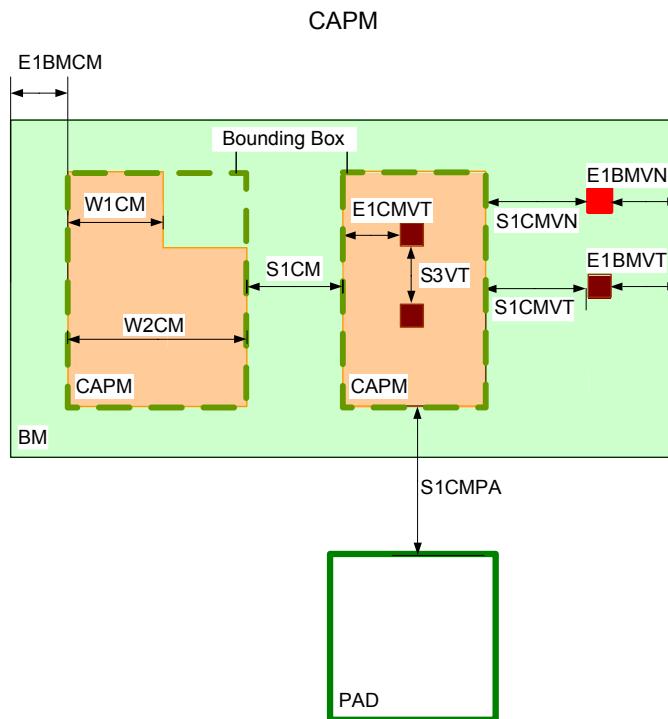


Figure 3.190 CAPM

3. Layer and Device rules → 3.26 MIM module→ 3.26.2 Device rules→ cmm4t, cmm5t, cmm6t

3.26.2 Device rules

cmm4t, cmm5t, cmm6t

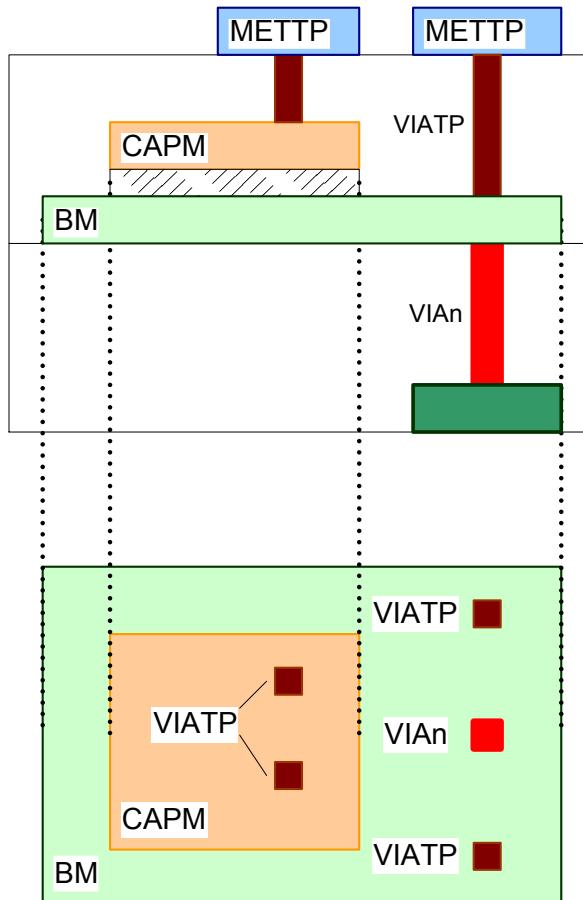


Figure 3.191 cmm4t, cmm5t, cmm6t

3. Layer and Device rules → 3.27 MIM23 module

3.27 MIM23 module

3.27.1 Layer rules

CAPM23F

Name	Description	Value	Unit
B1C3	CAPM23F without MET2 is not allowed	-	-
B2C3	CAPM23F overlap of VIA1 or PAD is not allowed	-	-
B3C3	CAPM23F is not allowed when CAPM, CAPM34F, CAPMH, CAPMH23F, CAPMH34F, CAPM2, CAPMH2, CAPM3 or CAPMH3 is present	-	-
B4C3	CAPM23F without module MET3 is not allowed	-	-
W1C3	Minimum CAPM23F width	2.0	μm
W2C3	Maximum CAPM23F bounding box size	30.0 x 30.0	μm x μm
	Note: The bounding box is the generated minimum rectangle enclosing the polygon.		
S1C3	Minimum CAPM23F spacing/notch	1.5	μm
S5V2	Minimum VIA2 spacing on CAPM23F	2.0	μm
S1C3PA	Minimum CAPM23F spacing to PAD	10.0	μm
S1C3V1	Minimum CAPM23F spacing to VIA1	0.5	μm
S1C3V2	Minimum CAPM23F spacing to VIA2	0.5	μm
E1C3V2	Minimum CAPM23F enclosure of VIA2	0.3	μm
E1M2C3	Minimum MET2 enclosure of CAPM23F	0.5	μm
E5M2V1	Minimum MET2 enclosure of VIA1	0.15	μm
	Note: This rule is related to all VIAs inside CAPM23F regions extended by 2.5μm.		
E6M2V2	Minimum MET2 enclosure of VIA2	0.15	μm
	Note: This rule is related to all VIAs inside CAPM23F regions extended by 2.5μm.		
Q3V2	Recommended minimum ratio of VIA2 to CAPM23F area	1.0	%

3. Layer and Device rules → 3.27 MIM23 module → 3.27.1 Layer rules → CAPM23F

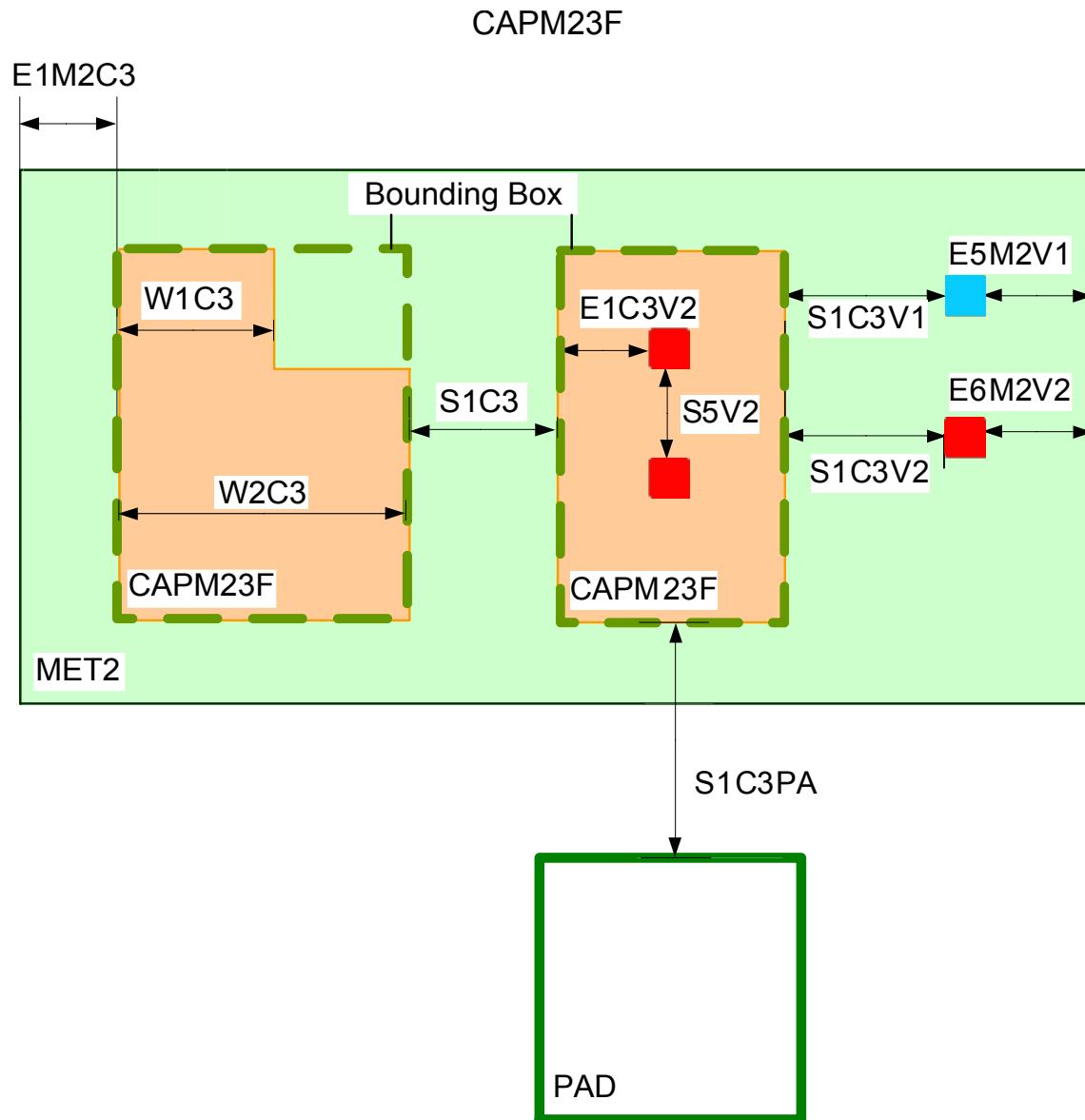


Figure 3.192 CAPM23F

3. Layer and Device rules → 3.27 MIM23 module→ 3.27.2 Device rules→ cmm3

3.27.2 Device rules

cmm3

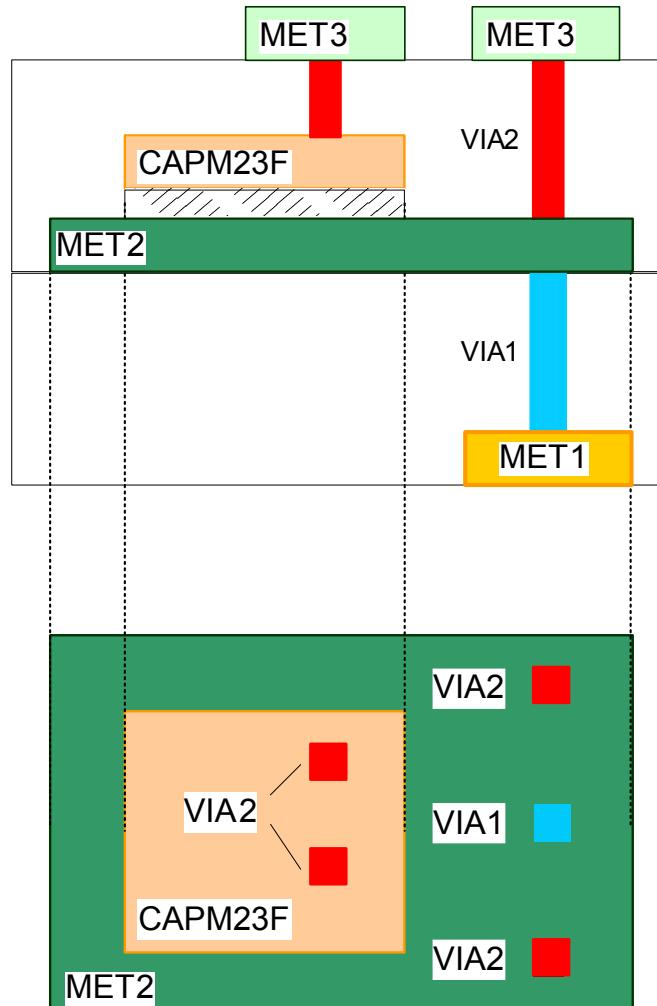


Figure 3.193 cmm3

3. Layer and Device rules → 3.28 MIM34 module

3.28 MIM34 module

3.28.1 Layer rules

CAPM34F

Name	Description	Value	Unit
B1C4	CAPM34F without MET3 is not allowed	-	-
B2C4	CAPM34F overlap of VIA2 or PAD is not allowed	-	-
B3C4	CAPM34F is not allowed when CAPM, CAPM23F, CAPMH, CAPMH23F, CAPMH34F, CAPM2, CAPMH2, CAPM3 or CAPMH3 is present	-	-
B4C4	CAPM34F without module MET4 is not allowed	-	-
W1C4	Minimum CAPM34F width	2.0	μm
W2C4	Maximum CAPM34F bounding box size	30.0 x 30.0	μm x μm
	Note: The bounding box is the generated minimum rectangle enclosing the polygon.		
S1C4	Minimum CAPM34F spacing/notch	1.5	μm
S5V3	Minimum VIA3 spacing on CAPM34F	2.0	μm
S1C4PA	Minimum CAPM34F spacing to PAD	10.0	μm
S1C4V2	Minimum CAPM34F spacing to VIA2	0.5	μm
S1C4V3	Minimum CAPM34F spacing to VIA3	0.5	μm
E1C4V3	Minimum CAPM34F enclosure of VIA3	0.3	μm
E1M3C4	Minimum MET3 enclosure of CAPM34F	0.5	μm
E6M3V2	Minimum MET3 enclosure of VIA2	0.15	μm
	Note: This rule is related to all VIAs inside CAPM34F regions extended by 2.5μm.		
E6M3V3	Minimum MET3 enclosure of VIA3	0.15	μm
	Note: This rule is related to all VIAs inside CAPM34F regions extended by 2.5μm.		
Q3V3	Recommended minimum ratio of VIA3 to CAPM34F area	1.0	%

3. Layer and Device rules → 3.28 MIM34 module → 3.28.1 Layer rules → CAPM34F

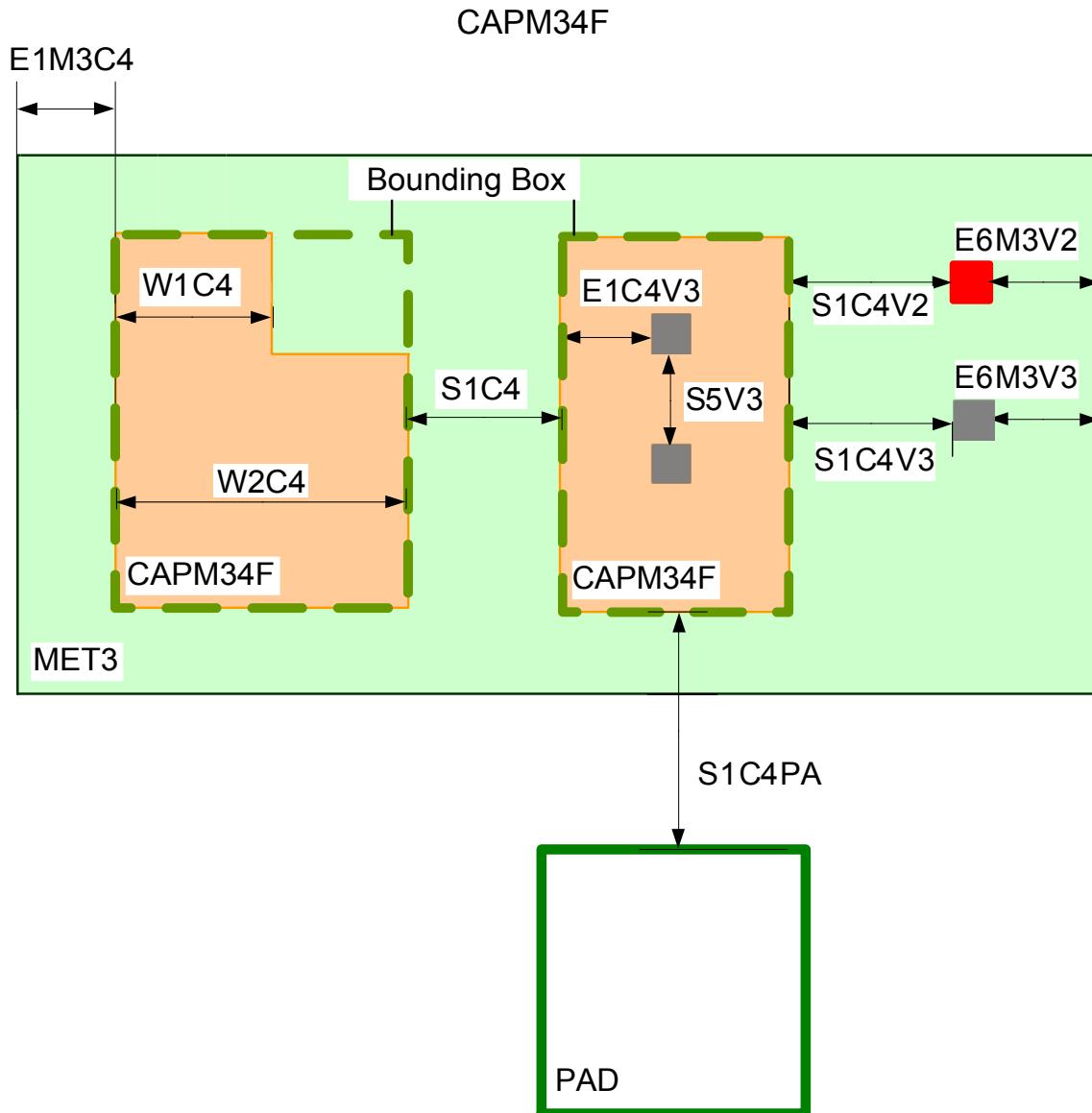


Figure 3.194 CAPM34F

3. Layer and Device rules → 3.28 MIM34 module → 3.28.2 Device rules → cmm4

3.28.2 Device rules

cmm4

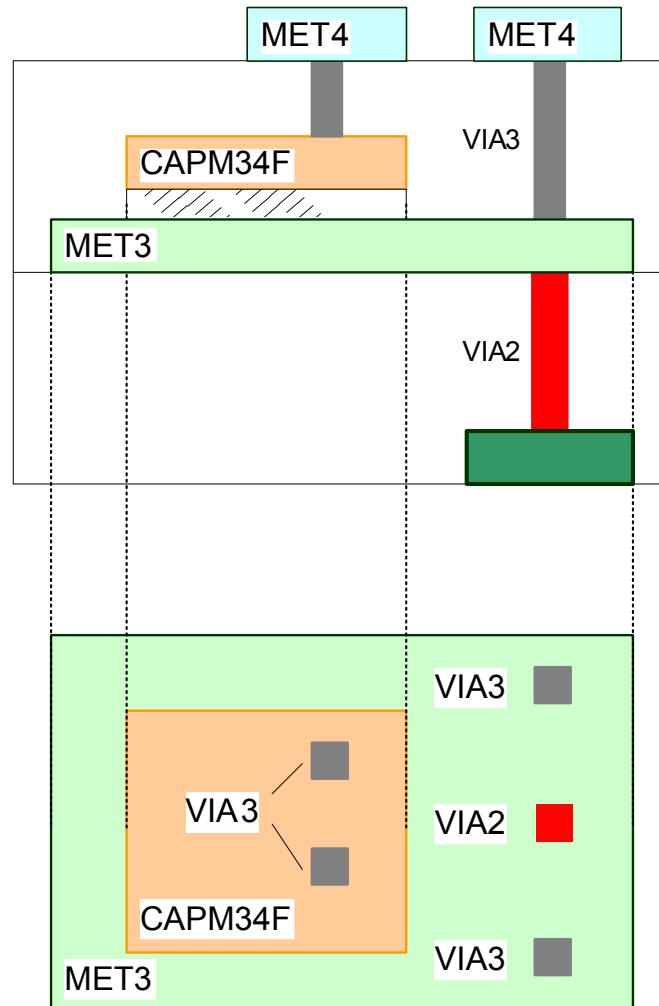


Figure 3.195 cmm4

3. Layer and Device rules → 3.29 DMIM module

3.29 DMIM module

3.29.1 Layer rules

CAPM2

Name	Description	Value	Unit
B10DM	CAPM2 without module MET4 or METMID is not allowed	-	-
B1DM	CAPM2 is not allowed when CAPM, CAPM23F, CAPM34F, CAPMH, CAPMH23F, CAPMH34F, CAPMH2, CAPM3 or CAPMH3 is present	-	-
B2DM	CAPM2 must be enclosed by MET2 and MET3	-	-
B3DM	CAPM2 must not be over VIA1 or PAD	-	-
B4DM	CAPM2 without VIA2 is not allowed	-	-
B5DM	CAPM2 without VIATP is not allowed Note: Valid if MET4 module is not selected.	-	-
B6DM	MET2 and METTP must be connected Note: CAPM2 must be enclosed by METTP. Note: Valid if MET4 module is not selected.	-	-
B7DM	CAPM2 without VIA3 is not allowed Note: Valid if MET4 or MET5 module is selected.	-	-
B8DM	MET2 and MET4 must be connected Note: CAPM2 must be enclosed by MET4. Note: Valid if MET4 or MET5 module is selected.	-	-
B9DM	CAPM2 without module MET3 is not allowed	-	-
W1DM	Minimum CAPM2 width	2.0	µm
W2DM	Maximum CAPM2 bounding box size Note: The bounding box is the generated minimum rectangle enclosing the polygon.	30.0 x 30.0	µm x µm
S1DM	Minimum CAPM2 spacing/notch	1.5	µm
S3V2	Minimum VIA2 spacing on CAPM2	2.0	µm
S3V3	Minimum VIA3 spacing on CAPM2 Note: Valid if MET4 or MET5 module is selected.	2.0	µm
S5VT	Minimum VIATP spacing on CAPM2 Note: Valid if MET4 module is not selected.	2.0	µm
S1DMPA	Minimum CAPM2 spacing to PAD	10.0	µm
S1DMV1	Minimum CAPM2 spacing to VIA1	0.5	µm
S1DMV2	Minimum CAPM2 spacing to VIA2	0.5	µm
S1DMV3	Minimum CAPM2 spacing to VIA3 Note: Valid if MET4 or MET5 module is selected.	0.5	µm
S1DMVT	Minimum CAPM2 spacing to VIATP Note: Valid if MET4 module is not selected.	0.5	µm
E1DMV2	Minimum CAPM2 enclosure of VIA2	0.3	µm
E1DMV3	Minimum CAPM2 enclosure of VIA3 Note: Valid if MET4 or MET5 module is selected.	0.3	µm
E1DMVT	Minimum CAPM2 enclosure of VIATP Note: Valid if MET4 module is not selected.	0.3	µm
E1M2DM	Minimum MET2 enclosure of CAPM2	0.5	µm
E1M3DM	Minimum MET3 enclosure of CAPM2	0.5	µm

3. Layer and Device rules → 3.29 DMIM module→ 3.29.1 Layer rules→ CAPM2

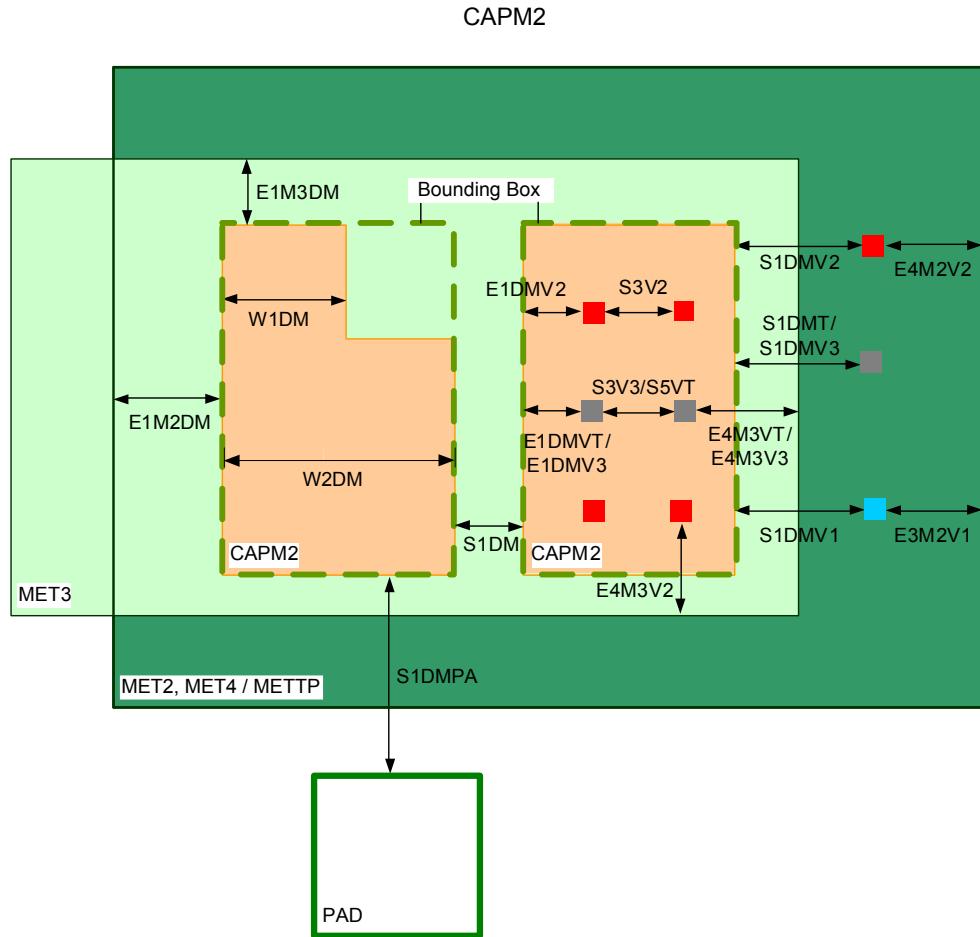
Name	Description	Value	Unit
E3M2V1	Minimum MET2 enclosure of VIA1 Note: This rule is related to all VIAs inside CAPM2 and CAPMH2 regions extended by 2.5µm.	0.15	µm
E4M2V2	Minimum MET2 enclosure of VIA2 Note: This rule is related to all VIAs inside CAPM2 and CAPMH2 regions extended by 2.5µm.	0.15	µm
E4M3V2	Minimum MET3 enclosure of VIA2 Note: This rule is related to all VIAs inside CAPM2 and CAPMH2 regions extended by 2.5µm.	0.15	µm
E4M3V3	Minimum MET3 enclosure of VIA3 Note: Valid if MET4 or MET5 module is selected. Note: This rule is related to all VIAs inside CAPM2 and CAPMH2 regions extended by 2.5µm.	0.15	µm
E4M3VT	Minimum MET3 enclosure of VIATP Note: Valid if MET4 module is not selected. Note: This rule is related to all VIAs inside CAPM2 and CAPMH2 regions extended by 2.5µm.	0.15	µm
Q1V2	Recommended minimum ratio of VIA2 to CAPM2 area	1.0	%
Q1V3	Recommended minimum ratio of VIA3 to CAPM2 area Note: Valid if MET4 or MET5 module is selected.	1.0	%
Q2VT	Recommended minimum ratio of VIATP to CAPM2 area Note: Valid if MET4 module is not selected.	1.0	%

Note: The placement of DMIM must start from MET2 as described in the Table for DMIM Construction below.

Table for DMIM Construction

module combination	structure of metal stacking	device	Top MIM metal
LPMOS	MET2 / CAPM2 / MET3 / CAPM2 / METTP	cdmm4t	METTP
MET4, MET5	MET2 / CAPM2 / MET3 / CAPM2 / MET4	cdmm4	MET4

3. Layer and Device rules → 3.29 DMIM module → 3.29.1 Layer rules → CAPM2

**Figure 3.196** CAPM2

3. Layer and Device rules → 3.29 DMIM module → 3.29.2 Device rules → cdmm4, cdmm4t

3.29.2 Device rules

cdmm4, cdmm4t

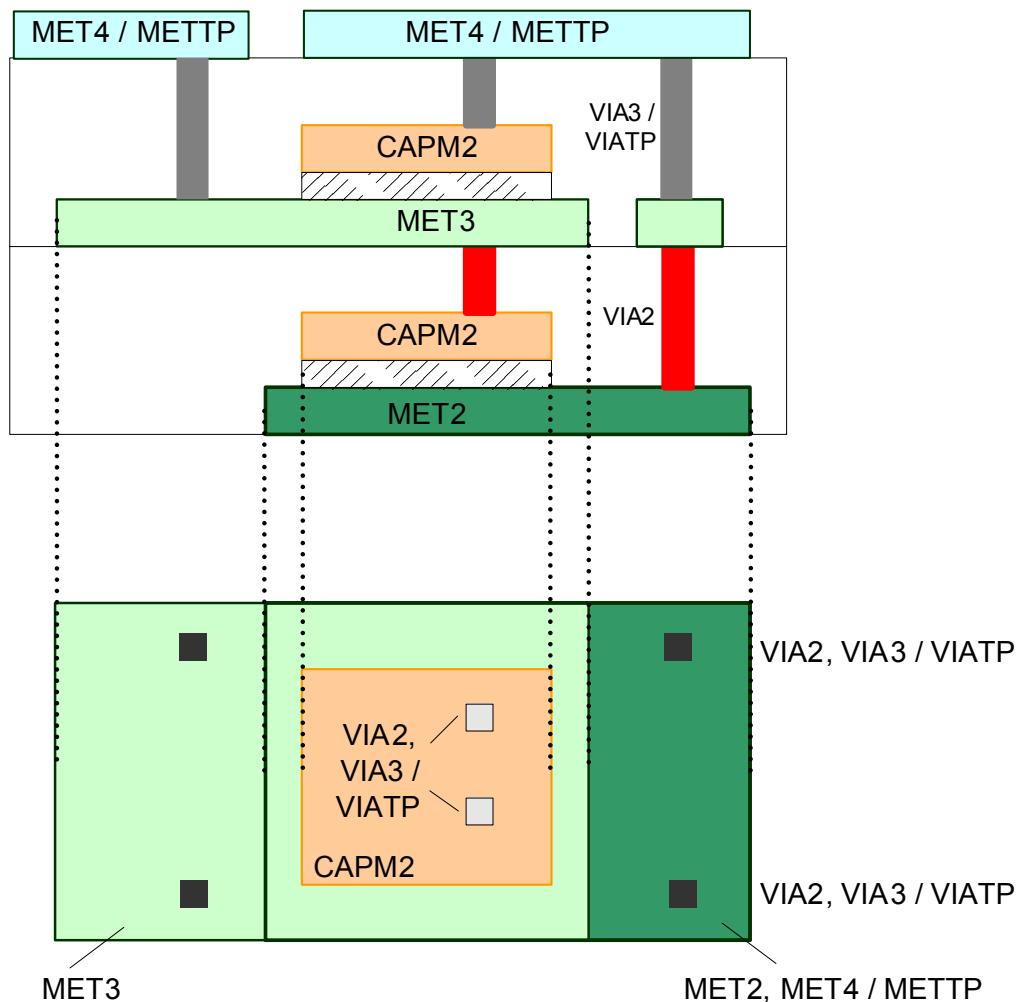


Figure 3.197 cdmm4t, cdmm4

3. Layer and Device rules → 3.30 TMIM module

3.30 TMIM module

3.30.1 Layer rules

CAPM3

Name	Description	Value	Unit
B10TM	CAPM3 without module MET4 is not allowed	-	-
B1TM	CAPM3 is not allowed when CAPM, CAPM23F, CAPM34F, CAPMH, CAPMH23F, CAPMH34F, CAPM2, CAPMH2 or CAPMH3 is present	-	-
B2TM	CAPM3 must be enclosed by MET2, MET3 and MET4	-	-
B3TM	CAPM3 must not be over VIA1 or PAD	-	-
B4TM	CAPM3 without VIA2 or VIA3 is not allowed	-	-
B5TM	MET2 and MET4 must be connected	-	-
B6TM	CAPM3 without VIATP is not allowed	-	-
	Note: Valid if MET4 module is selected and MET5 module is not selected.		
B7TM	MET3 and METTP must be connected	-	-
	Note: CAPM3 must be enclosed by METTP.		
	Note: Valid if MET4 module is selected and MET5 module is not selected.		
B8TM	CAPM3 without VIA4 is not allowed	-	-
	Note: Valid if MET5 module is selected.		
B9TM	MET3 and MET5 must be connected	-	-
	Note: Valid if MET5 module is selected.		
	Note: CAPM3 must be enclosed by MET5.		
W1TM	Minimum CAPM3 width	2.0	µm
W2TM	Maximum CAPM3 bounding box size	30.0 x 30.0	µm x µm
	Note: The bounding box is the generated minimum rectangle enclosing the polygon.		
S1TM	Minimum CAPM3 spacing/notch	1.5	µm
S3V4	Minimum VIA4 spacing on CAPM3	2.0	µm
	Note: Valid if MET5 module is selected.		
S4V2	Minimum VIA2 spacing on CAPM3	2.0	µm
S4V3	Minimum VIA3 spacing on CAPM3	2.0	µm
S6VT	Minimum VIATP spacing on CAPM3	2.0	µm
	Note: Valid if MET4 module is selected and MET5 module is not selected.		
S1TMPA	Minimum CAPM3 spacing to PAD	10.0	µm
S1TMV1	Minimum CAPM3 spacing to VIA1	0.5	µm
S1TMV2	Minimum CAPM3 spacing to VIA2	0.5	µm
S1TMV3	Minimum CAPM3 spacing to VIA3	0.5	µm
S1TMV4	Minimum CAPM3 spacing to VIA4	0.5	µm
	Note: Valid if MET5 module is selected.		
S1TMVT	Minimum CAPM3 spacing to VIATP	0.5	µm
	Note: Valid if MET4 module is selected and MET5 module is not selected.		
E1M2TM	Minimum MET2 enclosure of CAPM3	0.5	µm
E1M3TM	Minimum MET3 enclosure of CAPM3	0.5	µm
E1M4TM	Minimum MET4 enclosure of CAPM3	0.5	µm
E1TMV2	Minimum CAPM3 enclosure of VIA2	0.3	µm
E1TMV3	Minimum CAPM3 enclosure of VIA3	0.3	µm

3. Layer and Device rules → 3.30 TMIM module→ 3.30.1 Layer rules→ CAPM3

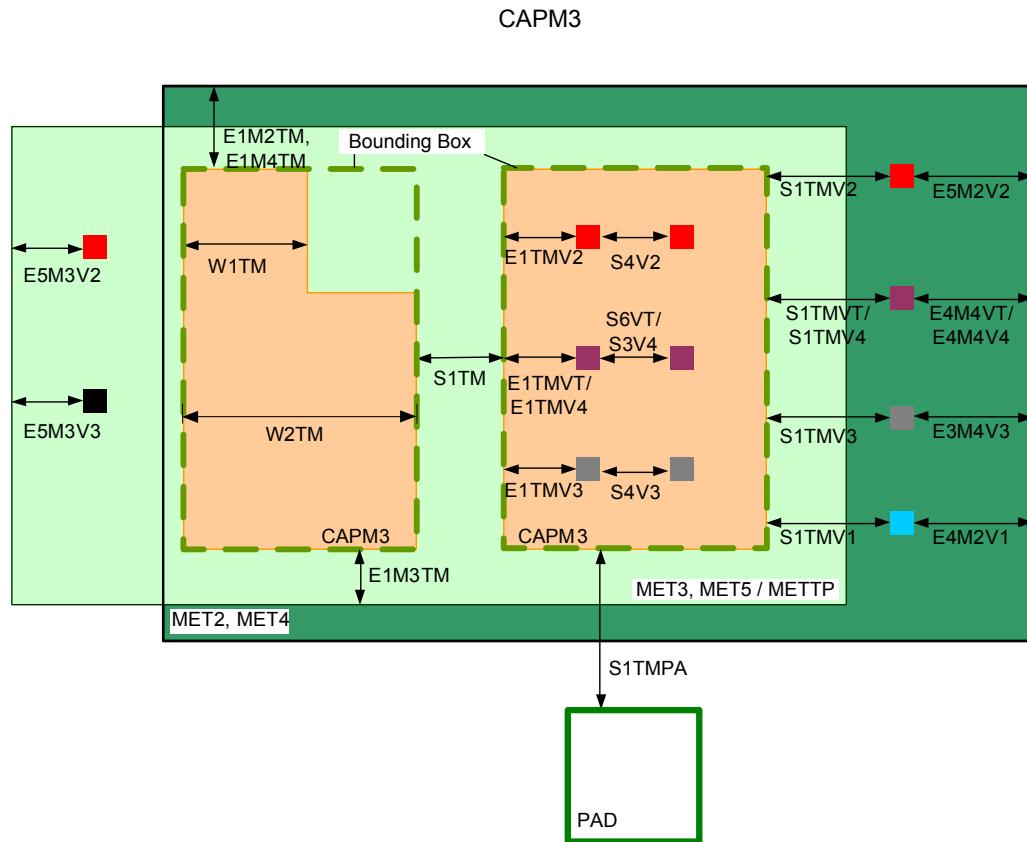
Name	Description	Value	Unit
E1TMV4	Minimum CAPM3 enclosure of VIA4 Note: Valid if MET5 module is selected.	0.3	µm
E1TMVT	Minimum CAPM3 enclosure of VIATP Note: Valid if MET4 module is selected and MET5 module is not selected.	0.3	µm
E3M4V3	Minimum MET4 enclosure of VIA3 Note: This rule is related to all VIAs inside CAPM3 and CAPMH3 regions extended by 2.5 µm.	0.15	µm
E4M2V1	Minimum MET2 enclosure of VIA1 Note: This rule is related to all VIAs inside CAPM3 and CAPMH3 regions extended by 2.5 µm.	0.15	µm
E4M4V4	Minimum MET4 enclosure of VIA4 Note: Valid if MET5 module is selected. Note: This rule is related to all VIAs inside CAPM3 and CAPMH3 regions extended by 2.5 µm.	0.15	µm
E4M4VT	Minimum MET4 enclosure of VIATP Note: This rule is related to all VIAs inside CAPM3 and CAPMH3 regions extended by 2.5 µm. Note: Valid if MET4 module is selected and MET5 module is not selected.	0.15	µm
E5M2V2	Minimum MET2 enclosure of VIA2 Note: This rule is related to all VIAs inside CAPM3 and CAPMH3 regions extended by 2.5 µm.	0.15	µm
E5M3V2	Minimum MET3 enclosure of VIA2 Note: This rule is related to all VIAs inside CAPM3 and CAPMH3 regions extended by 2.5 µm.	0.15	µm
E5M3V3	Minimum MET3 enclosure of VIA3 Note: This rule is related to all VIAs inside CAPM3 and CAPMH3 regions extended by 2.5 µm.	0.15	µm
Q1V4	Recommended minimum ratio of VIA4 to CAPM3 area Note: Valid if MET5 module is selected.	1.0	%
Q2V2	Recommended minimum ratio of VIA2 to CAPM3 area	1.0	%
Q2V3	Recommended minimum ratio of VIA3 to CAPM3 area	1.0	%
Q3VT	Recommended minimum ratio of VIATP to CAPM3 area Note: Valid if MET4 module is selected and MET5 module is not selected.	1.0	%

Note: The placement of TMIM must start from MET2 as described in the Table for TMIM Construction.

Table for TMIM Construction

module combination	structure of metal stacking	device	Top MIM metal
LPMOS	n/a	n/a	n/a
MET4	MET2 / CAPM3 / MET3 / CAPM3 / MET4 / CAPM3 / METTP	ctmm5t	METTP
MET5	MET2 / CAPM3 / MET3 / CAPM3 / MET4 / CAPM3 / MET5 / METTP	ctmm5	MET5

3. Layer and Device rules → 3.30 TMIM module→ 3.30.1 Layer rules→ CAPM3

**Figure 3.198** CAPM3

3. Layer and Device rules → 3.30 TMIM module→ 3.30.2 Device rules→ ctmm5, ctmm5t

3.30.2 Device rules

ctmm5, ctmm5t

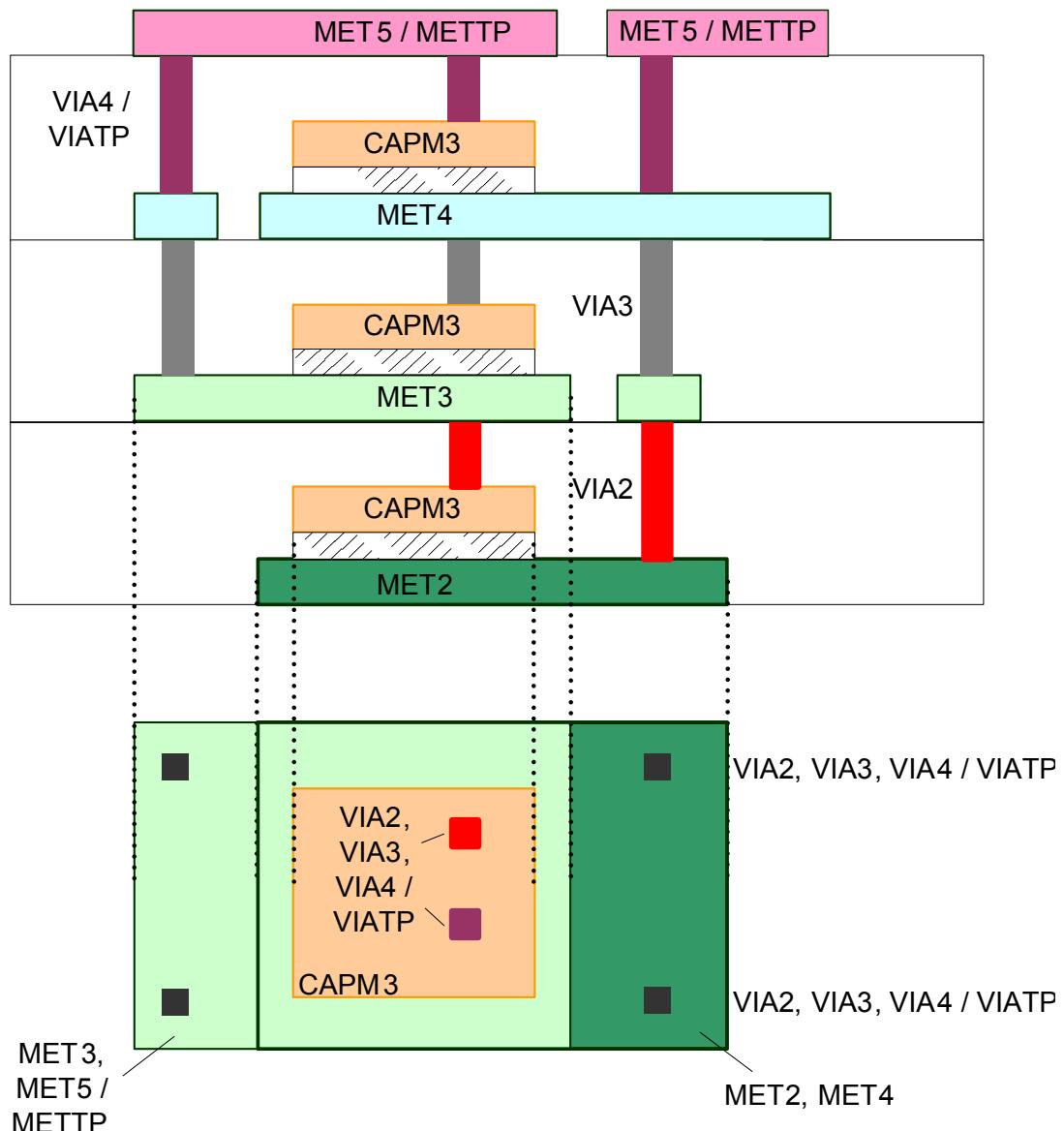


Figure 3.199 ctmm5t, ctmm5

3. Layer and Device rules → 3.31 MIMH module

3.31 MIMH module

3.31.1 Layer rules

CAPMH

Name	Description	Value	Unit
B1CH	CAPMH without BM is not allowed	-	-
B2CH	CAPMH overlap of VIA _n or PAD is not allowed	-	-
B3CH	CAPMH is not allowed when CAPM, CAPM23F, CAPM34F, CAPMH23F, CAPMH34F, CAPM2, CAPMH2, CAPM3 or CAPMH3 is present	-	-
B4CH	CAPMH without module METMID is not allowed	-	-
W1CH	Minimum CAPMH width	2.0	μm
W2CH	Maximum CAPMH bounding box size	30.0 x 30.0	μm x μm
	Note: The bounding box is the generated minimum rectangle enclosing the polygon.		
S1CH	Minimum CAPMH spacing/notch	1.5	μm
S4VT	Minimum VIATP spacing on CAPMH	2.0	μm
S1CHPA	Minimum CAPMH spacing to PAD	10.0	μm
S1CHVN	Minimum CAPMH spacing to VIA _n	0.5	μm
S1CHVT	Minimum CAPMH spacing to VIATP	0.5	μm
E1BMCH	Minimum BM enclosure of CAPMH	0.5	μm
E1CHVT	Minimum CAPMH enclosure of VIATP	0.3	μm
E2BMVN	Minimum BM enclosure of VIA _n	0.15	μm
	Note: This rule is related to all VIAs inside CAPMH regions extended by 2.5μm.		
E2BMVT	Minimum BM enclosure of VIATP	0.15	μm
	Note: This rule is related to all VIAs inside CAPMH regions extended by 2.5μm.		
Q4VT	Recommended minimum ratio of VIATP to CAPMH area	1.0	%

Note: The Single High Capacitance MIM Capacitor is located between the top metal and the metal layer underneath top metal. The table below shows the assignment of the MIMH bottom layer BM and the via layer VIA_n to the physical metal and via layers for the different metal module options.

Table for BM and VIA_n assignment

module combination	bottom MIM metal (BM)	device	VIA _n
LPMOS and not MET4	MET3	cmmh4t	VIA2
MET4 and not MET5	MET4	cmmh5t	VIA3
MET5	MET5	cmmh6t	VIA4

3. Layer and Device rules → 3.31 MIMH module→ 3.31.1 Layer rules→ CAPMH

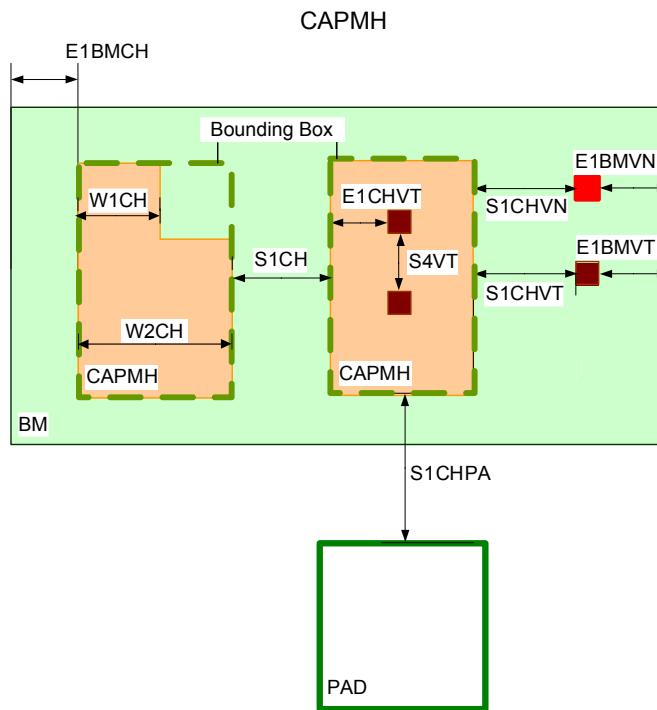


Figure 3.200 CAPMH

3. Layer and Device rules → 3.31 MIMH module → 3.31.2 Device rules → cmmh4t, cmmh5t, cmmh...

3.31.2 Device rules

cmmh4t, cmmh5t, cmmh6t

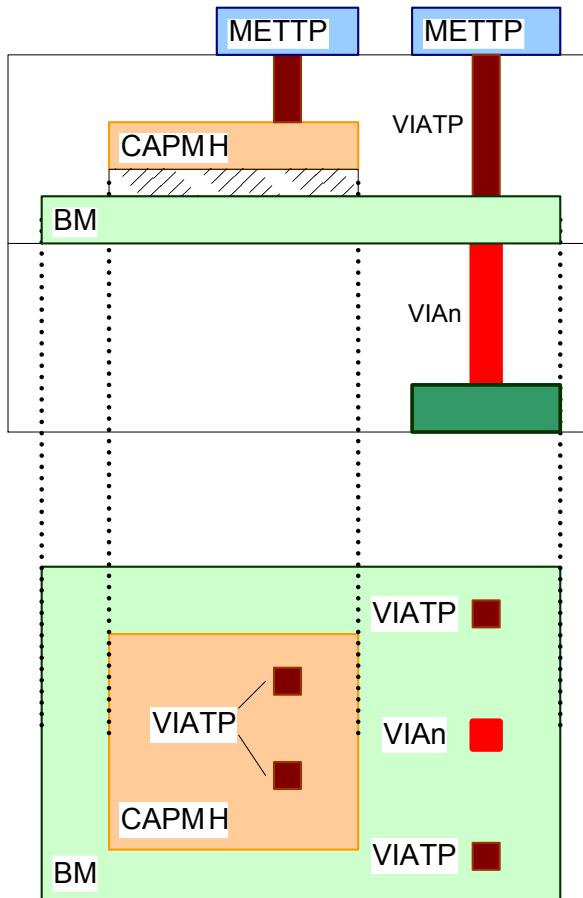


Figure 3.201 cmmh4t, cmmh5t, cmmh6t

3. Layer and Device rules → 3.32 MIMH23 module

3.32 MIMH23 module

3.32.1 Layer rules

CAPMH23F

Name	Description	Value	Unit
B1H3	CAPMH23F without MET2 is not allowed	-	-
B2H3	CAPMH23F overlap of VIA1 or PAD is not allowed	-	-
B3H3	CAPMH23F is not allowed when CAPM, CAPM23F, CAPM34F, CAPMH, CAPMH34F, CAPM2, CAPMH2, CAPM3 or CAPMH3 is present	-	-
B4H3	CAPMH23F without module MET3 is not allowed	-	-
W1H3	Minimum CAPMH23F width	2.0	μm
W2H3	Maximum CAPMH23F bounding box size	30.0 x 30.0	μm x μm
	Note: The bounding box is the generated minimum rectangle enclosing the polygon.		
S1H3	Minimum CAPMH23F spacing/notch	1.5	μm
S1H3PA	Minimum CAPMH23F spacing to PAD	10.0	μm
S1H3V1	Minimum CAPMH23F spacing to VIA1	0.5	μm
S1H3V2	Minimum CAPMH23F spacing to VIA2	0.5	μm
S6V2	Minimum VIA2 spacing on CAPMH23F	2.0	μm
E1H3V2	Minimum CAPMH23F enclosure of VIA2	0.3	μm
E1M2H3	Minimum MET2 enclosure of CAPMH23F	0.5	μm
E6M2V1	Minimum MET2 enclosure of VIA1	0.15	μm
	Note: This rule is related to all VIAs inside CAPMH23F regions extended by 2.5μm.		
E7M2V2	Minimum MET2 enclosure of VIA2	0.15	μm
	Note: This rule is related to all VIAs inside CAPMH23F regions extended by 2.5μm.		
Q4V2	Recommended minimum ratio of VIA2 to CAPMH23F area	1.0	%

3. Layer and Device rules → 3.32 MIMH23 module → 3.32.1 Layer rules → CAPMH23F

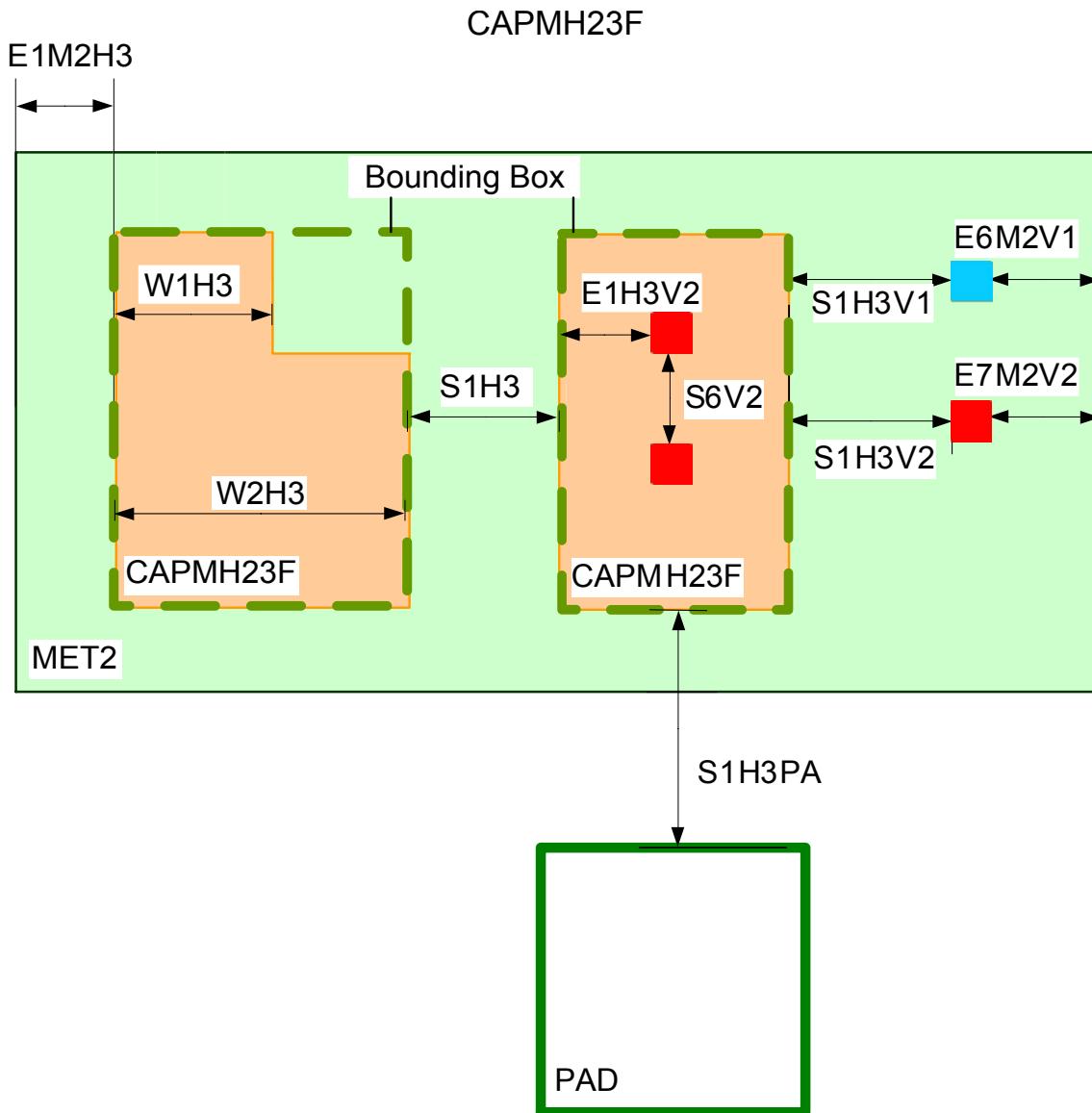


Figure 3.202 CAPMH23F

3. Layer and Device rules → 3.32 MIMH23 module → 3.32.2 Device rules → cmmh3

3.32.2 Device rules

cmmh3

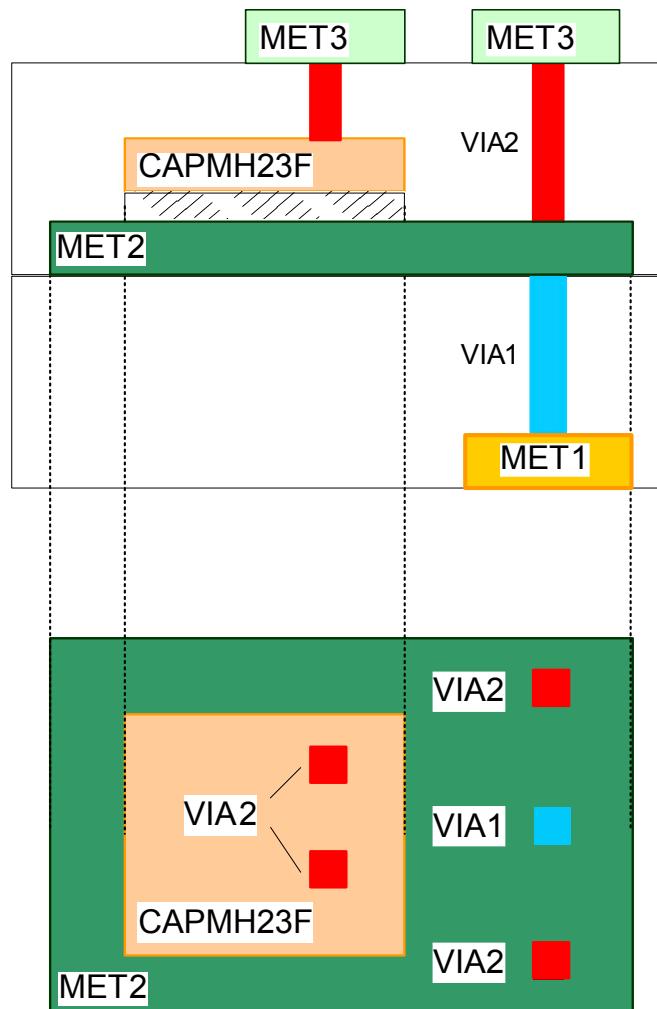


Figure 3.203 cmmh3

3. Layer and Device rules → 3.33 MIMH34 module

3.33 MIMH34 module

3.33.1 Layer rules

CAPMH34F

Name	Description	Value	Unit
B1H4	CAPMH34F without MET3 is not allowed	-	-
B2H4	CAPMH34F overlap of VIA2 or PAD is not allowed	-	-
B3H4	CAPMH34F is not allowed when CAPM, CAPM23F, CAPM34F, CAPMH, CAPMH23F, CAPM2, CAPMH2, CAPM3 or CAPMH3 is present	-	-
B4H4	CAPMH34F without module MET4 is not allowed	-	-
W1H4	Minimum CAPMH34F width	2.0	μm
W2H4	Maximum CAPMH34F bounding box size	30.0 x 30.0	μm x μm
	Note: The bounding box is the generated minimum rectangle enclosing the polygon.		
S1H4	Minimum CAPMH34F spacing/notch	1.5	μm
S6V3	Minimum VIA3 spacing on CAPMH34F	2.0	μm
S1H4PA	Minimum CAPMH34F spacing to PAD	10.0	μm
S1H4V2	Minimum CAPMH34F spacing to VIA2	0.5	μm
S1H4V3	Minimum CAPMH34F spacing to VIA3	0.5	μm
E1H4V3	Minimum CAPMH34F enclosure of VIA3	0.3	μm
E1M3H4	Minimum MET3 enclosure of CAPMH34F	0.5	μm
E7M3V2	Minimum MET3 enclosure of VIA2	0.15	μm
	Note: This rule is related to all VIAs inside CAPMH34F regions extended by 2.5μm.		
E7M3V3	Minimum MET3 enclosure of VIA3	0.15	μm
	Note: This rule is related to all VIAs inside CAPMH34F regions extended by 2.5μm.		
Q4V3	Recommended minimum ratio of VIA3 to CAPMH34F area	1.0	%

3. Layer and Device rules → 3.33 MIMH34 module → 3.33.1 Layer rules → CAPMH34F

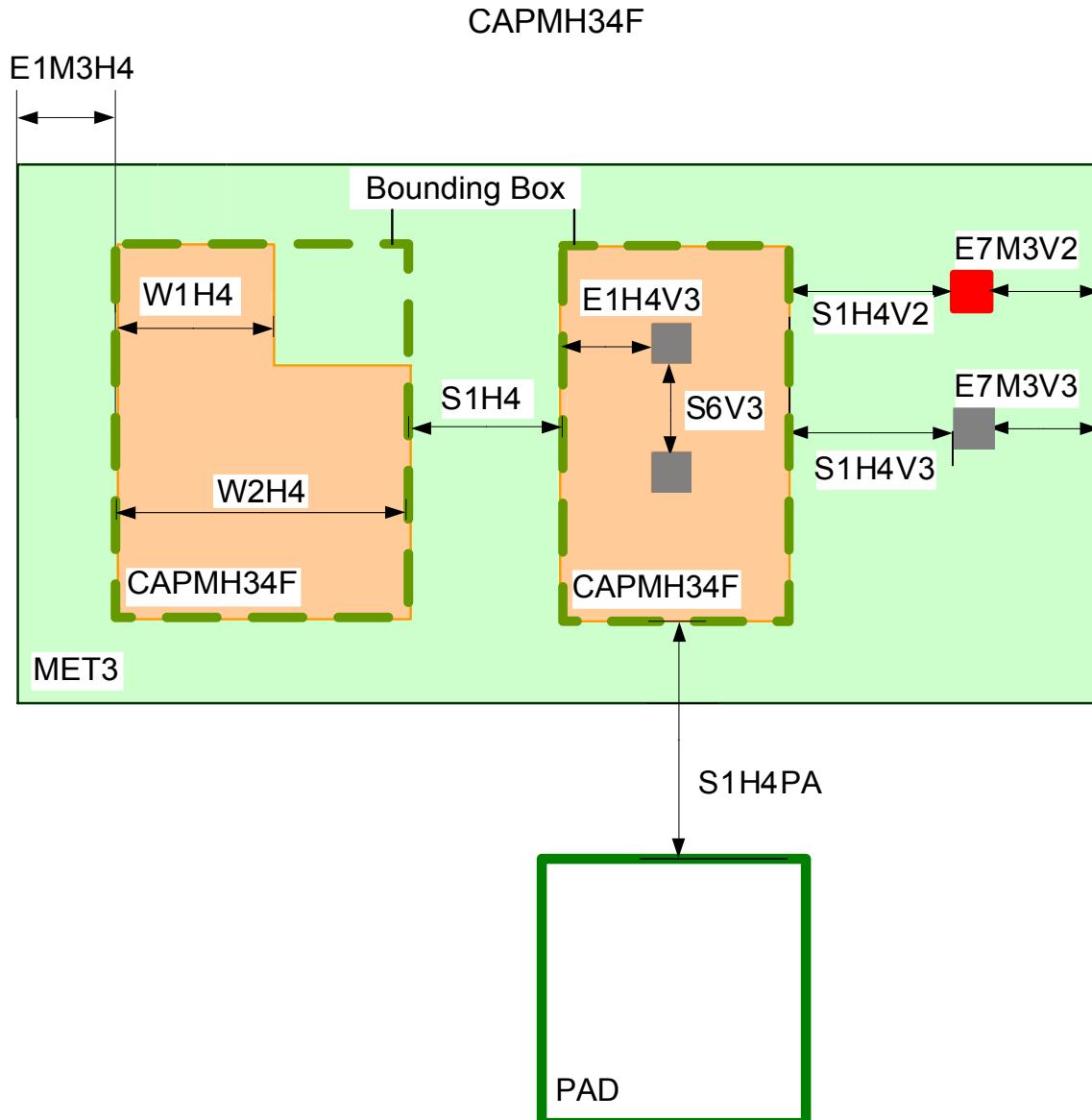


Figure 3.204 CAPMH34F

3. Layer and Device rules → 3.33 MIMH34 module → 3.33.2 Device rules → cmmh4

3.33.2 Device rules

cmmh4

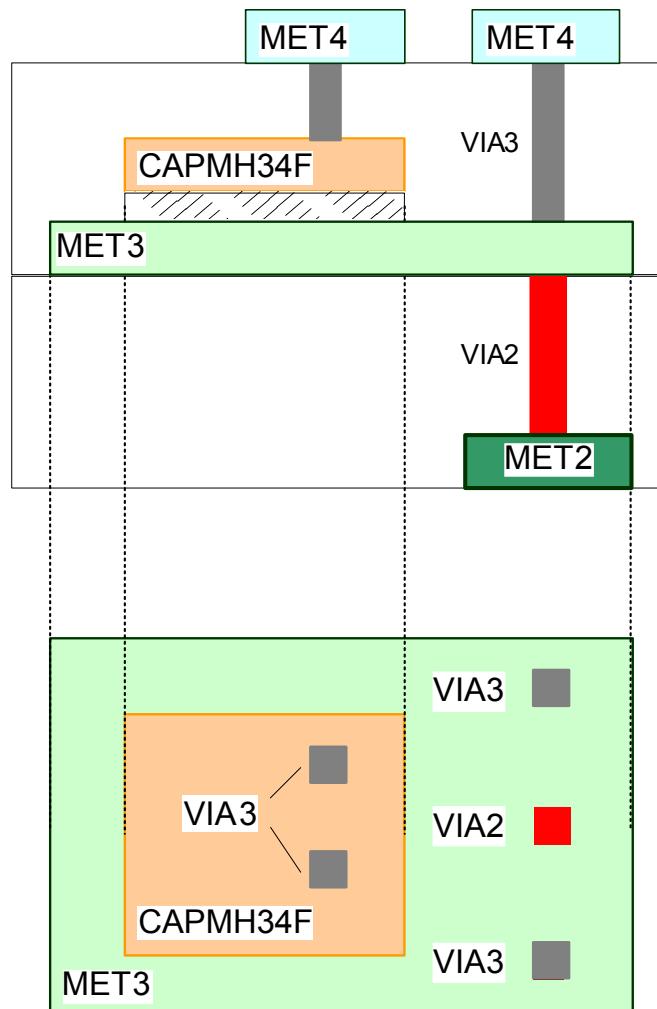


Figure 3.205 cmmh4

3. Layer and Device rules → 3.34 DMIMH module

3.34 DMIMH module

3.34.1 Layer rules

CAPMH2

Name	Description	Value	Unit
B10DH	CAPMH2 without module MET4 or METMID is not allowed	-	-
B1DH	CAPMH2 is not allowed when CAPM, CAPM23F, CAPM34F, CAPMH, CAPMH23F, CAPMH34F, CAPM2, CAPM3 or CAPMH3 is present	-	-
B2DH	CAPMH2 must be enclosed by MET2 and MET3	-	-
B3DH	CAPMH2 must not be over VIA1 or PAD	-	-
B4DH	CAPMH2 without VIA2 is not allowed	-	-
B5DH	CAPMH2 without VIATP is not allowed Note: Valid if MET4 module is not selected.	-	-
B6DH	MET2 and METTP must be connected Note: CAPMH2 must be enclosed by METTP. Note: Valid if MET4 module is not selected.	-	-
B7DH	CAPMH2 without VIA3 is not allowed Note: Valid if MET4 or MET5 module is selected.	-	-
B8DH	MET2 and MET4 must be connected Note: CAPMH2 must be enclosed by MET4. Note: Valid if MET4 or MET5 module is selected.	-	-
B9DH	CAPMH2 without module MET3 is not allowed	-	-
W1DH	Minimum CAPMH2 width	2.0	µm
W2DH	Maximum CAPMH2 bounding box size Note: The bounding box is the generated minimum rectangle enclosing the polygon.	30.0 x 30.0	µm x µm
S1DH	Minimum CAPMH2 spacing/notch	1.5	µm
S7V2	Minimum VIA2 spacing on CAPMH2	2.0	µm
S7V3	Minimum VIA3 spacing on CAPMH2 Note: Valid if MET4 or MET5 module is selected.	2.0	µm
S7VT	Minimum VIATP spacing on CAPMH2 Note: Valid if MET4 module is not selected.	2.0	µm
S1DHPA	Minimum CAPMH2 spacing to PAD	10.0	µm
S1DHV1	Minimum CAPMH2 spacing to VIA1	0.5	µm
S1DHV2	Minimum CAPMH2 spacing to VIA2	0.5	µm
S1DHV3	Minimum CAPMH2 spacing to VIA3 Note: Valid if MET4 or MET5 module is selected.	0.5	µm
S1DHVT	Minimum CAPMH2 spacing to VIATP Note: Valid if MET4 module is not selected.	0.5	µm
E1DHV2	Minimum CAPMH2 enclosure of VIA2	0.3	µm
E1DHV3	Minimum CAPMH2 enclosure of VIA3 Note: Valid if MET4 or MET5 module is selected.	0.3	µm
E1DHVT	Minimum CAPMH2 enclosure of VIATP Note: Valid if MET4 module is not selected.	0.3	µm
E1M2DH	Minimum MET2 enclosure of CAPMH2	0.5	µm
E1M3DH	Minimum MET3 enclosure of CAPMH2	0.5	µm

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3. Layer and Device rules → 3.34 DMIMH module→ 3.34.1 Layer rules→ CAPMH2

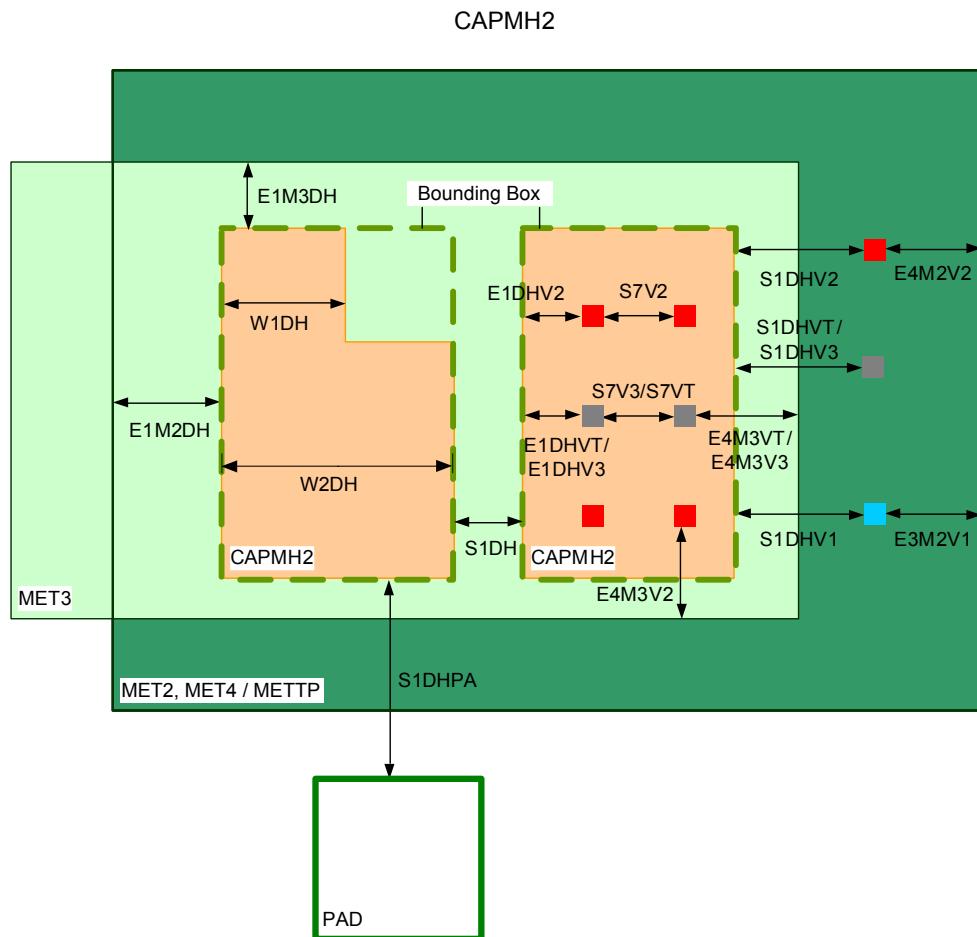
Name	Description	Value	Unit
E3M2V1	Minimum MET2 enclosure of VIA1 Note: This rule is related to all VIAs inside CAPM2 and CAPMH2 regions extended by 2.5µm.	0.15	µm
E4M2V2	Minimum MET2 enclosure of VIA2 Note: This rule is related to all VIAs inside CAPM2 and CAPMH2 regions extended by 2.5µm.	0.15	µm
E4M3V2	Minimum MET3 enclosure of VIA2 Note: This rule is related to all VIAs inside CAPM2 and CAPMH2 regions extended by 2.5µm.	0.15	µm
E4M3V3	Minimum MET3 enclosure of VIA3 Note: Valid if MET4 or MET5 module is selected. Note: This rule is related to all VIAs inside CAPM2 and CAPMH2 regions extended by 2.5µm.	0.15	µm
E4M3VT	Minimum MET3 enclosure of VIATP Note: Valid if MET4 module is not selected. Note: This rule is related to all VIAs inside CAPM2 and CAPMH2 regions extended by 2.5µm.	0.15	µm
Q5V2	Recommended minimum ratio of VIA2 to CAPMH2 area	1.0	%
Q5V3	Recommended minimum ratio of VIA3 to CAPMH2 area Note: Valid if MET4 or MET5 module is selected.	1.0	%
Q5VT	Recommended minimum ratio of VIATP to CAPMH2 area Note: Valid if MET4 module is not selected.	1.0	%

Note: The placement of DMIMH must start from MET2 as described in the Table for DMIMH Construction below.

Table for DMIMH Construction

module combination	structure of metal stacking	device	Top MIM metal
LPMOS	MET2 / CAPMH2 / MET3 / CAPMH2 / METTP	cdmmh4t	METTP
MET4, MET5	MET2 / CAPMH2 / MET3 / CAPMH2 / MET4	cdmmh4	MET4

3. Layer and Device rules → 3.34 DMIMH module → 3.34.1 Layer rules → CAPMH2

**Figure 3.206** CAPMH2

3. Layer and Device rules → 3.34 DMIMH module → 3.34.2 Device rules → cdmmh4, cdmmh4t

3.34.2 Device rules

cdmmh4, cdmmh4t

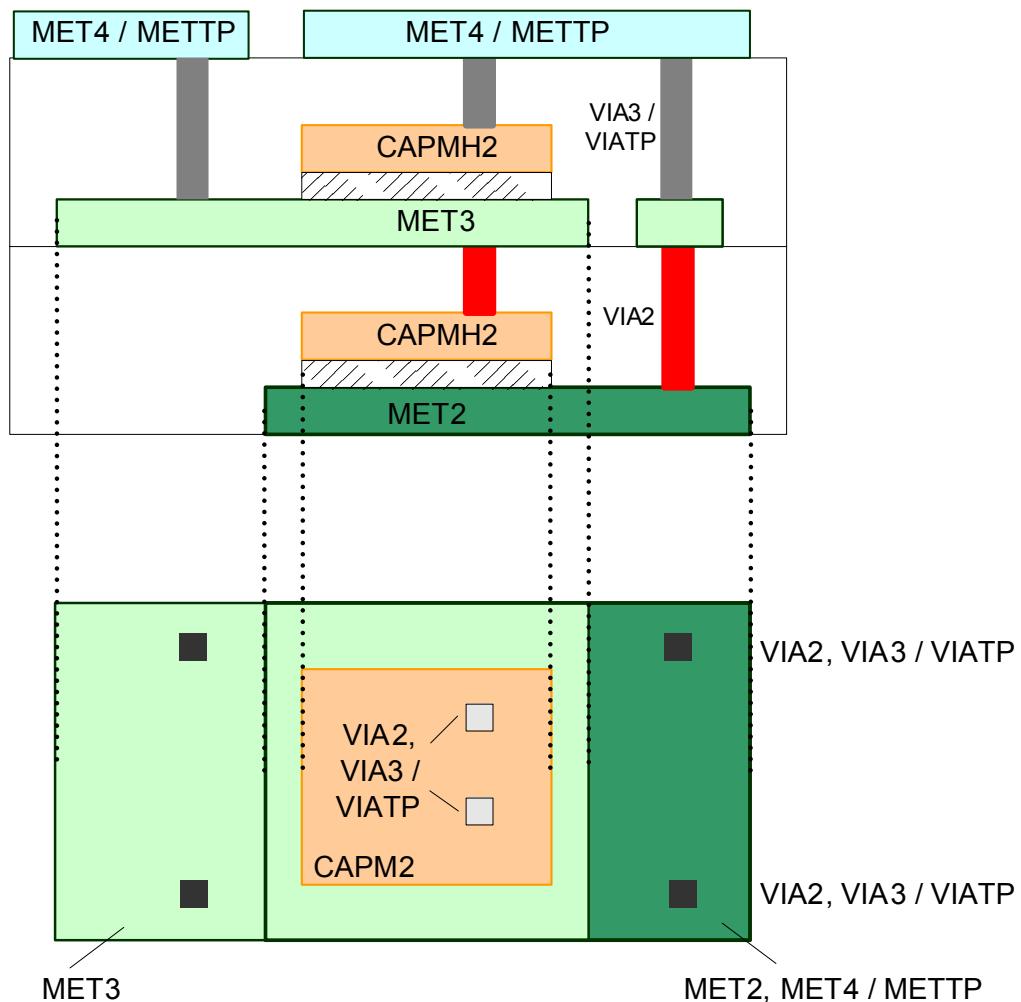


Figure 3.207 cdmmh4t, cdmmh4

3. Layer and Device rules → 3.35 TMIMH module

3.35 TMIMH module

3.35.1 Layer rules

CAPMH3

Name	Description	Value	Unit
B10TH	CAPMH3 without module MET4 is not allowed	-	-
B1TH	CAPMH3 is not allowed when CAPM, CAPM23F, CAPM34F, CAPMH, CAPMH23F, CAPMH34F, CAPM2, CAPMH2 or CAPM3 is present	-	-
B2TH	CAPMH3 must be enclosed by MET2, MET3 and MET4	-	-
B3TH	CAPMH3 must not be over VIA1 or PAD	-	-
B4TH	CAPMH3 without VIA2 or VIA3 is not allowed	-	-
B5TH	MET2 and MET4 must be connected	-	-
B6TH	CAPMH3 without VIATP is not allowed Note: Valid if MET4 module is selected and MET5 module is not selected.	-	-
B7TH	MET3 and METTP must be connected Note: CAPMH3 must be enclosed by METTP. Note: Valid if MET4 module is selected and MET5 module is not selected.	-	-
B8TH	CAPMH3 without VIA4 is not allowed Note: Valid if MET5 module is selected.	-	-
B9TH	MET3 and MET5 must be connected Note: CAPMH3 must be enclosed by MET5. Note: Valid if MET5 module is selected.	-	-
W1TH	Minimum CAPMH3 width	2.0	µm
W2TH	Maximum CAPMH3 bounding box size Note: The bounding box is the generated minimum rectangle enclosing the polygon.	30.0 x 30.0	µm x µm
S1TH	Minimum CAPMH3 spacing/notch	1.5	µm
S4V4	Minimum VIA4 spacing on CAPMH3 Note: Valid if MET5 module is selected.	2.0	µm
S8V2	Minimum VIA2 spacing on CAPMH3	2.0	µm
S8V3	Minimum VIA3 spacing on CAPMH3	2.0	µm
S8VT	Minimum VIATP spacing on CAPMH3 Note: Valid if MET4 module is selected and MET5 module is not selected.	2.0	µm
S1THPA	Minimum CAPMH3 spacing to PAD	10.0	µm
S1THV1	Minimum CAPMH3 spacing to VIA1	0.5	µm
S1THV2	Minimum CAPMH3 spacing to VIA2	0.5	µm
S1THV3	Minimum CAPMH3 spacing to VIA3	0.5	µm
S1THV4	Minimum CAPMH3 spacing to VIA4 Note: Valid if MET5 module is selected.	0.5	µm
S1THVT	Minimum CAPMH3 spacing to VIATP Note: Valid if MET4 module is selected and MET5 module is not selected.	0.5	µm
E1M2TH	Minimum MET2 enclosure of CAPMH3	0.5	µm
E1M3TH	Minimum MET3 enclosure of CAPMH3	0.5	µm
E1M4TH	Minimum MET4 enclosure of CAPMH3	0.5	µm
E1THV2	Minimum CAPMH3 enclosure of VIA2	0.3	µm
E1THV3	Minimum CAPMH3 enclosure of VIA3	0.3	µm

3. Layer and Device rules → 3.35 TMIMH module→ 3.35.1 Layer rules→ CAPMH3

Name	Description	Value	Unit
E1THV4	Minimum CAPMH3 enclosure of VIA4 Note: Valid if MET5 module is selected.	0.3	μm
E1THVT	Minimum CAPMH3 enclosure of VIATP Note: Valid if MET4 module is selected and MET5 module is not selected.	0.3	μm
E3M4V3	Minimum MET4 enclosure of VIA3 Note: This rule is related to all VIAs inside CAPM3 and CAPMH3 regions extended by 2.5 μm.	0.15	μm
E4M2V1	Minimum MET2 enclosure of VIA1 Note: This rule is related to all VIAs inside CAPM3 and CAPMH3 regions extended by 2.5 μm.	0.15	μm
E4M4V4	Minimum MET4 enclosure of VIA4 Note: Valid if MET5 module is selected. Note: This rule is related to all VIAs inside CAPM3 and CAPMH3 regions extended by 2.5 μm.	0.15	μm
E4M4VT	Minimum MET4 enclosure of VIATP Note: This rule is related to all VIAs inside CAPM3 and CAPMH3 regions extended by 2.5 μm. Note: Valid if MET4 module is selected and MET5 module is not selected.	0.15	μm
E5M2V2	Minimum MET2 enclosure of VIA2 Note: This rule is related to all VIAs inside CAPM3 and CAPMH3 regions extended by 2.5 μm.	0.15	μm
E5M3V2	Minimum MET3 enclosure of VIA2 Note: This rule is related to all VIAs inside CAPM3 and CAPMH3 regions extended by 2.5 μm.	0.15	μm
E5M3V3	Minimum MET3 enclosure of VIA3 Note: This rule is related to all VIAs inside CAPM3 and CAPMH3 regions extended by 2.5 μm.	0.15	μm
Q2V4	Recommended minimum ratio of VIA4 to CAPMH3 area Note: Valid if MET5 module is selected.	1.0	%
Q6V2	Recommended minimum ratio of VIA2 to CAPMH3 area	1.0	%
Q6V3	Recommended minimum ratio of VIA3 to CAPMH3 area	1.0	%
Q6VT	Recommended minimum ratio of VIATP to CAPMH3 area Note: Valid if MET4 module is selected and MET5 module is not selected.	1.0	%

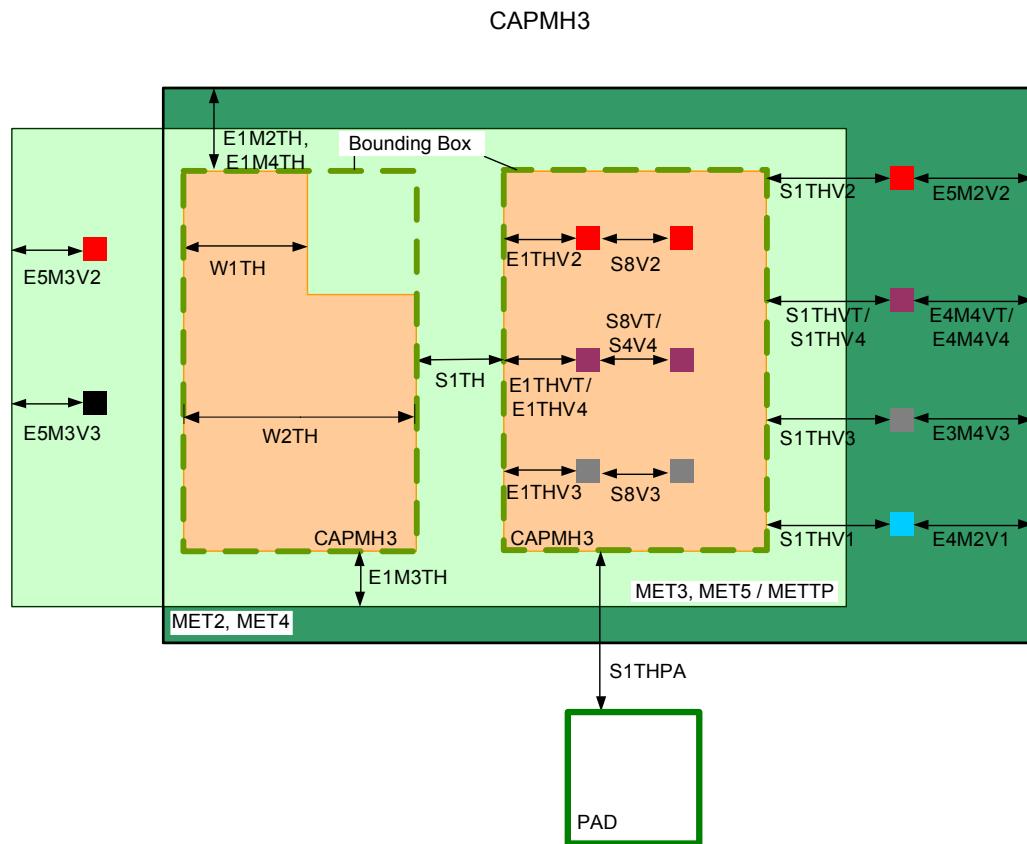
Note: All dummy generation is blocked inside CAPMH3 regions extended by 2.5μm.

Note: The placement of TMIMH must start from MET2 as described in the Table for TMIMH Construction.

Table for TMIMH Construction

module combination	structure of metal stacking	device	Top MIM metal
LPMOS	n/a	n/a	n/a
MET4	MET2 / CAPMH3 / MET3 / CAPMH3 / MET4 / CAPMH3 / METTP	ctmmh5t	METTP
MET5	MET2 / CAPMH3 / MET3 / CAPMH3 / MET4 / CAPMH3 / MET5	ctmmh5	MET5

3. Layer and Device rules → 3.35 TMIMH module → 3.35.1 Layer rules → CAPMH3

**Figure 3.208** CAPMH3

3. Layer and Device rules → 3.35 TMIMH module → 3.35.2 Device rules → ctmmh5, ctmmh5t

3.35.2 Device rules

ctmmh5, ctmmh5t

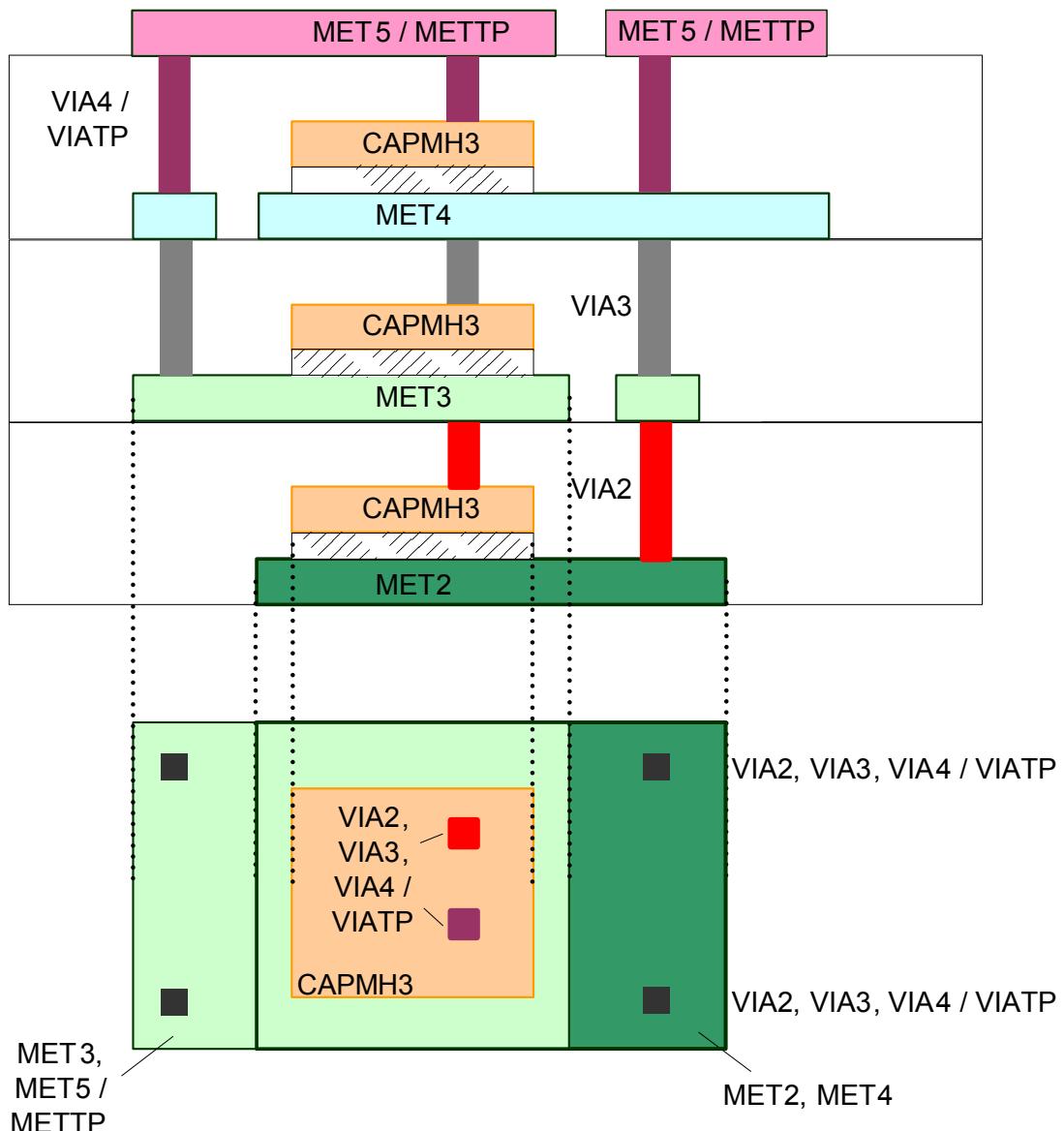


Figure 3.209 ctmmh5t, ctmmh5

3. Layer and Device rules → 3.36 NVM, FLASH modules

3.36 NVM, FLASH modules

Ready-to-use SONOS based non-volatile memory blocks are available for NVM (NVRAM) and FLASH (Flash) modules.

The rules of layers and devices only used for non-volatile memory blocks are not described in this specification. Because additional devices are not available for the NVM and FLASH modules this specification does not declare any additional rules.

3.36.1 Layer rules

SCI

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
BDSC	Not allowed to be used by customers Note: Layer for predefined memory blocks only. Reserved layer.	-	-

3. Layer and Device rules → 3.37 OTP3 module

3.37 OTP3 module

The OTP3 module delivers ready-to-use memory blocks. No device or layer rule for this module is described in this specification. Refer to the OTP block specifications regarding the process module combination which is required for the specific memory block.

3. Layer and Device rules → 3.38 ANODOP module

3.38 ANODOP module

3.38.1 Layer rules

ANODOP

Name	Description	Value	Unit
B1OA	ANODOP is only allowed for dphod#	-	-
W1OA	Minimum ANODOP width	0.44	µm
S1OA	Minimum ANODOP spacing/notch	0.44	µm

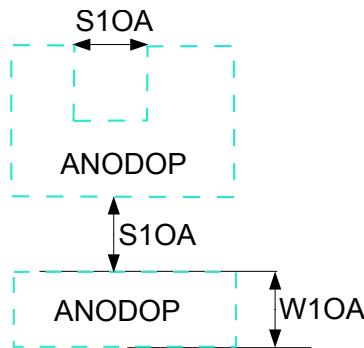


Figure 3.210 ANODOP

3. Layer and Device rules → 3.38 ANODOP module→ 3.38.2 Device rules→ dphod

3.38.2 Device rules

dphod

The layout of the dphod is predefined and only Width and Length can be changed in the range of 10µm and 500µm.

Note: The sixth terminal defines the light power input. It must be marked with text in the layer PHODEF (TEXT) which has to be placed on top of UVWIN area in top level layout.

3. Layer and Device rules → 3.38 ANODOP module→ 3.38.2 Device rules→ dphod

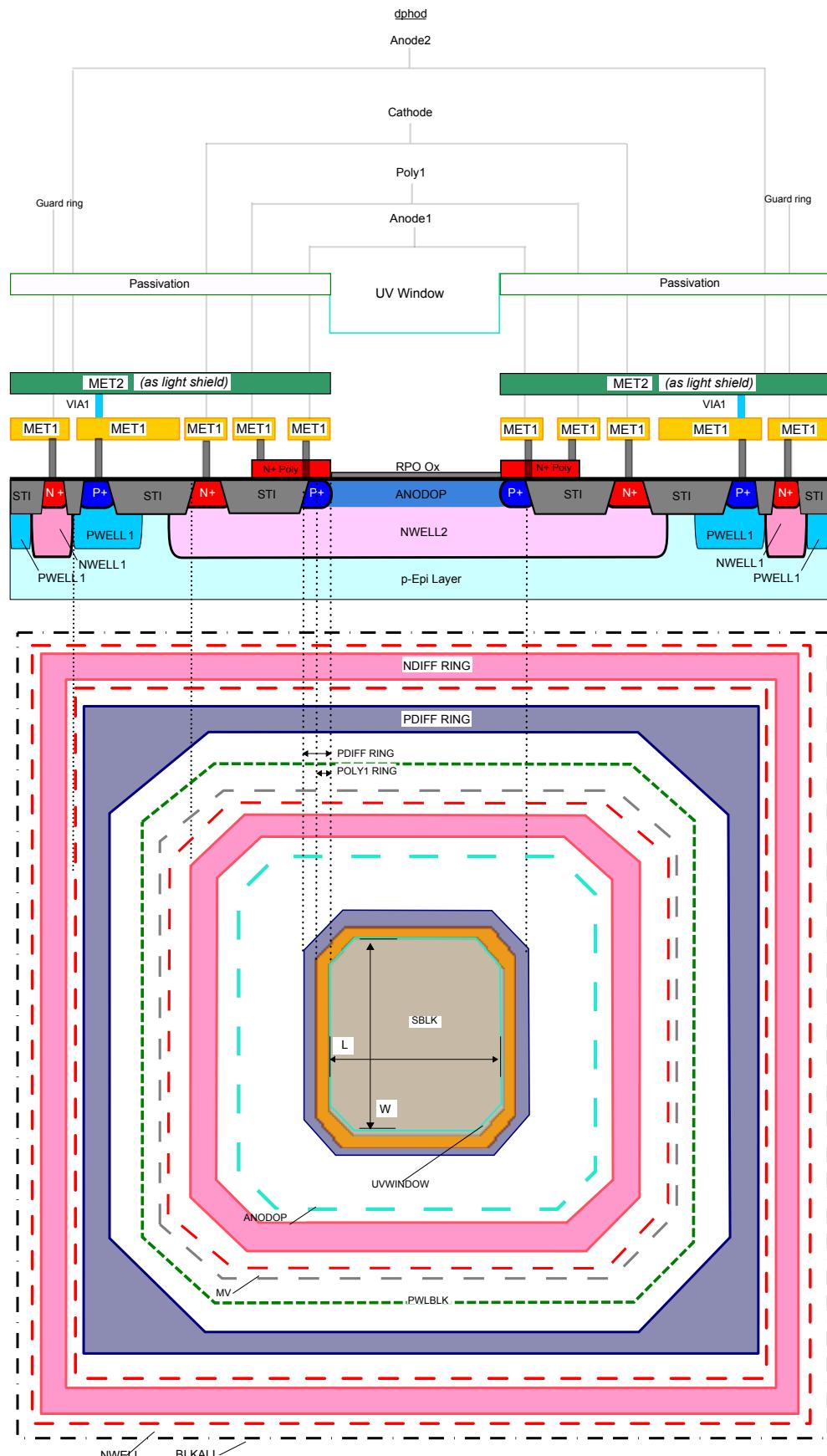


Figure 3.211 dphod

3. Layer and Device rules → 3.38 ANODOP module→ 3.38.2 Device rules→ dphod0

dphod0

The device dphod0 is a MET2 covered variant of dphod.

Note: The sixth terminal defines the light power input. It must be marked with text in the layer PHODEF (TEXT) which has to be placed on top of UVWIN area in top level layout.

Note: The layout of the dphod0 is predefined and only Width and Length can be changed in the range of 10µm and 500µm.

dphodfp

The device dphodfp is a POLY1 covered variant of dphod.

Note: The sixth terminal defines the light power input. It must be marked with text in the layer PHODEF (TEXT) which has to be placed on top of UVWIN area in top level layout.

Note: The layout of the dphodfp is predefined and only Width and Length can be changed in the range of 10µm and 500µm.

3. Layer and Device rules → 3.39 CATDOP module

3.39 CATDOP module

3.39.1 Layer rules

CATDOP

Name	Description	Value	Unit
B1OC	CATDOP is only allowed for dphoc#, davla#	-	-
W1OC	Minimum CATDOP width	0.44	µm
S1OC	Minimum CATDOP spacing/notch	0.44	µm
E1OCDF	Minimum CATDOP extension beyond DIFF	0.18	µm
A1OC	Minimum CATDOP area	0.3844	µm ²

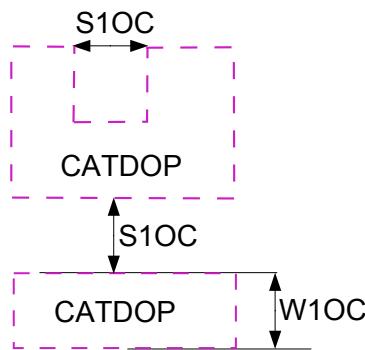


Figure 3.212 CATDOP

3. Layer and Device rules → 3.39 CATDOP module→ 3.39.2 Device rules→ dphoc

3.39.2 Device rules

dphoc

Note: The fifth terminal defines the light power input. It must be marked with text in the layer PHODEF (TEXT) which has to be placed on top of UVWIN area in top level layout.

Note: The layout of the dphoc is predefined and only Width and Length can be changed in the range of 10µm and 500µm.

3. Layer and Device rules → 3.39 CATDOP module → 3.39.2 Device rules → dphoc

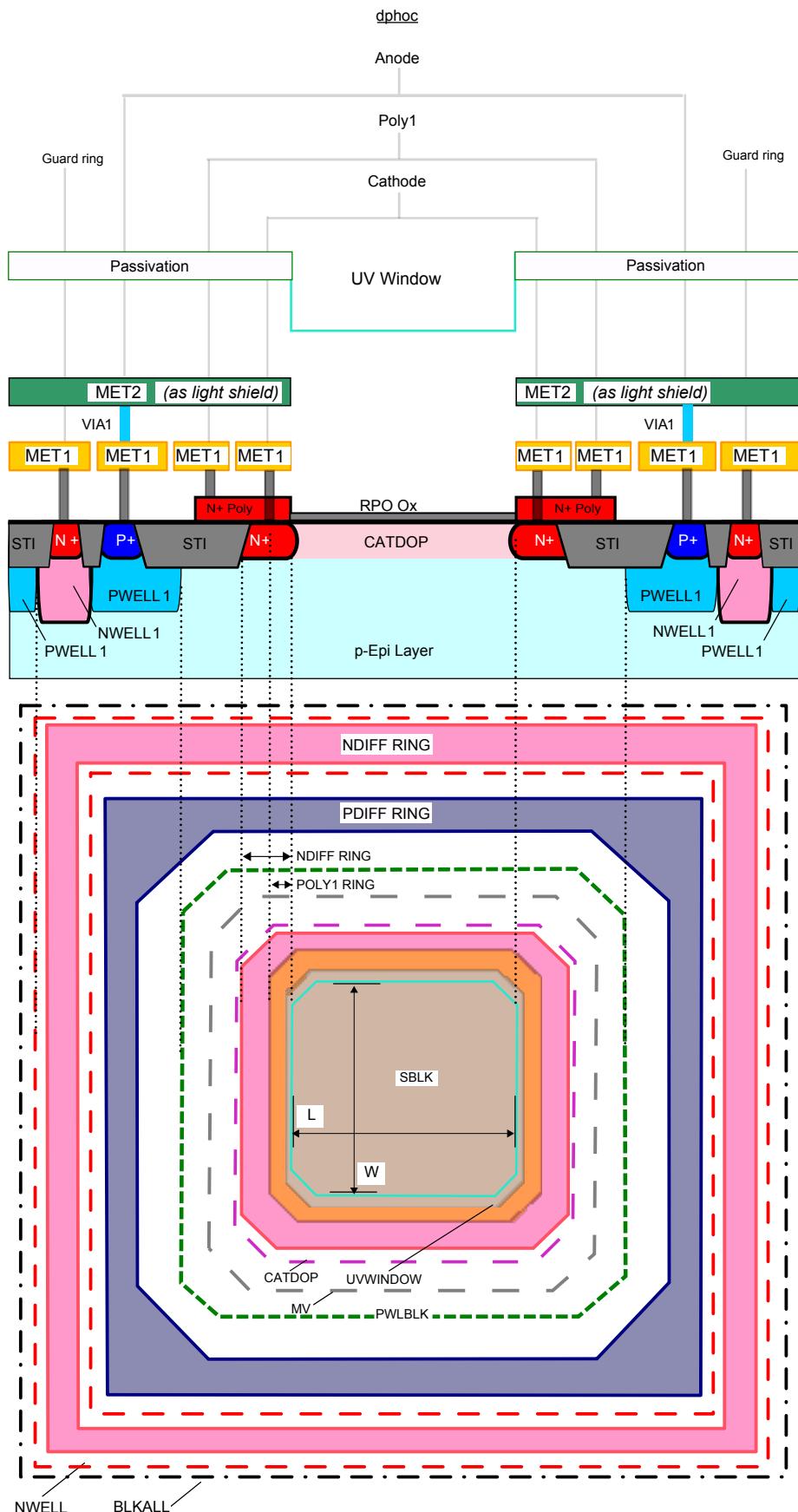


Figure 3.213 dphoc

3. Layer and Device rules → 3.39 CATDOP module→ 3.39.2 Device rules→ dphoc0

dphoc0

The device dphoc0 is a MET2 covered variant of dphoc.

Note: The fifth terminal defines the light power input. It must be marked with text in the layer PHODEF (TEXT) which has to be placed on top of UVWIN area in top level layout.

Note: The layout of the dphoc0 is predefined and only Width and Length can be changed in the range of 10µm and 500µm.

dphocfp

The device dphocfp is a POLY1 covered variant of dphoc.

Note: The fifth terminal defines the light power input. It must be marked with text in the layer PHODEF (TEXT) which has to be placed on top of UVWIN area in top level layout.

Note: The layout of the dphocfp is predefined and only Width and Length can be changed in the range of 10µm and 500µm.

3. Layer and Device rules → 3.40 UVWINDOW module

3.40 UVWINDOW module

3.40.1 Layer rules

UVWIN

Name	Description	Value	Unit
B1UV	UVWIN overlap of MET3, METTP, PAD is not allowed	-	-
B2UV	UVWIN overlap of POLY1 is not allowed (except dphocfp, dphodfp)	-	-
B3UV	UVWIN is only allowed for dphoc#, dphod#	-	-
B4UV	UVWIN without BLKALL is not allowed	-	-
W1UV	Minimum UVWIN width	3.0	μm
	Note: For best optical matching it is recommended that all UVWIN have the same size.		
W1DFUV	Maximum (DIFF overlap of UVWIN) bounding box size	502.0 x 502.0	μm x μm
	Note: The bounding box is the generated minimum rectangle enclosing the polygon.		
W2UV	Maximum UVWIN bounding box size	500.0 x 500.0	μm x μm
	Note: The bounding box is the generated minimum rectangle enclosing the polygon.		
S1UV	Minimum UVWIN spacing / notch	3.0	μm
S1UVM3	Minimum UVWIN spacing to MET3	1.5	μm
S1UVMT	Minimum UVWIN spacing to METTP	2.0	μm
S1UVPA	Minimum UVWIN to PAD spacing	5.0	μm
E1BAUV	Minimum BLKALL enclosure of UVWIN	2.0	μm

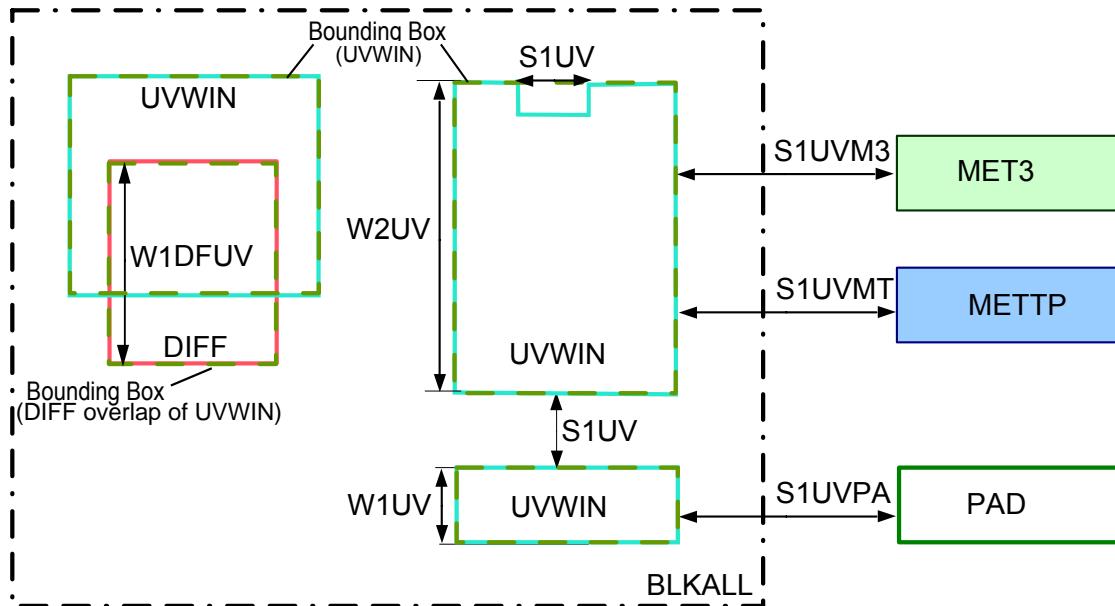


Figure 3.214 UVWIN

3. Layer and Device rules → 3.41 AVLA module

3.41 AVLA module

3.41.1 Layer rules

AML

Name	Description	Value	Unit
B1AM	AML is only allowed for davla#	-	-
B2AM	AML without CATDIFF is not allowed	-	-
W1AM	Minimum AML width	0.44	µm
S1AM	Minimum AML spacing / notch	0.44	µm
A1AM	Minimum AML area	0.3844	µm ²

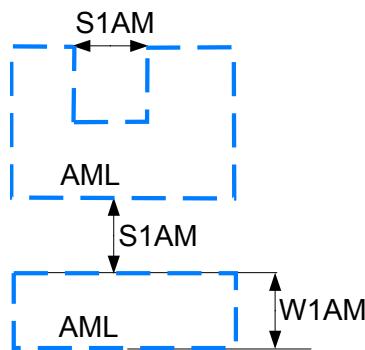


Figure 3.215 AML

3. Layer and Device rules → 3.41 AVLA module→ 3.41.2 Device rules→ dapda

3.41.2 Device rules

dapda

The layout of the dapda is predefined and only Width and Length can be changed in the range of 50µm and 200µm. The other rules support the fixed dimensions of the layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B1PBDC	CATDIFF without PWBLK is not allowed	-	-
B1SB	SBLK overlap of MET1, MET2, MET3, MET4, MET5, METTP or METTPL is not allowed	-	-
B2SB	SBLK without BLKALL is not allowed	-	-
B3AM	AML without SBLK is not allowed	-	-
B3NW	dapda/dapda0 without NWELL ring is not allowed	-	-
E1BASB	Minimum BLKALL enclosure of SBLK	1.7	µm
E1DCAM	Minimum CATDIFF enclosure of AML	1.0	µm
E1PBDC	Minimum PWBLK enclosure of CATDIFF	4.5	µm

Note: The third terminal defines the light power input. It must be marked with text in the layer PHODEF (TEXT) which has to be placed on top of AML area in top level layout.

3. Layer and Device rules → 3.41 AVLA module→ 3.41.2 Device rules→ dapda

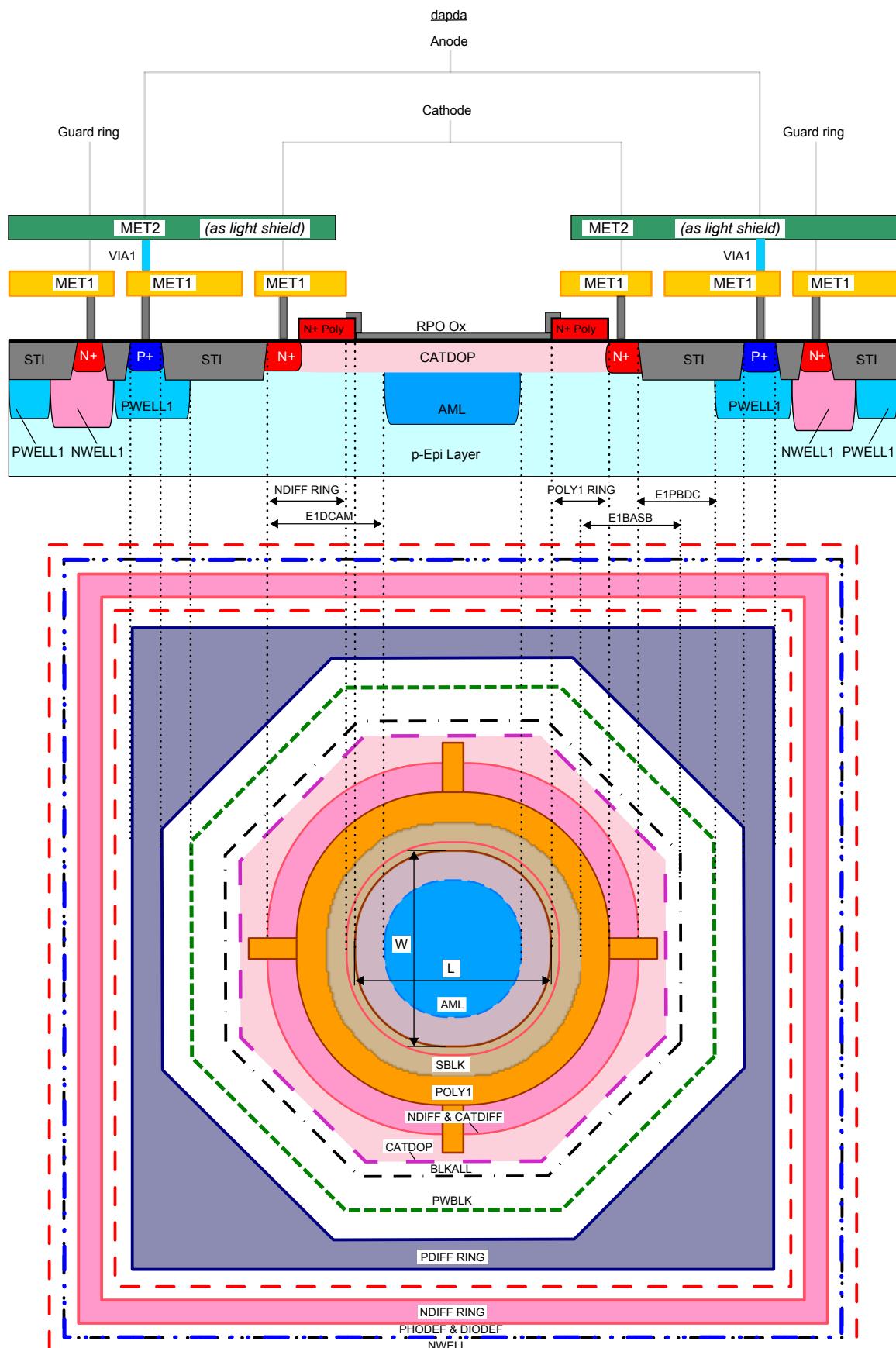


Figure 3.216 dapda

3. Layer and Device rules → 3.41 AVLA module→ 3.41.2 Device rules→ dapda0

dapda0

The device dapda0 is a MET2 covered variant of dapda.

The layout of the dapda0 is predefined and only Width and Length can be changed in the range of 50µm and 200µm. The other rules support the fixed dimensions of the layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B1PBDC	CATDIFF without PWBLK is not allowed	-	-
B2SB	SBLK without BLKALL is not allowed	-	-
B3AM	AML without SBLK is not allowed	-	-
B3NW	dapda/dapda0 without NWELL ring is not allowed	-	-
B6M2	dapda0/dspada0 without MET2 is not allowed Note: Holes in MET2 are allowed to satisfy the maximum metal width rule. The holes in MET2 must be surrounded by a VIA1 ring filled with MET1 completely.	-	-
E1BASB	Minimum BLKALL enclosure of SBLK	1.7	µm
E1DCAM	Minimum CATDIFF enclosure of AML	1.0	µm
E1PBDC	Minimum PWBLK enclosure of CATDIFF	4.5	µm

Note: The third terminal defines the light power input. It must be marked with text in the layer PHODEF (TEXT) which has to be placed on top of AML area in top level layout.

3. Layer and Device rules → 3.41 AVLA module→ 3.41.2 Device rules→ dspada

dspada

The layout of the dspada is predefined with a fixed width and length of 10 µm optical active area and an effective fill factor of 18.1 %. It must not be changed. The other rules support the fixed dimensions of the layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B1PBDC	CATDIFF without PWBLK is not allowed	-	-
B1SB	SBLK overlap of MET1, MET2, MET3, MET4, MET5, METTP or METTPL is not allowed	-	-
B2SB	SBLK without BLKALL is not allowed	-	-
B3AM	AML without SBLK is not allowed	-	-
E1BASB	Minimum BLKALL enclosure of SBLK	1.7	µm
E1DCAM	Minimum CATDIFF enclosure of AML	1.0	µm
E1PBDC	Minimum PWBLK enclosure of CATDIFF	4.5	µm

Note: The third terminal defines the light power input. It must be marked with text in the layer PHODEF (TEXT) which has to be placed on top of AML area in top level layout.

3. Layer and Device rules → 3.41 AVLA module→ 3.41.2 Device rules→ dspada

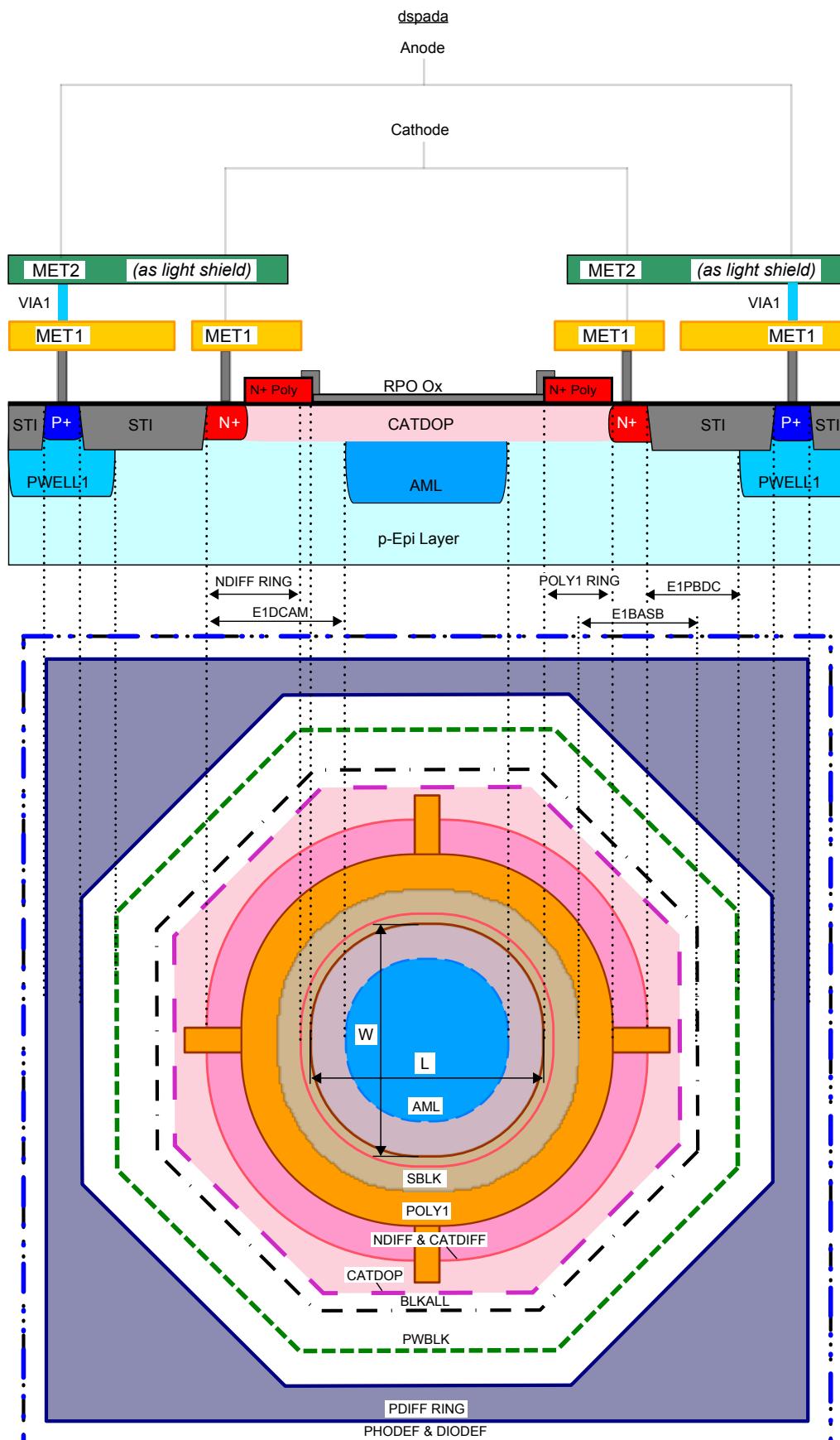


Figure 3.217 dspada

3. Layer and Device rules → 3.41 AVLA module→ 3.41.2 Device rules→ dspada0

dspada0

The device dspada0 is a MET2 covered variant of dspada.

The layout of the dspada0 is predefined with a fixed width and length of 10 µm optical active area and an effective fill factor of 0 %. It must not be changed. The other rules support the fixed dimensions of the layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B1PBDC	CATDIFF without PWBLK is not allowed	-	-
B2SB	SBLK without BLKALL is not allowed	-	-
B3AM	AML without SBLK is not allowed	-	-
B6M2	dapda0/dspada0 without MET2 is not allowed Note: Holes in MET2 are allowed to satisfy the maximum metal width rule. The holes in MET2 must be surrounded by a VIA1 ring filled with MET1 completely.	-	-
E1BASB	Minimum BLKALL enclosure of SBLK	1.7	µm
E1DCAM	Minimum CATDIFF enclosure of AML	1.0	µm
E1PBDC	Minimum PWBLK enclosure of CATDIFF	4.5	µm

Note: The third terminal defines the light power input. It must be marked with text in the layer PHODEF (TEXT) which has to be placed on top of AML area in top level layout.

3. Layer and Device rules → 3.42 BIPESD module

3.42 BIPESD module

3.42.1 Layer rules

HNW

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1HW	HNW without HVGOX and PWBLK is not allowed (except qpvhscr, dsb#)	-	-
B2HW	HNW must be surrounded by a GUARD RING consisting of PDIFF and HVPWELL	-	-
B3HW	HNW overlap of DNWELL, DNWELLMV, NWELL, HVPWELL, ISOPW, SCI, DEPL or PDD is not allowed. (except ISOPW and NWELL for qpvhscr, HVPWELL for qpvhbscr)	-	-
B5HW	HNW overlap of rpp1#, rnp1#, rpp1s#, MRES or HRES is not allowed	-	-
B4HW	HVNWELL crossing HNW edge is not allowed	-	-
W1HW	Minimum HNW width	8.0	µm
S1HW	Minimum HNW spacing/notch	10.0	µm
S1HWDN	Minimum HNW spacing to NDIFF	4.5	µm
S1HWDP	Fixed HNW spacing to PDIFF	4.0	µm
S1HWHN	Minimum HNW spacing to HVNWELL	10.0	µm
S1HWHP	Minimum HNW spacing to HVPWELL	3.76	µm
S1HWND	Minimum HNW spacing to NDF	10.0	µm
S1HWNW	Minimum HNW spacing to NWELL	10.0	µm
S1HWP1	Minimum HNW spacing to POLY1	5.35	µm
S1HWWD	Minimum HNW spacing to DNWELL	10.0	µm
S1HWWM	Minimum HNW spacing to DNWELLMV	10.0	µm
E1GHHW	Minimum HVGOX enclosure of HNW	0.5	µm
E1HWDN	Fixed HNW enclosure of NDIFF (except qpvhscr, qpvhbscr, dsb#)	2.0	µm
E1HWDP	Minimum HNW enclosure of PDIFF	2.86	µm
E1HWHN	Minimum HNW enclosure of HVNWELL	1.76	µm
E1HWP1	Minimum HNW enclosure of POLY1	2.95	µm
E1PBHW	Fixed PWBLK enclosure of HNW	4.0	µm

3. Layer and Device rules → 3.42 BIPESD module→ 3.42.1 Layer rules→ HNW

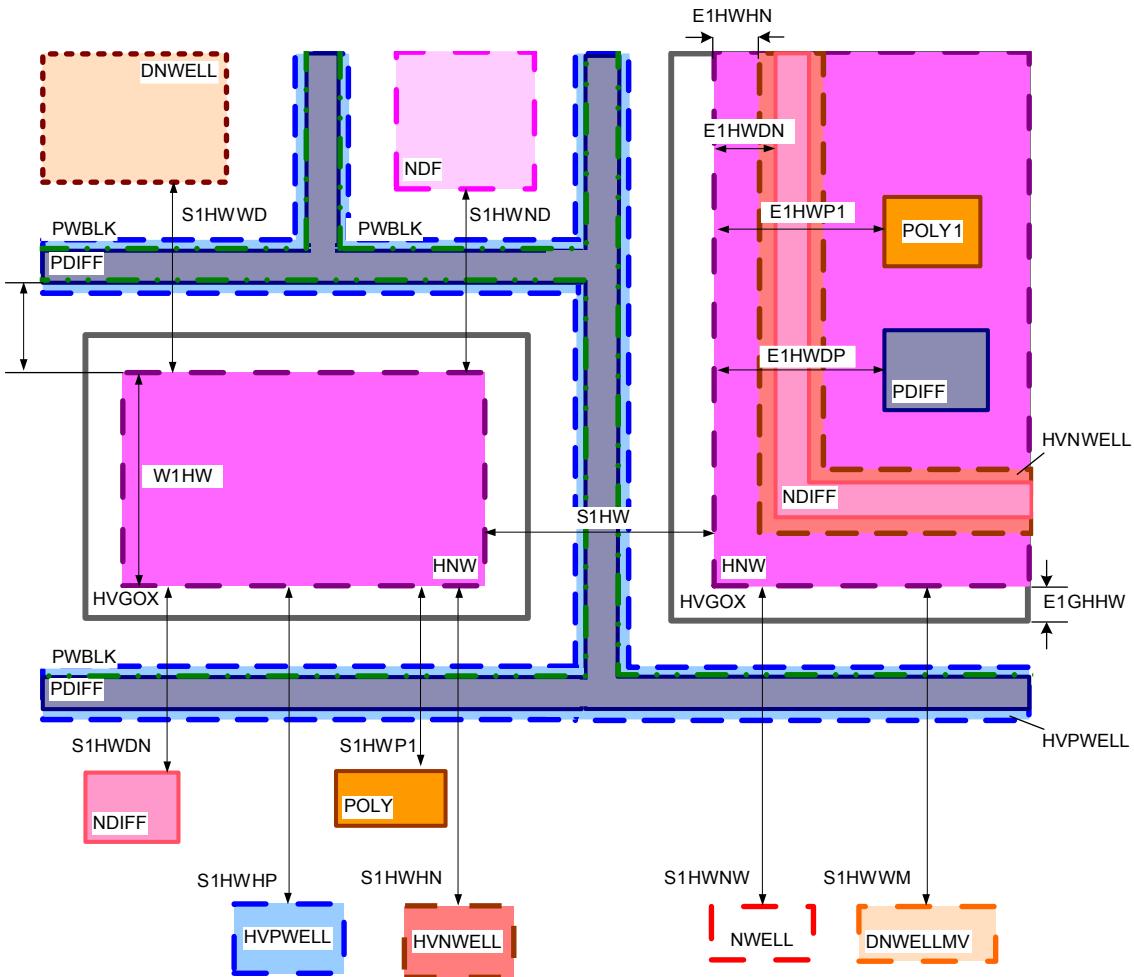


Figure 3.218 HNW

3. Layer and Device rules → 3.42 BIPESD module→ 3.42.1 Layer rules→ HVPWELL

HVPWELL

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1HP	HVPWELL must be contacted by PDIFF	-	-
B3HP	HVPWELL overlap of NWELL is not allowed	-	-
B5HP	HVPWELL overlap of DNWELL is not allowed Note: Valid inside DNWELLMV.	-	-
B2HP	DIFF crossing HVPWELL edge is not allowed (except ped, ned#, nm#, nh#, pmma, nmma)	-	-
B4HP	HVPWELL crossing DNWELL edge is not allowed	-	-
W1HP	Minimum HVPWELL width	0.9	μm
S1HP	Minimum HVPWELL spacing/notch	0.6	μm
S2HP	Minimum HVPWELL spacing (different net) Note: Not valid for channel region of pmma GATE (oversized by 0.43 μm).	3.0	μm
S1HPDN	Minimum HVPWELL spacing to NDIFF (except ned#)	0.43	μm
S1HPDP	Minimum HVPWELL spacing to PDIFF	0.43	μm
S1HPNW	Minimum HVPWELL spacing to NWELL Note: Valid inside DNWELLMV.	0.8	μm
S2HPDN	Fixed HVPWELL spacing to NDIFF (except ned#, ped#, qpvascr) Note: Valid inside DNWELL and NOT DNWELLMV.	3.0	μm
S2HPNW	Minimum HVPWELL spacing to NWELL Note: Valid inside DNWELL and NOT DNWELLMV.	3.0	μm
E1HPDN	Minimum HVPWELL enclosure of NDIFF	0.43	μm
E1HPDP	Minimum HVPWELL enclosure of PDIFF (except ped#, pmma, nmma) Note: Valid inside DNWELLMV/DNWELL.	0.43	μm

3. Layer and Device rules → 3.42 BIPESD module → 3.42.1 Layer rules → HVPWELL

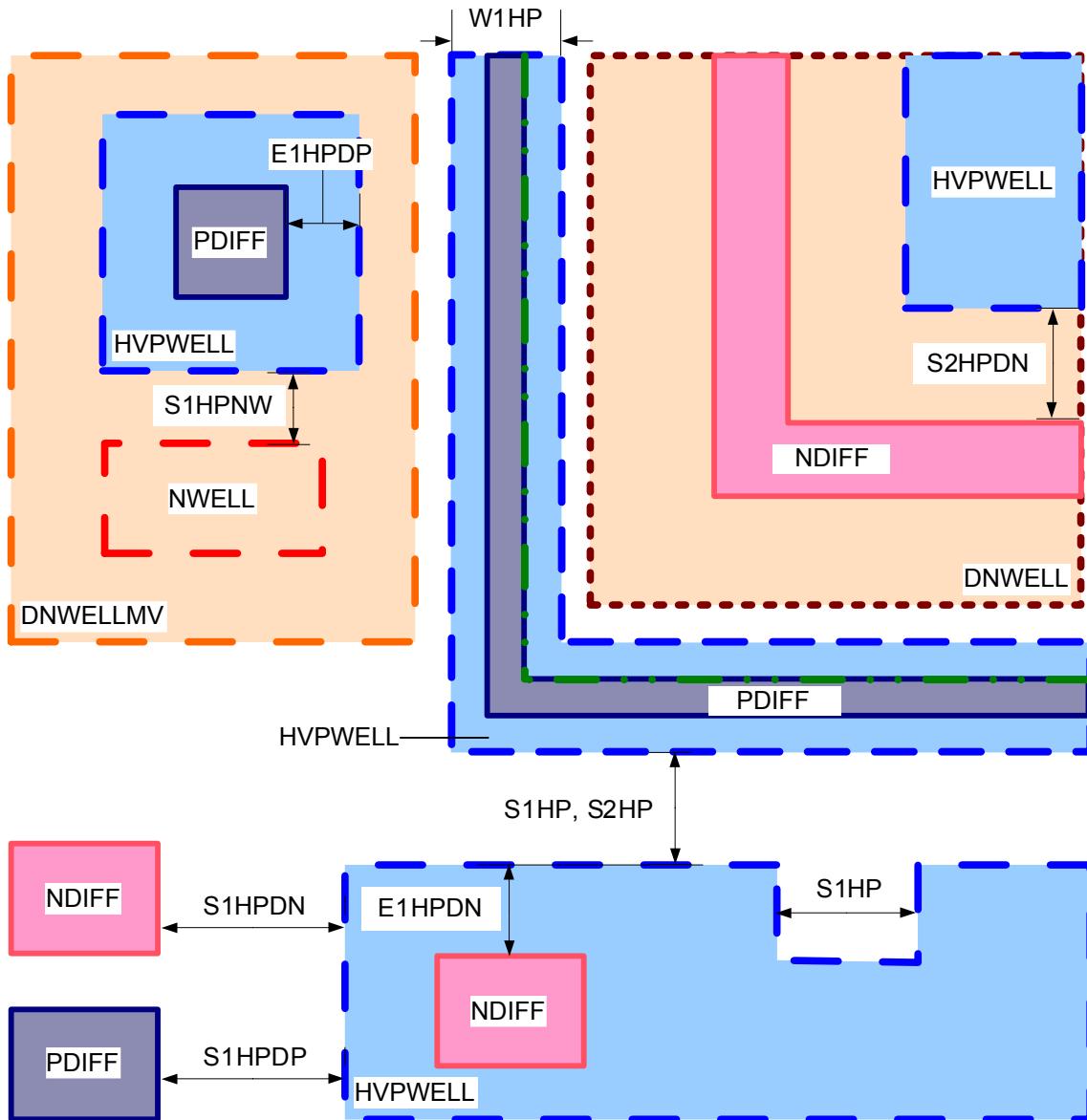


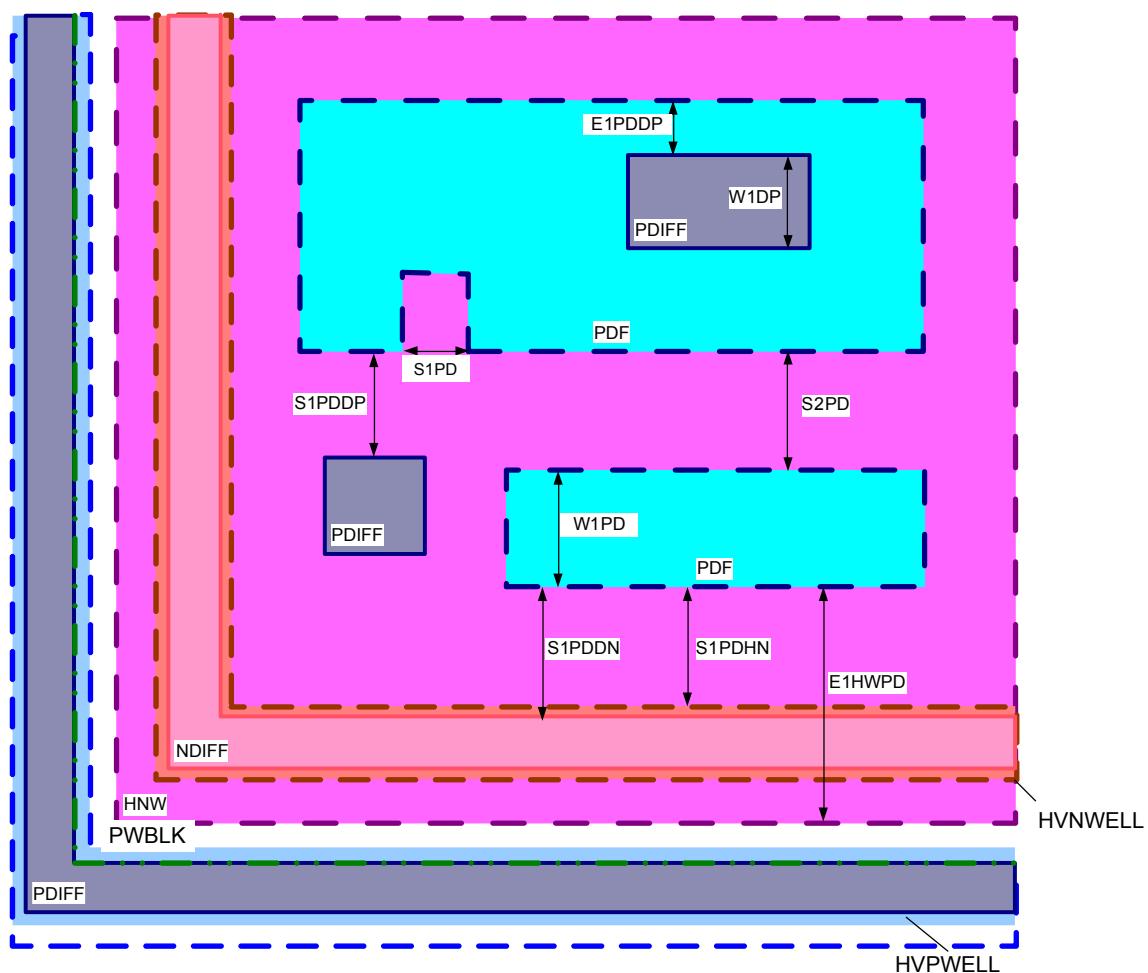
Figure 3.219 HVPWELL

3. Layer and Device rules → 3.42 BIPESD module→ 3.42.1 Layer rules→ PDF

PDF

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1PD	PDF without HNW is not allowed	-	-
B2PD	NDIFF overlap of PDF is not allowed (except qvhscr)	-	-
B3PD	PDF overlap of HVNWELL is not allowed	-	-
W1DP	Fixed PDIFF stripe width (except channel region of ph#, pm#)	0.42	μm
W1PD	Minimum PDF width (except phhv, pm#)	5.0	μm
S1PD	Minimum PDF spacing/notch (except channel region of pmmc)	2.2	μm
S2PD	Minimum PDF spacing (different net) (except channel region of phhv, pmmc)	5.0	μm
S1PDDN	Minimum PDF spacing to NDIFF (except qvhscr)	3.0	μm
S1PDDP	Minimum PDF spacing to PDIFF (except qvhscr)	4.0	μm
	Note: Valid for PDIFF outside PDF.		
S1PDHN	Minimum PDF spacing to HVNWELL (except channel region of ph#, pm#)	2.76	μm
E1HWPD	Minimum HNW enclosure of PDF	5.0	μm
E1PDDP	Minimum PDF enclosure of PDIFF (except channel region of ph#, pm#, qvhscr)	3.0	μm

**Figure 3.220 PDF**

3. Layer and Device rules → 3.42 BIPESD module→ 3.42.2 Device rules→ qpvhscr

3.42.2 Device rules

qpvhscr

Note: The layout of the qpvhscr vertical bipolar PNP transistor is pre-defined and only the emitter length can be changed in the range of 16 μ m to 150 μ m. Device qpvhscr has a fixed emitter width of 5.42 μ m. The drawing below is a basic sketch only and does not show all details.

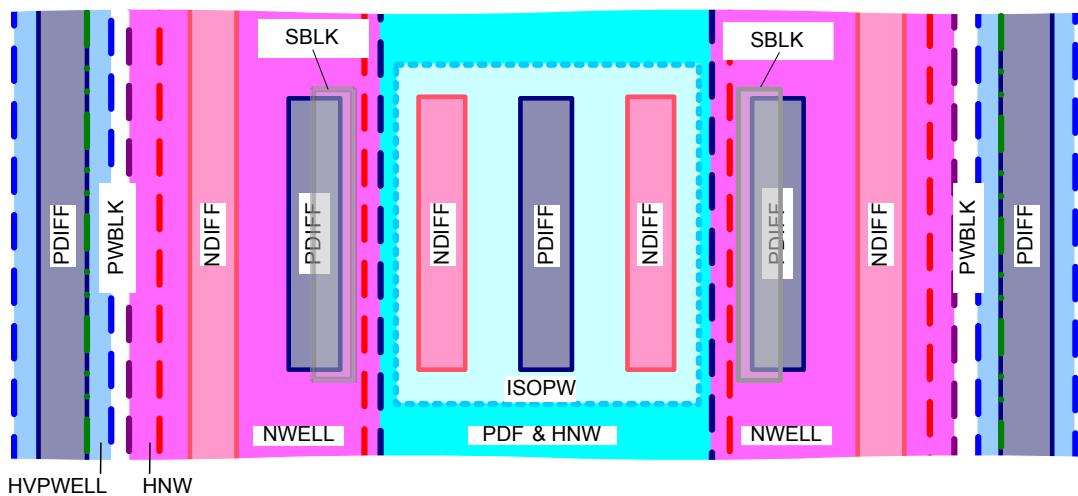
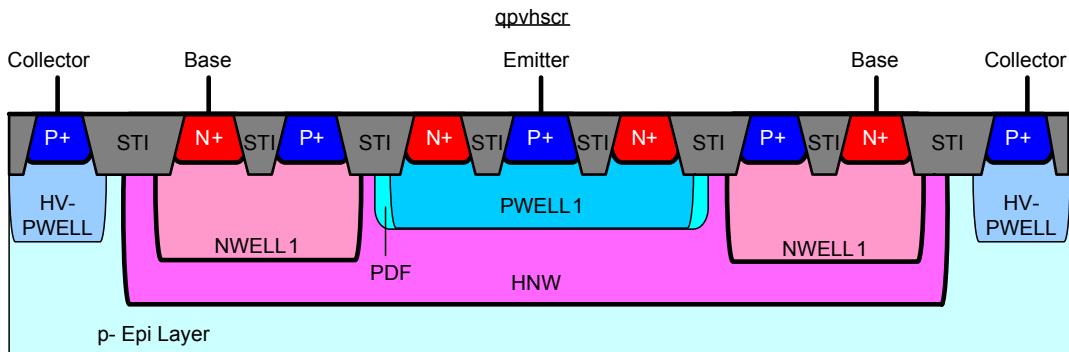


Figure 3.221 qpvhscr

3. Layer and Device rules → 3.43 ESDPNP module

3.43 ESDPNP module

3.43.1 Layer rules

HNW

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1HW	HNW without HVGOX and PWBLK is not allowed (except qpvhscr, dsb#)	-	-
B2HW	HNW must be surrounded by a GUARD RING consisting of PDIFF and HVPWELL	-	-
B3HW	HNW overlap of DNWELL, DNWELLMV, NWELL, HVPWELL, ISOPW, SCI, DEPL or PDD is not allowed. (except ISOPW and NWELL for qpvhscr, HVPWELL for qpvhbscr)	-	-
B5HW	HNW overlap of rpp1#, rnp1#, rpp1s#, MRES or HRES is not allowed	-	-
B4HW	HVNWELL crossing HNW edge is not allowed	-	-
W1HW	Minimum HNW width	8.0	μm
S1HW	Minimum HNW spacing/notch	10.0	μm
S1HWDN	Minimum HNW spacing to NDIF	4.5	μm
S1HWDP	Fixed HNW spacing to PDIFF	4.0	μm
S1HWHN	Minimum HNW spacing to HVNWELL	10.0	μm
S1HWHP	Minimum HNW spacing to HVPWELL	3.76	μm
S1HWND	Minimum HNW spacing to NDF	10.0	μm
S1HWNW	Minimum HNW spacing to NWELL	10.0	μm
S1HWP1	Minimum HNW spacing to POLY1	5.35	μm
S1HWWD	Minimum HNW spacing to DNWELL	10.0	μm
S1HWWM	Minimum HNW spacing to DNWELLMV	10.0	μm
E1GHHW	Minimum HVGOX enclosure of HNW	0.5	μm
E1HWDN	Fixed HNW enclosure of NDIF (except qpvhscr, qpvhbscr, dsb#)	2.0	μm
E1HWDP	Minimum HNW enclosure of PDIFF	2.86	μm
E1HWHN	Minimum HNW enclosure of HVNWELL	1.76	μm
E1HWP1	Minimum HNW enclosure of POLY1	2.95	μm
E1PBHW	Fixed PWBLK enclosure of HNW	4.0	μm

3. Layer and Device rules → 3.43 ESDPNP module → 3.43.1 Layer rules → HNW

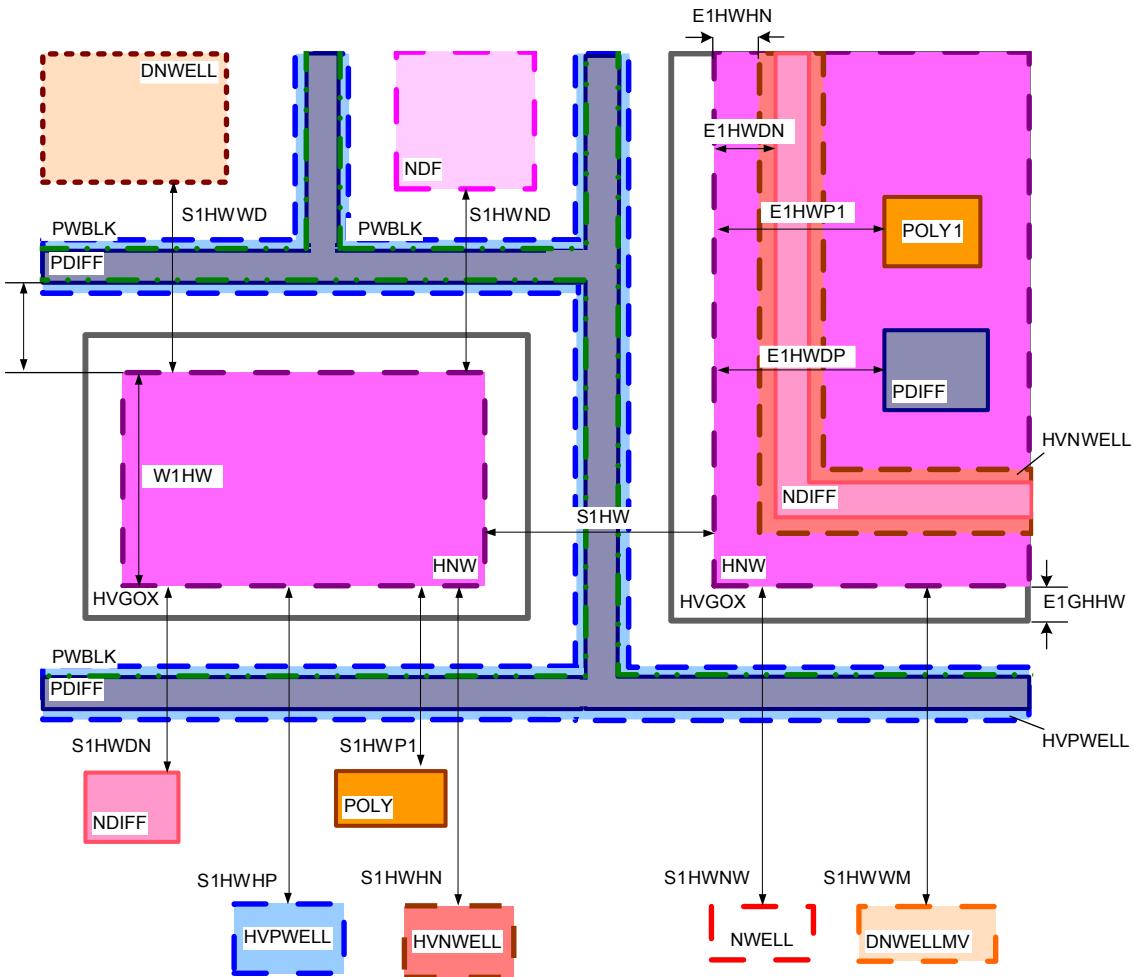


Figure 3.222 HNW

3. Layer and Device rules → 3.43 ESDPNP module→ 3.43.1 Layer rules→ HVGOX

HVGOX

Name	Description	Value	Unit
B1GHMV	HVGOX overlap of MV is not allowed	-	-
B1GH	DIFF crossing HVGOX edge is not allowed	-	-
W1GH	Minimum HVGOX width	0.6	μm
S1GH	Minimum HVGOX spacing/notch	1.0	μm
S1GHDF	Minimum HVGOX spacing to DIFF	0.2	μm
E1GHDF	Minimum HVGOX enclosure of DIFF	0.2	μm

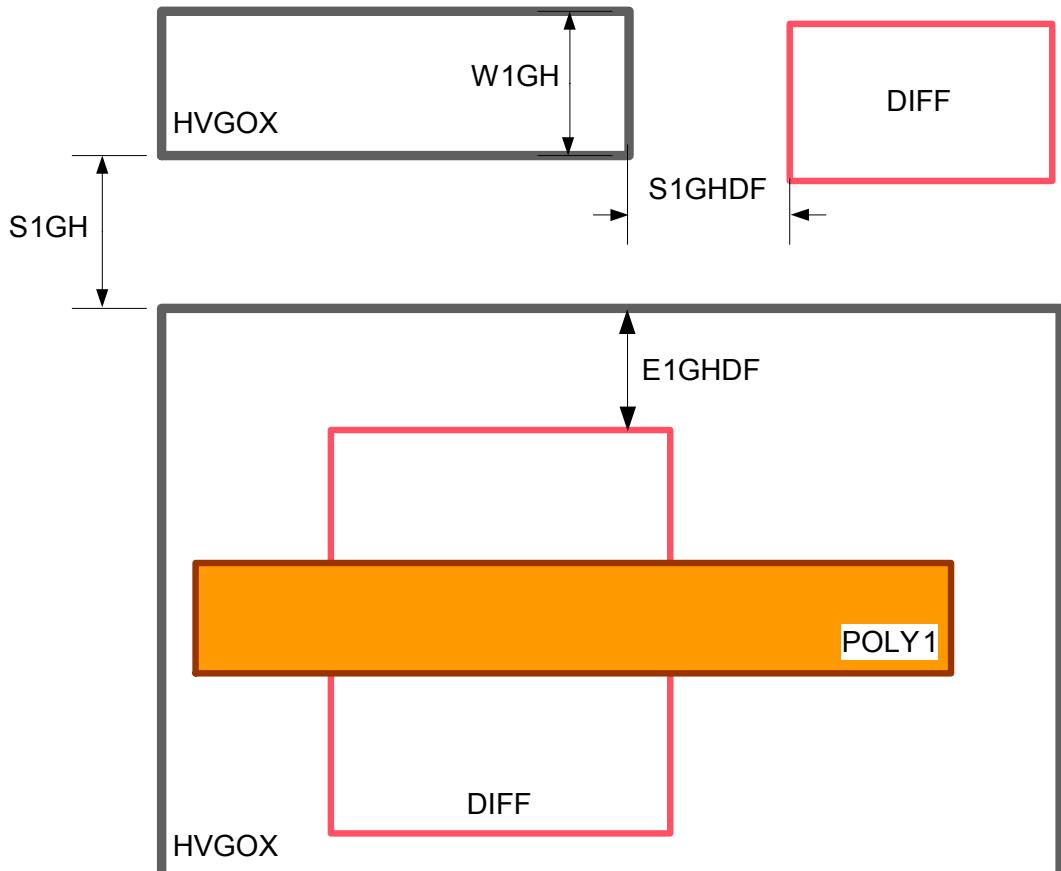


Figure 3.223 HVGOX

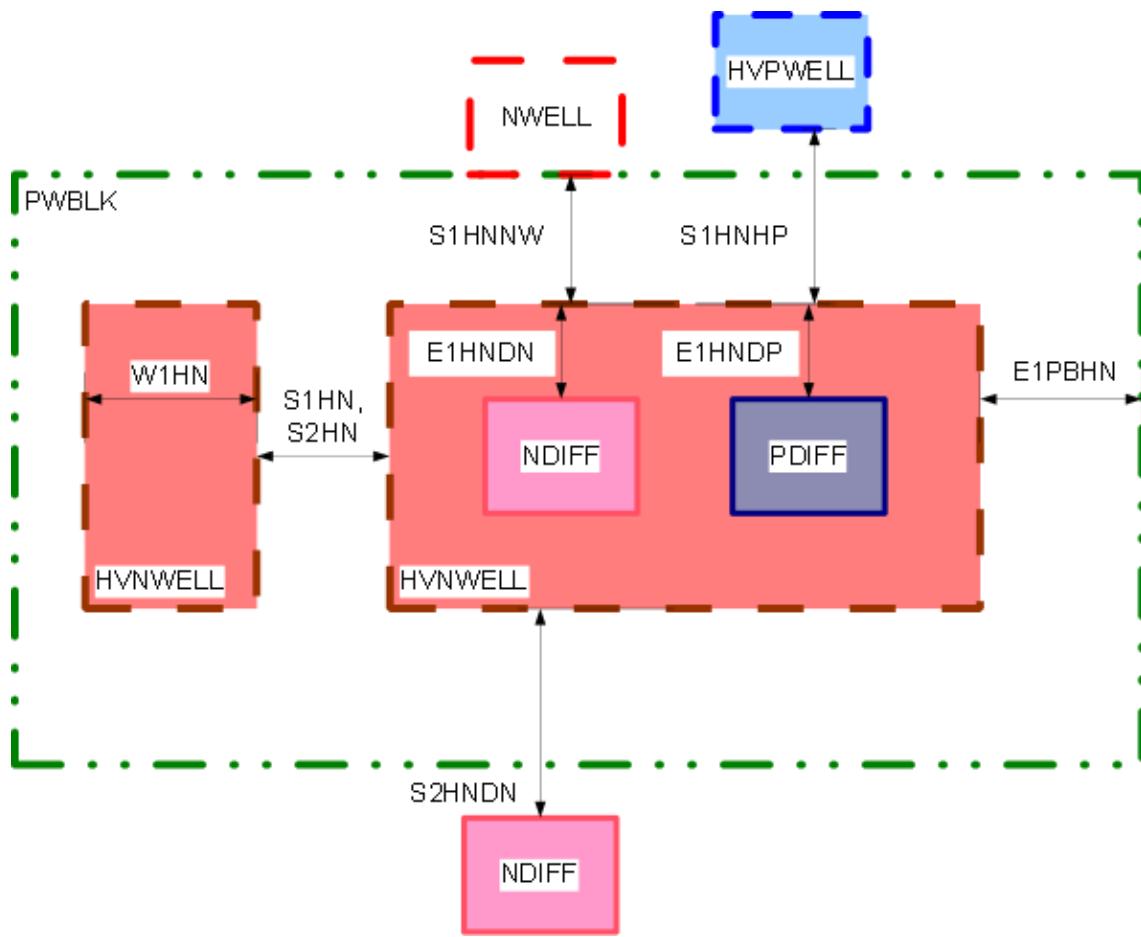
3. Layer and Device rules → 3.43 ESDPNP module→ 3.43.1 Layer rules→ HVNWELL

HVNWELL

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1HN	HVNWELL must be contacted by NDIFF	-	-
B2HN	HVNWELL overlap of HVPWELL or PDD is not allowed	-	-
B3HN	HVNWELL overlap of NWELL is not allowed (except qnva)	-	-
B5HN	HVNWELL without PWBLK is not allowed Note: Valid outside DNWELL/DNWELLMV/HNW.	-	-
B7HN	HVNWELL overlap of DNWELL is not allowed Note: Valid inside DNWELLMV.	-	-
B4HN	DIFF crossing HVNWELL edge is not allowed (except ped#, pmma, nmma, pm#, ph#, pma)	-	-
B6HN	HVNWELL crossing DNWELL edge is not allowed	-	-
W1HN	Minimum HVNWELL width	0.9	μm
S1HN	Minimum HVNWELL spacing/notch	0.6	μm
S2HN	Minimum HVNWELL spacing (different net) Note: Valid outside DNWELL/DNWELLMV/HNW.	7.0	μm
S1HNDN	Minimum HVNWELL spacing to NDIFF	0.43	μm
S1HNHP	Minimum HVNWELL spacing to HVPWELL (except ped#, pmma, nmma, qpvascr, qpvhbscr) Note: Valid outside of DNWELLMV.	3.0	μm
S1HNNW	Minimum HVNWELL spacing to NWELL	3.0	μm
S2HNDN	Minimum HVNWELL spacing to NDIFF Note: Valid outside DNWELL/DNWELLMV/HNW.	3.43	μm
S2HNHP	Minimum HVNWELL spacing to HVPWELL Note: Valid inside DNWELLMV.	0.8	μm
E1HNDN	Minimum HVNWELL enclosure of NDIFF (except qnva)	0.12	μm
E1HNDP	Minimum HVNWELL enclosure of PDIFF	0.43	μm
E1PBHN	Fixed PWBLK enclosure of HVNWELL (except nmma) Note: Valid outside DNWELL/DNWELLMV/HNW.	3.0	μm
E2HNDN	Minimum HVNWELL enclosure of NDIFF Note: Valid outside DNWELL/DNWELLMV/HNW.	0.43	μm

3. Layer and Device rules → 3.43 ESDPNP module → 3.43.1 Layer rules → HVNWELL

**Figure 3.224** HVNWELL

3. Layer and Device rules → 3.43 ESDPNP module→ 3.43.1 Layer rules→ HVPWELL

HVPWELL

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1HP	HVPWELL must be contacted by PDIFF	-	-
B3HP	HVPWELL overlap of NWELL is not allowed	-	-
B5HP	HVPWELL overlap of DNWELL is not allowed Note: Valid inside DNWELLMV.	-	-
B2HP	DIFF crossing HVPWELL edge is not allowed (except ped, ned#, nm#, nh#, pmma, nmma)	-	-
B4HP	HVPWELL crossing DNWELL edge is not allowed	-	-
W1HP	Minimum HVPWELL width	0.9	μm
S1HP	Minimum HVPWELL spacing/notch	0.6	μm
S2HP	Minimum HVPWELL spacing (different net) Note: Not valid for channel region of pmma GATE (oversized by 0.43 μm).	3.0	μm
S1HPDN	Minimum HVPWELL spacing to NDIFF (except ned#)	0.43	μm
S1HPDP	Minimum HVPWELL spacing to PDIFF	0.43	μm
S1HPNW	Minimum HVPWELL spacing to NWELL Note: Valid inside DNWELLMV.	0.8	μm
S2HPDN	Fixed HVPWELL spacing to NDIFF (except ned#, ped#, qpvascr) Note: Valid inside DNWELL and NOT DNWELLMV.	3.0	μm
S2HPNW	Minimum HVPWELL spacing to NWELL Note: Valid inside DNWELL and NOT DNWELLMV.	3.0	μm
E1HPDN	Minimum HVPWELL enclosure of NDIFF	0.43	μm
E1HPDP	Minimum HVPWELL enclosure of PDIFF (except ped#, pmma, nmma) Note: Valid inside DNWELLMV/DNWELL.	0.43	μm

3. Layer and Device rules → 3.43 ESDPNP module → 3.43.1 Layer rules → HVPWELL

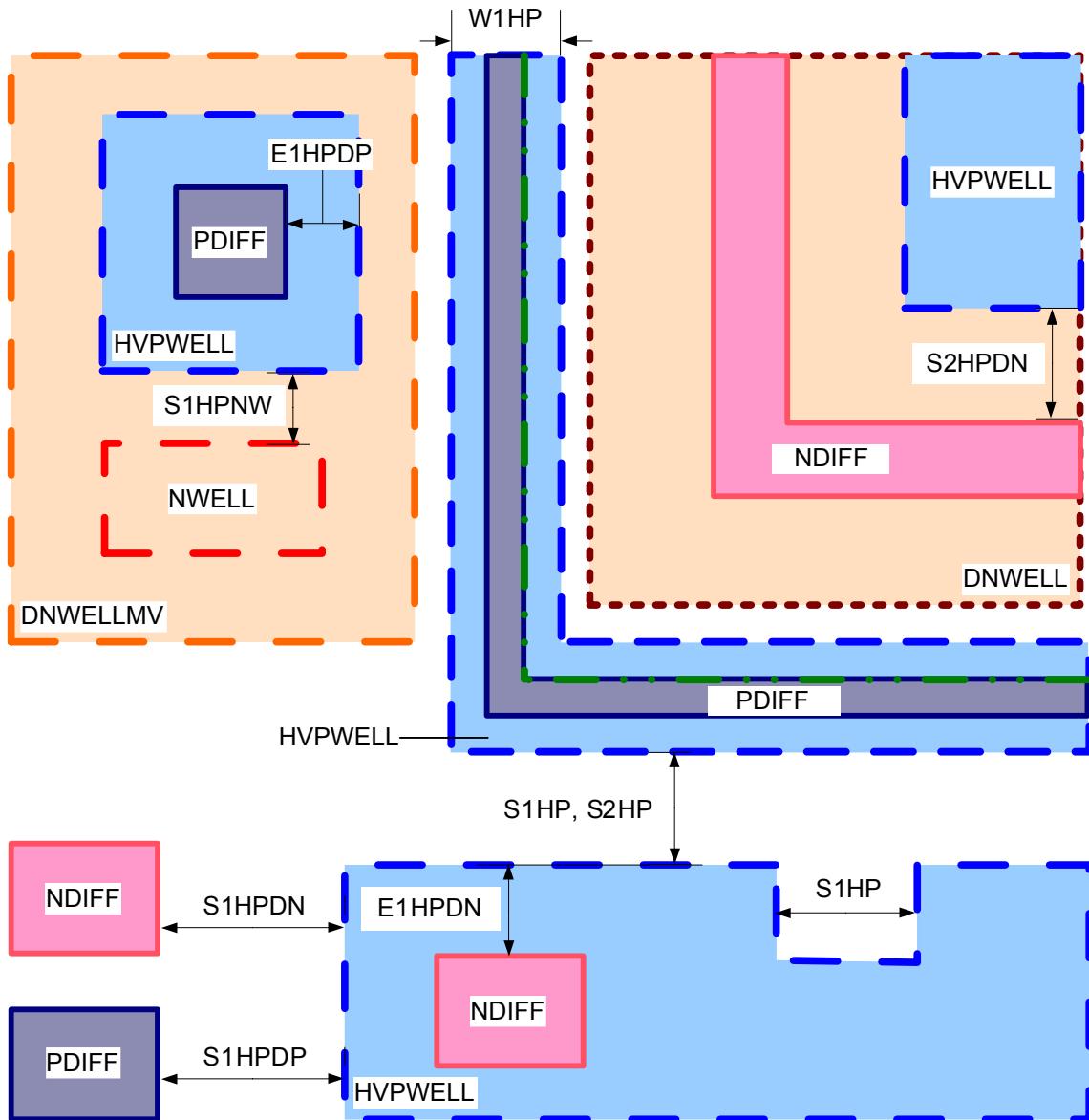


Figure 3.225 HVPWELL

3. Layer and Device rules → 3.43 ESDPNP module → 3.43.2 Device rules → qpvhbscr

3.43.2 Device rules

qpvhbscr

Note: The layout of the qpvhbscr vertical bipolar PNP transistor is pre-defined and only the emitter length can be changed in the range of 12 μ m to 150 μ m. Device qpvhbscr has a fixed emitter width of 6.7 μ m. The drawing below is a basic sketch only and does not show all details.

3. Layer and Device rules → 3.43 ESDPNP module → 3.43.2 Device rules → qpvhbscr

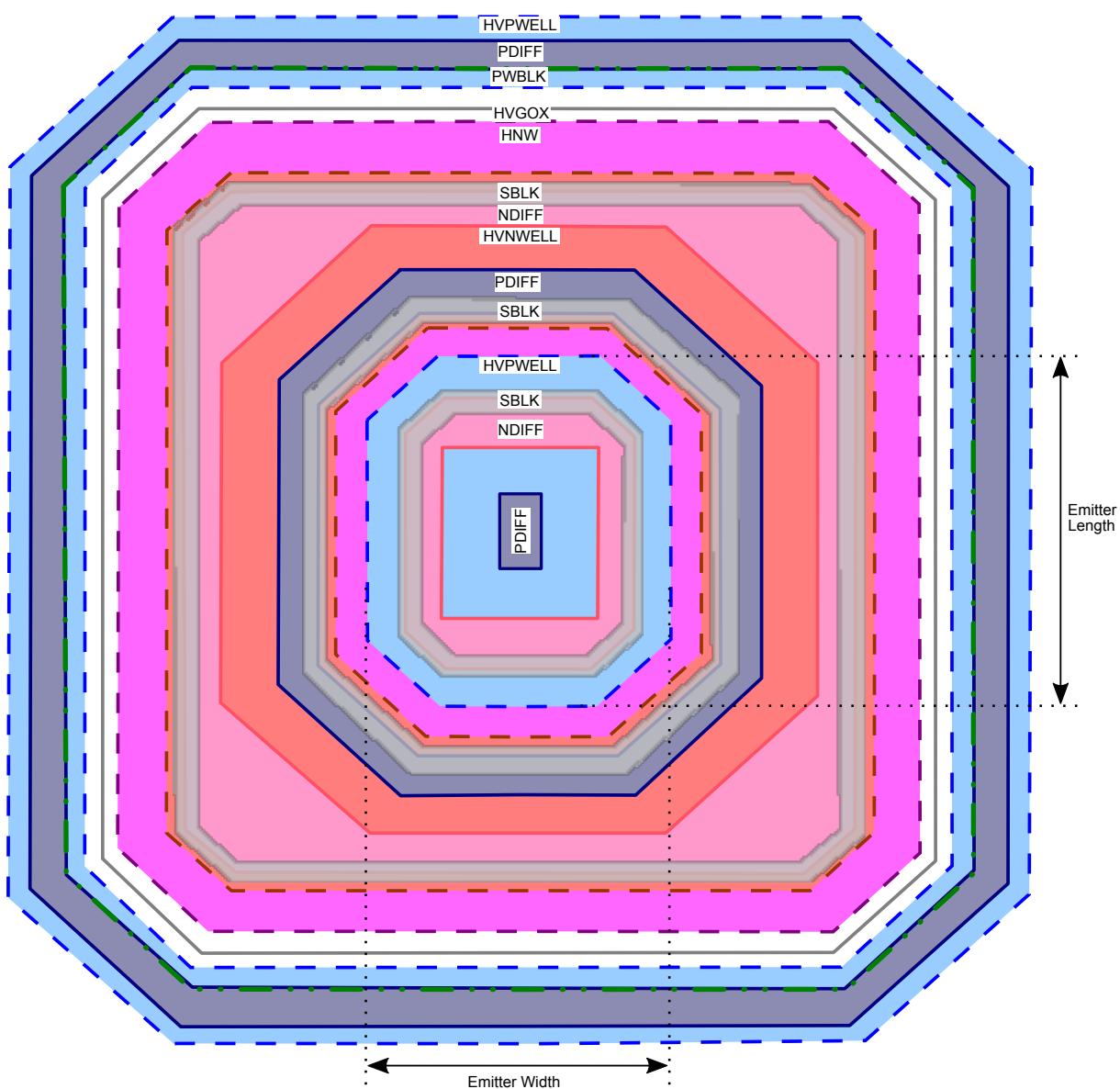
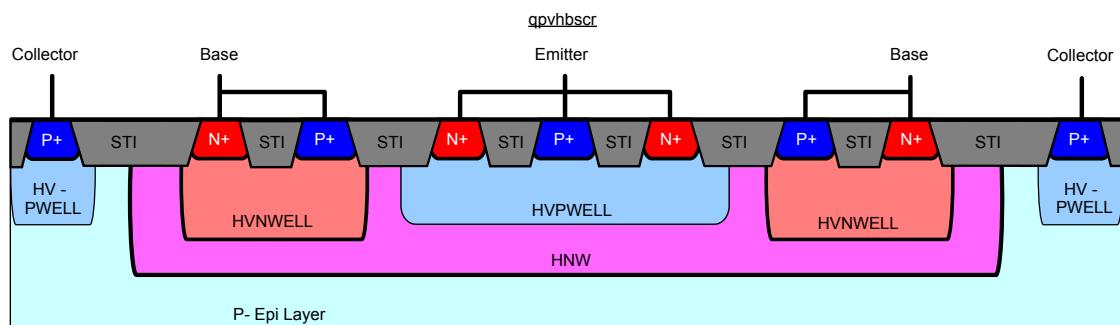


Figure 3.226 qpvhbscr

3. Layer and Device rules → 3.44 FLATPV module

3.44 FLATPV module

For the FLATPV module, a planar passivation layer is offered as an alternative to the standard passivation, which is non-planar. The passivation thickness above the top metal layer is unchanged, refer to parameter THV. This alternative passivation scheme may be suitable for post-processing or packaging solutions requiring planar passivation. Primitive devices are not defined for the FLATPV module.

3. Layer and Device rules → 3.45 SFLATPV module

3.45 SFLATPV module

For the SFLATPV module, a smooth and planar passivation layer is offered as an alternative to the standard passivation, which is non-planar. The passivation thickness above the top metal layer is unchanged, refer to parameter THV. This alternative passivation scheme is preferable for optical applications, with post processing steps, that need to rely on optical grade (polished) interface quality. Primitive devices are not defined for the SFLATPV module.

3. Layer and Device rules → 3.46 PIMIDE module

3.46 PIMIDE module

3.46.1 Layer rules

NOPIM

The layer NOPIM defines areas which are not covered by polyimide. PAD areas are realized by default as areas without polyimide according to the mask generation procedure (layer area including PAD + sizing).

Name	Description	Value	Unit
W1IB	Minimum NOPIM width	60.0	µm
S1IB	Minimum NOPIM spacing/notch	20.0	µm
S1IBPA	Minimum NOPIM spacing to PAD	40.0	µm

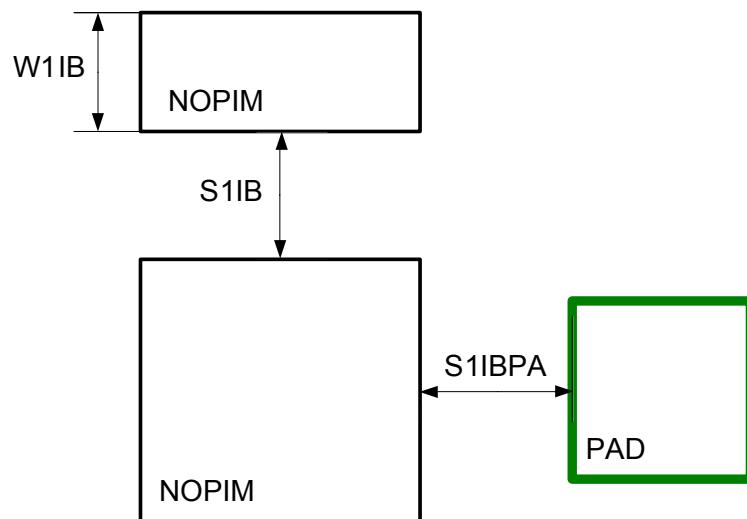


Figure 3.227 NOPIM

3. Layer and Device rules → 3.47 PHOTODIO module

3.47 PHOTODIO module

3.47.1 Device rules

dphoa, dphob

Name	Description	Value	Unit
B1SB	SBLK overlap of MET1, MET2, MET3, MET4, MET5, METTP or METTPL is not allowed	-	-
B2SB	SBLK without BLKALL is not allowed	-	-
E1BASB	Minimum BLKALL enclosure of SBLK	1.7	µm

Note: The layer PHODEF must enclose the pn junction, crossing the pn junction is not allowed.

Note: The third terminal defines the light power input. It must be marked with text in the layer PHODEF (TEXT) which has to be placed on top of DNWELLMV area in top level layout.

Note: The layout of the dphoa and dphob photodiodes are predefined and only Width and Length can be changed in the range of 10µm and 500µm. The other rules support the fixed dimensions of the layout or describe the relation to adjacent structures.

3. Layer and Device rules → 3.47 PHOTODIO module→ 3.47.1 Device rules→ dphoa, dphob

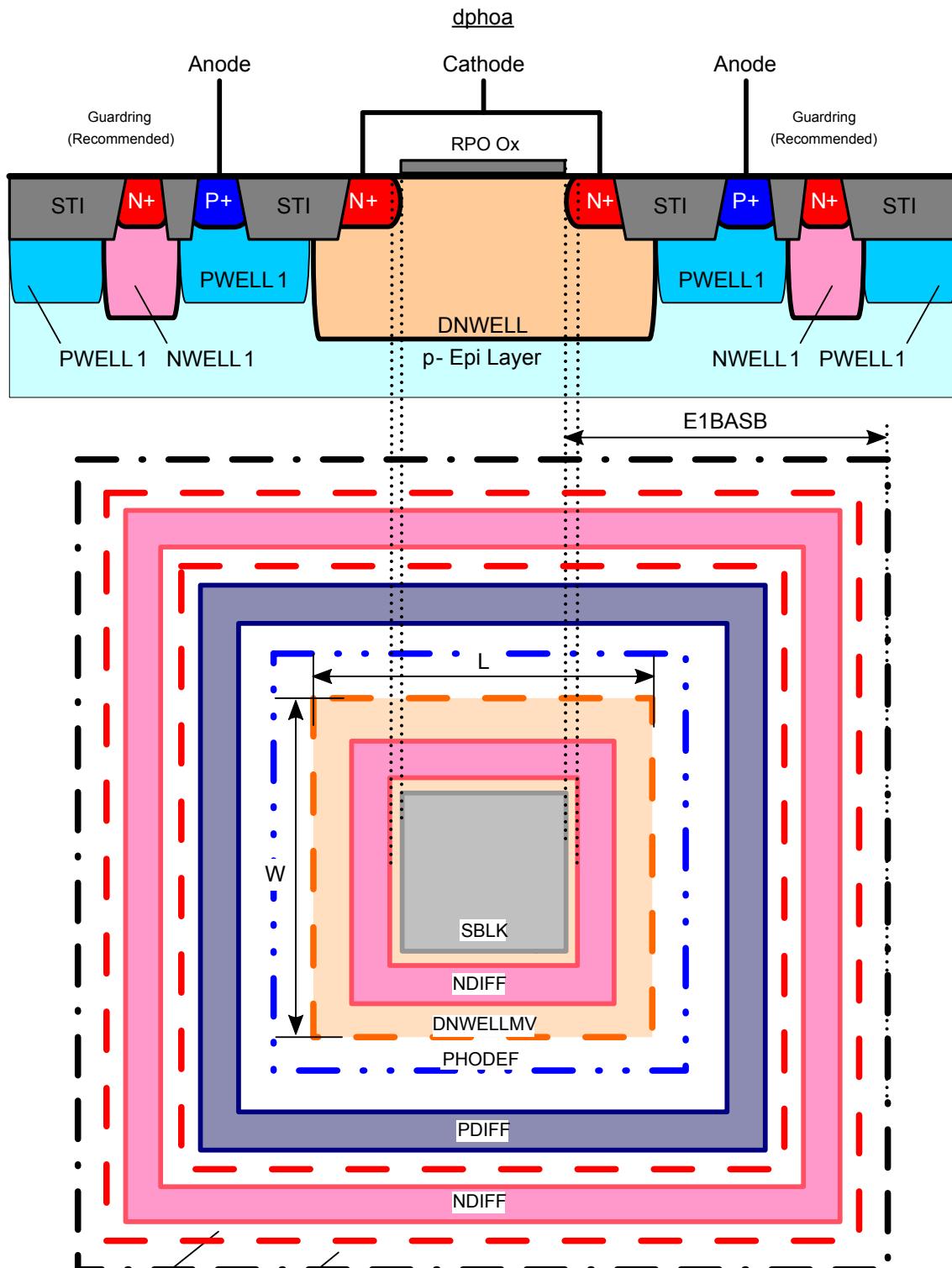


Figure 3.228 dphoa

3. Layer and Device rules → 3.47 PHOTODIO module→ 3.47.1 Device rules→ dphoa, dphob

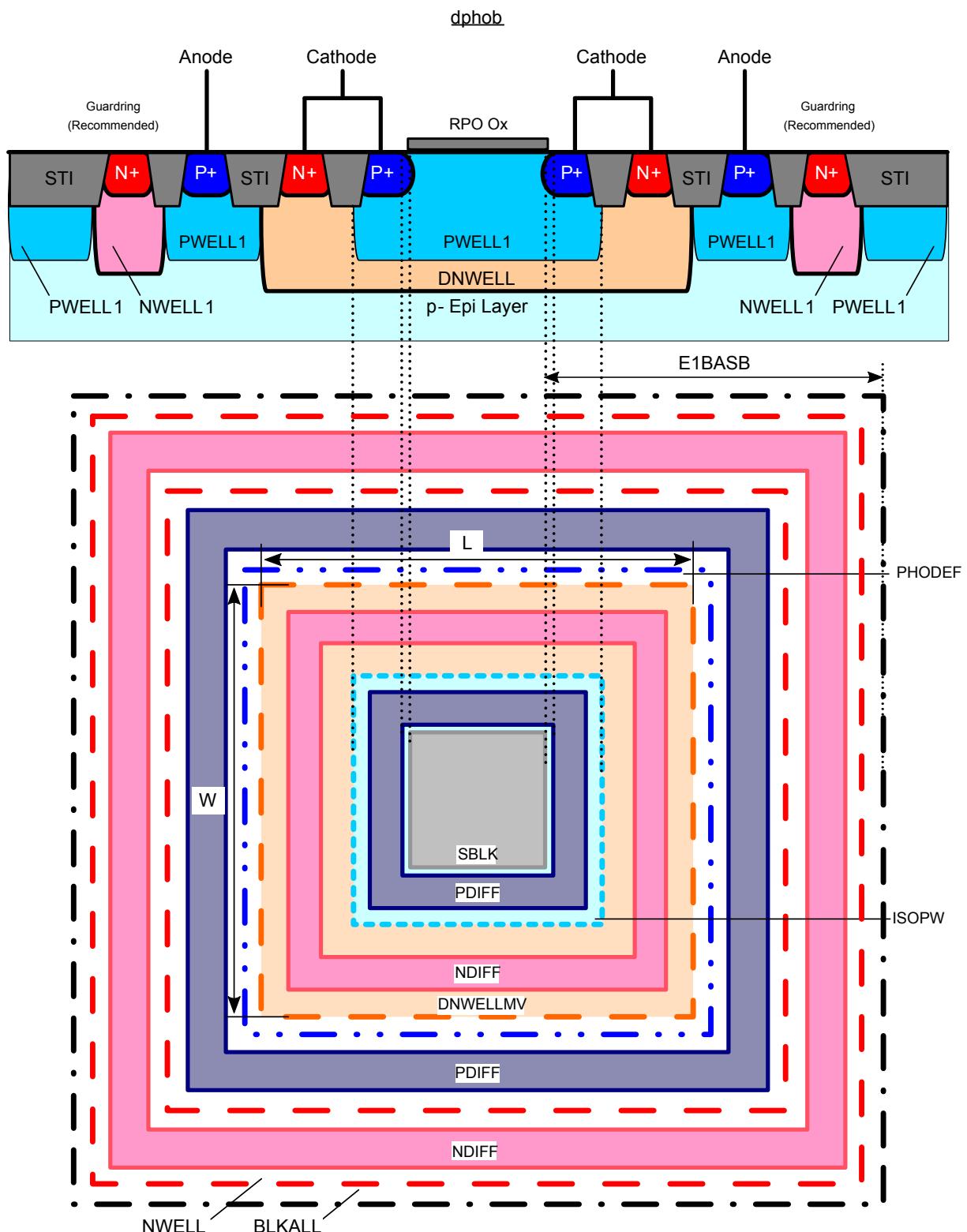


Figure 3.229 dphob

3. Layer and Device rules → 3.48 HALL module

3.48 HALL module

The HALL module delivers a ready-to-use Hall primitive device. No further device or layer rule for this module is described in this specification.

3.48.1 Layer rules

DPC

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
BDPC	Not allowed to be used by customers Note: Except for predefined devices. Reserved layer.	-	-

4. Periphery rules

4. Periphery rules

4.1 Layer rules

PAD

Name	Description	Value	Unit
B1PA	PAD without METTP is not allowed Note: Valid if METMID module is selected and METTHK module is not selected.	-	-
B4PA	PAD without METTPL is not allowed Note: Valid if METTHK module is selected.	-	-
W1PA	Minimum PAD width	15.0	µm
S1PA	Minimum PAD spacing/notch	7.0	µm
E1MLPA	Minimum METTPL enclosure of PAD Note: Valid if METTHK module is selected.	2.0	µm
E2MTPA	Minimum METTP enclosure of PAD Note: Valid if METMID module is selected and METTHK module is not selected.	2.0	µm

Note: Marking of PAD:

The following PAD types must be marked with text on the layer PAD (VERIFICATION):
 customer specific PAD with text "USERPAD"
 Circuit-Under-Pad Bond PAD with text "CUPAD"
 probe PAD with text "PROBEPAD"

If they have either no text or different text labels to those listed above, bond PAD rules will be used for checking the pad.

Important Notes:

The responsibility is wholly on the customer to agree with the assembly requirements of the assembly house used. Customer specific pad layouts are only checked with the rules of this section "PAD". The rules of this section are to ensure the correct preparation of openings in layer PAD within the wafer process. They do not include any considerations related to other layers, devices or to the assembly process employed.

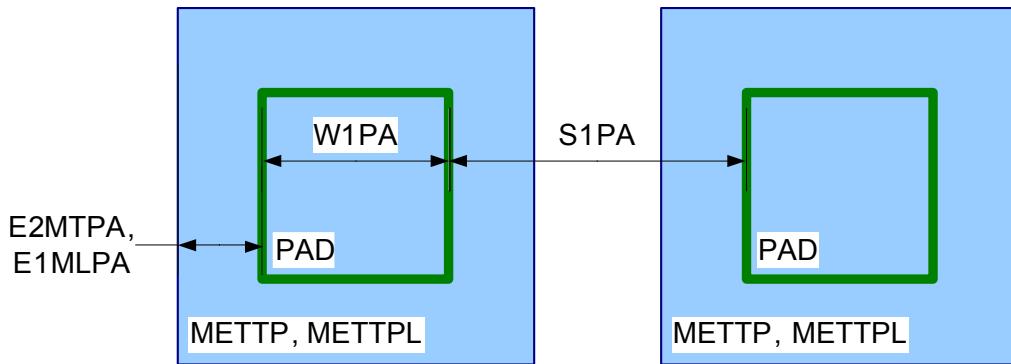
Customers must ensure that any extra requirements are satisfied, as X-FAB Semiconductor Foundries will take no responsibility for such items. For example:

- placing of further layers under PAD;
- placing of primitive devices under PAD;
- PAD spacing to any unrelated structures;
- assembly process influences;
- assembly design rules of the assembly house used;
- the needs of special assembly technologies (e.g. bumping, flip-chip, multi-die packaging).

Additional rules apply for bond pads and probe pads - see relevant sections.

If such items are used for Circuit-Under-Pad Bond Pad the customer is responsible for the qualification of the bond pad.

4. Periphery rules → 4.1 Layer rules→ PAD

**Figure 4.1** PAD

4. Periphery rules → 4.2 Pad-type rules

4.2 Pad-type rules

4 Metal METMID Circuit-Under-Pad Bond Pad

The following bond pad stacking for circuitry underneath bond pads applies when:

MET3 + METMID	MET3 / VIATP / METTP
MET4 + METMID	MET4 / VIATP / METTP
MET5 + METMID	MET5 / VIATP / METTP
METTHK	METTPL

Note: Rules are only appropriate to the modules which contain the relevant layers, as outlined above.

Name	Description	Value	Unit
E3M3PA	Minimum MET3 enclosure of PAD	2.0	µm
E6M3VT	Minimum MET3 enclosure of VIATP Note: VIA rules are related to all VIAs inside PAD regions extended by 2µm.	3.0	µm
E6MTVT	Minimum METTP enclosure of VIATP Note: VIA rules are related to all VIAs inside PAD regions extended by 2µm.	3.0	µm
R2VTPA	Minimum ratio of VIATP (in pad) area to PAD area	5.0	%
Q3PA	Minimum recommended PAD width	66.0	µm

Note: Circuit-Under-Pad bond pads allow non-critical circuitry underneath bond pads, as ESD structures or output drivers. For advice regarding the use of Circuit-Under-Pad bond pads within IC designs (regarding the handling of Circuit-Under-Pad bond pads during assembly etc) please refer to the [Application Note](#) available at "my X-FAB". Similarly, for reliability data for Circuit-Under-Pad bond pads please refer to the respective 'Bond Test Report'.

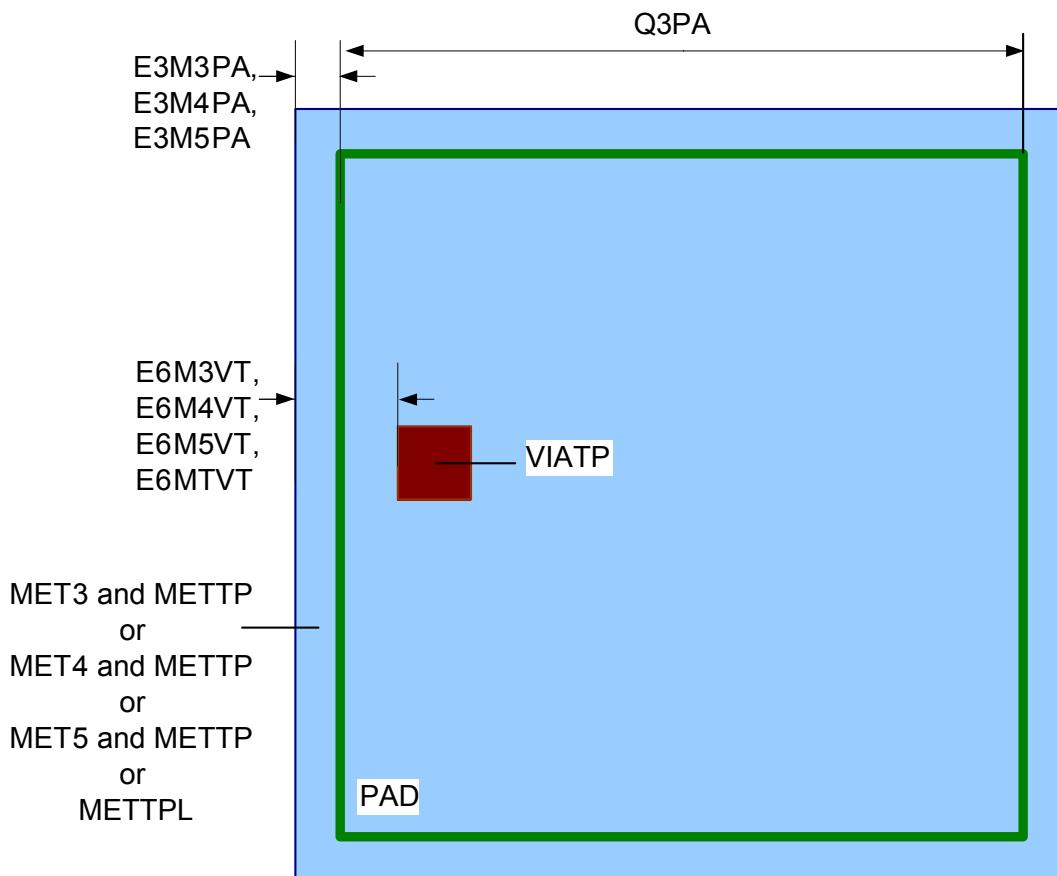


Figure 4.2 Circuit Under Pad

4. Periphery rules → 4.2 Pad-type rules → 5 Metal METMID + MET...

5 Metal METMID + METTHK Circuit-Under-Pad Bond Pad

The following bond pad stacking for circuitry underneath bond pads applies when:

MET3 + METMID	MET3 / VIATP / METTP
MET4 + METMID	MET4 / VIATP / METTP
MET5 + METMID	MET5 / VIATP / METTP
METTHK	METTPL

Note: Rules are only appropriate to the modules which contain the relevant layers, as outlined above.

Name	Description	Value	Unit
E3M3PA	Minimum MET3 enclosure of PAD	2.0	µm
E6M3VT	Minimum MET3 enclosure of VIATP	3.0	µm
	Note: VIA rules are related to all VIAs inside PAD regions extended by 2µm.		
E6MTVT	Minimum METTP enclosure of VIATP	3.0	µm
	Note: VIA rules are related to all VIAs inside PAD regions extended by 2µm.		
R2VTPA	Minimum ratio of VIATP (in pad) area to PAD area	5.0	%
Q3PA	Minimum recommended PAD width	66.0	µm

Note: Circuit-Under-Pad bond pads allow non-critical circuitry underneath bond pads, as ESD structures or output drivers. For advice regarding the use of Circuit-Under-Pad bond pads within IC designs (regarding the handling of Circuit-Under-Pad bond pads during assembly etc) please refer to the [Application Note](#) available at "my X-FAB". Similarly, for reliability data for Circuit-Under-Pad bond pads please refer to the respective 'Bond Test Report'.

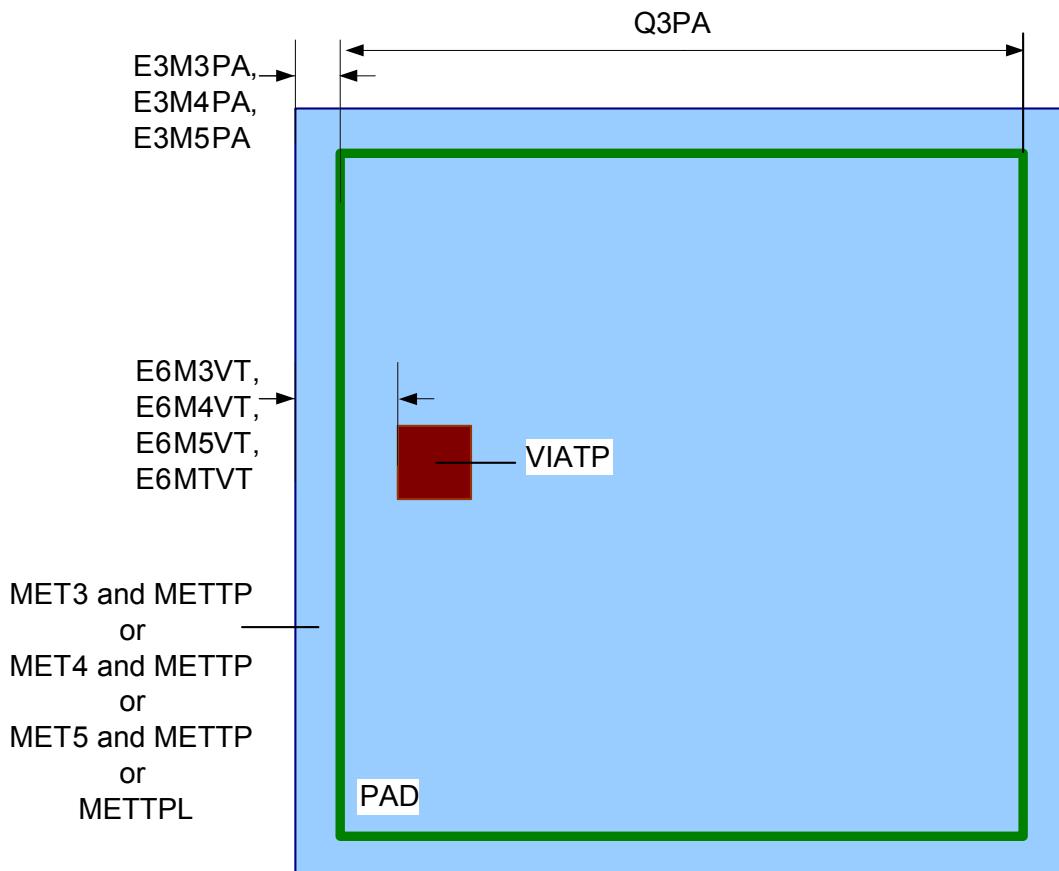


Figure 4.3 Circuit Under Pad

4. Periphery rules → 4.2 Pad-type rules→ 5 Metal METMID Circu...

5 Metal METMID Circuit-Under-Pad Bond Pad

The following bond pad stacking for circuitry underneath bond pads applies when:

MET3 + METMID	MET3 / VIATP / METTP
MET4 + METMID	MET4 / VIATP / METTP
MET5 + METMID	MET5 / VIATP / METTP
METTHK	METTPL

Note: Rules are only appropriate to the modules which contain the relevant layers, as outlined above.

Name	Description	Value	Unit
E3M3PA	Minimum MET3 enclosure of PAD	2.0	µm
E3M4PA	Minimum MET4 enclosure of PAD	2.0	µm
E6M4VT	Minimum MET4 enclosure of VIATP	3.0	µm
	Note: VIA rules are related to all VIAs inside PAD regions extended by 2µm.		
E6MTVT	Minimum METTP enclosure of VIATP	3.0	µm
	Note: VIA rules are related to all VIAs inside PAD regions extended by 2µm.		
R2VTPA	Minimum ratio of VIATP (in pad) area to PAD area	5.0	%
Q3PA	Minimum recommended PAD width	66.0	µm

Note: Circuit-Under-Pad bond pads allow non-critical circuitry underneath bond pads, as ESD structures or output drivers. For advice regarding the use of Circuit-Under-Pad bond pads within IC designs (regarding the handling of Circuit-Under-Pad bond pads during assembly etc) please refer to the [Application Note](#) available at "my X-FAB". Similarly, for reliability data for Circuit-Under-Pad bond pads please refer to the respective 'Bond Test Report'.

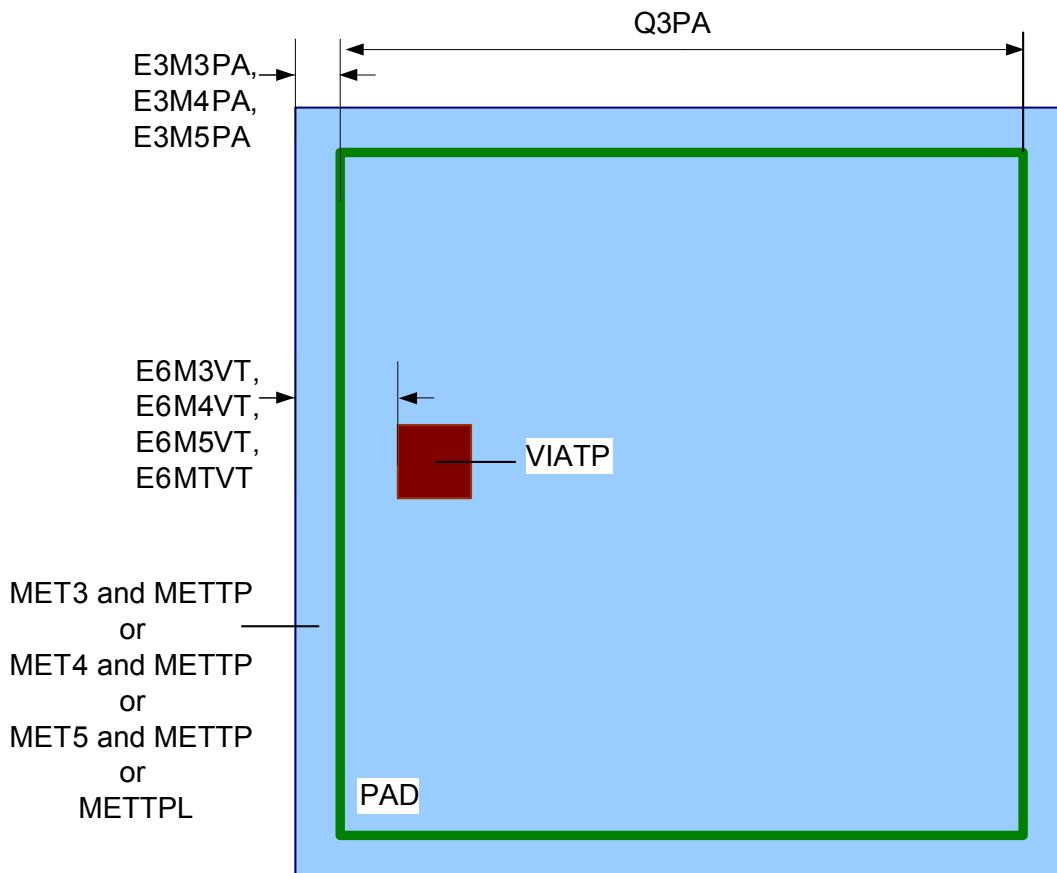


Figure 4.4 Circuit Under Pad

4. Periphery rules → 4.2 Pad-type rules→ 6 Metal METMID + MET...

6 Metal METMID + METTHK Circuit-Under-Pad Bond Pad

The following bond pad stacking for circuitry underneath bond pads applies when:

MET3 + METMID	MET3 / VIATP / METTP
MET4 + METMID	MET4 / VIATP / METTP
MET5 + METMID	MET5 / VIATP / METTP
METTHK	METTPL

Note: Rules are only appropriate to the modules which contain the relevant layers, as outlined above.

Name	Description	Value	Unit
E3M3PA	Minimum MET3 enclosure of PAD	2.0	µm
E3M4PA	Minimum MET4 enclosure of PAD	2.0	µm
E3M5PA	Minimum MET5 enclosure of PAD	2.0	µm
E6M4VT	Minimum MET4 enclosure of VIATP Note: VIA rules are related to all VIAs inside PAD regions extended by 2µm.	3.0	µm
E6MTVT	Minimum METTP enclosure of VIATP Note: VIA rules are related to all VIAs inside PAD regions extended by 2µm.	3.0	µm
R2VTPA	Minimum ratio of VIATP (in pad) area to PAD area	5.0	%
Q3PA	Minimum recommended PAD width	66.0	µm

Note: Circuit-Under-Pad bond pads allow non-critical circuitry underneath bond pads, as ESD structures or output drivers. For advice regarding the use of Circuit-Under-Pad bond pads within IC designs (regarding the handling of Circuit-Under-Pad bond pads during assembly etc) please refer to the [Application Note](#) available at "my X-FAB". Similarly, for reliability data for Circuit-Under-Pad bond pads please refer to the respective 'Bond Test Report'.

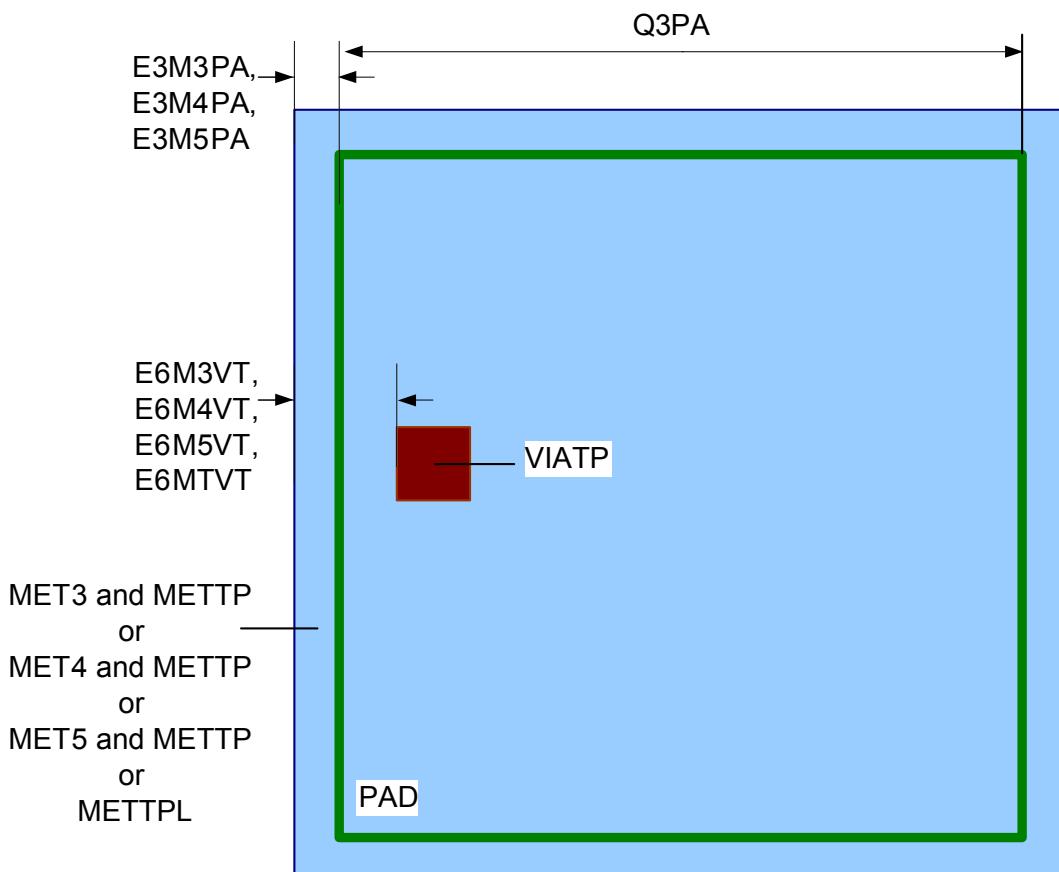


Figure 4.5 Circuit Under Pad

4. Periphery rules → 4.2 Pad-type rules→ 6 Metal METMID Circu...

6 Metal METMID Circuit-Under-Pad Bond Pad

The following bond pad stacking for circuitry underneath bond pads applies when:

MET3 + METMID	MET3 / VIATP / METTP
MET4 + METMID	MET4 / VIATP / METTP
MET5 + METMID	MET5 / VIATP / METTP
METTHK	METTPL

Note: Rules are only appropriate to the modules which contain the relevant layers, as outlined above.

Name	Description	Value	Unit
E3M3PA	Minimum MET3 enclosure of PAD	2.0	µm
E3M4PA	Minimum MET4 enclosure of PAD	2.0	µm
E6M5VT	Minimum MET5 enclosure of VIATP	3.0	µm
	Note: VIA rules are related to all VIAs inside PAD regions extended by 2µm.		
E6MTVT	Minimum METTP enclosure of VIATP	3.0	µm
	Note: VIA rules are related to all VIAs inside PAD regions extended by 2µm.		
R2VTPA	Minimum ratio of VIATP (in pad) area to PAD area	5.0	%
Q3PA	Minimum recommended PAD width	66.0	µm

Note: Circuit-Under-Pad bond pads allow non-critical circuitry underneath bond pads, as ESD structures or output drivers. For advice regarding the use of Circuit-Under-Pad bond pads within IC designs (regarding the handling of Circuit-Under-Pad bond pads during assembly etc) please refer to the [Application Note](#) available at "my X-FAB". Similarly, for reliability data for Circuit-Under-Pad bond pads please refer to the respective 'Bond Test Report'.

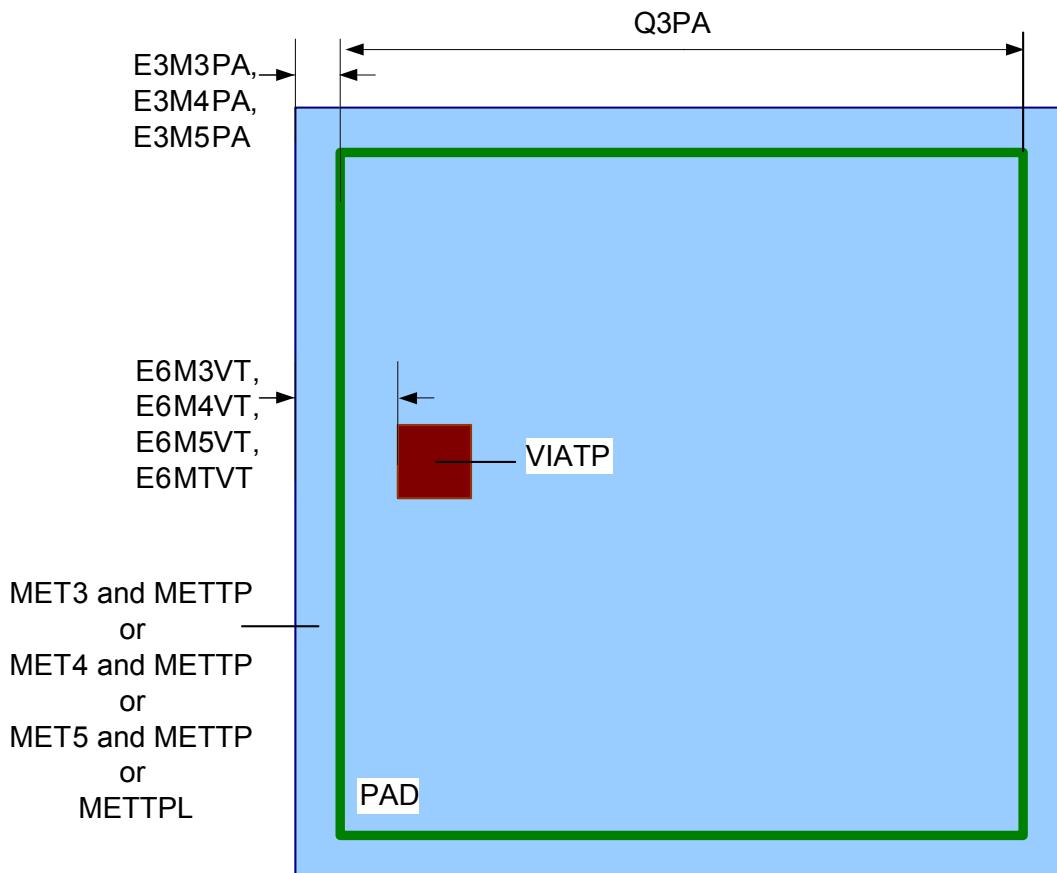


Figure 4.6 Circuit Under Pad

4. Periphery rules → 4.2 Pad-type rules → 4 Metal METMID Bond ...

4 Metal METMID Bond Pad, 5 Metal METMID + METTHK Bond Pad, 5 Metal METMID Bond Pad, 6 Metal METMID + METTHK Bond Pad, 6 Metal METMID Bond Pad

The bond pad stack is defined as follows:

Module	Bond Pad stack
LPMOS	MET1 / VIA1 / MET2 / VIA2 / MET3 / VIATP / METTP
MET3 with METTHK	MET1 / VIA1 / MET2 / VIA2 / MET3 / VIATP / METTP / VIATPL / METTPL
MET4	MET1 / VIA1 / MET2 / VIA2 / MET3 / VIA3 / MET4 / VIATP / METTP
MET4 with METTHK	MET1 / VIA1 / MET2 / VIA2 / MET3 / VIA3 / MET4 / VIATP / METTP / VIATPL / METTPL
MET5	MET1 / VIA1 / MET2 / VIA2 / MET3 / VIA3 / MET4 / VIA4 / MET5 / VIATP / METTP

Name	Description	Value	Unit
B2PA	PAD overlap of DIFF or POLY1 is not allowed Note: Not valid for DIFFDUMMY and P1DUMMY.	-	-
S2V1	Minimum VIA1 spacing Note: VIA rules are related to all VIAs inside PAD regions extended by 2µm.	0.45	µm
S2V2	Minimum VIA2 spacing Note: VIA rules are related to all VIAs inside PAD regions extended by 2µm.	0.45	µm
S2V3	Minimum VIA3 spacing Note: VIA rules are related to all VIAs inside PAD regions extended by 2µm.	0.45	µm
S2V4	Minimum VIA4 spacing Note: VIA rules are related to all VIAs inside PAD regions extended by 2µm.	0.45	µm
S1PADF	Minimum PAD spacing to DIFF Note: Not valid for DIFFDUMMY.	5.0	µm
S1PAM1	Minimum PAD spacing to MET1 (different net)	5.0	µm
S1PAM2	Minimum PAD spacing to MET2 (different net)	5.0	µm
S1PAM3	Minimum PAD spacing to MET3 (different net)	5.0	µm
S1PAM4	Minimum PAD spacing to MET4 (different net)	5.0	µm
S1PAM5	Minimum PAD spacing to MET5 (different net)	5.0	µm
S1PAML	Minimum PAD spacing to METTPL (different net)	5.0	µm
S1PAMT	Minimum PAD spacing to METTP (different net)	5.0	µm
S1PAP1	Minimum PAD spacing to POLY1 Note: Not valid for P1DUMMY.	5.0	µm
S1V2V1	Minimum VIA2 spacing to VIA1 Note: VIA rules are related to all VIAs inside PAD regions extended by 2µm. Note: VIA2 stacking over VIA1 is not allowed.	0.13	µm
S1V3V2	Minimum VIA3 spacing to VIA2 Note: VIA rules are related to all VIAs inside PAD regions extended by 2µm. Note: VIA3 stacking over VIA2 is not allowed.	0.13	µm
S1V4V3	Minimum VIA4 spacing to VIA3 Note: VIA rules are related to all VIAs inside PAD regions extended by 2µm. Note: VIA4 stacking over VIA3 is not allowed.	0.13	µm
S1VTV2	Minimum VIATP spacing to VIA2 Note: VIA rules are related to all VIAs inside PAD regions extended by 2µm. Note: VIATP stacking over VIA2 is not allowed. Note: Valid if MET4 module is not selected.	0.06	µm



4. Periphery rules → 4.2 Pad-type rules→ 4 Metal METMID Bond ...

Name	Description	Value	Unit
S1VTV3	Minimum VIATP spacing to VIA3	0.06	µm
	Note: VIA rules are related to all VIAs inside PAD regions extended by 2µm.		
	Note: VIATP stacking over VIA3 is not allowed.		
	Note: Valid if MET4 is selected and MET5 module is not selected.		
S1VTV4	Minimum VIATP spacing to VIA4	0.06	µm
	Note: VIA rules are related to all VIAs inside PAD regions extended by 2µm.		
	Note: VIATP stacking over VIA4 is not allowed.		
	Note: Valid if MET5 module is selected.		
E1M1PA	Minimum MET1 enclosure of PAD	2.0	µm
E1M2PA	Minimum MET2 enclosure of PAD	2.0	µm
E1M3PA	Minimum MET3 enclosure of PAD	2.0	µm
E1M4PA	Minimum MET4 enclosure of PAD	2.0	µm
E1M5PA	Minimum MET5 enclosure of PAD	2.0	µm
E1MTPA	Minimum METTP enclosure of PAD	2.0	µm
E2MLVL	Minimum METTPL enclosure of VIATPL	3.0	µm
	Note: VIA rules are related to all VIAs inside PAD regions extended by 2µm.		
E2MTVL	Minimum METTP enclosure of VIATPL	3.0	µm
	Note: VIA rules are related to all VIAs inside PAD regions extended by 2µm.		
E2MTVT	Minimum METTP enclosure of VIATP	3.0	µm
	Note: VIA rules are related to all VIAs inside PAD regions extended by 2µm.		
E3M1V1	Minimum MET1 and MET2 enclosure of VIA1	3.0	µm
	Note: VIA rules are related to all VIAs inside PAD regions extended by 2µm.		
E3M2V2	Minimum MET2 and MET3 enclosure of VIA2	3.0	µm
	Note: VIA rules are related to all VIAs inside PAD regions extended by 2µm.		
E3M3V3	Minimum MET3 and MET4 enclosure of VIA3	3.0	µm
	Note: VIA rules are related to all VIAs inside PAD regions extended by 2µm.		
E3M3VT	Minimum MET3 enclosure of VIATP	3.0	µm
	Note: VIA rules are related to all VIAs inside PAD regions extended by 2µm.		
	Note: Valid if MET4 module is not selected.		
E3M4V4	Minimum MET4 and MET5 enclosure of VIA4	3.0	µm
	Note: VIA rules are related to all VIAs inside PAD regions extended by 2µm.		
E3M4VT	Minimum MET4 enclosure of VIATP	3.0	µm
	Note: VIA rules are related to all VIAs inside PAD regions extended by 2µm.		
	Note: Valid if MET4 is selected and MET5 module is not selected.		
E3M5VT	Minimum MET5 enclosure of VIATP	3.0	µm
	Note: VIA rules are related to all VIAs inside PAD regions extended by 2µm.		
	Note: Valid if MET5 module is selected.		
R1V1PA	Minimum ratio of VIA1 (in pad) area to PAD area	5.0	%
R1V2PA	Minimum ratio of VIA2 (in pad) area to PAD area	5.0	%
R1V3PA	Minimum ratio of VIA3 (in pad) area to PAD area	5.0	%
R1V4PA	Minimum ratio of VIA4 (in pad) area to PAD area	5.0	%
R1VLPA	Minimum ratio of VIATPL (in pad) area to PAD area	5.0	%
R1VTPA	Minimum ratio of VIATP (in pad) area to PAD area	5.0	%
Q1PA	Minimum recommended bond PAD width	53.0	µm

Note: The VIAs should form a diamond shape in the center of the PAD opening.

4. Periphery rules → 4.2 Pad-type rules→ 4 Metal METMID Bond ...

E1M1PA
E1M2PA
E1M3PA
E1M4PA
E1M5PA
E1MTPA
E1MLPA

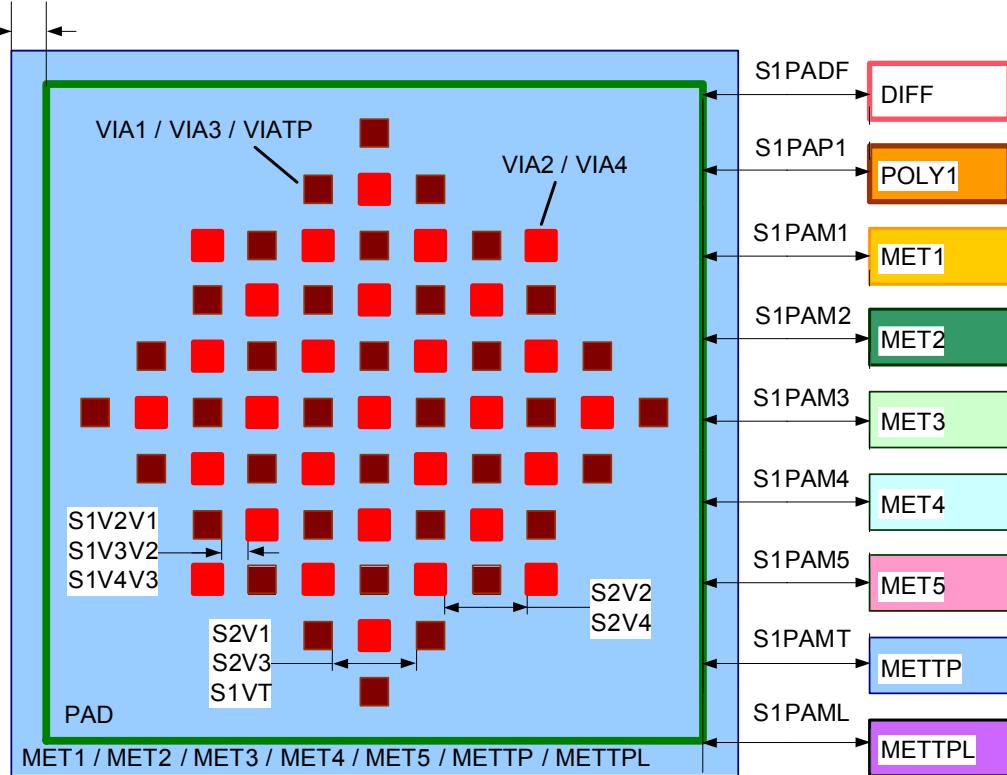


Figure 4.7 Bond Pad

4. Periphery rules → 4.2 Pad-type rules→ Probe Pad

Probe Pad

Name	Description	Value	Unit
B15PA	Probe PAD with VIATPL is not allowed Note: Valid if METTHK module is selected.	-	-
B3PA	Probe PAD with VIATP is not allowed Note: Valid if METTHK module is not selected.	-	-
S1PAVL	Minimum PAD spacing to VIATPL Note: Valid if METTHK module is selected.	2.0	μm
S1PAVT	Minimum PAD spacing to VIATP Note: Valid if METTHK module is not selected.	2.0	μm

Note: The use of probe PAD is on responsibility of the customer.

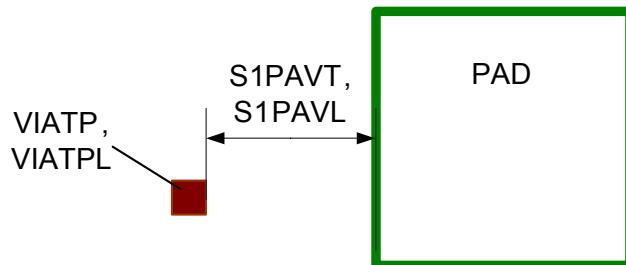


Figure 4.8 Probe Pad

4. Periphery rules → 4.3 Scribe rules

4.3 Scribe rules

Each single die is enclosed with a Peripheral Ring and a Scribe Lane.

By default all the layout data within the peripheral ring is added by X-FAB at the mask tooling stage, unless instruction is given in the SIFO document not to perform this task. In circumstances where the customer adds the peripheral ring by themselves, they should refer to the [Multi-Project Design Guide](#) available at "my X-FAB". This includes sample layout, a seal ring pcell and a dedicated technology file for use with the X-FAB Cadence design kit.

The final chip size is defined as follows:

final chip size = customer chip size + 2 x peripheral ring width + scribe lane width , multiple of 1 μ m

Peripheral Ring

This area contains the seal ring and a protective area without electrical structures. The peripheral ring width is defined as 15 μ m per side.

Scribe Lane

This area contains all structures for controlling, alignment, measurement etc. The single scribe lane width is defined as 80 μ m. Dependent on die size, used process family modules and reticle assembly, a multiple of 80 μ m can be necessary.

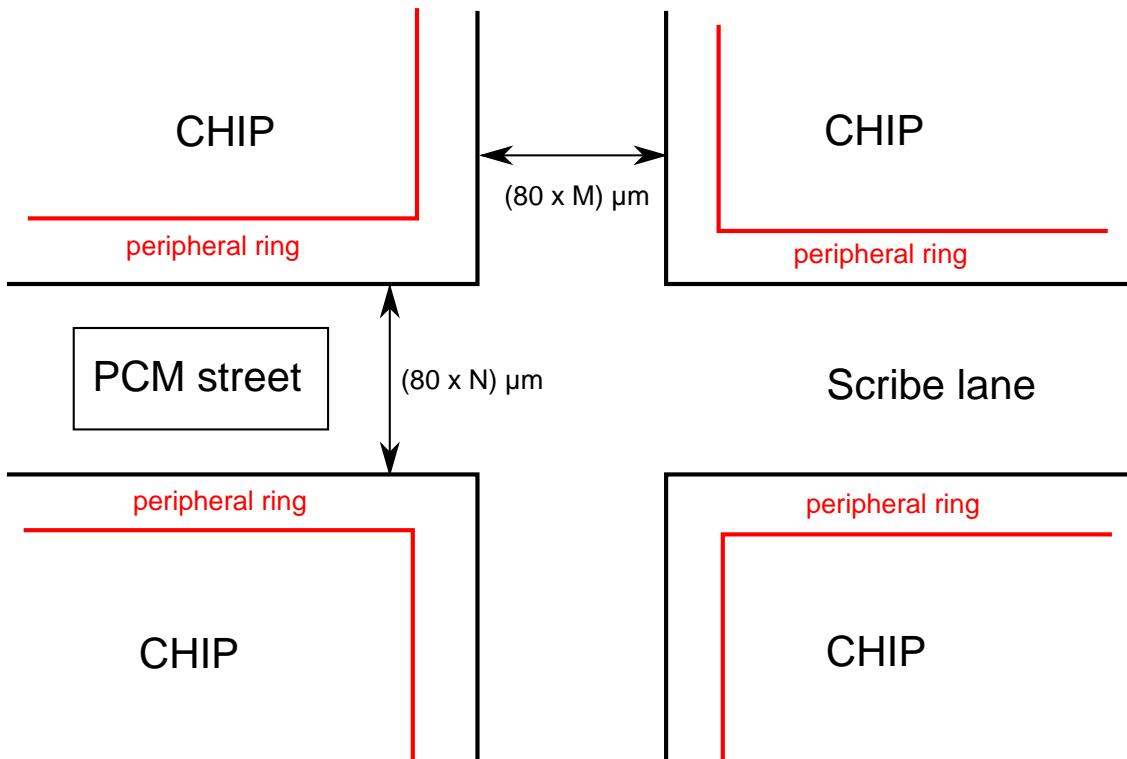


Figure 4.9 final chip size

4. Periphery rules → 4.4 Corner rules

4.4 Corner rules

Name	Description	Value	Unit
<u>B1CB</u>	Active circuitry inside CORNER box is not allowed	-	-
	Note: Only metal power rails and non-circuit structures, such as chip numbers, are allowed in this region.		
<u>W1CB</u>	Minimum CORNER box edge length	35.0	μm
	Note: Valid for a very small chip (EXTENT area size < 1mm ²).		
<u>W2CB</u>	Minimum CORNER box edge length	75.0	μm
	Note: Valid for a small chip (1mm ² <= EXTENT area size < 100mm ²).		
<u>W3CB</u>	Minimum CORNER box edge length	150.0	μm
	Note: Valid for a large chip (EXTENT area size >= 100mm ²).		
<u>S1MTCC</u>	Minimum metal track spacing to chip corner	35.0	μm
	Note: Valid for a very small chip (EXTENT area size < 1mm ²).		
<u>S2MTCC</u>	Minimum metal track spacing to chip corner	75.0	μm
	Note: Valid for a small chip (1mm ² <= EXTENT area size < 100mm ²).		
<u>S3MTCC</u>	Minimum metal track spacing to chip corner	150.0	μm
	Note: Valid for a large chip (EXTENT area size >= 100mm ²).		

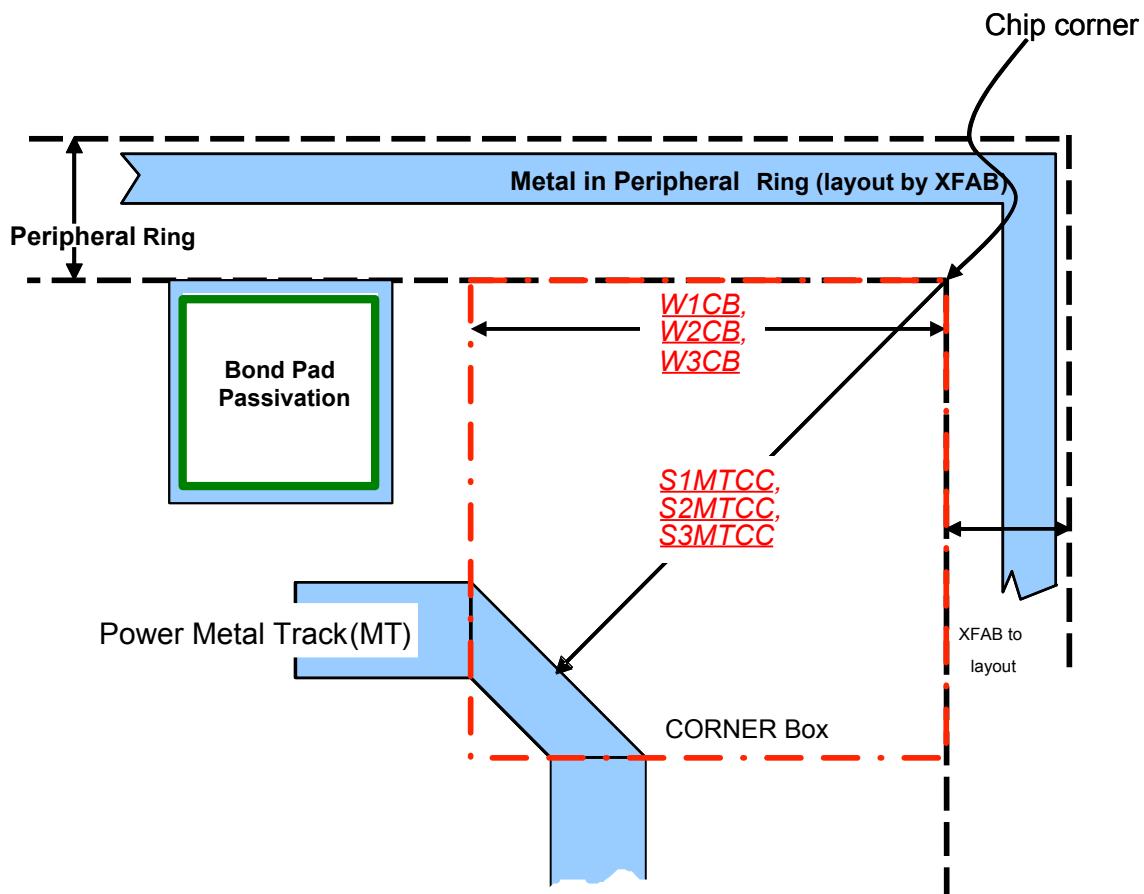


Figure 4.10 Corner Rules

5. Design related guidelines

5. Design related guidelines

5.1 Miscellaneous

It is generally good practice to ensure that as many taps as possible exist on the design, in order to minimize resistive effects on the circuit. Unless used as an active node, all wells must be connected to a power rail using a TAP connection.

For precision analogue devices, it is recommended to use non-minimum geometries. Such devices should not be covered with metal. If this is not possible metal coverage of matching devices should be identical.

For MIM devices stacked to subjacent primitive devices, it is recommended not to use the MIM device or the subjacent primitive devices as precision analogue devices.

The use of redundant contacts and redundant vias is recommended wherever it is possible in the design. Redundant via placement is supported by special functionality within the design kit.

It is strongly recommended to use MET2 or higher metal layers as high-voltage connection instead of MET1.

5. Design related guidelines → 5.2 Antenna Rule definitions

5.2 Antenna Rule definitions

The definition of antenna ration is given by the following equation:

$$Rx = \frac{P \times T}{WP \times LP} = \frac{\text{Metal Sidewall Area}}{\text{Sensitive Surface Area}}$$

Metal Sidewall Area Terms:

- P = floating metal perimeter connected to gate (μm)
- WM = the width of metal (μm)
- LM = the length of metal (μm)
- T = the thickness of metal (μm)

Sensitive Surface Area Terms:

- WP = connected transistor channel width (μm)
- LP = connected transistor channel length (μm)

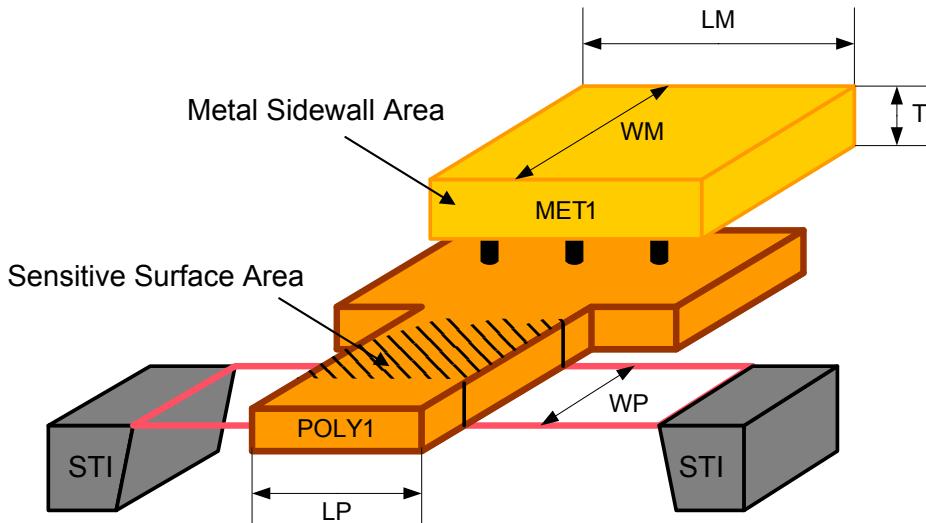
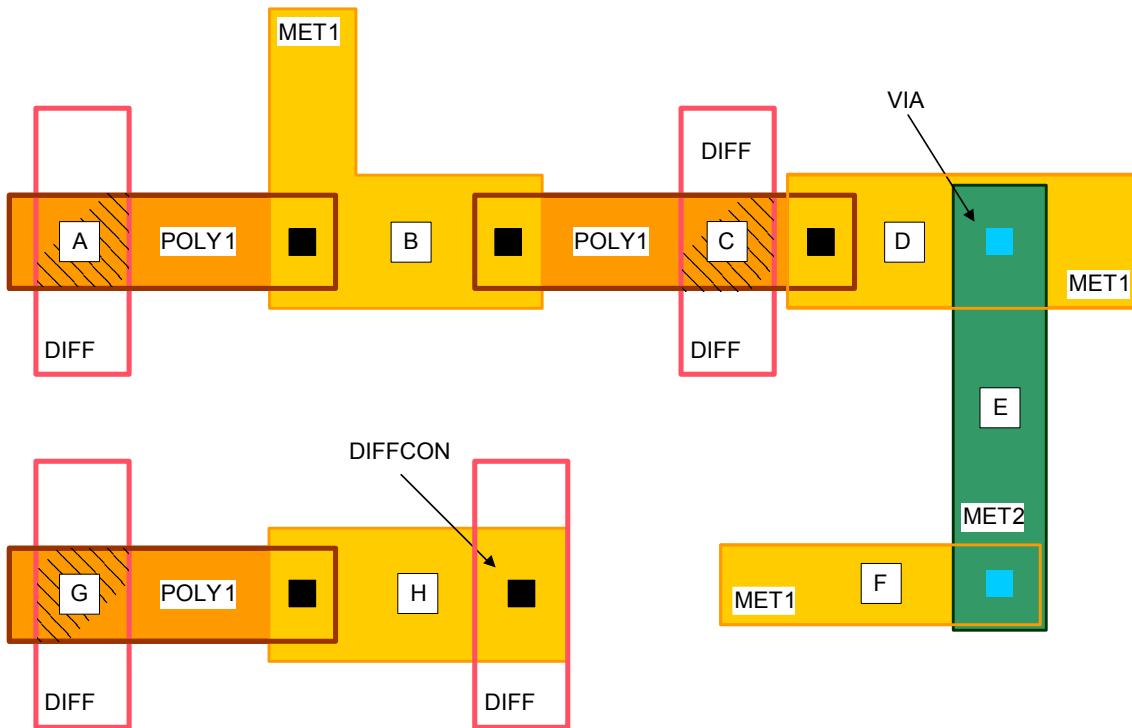


Figure 5.1 Antenna ratio definition (example for MET1)

5. Design related guidelines → 5.2 Antenna Rule definitions

**Figure 5.2** Contributing areas for antenna effects (example for MET1)Antenna ratios:

$$\frac{\text{area}(B + D)}{\text{area}(A + C)}$$

$$\frac{\text{area}(E)}{\text{area}(A + C)}$$

Note: Areas 'F' and 'H' do not contribute to antenna effects.

Note: Metal structures collect electric charge during ion-etching which can be a hazard for associated GATEs. Only metal areas without DIFFCONs must be considered.

MET1 areas connected to GATE via MET2 do not contribute. The similar approach applies to all the metal layers.

Please also refer to the "[Application Note MIM Capacitors](#)" available at "my X-FAB."

5. Design related guidelines → 5.3 NLEAK

5.3 NLEAK

Inversion will occur and a parasitic NLEAK channel will be formed if laterally positioned N-P-N areas are crossed by POLY1 or MET1 over STI and the voltage difference between these crossing lines and the interposed P-area exceeds the corresponding field threshold voltage for that combination. P-area is defined as PSUB or PTYPE_WELL.

Notes:

- For further information, please refer to the appropriate 'Parasitic field parameters' within the Process & Device Specification, or search for 'VTF' parameters in the SpecXplorer.
- Both the case of complete and partial overlap of these P-doped regions by a POLY1 or MET1 line should be considered.
- NLEAK channels can connect NDIFF and NTPYPE_WELL in any combination.
- NLEAK channels cannot be found automatically with verification tools.

The associated NLEAK channel of a field transistor can create unwanted electrical connections between two or more unrelated structures. Without loss of generality the following NLEAK constellations are possible with the XH018 layers. They are given as examples in cross sectional and plan view below. DNWELL stands for DNWELL or DNWELLMV. The gate may consist of POLY1 or MET1.

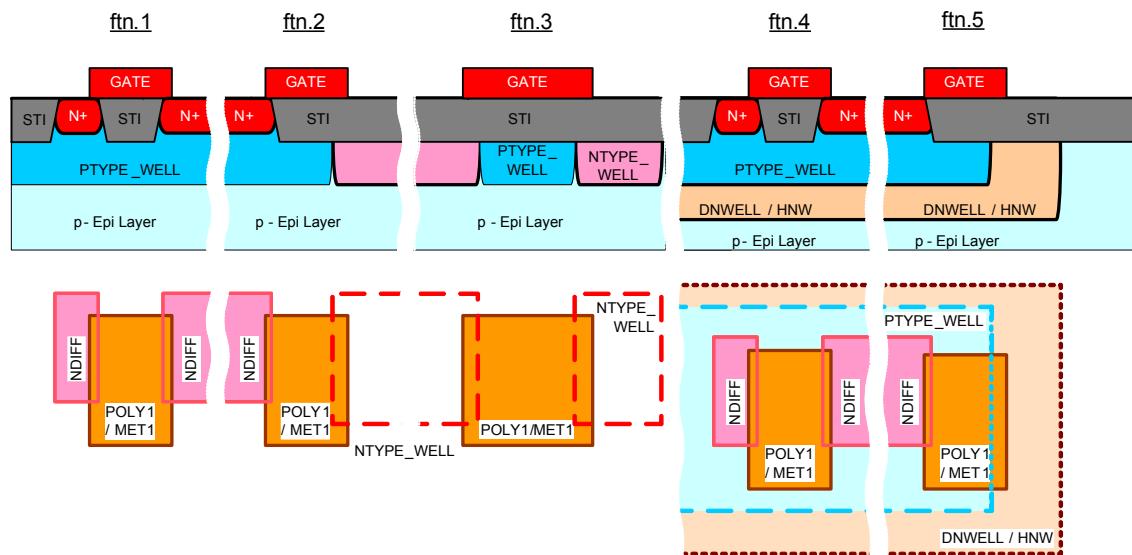


Figure 5.3 NLEAK channels

Implementing leakage suppression regions

Continuous NLEAK channels can be blocked by either inserting:

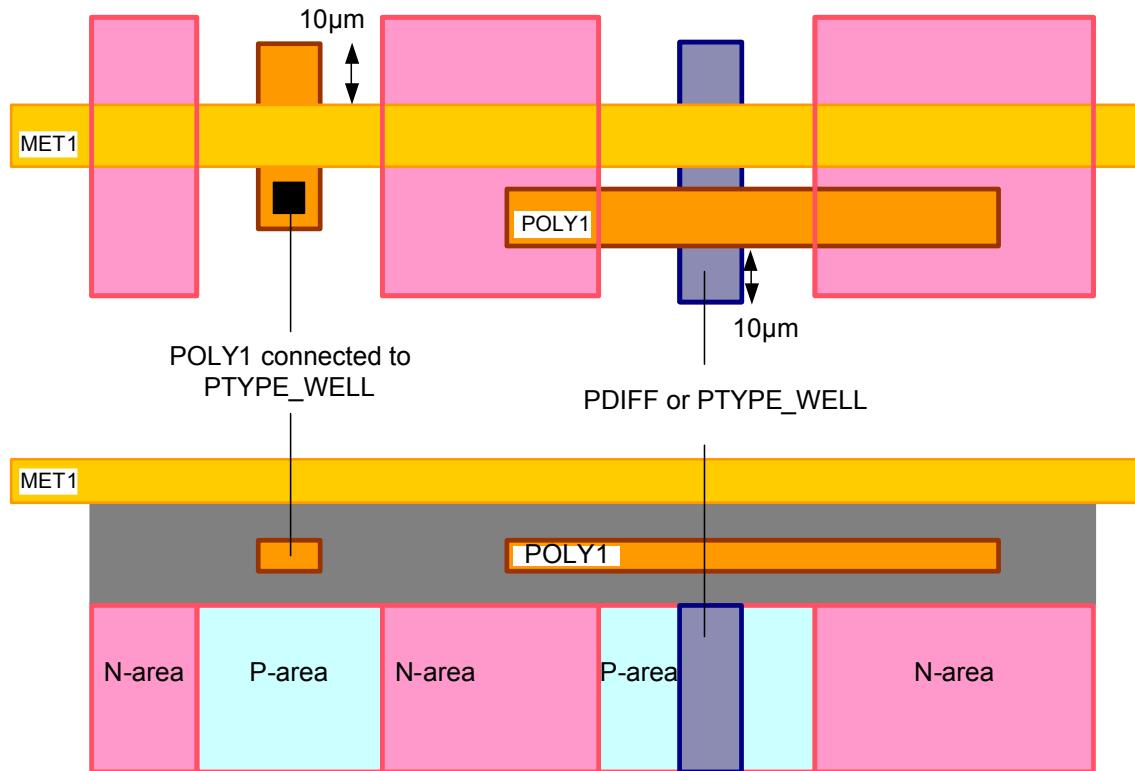
- P-areas with higher field threshold voltages
- PDIFF
- POLY1 (connected to the P-area, unless said area is PSUB in which case this will not work)
- Note that these activities are not allowed for predefined device layouts

When considering the size of the blocking regions the critical dimension is the extension beyond the offending polysilicon or metal lines. These dimensions are required in order to avoid the creation of continuous NLEAK channels (see diagram below):

Minimum PTYPE_WELL, PDIFF or POLY1 extension beyond POLY1HV or MET1HV is 10.0 µm



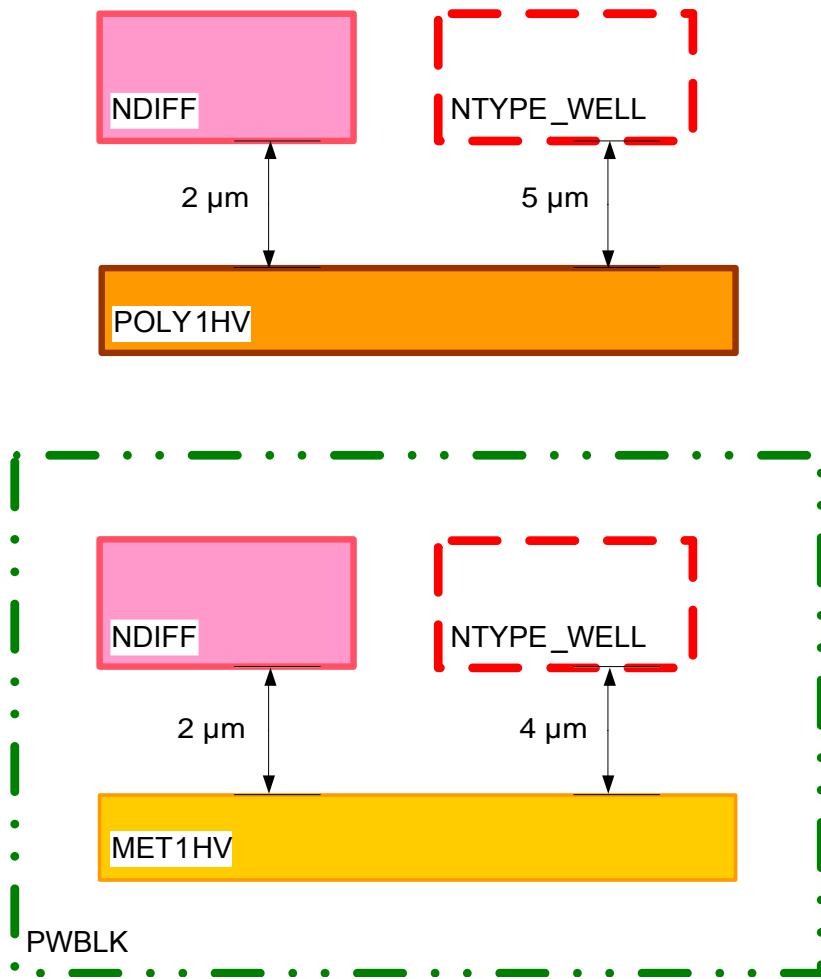
5. Design related guidelines → 5.3 NLEAK

**Figure 5.4** NLEAK Channels Suppression

Note: This diagram is only a conceptual illustration of a method to suppress field leakage. It might not reflect the actual device construction.

In addition to the cases described above, continuous NLEAK channels may already be formed if there is insufficient clearance between corresponding N-type regions and a polysilicon or metal line exceeding the respective field threshold voltage for the given well or well combination. In the case of transistors, NLEAK channels can extend beyond these lines and appear larger than the parasitic gate, such that P-area leakage can occur even if the parasitic gate only approaches it.

5. Design related guidelines → 5.3 NLEAK

**Figure 5.5** NLEAK related layer spacings

Minimum POLY1HV spacing to NDIFF over PTYPE_WELL is 2.00 μm

Minimum POLY1HV spacing to NTYPE_WELL is 5.00 μm

Minimum MET1HV spacing to NDIFF over PTYPE_WELL is 2.00 μm

Minimum MET1HV spacing to NTYPE_WELL is 4.00 μm

5. Design related guidelines → 5.4 PLEAK

5.4 PLEAK

Inversion will occur and a parasitic PLEAK channel will be formed if laterally positioned P-N-P areas are crossed by POLY1 or MET1 over STI and the voltage difference between these crossing lines and the interposed N-area exceeds the corresponding field threshold voltage for that combination. N-area is defined as NTYPE_WELL.

Notes:

- For further information, please refer to the appropriate 'Parasitic field parameters' within the Process & Device Specification, or search for 'VTF' parameters in the SpecXplorer.
- Both the case of complete and partial overlap of these NTYPE_WELL regions by a POLY1 or MET1 line should be considered. In the HNW MET2 lines should be considered too.
- PLEAK channels can connect PDIFF and PTYPE_WELL in any combination.
- PLEAK channels cannot be found automatically with verification tools.

The associated PLEAK channel of a field transistor can create unwanted electrical connections between two or more unrelated structures. Without loss of generality the following PLEAK constellations are possible with the XH018 layers. They are given as examples in cross sectional and plan view below. DNWELL stands for DNWELL or DNWELLMV. The gate may consist of POLY1 or MET1 and in case of HNW POLY1 or MET1 or MET2.

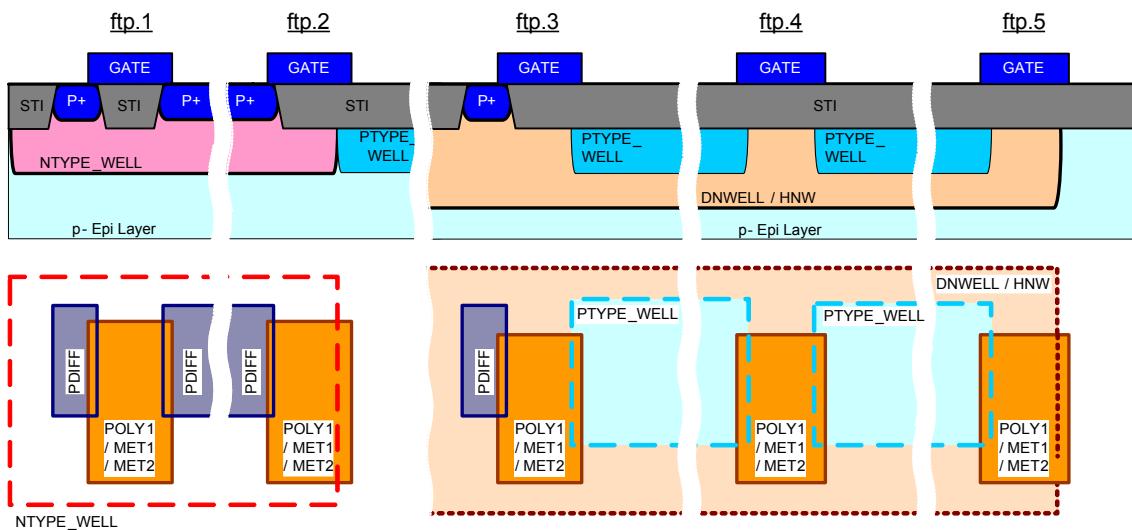


Figure 5.6 PLEAK field transistor configurations

Implementing leakage suppression regions

Continuous PLEAK channels can be blocked by either inserting:

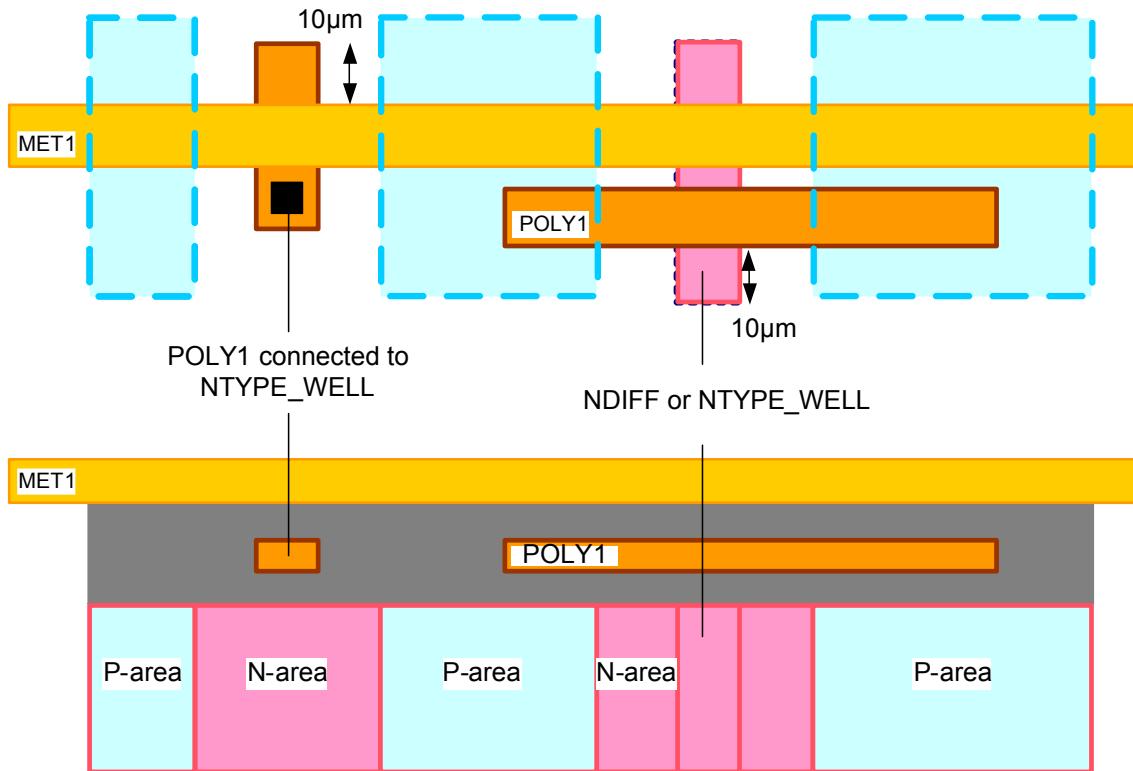
- N-areas with higher field threshold voltages
- NDIFF
- POLY1 (connected to the N-area) whenever possible
- Note that these activities are not allowed for predefined device layouts

When considering the size of the blocking regions the critical dimension is the extension beyond the offending polysilicon or metal lines. These dimensions are required in order to avoid the creation of continuous PLEAK channels (see diagram below):

Minimum NTYPE_WELL, NDIFF or POLY1 extension beyond POLY1HV or MET1HV is 10.0 µm.



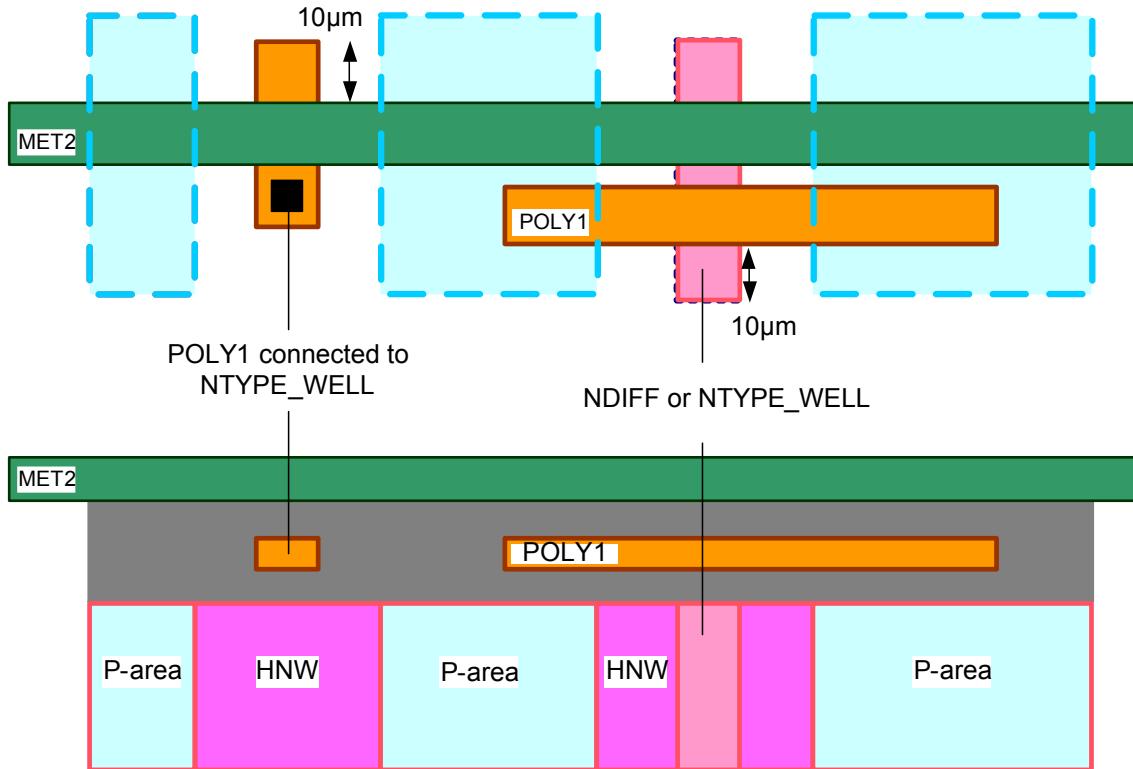
5. Design related guidelines → 5.4 PLEAK

**Figure 5.7** Suppression of PLEAK channels extension beyond POLY1HV or MET1HV

Note: This diagram is only a conceptual illustration of a method to suppressing field leakage. It might not reflect the actual device construction.

Minimum HNW, NDIFF or POLY1 extension beyond MET2HV is 10.0 µm

5. Design related guidelines → 5.4 PLEAK

**Figure 5.8** Suppression of PLEAK channels extension beyond MET2HV

Note: This diagram is only a conceptual illustration of a method to suppressing field leakage. It might not reflect the actual device construction.

In addition to the cases described above, continuous PLEAK channels may already be formed if there is insufficient clearance between corresponding P-type regions and a polysilicon or metal line exceeding the respective field threshold voltage for the given well or well combination.

In the case of transistors, PLEAK channels can extend beyond these lines and appear larger than the parasitic gate, such that N-area leakage can occur even if the parasitic gate only approaches it.

5. Design related guidelines → 5.4 PLEAK

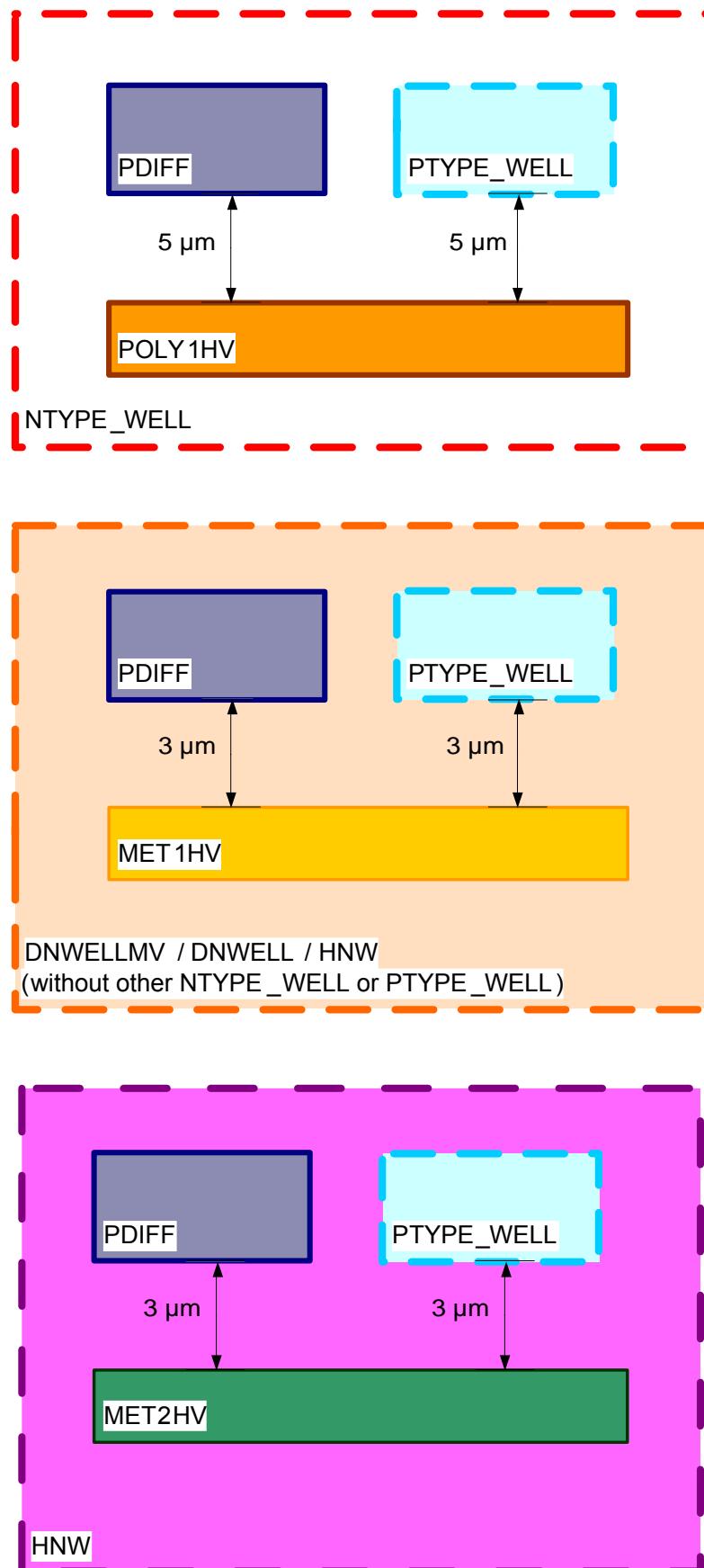


Figure 5.9 PLEAK related layer spacings

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5. Design related guidelines → 5.4 PLEAK

Minimum POLY1HV spacing to PDIFF over NTYPE_WELL is 5.00 μm

Minimum POLY1HV spacing to PTYPE_WELL over DNWELL, DNWELLMV or HNW is 5.00 μm

Minimum MET1HV spacing to PDIFF is 3.00 μm

Minimum MET2HV spacing to PDIFF in HNW is 3.00 μm

Minimum MET1HV spacing to PTYPE_WELL is 3.00 μm

Minimum MET2HV spacing to PTYPE_WELL in HNW is 3.00 μm

5. Design related guidelines → 5.5 Dummy Pattern Generation

5.5 Dummy Pattern Generation

Dummy pattern generation is necessary to ensure robust manufacturing and achieve better yields in lower geometry node such as 0.18µm technology.

Some advantages of dummy pattern insertion are listed below.

1. Better control of electrical parameters such as well resistance and breakdown voltage.

The 0.18µm technology node uses a Shallow Trench Isolation (STI) scheme to isolate primitive devices. STI uses Chemical Mechanical Polishing (CMP) to planarise the oxide which fills the trenches. If the active area pattern is non-uniform, over-polishing occurs ('dishing'), reducing the thickness of oxide in the trenches. Since well implants are performed through the trenches, electrical parameters like resistance and breakdown voltage can vary with the local pattern density. This is especially significant for high voltage devices. The addition of dummy pattern eliminates this problem.

2. Better CD and sidewall profile control.

Etch processes typically exhibit 'loading effects', where the etch rate depends on the pattern density. To achieve good critical dimension (CD) control and correct control of sidewall profiles, a uniform pattern density is necessary. This is achieved through the addition of dummy pattern. It is especially critical for poly and metal layers.

3. Better control of contact/via resistance and interlayer capacitance.

For metal layers, the dummy pattern generation reduces the thickness variation in the next dielectric layer (less dishing) which improves CD control for subsequent photolithography stages. A more uniform dielectric stack helps to reduce the variation in contact and via depth and results in smaller contact and via resistance variation and less variation in interlayer capacitance values.

Dummy fill insertion is applied in vacant layout spaces after the layout density scan using a design rule based script. The script identifies the vacant spaces and fills them with auto generated active/poly/metal dummies (purpose DUMMY) to equalise the pattern density as much as possible. Script based analysis is done to determine the regions of the layout violating density rules and the amount of dummy fill required in each region.

These auto generated dummy fill patterns/features are electrically isolated from the original layout.

The dummy layer generation is done for the following layers:

DIFF, POLY1, MET1, MET2, MET3, MET4, MET5, METTP, METTPL

The dummy pattern is generated by a software routine. It uses dummy blocking layers to define regions that must not have pattern fill added. In the Design Layers section of this document, the purpose of the dummy blocking layers is defined as "DMYBLK" as summarised below:

Layer	Design Layer	Remarks
DIFF, POLY	POLY1: DMYBLK	blocks DIFF and POLY1 dummy generation
MET1	MET1: DMYBLK	
MET2	MET2: DMYBLK	
METTP	METTP: DMYBLK	
MET3	MET3: DMYBLK	
MET4	MET4: DMYBLK	
MET5	MET5: DMYBLK	
METTPL	METTPL: DMYBLK	
BLKALL	BLKALL: DMYBLK	blocks all dummy generation

Important notes:

Dummy blocking layers should be used only on critical elements and not to block the entire layout.

Excessive use of dummy blocking layers might result in unsuitable design for manufacturing which could lead to poor performance with respect to inline defects and yield.

Note that the layer BLKALL removes ALL dummy fills; this is an unwanted by-product for the designer in many cases.

Dummy blocking areas can be used to prevent dummy pattern generation nearby or underneath sensitive circuit elements (e.g. to avoid additional parasitic capacitance).



5. Design related guidelines → 5.5 Dummy Pattern Generation

It is strongly recommended that the dummy blocking areas should only be used for the critical circuit elements.

The dummy pattern generation script does not guarantee that the minimum and maximum structure densities of the related layer are met. Please refer to rules R1DF, R1P1, R1M1, R2M1, R1M2, R2M2, R1M3, R2M3, R1M4, R2M4, R1M5, R2M5, R1MT, R2MT, R1ML, R2ML. These rules will be checked by X-FAB after IP replacement and dummy pattern generation.

It is recommended to use X-FAB's dummy pattern generation option (DUMMY_FILL included in the DRC for preview) to create dummy pattern. If the generated dummy pattern is not sufficient to meet the minimum requirements for pattern density, customers can draw additional dummy pattern following the dummy design rules (DIFFDUMMY, P1DUMMY, M1DUMMY, M2DUMMY, M3DUMMY, M4DUMMY, M5DUMMY, MTPDUMMY and MTPLDUMMY).

5. Design related guidelines → 5.6 Voltage class definitions

5.6 Voltage class definitions

With voltage class definitions, X-FAB offers a methodology for the voltage level information transfer between design and layout. The definition of tag devices (virtual devices which do not exist in silicon) allows an LVS check for coincidence and a DRC of the spacing rules for different voltage classes.

By using tag devices which assign a net to a specified voltage class, the correct and complete implementation from schematics to layout can be checked. For that purpose, the tag device symbol is placed to the net at schematics. At the layout, the voltage classification of the net is done by adding the tag device layout (label) to the shape.

The primitive device list shows which voltage classes and therefore which tag devices are defined for the process family.

The voltage of the net can vary within a wider range than defined by one voltage class. In such cases, one net can be part of several voltage classes and therefore several tag devices can coexist on the same net.

Between shapes without any tag labels, the basic spacing rules are valid.

Between shapes assigned to different voltage classes, different spacing might be required.

The following drawing illustrates the system used for voltage dependent spacing rules. Here the example with the voltage classes tag_25v and tag_60v is shown for layer MET1 (not wide metal):

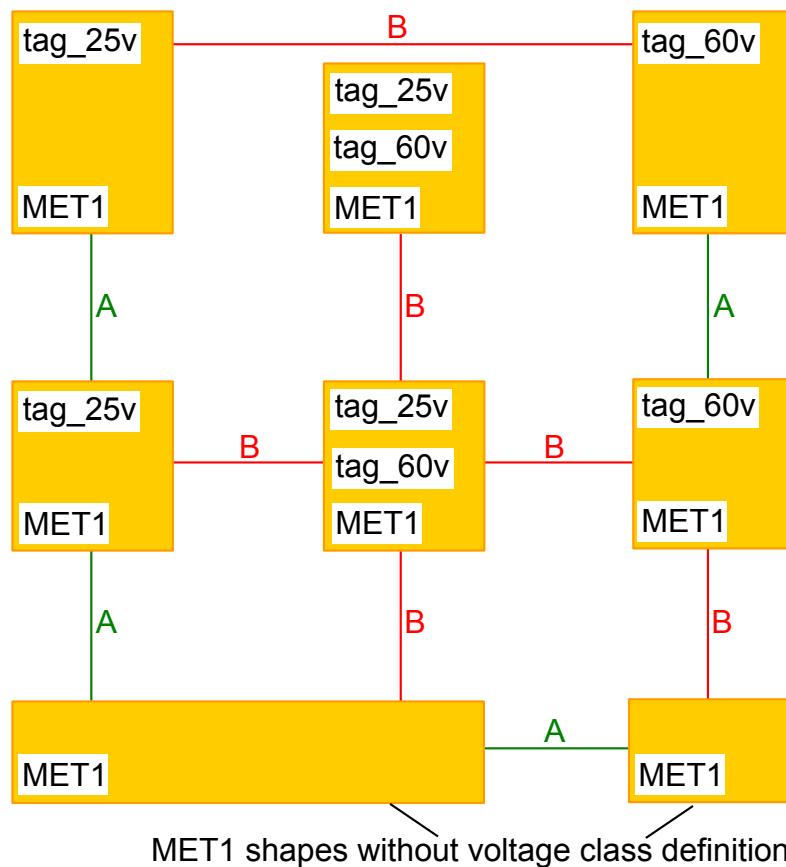


Figure 5.10 Voltage class

The resistor rules (for example Q1M1 in case of metal1 resistor) are warnings for thinking about the correct voltage class definition at both resistor terminals.

A resistor splits the net. If the resistor is assigned to a net having a voltage class then this voltage class is only assigned to one resistor terminal and the net ends. The other resistor terminal net requires an additional voltage class definition.

The resistor body is always part of both resistor terminal nets.

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