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Process and Device Specification XH018 - 0.18 µm Modular Mixed Signal HV CMOS

Document PDS_018_03
Release 8.0.1

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Table of Contents

1. Introduction

1.1 Related documents

Note: The specification documents listed in the table below do not contain information which is additional to that available in the SpecXplorer.

Description	Document number
Design Rule Specification XH018 - 0.18 µm Modular Mixed Signal HV CMOS	DR_018_03
PCM Acceptance Specification XH018 - 0.18 µm Modular Mixed Signal HV CMOS	PAS_018_03
Process Reliability Specification XH018 - 0.18 µm Modular Mixed Signal HV CMOS	PR_018_03

Note: Additional available specifications:
Design Rule Specification 0.18µm MIM Antenna Rules DR_018_10

Note: Note that additional documents and application notes related to this process family can be found in the relevant document container at "my X-FAB", under "Process Selection Documents" and "Technical Documents"

Note: Users may also wish to use the RelXplorer interactive application. This can provide information about device and layer reliability according to application specific mission profiles. For access to this see http://relxplorer.xfab.com

1.2 General notes

The specification describes parameters of the wafer process and of the available primitive devices. Data is provided for information to assist integrated circuit product development, especially for circuit design. This data can be seen in the columns Low/Typ/High.
Dispositional pass/fail parameters, which are used in the PCM test to check wafer electrical conformance prior to shipment, are also shown, in the columns LSL/USL.

Characteristic curves of the primitive devices showing measurement results of a typical wafer in comparison to the SPICE model simulations are available in the Device Characteristics Documentation (formerly Model Guides) on "my X-FAB".

This specification is valid excluding a process specific area around the wafer edge of 5mm width. In the affected area, the function, parameters and reliability of the structures are not guaranteed.

1.3 Support

Technical questions should be directed to:

X-FAB Semiconductor Foundries

web:	http://www.xfab.com	phone:	+49 361 427-6663
email:	hotline@xfab.com	fax:	+49 361 427-6631

1.4 SpecXplorer

All of the data in this specification document is also available online via the SpecXplorer website. For access to this, see http://specxplorer.xfab.com.

2. General

2.1 Process modules

For this process family, one main module exists.This main module must be chosen. This can then be combined with one or more additional modules. Please also refer to the tables showing the required and forbidden modules, because:

- some modules are only available in combination with other modules,
- some modules are not available in combination with other modules.

For a complete list of available metal layer combinations, refer to the table below:

Metal Options

number of metals	Available Metal Layer Combinations	Module names
4	MET1-MET2-MET3-METTP	LPMOS+MET3+METMID
5	MET1-MET2-MET3-MET4-METTP	LPMOS+MET3+MET4+METMID
5	MET1-MET2-MET3-METTP-METTPL	LPMOS+MET3+METMID+METTHK
6	MET1-MET2-MET3-MET4-MET5-METTP	LPMOS+MET3+MET4+MET5+METMID
6	MET1-MET2-MET3-MET4-METTP-METTPL	LPMOS+MET3+MET4+METMID +METTHK

2.1.1 Main modules

Name	No. of masks	Description	Typical devices, applications
LPMOS	19	1.8V / 3.3V low power CMOS module, single polysilicon, metal 1, metal 2	1.8V low power NMOS/ PMOS, 3.3V low power NMOS/ PMOS, PNP, well, polysilicon and metal resistors

Module restrictions for main modules

Name	Required modules	Forbidden modules
LPMOS	MET3 and METMID	-

2.1.2 Additional modules for LPMOS main module

Name	No. of masks	Description	Typical devices, applications
MET3	2	3-metal module, additional via2/metal 3 layers	more complex wiring
MET4	2	4-metal module, additional via3/metal 4 layers	more complex wiring
MET5	2	5-metal module, additional via4/metal 5 layers	more complex wiring
METMID	2	top metal module, additional top metal & via layers	more complex wiring
METTHK	2	thick metal module, additional thick metal and thick via layers	power distribution
CPOD	1	Polysilicon over diffusion capacitor	1.8V POD capacitor
CPODHV	2	High voltage polysilicon over diffusion capacitor	high voltage POD capacitor
	Note: If the CPODHV module is selected in combination with the HVMOS or HVNMOS or HVPMOS or ESDPNP module, the combined additional mask count is 0.		
MRPOLY	1	medium resistance polysilicon module	lightly P-doped POLY1 resistor
ISOMOS	1	triple well isolated CMOS module	isolated 1.8V or 3.3V CMOS in DNWELLMV
ISOMOS2	1	triple well isolated CMOS module	isolated 1.8V or 3.3V CMOS in DNWELL

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Name	No. of masks	Description	Typical devices, applications
HIGHTEMP	0	High temperature module	operating conditions up to +175°C
LVT	2	1.8V low Vt module additional NWELL and PWELL	1.8V low Vt NMOS and PMOS 1.8V isolated low Vt NMOS and PMOS
SVT	2	1.8V medium Vt module, additional NWELL and PWELL	1.8V medium Vt NMOS and PMOS 1.8V isolated
LNPMOS3	1	3.3V low noise PMOS module, additional NWELL4	3.3V low noise PMOS, 3.3V isolated low noise PMOS
ULN	1	Low noise CMOS module, additional ULN	1.8V & 3.3V low noise CMOS, 1.8V & 3.3V isolated low noise CMOS
DEPL	1	depletion module, depletion well implant	3.3V depletion NMOS, NPN
HVDEPL	1	High voltage depletion module, depletion well implant	32V depletion NMOS
DMOS	1	DMOS module, DMOS drift implant	40V / 45V NDMOS, 35V PDMOS
HVMOS	5	high voltage module, additional gate oxide, high voltage N-well and P-well	15V HV CMOS
	Note: If the ISOMOS module or ISOMOS2 module is selected in combination with the HVMOS module, the combined additional mask count is 5.		
HVNMOS	3	HVNMOS module, thick gate oxide	6V NMOS with thick gate oxide
	Note: 1.If the HVNMOS module is selected in combination with the HVMOS module, the combined additional mask count is 5. 2.If the HVNMOS module is selected in combination with the HVPMOS module, the combined additional mask count is 6. 3.If the HVNMOS module is selected in combination with the HVPMOS + NHVE module, the combined additional mask count is 6.		
NHVE	1	high voltage extension module, shallow N-well	10 / 15 / 45V HVNMOS
HVPMOS	6	HVPMOS module, thick gate oxide and high voltage N-well	6V PMOS with thick gate oxide
	Note: 1.If the HVPMOS module is selected in combination with the HVMOS module, the combined additional mask count is 7. 2.If the HVPMOS module is selected in combination with the HVNMOS + PHVE module, the combined additional mask count is 7.		
PHVE	1	high voltage extension module, shallow P-well	20 / 45V HVPMOS
SCHOTTKY	2	Schottky module	Schottky diode
	Note: 1.If the Schottky module is selected in combination with the HVMOS module, the combined additional mask count is 6. 2.If the Schottky module is selected in combination with the HVNMOS module, the combined additional mask count is 4. 3.If the Schottky module is selected in combination with the HVPMOS module, the combined additional mask count is 6.		
MIM	1	MIM capacitor module	MIM capacitor between metal top and metal layer underneath
MIM23	1	MIM capacitor module	MIM capacitor between metal 2 and metal 3
MIM34	1	MIM capacitor module	MIM capacitor between metal 3 and metal 4
DMIM	1	double MIM capacitor module	double MIM capacitor
TMIM	1	triple MIM capacitor module	triple MIM capacitor
MIMH	1	single high capacitance MIM capacitor module	single high capacitance MIM capacitor
MIMH23	1	high capacitance MIM capacitor module	MIM capacitor between metal 2 and metal 3
MIMH34	1	high capacitance MIM capacitor module	MIM capacitor between metal 3 and metal 4
DMIMH	1	double high capacitance MIM capacitor module	double high capacitance MIM capacitor
TMIMH	1	triple high capacitance MIM capacitor module	triple high capacitance MIM capacitor

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Name	No. of masks	Description	Typical devices, applications
NVM	2	non volatile memory module (SONOS based)	ready-to-use NVRAM memory blocks
	Note: For ready-to-use memory blocks, refer to the memory block specification regarding the process module combination which is required for the specific block.		
FLASH	0	Flash module	ready-to-use Flash memory blocks
	Note: For ready-to-use memory blocks, refer to the memory block specification regarding the process module combination which is required for the specific block.		
OTP3	0	One-Time Programmable memory module	ready to use OTP memory blocks
	Note: For ready-to-use memory blocks, refer to the memory block specification regarding the process module combination which is required for the specific block.		
ANODOP	1	UV diode module - anode implant	Photodiode
CATDOP	1	CATDOP module - cathode implant	Photodiode
UVWINDOW	0	UV diode module - opens UV sensitive window	Photodiode
AVLA	1	Avalanche photodiode module - avalanche multiplication implant	Avalanche photodiode
BIPESD	3	ESD module	ESD protected HV PNP transistor
	Note: 1.The BIPESD module must be selected for device qpvhscr only. 2.If the BIPESD module is selected in combination with the HVMOS module, the combined additional mask count is 7.		
ESDPNP	5	ESD module	ESD protected HV PNP transistor
	Note: 1.The ESDPNP module must be selected for device qpvhbscr only. 2.If the ESDPNP module is selected in combination with the HVPMOS module, the combined additional mask count is 6.		
FLATPV	0	Flat passivation	Flat passivation, post process
SFLATPV	0	Sensor Flat passivation	Flat passivation for microlense or colour filtering, post process
PIMIDE	1	polyimide module, resilient barrier layer on top of passivation	wafer overcoat for stress relief and passivation protection
PHOTODIO	0	Photodiode module	Photodiode
	Note: This module requires the addition of other modules or may not be used in combination with other modules, as listed in the table “Restrictions for Module Combinations”.		
HALL	3	Hall sensor module	Hall sensor
	Note: If the HALL module is selected in combination with the HVMOS module or the modules HVMOS AND DMOS, the combined additional mask count is 6.		

Module restrictions for LPMOS main module

Name	Required modules	Forbidden modules
MET3	-	-
MET4	MET3	ANODOP or UVWINDOW
MET5	MET4	METTHK
METMID	-	-
METTHK	METMID	MET5 or FLATPV or ANODOP or CATDOP or UVWINDOW or SFLATPV or AVLA
CPOD	-	-
CPODHV	CPOD	-
MRPOLY	-	-
ISOMOS	-	-
ISOMOS2	ISOMOS	-
HIGHTEMP	-	PHOTODIO or HALL or ANODOP

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Name	Required modules	Forbidden modules
LVT	-	-
SVT	-	-
LNPMOS3	-	-
ULN	-	-
DEPL	-	-
HVDEPL	NHVE	-
DMOS	HVMOS	-
HVMOS	-	-
HVNMOS	-	-
NHVE	HVNMOS	-
HVPMOS	-	-
PHVE	HVPMOS	-
SCHOTTKY	-	-
MIM	METMID	DMIM or DMIMH or MIMH or TMIM or TMIMH or MIM23 or MIM34 or MIMH23 or MIMH34
MIM23	MET3	MIM34 or MIMH23 or MIMH34 or MIM or DMIM or TMIM or MIMH or DMIMH or TMIMH
MIM34	MET4	MIM23 or MIMH23 or MIMH34 or MIM or DMIM or TMIM or MIMH or DMIMH or TMIMH
DMIM	MET3	MIM or TMIM or MIMH or DMIMH or TMIMH or MIM23 or MIM34 or MIMH23 or MIMH34
TMIM	MET4	MIM or DMIM or DMIMH or MIMH or TMIMH or MIM23 or MIM34 or MIMH23 or MIMH34
MIMH	METMID	MIM or MIM23 or MIM34 or DMIM or TMIM or MIMH23 or MIMH34 or DMIMH or TMIMH
MIMH23	MET3	MIM23 or MIM34 or MIMH34 or MIM or DMIM or TMIM or MIMH or DMIMH or TMIMH
MIMH34	MET4	MIM23 or MIM34 or MIMH23 or MIM or DMIM or TMIM or MIMH or DMIMH or TMIMH
DMIMH	MET3	MIM or DMIM or MIMH or TMIM or TMIMH or MIM23 or MIM34 or MIMH23 or MIMH34
TMIMH	MET4	MIM23 or MIM34 or MIMH23 or MIMH34 or MIM or DMIM or TMIM or MIMH or DMIMH
NVM	ISOMOS	-
FLASH	NVM	-
OTP3	-	-
ANODOP	UVWINDOW	MET4 or METTHK or HIGHTEMP
CATDOP	-	METTHK
UVWINDOW	MET3 and METMID	MET4 or METTHK
	Note: It is recommended to select either ANODOP or CATDOP module when the UVWINDOW module was selected. For any other use of UVWINDOW module, please contact X-FAB hotline.	
AVLA	CATDOP	PIMIDE or METTHK
BIPESD	-	-
ESDPNP	-	-
FLATPV	METMID	METTHK or SFLATPV
SFLATPV	METMID	METTHK or FLATPV
PIMIDE	-	AVLA

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Name	Required modules	Forbidden modules
PHOTODIO	ISOMOS	HIGHTEMP
HALL	-	HIGHTEMP

2.2 Process flows

2.2.1 for LPMOS main module

WIP reference	Process step	Process modules
n/a	wafer start	LPMOS
HVGOX	HV gate oxide	HVMOS
HNW	deep HV NWELL	HVPMOS, SCHOTTKY, BIPESD
ACTIVE	active / STI	LPMOS
DNWELL	deep NWELL	ISOMOS, ISOMOS2, HVMOS, PHOTODIO
HVWELL	HV wells	HVMOS
NDF	shallow HV Nwell	NHVE
PDF	shallow HV Pwell	PHVE
DMOS	DMOS drift implant	DMOS
DEPL	depletion implant	DEPL
HVDEPL	HV depletion implant	HVDEPL
NVM	non volatile memory	NVM, FLASH
WELL2	3.3V wells	LPMOS
CPOD	CPOD implant	CPOD
AML	Avalanche multiplication implant	AVLA
ANODOP	Anode implant for UV diode	ANODOP
CATDOP	Cathode implant	CATDOP
WELL1	1.8V wells	LPMOS
LVT	1.8V low Vt wells	LVT
SVT	1.8V medium Vt wells	SVT
GOX	dual gate oxide	LPMOS
POLY	poly silicon gate	LPMOS
SD	source/ drain implants	LPMOS
MRPOLY	MRPOLY implant	MRPOLY
SALICIDE	salicidation	LPMOS
METAL1	metal1	LPMOS
METAL2	metal2	LPMOS
MIM23/ MIMH23	single MIM capacitor	MIM23, MIMH23
DMIM1/DMIMH1	double MIM capacitor	DMIM, DMIMH
TMIM1/TMIMH1	triple MIM capacitor	TMIM, TMIMH
METAL3	metal3	MET3
MIM34/ MIMH34	single MIM capacitor	MIM34, MIMH34
DMIM2/DMIMH2	double MIM capacitor	DMIM, DMIMH
TMIM2/TMIMH2	triple MIM capacitor	TMIM, TMIMH
METAL4	metal4	MET4
TMIM3/TMIMH3	triple MIM capacitor	TMIM, TMIMH
METAL5	metal5	MET5
MIM/ MIMH	MIM capacitor	MIM, MIMH
METALTP	top metal	METMID
MTPL	thick metal	METTHK

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WIP reference	Process step	Process modules
FLATPV	planarized passivation	FLATPV
SFLATPV	planarized passivation	SFLATPV
PAD	passivation	LPMOS
PIMIDE	polyimide	PIMIDE

2.3 Wafer cross-section

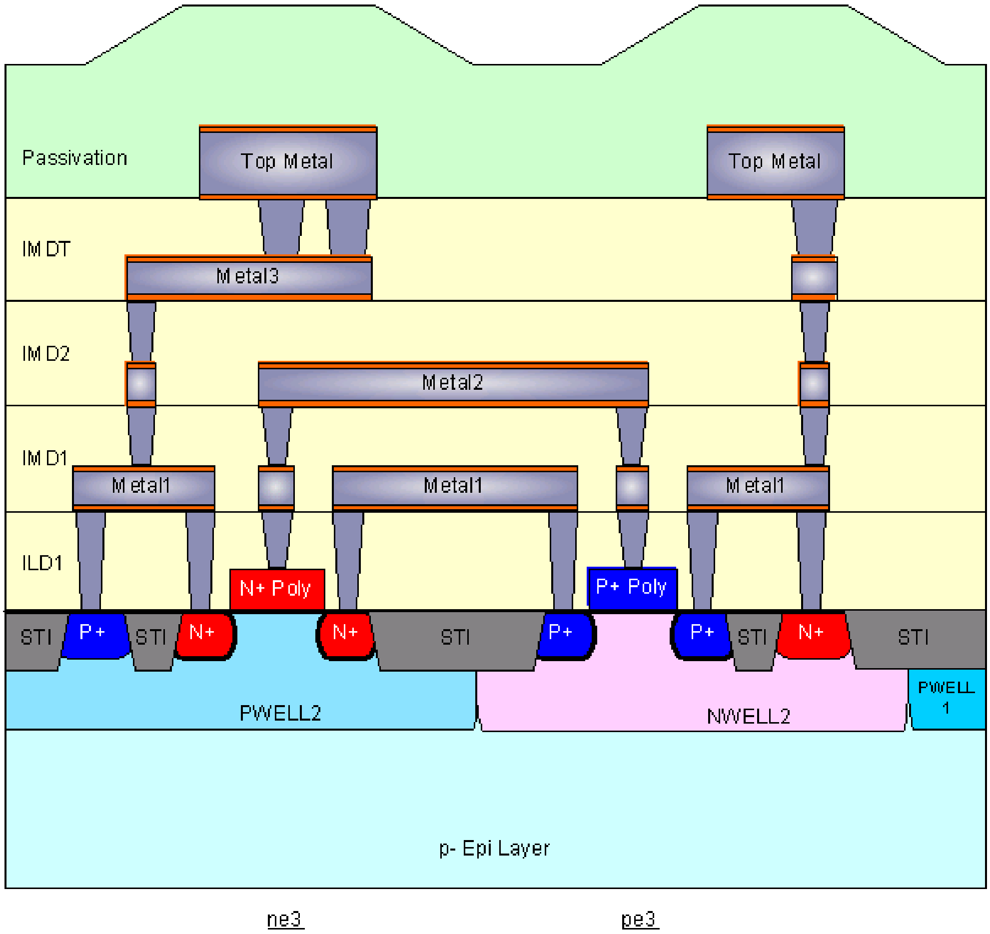

Figure 2.1 LPMOS + MET3 + METMID module transistors ne3, pe3

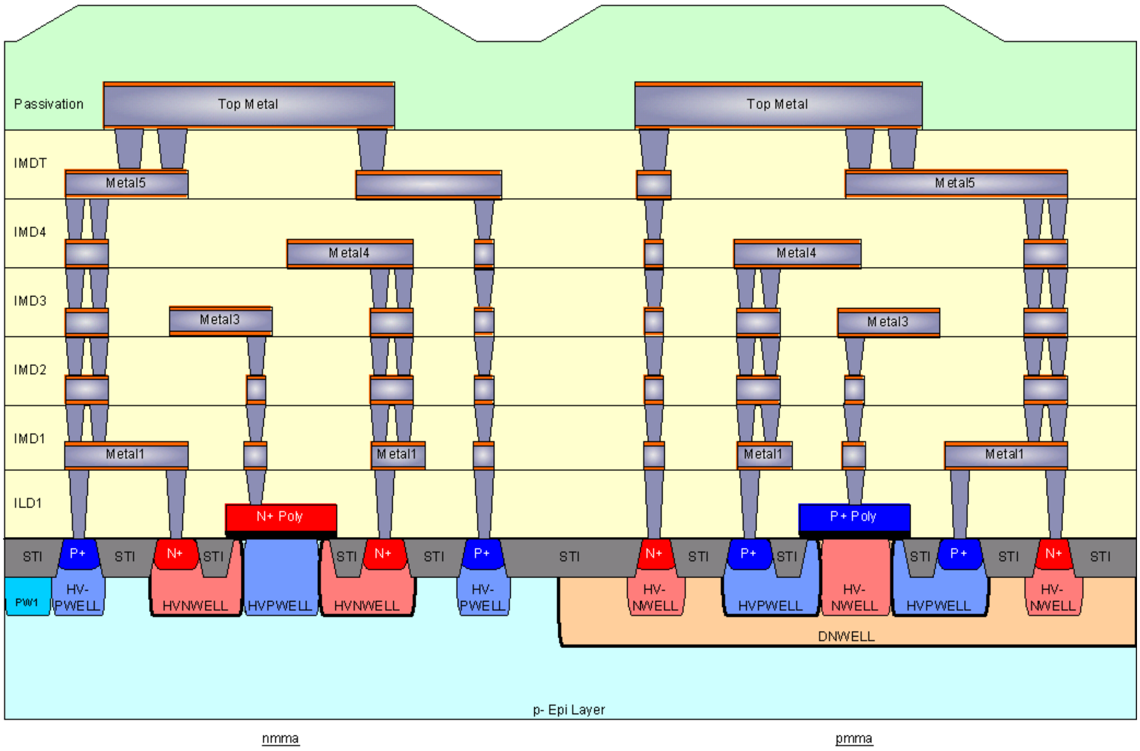

Figure 2.2 HVMOS module transistors nmma and pmma with MET3, MET4, MET5 and METMID module

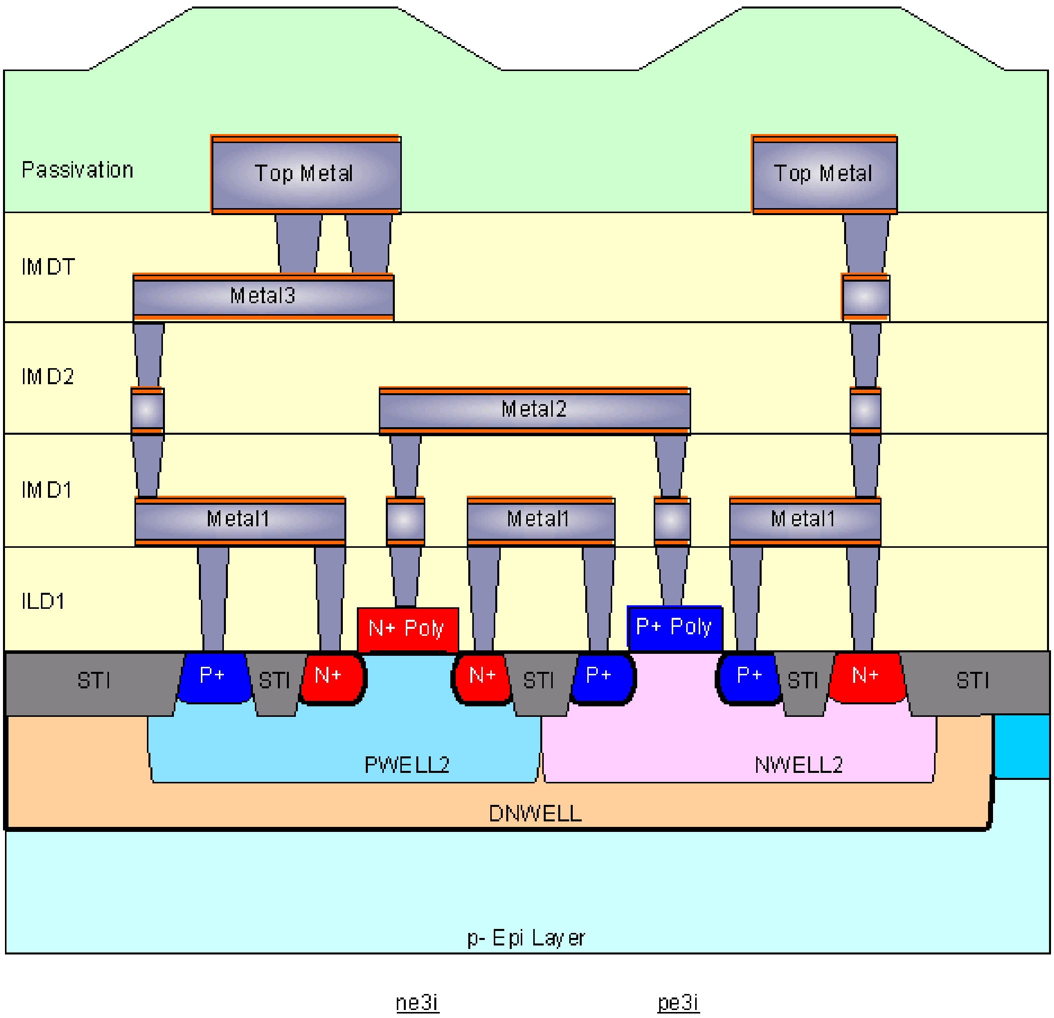

Figure 2.3 LPMOS + ISOMOS + MET3 + METMID module transistors ne3i, pe3i

2.4 Bond pad structure

2.4.1 4 Metal METMID Bond Pad

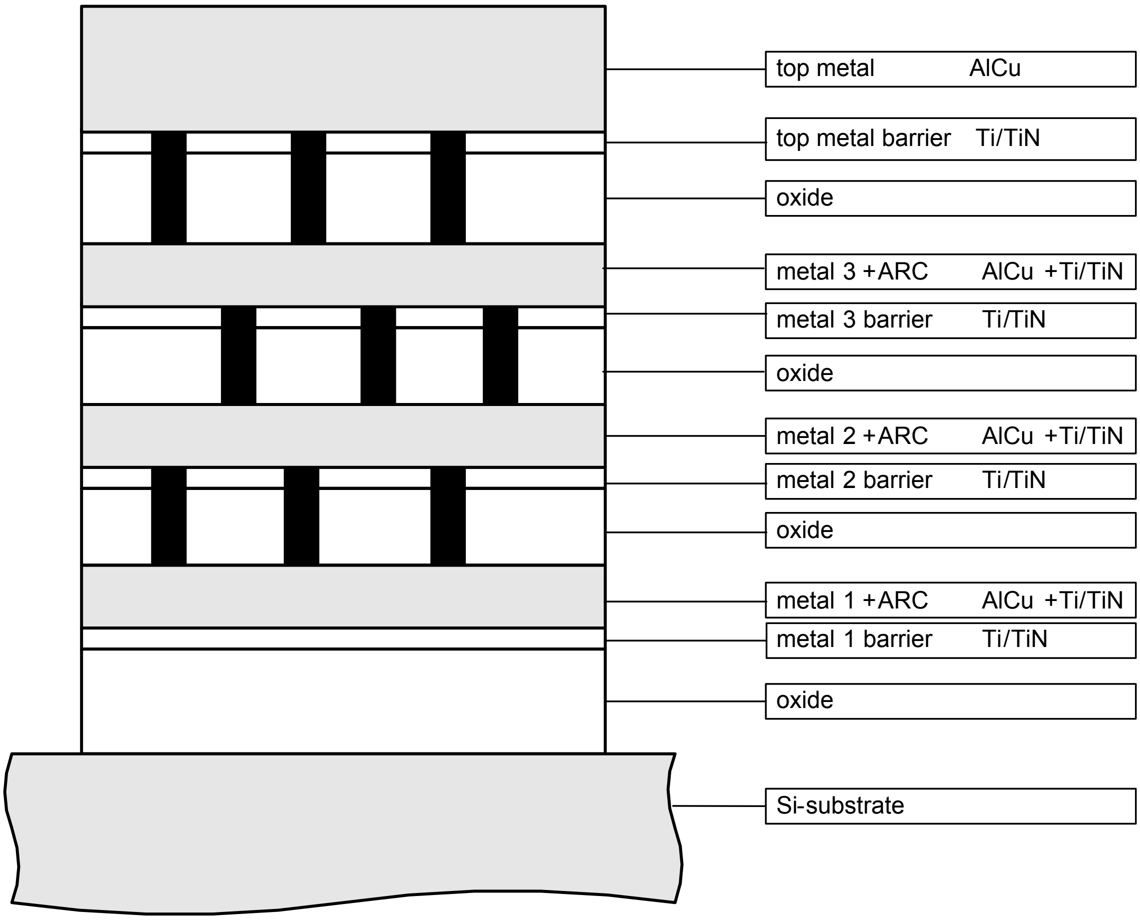

Figure 2.4 Principle of vertical structure of bond pads for four layer metal (only valid for the bond pad described by the Design Rule Specification)

Note: Top metal thickness at Bond Pad (typical value):

top metal	880 nm AlCu (0.5% Cu)

It is completely under customer's responsibility to communicate the bond pad structure as described above towards the assembly house to achieve a maximum of assembly performance by optimized assembly process parameters.

2.4.2 5 Metal METMID + METTHK Bond Pad

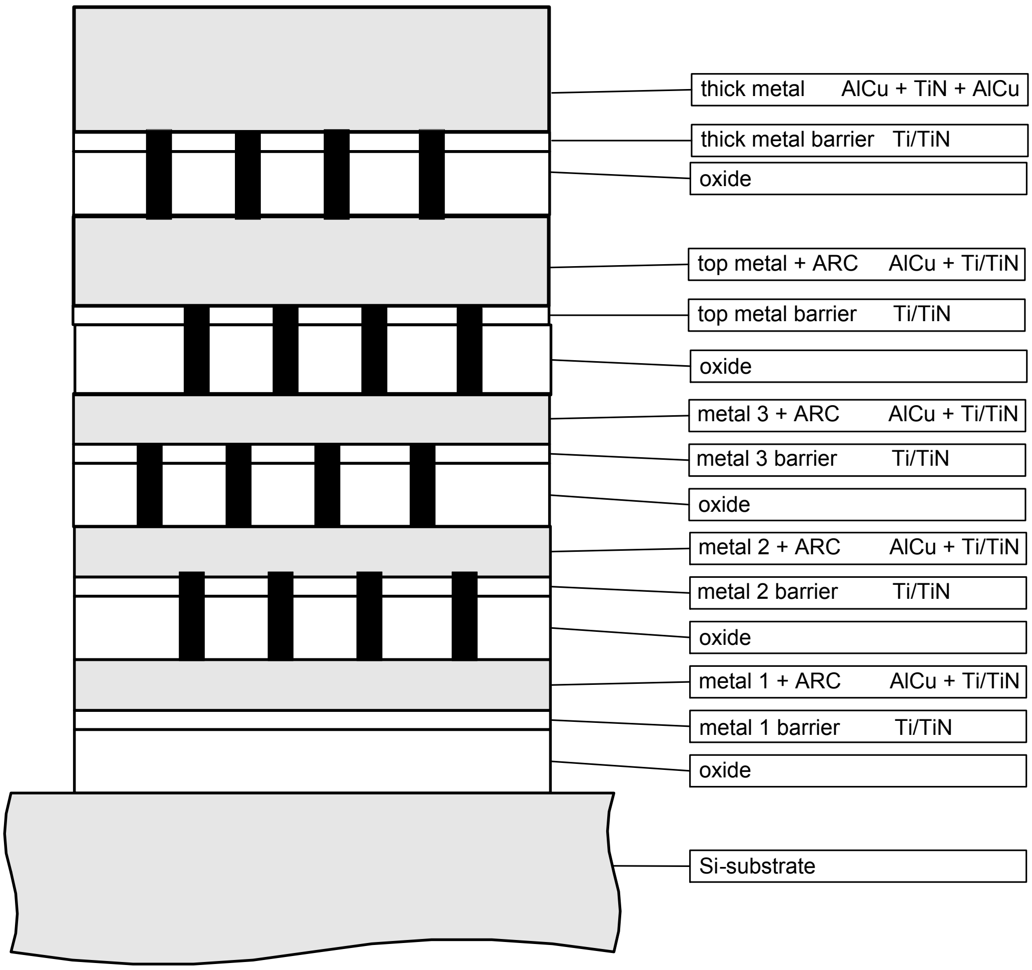

Figure 2.5 Principle of vertical structure of bond pads for five layers of metal
(only valid for the bond pad described by the Design Rule Specification)

Note: Top metal thickness at Bond Pad (typical value):

thick metal	1480 nm AlCu (0.5% Cu) + 40 nm TiN + 1480 nm AlCu (0.5% Cu)

It is completely under customer's responsibility to communicate the bond pad structure as described above towards the assembly house to achieve a maximum of assembly performance by optimized assembly process parameters.

2.4.3 5 Metal METMID Bond Pad

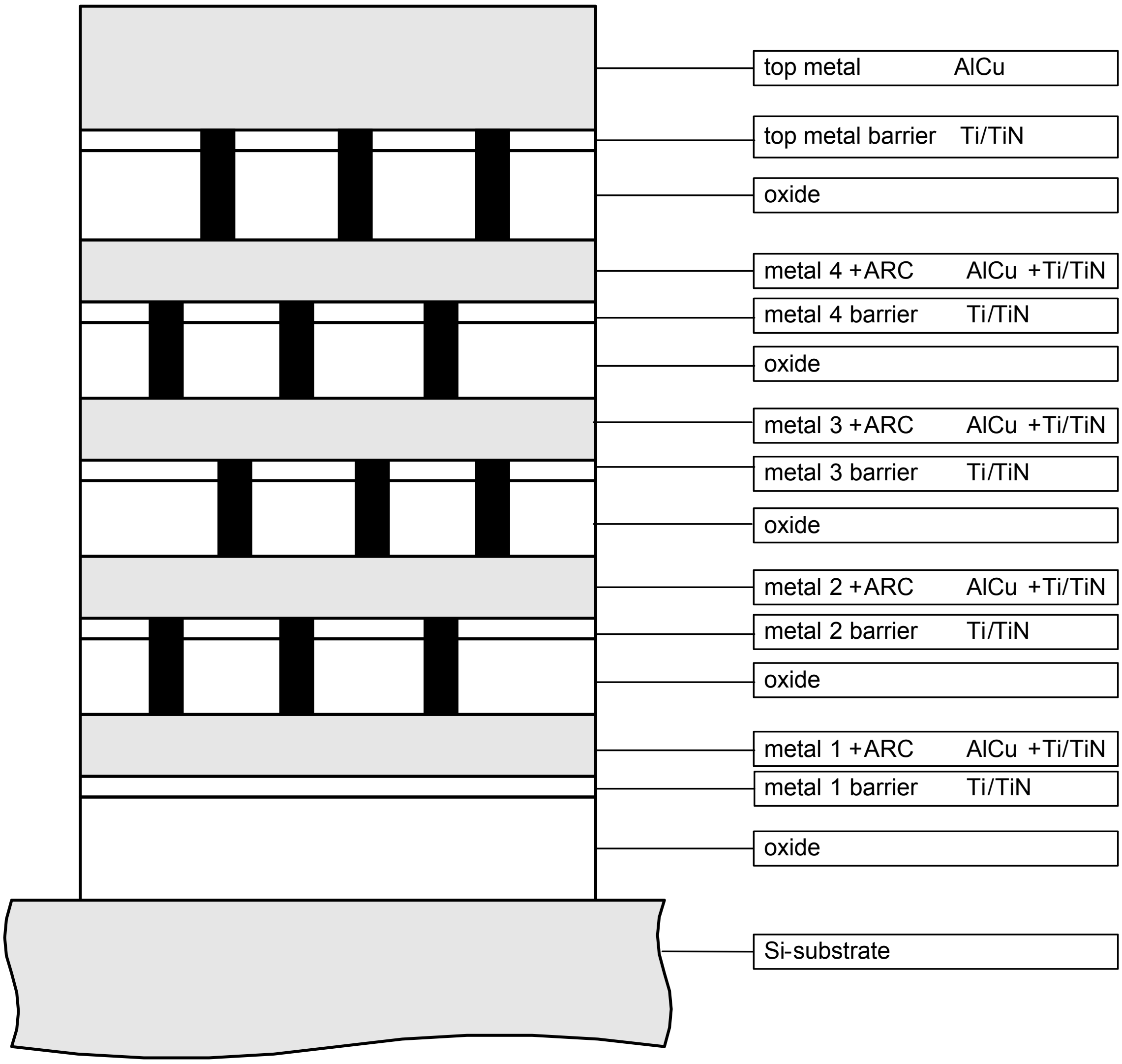

Figure 2.6 Principle of vertical structure of bond pads for five layers of metal (only valid for the bond pad described by the Design Rule Specification)

Note: Top metal thickness at Bond Pad (typical value):

top metal	880 nm AlCu (0.5% Cu)

It is completely under customer's responsibility to communicate the bond pad structure as described above towards the assembly house to achieve a maximum of assembly performance by optimized assembly process parameters.

2.4.4 6 Metal METMID + METTHK Bond Pad

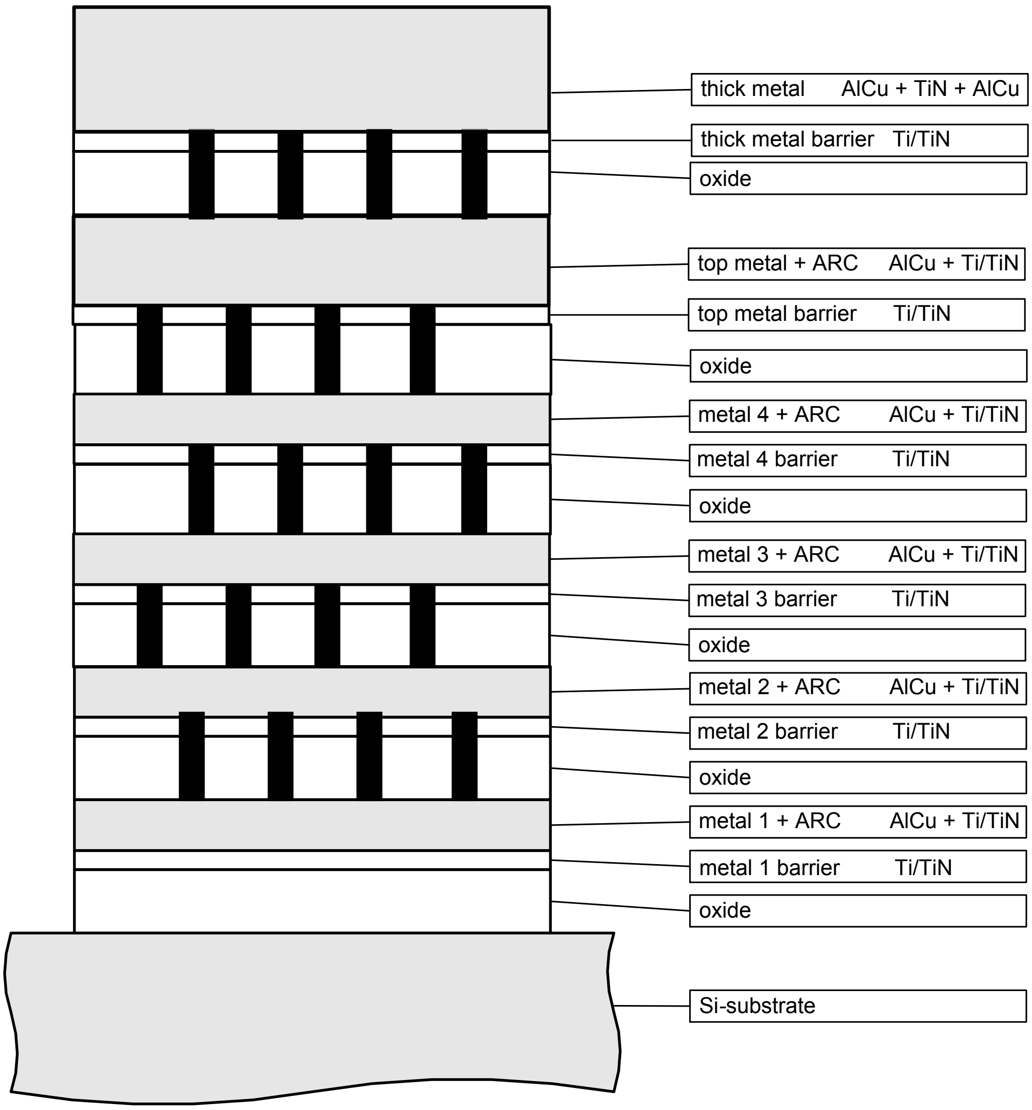

Figure 2.7 Principle of vertical structure of bond pads for six layers of metal (only valid for the bond pad described by the Design Rule Specification)

Note: Top metal thickness at Bond Pad (typical value):

thick metal	1480 nm AlCu (0.5% Cu) + 40 nm TiN + 1480 nm AlCu (0.5% Cu)

It is completely under customer's responsibility to communicate the bond pad structure as described above towards the assembly house to achieve a maximum of assembly performance by optimized assembly process parameters.

2.4.5 6 Metal METMID Bond Pad

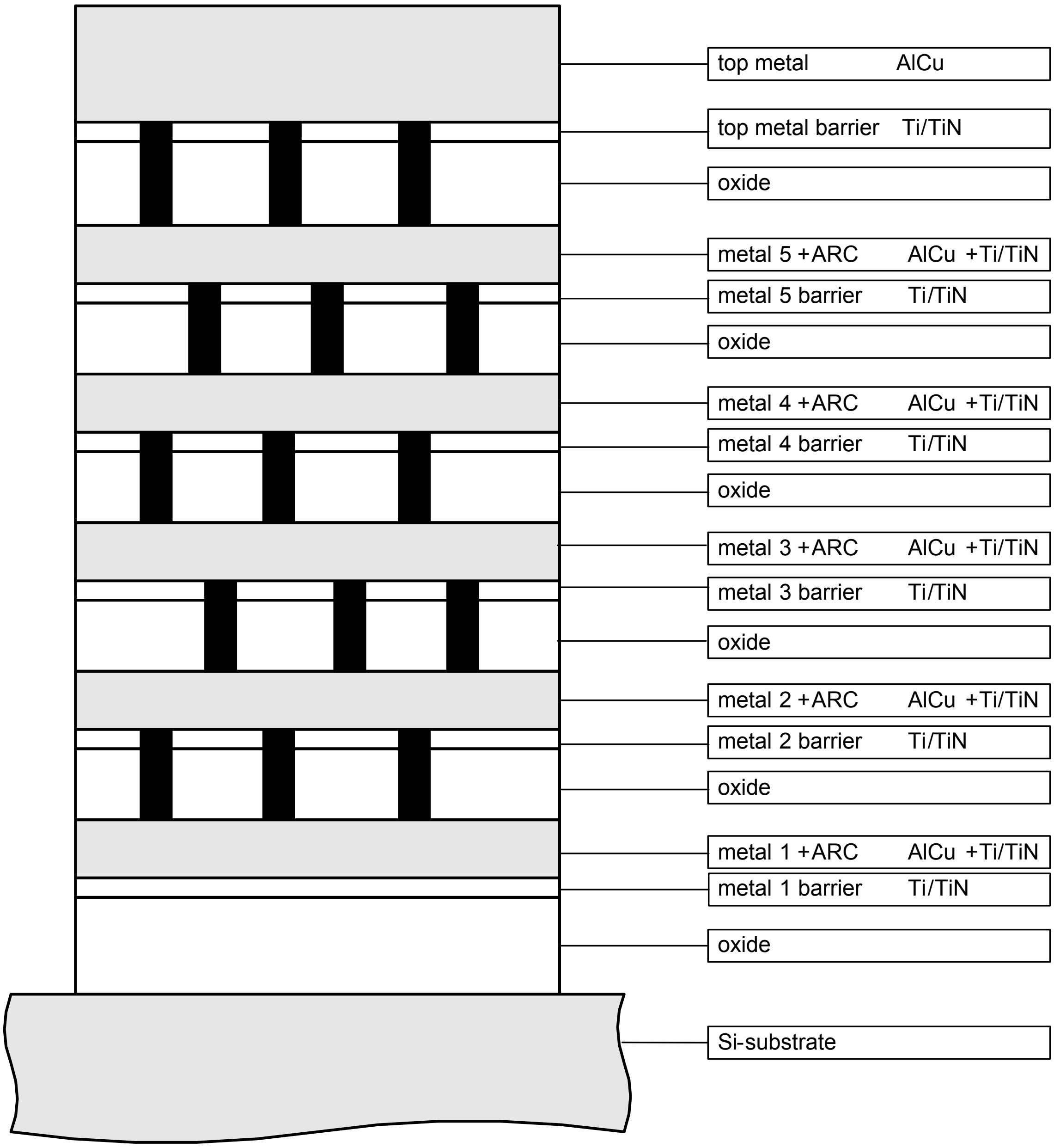

Figure 2.8 Principle of vertical structure of bond pads for six layers of metal (only valid for the bond pad described by the Design Rule Specification)

Note: Top metal thickness at Bond Pad (typical value):

top metal	880 nm AlCu (0.5% Cu)

It is completely under customer's responsibility to communicate the bond pad structure as described above towards the assembly house to achieve a maximum of assembly performance by optimized assembly process parameters.

2.5 Acronyms for operating conditions

Name	Description
VGS	Gate to source voltage
VGB	Gate to bulk voltage
VGD	Gate to drain voltage
VDS	Drain to source voltage
VDB	Drain to bulk voltage
VSB	Source to bulk voltage
VDpsub	Drain to p-substrate voltage
VBpsub	Bulk to p-substrate voltage
VSpsub	Source to p-substrate voltage
VCE	Collector to emitter voltage
VEB	Emitter to base voltage
VBC	Base to collector voltage
VCS	Collector to substrate voltage
Vterm-bulk	Terminal to bulk voltage
Vterm1-Vterm2	Terminal to terminal voltage
Vanode-Vcathode	Anode to cathode voltage
Vcathode-Vpsub	Cathode to p-substrate voltage
VIB	Isolation well to Bulk voltage
VIpsub	Isolation well to p-substrate voltage
JDL	Current density per width
JMax_CT_DC	Current density per contact, DC
JMax_DC	Current density per width, DC
JMax_N_DC	Current density per width for narrow tracks, DC
JMax_VI_DC	Current density per via, DC
JMax_CT_AC	Current density per contact, AC
JMax_AC	Current density per width, AC
JMax_N_AC	Current density per width for narrow tracks, AC
JMax_VI_AC	Current density per via, AC
T_Factor_1e4	Temperature correction factor, for 1E+04h lifetime
T_Factor_1e5	Temperature correction factor, for 1E+05h lifetime
Plight	Light power

2.6 Acronyms for measurement conditions

Name	Description
Vterm	Terminal voltage
Vlow	Lower voltage in measurement range
Vhigh	Upper voltage in measurement range
Vbias	Bias voltage
Vexcess	Excess bias voltage
VG	Voltage potential on gate terminal.
VD	Voltage potential on drain terminal.
VC	Voltage potential on collector terminal.
VSUB	Voltage potential on substate terminal
VE	Voltage potential on emitter terminal.
VL	Given voltage for leakage current measurement
VG-VT	Gate overdrive
Vrev	Reverse voltage
Ip	Current to sense for punch-through
Isupply	Hall sensor supply current
Ic	Collector current
Ie	Emitter current
Ib	Base current
Id	Drain current
Idio	Diode current
f	Frequency
T	temperature
Tnom	Nominal temperature
Er	Relative permittivity of the dielectric
λ	Wavelength
L	Device length
W	Device width
Pitch	Device pitch
LE	Emitter length
Ngates	Number of gates

2.7 Primitive devices

The primitive device list does not include all the required module combinations for the stated modules.
Refer also to the Module restrictions tables.

In addition to the capacitors stated in the primitive device list, it is also possible to use the capacitors built by the different gate oxides. These capacitors can be simulated by using the model of a transistor which has the respective oxide: for instance the ne and pe models in case of the 1.8V gate oxide.The operating conditions of the relating transistors are valid as well for these capacitors.

Minor changes of the simulation models might be generated due to continuous improvement of device and circuit simulation. Minor changes of models are described within the actual model data files. Please refer to further information within the current model path.

The qualification status of single devices can be checked in the Application Note "Primitive device release status" available at "my X-FAB"

The following devices are available for design:

2.7.1 LPMOS main module

MOS transistors

Name	Description	Required modules	Model rev.
ne	1.8V low power NMOS	-	4.0
pe	1.8V low power PMOS 4 terminals	-	4.0
pe_5 (1	1.8V low power PMOS 5 terminals	-	5.0
nel	1.8V low VT NMOS	LVT	6.0
pel	1.8V low VT PMOS 4 terminals	LVT	6.0
pel_5 (1	1.8V low VT PMOS 5 terminals	LVT	6.0
nei (2	isolated 1.8V low power NMOS 4 terminals	ISOMOS	4.0
nei_6 (1	isolated 1.8V low power NMOS in DNWELL 6 terminals	ISOMOS2 or (ISOMOS and HVMOS)	4.0
nei_m_6 (1	isolated 1.8V low power NMOS in DNWELLMV 6 terminals	ISOMOS	4.0
pei (2	isolated 1.8V low power PMOS 4 terminals	ISOMOS	4.0
pei_5 (1	isolated 1.8V low power PMOS in DNWELL 5 terminals	ISOMOS2 or (ISOMOS and HVMOS)	5.0
pei_m_5 (1	isolated 1.8V low power PMOS in DNWELLMV 5 terminals	ISOMOS	5.0
neli (2	isolated 1.8V low VT NMOS 4 terminals	LVT and ISOMOS	6.0
neli_6 (1	isolated 1.8V low VT NMOS in DNWELL 6 terminals	LVT and (ISOMOS2 or (ISOMOS and HVMOS))	6.0
neli_m_6 (1	isolated 1.8V low VT NMOS in DNWELLMV 6 terminals	LVT and ISOMOS	6.0
peli (2	isolated 1.8V low VT PMOS 4 terminals	LVT and ISOMOS	6.0
peli_5 (1	isolated 1.8V low VT PMOS in DNWELL 5 terminals	LVT and (ISOMOS2 or (ISOMOS and HVMOS))	6.0
peli_m_5 (1	isolated 1.8V low VT PMOS in DNWELLMV 5 terminals	LVT and ISOMOS	6.0
nesvt	1.8V medium VT NMOS	SVT	7.0
nesvti (2	isolated 1.8V medium VT NMOS 4 terminals	SVT and ISOMOS	7.0
nesvti_6 (1	isolated 1.8V medium VT NMOS in DNWELL 6 terminals	SVT and (ISOMOS2 or (ISOMOS and HVMOS))	7.0
nesvti_m_6 (1	isolated 1.8V medium VT NMOS in DNWELLMV 6 terminals	SVT and ISOMOS	7.0

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Name	Description	Required modules	Model rev.
pesvt	1.8V medium VT PMOS 4 terminals	SVT	7.0
pesvt_5 (1	1.8V medium VT PMOS 5 terminals	SVT	7.0
pesvti (2	isolated 1.8V medium VT PMOS 4 terminals	SVT and ISOMOS	7.0
pesvti_5 (1	isolated 1.8V medium VT PMOS in DNWELL 5 terminals	SVT and (ISOMOS2 or (ISOMOS and HVMOS))	7.0
pesvti_m_5 (1	isolated 1.8V medium VT PMOS in DNWELLMV 5 terminals	SVT and ISOMOS	7.0
nelna	1.8V low noise NMOS	ULN	7.0
nelnai (2	isolated 1.8V low noise NMOS 4 terminals	ULN and ISOMOS	7.0
nelnai_6 (1	isolated 1.8V low noise NMOS in DNWELL 6 terminals	ULN and (ISOMOS2 or (ISOMOS and HVMOS))	7.0
nelnai_m_6 (1	isolated 1.8V low noise NMOS in DNWELLMV 6 terminals	ULN and ISOMOS	7.0
nn3	3.3V native Vt NMOS	-	7.1
ne3	3.3V low power NMOS	-	4.1
pe3	3.3V low power PMOS 4 terminals	-	4.1
pe3_5(1	3.3V low power PMOS 5 terminals	-	5.0
ne3i (2	isolated 3.3V low power NMOS 4 terminals	ISOMOS	4.1
ne3i_6 (1	isolated 3.3V low power NMOS in DNWELL 6 terminals	ISOMOS2 or (ISOMOS and HVMOS)	4.1
ne3i_m_6 (1	isolated 3.3V low power NMOS in DNWELLMV 6 terminals	ISOMOS	4.1
pe3i (2	isolated 3.3V low power PMOS 4 terminals	ISOMOS	4.1
pe3i_5 (1	isolated 3.3V low power PMOS in DNWELL 5 terminals	ISOMOS2 or (ISOMOS and HVMOS)	5.0
pe3i_m_5 (1	isolated 3.3V low power PMOS in DNWELLMV 5 terminals	ISOMOS	5.0
ne3lna	3.3V low noise NMOS	ULN	7.0
ne3lnai (2	isolated 3.3V low noise NMOS 4 terminals	ULN and ISOMOS	7.0
ne3lnai_6 (1	isolated 3.3V low noise NMOS in DNWELL 6 terminals	ULN and (ISOMOS2 or (ISOMOS and HVMOS))	7.0
ne3lnai_m_6 (1	isolated 3.3V low noise NMOS in DNWELLMV 6 terminals	ULN and ISOMOS	7.0
pe3lna	3.3V low noise PMOS 4 terminals	ULN	7.0
pe3lna_5 (1	3.3V low noise PMOS 5 terminals	ULN	7.0
pe3lnai (2	isolated 3.3V low noise PMOS 4 terminals	ULN and ISOMOS	7.0
pe3lnai_5 (1	isolated 3.3V low noise PMOS in DNWELL 5 terminals	ULN and (ISOMOS2 or (ISOMOS and HVMOS))	7.0
pe3lnai_m_5 (1	isolated 3.3V low noise PMOS in DNWELLMV 5 terminals	ULN and ISOMOS	7.0
pe3ln	3.3V low noise PMOS 4 terminals	LNPMOS3	6.1
pe3ln_5 (1	3.3V low noise PMOS 5 terminals	LNPMOS3	6.1
pe3lni (2	isolated 3.3V low noise PMOS 4 terminals	LNPMOS3 and ISOMOS	6.1
pe3lni_5 (1	isolated 3.3V low noise PMOS in DNWELL 5 terminals	LNPMOS3 and (ISOMOS2 or (ISOMOS and HVMOS))	6.1

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Name	Description	Required modules	Model rev.
pe3lni_m_5 [1	isolated 3.3V low noise PMOS in DNWELLMV 5 terminals	LNPMOS3 and ISOMOS	6.1
nd3	3.3V depletion NMOS	DEPL	4.0
nd3i [2	isolated 3.3V depletion NMOS 4 terminals	(DEPL and ISOMOS) or (DEPL and HVMOS)	4.0
nd3i_6 [1	isolated 3.3V depletion NMOS in DNWELL 6 terminals	DEPL and HVMOS	4.0
nd3i_m_6 [1	isolated 3.3V depletion NMOS in DNWELLMV 6 terminals	DEPL and ISOMOS	4.0
nmma	10V HV NMOS	HVMOS	7.0
nmma_bjt [3	nmma with additional parasitic bjt model	HVMOS	7.0
pmma	15V HV PMOS	HVMOS	7.0
pmma_bjt [3	pmma with additional parasitic bjt model	HVMOS	7.0
nedi [4 [5	isolated 40V lateral n-DMOS	DMOS	7.0
nedi_bjt [3 [4 [5	nedi with additional parasitic bjt model	DMOS	7.0
nedia [5	isolated 45V lateral n-DMOS	DMOS	6.1
nedia_bjt [3 [5	nedia with additional parasitic bjt model	DMOS	6.1
ped2	35V lateral p-DMOS	DMOS	6.1
ped2_bjt [3	ped2 with additional parasitic bjt model	DMOS	6.1
ped	45V lateral p-DMOS	DMOS	6.1
ped_bjt [3	ped with additional parasitic bjt model	DMOS	6.1
nhv	45V asymmetrical HV NMOS	NHVE	7.0
nhv_bjt [3	nhv with additional parasitic bjt model	NHVE	7.0
nhhv	45V symmetrical HV NMOS	NHVE	7.0
nhhv_bjt [3	nhhv with additional parasitic bjt model	NHVE	7.0
nmc	10V asymmetrical HV NMOS	NHVE	7.0
nmc_bjt [3	nmc with additional parasitic bjt model	NHVE	7.0
nmmc	15V symmetrical HV NMOS	NHVE	7.0
nmmc_bjt [3	nmmc with additional parasitic bjt model	NHVE	7.0
nmmd	15V symmetrical HV NMOS	NHVE	7.0
nmmd_bjt [3	nmmd with additional parasitic bjt model	NHVE	7.0
nma	6V NMOS with thick gate oxide	HVNMOS	7.0
nma_bjt [3	nma with additional parasitic bjt model	HVNMOS	7.0
nhvd	32V asymmetrical HV depletion NMOS	HVDEPL	5.0
nhvd_bjt [3	nhvd with additional parasitic bjt model	HVDEPL	6.3
nhhvd	32V symmetrical HV depletion NMOS	HVDEPL	5.0
nhhvd_bjt [3	nhhvd with additional parasitic bjt model	HVDEPL	6.3
phv	45V asymmetrical HV PMOS	PHVE	7.0
phv_bjt [3	phv with additional parasitic bjt model	PHVE	7.0
phhv	45V symmetrical HV PMOS	PHVE	7.0
phhv_bjt [3	phhv with additional parasitic bjt model	PHVE	7.0
pmc	20V asymmetrical HV PMOS	PHVE	7.0

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Name	Description	Required modules	Model rev.
pmc_bjt [3]	pmc with additional parasitic bjt model	PHVE	7.0
pmmc	20V symmetrical HV PMOS	PHVE	7.0
pmmc_bjt [3]	pmmc with additional parasitic bjt model	PHVE	7.0
pma	6V PMOS with thick gate oxide	HVPMOS	7.0
pma_bjt [3]	pma with additional parasitic bjt model	HVPMOS	7.0

Note 1 These devices are variants of the corresponding basic device with underlying wells. Parameters of these devices are identical to the corresponding basic device.

Note 2 The ISOMOS2 or HVMOS module is needed, if isolated MOS transistors are placed in DNWELL instead of DNWELLMV.

Note 3 Parameters of these devices are identical to the corresponding basic device.

Note 4 This device has been superseded by 'nedia'.

Note 5 ‘nedia’ is a more robust device with a higher on-state drain-source breakdown voltage than ‘nedi’.

Bipolar transistors

Name	Description	Required modules	Model rev.
qpva	1.8V vertical PNP bipolar transistor; emitter area = 2µm x 2µm	-	4.0
qpvb	1.8V vertical PNP bipolar transistor; emitter area = 5µm x 5µm	-	4.0
qpvc	1.8V vertical PNP bipolar transistor; emitter area = 10µm x 10µm	-	4.0
qpva3	3.3V vertical PNP bipolar transistor; emitter area = 2µm x 2µm	-	4.0
qpvb3	3.3V vertical PNP bipolar transistor; emitter area = 5µm x 5µm	-	4.0
qpvc3	3.3V vertical PNP bipolar transistor; emitter area = 10µm x10µm	-	4.0
qnva	vertical NPN bipolar transistor	DEPL and HVMOS	1.0
qnvb	vertical NPN bipolar transistor	(DEPL and ISOMOS) or (DEPL and HVMOS)	3.0
qnvc	vertical NPN bipolar transistor	ISOMOS	7.0

Resistors

Name	Description	Required modules	Model rev.
rdn	1.8V NDIFF / PWELL1 resistor (non salicided)	-	6.3
rdp	1.8V PDIFF / NWELL1 resistor (non salicided)	-	6.3
rnw	1.8V NWELL1 / PSUB resistor (STI terminated)	-	6.3
rdn3	3.3V NDIFF / PWELL2 resistor (non salicided)	-	6.3
rdp3	3.3V PDIFF / NWELL2 resistor (non salicided)	-	6.3
rnw3	3.3V NWELL2 / PSUB resistor (STI terminated)	-	6.3
rdnwmv	5V DNWELLMV / PSUB resistor (STI terminated)	ISOMOS or HVMOS	6.3
rnp1	N-doped POLY1 resistor (non salicided), 2 terminals	-	6.3

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Name	Description	Required modules	Model rev.
rnp1_3[1]	N-doped POLY1 resistor (non-salicided), 3 terminals	-	6.3
rpp1	P-doped POLY1 resistor (non-salicided), 2 terminals	-	6.3
rpp1_3[1]	P-doped POLY1 resistor (non-salicided), 3 terminals	-	6.3
rpp1s	salicided P-doped POLY1 resistor, 2 terminals	-	6.3
rpp1s_3[1]	salicided P-doped POLY1 resistor, 3 terminals	-	6.3
rnp1h	high-ohmic N-doped POLY1 resistor (non salicided), 2 terminals	-	6.3
rnp1h_3[1]	high-ohmic N-doped POLY1 resistor (non salicided), 3 terminals	-	6.3
rpp1k1	lightly P-doped POLY1 resistor (non salicided), 2 terminals	MRPOLY	6.3
rpp1k1_3 [1]	lightly P-doped POLY1 resistor (non salicided), 3 terminals	MRPOLY	6.3
rm1	metal 1 resistor	-	7.0
rm2	metal 2 resistor	-	7.0
rm3	metal 3 resistor	MET3	7.0
rm4	metal 4 resistor	MET4	7.0
rm5	metal 5 resistor	MET5	7.0
rmtp	top metal resistor	METMID	7.0
rmtpl	thick metal resistor	METTHK	7.0

Note 1 These devices are variants of the corresponding basic device with an underlying well, but not crossing a well boundary. The models realise an improved description of bulk voltage dependency. Parameters of these devices are identical to the corresponding basic device.

Capacitors

Name	Description	Required modules	Forbidden modules	Model rev.
mosvc	1.8V N-type varactor	-	-	6.3
mosvc3	3.3V N-type varactor	-	-	6.3
mosvc3i	3.3V P-type varactor in DNWELL	ISOMOS2 or (ISOMOS and HVMOS)	-	6.3
mosvc3i_m	3.3V P-type varactor in DNWELLMV	ISOMOS	-	6.3
mosvci	1.8V P-type varactor in DNWELL	ISOMOS2 or (ISOMOS and HVMOS)	-	6.3
mosvci_m	1.8V P-type varactor in DNWELLMV	ISOMOS	-	6.3
cpod	1.8V POD capacitor	CPOD	-	7.0
cpodhv	POD capacitor (high voltage)	CPODHV or (CPOD and (HVMOS or HVNMOS or HVPMOS or ESDPNP))	-	7.0
csandwt3	POLY1 / metal1/ metal2/ metal3 capacitor	MET3	-	7.0
csandwt4	POLY1 / metal1/ metal2/ metal3/ metal4 capacitor	MET4	-	7.0
csandwt5	POLY1 / metal1/ metal2/ metal3/ metal4/ metal5 capacitor	MET5	-	7.0

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Name	Description	Required modules	Forbidden modules	Model rev.
csf2p	POLY1/metal1/metal2 fringe capacitor	-	-	7.0
csf3p	POLY1/metal1/metal2/metal3 fringe capacitor	MET3	-	7.0
csf3	10V metal1/metal2/metal3 fringe capacitor	MET3	-	7.0
csf3a	45V metal1/metal2/metal3 fringe capacitor	MET3	-	7.0
csf4	10V metal1/metal2/metal3/metal4 fringe capacitor	MET4	-	7.0
csf4a	45V metal1/metal2/metal3/metal4 fringe capacitor	MET4	-	7.0
csf5	10V metal1/metal2/metal3/metal4/ metal5 fringe capacitor	MET5	-	7.0
csf5a	45V metal1/metal2/metal3/metal4/ metal5 fringe capacitor	MET5	-	7.0
csft4	10V metal1/metal2/metal3/metaltop fringe capacitor	MET3 and METMID	MET4	7.0
csft4a	45V metal1/metal2/metal3/metaltop fringe capacitor	MET3 and METMID	MET4	7.0
csft5	10V metal1/metal2/metal3/metal4/ metaltop fringe capacitor	MET4 and METMID	MET5	7.0
csft5a	45V metal1/metal2/metal3/metal4/ metaltop fringe capacitor	MET4 and METMID	MET5	7.0
csft6	10V metal1/metal2/metal3/metal4/ metal5/metaltop fringe capacitor	MET5 and METMID	-	7.0
csft6a	45V metal1/metal2/metal3/metal4/ metal5/ metaltop fringe capacitor	MET5 and METMID	-	7.0
cmm3	single MIM capacitor between metal2 and metal3	MIM23	-	7.0
cmm4	single MIM capacitor between metal3 and metal4	MIM34	-	7.0
cmm4t	single MIM capacitor between metal3 and metaltop	MIM and MET3 and METMID	MET4	7.0
cmm5t	single MIM capacitor between metal4 and metaltop	MIM and MET4 and METMID	MET5	7.0
cmm6t	single MIM capacitor between metal5 and metaltop	MIM and MET5 and METMID	-	7.0
cmmh3	single MIM capacitor (high capacitance) between metal2 and metal3	MIMH23	-	7.0
cmmh4	single MIM capacitor (high capacitance) between metal3 and metal4	MIMH34	-	7.0
cmmh4t	single MIM capacitor (high capacitance) between metal3 and metaltop	MIMH and MET3 and METMID	MET4	7.0
cmmh5t	single MIM capacitor (high capacitance) between metal4 and metaltop	MIMH and MET4 and METMID	MET5	7.0
cmmh6t	single MIM capacitor (high capacitance) between metal5 and metaltop	MIMH and MET5 and METMID	-	7.0
cdmm4	double MIM capacitor between metal2, metal3 and metal4	MET4 and DMIM	-	7.0
cdmm4t	double MIM capacitor between metal2, metal3 and metaltop	DMIM and MET3 and METMID	MET4	7.0

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Name	Description	Required modules	Forbidden modules	Model rev.
cdmmh4	double MIM capacitor (high capacitance) between metal2, metal3 and metal4	MET4 and DMIMH	-	7.0
cdmmh4t	double MIM capacitor (high capacitance) between metal2, metal3 and metaltop	DMIMH and MET3 and METMID	MET4	7.0
ctmm5	triple MIM capacitor between metal2, metal3, metal4 and metal5	MET5 and TMIM	-	7.0
ctmm5t	triple MIM capacitor between metal2, metal3, metal4 and metaltop	TMIM and MET4 and METMID	MET5	7.0
ctmmh5	triple MIM capacitor (high capacitance) between metal2, metal3, metal4 and metal5	MET5 and TMIMH	-	7.0
ctmmh5t	triple MIM capacitor (high capacitance) between metal2, metal3, metal4 and metaltop	(MET4 and METMID) and TMIMH	MET5	7.0

Diodes

Name	Description	Required modules	Model rev.
dn	diode NDIFF / PWELL1,3,5 (1.8V)	-	7.0
dp	diode PDIFF / NWELL1,3,5 (1.8V)	-	7.0
dnw	diode NWELL1,3,5 / PSUB (1.8V)	-	7.0
dn3	diode NDIFF / PWELL2 (3.3V)	-	7.0
dp3	diode PDIFF / NWELL2,4 (3.3V)	-	7.0
dnw3	diode NWELL2,4 / PSUB (3.3V)	-	7.0
dnn3[(1]	diode NDIFF/ PSUB (3.3V)	-	7.0
ddnwmv	diode DNWELLMV / PSUB	ISOMOS or HVMOS	7.0
dpdnwmv	diode PDIFF / DNWELLMV	ISOMOS or HVMOS	7.0
dipdnwmv	diode PWELL1,2 / DNWELLMV	ISOMOS or HVMOS	7.0
ddnw	diode DNWELL / PSUB	ISOMOS2 or HVMOS	7.0
dpdnw	diode PDIFF / DNWELL	ISOMOS2 or HVMOS	7.0
dipdnw	diode PWELL1,2 / DNWELL	ISOMOS2 or (HVMOS and ISOMOS)	7.0
dnhpw	diode NDIFF / HVPWELL	HVMOS	7.0
dphnw	diode PDIFF / HVNWELL	HVMOS	7.0
dhpw	diode HVPWELL / DNWELL	ISOMOS2 or HVMOS	7.0
dhnw	diode HVNWELL / PSUB	HVMOS	7.0
dndf	diode NDF / PSUB	NHVE	7.0
dpdwhn	diode PDF / HNW	PHVE	7.0
dwhn	diode HNW / PSUB	HVPMOS	7.0
dpwhn	diode PDIFF / HNW	HVPMOS	7.0
p_dn3dpl	parasitic junction diode NDIFF / DEPL (3.3V)	DEPL	7.0
p_ddpldnw	parasitic junction diode DEPL / DNWELL	DEPL and (HVMOS or ISOMOS or ISOMOS2)	7.0
p_dpdddnw	parasitic junction diode PDD / DNWELL	DMOS	7.0
p_dpndf	parasitic junction diode PDIFF / NDF	NHVE or HVPMOS	7.0

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Name	Description	Required modules	Model rev.
p_dbn	parasitic junction diode CPOD n+ / PSUB	CPOD	7.0
dsba	18V Schottky diode	SCHOTTKY	7.1
dsb [2]	18V Schottky diode	SCHOTTKY	7.1
dpol	polysilicon diode	-	7.0
dnp20	20V N-type protection diode	NHVE	3.0
dpp20	20V P-type protection diode	HVMOS	3.0
dphoa	Photodiode for visible and infrared light detection	PHOTODIO	7.0
dphob	Photodiode for infrared light detection	PHOTODIO	7.0
dphoc	Photodiode for ultraviolet, visible and infrared light detection	CATDOP and UVWINDOW	6.0
dphoc0	Blind (metal covered) reference photodiode for ultraviolet, visible and infrared light detection	CATDOP and UVWINDOW	6.0
dphocfp	Blind (poly covered) reference photodiode for ultraviolet, visible and infrared light detection	CATDOP and UVWINDOW	6.0
dphod	Photodiode for ultraviolet, visible and infrared light detection	ANODOP and UVWINDOW	6.0
dphod0	Blind (metal covered) reference photodiode for ultraviolet, visible and infrared light detection	ANODOP and UVWINDOW	6.0
dphodfp	Blind (poly covered) reference photodiode for ultraviolet, visible and infrared light detection	ANODOP and UVWINDOW	6.0
dapda [3]	Avalanche photodiode with breakdown voltage < 20V	CATDOP and AVLA	8.0
dapda0 [3]	Blind (metal covered) reference avalanche photodiode with breakdown voltage < 20V	CATDOP and AVLA	8.0
dspada [3]	Single-photon avalanche diode for low light levels with breakdown voltage < 20V	CATDOP and AVLA	8.0
dspada0 [3]	Single-photon avalanche diode for high light levels (metal covered) with breakdown voltage < 20V	CATDOP and AVLA	8.0

Note 1 This diode is only available along with the corresponding transistor where it is used as source/drain.

Note 2 The device dsb is superseded by dsba.

Note 3 Please refer to the documentation on "my X-FAB":
"Application Note - Avalanche Photodiodes"

Memories

Name	Description	Required modules	Model rev.
pfuse	polysilicon fuse	-	6.3

Sensors

Name	Description	Required modules	Model rev.
hall1	Hall sensor (available on request)	HALL	2.2

Virtual devices

Name	Description	Required modules	Model rev.
tag_25v [1	defines voltage class for net with ≤ 25V related to PSUB	-	7.0
tag_60v [1	defines voltage class for net with > 25V ≤ 60V related to PSUB	-	7.0

Note 1 These devices are not fabricated on silicon; they are available for DRC and LVS voltage class checks only. For further information, please refer to the design related guideline “Voltage class definitions”.

ESD devices

Name	Description	Required modules	Model rev.
qpvhbscr	ESD protected HV PNP bipolar transistor	ESDPNP	6.1
qpvascr [1	HVPWELL in DNWELL isolated scr	HVMOS	4.0
rdp_io [1	PDIFF drain ballast resistor of pmb (Pdiff in HVNWELL in DNW)	HVMOS	4.0
rdn_esd [1	NDIFF drain ballast resistor of ESD nma (Ndiff in HVPWELL)	HVNMOS	4.0
rdp_esd [1	PDIFF drain ballast resistor of ESD pma (Pdiff in HVNWELL in HNW)	HVPMOS	4.0
rnw_scr [1	1.8V LV NMOS triggered SCR dio/res network resistor	-	4.0
rnw3_scr [1	3.3V LV NMOS triggered SCR dio/res network resistor	-	4.0
qpvhscr	ESD protected HV PNP bipolar transistor	BIPESD	7.0
pmb [1	5V ESD PMOS	HVMOS	7.0

Note 1 These devices are only allowed to be used for ESD protection. Please refer to the ESD documentation on "my X-FAB":
"Basic ESD Guidelines"
"XH018 ESD Protection Device and Latch-up Guidelines"
"XH018 MOS TLP I-V Characteristics"
"XH018 TLP I-V Characteristics"

3. Parameters

This section contains geometrical and electrical parameters that have been extracted primarily from measurements within the fabrication process or from special process monitor structures placed along the scribe lane.

Parameters which describe temperature dependence have been extracted in the temperature range 27°C< T < 175°C. All the other measurements have been done at T0 = 27°C, unless otherwise stated.

The specified limits of the dispositional pass/fail process parameters:
LSL Lower Specification Limit
USL Upper Specification Limit

describe the parameter ranges of the delivered wafer quality. These parameter ranges are based on the 6 sigma values of the parameter distribution. These specification limits are the basis for Cp and Cpk evaluations.

For the following process parameters, the LSL and USL limits do not reflect the statistics of the process but merely represent that the value(s) pass(es) the particular limit:

- Parameters which are marked by a corresponding note

The stated LSL or USL limits of those parameters are selection limits only and are not allowed for Cp and Cpk evaluations.

For process parameters having a normal distribution, the Low and High values are the 3 sigma values of the parameter distribution.

For process parameters having a non-normal distribution, the Low and High values encompass the same fraction of the distribution as a +/- 3 sigma range would include for a normal distribution.

Designers may use the Low and High values to understand circuit sensitivities, but for more robust designs the wider parameter ranges available in the LSL and USL values should be used. Note that all of these values are also available in the simulation models.

For the following process parameters, the Low and High values (where quoted) do not reflect process statistics:

- Breakdown voltages having Low value only,
- Punch-through voltages,
- Structural and geometrical parameters except gate oxide thickness,
- Wafer material parameters,
- Field threshold voltage parameters,
- Parasitic capacitance parameters,
- Junction diode capacitance parameters,
- Off-state leakage parameters,
- Temperature coefficient parameters,
- Parameters which are marked by a corresponding note;

The device parameters must not be used for circuit simulation purposes. They are extracted from simplified model equations in order to increase the speed of the measurements. Special circuit simulation device parameters are related to the Process Related Guideline "Simulation Models" These are extracted from the complete set of model equations in order to give the best fit of the entire characteristic for all operating points. Therefore, device parameters may differ from their corresponding circuit simulation device parameters.

The breakdown voltage parameters within this section do not describe the allowed operating voltages of the devices. For maximum operating voltages required for reliable device operation, please refer to device operating conditions.

Only a subset of the parameters is measured regularly. The complete set of parameters is only available for wafers with updated process control monitor test structures.

Characteristic curves of the primitive devices showing measurement results of a typical wafer in comparison to the SPICE model simulations are available in the Device Characteristics Documentation (formerly Model Guides) on "my X-FAB."

Operating Conditions

Functional operation of the device at conditions between maximum operating conditions and absolute maximum (or between minimum and absolute minimum) is not implied. Exposure to these conditions for extended periods may affect device reliability (e.g. hot carrier degradation, oxide breakdown). Applying conditions beyond absolute values may be destructive to the devices.

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In addition to the stated operating conditions, the process reliability parameters must also be considered. These include lifetimes and detailed SOA descriptions.

Parasitics have the same maximum operating voltage as the primitive device they exist within.

Junction Temperature

The junction temperature range is defined as:
Operating conditions: Tj = -40°C … +175°C
Absolute maximum ratings: Tj = -55°C / +185°C

3.1 LPMOS main module

3.1.1 Device independent parameters

Structural and geometrical parameters

Name	Description	Low	Typ	High	Unit
EPS_ILD1	metal 1 / substrate equivalent dielectric constant	-	4	-	-
	Note: The values for dielectric permittivity are mean values only, because the dielectric consists of a stack of layers each with a different permittivity				
EPS_IMD1	metal 1 / metal 2 equivalent dielectric constant	-	4	-	-
	Note: The values for dielectric permittivity are mean values only, because the dielectric consists of a stack of layers each with a different permittivity				
RSWAFE	epi wafer: epi layer resistivity	13.5	15	16.5	Ωcm
RSWAFS	epi wafer: wafer substrate resistivity	-	0.01	-	Ωcm
THD_ILD1	metal 1 - active dielectric thickness	840	990	1140	nm
THD_IMD1	metal 2 - metal 1 dielectric thickness	765	850	935	nm
THD_M1P1	metal 1 - poly 1 dielectric thickness	640	790	940	nm
THD_M1STI	metal 1 field dielectric thickness	1240	1390	1540	nm
THGN	1.8V gate oxide thickness (measured on NMOS capacitor)	3.9	4.1	4.3	nm
THGN3	3.3V gate oxide thickness (measured on NMOS capacitor)	6.2	6.5	6.8	nm
THGP	1.8V gate oxide thickness (measured on PMOS capacitor)	3.7	3.9	4.1	nm
THGP3	3.3V gate oxide thickness (measured on PMOS capacitor)	6	6.3	6.6	nm
THV	passivation thickness	1570	1750	1930	nm
	Note: Passivation is composed from the following stack (bottom to top): silicon oxide/silicon nitride.				
THV_THK	passivation thickness with METTHK module	1920	2200	2480	nm
	Note: Passivation is composed from the following stack (bottom to top): silicon oxide/silicon nitride.				
TH_EPI	epi wafer: epi layer thickness	-	10	-	µm
TH_M1	metal 1 thickness	505	565	625	nm
TH_M2	metal 2 thickness	505	565	625	nm
TH_P1	poly 1 thickness	180	200	220	nm
TH_WAF	wafer thickness (without epi layer)	710	725	740	µm
XJ_N	N+ source/ drain junction depth	-	0.2	-	µm
XJ_NW1	NWELL1 junction depth	-	1.5	-	µm
XJ_NW2	NWELL2 junction depth	-	1.5	-	µm

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Name	Description	Low	Typ	High	Unit
XJ_P	P+ source/ drain junction depth	-	0.2	-	µm
XT_STI	STI depth	360	400	440	nm

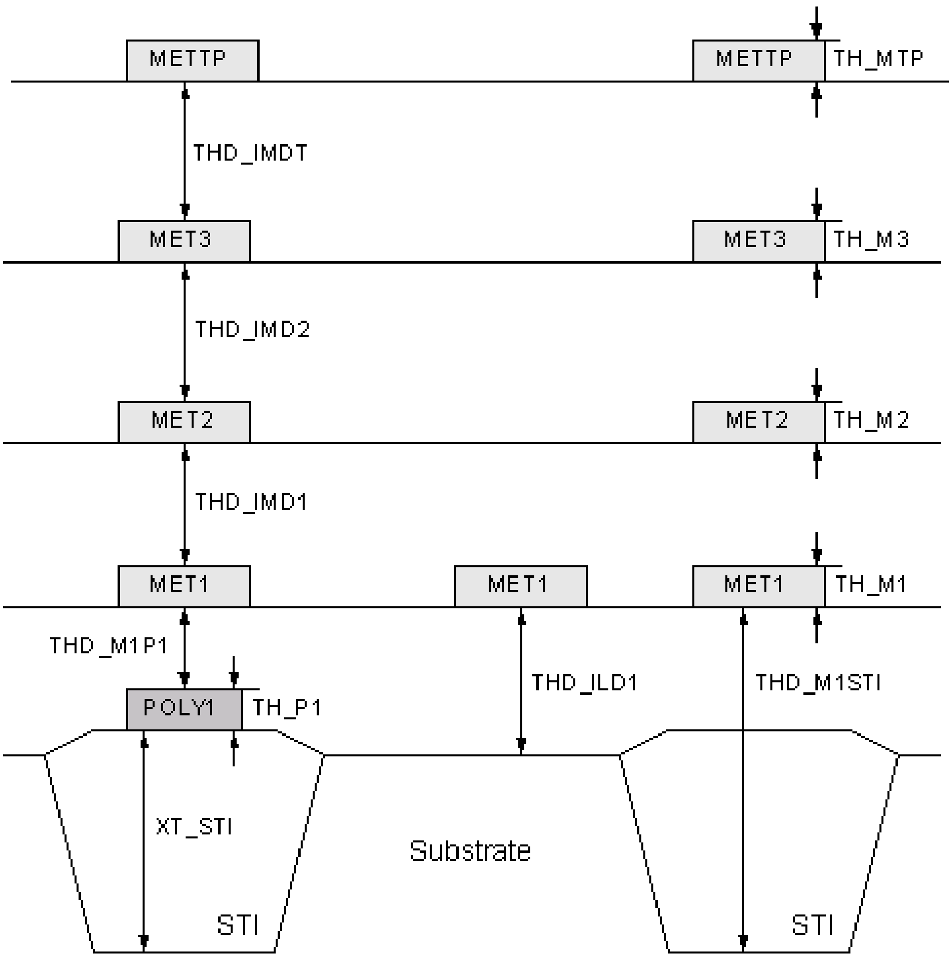

Figure 3.1 Cross-Sectional diagram showing layer thickness values

Note: The values for dielectric permittivity are mean values only, because the dielectric consists of a stack of layers each with a different permittivity.

Parasitic field parameters

Negative values are considered as absolute values for their limits.

Name	Description	Low	Typ	High	Unit
VTFNM1PW1	n-channel threshold voltage metal 1 on field over PWELL1 @ VD=1.8V, Id=1µA, L=0.28µm, W=210µm	40	-	-	V
VTFNM1PW2	n-channel threshold voltage metal 1 on field over PWELL2 @ VD=3.3V, Id=1µA, L=0.28µm, W=210µm	40	-	-	V
VTFNM2PW1	n-channel threshold voltage metal 2 on field over PWELL1 @ VD=1.8V, Id=1µA, L=0.28µm, W=210µm	70	-	-	V
VTFNM2PW2	n-channel threshold voltage metal 2 on field over PWELL2 @ VD=3.3V, Id=1µA, L=0.28µm, W=210µm	70	-	-	V
VTFNP1PW1	n-channel threshold voltage poly 1 on field over PWELL1 @ VD=1.8V, Id=1µA, L=0.28µm, W=210µm	8	-	-	V

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Name	Description	Low	Typ	High	Unit
VTFNP1PW2	n-channel threshold voltage poly 1 on field over PWELL2, @ VD=3.3V, Id=1µA, L=0.28µm, W=210µm	8	-	-	V
VTFPM1NW1	p-channel threshold voltage metal 1 on field over NWELL1, @ VD=-1.8V, Id=-1µA, L=0.28µm, W=210µm	-40	-	-	V
VTFPM1NW2	p-channel threshold voltage metal 1 on field over NWELL2 @ VD=-3.3V, Id=-1µA, L=0.28µm, W=210µm	-40	-	-	V
VTFPM2NW1	p-channel threshold voltage metal 2 on field over NWELL1 @ VD=-1.8V, Id=-1µA, L=0.28µm, W=210µm	-70	-	-	V
VTFPM2NW2	p-channel threshold voltage metal 2 on field over NWELL2, @ VD=-3.3V, Id=-1µA, L=0.28µm, W=210µm	-70	-	-	V
VTFPP1NW1	p-channel threshold voltage poly 1 on field over NWELL1 @ VD=-1.8V, Id=-1µA, L=0.28µm, W=210µm	-8	-	-	V
VTFPP1NW2	p-channel threshold voltage poly 1 on field over NWELL2 @ VD=-3.3V, Id=-1µA, L=0.28µm, W=210µm	-8	-	-	V

Sheet and contact resistance parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RCTNDM	metal 1 - N+ contact resistance	-	5.5	7.5	9.8	12	Ω/cnt
RCTNMP1	metal 1 - N+ poly 1 contact resistance	-	5.5	7.5	9.8	12	Ω/cnt
RCTPDM	metal 1 - P+ contact resistance	-	5.5	7.5	9.8	12	Ω/cnt
RCTPMP1	metal 1 - P+ poly 1 contact resistance	-	5.5	7.5	9.8	12	Ω/cnt
RSRNNS	NDIFF (salicided) sheet resistance	3.3	4.8	6.3	7.8	9.3	Ω/□
RSRNP1S	N+ poly 1 (salicided) sheet resistance	-	-	8.1	-	-	Ω/□
RSRNW1	NWELL1 sheet resistance (STI terminated)	790	880	970	1060	1150	Ω/□
RSRNW23	NWELL2 sheet resistance (STI terminated)	790	880	970	1060	1150	Ω/□
RSRPPS	PDIFF (salicided) sheet resistance	3.9	5.4	6.9	8.4	9.9	Ω/□
RSR_M1	metal 1 sheet resistance	61	69	77	85	93	mΩ/□
RSR_M2	metal 2 sheet resistance	58	66	74	82	90	mΩ/□
RVI_V1	VIA1 resistance	-	3	4.5	6.75	9	Ω/via
TC1_CT	contact resistance temperature coefficient 1	-	-	2.15	-	-	1e-03/K
TC1_V1	VIA1 resistance temperature coefficient 1	-	-	1.1	-	-	1e-03/K
TC2_CT	contact resistance temperature coefficient 2	-	-	0	-	-	1e-06/K²
TC2_V1	VIA1 resistance temperature coefficient 2	-	-	0	-	-	1e-06/K²
WERNNS	NDIFF (salicided) effective width @ W=0.42µm	-	0.4	0.46	0.52	-	µm
WERNP1S	N+ poly 1 (salicided) effective width @ W=0.42µm	-	0.22	0.28	0.34	-	µm
WERPPS	PDIFF (salicided) effective width @ W=0.42µm	-	0.39	0.45	0.51	-	µm

Note: The values of the sheet resistances (except for the metals) depend on the used operating conditions. For detailed information, refer to the simulation models.

Gate oxide parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDON	1.8V NMOS gate oxide breakdown voltage @ Ibr=0.1nA/µm²	4.5	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BDON3	3.3V NMOS gate oxide breakdown voltage @ Ibr=0.1nA/µm²	6	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BDOP	1.8V PMOS gate oxide breakdown voltage @ Ibr=0.1nA/µm²	4.1	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BDOP3	3.3V PMOS gate oxide breakdown voltage @ Ibr=0.1nA/µm²	6	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CGAN	1.8V NMOS gate oxide area capacitance @ Vbias=1.8V	-	8.06	8.46	8.91	-	fF/µm²
CGAN3	3.3V NMOS gate oxide area capacitance @ Vbias=3.6V	-	5.09	5.29	5.5	-	fF/µm²
CGAP	1.8V PMOS gate oxide area capacitance @ Vbias=-1.8V	8.05	8.46	8.91	9.4	9.95	fF/µm²
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CGAP3	3.3V PMOS gate oxide area capacitance @ Vbias=-3.6V	5.05	5.25	5.46	5.69	5.93	fF/µm²
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CGON	1.8V NMOS gate – source/drain overlap	-	-	0.33	-	-	fF/µm
CGON3	3.3V NMOS gate – source/drain overlap	-	-	0.23	-	-	fF/µm
CGOP	1.8V PMOS gate – source/drain overlap	-	-	0.32	-	-	fF/µm
CGOP3	3.3V PMOS gate – source/drain overlap	-	-	0.22	-	-	fF/µm

Parasitic capacitance parameters

The following table provides a principal overview with respect to interconnect capacitances.

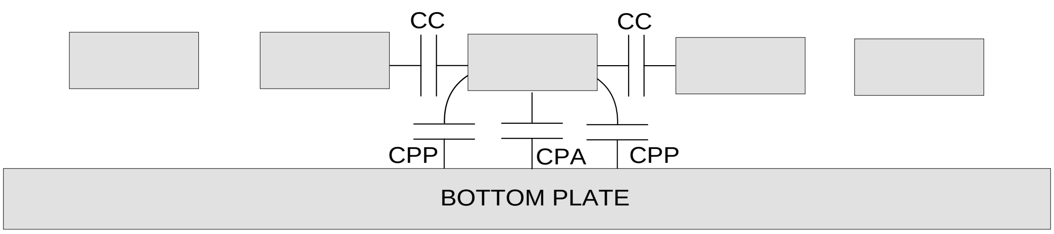

Figure 3.2 Parasitic capacitance structure

Name	Description	Typ	Unit
CC_M1M1	coupling capacitance metal 1 – metal 1	113	aF/µm
CC_M2M2	coupling capacitance metal 2 – metal 2	97	aF/µm
CC_P1P1	coupling capacitance poly 1 – poly 1	56	aF/µm

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Name	Description	Typ	Unit
CPAM1DIFF	metal 1 – active area capacitance	35.9	aF/µm²
CPAM1P1	metal 1 – poly 1 area capacitance	45.4	aF/µm²
CPAM1STI	metal 1 – field area (STI) area capacitance	25.6	aF/µm²
CPAM2DIFF	metal 2 – active area capacitance	14.6	aF/µm²
CPAM2M1	metal 2 – metal 1 area capacitance	41.5	aF/µm²
CPAM2P1	metal 2 – poly 1 area capacitance	16	aF/µm²
CPAM2STI	metal 2 – field area (STI) area capacitance	12.5	aF/µm²
CPASTI	poly 1 – field area (STI) area capacitance	88.5	aF/µm²
CPPM1DIFF	metal 1 – active perimeter capacitance	10.3	aF/µm
CPPM1P1	metal 1 – poly 1 perimeter capacitance	7.8	aF/µm
CPPM1STI	metal 1 – field area (STI) perimeter capacitance	9.2	aF/µm
CPPM2DIFF	metal 2 – active perimeter capacitance	7.9	aF/µm
CPPM2M1	metal 2 – metal 1 perimeter capacitance	8.3	aF/µm
CPPM2P1	metal 2 – poly 1 perimeter capacitance	5	aF/µm
CPPM2STI	metal 2 – field area (STI) perimeter capacitance	7.6	aF/µm
CPPSTI	poly 1 – field area (STI) perimeter capacitance	15.1	aF/µm

Physical layer operating conditions

Name	Structure	Temp. range	Abs. min	Min	Max	Abs. max	Unit
JMax_CT_DC(1	Contact	-40°C to 175°C	-	-	0.53	-	mA/cnt
JMax_DC(1	Poly 1	-40°C to 175°C	-	-	1	-	mA/µm
JMax_DC(2 (1	Metal 1	-40°C to 175°C	-	-	1	20	mA/µm
JMax_DC(2 (1	Metal 2	-40°C to 175°C	-	-	1	20	mA/µm
JMax_N_DC(3 (1	Metal 1	-40°C to 175°C	-	-	0.5	20	mA/µm
JMax_N_DC(3 (1	Metal 2	-40°C to 175°C	-	-	0.5	20	mA/µm
JMax_VI_DC(1	Via 1	-40°C to 175°C	-	-	0.28	20	mA/via
JMax_CT_AC(4	Contact	-40°C to 175°C	-	-	2.4	-	mA/cnt
JMax_AC(2 (4	Metal 1	-40°C to 175°C	-	-	4.5	20	mA/µm
JMax_AC(2 (4	Metal 2	-40°C to 175°C	-	-	4.5	20	mA/µm
JMax_N_AC(3 (4	Metal 1	-40°C to 175°C	-	-	2.2	20	mA/µm
JMax_N_AC(3 (4	Metal 2	-40°C to 175°C	-	-	2.2	20	mA/µm
JMax_VI_AC(4	Via 1	-40°C to 175°C	-	-	1.3	20	mA/via
T_Factor_1e4(5 (6	Contact	-40°C to 85°C	-	4.25	-	-	-
T_Factor_1e4(5 (6	Metal 1	-40°C to 85°C	-	3.13	-	-	-
T_Factor_1e4(5 (6	Metal 2	-40°C to 85°C	-	3.13	-	-	-
T_Factor_1e4(5 (6	Via 1	-40°C to 85°C	-	4.25	-	-	-
T_Factor_1e4(7 (6	Contact	85°C to 125°C	-	1.16	-	-	-
T_Factor_1e4(7 (6	Metal 1	85°C to 125°C	-	1	-	-	-
T_Factor_1e4(7 (6	Metal 2	85°C to 125°C	-	1	-	-	-
T_Factor_1e4(7 (6	Via 1	85°C to 125°C	-	1.16	-	-	-
T_Factor_1e4(8 (6	Contact	125°C to 175°C	-	0.31	-	-	-

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Name	Structure	Temp. range	Abs. min	Min	Max	Abs. max	Unit
T_Factor_1e4[8,6]	Metal 1	125°C to 175°C	-	0.32	-	-	-
T_Factor_1e4[8,6]	Metal 2	125°C to 175°C	-	0.32	-	-	-
T_Factor_1e4[8,6]	Via 1	125°C to 175°C	-	0.31	-	-	-
T_Factor_1e5[5,6]	Contact	-40°C to 85°C	-	1.35	-	-	-
T_Factor_1e5[5,6]	Metal 1	-40°C to 85°C	-	1	-	-	-
T_Factor_1e5[5,6]	Metal 2	-40°C to 85°C	-	1	-	-	-
T_Factor_1e5[5,6]	Via 1	-40°C to 85°C	-	1.35	-	-	-
T_Factor_1e5[7,6]	Contact	85°C to 125°C	-	0.37	-	-	-
T_Factor_1e5[7,6]	Metal 1	85°C to 125°C	-	0.32	-	-	-
T_Factor_1e5[7,6]	Metal 2	85°C to 125°C	-	0.32	-	-	-
T_Factor_1e5[7,6]	Via 1	85°C to 125°C	-	0.37	-	-	-
T_Factor_1e5[8,6]	Contact	125°C to 175°C	-	0.1	-	-	-
T_Factor_1e5[8,6]	Metal 1	125°C to 175°C	-	0.1	-	-	-
T_Factor_1e5[8,6]	Metal 2	125°C to 175°C	-	0.1	-	-	-
T_Factor_1e5[8,6]	Via 1	125°C to 175°C	-	0.1	-	-	-

Note 1 Max values of JMAX*DC refer to rms/avg values. Abs. max values of JMAX*DC refer to peak values.

Note 2 track width > 0.44µm.

Note 3 track width ≤ 0.44µm.

Note 4 Max values of JMAX*AC refer to rms values. Abs. max values of JMAX*AC refer to peak values.

Note 5 The temperature correction factor remains constant at the stated value across the whole temperatures range.

Note 6 Temperature correction factors allow the scaling of the current density according to the required lifetime and temperature. For more detailed information, please refer to the Interconnect reliability sections of the SpecXplorer or Process Reliability Specification.

Note 7 The temperature correction factor is interpolated between given values for temperatures above 85°C.

Note 8 The temperature correction factor is interpolated between given values for temperatures above 125°C

3.1.2 Device parameters

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Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VGD	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDB	-40°C to 175°C	-0.5	0	1.98	2.3	V
VSB	-40°C to 175°C	-0.5	0	1.98	2.3	V

Note: The node B (BULK) is: PWELL1.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNES	drain-source breakdown @ VG=0V, Id=1µA, L=0.18µm	3.6	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						

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Name	Description	LSL	Low	Typ	High	USL	Unit
BEXNE	mobility exponent	-	-	-1.7	-	-	-
FC_NE	corner frequency @ VD=1.8V, Id=1µA, L=10µm, W=10µm	-	-	1.21	-	-	kHz
GAMNE	body factor long channel @ L=10µm, W=10µm	-	-	0.7	-	-	√V
IDSNES	saturation current @ VG=1.8V, VD=1.8V, L=0.18µm, W=10µm	340	407	475	543	610	µA/µm
IOFNES	off-state leakage @ VD=1.8V, L=0.18µm, W=10µm	-	-	-	3	-	pA/µm
ISBNES	bulk current @ VD=1.8V, L=0.18µm	-	-	0.05	-	-	µA/µm
KP_NE	gain factor long channel @ L=10µm, W=10µm	-	-	256	-	-	µA/V²
LEFNE	effective channel length @ L=0.18µm	-	-	0.16	-	-	µm
NOINE	Input referred noise @ VD=1.8V, Id=1µA, f=1Hz, L=10µm, W=10µm	-	-	11.2	-	-	µV.µm/ √(Hz)
STSNE	subthreshold slope @ VD=1.8V	-	-	12	-	-	decade/V
TC_VTXNE	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	-0.89	-	-	mV/K
U0_NE	effective mobility	-	-	307	-	-	cm²/Vs
VTINEL	threshold voltage long channel @ VD=0.1V, L=10µm, W=10µm	0.47	0.5	0.53	0.56	0.59	V
VTINES	threshold voltage short channel @ VD=0.1V, L=0.18µm, W=10µm	0.46	0.52	0.58	0.64	0.7	V
VTINESS	threshold voltage small channel @ VD=0.1V, L=0.18µm, W=0.22µm	-	-	0.45	-	-	V
VTXNES	extrapolated threshold voltage short channel @ VD=0.1V, L=0.18µm, W=10µm	-	-	0.65	-	-	V
WEFNE	effective channel width @ W=0.22µm	-	-	0.17	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTNE	Pelgrom coefficient gain factor mismatch	0.76	%µm
AIDNE00	Pelgrom coefficient ID mismatch @ VG-VT=0V	7.75	%µm
AIDNE01	Pelgrom coefficient ID mismatch @ VG-VT=0.1V	4.99	%µm
AIDNE02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	3.45	%µm
AIDNE04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	1.99	%µm
AIDNE06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	1.35	%µm
AIDNE08	Pelgrom coefficient ID mismatch @ VG-VT=0.8V	1.02	%µm
AIDNE10	Pelgrom coefficient ID mismatch @ VG-VT=1V	0.82	%µm
AIDNE14	Pelgrom coefficient ID mismatch @ VG-VT=1.4V	0.62	%µm
AVTNE	Pelgrom coefficient VT mismatch	4.89	mVµm
DLTNE	transistor delta length	0.02	µm
DWTNE	transistor delta width	0.05	µm

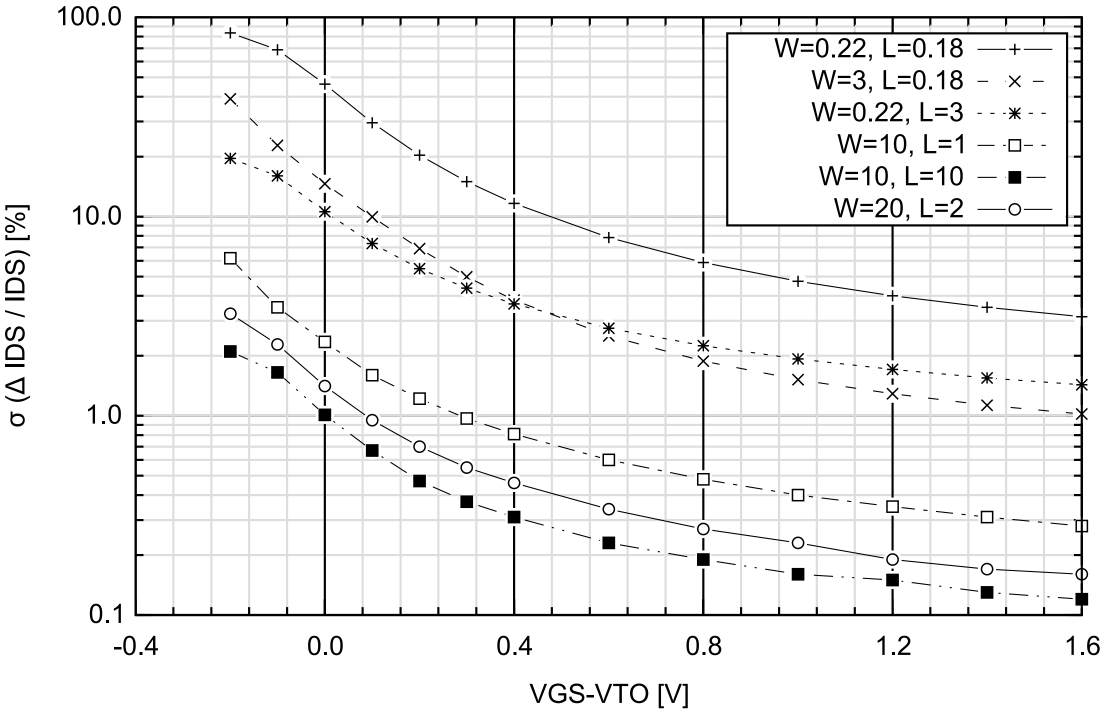

Figure 3.3 Device ne: drain current matching vs. VGS-VTO (typical values, drawn W and L)

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Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VGD	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDB	-40°C to 175°C	-2.3	-1.98	0	0.5	V
VSB	-40°C to 175°C	-2.3	-1.98	0	0.5	V
VBpsub	-40°C to 175°C	-0.5	0	1.98	2.3	V

Note: The node B (BULK) is: NWELL1.

Process parameters

Negative values are considered as absolute values for their limits.

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPES	drain-source breakdown @ VG=0V, Id=-1μA, L=0.18μm	3.6	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXPE	mobility exponent	-	-	-1	-	-	-
FC_PE	corner frequency @ VD=1.8V, Id=1μA, L=10μm, W=10μm	-	-	0.3	-	-	kHz
GAMPE	body factor long channel @ L=10μm, W=10μm	-	-	0.86	-	-	√V
IDSPES	saturation current @ VG=-1.8V, VD=-1.8V, L=0.18μm, W=10μm	110	140	170	200	230	μA/μm

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Name	Description	LSL	Low	Typ	High	USL	Unit
IOFPES	off-state leakage @ VD=-1.8V, L=0.18µm, W=10µm	-	-	-	3	-	pA/µm
ISBPES	bulk current @ VD=-1.8V, L=0.18µm	-	-	0.1	-	-	nA/µm
KP_PE	gain factor long channel @ L=10µm, W=10µm	-	-	52	-	-	µA/V²
LEFPE	effective channel length @ L=0.18µm	-	-	0.15	-	-	µm
NOIPE	Input referred noise @ VD=-1.8V, Id=-1µA, f=1Hz, L=10µm, W=10µm	-	-	17	-	-	µV.µm/√(Hz)
STSPE	subthreshold slope @ VD=-1.8V	-	-	11	-	-	decade/V
TC_VTXPE	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	0.91	-	-	mV/K
U0_PE	effective mobility	-	-	59	-	-	cm²/Vs
VTIPEL	threshold voltage long channel @ VD=-0.1V, L=10µm, W=10µm	-0.64	-0.67	-0.7	-0.73	-0.76	V
VTIPES	threshold voltage short channel @ VD=-0.1V, L=0.18µm, W=10µm	-0.55	-0.6	-0.65	-0.7	-0.75	V
VTIPESS	threshold voltage small channel @ VD=-0.1V, L=0.18µm, W=0.22µm	-	-	-0.6	-	-	V
VTXPES	extrapolated threshold voltage short channel @ VD=-0.1V, L=0.18µm, W=10µm	-	-	-0.65	-	-	V
WEFPE	effective channel width @ W=0.22µm	-	-	0.25	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTPE	Pelgrom coefficient gain factor mismatch	1.07	%µm
AIDPE00	Pelgrom coefficient ID mismatch @ VG-VT=0V	7.87	%µm
AIDPE01	Pelgrom coefficient ID mismatch @ VG-VT=0.1V	5.24	%µm
AIDPE02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	3.64	%µm
AIDPE04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	2.12	%µm
AIDPE06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	1.5	%µm
AIDPE08	Pelgrom coefficient ID mismatch @ VG-VT=0.8V	1.17	%µm
AIDPE10	Pelgrom coefficient ID mismatch @ VG-VT=1V	0.97	%µm
AIDPE14	Pelgrom coefficient ID mismatch @ VG-VT=1.4V	0.77	%µm
AVTPE	Pelgrom coefficient VT mismatch	5.03	mVµm
DLTPE	transistor delta length	0.03	µm
DWTPE	transistor delta width	-0.03	µm

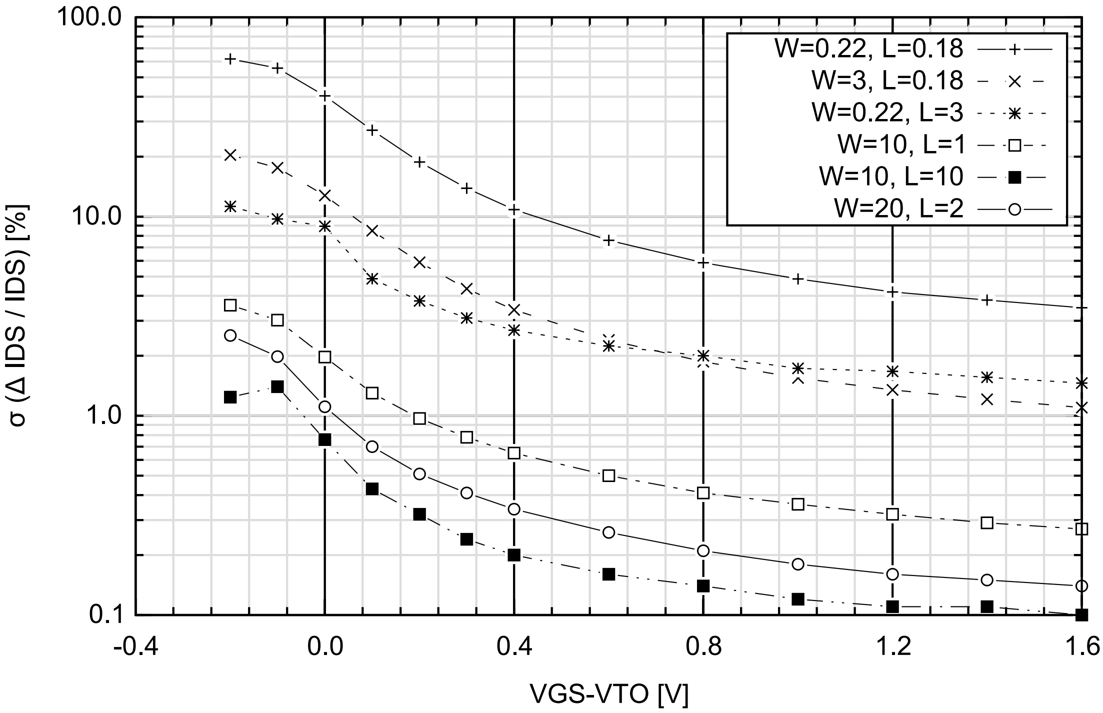

Figure 3.4 Device pe: drain current matching vs. VGS-VTO (typical values, drawn W and L)

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Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-4	-3.6	3.6	4	V
VGD	-40°C to 175°C	-4	-3.6	3.6	4	V
VDS	-40°C to 175°C	-4	-3.6	3.6	4	V
VDB	-40°C to 175°C	-0.5	0	3.6	4	V
VSB	-40°C to 175°C	-0.5	0	3.6	4	V

Note: The node B (BULK) is: PSUB

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNN3S	drain-source breakdown @ VG=-3.3V, Id=1µA, L=1µm	-	4	-	-	-	V
FC_NN3	corner frequency @ VD=3.3V, Id=1µA, L=10µm, W=10µm	-	-	0.98	-	-	kHz
GAMNN3	body factor long channel @ L=10µm, W=10µm	-	-	0.053	-	-	√V
IDSNN3S	saturation current @ VG=3.3V, VD=3.3V, L=1µm, W=10µm	560	605	650	695	740	µA/µm
KP_NN3	gain factor long channel @ L=10µm, W=10µm	-	-	260	-	-	µA/V²
LEFNN3	effective channel length @ L=1µm	-	-	0.85	-	-	µm
NOINN3	Input referred noise @ VD=3.3V, Id=1µA, f=1Hz, L=10µm, W=10µm	-	-	6.8	-	-	µV.µm/ √(Hz)

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Name	Description	LSL	Low	Typ	High	USL	Unit
VTXNN3L	extrapolated threshold voltage long channel @ VD=0.1V, L=10µm, W=10µm	-	-	-0.13	-	-	V
VTXNN3S	threshold voltage short channel @ VD=0.1V, L=1µm, W=10µm	-0.28	-0.23	-0.18	-0.13	-0.08	V
WEFNN3	effective channel width @ W=1µm	-	-	1	-	-	µm

Note: It is strongly recommended to use a channel length of ≥ 2µm when the nn3 is operated in the sub-threshold region.

Matching parameters

Name	Description	Typ	Unit
ABTNN3	Pelgrom coefficient gain factor mismatch	0.7	%µm
AIDNN300	Pelgrom coefficient ID mismatch @ VG-VT=0V	6.93	%µm
AIDNN302	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	4.75	%µm
AIDNN304	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	2.43	%µm
AIDNN306	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	1.56	%µm
AIDNN310	Pelgrom coefficient ID mismatch @ VG-VT=1V	0.91	%µm
AIDNN315	Pelgrom coefficient ID mismatch @ VG-VT=1.5V	0.64	%µm
AIDNN320	Pelgrom coefficient ID mismatch @ VG-VT=2V	0.49	%µm
AIDNN330	Pelgrom coefficient ID mismatch @ VG-VT=3V	0.4	%µm
AVTNN3	Pelgrom coefficient VT mismatch	4.42	mVµm
DLTNN3	transistor delta length	0.15	µm
DWTNN3	transistor delta width	0	µm

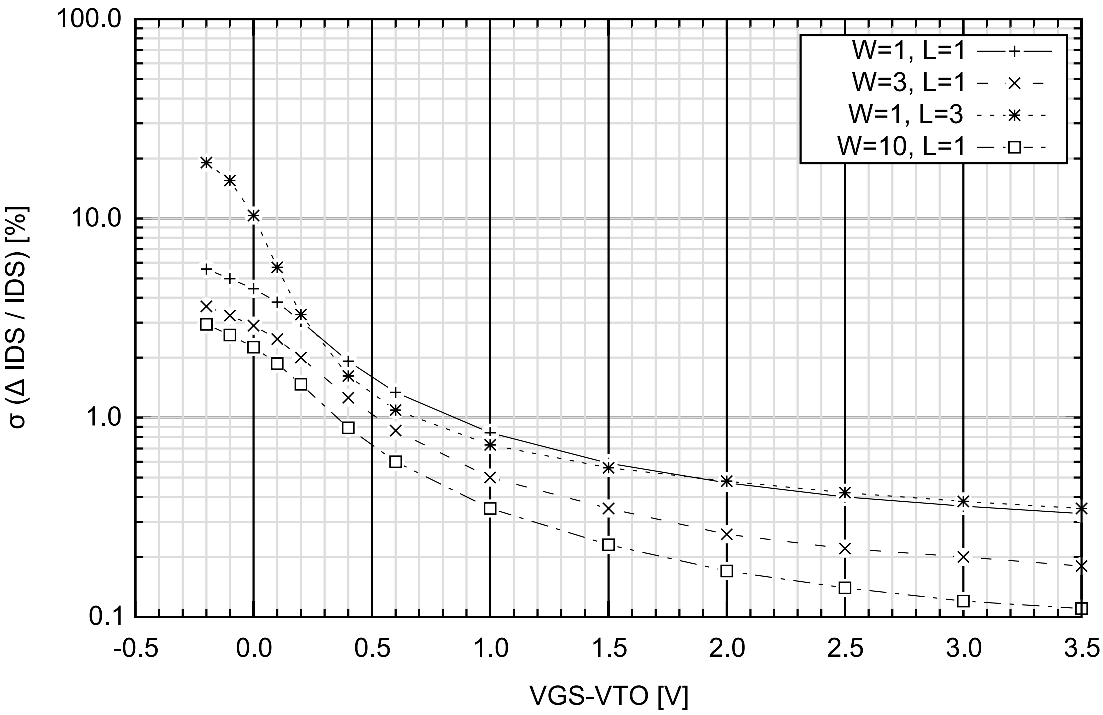

Figure 3.5 Device nn3: drain current matching vs. VGS-VTO (typical values, drawn W and L)

ne3

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-4	-3.6	3.6	4	V
VGD	-40°C to 175°C	-4	-3.6	3.6	4	V
VDS	-40°C to 175°C	-4	-3.6	3.6	4	V
VDB	-40°C to 175°C	-0.5	0	3.6	4	V
VSB	-40°C to 175°C	-0.5	0	3.6	4	V

Note: The node B (BULK) is: PWELL2

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNE3S	drain-source breakdown @ VG=0V, Id=1µA, L=0.35µm	5	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXNE3	mobility exponent	-	-	-1.7	-	-	-
FC_NE3	corner frequency @ VD=3.3V, Id=1µA, L=10µm, W=10µm	-	-	1.89	-	-	kHz
GAMNE3	body factor long channel @ L=10µm, W=10µm	-	-	0.92	-	-	√V
IDSNE3S	saturation current @ VG=3.3V, VD=3.3V, L=0.35µm, W=10µm	515	560	605	650	695	µA/µm
IOFNE3S	off-state leakage @ VD=3.3V, L=0.35µm, W=10µm	-	-	-	3	-	pA/µm
ISBNE3S	bulk current @ VD=3.3V, L=0.35µm	-	-	1	-	-	µA/µm
KP_NE3	gain factor long channel @ L=10µm, W=10µm	-	-	190	-	-	$\mu A/V^2$
LEFNE3	effective channel length @ L=0.35µm	-	-	0.33	-	-	µm
NOINE3	Input referred noise @ VD=3.3V, Id=1µA, f=1Hz, L=10µm, W=10µm	-	-	19.2	-	-	µV.µm/√(Hz)
STSNE3	subthreshold slope @ VD=3.3V	-	-	11	-	-	decade/V
TC_VTXNE3	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	-1	-	-	mV/K
U0_NE3	effective mobility	-	-	360	-	-	cm^2/Vs
VTINE3L	threshold voltage long channel @ VD=0.1V, L=10µm, W=10µm	0.6	0.63	0.66	0.69	0.72	V
VTINE3S	threshold voltage short channel @ VD=0.1V, L=0.35µm, W=10µm	0.61	0.65	0.69	0.73	0.77	V
VTINE3SS	threshold voltage small channel @ VD=0.1V, L=0.35µm, W=0.22µm	-	-	0.53	-	-	V
VTXNE3S	extrapolated threshold voltage short channel @ VD=0.1V, L=0.35µm, W=10µm	-	-	0.72	-	-	V
WEFNE3	effective channel width @ W=0.22µm	-	-	0.18	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTNE3	Pelgrom coefficient gain factor mismatch	0.98	%µm

⇒

Name	Description	Typ	Unit
AIDNE300	Pelgrom coefficient ID mismatch @ VG-VT=0V	12.7	%µm
AIDNE302	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	6.22	%µm
AIDNE304	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	3.57	%µm
AIDNE306	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	2.38	%µm
AIDNE310	Pelgrom coefficient ID mismatch @ VG-VT=1V	1.38	%µm
AIDNE315	Pelgrom coefficient ID mismatch @ VG-VT=1.5V	0.92	%µm
AIDNE320	Pelgrom coefficient ID mismatch @ VG-VT=2V	0.71	%µm
AIDNE330	Pelgrom coefficient ID mismatch @ VG-VT=3V	0.53	%µm
AVTNE3	Pelgrom coefficient VT mismatch	8.92	mVµm
DLTNE3	transistor delta length	0.02	µm
DWTNE3	transistor delta width	0.04	µm

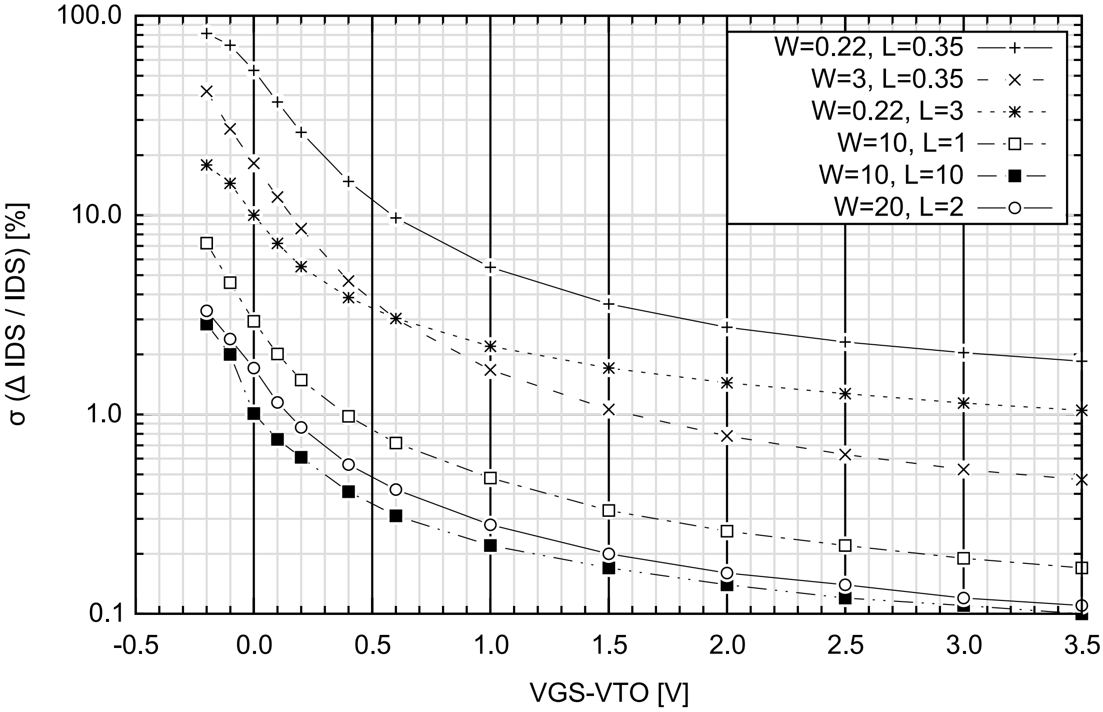

Figure 3.6 Device ne3: drain current matching vs. VGS-VTO (typical values, drawn W and L)

pe3, pe3_5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-4	-3.6	3.6	4	V
VGD	-40°C to 175°C	-4	-3.6	3.6	4	V
VDS	-40°C to 175°C	-4	-3.6	3.6	4	V
VDB	-40°C to 175°C	-4	-3.6	0	0.5	V
VSB	-40°C to 175°C	-4	-3.6	0	0.5	V
VBpsub	-40°C to 175°C	-0.5	0	3.6	4	V

Note: The node B (BULK) is: NWELL2.

Process parameters

Negative values are considered as absolute values for their limits.

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPE3S	drain-source breakdown @ VG=0V, Id=-1µA, L=0.3µm	5	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXPE3	mobility exponent	-	-	-1.1	-	-	-
FC_PE3	corner frequency @ VD=3.3V, Id=1µA, L=10µm, W=10µm	-	-	0.22	-	-	kHz
GAMPE3	body factor long channel @ L=10µm, W=10µm	-	-	0.86	-	-	√V
IDSPE3S	saturation current @ VG=-3.3V, VD=-3.3V, L=0.3µm, W=10µm	230	268	305	343	380	µA/µm
IOFPE3S	off-state leakage @ VD=-3.3V, L=0.3µm, W=10µm	-	-	-	3	-	pA/µm
ISBPE3S	bulk current @ VD=-3.3V, L=0.3µm	-	-	0.1	-	-	µA/µm
KP_PE3	gain factor long channel @ L=10µm, W=10µm	-	-	42	-	-	µA/V²
LEFPE3	effective channel length @ L=0.3µm	-	-	0.25	-	-	µm
NOIPE3	Input referred noise @ VD=-3.3V, Id=-1µA, f=1Hz, L=10µm, W=10µm	-	-	12.1	-	-	µV.µm/ √(Hz)
STSPE3	subthreshold slope @ VD=-3.3V	-	-	11	-	-	decade/V
TC_VTXPE3	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	1	-	-	mV/K
U0_PE3	effective mobility	-	-	77	-	-	cm²/Vs
VTIPE3L	threshold voltage long channel @ VD=-0.1V, L=10µm, W=10µm	-0.6	-0.63	-0.66	-0.69	-0.72	V
VTIPE3S	threshold voltage short channel @ VD=-0.1V, L=0.3µm, W=10µm	-0.55	-0.59	-0.63	-0.67	-0.71	V
VTIPE3SS	threshold voltage small channel @ VD=-0.1V, L=0.3µm, W=0.22µm	-	-	-0.6	-	-	V
VTXPE3S	extrapolated threshold voltage short channel @ VD=-0.1V, L=0.3µm, W=10µm	-	-	-0.58	-	-	V
WEFPE3	effective channel width @ W=0.22µm	-	-	0.22	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTPE3	Pelgrom coefficient gain factor mismatch	0.83	%µm
AIDPE300	Pelgrom coefficient ID mismatch @ VG-VT=0V	8.91	%µm
AIDPE302	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	4.05	%µm
AIDPE304	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	2.39	%µm
AIDPE306	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	1.68	%µm
AIDPE310	Pelgrom coefficient ID mismatch @ VG-VT=1V	1.09	%µm
AIDPE315	Pelgrom coefficient ID mismatch @ VG-VT=1.5V	0.8	%µm
AIDPE320	Pelgrom coefficient ID mismatch @ VG-VT=2V	0.66	%µm
AIDPE330	Pelgrom coefficient ID mismatch @ VG-VT=3V	0.53	%µm
AVTPE3	Pelgrom coefficient VT mismatch	5.56	mVµm
DLTPE3	transistor delta length	0.05	µm

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Name	Description	Typ	Unit
DWTPE3	transistor delta width	0	µm

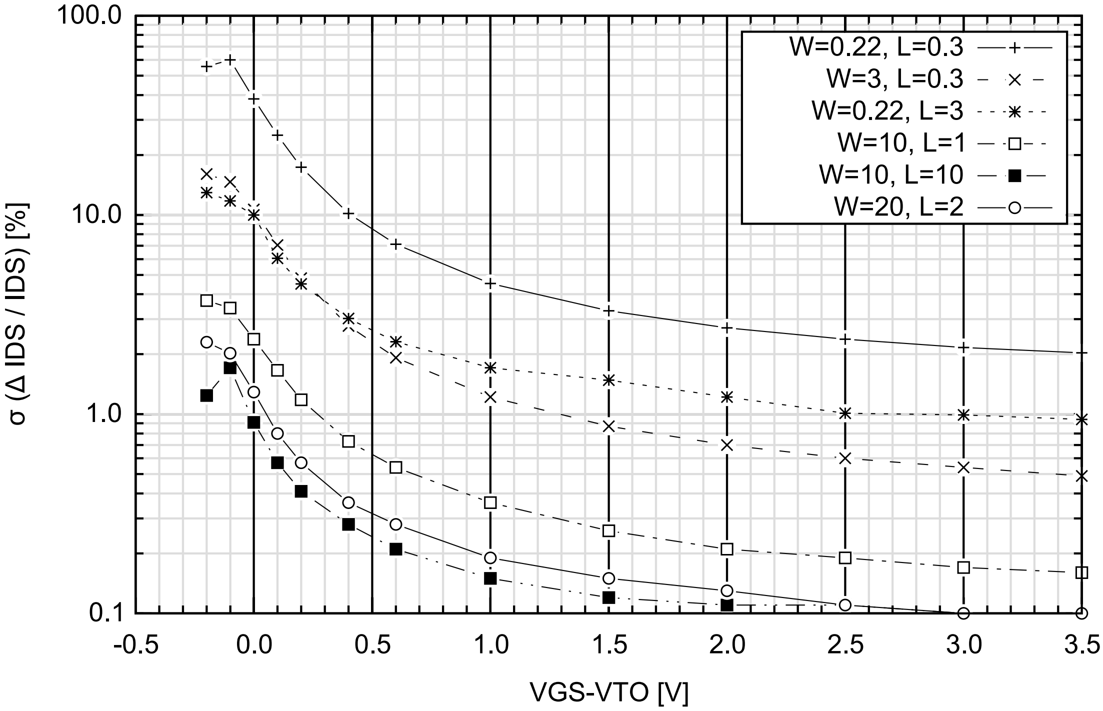

Figure 3.7 Device pe3: drain current matching vs. VGS-VTO (typical values, drawn W and L)

qpva

emitter area: 2x2µm^2

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VCE	-40°C to 175°C	-2.3	-1.98	0	0.5	V
VEB	-40°C to 175°C	-2.3	-1.98	1.5	-	V
VBC	-40°C to 175°C	-0.5	0	1.98	2.3	V

Process parameters

Name	Description	Typ	Unit
EVFPA	Early voltage @ Ib=-1µA	250	V
HFMPA	current gain @ Ie=1µA	2.5	-
VBEPA	base-emitter voltage @ Ie=1µA	710	mV

Matching parameters

Name	Description	Typ	Unit
SIBPA1	standard deviation IB mismatch @ Ic=100nA	1.55	%
SIBPA2	standard deviation IB mismatch @ Ic=10µA	1.47	%
SICPA1	standard deviation IC mismatch @ Ic=100nA	0.27	%
SICPA2	standard deviation IC mismatch @ Ic=10µA	0.23	%
SVBPA1	standard deviation VBE mismatch @ Ie=100nA	0.36	mV

⇒

Name	Description	Typ	Unit
SVBPA2	standard deviation VBE mismatch @ Ie=10µA	0.2	mV

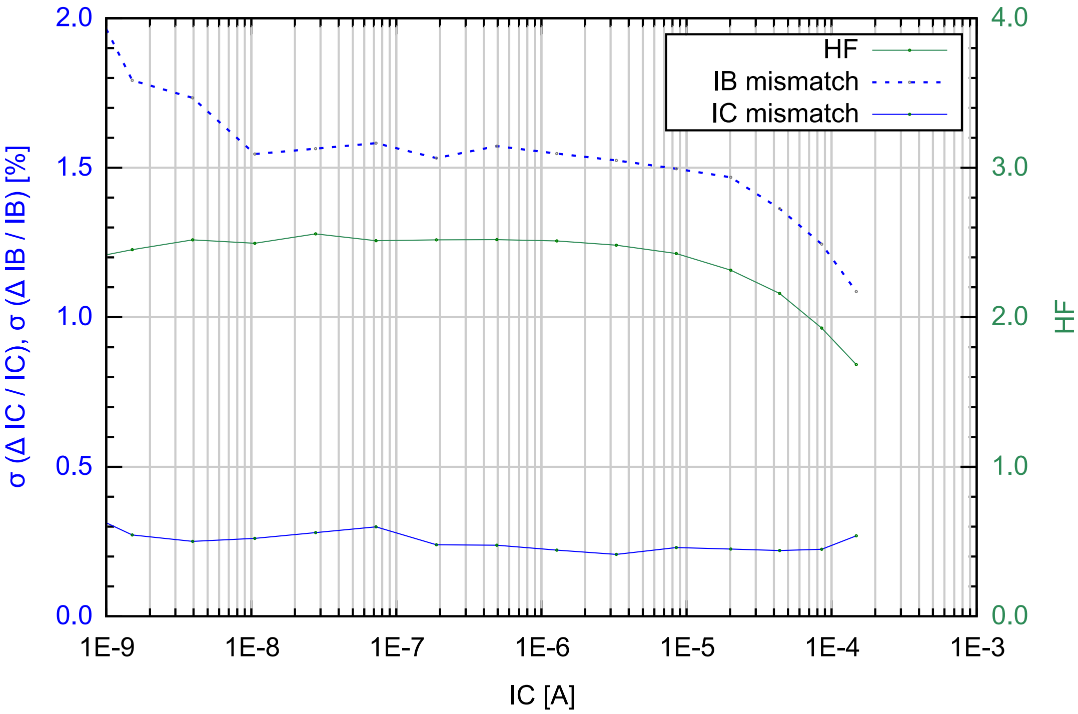

Figure 3.8 Device qpva: IC matching and IB matching vs. IC (typical values)

qpvb

emitter area: 5x5µm^2

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VCE	-40°C to 175°C	-2.3	-1.98	0	0.5	V
VEB	-40°C to 175°C	-2.3	-1.98	1.5	-	V
VBC	-40°C to 175°C	-0.5	0	1.98	2.3	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
EVFPB	Early voltage @ Ib=-1µA	-	-	150	-	-	V
HFMPB	current gain @ Ie=1µA	-	-	2.6	-	-	-
VBEPB	base-emitter voltage @ Ie=1µA	659	664	669	674	679	mV

Matching parameters

Name	Description	Typ	Unit
SIBPB1	standard deviation IB mismatch @ Ic=100nA	0.52	%
SIBPB2	standard deviation IB mismatch @ Ic=10µA	0.5	%
SICPB1	standard deviation IC mismatch @ Ic=100nA	0.13	%
SICPB2	standard deviation IC mismatch @ Ic=10µA	0.13	%
SVBPB1	standard deviation VBE mismatch @ Ie=100nA	0.26	mV

⇒

Name	Description	Typ	Unit
SVBPB2	standard deviation VBE mismatch @ Ie=10µA	0.12	mV

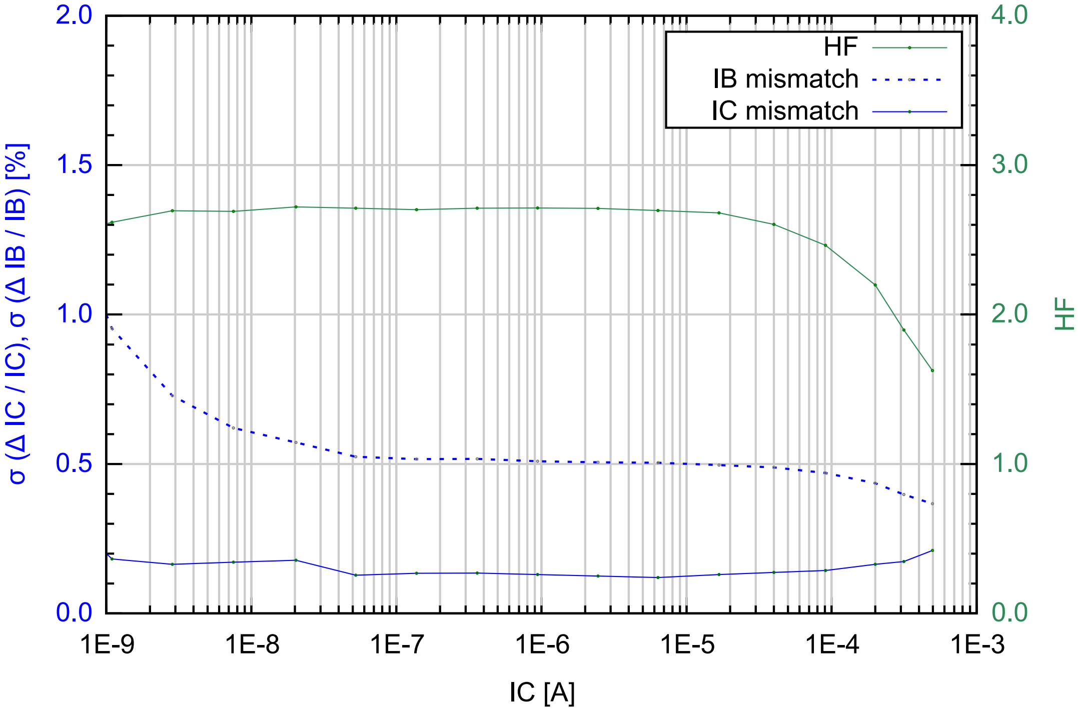

Figure 3.9 Device qpvb: IC matching and IB matching vs. IC (typical values)

qpvc

emitter area: 10x10µm^2

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VCE	-40°C to 175°C	-2.3	-1.98	0	0.5	V
VEB	-40°C to 175°C	-2.3	-1.98	1.5	-	V
VBC	-40°C to 175°C	-0.5	0	1.98	2.3	V

Process parameters

Name	Description	Typ	Unit
EVFPC	Early voltage @ Ib=-1µA	100	V
HFMPC	current gain @ Ie=1µA	2.8	-
VBEPC	base-emitter voltage @ Ie=1µA	636	mV

Matching parameters

Name	Description	Typ	Unit
SIBPC1	standard deviation IB mismatch @ Ic=100nA	0.23	%
SIBPC2	standard deviation IB mismatch @ Ic=10µA	0.23	%
SICPC1	standard deviation IC mismatch @ Ic=100nA	0.09	%
SICPC2	standard deviation IC mismatch @ Ic=10µA	0.11	%
SVBPC1	standard deviation VBE mismatch @ Ie=100nA	0.2	mV

⇒

Name	Description	Typ	Unit
SVBPC2	standard deviation VBE mismatch @ Ie=10µA	0.08	mV

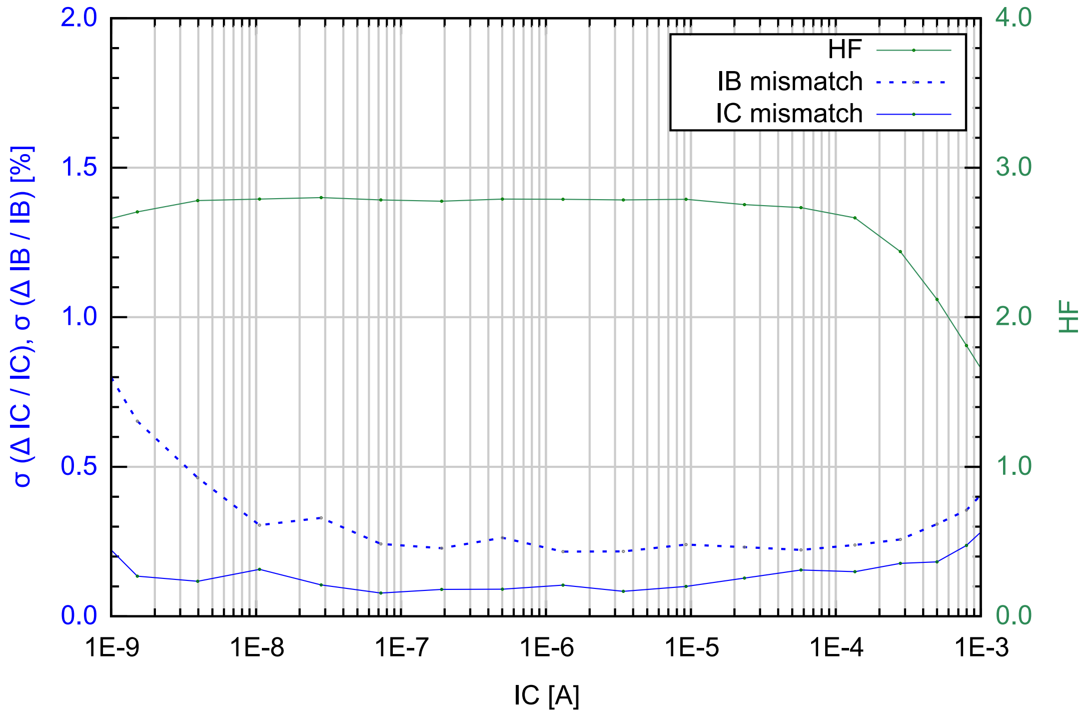

Figure 3.10 Device qpvc: IC matching and IB matching vs. IC (typical values)

qpva3

emitter area: 2x2µm^2

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VCE	-40°C to 175°C	-4	-3.6	0	0.5	V
VEB	-40°C to 175°C	-4	-3.6	1.5	-	V
VBC	-40°C to 175°C	-0.5	0	3.6	4	V

Process parameters

Name	Description	Typ	Unit
EVFPA3	Early voltage @ Ib=-1µA	250	V
HFMPA3	current gain @ Ie=1µA	2.3	-
VBEPA3	base-emitter voltage @ Ie=1µA	709	mV

Matching parameters

Name	Description	Typ	Unit
SIBPA31	standard deviation IB mismatch @ Ic=100nA	1.26	%
SIBPA32	standard deviation IB mismatch @ Ic=10µA	1.27	%
SICPA31	standard deviation IC mismatch @ Ic=100nA	0.25	%
SICPA32	standard deviation IC mismatch @ Ic=10µA	0.22	%
SVBPA31	standard deviation VBE mismatch @ Ic=100nA	0.32	mV

⇒

Name	Description	Typ	Unit
SVBPA32	standard deviation VBE mismatch @ Ic=10µA	0.16	mV

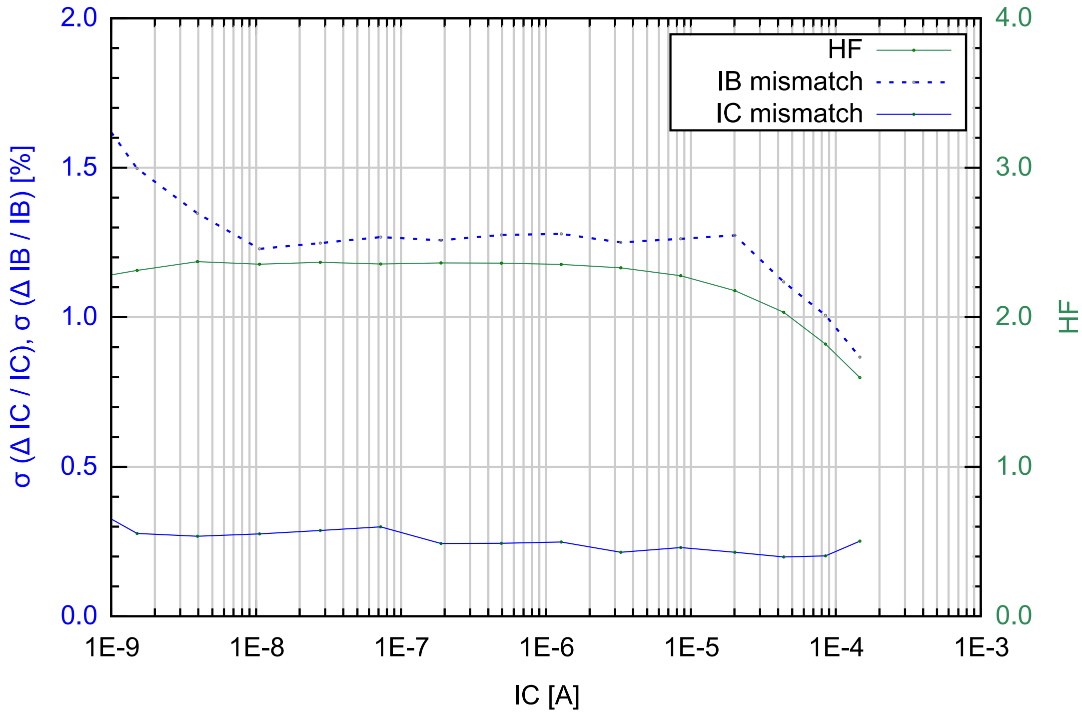

Figure 3.11 Device qpva3: IC matching and IB matching vs. IC (typical values)

qpvb3

emitter area: 5x5µm^2

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VCE	-40°C to 175°C	-4	-3.6	0	0.5	V
VEB	-40°C to 175°C	-4	-3.6	1.5	-	V
VBC	-40°C to 175°C	-0.5	0	3.6	4	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
EVFPB3	Early voltage @ Ib=-1µA	-	-	150	-	-	V
HFMPB3	current gain @ Ie=1µA	-	-	2.5	-	-	-
VBEPB3	base-emitter voltage @ Ie=1µA	659	664	669	674	679	mV

Matching parameters

Name	Description	Typ	Unit
SIBPB31	standard deviation IB mismatch @ Ic=100nA	0.5	%
SIBPB32	standard deviation IB mismatch @ Ic=10µA	0.46	%
SICPB31	standard deviation IB mismatch @ Ic=100nA	0.13	%
SICPB32	standard deviation IB mismatch @ Ic=10µA	0.14	%
SVBPB31	standard deviation VBE mismatch @ Ic=100nA	0.23	mV

⇒

Name	Description	Typ	Unit
SVBPB32	standard deviation VBE mismatch @ Ic=10μA	0.12	mV

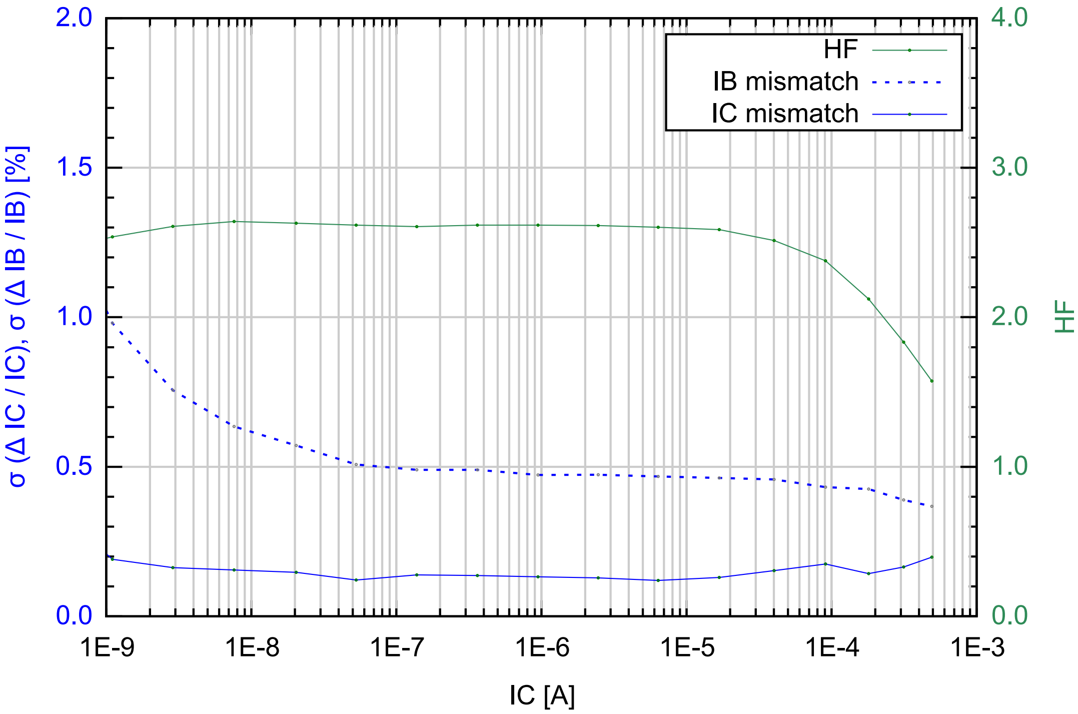

Figure 3.12 Device qpvb3: IC matching and IB matching vs. IC (typical values)

qpvc3

emitter area: 10x10μm^2

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VCE	-40°C to 175°C	-4	-3.6	0	0.5	V
VEB	-40°C to 175°C	-4	-3.6	1.5	-	V
VBC	-40°C to 175°C	-0.5	0	3.6	4	V

Process parameters

Name	Description	Typ	Unit
EVFPC3	Early voltage @ Ib=-1μA	100	V
HFMPC3	current gain @ Ie=1μA	2.7	-
VBEPC3	base-emitter voltage @ Ie=1μA	635	mV

Matching parameters

Name	Description	Typ	Unit
SIBPC31	standard deviation IB mismatch @ Ic=100nA	0.23	%
SIBPC32	standard deviation IB mismatch @ Ic=10μA	0.22	%
SICPC31	standard deviation IC mismatch @ Ic=100nA	0.11	%
SICPC32	standard deviation IC mismatch @ Ic=10μA	0.11	%
SVBPC31	standard deviation VBE mismatch @ Ic=100nA	0.19	mV

⇒

Name	Description	Typ	Unit
SVBPC32	standard deviation VBE mismatch @ Ic=10µA	0.09	mV

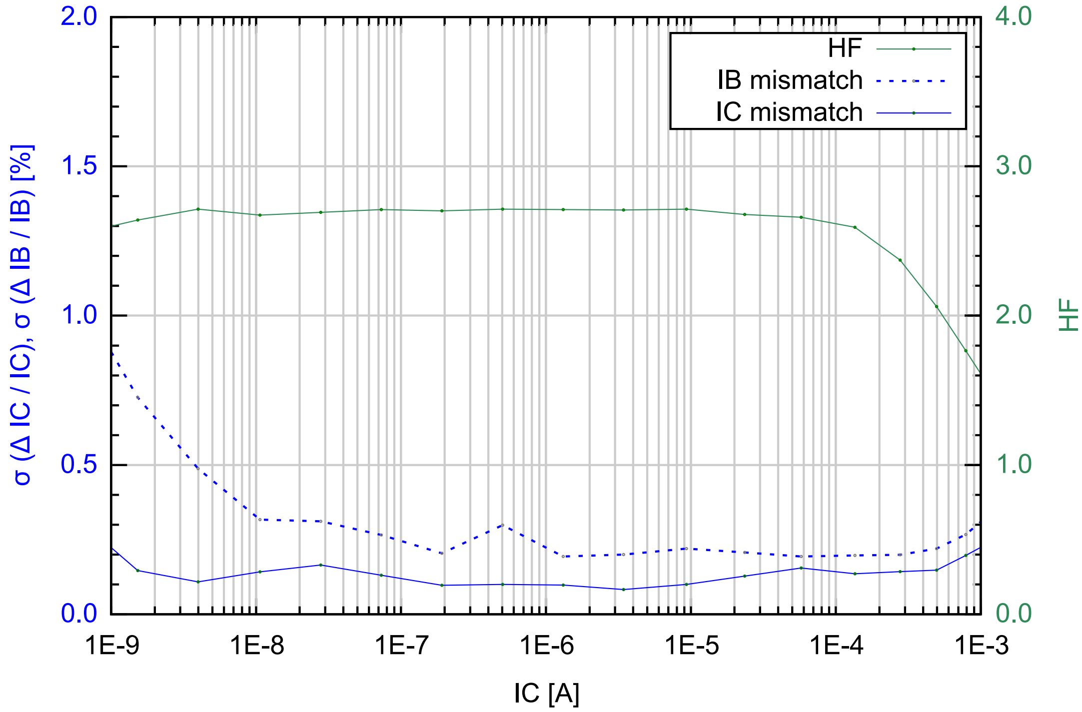

Figure 3.13 Device qpvc3: IC matching and IB matching vs. IC (typical values)

rdn

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-0.5	0	1.98	2.3	V

Note: The node B (BULK) is PWELL1

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSENNSB	NDIFF silicide block edge resistance per terminal	-	-	12	-	-	Ωµm
RSRNN	NDIFF sheet resistance	52	58	64	70	76	Ω/□
TC1NN	NDIFF temperature coefficient 1	-	1.3	1.42	1.54	-	1e-03/K
TC1NNRSE	NDIFF silicide block edge resistance temperature coefficient 1	-	-	0.27	-	-	1e-03/K
TC2NN	NDIFF temperature coefficient 2	-	0.35	0.7	1.05	-	1e-06/K²
TC2NNRSE	NDIFF silicide block edge resistance temperature coefficient 2	-	-	-1	-	-	1e-06/K²
WERNN	NDIFF effective width @ W=0.42µm	-	0.29	0.35	0.41	-	µm

Matching parameters

Name	Description	Typ	Unit
AR_NN	Pelgrom coefficient resistor mismatch	1.19	%µm

⇒

Name	Description	Typ	Unit
DWRNN	resistor delta width	0.07	µm

rdp

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VBpsub	-40°C to 175°C	-0.5	0	5.5	7	V
Vterm-bulk	-40°C to 175°C	-2.3	-1.98	0	0.5	V

Note: The node B (BULK) is NWELL1

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSEPPSB	PDIFF silicide block edge resistance per terminal	-	-	35	-	-	Ωµm
RSRPP	PDIFF sheet resistance	95	112	130	148	165	Ω/□
TC1PP	PDIFF temperature coefficient 1	-	1.2	1.3	1.4	-	1e-03/K
TC1PPRSE	PDIFF silicide block edge resistance temperature coefficient 1	-	-	-0.25	-	-	1e-03/K
TC2PP	PDIFF temperature coefficient 2	-	0.4	0.8	1.2	-	1e-06/K²
TC2PPRSE	PDIFF silicide block edge resistance temperature coefficient 2	-	-	-2	-	-	1e-06/K²
WERPP	PDIFF effective width @ W=0.42µm	-	0.26	0.32	0.38	-	µm

Matching parameters

Name	Description	Typ	Unit
AR_PP	Pelgrom coefficient resistor mismatch	1.3	%µm
DWRPP	resistor delta width	0.1	µm

rnw

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-0.5	0	5.5	7	V

Note: The node B (BULK) is PSUB

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSRNW1	NWELL1 sheet resistance (STI terminated)	790	880	970	1060	1150	Ω/□
TC1NW1	NWELL1 temperature coefficient 1	-	2.6	2.9	3.2	-	1e-03/K
TC2NW1	NWELL1 temperature coefficient 2	-	7.4	9.2	11	-	1e-06/K²
WERNW1	NWELL1 effective width @ W=2µm	-	1.6	1.75	1.9	-	µm

Matching parameters

Name	Description	Typ	Unit
AR_NW1	Pelgrom coefficient resistor mismatch	0.61	%µm

⇒

Name	Description	Typ	Unit
DWRNW1	resistor delta width	0.25	µm

rdn3

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-0.5	0	3.6	4	V

Note: The node B (BULK) is PWELL2

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSENN3SB	NDIFF3 silicide block edge resistance per terminal	-	-	12	-	-	Ωµm
RSRNN3	NDIFF3 sheet resistance	49	55	61	67	73	Ω/□
TC1NN3	NDIFF3 temperature coefficient 1	-	1.3	1.42	1.54	-	1e-03/K
TC1NN3RSE	NDIFF3 silicide block edge resistance temperature coefficient 1	-	-	0.12	-	-	1e-03/K
TC2NN3	NDIFF3 temperature coefficient 2	-	0.35	0.7	1.05	-	1e-06/K²
TC2NN3RSE	NDIFF3 silicide block edge resistance temperature coefficient 1	-	-	-0.3	-	-	1e-06/K²
WERNN3	NDIFF3 effective width @ W=0.42µm	-	0.29	0.35	0.41	-	µm

Matching parameters

Name	Description	Typ	Unit
AR_NN3	Pelgrom coefficient resistor mismatch	1.12	%µm
DWRNN3	resistor delta width	0.07	µm

rdp3

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VBpsub	-40°C to 175°C	-0.5	0	5.5	7	V
Vterm-bulk	-40°C to 175°C	-4	-3.6	0	0.5	V

Note: The node B (BULK) is NWELL2

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSEPP3SB	PDIFF3 silicide block edge resistance per terminal	-	-	35	-	-	Ωµm
RSRPP3	PDIFF3 sheet resistance	90	107	125	143	160	Ω/□
TC1PP3	PDIFF3 temperature coefficient 1	-	1.2	1.3	1.4	-	1e-03/K
TC1PP3RSE	PDIFF3 silicide block edge resistance temperature coefficient 1	-	-	-0.28	-	-	1e-03/K
TC2PP3	PDIFF3 temperature coefficient 2	-	0.4	0.8	1.2	-	1e-06/K²
TC2PP3RSE	PDIFF3 silicide block edge resistance temperature coefficient 2	-	-	-3	-	-	1e-06/K²
WERPP3	PDIFF3 effective width @ W=0.42µm	-	0.24	0.3	0.36	-	µm

Matching parameters

Name	Description	Typ	Unit
AR_PP3	Pelgrom coefficient resistor mismatch	1.31	%µm
DWRPP3	resistor delta width	0.12	µm

rnw3

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-0.5	0	5.5	7	V

Note: The node B (BULK) is PSUB

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSRNW23	NWELL2 sheet resistance (STI terminated)	790	880	970	1060	1150	Ω/□
TC1NW2	NWELL2 temperature coefficient 1	-	2.6	2.9	3.2	-	1e-03/K
TC2NW2	NWELL2 temperature coefficient 2	-	7.4	9.2	11	-	1e-06/K²
WERNW23	NWELL2 effective width @ W=2µm	-	1.6	1.75	1.9	-	µm

Matching parameters

Name	Description	Typ	Unit
AR_NW2	Pelgrom coefficient resistor mismatch	0.59	%µm
DWRNW2	resistor delta width	0.25	µm

rnp1, rnp1_3

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk(1	-40°C to 175°C	-50	-45	45	50	V
JDL	-40°C to 175°C	-	-	0.45	-	mA/µm

Note 1 An inversion layer is formed in the bulk underneath the poly if the terminal-to-bulk voltage exceeds the field threshold voltage. Field threshold voltages are specified in the "Parameters" section

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSENP1SB	N+ poly 1 silicide block edge resistance per terminal	-	-	65	-	-	Ωµm
RSRNP1	N+ poly 1 sheet resistance	200	260	320	380	440	Ω/□
TC1NP1	N+ poly 1 temperature coefficient 1	-	-1.55	-1.38	-1.21	-	1e-03/K
TC1NP1RSE	N+ poly 1 silicide block edge resistance temperature coefficient 1	-	-	-1.4	-	-	1e-03/K
TC2NP1	N+ poly 1 temperature coefficient 2	-	1.7	2.3	2.9	-	1e-06/K²
TC2NP1RSE	N+ poly 1 silicide block edge resistance temperature coefficient 2	-	-	0.3	-	-	1e-06/K²
VCBNP1	N+ poly 1 bulk voltage coefficient	-	-	0.08	-	-	1e-03/V
WERNP1	N+ poly 1 effective width @ W=0.42µm	-	0.26	0.32	0.38	-	µm

Matching parameters

Name	Description	Typ	Unit
AR_NP1	Pelgrom coefficient resistor mismatch	3.4	%µm
DWRNP1	resistor delta width	0.1	µm

rpp1, rpp1_3

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk(1	-40°C to 175°C	-50	-45	45	50	V
JDL	-40°C to 175°C	-	-	0.45	-	mA/µm

Note 1 An inversion layer is formed in the bulk underneath the poly if the terminal-to-bulk voltage exceeds the field threshold voltage. The field threshold voltages are specified in section "3. Process & Device Parameters".

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSEPP1SB	P+ poly 1 silicide block edge resistance per terminal	-	-	70	-	-	Ωµm
RSRPP1	P+ poly 1 sheet resistance	220	250	280	310	340	Ω/☐
TC1PP1	P+ poly 1 temperature coefficient 1	-	-0.17	-0.11	-0.05	-	1e-03/K
TC1PP1RSE	P+ poly 1 silicide block edge resistance temperature coefficient 1	-	-	-1.2	-	-	1e-03/K
TC2PP1	P+ poly 1 temperature coefficient 2	-	0.5	0.7	0.9	-	1e-06/K^2
TC2PP1RSE	P+ poly 1 silicide block edge resistance temperature coefficient 2	-	-	0.2	-	-	1e-06/K^2
VCBPP1	P+ poly 1 bulk voltage coefficient	-	-	-0.05	-	-	1e-03/V
WERPP1	P+ poly 1 effective width @ W=0.42µm	-	0.3	0.36	0.42	-	µm

Matching parameters

Name	Description	Typ	Unit
AR_PP1	Pelgrom coefficient resistor mismatch	1.49	%µm
DWRPP1	resistor delta width	0.06	µm

rpp1s, rpp1s_3

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk(1	-40°C to 175°C	-50	-45	45	50	V

Note 1 An inversion layer is formed in the bulk underneath the poly if the terminal-to-bulk voltage exceeds the field threshold voltage. The field threshold voltages are specified in section "3. Process & Device Parameters".

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSRPP1S	P+ poly 1 (salicided) sheet resistance	5.2	6.35	7.5	8.65	9.8	Ω/☐
TC1PP1S	P+ poly 1 (salicided) temperature coefficient 1	-	2.56	2.92	3.28	-	1e-03/K

⇒

Name	Description	LSL	Low	Typ	High	USL	Unit
TC2PP1S	P+ poly 1 (salicided) temperature coefficient 2	-	-0.25	0.95	2.15	-	1e-06/K²
WERPP1S	P+ poly 1 (salicided) effective width @ W=0.18µm	-	0.18	0.21	0.24	-	µm

Matching parameters

Name	Description	Typ	Unit
AR_PP1S	Pelgrom coefficient resistor mismatch	1.46	%µm
DWRPP1S	resistor delta width	-0.03	µm

rnp1h, rnp1h_3

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk[1]	-40°C to 175°C	-50	-45	45	50	V
JDL	-40°C to 175°C	-	-	0.1	-	mA/µm

Note 1 An inversion layer is formed in the bulk underneath the poly if the terminal-to-bulk voltage exceeds the field threshold voltage. The field threshold voltages are specified in section "3. Process & Device Parameters".

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSRNP1H	high-ohmic N-doped poly 1 sheet resistance	4.8	5.35	6.3	7.05	7.8	kΩ/☐
TC1NP1H	high-ohmic N-doped poly 1 temperature coefficient 1	-	-4.4	-4	-3.6	-	1e-03/K
TC2NP1H	high-ohmic N-doped poly 1 temperature coefficient 2	-	11	12.5	14	-	1e-06/K²
VCBNP1H	high-ohmic N-doped poly 1 bulk voltage coefficient	-	-	0.35	-	-	1e-03/V
WERNP1H	high-ohmic N-doped poly 1 effective width @ W=0.42µm	-	0.31	0.37	0.43	-	µm

Matching parameters

Name	Description	Typ	Unit
AR_NP1H	Pelgrom coefficient resistor mismatch	2.63	%µm
DWRNP1H	resistor delta width	0.05	µm

rm1

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-50	-45	45	50	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSR_M1	metal 1 sheet resistance	61	69	77	85	93	mΩ/☐
TC1_MET	metal 1 / metal 2 temperature coefficient 1	-	-	3.4	-	-	1e-03/K

⇒

Name	Description	LSL	Low	Typ	High	USL	Unit
TC2_MET	metal 1 / metal 2 temperature coefficient 2	-	-	0	-	-	1e-06/K²
WER_M1B	metal 1 effective width @ W=0.23µm	-	0.18	0.21	0.24	-	µm

rm2

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-50	-45	45	50	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSR_M2	metal 2 sheet resistance	58	66	74	82	90	mΩ/☐
TC1_MET	metal 1 / metal 2 temperature coefficient 1	-	-	3.4	-	-	1e-03/K
TC2_MET	metal 1 / metal 2 temperature coefficient 2	-	-	0	-	-	1e-06/K²
WER_M2	metal 2 effective width @ W=0.28µm	-	0.2	0.24	0.28	-	µm

mosvc

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGB	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VBpsub	-40°C to 175°C	-0.5	0	5.5	7	V

Process parameters

Name	Description	Typ	Unit
CNV_MVC	varactor capacitance at negative voltage @ Vterm=-1.8V, f=100kHz	2.6	fF/µm²
CPV_MVC	varactor capacitance at positive voltage @ Vterm=1.8V, f=100kHz	8.1	fF/µm²
TUR_MVC	tuning range @ Vlow=-1.8V, Vhigh=1.8V, f=100kHz	70	%

mosvc3

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGB	-40°C to 175°C	-2.3	-1.98	3.6	4	V
VBpsub	-40°C to 175°C	-0.5	0	5.5	7	V

Process parameters

Name	Description	Typ	Unit
CNV_MVC3	varactor capacitance at negative voltage @ Vterm=-1.8V, f=100kHz	1.7	fF/µm²
CPV_MVC3	varactor capacitance at positive voltage @ Vterm=3.3V, f=100kHz	5	fF/µm²
TUR_MVC3	tuning range @ Vlow=-1.8V, Vhigh=3.3V, f=100kHz	70	%

csf2p

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk[1	-40°C to 175°C	-50	-45	45	50	V
Vterm1-Vterm2	-40°C to 175°C	-7	-5.5	5.5	7	V

Note 1 An inversion layer is formed in the bulk underneath the poly if the terminal-to-bulk voltage exceeds the field threshold voltage.The field threshold voltages are specified in section "3. Process & Device Parameters".

Process parameters

Name	Description	Low	Typ	High	Unit
BDO_SFP2	csf2p breakdown voltage @ Ibr=1µA	15	-	-	V
CA_SFP2_B	csf2p capacitance per cell @ Vbias=0V, L=10.8µm, W=4.48µm	22.8	25.2	27.6	fF
IL_SFP2	csf2p leakage current @ VL=5.5V	-	-	50	fA/cell
TC1_SFP2	csf2p temperature coefficient 1 @ Tnom=27°C	-	0.25	-	1e-03/K
TC2_SFP2	csf2p temperature coefficient 2 @ Tnom=27°C	-	-1.2	-	1e-06/K²
VC1_SFP2	csf2p capacitor voltage coefficient 1	-	81	-	ppm/V
VC2_SFP2	csf2p capacitor voltage coefficient 2	-	100	-	ppm/V²

Matching parameters

Name	Description	Low	Typ	High	Unit
SC_SFP2	standard deviation capacitor mismatch	-	0.06	0.08	%
	Note: The values of this parameter do not reflect the statistics of the process. The high value corresponds to 1 unit cell; the typical value is valid for >= 8 unit cells.				

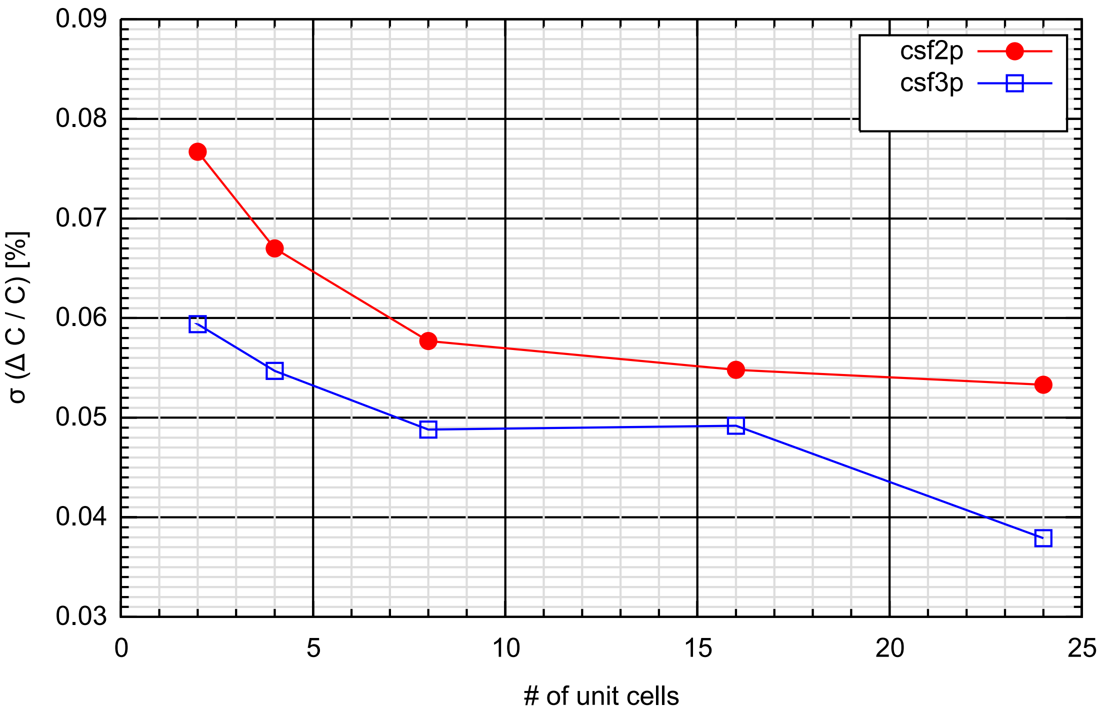

Figure 3.14 Device csf2p, csf3p: capacitor matching vs. number of fringe cap unit cells (typical values)

dn

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-2.3	-1.98	0	0.5	V

Note: The Junction diodes must not be used in forward operation for normal operation mode.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVJNPW1	breakdown voltage NDIFF / PWELL1 @ Irev=1µA	6	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CJANPW1	area junction capacitance	-	-	1.11	-	-	fF/µm²
CJPNPW1	sidewall junction capacitance	-	-	0.09	-	-	fF/µm
ILANPW1	area leakage current @ Vrev=1.98V, T=27°C	-	-	0.042	-	-	fA/µm²
ILANPW1HT	area leakage current @ Vrev=1.98V, T=175°C	-	-	0.75	-	-	pA/µm²
ILPNPW1	sidewall leakage current @ Vrev=1.98V, T=27°C	-	-	0.06	-	-	fA/µm
ILPNPW1HT	sidewall leakage current @ Vrev=1.98V, T=175°C	-	-	0.59	-	-	pA/µm
MJANPW1	area grading coefficient	-	-	0.4	-	-	-
MJPNPW1	sidewall grading coefficient	-	-	0.61	-	-	-
PBANPW1	area junction potential	-	-	0.75	-	-	V
PBPNPW1	sidewall junction potential	-	-	0.8	-	-	V

Note: dn is also used as parasitic diode p_dn.

dp

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode[1]	-40°C to 175°C	-2.3	-1.98	0	0.5	V

Note 1 Isolated from P-substrate by dnw.

Note: The Junction diodes must not be used in forward operation for normal operation mode.

Note: For diodes which are isolated from the P-substrate, please also refer to the operating conditions for the isolating diode.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVJPNW1	breakdown voltage PDIFF / NWELL1 @ Irev=-1µA	6	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CJAPNW1	area junction capacitance	-	-	1.02	-	-	fF/µm²
CJPPNW1	sidewall junction capacitance	-	-	0.06	-	-	fF/µm
ILAPNW1	area leakage current @ Vrev=-1.98V, T=27°C	-	-	0.002	-	-	fA/µm²

⇒

Name	Description	LSL	Low	Typ	High	USL	Unit
ILAPNW1HT	area leakage current @ Vrev=-1.98V, T=175°C	-	-	0.35	-	-	pA/µm²
ILPPNW1	sidewall leakage current @ Vrev=-1.98V, T=27°C	-	-	0.111	-	-	fA/µm
ILPPNW1HT	sidewall leakage current @ Vrev=-1.98V, T=175°C	-	-	0.34	-	-	pA/µm
MJAPNW1	area grading coefficient	-	-	0.37	-	-	-
MJPPNW1	sidewall grading coefficient	-	-	0.05	-	-	-
PBAPNW1	area junction potential	-	-	0.73	-	-	V
PBPPNW1	sidewall junction potential	-	-	0.82	-	-	V

Note: dp is also used as parasitic diode p_dp.

dnw

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-7	-5.5	0	0.5	V

Note: The Junction diodes must not be used in forward operation for normal operation mode.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVJNW1	breakdown voltage NWELL1 / PSUB @ Irev=1µA	9	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CJANW1	area junction capacitance	-	-	0.1	-	-	fF/µm²
CJPNW1	sidewall junction capacitance	-	-	0.49	-	-	fF/µm
ILANW1	area leakage current @ Vrev=5.5V, T=27°C	-	-	0.0001	-	-	fA/µm²
ILANW1HT	area leakage current @ Vrev=5.5V, T=175°C	-	-	1.15	-	-	pA/µm²
ILPNW1	sidewall leakage current @ Vrev=5.5V, T=27°C	-	-	0.174	-	-	fA/µm
ILPNW1HT	sidewall leakage current @ Vrev=5.5V, T=175°C	-	-	1.46	-	-	pA/µm
MJANW1	area grading coefficient	-	-	0.45	-	-	-
MJPNW1	sidewall grading coefficient	-	-	0.33	-	-	-
PBANW1	area junction potential	-	-	0.47	-	-	V
PBPNW1	sidewall junction potential	-	-	0.63	-	-	V

Note: dnw is also used as parasitic diode p_dnw.

dn3

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-4	-3.6	0	0.5	V

Note: The Junction diodes must not be used in forward operation for normal operation mode.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVJNPW2	breakdown voltage NDIFF / PWELL2 @ Irev=1µA	6	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CJANPW2	area junction capacitance	-	-	0.87	-	-	fF/µm²
CJPNPW2	sidewall junction capacitance	-	-	0.08	-	-	fF/µm
ILANPW2	area leakage current @ Vrev=3.6V, T=27°C	-	-	0.006	-	-	fA/µm²
ILANPW2HT	area leakage current @ Vrev=3.6V, T=175°C	-	-	0.8	-	-	pA/µm²
ILPNPW2	sidewall leakage current @ Vrev=3.6V, T=27°C	-	-	0.217	-	-	fA/µm
ILPNPW2HT	sidewall leakage current @ Vrev=3.6V, T=175°C	-	-	0.88	-	-	pA/µm
MJANPW2	area grading coefficient	-	-	0.33	-	-	-
MJPNPW2	sidewall grading coefficient	-	-	0.05	-	-	-
PBANPW2	area junction potential	-	-	0.71	-	-	V
PBPNPW2	sidewall junction potential	-	-	0.71	-	-	V

Note: dn3 is also used as parasitic diode p_dn3.

dp3

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode[1]	-40°C to 175°C	-4	-3.6	0	0.5	V

Note 1 Isolated from P-substrate by dnw3.

Note: The Junction diodes must not be used in forward operation for normal operation mode.

Note: For diodes which are isolated from the P-substrate, please also refer to the operating conditions for the isolating diode.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVJPNW2	breakdown voltage PDIFF / NWELL2 @ Irev=-1µA	6	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CJAPNW2	area junction capacitance	-	-	1.01	-	-	fF/µm²
CJPPNW2	sidewall junction capacitance	-	-	0.07	-	-	fF/µm
ILAPNW2	area leakage current @ Vrev=-3.6V, T=27°C	-	-	0.006	-	-	fA/µm²
ILAPNW2HT	area leakage current @ Vrev=-3.6V, T=175°C	-	-	0.38	-	-	pA/µm²
ILPPNW2	sidewall leakage current @ Vrev=-3.6V, T=27°C	-	-	0.374	-	-	fA/µm
ILPPNW2HT	sidewall leakage current @ Vrev=-3.6V, T=175°C	-	-	0.71	-	-	pA/µm
MJAPNW2	area grading coefficient	-	-	0.38	-	-	-
MJPPNW2	sidewall grading coefficient	-	-	0.05	-	-	-
PBAPNW2	area junction potential	-	-	0.73	-	-	V

⇒

Name	Description	LSL	Low	Typ	High	USL	Unit
PBPPNW2	sidewall junction potential	-	-	0.93	-	-	V

Note: dp3 is also used as parasitic diode p_dp3.

dnw3

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-7	-5.5	0	0.5	V

Note: The Junction diodes must not be used in forward operation for normal operation mode.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVJNW2	breakdown voltage NWELL2 / PSUB @ Irev=1µA	9	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CJANW2	area junction capacitance	-	-	0.1	-	-	fF/µm²
CJPNW2	sidewall junction capacitance	-	-	0.49	-	-	fF/µm
ILANW2	area leakage current @ Vrev=5.5V, T=27°C	-	-	0.0001	-	-	fA/µm²
ILANW2HT	area leakage current @ Vrev=5.5V, T=175°C	-	-	1.04	-	-	pA/µm²
ILPNW2	sidewall leakage current @ Vrev=5.5V, T=27°C	-	-	0.171	-	-	fA/µm
ILPNW2HT	sidewall leakage current @ Vrev=5.5V, T=175°C	-	-	1.37	-	-	pA/µm
MJANW2	area grading coefficient	-	-	0.45	-	-	-
MJPNW2	sidewall grading coefficient	-	-	0.34	-	-	-
PBANW2	area junction potential	-	-	0.52	-	-	V
PBPNW2	sidewall junction potential	-	-	0.65	-	-	V

Note: dnw3 is also used as parasitic diode p_dnw3.

dnn3

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-4	-3.6	0	0.5	V

Process parameters

Name	Description	Typ	Unit
CJANN3	area junction capacitance	0.07	fF/µm²
CJPNN3	sidewall junction capacitance	0.17	fF/µm
ILANN3	area leakage current @ Vrev=3.6V, T=27°C	0.033	fA/µm²
ILANN3HT	area leakage current @ Vrev=3.6V, T=175°C	17.4	pA/µm²
ILPNN3	sidewall leakage current @ Vrev=3.6V, T=27°C	0.121	fA/µm
ILPNN3HT	sidewall leakage current @ Vrev=3.6V, T=175°C	12	pA/µm
MJANN3	area grading coefficient	0.95	-

⇒

Name	Description	Typ	Unit
MJPNN3	sidewall grading coefficient	0.06	-
PBANN3	area junction potential	0.54	V
PBPNN3	sidewall junction potential	0.54	V

dpol

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-50	-45	45	50	V
Vanode-Vcathode	-40°C to 175°C	-5	-3.6	1.5	-	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
VDFPIN	polysilicon diode forward voltage @ Idio=1µA, W=20µm	-	-	0.8	1.15	1.5	V
VR_PIN	diode reverse voltage @ Id=-100nA, W=20µm	10	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						

pfuse

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm1-Vterm2(1	-40°C to 175°C	-0.2	-0.1	0.1	0.2	V
Vterm1-Vterm2(2	-40°C to 175°C	-5	-3.6	3.6	5	V

Note 1 unprogrammed state

Note 2 programmed state

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RP_FUSE	programmed fuse resistance @ Vbias=3.3V	-	100	-	-	-	kΩ
	Note: The values of this parameter do not reflect the statistics of the process.						
RU_FUSE	unprogrammed fuse resistance @ Isupply=50µA	11	23	35	47	59	Ω

Note: For the primitive device pfuse, the programming conditions and further information are available in the "Application Note – EasyFuse" on "my X-FAB."

3.2 MET3 module

3.2.1 Device independent parameters

Structural and geometrical parameters

Name	Description	Low	Typ	High	Unit
EPS_IMD2	metal 2 / metal 3 equivalent dielectric constant	-	4	-	-
	Note: The values for dielectric permittivity are mean values only, because the dielectric consists of a stack of layers each with a different permittivity				
THD_IMD2	metal 3 – metal 2 dielectric thickness	765	850	935	nm
TH_M3	metal 3 thickness	505	565	625	nm

Sheet and contact resistance parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSR_M3	metal 3 sheet resistance	58	66	74	82	90	mΩ/☐
RVI_V2	VIA2 resistance	-	3	4.5	6.75	9	Ω/via
TC1_V234	VIA2,3,4 resistance temperature coefficient 1	-	-	1.1	-	-	1e-03/K
TC2_V234	VIA2,3,4 resistance temperature coefficient 2	-	-	0	-	-	1e-06/K²

Parasitic capacitance parameters

The following table provides a principal overview with respect to interconnect capacitances. More extensive data will be available on request.

Name	Description	Typ	Unit
CC_M3M3	coupling capacitance metal 3 – metal 3	98	aF/µm
CPAM3DIFF	metal 3 – active area capacitance	9.2	aF/µm²
CPAM3M1	metal 3 – metal 1 area capacitance	15.5	aF/µm²
CPAM3M2	metal 3 – metal 2 area capacitance	41.5	aF/µm²
CPAM3P1	metal 3 – poly 1 area capacitance	9.5	aF/µm²
CPAM3STI	metal 3 – field area (STI) area capacitance	8.3	aF/µm²
CPPM3DIFF	metal 3 – active perimeter capacitance	7.2	aF/µm
CPPM3M1	metal 3 – metal 1 perimeter capacitance	5	aF/µm
CPPM3M2	metal 3 – metal 2 perimeter capacitance	8.3	aF/µm
CPPM3P1	metal 3 – poly 1 perimeter capacitance	4.1	aF/µm
CPPM3STI	metal 3 – field area (STI) perimeter capacitance	7	aF/µm

Physical layer operating conditions

Name	Structure	Temp. range	Abs. min	Min	Max	Abs. max	Unit
JMax_DC(1 (2	Metal 3	-40°C to 175°C	-	-	1	20	mA/µm
JMax_N_DC(3 (2	Metal 3	-40°C to 175°C	-	-	0.5	20	mA/µm
JMax_VI_DC(2	Via 2	-40°C to 175°C	-	-	0.28	20	mA/via
JMax_AC(1 (4	Metal 3	-40°C to 175°C	-	-	4.5	20	mA/µm
JMax_N_AC(3 (4	Metal 3	-40°C to 175°C	-	-	2.2	20	mA/µm

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Name	Structure	Temp. range	Abs. min	Min	Max	Abs. max	Unit
JMax_VI_AC[4]	Via 2	-40°C to 175°C	-	-	1.3	20	mA/via
T_Factor_1e4[5,6]	Metal 3	-40°C to 85°C	-	3.13	-	-	-
T_Factor_1e4[5,6]	Via 2	-40°C to 85°C	-	4.25	-	-	-
T_Factor_1e4[7,6]	Metal 3	85°C to 125°C	-	1	-	-	-
T_Factor_1e4[7,6]	Via 2	85°C to 125°C	-	1.16	-	-	-
T_Factor_1e4[8,6]	Metal 3	125°C to 175°C	-	0.32	-	-	-
T_Factor_1e4[8,6]	Via 2	125°C to 175°C	-	0.31	-	-	-
T_Factor_1e5[5,6]	Metal 3	-40°C to 85°C	-	1	-	-	-
T_Factor_1e5[5,6]	Via 2	-40°C to 85°C	-	1.35	-	-	-
T_Factor_1e5[7,6]	Metal 3	85°C to 125°C	-	0.32	-	-	-
T_Factor_1e5[7,6]	Via 2	85°C to 125°C	-	0.37	-	-	-
T_Factor_1e5[8,6]	Metal 3	125°C to 175°C	-	0.1	-	-	-
T_Factor_1e5[8,6]	Via 2	125°C to 175°C	-	0.1	-	-	-

Note 1 track width > 0.44µm.

Note 2 Max values of JMAX*DC refer to rms/avg values. Abs. max values of JMAX*DC refer to peak values.

Note 3 track width ≤ 0.44µm.

Note 4 Max values of JMAX*AC refer to rms values. Abs. max values of JMAX*AC refer to peak values.

Note 5 The temperature correction factor remains constant at the stated value across the whole temperatures range.

Note 6 Temperature correction factors allow the scaling of the current density according to the required lifetime and temperature. For more detailed information, please refer to the Interconnect reliability sections of the SpecXplorer or Process Reliability Specification.

Note 7 The temperature correction factor is interpolated between given values for temperatures above 85°C.

Note 8 The temperature correction factor is interpolated between given values for temperatures above 125°C

3.2.2 Device parameters

rm3

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-50	-45	45	50	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSR_M3	metal 3 sheet resistance	58	66	74	82	90	mΩ/☐
TC1_M3	metal 3 temperature coefficient 1	-	-	3.4	-	-	1e-03/K
TC2_M3	metal 3 temperature coefficient 2	-	-	0	-	-	1e-06/K²
WER_M3	metal 3 effective width @ W=0.28µm	-	0.2	0.24	0.28	-	µm

csandwt3

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk[1]	-40°C to 175°C	-50	-45	45	50	V

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Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm1-Vterm2	-40°C to 175°C	-50	-45	45	50	V

Note 1 An inversion layer is formed in the bulk underneath the poly if the terminal-to-bulkvoltage exceeds the field threshold voltage.The field threshold voltages are specified in section "3. Parameters"

Process parameters

Name	Description	Low	Typ	High	Unit
CAA_SANDW3B	POLY1 / metal1/ metal2/ metal3 sandwich area capacitance @ Vbias=0V	0.125	0.155	0.185	fF/μm²
CAP_SANDW3	POLY1 / metal1/ metal2/ metal3 sandwich perimeter capacitance	-	0.055	-	fF/μm

Matching parameters

Name	Description	Typ	Unit
AC_SANDW3	Pelgrom coefficient capacitor mismatch	0.65	%μm

csf3p

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk[(1]	-40°C to 175°C	-50	-45	45	50	V
Vterm1-Vterm2	-40°C to 175°C	-7	-5.5	5.5	7	V

Note 1 An inversion layer is formed in the bulk underneath the poly if the terminal-to-bulk voltage exceeds the field threshold voltage.The field threshold voltages are specified in section "3. Parameters"

Process parameters

Name	Description	Low	Typ	High	Unit
BDO_SFP3	csf3p breakdown voltage @ Ibr=1μA	15	-	-	V
CA_SFP3_B	csf3p capacitance per cell @ Vbias=0V, L=10.8μm, W=4.48μm	33.2	36.8	40.4	fF
IL_SFP3	csf3p leakage current @ VL=5.5V	-	-	50	fA/cell
TC1_SFP3	csf3p temperature coefficient 1 @ Tnom=27°C	-	0.155	-	1e-03/K
TC2_SFP3	csf3p temperature coefficient 2 @ Tnom=27°C	-	-0.83	-	1e-06/K²
VC1_SFP3	csf3p capacitor voltage coefficient 1	-	80	-	ppm/V
VC2_SFP3	csf3p capacitor voltage coefficient 2	-	68	-	ppm/V²

Matching parameters

Name	Description	Low	Typ	High	Unit
SC_SFP3	standard deviation capacitor mismatch	-	0.05	0.065	%
	Note: The values of this parameter do not reflect the statistics of the process. The high value corresponds to 1 unit cell; the typical value is valid for >= 8 unit cells.				

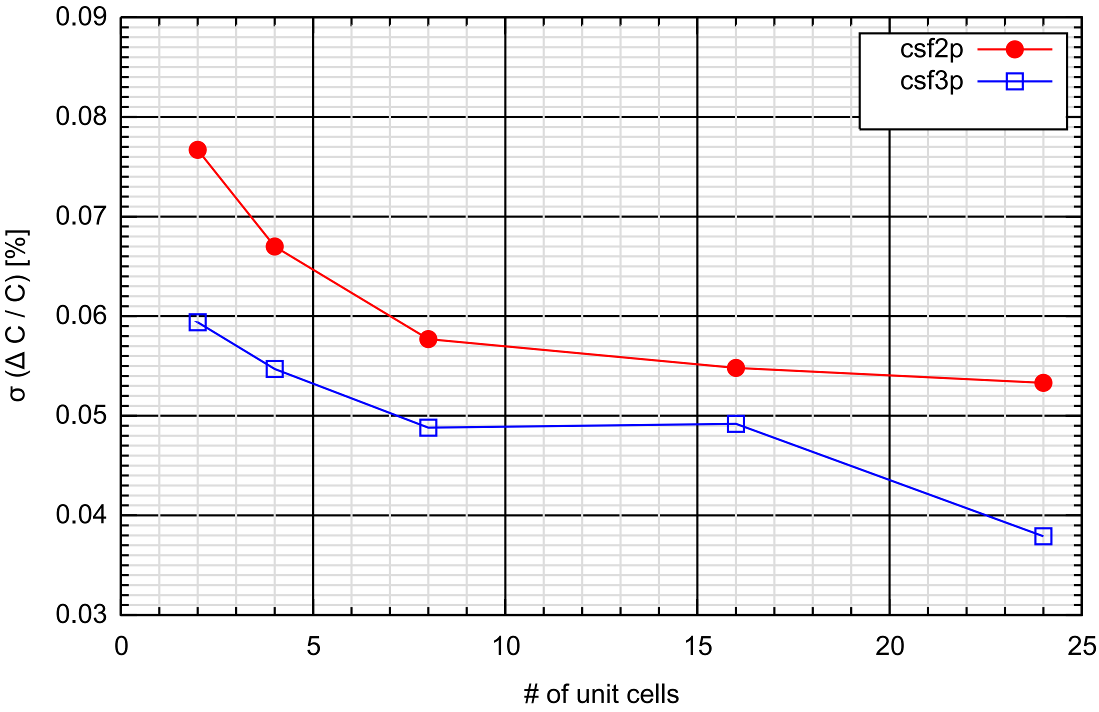

Figure 3.15 Device csf2p, csf3p: capacitor matching vs. number of fringe cap unit cells (typical values)

csf3

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-50	-45	45	50	V
Vterm1-Vterm2	-40°C to 175°C	-12	-10	10	12	V

Process parameters

Name	Description	Low	Typ	High	Unit
BDO_SF3	csf3 breakdown voltage @ Ibr=1μA	35	-	-	V
CA_SF3_B	csf3 capacitance per cell @ Vbias=0V, L=10.8μm, W=4.48μm	30.2	32.9	35.6	fF
IL_SF3	csf3 leakage current @ VL=10V	-	-	30	fA/cell
TC1_SF3	csf3 temperature coefficient 1 @ Tnom=27°C	-	-70	-	1e-06/K

Matching parameters

Name	Description	Low	Typ	High	Unit
SC_SF3	standard deviation capacitor mismatch	-	0.05	0.065	%
	Note: The values of this parameter do not reflect the statistics of the process. The high value corresponds to 1 unit cell; the typical value is valid for >= 8 unit cells.				

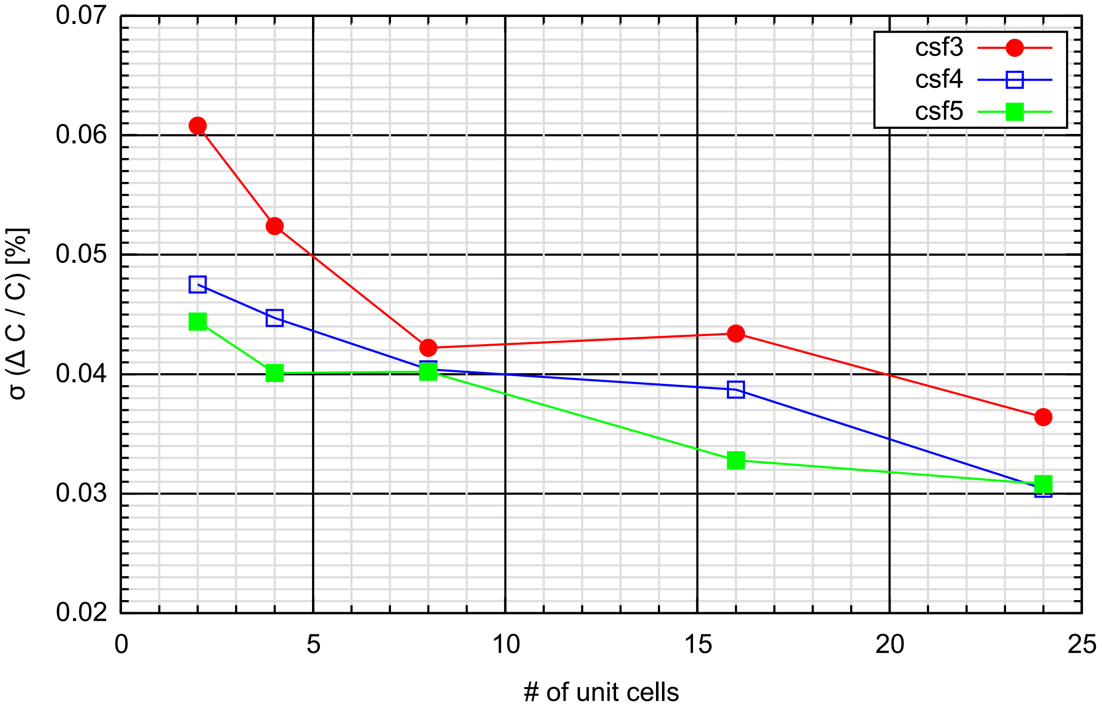

Figure 3.16 Device csf3, csf4, csf5: capacitor matching vs. number of fringe cap unit cells (typical values)

csf3a

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-50	-45	45	50	V
Vterm1-Vterm2	-40°C to 175°C	-50	-45	45	50	V

Process parameters

Name	Description	Low	Typ	High	Unit
BDO_SF3A	csf3a breakdown voltage @ Ibr=1µA	70	-	-	V
CA_SF3A_B	csf3a capacitance per cell @ Vbias=0V, L=11.1µm, W=5.76µm	21.6	23.9	26.2	fF
IL_SF3A	csf3a leakage current @ VL=45V	-	-	35	fA/cell
TC1_SF3A	csf3a temperature coefficient 1 @ Tnom=27°C	-	-70	-	1e-06/K

Matching parameters

Name	Description	Low	Typ	High	Unit
SC_SF3A	standard deviation capacitor mismatch	-	0.035	0.045	%
	Note: The values of this parameter do not reflect the statistics of the process. The high value corresponds to 1 unit cell; the typical value is valid for >= 8 unit cells.				

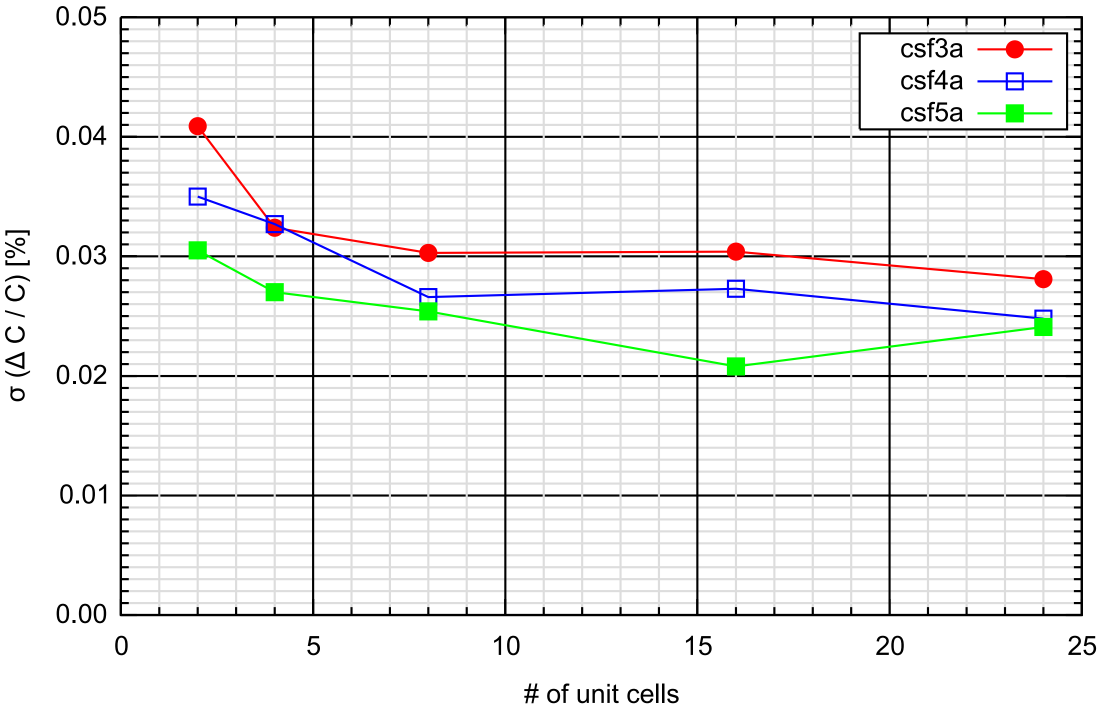

Figure 3.17 Device csf3a, csf4a, csf5a: capacitor matching vs. number of fringe cap unit cells (typical values)

3.3 MET4 module

3.3.1 Device independent parameters

Structural and geometrical parameters

Name	Description	Low	Typ	High	Unit
EPS_IMD3	metal 3 / metal 4 equivalent dielectric constant	-	4	-	-
	Note: The values for dielectric permittivity are mean values only, because the dielectric consists of a stack of layers each with a different permittivity				
THD_IMD3	metal 4 - metal 3 dielectric thickness	765	850	935	nm
TH_M4	metal 4 thickness	505	565	625	nm

Sheet and contact resistance parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSR_M4	metal 4 sheet resistance	58	66	74	82	90	mΩ/☐
RVI_V3	VIA3 resistance	-	3	4.5	6.75	9	Ω/via
TC1_V234	VIA2,3,4 resistance temperature coefficient 1	-	-	1.1	-	-	1e-03/K
TC2_V234	VIA2,3,4 resistance temperature coefficient 2	-	-	0	-	-	1e-06/K²

Parasitic capacitance parameters

The following table provides a principal overview with respect to interconnect capacitances. More extensive data will be available on request.

Name	Description	Typ	Unit
CC_M4M4	coupling capacitance metal 4 – metal 4	99	aF/µm
CPAM4DIFF	metal 4 – active area capacitance	6.6	aF/µm²
CPAM4M1	metal 4 – metal 1 area capacitance	9.5	aF/µm²
CPAM4M2	metal 4 – metal 2 area capacitance	15.5	aF/µm²
CPAM4M3	metal 4 – metal 3 area capacitance	41.5	aF/µm²
CPAM4P1	metal 4 – poly 1 area capacitance	6.8	aF/µm²
CPAM4STI	metal 4 – field area (STI) area capacitance	6.2	aF/µm²
CPPM4DIFF	metal 4 – active perimeter capacitance	6.8	aF/µm
CPPM4M1	metal 4 – metal 1 perimeter capacitance	4.1	aF/µm
CPPM4M2	metal 4 – metal 2 perimeter capacitance	5	aF/µm
CPPM4M3	metal 4 – metal 3 perimeter capacitance	8.3	aF/µm
CPPM4P1	metal 4 – poly 1 perimeter capacitance	3.7	aF/µm
CPPM4STI	metal 4 – field area (STI) perimeter capacitance	6.7	aF/µm

Physical layer operating conditions

Name	Structure	Temp. range	Abs. min	Min	Max	Abs. max	Unit
JMax_DC(1 (2	Metal 4	-40°C to 175°C	-	-	1	20	mA/µm
JMax_N_DC(3 (2	Metal 4	-40°C to 175°C	-	-	0.5	20	mA/µm

⇒

Name	Structure	Temp. range	Abs. min	Min	Max	Abs. max	Unit
JMax_VI_DC[2]	Via 3	-40°C to 175°C	-	-	0.28	20	mA/via
JMax_AC[1 4]	Metal 4	-40°C to 175°C	-	-	4.5	20	mA/µm
JMax_N_AC[3 4]	Metal 4	-40°C to 175°C	-	-	2.2	20	mA/µm
JMax_VI_AC[4]	Via 3	-40°C to 175°C	-	-	1.3	20	mA/via
T_Factor_1e4[5 6]	Metal 4	-40°C to 85°C	-	3.13	-	-	-
T_Factor_1e4[5 6]	Via 3	-40°C to 85°C	-	4.25	-	-	-
T_Factor_1e4[7 6]	Metal 4	85°C to 125°C	-	1	-	-	-
T_Factor_1e4[7 6]	Via 3	85°C to 125°C	-	1.16	-	-	-
T_Factor_1e4[8 6]	Metal 4	125°C to 175°C	-	0.32	-	-	-
T_Factor_1e4[8 6]	Via 3	125°C to 175°C	-	0.31	-	-	-
T_Factor_1e5[5 6]	Metal 4	-40°C to 85°C	-	1	-	-	-
T_Factor_1e5[5 6]	Via 3	-40°C to 85°C	-	1.35	-	-	-
T_Factor_1e5[7 6]	Metal 4	85°C to 125°C	-	0.32	-	-	-
T_Factor_1e5[7 6]	Via 3	85°C to 125°C	-	0.37	-	-	-
T_Factor_1e5[8 6]	Metal 4	125°C to 175°C	-	0.1	-	-	-
T_Factor_1e5[8 6]	Via 3	125°C to 175°C	-	0.1	-	-	-

Note 1 track width > 0.44µm.

Note 2 Max values of JMAX*DC refer to rms/avg values. Abs. max values of JMAX*DC refer to peak values.

Note 3 track width ≤ 0.44µm.

Note 4 Max values of JMAX*AC refer to rms values. Abs. max values of JMAX*AC refer to peak values.

Note 5 The temperature correction factor remains constant at the stated value across the whole temperatures range.

Note 6 Temperature correction factors allow the scaling of the current density according to the required lifetime and temperature. For more detailed information, please refer to the Interconnect reliability sections of the SpecXplorer or Process Reliability Specification.

Note 7 The temperature correction factor is interpolated between given values for temperatures above 85°C.

Note 8 The temperature correction factor is interpolated between given values for temperatures above 125°C

3.3.2 Device parameters

rm4

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-50	-45	45	50	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSR_M4	metal 4 sheet resistance	58	66	74	82	90	mΩ/☐
TC1_M4	metal 4 temperature coefficient 1	-	-	3.4	-	-	1e-03/K
TC2_M4	metal 4 temperature coefficient 2	-	-	0	-	-	1e-06/K²
WER_M4	metal 4 effective width @ W=0.28µm	-	0.2	0.24	0.28	-	µm

csandwt4

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk[1]	-40°C to 175°C	-50	-45	45	50	V
Vterm1-Vterm2	-40°C to 175°C	-50	-45	45	50	V

Note 1 An inversion layer is formed in the bulk underneath the poly if the terminal-to-bulkvoltage exceeds the field threshold voltage.The field threshold voltages are specified in section "3. Parameters"

Process parameters

Name	Description	Low	Typ	High	Unit
CAA_SANDW4B	POLY1 / metal1/ metal2/ metal3/ metal4 sandwich area capacitance @ Vbias=0V	0.16	0.2	0.24	fF/µm²
CAP_SANDW4	POLY1 / metal1/ metal2/ metal3/ metal4 sandwich perimeter capacitance	-	0.085	-	fF/µm

Matching parameters

Name	Description	Typ	Unit
AC_SANDW4	Pelgrom coefficient capacitor mismatch	0.46	%µm

csf4

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-50	-45	45	50	V
Vterm1-Vterm2	-40°C to 175°C	-12	-10	10	12	V

Process parameters

Name	Description	Low	Typ	High	Unit
BDO_SF4	csf4 breakdown voltage @ Ibr=1µA	35	-	-	V
CA_SF4_B	csf4 capacitance per cell @ Vbias=0V, L=10.8µm, W=4.48µm	41.3	45	48.7	fF
IL_SF4	csf4 leakage current @ VL=10V	-	-	30	fA/cell
TC1_SF4	csf4 temperature coefficient 1 @ Tnom=27°C	-	-70	-	1e-06/K

Matching parameters

Name	Description	Low	Typ	High	Unit
SC_SF4	standard deviation capacitor mismatch	-	0.045	0.055	%
	Note: The values of this parameter do not reflect the statistics of the process. The high value corresponds to 1 unit cell; the typical value is valid for >= 8 unit cells.				

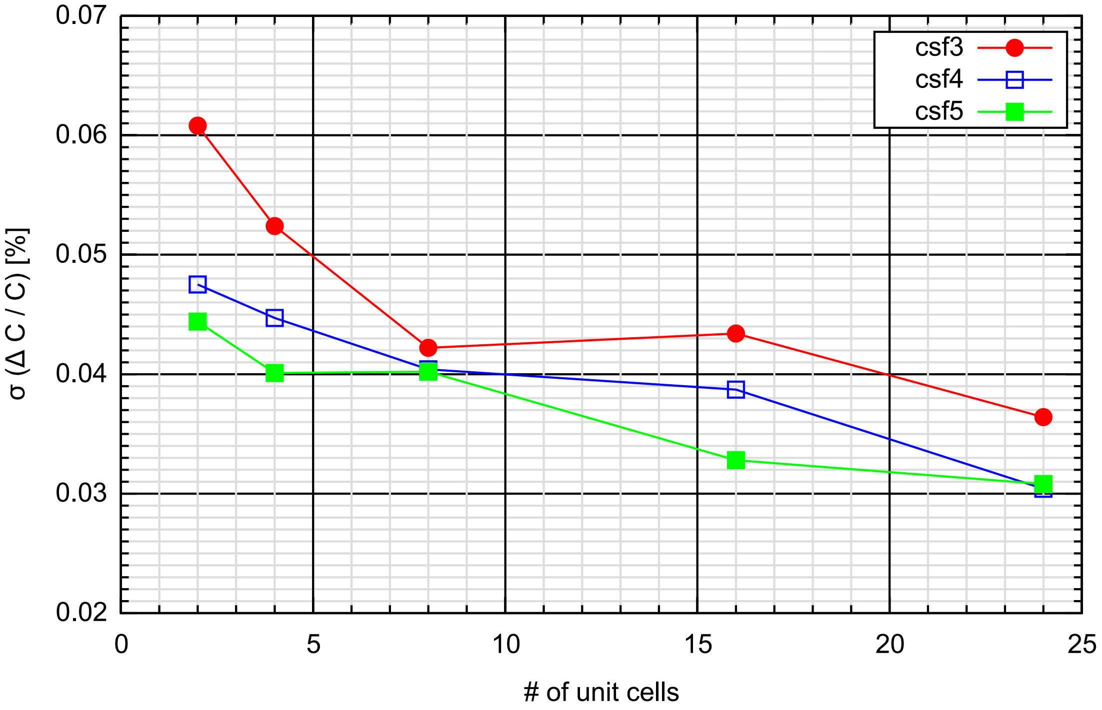

Figure 3.18 Device csf3, csf4, csf5: capacitor matching vs. number of fringe cap unit cells (typical values)

csf4a

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-50	-45	45	50	V
Vterm1-Vterm2	-40°C to 175°C	-50	-45	45	50	V

Process parameters

Name	Description	Low	Typ	High	Unit
BDO_SF4A	csf4a breakdown voltage @ Ibr=1µA	70	-	-	V
CA_SF4A_B	csf4a capacitance per cell @ Vbias=0V, L=11.1µm, W=5.76µm	30.2	32.9	35.6	fF
IL_SF4A	csf4a leakage current @ VL=45V	-	-	35	fA/cell
TC1_SF4A	csf4a temperature coefficient 1 @ Tnom=27°C	-	-70	-	1e-06/K

Matching parameters

Name	Description	Low	Typ	High	Unit
SC_SF4A	standard deviation capacitor mismatch	-	0.032	0.04	%
	Note: The values of this parameter do not reflect the statistics of the process. The high value corresponds to 1 unit cell; the typical value is valid for >= 8 unit cells.				

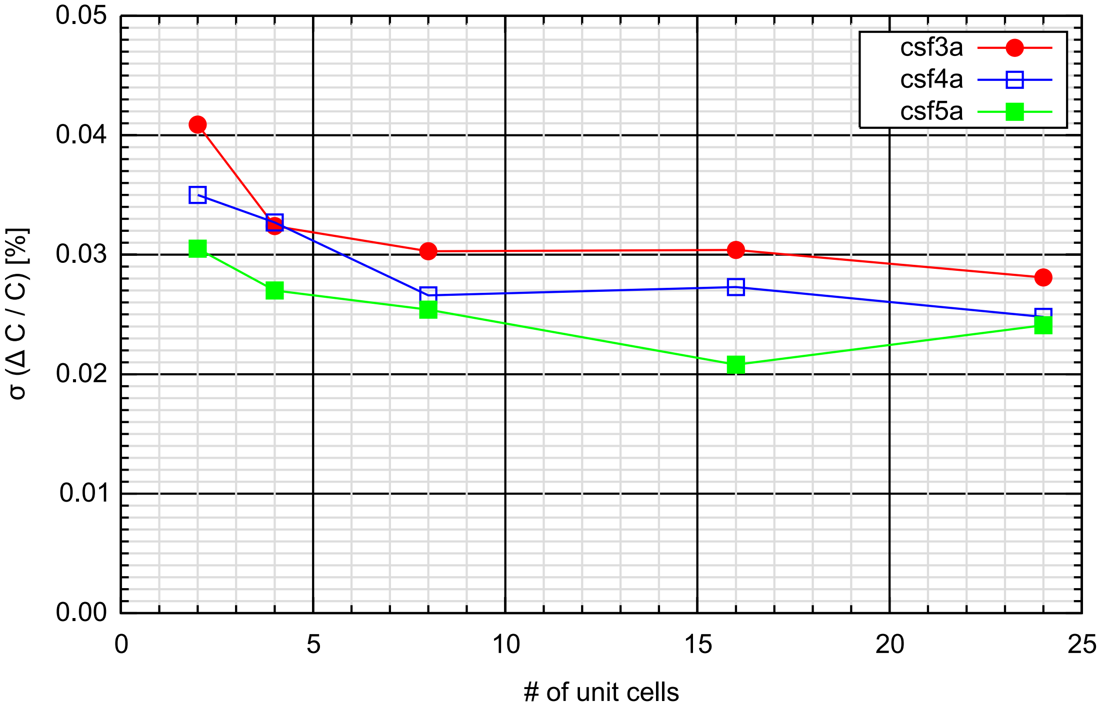

Figure 3.19 Device csf3a, csf4a, csf5a: capacitor matching vs. number of fringe cap unit cells (typical values)

3.4 MET5 module

3.4.1 Device independent parameters

Structural and geometrical parameters

Name	Description	Low	Typ	High	Unit
EPS_IMD4	metal 4 / metal 5 equivalent dielectric constant	-	4	-	-
	Note: The values for dielectric permittivity are mean values only, because the dielectric consists of a stack of layers each with a different permittivity				
THD_IMD4	metal 5 - metal 4 dielectric thickness	765	850	935	nm
TH_M5	metal 5 thickness	505	565	625	nm

Sheet and contact resistance parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSR_M5	metal 5 sheet resistance	58	66	74	82	90	mΩ/☐
RVI_V4	VIA4 resistance	-	3	4.5	6.75	9	Ω/via
TC1_V234	VIA2,3,4 resistance temperature coefficient 1	-	-	1.1	-	-	1e-03/K
TC2_V234	VIA2,3,4 resistance temperature coefficient 2	-	-	0	-	-	1e-06/K²

Parasitic capacitance parameters

The following table provides a principal overview with respect to interconnect capacitances. More extensive data will be available on request.

Name	Description	Typ	Unit
CC_M5M5	coupling capacitance metal 5 – metal 5	99	aF/µm
CPAM5DIFF	metal 5 – active area capacitance	5.2	aF/µm²
CPAM5M1	metal 5 – metal 1 area capacitance	6.8	aF/µm²
CPAM5M2	metal 5 – metal 2 area capacitance	9.5	aF/µm²
CPAM5M3	metal 5 – metal 3 area capacitance	15.5	aF/µm²
CPAM5M4	metal 5 – metal 4 area capacitance	41.5	aF/µm²
CPAM5P1	metal 5 – poly 1 area capacitance	5.3	aF/µm²
CPAM5STI	metal 5 – field area (STI) area capacitance	4.9	aF/µm²
CPPM5DIFF	metal 5 – active perimeter capacitance	6.6	aF/µm
CPPM5M1	metal 5 – metal 1 perimeter capacitance	3.7	aF/µm
CPPM5M2	metal 5 – metal 2 perimeter capacitance	4.1	aF/µm
CPPM5M3	metal 5 – metal 3 perimeter capacitance	5	aF/µm
CPPM5M4	metal 5 – metal 4 perimeter capacitance	8.3	aF/µm
CPPM5P1	metal 5 – poly 1 perimeter capacitance	3.5	aF/µm
CPPM5STI	metal 5 – field area (STI) perimeter capacitance	6.5	aF/µm

Physical layer operating conditions

Name	Structure	Temp. range	Abs. min	Min	Max	Abs. max	Unit
JMax_DC[(1 (2]	Metal 5	-40°C to 175°C	-	-	1	20	mA/µm

⇒

Name	Structure	Temp. range	Abs. min	Min	Max	Abs. max	Unit
JMax_N_DC[3][2]	Metal 5	-40°C to 175°C	-	-	0.5	20	mA/µm
JMax_VI_DC[2]	Via 4	-40°C to 175°C	-	-	0.28	20	mA/via
JMax_AC[1][4]	Metal 5	-40°C to 175°C	-	-	4.5	20	mA/µm
JMax_N_AC[3][4]	Metal 5	-40°C to 175°C	-	-	2.2	20	mA/µm
JMax_VI_AC[4]	Via 4	-40°C to 175°C	-	-	1.3	20	mA/via
T_Factor_1e4[5][6]	Metal 5	-40°C to 85°C	-	3.13	-	-	-
T_Factor_1e4[5][6]	Via 4	-40°C to 85°C	-	4.25	-	-	-
T_Factor_1e4[7][6]	Metal 5	85°C to 125°C	-	1	-	-	-
T_Factor_1e4[7][6]	Via 4	85°C to 125°C	-	1.16	-	-	-
T_Factor_1e4[8][6]	Metal 5	125°C to 175°C	-	0.32	-	-	-
T_Factor_1e4[8][6]	Via 4	125°C to 175°C	-	0.31	-	-	-
T_Factor_1e5[5][6]	Metal 5	-40°C to 85°C	-	1	-	-	-
T_Factor_1e5[5][6]	Via 4	-40°C to 85°C	-	1.35	-	-	-
T_Factor_1e5[7][6]	Metal 5	85°C to 125°C	-	0.32	-	-	-
T_Factor_1e5[7][6]	Via 4	85°C to 125°C	-	0.37	-	-	-
T_Factor_1e5[8][6]	Metal 5	125°C to 175°C	-	0.1	-	-	-
T_Factor_1e5[8][6]	Via 4	125°C to 175°C	-	0.1	-	-	-

Note 1 track width > 0.44µm.

Note 2 Max values of JMAX*DC refer to rms/avg values. Abs. max values of JMAX*DC refer to peak values.

Note 3 track width ≤ 0.44µm.

Note 4 Max values of JMAX*AC refer to rms values. Abs. max values of JMAX*AC refer to peak values.

Note 5 The temperature correction factor remains constant at the stated value across the whole temperatures range.

Note 6 Temperature correction factors allow the scaling of the current density according to the required lifetime and temperature. For more detailed information, please refer to the Interconnect reliability sections of the SpecXplorer or Process Reliability Specification.

Note 7 The temperature correction factor is interpolated between given values for temperatures above 85°C.

Note 8 The temperature correction factor is interpolated between given values for temperatures above 125°C

3.4.2 Device parameters

rm5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-50	-45	45	50	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSR_M5	metal 5 sheet resistance	58	66	74	82	90	mΩ/□
TC1_M5	metal 5 temperature coefficient 1	-	-	3.4	-	-	1e-03/K
TC2_M5	metal 5 temperature coefficient 2	-	-	0	-	-	1e-06/K²
WER_M5	metal 5 effective width @ W=0.28µm	-	0.2	0.24	0.28	-	µm

csandwt5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk[1]	-40°C to 175°C	-50	-45	45	50	V
Vterm1-Vterm2	-40°C to 175°C	-50	-45	45	50	V

Note 1 An inversion layer is formed in the bulk underneath the poly if the terminal-to-bulkvoltage exceeds the field threshold voltage.The field threshold voltages are specified in section "3. Parameters"

Process parameters

Name	Description	Low	Typ	High	Unit
CAA_SANDW5B	POLY1 / metal1/ metal2/ metal3/ metal4/ metal5 sandwich area capacitance @ Vbias=0V	0.2	0.25	0.3	fF/µm²
CAP_SANDW5	POLY1 / metal1/ metal2/ metal3/ metal4/ metal5 sandwich perimeter capacitance	-	0.145	-	fF/µm

Matching parameters

Name	Description	Typ	Unit
AC_SANDW5	Pelgrom coefficient capacitor mismatch	0.39	%µm

csf5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-50	-45	45	50	V
Vterm1-Vterm2	-40°C to 175°C	-12	-10	10	12	V

Process parameters

Name	Description	Low	Typ	High	Unit
BDO_SF5	csf5 breakdown voltage @ Ibr=1µA	35	-	-	V
CA_SF5_B	csf5 capacitance per cell @ Vbias=0V, L=10.8µm, W=4.48µm	52.3	57.1	61.9	fF
IL_SF5	csf5 leakage current @ VL=10V	-	-	30	fA/cell
TC1_SF5	csf5 temperature coefficient 1 @ Tnom=27°C	-	-70	-	1e-06/K

Matching parameters

Name	Description	Low	Typ	High	Unit
SC_SF5	standard deviation capacitor mismatch	-	0.04	0.05	%
	Note: The values of this parameter do not reflect the statistics of the process. The high value corresponds to 1 unit cell; the typical value is valid for >= 8 unit cells.				

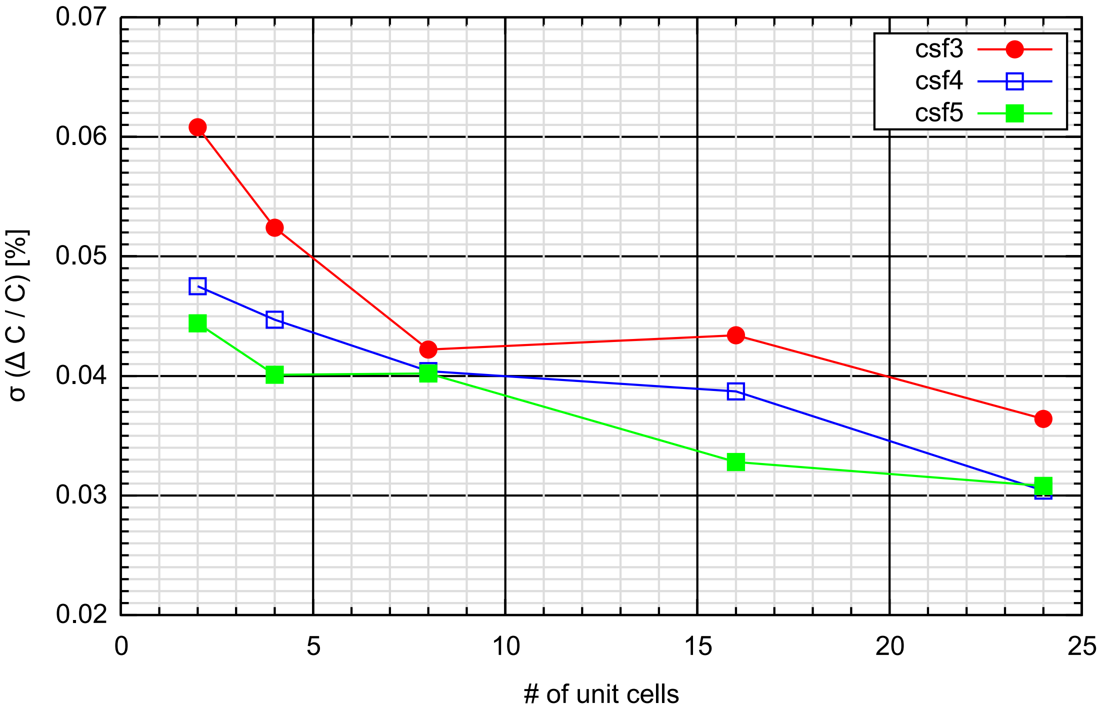

Figure 3.20 Device csf3, csf4, csf5: capacitor matching vs. number of fringe cap unit cells (typical values)

csf5a

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-50	-45	45	50	V
Vterm1-Vterm2	-40°C to 175°C	-50	-45	45	50	V

Process parameters

Name	Description	Low	Typ	High	Unit
BDO_SF5A	csf5a breakdown voltage @ Ibr=1µA	70	-	-	V
CA_SF5A_B	csf5a capacitance per cell @ Vbias=0V, L=11.1µm, W=5.76µm	37.8	41.8	45.8	fF
IL_SF5A	csf5a leakage current @ VL=45V	-	-	35	fA/cell
TC1_SF5A	csf5a temperature coefficient 1 @ Tnom=27°C	-	-70	-	1e-06/K

Note: The device csf5a is only available with the MET5 module.

Matching parameters

Name	Description	Low	Typ	High	Unit
SC_SF5A	standard deviation capacitor mismatch	-	0.029	0.035	%
	Note: The values of this parameter do not reflect the statistics of the process. The high value corresponds to 1 unit cell; the typical value is valid for >= 8 unit cells.				

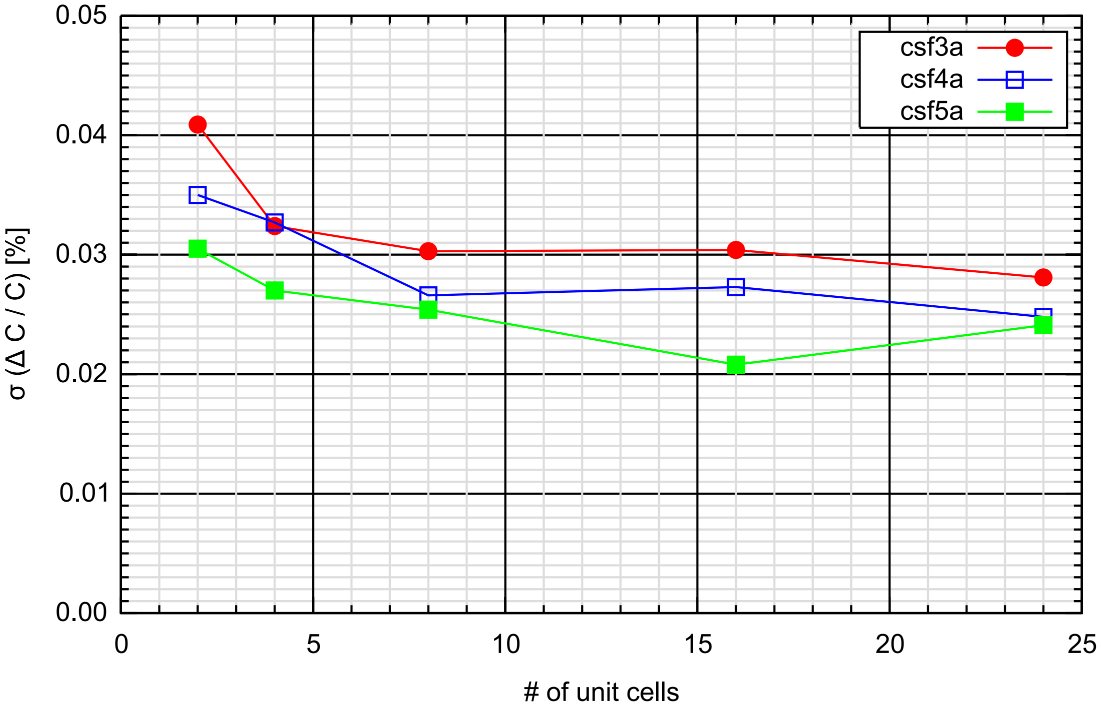

Figure 3.21 Device csf3a, csf4a, csf5a: capacitor matching vs. number of fringe cap unit cells (typical values)

3.5 METMID module

3.5.1 Device independent parameters

Structural and geometrical parameters

Name	Description	Low	Typ	High	Unit
EPS_IMDTP	metal underneath top metal / top metal equivalent dielectric constant	-	4	-	-
	Note: The values for dielectric permittivity are mean values only, because the dielectric consists of a stack of layers each with a different permittivity				
THD_IMDT	top metal – metal underneath top metal dielectric thickness	885	1000	1115	nm
TH_MTP	top metal thickness	885	985	1085	nm

Sheet and contact resistance parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSR_MTPB	top metal sheet resistance	22	26.5	31	35.5	40	mΩ/□
RVI_VTP	VIATP resistance	-	1.6	2	3.2	4.4	Ω/via
TC1_VTP	VIATP resistance temperature coefficient 1	-	-	1.35	-	-	1e-03/K
TC2_VTP	VIATP resistance temperature coefficient 2	-	-	0	-	-	1e-06/K^2

Parasitic capacitance parameters

The following table provides a principal overview with respect to interconnect capacitances. More extensive data will be available on request.

Name	Description	Typ	Unit
CC_MTPMTP4	coupling capacitance top metal – top metal (4 metal layers)	94	aF/µm
CC_MTPMTP5	coupling capacitance top metal – top metal (5 metal layers)	94	aF/µm
CC_MTPMTP6	coupling capacitance top metal – top metal (6 metal layers)	94	aF/µm
CPAMTPDIF4	top metal – active area capacitance (4 metal layers)	6.5	aF/µm²
CPAMTPDIF5	top metal – active area capacitance (5 metal layers)	5.1	aF/µm²
CPAMTPDIF6	top metal – active area capacitance (6 metal layers)	4.2	aF/µm²
CPAMTPM1_4	top metal – metal 1 area capacitance (4 metal layers)	9.1	aF/µm²
CPAMTPM1_5	top metal – metal 1 area capacitance (5 metal layers)	6.6	aF/µm²
CPAMTPM1_6	top metal – metal 1 area capacitance (6 metal layers)	5.2	aF/µm²
CPAMTPM2_4	top metal – metal 2 area capacitance (4 metal layers)	14.5	aF/µm²
CPAMTPM2_5	top metal – metal 2 area capacitance (5 metal layers)	9.1	aF/µm²
CPAMTPM2_6	top metal – metal 2 area capacitance (6 metal layers)	6.6	aF/µm²
CPAMTPM3_4	top metal – metal 3 area capacitance (4 metal layers)	35.3	aF/µm²
CPAMTPM3_5	top metal – metal 3 area capacitance (5 metal layers)	14.5	aF/µm²
CPAMTPM3_6	top metal – metal 3 area capacitance (6 metal layers)	9.1	aF/µm²
CPAMTPM4_5	top metal – metal 4 area capacitance (5 metal layers)	35.3	aF/µm²
CPAMTPM4_6	top metal – metal 4 area capacitance (6 metal layers)	14.5	aF/µm²
CPAMTPM5_6	top metal – metal 5 area capacitance (6 metal layers)	35.3	aF/µm²

⇒

Name	Description	Typ	Unit
CPAMTPP1_4	top metal – poly 1 area capacitance (4 metal layers)	6.7	aF/μm^2
CPAMTPP1_5	top metal – poly 1 area capacitance (5 metal layers)	5.2	aF/μm^2
CPAMTPP1_6	top metal – poly 1 area capacitance (6 metal layers)	4.3	aF/μm^2
CPAMTPSTI4	top metal – field area (STI) area capacitance (4 metal layers)	6	aF/μm^2
CPAMTPSTI5	top metal – field area (STI) area capacitance (5 metal layers)	4.8	aF/μm^2
CPAMTPSTI6	top metal – field area (STI) area capacitance (6 metal layers)	4	aF/μm^2
CPPMTPDIF4	top metal – active perimeter capacitance (4 metal layers)	6.7	aF/µm
CPPMTPDIF5	top metal – active perimeter capacitance (5 metal layers)	6.5	aF/µm
CPPMTPDIF6	top metal – active perimeter capacitance (6 metal layers)	6.2	aF/µm
CPPMTPM1_4	top metal – metal 1 perimeter capacitance (4 metal layers)	4.4	aF/µm
CPPMTPM1_5	top metal – metal 1 perimeter capacitance (5 metal layers)	3.9	aF/µm
CPPMTPM1_6	top metal – metal 1 perimeter capacitance (6 metal layers)	3.6	aF/µm
CPPMTPM2_4	top metal – metal 2 perimeter capacitance (4 metal layers)	5.5	aF/µm
CPPMTPM2_5	top metal – metal 2 perimeter capacitance (5 metal layers)	4.4	aF/µm
CPPMTPM2_6	top metal – metal 2 perimeter capacitance (6 metal layers)	3.9	aF/µm
CPPMTPM3_4	top metal – metal 3 perimeter capacitance (4 metal layers)	9.5	aF/µm
CPPMTPM3_5	top metal – metal 3 perimeter capacitance (5 metal layers)	5.5	aF/µm
CPPMTPM3_6	top metal – metal 3 perimeter capacitance (6 metal layers)	4.4	aF/µm
CPPMTPM4_5	top metal – metal 4 perimeter capacitance (5 metal layers)	9.5	aF/µm
CPPMTPM4_6	top metal – metal 4 perimeter capacitance (6 metal layers)	5.5	aF/µm
CPPMTPM5_6	top metal – metal 5 perimeter capacitance (6 metal layers)	9.5	aF/µm
CPPMTPP1_4	top metal – poly 1 perimeter capacitance (4 metal layers)	3.9	aF/µm
CPPMTPP1_5	top metal – poly 1 perimeter capacitance (5 metal layers)	3.6	aF/µm
CPPMTPP1_6	top metal – poly 1 perimeter capacitance (6 metal layers)	3.4	aF/µm
CPPMTPSTI4	top metal – field area (STI) perimeter capacitance (4 metal layers)	6.6	aF/µm
CPPMTPSTI5	top metal – field area (STI) perimeter capacitance (5 metal layers)	6.4	aF/µm
CPPMTPSTI6	top metal – field area (STI) perimeter capacitance (6 metal layers)	6.1	aF/µm

Physical layer operating conditions

Name	Structure	Temp. range	Abs. min	Min	Max	Abs. max	Unit
JMax_DC[(1 (2]	Top metal	-40°C to 175°C	-	-	1.6	32	mA/µm
JMax_VI_DC[(2]	Top Via	-40°C to 175°C	-	-	0.7	32	mA/via
JMax_AC[(1 (3]	Top metal	-40°C to 175°C	-	-	7.2	32	mA/µm
JMax_VI_AC[(3]	Top Via	-40°C to 175°C	-	-	3.1	32	mA/via
T_Factor_1e4[(4 (5]	Top metal	-40°C to 85°C	-	3.13	-	-	-
T_Factor_1e4[(4 (5]	Top Via	-40°C to 85°C	-	4.25	-	-	-
T_Factor_1e4[(6 (5]	Top metal	85°C to 125°C	-	1	-	-	-
T_Factor_1e4[(6 (5]	Top Via	85°C to 125°C	-	1.16	-	-	-
T_Factor_1e4[(7 (5]	Top metal	125°C to 175°C	-	0.32	-	-	-
T_Factor_1e4[(7 (5]	Top Via	125°C to 175°C	-	0.31	-	-	-
T_Factor_1e5[(4 (5]	Top metal	-40°C to 85°C	-	1	-	-	-
T_Factor_1e5[(4 (5]	Top Via	-40°C to 85°C	-	1.35	-	-	-

⇒

Name	Structure	Temp. range	Abs. min	Min	Max	Abs. max	Unit
T_Factor_1e5(6 (5	Top metal	85°C to 125°C	-	0.32	-	-	-
T_Factor_1e5(6 (5	Top Via	85°C to 125°C	-	0.37	-	-	-
T_Factor_1e5(7 (5	Top metal	125°C to 175°C	-	0.1	-	-	-
T_Factor_1e5(7 (5	Top Via	125°C to 175°C	-	0.1	-	-	-

Note 1 Valid for all widths.

Note 2 Max values of JMAX*DC refer to rms/avg values. Abs. max values of JMAX*DC refer to peak values.

Note 3 Max values of JMAX*AC refer to rms values. Abs. max values of JMAX*AC refer to peak values.

Note 4 The temperature correction factor remains constant at the stated value across the whole temperatures range.

Note 5 Temperature correction factors allow the scaling of the current density according to the required lifetime and temperature. For more detailed information, please refer to the Interconnect reliability sections of the SpecXplorer or Process Reliability Specification.

Note 6 The temperature correction factor is interpolated between given values for temperatures above 85°C.

Note 7 The temperature correction factor is interpolated between given values for temperatures above 125°C

3.5.2 Device parameters

rmtp

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-50	-45	45	50	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSR_MTPB	top metal sheet resistance	22	26.5	31	35.5	40	mΩ/☐
TC1_MTP	top metal temperature coefficient 1	-	-	3.2	-	-	1e-03/K
TC2_MTP	top metal temperature coefficient 2	-	-	0	-	-	1e-06/K²
WER_MTP	top metal effective width @ W=0.44μm	-	0.26	0.32	0.38	-	μm

csft4

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-50	-45	45	50	V
Vterm1-Vterm2	-40°C to 175°C	-12	-10	10	12	V

Process parameters

Name	Description	Low	Typ	High	Unit
BDO_SFT4	csft4 breakdown voltage @ Ibr=1μA	35	-	-	V
CA_SFT4_B	csft4 capacitance per cell @ Vbias=0V, L=10.8μm, W=4.48μm	33.4	36.5	39.6	fF
IL_SFT4	csft4 leakage current @ VL=10V	-	-	30	fA/cell
TC1_SFT4	csft4 temperature coefficient 1 @ Tnom=27°C	-	-70	-	1e-06/K

Matching parameters

Name	Description	Low	Typ	High	Unit
SC_SFT4	standard deviation capacitor mismatch	-	0.052	0.062	%
	Note: The values of this parameter do not reflect the statistics of the process. The high value corresponds to 1 unit cell; the typical value is valid for >= 8 unit cells.				

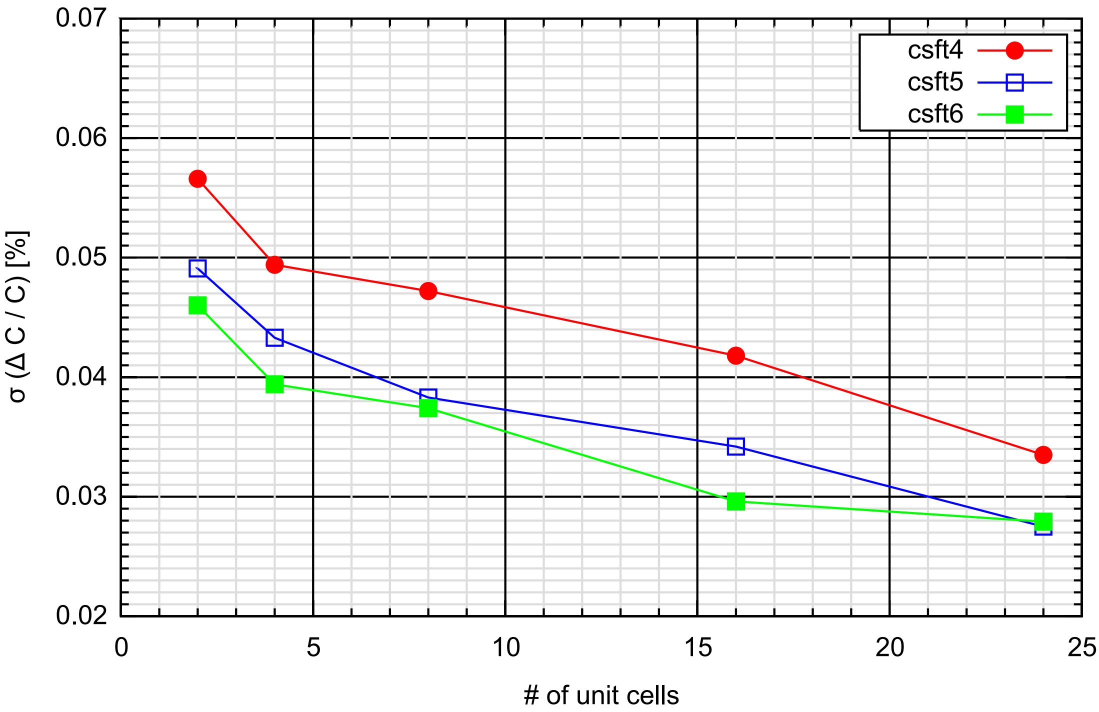

Figure 3.22 Device csft4, csft5, csft6: capacitor matching vs. number of fringe cap unit cells (typical values)

csft4a

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-50	-45	45	50	V
Vterm1-Vterm2	-40°C to 175°C	-50	-45	45	50	V

Process parameters

Name	Description	Low	Typ	High	Unit
BDO_SFT4A	csft4a breakdown voltage @ Ibr=1μA	70	-	-	V
CA_SFT4A_B	csft4a capacitance per cell @ Vbias=0V, L=11.1μm, W=5.76μm	26	28.7	31.4	fF
IL_SFT4A	csft4a leakage current @ VL=45V	-	-	35	fA/cell
TC1_SFT4A	csft4a temperature coefficient 1 @ Tnom=27°C	-	-70	-	1e-06/K

Matching parameters

Name	Description	Low	Typ	High	Unit
SC_SFT4A	standard deviation capacitor mismatch	-	0.033	0.042	%
	Note: The values of this parameter do not reflect the statistics of the process. The high value corresponds to 1 unit cell; the typical value is valid for >= 8 unit cells.				

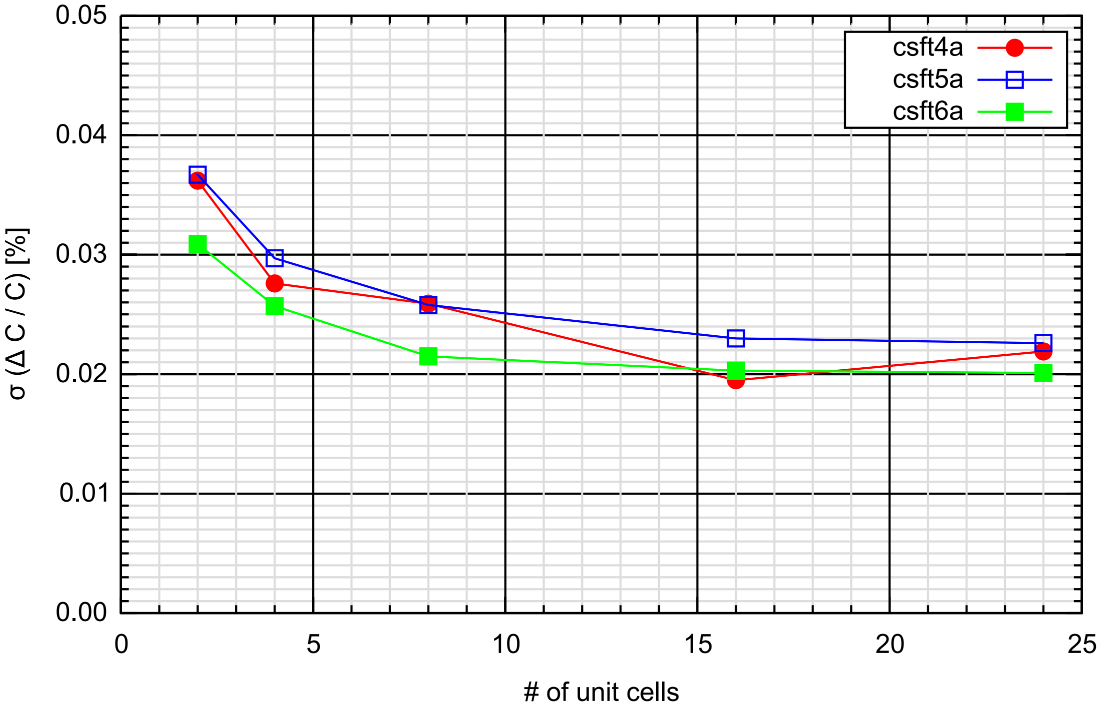

Figure 3.23 Device csft4a, csft5a, csft6a: capacitor matching vs. number of fringe cap unit cells (typical values)

csft5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-50	-45	45	50	V
Vterm1-Vterm2	-40°C to 175°C	-12	-10	10	12	V

Process parameters

Name	Description	Low	Typ	High	Unit
BDO_SFT5	csft5 breakdown voltage @ Ibr=1μA	35	-	-	V
CA_SFT5_B	csft5 capacitance per cell @ Vbias=0V, L=10.8μm, W=4.48μm	45	49.1	53.2	fF
IL_SFT5	csft5 leakage current @ VL=10V	-	-	30	fA/cell
TC1_SFT5	csft5 temperature coefficient 1 @ Tnom=27°C	-	-70	-	1e-06/K

Note: The device csft5 is only available with the MET4 and METMID are selected and MET5 module is not selected.

Matching parameters

Name	Description	Low	Typ	High	Unit
SC_SFT5	standard deviation capacitor mismatch	-	0.045	0.055	%
	Note: The values of this parameter do not reflect the statistics of the process. The high value corresponds to 1 unit cell; the typical value is valid for >= 8 unit cells.				

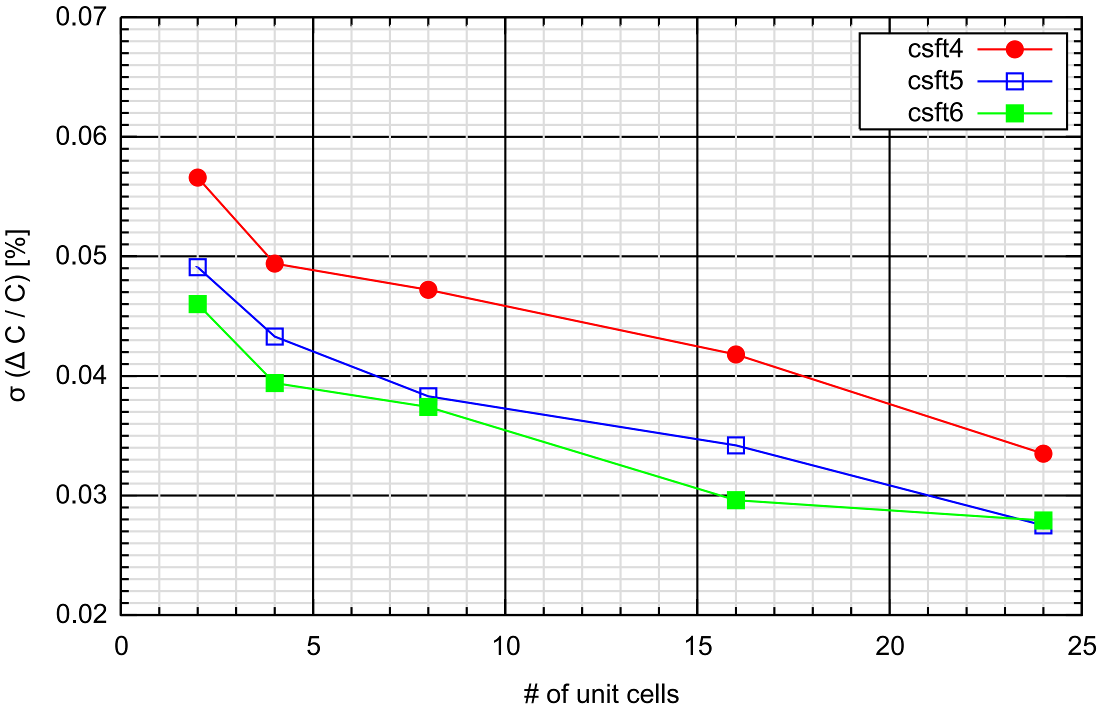

Figure 3.24 Device csft4, csft5, csft6: capacitor matching vs. number of fringe cap unit cells (typical values)

csft5a

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-50	-45	45	50	V
Vterm1-Vterm2	-40°C to 175°C	-50	-45	45	50	V

Process parameters

Name	Description	Low	Typ	High	Unit
BDO_SFT5A	csft5a breakdown voltage @ Ibr=1μA	70	-	-	V
CA_SFT5A_B	csft5a capacitance per cell @ Vbias=0V, L=11.1μm, W=5.76μm	34.1	37.7	41.3	fF
IL_SFT5A	csft5a leakage current @ VL=45V	-	-	35	fA/cell
TC1_SFT5A	csft5a temperature coefficient 1 @ Tnom=27°C	-	-70	-	1e-06/K

Note: The device csft5a is only available with the MET4 and METMID are selected and MET5 module is not selected.

Matching parameters

Name	Description	Low	Typ	High	Unit
SC_SFT5A	standard deviation capacitor mismatch	-	0.03	0.04	%
	Note: The values of this parameter do not reflect the statistics of the process. The high value corresponds to 1 unit cell; the typical value is valid for >= 8 unit cells.				

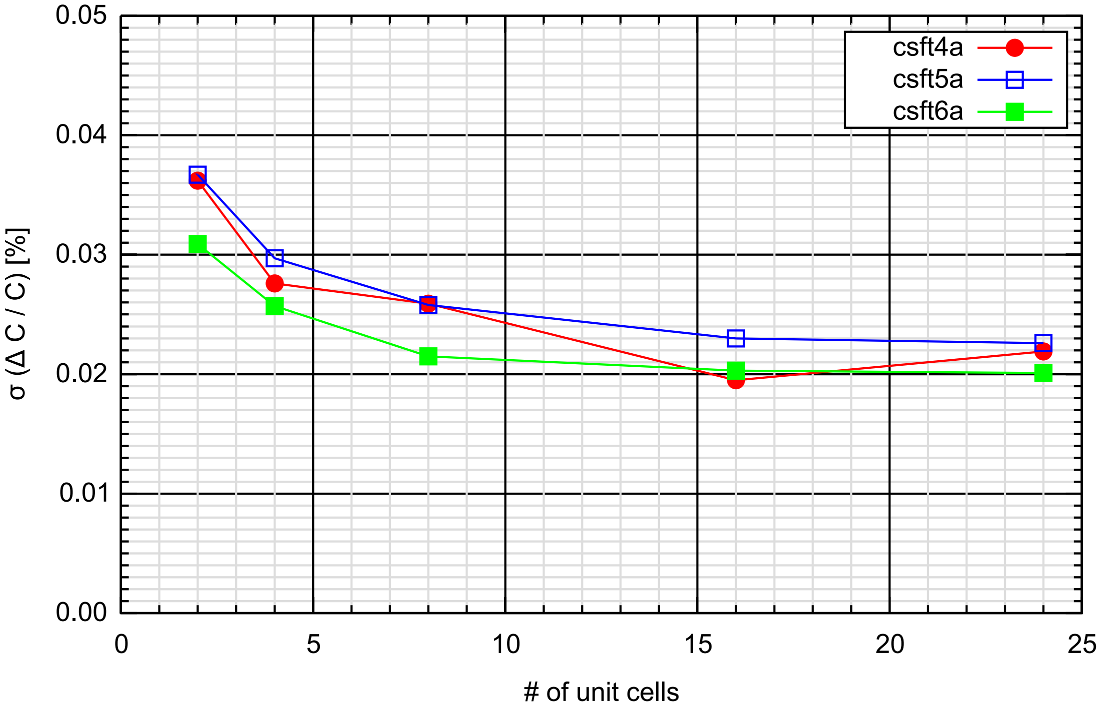

Figure 3.25 Device csft4a, csft5a, csft6a: capacitor matching vs. number of fringe cap unit cells (typical values)

csft6

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-50	-45	45	50	V
Vterm1-Vterm2	-40°C to 175°C	-12	-10	10	12	V

Process parameters

Name	Description	Low	Typ	High	Unit
BDO_SFT6	csft6 breakdown voltage @ Ibr=1µA	35	-	-	V
CA_SFT6_B	csft6 capacitance per cell @ Vbias=0V, L=10.8µm, W=4.48µm	56.4	61.5	66.6	fF
IL_SFT6	csft6 leakage current @ VL=10V	-	-	30	fA/cell
TC1_SFT6	csft6 temperature coefficient 1 @ Tnom=27°C	-	-70	-	1e-06/K

Note: The device csft6 is only available if modules MET5 and METMID are selected.

Matching parameters

Name	Description	Low	Typ	High	Unit
SC_SFT6	standard deviation capacitor mismatch	-	0.042	0.05	%
	Note: The values of this parameter do not reflect the statistics of the process. The high value corresponds to 1 unit cell; the typical value is valid for >= 8 unit cells.				

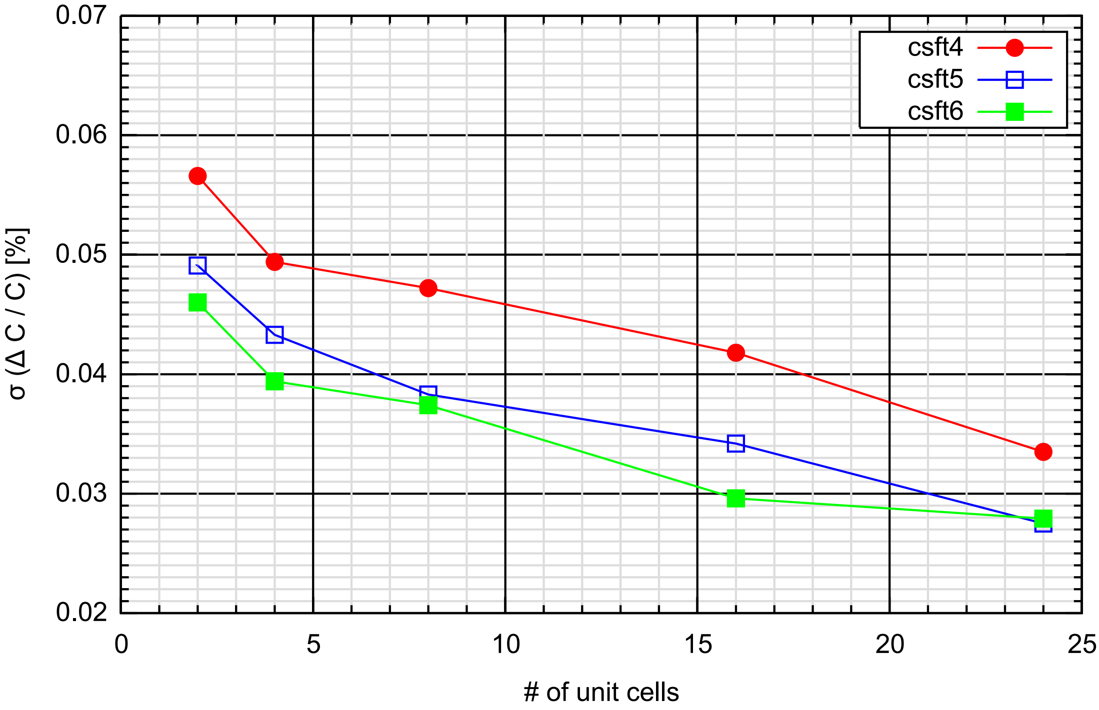

Figure 3.26 Device csft4, csft5, csft6: capacitor matching vs. number of fringe cap unit cells (typical values)

csft6a

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-50	-45	45	50	V
Vterm1-Vterm2	-40°C to 175°C	-50	-45	45	50	V

Process parameters

Name	Description	Low	Typ	High	Unit
BDO_SFT6A	csft6a breakdown voltage @ Ibr=1μA	70	-	-	V
CA_SFT6A_B	csft6a capacitance per cell @ Vbias=0V, L=11.1μm, W=5.76μm	42.1	46.6	51.1	fF
IL_SFT6A	csft6a leakage current @ VL=45V	-	-	35	fA/cell
TC1_SFT6A	csft6a temperature coefficient 1 @ Tnom=27°C	-	-70	-	1e-06/K

Note: The device csft6a is only available if modules MET5 and METMID are selected.

Matching parameters

Name	Description	Low	Typ	High	Unit
SC_SFT6A	standard deviation capacitor mismatch	-	0.026	0.036	%
	Note: The values of this parameter do not reflect the statistics of the process. The high value corresponds to 1 unit cell; the typical value is valid for >= 8 unit cells.				

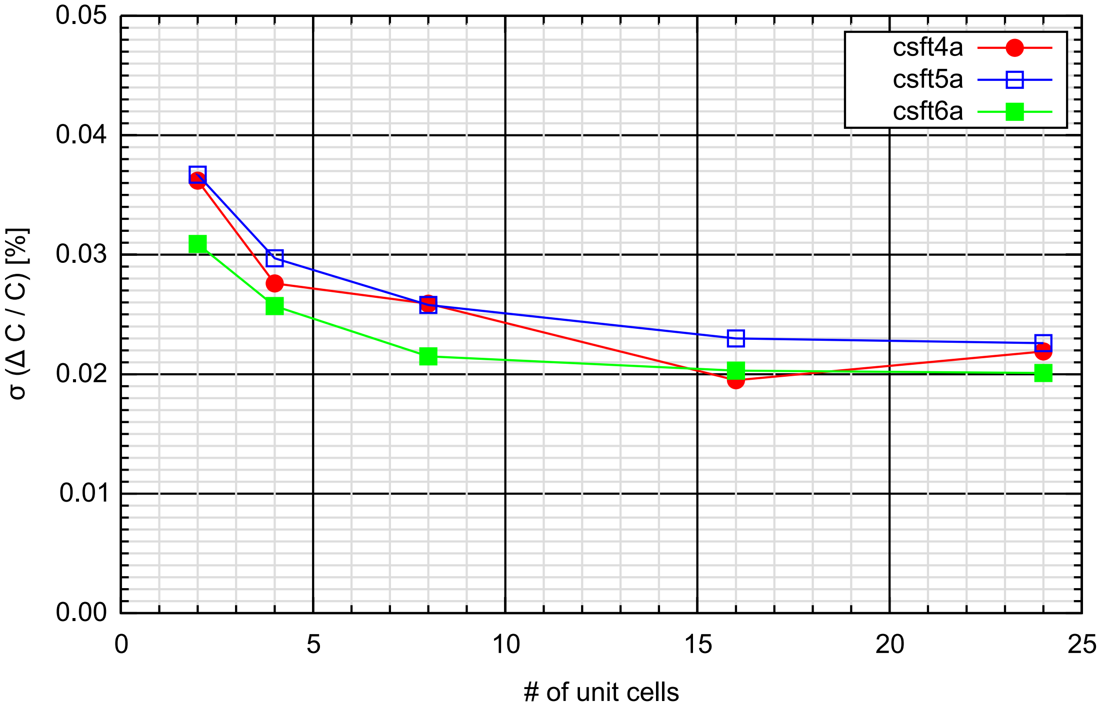

Figure 3.27 Device csft4a, csft5a, csft6a: capacitor matching vs. number of fringe cap unit cells (typical values)

3.6 METTHK module

3.6.1 Device independent parameters

Structural and geometrical parameters

Name	Description	Low	Typ	High	Unit
EPS_IMDTPL	metal underneath thick metal / thick metal equivalent dielectric constant	-	4	-	-
	Note: The values for dielectric permittivity are mean values only, because the dielectric consists of a stack of layers each with a different permittivity				
THD_IMDTPL	thick metal – top metal dielectric thickness	890	1000	1110	nm
TH_MTPL	thick metal thickness	2800	3110	3420	nm

Sheet and contact resistance parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSR_MTPLB	thick metal sheet resistance	7.7	8.9	10.1	11.3	12.5	mΩ/□
RVI_VTPL	thick via resistance	-	0.9	1.2	1.8	2.4	Ω/via
TC1_VTPL	VIATPL resistance temperature coefficient 1	-	-	1.35	-	-	1e-03/K
TC2_VTPL	VIATPL resistance temperature coefficient 2	-	-	0	-	-	1e-06/K²

Parasitic capacitance parameters

The following table provides a principal overview with respect to interconnect capacitances. More extensive data will be available on request.

Name	Description	Typ	Unit
CC_MTLMTL	coupling capacitance thick metal – thick metal	78	aF/µm
CPAMTLDIFF5	thick metal – active area capacitance (5 metal layers with METTP and METTHK)	4.8	aF/µm²
CPAMTLDIFF6	thick metal – active area capacitance (6 metal layers with METTP and METTHK)	4.1	aF/µm²
CPAMTLM15	thick metal – metal 1 area capacitance (5 metal layers with METTP and METTHK)	6.1	aF/µm²
CPAMTLM16	thick metal – metal 1 area capacitance (6 metal layers with METTP and METTHK)	4.9	aF/µm²
CPAMTLM25	thick metal – metal 2 area capacitance (5 metal layers with METTP and METTHK)	8	aF/µm²
CPAMTLM26	thick metal – metal 2 area capacitance (6 metal layers with METTP and METTHK)	6.1	aF/µm²
CPAMTLM35	thick metal – metal 3 area capacitance (5 metal layers with METTP and METTHK)	11.8	aF/µm²
CPAMTLM36	thick metal – metal 3 area capacitance (6 metal layers with METTP and METTHK)	8	aF/µm²
CPAMTLM46	thick metal – metal 4 area capacitance (6 metal layers with METTP and METTHK)	11.8	aF/µm²
CPAMTLMTP5	thick metal – top metal area capacitance (5 metal layers with METTP and METTHK)	35.7	aF/µm²
CPAMTLMTP6	thick metal – top metal area capacitance (6 metal layers with METTP and METTHK)	35.7	aF/µm²

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Name	Description	Typ	Unit
CPAMTLP15	thick metal – poly 1 area capacitance (5 metal layers with METTP and METTHK)	5	aF/µm²
CPAMTLP16	thick metal – poly 1 area capacitance (6 metal layers with METTP and METTHK)	4.1	aF/µm²
CPAMTLSTI5	thick metal – field area (STI) area capacitance (5 metal layers with METTP and METTHK)	4.6	aF/µm²
CPAMTLSTI6	thick metal – field area (STI) area capacitance (6metal layers with METTP and METTHK)	3.9	aF/µm²
CPPMTLDIFF5	thick metal – active perimeter capacitance (5 metal layers with METTP and METTHK)	8.8	aF/µm
CPPMTLDIFF6	thick metal – active perimeter capacitance (6 metal layers with METTP and METTHK)	8	aF/µm
CPPMTLM15	thick metal – metal 1 perimeter capacitance (5 metal layers with METTP and METTHK)	8	aF/µm
CPPMTLM16	thick metal – metal 1 perimeter capacitance (6 metal layers with METTP and METTHK)	6.7	aF/µm
CPPMTLM25	thick metal – metal 2 perimeter capacitance (5 metal layers with METTP and METTHK)	10.1	aF/µm
CPPMTLM26	thick metal – metal 2 perimeter capacitance (6 metal layers with METTP and METTHK)	8	aF/µm
CPPMTLM35	thick metal – metal 3 perimeter capacitance (5 metal layers with METTP and METTHK)	13.9	aF/µm
CPPMTLM36	thick metal – metal 3 perimeter capacitance (6 metal layers with METTP and METTHK)	10.1	aF/µm
CPPMTLM46	thick metal – metal 4 perimeter capacitance (6 metal layers with METTP and METTHK)	13.9	aF/µm
CPPMTLMTP5	thick metal – top metal perimeter capacitance (5 metal layers with METTP and METTHK)	31.1	aF/µm
CPPMTLMTP6	thick metal – top metal perimeter capacitance (6 metal layers with METTP and METTHK)	31.1	aF/µm
CPPMTLP15	thick metal – poly 1 perimeter capacitance (5 metal layers with METTP and METTHK)	6.7	aF/µm
CPPMTLP16	thick metal – poly 1 perimeter capacitance (6 metal layers with METTP and METTHK)	5.8	aF/µm
CPPMTLSTI5	thick metal – field perimeter (STI) perimeter capacitance (5 metal layers with METTP and METTHK)	8.6	aF/µm
CPPMTLSTI6	thick metal – field perimeter (STI) perimeter capacitance (6metal layers with METTP and METTHK)	7.9	aF/µm

Physical layer operating conditions

Name	Structure	Temp. range	Abs. min	Min	Max	Abs. max	Unit
JMax_DC[1,2]	Thick Metal	-40°C to 175°C	-	-	6	32	mA/µm
JMax_VI_DC[2]	Thick Via	-40°C to 175°C	-	-	1	32	mA/via
JMax_AC[1,3]	Thick Metal	-40°C to 175°C	-	-	10	32	mA/µm
JMax_VI_AC[3]	Thick Via	-40°C to 175°C	-	-	4.5	32	mA/via
T_Factor_1e4[4,5]	Thick Metal	-40°C to 85°C	-	3.13	-	-	-
T_Factor_1e4[4,5]	Thick Via	-40°C to 85°C	-	4.25	-	-	-
T_Factor_1e4[6,5]	Thick Metal	85°C to 125°C	-	1	-	-	-

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Name	Structure	Temp. range	Abs. min	Min	Max	Abs. max	Unit
T_Factor_1e4[6][5]	Thick Via	85°C to 125°C	-	1.16	-	-	-
T_Factor_1e4[7][5]	Thick Metal	125°C to 175°C	-	0.32	-	-	-
T_Factor_1e4[7][5]	Thick Via	125°C to 175°C	-	0.31	-	-	-
T_Factor_1e5[4][5]	Thick Metal	-40°C to 85°C	-	1	-	-	-
T_Factor_1e5[4][5]	Thick Via	-40°C to 85°C	-	1.35	-	-	-
T_Factor_1e5[6][5]	Thick Metal	85°C to 125°C	-	0.32	-	-	-
T_Factor_1e5[6][5]	Thick Via	85°C to 125°C	-	0.37	-	-	-
T_Factor_1e5[7][5]	Thick Metal	125°C to 175°C	-	0.1	-	-	-
T_Factor_1e5[7][5]	Thick Via	125°C to 175°C	-	0.1	-	-	-

Note 1 Valid for all widths.

Note 2 Max values of JMAX*DC refer to rms/avg values. Abs. max values of JMAX*DC refer to peak values.

Note 3 Max values of JMAX*AC refer to rms values. Abs. max values of JMAX*AC refer to peak values.

Note 4 The temperature correction factor remains constant at the stated value across the whole temperatures range.

Note 5 Temperature correction factors allow the scaling of the current density according to the required lifetime and temperature. For more detailed information, please refer to the Interconnect reliability sections of the SpecXplorer or Process Reliability Specification.

Note 6 The temperature correction factor is interpolated between given values for temperatures above 85°C.

Note 7 The temperature correction factor is interpolated between given values for temperatures above 125°C

3.6.2 Device parameters

rmtpl

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-50	-45	45	50	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSR_MTPLB	thick metal sheet resistance	7.7	8.9	10.1	11.3	12.5	mΩ/□
TC1_MTPL	thick metal temperature coefficient 1	-	-	3.8	-	-	1e-03/K
TC2_MTPL	thick metal temperature coefficient 2	-	-	0	-	-	1e-06/K^2
WER_MTPLB	thick metal resistor effective width @ W=3µm	-	2.55	3	3.45	-	µm

3.7 CPOD module

3.7.1 Device independent parameters

Sheet and contact resistance parameters

Name	Description	Low	Typ	High	Unit
RSR_BNIMP	BNIMP sheet resistance (cpod)	290	310	330	Ω/☐

3.7.2 Device parameters

cpod

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGB	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VBpsub(1	-40°C to 175°C	-0.5	0	18	20	V

Note 1 VBpsub is the voltage between the bottom active terminal of the device and the bulk material underneath the device. The bottom plate must have a positive voltage related to p-substrate.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_POD	cpod breakdown voltage @ Ibr=0.1nA/µm²	3	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CAA_POD	cpod area capacitance @ Vbias=0V	6.5	7.1	7.7	8.3	8.9	fF/µm²
CAP_POD	cpod perimeter capacitance	-	0.3	0.35	0.4	-	fF/µm
TCC_POD	cpod capacitance temperature coefficient	-	-	-0.015	-	-	1e-03/K
VC1_POD	cpod capacitance voltage coefficient 1	-	-	90000	-	-	ppm/V
VC2_POD	cpod capacitance voltage coefficient 2	-	-	-36000	-	-	ppm/V²

Matching parameters

Name	Description	Low	Typ	High	Unit
AC_POD	Pelgrom coefficient capacitor mismatch	-	0.7	1.14	%µm
	Note: The typical values of this parameter is valid for a device area larger than 100µm².				

3.8 CPODHV module

3.8.1 Device independent parameters

Sheet and contact resistance parameters

Name	Description	Low	Typ	High	Unit
RSR_BNIMPHV	BNIMP sheet resistance (cpodhv)	760	815	870	Ω/☐

3.8.2 Device parameters

cpodhv

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGB	-40°C to 175°C	-20	-18	18	20	V
VBpsub[(1]	-40°C to 175°C	-0.5	0	18	20	V

Note 1 VBpsub is the voltage between the bottom active terminal of the device and the bulk material underneath the device. The bottom plate must have a positive voltage related to p-substrate.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_PODHV	cpodhv breakdown voltage @ Ibr=0.1nA/µm²	30	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CAA_PODHV	cpodhv area capacitance @ Vbias=0V	0.85	0.93	1	1.07	1.15	fF/µm²
CAP_PODHV	cpodhv perimeter capacitance	-	0.15	0.18	0.21	-	fF/µm
TCC_PODHV	cpodhv capacitance temperature coefficient	-	-	0.08	-	-	1e-03/K
VC1_PODHV	cpodhv capacitance voltage coefficient 1	-	-	1700	-	-	ppm/V
VC2_PODHV	cpodhv capacitance voltage coefficient 2	-	-	-80	-	-	ppm/V²

3.9 MRPOLY module

3.9.1 Device parameters

rpp1k1, rpp1k1_3

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk[1	-40°C to 175°C	-50	-45	45	50	V
JDL	-40°C to 175°C	-	-	0.25	-	mA/µm

Note 1 An inversion layer is formed in the bulk underneath the poly if the terminal-to-bulk voltage exceeds the field threshold voltage. The field threshold voltages are specified in section "3. Process & Device Parameters".

Process parameters

Negative values are considered as absolute values for their limits.

Name	Description	LSL	Low	Typ	High	USL	Unit
RSE_MRPSB	medium resistance poly 1 silicide block edge resistance per terminal	-	-	100	-	-	Ωµm
RSR_MRP	medium resistive poly 1 sheet resistance	760	860	960	1060	1160	Ω/☐
TC1MRP	medium resistive poly1 temperature coefficient 1	-	-0.95	-0.85	-0.75	-	1e-03/K
TC1MRPRSE	medium resistance poly 1 silicide block edge resistance temperature coefficient 1	-	-	-1.5	-	-	1e-03/K
TC2MRP	medium resistive poly1 temperature coefficient 2	-	1.1	1.6	2.1	-	1e-06/K²
TC2MRPRSE	medium resistance poly 1 silicide block edge resistance temperature coefficient 2	-	-	3	-	-	1e-06/K²
VCBMRP	medium resistive poly 1 bulk voltage coefficient	-	-	-0.122	-	-	1e-03/V
WERMRP	medium resistive poly 1 effective width @ W=0.42µm	-	0.34	0.37	0.4	-	µm

Matching parameters

Name	Description	Typ	Unit
AR_MRP	Pelgrom coefficient resistor mismatch	1.79	%µm
DWRMRP	resistor delta width	0.05	µm

3.10 ISOMOS module

3.10.1 Device independent parameters

Structural and geometrical parameters

Name	Description	Typ	Unit
XJ_DNW	DNWELLMV/DNWELL junction depth	2.8	µm
XJ_PW1DNW	PWELL1 in DNWELLMV/DNWELL junction depth	1	µm
	Note: This parameter is only available if the HVMOS and ISOMOS modules are selected.		
XJ_PW2DNW	PWELL2 in DNWELLMV/DNWELL junction depth	1	µm
	Note: This parameter is only available if the HVMOS and ISOMOS modules are selected.		

Sheet and contact resistance parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSSNWDMV	DNWELLMV sheet resistance (STI terminated) @ Vterm=3.3V, W=10µm	1.2	1.35	1.5	1.65	1.8	kΩ/☐

3.10.2 Device parameters

nei

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VGD	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDB	-40°C to 175°C	-0.5	0	1.98	2.3	V
VSB	-40°C to 175°C	-0.5	0	1.98	2.3	V

Note: The node B (BULK) is: PWELL1.

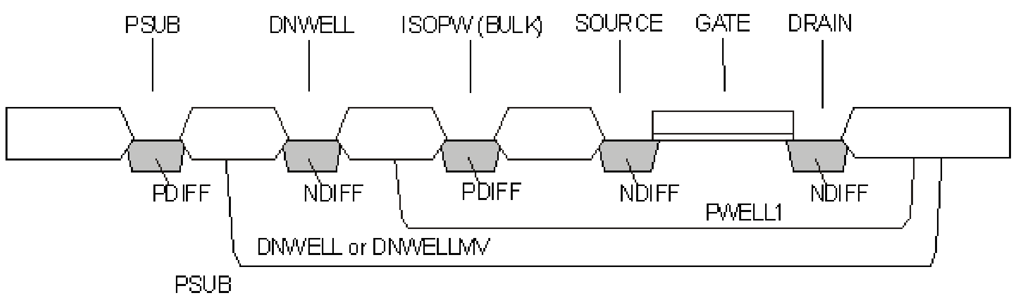

Figure 3.28 Additional Operating Conditions

Note: nei in DNWELL

$$\begin{aligned} V_{PSUB} &\leq V_{DNWELL} \leq V_{PSUB} + 45(50)V \\ V_{DNWELL} - 8(10)V &\leq V_{PWELL1} \leq V_{DNWELL} \end{aligned}$$

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nei in DNWELLMV

$$\begin{array}{lllll} V_{PSUB} & \leq & V_{DNWELL} & \leq & V_{PSUB} + 10(12)V \\ V_{DNWELLMV} - 8(10)V & \leq & V_{PWELL1} & \leq & V_{DNWELLMV} \end{array}$$

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNEIS	drain-source breakdown @ VG=0V, Id=1µA, L=0.18µm	3.6	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXNEI	mobility exponent	-	-	-1.7	-	-	-
FC_NEI	corner frequency @ VD=1.8V, Id=1µA, L=10µm, W=10µm	-	-	1.21	-	-	kHz
GAMNEI	body factor long channel @ L=10µm, W=10µm	-	-	0.7	-	-	√V
IDSNEIS	saturation current @ VG=1.8V, VD=1.8V, L=0.18µm, W=10µm	340	407	475	543	610	µA/µm
IOFNEIS	off-state leakage @ VD=1.8V, L=0.18µm, W=10µm	-	-	-	3	-	pA/µm
ISBNEIS	bulk current @ VD=1.8V, L=0.18µm	-	-	0.05	-	-	µA/µm
KP_NEI	gain factor long channel @ L=10µm, W=10µm	-	-	243	-	-	µA/V²
LEFNEI	effective channel length @ L=0.18µm	-	-	0.16	-	-	µm
NOINEI	Input referred noise @ VD=1.8V, Id=1µA, f=1Hz, L=10µm, W=10µm	-	-	11.2	-	-	µV.µm/√(Hz)
STSNEI	subthreshold slope @ VD=1.8V	-	-	12	-	-	decade/V
TC_VTXNEI	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	-0.89	-	-	mV/K
U0_NEI	effective mobility	-	-	307	-	-	cm²/Vs
VTINEIL	threshold voltage long channel @ VD=0.1V, L=10µm, W=10µm	0.47	0.5	0.53	0.56	0.59	V
VTINEIS	threshold voltage short channel @ VD=0.1V, L=0.18µm, W=10µm	0.46	0.52	0.58	0.64	0.7	V
VTINEISS	threshold voltage small channel @ VD=0.1V, L=0.18µm, W=0.22µm	-	-	0.45	-	-	V
VTXNEIS	extrapolated threshold voltage short channel @ VD=0.1V, L=0.18µm, W=10µm	-	-	0.65	-	-	V
WEFNEI	effective channel width @ W=0.22µm	-	-	0.17	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTNEI	Pelgrom coefficient gain factor mismatch	0.63	%µm
AIDNEI00	Pelgrom coefficient ID mismatch @ VG-VT=0V	7.43	%µm
AIDNEI01	Pelgrom coefficient ID mismatch @ VG-VT=0.1V	5.03	%µm
AIDNEI02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	3.55	%µm
AIDNEI04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	2.05	%µm
AIDNEI06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	1.4	%µm
AIDNEI08	Pelgrom coefficient ID mismatch @ VG-VT=0.8V	1.05	%µm
AIDNEI10	Pelgrom coefficient ID mismatch @ VG-VT=1V	0.86	%µm

⇒

Name	Description	Typ	Unit
AIDNEI14	Pelgrom coefficient ID mismatch @ VG-VT=1.4V	0.64	%µm
AVTNEI	Pelgrom coefficient VT mismatch	5.1	mVµm
DLTNEI	transistor delta length	0.02	µm
DWTNEI	transistor delta width	0.05	µm

nei_m_6

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VGD	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDB	-40°C to 175°C	-0.5	0	1.98	2.3	V
VSB	-40°C to 175°C	-0.5	0	1.98	2.3	V
VIpsub	-40°C to 175°C	-0.5	0	10	12	V
VIB	-40°C to 175°C	-0.5	0	8	10	V

Note: The node B (BULK) is: PWELL1.

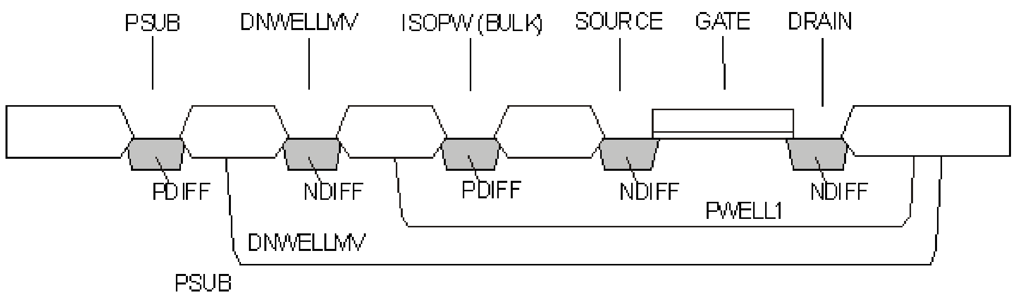

Figure 3.29 Additional Operating Conditions

Note: nei_m_6 in DNWELLMV

$$\begin{array}{lclcl} V_{PSUB} & \leq & V_{DNWELL} & \leq & V_{PSUB} + 10(12)V \\ V_{DNWELLMV} - 8(10)V & \leq & V_{PWELL1} & \leq & V_{DNWELLMV} \end{array}$$

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNEIS	drain-source breakdown @ VG=0V, Id=1µA, L=0.18µm	3.6	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXNEI	mobility exponent	-	-	-1.7	-	-	-
FC_NEI	corner frequency @ VD=1.8V, Id=1µA, L=10µm, W=10µm	-	-	1.21	-	-	kHz
GAMNEI	body factor long channel @ L=10µm, W=10µm	-	-	0.7	-	-	√V

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Name	Description	LSL	Low	Typ	High	USL	Unit
IDSNEIS	saturation current @ VG=1.8V, VD=1.8V, L=0.18µm, W=10µm	340	407	475	543	610	µA/µm
IOFNEIS	off-state leakage @ VD=1.8V, L=0.18µm, W=10µm	-	-	-	3	-	pA/µm
ISBNEIS	bulk current @ VD=1.8V, L=0.18µm	-	-	0.05	-	-	µA/µm
KP_NEI	gain factor long channel @ L=10µm, W=10µm	-	-	243	-	-	µA/V²
LEFNEI	effective channel length @ L=0.18µm	-	-	0.16	-	-	µm
NOINEI	Input referred noise @ VD=1.8V, Id=1µA, f=1Hz, L=10µm, W=10µm	-	-	11.2	-	-	µV.µm/√(Hz)
STSNEI	subthreshold slope @ VD=1.8V	-	-	12	-	-	decade/V
TC_VTXNEI	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	-0.89	-	-	mV/K
U0_NEI	effective mobility	-	-	307	-	-	cm²/Vs
VTINEIL	threshold voltage long channel @ VD=0.1V, L=10µm, W=10µm	0.47	0.5	0.53	0.56	0.59	V
VTINEIS	threshold voltage short channel @ VD=0.1V, L=0.18µm, W=10µm	0.46	0.52	0.58	0.64	0.7	V
VTINEISS	threshold voltage small channel @ VD=0.1V, L=0.18µm, W=0.22µm	-	-	0.45	-	-	V
VTXNEIS	extrapolated threshold voltage short channel @ VD=0.1V, L=0.18µm, W=10µm	-	-	0.65	-	-	V
WEFNEI	effective channel width @ W=0.22µm	-	-	0.17	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTNEI	Pelgrom coefficient gain factor mismatch	0.63	%µm
AIDNEI00	Pelgrom coefficient ID mismatch @ VG-VT=0V	7.43	%µm
AIDNEI01	Pelgrom coefficient ID mismatch @ VG-VT=0.1V	5.03	%µm
AIDNEI02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	3.55	%µm
AIDNEI04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	2.05	%µm
AIDNEI06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	1.4	%µm
AIDNEI08	Pelgrom coefficient ID mismatch @ VG-VT=0.8V	1.05	%µm
AIDNEI10	Pelgrom coefficient ID mismatch @ VG-VT=1V	0.86	%µm
AIDNEI14	Pelgrom coefficient ID mismatch @ VG-VT=1.4V	0.64	%µm
AVTNEI	Pelgrom coefficient VT mismatch	5.1	mVµm
DLTNEI	transistor delta length	0.02	µm
DWTNEI	transistor delta width	0.05	µm

pei

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VGD	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDB	-40°C to 175°C	-2.3	-1.98	0	0.5	V

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Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VSB	-40°C to 175°C	-2.3	-1.98	0	0.5	V
VBpsub[1]	-40°C to 175°C	-0.5	0	10	12	V

Note 1 If DNWELL instead of DNWELLMV is used for the isolated PMOS transistors, then max. VBpsub = 45 (50)V.

Note: The node B (BULK) is: NWELL1.

Process parameters

Negative values are considered as absolute values for their limits.

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPEIS	drain-source breakdown @ VG=0V, Id=-1µA, L=0.18µm	3.6	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXPEI	mobility exponent	-	-	-1	-	-	-
FC_PEI	corner frequency @ VD=1.8V, Id=1µA, L=10µm, W=10µm	-	-	0.3	-	-	kHz
GAMPEI	body factor long channel @ L=10µm, W=10µm	-	-	0.86	-	-	√V
IDSPEIS	saturation current @ VG=-1.8V, VD=-1.8V, L=0.18µm, W=10µm	110	140	170	200	230	µA/µm
IOFPEIS	off-state leakage @ VD=-1.8V, L=0.18µm, W=10µm	-	-	-	3	-	pA/µm
ISBPEIS	bulk current @ VD=-1.8V, L=0.18µm	-	-	0.1	-	-	nA/µm
KP_PEI	gain factor long channel @ L=10µm, W=10µm	-	-	52	-	-	µA/V²
LEFPEI	effective channel length @ L=0.18µm	-	-	0.15	-	-	µm
NOIPEI	Input referred noise @ VD=-1.8V, Id=-1µA, f=1Hz, L=10µm, W=10µm	-	-	17	-	-	µV.µm/ √(Hz)
STSPEI	subthreshold slope @ VD=-1.8V	-	-	11	-	-	decade/V
TC_VTXPEI	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	0.91	-	-	mV/K
U0_PEI	effective mobility	-	-	59	-	-	cm²/Vs
VTIPEIL	threshold voltage long channel @ VD=-0.1V, L=10µm, W=10µm	-0.64	-0.67	-0.7	-0.73	-0.76	V
VTIPEIS	threshold voltage short channel @ VD=-0.1V, L=0.18µm, W=10µm	-0.55	-0.6	-0.65	-0.7	-0.75	V
VTIPEISS	threshold voltage small channel @ VD=-0.1V, L=0.18µm, W=0.22µm	-	-	-0.6	-	-	V
VTXPEIS	extrapolated threshold voltage short channel @ VD=-0.1V, L=0.18µm, W=10µm	-	-	-0.65	-	-	V
WEFPEI	effective channel width @ W=0.22µm	-	-	0.25	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTPEI	Pelgrom coefficient gain factor mismatch	1.01	%µm
AIDPEI00	Pelgrom coefficient ID mismatch @ VG-VT=0V	7.79	%µm
AIDPEI01	Pelgrom coefficient ID mismatch @ VG-VT=0.1V	5.14	%µm
AIDPEI02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	3.56	%µm
AIDPEI04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	2.11	%µm

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Name	Description	Typ	Unit
AIDPEI06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	1.52	%µm
AIDPEI08	Pelgrom coefficient ID mismatch @ VG-VT=0.8V	1.21	%µm
AIDPEI10	Pelgrom coefficient ID mismatch @ VG-VT=1V	1.03	%µm
AIDPEI14	Pelgrom coefficient ID mismatch @ VG-VT=1.4V	0.81	%µm
AVTPEI	Pelgrom coefficient VT mismatch	5.09	mVµm
DLTPEI	transistor delta length	0.03	µm
DWTPEI	transistor delta width	-0.03	µm

pei_m_5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VGD	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDB	-40°C to 175°C	-2.3	-1.98	0	0.5	V
VSB	-40°C to 175°C	-2.3	-1.98	0	0.5	V
VBpsub	-40°C to 175°C	-0.5	0	10	12	V

Note: The node B (BULK) is: NWELL1.

Process parameters

Negative values are considered as absolute values for their limits.

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPEIS	drain-source breakdown @ VG=0V, Id=-1µA, L=0.18µm	3.6	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXPEI	mobility exponent	-	-	-1	-	-	-
FC_PEI	corner frequency @ VD=1.8V, Id=1µA, L=10µm, W=10µm	-	-	0.3	-	-	kHz
GAMPEI	body factor long channel @ L=10µm, W=10µm	-	-	0.86	-	-	√V
IDSPEIS	saturation current @ VG=-1.8V, VD=-1.8V, L=0.18µm, W=10µm	110	140	170	200	230	µA/µm
IOFPEIS	off-state leakage @ VD=-1.8V, L=0.18µm, W=10µm	-	-	-	3	-	pA/µm
ISBPEIS	bulk current @ VD=-1.8V, L=0.18µm	-	-	0.1	-	-	nA/µm
KP_PEI	gain factor long channel @ L=10µm, W=10µm	-	-	52	-	-	µA/V²
LEFPEI	effective channel length @ L=0.18µm	-	-	0.15	-	-	µm
NOIPEI	Input referred noise @ VD=-1.8V, Id=-1µA, f=1Hz, L=10µm, W=10µm	-	-	17	-	-	µV.µm/ √(Hz)
STSPEI	subthreshold slope @ VD=-1.8V	-	-	11	-	-	decade/V
TC_VTXPEI	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	0.91	-	-	mV/K
U0_PEI	effective mobility	-	-	59	-	-	cm²/Vs
VTIPEIL	threshold voltage long channel @ VD=-0.1V, L=10µm, W=10µm	-0.64	-0.67	-0.7	-0.73	-0.76	V

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Name	Description	LSL	Low	Typ	High	USL	Unit
VTIPEIS	threshold voltage short channel @ VD=-0.1V, L=0.18µm, W=10µm	-0.55	-0.6	-0.65	-0.7	-0.75	V
VTIPEISS	threshold voltage small channel @ VD=-0.1V, L=0.18µm, W=0.22µm	-	-	-0.6	-	-	V
VTXPEIS	extrapolated threshold voltage short channel @ VD=-0.1V, L=0.18µm, W=10µm	-	-	-0.65	-	-	V
WEFPEI	effective channel width @ W=0.22µm	-	-	0.25	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTPEI	Pelgrom coefficient gain factor mismatch	1.01	%µm
AIDPEI00	Pelgrom coefficient ID mismatch @ VG-VT=0V	7.79	%µm
AIDPEI01	Pelgrom coefficient ID mismatch @ VG-VT=0.1V	5.14	%µm
AIDPEI02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	3.56	%µm
AIDPEI04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	2.11	%µm
AIDPEI06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	1.52	%µm
AIDPEI08	Pelgrom coefficient ID mismatch @ VG-VT=0.8V	1.21	%µm
AIDPEI10	Pelgrom coefficient ID mismatch @ VG-VT=1V	1.03	%µm
AIDPEI14	Pelgrom coefficient ID mismatch @ VG-VT=1.4V	0.81	%µm
AVTPEI	Pelgrom coefficient VT mismatch	5.09	mVµm
DLTPEI	transistor delta length	0.03	µm
DWTPEI	transistor delta width	-0.03	µm

ne3i

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-4	-3.6	3.6	4	V
VGD	-40°C to 175°C	-4	-3.6	3.6	4	V
VDS	-40°C to 175°C	-4	-3.6	3.6	4	V
VDB	-40°C to 175°C	-0.5	0	3.6	4	V
VSB	-40°C to 175°C	-0.5	0	3.6	4	V

Note: The node B (BULK) is: PWELL2

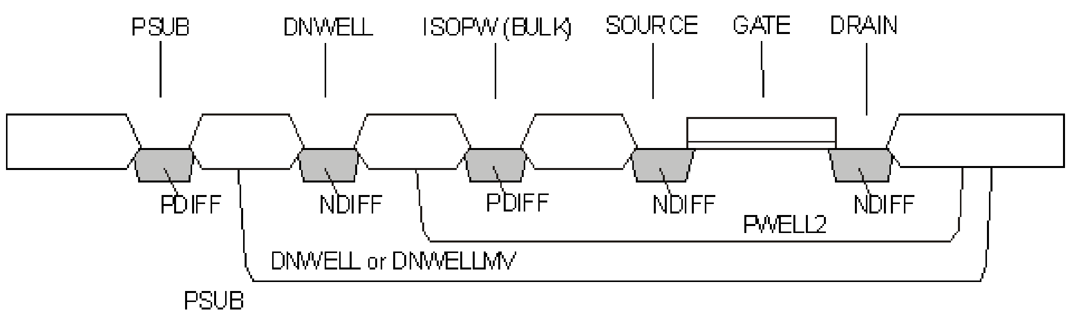

Figure 3.30 Additional Operating Conditions

Note: ne3i in DNWELL

$$\begin{array}{lllll} V_{PSUB} & \leq & V_{DNWELL} & \leq & V_{PSUB} + 45(50)V \\ V_{DNWELL} - 8(10)V & \leq & V_{PWELL2} & \leq & V_{DNWELL} \end{array}$$

ne3i in DNWELLMV

$$\begin{array}{lllll} V_{PSUB} & \leq & V_{DNWELLMV} & \leq & V_{PSUB} + 10(12)V \\ V_{DNWELLMV} - 8(10)V & \leq & V_{PWELL2} & \leq & V_{DNWELLMV} \end{array}$$

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNE3IS	drain-source breakdown @ VG=0V, Id=1µA, L=0.35µm	5	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXNE3I	mobility exponent	-	-	-1.7	-	-	-
FC_NE3I	corner frequency @ VD=3.3V, Id=1µA, L=10µm, W=10µm	-	-	1.89	-	-	kHz
GAMNE3I	body factor long channel @ L=10µm, W=10µm	-	-	0.92	-	-	√V
IDSNE3IS	saturation current @ VG=3.3V, VD=3.3V, L=0.35µm, W=10µm	525	570	615	660	705	µA/µm
IOFNE3IS	off-state leakage @ VD=3.3V, L=0.35µm, W=10µm	-	-	-	3	-	pA/µm
ISBNE3IS	bulk current @ VD=3.3V, L=0.35µm	-	-	1	-	-	µA/µm
KP_NE3I	gain factor long channel @ L=10µm, W=10µm	-	-	190	-	-	µA/V²
LEFNE3I	effective channel length @ L=0.35µm	-	-	0.33	-	-	µm
NOINE3I	Input referred noise @ VD=3.3V, Id=1µA, f=1Hz, L=10µm, W=10µm	-	-	19.2	-	-	µV.µm/ √(Hz)
STSNE3I	subthreshold slope @ VD=3.3V	-	-	11	-	-	decade/V
TC_VTXNE3I	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	-1	-	-	mV/K
U0_NE3I	effective mobility	-	-	360	-	-	cm²/Vs
VTINE3IL	threshold voltage long channel @ VD=0.1V, L=10µm, W=10µm	0.6	0.63	0.66	0.69	0.72	V
VTINE3IS	threshold voltage short channel @ VD=0.1V, L=0.35µm, W=10µm	0.585	0.625	0.665	0.705	0.745	V
VTINE3ISS	threshold voltage small channel @ VD=0.1V, L=0.35µm, W=0.22µm	-	-	0.53	-	-	V
VTXNE3IS	extrapolated threshold voltage short channel @ VD=0.1V, L=0.35µm, W=10µm	-	-	0.72	-	-	V
WEFNE3I	effective channel width @ W=0.22µm	-	-	0.18	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTNE3I	Pelgrom coefficient gain factor mismatch	0.98	%µm
AIDNE3I00	Pelgrom coefficient ID mismatch @ VG-VT=0V	13.2	%µm

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Name	Description	Typ	Unit
AIDNE3I02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	6.49	%µm
AIDNE3I04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	3.71	%µm
AIDNE3I06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	2.48	%µm
AIDNE3I10	Pelgrom coefficient ID mismatch @ VG-VT=1V	1.45	%µm
AIDNE3I15	Pelgrom coefficient ID mismatch @ VG-VT=1.5V	0.97	%µm
AIDNE3I20	Pelgrom coefficient ID mismatch @ VG-VT=2V	0.75	%µm
AIDNE3I30	Pelgrom coefficient ID mismatch @ VG-VT=3V	0.55	%µm
AVTNE3I	Pelgrom coefficient VT mismatch	9.24	mVµm
DLTNE3I	transistor delta length	0.02	µm
DWTNE3I	transistor delta width	0.04	µm

ne3i_m_6

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-4	-3.6	3.6	4	V
VGD	-40°C to 175°C	-4	-3.6	3.6	4	V
VDS	-40°C to 175°C	-4	-3.6	3.6	4	V
VDB	-40°C to 175°C	-0.5	0	3.6	4	V
VSB	-40°C to 175°C	-0.5	0	3.6	4	V
VIpsub	-40°C to 175°C	-0.5	0	10	12	V
VIB	-40°C to 175°C	-0.5	0	8	10	V

Note: The node B (BULK) is: PWELL2

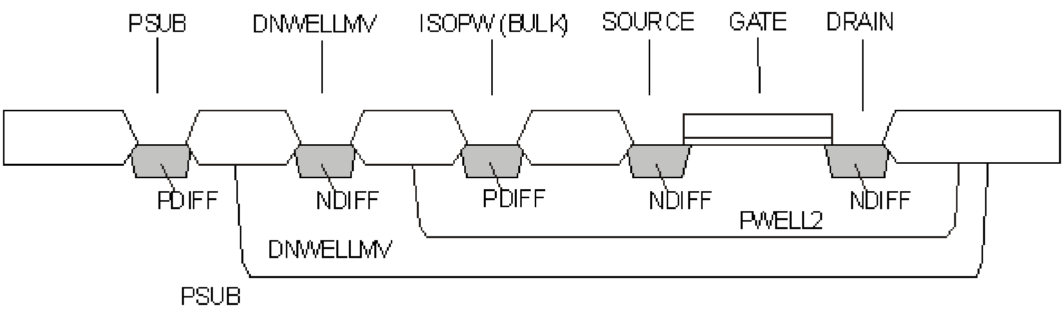

Figure 3.31 Additional Operating Conditions

Note: ne3i_m_6 in DNWELLMV

$$\begin{array}{lclcl} V_{PSUB} & \leq & V_{DNWELLMV} & \leq & V_{PSUB} + 10(12)V \\ V_{DNWELLMV} - 8(10)V & \leq & V_{PWELL2} & \leq & V_{DNWELLMV} \end{array}$$

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNE3IS	drain-source breakdown @ VG=0V, Id=1µA, L=0.35µm	5	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						

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Name	Description	LSL	Low	Typ	High	USL	Unit
BEXNE3I	mobility exponent	-	-	-1.7	-	-	-
FC_NE3I	corner frequency @ VD=3.3V, Id=1µA, L=10µm, W=10µm	-	-	1.89	-	-	kHz
GAMNE3I	body factor long channel @ L=10µm, W=10µm	-	-	0.92	-	-	√V
IDSNE3IS	saturation current @ VG=3.3V, VD=3.3V, L=0.35µm, W=10µm	525	570	615	660	705	µA/µm
IOFNE3IS	off-state leakage @ VD=3.3V, L=0.35µm, W=10µm	-	-	-	3	-	pA/µm
ISBNE3IS	bulk current @ VD=3.3V, L=0.35µm	-	-	1	-	-	µA/µm
KP_NE3I	gain factor long channel @ L=10µm, W=10µm	-	-	190	-	-	µA/V²
LEFNE3I	effective channel length @ L=0.35µm	-	-	0.33	-	-	µm
NOINE3I	Input referred noise @ VD=3.3V, Id=1µA, f=1Hz, L=10µm, W=10µm	-	-	19.2	-	-	µV.µm/√(Hz)
STSNE3I	subthreshold slope @ VD=3.3V	-	-	11	-	-	decade/V
TC_VTXNE3I	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	-1	-	-	mV/K
U0_NE3I	effective mobility	-	-	360	-	-	cm²/Vs
VTINE3IL	threshold voltage long channel @ VD=0.1V, L=10µm, W=10µm	0.6	0.63	0.66	0.69	0.72	V
VTINE3IS	threshold voltage short channel @ VD=0.1V, L=0.35µm, W=10µm	0.585	0.625	0.665	0.705	0.745	V
VTINE3ISS	threshold voltage small channel @ VD=0.1V, L=0.35µm, W=0.22µm	-	-	0.53	-	-	V
VTXNE3IS	extrapolated threshold voltage short channel @ VD=0.1V, L=0.35µm, W=10µm	-	-	0.72	-	-	V
WEFNE3I	effective channel width @ W=0.22µm	-	-	0.18	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTNE3I	Pelgrom coefficient gain factor mismatch	0.98	%µm
AIDNE3I00	Pelgrom coefficient ID mismatch @ VG-VT=0V	13.2	%µm
AIDNE3I02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	6.49	%µm
AIDNE3I04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	3.71	%µm
AIDNE3I06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	2.48	%µm
AIDNE3I10	Pelgrom coefficient ID mismatch @ VG-VT=1V	1.45	%µm
AIDNE3I15	Pelgrom coefficient ID mismatch @ VG-VT=1.5V	0.97	%µm
AIDNE3I20	Pelgrom coefficient ID mismatch @ VG-VT=2V	0.75	%µm
AIDNE3I30	Pelgrom coefficient ID mismatch @ VG-VT=3V	0.55	%µm
AVTNE3I	Pelgrom coefficient VT mismatch	9.24	mVµm
DLTNE3I	transistor delta length	0.02	µm
DWTNE3I	transistor delta width	0.04	µm

pe3i

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-4	-3.6	3.6	4	V
VGD	-40°C to 175°C	-4	-3.6	3.6	4	V
VDS	-40°C to 175°C	-4	-3.6	3.6	4	V
VDB	-40°C to 175°C	-4	-3.6	0	0.5	V
VSB	-40°C to 175°C	-4	-3.6	0	0.5	V
VBpsub[(1]	-40°C to 175°C	-0.5	0	10	12	V

Note 1 If DNWELL instead of DNWELLMV is used for the isolated PMOS transistors, then max. VBpsub = 45 (50)V.

Note: The node B (BULK) is: NWELL2.

Process parameters

Negative values are considered as absolute values for their limits.

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPE3IS	drain-source breakdown @ VG=0V, Id=-1µA, L=0.3µm	5	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXPE3I	mobility exponent	-	-	-1.1	-	-	-
FC_PE3I	corner frequency @ VD=3.3V, Id=1µA, L=10µm, W=10µm	-	-	0.22	-	-	kHz
GAMPE3I	body factor long channel @ L=10µm, W=10µm	-	-	0.86	-	-	√V
IDSPE3IS	saturation current @ VG=-3.3V, VD=-3.3V, L=0.3µm, W=10µm	230	268	305	343	380	µA/µm
IOFPE3IS	off-state leakage @ VD=-3.3V, L=0.3µm, W=10µm	-	-	-	3	-	pA/µm
ISBPE3IS	bulk current @ VD=-3.3V, L=0.3µm	-	-	0.1	-	-	µA/µm
KP_PE3I	gain factor long channel @ L=10µm, W=10µm	-	-	42	-	-	µA/V²
LEFPE3I	effective channel length @ L=0.3µm	-	-	0.25	-	-	µm
NOIPE3I	Input referred noise @ VD=-3.3V, Id=-1µA, f=1Hz, L=10µm, W=10µm	-	-	12.1	-	-	µV.µm/√(Hz)
STSPE3I	subthreshold slope @ VD=-3.3V	-	-	11	-	-	decade/V
TC_VTXPE3I	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	1	-	-	mV/K
U0_PE3I	effective mobility	-	-	77	-	-	cm²/Vs
VTIPE3IL	threshold voltage long channel @ VD=-0.1V, L=10µm, W=10µm	-0.6	-0.63	-0.66	-0.69	-0.72	V
VTIPE3IS	threshold voltage short channel @ VD=-0.1V, L=0.3µm, W=10µm	-0.55	-0.59	-0.63	-0.67	-0.71	V
VTIPE3ISS	threshold voltage small channel @ VD=-0.1V, L=0.3µm, W=0.22µm	-	-	-0.6	-	-	V
VTXPE3IS	extrapolated threshold voltage short channel @ VD=-0.1V, L=0.3µm, W=10µm	-	-	-0.58	-	-	V
WEFPE3I	effective channel width @ W=0.22µm	-	-	0.22	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTPE3I	Pelgrom coefficient gain factor mismatch	0.94	%µm
AIDPE3I00	Pelgrom coefficient ID mismatch @ VG-VT=0V	9.22	%µm
AIDPE3I02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	3.91	%µm
AIDPE3I04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	2.28	%µm
AIDPE3I06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	1.6	%µm
AIDPE3I10	Pelgrom coefficient ID mismatch @ VG-VT=1V	1.03	%µm
AIDPE3I15	Pelgrom coefficient ID mismatch @ VG-VT=1.5V	0.77	%µm
AIDPE3I20	Pelgrom coefficient ID mismatch @ VG-VT=2V	0.65	%µm
AIDPE3I30	Pelgrom coefficient ID mismatch @ VG-VT=3V	0.53	%µm
AVTPE3I	Pelgrom coefficient VT mismatch	5.47	mVµm
DLTPE3I	transistor delta length	0.05	µm
DWTPE3I	transistor delta width	0	µm

pe3i_m_5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-4	-3.6	3.6	4	V
VGD	-40°C to 175°C	-4	-3.6	3.6	4	V
VDS	-40°C to 175°C	-4	-3.6	3.6	4	V
VDB	-40°C to 175°C	-4	-3.6	0	0.5	V
VSB	-40°C to 175°C	-4	-3.6	0	0.5	V
VBpsub	-40°C to 175°C	-0.5	0	10	12	V

Note: The node B (BULK) is: NWELL2.

Process parameters

Negative values are considered as absolute values for their limits.

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPE3IS	drain-source breakdown @ VG=0V, Id=-1µA, L=0.3µm	5	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXPE3I	mobility exponent	-	-	-1.1	-	-	-
FC_PE3I	corner frequency @ VD=3.3V, Id=1µA, L=10µm, W=10µm	-	-	0.22	-	-	kHz
GAMPE3I	body factor long channel @ L=10µm, W=10µm	-	-	0.86	-	-	√V
IDSPE3IS	saturation current @ VG=-3.3V, VD=-3.3V, L=0.3µm, W=10µm	230	268	305	343	380	µA/µm
IOFPE3IS	off-state leakage @ VD=-3.3V, L=0.3µm, W=10µm	-	-	-	3	-	pA/µm
ISBPE3IS	bulk current @ VD=-3.3V, L=0.3µm	-	-	0.1	-	-	µA/µm
KP_PE3I	gain factor long channel @ L=10µm, W=10µm	-	-	42	-	-	µA/V²
LEFPE3I	effective channel length @ L=0.3µm	-	-	0.25	-	-	µm

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Name	Description	LSL	Low	Typ	High	USL	Unit
NOIPE3I	Input referred noise @ VD=-3.3V, Id=-1µA, f=1Hz, L=10µm, W=10µm	-	-	12.1	-	-	µV.µm/√(Hz)
STSPE3I	subthreshold slope @ VD=-3.3V	-	-	11	-	-	decade/V
TC_VTXPE3I	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	1	-	-	mV/K
U0_PE3I	effective mobility	-	-	77	-	-	cm²/Vs
VTIPE3IL	threshold voltage long channel @ VD=-0.1V, L=10µm, W=10µm	-0.6	-0.63	-0.66	-0.69	-0.72	V
VTIPE3IS	threshold voltage short channel @ VD=-0.1V, L=0.3µm, W=10µm	-0.55	-0.59	-0.63	-0.67	-0.71	V
VTIPE3ISS	threshold voltage small channel @ VD=-0.1V, L=0.3µm, W=0.22µm	-	-	-0.6	-	-	V
VTXPE3IS	extrapolated threshold voltage short channel @ VD=-0.1V, L=0.3µm, W=10µm	-	-	-0.58	-	-	V
WEFPE3I	effective channel width @ W=0.22µm	-	-	0.22	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTPE3I	Pelgrom coefficient gain factor mismatch	0.94	%µm
AIDPE3I00	Pelgrom coefficient ID mismatch @ VG-VT=0V	9.22	%µm
AIDPE3I02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	3.91	%µm
AIDPE3I04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	2.28	%µm
AIDPE3I06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	1.6	%µm
AIDPE3I10	Pelgrom coefficient ID mismatch @ VG-VT=1V	1.03	%µm
AIDPE3I15	Pelgrom coefficient ID mismatch @ VG-VT=1.5V	0.77	%µm
AIDPE3I20	Pelgrom coefficient ID mismatch @ VG-VT=2V	0.65	%µm
AIDPE3I30	Pelgrom coefficient ID mismatch @ VG-VT=3V	0.53	%µm
AVTPE3I	Pelgrom coefficient VT mismatch	5.47	mVµm
DLTPE3I	transistor delta length	0.05	µm
DWTPE3I	transistor delta width	0	µm

qnvc

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VCE	-40°C to 175°C	-4	-3.6	3.6	4	V
VEB	-40°C to 175°C	-	-1.5	2.5	3	V
VBC	-40°C to 175°C	-4	-3.6	1.5	-	V
VCS	-40°C to 175°C	-0.5	0	15	17	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BA_NVC	active breakdown voltage @ Ib=500nA	-	-	12	-	-	V

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Name	Description	LSL	Low	Typ	High	USL	Unit
BCEONVC	collector- emitter breakdown voltage (base open) @ Ic=1µA	10	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
EVFNVC	early voltage @ Ib=2µA	-	50	79	-	-	V
HFHNVC	high current beta @ VC=2V, Ib=200µA	-	-	9.5	-	-	-
HFMNVC	current gain @ Ib=0.1µA	12	15.3	18.5	-	-	-
IEBNVC	emitter- base leakage current @ VE=2V	-	-	-	0.1	-	nA/µm
TC_VBENVC	base- emitter voltage temperature coefficient	-	-	-1.7	-	-	mV/K
VBENVC	base- emitter voltage @ VC=2V, Ib=0.1µA	685	690	695	700	705	mV

Note: The parameters are specified for the drawn emitter length of 3 µm.

Matching parameters

Name	Description	Typ	Unit
SIBNVC101	standard deviation IB mismatch @ Ic=100nA, LE=10µm	1.07	%
SIBNVC102	standard deviation IB mismatch @ Ic=100µA, LE=10µm	0.54	%
SIBNVC31	standard deviation IB mismatch @ Ic=100nA, LE=3µm	1.44	%
SIBNVC32	standard deviation IB mismatch @ Ic=100µA, LE=3µm	1	%
SIBNVC501	standard deviation IB mismatch @ Ic=100nA, LE=50µm	0.89	%
SIBNVC502	standard deviation IB mismatch @ Ic=100µA, LE=50µm	0.28	%
SICNVC101	standard deviation IC mismatch @ Ic=100nA, LE=10µm	0.51	%
SICNVC102	standard deviation IC mismatch @ Ic=100µA, LE=10µm	0.18	%
SICNVC31	standard deviation IC mismatch @ Ic=100nA, LE=3µm	0.6	%
SICNVC32	standard deviation IC mismatch @ Ic=100µA, LE=3µm	0.28	%
SICNVC501	standard deviation IC mismatch @ Ic=100nA, LE=50µm	0.38	%
SICNVC502	standard deviation IC mismatch @ Ic=100µA, LE=50µm	0.15	%
SVBNVC101	standard deviation VBE mismatch @ Ic=100nA, LE=10µm	0.06	mV
SVBNVC102	standard deviation VBE mismatch @ Ic=100µA, LE=10µm	0.27	mV
SVBNVC31	standard deviation VBE mismatch @ Ic=100nA, LE=3µm	0.09	mV
SVBNVC32	standard deviation VBE mismatch @ Ic=100µA, LE=3µm	0.3	mV
SVBNVC501	standard deviation VBE mismatch @ Ic=100nA, LE=50µm	0.05	mV
SVBNVC502	standard deviation VBE mismatch @ Ic=100µA, LE=50µm	0.3	mV

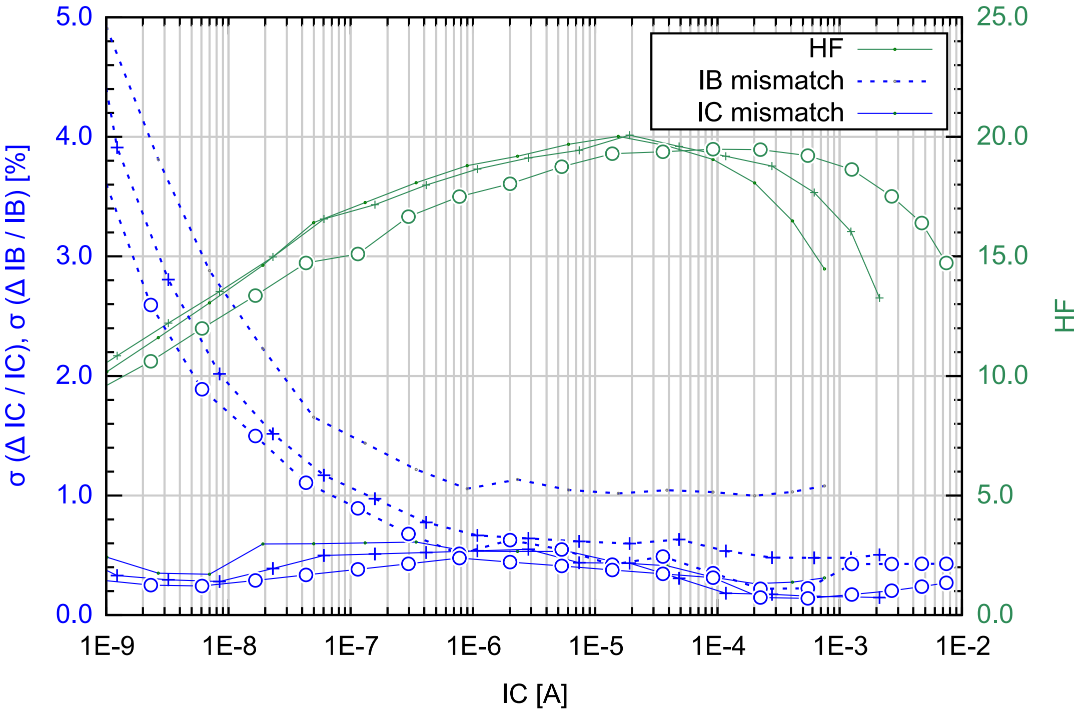

Figure 3.32 Device qnvc: IC matching and IB matching vs. IC (typical values) ----- LE=3µm, --+-- LE=10µm, --o-- LE=50µm

rdnwmv

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-0.5	0	5.5	7	V

Note: The node B (BULK) is PSUB

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSSNWDMV	DNWELLMV sheet resistance (STI terminated) @ Vterm=3.3V, W=10µm	1.2	1.35	1.5	1.65	1.8	kΩ/□
TC1NWDMV	DNWELLMV temperature coefficient 1	-	5.2	5.6	6	-	1e-03/K
TC2NWDMV	DNWELLMV temperature coefficient 2	-	12	15	18	-	1e-06/K²
WERNWDMV	DNWELLMV effective width @ W=2µm	-	1.6	1.75	1.9	-	µm

Matching parameters

Name	Description	Typ	Unit
AR_NWDMV	Pelgrom coefficient resistor mismatch	4.96	%µm
DWRNWDMV	resistor delta width	0.25	µm

mosvc3i_m

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGB	-40°C to 175°C	-4	-3.6	1.98	2.3	V
VIB	-40°C to 175°C	-0.5	0	5.5	7	V
VIpsub	-40°C to 175°C	-0.5	0	10	12	V

Process parameters

Name	Description	Typ	Unit
CNV_MVC3I_M	varactor capacitance at negative voltage @ Vterm=-3.3V, f=100kHz	5	fF/µm²
CPV_MVC3I_M	varactor capacitance at positive voltage @ Vterm=1.8V, f=100kHz	1.6	fF/µm²
TUR_MVC3I_M	tuning range @ Vlow=-3.3V, Vhigh=1.8V, f=100kHz	70	%

mosvci_m

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGB	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VIB	-40°C to 175°C	-0.5	0	5.5	7	V
VIpsub	-40°C to 175°C	-0.5	0	10	12	V

Process parameters

Name	Description	Typ	Unit
CNV_MVCI_M	varactor capacitance at negative voltage @ Vterm=-1.8V, f=100kHz	8.1	fF/µm²
CPV_MVCI_M	varactor capacitance at positive voltage @ Vterm=1.8V, f=100kHz	2	fF/µm²
TUR_MVCI_M	tuning range @ Vlow=-1.8V, Vhigh=1.8V, f=100kHz	75	%

ddnwmv

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-12	-10	0	0.5	V

Note: The Junction diodes must not be used in forward operation for normal operation mode.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVJNWDMV	breakdown voltage DNWELLMV / PSUB @ Irev=1µA	15	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CJANWDMV	area junction capacitance	-	-	0.07	-	-	fF/µm²
CJPNWDMV	sidewall junction capacitance	-	-	0.59	-	-	fF/µm
ILANWDMV	area leakage current @ Vrev=10V, T=27°C	-	-	0.0001	-	-	fA/µm²
ILANWDMVHT	area leakage current @ Vrev=10V, T=175°C	-	-	1.09	-	-	pA/µm²

⇒

Name	Description	LSL	Low	Typ	High	USL	Unit
ILPNWDMV	sidewall leakage current @ Vrev=10V, T=27°C	-	-	0.442	-	-	fA/µm
ILPNWDMVHT	sidewall leakage current @ Vrev=10V, T=175°C	-	-	3.81	-	-	pA/µm
MJANWDMV	area grading coefficient	-	-	0.29	-	-	-
MJPNWDMV	sidewall grading coefficient	-	-	0.36	-	-	-
PBANWDMV	area junction potential	-	-	0.46	-	-	V
PBPNWDMV	sidewall junction potential	-	-	0.54	-	-	V

Note: ddnwmv is also used as parasitic diode p_ddnwmv.

dpdnwmv

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode[(1]	-40°C to 175°C	-7	-5.5	0	0.5	V

Note 1 Isolated from P-substrate by ddnwmv.

Note: The Junction diodes must not be used in forward operation for normal operation mode.

Note: For diodes which are isolated from the P-substrate, please also refer to the operating conditions for the isolating diode.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVJPDNWMV	breakdown voltage PDIFF / DNWELLMV @ Irev=-1µA	10	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CJAPDNWMV	area junction capacitance	-	-	0.56	-	-	fF/µm²
CJPPDNWMV	sidewall junction capacitance	-	-	0.09	-	-	fF/µm
ILAPDNWMV	area leakage current @ Vrev=-5.5V, T=27°C	-	-	0.01	-	-	fA/µm²
ILAPDNWMVHT	area leakage current @ Vrev=-5.5V, T=175°C	-	-	0.38	-	-	pA/µm²
ILPPDNWMV	sidewall leakage current @ Vrev=-5.5V, T=27°C	-	-	0.521	-	-	fA/µm
ILPPDNWMVHT	sidewall leakage current @ Vrev=-5.5V, T=175°C	-	-	1.2	-	-	pA/µm
MJAPDNWMV	area grading coefficient	-	-	0.37	-	-	-
MJPPDNWMV	sidewall grading coefficient	-	-	0.05	-	-	-
PBAPDNWMV	area junction potential	-	-	0.6	-	-	V
PBPPDNWMV	sidewall junction potential	-	-	1.2	-	-	V

Note: dpdnwmv is also used as parasitic diode p_dpdnwmv.

dipdnwmv

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode[(1]	-40°C to 175°C	-10	-8	0	0.5	V

Note 1 For device dipdnwmv. Isolated from P-substrate by ddnwmv.

3. Parameters → 3.10 ISOMOS module→ 3.10.2 Device parameters→ dipdnwmv→ Operating conditions

Note: The Junction diodes must not be used in forward operation for normal operation mode.

Note: For diodes which are isolated from the P-substrate, please also refer to the operating conditions for the isolating diode.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVJP1NWDMV	breakdown voltage PWELL1 / DNWELLMV @ Irev=-1µA	15	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BVJP2NWDMV	breakdown voltage PWELL2 / DNWELLMV @ Irev=-1µA	15	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CJAPINWDMV	area junction capacitance	-	-	0.34	-	-	fF/µm²
CJPPINWDMV	sidewall junction capacitance	-	-	0.3	-	-	fF/µm
ILAPINWDMV	area leakage current @ Vrev=-8V, T=27°C	-	-	0.003	-	-	fA/µm²
ILAPINWDMVHT	area leakage current @ Vrev=-8V, T=175°C	-	-	0.34	-	-	pA/µm²
ILPPINWDMV	sidewall leakage current @ Vrev=-8V, T=27°C	-	-	0.122	-	-	fA/µm
ILPPINWDMVHT	sidewall leakage current @ Vrev=-8V, T=175°C	-	-	0.42	-	-	pA/µm
MJAPINWDMV	area grading coefficient	-	-	0.51	-	-	-
MJPPINWDMV	sidewall grading coefficient	-	-	0.27	-	-	-
PBAPINWDMV	area junction potential	-	-	0.68	-	-	V
PBPPINWDMV	sidewall junction potential	-	-	0.57	-	-	V

Note: dipdnwmv is also used as parasitic diode p_dipdnwmv.

3.11 ISOMOS2 module

3.11.1 Device independent parameters

Structural and geometrical parameters

Name	Description	Typ	Unit
XJ_DNW	DNWELLMV/DNWELL junction depth	2.8	µm
XJ_HPWDNW	HVPWELL in DNWELL junction depth	1.3	µm
XJ_NHPW	N+ source/ drain junction depth in HVPWELL	0.2	µm
XJ_PW1DNW	PWELL1 in DNWELLMV/DNWELL junction depth	1	µm
	Note: This parameter is only available if the HVMOS and ISOMOS modules are selected.		
XJ_PW2DNW	PWELL2 in DNWELLMV/DNWELL junction depth	1	µm
	Note: This parameter is only available if the HVMOS and ISOMOS modules are selected.		

Sheet and contact resistance parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSSNWD	DNWELL sheet resistance (STI terminated) @ W=10µm	1.2	1.35	1.5	1.65	1.8	kΩ/☐
RSSPW1DNW	PWELL1 in DNWELLMV/DNWELL sheet resistance, (STI terminated) @ W=20µm	2.4	2.65	2.9	3.15	3.4	kΩ/☐
	Note: This parameter is only available if the HVMOS and ISOMOS modules are selected.						
RSSPW2DNW	PWELL2 in DNWELLMV/DNWELL sheet resistance, (STI terminated) @ W=20µm	2.5	2.75	3	3.25	3.5	kΩ/☐
	Note: This parameter is only available if the HVMOS and ISOMOS modules are selected.						

3.11.2 Device parameters

nei_6

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VGD	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDB	-40°C to 175°C	-0.5	0	1.98	2.3	V
VSB	-40°C to 175°C	-0.5	0	1.98	2.3	V
VIpsub	-40°C to 175°C	-0.5	0	45	50	V
VIB	-40°C to 175°C	-0.5	0	8	10	V

Note: The node B (BULK) is: PWELL1.

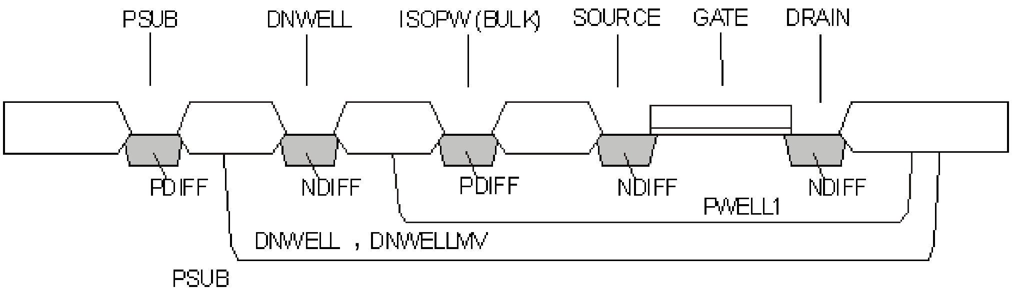

Figure 3.33 Additional Operating Conditions

Note: nei_6 in DNWELL

$$
\begin{array}{lcccl}
V_{PSUB} & \leq & V_{DNWELL} & \leq & V_{PSUB}+45(50)V \\
V_{DNWELL}-8(10)V & \leq & V_{PWELL1} & \leq & V_{DNWELL}
\end{array}
$$

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNEIS	drain-source breakdown @ VG=0V, Id=1µA, L=0.18µm	3.6	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXNEI	mobility exponent	-	-	-1.7	-	-	-
FC_NEI	corner frequency @ VD=1.8V, Id=1µA, L=10µm, W=10µm	-	-	1.21	-	-	kHz
GAMNEI	body factor long channel @ L=10µm, W=10µm	-	-	0.7	-	-	√V
IDSNEIS	saturation current @ VG=1.8V, VD=1.8V, L=0.18µm, W=10µm	340	407	475	543	610	µA/µm
IOFNEIS	off-state leakage @ VD=1.8V, L=0.18µm, W=10µm	-	-	-	3	-	pA/µm
ISBNEIS	bulk current @ VD=1.8V, L=0.18µm	-	-	0.05	-	-	µA/µm
KP_NEI	gain factor long channel @ L=10µm, W=10µm	-	-	243	-	-	µA/V²
LEFNEI	effective channel length @ L=0.18µm	-	-	0.16	-	-	µm
NOINEI	Input referred noise @ VD=1.8V, Id=1µA, f=1Hz, L=10µm, W=10µm	-	-	11.2	-	-	µV.µm/ √(Hz)
STSNEI	subthreshold slope @ VD=1.8V	-	-	12	-	-	decade/V
TC_VTXNEI	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	-0.89	-	-	mV/K
U0_NEI	effective mobility	-	-	307	-	-	cm²/Vs
VTINEIL	threshold voltage long channel @ VD=0.1V, L=10µm, W=10µm	0.47	0.5	0.53	0.56	0.59	V
VTINEIS	threshold voltage short channel @ VD=0.1V, L=0.18µm, W=10µm	0.46	0.52	0.58	0.64	0.7	V
VTINEISS	threshold voltage small channel @ VD=0.1V, L=0.18µm, W=0.22µm	-	-	0.45	-	-	V

⇒

Name	Description	LSL	Low	Typ	High	USL	Unit
VTXNEIS	extrapolated threshold voltage short channel @ VD=0.1V, L=0.18µm, W=10µm	-	-	0.65	-	-	V
WEFNEI	effective channel width @ W=0.22µm	-	-	0.17	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTNEI	Pelgrom coefficient gain factor mismatch	0.63	%µm
AIDNEI00	Pelgrom coefficient ID mismatch @ VG-VT=0V	7.43	%µm
AIDNEI01	Pelgrom coefficient ID mismatch @ VG-VT=0.1V	5.03	%µm
AIDNEI02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	3.55	%µm
AIDNEI04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	2.05	%µm
AIDNEI06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	1.4	%µm
AIDNEI08	Pelgrom coefficient ID mismatch @ VG-VT=0.8V	1.05	%µm
AIDNEI10	Pelgrom coefficient ID mismatch @ VG-VT=1V	0.86	%µm
AIDNEI14	Pelgrom coefficient ID mismatch @ VG-VT=1.4V	0.64	%µm
AVTNEI	Pelgrom coefficient VT mismatch	5.1	mVµm
DLTNEI	transistor delta length	0.02	µm
DWTNEI	transistor delta width	0.05	µm

pei_5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VGD	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDB	-40°C to 175°C	-2.3	-1.98	0	0.5	V
VSB	-40°C to 175°C	-2.3	-1.98	0	0.5	V
VBpsub	-40°C to 175°C	-0.5	0	45	50	V

Note: The node B (BULK) is: NWELL1.

Process parameters

Negative values are considered as absolute values for their limits.

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPEIS	drain-source breakdown @ VG=0V, Id=-1µA, L=0.18µm	3.6	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXPEI	mobility exponent	-	-	-1	-	-	-
FC_PEI	corner frequency @ VD=1.8V, Id=1µA, L=10µm, W=10µm	-	-	0.3	-	-	kHz
GAMPEI	body factor long channel @ L=10µm, W=10µm	-	-	0.86	-	-	√V
IDSPEIS	saturation current @ VG=-1.8V, VD=-1.8V, L=0.18µm, W=10µm	110	140	170	200	230	µA/µm
IOFPEIS	off-state leakage @ VD=-1.8V, L=0.18µm, W=10µm	-	-	-	3	-	pA/µm

⇒

Name	Description	LSL	Low	Typ	High	USL	Unit
ISBPEIS	bulk current @ VD=-1.8V, L=0.18µm	-	-	0.1	-	-	nA/µm
KP_PEI	gain factor long channel @ L=10µm, W=10µm	-	-	52	-	-	µA/V²
LEFPEI	effective channel length @ L=0.18µm	-	-	0.15	-	-	µm
NOIPEI	Input referred noise @ VD=-1.8V, Id=-1µA, f=1Hz, L=10µm, W=10µm	-	-	17	-	-	µV.µm/√(Hz)
STSPEI	subthreshold slope @ VD=-1.8V	-	-	11	-	-	decade/V
TC_VTXPEI	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	0.91	-	-	mV/K
U0_PEI	effective mobility	-	-	59	-	-	cm²/Vs
VTIPEIL	threshold voltage long channel @ VD=-0.1V, L=10µm, W=10µm	-0.64	-0.67	-0.7	-0.73	-0.76	V
VTIPEIS	threshold voltage short channel @ VD=-0.1V, L=0.18µm, W=10µm	-0.55	-0.6	-0.65	-0.7	-0.75	V
VTIPEISS	threshold voltage small channel @ VD=-0.1V, L=0.18µm, W=0.22µm	-	-	-0.6	-	-	V
VTXPEIS	extrapolated threshold voltage short channel @ VD=-0.1V, L=0.18µm, W=10µm	-	-	-0.65	-	-	V
WEFPEI	effective channel width @ W=0.22µm	-	-	0.25	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTPEI	Pelgrom coefficient gain factor mismatch	1.01	%µm
AIDPEI00	Pelgrom coefficient ID mismatch @ VG-VT=0V	7.79	%µm
AIDPEI01	Pelgrom coefficient ID mismatch @ VG-VT=0.1V	5.14	%µm
AIDPEI02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	3.56	%µm
AIDPEI04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	2.11	%µm
AIDPEI06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	1.52	%µm
AIDPEI08	Pelgrom coefficient ID mismatch @ VG-VT=0.8V	1.21	%µm
AIDPEI10	Pelgrom coefficient ID mismatch @ VG-VT=1V	1.03	%µm
AIDPEI14	Pelgrom coefficient ID mismatch @ VG-VT=1.4V	0.81	%µm
AVTPEI	Pelgrom coefficient VT mismatch	5.09	mVµm
DLTPEI	transistor delta length	0.03	µm
DWTPEI	transistor delta width	-0.03	µm

ne3i_6

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-4	-3.6	3.6	4	V
VGD	-40°C to 175°C	-4	-3.6	3.6	4	V
VDS	-40°C to 175°C	-4	-3.6	3.6	4	V
VDB	-40°C to 175°C	-0.5	0	3.6	4	V
VSB	-40°C to 175°C	-0.5	0	3.6	4	V
VIB	-40°C to 175°C	-0.5	0	8	10	V
VIpsub	-40°C to 175°C	-0.5	0	45	50	V

Note: The node B (BULK) is: PWELL2

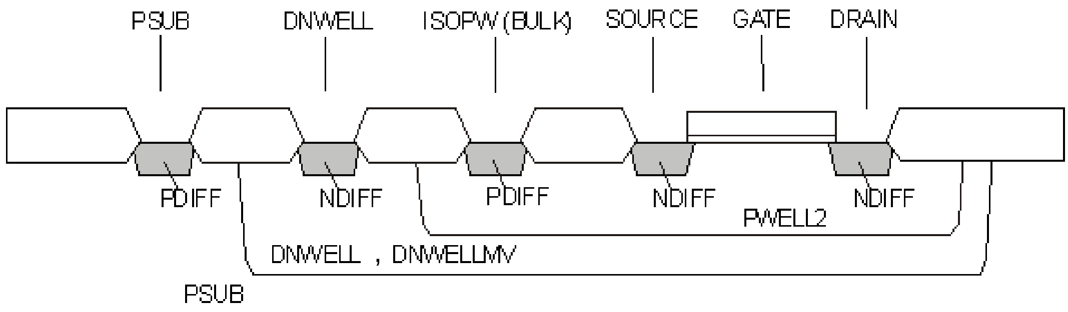

Figure 3.34 Additional Operating Conditions

Note: ne3i_6 in DNWELL

$$\begin{array}{lclcl} V_{PSUB} & \leq & V_{DNWELL} & \leq & V_{PSUB} + 45(50)V \\ V_{DNWELL} - 8(10)V & \leq & V_{PWELL2} & \leq & V_{DNWELL} \end{array}$$

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNE3IS	drain-source breakdown @ VG=0V, Id=1µA, L=0.35µm	5	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXNE3I	mobility exponent	-	-	-1.7	-	-	-
FC_NE3I	corner frequency @ VD=3.3V, Id=1µA, L=10µm, W=10µm	-	-	1.89	-	-	kHz
GAMNE3I	body factor long channel @ L=10µm, W=10µm	-	-	0.92	-	-	√V
IDSNE3IS	saturation current @ VG=3.3V, VD=3.3V, L=0.35µm, W=10µm	525	570	615	660	705	µA/µm
IOFNE3IS	off-state leakage @ VD=3.3V, L=0.35µm, W=10µm	-	-	-	3	-	pA/µm
ISBNE3IS	bulk current @ VD=3.3V, L=0.35µm	-	-	1	-	-	µA/µm
KP_NE3I	gain factor long channel @ L=10µm, W=10µm	-	-	190	-	-	µA/V²
LEFNE3I	effective channel length @ L=0.35µm	-	-	0.33	-	-	µm
NOINE3I	Input referred noise @ VD=3.3V, Id=1µA, f=1Hz, L=10µm, W=10µm	-	-	19.2	-	-	µV.µm/ √(Hz)
STSNE3I	subthreshold slope @ VD=3.3V	-	-	11	-	-	decade/V
TC_VTXNE3I	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	-1	-	-	mV/K
U0_NE3I	effective mobility	-	-	360	-	-	cm²/Vs
VTINE3IL	threshold voltage long channel @ VD=0.1V, L=10µm, W=10µm	0.6	0.63	0.66	0.69	0.72	V
VTINE3IS	threshold voltage short channel @ VD=0.1V, L=0.35µm, W=10µm	0.585	0.625	0.665	0.705	0.745	V
VTINE3ISS	threshold voltage small channel @ VD=0.1V, L=0.35µm, W=0.22µm	-	-	0.53	-	-	V

⇒

Name	Description	LSL	Low	Typ	High	USL	Unit
VTXNE3IS	extrapolated threshold voltage short channel @ VD=0.1V, L=0.35µm, W=10µm	-	-	0.72	-	-	V
WEFNE3I	effective channel width @ W=0.22µm	-	-	0.18	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTNE3I	Pelgrom coefficient gain factor mismatch	0.98	%µm
AIDNE3I00	Pelgrom coefficient ID mismatch @ VG-VT=0V	13.2	%µm
AIDNE3I02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	6.49	%µm
AIDNE3I04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	3.71	%µm
AIDNE3I06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	2.48	%µm
AIDNE3I10	Pelgrom coefficient ID mismatch @ VG-VT=1V	1.45	%µm
AIDNE3I15	Pelgrom coefficient ID mismatch @ VG-VT=1.5V	0.97	%µm
AIDNE3I20	Pelgrom coefficient ID mismatch @ VG-VT=2V	0.75	%µm
AIDNE3I30	Pelgrom coefficient ID mismatch @ VG-VT=3V	0.55	%µm
AVTNE3I	Pelgrom coefficient VT mismatch	9.24	mVµm
DLTNE3I	transistor delta length	0.02	µm
DWTNE3I	transistor delta width	0.04	µm

pe3i_5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-4	-3.6	3.6	4	V
VGD	-40°C to 175°C	-4	-3.6	3.6	4	V
VDS	-40°C to 175°C	-4	-3.6	3.6	4	V
VDB	-40°C to 175°C	-4	-3.6	0	0.5	V
VSB	-40°C to 175°C	-4	-3.6	0	0.5	V
VBpsub	-40°C to 175°C	-0.5	0	45	50	V

Note: The node B (BULK) is: NWELL2.

Process parameters

Negative values are considered as absolute values for their limits.

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPE3IS	drain-source breakdown @ VG=0V, Id=-1µA, L=0.3µm	5	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXPE3I	mobility exponent	-	-	-1.1	-	-	-
FC_PE3I	corner frequency @ VD=3.3V, Id=1µA, L=10µm, W=10µm	-	-	0.22	-	-	kHz
GAMPE3I	body factor long channel @ L=10µm, W=10µm	-	-	0.86	-	-	√V
IDSPE3IS	saturation current @ VG=-3.3V, VD=-3.3V, L=0.3µm, W=10µm	230	268	305	343	380	µA/µm
IOFPE3IS	off-state leakage @ VD=-3.3V, L=0.3µm, W=10µm	-	-	-	3	-	pA/µm

⇒

Name	Description	LSL	Low	Typ	High	USL	Unit
ISBPE3IS	bulk current @ VD=-3.3V, L=0.3µm	-	-	0.1	-	-	µA/µm
KP_PE3I	gain factor long channel @ L=10µm, W=10µm	-	-	42	-	-	$\mu A/V^2$
LEFPE3I	effective channel length @ L=0.3µm	-	-	0.25	-	-	µm
NOIPE3I	Input referred noise @ VD=-3.3V, Id=-1µA, f=1Hz, L=10µm, W=10µm	-	-	12.1	-	-	µV.µm/√(Hz)
STSPE3I	subthreshold slope @ VD=-3.3V	-	-	11	-	-	decade/V
TC_VTXPE3I	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	1	-	-	mV/K
U0_PE3I	effective mobility	-	-	77	-	-	cm^2/Vs
VTIPE3IL	threshold voltage long channel @ VD=-0.1V, L=10µm, W=10µm	-0.6	-0.63	-0.66	-0.69	-0.72	V
VTIPE3IS	threshold voltage short channel @ VD=-0.1V, L=0.3µm, W=10µm	-0.55	-0.59	-0.63	-0.67	-0.71	V
VTIPE3ISS	threshold voltage small channel @ VD=-0.1V, L=0.3µm, W=0.22µm	-	-	-0.6	-	-	V
VTXPE3IS	extrapolated threshold voltage short channel @ VD=-0.1V, L=0.3µm, W=10µm	-	-	-0.58	-	-	V
WEFPE3I	effective channel width @ W=0.22µm	-	-	0.22	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTPE3I	Pelgrom coefficient gain factor mismatch	0.94	%µm
AIDPE3I00	Pelgrom coefficient ID mismatch @ VG-VT=0V	9.22	%µm
AIDPE3I02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	3.91	%µm
AIDPE3I04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	2.28	%µm
AIDPE3I06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	1.6	%µm
AIDPE3I10	Pelgrom coefficient ID mismatch @ VG-VT=1V	1.03	%µm
AIDPE3I15	Pelgrom coefficient ID mismatch @ VG-VT=1.5V	0.77	%µm
AIDPE3I20	Pelgrom coefficient ID mismatch @ VG-VT=2V	0.65	%µm
AIDPE3I30	Pelgrom coefficient ID mismatch @ VG-VT=3V	0.53	%µm
AVTPE3I	Pelgrom coefficient VT mismatch	5.47	mVµm
DLTPE3I	transistor delta length	0.05	µm
DWTPE3I	transistor delta width	0	µm

mosvc3i

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGB	-40°C to 175°C	-4	-3.6	1.98	2.3	V
VIB	-40°C to 175°C	-0.5	0	5.5	7	V
VIpsub	-40°C to 175°C	-0.5	0	45	50	V

Process parameters

Name	Description	Typ	Unit
CNV_MVC3I	varactor capacitance at negative voltage @ Vterm=-3.3V, f=100kHz	5	$fF/\mu m^2$

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Name	Description	Typ	Unit
CPV_MVC3I	varactor capacitance at positive voltage @ Vterm=1.8V, f=100kHz	1.6	fF/µm²
TUR_MVC3I	tuning range @ Vlow=-3.3V, Vhigh=1.8V, f=100kHz	70	%

mosvci

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGB	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VIB	-40°C to 175°C	-0.5	0	5.5	7	V
VIpsub	-40°C to 175°C	-0.5	0	45	50	V

Process parameters

Name	Description	Typ	Unit
CNV_MVCI	varactor capacitance at negative voltage @ Vterm=-1.8V, f=100kHz	8.1	fF/µm²
CPV_MVCI	varactor capacitance at positive voltage @ Vterm=1.8V, f=100kHz	2	fF/µm²
TUR_MVCI	tuning range @ Vlow=-1.8V, Vhigh=1.8V, f=100kHz	75	%

3.12 HIGHTEMP module

This module must be selected for IC designs operating at junction temperatures above 125°C (operating conditions). The module qualification status for temperature range -40°C…+175°C may differ from that at-40°C…+125°C.

For operating conditions and reliability information, please refer to respective operating conditions section and the Process Reliability Specification for details.

For all process and device parameters, please refer to respective process parameter sections describing the relevant parameters.

3.13 LVT module

3.13.1 Device parameters

nel

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VGD	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDB	-40°C to 175°C	-0.5	0	1.98	2.3	V
VSB	-40°C to 175°C	-0.5	0	1.98	2.3	V

Note: The node B (BULK) is: PWELL3.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNELS	drain-source breakdown @ VG=0V, Id=1µA, L=0.18µm	3.6	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXNEL	mobility exponent	-	-	-1.8	-	-	-
FC_NEL	corner frequency @ VD=1.8V, Id=1µA, L=10µm, W=10µm	-	-	0.43	-	-	kHz
GAMNEL	body factor long channel @ L=10µm, W=10µm	-	-	0.56	-	-	√V
IDSNELS	saturation current @ VG=1.8V, VD=1.8V, L=0.18µm, W=10µm	460	535	610	685	760	µA/µm
IOFNELS	off-state leakage @ VD=1.8V, L=0.18µm, W=10µm	-	-	-	5	-	nA/µm
ISBNELS	bulk current @ VD=1.8V, L=0.18µm	-	-	0.1	-	-	µA/µm
KP_NEL	gain factor long channel @ L=10µm, W=10µm	-	-	290	-	-	µA/V²
LEFNEL	effective channel length @ L=0.18µm	-	-	0.17	-	-	µm
NOINEL	Input referred noise @ VD=1.8V, Id=1µA, f=1Hz, L=10µm, W=10µm	-	-	7.3	-	-	µV.µm/ √(Hz)
STSNEL	subthreshold slope @ VD=1.8V	-	-	12	-	-	decade/V
TC_VTXNEL	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	-0.78	-	-	mV/K
U0_NEL	effective mobility	-	-	345	-	-	cm²/Vs
VTINELL	threshold voltage long channel @ VD=0.1V, L=10µm, W=10µm	0.29	0.32	0.35	0.38	0.41	V
VTINELS	threshold voltage short channel @ VD=0.1V, L=0.18µm, W=10µm	0.26	0.305	0.35	0.395	0.44	V
VTINELSS	threshold voltage small channel @ VD=0.1V, L=0.18µm, W=0.22µm	-	-	0.275	-	-	V
VTXNELS	extrapolated threshold voltage short channel @ VD=0.1V, L=0.18µm, W=10µm	-	-	0.41	-	-	V
WEFNEL	effective channel width @ W=0.22µm	-	-	0.2	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTNEL	Pelgrom coefficient gain factor mismatch	0.59	%µm
AIDNEL00	Pelgrom coefficient ID mismatch @ VG-VT=0V	6.72	%µm
AIDNEL01	Pelgrom coefficient ID mismatch @ VG-VT=0.1V	4.31	%µm
AIDNEL02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	2.9	%µm
AIDNEL04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	1.59	%µm
AIDNEL06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	1.07	%µm
AIDNEL08	Pelgrom coefficient ID mismatch @ VG-VT=0.8V	0.82	%µm
AIDNEL10	Pelgrom coefficient ID mismatch @ VG-VT=1V	0.67	%µm
AIDNEL14	Pelgrom coefficient ID mismatch @ VG-VT=1.4V	0.52	%µm
AVTNEL	Pelgrom coefficient VT mismatch	4.05	mVµm
DLTNEL	transistor delta length	0.01	µm
DWTNEL	transistor delta width	0.02	µm

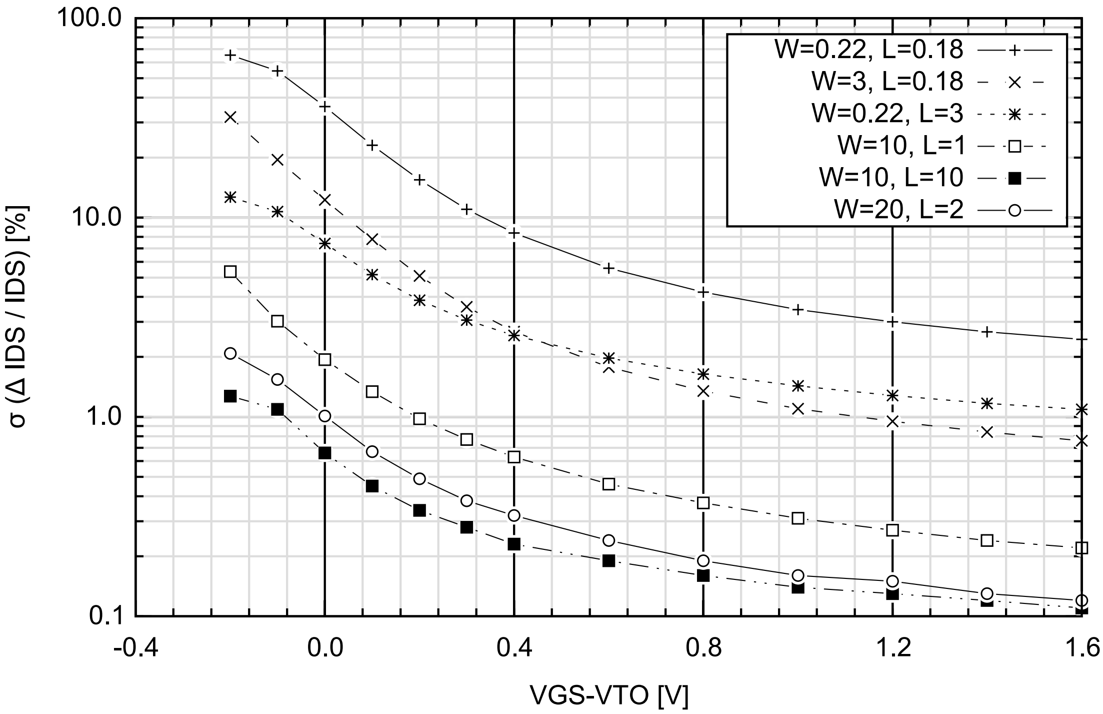

Figure 3.35 Device nel: drain current matching vs. VGS-VTO (typical values, drawn W and L)

pel, pel_5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VGD	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDB	-40°C to 175°C	-2.3	-1.98	0	0.5	V
VSB	-40°C to 175°C	-2.3	-1.98	0	0.5	V
VBpsub	-40°C to 175°C	-0.5	0	1.98	2.3	V

Note: The node B (BULK) is: NWELL3.

Process parameters

Negative values are considered as absolute values for their limits.

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPELS	drain-source breakdown @ VG=0V, Id=-1µA, L=0.18µm	3.6	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXPEL	mobility exponent	-	-	-1.13	-	-	-
FC_PEL	corner frequency @ VD=1.8V, Id=1µA, L=10µm, W=10µm	-	-	0.28	-	-	kHz
GAMPEL	body factor long channel @ L=10µm, W=10µm	-	-	0.44	-	-	√V
IDSPELS	saturation current @ VG=-1.8V, VD=-1.8V, L=0.18µm, W=10µm	200	250	300	350	400	µA/µm
IOFPELS	off-state leakage @ VD=-1.8V, L=0.18µm, W=10µm	-	-	-	10	-	nA/µm
KP_PEL	gain factor long channel @ L=10µm, W=10µm	-	-	65	-	-	$\mu A/V^2$
LEFPEL	effective channel length @ L=0.18µm	-	-	0.15	-	-	µm
NOIPEL	Input referred noise @ VD=-1.8V, Id=-1µA, f=1Hz, L=10µm, W=10µm	-	-	7.8	-	-	µV.µm/ √(Hz)
STSPEL	subthreshold slope @ VD=-1.8V	-	-	11	-	-	decade/V
TC_VTXPEL	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	0.76	-	-	mV/K
U0_PEL	effective mobility	-	-	75	-	-	cm^2/Vs
VTIPELL	threshold voltage long channel @ VD=-0.1V, L=10µm, W=10µm	-0.33	-0.36	-0.39	-0.42	-0.45	V
VTIPELS	threshold voltage short channel @ VD=-0.1V, L=0.18µm, W=10µm	-0.24	-0.3	-0.36	-0.42	-0.48	V
VTIPELSS	threshold voltage small channel @ VD=-0.1V, L=0.18µm, W=0.22µm	-	-	-0.35	-	-	V
VTXPELS	extrapolated threshold voltage short channel @ VD=-0.1V, L=0.18µm, W=10µm	-	-	-0.36	-	-	V
WEFPEL	effective channel width @ W=0.22µm	-	-	0.23	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTPEL	Pelgrom coefficient gain factor mismatch	0.65	%µm
AIDPEL00	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	7.1	%µm
AIDPEL01	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	4.5	%µm
AIDPEL02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	2.88	%µm
AIDPEL04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	1.62	%µm
AIDPEL06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	1.15	%µm
AIDPEL08	Pelgrom coefficient ID mismatch @ VG-VT=0.8V	0.91	%µm
AIDPEL10	Pelgrom coefficient ID mismatch @ VG-VT=1V	0.77	%µm
AIDPEL14	Pelgrom coefficient ID mismatch @ VG-VT=1.4V	0.61	%µm
AVTPEL	Pelgrom coefficient VT mismatch	3.48	mVµm

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Name	Description	Typ	Unit
DLTPEL	transistor delta length	0.03	µm
DWTPEL	transistor delta width	-0.01	µm

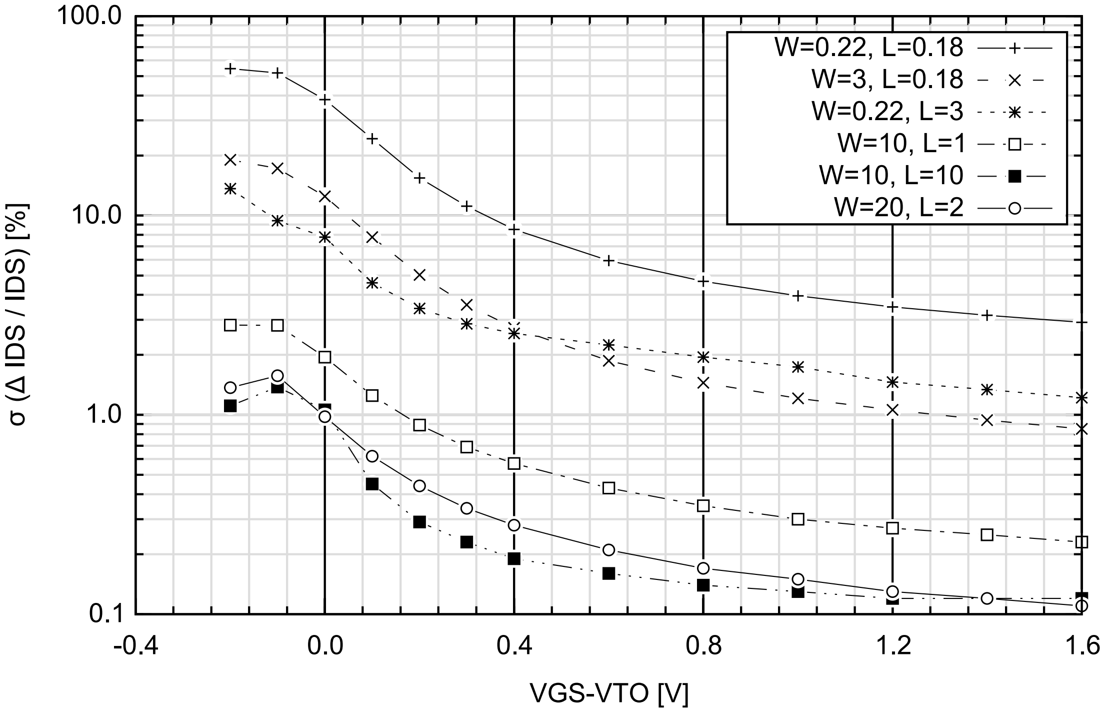

Figure 3.36 Device pel: drain current matching vs. VGS-VTO (typical values, drawn W and L)

neli

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VGD	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDB	-40°C to 175°C	-0.5	0	1.98	2.3	V
VSB	-40°C to 175°C	-0.5	0	1.98	2.3	V

Note: The node B (BULK) is: PWELL3.

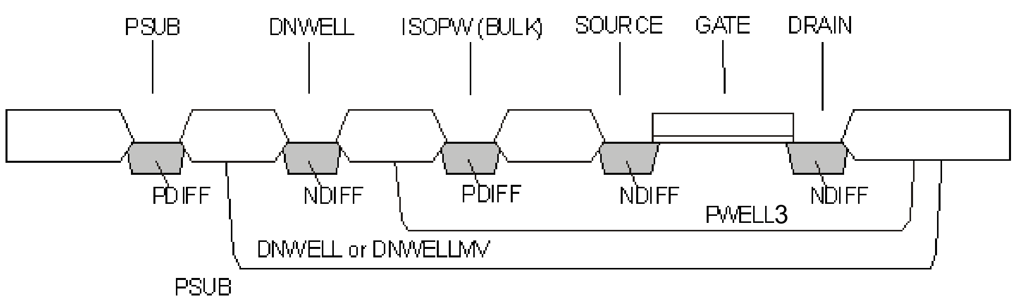

Figure 3.37 Additional Operating Conditions

Note: neli in DNWELL

$$
\begin{array}{lllll}
V_{PSUB} & \leq & V_{DNWELL} & \leq & V_{PSUB} + 45(50)V \\
V_{DNWELL} - 8(10)V & \leq & V_{PWELL3} & \leq & V_{DNWELL}
\end{array}
$$

neli in DNWELLMV

$$
\begin{array}{lllll}
V_{PSUB} & \leq & V_{DNWELL} & \leq & V_{PSUB} + 10(12)V \\
V_{DNWELLMV} - 8(10)V & \leq & V_{PWELL3} & \leq & V_{DNWELLMV}
\end{array}
$$

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNELIS	drain-source breakdown @ VG=0V, Id=1µA, L=0.18µm	3.6	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXNELI	mobility exponent	-	-	-1.8	-	-	-
FC_NELI	corner frequency @ VD=1.8V, Id=1µA, L=10µm, W=10µm	-	-	0.43	-	-	kHz
GAMNELI	body factor long channel @ L=10µm, W=10µm	-	-	0.56	-	-	√V
IDSNELIS	saturation current @ VG=1.8V, VD=1.8V, L=0.18µm, W=10µm	460	535	610	685	760	µA/µm
IOFNELIS	off-state leakage @ VD=1.8V, L=0.18µm, W=10µm	-	-	-	5	-	nA/µm
ISBNELIS	bulk current @ VD=1.8V, L=0.18µm	-	-	0.1	-	-	µA/µm
KP_NELI	gain factor long channel @ L=10µm, W=10µm	-	-	290	-	-	µA/V²
LEFNELI	effective channel length @ L=0.18µm	-	-	0.17	-	-	µm
NOINELI	Input referred noise @ VD=1.8V, Id=1µA, f=1Hz, L=10µm, W=10µm	-	-	7.3	-	-	µV.µm/ √(Hz)
STSNELI	subthreshold slope @ VD=1.8V	-	-	12	-	-	decade/V
TC_VTXNELI	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	-0.78	-	-	mV/K
U0_NELI	effective mobility	-	-	345	-	-	cm²/Vs
VTINELIL	threshold voltage long channel @ VD=0.1V, L=10µm, W=10µm	0.29	0.32	0.35	0.38	0.41	V
VTINELIS	threshold voltage short channel @ VD=0.1V, L=0.18µm, W=10µm	0.26	0.305	0.35	0.395	0.44	V
VTINELISS	threshold voltage small channel @ VD=0.1V, L=0.18µm, W=0.22µm	-	-	0.275	-	-	V
VTXNELIS	extrapolated threshold voltage short channel @ VD=0.1V, L=0.18µm, W=10µm	-	-	0.41	-	-	V
WEFNELI	effective channel width @ W=0.22µm	-	-	0.2	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTNELI	Pelgrom coefficient gain factor mismatch	0.59	%µm
AIDNELI00	Pelgrom coefficient ID mismatch @ VG-VT=0V	6.76	%µm

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Name	Description	Typ	Unit
AIDNELI01	Pelgrom coefficient ID mismatch @ VG-VT=0.1V	4.39	%µm
AIDNELI02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	2.99	%µm
AIDNELI04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	1.65	%µm
AIDNELI06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	1.11	%µm
AIDNELI08	Pelgrom coefficient ID mismatch @ VG-VT=0.8V	0.84	%µm
AIDNELI10	Pelgrom coefficient ID mismatch @ VG-VT=1V	0.69	%µm
AIDNELI14	Pelgrom coefficient ID mismatch @ VG-VT=1.4V	0.53	%µm
AVTNELI	Pelgrom coefficient VT mismatch	4.04	mVµm
DLTNELI	transistor delta length	0.01	µm
DWTNELI	transistor delta width	0.02	µm

neli_6

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VGD	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDB	-40°C to 175°C	-0.5	0	1.98	2.3	V
VSB	-40°C to 175°C	-0.5	0	1.98	2.3	V
VIB	-40°C to 175°C	-0.5	0	8	10	V
VIpsub	-40°C to 175°C	-0.5	0	45	50	V

Note: The node B (BULK) is: PWELL3.

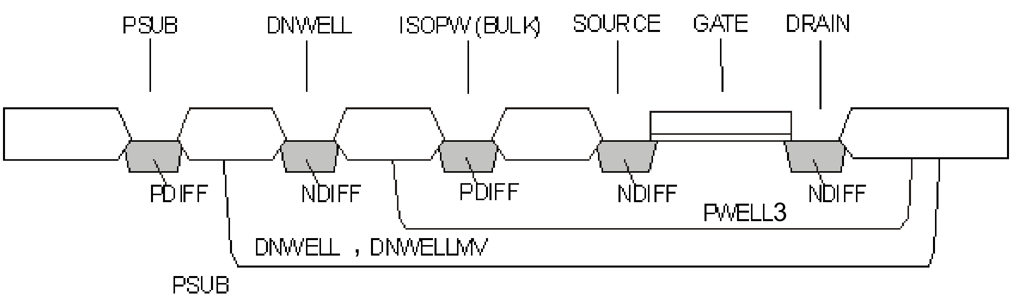

Figure 3.38 Additional Operating Conditions

Note: neli_6 in DNWELL

$$\begin{array}{lclcl} V_{PSUB} & \leq & V_{DNWELL} & \leq & V_{PSUB} + 45(50)V \\ V_{DNWELL} - 8(10)V & \leq & V_{PWELL3} & \leq & V_{DNWELL} \end{array}$$

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNELIS	drain-source breakdown @ VG=0V, Id=1µA, L=0.18µm	3.6	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						

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Name	Description	LSL	Low	Typ	High	USL	Unit
BEXNELI	mobility exponent	-	-	-1.8	-	-	-
FC_NELI	corner frequency @ VD=1.8V, Id=1µA, L=10µm, W=10µm	-	-	0.43	-	-	kHz
GAMNELI	body factor long channel @ L=10µm, W=10µm	-	-	0.56	-	-	√V
IDSNELIS	saturation current @ VG=1.8V, VD=1.8V, L=0.18µm, W=10µm	460	535	610	685	760	µA/µm
IOFNELIS	off-state leakage @ VD=1.8V, L=0.18µm, W=10µm	-	-	-	5	-	nA/µm
ISBNELIS	bulk current @ VD=1.8V, L=0.18µm	-	-	0.1	-	-	µA/µm
KP_NELI	gain factor long channel @ L=10µm, W=10µm	-	-	290	-	-	µA/V²
LEFNELI	effective channel length @ L=0.18µm	-	-	0.17	-	-	µm
NOINELI	Input referred noise @ VD=1.8V, Id=1µA, f=1Hz, L=10µm, W=10µm	-	-	7.3	-	-	µV.µm/√(Hz)
STSNELI	subthreshold slope @ VD=1.8V	-	-	12	-	-	decade/V
TC_VTXNELI	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	-0.78	-	-	mV/K
U0_NELI	effective mobility	-	-	345	-	-	cm²/Vs
VTINELIL	threshold voltage long channel @ VD=0.1V, L=10µm, W=10µm	0.29	0.32	0.35	0.38	0.41	V
VTINELIS	threshold voltage short channel @ VD=0.1V, L=0.18µm, W=10µm	0.26	0.305	0.35	0.395	0.44	V
VTINELISS	threshold voltage small channel @ VD=0.1V, L=0.18µm, W=0.22µm	-	-	0.275	-	-	V
VTXNELIS	extrapolated threshold voltage short channel @ VD=0.1V, L=0.18µm, W=10µm	-	-	0.41	-	-	V
WEFNELI	effective channel width @ W=0.22µm	-	-	0.2	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTNELI	Pelgrom coefficient gain factor mismatch	0.59	%µm
AIDNELI00	Pelgrom coefficient ID mismatch @ VG-VT=0V	6.76	%µm
AIDNELI01	Pelgrom coefficient ID mismatch @ VG-VT=0.1V	4.39	%µm
AIDNELI02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	2.99	%µm
AIDNELI04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	1.65	%µm
AIDNELI06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	1.11	%µm
AIDNELI08	Pelgrom coefficient ID mismatch @ VG-VT=0.8V	0.84	%µm
AIDNELI10	Pelgrom coefficient ID mismatch @ VG-VT=1V	0.69	%µm
AIDNELI14	Pelgrom coefficient ID mismatch @ VG-VT=1.4V	0.53	%µm
AVTNELI	Pelgrom coefficient VT mismatch	4.04	mVµm
DLTNELI	transistor delta length	0.01	µm
DWTNELI	transistor delta width	0.02	µm

neli_m_6

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VGD	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDB	-40°C to 175°C	-0.5	0	1.98	2.3	V
VSB	-40°C to 175°C	-0.5	0	1.98	2.3	V
VIB	-40°C to 175°C	-0.5	0	8	10	V
VIpsub	-40°C to 175°C	-0.5	0	10	12	V

Note: The node B (BULK) is: PWELL3.

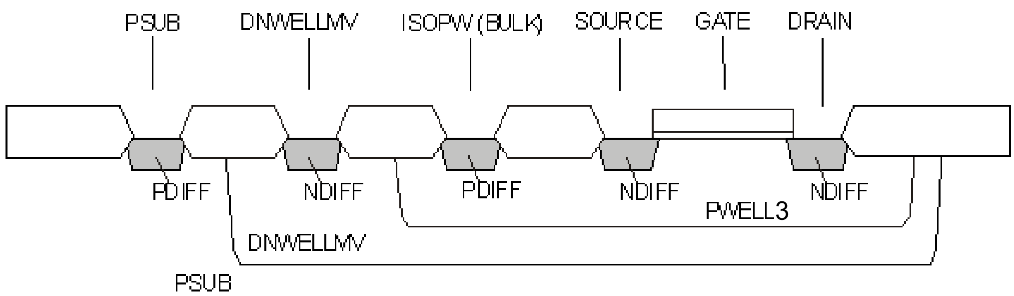

Figure 3.39 Additional Operating Conditions

Note: neli_m_6 in DNWELLMV

$$\begin{array}{lclcl} V_{PSUB} & \leq & V_{DNWELL} & \leq & V_{PSUB} + 10(12)V \\ V_{DNWELLMV} - 8(10)V & \leq & V_{PWELL3} & \leq & V_{DNWELLMV} \end{array}$$

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNELIS	drain-source breakdown @ VG=0V, Id=1µA, L=0.18µm	3.6	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXNELI	mobility exponent	-	-	-1.8	-	-	-
FC_NELI	corner frequency @ VD=1.8V, Id=1µA, L=10µm, W=10µm	-	-	0.43	-	-	kHz
GAMNELI	body factor long channel @ L=10µm, W=10µm	-	-	0.56	-	-	√V
IDSNELIS	saturation current @ VG=1.8V, VD=1.8V, L=0.18µm, W=10µm	460	535	610	685	760	µA/µm
IOFNELIS	off-state leakage @ VD=1.8V, L=0.18µm, W=10µm	-	-	-	5	-	nA/µm
ISBNELIS	bulk current @ VD=1.8V, L=0.18µm	-	-	0.1	-	-	µA/µm
KP_NELI	gain factor long channel @ L=10µm, W=10µm	-	-	290	-	-	µA/V²

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Name	Description	LSL	Low	Typ	High	USL	Unit
LEFNELI	effective channel length @ L=0.18µm	-	-	0.17	-	-	µm
NOINELI	Input referred noise @ VD=1.8V, Id=1µA, f=1Hz, L=10µm, W=10µm	-	-	7.3	-	-	µV.µm/√(Hz)
STSNELI	subthreshold slope @ VD=1.8V	-	-	12	-	-	decade/V
TC_VTXNELI	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	-0.78	-	-	mV/K
U0_NELI	effective mobility	-	-	345	-	-	cm²/Vs
VTINELIL	threshold voltage long channel @ VD=0.1V, L=10µm, W=10µm	0.29	0.32	0.35	0.38	0.41	V
VTINELIS	threshold voltage short channel @ VD=0.1V, L=0.18µm, W=10µm	0.26	0.305	0.35	0.395	0.44	V
VTINELISS	threshold voltage small channel @ VD=0.1V, L=0.18µm, W=0.22µm	-	-	0.275	-	-	V
VTXNELIS	extrapolated threshold voltage short channel @ VD=0.1V, L=0.18µm, W=10µm	-	-	0.41	-	-	V
WEFNELI	effective channel width @ W=0.22µm	-	-	0.2	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTNELI	Pelgrom coefficient gain factor mismatch	0.59	%µm
AIDNELI00	Pelgrom coefficient ID mismatch @ VG-VT=0V	6.76	%µm
AIDNELI01	Pelgrom coefficient ID mismatch @ VG-VT=0.1V	4.39	%µm
AIDNELI02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	2.99	%µm
AIDNELI04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	1.65	%µm
AIDNELI06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	1.11	%µm
AIDNELI08	Pelgrom coefficient ID mismatch @ VG-VT=0.8V	0.84	%µm
AIDNELI10	Pelgrom coefficient ID mismatch @ VG-VT=1V	0.69	%µm
AIDNELI14	Pelgrom coefficient ID mismatch @ VG-VT=1.4V	0.53	%µm
AVTNELI	Pelgrom coefficient VT mismatch	4.04	mVµm
DLTNELI	transistor delta length	0.01	µm
DWTNELI	transistor delta width	0.02	µm

peli

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VGD	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDB	-40°C to 175°C	-2.3	-1.98	0	0.5	V
VSB	-40°C to 175°C	-2.3	-1.98	0	0.5	V
VBpsub(1	-40°C to 175°C	-0.5	0	10	12	V

Note 1 If DNWELL instead of DNWELLMV is used for the isolated PMOS transistors, then max. VBpsub = 45 (50)V.

Note: The node B (BULK) is: NWELL3.

Process parameters

Negative values are considered as absolute values for their limits.

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPELIS	drain-source breakdown @ VG=0V, Id=-1µA, L=0.18µm	3.6	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXPELI	mobility exponent	-	-	-1.13	-	-	-
FC_PELI	corner frequency @ VD=1.8V, Id=1µA, L=10µm, W=10µm	-	-	0.28	-	-	kHz
GAMPELI	body factor long channel @ L=10µm, W=10µm	-	-	0.44	-	-	√V
IDSPELIS	saturation current @ VG=-1.8V, VD=-1.8V, L=0.18µm, W=10µm	200	250	300	350	400	µA/µm
IOFPELIS	off-state leakage @ VD=-1.8V, L=0.18µm, W=10µm	-	-	-	10	-	nA/µm
KP_PELI	gain factor long channel @ L=10µm, W=10µm	-	-	65	-	-	µA/V²
LEFPELI	effective channel length @ L=0.18µm	-	-	0.15	-	-	µm
NOIPELI	Input referred noise @ VD=-1.8V, Id=-1µA, f=1Hz, L=10µm, W=10µm	-	-	7.8	-	-	µV.µm/ √(Hz)
STSPELI	subthreshold slope @ VD=-1.8V	-	-	11	-	-	decade/V
TC_VTXPELI	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	0.76	-	-	mV/K
U0_PELI	effective mobility	-	-	75	-	-	cm²/Vs
VTIPELIL	threshold voltage long channel @ VD=-0.1V, L=10µm, W=10µm	-0.33	-0.36	-0.39	-0.42	-0.45	V
VTIPELIS	threshold voltage short channel @ VD=-0.1V, L=0.18µm, W=10µm	-0.24	-0.3	-0.36	-0.42	-0.48	V
VTIPELISS	threshold voltage small channel @ VD=-0.1V, L=0.18µm, W=0.22µm	-	-	-0.35	-	-	V
VTXPELIS	extrapolated threshold voltage short channel @ VD=-0.1V, L=0.18µm, W=10µm	-	-	-0.36	-	-	V
WEFPELI	effective channel width @ W=0.22µm	-	-	0.23	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTPELI	Pelgrom coefficient gain factor mismatch	0.69	%µm
AIDPELI00	Pelgrom coefficient ID mismatch @ VG-VT=0V	7.74	%µm
AIDPELI01	Pelgrom coefficient ID mismatch @ VG-VT=0.1V	4.71	%µm
AIDPELI02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	3.12	%µm
AIDPELI04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	1.73	%µm
AIDPELI06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	1.22	%µm
AIDPELI08	Pelgrom coefficient ID mismatch @ VG-VT=0.8V	0.98	%µm
AIDPELI10	Pelgrom coefficient ID mismatch @ VG-VT=1V	0.83	%µm
AIDPELI14	Pelgrom coefficient ID mismatch @ VG-VT=1.4V	0.67	%µm
AVTPELI	Pelgrom coefficient VT mismatch	3.78	mVµm
DLTPELI	transistor delta length	0.03	µm

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Name	Description	Typ	Unit
DWTPELI	transistor delta width	-0.01	µm

peli_5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VGD	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDB	-40°C to 175°C	-2.3	-1.98	0	0.5	V
VSB	-40°C to 175°C	-2.3	-1.98	0	0.5	V
VBpsub	-40°C to 175°C	-0.5	0	45	50	V

Note: The node B (BULK) is: NWELL3.

Process parameters

Negative values are considered as absolute values for their limits.

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPELIS	drain-source breakdown @ VG=0V, Id=-1µA, L=0.18µm	3.6	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXPELI	mobility exponent	-	-	-1.13	-	-	-
FC_PELI	corner frequency @ VD=1.8V, Id=1µA, L=10µm, W=10µm	-	-	0.28	-	-	kHz
GAMPELI	body factor long channel @ L=10µm, W=10µm	-	-	0.44	-	-	√V
IDSPELIS	saturation current @ VG=-1.8V, VD=-1.8V, L=0.18µm, W=10µm	200	250	300	350	400	µA/µm
IOFPELIS	off-state leakage @ VD=-1.8V, L=0.18µm, W=10µm	-	-	-	10	-	nA/µm
KP_PELI	gain factor long channel @ L=10µm, W=10µm	-	-	65	-	-	µA/V²
LEFPELI	effective channel length @ L=0.18µm	-	-	0.15	-	-	µm
NOIPELI	Input referred noise @ VD=-1.8V, Id=-1µA, f=1Hz, L=10µm, W=10µm	-	-	7.8	-	-	µV.µm/√(Hz)
STSPELI	subthreshold slope @ VD=-1.8V	-	-	11	-	-	decade/V
TC_VTXPELI	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	0.76	-	-	mV/K
U0_PELI	effective mobility	-	-	75	-	-	cm²/Vs
VTIPELIL	threshold voltage long channel @ VD=-0.1V, L=10µm, W=10µm	-0.33	-0.36	-0.39	-0.42	-0.45	V
VTIPELIS	threshold voltage short channel @ VD=-0.1V, L=0.18µm, W=10µm	-0.24	-0.3	-0.36	-0.42	-0.48	V
VTIPELISS	threshold voltage small channel @ VD=-0.1V, L=0.18µm, W=0.22µm	-	-	-0.35	-	-	V
VTXPELIS	extrapolated threshold voltage short channel @ VD=-0.1V, L=0.18µm, W=10µm	-	-	-0.36	-	-	V
WEFPELI	effective channel width @ W=0.22µm	-	-	0.23	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTPELI	Pelgrom coefficient gain factor mismatch	0.69	%µm
AIDPELI00	Pelgrom coefficient ID mismatch @ VG-VT=0V	7.74	%µm
AIDPELI01	Pelgrom coefficient ID mismatch @ VG-VT=0.1V	4.71	%µm
AIDPELI02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	3.12	%µm
AIDPELI04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	1.73	%µm
AIDPELI06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	1.22	%µm
AIDPELI08	Pelgrom coefficient ID mismatch @ VG-VT=0.8V	0.98	%µm
AIDPELI10	Pelgrom coefficient ID mismatch @ VG-VT=1V	0.83	%µm
AIDPELI14	Pelgrom coefficient ID mismatch @ VG-VT=1.4V	0.67	%µm
AVTPELI	Pelgrom coefficient VT mismatch	3.78	mVµm
DLTPELI	transistor delta length	0.03	µm
DWTPELI	transistor delta width	-0.01	µm

peli_m_5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VGD	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDB	-40°C to 175°C	-2.3	-1.98	0	0.5	V
VSB	-40°C to 175°C	-2.3	-1.98	0	0.5	V
VBpsub	-40°C to 175°C	-0.5	0	10	12	V

Note: The node B (BULK) is: NWELL3.

Process parameters

Negative values are considered as absolute values for their limits.

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPELIS	drain-source breakdown @ VG=0V, Id=-1µA, L=0.18µm	3.6	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXPELI	mobility exponent	-	-	-1.13	-	-	-
FC_PELI	corner frequency @ VD=1.8V, Id=1µA, L=10µm, W=10µm	-	-	0.28	-	-	kHz
GAMPELI	body factor long channel @ L=10µm, W=10µm	-	-	0.44	-	-	√V
IDSPELIS	saturation current @ VG=-1.8V, VD=-1.8V, L=0.18µm, W=10µm	200	250	300	350	400	µA/µm
IOFPELIS	off-state leakage @ VD=-1.8V, L=0.18µm, W=10µm	-	-	-	10	-	nA/µm
KP_PELI	gain factor long channel @ L=10µm, W=10µm	-	-	65	-	-	µA/V²
LEFPELI	effective channel length @ L=0.18µm	-	-	0.15	-	-	µm
NOIPELI	Input referred noise @ VD=-1.8V, Id=-1µA, f=1Hz, L=10µm, W=10µm	-	-	7.8	-	-	µV.µm/√(Hz)

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Name	Description	LSL	Low	Typ	High	USL	Unit
STSPELI	subthreshold slope @ VD=-1.8V	-	-	11	-	-	decade/V
TC_VTXPELI	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	0.76	-	-	mV/K
U0_PELI	effective mobility	-	-	75	-	-	cm²/Vs
VTIPELIL	threshold voltage long channel @ VD=-0.1V, L=10µm, W=10µm	-0.33	-0.36	-0.39	-0.42	-0.45	V
VTIPELIS	threshold voltage short channel @ VD=-0.1V, L=0.18µm, W=10µm	-0.24	-0.3	-0.36	-0.42	-0.48	V
VTIPELISS	threshold voltage small channel @ VD=-0.1V, L=0.18µm, W=0.22µm	-	-	-0.35	-	-	V
VTXPELIS	extrapolated threshold voltage short channel @ VD=-0.1V, L=0.18µm, W=10µm	-	-	-0.36	-	-	V
WEFPELI	effective channel width @ W=0.22µm	-	-	0.23	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTPELI	Pelgrom coefficient gain factor mismatch	0.69	%µm
AIDPELI00	Pelgrom coefficient ID mismatch @ VG-VT=0V	7.74	%µm
AIDPELI01	Pelgrom coefficient ID mismatch @ VG-VT=0.1V	4.71	%µm
AIDPELI02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	3.12	%µm
AIDPELI04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	1.73	%µm
AIDPELI06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	1.22	%µm
AIDPELI08	Pelgrom coefficient ID mismatch @ VG-VT=0.8V	0.98	%µm
AIDPELI10	Pelgrom coefficient ID mismatch @ VG-VT=1V	0.83	%µm
AIDPELI14	Pelgrom coefficient ID mismatch @ VG-VT=1.4V	0.67	%µm
AVTPELI	Pelgrom coefficient VT mismatch	3.78	mVµm
DLTPELI	transistor delta length	0.03	µm
DWTPELI	transistor delta width	-0.01	µm

3.14 SVT module

3.14.1 Device parameters

nesvt

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VGD	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDB	-40°C to 175°C	-0.5	0	1.98	2.3	V
VSB	-40°C to 175°C	-0.5	0	1.98	2.3	V

Note: The node B (BULK) is: PWELL5.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNESVTS	drain-source breakdown @ VG=0V, Id=1µA, L=0.18µm	3.6	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXNESVT	mobility exponent	-	-	-1.73	-	-	-
FC_NESVT	corner frequency @ VD=1.8V, Id=1µA, L=10µm, W=10µm	-	-	4.5	-	-	kHz
GA_NESVT	body factor long channel @ L=10µm, W=10µm	-	-	0.65	-	-	√V
IDSNESVTS	saturation current @ VG=1.8V, VD=1.8V, L=0.18µm, W=10µm	400	475	550	625	700	µA/µm
IOFNESVTS	off-state leakage @ VD=1.8V, L=0.18µm, W=10µm	-	-	-	40	-	pA/µm
ISBNESVTS	bulk current @ VD=1.8V, L=0.18µm	-	-	0.02	-	-	µA/µm
KP_NESVT	gain factor long channel @ L=10µm, W=10µm	-	-	261	-	-	$\mu A/V^2$
LEFNESVT	effective channel length @ L=0.18µm	-	-	0.16	-	-	µm
NOINESVT	Input referred noise @ VD=1.8V, Id=1µA, f=1Hz, L=10µm, W=10µm	-	-	14.9	-	-	µV.µm/ √(Hz)
STSNESVT	subthreshold slope @ VD=1.8V	-	-	11.9	-	-	decade/V
TC_VTXNESVT	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	0.84	-	-	mV/K
U0_NESVT	effective mobility	-	-	311	-	-	cm^2/Vs
VTINESVTL	threshold voltage long channel @ VD=0.1V, L=10µm, W=10µm	0.4	0.43	0.46	0.49	0.52	V
VTINESVTS	threshold voltage short channel @ VD=0.1V, L=0.18µm, W=10µm	0.38	0.42	0.47	0.52	0.56	V
VTINESVTSS	threshold voltage small channel @ VD=0.1V, L=0.18µm, W=0.22µm	-	-	0.36	-	-	V
VTXNESVTS	extrapolated threshold voltage short channel @ VD=0.1V, L=0.18µm, W=10µm	-	-	0.54	-	-	V
WEFNESVT	effective channel width @ W=0.22µm	-	-	0.17	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTNESVT	Pelgrom coefficient gain factor mismatch	0.66	%µm
AIDNESVT00	Pelgrom coefficient ID mismatch @ VG-VT=0V	7.3	%µm
AIDNESVT01	Pelgrom coefficient ID mismatch @ VG-VT=0.1V	4.66	%µm
AIDNESVT02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	3.13	%µm
AIDNESVT04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	1.69	%µm
AIDNESVT06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	1.11	%µm
AIDNESVT08	Pelgrom coefficient ID mismatch @ VG-VT=0.8V	0.83	%µm
AIDNESVT10	Pelgrom coefficient ID mismatch @ VG-VT=1V	0.67	%µm
AIDNESVT14	Pelgrom coefficient ID mismatch @ VG-VT=1.4V	0.51	%µm
AVTNESVT	Pelgrom coefficient VT mismatch	4.35	mVµm
DLTNESVT	transistor delta length	0.02	µm
DWTNESVT	transistor delta width	0.05	µm

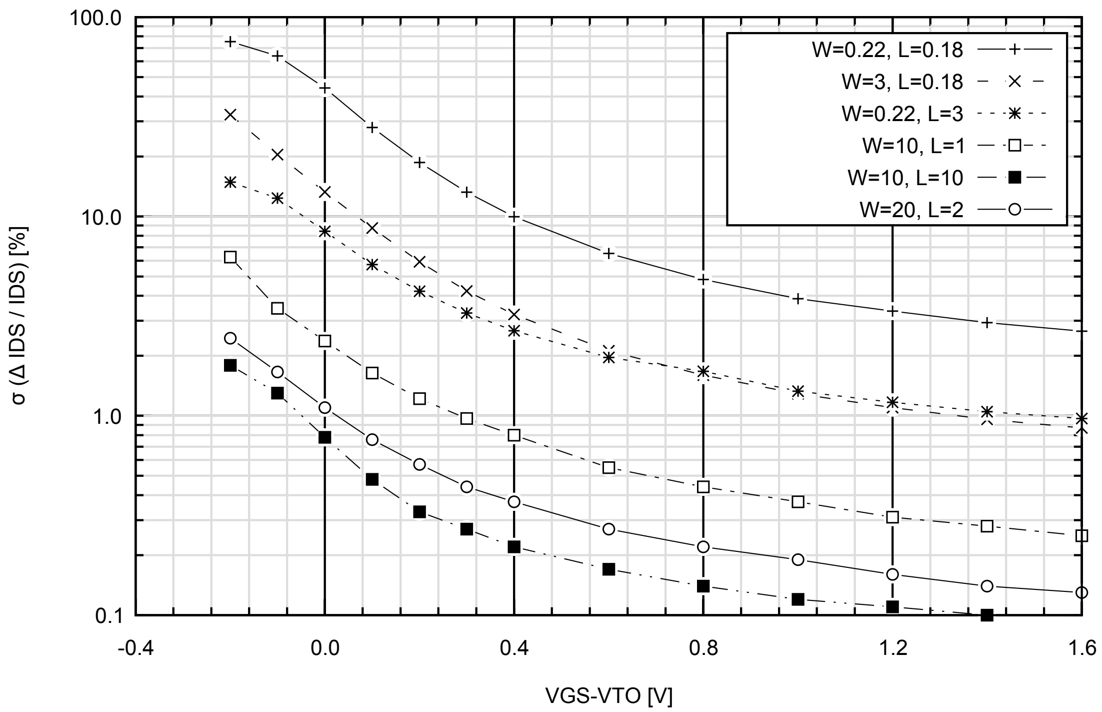

Figure 3.40 Device nesvt: drain current matching vs. VGS-VTO (typical values, drawn W and L)

nesvti

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40 °C to 175 °C	-2.3	-1.98	1.98	2.3	V
VGD	-40 °C to 175 °C	-2.3	-1.98	1.98	2.3	V
VDS	-40 °C to 175 °C	-2.3	-1.98	1.98	2.3	V
VDB	-40 °C to 175 °C	-0.5	0	1.98	2.3	V
VSB	-40 °C to 175 °C	-0.5	0	1.98	2.3	V

Note: The node B (BULK) is: PWELL5.

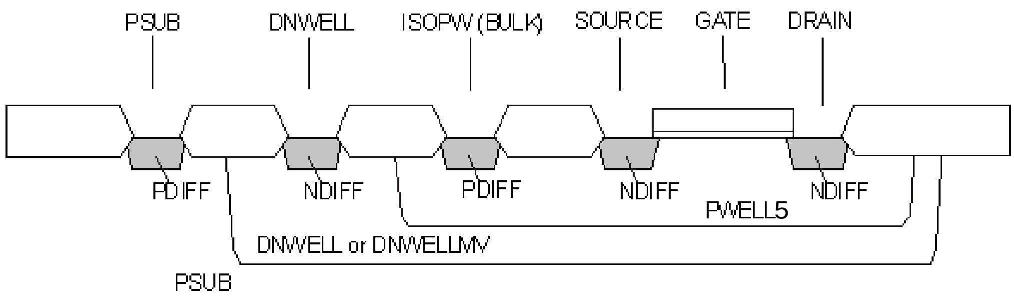

Figure 3.41 Additional Operating Conditions

Note: nesvti in DNWELL

$$\begin{array}{lclcl} V_{PSUB} & \leq & V_{DNWELL} & \leq & V_{PSUB} + 45(50)V \\ V_{DNWELL} - 8(10)V & \leq & V_{PWELL1} & \leq & V_{DNWELL} \end{array}$$

nesvti in DNWELLMV

$$\begin{array}{lclcl} V_{PSUB} & \leq & V_{DNWELL} & \leq & V_{PSUB} + 10(12)V \\ V_{DNWELLMV} - 8(10)V & \leq & V_{PWELL1} & \leq & V_{DNWELLMV} \end{array}$$

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNESVTIS	drain-source breakdown @ VG=0V, Id=1µA, L=0.18µm	3.6	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXNESVTI	mobility exponent	-	-	-1.73	-	-	-
FC_NESVTI	corner frequency @ VD=1.8V, Id=1µA, L=10µm, W=10µm	-	-	4.5	-	-	kHz
GA_NESVTI	body factor long channel @ L=10µm, W=10µm	-	-	0.64	-	-	√V
IDSNESVTIS	saturation current @ VG=1.8V, VD=1.8V, L=0.18µm, W=10µm	400	475	550	625	700	µA/µm
IOFNESVTIS	off-state leakage @ VD=1.8V, L=0.18µm, W=10µm	-	-	-	40	-	pA/µm
ISBNESVTIS	bulk current @ VD=1.8V, L=0.18µm	-	-	0.02	-	-	µA/µm
KP_NESVTI	gain factor long channel @ L=10µm, W=10µm	-	-	267	-	-	µA/V²
LEFNESVTI	effective channel length @ L=0.18µm	-	-	0.16	-	-	µm
NOINESVTI	Input referred noise @ VD=1.8V, Id=1µA, f=1Hz, L=10µm, W=10µm	-	-	14.9	-	-	µV.µm/√(Hz)
STSNESVTI	subthreshold slope @ VD=1.8V	-	-	11.6	-	-	decade/V
TC_VTXNESVTI	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	-0.84	-	-	mV/K
U0_NESVTI	effective mobility	-	-	318	-	-	cm²/Vs
VTINESVTIL	threshold voltage long channel @ VD=0.1V, L=10µm, W=10µm	0.39	0.42	0.45	0.48	0.51	V

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Name	Description	LSL	Low	Typ	High	USL	Unit
VTINESVTIS	threshold voltage short channel @ VD=0.1V, L=0.18µm, W=10µm	0.37	0.41	0.46	0.51	0.55	V
VTINESVTISS	threshold voltage small channel @ VD=0.1V, L=0.18µm, W=0.22µm	-	-	0.36	-	-	V
VTXNESVTIS	extrapolated threshold voltage short channel @ VD=0.1V, L=0.18µm, W=10µm	-	-	0.54	-	-	V
WEFNESVTI	effective channel width @ W=0.22µm	-	-	0.19	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTNESVTI	Pelgrom coefficient gain factor mismatch	0.71	%µm
AIDNESVTI00	Pelgrom coefficient ID mismatch @ VG-VT=0V	7.43	%µm
AIDNESVTI01	Pelgrom coefficient ID mismatch @ VG-VT=0.1V	4.76	%µm
AIDNESVTI02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	3.23	%µm
AIDNESVTI04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	1.79	%µm
AIDNESVTI06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	1.21	%µm
AIDNESVTI08	Pelgrom coefficient ID mismatch @ VG-VT=0.8V	0.92	%µm
AIDNESVTI10	Pelgrom coefficient ID mismatch @ VG-VT=1V	0.75	%µm
AIDNESVTI14	Pelgrom coefficient ID mismatch @ VG-VT=1.4V	0.58	%µm
AVTNESVTI	Pelgrom coefficient VT mismatch	4.46	mVµm
DLTNESVTI	transistor delta length	0.02	µm
DWTNESVTI	transistor delta width	0.03	µm

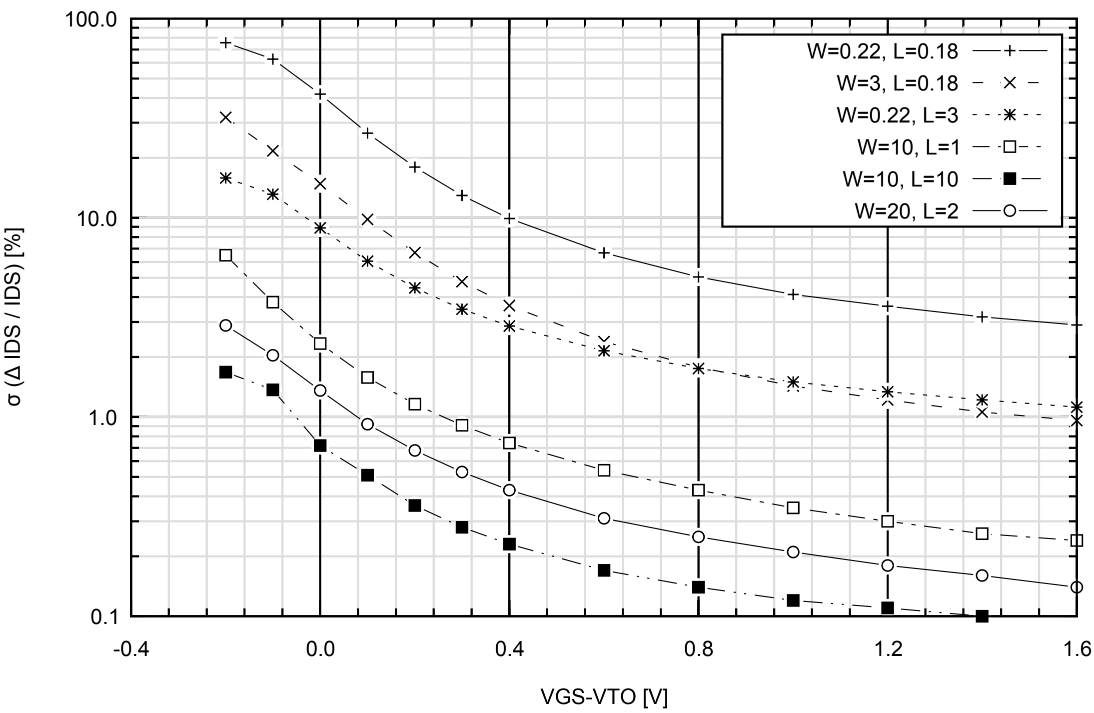

Figure 3.42 Device nesvti: drain current matching vs. VGS-VTO (typical values, drawn W and L)

nesvti_6

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VGD	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDB	-40°C to 175°C	-0.5	0	1.98	2.3	V
VSB	-40°C to 175°C	-0.5	0	1.98	2.3	V
VIpsub	-40°C to 175°C	-0.5	0	45	50	V
VIB	-40°C to 175°C	-0.5	0	8	10	V

Note: The node B (BULK) is: PWELL5.

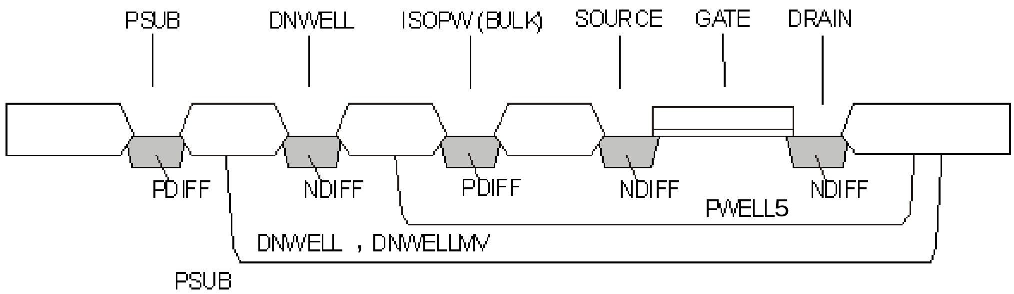

Figure 3.43 Additional Operating Conditions

Note: nesvti_6 in DNWELL

$$
\begin{aligned}
V_{PSUB} &\leq V_{DNWELL} \leq V_{PSUB} + 45(50)V \\
V_{DNWELL} - 8(10)V &\leq V_{PWELL1} \leq V_{DNWELL}
\end{aligned}
$$

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNESVTIS	drain-source breakdown @ VG=0V, Id=1µA, L=0.18µm	3.6	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXNESVTI	mobility exponent	-	-	-1.73	-	-	-
FC_NESVTI	corner frequency @ VD=1.8V, Id=1µA, L=10µm, W=10µm	-	-	4.5	-	-	kHz
GA_NESVTI	body factor long channel @ L=10µm, W=10µm	-	-	0.64	-	-	√V
IDSNESVTIS	saturation current @ VG=1.8V, VD=1.8V, L=0.18µm, W=10µm	400	475	550	625	700	µA/µm
IOFNESVTIS	off-state leakage @ VD=1.8V, L=0.18µm, W=10µm	-	-	-	40	-	pA/µm
ISBNESVTIS	bulk current @ VD=1.8V, L=0.18µm	-	-	0.02	-	-	µA/µm
KP_NESVTI	gain factor long channel @ L=10µm, W=10µm	-	-	267	-	-	µA/V²
LEFNESVTI	effective channel length @ L=0.18µm	-	-	0.16	-	-	µm

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Name	Description	LSL	Low	Typ	High	USL	Unit
NOINESVTI	Input referred noise @ VD=1.8V, Id=1µA, f=1Hz, L=10µm, W=10µm	-	-	14.9	-	-	µV.µm/ √(Hz)
STSNESVTI	subthreshold slope @ VD=1.8V	-	-	11.6	-	-	decade/V
TC_VTXNESVTI	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	-0.84	-	-	mV/K
U0_NESVTI	effective mobility	-	-	318	-	-	cm²/Vs
VTINESVTIL	threshold voltage long channel @ VD=0.1V, L=10µm, W=10µm	0.39	0.42	0.45	0.48	0.51	V
VTINESVTIS	threshold voltage short channel @ VD=0.1V, L=0.18µm, W=10µm	0.37	0.41	0.46	0.51	0.55	V
VTINESVTISS	threshold voltage small channel @ VD=0.1V, L=0.18µm, W=0.22µm	-	-	0.36	-	-	V
VTXNESVTIS	extrapolated threshold voltage short channel @ VD=0.1V, L=0.18µm, W=10µm	-	-	0.54	-	-	V
WEFNESVTI	effective channel width @ W=0.22µm	-	-	0.19	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTNESVTI	Pelgrom coefficient gain factor mismatch	0.71	%µm
AIDNESVTI00	Pelgrom coefficient ID mismatch @ VG-VT=0V	7.43	%µm
AIDNESVTI01	Pelgrom coefficient ID mismatch @ VG-VT=0.1V	4.76	%µm
AIDNESVTI02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	3.23	%µm
AIDNESVTI04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	1.79	%µm
AIDNESVTI06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	1.21	%µm
AIDNESVTI08	Pelgrom coefficient ID mismatch @ VG-VT=0.8V	0.92	%µm
AIDNESVTI10	Pelgrom coefficient ID mismatch @ VG-VT=1V	0.75	%µm
AIDNESVTI14	Pelgrom coefficient ID mismatch @ VG-VT=1.4V	0.58	%µm
AVTNESVTI	Pelgrom coefficient VT mismatch	4.46	mVµm
DLTNESVTI	transistor delta length	0.02	µm
DWTNESVTI	transistor delta width	0.03	µm

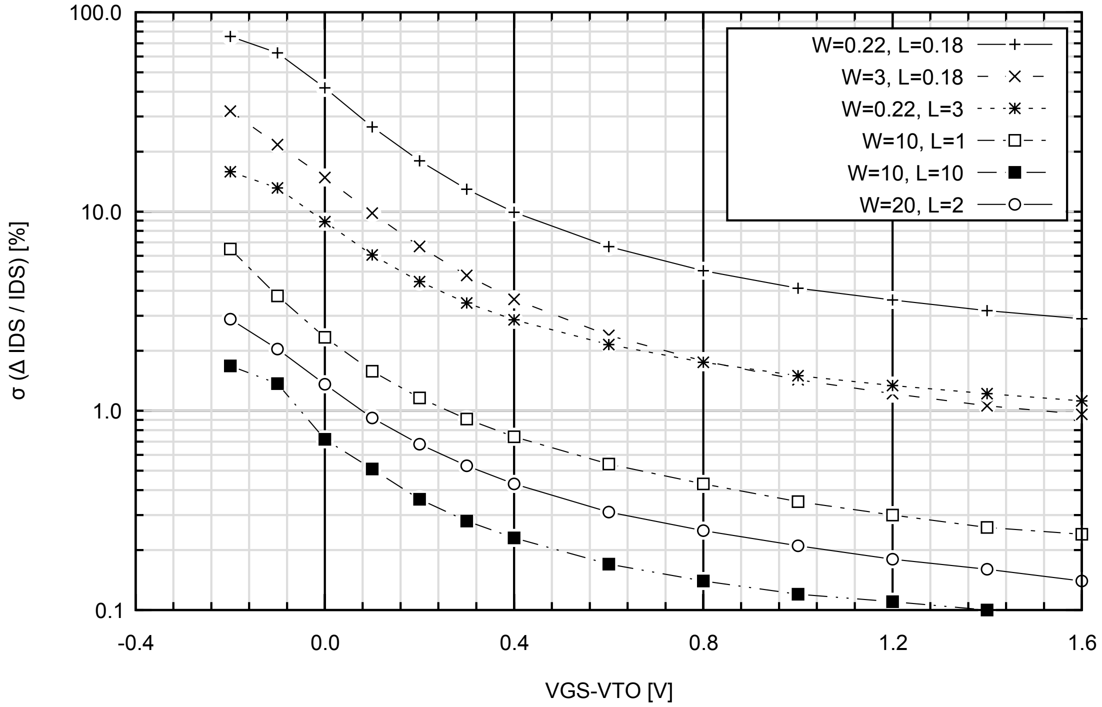

Figure 3.44 Device nesvti: drain current matching vs. VGS-VTO (typical values, drawn W and L)

nesvti_m_6

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VGD	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDB	-40°C to 175°C	-0.5	0	1.98	2.3	V
VSB	-40°C to 175°C	-0.5	0	1.98	2.3	V
VIpsub	-40°C to 175°C	-0.5	0	10	12	V
VIB	-40°C to 175°C	-0.5	0	8	10	V

Note: The node B (BULK) is: PWELL5.

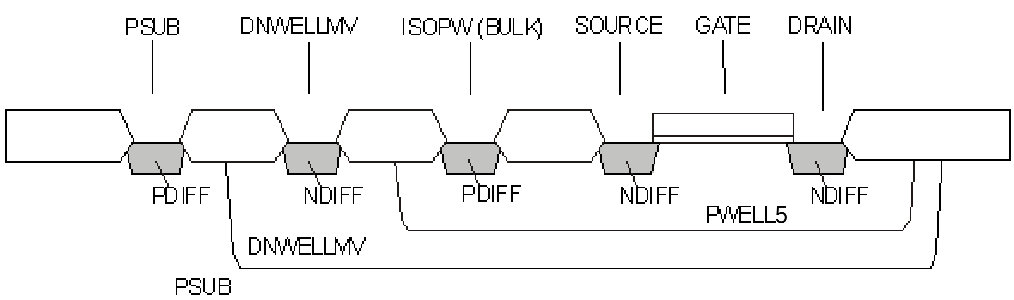

Figure 3.45 Additional Operating Conditions

Note: nesvti_m_6 in DNWELLMV

$$\begin{array}{lclcl} V_{PSUB} & \leq & V_{DNWELL} & \leq & V_{PSUB} + 10(12)V \\ V_{DNWELLMV} - 8(10)V & \leq & V_{PWELL1} & \leq & V_{DNWELLMV} \end{array}$$

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNESVTIS	drain-source breakdown @ VG=0V, Id=1μA, L=0.18μm	3.6	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXNESVTI	mobility exponent	-	-	-1.73	-	-	-
FC_NESVTI	corner frequency @ VD=1.8V, Id=1μA, L=10μm, W=10μm	-	-	4.5	-	-	kHz
GA_NESVTI	body factor long channel @ L=10μm, W=10μm	-	-	0.64	-	-	√V
IDSNESVTIS	saturation current @ VG=1.8V, VD=1.8V, L=0.18μm, W=10μm	400	475	550	625	700	μA/μm
IOFNESVTIS	off-state leakage @ VD=1.8V, L=0.18μm, W=10μm	-	-	-	40	-	pA/μm
ISBNESVTIS	bulk current @ VD=1.8V, L=0.18μm	-	-	0.02	-	-	μA/μm
KP_NESVTI	gain factor long channel @ L=10μm, W=10μm	-	-	267	-	-	μA/V²
LEFNESVTI	effective channel length @ L=0.18μm	-	-	0.16	-	-	μm
NOINESVTI	Input referred noise @ VD=1.8V, Id=1μA, f=1Hz, L=10μm, W=10μm	-	-	14.9	-	-	μV.μm/ √(Hz)
STSNESVTI	subthreshold slope @ VD=1.8V	-	-	11.6	-	-	decade/V
TC_VTXNESVTI	threshold voltage temperature coefficient @ L=10μm, W=10μm	-	-	-0.84	-	-	mV/K
U0_NESVTI	effective mobility	-	-	318	-	-	cm²/Vs
VTINESVTIL	threshold voltage long channel @ VD=0.1V, L=10μm, W=10μm	0.39	0.42	0.45	0.48	0.51	V
VTINESVTIS	threshold voltage short channel @ VD=0.1V, L=0.18μm, W=10μm	0.37	0.41	0.46	0.51	0.55	V
VTINESVTISS	threshold voltage small channel @ VD=0.1V, L=0.18μm, W=0.22μm	-	-	0.36	-	-	V
VTXNESVTIS	extrapolated threshold voltage short channel @ VD=0.1V, L=0.18μm, W=10μm	-	-	0.54	-	-	V
WEFNESVTI	effective channel width @ W=0.22μm	-	-	0.19	-	-	μm

Matching parameters

Name	Description	Typ	Unit
ABTNESVTI	Pelgrom coefficient gain factor mismatch	0.71	%μm
AIDNESVTI00	Pelgrom coefficient ID mismatch @ VG-VT=0V	7.43	%μm
AIDNESVTI01	Pelgrom coefficient ID mismatch @ VG-VT=0.1V	4.76	%μm
AIDNESVTI02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	3.23	%μm
AIDNESVTI04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	1.79	%μm
AIDNESVTI06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	1.21	%μm
AIDNESVTI08	Pelgrom coefficient ID mismatch @ VG-VT=0.8V	0.92	%μm

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Name	Description	Typ	Unit
AIDNESVTI10	Pelgrom coefficient ID mismatch @ VG-VT=1V	0.75	%µm
AIDNESVTI14	Pelgrom coefficient ID mismatch @ VG-VT=1.4V	0.58	%µm
AVTNESVTI	Pelgrom coefficient VT mismatch	4.46	mVµm
DLTNESVTI	transistor delta length	0.02	µm
DWTNESVTI	transistor delta width	0.03	µm

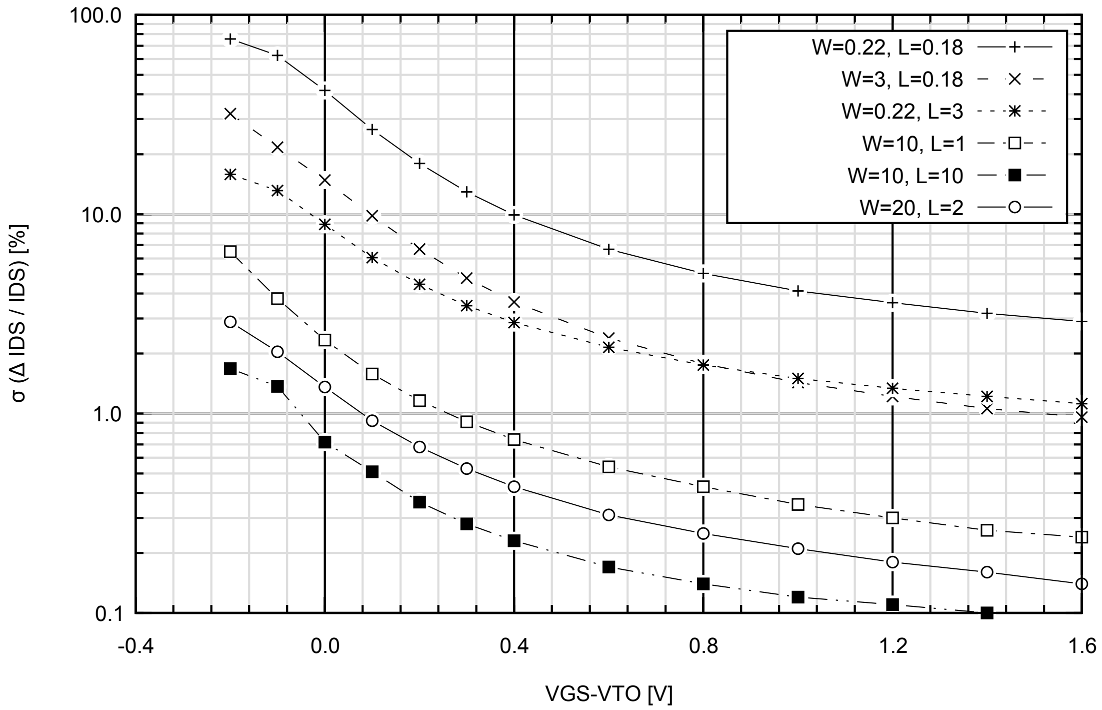

Figure 3.46 Device nesvti: drain current matching vs. VGS-VTO (typical values, drawn W and L)

pesvt

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VGD	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDB	-40°C to 175°C	-2.3	-1.98	0	0.5	V
VSB	-40°C to 175°C	-2.3	-1.98	0	0.5	V
VBpsub	-40°C to 175°C	-0.5	0	1.98	2.3	V

Note: The node B (BULK) is: NWELL5.

Process parameters

Negative values are considered as absolute values for their limits.

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPESVTS	drain-source breakdown @ VG=0V, Id=-1µA, L=0.18µm	3.6	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXPESVT	mobility exponent	-	-	-1.02	-	-	-

⇒

Name	Description	LSL	Low	Typ	High	USL	Unit
FC_PESVT	corner frequency @ VD=1.8V, Id=1µA, L=10µm, W=10µm	-	-	0.47	-	-	kHz
GA_PESVT	body factor long channel @ L=10µm, W=10µm	-	-	0.64	-	-	√V
IDSPESVTS	saturation current @ VG=-1.8V, VD=-1.8V, L=0.18µm, W=10µm	155	205	255	305	355	µA/µm
IOFPESVTS	off-state leakage @ VD=-1.8V, L=0.18µm, W=10µm	-	-	-	40	-	pA/µm
KP_PESVT	gain factor long channel @ L=10µm, W=10µm	-	-	58	-	-	$\mu A/V^2$
LEFPESVT	effective channel length @ L=0.18µm	-	-	0.13	-	-	µm
NOIPESVT	Input referred noise @ VD=-1.8V, Id=-1µA, f=1Hz, L=10µm, W=10µm	-	-	14.2	-	-	µV.µm/ √(Hz)
STSPESVT	subthreshold slope @ VD=-1.8V	-	-	12.1	-	-	decade/V
TC_VTXPESVT	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	-0.81	-	-	mV/K
U0_PESVT	effective mobility	-	-	71	-	-	cm^2/Vs
VTIPESVTL	threshold voltage long channel @ VD=-0.1V, L=10µm, W=10µm	-0.46	-0.49	-0.52	-0.55	-0.58	V
VTIPESVTS	threshold voltage short channel @ VD=-0.1V, L=0.18µm, W=10µm	-0.36	-0.42	-0.48	-0.54	-0.6	V
VTIPESVTSS	threshold voltage small channel @ VD=-0.1V, L=0.18µm, W=0.22µm	-	-	-0.47	-	-	V
VTXPESVTS	extrapolated threshold voltage short channel @ VD=-0.1V, L=0.18µm, W=10µm	-	-	-0.48	-	-	V
WEFPESVT	effective channel width @ W=0.22µm	-	-	0.25	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTPESVT	Pelgrom coefficient gain factor mismatch	0.74	%µm
AIDPESVT00	Pelgrom coefficient ID mismatch @ VG-VT=0V	8.15	%µm
AIDPESVT01	Pelgrom coefficient ID mismatch @ VG-VT=0.1V	5.16	%µm
AIDPESVT02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	3.46	%µm
AIDPESVT04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	1.94	%µm
AIDPESVT06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	1.33	%µm
AIDPESVT08	Pelgrom coefficient ID mismatch @ VG-VT=0.8V	1.02	%µm
AIDPESVT10	Pelgrom coefficient ID mismatch @ VG-VT=1V	0.85	%µm
AIDPESVT14	Pelgrom coefficient ID mismatch @ VG-VT=1.4V	0.66	%µm
AVTPESVT	Pelgrom coefficient VT mismatch	4.54	mVµm
DLTPESVT	transistor delta length	0.05	µm
DWTPESVT	transistor delta width	-0.03	µm

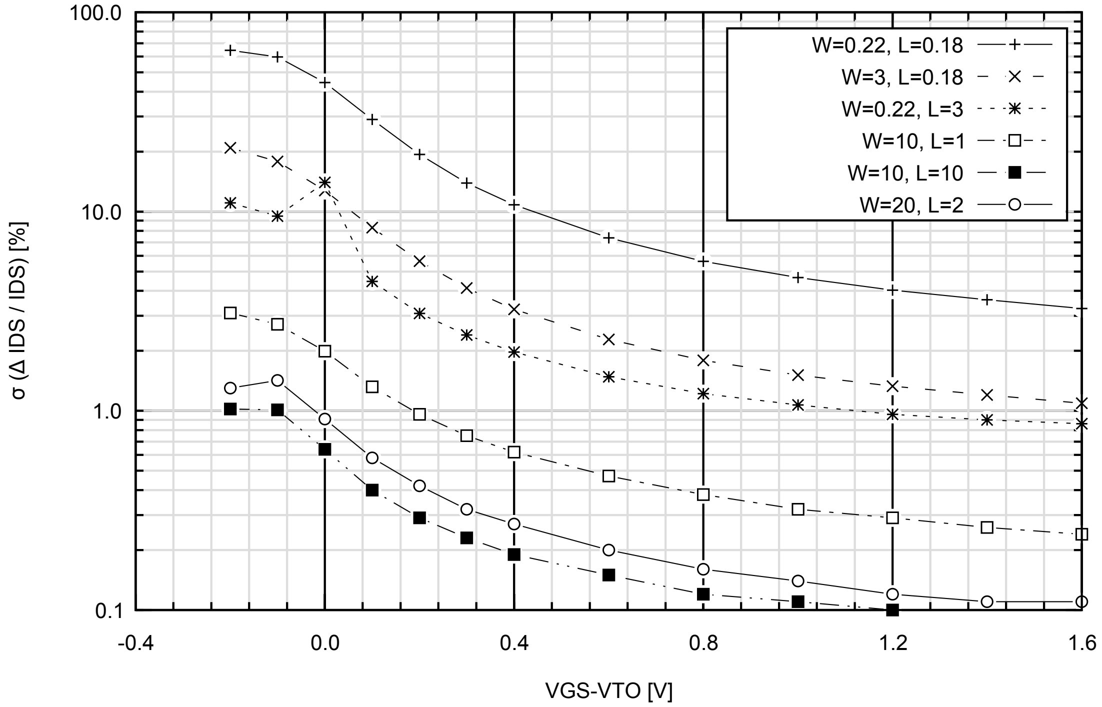

Figure 3.47 Device pesvt: drain current matching vs. VGS-VTO (typical values, drawn W and L)

pesvt_5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VGD	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDB	-40°C to 175°C	-2.3	-1.98	0	0.5	V
VSB	-40°C to 175°C	-2.3	-1.98	0	0.5	V
VBpsub	-40°C to 175°C	-0.5	0	1.98	2.3	V

Note: The node B (BULK) is: NWELL5.

Process parameters

Negative values are considered as absolute values for their limits.

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPESVTS	drain-source breakdown @ VG=0V, Id=-1µA, L=0.18µm	3.6	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXPESVT	mobility exponent	-	-	-1.02	-	-	-
FC_PESVT	corner frequency @ VD=1.8V, Id=1µA, L=10µm, W=10µm	-	-	0.47	-	-	kHz
GA_PESVT	body factor long channel @ L=10µm, W=10µm	-	-	0.64	-	-	√V
IDSPESVTS	saturation current @ VG=-1.8V, VD=-1.8V, L=0.18µm, W=10µm	155	205	255	305	355	µA/µm

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Name	Description	LSL	Low	Typ	High	USL	Unit
IOFPESVTS	off-state leakage @ VD=-1.8V, L=0.18µm, W=10µm	-	-	-	40	-	pA/µm
KP_PESVT	gain factor long channel @ L=10µm, W=10µm	-	-	58	-	-	µA/V²
LEFPESVT	effective channel length @ L=0.18µm	-	-	0.13	-	-	µm
NOIPESVT	Input referred noise @ VD=-1.8V, Id=-1µA, f=1Hz, L=10µm, W=10µm	-	-	14.2	-	-	µV.µm/ √(Hz)
STSPESVT	subthreshold slope @ VD=-1.8V	-	-	12.1	-	-	decade/V
TC_VTXPESVT	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	-0.81	-	-	mV/K
U0_PESVT	effective mobility	-	-	71	-	-	cm²/Vs
VTIPESVTL	threshold voltage long channel @ VD=-0.1V, L=10µm, W=10µm	-0.46	-0.49	-0.52	-0.55	-0.58	V
VTIPESVTS	threshold voltage short channel @ VD=-0.1V, L=0.18µm, W=10µm	-0.36	-0.42	-0.48	-0.54	-0.6	V
VTIPESVTSS	threshold voltage small channel @ VD=-0.1V, L=0.18µm, W=0.22µm	-	-	-0.47	-	-	V
VTXPESVTS	extrapolated threshold voltage short channel @ VD=-0.1V, L=0.18µm, W=10µm	-	-	-0.48	-	-	V
WEFPESVT	effective channel width @ W=0.22µm	-	-	0.25	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTPESVT	Pelgrom coefficient gain factor mismatch	0.74	%µm
AIDPESVT00	Pelgrom coefficient ID mismatch @ VG-VT=0V	8.15	%µm
AIDPESVT01	Pelgrom coefficient ID mismatch @ VG-VT=0.1V	5.16	%µm
AIDPESVT02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	3.46	%µm
AIDPESVT04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	1.94	%µm
AIDPESVT06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	1.33	%µm
AIDPESVT08	Pelgrom coefficient ID mismatch @ VG-VT=0.8V	1.02	%µm
AIDPESVT10	Pelgrom coefficient ID mismatch @ VG-VT=1V	0.85	%µm
AIDPESVT14	Pelgrom coefficient ID mismatch @ VG-VT=1.4V	0.66	%µm
AVTPESVT	Pelgrom coefficient VT mismatch	4.54	mVµm
DLTPESVT	transistor delta length	0.05	µm
DWTPESVT	transistor delta width	-0.03	µm

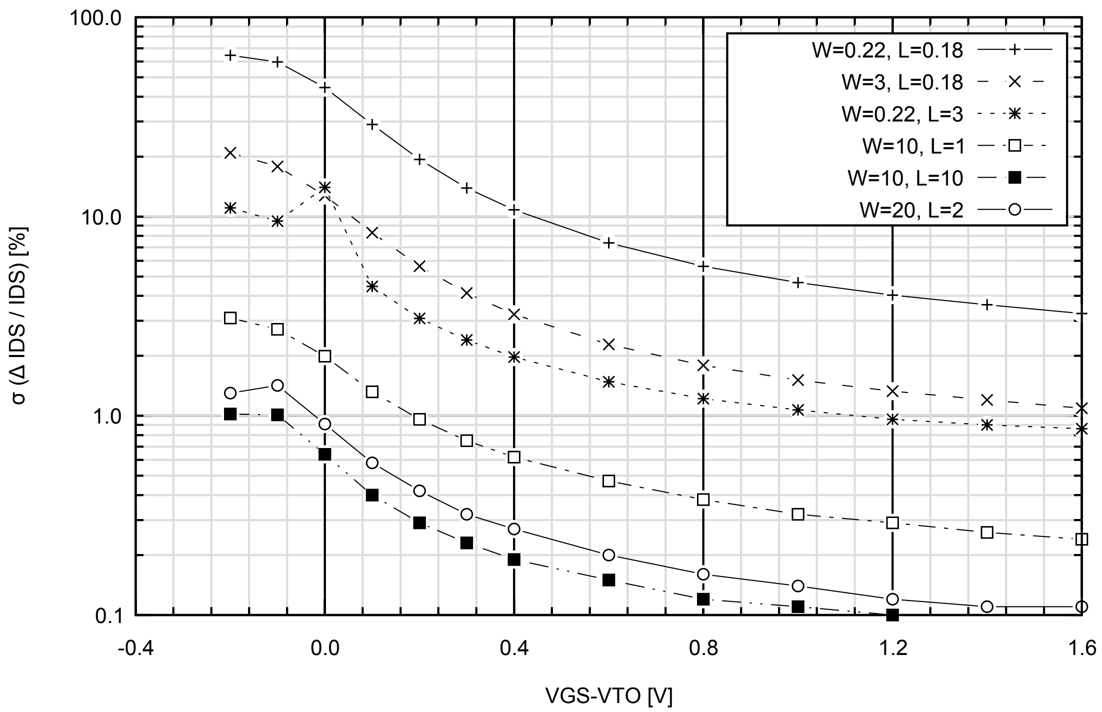

Figure 3.48 Device pesvt: drain current matching vs. VGS-VTO (typical values, drawn W and L)

pesvti

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40 °C to 175 °C	-2.3	-1.98	1.98	2.3	V
VGD	-40 °C to 175 °C	-2.3	-1.98	1.98	2.3	V
VDS	-40 °C to 175 °C	-2.3	-1.98	1.98	2.3	V
VDB	-40 °C to 175 °C	-2.3	-1.98	0	0.5	V
VSB	-40 °C to 175 °C	-2.3	-1.98	0	0.5	V
VBpsub(1	-40 °C to 175 °C	-0.5	0	10	12	V

Note 1 If DNWELL instead of DNWELLMV is used for the isolated PMOS transistors, then max. VBpsub = 45 (50)V.

Note: The node B (BULK) is: NWELL5.

Process parameters

Negative values are considered as absolute values for their limits.

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPESVTIS	drain-source breakdown @ VG=0V, Id=-1µA, L=0.18µm	3.6	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXPESVTI	mobility exponent	-	-	-1.02	-	-	-
FC_PESVTI	corner frequency @ VD=1.8V, Id=1µA, L=10µm, W=10µm	-	-	0.47	-	-	kHz
GA_PESVTI	body factor long channel @ L=10µm, W=10µm	-	-	0.62	-	-	√V
IDSPESVTIS	saturation current @ VG=-1.8V, VD=-1.8V, L=0.18µm, W=10µm	155	205	255	305	355	µA/µm

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Name	Description	LSL	Low	Typ	High	USL	Unit
IOFPESVTIS	off-state leakage @ VD=-1.8V, L=0.18µm, W=10µm	-	-	-	40	-	pA/µm
KP_PESVTI	gain factor long channel @ L=10µm, W=10µm	-	-	58	-	-	µA/V²
LEFPESVTI	effective channel length @ L=0.18µm	-	-	0.13	-	-	µm
NOIPESVTI	Input referred noise @ VD=-1.8V, Id=-1µA, f=1Hz, L=10µm, W=10µm	-	-	14.2	-	-	µV.µm/ √(Hz)
STSPESVTI	subthreshold slope @ VD=-1.8V	-	-	11.4	-	-	decade/V
TC_VTXPESVTI	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	0.81	-	-	mV/K
U0_PESVTI	effective mobility	-	-	67	-	-	cm²/Vs
VTIPESVTIL	threshold voltage long channel @ VD=-0.1V, L=10µm, W=10µm	-0.46	-0.49	-0.52	-0.55	-0.58	V
VTIPESVTIS	threshold voltage short channel @ VD=-0.1V, L=0.18µm, W=10µm	-0.36	-0.42	-0.48	-0.54	-0.6	V
VTIPESVTISS	threshold voltage small channel @ VD=-0.1V, L=0.18µm, W=0.22µm	-	-	-0.48	-	-	V
VTXPESVTIS	extrapolated threshold voltage short channel @ VD=-0.1V, L=0.18µm, W=10µm	-	-	-0.49	-	-	V
WEFPESVTI	effective channel width @ W=0.22µm	-	-	0.25	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTPESVTI	Pelgrom coefficient gain factor mismatch	0.7	%µm
AIDPESVTI00	Pelgrom coefficient ID mismatch @ VG-VT=0V	8.19	%µm
AIDPESVTI01	Pelgrom coefficient ID mismatch @ VG-VT=0.1V	5.14	%µm
AIDPESVTI02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	3.4	%µm
AIDPESVTI04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	1.88	%µm
AIDPESVTI06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	1.32	%µm
AIDPESVTI08	Pelgrom coefficient ID mismatch @ VG-VT=0.8V	1.03	%µm
AIDPESVTI10	Pelgrom coefficient ID mismatch @ VG-VT=1V	0.86	%µm
AIDPESVTI14	Pelgrom coefficient ID mismatch @ VG-VT=1.4V	0.67	%µm
AVTPESVTI	Pelgrom coefficient VT mismatch	4.1	mVµm
DLTPESVTI	transistor delta length	0.05	µm
DWTPESVTI	transistor delta width	-0.03	µm

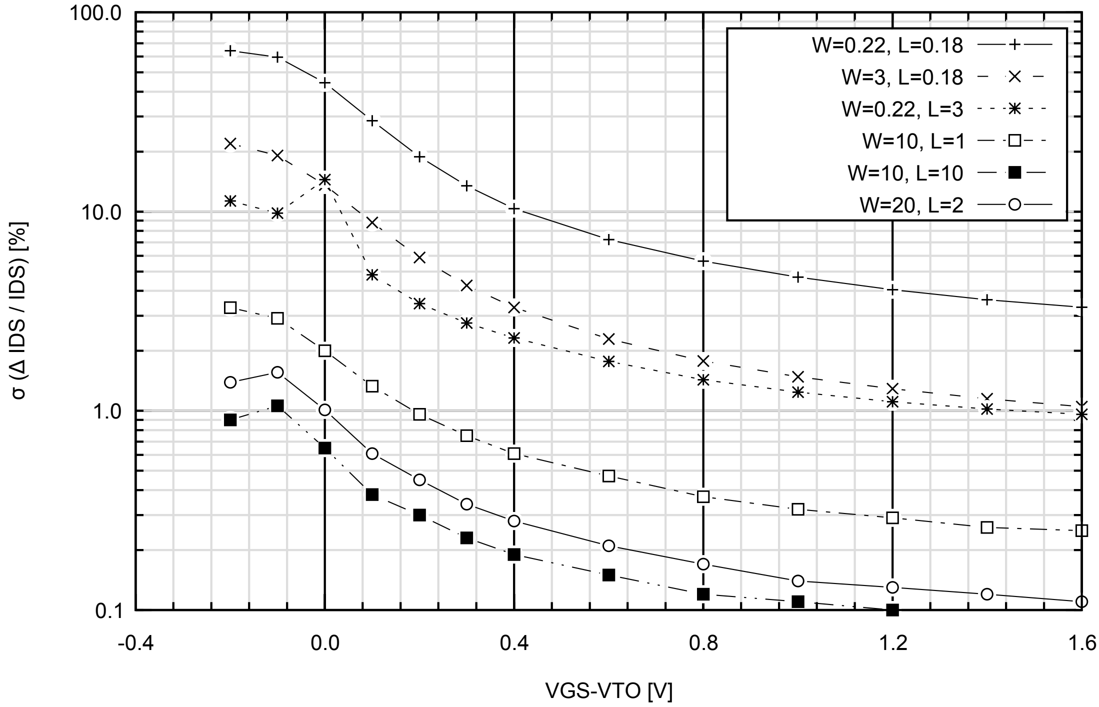

Figure 3.49 Device pesvti: drain current matching vs. VGS-VTO (typical values, drawn W and L)

pesvti_5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40 °C to 175 °C	-2.3	-1.98	1.98	2.3	V
VGD	-40 °C to 175 °C	-2.3	-1.98	1.98	2.3	V
VDS	-40 °C to 175 °C	-2.3	-1.98	1.98	2.3	V
VDB	-40 °C to 175 °C	-2.3	-1.98	0	0.5	V
VSB	-40 °C to 175 °C	-2.3	-1.98	0	0.5	V
VBpsub	-40 °C to 175 °C	-0.5	0	45	50	V

Note: The node B (BULK) is: NWELL5.

Process parameters

Negative values are considered as absolute values for their limits.

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPESVTIS	drain-source breakdown @ VG=0V, Id=-1µA, L=0.18µm	3.6	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXPESVTI	mobility exponent	-	-	-1.02	-	-	-
FC_PESVTI	corner frequency @ VD=1.8V, Id=1µA, L=10µm, W=10µm	-	-	0.47	-	-	kHz
GA_PESVTI	body factor long channel @ L=10µm, W=10µm	-	-	0.62	-	-	√V
IDSPESVTIS	saturation current @ VG=-1.8V, VD=-1.8V, L=0.18µm, W=10µm	155	205	255	305	355	µA/µm

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Name	Description	LSL	Low	Typ	High	USL	Unit
IOFPESVTIS	off-state leakage @ VD=-1.8V, L=0.18µm, W=10µm	-	-	-	40	-	pA/µm
KP_PESVTI	gain factor long channel @ L=10µm, W=10µm	-	-	58	-	-	µA/V²
LEFPESVTI	effective channel length @ L=0.18µm	-	-	0.13	-	-	µm
NOIPESVTI	Input referred noise @ VD=-1.8V, Id=-1µA, f=1Hz, L=10µm, W=10µm	-	-	14.2	-	-	µV.µm/√(Hz)
STSPESVTI	subthreshold slope @ VD=-1.8V	-	-	11.4	-	-	decade/V
TC_VTXPESVTI	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	0.81	-	-	mV/K
U0_PESVTI	effective mobility	-	-	67	-	-	cm²/Vs
VTIPESVTIL	threshold voltage long channel @ VD=-0.1V, L=10µm, W=10µm	-0.46	-0.49	-0.52	-0.55	-0.58	V
VTIPESVTIS	threshold voltage short channel @ VD=-0.1V, L=0.18µm, W=10µm	-0.36	-0.42	-0.48	-0.54	-0.6	V
VTIPESVTISS	threshold voltage small channel @ VD=-0.1V, L=0.18µm, W=0.22µm	-	-	-0.48	-	-	V
VTXPESVTIS	extrapolated threshold voltage short channel @ VD=-0.1V, L=0.18µm, W=10µm	-	-	-0.49	-	-	V
WEFPESVTI	effective channel width @ W=0.22µm	-	-	0.25	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTPESVTI	Pelgrom coefficient gain factor mismatch	0.7	%µm
AIDPESVTI00	Pelgrom coefficient ID mismatch @ VG-VT=0V	8.19	%µm
AIDPESVTI01	Pelgrom coefficient ID mismatch @ VG-VT=0.1V	5.14	%µm
AIDPESVTI02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	3.4	%µm
AIDPESVTI04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	1.88	%µm
AIDPESVTI06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	1.32	%µm
AIDPESVTI08	Pelgrom coefficient ID mismatch @ VG-VT=0.8V	1.03	%µm
AIDPESVTI10	Pelgrom coefficient ID mismatch @ VG-VT=1V	0.86	%µm
AIDPESVTI14	Pelgrom coefficient ID mismatch @ VG-VT=1.4V	0.67	%µm
AVTPESVTI	Pelgrom coefficient VT mismatch	4.1	mVµm
DLTPESVTI	transistor delta length	0.05	µm
DWTPESVTI	transistor delta width	-0.03	µm

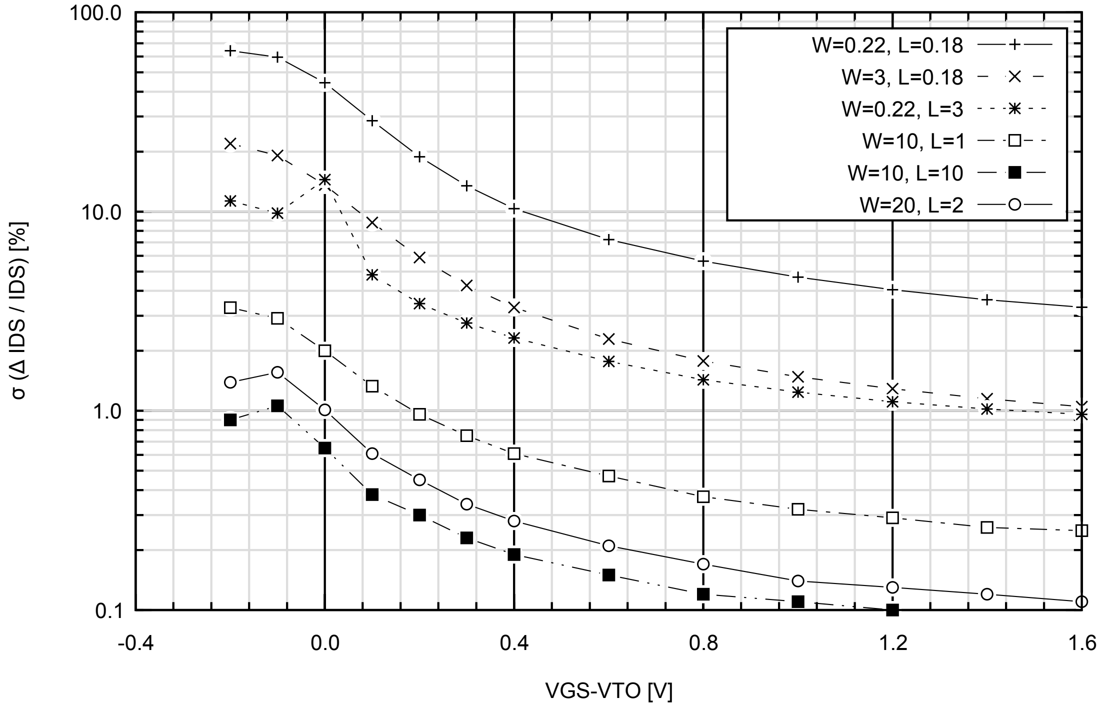

Figure 3.50 Device pesvti: drain current matching vs. VGS-VTO (typical values, drawn W and L)

pesvti_m_5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VGD	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDB	-40°C to 175°C	-2.3	-1.98	0	0.5	V
VSB	-40°C to 175°C	-2.3	-1.98	0	0.5	V
VBpsub	-40°C to 175°C	-0.5	0	10	12	V

Note: The node B (BULK) is: NWELL5.

Process parameters

Negative values are considered as absolute values for their limits.

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPESVTIS	drain-source breakdown @ VG=0V, Id=-1µA, L=0.18µm	3.6	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXPESVTI	mobility exponent	-	-	-1.02	-	-	-
FC_PESVTI	corner frequency @ VD=1.8V, Id=1µA, L=10µm, W=10µm	-	-	0.47	-	-	kHz
GA_PESVTI	body factor long channel @ L=10µm, W=10µm	-	-	0.62	-	-	√V
IDSPESVTIS	saturation current @ VG=-1.8V, VD=-1.8V, L=0.18µm, W=10µm	155	205	255	305	355	µA/µm

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Name	Description	LSL	Low	Typ	High	USL	Unit
IOFPESVTIS	off-state leakage @ VD=-1.8V, L=0.18µm, W=10µm	-	-	-	40	-	pA/µm
KP_PESVTI	gain factor long channel @ L=10µm, W=10µm	-	-	58	-	-	µA/V²
LEFPESVTI	effective channel length @ L=0.18µm	-	-	0.13	-	-	µm
NOIPESVTI	Input referred noise @ VD=-1.8V, Id=-1µA, f=1Hz, L=10µm, W=10µm	-	-	14.2	-	-	µV.µm/√(Hz)
STSPESVTI	subthreshold slope @ VD=-1.8V	-	-	11.4	-	-	decade/V
TC_VTXPESVTI	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	0.81	-	-	mV/K
U0_PESVTI	effective mobility	-	-	67	-	-	cm²/Vs
VTIPESVTIL	threshold voltage long channel @ VD=-0.1V, L=10µm, W=10µm	-0.46	-0.49	-0.52	-0.55	-0.58	V
VTIPESVTIS	threshold voltage short channel @ VD=-0.1V, L=0.18µm, W=10µm	-0.36	-0.42	-0.48	-0.54	-0.6	V
VTIPESVTISS	threshold voltage small channel @ VD=-0.1V, L=0.18µm, W=0.22µm	-	-	-0.48	-	-	V
VTXPESVTIS	extrapolated threshold voltage short channel @ VD=-0.1V, L=0.18µm, W=10µm	-	-	-0.49	-	-	V
WEFPESVTI	effective channel width @ W=0.22µm	-	-	0.25	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTPESVTI	Pelgrom coefficient gain factor mismatch	0.7	%µm
AIDPESVTI00	Pelgrom coefficient ID mismatch @ VG-VT=0V	8.19	%µm
AIDPESVTI01	Pelgrom coefficient ID mismatch @ VG-VT=0.1V	5.14	%µm
AIDPESVTI02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	3.4	%µm
AIDPESVTI04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	1.88	%µm
AIDPESVTI06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	1.32	%µm
AIDPESVTI08	Pelgrom coefficient ID mismatch @ VG-VT=0.8V	1.03	%µm
AIDPESVTI10	Pelgrom coefficient ID mismatch @ VG-VT=1V	0.86	%µm
AIDPESVTI14	Pelgrom coefficient ID mismatch @ VG-VT=1.4V	0.67	%µm
AVTPESVTI	Pelgrom coefficient VT mismatch	4.1	mVµm
DLTPESVTI	transistor delta length	0.05	µm
DWTPESVTI	transistor delta width	-0.03	µm

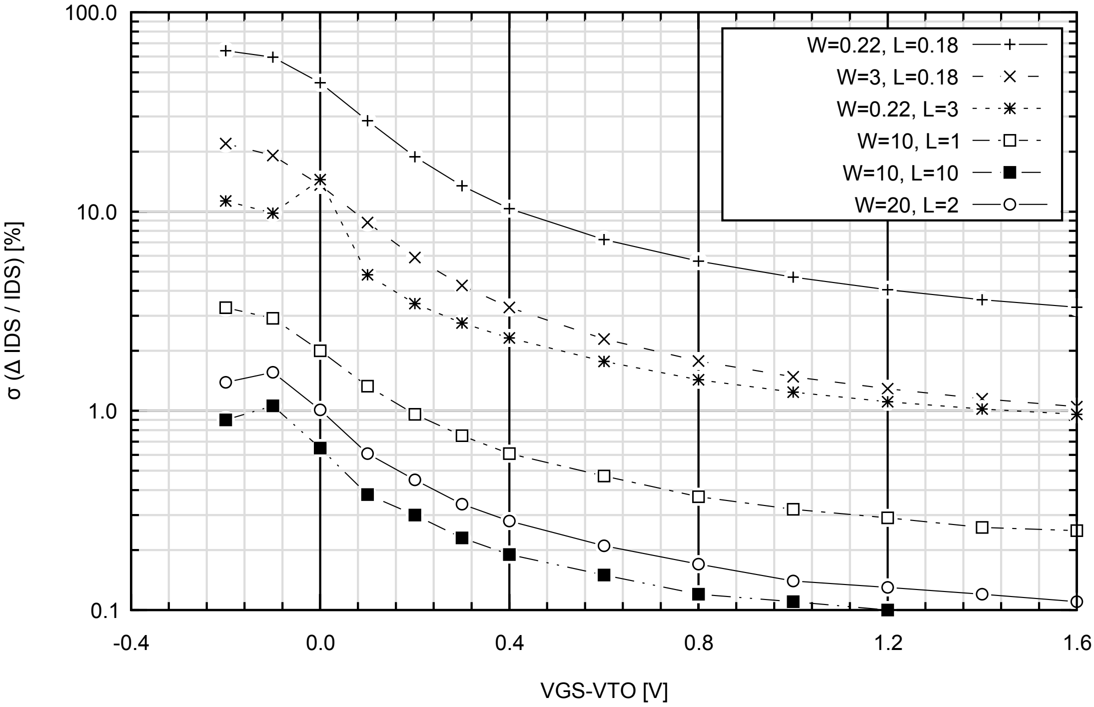

Figure 3.51 Device pesvti: drain current matching vs. VGS-VTO (typical values, drawn W and L)

3.15 LNPMOS3 module

3.15.1 Device independent parameters

Gate oxide parameters

Implementation of the LNPMOS3 module results in changing the gate oxide capacitance only because of different implant conditions. This parameter is not suitable for gate oxide thickness calculation.

Name	Description	LSL	Low	Typ	High	USL	Unit
CGAP3LN	3.3V low noise PMOS gate oxide area capacitance @ Vbias=-3.3V	4.82	5.03	5.26	5.51	5.79	fF/µm²
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						

3.15.2 Device parameters

pe3ln, pe3ln_5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40 °C to 175 °C	-4	-3.6	3.6	4	V
VGD	-40 °C to 175 °C	-4	-3.6	3.6	4	V
VDS	-40 °C to 175 °C	-4	-3.6	3.6	4	V
VDB	-40 °C to 175 °C	-4	-3.6	0	0.5	V
VSB	-40 °C to 175 °C	-4	-3.6	0	0.5	V
VBpsub	-40 °C to 175 °C	-0.5	0	3.6	4	V

Note: The node B (BULK) is: NWELL4.

Process parameters

Negative values are considered as absolute values for their limits.

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPE3LNS	drain-source breakdown @ VG=0V, Id=-1µA, L=0.5µm	5	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXPE3LN	mobility exponent	-	-	-1	-	-	-
FC_PE3LN	corner frequency @ VD=3.3V, Id=1µA, L=10µm, W=10µm	-	-	0.19	-	-	kHz
GAMPE3LN	body factor long channel @ L=10µm, W=10µm	-	-	6.2	-	-	√V
IDSPE3LNS	saturation current @ VG=-3.3V, VD=-3.3V, L=0.5µm	175	212	250	288	325	µA/µm
IOFPE3LNS	off-state leakage @ VD=-3.3V, L=0.5µm, W=10µm	-	-	-	15	-	pA/µm
ISBPE3LNS	bulk current @ VD=-3.3V, L=0.5µm	-	-	0.01	-	-	µA/µm
KP_PE3LN	gain factor long channel @ L=10µm, W=10µm	-	-	62	-	-	µA/V²
LEFPE3LN	effective channel length @ L=0.5µm	-	-	0.46	-	-	µm
NOIPE3LN	Input referred noise @ VD=-3.3V, Id=-1µA, f=1Hz, L=10µm, W=10µm	-	-	5.5	-	-	µV.µm/ √(Hz)
STSPE3LN	subthreshold slope @ VD=-3.3V	-	-	12.3	-	-	decade/V
TC_VTXPE3LN	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	1.5	-	-	mV/K

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Name	Description	LSL	Low	Typ	High	USL	Unit
U0_PE3LN	effective mobility	-	-	118	-	-	cm²/Vs
VTIPE3LNL	threshold voltage long channel @ VD=-0.1V, L=10µm, W=10µm	-0.91	-0.94	-0.97	-1	-1.03	V
VTIPE3LNS	threshold voltage short channel @ VD=-0.1V, L=0.5µm, W=10µm	-0.82	-0.87	-0.92	-0.97	-1.02	V
VTIPE3LNSS	threshold voltage small channel @ VD=-0.1V, L=0.5µm, W=0.22µm	-	-	-0.91	-	-	V
VTXPE3LNS	extrapolated threshold voltage short channel @ VD=-0.1V, L=0.5µm, W=10µm	-	-	-0.92	-	-	V
WEFPE3LN	effective channel width @ W=0.22µm	-	-	0.2	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTPE3LN	Pelgrom coefficient gain factor mismatch	0.82	%µm
AIDPE3LN00	Pelgrom coefficient ID mismatch @ VG-VT=0V	19.8	%µm
AIDPE3LN02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	7.61	%µm
AIDPE3LN04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	4.06	%µm
AIDPE3LN06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	2.7	%µm
AIDPE3LN10	Pelgrom coefficient ID mismatch @ VG-VT=1V	1.61	%µm
AIDPE3LN15	Pelgrom coefficient ID mismatch @ VG-VT=1.5V	1.11	%µm
AIDPE3LN20	Pelgrom coefficient ID mismatch @ VG-VT=2V	0.88	%µm
AIDPE3LN30	Pelgrom coefficient ID mismatch @ VG-VT=3V	0.66	%µm
AVTPE3LN	Pelgrom coefficient VT mismatch	8.6	mVµm
DLTPE3LN	transistor delta length	0.04	µm
DWTPE3LN	transistor delta width	0.02	µm

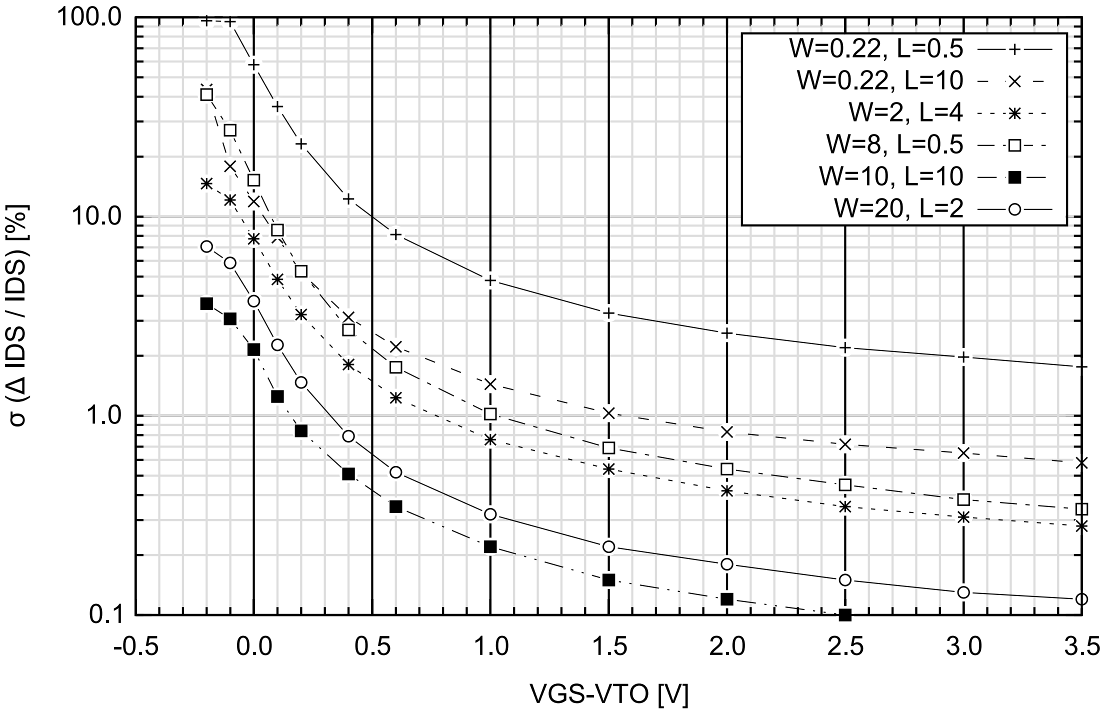

Figure 3.52 Device pe3ln: drain current matching vs. VGS-VTO (typical values, drawn W and L)

pe3lni

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-4	-3.6	3.6	4	V
VGD	-40°C to 175°C	-4	-3.6	3.6	4	V
VDS	-40°C to 175°C	-4	-3.6	3.6	4	V
VDB	-40°C to 175°C	-4	-3.6	0	0.5	V
VSB	-40°C to 175°C	-4	-3.6	0	0.5	V
VBpsub(1	-40°C to 175°C	-0.5	0	10	12	V

Note 1 If DNWELL instead of DNWELLMV is used for the isolated PMOS transistors, then max. VBpsub = 45 (50)V.

Note: The node B (BULK) is: NWELL4.

Process parameters

Negative values are considered as absolute values for their limits.

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPE3LNIS	drain-source breakdown @ VG=0V, Id=-1µA, L=0.5µm	5	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXPE3LNI	mobility exponent	-	-	-1	-	-	-
FC_PE3LNI	corner frequency @ VD=3.3V, Id=1µA, L=10µm, W=10µm	-	-	0.19	-	-	kHz
GAMPE3LNI	body factor long channel @ L=10µm, W=10µm	-	-	6.2	-	-	√V
IDSPE3LNIS	saturation current @ VG=-3.3V, VD=-3.3V, L=0.5µm, W=10µm	175	212	250	288	325	µA/µm

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Name	Description	LSL	Low	Typ	High	USL	Unit
IOFPE3LNIS	off-state leakage @ VD=-3.3V, L=0.5µm, W=10µm	-	-	-	15	-	pA/µm
ISBPE3LNIS	bulk current @ VD=-3.3V, L=0.5µm	-	-	0.01	-	-	µA/µm
KP_PE3LNI	gain factor long channel @ L=10µm, W=10µm	-	-	62	-	-	$\mu A/V^2$
LEFPE3LNI	effective channel length @ L=0.5µm	-	-	0.46	-	-	µm
NOIPE3LNI	Input referred noise @ VD=-3.3V, Id=-1µA, f=1Hz, L=10µm, W=10µm	-	-	5.5	-	-	µV.µm/√(Hz)
STSPE3LNI	subthreshold slope @ VD=-3.3V	-	-	12.3	-	-	decade/V
TC_VTXPE3LNI	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	1.5	-	-	mV/K
U0_PE3LNI	effective mobility	-	-	118	-	-	cm^2/Vs
VTIPE3LNIL	threshold voltage long channel @ VD=-0.1V, L=10µm, W=10µm	-0.91	-0.94	-0.97	-1	-1.03	V
VTIPE3LNIS	threshold voltage short channel @ VD=-0.1V, L=0.5µm, W=10µm	-0.82	-0.87	-0.92	-0.97	-1.02	V
VTIPE3LNISS	threshold voltage small channel @ VD=-0.1V, L=0.5µm, W=0.22µm	-	-	-0.91	-	-	V
VTXPE3LNIS	extrapolated threshold voltage short channel @ VD=-0.1V, L=0.5µm, W=10µm	-	-	-0.92	-	-	V
WEFPE3LNI	effective channel width @ W=0.22µm	-	-	0.2	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTPE3LNI	Pelgrom coefficient gain factor mismatch	0.84	%µm
AIDPE3LNI00	Pelgrom coefficient ID mismatch @ VG-VT=0V	18.7	%µm
AIDPE3LNI02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	7.08	%µm
AIDPE3LNI04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	3.79	%µm
AIDPE3LNI06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	2.56	%µm
AIDPE3LNI10	Pelgrom coefficient ID mismatch @ VG-VT=1V	1.58	%µm
AIDPE3LNI15	Pelgrom coefficient ID mismatch @ VG-VT=1.5V	1.11	%µm
AIDPE3LNI20	Pelgrom coefficient ID mismatch @ VG-VT=2V	0.89	%µm
AIDPE3LNI30	Pelgrom coefficient ID mismatch @ VG-VT=3V	0.66	%µm
AVTPE3LNI	Pelgrom coefficient VT mismatch	8.3	mVµm
DLTPE3LNI	transistor delta length	0.04	µm
DWTPE3LNI	transistor delta width	0.02	µm

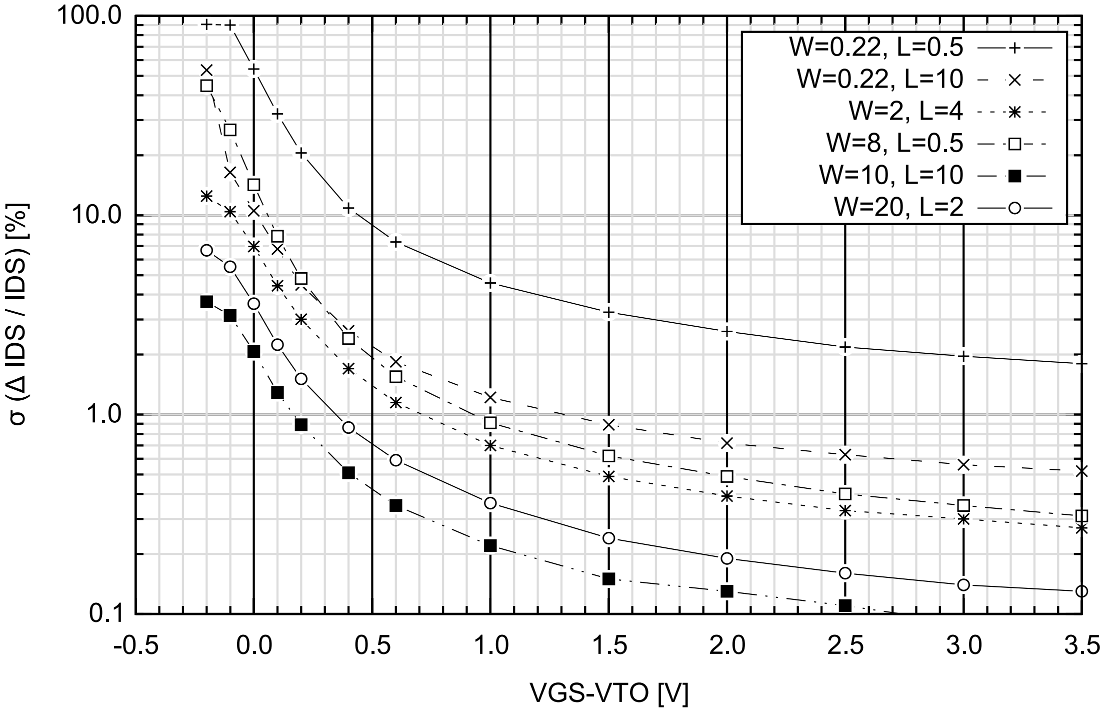

Figure 3.53 Device pe3lni: drain current matching vs. VGS-VTO (typical values, drawn W and L)

pe3lni_5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-4	-3.6	3.6	4	V
VGD	-40°C to 175°C	-4	-3.6	3.6	4	V
VDS	-40°C to 175°C	-4	-3.6	3.6	4	V
VDB	-40°C to 175°C	-4	-3.6	0	0.5	V
VSB	-40°C to 175°C	-4	-3.6	0	0.5	V
VBpsub	-40°C to 175°C	-0.5	0	45	50	V

Note: The node B (BULK) is: NWELL4.

Process parameters

Negative values are considered as absolute values for their limits.

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPE3LNIS	drain-source breakdown @ VG=0V, Id=-1μA, L=0.5μm	5	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXPE3LNI	mobility exponent	-	-	-1	-	-	-
FC_PE3LNI	corner frequency @ VD=3.3V, Id=1μA, L=10μm, W=10μm	-	-	0.19	-	-	kHz
GAMPE3LNI	body factor long channel @ L=10μm, W=10μm	-	-	6.2	-	-	√V
IDSPE3LNIS	saturation current @ VG=-3.3V, VD=-3.3V, L=0.5μm, W=10μm	175	212	250	288	325	μA/μm

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Name	Description	LSL	Low	Typ	High	USL	Unit
IOFPE3LNIS	off-state leakage @ VD=-3.3V, L=0.5µm, W=10µm	-	-	-	15	-	pA/µm
ISBPE3LNIS	bulk current @ VD=-3.3V, L=0.5µm	-	-	0.01	-	-	µA/µm
KP_PE3LNI	gain factor long channel @ L=10µm, W=10µm	-	-	62	-	-	$\mu A/V^2$
LEFPE3LNI	effective channel length @ L=0.5µm	-	-	0.46	-	-	µm
NOIPE3LNI	Input referred noise @ VD=-3.3V, Id=-1µA, f=1Hz, L=10µm, W=10µm	-	-	5.5	-	-	µV.µm/ √(Hz)
STSPE3LNI	subthreshold slope @ VD=-3.3V	-	-	12.3	-	-	decade/V
TC_VTXPE3LNI	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	1.5	-	-	mV/K
U0_PE3LNI	effective mobility	-	-	118	-	-	cm^2/Vs
VTIPE3LNIL	threshold voltage long channel @ VD=-0.1V, L=10µm, W=10µm	-0.91	-0.94	-0.97	-1	-1.03	V
VTIPE3LNIS	threshold voltage short channel @ VD=-0.1V, L=0.5µm, W=10µm	-0.82	-0.87	-0.92	-0.97	-1.02	V
VTIPE3LNISS	threshold voltage small channel @ VD=-0.1V, L=0.5µm, W=0.22µm	-	-	-0.91	-	-	V
VTXPE3LNIS	extrapolated threshold voltage short channel @ VD=-0.1V, L=0.5µm, W=10µm	-	-	-0.92	-	-	V
WEFPE3LNI	effective channel width @ W=0.22µm	-	-	0.2	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTPE3LNI	Pelgrom coefficient gain factor mismatch	0.84	%µm
AIDPE3LNI00	Pelgrom coefficient ID mismatch @ VG-VT=0V	18.7	%µm
AIDPE3LNI02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	7.08	%µm
AIDPE3LNI04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	3.79	%µm
AIDPE3LNI06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	2.56	%µm
AIDPE3LNI10	Pelgrom coefficient ID mismatch @ VG-VT=1V	1.58	%µm
AIDPE3LNI15	Pelgrom coefficient ID mismatch @ VG-VT=1.5V	1.11	%µm
AIDPE3LNI20	Pelgrom coefficient ID mismatch @ VG-VT=2V	0.89	%µm
AIDPE3LNI30	Pelgrom coefficient ID mismatch @ VG-VT=3V	0.66	%µm
AVTPE3LNI	Pelgrom coefficient VT mismatch	8.3	mVµm
DLTPE3LNI	transistor delta length	0.04	µm
DWTPE3LNI	transistor delta width	0.02	µm

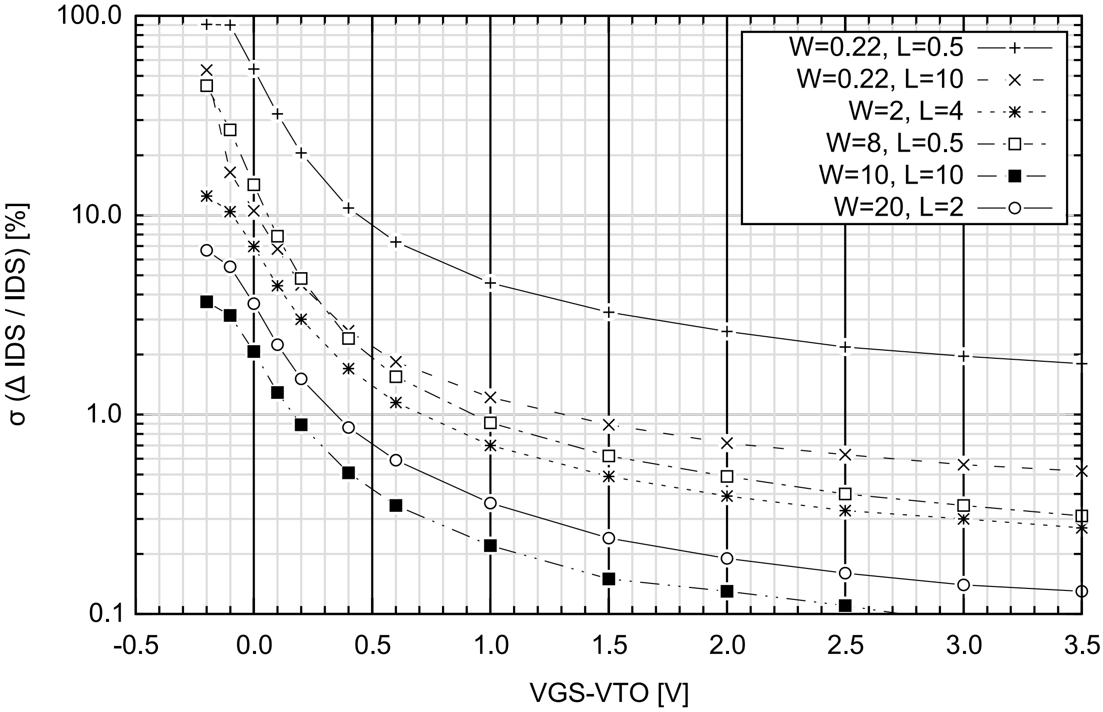

Figure 3.54 Device pe3lni: drain current matching vs. VGS-VTO (typical values, drawn W and L)

pe3lni_m_5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-4	-3.6	3.6	4	V
VGD	-40°C to 175°C	-4	-3.6	3.6	4	V
VDS	-40°C to 175°C	-4	-3.6	3.6	4	V
VDB	-40°C to 175°C	-4	-3.6	0	0.5	V
VSB	-40°C to 175°C	-4	-3.6	0	0.5	V
VBpsub	-40°C to 175°C	-0.5	0	10	12	V

Note: The node B (BULK) is: NWELL4.

Process parameters

Negative values are considered as absolute values for their limits.

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPE3LNIS	drain-source breakdown @ VG=0V, Id=-1μA, L=0.5μm	5	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXPE3LNI	mobility exponent	-	-	-1	-	-	-
FC_PE3LNI	corner frequency @ VD=3.3V, Id=1μA, L=10μm, W=10μm	-	-	0.19	-	-	kHz
GAMPE3LNI	body factor long channel @ L=10μm, W=10μm	-	-	6.2	-	-	√V
IDSPE3LNIS	saturation current @ VG=-3.3V, VD=-3.3V, L=0.5μm, W=10μm	175	212	250	288	325	μA/μm

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Name	Description	LSL	Low	Typ	High	USL	Unit
IOFPE3LNIS	off-state leakage @ VD=-3.3V, L=0.5µm, W=10µm	-	-	-	15	-	pA/µm
ISBPE3LNIS	bulk current @ VD=-3.3V, L=0.5µm	-	-	0.01	-	-	µA/µm
KP_PE3LNI	gain factor long channel @ L=10µm, W=10µm	-	-	62	-	-	µA/V²
LEFPE3LNI	effective channel length @ L=0.5µm	-	-	0.46	-	-	µm
NOIPE3LNI	Input referred noise @ VD=-3.3V, Id=-1µA, f=1Hz, L=10µm, W=10µm	-	-	5.5	-	-	µV.µm/ √(Hz)
STSPE3LNI	subthreshold slope @ VD=-3.3V	-	-	12.3	-	-	decade/V
TC_VTXPE3LNI	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	1.5	-	-	mV/K
U0_PE3LNI	effective mobility	-	-	118	-	-	cm²/Vs
VTIPE3LNIL	threshold voltage long channel @ VD=-0.1V, L=10µm, W=10µm	-0.91	-0.94	-0.97	-1	-1.03	V
VTIPE3LNIS	threshold voltage short channel @ VD=-0.1V, L=0.5µm, W=10µm	-0.82	-0.87	-0.92	-0.97	-1.02	V
VTIPE3LNISS	threshold voltage small channel @ VD=-0.1V, L=0.5µm, W=0.22µm	-	-	-0.91	-	-	V
VTXPE3LNIS	extrapolated threshold voltage short channel @ VD=-0.1V, L=0.5µm, W=10µm	-	-	-0.92	-	-	V
WEFPE3LNI	effective channel width @ W=0.22µm	-	-	0.2	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTPE3LNI	Pelgrom coefficient gain factor mismatch	0.84	%µm
AIDPE3LNI00	Pelgrom coefficient ID mismatch @ VG-VT=0V	18.7	%µm
AIDPE3LNI02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	7.08	%µm
AIDPE3LNI04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	3.79	%µm
AIDPE3LNI06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	2.56	%µm
AIDPE3LNI10	Pelgrom coefficient ID mismatch @ VG-VT=1V	1.58	%µm
AIDPE3LNI15	Pelgrom coefficient ID mismatch @ VG-VT=1.5V	1.11	%µm
AIDPE3LNI20	Pelgrom coefficient ID mismatch @ VG-VT=2V	0.89	%µm
AIDPE3LNI30	Pelgrom coefficient ID mismatch @ VG-VT=3V	0.66	%µm
AVTPE3LNI	Pelgrom coefficient VT mismatch	8.3	mVµm
DLTPE3LNI	transistor delta length	0.04	µm
DWTPE3LNI	transistor delta width	0.02	µm

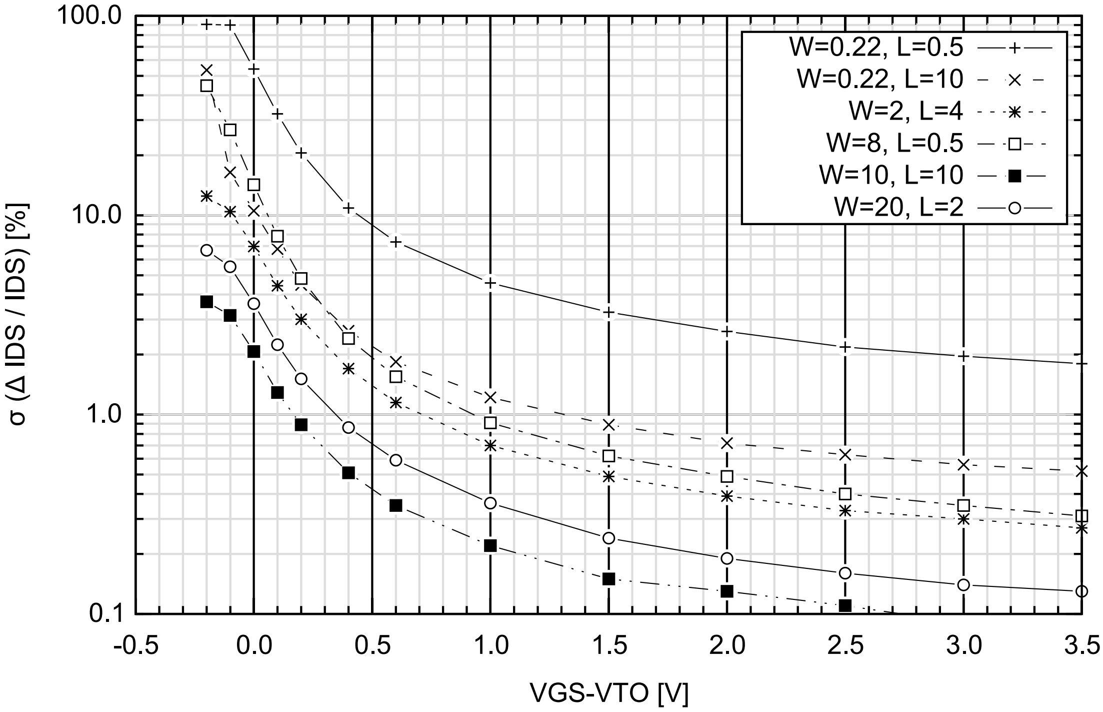

Figure 3.55 Device pe3lni: drain current matching vs. VGS-VTO (typical values, drawn W and L)

3.16 ULN module

3.16.1 Device parameters

nelna

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VGD	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDB	-40°C to 175°C	-0.5	0	1.98	2.3	V
VSB	-40°C to 175°C	-0.5	0	1.98	2.3	V

Note: The node B (BULK) is: PWELL1.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNELNAS	drain-source breakdown @ VG=0V, Id=1µA, L=0.18µm	3.6	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXNELNA	mobility exponent	-	-	-1.6	-	-	-
FC_NELNA	corner frequency @ VD=1.8V, Id=1µA, L=10µm, W=10µm	-	-	0.27	-	-	kHz
GA_NELNA	body factor long channel @ L=10µm, W=10µm	-	-	0.77	-	-	√V
IDSNELNAS	saturation current @ VG=1.8V, VD=1.8V, L=0.18µm, W=10µm	292	376	460	544	628	µA/µm
IOFNELNAS	off-state leakage @ VD=1.8V, L=0.18µm, W=10µm	-	-	-	3	-	pA/µm
ISBNELNAS	bulk current @ VD=1.8V, L=0.18µm	-	-	0.06	-	-	µA/µm
KP_NELNA	gain factor long channel @ L=10µm, W=10µm	-	-	223	-	-	µA/V²
LEFNELNA	effective channel length @ L=0.18µm	-	-	0.15	-	-	µm
NOINELNA	Input referred noise @ VD=1.8V, Id=1µA, f=1Hz, L=10µm, W=10µm	-	-	7.8	-	-	µV.µm/√(Hz)
STSNELNA	subthreshold slope @ VD=1.8V	-	-	11.7	-	-	decade/V
TC_VTXNELNA	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	-0.87	-	-	mV/K
U0_NELNA	effective mobility	-	-	310	-	-	cm²/Vs
VTINELNAL	threshold voltage long channel @ VD=0.1V, L=10µm, W=10µm	0.52	0.55	0.58	0.61	0.64	V
VTINELNAS	threshold voltage short channel @ VD=0.1V, L=0.18µm, W=10µm	0.47	0.54	0.61	0.68	0.75	V
VTINELNASS	threshold voltage small channel @ VD=0.1V, L=0.18µm, W=0.22µm	-	-	0.48	-	-	V
VTXNELNAS	extrapolated threshold voltage short channel @ VD=0.1V, L=0.18µm, W=10µm	-	-	0.68	-	-	V
WEFNELNA	effective channel width @ W=0.22µm	-	-	0.17	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTNELNA	Pelgrom coefficient gain factor mismatch	0.69	%µm
AIDNELNA00	Pelgrom coefficient ID mismatch @ VG-VT=0V	7.64	%µm
AIDNELNA01	Pelgrom coefficient ID mismatch @ VG-VT=0.1V	5.3	%µm
AIDNELNA02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	3.79	%µm
AIDNELNA04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	2.19	%µm
AIDNELNA06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	1.49	%µm
AIDNELNA08	Pelgrom coefficient ID mismatch @ VG-VT=0.8V	1.12	%µm
AIDNELNA10	Pelgrom coefficient ID mismatch @ VG-VT=1V	0.91	%µm
AIDNELNA14	Pelgrom coefficient ID mismatch @ VG-VT=1.4V	0.69	%µm
AVTNELNA	Pelgrom coefficient VT mismatch	5.76	mVµm
DLTNELNA	transistor delta length	0.03	µm
DWTNELNA	transistor delta width	0.05	µm

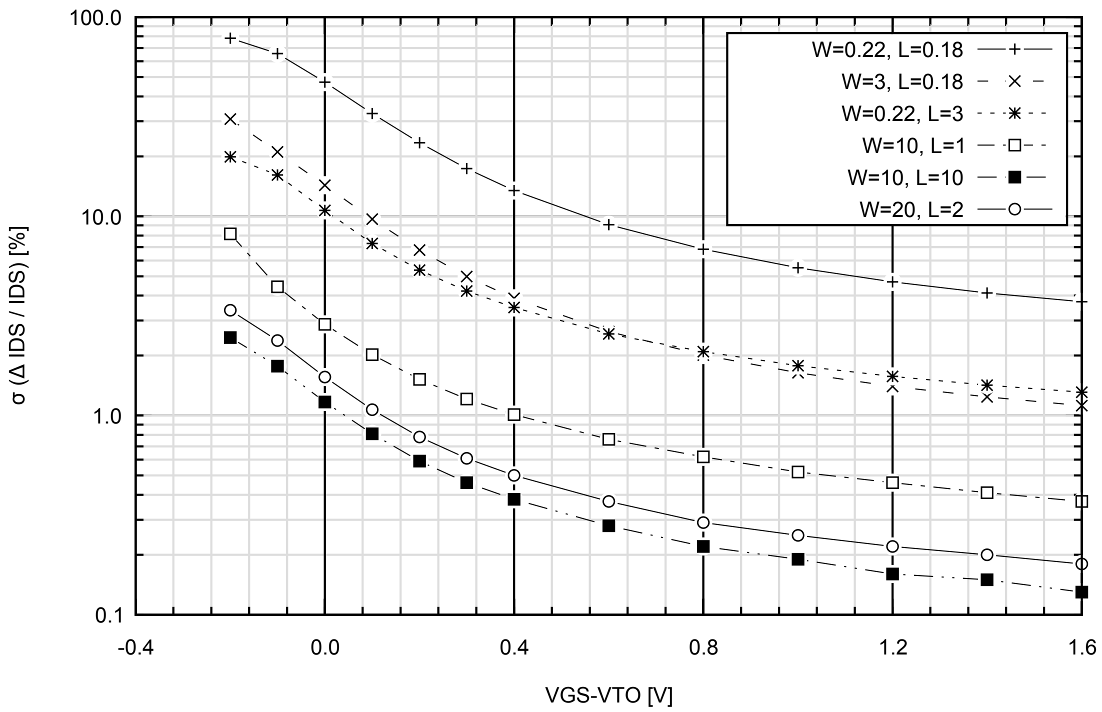

Figure 3.56 Device nelna: drain current matching vs. VGS-VTO (typical values, drawn W and L)

nelnai

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VGD	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDB	-40°C to 175°C	-0.5	0	1.98	2.3	V
VSB	-40°C to 175°C	-0.5	0	1.98	2.3	V

Note: The node B (BULK) is: PWELL1.

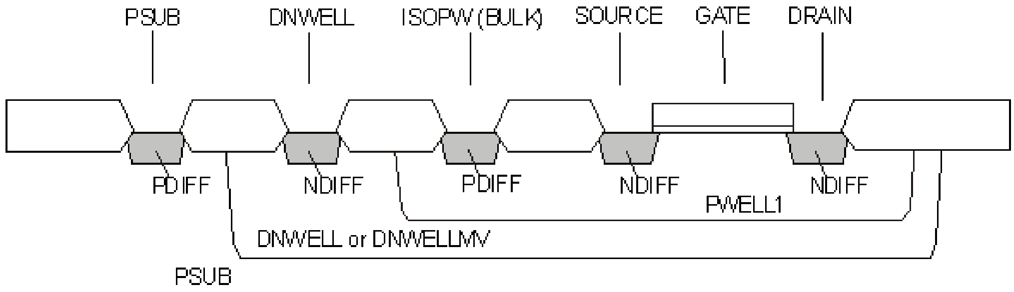

Figure 3.57 Additional Operating Conditions

Note: nelnai in DNWELL

$$
\begin{array}{lclcl}
V_{PSUB} & \leq & V_{DNWELL} & \leq & V_{PSUB} + 45(50)V \\
V_{DNWELL} - 8(10)V & \leq & V_{PWELL1} & \leq & V_{DNWELL}
\end{array}
$$

nelnai in DNWELLMV

$$
\begin{array}{lclcl}
V_{PSUB} & \leq & V_{DNWELL} & \leq & V_{PSUB} + 10(12)V \\
V_{DNWELLMV} - 8(10)V & \leq & V_{PWELL1} & \leq & V_{DNWELLMV}
\end{array}
$$

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNELNAIS	drain-source breakdown @ VG=0V, Id=1µA, L=0.18µm	3.6	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXNELNAI	mobility exponent	-	-	-1.6	-	-	-
FC_NELNAI	corner frequency @ VD=1.8V, Id=1µA, L=10µm, W=10µm	-	-	0.27	-	-	kHz
GA_NELNAI	body factor long channel @ L=10µm, W=10µm	-	-	0.63	-	-	√V
IDSNELNAIS	saturation current @ VG=1.8V, VD=1.8V, L=0.18µm, W=10µm	292	376	460	544	628	µA/µm
IOFNELNAIS	off-state leakage @ VD=1.8V, L=0.18µm, W=10µm	-	-	-	3	-	pA/µm
ISBNELNAIS	bulk current @ VD=1.8V, L=0.18µm	-	-	0.06	-	-	µA/µm
KP_NELNAI	gain factor long channel @ L=10µm, W=10µm	-	-	226	-	-	µA/V²
LEFNELNAI	effective channel length @ L=0.18µm	-	-	0.14	-	-	µm
NOINELNAI	Input referred noise @ VD=1.8V, Id=1µA, f=1Hz, L=10µm, W=10µm	-	-	7.8	-	-	µV.µm/√(Hz)
STSNELNAI	subthreshold slope @ VD=1.8V	-	-	11.7	-	-	decade/V
TC_VTXNELNAI	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	-0.87	-	-	mV/K
U0_NELNAI	effective mobility	-	-	323	-	-	cm²/Vs
VTINELNAIL	threshold voltage long channel @ VD=0.1V, L=10µm, W=10µm	0.51	0.54	0.57	0.6	0.63	V

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3. Parameters → 3.16 ULN module→ 3.16.1 Device parameters→ nelnai→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
VTINELNAIS	threshold voltage short channel @ VD=0.1V, L=0.18µm, W=10µm	0.46	0.53	0.6	0.67	0.74	V
VTINELNAISS	threshold voltage small channel @ VD=0.1V, L=0.18µm, W=0.22µm	-	-	0.49	-	-	V
VTXNELNAIS	extrapolated threshold voltage short channel @ VD=0.1V, L=0.18µm, W=10µm	-	-	0.69	-	-	V
WEFNELNAI	effective channel width @ W=0.22µm	-	-	0.17	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTNELNAI	Pelgrom coefficient gain factor mismatch	0.62	%µm
AIDNELNAI00	Pelgrom coefficient ID mismatch @ VG-VT=0V	7.71	%µm
AIDNELNAI01	Pelgrom coefficient ID mismatch @ VG-VT=0.1V	5.35	%µm
AIDNELNAI02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	3.74	%µm
AIDNELNAI04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	2.09	%µm
AIDNELNAI06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	1.39	%µm
AIDNELNAI08	Pelgrom coefficient ID mismatch @ VG-VT=0.8V	1.04	%µm
AIDNELNAI10	Pelgrom coefficient ID mismatch @ VG-VT=1V	0.84	%µm
AIDNELNAI14	Pelgrom coefficient ID mismatch @ VG-VT=1.4V	0.62	%µm
AVTNELNAI	Pelgrom coefficient VT mismatch	5.79	mVµm
DLTNELNAI	transistor delta length	0.04	µm
DWTNELNAI	transistor delta width	0.05	µm

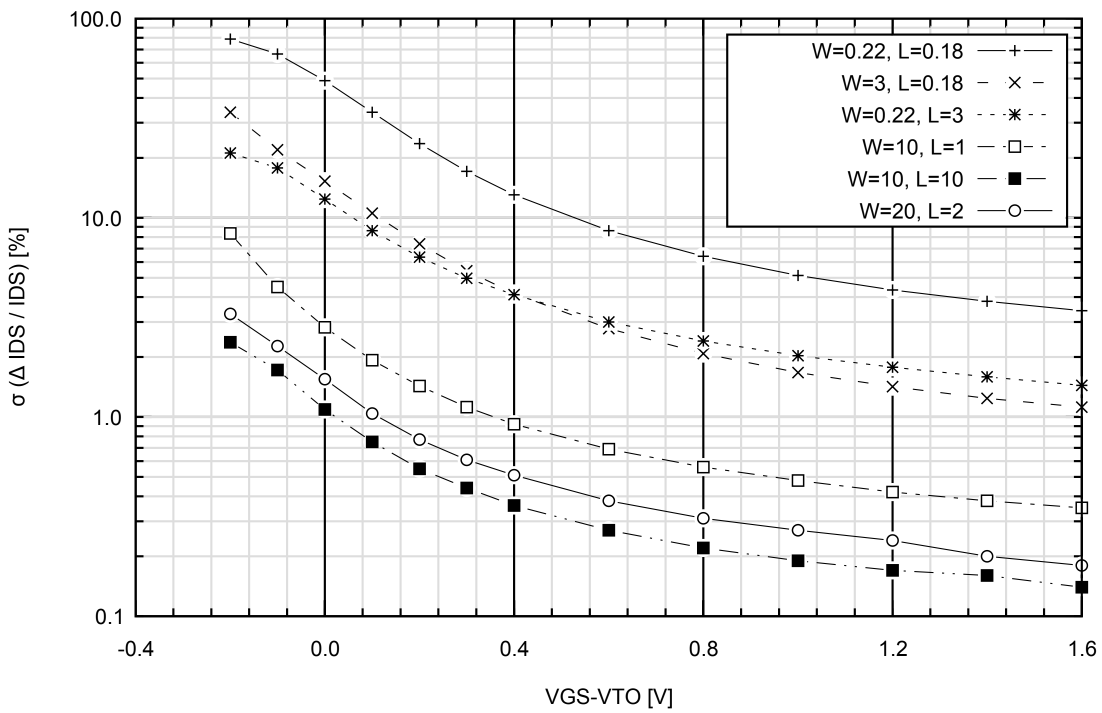

Figure 3.58 Device nelnai: drain current matching vs. VGS-VTO (typical values, drawn W and L)

nelnai_6

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VGD	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDB	-40°C to 175°C	-0.5	0	1.98	2.3	V
VSB	-40°C to 175°C	-0.5	0	1.98	2.3	V
VIpsub	-40°C to 175°C	-0.5	0	45	50	V
VIB	-40°C to 175°C	-0.5	0	8	10	V

Note: The node B (BULK) is: PWELL1.

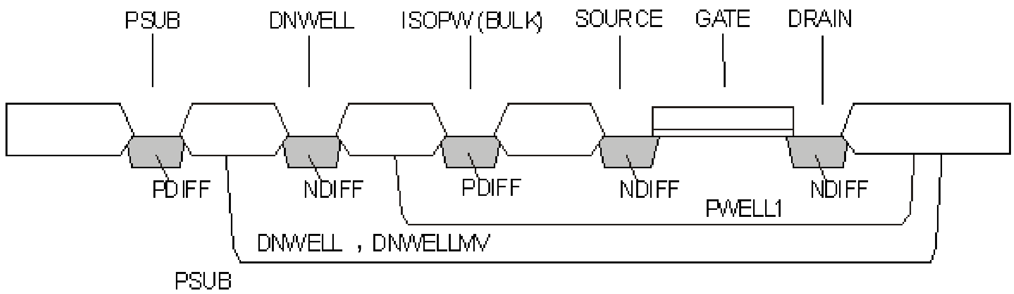

Figure 3.59 Additional Operating Conditions

Note: nelnai_6 in DNWELL

$$\begin{aligned} V_{PSUB} &\leq V_{DNWELL} \leq V_{PSUB} + 45(50)V \\ V_{DNWELL} - 8(10)V &\leq V_{PWELL1} \leq V_{DNWELL} \end{aligned}$$

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNELNAIS	drain-source breakdown @ VG=0V, Id=1µA, L=0.18µm	3.6	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXNELNAI	mobility exponent	-	-	-1.6	-	-	-
FC_NELNAI	corner frequency @ VD=1.8V, Id=1µA, L=10µm, W=10µm	-	-	0.27	-	-	kHz
GA_NELNAI	body factor long channel @ L=10µm, W=10µm	-	-	0.63	-	-	√V
IDSNELNAIS	saturation current @ VG=1.8V, VD=1.8V, L=0.18µm, W=10µm	292	376	460	544	628	µA/µm
IOFNELNAIS	off-state leakage @ VD=1.8V, L=0.18µm, W=10µm	-	-	-	3	-	pA/µm
ISBNELNAIS	bulk current @ VD=1.8V, L=0.18µm	-	-	0.06	-	-	µA/µm
KP_NELNAI	gain factor long channel @ L=10µm, W=10µm	-	-	226	-	-	µA/V²
LEFNELNAI	effective channel length @ L=0.18µm	-	-	0.14	-	-	µm

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Name	Description	LSL	Low	Typ	High	USL	Unit
NOINELNAI	Input referred noise @ VD=1.8V, Id=1µA, f=1Hz, L=10µm, W=10µm	-	-	7.8	-	-	µV.µm/√(Hz)
STSNELNAI	subthreshold slope @ VD=1.8V	-	-	11.7	-	-	decade/V
TC_VTXNELNAI	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	-0.87	-	-	mV/K
U0_NELNAI	effective mobility	-	-	323	-	-	cm^2/Vs
VTINELNAIL	threshold voltage long channel @ VD=0.1V, L=10µm, W=10µm	0.51	0.54	0.57	0.6	0.63	V
VTINELNAIS	threshold voltage short channel @ VD=0.1V, L=0.18µm, W=10µm	0.46	0.53	0.6	0.67	0.74	V
VTINELNAISS	threshold voltage small channel @ VD=0.1V, L=0.18µm, W=0.22µm	-	-	0.49	-	-	V
VTXNELNAIS	extrapolated threshold voltage short channel @ VD=0.1V, L=0.18µm, W=10µm	-	-	0.69	-	-	V
WEFNELNAI	effective channel width @ W=0.22µm	-	-	0.17	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTNELNAI	Pelgrom coefficient gain factor mismatch	0.62	%µm
AIDNELNAI00	Pelgrom coefficient ID mismatch @ VG-VT=0V	7.71	%µm
AIDNELNAI01	Pelgrom coefficient ID mismatch @ VG-VT=0.1V	5.35	%µm
AIDNELNAI02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	3.74	%µm
AIDNELNAI04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	2.09	%µm
AIDNELNAI06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	1.39	%µm
AIDNELNAI08	Pelgrom coefficient ID mismatch @ VG-VT=0.8V	1.04	%µm
AIDNELNAI10	Pelgrom coefficient ID mismatch @ VG-VT=1V	0.84	%µm
AIDNELNAI14	Pelgrom coefficient ID mismatch @ VG-VT=1.4V	0.62	%µm
AVTNELNAI	Pelgrom coefficient VT mismatch	5.79	mVµm
DLTNELNAI	transistor delta length	0.04	µm
DWTNELNAI	transistor delta width	0.05	µm

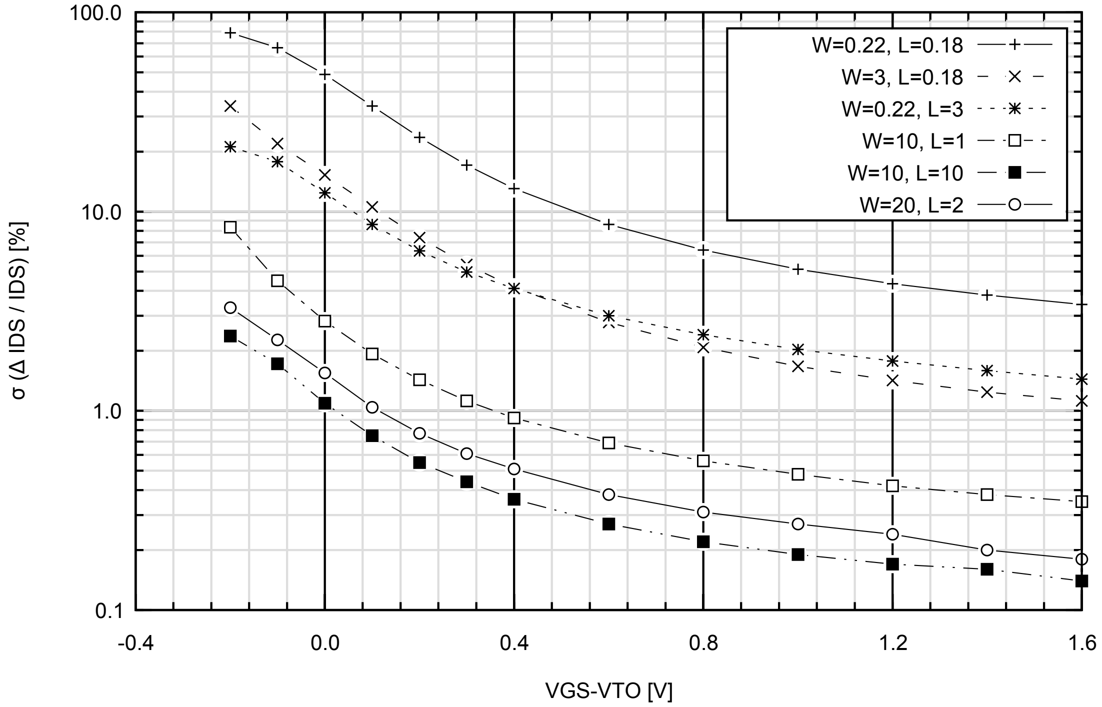

Figure 3.60 Device nelnai: drain current matching vs. VGS-VTO (typical values, drawn W and L)

nelnai_m_6

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VGD	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDB	-40°C to 175°C	-0.5	0	1.98	2.3	V
VSB	-40°C to 175°C	-0.5	0	1.98	2.3	V
VIpsub	-40°C to 175°C	-0.5	0	10	12	V
VIB	-40°C to 175°C	-0.5	0	8	10	V

Note: The node B (BULK) is: PWELL1.

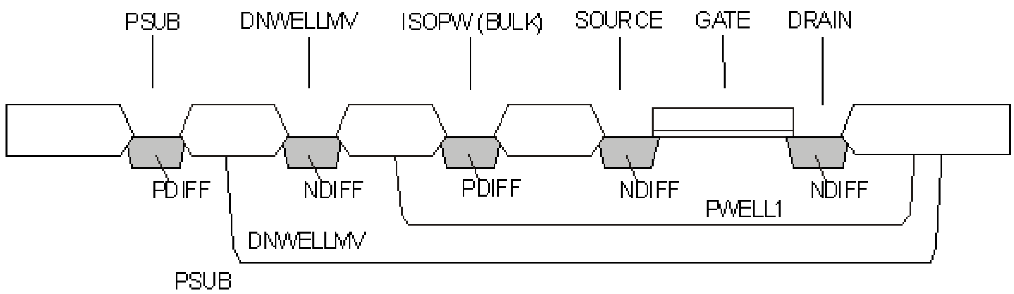

Figure 3.61 Additional Operating Conditions

Note: nelnai_m_6 in DNWELLMV

$$\begin{array}{lcccl} V_{PSUB} & \leq & V_{DNWELL} & \leq & V_{PSUB} + 10(12)V \\ V_{DNWELLMV} - 8(10)V & \leq & V_{PWELL1} & \leq & V_{DNWELLMV} \end{array}$$

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNELNAIS	drain-source breakdown @ VG=0V, Id=1μA, L=0.18μm	3.6	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXNELNAI	mobility exponent	-	-	-1.6	-	-	-
FC_NELNAI	corner frequency @ VD=1.8V, Id=1μA, L=10μm, W=10μm	-	-	0.27	-	-	kHz
GA_NELNAI	body factor long channel @ L=10μm, W=10μm	-	-	0.63	-	-	√V
IDSNELNAIS	saturation current @ VG=1.8V, VD=1.8V, L=0.18μm, W=10μm	292	376	460	544	628	μA/μm
IOFNELNAIS	off-state leakage @ VD=1.8V, L=0.18μm, W=10μm	-	-	-	3	-	pA/μm
ISBNELNAIS	bulk current @ VD=1.8V, L=0.18μm	-	-	0.06	-	-	μA/μm
KP_NELNAI	gain factor long channel @ L=10μm, W=10μm	-	-	226	-	-	μA/V²
LEFNELNAI	effective channel length @ L=0.18μm	-	-	0.14	-	-	μm
NOINELNAI	Input referred noise @ VD=1.8V, Id=1μA, f=1Hz, L=10μm, W=10μm	-	-	7.8	-	-	μV.μm/√(Hz)
STSNELNAI	subthreshold slope @ VD=1.8V	-	-	11.7	-	-	decade/V
TC_VTXNELNAI	threshold voltage temperature coefficient @ L=10μm, W=10μm	-	-	-0.87	-	-	mV/K
U0_NELNAI	effective mobility	-	-	323	-	-	cm²/Vs
VTINELNAIL	threshold voltage long channel @ VD=0.1V, L=10μm, W=10μm	0.51	0.54	0.57	0.6	0.63	V
VTINELNAIS	threshold voltage short channel @ VD=0.1V, L=0.18μm, W=10μm	0.46	0.53	0.6	0.67	0.74	V
VTINELNAISS	threshold voltage small channel @ VD=0.1V, L=0.18μm, W=0.22μm	-	-	0.49	-	-	V
VTXNELNAIS	extrapolated threshold voltage short channel @ VD=0.1V, L=0.18μm, W=10μm	-	-	0.69	-	-	V
WEFNELNAI	effective channel width @ W=0.22μm	-	-	0.17	-	-	μm

Matching parameters

Name	Description	Typ	Unit
ABTNELNAI	Pelgrom coefficient gain factor mismatch	0.62	%μm
AIDNELNAI00	Pelgrom coefficient ID mismatch @ VG-VT=0V	7.71	%μm
AIDNELNAI01	Pelgrom coefficient ID mismatch @ VG-VT=0.1V	5.35	%μm
AIDNELNAI02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	3.74	%μm
AIDNELNAI04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	2.09	%μm
AIDNELNAI06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	1.39	%μm
AIDNELNAI08	Pelgrom coefficient ID mismatch @ VG-VT=0.8V	1.04	%μm

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Name	Description	Typ	Unit
AIDNELNAI10	Pelgrom coefficient ID mismatch @ VG-VT=1V	0.84	%µm
AIDNELNAI14	Pelgrom coefficient ID mismatch @ VG-VT=1.4V	0.62	%µm
AVTNELNAI	Pelgrom coefficient VT mismatch	5.79	mVµm
DLTNELNAI	transistor delta length	0.04	µm
DWTNELNAI	transistor delta width	0.05	µm

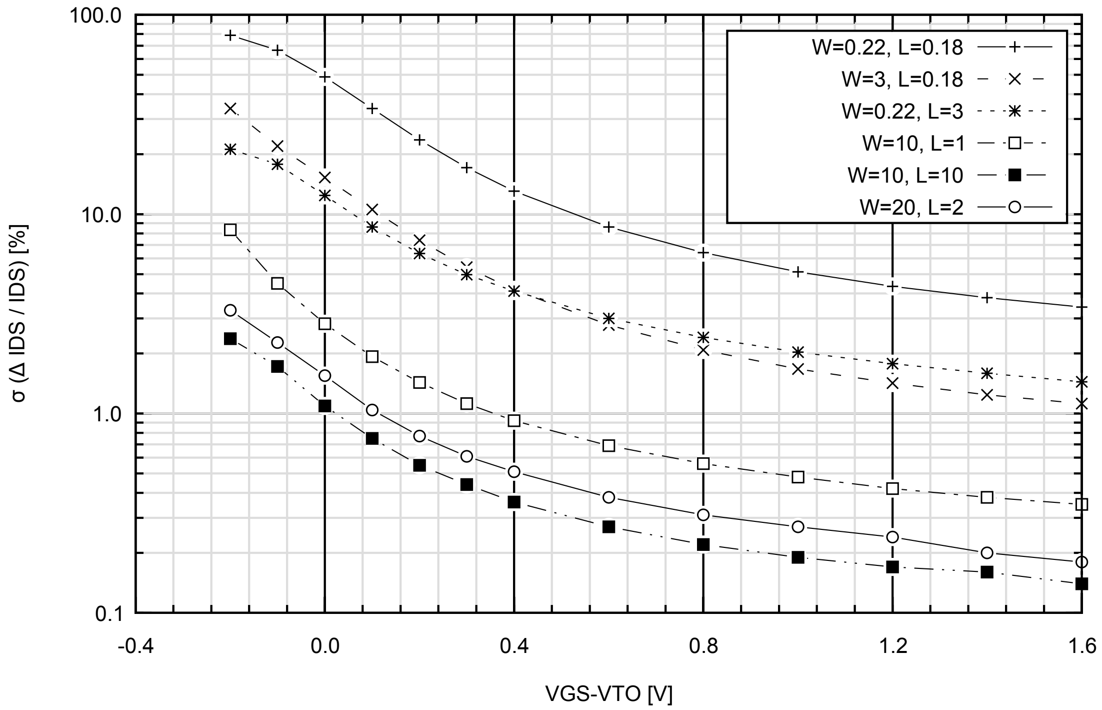

Figure 3.62 Device nelnai: drain current matching vs. VGS-VTO (typical values, drawn W and L)

ne3lna

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-4	-3.6	3.6	4	V
VGD	-40°C to 175°C	-4	-3.6	3.6	4	V
VDS	-40°C to 175°C	-4	-3.6	3.6	4	V
VDB	-40°C to 175°C	-0.5	0	3.6	4	V
VSB	-40°C to 175°C	-0.5	0	3.6	4	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNE3LNAS	drain-source breakdown @ VG=0V, Id=1µA, L=0.35µm	5	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXNE3LNA	mobility exponent	-	-	-1.82	-	-	-
FC_NE3LNA	corner frequency @ VD=3.3V, Id=1µA, L=10µm, W=10µm	-	-	0.41	-	-	kHz
GA_NE3LNA	body factor long channel @ L=10µm, W=10µm	-	-	1.6	-	-	√V

⇒

Name	Description	LSL	Low	Typ	High	USL	Unit
IDSNE3LNAS	saturation current @ VG=3.3V, VD=3.3V, L=0.35µm, W=10µm	490	535	580	625	670	µA/µm
IOFNE3LNAS	off-state leakage @ VD=3.3V, L=0.35µm, W=10µm	-	-	-	3	-	pA/µm
ISBNE3LNAS	bulk current @ VD=3.3V, L=0.35µm	-	-	1.08	-	-	µA/µm
KP_NE3LNA	gain factor long channel @ L=10µm, W=10µm	-	-	180	-	-	µA/V²
LEFNE3LNA	effective channel length @ L=0.35µm	-	-	0.31	-	-	µm
NOINE3LNA	Input referred noise @ VD=3.3V, Id=1µA, f=1Hz, L=10µm, W=10µm	-	-	9.2	-	-	µV.µm/√(Hz)
STSNE3LNA	subthreshold slope @ VD=3.3V	-	-	10.1	-	-	decade/V
TC_VTXNE3LNA	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	-1.1	-	-	mV/K
U0_NE3LNA	effective mobility	-	-	375	-	-	cm²/Vs
VTINE3LNAL	threshold voltage long channel @ VD=0.1V, L=10µm, W=10µm	0.66	0.69	0.72	0.75	0.78	V
VTINE3LNAS	threshold voltage short channel @ VD=0.1V, L=0.35µm, W=10µm	0.66	0.7	0.74	0.78	0.82	V
VTINE3LNASS	threshold voltage small channel @ VD=0.1V, L=0.35µm, W=0.22µm	-	-	0.6	-	-	V
VTXNE3LNAS	extrapolated threshold voltage short channel @ VD=0.1V, L=0.35µm, W=10µm	-	-	0.79	-	-	V
WEFNE3LNA	effective channel width @ W=0.22µm	-	-	0.16	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTNE3LNA	Pelgrom coefficient gain factor mismatch	0.91	%µm
AIDNE3LNA00	Pelgrom coefficient ID mismatch @ VG-VT=0V	13.6	%µm
AIDNE3LNA02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	6.85	%µm
AIDNE3LNA04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	3.93	%µm
AIDNE3LNA06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	2.62	%µm
AIDNE3LNA10	Pelgrom coefficient ID mismatch @ VG-VT=1V	1.54	%µm
AIDNE3LNA15	Pelgrom coefficient ID mismatch @ VG-VT=1.5V	1.04	%µm
AIDNE3LNA20	Pelgrom coefficient ID mismatch @ VG-VT=2V	0.8	%µm
AIDNE3LNA30	Pelgrom coefficient ID mismatch @ VG-VT=3V	0.59	%µm
AVTNE3LNA	Pelgrom coefficient VT mismatch	10.6	mVµm
DLTNE3LNA	transistor delta length	0.04	µm
DWTNE3LNA	transistor delta width	0.06	µm

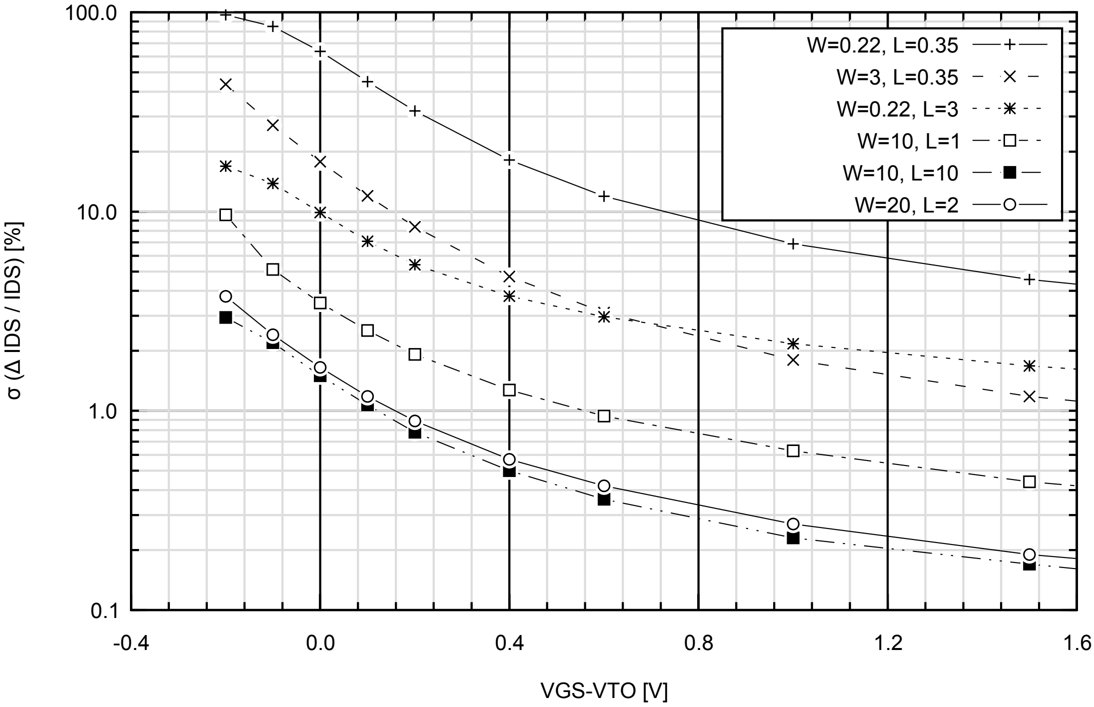

Figure 3.63 Device ne3lna: drain current matching vs. VGS-VTO (typical values, drawn W and L)

ne3lnai

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-4	-3.6	3.6	4	V
VGD	-40°C to 175°C	-4	-3.6	3.6	4	V
VDS	-40°C to 175°C	-4	-3.6	3.6	4	V
VDB	-40°C to 175°C	-0.5	0	3.6	4	V
VSB	-40°C to 175°C	-0.5	0	3.6	4	V

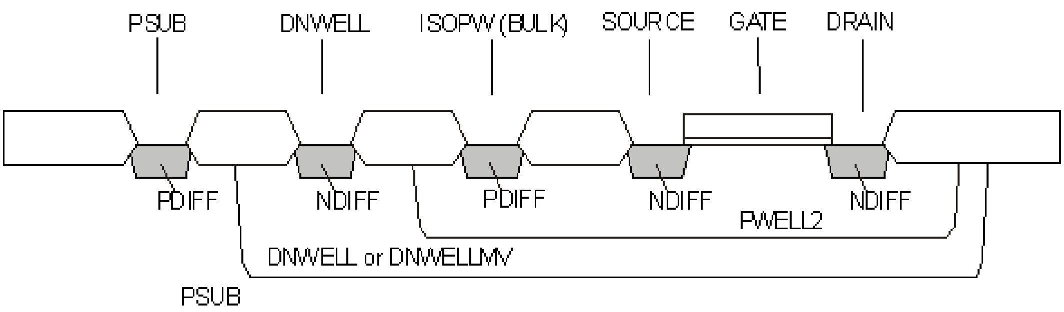

Figure 3.64 Additional Operating Conditions

Note: ne3lnai in DNWELL

$$
\begin{aligned}
V_{PSUB} &\leq V_{DNWELL} \leq V_{PSUB} + 45(50)V \\
V_{DNWELL} - 8(10)V &\leq V_{PWELL2} \leq V_{DNWELL}
\end{aligned}
$$

⇒

ne3lnai in DNWELLMV

$$V_{PSUB} \leq V_{DNWELLMV} \leq V_{PSUB} + 10(12)V$$
$$V_{DNWELLMV} - 8(10)V \leq V_{PWELL2} \leq V_{DNWELLMV}$$

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNE3LNAIS	drain-source breakdown @ VG=0V, Id=1µA, L=0.35µm	5	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXNE3LNAI	mobility exponent	-	-	-1.82	-	-	-
FC_NE3LNAI	corner frequency @ VD=3.3V, Id=1µA, L=10µm, W=10µm	-	-	0.41	-	-	kHz
GA_NE3LNAI	body factor long channel @ L=10µm, W=10µm	-	-	1.33	-	-	√V
IDSNE3LNAIS	saturation current @ VG=3.3V, VD=3.3V, L=0.35µm, W=10µm	500	545	590	635	680	µA/µm
IOFNE3LNAIS	off-state leakage @ VD=3.3V, L=0.35µm, W=10µm	-	-	-	3	-	pA/µm
ISBNE3LNAIS	bulk current @ VD=3.3V, L=0.35µm	-	-	1.1	-	-	µA/µm
KP_NE3LNAI	gain factor long channel @ L=10µm, W=10µm	-	-	180	-	-	µA/V²
LEFNE3LNAI	effective channel length @ L=0.35µm	-	-	0.31	-	-	µm
NOINE3LNAI	Input referred noise @ VD=3.3V, Id=1µA, f=1Hz, L=10µm, W=10µm	-	-	9.2	-	-	µV.µm/ √(Hz)
STSNE3LNAI	subthreshold slope @ VD=3.3V	-	-	10.2	-	-	decade/V
TC_VTXNE3LNAI	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	-1.1	-	-	mV/K
U0_NE3LNAI	effective mobility	-	-	375	-	-	cm²/Vs
VTINE3LNAIL	threshold voltage long channel @ VD=0.1V, L=10µm, W=10µm	0.65	0.68	0.71	0.74	0.77	V
VTINE3LNAIS	threshold voltage short channel @ VD=0.1V, L=0.35µm, W=10µm	0.64	0.68	0.72	0.76	0.8	V
VTINE3LNAISS	threshold voltage small channel @ VD=0.1V, L=0.35µm, W=0.22µm	-	-	0.58	-	-	V
VTXNE3LNAIS	extrapolated threshold voltage short channel @ VD=0.1V, L=0.35µm, W=10µm	-	-	0.77	-	-	V
WEFNE3LNAI	effective channel width @ W=0.22µm	-	-	0.16	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTNE3LNAI	Pelgrom coefficient gain factor mismatch	0.81	%µm
AIDNE3LNAI00	Pelgrom coefficient ID mismatch @ VG-VT=0V	12.6	%µm
AIDNE3LNAI02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	6.34	%µm
AIDNE3LNAI04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	3.62	%µm
AIDNE3LNAI06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	2.41	%µm
AIDNE3LNAI10	Pelgrom coefficient ID mismatch @ VG-VT=1V	1.41	%µm
AIDNE3LNAI15	Pelgrom coefficient ID mismatch @ VG-VT=1.5V	0.94	%µm

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Name	Description	Typ	Unit
AIDNE3LNAI20	Pelgrom coefficient ID mismatch @ VG-VT=2V	0.72	%µm
AIDNE3LNAI30	Pelgrom coefficient ID mismatch @ VG-VT=3V	0.52	%µm
AVTNE3LNAI	Pelgrom coefficient VT mismatch	9.13	mVµm
DLTNE3LNAI	transistor delta length	0.04	µm
DWTNE3LNAI	transistor delta width	0.06	µm

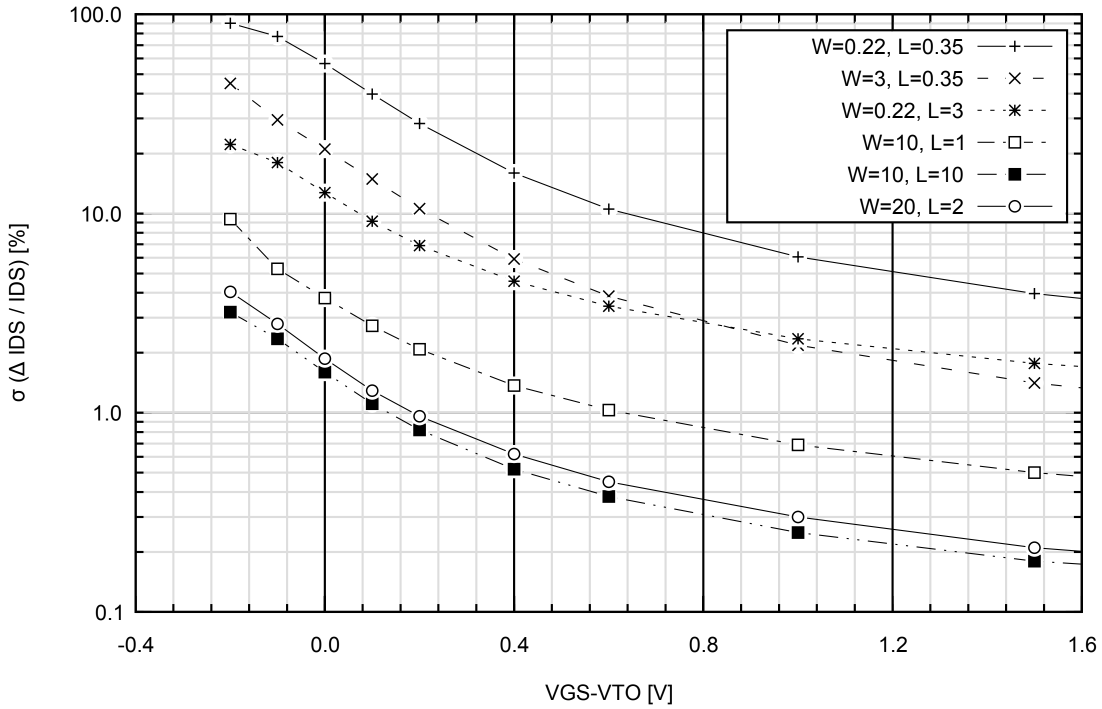

Figure 3.65 Device ne3lnai: drain current matching vs. VGS-VTO (typical values, drawn W and L)

ne3lnai_6

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-4	-3.6	3.6	4	V
VGD	-40°C to 175°C	-4	-3.6	3.6	4	V
VDS	-40°C to 175°C	-4	-3.6	3.6	4	V
VDB	-40°C to 175°C	-0.5	0	3.6	4	V
VSB	-40°C to 175°C	-0.5	0	3.6	4	V
VIpsub	-40°C to 175°C	-0.5	0	45	50	V
VIB	-40°C to 175°C	-0.5	0	8	10	V

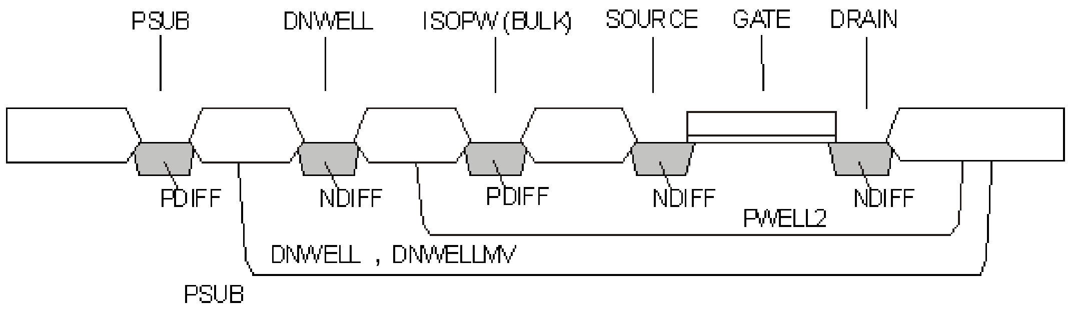

Figure 3.66 Additional Operating Conditions

Note: ne3lnai_6 in DNWELL

$$
\begin{array}{lcccl}
V_{PSUB} & \leq & V_{DNWELL} & \leq & V_{PSUB} + 45(50)V \\
V_{DNWELL} - 8(10)V & \leq & V_{PWELL2} & \leq & V_{DNWELL}
\end{array}
$$

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNE3LNAIS	drain-source breakdown @ VG=0V, Id=1µA, L=0.35µm	5	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXNE3LNAI	mobility exponent	-	-	-1.82	-	-	-
FC_NE3LNAI	corner frequency @ VD=3.3V, Id=1µA, L=10µm, W=10µm	-	-	0.41	-	-	kHz
GA_NE3LNAI	body factor long channel @ L=10µm, W=10µm	-	-	1.33	-	-	√V
IDSNE3LNAIS	saturation current @ VG=3.3V, VD=3.3V, L=0.35µm, W=10µm	500	545	590	635	680	µA/µm
IOFNE3LNAIS	off-state leakage @ VD=3.3V, L=0.35µm, W=10µm	-	-	-	3	-	pA/µm
ISBNE3LNAIS	bulk current @ VD=3.3V, L=0.35µm	-	-	1.1	-	-	µA/µm
KP_NE3LNAI	gain factor long channel @ L=10µm, W=10µm	-	-	180	-	-	µA/V²
LEFNE3LNAI	effective channel length @ L=0.35µm	-	-	0.31	-	-	µm
NOINE3LNAI	Input referred noise @ VD=3.3V, Id=1µA, f=1Hz, L=10µm, W=10µm	-	-	9.2	-	-	µV.µm/√(Hz)
STSNE3LNAI	subthreshold slope @ VD=3.3V	-	-	10.2	-	-	decade/V
TC_VTXNE3LNAI	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	-1.1	-	-	mV/K
U0_NE3LNAI	effective mobility	-	-	375	-	-	cm²/Vs
VTINE3LNAIL	threshold voltage long channel @ VD=0.1V, L=10µm, W=10µm	0.65	0.68	0.71	0.74	0.77	V
VTINE3LNAIS	threshold voltage short channel @ VD=0.1V, L=0.35µm, W=10µm	0.64	0.68	0.72	0.76	0.8	V
VTINE3LNAISS	threshold voltage small channel @ VD=0.1V, L=0.35µm, W=0.22µm	-	-	0.58	-	-	V

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Name	Description	LSL	Low	Typ	High	USL	Unit
VTXNE3LNAIS	extrapolated threshold voltage short channel @ VD=0.1V, L=0.35µm, W=10µm	-	-	0.77	-	-	V
WEFNE3LNAI	effective channel width @ W=0.22µm	-	-	0.16	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTNE3LNAI	Pelgrom coefficient gain factor mismatch	0.81	%µm
AIDNE3LNAI00	Pelgrom coefficient ID mismatch @ VG-VT=0V	12.6	%µm
AIDNE3LNAI02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	6.34	%µm
AIDNE3LNAI04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	3.62	%µm
AIDNE3LNAI06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	2.41	%µm
AIDNE3LNAI10	Pelgrom coefficient ID mismatch @ VG-VT=1V	1.41	%µm
AIDNE3LNAI15	Pelgrom coefficient ID mismatch @ VG-VT=1.5V	0.94	%µm
AIDNE3LNAI20	Pelgrom coefficient ID mismatch @ VG-VT=2V	0.72	%µm
AIDNE3LNAI30	Pelgrom coefficient ID mismatch @ VG-VT=3V	0.52	%µm
AVTNE3LNAI	Pelgrom coefficient VT mismatch	9.13	mVµm
DLTNE3LNAI	transistor delta length	0.04	µm
DWTNE3LNAI	transistor delta width	0.06	µm

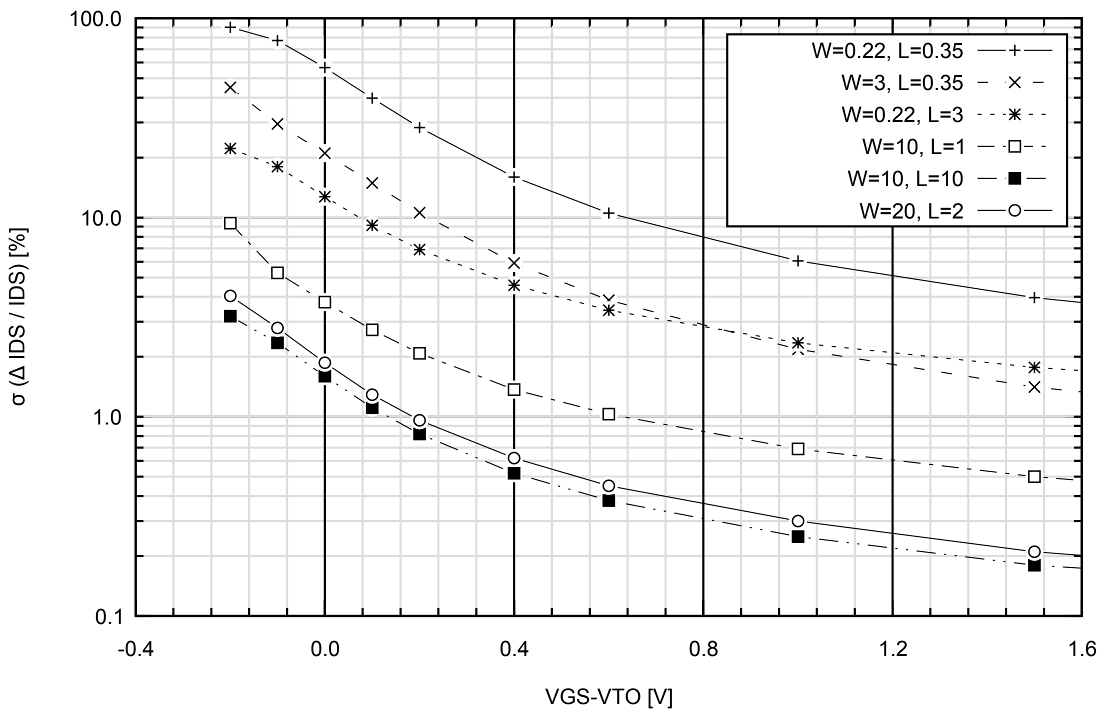

Figure 3.67 Device ne3lnai: drain current matching vs. VGS-VTO (typical values, drawn W and L)

ne3lnai_m_6

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-4	-3.6	3.6	4	V
VGD	-40°C to 175°C	-4	-3.6	3.6	4	V

⇒

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VDS	-40°C to 175°C	-4	-3.6	3.6	4	V
VDB	-40°C to 175°C	-0.5	0	3.6	4	V
VSB	-40°C to 175°C	-0.5	0	3.6	4	V
VIpsub	-40°C to 175°C	-0.5	0	10	12	V
VIB	-40°C to 175°C	-0.5	0	8	10	V

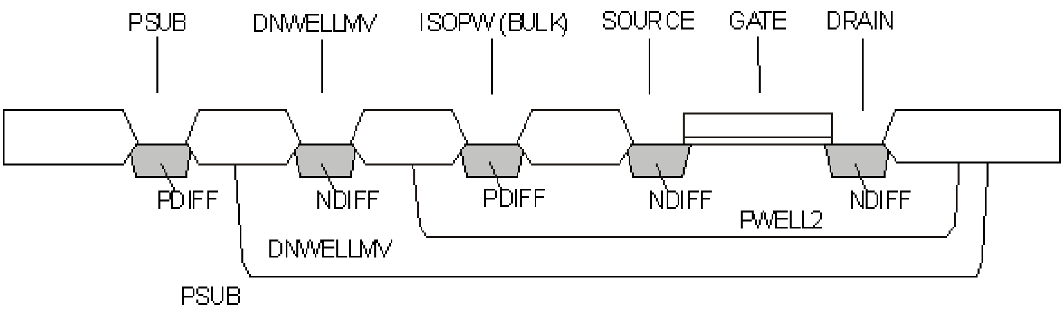

Figure 3.68 Additional Operating Conditions

Note: ne3lnai_m_6 in DNWELLMV

$$
\begin{array}{rcccl}
V_{PSUB} & \leq & V_{DNWELLMV} & \leq & V_{PSUB} + 10(12)V \\
V_{DNWELLMV} - 8(10)V & \leq & V_{PWELL2} & \leq & V_{DNWELLMV}
\end{array}
$$

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNE3LNAIS	drain-source breakdown @ VG=0V, Id=1µA, L=0.35µm	5	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXNE3LNAI	mobility exponent	-	-	-1.82	-	-	-
FC_NE3LNAI	corner frequency @ VD=3.3V, Id=1µA, L=10µm, W=10µm	-	-	0.41	-	-	kHz
GA_NE3LNAI	body factor long channel @ L=10µm, W=10µm	-	-	1.33	-	-	√V
IDSNE3LNAIS	saturation current @ VG=3.3V, VD=3.3V, L=0.35µm, W=10µm	500	545	590	635	680	µA/µm
IOFNE3LNAIS	off-state leakage @ VD=3.3V, L=0.35µm, W=10µm	-	-	-	3	-	pA/µm
ISBNE3LNAIS	bulk current @ VD=3.3V, L=0.35µm	-	-	1.1	-	-	µA/µm
KP_NE3LNAI	gain factor long channel @ L=10µm, W=10µm	-	-	180	-	-	µA/V²
LEFNE3LNAI	effective channel length @ L=0.35µm	-	-	0.31	-	-	µm
NOINE3LNAI	Input referred noise @ VD=3.3V, Id=1µA, f=1Hz, L=10µm, W=10µm	-	-	9.2	-	-	µV.µm/√(Hz)
STSNE3LNAI	subthreshold slope @ VD=3.3V	-	-	10.2	-	-	decade/V
TC_VTXNE3LNAI	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	-1.1	-	-	mV/K
U0_NE3LNAI	effective mobility	-	-	375	-	-	cm²/Vs

⇒

Name	Description	LSL	Low	Typ	High	USL	Unit
VTINE3LNAIL	threshold voltage long channel @ VD=0.1V, L=10µm, W=10µm	0.65	0.68	0.71	0.74	0.77	V
VTINE3LNAIS	threshold voltage short channel @ VD=0.1V, L=0.35µm, W=10µm	0.64	0.68	0.72	0.76	0.8	V
VTINE3LNAISS	threshold voltage small channel @ VD=0.1V, L=0.35µm, W=0.22µm	-	-	0.58	-	-	V
VTXNE3LNAIS	extrapolated threshold voltage short channel @ VD=0.1V, L=0.35µm, W=10µm	-	-	0.77	-	-	V
WEFNE3LNAI	effective channel width @ W=0.22µm	-	-	0.16	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTNE3LNAI	Pelgrom coefficient gain factor mismatch	0.81	%µm
AIDNE3LNAI00	Pelgrom coefficient ID mismatch @ VG-VT=0V	12.6	%µm
AIDNE3LNAI02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	6.34	%µm
AIDNE3LNAI04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	3.62	%µm
AIDNE3LNAI06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	2.41	%µm
AIDNE3LNAI10	Pelgrom coefficient ID mismatch @ VG-VT=1V	1.41	%µm
AIDNE3LNAI15	Pelgrom coefficient ID mismatch @ VG-VT=1.5V	0.94	%µm
AIDNE3LNAI20	Pelgrom coefficient ID mismatch @ VG-VT=2V	0.72	%µm
AIDNE3LNAI30	Pelgrom coefficient ID mismatch @ VG-VT=3V	0.52	%µm
AVTNE3LNAI	Pelgrom coefficient VT mismatch	9.13	mVµm
DLTNE3LNAI	transistor delta length	0.04	µm
DWTNE3LNAI	transistor delta width	0.06	µm

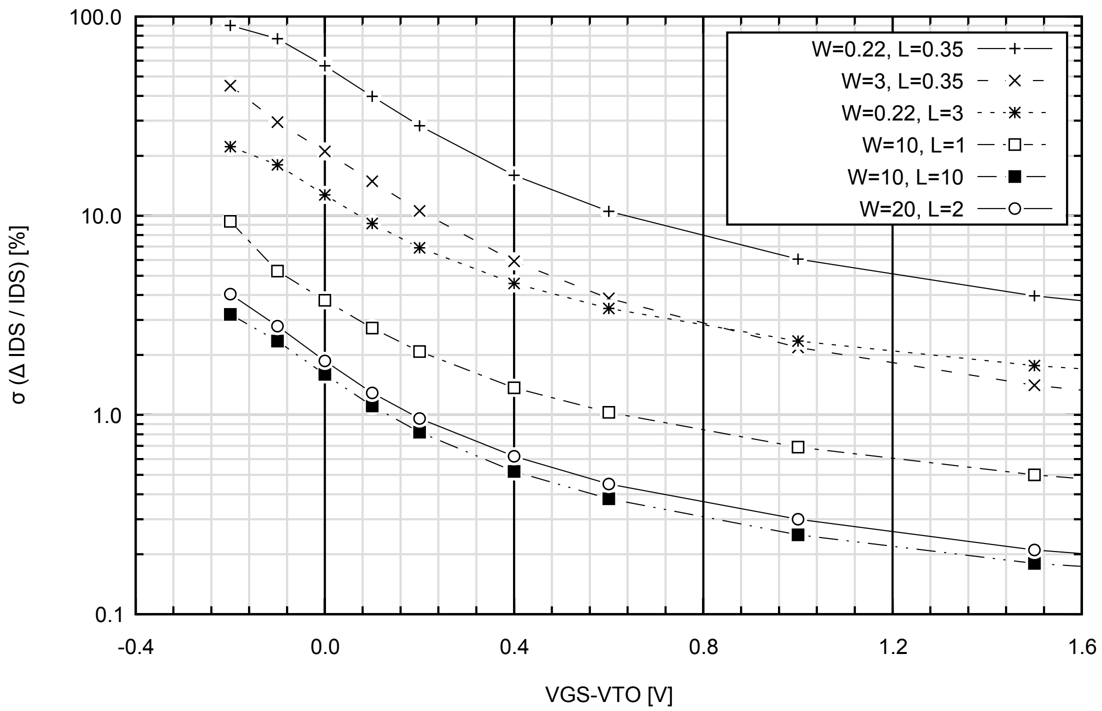

Figure 3.69 Device ne3lnai: drain current matching vs. VGS-VTO (typical values, drawn W and L)

pe3lna, pe3lna_5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-4	-3.6	3.6	4	V
VGD	-40°C to 175°C	-4	-3.6	3.6	4	V
VDS	-40°C to 175°C	-4	-3.6	3.6	4	V
VDB	-40°C to 175°C	-4	-3.6	0	0.5	V
VSB	-40°C to 175°C	-4	-3.6	0	0.5	V
VBpsub	-40°C to 175°C	-0.5	0	3.6	4	V

Process parameters

Negative values are considered as absolute values for their limits.

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPE3LNAS	drain-source breakdown @ VG=0V, Id=-1µA, L=0.3µm	5	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXPE3LNA	mobility exponent	-	-	-1.16	-	-	-
FC_PE3LNA	corner frequency @ VD=3.3V, Id=1µA, L=10µm, W=10µm	-	-	0.33	-	-	kHz
GA_PE3LNA	body factor long channel @ L=10µm, W=10µm	-	-	0.94	-	-	√V
IDSPE3LNAS	saturation current @ VG=-3.3V, VD=-3.3V, L=0.3µm, W=10µm	225	262	300	338	375	µA/µm
IOFPE3LNAS	off-state leakage @ VD=-3.3V, L=0.3µm, W=10µm	-	-	-	3	-	pA/µm
KP_PE3LNA	gain factor long channel @ L=10µm, W=10µm	-	-	40	-	-	µA/V²
LEFPE3LNA	effective channel length @ L=0.3µm	-	-	0.24	-	-	µm
NOIPE3LNA	Input referred noise @ VD=-3.3V, Id=-1µA, f=1Hz, L=10µm, W=10µm	-	-	10	-	-	µV.µm/√(Hz)
STSPE3LNA	subthreshold slope @ VD=-3.3V	-	-	11	-	-	decade/V
TC_VTXPE3LNA	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	1.1	-	-	mV/K
U0_PE3LNA	effective mobility	-	-	80	-	-	cm²/Vs
VTIPE3LNAL	threshold voltage long channel @ VD=-0.1V, L=10µm, W=10µm	-0.62	-0.65	-0.68	-0.71	-0.74	V
VTIPE3LNAS	threshold voltage short channel @ VD=-0.1V, L=0.3µm, W=10µm	-0.55	-0.59	-0.63	-0.67	-0.71	V
VTIPE3LNASS	threshold voltage small channel @ VD=-0.1V, L=0.3µm, W=0.22µm	-	-	-0.59	-	-	V
VTXPE3LNAS	extrapolated threshold voltage short channel @ VD=-0.1V, L=0.3µm, W=10µm	-	-	-0.6	-	-	V
WEFPE3LNA	effective channel width @ W=0.22µm	-	-	0.24	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTPE3LNA	Pelgrom coefficient gain factor mismatch	0.56	%µm
AIDPE3LNA00	Pelgrom coefficient ID mismatch @ VG-VT=0V	9.06	%µm

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Name	Description	Typ	Unit
AIDPE3LNA02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	3.96	%µm
AIDPE3LNA04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	2.3	%µm
AIDPE3LNA06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	1.61	%µm
AIDPE3LNA10	Pelgrom coefficient ID mismatch @ VG-VT=1V	1.03	%µm
AIDPE3LNA15	Pelgrom coefficient ID mismatch @ VG-VT=1.5V	0.73	%µm
AIDPE3LNA20	Pelgrom coefficient ID mismatch @ VG-VT=2V	0.59	%µm
AIDPE3LNA30	Pelgrom coefficient ID mismatch @ VG-VT=3V	0.46	%µm
AVTPE3LNA	Pelgrom coefficient VT mismatch	4.86	mVµm
DLTPE3LNA	transistor delta length	0.06	µm
DWTPE3LNA	transistor delta width	-0.02	µm

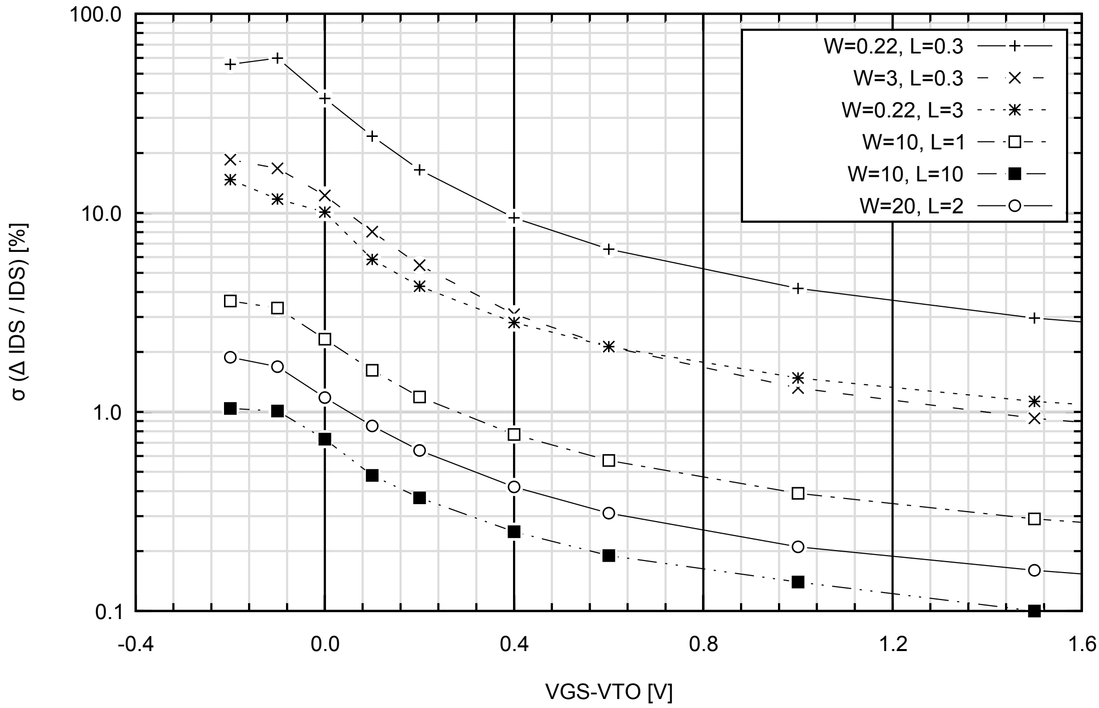

Figure 3.70 Device pe3lna: drain current matching vs. VGS-VTO (typical values, drawn W and L)

pe3lnai

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40 °C to 175 °C	-4	-3.6	3.6	4	V
VGD	-40 °C to 175 °C	-4	-3.6	3.6	4	V
VDS	-40 °C to 175 °C	-4	-3.6	3.6	4	V
VDB	-40 °C to 175 °C	-4	-3.6	0	0.5	V
VSB	-40 °C to 175 °C	-4	-3.6	0	0.5	V
VBpsub(1	-40 °C to 175 °C	-0.5	0	10	12	V

Note 1 If DNWELL instead of DNWELLMV is used for the isolated PMOS transistors, then max. VBpsub = 45 (50)V.

Process parameters

Negative values are considered as absolute values for their limits.

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPE3LNAIS	drain-source breakdown @ VG=0V, Id=-1µA, L=0.3µm	5	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXPE3LNAI	mobility exponent	-	-	-1.16	-	-	-
FC_PE3LNAI	corner frequency @ VD=3.3V, Id=1µA, L=10µm, W=10µm	-	-	0.33	-	-	kHz
GA_PE3LNAI	body factor long channel @ L=10µm, W=10µm	-	-	0.94	-	-	√V
IDSPE3LNAIS	saturation current @ VG=-3.3V, VD=-3.3V, L=0.3µm, W=10µm	225	263	300	338	375	µA/µm
IOFPE3LNAIS	off-state leakage @ VD=-3.3V, L=0.3µm, W=10µm	-	-	-	3	-	pA/µm
KP_PE3LNAI	gain factor long channel @ L=10µm, W=10µm	-	-	40	-	-	µA/V²
LEFPE3LNAI	effective channel length @ L=0.3µm	-	-	0.24	-	-	µm
NOIPE3LNAI	Input referred noise @ VD=-3.3V, Id=-1µA, f=1Hz, L=10µm, W=10µm	-	-	10	-	-	µV.µm/√(Hz)
STSPE3LNAI	subthreshold slope @ VD=-3.3V	-	-	10.8	-	-	decade/V
TC_VTXPE3LNAI	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	1.1	-	-	mV/K
U0_PE3LNAI	effective mobility	-	-	81	-	-	cm²/Vs
VTIPE3LNAIL	threshold voltage long channel @ VD=-0.1V, L=10µm, W=10µm	-0.62	-0.65	-0.68	-0.71	-0.74	V
VTIPE3LNAIS	threshold voltage short channel @ VD=-0.1V, L=0.3µm, W=10µm	-0.55	-0.59	-0.63	-0.67	-0.71	V
VTIPE3LNAISS	threshold voltage small channel @ VD=-0.1V, L=0.3µm, W=0.22µm	-	-	-0.59	-	-	V
VTXPE3LNAIS	extrapolated threshold voltage short channel @ VD=-0.1V, L=0.3µm, W=10µm	-	-	-0.62	-	-	V
WEFPE3LNAI	effective channel width @ W=0.22µm	-	-	0.24	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTPE3LNAI	Pelgrom coefficient gain factor mismatch	0.67	%µm
AIDPE3LNAI00	Pelgrom coefficient ID mismatch @ VG-VT=0V	9.31	%µm
AIDPE3LNAI02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	4.09	%µm
AIDPE3LNAI04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	2.31	%µm
AIDPE3LNAI06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	1.57	%µm
AIDPE3LNAI10	Pelgrom coefficient ID mismatch @ VG-VT=1V	0.97	%µm
AIDPE3LNAI15	Pelgrom coefficient ID mismatch @ VG-VT=1.5V	0.68	%µm
AIDPE3LNAI20	Pelgrom coefficient ID mismatch @ VG-VT=2V	0.55	%µm
AIDPE3LNAI30	Pelgrom coefficient ID mismatch @ VG-VT=3V	0.42	%µm
AVTPE3LNAI	Pelgrom coefficient VT mismatch	5.57	mVµm
DLTPE3LNAI	transistor delta length	0.06	µm
DWTPE3LNAI	transistor delta width	-0.02	µm

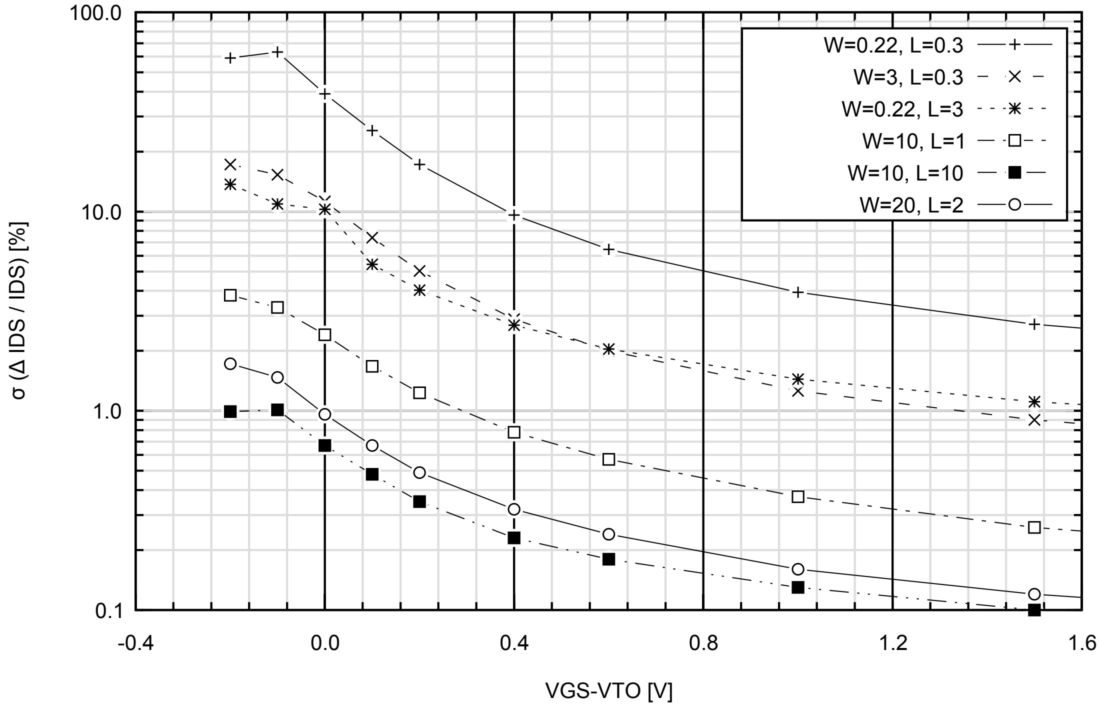

Figure 3.71 Device pe3lnai: drain current matching vs. VGS-VTO (typical values, drawn W and L)

pe3lnai_5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-4	-3.6	3.6	4	V
VGD	-40°C to 175°C	-4	-3.6	3.6	4	V
VDS	-40°C to 175°C	-4	-3.6	3.6	4	V
VDB	-40°C to 175°C	-4	-3.6	0	0.5	V
VSB	-40°C to 175°C	-4	-3.6	0	0.5	V
VBpsub	-40°C to 175°C	-0.5	0	45	50	V

Process parameters

Negative values are considered as absolute values for their limits.

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPE3LNAIS	drain-source breakdown @ VG=0V, Id=-1μA, L=0.3μm	5	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXPE3LNAI	mobility exponent	-	-	-1.16	-	-	-
FC_PE3LNAI	corner frequency @ VD=3.3V, Id=1μA, L=10μm, W=10μm	-	-	0.33	-	-	kHz
GA_PE3LNAI	body factor long channel @ L=10μm, W=10μm	-	-	0.94	-	-	√V
IDSPE3LNAIS	saturation current @ VG=-3.3V, VD=-3.3V, L=0.3μm, W=10μm	225	263	300	338	375	μA/μm
IOFPE3LNAIS	off-state leakage @ VD=-3.3V, L=0.3μm, W=10μm	-	-	-	3	-	pA/μm

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Name	Description	LSL	Low	Typ	High	USL	Unit
KP_PE3LNAI	gain factor long channel @ L=10µm, W=10µm	-	-	40	-	-	µA/V²
LEFPE3LNAI	effective channel length @ L=0.3µm	-	-	0.24	-	-	µm
NOIPE3LNAI	Input referred noise @ VD=-3.3V, Id=-1µA, f=1Hz, L=10µm, W=10µm	-	-	10	-	-	µV.µm/√(Hz)
STSPE3LNAI	subthreshold slope @ VD=-3.3V	-	-	10.8	-	-	decade/V
TC_VTXPE3LNAI	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	1.1	-	-	mV/K
U0_PE3LNAI	effective mobility	-	-	81	-	-	cm²/Vs
VTIPE3LNAIL	threshold voltage long channel @ VD=-0.1V, L=10µm, W=10µm	-0.62	-0.65	-0.68	-0.71	-0.74	V
VTIPE3LNAIS	threshold voltage short channel @ VD=-0.1V, L=0.3µm, W=10µm	-0.55	-0.59	-0.63	-0.67	-0.71	V
VTIPE3LNAISS	threshold voltage small channel @ VD=-0.1V, L=0.3µm, W=0.22µm	-	-	-0.59	-	-	V
VTXPE3LNAIS	extrapolated threshold voltage short channel @ VD=-0.1V, L=0.3µm, W=10µm	-	-	-0.62	-	-	V
WEFPE3LNAI	effective channel width @ W=0.22µm	-	-	0.24	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTPE3LNAI	Pelgrom coefficient gain factor mismatch	0.67	%µm
AIDPE3LNAI00	Pelgrom coefficient ID mismatch @ VG-VT=0V	9.31	%µm
AIDPE3LNAI02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	4.09	%µm
AIDPE3LNAI04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	2.31	%µm
AIDPE3LNAI06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	1.57	%µm
AIDPE3LNAI10	Pelgrom coefficient ID mismatch @ VG-VT=1V	0.97	%µm
AIDPE3LNAI15	Pelgrom coefficient ID mismatch @ VG-VT=1.5V	0.68	%µm
AIDPE3LNAI20	Pelgrom coefficient ID mismatch @ VG-VT=2V	0.55	%µm
AIDPE3LNAI30	Pelgrom coefficient ID mismatch @ VG-VT=3V	0.42	%µm
AVTPE3LNAI	Pelgrom coefficient VT mismatch	5.57	mVµm
DLTPE3LNAI	transistor delta length	0.06	µm
DWTPE3LNAI	transistor delta width	-0.02	µm

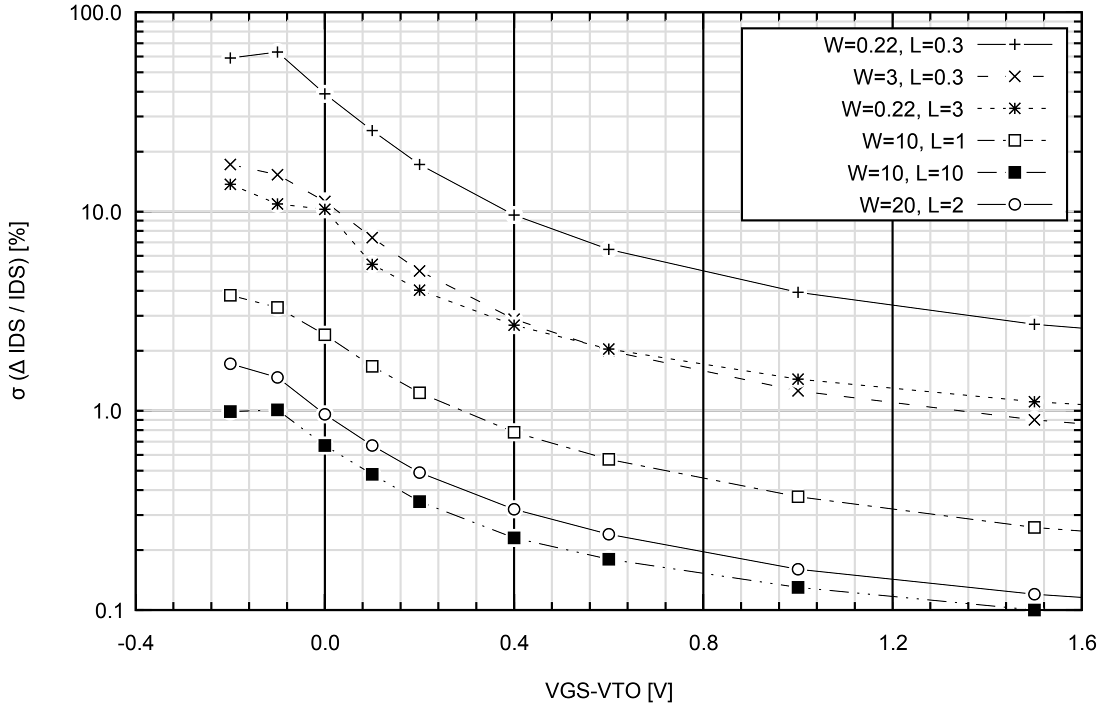

Figure 3.72 Device pe3lnai: drain current matching vs. VGS-VTO (typical values, drawn W and L)

pe3lnai_m_5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-4	-3.6	3.6	4	V
VGD	-40°C to 175°C	-4	-3.6	3.6	4	V
VDS	-40°C to 175°C	-4	-3.6	3.6	4	V
VDB	-40°C to 175°C	-4	-3.6	0	0.5	V
VSB	-40°C to 175°C	-4	-3.6	0	0.5	V
VBpsub	-40°C to 175°C	-0.5	0	10	12	V

Process parameters

Negative values are considered as absolute values for their limits.

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPE3LNAIS	drain-source breakdown @ VG=0V, Id=-1μA, L=0.3μm	5	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXPE3LNAI	mobility exponent	-	-	-1.16	-	-	-
FC_PE3LNAI	corner frequency @ VD=3.3V, Id=1μA, L=10μm, W=10μm	-	-	0.33	-	-	kHz
GA_PE3LNAI	body factor long channel @ L=10μm, W=10μm	-	-	0.94	-	-	√V
IDSPE3LNAIS	saturation current @ VG=-3.3V, VD=-3.3V, L=0.3μm, W=10μm	225	263	300	338	375	μA/μm
IOFPE3LNAIS	off-state leakage @ VD=-3.3V, L=0.3μm, W=10μm	-	-	-	3	-	pA/μm

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Name	Description	LSL	Low	Typ	High	USL	Unit
KP_PE3LNAI	gain factor long channel @ L=10µm, W=10µm	-	-	40	-	-	µA/V²
LEFPE3LNAI	effective channel length @ L=0.3µm	-	-	0.24	-	-	µm
NOIPE3LNAI	Input referred noise @ VD=-3.3V, Id=-1µA, f=1Hz, L=10µm, W=10µm	-	-	10	-	-	µV.µm/√(Hz)
STSPE3LNAI	subthreshold slope @ VD=-3.3V	-	-	10.8	-	-	decade/V
TC_VTXPE3LNAI	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	1.1	-	-	mV/K
U0_PE3LNAI	effective mobility	-	-	81	-	-	cm²/Vs
VTIPE3LNAIL	threshold voltage long channel @ VD=-0.1V, L=10µm, W=10µm	-0.62	-0.65	-0.68	-0.71	-0.74	V
VTIPE3LNAIS	threshold voltage short channel @ VD=-0.1V, L=0.3µm, W=10µm	-0.55	-0.59	-0.63	-0.67	-0.71	V
VTIPE3LNAISS	threshold voltage small channel @ VD=-0.1V, L=0.3µm, W=0.22µm	-	-	-0.59	-	-	V
VTXPE3LNAIS	extrapolated threshold voltage short channel @ VD=-0.1V, L=0.3µm, W=10µm	-	-	-0.62	-	-	V
WEFPE3LNAI	effective channel width @ W=0.22µm	-	-	0.24	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTPE3LNAI	Pelgrom coefficient gain factor mismatch	0.67	%µm
AIDPE3LNAI00	Pelgrom coefficient ID mismatch @ VG-VT=0V	9.31	%µm
AIDPE3LNAI02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	4.09	%µm
AIDPE3LNAI04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	2.31	%µm
AIDPE3LNAI06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	1.57	%µm
AIDPE3LNAI10	Pelgrom coefficient ID mismatch @ VG-VT=1V	0.97	%µm
AIDPE3LNAI15	Pelgrom coefficient ID mismatch @ VG-VT=1.5V	0.68	%µm
AIDPE3LNAI20	Pelgrom coefficient ID mismatch @ VG-VT=2V	0.55	%µm
AIDPE3LNAI30	Pelgrom coefficient ID mismatch @ VG-VT=3V	0.42	%µm
AVTPE3LNAI	Pelgrom coefficient VT mismatch	5.57	mVµm
DLTPE3LNAI	transistor delta length	0.06	µm
DWTPE3LNAI	transistor delta width	-0.02	µm

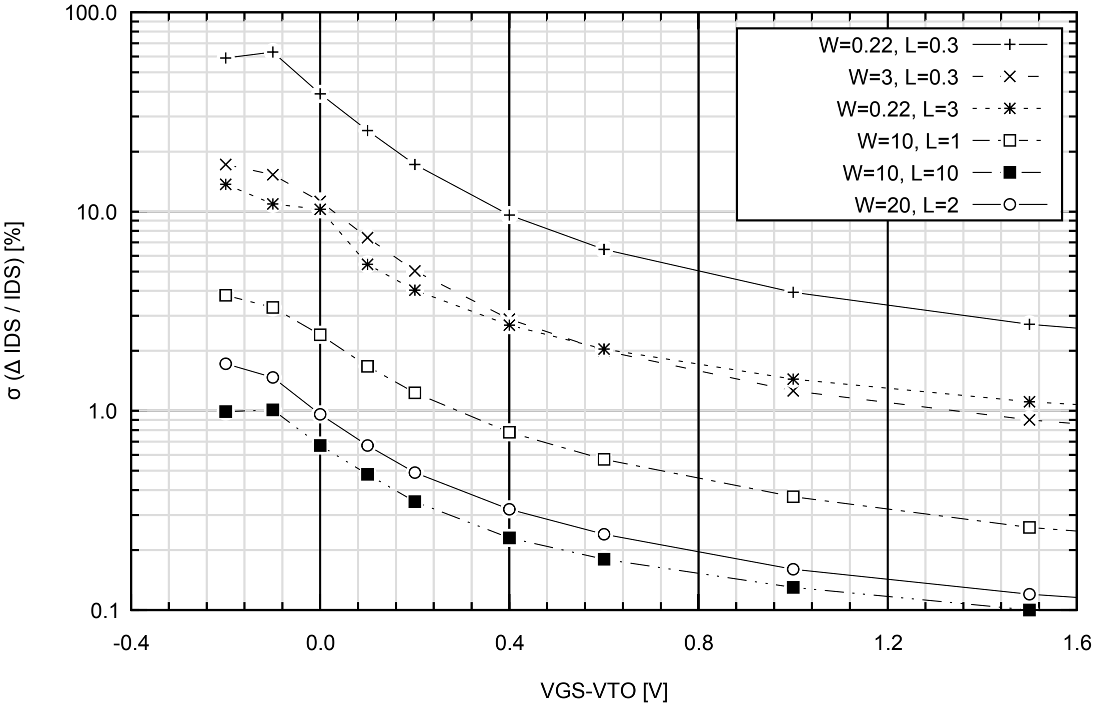

Figure 3.73 Device pe3lnai: drain current matching vs. VGS-VTO (typical values, drawn W and L)

3.17 DEPL module

3.17.1 Device independent parameters

Structural and geometrical parameters

Name	Description	Typ	Unit
XJ_PDEPL	Depletion well in DNWELLMV/DNWELL junction depth	1	µm
	Note: This parameter is only available if the DEPL and ISOMOS modules are selected.		

Sheet and contact resistance parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSSPDPL	Depletion well in DNWELLMV/ DNWELL sheet resistance @ W=20µm	2.9	3.15	3.4	3.65	3.9	kΩ/☐
	Note: This parameter is only available if the DEPL and ISOMOS modules are selected.						

Gate oxide parameters

Name	Description	Typ	Unit
CGADPL	3.3V depletion gate oxide area capacitance	5.2	fF/µm²
CGODPL	3.3V depletion gate – source/drain overlap	0.16	fF/µm

3.17.2 Device parameters

nd3

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-4	-3.6	3.6	4	V
VGD	-40°C to 175°C	-4	-3.6	3.6	4	V
VDS	-40°C to 175°C	-4	-3.6	3.6	4	V
VDB	-40°C to 175°C	-0.5	0	3.6	4	V
VSB	-40°C to 175°C	-0.5	0	3.6	4	V

Note: The node B (BULK) is: DEPL

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSND3S	drain-source breakdown @ VG=-3.3V, Id=1µA, L=0.7µm	5	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXND3	mobility exponent	-	-	-0.2	-	-	-
FC_ND3	corner frequency @ VD=3.3V, Id=1µA, L=10µm, W=10µm	-	-	1.53	-	-	kHz
GAMND3L	body factor long channel @ L=10µm, W=10µm	-	-	0.6	-	-	√V
IDSND3S0	saturation current @ VG=3.3V, VD=3.3V, L=0.7µm, W=10µm	630	680	730	780	830	µA/µm
ISBND3S	bulk current @ VD=3.3V, L=0.7µm	-	-	0.17	-	-	µA/µm
KP_ND3L	gain factor long channel @ L=10µm, W=10µm	-	-	210	-	-	µA/V²

⇒

Name	Description	LSL	Low	Typ	High	USL	Unit
LEFND3	effective channel length @ L=0.7µm	-	-	0.65	-	-	µm
NOIND3	Input referred noise @ VD=3.3V, Id=1µA, f=1Hz, L=10µm, W=10µm	-	-	12.9	-	-	µV.µm/ √(Hz)
TC_VTXND3S	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	-1.3	-	-	mV/K
VTXND3L	extrapolated threshold voltage long channel @ VD=0.1V, L=10µm, W=10µm	-	-0.39	-0.3	-0.21	-	V
VTXND3S	extrapolated threshold voltage short channel @ VD=0.1V, L=0.7µm, W=10µm	-0.35	-0.28	-0.2	-0.12	-0.05	V
WEFND3	effective channel width @ W=0.44µm	-	-	0.35	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTND3	Pelgrom coefficient gain factor mismatch	1.21	%µm
AIDND300	Pelgrom coefficient ID mismatch @ VG-VT=0V	21.8	%µm
AIDND302	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	9.21	%µm
AIDND304	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	5.21	%µm
AIDND306	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	3.47	%µm
AIDND310	Pelgrom coefficient ID mismatch @ VG-VT=1V	2.04	%µm
AIDND315	Pelgrom coefficient ID mismatch @ VG-VT=1.5V	1.36	%µm
AIDND320	Pelgrom coefficient ID mismatch @ VG-VT=2V	1.05	%µm
AIDND330	Pelgrom coefficient ID mismatch @ VG-VT=3V	0.75	%µm
AVTND3	Pelgrom coefficient VT mismatch	11.2	mVµm
DLTND3	transistor delta length	0.05	µm
DWTND3	transistor delta width	0.09	µm

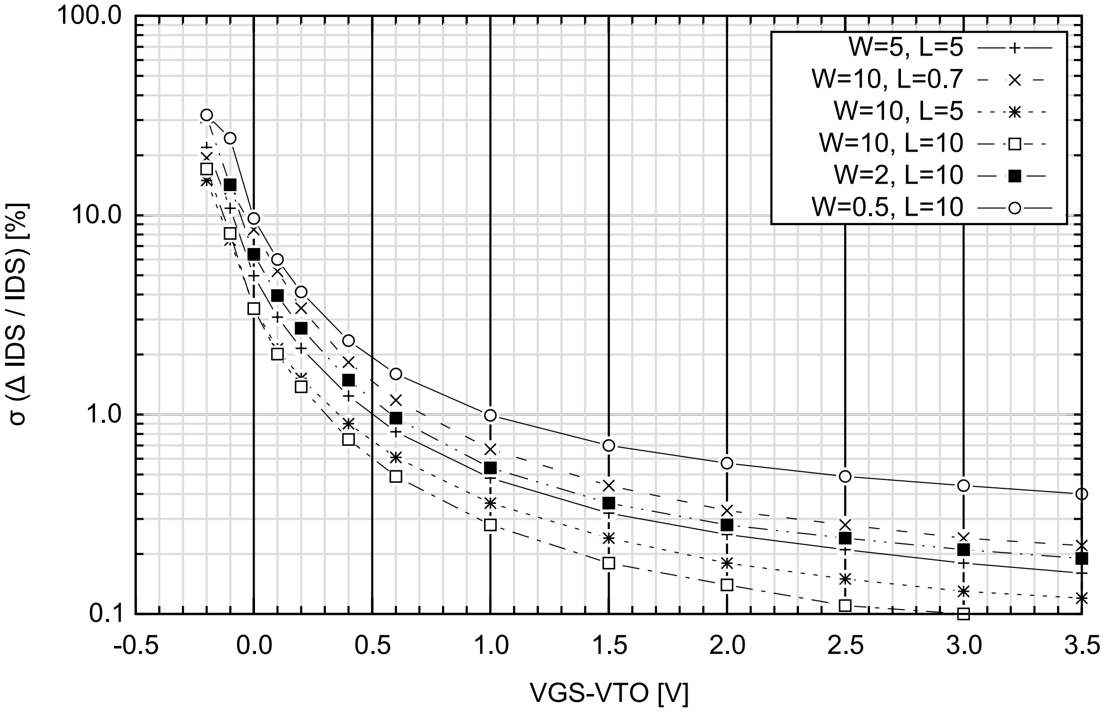

Figure 3.74 Device nd3: drain current matching vs. VGS-VTO (typical values, drawn W and L)

nd3i

nd3i is only available if DEPL and ISOMOS or DEPL and HVMOS modules are selected.

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-4	-3.6	3.6	4	V
VGD	-40°C to 175°C	-4	-3.6	3.6	4	V
VDS	-40°C to 175°C	-4	-3.6	3.6	4	V
VDB	-40°C to 175°C	-0.5	0	3.6	4	V
VSB	-40°C to 175°C	-0.5	0	3.6	4	V

Note: The node B (BULK) is: DEPL

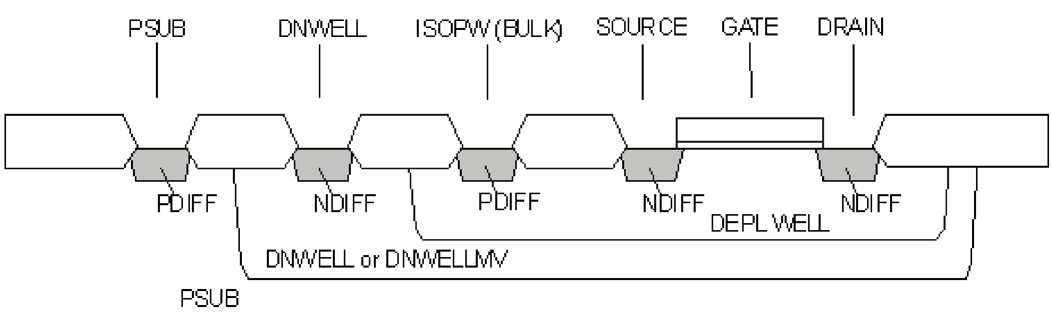

Figure 3.75 Additional Operating Conditions

Note: nd3i in DNWELL

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$$\begin{array}{lclcl} V_{PSUB} & \leq & V_{DNWELL} & \leq & V_{PSUB} + 45(50)V \\ V_{DNWELL} - 8(10)V & \leq & V_{DEPLWELL} & \leq & V_{DNWELL} \end{array}$$

nd3i in DNWELLMV

$$\begin{array}{lclcl} V_{PSUB} & \leq & V_{DNWELLMV} & \leq & V_{PSUB} + \ 10(12)V \\ V_{DNWELLV} - 8(10)V & \leq & V_{DEPLWELL} & \leq & V_{DNWELLMV} \end{array}$$

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSND3IS	drain-source breakdown @ VG=-3.3V, Id=1µA, L=0.7µm	-	5	-	-	-	V
BEXND3I	mobility exponent	-	-	-0.2	-	-	-
FC_ND3I	corner frequency @ VD=3.3V, Id=1µA, L=10µm, W=10µm	-	-	1.53	-	-	kHz
GAMND3IL	body factor long channel @ L=10µm, W=10µm	-	-	0.6	-	-	√V
IDSND3IS	saturation current @ VG=3.3V, VD=3.3V, L=0.7µm, W=10µm	640	690	740	790	840	µA/µm
ISBND3IS	bulk current @ VD=3.3V, L=0.7µm	-	-	0.17	-	-	µA/µm
KP_ND3IL	gain factor long channel @ L=10µm, W=10µm	-	-	210	-	-	µA/V²
LEFND3I	effective channel length @ L=0.7µm	-	-	0.65	-	-	µm
NOIND3I	Input referred noise @ VD=3.3V, Id=1µA, f=1Hz, L=10µm, W=10µm	-	-	12.9	-	-	µV.µm/√(Hz)
TC_VTXND3I	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	-1.3	-	-	mV/K
VTXND3IL	extrapolated threshold voltage long channel @ VD=0.1V, L=10µm, W=10µm	-	-0.42	-0.33	-0.24	-	V
VTXND3IS	extrapolated threshold voltage short channel @ VD=0.1V, L=0.7µm, W=10µm	-0.39	-0.32	-0.24	-0.16	-0.09	V
WEFND3I	effective channel width @ W=0.44µm	-	-	0.35	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTND3I	Pelgrom coefficient gain factor mismatch	0.88	%µm
AIDND3I00	Pelgrom coefficient ID mismatch @ VG-VT=0V	9.74	%µm
AIDND3I02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	5.41	%µm
AIDND3I04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	3.57	%µm
AIDND3I06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	2.65	%µm
AIDND3I10	Pelgrom coefficient ID mismatch @ VG-VT=1V	1.8	%µm
AIDND3I15	Pelgrom coefficient ID mismatch @ VG-VT=1.5V	1.35	%µm
AIDND3I20	Pelgrom coefficient ID mismatch @ VG-VT=2V	1.12	%µm
AIDND3I30	Pelgrom coefficient ID mismatch @ VG-VT=3V	0.9	%µm
AVTND3I	Pelgrom coefficient VT mismatch	7.88	mVµm
DLTND3I	transistor delta length	0.05	µm

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Name	Description	Typ	Unit
DWTND3I	transistor delta width	0.09	µm

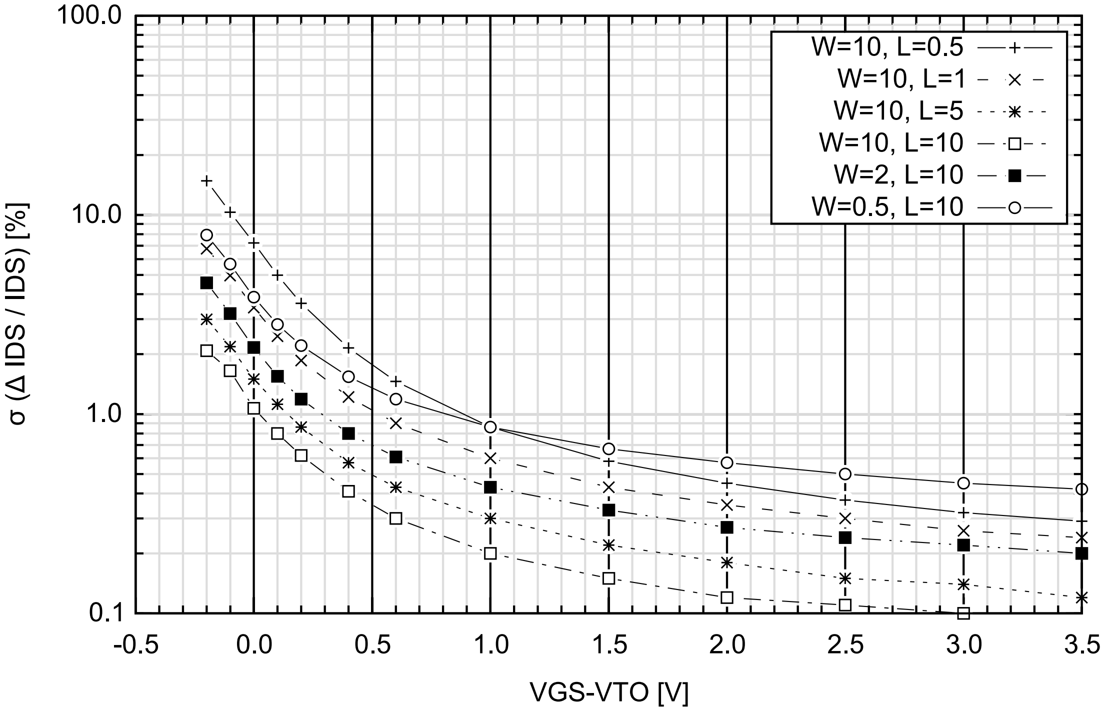

Figure 3.76 Device nd3i: drain current matching vs. VGS-VTO (typical values, drawn W and L)

nd3i_6

nd3i_6 is only available if DEPL and HVMOS modules are selected.

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-4	-3.6	3.6	4	V
VGD	-40°C to 175°C	-4	-3.6	3.6	4	V
VDS	-40°C to 175°C	-4	-3.6	3.6	4	V
VDB	-40°C to 175°C	-0.5	0	3.6	4	V
VSB	-40°C to 175°C	-0.5	0	3.6	4	V
VIB	-40°C to 175°C	-0.5	0	8	10	V
VIpsub	-40°C to 175°C	-0.5	0	45	50	V

Note: The node B (BULK) is: DEPL

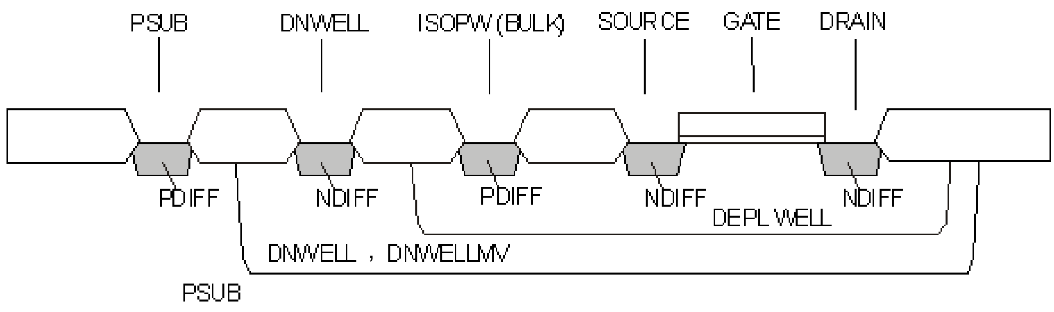

Figure 3.77 Additional Operating Conditions

Note: nd3i_6 in DNWELL

$$\begin{array}{lllll} V_{PSUB} & \leq & V_{DNWELL} & \leq & V_{PSUB} + 45(50)V \\ V_{DNWELL} - 8(10)V & \leq & V_{DEPLWELL} & \leq & V_{DNWELL} \end{array}$$

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSND3IS	drain-source breakdown @ VG=-3.3V, Id=1µA, L=0.7µm	-	5	-	-	-	V
BEXND3I	mobility exponent	-	-	-0.2	-	-	-
FC_ND3I	corner frequency @ VD=3.3V, Id=1µA, L=10µm, W=10µm	-	-	1.53	-	-	kHz
GAMND3IL	body factor long channel @ L=10µm, W=10µm	-	-	0.6	-	-	√V
IDSND3IS	saturation current @ VG=3.3V, VD=3.3V, L=0.7µm, W=10µm	640	690	740	790	840	µA/µm
ISBND3IS	bulk current @ VD=3.3V, L=0.7µm	-	-	0.17	-	-	µA/µm
KP_ND3IL	gain factor long channel @ L=10µm, W=10µm	-	-	210	-	-	µA/V²
LEFND3I	effective channel length @ L=0.7µm	-	-	0.65	-	-	µm
NOIND3I	Input referred noise @ VD=3.3V, Id=1µA, f=1Hz, L=10µm, W=10µm	-	-	12.9	-	-	µV.µm/√(Hz)
TC_VTXND3I	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	-1.3	-	-	mV/K
VTXND3IL	extrapolated threshold voltage long channel @ VD=0.1V, L=10µm, W=10µm	-	-0.42	-0.33	-0.24	-	V
VTXND3IS	extrapolated threshold voltage short channel @ VD=0.1V, L=0.7µm, W=10µm	-0.39	-0.32	-0.24	-0.16	-0.09	V
WEFND3I	effective channel width @ W=0.44µm	-	-	0.35	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTND3I	Pelgrom coefficient gain factor mismatch	0.88	%µm
AIDND3I00	Pelgrom coefficient ID mismatch @ VG-VT=0V	9.74	%µm
AIDND3I02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	5.41	%µm

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Name	Description	Typ	Unit
AIDND3I04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	3.57	%µm
AIDND3I06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	2.65	%µm
AIDND3I10	Pelgrom coefficient ID mismatch @ VG-VT=1V	1.8	%µm
AIDND3I15	Pelgrom coefficient ID mismatch @ VG-VT=1.5V	1.35	%µm
AIDND3I20	Pelgrom coefficient ID mismatch @ VG-VT=2V	1.12	%µm
AIDND3I30	Pelgrom coefficient ID mismatch @ VG-VT=3V	0.9	%µm
AVTND3I	Pelgrom coefficient VT mismatch	7.88	mVµm
DLTND3I	transistor delta length	0.05	µm
DWTND3I	transistor delta width	0.09	µm

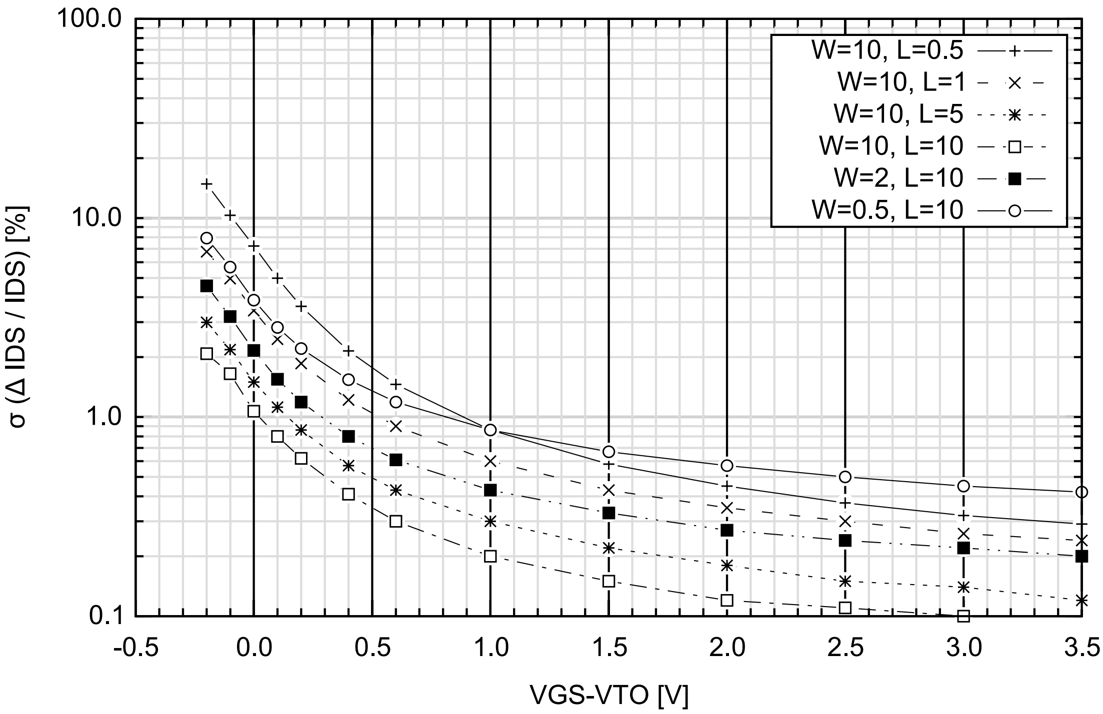

Figure 3.78 Device nd3i: drain current matching vs. VGS-VTO (typical values, drawn W and L)

nd3i_m_6

nd3i_m_6 is only available if DEPL and ISOMOS modules are selected.

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40 °C to 175 °C	-4	-3.6	3.6	4	V
VGD	-40 °C to 175 °C	-4	-3.6	3.6	4	V
VDS	-40 °C to 175 °C	-4	-3.6	3.6	4	V
VDB	-40 °C to 175 °C	-0.5	0	3.6	4	V
VSB	-40 °C to 175 °C	-0.5	0	3.6	4	V
VIpsub	-40 °C to 175 °C	-0.5	0	10	12	V
VIB	-40 °C to 175 °C	-0.5	0	8	10	V

Note: The node B (BULK) is: DEPL

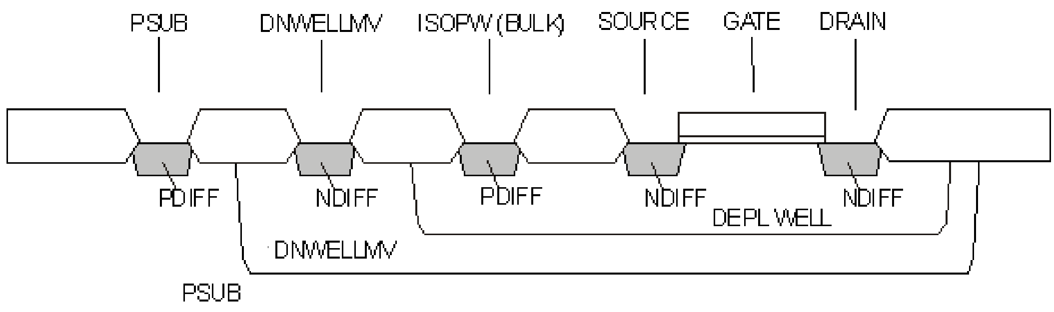

Figure 3.79 Additional Operating Conditions

Note: nd3i_m_6 in DNWELLMV

$$
\begin{array}{lclcl}
V_{PSUB} & \leq & V_{DNWELLMV} & \leq & V_{PSUB} + 10(12)V \\
V_{DNWELLV} - 8(10)V & \leq & V_{DEPLWELL} & \leq & V_{DNWELLMV}
\end{array}
$$

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSND3IS	drain-source breakdown @ VG=-3.3V, Id=1µA, L=0.7µm	-	5	-	-	-	V
BEXND3I	mobility exponent	-	-	-0.2	-	-	-
FC_ND3I	corner frequency @ VD=3.3V, Id=1µA, L=10µm, W=10µm	-	-	1.53	-	-	kHz
GAMND3IL	body factor long channel @ L=10µm, W=10µm	-	-	0.6	-	-	√V
IDSND3IS	saturation current @ VG=3.3V, VD=3.3V, L=0.7µm, W=10µm	640	690	740	790	840	µA/µm
ISBND3IS	bulk current @ VD=3.3V, L=0.7µm	-	-	0.17	-	-	µA/µm
KP_ND3IL	gain factor long channel @ L=10µm, W=10µm	-	-	210	-	-	µA/V²
LEFND3I	effective channel length @ L=0.7µm	-	-	0.65	-	-	µm
NOIND3I	Input referred noise @ VD=3.3V, Id=1µA, f=1Hz, L=10µm, W=10µm	-	-	12.9	-	-	µV.µm/ √(Hz)
TC_VTXND3I	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	-1.3	-	-	mV/K
VTXND3IL	extrapolated threshold voltage long channel @ VD=0.1V, L=10µm, W=10µm	-	-0.42	-0.33	-0.24	-	V
VTXND3IS	extrapolated threshold voltage short channel @ VD=0.1V, L=0.7µm, W=10µm	-0.39	-0.32	-0.24	-0.16	-0.09	V
WEFND3I	effective channel width @ W=0.44µm	-	-	0.35	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTND3I	Pelgrom coefficient gain factor mismatch	0.88	%µm
AIDND3I00	Pelgrom coefficient ID mismatch @ VG-VT=0V	9.74	%µm
AIDND3I02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	5.41	%µm
AIDND3I04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	3.57	%µm

⇒

Name	Description	Typ	Unit
AIDND3I06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	2.65	%µm
AIDND3I10	Pelgrom coefficient ID mismatch @ VG-VT=1V	1.8	%µm
AIDND3I15	Pelgrom coefficient ID mismatch @ VG-VT=1.5V	1.35	%µm
AIDND3I20	Pelgrom coefficient ID mismatch @ VG-VT=2V	1.12	%µm
AIDND3I30	Pelgrom coefficient ID mismatch @ VG-VT=3V	0.9	%µm
AVTND3I	Pelgrom coefficient VT mismatch	7.88	mVµm
DLTND3I	transistor delta length	0.05	µm
DWTND3I	transistor delta width	0.09	µm

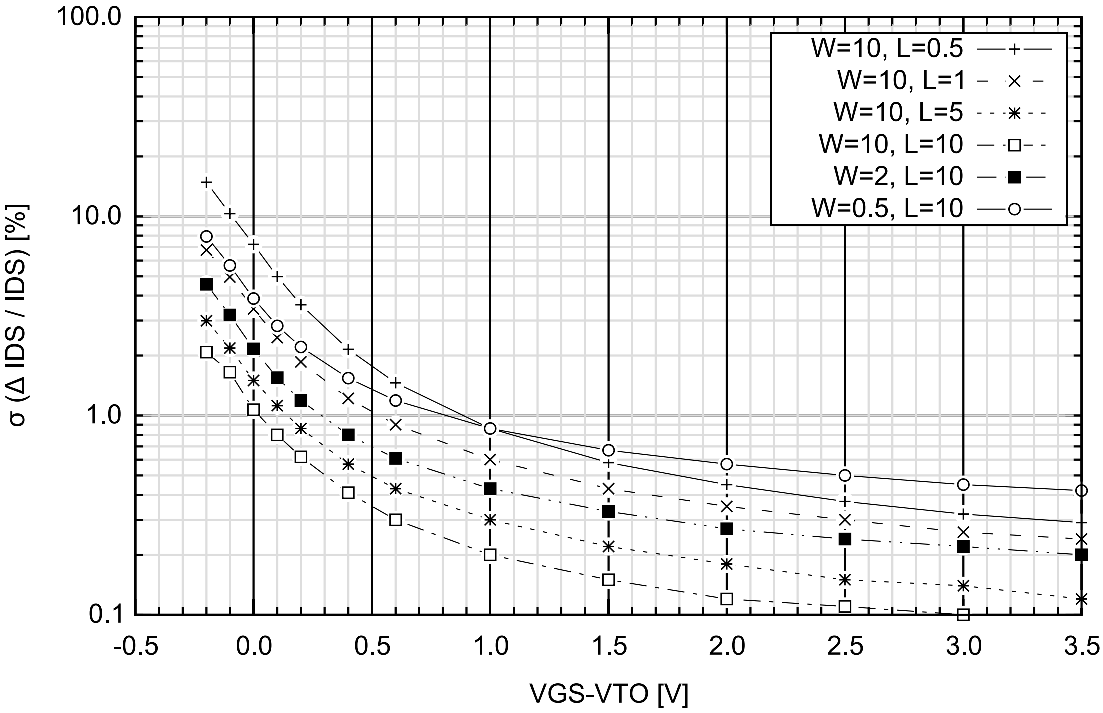

Figure 3.80 Device nd3i: drain current matching vs. VGS-VTO (typical values, drawn W and L)

qnva

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VCE	-40°C to 175°C	-4	-3.6	3.6	4	V
VEB	-40°C to 175°C	-	-1.5	2.5	3	V
VBC	-40°C to 175°C	-4	-3.6	1.5	-	V
VCS	-40°C to 175°C	-0.5	0	15	17	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BA_NVA	active breakdown voltage @ Ib=500nA	-	-	3.6	-	-	V
BCEONVA	collector- emitter breakdown voltage (base open) @ Ic=1µA	10	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						

⇒

Name	Description	LSL	Low	Typ	High	USL	Unit
EVFNVA	early voltage @ Ib=2µA	-	8	16	-	-	V
HFHNVA	high current beta @ VC=2V, Ib=200µA	-	-	15	-	-	-
HFMNVA	current gain @ Ib=0.1µA	-	21	-	-	-	-
IEBNVA	emitter- base leakage current @ VE=2V	-	-	-	5	-	nA/µm
TC_VBENVA	base- emitter voltage temperature coefficient	-	-	-1.6	-	-	mV/K
VBENVA	base- emitter voltage @ VC=2V, Ib=0.1µA	690	700	710	720	730	mV

Note: The parameters are specified for the drawn emitter length of 3 µm.

Matching parameters

Name	Description	Typ	Unit
SIBNVA101	standard deviation IB mismatch @ Ic=100nA, LE=10µm	3.74	%
SIBNVA102	standard deviation IB mismatch @ Ic=100µA, LE=10µm	0.72	%
SIBNVA31	standard deviation IB mismatch @ Ic=100nA, LE=3µm	4.2	%
SIBNVA32	standard deviation IB mismatch @ Ic=100µA, LE=3µm	1.09	%
SIBNVA51	standard deviation IB mismatch @ Ic=100nA, LE=5µm	3.63	%
SIBNVA52	standard deviation IB mismatch @ Ic=100µA, LE=5µm	0.93	%
SICNVA101	standard deviation IC mismatch @ Ic=100nA, LE=10µm	0.57	%
SICNVA102	standard deviation IC mismatch @ Ic=100µA, LE=10µm	0.34	%
SICNVA31	standard deviation IC mismatch @ Ic=100nA, LE=3µm	0.67	%
SICNVA32	standard deviation IC mismatch @ Ic=100µA, LE=3µm	0.45	%
SICNVA51	standard deviation IC mismatch @ Ic=100nA, LE=5µm	0.63	%
SICNVA52	standard deviation IC mismatch @ Ic=100µA, LE=5µm	0.38	%
SVBNVA101	standard deviation VBE mismatch @ Ic=100nA, LE=10µm	0.08	mV
SVBNVA102	standard deviation VBE mismatch @ Ic=100µA, LE=10µm	0.29	mV
SVBNVA31	standard deviation VBE mismatch @ Ic=100nA, LE=3µm	0.14	mV
SVBNVA32	standard deviation VBE mismatch @ Ic=100µA, LE=3µm	0.28	mV
SVBNVA51	standard deviation VBE mismatch @ Ic=100nA, LE=5µm	0.11	mV
SVBNVA52	standard deviation VBE mismatch @ Ic=100µA, LE=5µm	0.29	mV

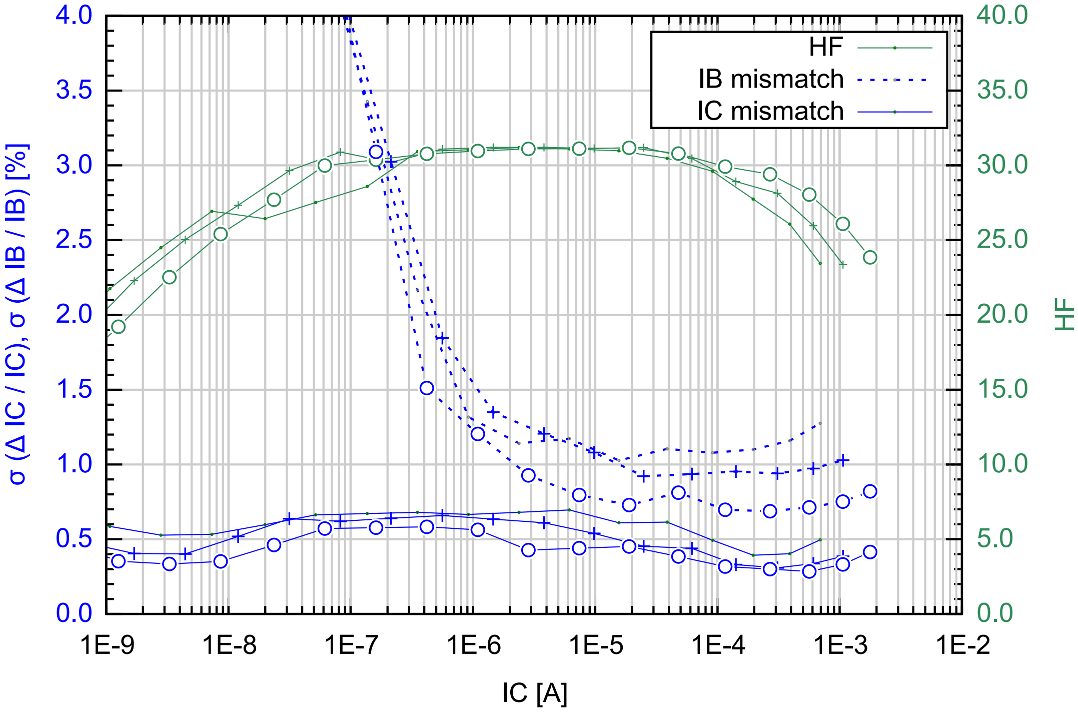

Figure 3.81 Device qnva: IC matching and IB matching vs. IC (typical values) ----- LE=3µm, --+-- LE=5µm, --o-- LE=10µm

qnvb

This device is only available if DEPL and ISOMOS or DEPL and HVMOS modules are selected.

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VCE	-40°C to 175°C	-4	-3.6	3.6	4	V
VEB	-40°C to 175°C	-	-1.5	2.5	3	V
VBC	-40°C to 175°C	-4	-3.6	1.5	-	V
VCS	-40°C to 175°C	-0.5	0	15	17	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BA_NVB	active breakdown voltage @ Ib=500nA	-	-	4.5	-	-	V
BCEONVB	collector- emitter breakdown voltage (base open) @ Ic=1µA	4.5	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
EVFNVB	early voltage @ Ib=2µA	-	4	8.5	-	-	V
HFHNVB	high current beta @ VC=2V, Ib=200µA	-	-	15	-	-	-
HFMNVB	current gain @ Ib=0.1µA	-	40	85	-	-	-
IEBNVB	emitter- base leakage current @ VE=2V	-	-	-	0.1	-	nA/µm
TC_VBENVB	base- emitter voltage temperature coefficient	-	-	-1.7	-	-	mV/K

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Name	Description	LSL	Low	Typ	High	USL	Unit
VBENVB	base- emitter voltage @ VC=2V, Ib=0.1µA	690	695	700	705	710	mV

Note: The parameters are specified for the drawn emitter length of 3 µm.

Matching parameters

Name	Description	Typ	Unit
SIBNVB101	standard deviation IB mismatch @ Ic=100nA, LE=10µm	2	%
SIBNVB102	standard deviation IB mismatch @ Ic=100µA, LE=10µm	0.65	%
SIBNVB31	standard deviation IB mismatch @ Ic=100nA, LE=3µm	2.4	%
SIBNVB32	standard deviation IB mismatch @ Ic=100µA, LE=3µm	1.14	%
SIBNVB501	standard deviation IB mismatch @ Ic=100nA, LE=50µm	1.43	%
SIBNVB502	standard deviation IB mismatch @ Ic=100µA, LE=50µm	0.5	%
SICNVB101	standard deviation IC mismatch @ Ic=100nA, LE=10µm	0.95	%
SICNVB102	standard deviation IC mismatch @ Ic=100µA, LE=10µm	0.64	%
SICNVB31	standard deviation IC mismatch @ Ic=100nA, LE=3µm	1.41	%
SICNVB32	standard deviation IC mismatch @ Ic=100µA, LE=3µm	0.92	%
SICNVB501	standard deviation IC mismatch @ Ic=100nA, LE=50µm	0.68	%
SICNVB502	standard deviation IC mismatch @ Ic=100µA, LE=50µm	0.45	%
SVBNVB101	standard deviation VBE mismatch @ Ic=100nA, LE=10µm	0.27	mV
SVBNVB102	standard deviation VBE mismatch @ Ic=100µA, LE=10µm	0.37	mV
SVBNVB31	standard deviation VBE mismatch @ Ic=100nA, LE=3µm	0.43	mV
SVBNVB32	standard deviation VBE mismatch @ Ic=100µA, LE=3µm	0.42	mV
SVBNVB501	standard deviation VBE mismatch @ Ic=100nA, LE=50µm	0.14	mV
SVBNVB502	standard deviation VBE mismatch @ Ic=100µA, LE=50µm	0.32	mV

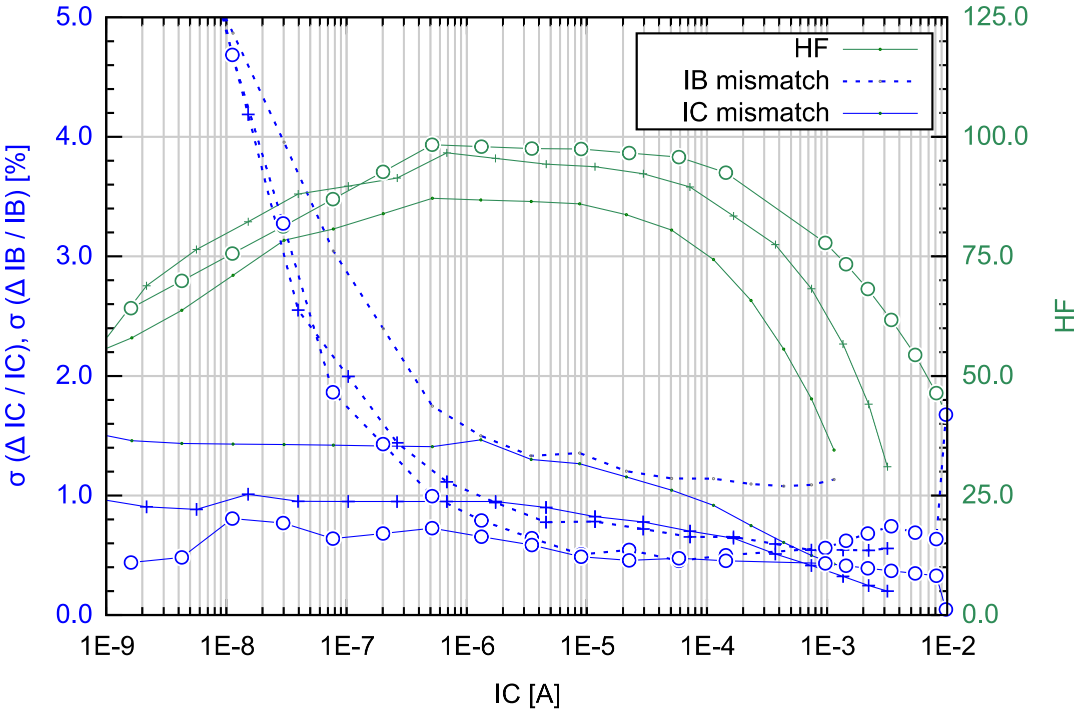

Figure 3.82 Device qnvb: IC matching and IB matching vs. IC (typical values) ----- LE=3µm, --+-- LE=10µm, --o-- LE=50µm

p_dn3dpl

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVJNDPL	breakdown voltage NDIFF / DEPL @ Irev=1µA	6	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BVJPDPLNW	breakdown voltage DEPL / NWELL @ Irev=-1µA	9	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CJANDPL	area junction capacitance	-	-	0.95	-	-	fF/µm²
CJPNDPL	sidewall junction capacitance	-	-	0.11	-	-	fF/µm
ILANDPL	area leakage current @ Vrev=3.6V, T=27°C	-	-	0.008	-	-	fA/µm²
ILANDPLHT	area leakage current @ Vrev=3.6V, T=175°C	-	-	0.75	-	-	pA/µm²
ILPNDPL	sidewall leakage current @ Vrev=3.6V, T=27°C	-	-	0.391	-	-	fA/µm
ILPNDPLHT	sidewall leakage current @ Vrev=3.6V, T=175°C	-	-	1.08	-	-	pA/µm
MJANDPL	area grading coefficient	-	-	0.33	-	-	-
MJPNDPL	sidewall grading coefficient	-	-	0.18	-	-	-
PBANDPL	area junction potential	-	-	0.72	-	-	V
PBPNDPL	sidewall junction potential	-	-	0.73	-	-	V

p_ddpldnw

This device is only available if DEPL and HVMOS modules are selected.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVJPDPLNWD	breakdown voltage DEPL / DNWELL @ Irev=-1µA	15	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CJAPDPLNWD	area junction capacitance	-	-	0.34	-	-	fF/µm²
CJPPDPLNWD	sidewall junction capacitance	-	-	0.46	-	-	fF/µm
ILAPDPLNWD	area leakage current @ Vrev=-8V, T=27°C	-	-	0.001	-	-	fA/µm²
ILAPDPLNWDHT	area leakage current @ Vrev=-8V, T=175°C	-	-	0.28	-	-	pA/µm²
ILPPDPLNWD	sidewall leakage current @ Vrev=-8V, T=27°C	-	-	0.184	-	-	fA/µm
ILPPDPLNWDHT	sidewall leakage current @ Vrev=-8V, T=175°C	-	-	0.5	-	-	pA/µm
MJAPDPLNWD	area grading coefficient	-	-	0.49	-	-	-
MJPPDPLNWD	sidewall grading coefficient	-	-	0.53	-	-	-
PBAPDPLNWD	area junction potential	-	-	0.59	-	-	V
PBPPDPLNWD	sidewall junction potential	-	-	0.59	-	-	V

3.18 HVDEPL module

3.18.1 Device independent parameters

Structural and geometrical parameters

Name	Description	Typ	Unit
XJ_HDEPL	HV Depletion in HVPWELL junction depth	0.1	µm

3.18.2 Device parameters

nhvd, nhvd_bjt

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-20	-18	18	20	V
VGB	-40°C to 175°C	-20	-18	18	20	V
VGD	-40°C to 175°C	-50	-45	18	20	V
VDS	-40°C to 175°C	-7	-5	32	45	V
VDB	-40°C to 175°C	-0.3	0	32	45	V
VSB	-40°C to 175°C	-0.3	0	5	7	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNHVD	drain-source breakdown @ VG=-5V, Id=1µA	50	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BDSONNHVD	on-state drain-source breakdown @ VG=18V, Id=1µA, L=3µm	-	-	22	-	-	V
ID0NHVD	saturation current @ VG=0V, VD=20V, L=3µm	2.1	4.8	7.5	10.2	12.9	µA/µm
IDSNHVD18	saturation current @ VG=18V, VD=20V, L=3µm, W=20µm	-	-	160	-	-	µA/µm
IDSNHVD5	saturation current @ VG=5V, VD=20V, L=3µm, W=20µm	-	-	110	-	-	µA/µm
ROANHVD18	area specific on-resistance @ VG=18V, VD=0.1V, L=3µm, Pitch=6.48µm	-	-	167	-	-	mΩmm²
RO_NHVD18	on-resistance @ VG=18V, VD=0.1V, L=3µm	20	23.5	27	30.5	34	kΩµm
RO_NHVD5	on-resistance @ VG=5V, VD=0.1V, L=3µm	-	-	37	-	-	kΩµm
TC_VTXNHVD	threshold voltage temperature coefficient @ Tnom=27°C	-	-	-3	-	-	mV/K
VTXNHVDL	extrapolated threshold voltage long channel @ VD=0.1V, L=10µm, W=20µm	-	-	-1.1	-	-	V
VTXNHVDS	extrapolated threshold voltage short channel @ VD=0.1V, L=3µm, W=20µm	-	-	-1.15	-	-	V

nhhvd, nhhvd_bjt

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-20	-18	18	20	V
VGB	-40°C to 175°C	-20	-18	18	20	V
VGD	-40°C to 175°C	-50	-45	18	20	V
VDS	-40°C to 175°C	-45	-32	32	45	V
VDB	-40°C to 175°C	-0.3	0	32	45	V
VSB	-40°C to 175°C	-0.3	0	32	35	V

Process parameters

Name	Description	Low	Typ	High	Unit
BDSNHHVD	drain-source breakdown @ VG=-5V, Id=1µA	50	-	-	V
BDSONNHHVD	on-state drain-source breakdown @ VG=18V, Id=1µA, L=5µm	-	40	-	V
ID0NHHVD	saturation current @ VG=0V, VD=20V, L=5µm	-	3	-	µA/µm
IDSNHHVD18	saturation current @ VG=18V, VD=20V, L=5µm, W=20µm	-	90	-	µA/µm
IDSNHHVD5	saturation current @ VG=5V, VD=20V, L=5µm, W=20µm	-	45	-	µA/µm
ROANHHVD18	area specific on-resistance @ VG=18V, VD=0.1V, L=5µm, Pitch=11.42µm	-	514	-	mΩmm²
RO_NHHVD18	on-resistance @ VG=18V, VD=0.1V, L=5µm	-	53	-	kΩµm
RO_NHHVD5	on-resistance @ VG=5V, VD=0.1V, L=5µm	-	70	-	kΩµm
TC_VTXNHHVD	threshold voltage temperature coefficient @ Tnom=27°C, L=10µm, W=20µm	-	-3.6	-	mV/K
VTXNHHVDL	extrapolated threshold voltage long channel @ VD=0.1V, L=10µm, W=20µm	-	-0.9	-	V
VTXNHHVDS	extrapolated threshold voltage short channel @ VD=0.1V, L=5µm, W=20µm	-	-1	-	V

3.19 DMOS module

3.19.1 Device parameters

nedi, nedi_bjt

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-20	-18	18	20	V
VGD	-40°C to 175°C	-45	-40	18	20	V
VDS	-40°C to 175°C	-0.5	0	40	45	V
VDpsub	-40°C to 175°C	-0.5	0	40	45	V
VSpsub	-40°C to 175°C	-0.5	0	40	45	V

Note: The node B (BULK) is: HVPWELL

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNEDI	drain-source breakdown @ VG=0V, Id=1µA, L=0.65µm	45.5	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BDSONNEDI	on-state drain-source breakdown @ VG=18V, L=0.65µm	-	-	22	-	-	V
BPRNEDI	Punch-through voltage (reverse) with open drain @ Ip=-1µA, L=0.65µm, W=90µm	-	20	-	-	-	V
BVPNEDI	HV PWELL- DNWELL- PSUB punch through voltage @ Ip=1µA	55	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
IDSNEDI5	saturation current @ VG=5V, VD=20V, L=0.65µm, W=90µm	90	100	110	120	130	µA/µm
ROANEDI10	area specific on-resistance @ VG=10V, VD=0.1V, L=0.65µm, W=90µm, Pitch=3.81µm	40	50	60	70	80	mΩmm²
	Note: The value is calculated for a transistor having minimum source drain pitch. Design related bulk contacts and metal resistances are not included.						
RO_NEDI10	on-resistance @ VG=10V, VD=0.1V, L=0.65µm, W=90µm	-	-	15	-	-	kΩµm
RO_NEDI5	on-resistance @ VG=5V, VD=0.1V, L=0.65µm, W=90µm	-	-	19	-	-	kΩµm
TC_VTXNEDI	threshold voltage temperature coefficient @ L=0.65µm, W=90µm	-	-	-2.9	-	-	mV/K
VT1NEDI	snap-back trigger voltage @ VGS=18V, W=400µm, Ngates=8	-	-	20	-	-	V
	Note: For detailed TLP I-V characteristics, refer to "XH018 Technical Report MOS TLP Characteristics" at "my X-FAB"						
VTINEDI	threshold voltage @ VD=0.1V, L=0.65µm, W=90µm	-	-	1.63	-	-	V
VTXNEDI	extrapolated threshold voltage @ VD=0.1V, L=0.65µm, W=90µm	1.3	1.45	1.6	1.75	1.9	V

Matching parameters

Name	Description	Typ	Unit
ABTNEDI	Pelgrom coefficient gain factor mismatch	2.55	%µm
AIDNEDI00	Pelgrom coefficient ID mismatch @ VG-VT=0V	25.4	%µm
AIDNEDI02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	14.9	%µm
AIDNEDI04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	9.74	%µm
AIDNEDI06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	6.98	%µm
AIDNEDI10	Pelgrom coefficient ID mismatch @ VG-VT=1V	4.29	%µm
AIDNEDI20	Pelgrom coefficient ID mismatch @ VG-VT=2V	2.11	%µm
AIDNEDI30	Pelgrom coefficient ID mismatch @ VG-VT=3V	1.97	%µm
AIDNEDI50	Pelgrom coefficient ID mismatch @ VG-VT=5V	3.03	%µm
AVTNEDI	Pelgrom coefficient VT mismatch	26.5	mVµm
DLTNEDI	transistor delta length	0.02	µm
DWTNEDI	transistor delta width	0.02	µm

nedia, nedia_bjt

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-20	-18	18	20	V
VGD	-40°C to 175°C	-50	-45	18	20	V
VDS	-40°C to 175°C	-0.5	0	45	50	V
VDpsub	-40°C to 175°C	-0.5	0	45	50	V
VSpsub	-40°C to 175°C	-0.5	0	45	50	V

Note: The node B (BULK) is: HVPWELL

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNEDIA	drain-source breakdown @ VG=0V, Id=1µA, L=1.25µm	55	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BDSONNEDIA	on-state drain-source breakdown @ VG=18V, L=1.25µm	-	-	50	-	-	V
BPRNEDIA	Punch-through voltage (reverse) with open drain @ Ip=-1µA, L=1.25µm, W=80µm	-	18	-	-	-	V
BVPNEDIA	HV PWELL- PSUB punch through voltage @ Ip=1µA	55	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
IDSNEDIA5	saturation current @ VG=5V, VD=20V, L=1.25µm, W=80µm	62	72	82	92	102	µA/µm
ROANEDIA10	area specific on-resistance @ VG=10V, VD=0.1V, L=1.25µm, W=80µm, Pitch=5.95µm	74	94	114	134	154	mΩmm²
	Note: The value is calculated for a transistor having minimum source drain pitch. Design related bulk contacts and metal resistances are not included.						
RO_NEDIA10	on-resistance @ VG=10V, VD=0.1V, L=1.25µm, W=80µm	-	-	19	-	-	kΩµm

⇒

Name	Description	LSL	Low	Typ	High	USL	Unit
RO_NEDIA5	on-resistance @ VG=5V, VD=0.1V, L=1.25µm, W=80µm	-	-	25	-	-	kΩµm
TC_VTXNEDIA	threshold voltage temperature coefficient @ L=1.25µm, W=80µm	-	-	-3.1	-	-	mV/K
VT1NEDIA	snap-back trigger voltage @ VGS=18V, W=400µm, Ngates=8	-	-	47	-	-	V
	Note: For detailed TLP I-V characteristics, refer to "XH018 Technical Report MOS TLP Characteristics" at "my X-FAB"						
VTINEDIA	threshold voltage @ VD=0.1V, L=1.25µm, W=80µm	-	-	1.65	-	-	V
VTXNEDIA	extrapolated threshold voltage @ VD=0.1V, L=1.25µm, W=80µm	1.3	1.45	1.6	1.75	1.9	V

Note: nedia has better ESD protection capability than nedi. Please refer to the ESD document "XH018 TLP I-V Characteristics" at "my X-FAB."

Matching parameters

Name	Description	Typ	Unit
ABTNEDIA	Pelgrom coefficient gain factor mismatch	4.06	%µm
AIDNEDIA00	Pelgrom coefficient ID mismatch @ VG-VT=0V	33.4	%µm
AIDNEDIA02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	19.6	%µm
AIDNEDIA04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	12.7	%µm
AIDNEDIA06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	9.18	%µm
AIDNEDIA10	Pelgrom coefficient ID mismatch @ VG-VT=1V	5.79	%µm
AIDNEDIA20	Pelgrom coefficient ID mismatch @ VG-VT=2V	3.06	%µm
AIDNEDIA30	Pelgrom coefficient ID mismatch @ VG-VT=3V	3.38	%µm
AIDNEDIA50	Pelgrom coefficient ID mismatch @ VG-VT=5V	4.98	%µm
AVTNEDIA	Pelgrom coefficient VT mismatch	43.5	mVµm
DLTNEDIA	transistor delta length	0.1	µm
DWTNEDIA	transistor delta width	-19	µm

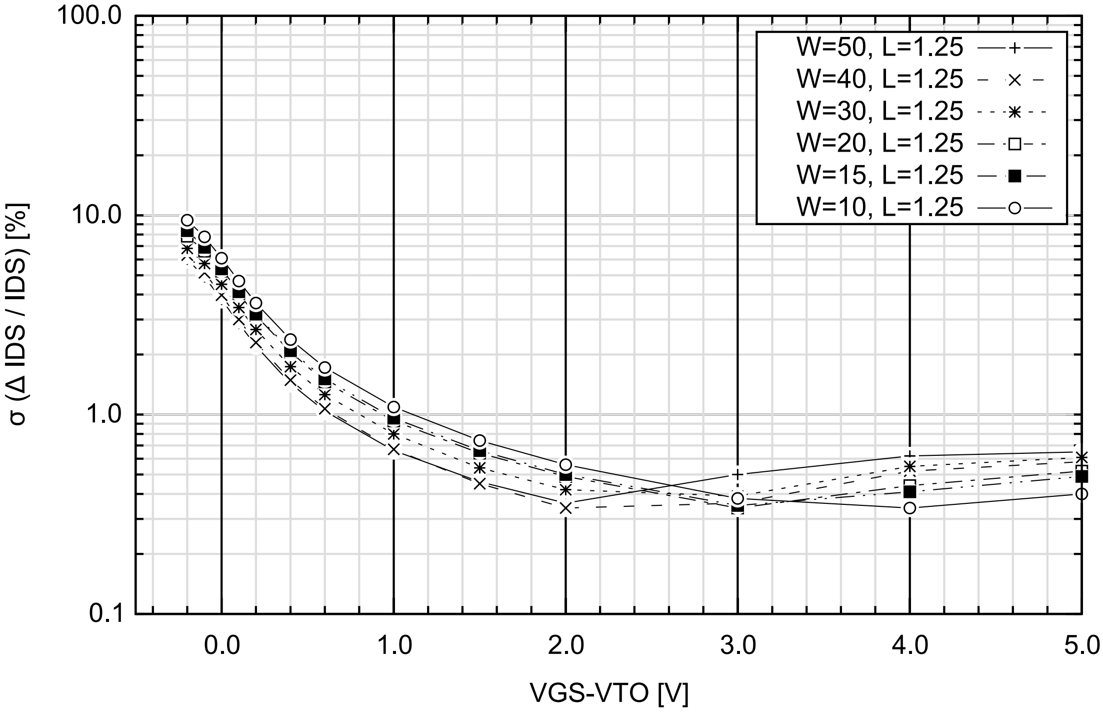

Figure 3.83 Device nedia: drain current matching vs. VGS-VTO (typical values, drawn W and L)

ped2, ped2_bjt

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-20	-18	18	20	V
VGD	-40°C to 175°C	-20	-18	35	40	V
VDS	-40°C to 175°C	-40	-35	0	0.5	V
VDB	-40°C to 175°C	-40	-35	0	0.5	V
VDpsub	-40°C to 175°C	-12	-10	35	40	V
VBpsub	-40°C to 175°C	-0.5	0	35	40	V

Note: The node B (BULK) is: HVNWELL

Process parameters

Negative values are considered as absolute values for their limits.

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPED2	drain-source breakdown @ VSUB=0V, Id=-1µA, L=0.94µm	40.5	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BPRPED2	Punch-through voltage (reverse) with open bulk @ Ip=-1µA, L=0.94µm, W=90µm	-	10	-	-	-	V
BVPPED2	PDD - DNWELL - PSUB punch through voltage @ Ip=1µA	51	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
IDSPED2_5	saturation current @ VG=-5V, VD=-20V, L=0.94µm, W=90µm	26	36	46	56	66	µA/µm

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Name	Description	LSL	Low	Typ	High	USL	Unit
ROAPED2	area specific on-resistance @ VG=-10V, VD=-0.1V, L=0.94µm, W=90µm, Pitch=4.385µm	-	162	185	208	230	mΩmm²
	Note: The value is calculated for a transistor having minimum source drain pitch. Design related bulk contacts and metal resistances are not included.						
RO_PED2_10	on-resistance @ VG=-10V, VD=-0.1V, L=0.94µm, W=90µm	-	-	42	-	-	kΩµm
RO_PED2_5	on- resistance @ VG=-5V, VD=-0.1V, L=0.94µm, W=90µm	-	-	57	-	-	kΩµm
TC_VTXPED2	threshold voltage temperature coefficient @ L=0.94µm, W=90µm	-	-	3.3	-	-	mV/K
VTIPED2	threshold voltage @ VD=-0.1V, L=0.94µm, W=90µm	-	-	-2	-	-	V
VTXPED2	extrapolated threshold voltage @ VD=-0.1V, L=0.94µm, W=90µm	-1.6	-1.85	-2.1	-2.35	-2.6	V

Matching parameters

Name	Description	Typ	Unit
ABTPED2	Pelgrom coefficient gain factor mismatch	4.16	%µm
AIDPED200	Pelgrom coefficient ID mismatch @ VG-VT=0V	25.5	%µm
AIDPED202	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	16.9	%µm
AIDPED204	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	11.9	%µm
AIDPED206	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	8.94	%µm
AIDPED210	Pelgrom coefficient ID mismatch @ VG-VT=1V	5.81	%µm
AIDPED220	Pelgrom coefficient ID mismatch @ VG-VT=2V	3.01	%µm
AIDPED230	Pelgrom coefficient ID mismatch @ VG-VT=3V	1.96	%µm
AIDPED250	Pelgrom coefficient ID mismatch @ VG-VT=5V	1.77	%µm
AVTPED2	Pelgrom coefficient VT mismatch	44	mVµm
DLTPED2	transistor delta length	0.02	µm
DWTPED2	transistor delta width	0.02	µm

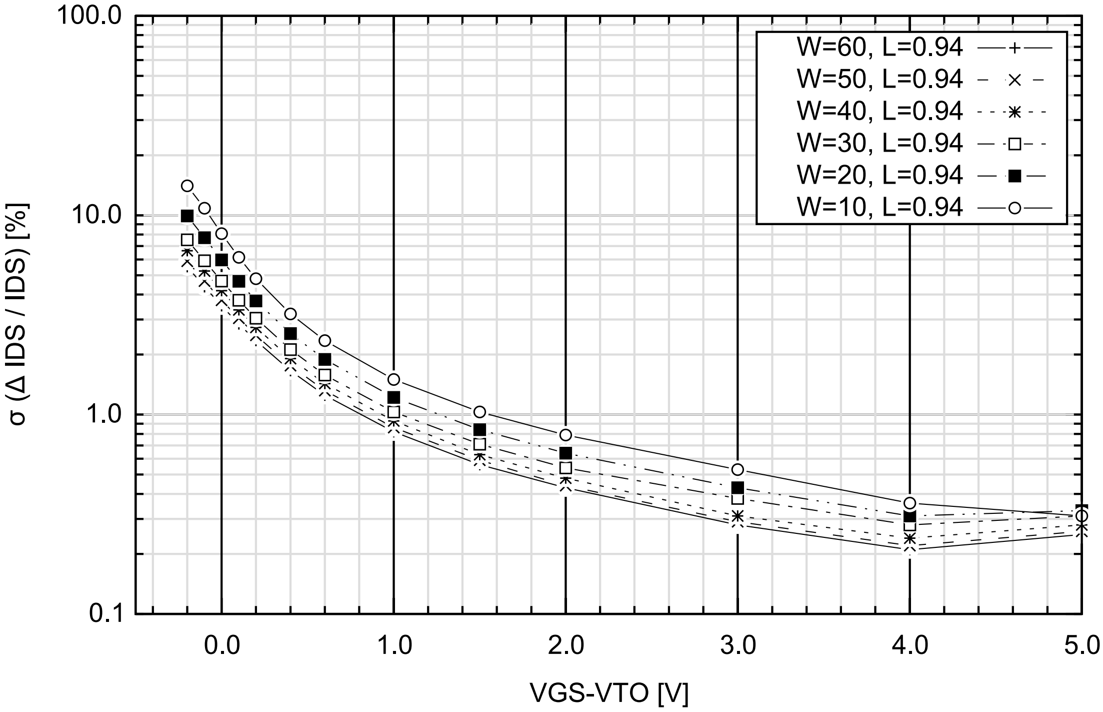

Figure 3.84 Device ped2: drain current matching vs. VGS-VTO (typical values, drawn W and L)

ped, ped_bjt

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40 °C to 175 °C	-20	-18	18	20	V
VGD	-40 °C to 175 °C	-20	-18	45	50	V
VDS	-40 °C to 175 °C	-50	-45	0	0.5	V
VDB	-40 °C to 175 °C	-50	-45	0	0.5	V
VDpsub	-40 °C to 175 °C	-12	-10	45	50	V
VBpsub	-40 °C to 175 °C	-0.5	0	45	50	V

Note: The node B (BULK) is: HVNWELL

Process parameters

Negative values are considered as absolute values for their limits.

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPED	drain-source breakdown @ VSUB=0V, Id=-1µA, L=0.94µm	50.5	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BPRPED	Punch-through voltage (reverse) with open bulk @ Ip=-1µA, L=0.94µm, W=90µm	-	10	-	-	-	V
BVPPED	PDD- DNWELL- PSUB punch through voltage @ Ip=1µA	51	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
IDSPED5	saturation current @ VG=-5V, VD=-20V, L=0.94µm, W=90µm	21	31	41	51	61	µA/µm

⇒

Name	Description	LSL	Low	Typ	High	USL	Unit
ROAPED	area specific on-resistance @ VG=-10V, VD=-0.1V, L=0.94µm, W=90µm, Pitch=4.4µm	-	-	215	240	260	mΩmm²
	Note: The value is calculated for a transistor having minimum source drain pitch. Design related bulk contacts and metal resistances are not included.						
RO_PED10	on-resistance @ VG=-10V, VD=-0.1V, L=0.94µm, W=90µm	-	-	48	-	-	kΩµm
RO_PED5	on- resistance @ VG=-5V, VD=-0.1V, L=0.94µm, W=90µm	-	-	61	-	-	kΩµm
TC_VTXPED	threshold voltage temperature coefficient @ L=0.94µm, W=90µm	-	-	3.2	-	-	mV/K
VTIPED	threshold voltage @ VD=-0.1V, L=0.94µm, W=90µm	-	-	-1.95	-	-	V
VTXPED	extrapolated threshold voltage @ VD=-0.1V, L=0.94µm, W=90µm	-1.6	-1.85	-2.1	-2.35	-2.6	V

Matching parameters

Name	Description	Typ	Unit
ABTPED	Pelgrom coefficient gain factor mismatch	6.82	%µm
AIDPED00	Pelgrom coefficient ID mismatch @ VG-VT=0V	30.3	%µm
AIDPED02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	20.4	%µm
AIDPED04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	14.7	%µm
AIDPED06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	11.2	%µm
AIDPED10	Pelgrom coefficient ID mismatch @ VG-VT=1V	7.43	%µm
AIDPED20	Pelgrom coefficient ID mismatch @ VG-VT=2V	3.95	%µm
AIDPED30	Pelgrom coefficient ID mismatch @ VG-VT=3V	2.55	%µm
AIDPED50	Pelgrom coefficient ID mismatch @ VG-VT=5V	2.28	%µm
AVTPED	Pelgrom coefficient VT mismatch	61.8	mVµm
DLTPED	transistor delta length	0	µm
DWTPED	transistor delta width	-2	µm

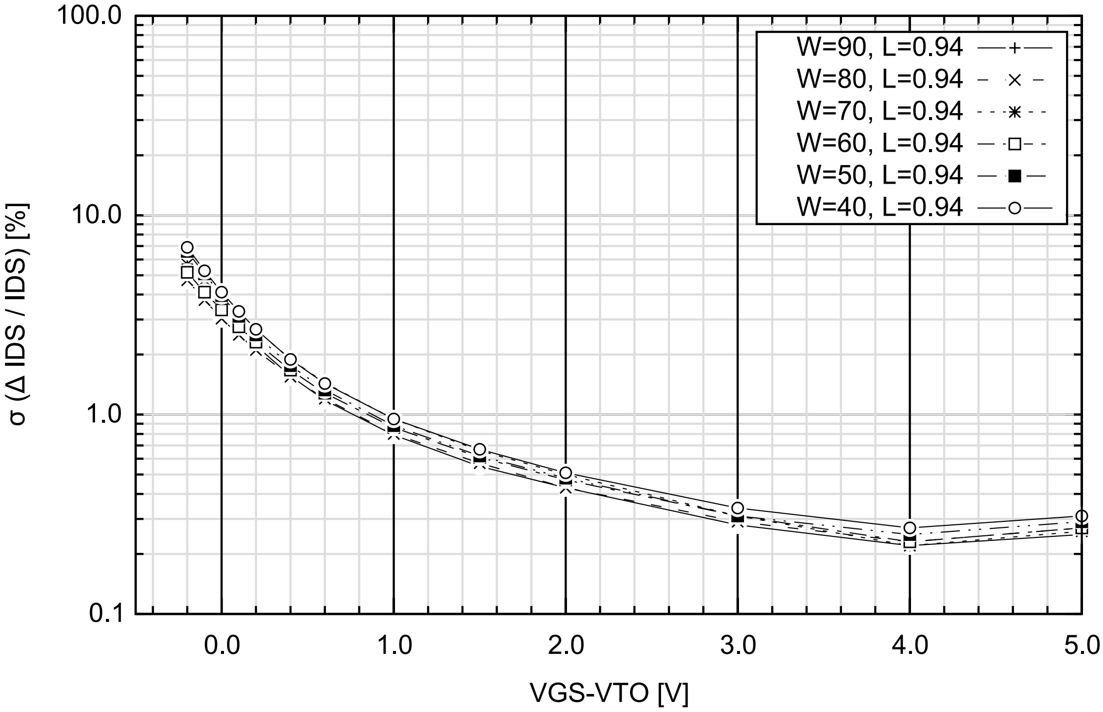

Figure 3.85 Device ped: drain current matching vs. VGS-VTO (typical values, drawn W and L)

p_dpdddnw

Process parameters

Name	Description	Typ	Unit
CJAPDDNWD	area junction capacitance	0.7	fF/µm²
CJPPDDNWD	sidewall junction capacitance	0.04	fF/µm
ILAPDDNWD	area leakage current @ Vrev=-45V, T=27°C	0.0001	fA/µm²
ILAPDDNWDHT	area leakage current @ Vrev=-45V, T=175°C	0.4	pA/µm²
ILPPDDNWD	sidewall leakage current @ Vrev=-45V, T=27°C	3.805	fA/µm
ILPPDDNWDHT	sidewall leakage current @ Vrev=-45V, T=175°C	5.9	pA/µm
MJAPDDNWD	area grading coefficient	0.95	-
MJPPDDNWD	sidewall grading coefficient	0.12	-
PBAPDDNWD	area junction potential	0.9	V
PBPPDDNWD	sidewall junction potential	1.2	V

3.20 HVMOS module

3.20.1 Device independent parameters

Structural and geometrical parameters

Name	Description	Low	Typ	High	Unit
THGHN	HV gate oxide thickness (measured on NMOS capacitor)	38.6	40.6	42.6	nm
THGHP	HV gate oxide thickness (measured on PMOS capacitor)	38.6	40.6	42.6	nm
XJ_DNW	DNWELLMV/DNWELL junction depth	-	2.8	-	µm
XJ_HNW	HVNWELL junction depth	-	1.8	-	µm
XJ_HPWDNW	HVPWELL in DNWELL junction depth	-	1.3	-	µm
XJ_NHPW	N+ source/ drain junction depth in HVPWELL	-	0.2	-	µm
XJ_PHNW	P+ source/ drain junction depth in HVNWELL	-	0.2	-	µm
XJ_PW1DNW	PWELL1 in DNWELLMV/DNWELL junction depth	-	1	-	µm
	Note: This parameter is only available if the HVMOS and ISOMOS modules are selected.				
XJ_PW2DNW	PWELL2 in DNWELLMV/DNWELL junction depth	-	1	-	µm
	Note: This parameter is only available if the HVMOS and ISOMOS modules are selected.				

Parasitic field parameters

Negative values are considered as absolute values for their limits.

Name	Description	Low	Typ	High	Unit
VTFPM1HNW	p-channel threshold voltage metal 1 on field over HVNWELL @ VD=-12V, Id=-1µA, L=0.28µm, W=210µm	-40	-	-	V
VTFPM2HNW	p-channel threshold voltage metal 2 on field over HVNWELL @ VD=-12V, Id=-1µA, L=0.28µm, W=210µm	-70	-	-	V
VTFPP1HNW	p-channel threshold voltage poly 1 on field over HVNWELL @ VD=-12V, Id=-1µA, L=0.28µm, W=210µm	-8	-	-	V

Sheet and contact resistance parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSSHNW	HVNWELL sheet resistance (STI terminated) @ W=20µm	0.79	0.84	0.89	0.94	0.99	kΩ/☐
RSSNWD	DNWELL sheet resistance (STI terminated) @ W=10µm	1.2	1.35	1.5	1.65	1.8	kΩ/☐
RSSNWDMV	DNWELLMV sheet resistance (STI terminated) @ Vterm=3.3V, W=10µm	1.2	1.35	1.5	1.65	1.8	kΩ/☐
RSSPW1DNW	PWELL1 in DNWELLMV/DNWELL sheet resistance, (STI terminated) @ W=20µm	2.4	2.65	2.9	3.15	3.4	kΩ/☐
	Note: This parameter is only available if the HVMOS and ISOMOS modules are selected.						
RSSPW2DNW	PWELL2 in DNWELLMV/DNWELL sheet resistance, (STI terminated) @ W=20µm	2.5	2.75	3	3.25	3.5	kΩ/☐
	Note: This parameter is only available if the HVMOS and ISOMOS modules are selected.						

Gate oxide parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDONH	HV NMOS gate oxide breakdown voltage @ Ibr=0.1nA/µm²	30	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BDOPH	HV PMOS gate oxide breakdown voltage @ Ibr=0.1nA/µm²	30	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CGANH	HV NMOS gate oxide area capacitance @ Vbias=8V	-	0.81	0.85	0.89	-	fF/µm²
CGAPH	HV PMOS gate oxide area capacitance @ Vbias=-8V	0.77	0.81	0.85	0.89	0.94	fF/µm²
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CGONH	HV NMOS gate – source/drain overlap	-	-	0.48	-	-	fF/µm
CGOPH	HV PMOS gate – source/drain overlap	-	-	0.48	-	-	fF/µm

3.20.2 Device parameters

nmma, nmma_bjt

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-12	-10	10	12	V
VGD	-40°C to 175°C	-12	-10	10	12	V
VDS	-40°C to 175°C	-12	-10	10	12	V
VDB	-40°C to 175°C	-0.5	0	10	12	V
VSB	-40°C to 175°C	-0.5	0	10	12	V

Note: The node B (BULK) is: HVPWELL

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNMMAS	drain-source breakdown @ VG=0V, Id=1µA, L=2.9µm	15	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BDSONNMMA	on-state drain-source breakdown @ VG=18V, L=2.9µm	-	-	15	-	-	V
GAMNMMAL	body factor long channel @ L=20µm, W=20µm	-	-	2.3	-	-	√V
IDSNMMAS10	saturation current @ VG=10V, VD=10V, L=2.9µm, W=20µm	-	-	191	-	-	µA/µm
IDSNMMAS5	saturation current @ VG=5V, VD=5V, L=2.9µm, W=20µm	44	48	52	56	60	µA/µm
IOFNMMAS	off-state leakage @ VD=10V, L=2.9µm, W=20µm	-	-	-	15	-	pA/µm
ISBNMMAS	bulk current @ VD=10V, L=2.9µm	-	-	5	-	-	µA/µm

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Name	Description	LSL	Low	Typ	High	USL	Unit
ROANMMA10	area specific on-resistance @ VG=10V, VD=0.1V, L=2.9µm, Pitch=4.72µm	-	-	60.5	-	-	mΩmm²
	Note: The value is calculated for a transistor having minimum source drain pitch. Design related bulk contacts and metal resistances are not included.						
RO_NMMAS10	on-resistance @ VG=10V, VD=0.1V, L=2.9µm	-	-	13	-	-	kΩµm
RO_NMMAS5	on-resistance @ VG=5V, VD=0.1V, L=2.9µm	-	-	21	-	-	kΩµm
STSNMMAS	subthreshold slope @ VD=0.1V	-	-	7	-	-	decade/V
TC_VTXNMMA	threshold voltage temperature coefficient @ L=20µm, W=20µm	-	-	-2.8	-	-	mV/K
VT1NMMA	snap-back trigger voltage @ VGS=10V, L=2.9µm, W=50µm, Ngates=20	-	-	19	-	-	V
	Note: For detailed TLP I-V characteristics, refer to "XH018 Technical Report MOS TLP Characteristics" at "my X-FAB"						
VTINMMAL	threshold voltage long channel @ VD=0.1V, L=20µm, W=20µm	-	-	1.45	-	-	V
VTXNMMAL	extrapolated threshold voltage long channel @ VD=0.1V, L=20µm, W=20µm	1.25	1.37	1.5	1.63	1.75	V
VTXNMMAS	extrapolated threshold voltage short channel @ VD=0.1V, L=2.9µm, W=20µm	1.3	1.42	1.55	1.68	1.8	V

Matching parameters

Name	Description	Typ	Unit
ABTNMMA	Pelgrom coefficient gain factor mismatch	4.83	%µm
AIDNMMA00	Pelgrom coefficient ID mismatch @ VG-VT=0V	30.1	%µm
AIDNMMA02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	16.8	%µm
AIDNMMA04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	11.2	%µm
AIDNMMA06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	8.17	%µm
AIDNMMA10	Pelgrom coefficient ID mismatch @ VG-VT=1V	5.28	%µm
AIDNMMA20	Pelgrom coefficient ID mismatch @ VG-VT=2V	2.77	%µm
AIDNMMA30	Pelgrom coefficient ID mismatch @ VG-VT=3V	1.89	%µm
AIDNMMA50	Pelgrom coefficient ID mismatch @ VG-VT=5V	1.22	%µm
AVTNMMA	Pelgrom coefficient VT mismatch	45.6	mVµm
DLTNMMA	transistor delta length	0	µm
DWTNMMA	transistor delta width	0.05	µm

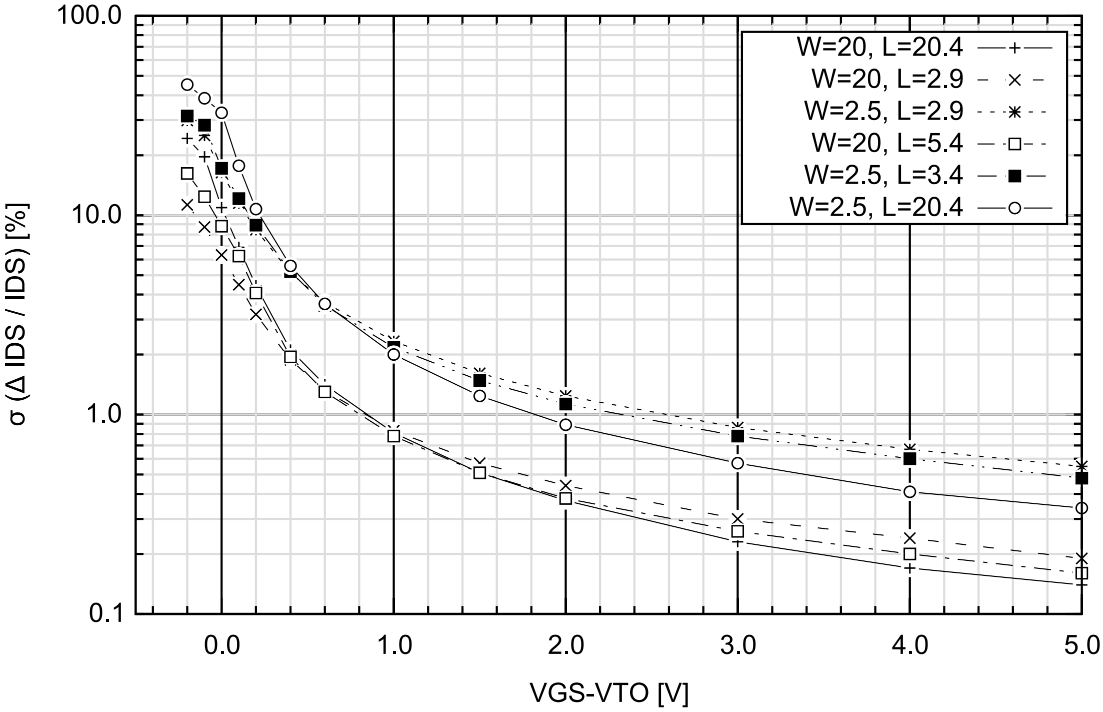

Figure 3.86 Device nmma: drain current matching vs. VGS-VTO (typical values, drawn W and L)

pmma, pmma_bjt

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-17	-15	15	17	V
VGD	-40°C to 175°C	-17	-15	15	17	V
VDS	-40°C to 175°C	-17	-15	15	17	V
VDB	-40°C to 175°C	-17	-15	0	0.5	V
VSB	-40°C to 175°C	-17	-15	0	0.5	V
VBpsub	-40°C to 175°C	-0.5	0	15	17	V

Note: The node B (BULK) is: HVNWELL

Process parameters

Negative values are considered as absolute values for their limits.

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPMMAS	drain-source breakdown @ VSUB=0V, Id=-1μA, L=2.9μm	20	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BPRPMMA	Punch-through voltage (reverse) with open bulk @ Ip=-1μA, L=2.9μm, W=20μm	-	15	-	-	-	V
GAMPMMAL	body factor long channel @ L=20μm, W=20μm	-	-	2	-	-	√V
IDSPMMAS10	saturation current @ VG=-10V, VD=-10V, L=2.9μm, W=20μm	-	-	79	-	-	μA/μm
IDSPMMAS5	saturation current @ VG=-5V, VD=-5V, L=2.9μm, W=20μm	15	17.3	19.5	21.8	24	μA/μm

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Name	Description	LSL	Low	Typ	High	USL	Unit
IOFPMMAS	off-state leakage @ VD=-15V, L=2.9µm, W=20µm	-	-	-	15	-	pA/µm
ISBPMMAS	bulk current @ VD=-15V, L=2.9µm	-	-	0.7	-	-	µA/µm
ROAPMMA10	area specific on-resistance @ VG=-10V, VD=-0.1V, L=2.9µm, Pitch=4.72µm	-	-	202	-	-	mΩmm²
	Note: The value is calculated for a transistor having minimum source drain pitch. Design related bulk contacts and metal resistances are not included.						
RO_PMMAS10	on-resistance @ VG=-10V, VD=-0.1V, L=2.9µm	-	-	43	-	-	kΩµm
RO_PMMAS5	on-resistance @ VG=-5V, VD=-0.1V, L=2.9µm	-	-	69	-	-	kΩµm
STSPMMAS	subthreshold slope @ VD=-0.1V	-	-	7.5	-	-	decade/V
TC_VTXPMMA	threshold voltage temperature coefficient @ L=20µm, W=20µm	-	-	2.5	-	-	mV/K
VTIPMMAL	threshold voltage long channel @ VD=-0.1V, L=20µm, W=20µm	-	-	-1.5	-	-	V
VTXPMMAL	extrapolated threshold voltage long channel @ VD=-0.1V, L=20µm, W=20µm	-1.2	-1.35	-1.5	-1.65	-1.8	V
VTXPMMAS	extrapolated threshold voltage short channel @ VD=-0.1V, L=2.9µm, W=20µm	-1.12	-1.27	-1.42	-1.57	-1.72	V

Matching parameters

Name	Description	Typ	Unit
ABTPMMA	Pelgrom coefficient gain factor mismatch	4.47	%µm
AIDPMMA00	Pelgrom coefficient ID mismatch @ VG-VT=0V	44	%µm
AIDPMMA02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	22.3	%µm
AIDPMMA04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	13.4	%µm
AIDPMMA06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	9.46	%µm
AIDPMMA10	Pelgrom coefficient ID mismatch @ VG-VT=1V	6	%µm
AIDPMMA20	Pelgrom coefficient ID mismatch @ VG-VT=2V	3.17	%µm
AIDPMMA30	Pelgrom coefficient ID mismatch @ VG-VT=3V	2.19	%µm
AIDPMMA50	Pelgrom coefficient ID mismatch @ VG-VT=5V	1.4	%µm
AVTPMMA	Pelgrom coefficient VT mismatch	46.7	mVµm
DLTPMMA	transistor delta length	0	µm
DWTPMMA	transistor delta width	0.35	µm

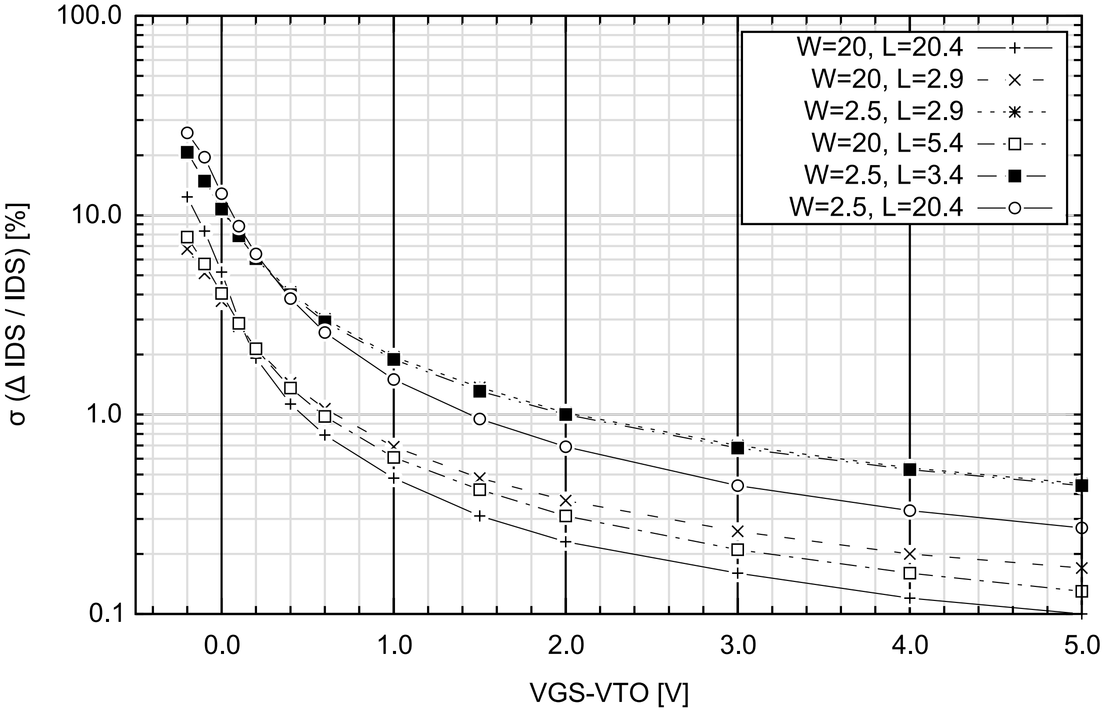

Figure 3.87 Device pmma: drain current matching vs. VGS-VTO (typical values, drawn W and L)

rdnwmv

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-0.5	0	5.5	7	V

Note: The node B (BULK) is PSUB

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSSNWDMV	DNWELLMV sheet resistance (STI terminated) @ Vterm=3.3V, W=10µm	1.2	1.35	1.5	1.65	1.8	kΩ/☐
TC1NWDMV	DNWELLMV temperature coefficient 1	-	5.2	5.6	6	-	1e-03/K
TC2NWDMV	DNWELLMV temperature coefficient 2	-	12	15	18	-	1e-06/K²
WERNWDMV	DNWELLMV effective width @ W=2µm	-	1.6	1.75	1.9	-	µm

Matching parameters

Name	Description	Typ	Unit
AR_NWDMV	Pelgrom coefficient resistor mismatch	4.96	%µm
DWRNWDMV	resistor delta width	0.25	µm

ddnwmv

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-12	-10	0	0.5	V

Note: The Junction diodes must not be used in forward operation for normal operation mode.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVJNWDMV	breakdown voltage DNWELLMV / PSUB @ Irev=1µA	15	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CJANWDMV	area junction capacitance	-	-	0.07	-	-	fF/µm²
CJPNWDMV	sidewall junction capacitance	-	-	0.59	-	-	fF/µm
ILANWDMV	area leakage current @ Vrev=10V, T=27°C	-	-	0.0001	-	-	fA/µm²
ILANWDMVHT	area leakage current @ Vrev=10V, T=175°C	-	-	1.09	-	-	pA/µm²
ILPNWDMV	sidewall leakage current @ Vrev=10V, T=27°C	-	-	0.442	-	-	fA/µm
ILPNWDMVHT	sidewall leakage current @ Vrev=10V, T=175°C	-	-	3.81	-	-	pA/µm
MJANWDMV	area grading coefficient	-	-	0.29	-	-	-
MJPNWDMV	sidewall grading coefficient	-	-	0.36	-	-	-
PBANWDMV	area junction potential	-	-	0.46	-	-	V
PBPNWDMV	sidewall junction potential	-	-	0.54	-	-	V

Note: ddnwmv is also used as parasitic diode p_ddnwmv.

dpdnwmv

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode(1	-40°C to 175°C	-7	-5.5	0	0.5	V

Note 1 Isolated from P-substrate by ddnwmv.

Note: The Junction diodes must not be used in forward operation for normal operation mode.

Note: For diodes which are isolated from the P-substrate, please also refer to the operating conditions for the isolating diode.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVJPDNWMV	breakdown voltage PDIFF / DNWELLMV @ Irev=-1µA	10	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CJAPDNWMV	area junction capacitance	-	-	0.56	-	-	fF/µm²
CJPPDNWMV	sidewall junction capacitance	-	-	0.09	-	-	fF/µm
ILAPDNWMV	area leakage current @ Vrev=-5.5V, T=27°C	-	-	0.01	-	-	fA/µm²

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Name	Description	LSL	Low	Typ	High	USL	Unit
ILAPDNWMVHT	area leakage current @ Vrev=-5.5V, T=175°C	-	-	0.38	-	-	pA/µm²
ILPPDNWMV	sidewall leakage current @ Vrev=-5.5V, T=27°C	-	-	0.521	-	-	fA/µm
ILPPDNWMVHT	sidewall leakage current @ Vrev=-5.5V, T=175°C	-	-	1.2	-	-	pA/µm
MJAPDNWMV	area grading coefficient	-	-	0.37	-	-	-
MJPPDNWMV	sidewall grading coefficient	-	-	0.05	-	-	-
PBAPDNWMV	area junction potential	-	-	0.6	-	-	V
PBPPDNWMV	sidewall junction potential	-	-	1.2	-	-	V

Note: dpdnwmv is also used as parasitic diode p_dpdnwmv.

dipdnwmv

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode[1]	-40°C to 175°C	-10	-8	0	0.5	V

Note 1 For device dipdnwmv. Isolated from P-substrate by ddnwmv.

Note: The Junction diodes must not be used in forward operation for normal operation mode.

Note: For diodes which are isolated from the P-substrate, please also refer to the operating conditions for the isolating diode.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVJP1NWDMV	breakdown voltage PWELL1 / DNWELLMV @ Irev=-1µA	15	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BVJP2NWDMV	breakdown voltage PWELL2 / DNWELLMV @ Irev=-1µA	15	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CJAPINWDMV	area junction capacitance	-	-	0.34	-	-	fF/µm²
CJPPINWDMV	sidewall junction capacitance	-	-	0.3	-	-	fF/µm
ILAPINWDMV	area leakage current @ Vrev=-8V, T=27°C	-	-	0.003	-	-	fA/µm²
ILAPINWDMVHT	area leakage current @ Vrev=-8V, T=175°C	-	-	0.34	-	-	pA/µm²
ILPPINWDMV	sidewall leakage current @ Vrev=-8V, T=27°C	-	-	0.122	-	-	fA/µm
ILPPINWDMVHT	sidewall leakage current @ Vrev=-8V, T=175°C	-	-	0.42	-	-	pA/µm
MJAPINWDMV	area grading coefficient	-	-	0.51	-	-	-
MJPPINWDMV	sidewall grading coefficient	-	-	0.27	-	-	-
PBAPINWDMV	area junction potential	-	-	0.68	-	-	V
PBPPINWDMV	sidewall junction potential	-	-	0.57	-	-	V

Note: dipdnwmv is also used as parasitic diode p_dipdnwmv.

ddnw

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-50	-45	0	0.5	V

Note: The Junction diodes must not be used in forward operation for normal operation mode.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVJNWD	breakdown voltage DNWELL / PSUB @ Irev=1µA	80	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CJANWD	area junction capacitance	-	-	0.06	-	-	fF/µm²
CJPNWD	sidewall junction capacitance	-	-	0.27	-	-	fF/µm
ILANWD	area leakage current @ Vrev=45V, T=27°C	-	-	0.0002	-	-	fA/µm²
ILANWDHT	area leakage current @ Vrev=45V, T=175°C	-	-	1.32	-	-	pA/µm²
ILPNWD	sidewall leakage current @ Vrev=45V, T=27°C	-	-	0.839	-	-	fA/µm
ILPNWDHT	sidewall leakage current @ Vrev=45V, T=175°C	-	-	3.33	-	-	pA/µm
MJANWD	area grading coefficient	-	-	0.23	-	-	-
MJPNWD	sidewall grading coefficient	-	-	0.21	-	-	-
PBANWD	area junction potential	-	-	0.46	-	-	V
PBPNWD	sidewall junction potential	-	-	0.46	-	-	V

Note: ddnw is also used as parasitic diode p_ddnw.

dpdnw

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode[1	-40°C to 175°C	-7	-5.5	0	0.5	V

Note 1 Isolated from P-substrate by ddnw.

Note: The Junction diodes must not be used in forward operation for normal operation mode.

Note: For diodes which are isolated from the P-substrate, please also refer to the operating conditions for the isolating diode.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVJPDNW	breakdown voltage PDIFF / DNWELL @ Irev=-1µA	10	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CJAPDNW	area junction capacitance	-	-	0.56	-	-	fF/µm²
CJPPDNW	sidewall junction capacitance	-	-	0.09	-	-	fF/µm
ILAPDNW	area leakage current @ Vrev=-5.5V, T=27°C	-	-	0.003	-	-	fA/µm²

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Name	Description	LSL	Low	Typ	High	USL	Unit
ILAPDNWHT	area leakage current @ Vrev=-5.5V, T=175°C	-	-	0.33	-	-	pA/µm²
ILPPDNW	sidewall leakage current @ Vrev=-5.5V, T=27°C	-	-	0.855	-	-	fA/µm
ILPPDNWHT	sidewall leakage current @ Vrev=-5.5V, T=175°C	-	-	2.2	-	-	pA/µm
MJAPDNW	area grading coefficient	-	-	0.37	-	-	-
MJPPDNW	sidewall grading coefficient	-	-	0.05	-	-	-
PBAPDNW	area junction potential	-	-	0.6	-	-	V
PBPPDNW	sidewall junction potential	-	-	1.2	-	-	V

Note: dpdnw is also used as parasitic diode p_dpdnw.

dipdnw

This device is only available if ISOMOS and HVMOS modules are selected.

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode[(1]	-40°C to 175°C	-10	-8	0	0.5	V

Note 1 Isolated from P-substrate by ddnw.

Note: The Junction diodes must not be used in forward operation for normal operation mode.

Note: For diodes which are isolated from the P-substrate, please also refer to the operating conditions for the isolating diode.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVJP1NWD	breakdown voltage PWELL1 / DNWELL @ Irev=-1µA	15	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BVJP2NWD	breakdown voltage PWELL2 / DNWELL @ Irev=-1µA	15	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CJAPINWD	area junction capacitance	-	-	0.36	-	-	fF/µm²
CJPPINWD	sidewall junction capacitance	-	-	0.44	-	-	fF/µm
ILAPINWD	area leakage current @ Vrev=-8V, T=27°C	-	-	0.0003	-	-	fA/µm²
ILAPINWDHT	area leakage current @ Vrev=-8V, T=175°C	-	-	0.28	-	-	pA/µm²
ILPPINWD	sidewall leakage current @ Vrev=-8V, T=27°C	-	-	0.179	-	-	fA/µm
ILPPINWDHT	sidewall leakage current @ Vrev=-8V, T=175°C	-	-	0.7	-	-	pA/µm
MJAPINWD	area grading coefficient	-	-	0.5	-	-	-
MJPPINWD	sidewall grading coefficient	-	-	0.5	-	-	-
PBAPINWD	area junction potential	-	-	0.57	-	-	V
PBPPINWD	sidewall junction potential	-	-	0.54	-	-	V

Note: dipdnw is also used as parasitic diode p_dipdnw.

dnhpw

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-7	-5.5	0	0.5	V

Note: The Junction diodes must not be used in forward operation for normal operation mode.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVJNPHW	breakdown voltage NDIFF / HVPWELL @ Irev=1μA	9	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BVPNDNWD	NDIFF- HVPWELL- DNWELL punch-through voltage @ Ip=1μA	-	10	-	-	-	V
CJANPHW	area junction capacitance	-	-	0.77	-	-	fF/μm²
CJPNPHW	sidewall junction capacitance	-	-	0.09	-	-	fF/μm
ILANPHW	area leakage current @ Vrev=5.5V, T=27°C	-	-	0.01	-	-	fA/μm²
ILANPHWHT	area leakage current @ Vrev=5.5V, T=175°C	-	-	0.16	-	-	pA/μm²
ILPNPHW	sidewall leakage current @ Vrev=5.5V, T=27°C	-	-	0.217	-	-	fA/μm
ILPNPHWHT	sidewall leakage current @ Vrev=5.5V, T=175°C	-	-	0.92	-	-	pA/μm
MJANPHW	area grading coefficient	-	-	0.34	-	-	-
MJPNPHW	sidewall grading coefficient	-	-	0.06	-	-	-
PBANPHW	area junction potential	-	-	0.68	-	-	V
PBPNPHW	sidewall junction potential	-	-	0.75	-	-	V

Note: dnhpw is also used as parasitic diode p_dnhpw.

dphnw

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode[1]	-40°C to 175°C	-7	-5.5	0	0.5	V

Note 1 Isolated from P-substrate by dhnw.

Note: The Junction diodes must not be used in forward operation for normal operation mode.

Note: For diodes which are isolated from the P-substrate, please also refer to the operating conditions for the isolating diode.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVJPNHW	breakdown voltage PDIFF / HVNWELL @ Irev=-1μA	9	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CJAPNHW	area junction capacitance	-	-	0.62	-	-	fF/μm²
CJPPNHW	sidewall junction capacitance	-	-	0.05	-	-	fF/μm
ILAPNHW	area leakage current @ Vrev=-5.5V, T=27°C	-	-	0.01	-	-	fA/μm²

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Name	Description	LSL	Low	Typ	High	USL	Unit
ILAPNHWHT	area leakage current @ Vrev=-5.5V, T=175°C	-	-	0.38	-	-	pA/µm²
ILPPNHW	sidewall leakage current @ Vrev=-5.5V, T=27°C	-	-	0.604	-	-	fA/µm
ILPPNHWHT	sidewall leakage current @ Vrev=-5.5V, T=175°C	-	-	1.2	-	-	pA/µm
MJAPNHW	area grading coefficient	-	-	0.26	-	-	-
MJPPNHW	sidewall grading coefficient	-	-	0.05	-	-	-
PBAPNHW	area junction potential	-	-	0.6	-	-	V
PBPPNHW	sidewall junction potential	-	-	1.2	-	-	V

Note: dphnw is also used as parasitic diode p_dphnw.

dhpw

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-17	-15	0	0.5	V
Vcathode-Vpsub	-40°C to 175°C	-0.5	0	45	50	V

Note: The Junction diodes must not be used in forward operation for normal operation mode.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVJPHWNWD	breakdown voltage HVPWELL / DNWELL @ Irev=-1µA	20	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CJAPHWNWD	area junction capacitance	-	-	0.25	-	-	fF/µm²
CJPPHWNWD	sidewall junction capacitance	-	-	0.36	-	-	fF/µm
ILAPHWNWD	area leakage current @ Vrev=-15V, T=27°C	-	-	0.002	-	-	fA/µm²
ILAPHWNWDHT	area leakage current @ Vrev=-15V, T=175°C	-	-	0.3	-	-	pA/µm²
ILPPHWNWD	sidewall leakage current @ Vrev=-15V, T=27°C	-	-	0.472	-	-	fA/µm
ILPPHWNWDHT	sidewall leakage current @ Vrev=-15V, T=175°C	-	-	1.6	-	-	pA/µm
MJAPHWNWD	area grading coefficient	-	-	0.33	-	-	-
MJPPHWNWD	sidewall grading coefficient	-	-	0.28	-	-	-
PBAPHWNWD	area junction potential	-	-	0.48	-	-	V
PBPPHWNWD	sidewall junction potential	-	-	0.48	-	-	V

Note: dhpw is also used as parasitic diode p_dhpw.

dhnw

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-17	-15	0	0.5	V

Note: The Junction diodes must not be used in forward operation for normal operation mode.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVJNHW	breakdown voltage HVNWELL / PSUB @ Irev=1µA	47	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CJANHW	area junction capacitance	-	-	0.1	-	-	fF/µm²
CJPNHW	sidewall junction capacitance	-	-	0.21	-	-	fF/µm
ILANHW	area leakage current @ Vrev=15V, T=27°C	-	-	0.0001	-	-	fA/µm²
ILANHWHT	area leakage current @ Vrev=15V, T=175°C	-	-	0.93	-	-	pA/µm²
ILPNHW	sidewall leakage current @ Vrev=15V, T=27°C	-	-	0.511	-	-	fA/µm
ILPNHWHT	sidewall leakage current @ Vrev=15V, T=175°C	-	-	5.75	-	-	pA/µm
MJANHW	area grading coefficient	-	-	0.46	-	-	-
MJPNHW	sidewall grading coefficient	-	-	0.3	-	-	-
PBANHW	area junction potential	-	-	0.46	-	-	V
PBPNHW	sidewall junction potential	-	-	0.46	-	-	V

Note: dhnw is also used as parasitic diode p_dhnw.

p_ddpldnw

This device is only available if DEPL and HVMOS modules are selected.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVJPDPLNWD	breakdown voltage DEPL / DNWELL @ Irev=-1µA	15	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CJAPDPLNWD	area junction capacitance	-	-	0.34	-	-	fF/µm²
CJPPDPLNWD	sidewall junction capacitance	-	-	0.46	-	-	fF/µm
ILAPDPLNWD	area leakage current @ Vrev=-8V, T=27°C	-	-	0.001	-	-	fA/µm²
ILAPDPLNWDHT	area leakage current @ Vrev=-8V, T=175°C	-	-	0.28	-	-	pA/µm²
ILPPDPLNWD	sidewall leakage current @ Vrev=-8V, T=27°C	-	-	0.184	-	-	fA/µm
ILPPDPLNWDHT	sidewall leakage current @ Vrev=-8V, T=175°C	-	-	0.5	-	-	pA/µm
MJAPDPLNWD	area grading coefficient	-	-	0.49	-	-	-
MJPPDPLNWD	sidewall grading coefficient	-	-	0.53	-	-	-
PBAPDPLNWD	area junction potential	-	-	0.59	-	-	V
PBPPDPLNWD	sidewall junction potential	-	-	0.59	-	-	V

dpp20

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-	-30	0	0.5	V

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Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vcathode-Vpsub	-40°C to 175°C	-0.5	0	45	50	V

Note: The Junction diodes must not be used in forward operation for normal operation mode.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BV_DPP20	dpp20 breakdown voltage @ Irev=-1µA	20	22	24	26	28	V
IL_DPP20	dpp20 leakage current @ VL=-15V, T=175°C, W=20µm	-	-	100	-	-	pA
TC_BVDPP20	dpp20 breakdown voltage temperature coefficient	-	-	18	-	-	mV/K

3.21 HVNMOS module

3.21.1 Device independent parameters

Structural and geometrical parameters

Name	Description	Typ	Unit
XJ_HPWDNW	HVPWELL in DNWELL junction depth	1.3	µm
XJ_NHPW	N+ source/ drain junction depth in HVPWELL	0.2	µm

Gate oxide parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDONH	HV NMOS gate oxide breakdown voltage @ Ibr=0.1nA/µm²	30	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BDOPH	HV PMOS gate oxide breakdown voltage @ Ibr=0.1nA/µm²	30	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CGANH	HV NMOS gate oxide area capacitance @ Vbias=8V	-	0.81	0.85	0.89	-	fF/µm²
CGAPH	HV PMOS gate oxide area capacitance @ Vbias=-8V	0.77	0.81	0.85	0.89	0.94	fF/µm²
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CGONH	HV NMOS gate – source/drain overlap	-	-	0.48	-	-	fF/µm
CGOPH	HV PMOS gate – source/drain overlap	-	-	0.48	-	-	fF/µm

3.21.2 Device parameters

nma, nma_bjt

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-20	-18	18	20	V
VGD	-40°C to 175°C	-20	-18	18	20	V
VDS	-40°C to 175°C	-8	-6	6	8	V
VDB	-40°C to 175°C	-0.5	0	6	8	V
VSB	-40°C to 175°C	-0.5	0	6	8	V

Note: The node B (BULK) is: HVPWELL

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNMA	drain-source breakdown @ VG=0V, Id=1µA	8.5	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
IDSNMA10	saturation current @ VG=10V, VD=6V, L=1µm, W=20µm	-	-	378	-	-	µA/µm
IDSNMA5	saturation current @ VG=5V, VD=6V, L=1µm, W=20µm	110	125	140	155	170	µA/µm

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Name	Description	LSL	Low	Typ	High	USL	Unit
RO_NMA10	on-resistance @ VG=10V, VD=0.1V, L=1µm	-	-	3.6	-	-	kΩµm
RO_NMA5	on-resistance @ VG=5V, VD=0.1V, L=1µm	-	5.8	6.7	7.6	-	kΩµm
TC_VTXNMA	threshold voltage temperature coefficient @ L=1µm, W=20µm	-	-	-2.4	-	-	mV/K
VTXNMA	extrapolated threshold voltage @ VD=0.1V, L=1µm, W=20µm	1.03	1.13	1.23	1.33	1.43	V

Matching parameters

Name	Description	Typ	Unit
ABTNMA	Pelgrom coefficient gain factor mismatch	2.72	%µm
AIDNMA00	Pelgrom coefficient ID mismatch @ VG-VT=0V	31.9	%µm
AIDNMA02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	16.6	%µm
AIDNMA04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	9.76	%µm
AIDNMA06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	6.42	%µm
AIDNMA10	Pelgrom coefficient ID mismatch @ VG-VT=1V	3.48	%µm
AIDNMA20	Pelgrom coefficient ID mismatch @ VG-VT=2V	1.84	%µm
AIDNMA30	Pelgrom coefficient ID mismatch @ VG-VT=3V	2.47	%µm
AIDNMA50	Pelgrom coefficient ID mismatch @ VG-VT=5V	2.69	%µm
AVTNMA	Pelgrom coefficient VT mismatch	24	mVµm
DLTNMA	transistor delta length	0.6	µm
DWTNMA	transistor delta width	0	µm

3.22 NHVE module

3.22.1 Device independent parameters

Structural and geometrical parameters

Name	Description	Typ	Unit
XJ_NDF	NDF junction depth	1	µm

Parasitic field parameters

Negative values are considered as absolute values for their limits.

Name	Description	Low	Typ	High	Unit
VTFNM1HPW	n-channel threshold voltage metal 1 on field over HVPWELL @ VD=12V, Id=1µA, L=0.28µm, W=210µm	40	-	-	V
VTFNM2HPW	n-channel threshold voltage metal 2 on field over HVPWELL @ VD=12V, Id=1µA, L=0.28µm, W=210µm	70	-	-	V
VTFNP1HPW	n-channel threshold voltage poly 1 on field over HVPWELL @ VD=12V, Id=1µA, L=0.28µm, W=210µm	8	-	-	V

Sheet and contact resistance parameters

Name	Description	Typ	Unit
RSSNDF	NDF in PSUB sheet resistance, (STI terminated) @ W=5µm	9.2	kΩ/☐

3.22.2 Device parameters

nhv, nhv_bjt

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-20	-18	18	20	V
VGB	-40°C to 175°C	-20	-18	18	20	V
VGD	-40°C to 175°C	-50	-45	18	20	V
VDS	-40°C to 175°C	-8	-6	45	50	V
VDB	-40°C to 175°C	-0.5	0	45	50	V
VSB	-40°C to 175°C	-0.5	0	6	8	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNHV	drain-source breakdown @ VG=0V, Id=1µA	50.5	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BDSONNHV	on-state drain-source breakdown @ VG=18V, L=3µm	-	-	22	-	-	V
IDSNHV10	saturation current @ VG=10V, VD=20V, L=3µm, W=20µm	90	110	130	150	170	µA/µm
IDSNHV5	saturation current @ VG=5V, VD=20V, L=3µm, W=20µm	-	-	63	-	-	µA/µm

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Name	Description	LSL	Low	Typ	High	USL	Unit
ROANHV10	area specific on-resistance @ VG=10V, VD=0.1V, L=3µm, Pitch=6.48µm	-	-	214	-	-	mΩmm²
	Note: The value is calculated for a transistor having minimum source drain pitch. Design related bulk contacts and metal resistances are not included.						
RO_NHV10	on-resistance @ VG=10V, VD=0.1V, L=3µm	-	-	33	-	-	kΩµm
RO_NHV5	on-resistance @ VG=5V, VD=0.1V, L=3µm	-	-	42	-	-	kΩµm
TC_VTXNHV	threshold voltage temperature coefficient @ L=10µm, W=20µm	-	-	-3	-	-	mV/K
VT1NHV	snap-back trigger voltage @ VGS=18V, L=3µm, W=100µm, Ngates=10	-	-	23	-	-	V
	Note: For detailed TLP I-V characteristics, refer to "XH018 Technical Report MOS TLP Characteristics" at "my X-FAB"						
VTINHVL	threshold voltage long channel @ VD=0.1V, L=10µm, W=20µm	-	-	1.63	-	-	V
VTXNHVL	extrapolated threshold voltage long channel @ VD=0.1V, L=10µm, W=20µm	-	-	1.65	-	-	V
VTXNHVS	extrapolated threshold voltage short channel @ VD=0.1V, L=3µm, W=20µm	1.3	1.45	1.6	1.75	1.9	V

Matching parameters

Name	Description	Typ	Unit
ABTNHV	Pelgrom coefficient gain factor mismatch	10.7	%µm
AIDNHV00	Pelgrom coefficient ID mismatch @ VG-VT=0V	92.6	%µm
AIDNHV02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	46	%µm
AIDNHV04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	27.6	%µm
AIDNHV06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	19	%µm
AIDNHV10	Pelgrom coefficient ID mismatch @ VG-VT=1V	11.3	%µm
AIDNHV20	Pelgrom coefficient ID mismatch @ VG-VT=2V	5.41	%µm
AIDNHV30	Pelgrom coefficient ID mismatch @ VG-VT=3V	3.64	%µm
AIDNHV50	Pelgrom coefficient ID mismatch @ VG-VT=5V	5.57	%µm
AVTNHV	Pelgrom coefficient VT mismatch	109.5	mVµm
DLTNHV	transistor delta length	-0.5	µm
DWTNHV	transistor delta width	-0.4	µm

nhhv, nhhv_bjt

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-20	-18	18	20	V
VGB	-40°C to 175°C	-20	-18	18	20	V
VGD	-40°C to 175°C	-50	-45	18	20	V
VDS	-40°C to 175°C	-50	-45	45	50	V
VDB	-40°C to 175°C	-0.5	0	45	50	V

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Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VSB	-40°C to 175°C	-0.5	0	45	50	V

Note: The node B (BULK) is: HVPWELL

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNHHV	drain-source breakdown @ VG=0V, Id=1µA	50.5	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BDSONNHHV	on-state drain-source breakdown @ VG=18V, L=5µm	-	-	40	-	-	V
IDSNHHV10	saturation current @ VG=10V, VD=20V, L=5µm, W=20µm	38	50	62	74	86	µA/µm
IDSNHHV5	saturation current @ VG=5V, VD=20V, L=5µm, W=20µm	-	-	20	-	-	µA/µm
ROANHHV10	area specific on-resistance @ VG=10V, VD=0.1V, L=5µm, Pitch=11.42µm	-	-	686	-	-	mΩmm²
	Note: The value is calculated for a transistor having minimum source drain pitch. Design related bulk contacts and metal resistances are not included.						
RO_NHHV10	on-resistance @ VG=10V, VD=0.1V, L=5µm	-	-	60	-	-	kΩµm
RO_NHHV5	on-resistance @ VG=5V, VD=0.1V, L=5µm	-	-	76	-	-	kΩµm
TC_VTXNHHV	threshold voltage temperature coefficient @ L=10µm, W=20µm	-	-	-3.6	-	-	mV/K
VT1NHHV	snap-back trigger voltage @ VGS=18V, L=5µm, W=100µm, Ngates=10	-	-	40	-	-	V
	Note: For detailed TLP I-V characteristics, refer to "XH018 Technical Report MOS TLP Characteristics" at "my X-FAB"						
VTINHHVL	threshold voltage long channel @ VD=0.1V, L=10µm, W=20µm	-	-	1.87	-	-	V
VTXNHHVL	extrapolated threshold voltage long channel @ VD=0.1V, L=10µm, W=20µm	1.47	1.62	1.77	1.92	2.07	V
VTXNHHVS	extrapolated threshold voltage short channel @ VD=0.1V, L=5µm, W=20µm	1.42	1.57	1.72	1.87	2.02	V

Matching parameters

Name	Description	Typ	Unit
ABTNHHV	Pelgrom coefficient gain factor mismatch	7.39	%µm
AIDNHHV00	Pelgrom coefficient ID mismatch @ VG-VT=0V	81.2	%µm
AIDNHHV02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	38.3	%µm
AIDNHHV04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	22.9	%µm
AIDNHHV06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	16	%µm
AIDNHHV10	Pelgrom coefficient ID mismatch @ VG-VT=1V	9.95	%µm
AIDNHHV20	Pelgrom coefficient ID mismatch @ VG-VT=2V	5.59	%µm
AIDNHHV30	Pelgrom coefficient ID mismatch @ VG-VT=3V	4.48	%µm
AIDNHHV50	Pelgrom coefficient ID mismatch @ VG-VT=5V	4.18	%µm

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Name	Description	Typ	Unit
AVTNHHV	Pelgrom coefficient VT mismatch	80.5	mVµm
DLTNHHV	transistor delta length	1.2	µm
DWTNHHV	transistor delta width	0	µm

nmc, nmc_bjt

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-20	-18	18	20	V
VGD	-40°C to 175°C	-20	-18	18	20	V
VDS	-40°C to 175°C	-0.5	0	10	12	V
VDB	-40°C to 175°C	-0.5	0	10	12	V
VSB	-40°C to 175°C	-0.5	0	2	3	V

Note: The node B (BULK) is: HVPWELL

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNMC	drain-source breakdown @ VG=0V, Id=1µA	21	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BDSONNMC	on-state drain-source breakdown @ VG=18V, L=1.5µm	-	-	15	-	-	V
IDSNMC10	saturation current @ VG=10V, VD=10V, L=1.5µm, W=20µm	-	-	145	-	-	µA/µm
IDSNMC5	saturation current @ VG=5V, VD=5V, L=1.5µm, W=20µm	54	67	80	93	106	µA/µm
RO_NMC10	on-resistance @ VG=10V, VD=0.1V, L=1.5µm	-	-	13	-	-	kΩµm
RO_NMC5	on-resistance @ VG=5V, VD=0.1V, L=1.5µm	13	16	19	22	25	kΩµm
TC_VTXNMC	threshold voltage temperature coefficient @ L=1.5µm, W=20µm	-	-	-2.7	-	-	mV/K
VT1NMC	snap-back trigger voltage @ VGS=18V, L=1.5µm, W=40µm, Ngates=40	-	-	15	-	-	V
	Note: For detailed TLP I-V characteristics, refer to "XH018 Technical Report MOS TLP Characteristics" at "my X-FAB"						
VTXNMC	extrapolated threshold voltage @ VD=0.1V, L=1.5µm, W=20µm	1.05	1.22	1.4	1.58	1.75	V

Matching parameters

Name	Description	Typ	Unit
ABTNMC	Pelgrom coefficient gain factor mismatch	2.69	%µm
AIDNMC00	Pelgrom coefficient ID mismatch @ VG-VT=0V	32.6	%µm
AIDNMC02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	16.3	%µm
AIDNMC04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	10.2	%µm
AIDNMC06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	7.2	%µm
AIDNMC10	Pelgrom coefficient ID mismatch @ VG-VT=1V	4.54	%µm

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Name	Description	Typ	Unit
AIDNMC20	Pelgrom coefficient ID mismatch @ VG-VT=2V	2.37	%µm
AIDNMC30	Pelgrom coefficient ID mismatch @ VG-VT=3V	3.07	%µm
AIDNMC50	Pelgrom coefficient ID mismatch @ VG-VT=5V	4.61	%µm
AVTNMC	Pelgrom coefficient VT mismatch	25.9	mVµm
DLTNMC	transistor delta length	0.6	µm
DWTNMC	transistor delta width	0	µm

nmmc, nmmc_bjt

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-20	-18	18	20	V
VGB	-40°C to 175°C	-20	-18	18	20	V
VGD	-40°C to 175°C	-20	-18	18	20	V
VDS	-40°C to 175°C	-17	-15	15	17	V
VDB	-40°C to 175°C	-0.5	0	15	17	V
VSB	-40°C to 175°C	-0.5	0	2	3	V

Note: The node B (BULK) is: HVPWELL

Note: It is recommended to use device nmmd when higher VSB is required.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNMMC	drain-source breakdown @ VG=0V, Ib=1µA	21	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BDSONNMMC	on-state drain-source breakdown @ VG=18V, L=2µm	-	-	18	-	-	V
IDSNMMC10	saturation current @ VG=10V, VD=10V, L=2µm, W=20µm	-	-	86	-	-	µA/µm
IDSNMMC5	saturation current @ VG=5V, VD=5V, L=2µm, W=20µm	29	35	41	47	53	µA/µm
ROANMMC10	area specific on-resistance @ VG=10V, VD=0.1V, L=2µm, Pitch=4.42µm	-	-	99	-	-	mΩmm²
	Note: The value is calculated for a transistor having minimum source drain pitch. Design related bulk contacts and metal resistances are not included.						
RO_NMMC10	on-resistance @ VG=10V, VD=0.1V, L=2µm	-	-	22	-	-	kΩµm
RO_NMMC5	on-resistance @ VG=5V, VD=0.1V, L=2µm	-	-	31	-	-	kΩµm
TC_VTXNMMC	threshold voltage temperature coefficient @ L=10µm, W=20µm	-	-	-2.8	-	-	mV/K
VT1NMMC	snap-back trigger voltage @ VGS=18V, L=2µm, W=100µm, Ngates=10	-	-	18	-	-	V
	Note: For detailed TLP I-V characteristics, refer to "XH018 Technical Report MOS TLP Characteristics" at "my X-FAB"						
VTINMMCL	threshold voltage long channel @ VD=0.1V, L=10µm, W=20µm	-	-	1.32	-	-	V

⇒

Name	Description	LSL	Low	Typ	High	USL	Unit
VTXNMMCL	extrapolated threshold voltage long channel @ VD=0.1V, L=10µm, W=20µm	1.08	1.23	1.38	1.53	1.68	V
VTXNMMCS	extrapolated threshold voltage short channel @ VD=0.1V, L=2µm, W=20µm	1.18	1.33	1.48	1.63	1.78	V

Matching parameters

Name	Description	Typ	Unit
ABTNMMC	Pelgrom coefficient gain factor mismatch	2.12	%µm
AIDNMMC00	Pelgrom coefficient ID mismatch @ VG-VT=0V	30.5	%µm
AIDNMMC02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	15.6	%µm
AIDNMMC04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	9.7	%µm
AIDNMMC06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	6.84	%µm
AIDNMMC10	Pelgrom coefficient ID mismatch @ VG-VT=1V	4.35	%µm
AIDNMMC20	Pelgrom coefficient ID mismatch @ VG-VT=2V	2.39	%µm
AIDNMMC30	Pelgrom coefficient ID mismatch @ VG-VT=3V	1.89	%µm
AIDNMMC50	Pelgrom coefficient ID mismatch @ VG-VT=5V	2.77	%µm
AVTNMMC	Pelgrom coefficient VT mismatch	24.1	mVµm
DLTNMMC	transistor delta length	0.8	µm
DWTNMMC	transistor delta width	0	µm

nmmd, nmmd_bjt

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-20	-18	18	20	V
VGB	-40°C to 175°C	-20	-18	18	20	V
VGD	-40°C to 175°C	-20	-18	18	20	V
VDS	-40°C to 175°C	-17	-15	15	17	V
VDB	-40°C to 175°C	-0.5	0	15	17	V
VSB	-40°C to 175°C	-0.5	0	15	17	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNMMD	drain-source breakdown @ VG=0V, Id=1µA	21	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BDSONNMMD	on-state drain-source breakdown @ VG=18V, L=3.2µm	-	-	20	-	-	V
IDSNMMD10	saturation current @ VG=10V, VD=10V, L=3.2µm, W=20µm	-	-	130	-	-	µA/µm
IDSNMMD5	saturation current @ VG=5V, VD=5V, L=3.2µm, W=20µm	30	38	46	54	62	µA/µm

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Name	Description	LSL	Low	Typ	High	USL	Unit
ROANMMD10	area specific on-resistance @ VG=10V, VD=0.1V, L=3.2µm, Pitch=5.62µm	-	-	112	-	-	mΩmm²
	Note: The value is calculated for a transistor having minimum source drain pitch. Design related bulk contacts and metal resistances are not included.						
RO_NMMD10	on-resistance @ VG=10V, VD=0.1V, L=3.2µm	-	-	20	-	-	kΩµm
RO_NMMD5	on-resistance @ VG=5V, VD=0.1V, L=3.2µm	-	-	28	-	-	kΩµm
TC_VTXNMMD	threshold voltage temperature coefficient @ L=3.2µm, W=20µm	-	-	-3	-	-	mV/K
VTXNMMDS	extrapolated threshold voltage short channel @ VD=0.1V, L=3.2µm, W=20µm	1.4	1.55	1.7	1.85	2	V

Matching parameters

Name	Description	Typ	Unit
ABTNMMD	Pelgrom coefficient gain factor mismatch	3.6	%µm
AIDNMMD00	Pelgrom coefficient ID mismatch @ VG-VT=0V	48.5	%µm
AIDNMMD02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	27.1	%µm
AIDNMMD04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	17.4	%µm
AIDNMMD06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	12.5	%µm
AIDNMMD10	Pelgrom coefficient ID mismatch @ VG-VT=1V	8.25	%µm
AIDNMMD20	Pelgrom coefficient ID mismatch @ VG-VT=2V	4.65	%µm
AIDNMMD30	Pelgrom coefficient ID mismatch @ VG-VT=3V	3.65	%µm
AIDNMMD50	Pelgrom coefficient ID mismatch @ VG-VT=5V	3.56	%µm
AVTNMMD	Pelgrom coefficient VT mismatch	50.4	mVµm
DLTNMMD	transistor delta length	0	µm
DWTNMMD	transistor delta width	0	µm

dndf

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-50	-45	0	0.5	V

Note: The Junction diodes must not be used in forward operation for normal operation mode.

Process parameters

Name	Description	Low	Typ	High	Unit
BVJNDF	breakdown voltage NDF / PSUB @ Irev=1µA	50.5	-	-	V
CJANDF	area junction capacitance	-	0.08	-	fF/µm²
CJPNDF	sidewall junction capacitance	-	0.16	-	fF/µm
ILANDF	area leakage current @ Vrev=45V, T=27°C	-	0.0001	-	fA/µm²
ILANDFHT	area leakage current @ Vrev=45V, T=175°C	-	1.03	-	pA/µm²
ILPNDF	sidewall leakage current @ Vrev=45V, T=27°C	-	1.174	-	fA/µm
ILPNDFHT	sidewall leakage current @ Vrev=45V, T=175°C	-	8.76	-	pA/µm
MJANDF	area grading coefficient	-	0.28	-	-

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Name	Description	Low	Typ	High	Unit
MJPNDF	sidewall grading coefficient	-	0.18	-	-
PBANDF	area junction potential	-	0.46	-	V
PBPNDF	sidewall junction potential	-	0.46	-	V

Note: dndf is also used as parasitic diode p_dndf.

p_dpndf

Process parameters

Name	Description	Typ	Unit
CJAPNDF	area junction capacitance	0.63	fF/µm²
CJPPNDF	sidewall junction capacitance	0.09	fF/µm
ILAPNDF	area leakage current @ Vrev=-6V, T=27°C	0.004	fA/µm²
ILAPNDFHT	area leakage current @ Vrev=-6V, T=175°C	0.4	pA/µm²
ILPPNDF	sidewall leakage current @ Vrev=-6V, T=27°C	0.295	fA/µm
ILPPNDFHT	sidewall leakage current @ Vrev=-6V, T=175°C	0.75	pA/µm
MJAPNDF	area grading coefficient	0.55	-
MJPPNDF	sidewall grading coefficient	0.05	-
PBAPNDF	area junction potential	0.83	V
PBPPNDF	sidewall junction potential	1.2	V

dnp20

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-	-30	0	0.5	V

Note: The Junction diodes must not be used in forward operation for normal operation mode.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BV_DNP20	dnp20 breakdown voltage @ Irev=1µA	21	23	25	27	29	V
IL_DNP20	dnp20 leakage current @ VL=15V, T=175°C, W=20µm	-	-	300	-	-	pA
TC_BVDNP20	dnp20 breakdown voltage temperature coefficient	-	-	10	-	-	mV/K

3.23 HVPMOS module

3.23.1 Device independent parameters

Structural and geometrical parameters

Name	Description	Typ	Unit
XJ_HNW	HVNWELL junction depth	1.8	µm
XJ_HPWDNW	HVPWELL in DNWELL junction depth	1.3	µm
XJ_NHPW	N+ source/ drain junction depth in HVPWELL	0.2	µm
XJ_PDWHN	PDF in HNW junction depth	0.9	µm
XJ_PHNW	P+ source/ drain junction depth in HVNWELL	0.2	µm
XJ_PWHN	P+ source/ drain junction depth in HNW	0.2	µm
XJ_WHN	HNW junction depth	4.5	µm

Parasitic field parameters

Negative values are considered as absolute values for their limits.

Name	Description	Low	Typ	High	Unit
VTFPM1WHN	p-channel threshold voltage metal 1 on field over HNW @ VD=-12V, Id=-1µA	-10	-	-	V
VTFPM2WHN	p-channel threshold voltage metal 2 on field over HNW @ VD=-12V, Id=-1µA	-25	-	-	V
VTFPP1WHN	p-channel threshold voltage poly 1 on field over HNW @ VD=-12V, Id=-1µA	-2	-	-	V
VTFPP1WHNH	p-channel threshold voltage poly 1 on field over HNW / HVNWELL @ VD=-12V, Id=-1µA	-20	-	-	V
VTFPWM2HNH	p-channel threshold voltage metal 1 on field over HNW / HVNWELL @ VD=-12V, Id=-1µA	-60	-	-	V

Sheet and contact resistance parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSSHNW	HVNWELL sheet resistance (STI terminated) @ W=20µm	0.79	0.84	0.89	0.94	0.99	kΩ/☐
RSSWHN	HNW in PSUB sheet resistance (STI terminated) @ W=6µm	-	-	3	-	-	kΩ/☐

Gate oxide parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDONH	HV NMOS gate oxide breakdown voltage @ Ibr=0.1nA/µm²	30	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BDOPH	HV PMOS gate oxide breakdown voltage @ Ibr=0.1nA/µm²	30	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CGANH	HV NMOS gate oxide area capacitance @ Vbias=8V	-	0.81	0.85	0.89	-	fF/µm²
CGAPH	HV PMOS gate oxide area capacitance @ Vbias=-8V	0.77	0.81	0.85	0.89	0.94	fF/µm²
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						

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Name	Description	LSL	Low	Typ	High	USL	Unit
CGONH	HV NMOS gate – source/drain overlap	-	-	0.48	-	-	fF/µm
CGOPH	HV PMOS gate – source/drain overlap	-	-	0.48	-	-	fF/µm

3.23.2 Device parameters

pma, pma_bjt

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-20	-18	18	20	V
VGD	-40°C to 175°C	-20	-18	18	20	V
VDS	-40°C to 175°C	-8	-6	6	8	V
VDB	-40°C to 175°C	-8	-6	0	0.5	V
VSB	-40°C to 175°C	-8	-6	0	0.5	V
VBpsub	-40°C to 175°C	-0.5	0	45	50	V

Note: The node B (BULK) is: HNW

Process parameters

Negative values are considered as absolute values for their limits.

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPMA	drain-source breakdown @ VSUB=0V, Id=-1µA	8.5	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
IDSPMA10	saturation current @ VG=-10V, VD=-6V, L=1µm, W=20µm	-	-	180	-	-	µA/µm
IDSPMA5	saturation current @ VG=-5V, VD=-6V, L=1µm, W=20µm	40	47	55	63	70	µA/µm
RO_PMA10	on-resistance @ VG=-10V, VD=-0.1V, L=1µm	-	-	13	-	-	kΩµm
RO_PMA5	on-resistance @ VG=-5V, VD=-0.1V, L=1µm	-	20	23	26	-	kΩµm
TC_VTXPMA	threshold voltage temperature coefficient @ L=1µm, W=20µm	-	-	2.1	-	-	mV/K
VTXPMA	extrapolated threshold voltage @ VD=-0.1V, L=1µm, W=20µm	-0.9	-1.05	-1.2	-1.35	-1.5	V

Matching parameters

Name	Description	Typ	Unit
ABTPMA	Pelgrom coefficient gain factor mismatch	2.98	%µm
AIDPMA00	Pelgrom coefficient ID mismatch @ VG-VT=0V	58.6	%µm
AIDPMA02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	34.1	%µm
AIDPMA04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	21.4	%µm
AIDPMA06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	14.9	%µm
AIDPMA10	Pelgrom coefficient ID mismatch @ VG-VT=1V	8.94	%µm
AIDPMA20	Pelgrom coefficient ID mismatch @ VG-VT=2V	4.27	%µm

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Name	Description	Typ	Unit
AIDPMA30	Pelgrom coefficient ID mismatch @ VG-VT=3V	2.59	%µm
AIDPMA50	Pelgrom coefficient ID mismatch @ VG-VT=5V	1.2	%µm
AVTPMA	Pelgrom coefficient VT mismatch	39.4	mVµm
DLTPMA	transistor delta length	0.15	µm
DWTPMA	transistor delta width	0	µm

dwhn

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-50	-45	0	0.5	V

Note: The Junction diodes must not be used in forward operation for normal operation mode.

Process parameters

Name	Description	Low	Typ	High	Unit
BVJWHN	breakdown voltage HNW / PSUB @ Irev=1µA	50	-	-	V
CJAWHN	area junction capacitance	-	0.07	-	fF/µm²
CJPWHN	sidewall junction capacitance	-	0.44	-	fF/µm
ILAWHN	area leakage current @ Vrev=45V, T=27°C	-	0.0001	-	fA/µm²
ILAWHNHT	area leakage current @ Vrev=45V, T=175°C	-	1.12	-	pA/µm²
ILPWHN	sidewall leakage current @ Vrev=45V, T=27°C	-	1.039	-	fA/µm
ILPWHNHT	sidewall leakage current @ Vrev=45V, T=175°C	-	8.8	-	pA/µm
MJAWHN	area grading coefficient	-	0.39	-	-
MJPWHN	sidewall grading coefficient	-	0.95	-	-
PBAWHN	area junction potential	-	1.2	-	V
PBPWHN	sidewall junction potential	-	0.49	-	V

Note: dwhn is also used as parasitic diode p_dwhn.

dpwhn

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode[1	-40°C to 175°C	-22	-20	0	0.5	V

Note 1 Isolated from P-substrate by dwhn.

Note: The Junction diodes must not be used in forward operation for normal operation mode.

Note: For diodes which are isolated from the P-substrate, please also refer to the operating conditions for the isolating diode.

Process parameters

Name	Description	Low	Typ	High	Unit
BVJPWHNH	breakdown voltage PDIFF/ HNW (high side) @ Irev=-1µA	22	-	-	V
BVJPWHNL	breakdown voltage PDIFF/ HNW (low side) @ Irev=-1µA	22	-	-	V
CJAPWHN	area junction capacitance	-	0.21	-	fF/µm²
CJPPWHN	sidewall junction capacitance	-	0.11	-	fF/µm

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Name	Description	Low	Typ	High	Unit
ILAPWHN	area leakage current @ Vrev=-20V, T=27°C	-	0.014	-	fA/µm²
ILAPWHNHT	area leakage current @ Vrev=-20V, T=175°C	-	0.4	-	pA/µm²
ILPPWHN	sidewall leakage current @ Vrev=-20V, T=27°C	-	12.12	-	fA/µm
ILPPWHNHT	sidewall leakage current @ Vrev=-20V, T=175°C	-	7.54	-	pA/µm
MJAPWHN	area grading coefficient	-	0.4	-	-
MJPPWHN	sidewall grading coefficient	-	0.05	-	-
PBAPWHN	area junction potential	-	0.55	-	V
PBPPWHN	sidewall junction potential	-	1.2	-	V

Note: dpwhn is also used as parasitic diode p_dpwhn.

p_dpndf

Process parameters

Name	Description	Typ	Unit
CJAPNDF	area junction capacitance	0.63	fF/µm²
CJPPNDF	sidewall junction capacitance	0.09	fF/µm
ILAPNDF	area leakage current @ Vrev=-6V, T=27°C	0.004	fA/µm²
ILAPNDFHT	area leakage current @ Vrev=-6V, T=175°C	0.4	pA/µm²
ILPPNDF	sidewall leakage current @ Vrev=-6V, T=27°C	0.295	fA/µm
ILPPNDFHT	sidewall leakage current @ Vrev=-6V, T=175°C	0.75	pA/µm
MJAPNDF	area grading coefficient	0.55	-
MJPPNDF	sidewall grading coefficient	0.05	-
PBAPNDF	area junction potential	0.83	V
PBPPNDF	sidewall junction potential	1.2	V

3.24 PHVE module

3.24.1 Device independent parameters

Sheet and contact resistance parameters

Name	Description	Typ	Unit
RSSPDWHN	PDF in HNW sheet resistance, (STI terminated) @ W=5µm	10	kΩ/☐

3.24.2 Device parameters

phv, phv_bjt

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-20	-18	18	20	V
VGB	-40°C to 175°C	-20	-18	18	20	V
VGD	-40°C to 175°C	-20	-18	45	50	V
VDS	-40°C to 175°C	-50	-45	6	8	V
VDB	-40°C to 175°C	-50	-45	0	0.5	V
VSB	-40°C to 175°C	-8	-6	0	0.5	V
VBpsub	-40°C to 175°C	-0.5	0	45	50	V

Note: The node B (BULK) is: HNW

Process parameters

Negative values are considered as absolute values for their limits.

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPHV	drain-source breakdown @ VSUB=0V, Id=-1µA	51	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BPRPHV	Punch-through voltage (reverse) with open bulk @ Ip=-1µA, L=2µm, W=20µm	-	45	-	-	-	V
BVPPHV	drain-psub punch through voltage @ Ip=1µA	60	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
IDSPHV10	saturation current @ VG=-10V, VD=-20V, L=2µm, W=20µm	77	89	102	115	127	µA/µm
IDSPHV5	saturation current @ VG=-5V, VD=-20V, L=2µm, W=20µm	-	-	28	-	-	µA/µm
ROAPHV10	area specific on-resistance @ VG=-10V, VD=-0.1V, L=2µm, Pitch=4.98µm	-	-	280	-	-	mΩmm²
	Note: The value is calculated for a transistor having minimum source drain pitch. Design related bulk contacts and metal resistances are not included.						
RO_PHV10	on-resistance @ VG=-10V, VD=-0.1V, L=2µm	-	-	56	-	-	kΩµm
RO_PHV5	on-resistance @ VG=-5V, VD=-0.1V, L=2µm	-	-	78	-	-	kΩµm

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Name	Description	LSL	Low	Typ	High	USL	Unit
TC_VTXPHV	threshold voltage temperature coefficient @ L=10μm, W=20μm	-	-	2.4	-	-	mV/K
VTIPHVL	threshold voltage long channel @ VD=-0.1V, L=10μm, W=20μm	-	-	-1.38	-	-	V
VTXPHVL	extrapolated threshold voltage long channel @ VD=-0.1V, L=10μm, W=20μm	-	-	-1.38	-	-	V
VTXPHVS	extrapolated threshold voltage short channel @ VD=-0.1V, L=2μm, W=20μm	-1.05	-1.2	-1.35	-1.5	-1.65	V

Matching parameters

Name	Description	Typ	Unit
ABTPHV	Pelgrom coefficient gain factor mismatch	4.84	%μm
AIDPHV00	Pelgrom coefficient ID mismatch @ VG-VT=0V	33.9	%μm
AIDPHV02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	18.6	%μm
AIDPHV04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	12.2	%μm
AIDPHV06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	8.04	%μm
AIDPHV10	Pelgrom coefficient ID mismatch @ VG-VT=1V	5.98	%μm
AIDPHV20	Pelgrom coefficient ID mismatch @ VG-VT=2V	3.37	%μm
AIDPHV30	Pelgrom coefficient ID mismatch @ VG-VT=3V	2.42	%μm
AIDPHV50	Pelgrom coefficient ID mismatch @ VG-VT=5V	1.54	%μm
AVTPHV	Pelgrom coefficient VT mismatch	60.3	mVμm
DLTPHV	transistor delta length	0	μm
DWTPHV	transistor delta width	0	μm

phhv, phhv_bjt

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-20	-18	18	20	V
VGB	-40°C to 175°C	-20	-18	18	20	V
VGD	-40°C to 175°C	-20	-18	45	50	V
VDS	-40°C to 175°C	-50	-45	45	50	V
VDB	-40°C to 175°C	-50	-45	0	0.5	V
VSB	-40°C to 175°C	-50	-45	0	0.5	V
VBpsub	-40°C to 175°C	-0.5	0	45	50	V

Note: The node B (BULK) is: HNW

Process parameters

Negative values are considered as absolute values for their limits.

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPHHV	drain-source breakdown @ VSUB=0V, Id=-1μA	51	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						

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Name	Description	LSL	Low	Typ	High	USL	Unit
BPRPHHV	Punch-through voltage (reverse) with open bulk @ Ip=-1µA, L=3.5µm, W=20µm	-	45	-	-	-	V
BVPPHHV	drain-psub punch through voltage @ Ip=1µA	60	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
IDSPHHV10	saturation current @ VG=-10V, VD=-20V, L=3.5µm, W=20µm	29	34	39	44	49	µA/µm
IDSPHHV5	saturation current @ VG=-5V, VD=-20V, L=3.5µm, W=20µm	-	-	10	-	-	µA/µm
ROAPHHV10	area specific on-resistance @ VG=-10V, VD=-0.1V, L=3.5µm, Pitch=8.92µm	-	-	900	-	-	mΩmm²
	Note: The value is calculated for a transistor having minimum source drain pitch. Design related bulk contacts and metal resistances are not included.						
RO_PHHV10	on-resistance @ VG=-10V, VD=-0.1V, L=3.5µm	-	-	101	-	-	kΩµm
RO_PHHV5	on-resistance @ VG=-5V, VD=-0.1V, L=3.5µm	-	-	140	-	-	kΩµm
TC_VTXPHHV	threshold voltage temperature coefficient @ L=10µm, W=20µm	-	-	2.7	-	-	mV/K
VTIPHHVL	threshold voltage long channel @ VD=-0.1V, L=10µm, W=20µm	-	-	-1.5	-	-	V
VTXPHHVL	extrapolated threshold voltage long channel @ VD=-0.1V, L=10µm, W=20µm	-1.11	-1.26	-1.41	-1.56	-1.71	V
VTXPHHVS	extrapolated threshold voltage short channel @ VD=-0.1V, L=0.35µm, W=20µm	-1.21	-1.36	-1.51	-1.66	-1.81	V

Matching parameters

Name	Description	Typ	Unit
ABTPHHV	Pelgrom coefficient gain factor mismatch	6.09	%µm
AIDPHHV00	Pelgrom coefficient ID mismatch @ VG-VT=0V	52.3	%µm
AIDPHHV02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	24.4	%µm
AIDPHHV04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	20.3	%µm
AIDPHHV06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	13.3	%µm
AIDPHHV10	Pelgrom coefficient ID mismatch @ VG-VT=1V	7.15	%µm
AIDPHHV20	Pelgrom coefficient ID mismatch @ VG-VT=2V	3.16	%µm
AIDPHHV30	Pelgrom coefficient ID mismatch @ VG-VT=3V	2.28	%µm
AIDPHHV50	Pelgrom coefficient ID mismatch @ VG-VT=5V	1.68	%µm
AVTPHHV	Pelgrom coefficient VT mismatch	59.3	mVµm
DLTPHHV	transistor delta length	0	µm
DWTPHHV	transistor delta width	0	µm

pmc, pmc_bjt

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-20	-18	18	20	V

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Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGD	-40°C to 175°C	-20	-18	18	20	V
VDS	-40°C to 175°C	-22	-20	6	8	V
VDB	-40°C to 175°C	-22	-20	0	0.5	V
VSB	-40°C to 175°C	-8	-6	0	0.5	V
VBpsub	-40°C to 175°C	-0.5	0	45	50	V

Note: The node B (BULK) is: HNW

Process parameters

Negative values are considered as absolute values for their limits.

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPMC	drain-source breakdown @ VSUB=0V, Id=-1µA	24	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BPRPMC	Punch-through voltage (reverse) with open bulk @ Ip=-1µA, L=1.3µm, W=20µm	-	40	-	-	-	V
BVPPMC	drain-psub punch through voltage @ Ip=1µA	-	-	97	-	-	V
IDSPMC10	saturation current @ VG=-10V, VD=-10V, L=1.3µm, W=20µm	-	-	126	-	-	µA/µm
IDSPMC5	saturation current @ VG=-5V, VD=-5V, L=1.3µm, W=20µm	35	41	47	53	59	µA/µm
RO_PMC10	on-resistance @ VG=-10V, VD=-0.1V, L=1.3µm	-	-	34	-	-	kΩµm
RO_PMC5	on-resistance @ VG=-5V, VD=-0.1V, L=1.3µm	41	44	47	50	53	kΩµm
TC_VTXPMC	threshold voltage temperature coefficient @ L=1.3µm, W=20µm	-	-	2.3	-	-	mV/K
VTXPMC	extrapolated threshold voltage @ VD=-0.1V, L=1.3µm, W=20µm	-0.85	-1	-1.15	-1.3	-1.45	V

Matching parameters

Name	Description	Typ	Unit
ABTPMC	Pelgrom coefficient gain factor mismatch	1.65	%µm
AIDPMC00	Pelgrom coefficient ID mismatch @ VG-VT=0V	25.2	%µm
AIDPMC02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	13.1	%µm
AIDPMC04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	7.94	%µm
AIDPMC06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	5.52	%µm
AIDPMC10	Pelgrom coefficient ID mismatch @ VG-VT=1V	3.36	%µm
AIDPMC20	Pelgrom coefficient ID mismatch @ VG-VT=2V	1.72	%µm
AIDPMC30	Pelgrom coefficient ID mismatch @ VG-VT=3V	1.17	%µm
AIDPMC50	Pelgrom coefficient ID mismatch @ VG-VT=5V	0.73	%µm
AVTPMC	Pelgrom coefficient VT mismatch	20	mVµm
DLTPMC	transistor delta length	0.89	µm
DWTPMC	transistor delta width	0	µm

pmmc, pmmc_bjt

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-20	-18	18	20	V
VGB	-40°C to 175°C	-20	-18	18	20	V
VGD	-40°C to 175°C	-20	-18	18	20	V
VDS	-40°C to 175°C	-22	-20	20	22	V
VDB	-40°C to 175°C	-22	-20	0	0.5	V
VSB	-40°C to 175°C	-22	-20	0	0.5	V
VBpsub	-40°C to 175°C	-0.5	0	45	50	V

Note: The node B (BULK) is: HNW

Process parameters

Negative values are considered as absolute values for their limits.

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPMMC	drain-source breakdown @ VSUB=0V, Id=-1μA	24	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BPRPMMC	Punch-through voltage (reverse) with open bulk @ Ip=-1μA, L=1.8μm, W=20μm	-	40	-	-	-	V
BVPPMMC	drain-psub punch through voltage @ Ip=1μA	-	-	97	-	-	V
IDSPMMC10	saturation current @ VG=-10V, VD=-10V, L=1.8μm, W=20μm	-	-	70	-	-	μA/μm
IDSPMMC5	saturation current @ VG=-5V, VD=-5V, L=1.8μm, W=20μm	15	18	21	24	27	μA/μm
ROAPMMC10	area specific on-resistance @ VG=-10V, VD=-0.1V, L=1.8μm, Pitch=4.22μm	-	-	228	-	-	mΩmm²
	Note: The value is calculated for a transistor having minimum source drain pitch. Design related bulk contacts and metal resistances are not included.						
RO_PMMC10	on-resistance @ VG=-10V, VD=-0.1V, L=1.8μm	-	-	54	-	-	kΩμm
RO_PMMC5	on-resistance @ VG=-5V, VD=-0.1V, L=1.8μm	-	-	73	-	-	kΩμm
TC_VTXPMMC	threshold voltage temperature coefficient @ L=10μm, W=20μm	-	-	2.4	-	-	mV/K
VTIPMMCL	threshold voltage long channel @ VD=-0.1V, L=10μm, W=20μm	-	-	-1.4	-	-	V
VTXPMMCL	extrapolated threshold voltage long channel @ VD=-0.1V, L=10μm, W=20μm	-1	-1.15	-1.3	-1.45	-1.6	V
VTXPMMCS	extrapolated threshold voltage short channel @ VD=-0.1V, L=1.8μm, W=20μm	-1.25	-1.4	-1.55	-1.7	-1.85	V

Matching parameters

Name	Description	Typ	Unit
ABTPMMC	Pelgrom coefficient gain factor mismatch	2.8	%μm

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Name	Description	Typ	Unit
AIDPMMC00	Pelgrom coefficient ID mismatch @ VG-VT=0V	36.1	%µm
AIDPMMC02	Pelgrom coefficient ID mismatch @ VG-VT=0.2V	17.8	%µm
AIDPMMC04	Pelgrom coefficient ID mismatch @ VG-VT=0.4V	10.7	%µm
AIDPMMC06	Pelgrom coefficient ID mismatch @ VG-VT=0.6V	7.5	%µm
AIDPMMC10	Pelgrom coefficient ID mismatch @ VG-VT=1V	4.61	%µm
AIDPMMC20	Pelgrom coefficient ID mismatch @ VG-VT=2V	2.43	%µm
AIDPMMC30	Pelgrom coefficient ID mismatch @ VG-VT=3V	1.74	%µm
AIDPMMC50	Pelgrom coefficient ID mismatch @ VG-VT=5V	1.2	%µm
AVTPMMC	Pelgrom coefficient VT mismatch	31.4	mVµm
DLTPMMC	transistor delta length	0.75	µm
DWTPMMC	transistor delta width	0	µm

dpdwhn

Operating conditions

Note: The Junction diodes must not be used in forward operation for normal operation mode.

Note: For diodes which are isolated from the P-substrate, please also refer to the operating conditions for the isolating diode.

Note: For diode dpdwhn in HNW isolated from p-substrate, please refer to the below operating conditions:

$$\begin{aligned} VPSUB &\leq VHNW \leq 45V \\ VHNW - 45V &\leq VPDF \leq VHNW \\ VPSUB - 32V &\leq VPDF \leq VHNW \end{aligned}$$

Process parameters

Name	Description	Low	Typ	High	Unit
BVJPDWHNH	breakdown voltage PDF / HNW (high side) @ Irev=-1µA	50	-	-	V
BVJPDWHNL	breakdown voltage PDF / HNW (low side) @ Irev=-1µA	35	-	-	V
CJAPDWHN	area junction capacitance	-	0.21	-	fF/µm²
CJPPDWHN	sidewall junction capacitance	-	0.27	-	fF/µm
ILAPDWHN	area leakage current @ Vrev=-45V, T=27°C	-	0.006	-	fA/µm²
ILAPDWHNHT	area leakage current @ Vrev=-45V, T=175°C	-	0.27	-	pA/µm²
ILPPDWHN	sidewall leakage current @ Vrev=-45V, T=27°C	-	0.794	-	fA/µm
ILPPDWHNHT	sidewall leakage current @ Vrev=-45V, T=175°C	-	3.31	-	pA/µm
MJAPDWHN	area grading coefficient	-	0.52	-	-
MJPPDWHN	sidewall grading coefficient	-	0.81	-	-
PBAPDWHN	area junction potential	-	1.2	-	V
PBPPDWHN	sidewall junction potential	-	1.2	-	V
RSSPDWHN	PDF in HNW sheet resistance, (STI terminated) @ W=5µm	-	10	-	kΩ/□

Note: dpdwhn is also used as parasitic diode p_dpdwhn.

3.25 SCHOTTKY module

3.25.1 Device independent parameters

Structural and geometrical parameters

Name	Description	Typ	Unit
XJ_HPWDNW	HVPWELL in DNWELL junction depth	1.3	µm
XJ_NHPW	N+ source/ drain junction depth in HVPWELL	0.2	µm
XJ_PDWHN	PDF in HNW junction depth	0.9	µm
XJ_PWHN	P+ source/ drain junction depth in HNW	0.2	µm
XJ_WHN	HNW junction depth	4.5	µm

Parasitic field parameters

Name	Description	Low	Typ	High	Unit
VTFPM1WHN	p-channel threshold voltage metal 1 on field over HNW @ VD=-12V, Id=-1µA	-10	-	-	V
VTFPM2WHN	p-channel threshold voltage metal 2 on field over HNW @ VD=-12V, Id=-1µA	-25	-	-	V
VTFPP1WHN	p-channel threshold voltage poly 1 on field over HNW @ VD=-12V, Id=-1µA	-2	-	-	V
VTFPP1WHNH	p-channel threshold voltage poly 1 on field over HNW / HVNWELL @ VD=-12V, Id=-1µA	-20	-	-	V
VTFPWM2HNH	p-channel threshold voltage metal 1 on field over HNW / HVNWELL @ VD=-12V, Id=-1µA	-60	-	-	V

Note: Negative values are considered as absolute values for their limits.

Sheet and contact resistance parameters

Name	Description	Typ	Unit
RSSWHN	HNW in PSUB sheet resistance (STI terminated) @ W=6µm	3	kΩ/☐

3.25.2 Device parameters

dsba

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-20	-18	1.5	-	V
Vcathode-Vpsub	-40°C to 175°C	-0.5	0	45	50	V

Note: The max. forward current is not limited by the Schottky diode itself, but by the specified max. current density of the interconnects.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BV_DSBAL	breakdown voltage @ Irev=-1mA, L=0.94µm, W=50µm	20.5	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BV_DSBAS	breakdown voltage @ Irev=-50µA, L=0.94µm, W=2.4µm	20.5	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						

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Name	Description	LSL	Low	Typ	High	USL	Unit
HF_DSBA	parasitic current gain, diode @ Vbias=0.6V, L=0.94µm, W=2.4µm	-	-	0.03	-	-	-
IDFDSBAL	forward current @ Vbias=0.6V, L=0.94µm, W=50µm	-	-	215	-	-	µA
IDFDSBAS	forward current @ Vbias=0.6V, L=0.94µm, W=2.4µm	-	-	8.5	-	-	µA
IL_DSBAL10	leakage current @ VL=-10V, L=0.94µm, W=50µm	-	-	0.2	-	100	nA
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
IL_DSBAL3	leakage current @ VL=-3.6V, L=0.94µm, W=50µm	-	-	0.08	-	-	nA
IL_DSBAS10	leakage current @ VL=-10V, L=0.94µm, W=2.4µm	-	-	0.01	-	-	nA
IL_DSBAS3	leakage current @ VL=-3.6V, L=0.94µm, W=2.4µm	-	-	0.004	-	-	nA
TC_VDFDSBAL	forward voltage temperature coefficient	-	-	-1.3	-	-	mV/K
VDFDSBAL	forward voltage @ Id=200µA, L=0.94µm, W=50µm	-	-	0.59	-	-	V
VDFDSBAS	forward voltage @ Id=10µA, L=0.94µm, W=2.4µm	0.55	0.58	0.61	0.64	0.67	V

dsb

The device dsb is superseded by dsba. Please use dsba, in particular for diode leakage sensitive designs.

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-20	-18	1.5	-	V
Vcathode-Vpsub	-40°C to 175°C	-0.5	0	45	50	V

Note: The max. forward current is not limited by the Schottky diode itself, but by the specified max. current density of the interconnects.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BV_DSB	breakdown voltage @ Irev=-50µA	20.5	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
HF_DSB	parasitic current gain, diode @ Vbias=0.6V, L=0.94µm, W=2.4µm	-	-	-	0.01	-	-
IDFDSB	forward current @ Vbias=0.6V, L=0.94µm, W=2.4µm	-	-	31	-	-	µA
IDFDSBW	forward current per µm width (W= 5 – 50 µm) @ Vbias=0.6V	-	-	17	-	-	µA/µm
IL_DSB10	leakage current @ VL=-10V, L=0.94µm, W=2.4µm	-	-	6	-	-	nA
IL_DSB3	leakage current @ VL=-3.6V, L=0.94µm, W=2.4µm	-	-	1.25	-	-	nA
IL_DSBL10	leakage current @ VL=-10V, L=0.94µm, W=50µm	-	-	50000	-	-	nA

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Name	Description	LSL	Low	Typ	High	USL	Unit
IL_DSBL3	leakage current @ VL=-3.6V, L=0.94µm, W=50µm	-	-	10000	-	-	nA
VDFDSB	forward voltage @ Id=10µA, L=0.94µm, W=2.4µm	0.34	0.39	0.45	0.51	0.56	V

Note: The diode leakage does not scale linearly with diode width.

3.26 MIM module

3.26.1 Device parameters

cmm4t

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-50	-45	45	50	V
Vterm1-Vterm2	-40°C to 175°C	-12	-10	10	12	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_MIM4T	cmm4t breakdown voltage @ Ibr=0.6µA	20	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CAA_MIM4T	cmm4t area capacitance @ Vbias=0V	0.85	0.92	1	1.08	1.15	fF/µm²
CAP_MIM4T	cmm4t perimeter capacitance	-	-	170	-	-	aF/µm
IL_MIM4T	cmm4t leakage current @ VL=7V	-	-	-	0.1	-	fA/µm²
QF_MIM4T	cmm4t quality factor @ f=1GHz	-	-	200	-	-	-
TCCMIM4T	cmm4t temperature coefficient	-	-	40	-	-	1e-06/K
THD_MIM4T	cmm4t equivalent dielectric thickness @ Er=7.3	-	-	65	-	-	nm
VC1_MIM4T	cmm4t capacitor voltage coefficient 1	-	-	-15	-	-	ppm/V
VC2_MIM4T	cmm4t capacitor voltage coefficient 2	-	-	3.5	-	-	ppm/V²

Matching parameters

Name	Description	Typ	Unit
AC_MIM	Pelgrom coefficient capacitor mismatch	0.28	%µm

cmm5t

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-50	-45	45	50	V
Vterm1-Vterm2	-40°C to 175°C	-12	-10	10	12	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_MIM5T	cmm5t breakdown voltage @ Ibr=0.6µA	20	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CAA_MIM5T	cmm5t area capacitance @ Vbias=0V	0.85	0.92	1	1.08	1.15	fF/µm²
CAP_MIM5T	cmm5t perimeter capacitance	-	-	170	-	-	aF/µm
IL_MIM5T	cmm5t leakage current @ VL=7V	-	-	-	0.1	-	fA/µm²
QF_MIM5T	cmm5t quality factor @ f=1GHz	-	-	200	-	-	-
TCCMIM5T	cmm5t temperature coefficient	-	-	40	-	-	1e-06/K

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Name	Description	LSL	Low	Typ	High	USL	Unit
THD_MIM5T	cmm5t equivalent dielectric thickness @ Er=7.3	-	-	65	-	-	nm
VC1_MIM5T	cmm5t capacitor voltage coefficient 1	-	-	-15	-	-	ppm/V
VC2_MIM5T	cmm5t capacitor voltage coefficient 2	-	-	3.5	-	-	ppm/V²

Matching parameters

Name	Description	Typ	Unit
AC_MIM	Pelgrom coefficient capacitor mismatch	0.28	%µm

cmm6t

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-50	-45	45	50	V
Vterm1-Vterm2	-40°C to 175°C	-12	-10	10	12	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_MIM6T	cmm6t breakdown voltage @ Ibr=0.6µA	20	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CAA_MIM6T	cmm6t area capacitance @ Vbias=0V	0.85	0.92	1	1.08	1.15	fF/µm²
CAP_MIM6T	cmm6t perimeter capacitance	-	-	170	-	-	aF/µm
IL_MIM6T	cmm6t leakage current @ VL=7V	-	-	-	0.1	-	fA/µm²
QF_MIM6T	cmm6t quality factor @ f=1GHz	-	-	200	-	-	-
TCCMIM6T	cmm6t temperature coefficient	-	-	40	-	-	1e-06/K
THD_MIM6T	cmm6t equivalent dielectric thickness @ Er=7.3	-	-	65	-	-	nm
VC1_MIM6T	cmm6t capacitor voltage coefficient 1	-	-	-15	-	-	ppm/V
VC2_MIM6T	cmm6t capacitor voltage coefficient 2	-	-	3.5	-	-	ppm/V²

Matching parameters

Name	Description	Typ	Unit
AC_MIM	Pelgrom coefficient capacitor mismatch	0.28	%µm

3.27 MIM23 module

3.27.1 Device parameters

cmm3

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-50	-45	45	50	V
Vterm1-Vterm2	-40°C to 175°C	-12	-10	10	12	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_MIM3	cmm3 breakdown voltage @ Ibr=0.6μA	20	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CAA_MIM3	cmm3 area capacitance @ Vbias=0V	0.85	0.92	1	1.08	1.15	fF/μm²
CAP_MIM3	cmm3 perimeter capacitance	-	-	170	-	-	aF/μm
IL_MIM3	cmm3 leakage current @ VL=7V	-	-	-	0.1	-	fA/μm²
QF_MIM3	cmm3 quality factor @ f=1GHz	-	-	200	-	-	-
TCCMIM3	cmm3 temperature coefficient	-	-	40	-	-	1e-06/K
THD_MIM3	cmm3 equivalent dielectric thickness @ Er=7.3	-	-	65	-	-	nm
VC1_MIM3	cmm3 capacitor voltage coefficient 1	-	-	-15	-	-	ppm/V
VC2_MIM3	cmm3 capacitor voltage coefficient 2	-	-	3.5	-	-	ppm/V²

Matching parameters

Name	Description	Typ	Unit
AC_MIM	Pelgrom coefficient capacitor mismatch	0.28	%μm

3.28 MIM34 module

3.28.1 Device parameters

cmm4

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-50	-45	45	50	V
Vterm1-Vterm2	-40°C to 175°C	-12	-10	10	12	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_MIM4	cmm4 breakdown voltage @ Ibr=0.6μA	20	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CAA_MIM4	cmm4 area capacitance @ Vbias=0V	0.85	0.92	1	1.08	1.15	fF/μm²
CAP_MIM4	cmm4 perimeter capacitance	-	-	170	-	-	aF/μm
IL_MIM4	cmm4 leakage current @ VL=7V	-	-	-	0.1	-	fA/μm²
QF_MIM4	cmm4 quality factor @ f=1GHz	-	-	200	-	-	-
TCCMIM4	cmm4 temperature coefficient	-	-	40	-	-	1e-06/K
THD_MIM4	cmm4 equivalent dielectric thickness @ Er=7.3	-	-	65	-	-	nm
VC1_MIM4	cmm4 capacitor voltage coefficient 1	-	-	-15	-	-	ppm/V
VC2_MIM4	cmm4 capacitor voltage coefficient 2	-	-	3.5	-	-	ppm/V²

Matching parameters

Name	Description	Typ	Unit
AC_MIM	Pelgrom coefficient capacitor mismatch	0.28	%μm

3.29 DMIM module

3.29.1 Device parameters

cdmm4

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-50	-45	45	50	V
Vterm1-Vterm2	-40°C to 175°C	-12	-10	10	12	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_DMIM4	cdmm4 breakdown voltage @ Ibr=0.6µA	20	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CAA_DMIM4	cdmm4 area capacitance @ Vbias=0V	1.7	1.85	2	2.15	2.3	fF/µm²
CAP_DMIM4	cdmm4 perimeter capacitance	-	-	230	-	-	aF/µm
IL_DMIM4	cdmm4 leakage current @ VL=7V	-	-	-	0.1	-	fA/µm²
QF_DMIM4	cdmm4 quality factor @ f=1GHz	-	-	100	-	-	-
TCCDMIM4	cdmm4 temperature coefficient	-	-	40	-	-	1e-06/K
THD_DMIM4	cdmm4 equivalent dielectric thickness @ Er=7.3	-	-	32.5	-	-	nm
VC1_DMIM4	cdmm4 capacitor voltage coefficient 1	-	-	3	-	-	ppm/V
	Note: As the capacitors' connections are cross-coupled, the linear voltage coefficient term is small.						
VC2_DMIM4	cdmm4 capacitor voltage coefficient 2	-	-	3.5	-	-	ppm/V²

Matching parameters

Name	Description	Typ	Unit
AC_DMIM	Pelgrom coefficient capacitor mismatch	0.2	%µm

cdmm4t

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-50	-45	45	50	V
Vterm1-Vterm2	-40°C to 175°C	-12	-10	10	12	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_DMIM4T	cdmm4t breakdown voltage @ Ibr=0.6µA	20	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CAA_DMIM4T	cdmm4t area capacitance @ Vbias=0V	1.7	1.85	2	2.15	2.3	fF/µm²
CAP_DMIM4T	cdmm4t perimeter capacitance	-	-	230	-	-	aF/µm
IL_DMIM4T	cdmm4t leakage current @ VL=7V	-	-	-	0.1	-	fA/µm²
QF_DMIM4T	cdmm4t quality factor @ f=1GHz	-	-	100	-	-	-

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Name	Description	LSL	Low	Typ	High	USL	Unit
TCCDMIM4T	cdmm4t temperature coefficient	-	-	40	-	-	1e-06/K
THD_DMIM4T	cdmm4t equivalent dielectric thickness @ Er=7.3	-	-	32.5	-	-	nm
VC1_DMIM4T	cdmm4t capacitor voltage coefficient 1	-	-	3	-	-	ppm/V
	Note: As the capacitors' connections are cross-coupled, the linear voltage coefficient term is small.						
VC2_DMIM4T	cdmm4t capacitor voltage coefficient 2	-	-	3.5	-	-	ppm/V²

Matching parameters

Name	Description	Typ	Unit
AC_DMIM	Pelgrom coefficient capacitor mismatch	0.2	%µm

3.30 TMIM module

3.30.1 Device parameters

ctmm5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-50	-45	45	50	V
Vterm1-Vterm2	-40°C to 175°C	-12	-10	10	12	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_TMIM5	ctmm5 breakdown voltage @ Ibr=0.6μA	20	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CAA_TMIM5	ctmm5 area capacitance @ Vbias=0V	2.55	2.77	3	3.23	3.45	fF/μm²
CAP_TMIM5	ctmm5 perimeter capacitance	-	-	365	-	-	aF/μm
IL_TMIM5	ctmm5 leakage current @ VL=7V	-	-	-	0.1	-	fA/μm²
QF_TMIM5	ctmm5 quality factor @ f=1GHz	-	-	65	-	-	-
TCCTMIM5	ctmm5 temperature coefficient	-	-	40	-	-	1e-06/K
THD_TMIM5	ctmm5 equivalent dielectric thickness @ Er=7.3	-	-	22	-	-	nm
VC1_TMIM5	ctmm5 capacitor voltage coefficient 1	-	-	-15	-	-	ppm/V
VC2_TMIM5	ctmm5 capacitor voltage coefficient 2	-	-	3.5	-	-	ppm/V²

Matching parameters

Name	Description	Typ	Unit
AC_TMIM	Pelgrom coefficient capacitor mismatch	0.16	%μm

ctmm5t

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-50	-45	45	50	V
Vterm1-Vterm2	-40°C to 175°C	-12	-10	10	12	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_TMIM5T	ctmm5t breakdown voltage @ Ibr=0.6μA	20	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CAA_TMIM5T	ctmm5t area capacitance @ Vbias=0V	2.55	2.77	3	3.23	3.45	fF/μm²
CAP_TMIM5T	ctmm5t perimeter capacitance	-	-	365	-	-	aF/μm
IL_TMIM5T	ctmm5t leakage current @ VL=7V	-	-	-	0.1	-	fA/μm²
QF_TMIM5T	ctmm5t quality factor @ f=1GHz	-	-	65	-	-	-
TCCTMIM5T	ctmm5t temperature coefficient	-	-	40	-	-	1e-06/K

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Name	Description	LSL	Low	Typ	High	USL	Unit
THD_TMIM5T	ctmm5t equivalent dielectric thickness @ Er=7.3	-	-	22	-	-	nm
VC1_TMIM5T	ctmm5t capacitor voltage coefficient 1	-	-	-15	-	-	ppm/V
VC2_TMIM5T	ctmm5t capacitor voltage coefficient 2	-	-	3.5	-	-	ppm/V^2

Matching parameters

Name	Description	Typ	Unit
AC_TMIM	Pelgrom coefficient capacitor mismatch	0.16	%µm

3.31 MIMH module

3.31.1 Device parameters

cmmh4t

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-50	-45	45	50	V
Vterm1-Vterm2	-40°C to 175°C	-7	-5.5	5.5	7	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_MIMH4T	cmmh4t breakdown voltage @ Ibr=0.6μA	10	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CAA_MIMH4TB	cmmh4t area capacitance @ Vbias=0V	1.75	2.05	2.35	2.65	2.95	fF/μm²
CAP_MIMH4T	cmmh4t perimeter capacitance	-	-	67	-	-	aF/μm
IL_MIMH4T	cmmh4t leakage current @ VL=7V	-	-	-	10	-	fA/μm²
QF_MIMH4T	cmmh4t quality factor @ f=1GHz	-	-	90	-	-	-
TCCMIMH4T	cmmh4t temperature coefficient	-	-	47	-	-	1e-06/K
THD_MIMH4TB	cmmh4t equivalent dielectric thickness @ Er=7.3	-	-	27.6	-	-	nm
VC1_MIMH4T	cmmh4t capacitor voltage coefficient 1	-	-	-120	-	-	ppm/V
VC2_MIMH4T	cmmh4t capacitor voltage coefficient 2	-	-	35	-	-	ppm/V²

Matching parameters

Name	Description	Typ	Unit
AC_MIMH	Pelgrom coefficient capacitor mismatch	0.3	%μm

cmmh5t

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-50	-45	45	50	V
Vterm1-Vterm2	-40°C to 175°C	-7	-5.5	5.5	7	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_MIMH5T	cmmh5t breakdown voltage @ Ibr=0.6μA	10	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CAA_MIMH5TB	cmmh5t area capacitance @ Vbias=0V	1.75	2.05	2.35	2.65	2.95	fF/μm²
CAP_MIMH5T	cmmh5t perimeter capacitance	-	-	67	-	-	aF/μm
IL_MIMH5T	cmmh5t leakage current @ VL=7V	-	-	-	10	-	fA/μm²
QF_MIMH5T	cmmh5t quality factor @ f=1GHz	-	-	90	-	-	-

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Name	Description	LSL	Low	Typ	High	USL	Unit
TCCMIMH5T	cmmh5t temperature coefficient	-	-	47	-	-	1e-06/K
THD_MIMH5TB	cmmh5t equivalent dielectric thickness @ Er=7.3	-	-	27.6	-	-	nm
VC1_MIMH5T	cmmh5t capacitor voltage coefficient 1	-	-	-120	-	-	ppm/V
VC2_MIMH5T	cmmh5t capacitor voltage coefficient 2	-	-	35	-	-	ppm/V²

Matching parameters

Name	Description	Typ	Unit
AC_MIMH	Pelgrom coefficient capacitor mismatch	0.3	%µm

cmmh6t

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-50	-45	45	50	V
Vterm1-Vterm2	-40°C to 175°C	-7	-5.5	5.5	7	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_MIMH6T	cmmh6t breakdown voltage @ Ibr=0.6µA	10	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CAA_MIMH6TB	cmmh6t area capacitance @ Vbias=0V	1.75	2.05	2.35	2.65	2.95	fF/µm²
CAP_MIMH6T	cmmh6t perimeter capacitance	-	-	67	-	-	aF/µm
IL_MIMH6T	cmmh6t leakage current @ VL=7V	-	-	-	10	-	fA/µm²
QF_MIMH6T	cmmh6t quality factor @ f=1GHz	-	-	90	-	-	-
TCCMIMH6T	cmmh6t temperature coefficient	-	-	47	-	-	1e-06/K
THD_MIMH6TB	cmmh6t equivalent dielectric thickness @ Er=7.3	-	-	27.6	-	-	nm
VC1_MIMH6T	cmmh6t capacitor voltage coefficient 1	-	-	-120	-	-	ppm/V
VC2_MIMH6T	cmmh6t capacitor voltage coefficient 2	-	-	35	-	-	ppm/V²

Matching parameters

Name	Description	Typ	Unit
AC_MIMH	Pelgrom coefficient capacitor mismatch	0.3	%µm

3.32 MIMH23 module

3.32.1 Device parameters

cmmh3

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-50	-45	45	50	V
Vterm1-Vterm2	-40°C to 175°C	-7	-5.5	5.5	7	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_MIMH3	cmmh3 breakdown voltage @ Ibr=0.6μA	10	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CAA_MIMH3B	cmmh3 area capacitance @ Vbias=0V	1.75	2.1	2.35	2.7	2.95	fF/μm²
CAP_MIMH3	cmmh3 perimeter capacitance	-	-	67	-	-	aF/μm
IL_MIMH3	cmmh3 leakage current @ VL=7V	-	-	-	10	-	fA/μm²
QF_MIMH3	cmmh3 quality factor @ f=1GHz	-	-	90	-	-	-
TCCMIMH3	cmmh3 temperature coefficient	-	-	47	-	-	1e-06/K
THD_MIMH3	cmmh3 equivalent dielectric thickness @ Er=7.3	-	-	27.6	-	-	nm
VC1_MIMH3	cmmh3 capacitor voltage coefficient 1	-	-	-120	-	-	ppm/V
VC2_MIMH3	cmmh3 capacitor voltage coefficient 2	-	-	35	-	-	ppm/V²

Matching parameters

Name	Description	Typ	Unit
AC_MIMH	Pelgrom coefficient capacitor mismatch	0.3	%μm

3.33 MIMH34 module

3.33.1 Device parameters

cmmh4

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-50	-45	45	50	V
Vterm1-Vterm2	-40°C to 175°C	-7	-5.5	5.5	7	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_MIMH4	cmmh4 breakdown voltage @ Ibr=0.6μA	10	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CAA_MIMH4B	cmmh4 area capacitance @ Vbias=0V	1.75	2.1	2.35	2.7	2.95	fF/μm²
CAP_MIMH4	cmmh4 perimeter capacitance	-	-	67	-	-	aF/μm
IL_MIMH4	cmmh4 leakage current @ VL=7V	-	-	-	10	-	fA/μm²
QF_MIMH4	cmmh4 quality factor @ f=1GHz	-	-	90	-	-	-
TCCMIMH4	cmmh4 temperature coefficient	-	-	47	-	-	1e-06/K
THD_MIMH4	cmmh4 equivalent dielectric thickness @ Er=7.3	-	-	27.6	-	-	nm
VC1_MIMH4	cmmh4 capacitor voltage coefficient 1	-	-	-120	-	-	ppm/V
VC2_MIMH4	cmmh4 capacitor voltage coefficient 2	-	-	35	-	-	ppm/V²

Matching parameters

Name	Description	Typ	Unit
AC_MIMH	Pelgrom coefficient capacitor mismatch	0.3	%μm

3.34 DMIMH module

3.34.1 Device parameters

cdmmh4

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-50	-45	45	50	V
Vterm1-Vterm2	-40°C to 175°C	-7	-5.5	5.5	7	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_DMIMH4	cdmmh4 breakdown voltage @ Ibr=0.6μA	10	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CAA_DMIMH4B	cdmmh4 area capacitance @ Vbias=0V	3.5	4.1	4.7	5.3	5.9	fF/μm²
CAP_DMIMH4	cdmmh4 perimeter capacitance	-	-	220	-	-	aF/μm
IL_DMIMH4	cdmmh4 leakage current @ VL=7V	-	-	-	10	-	fA/μm²
QF_DMIMH4	cdmmh4 quality factor @ f=1GHz	-	-	40	-	-	-
TCCDMIMH4	cdmmh4 temperature coefficient	-	-	47	-	-	1e-06/K
THD_DMIMH4B	cdmmh4 equivalent dielectric thickness @ Er=7.3	-	-	13.8	-	-	nm
VC1_DMIMH4	cdmmh4 capacitor voltage coefficient 1	-	-	-20	-	-	ppm/V
	Note: As the capacitors' connections are cross-coupled, the linear voltage coefficient term is small.						
VC2_DMIMH4	cdmmh4 capacitor voltage coefficient 2	-	-	35	-	-	ppm/V²

Matching parameters

Name	Description	Typ	Unit
AC_DMIMH	Pelgrom coefficient capacitor mismatch	0.22	%μm

cdmmh4t

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-50	-45	45	50	V
Vterm1-Vterm2	-40°C to 175°C	-7	-5.5	5.5	7	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_DMIMH4T	cdmmh4t breakdown voltage @ Ibr=0.6μA	10	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CAA_DMIMH4TB	cdmmh4t area capacitance @ Vbias=0V	3.5	4.1	4.7	5.3	5.9	fF/μm²
CAP_DMIMH4T	cdmmh4t perimeter capacitance	-	-	220	-	-	aF/μm
IL_DMIMH4T	cdmmh4t leakage current @ VL=7V	-	-	-	10	-	fA/μm²

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Name	Description	LSL	Low	Typ	High	USL	Unit
QF_DMIMH4T	cdmmh4t quality factor @ f=1GHz	-	-	40	-	-	-
TCCDMIMH4T	cdmmh4t temperature coefficient	-	-	47	-	-	1e-06/K
THD_DMIMH4TB	cdmmh4t equivalent dielectric thickness @ Er=7.3	-	-	13.8	-	-	nm
VC1_DMIMH4T	cdmmh4t capacitor voltage coefficient 1	-	-	-20	-	-	ppm/V
	Note: As the capacitors' connections are cross-coupled, the linear voltage coefficient term is small.						
VC2_DMIMH4T	cdmmh4t capacitor voltage coefficient 2	-	-	35	-	-	ppm/V²

Matching parameters

Name	Description	Typ	Unit
AC_DMIMH	Pelgrom coefficient capacitor mismatch	0.22	%µm

3.35 TMIMH module

3.35.1 Device parameters

ctmmh5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-50	-45	45	50	V
Vterm1-Vterm2	-40°C to 175°C	-7	-5.5	5.5	7	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_TMIMH5	ctmmh5 breakdown voltage @ Ibr=0.6μA	10	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CAA_TMIMH5B	ctmmh5 area capacitance @ Vbias=0V	5.25	6.15	7.05	7.95	8.85	fF/μm²
CAP_TMIMH5	ctmmh5 perimeter capacitance	-	-	300	-	-	aF/μm
IL_TMIMH5	ctmmh5 leakage current @ VL=7V	-	-	-	10	-	fA/μm²
QF_TMIMH5	ctmmh5 quality factor @ f=1GHz	-	-	30	-	-	-
TCCTMIMH5	ctmmh5 temperature coefficient	-	-	47	-	-	1e-06/K
THD_TMIMH5B	ctmmh5 equivalent dielectric thickness @ Er=7.3	-	-	9.2	-	-	nm
VC1_TMIMH5	ctmmh5 capacitor voltage coefficient 1	-	-	-120	-	-	ppm/V
VC2_TMIMH5	ctmmh5 capacitor voltage coefficient 2	-	-	35	-	-	ppm/V²

Matching parameters

Name	Description	Typ	Unit
AC_TMIMH	Pelgrom coefficient capacitor mismatch	0.17	%μm

ctmmh5t

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-50	-45	45	50	V
Vterm1-Vterm2	-40°C to 175°C	-7	-5.5	5.5	7	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_TMIMH5T	ctmmh5t breakdown voltage @ Ibr=0.6μA	10	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CAA_TMIMH5TB	ctmmh5t area capacitance @ Vbias=0V	5.25	6.15	7.05	7.95	8.85	fF/μm²
CAP_TMIMH5T	ctmmh5t perimeter capacitance	-	-	300	-	-	aF/μm
IL_TMIMH5T	ctmmh5t leakage current @ VL=7V	-	-	-	10	-	fA/μm²
QF_TMIMH5T	ctmmh5t quality factor @ f=1GHz	-	-	30	-	-	-

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Name	Description	LSL	Low	Typ	High	USL	Unit
TCCTMIMH5T	ctmmh5t temperature coefficient	-	-	47	-	-	1e-06/K
THD_TMIMH5TB	ctmmh5t equivalent dielectric thickness @ Er=7.3	-	-	9.2	-	-	nm
VC1_TMIMH5T	ctmmh5t capacitor voltage coefficient 1	-	-	-120	-	-	ppm/V
VC2_TMIMH5T	ctmmh5t capacitor voltage coefficient 2	-	-	35	-	-	ppm/V²

Matching parameters

Name	Description	Typ	Unit
AC_TMIMH	Pelgrom coefficient capacitor mismatch	0.17	%µm

3.36 NVM module

Ready-to-use SONOS based non-volatile memory blocks are available for NVM (NVRAM) and FLASH (Flash) modules.

The parameters of layers and devices only used for the non-volatile memories are not described in this specification. Special additional tests are performed for the quality monitoring of the non-volatile memories.

The parameters and characteristics of the different non-volatile IP blocks are described in the corresponding IP block specifications

3.37 FLASH module

Ready-to-use SONOS based non-volatile memory blocks are available for NVM (NVRAM) and FLASH (Flash) modules.

The parameters of layers and devices only used for the non-volatile memories are not described in this specification. Special additional tests are performed for the quality monitoring of the non-volatile memories.

The parameters and characteristics of the different non-volatile IP blocks are described in the corresponding IP block specifications

3.38 OTP3 module

Ready-to-use trim OTP blocks are available for OTP3 module (compiler). The parameters and characteristics of the OTP IP blocks are described in the corresponding block specification.

3.39 ANODOP module

3.39.1 Device independent parameters

Structural and geometrical parameters

Name	Description	Typ	Unit
XJ_PANODOP	ANODOP junction depth	200	nm

Sheet and contact resistance parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSS_OA	ANODOP sheet resistance @ W=5µm	166	187	208	229	250	Ω/□

3.39.2 Device parameters

dphod

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode[1]	-40°C to 125°C	-6	-5	0	0.5	V
Vanode-Vcathode[2]	-40°C to 125°C	-12	-10	0	0.5	V

Note 1 anode=anode1

Note 2 anode=anode2

Note: The photodiode must not be used in forward operation for normal operation mode.
Vpoly & Vanode1 & Vanode2 = 0V, Vguard=0.9V, Vcathode sweep
Vpoly = Vanode1 is mandatory

Process parameters

Anode1: ANODOP, Cathode: NWELL, Anode2: p-Epi Substrate

Name	Description	Low	Typ	High	Unit
CJA_1DPHD	area junction capacitance pn 1	-	0.93	-	fF/µm²
CJP_1DPHD	perimeter junction capacitance pn 1	-	0.001	-	fF/µm
ILA_1DPHD	diode area leakage current pn 1 @ Vrev=3.6V, T=27°C	-	0.2	-	aA/µm²
ILA_1DPHDHT	diode area leakage current pn 1 @ Vrev=3.6V, T=125°C	-	1.15	-	fA/µm²
ILP_1DPHD	diode perimeter leakage current pn 1 @ Vrev=3.6V, T=27°C	-	0.85	-	fA/µm
ILP_1DPHDHT	diode perimeter leakage current pn 1 @ Vrev=3.6V, T=125°C	-	200	-	fA/µm
MJA_1DPHD	area grading coefficient pn 1	-	0.37	-	-
MJP_1DPHD	sidewall grading coefficient pn 1	-	0.01	-	-
ORP_1DPHD300	optical responsivity anode 1 @ Vrev=2V, T=27°C, λ=300nm	-	0.11	-	A/W
ORP_1DPHD405	optical responsivity anode 1 @ Vrev=2V, T=27°C, λ=405nm	-	0.21	-	A/W
ORP_1DPHD650	optical responsivity anode 1 @ Vrev=2V, T=27°C, λ=650nm	-	0.07	-	A/W
ORP_1DPHD850	optical responsivity anode 1 @ Vrev=2V, T=27°C, λ=850nm	-	0.01	-	A/W

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Name	Description	Low	Typ	High	Unit
PBA_1DPHD	diffusion potential area pn 1	-	0.73	-	V
PBP_1DPHD	diffusion potential perimeter pn 1	-	0.86	-	V
CJA_2DPHD	area junction capacitance pn 2	-	0.1	-	fF/µm²
CJP_2DPHD	perimeter junction capacitance pn 2	-	0.47	-	fF/µm
ILA_2DPHD	diode area leakage current pn 2 @ Vrev=3.6V, T=27°C	-	-	0.1	aA/µm²
ILA_2DPHDHT	diode area leakage current pn 2 @ Vrev=3.6V, T=125°C	-	1.5	-	fA/µm²
ILP_2DPHD	diode perimeter leakage current pn 2 @ Vrev=3.6V, T=27°C	-	0.38	-	fA/µm
ILP_2DPHDHT	diode perimeter leakage current pn 2 @ Vrev=3.6V, T=125°C	-	250	-	fA/µm
MJA_2DPHD	area grading coefficient pn 2	-	0.47	-	-
MJP_2DPHD	sidewall grading coefficient pn 2	-	0.14	-	-
ORP_2DPHD300	optical responsivity anode 2 @ Vrev=2V, T=27°C, λ=300nm	-	-	0.003	A/W
ORP_2DPHD405	optical responsivity anode 2 @ Vrev=2V, T=27°C, λ=405nm	-	0.01	-	A/W
ORP_2DPHD650	optical responsivity anode 2 @ Vrev=2V, T=27°C, λ=650nm	-	0.3	-	A/W
ORP_2DPHD850	optical responsivity anode 2 @ Vrev=2V, T=27°C, λ=850nm	-	0.25	-	A/W
PBA_2DPHD	diffusion potential area pn 2	-	0.62	-	V
PBP_2DPHD	diffusion potential perimeter pn 2	-	0.36	-	V

Note: Optical responsivity measurement bias conditions: Vpoly = Vanode1=0V, Vcathode= 2V, Vanode2= 0V, Vguard= 0.9V

dphod0

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode(1	-40°C to 125°C	-6	-5	0	0.5	V
Vanode-Vcathode(2	-40°C to 125°C	-12	-10	0	0.5	V

Note 1 anode=anode1

Note 2 anode=anode2

Note: The photodiode must not be used in forward operation for normal operation mode.
Vpoly & Vanode1 & Vanode2 = 0V, Vguard=0.9V, Vcathode sweep
Vpoly = Vanode1 is mandatory

Process parameters

Anode1: ANODOP, Cathode: NWELL, Anode2: p-Epi Substrate

Name	Description	Low	Typ	High	Unit
CJA_1DPHD0	area junction capacitance pn 1	-	0.94	-	fF/µm²
CJP_1DPHD0	perimeter junction capacitance pn 1	-	0.001	-	fF/µm
ILA_1DPHD0	diode area leakage current pn 1 @ Vrev=3.6V, T=27°C	-	0.6	-	aA/µm²
ILA_1DPHD0HT	diode area leakage current pn 1 @ Vrev=3.6V, T=125°C	-	0.51	-	fA/µm²
ILP_1DPHD0	diode perimeter leakage current pn 1 @ Vrev=3.6V, T=27°C	-	1	-	fA/µm

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Name	Description	Low	Typ	High	Unit
ILP_1DPHD0HT	diode perimeter leakage current pn 1 @ Vrev=3.6V, T=125°C	-	250	-	fA/µm
MJA_1DPHD0	area grading coefficient pn 1	-	0.37	-	-
MJP_1DPHD0	sidewall grading coefficient pn 1	-	0.01	-	-
ORP_1DPHD0300	optical responsivity anode 1 @ Vrev=2V, T=27°C, λ=300nm	-	-	0.003	A/W
ORP_1DPHD0405	optical responsivity anode 1 @ Vrev=2V, T=27°C, λ=405nm	-	-	0.003	A/W
ORP_1DPHD0650	optical responsivity anode 1 @ Vrev=2V, T=27°C, λ=650nm	-	-	0.003	A/W
ORP_1DPHD0850	optical responsivity anode 1 @ Vrev=2V, T=27°C, λ=850nm	-	-	0.003	A/W
PBA_1DPHD0	diffusion potential area pn 1	-	0.73	-	V
PBP_1DPHD0	diffusion potential perimeter pn 1	-	0.86	-	V
CJA_2DPHD0	area junction capacitance pn 2	-	0.1	-	fF/µm²
CJP_2DPHD0	perimeter junction capacitance pn 2	-	0.45	-	fF/µm
ILA_2DPHD0	diode area leakage current pn 2 @ Vrev=3.6V, T=27°C	-	-	0.1	aA/µm²
ILA_2DPHD0HT	diode area leakage current pn 2 @ Vrev=3.6V, T=125°C	-	1.7	-	fA/µm²
ILP_2DPHD0	diode perimeter leakage current pn 2 @ Vrev=3.6V, T=27°C	-	0.4	-	fA/µm
ILP_2DPHD0HT	diode perimeter leakage current pn 2 @ Vrev=3.6V, T=125°C	-	280	-	fA/µm
MJA_2DPHD0	area grading coefficient pn 2	-	0.48	-	-
MJP_2DPHD0	sidewall grading coefficient pn 2	-	0.13	-	-
ORP_2DPHD0300	optical responsivity anode 2 @ Vrev=2V, T=27°C, λ=300nm	-	-	0.003	A/W
ORP_2DPHD0405	optical responsivity anode 2 @ Vrev=2V, T=27°C, λ=405nm	-	-	0.003	A/W
ORP_2DPHD0650	optical responsivity anode 2 @ Vrev=2V, T=27°C, λ=650nm	-	-	0.003	A/W
ORP_2DPHD0850	optical responsivity anode 2 @ Vrev=2V, T=27°C, λ=850nm	-	-	0.003	A/W
PBA_2DPHD0	diffusion potential area pn 2	-	0.56	-	V
PBP_2DPHD0	diffusion potential perimeter pn 2	-	0.36	-	V

Note: Optical responsivity measurement bias conditions: Vpoly = Vanode1=0V, Vcathode= 2V, Vanode2= 0V, Vguard= 0.9V

dphodfp

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode[1]	-40°C to 125°C	-6	-5	0	0.5	V
Vanode-Vcathode[2]	-40°C to 125°C	-12	-10	0	0.5	V

Note 1 anode=anode1

Note 2 anode=anode2

Note: The photodiode must not be used in forward operation for normal operation mode.
Vpoly & Vanode1 & Vanode2 = 0V, Vguard=0.9V, Vcathode sweep
Vpoly = Vanode1 is mandatory

Process parameters

Anode1: ANODOP, Cathode: NWELL, Anode2: p-Epi Substrate

Name	Description	Low	Typ	High	Unit
CJA_1DPHDFP	area junction capacitance pn 1	-	0.94	-	fF/µm²
CJP_1DPHDFP	perimeter junction capacitance pn 1	-	0.001	-	fF/µm
ILA_1DPHDFP	diode area leakage current pn 1 @ Vrev=3.6V, T=27°C	-	0.6	-	aA/µm²
ILA_1DPHDFPHT	diode area leakage current pn 1 @ Vrev=3.6V, T=125°C	-	0.64	-	fA/µm²
ILP_1DPHDFP	diode perimeter leakage current pn 1 @ Vrev=3.6V, T=27°C	-	0.9	-	fA/µm
ILP_1DPHDFPHT	diode perimeter leakage current pn 1 @ Vrev=3.6V, T=125°C	-	210	-	fA/µm
MJA_1DPHDFP	area grading coefficient pn 1	-	0.37	-	-
MJP_1DPHDFP	sidewall grading coefficient pn 1	-	0.01	-	-
ORP_1DPHDFP300	optical responsivity anode 1 @ Vrev=2V, T=27°C, λ=300nm	-	-	0.003	A/W
ORP_1DPHDFP405	optical responsivity anode 1 @ Vrev=2V, T=27°C, λ=405nm	-	0.01	-	A/W
ORP_1DPHDFP650	optical responsivity anode 1 @ Vrev=2V, T=27°C, λ=650nm	-	0.06	-	A/W
ORP_1DPHDFP850	optical responsivity anode 1 @ Vrev=2V, T=27°C, λ=850nm	-	0.02	-	A/W
PBA_1DPHDFP	diffusion potential area pn 1	-	0.73	-	V
PBP_1DPHDFP	diffusion potential perimeter pn 1	-	0.33	-	V
CJA_2DPHDFP	area junction capacitance pn 2	-	0.1	-	fF/µm²
CJP_2DPHDFP	perimeter junction capacitance pn 2	-	0.47	-	fF/µm
ILA_2DPHDFP	diode area leakage current pn 2 @ Vrev=3.6V, T=27°C	-	0.1	-	aA/µm²
ILA_2DPHDFPHT	diode area leakage current pn 2 @ Vrev=3.6V, T=125°C	-	1.4	-	fA/µm²
ILP_2DPHDFP	diode perimeter leakage current pn 2 @ Vrev=3.6V, T=27°C	-	0.4	-	fA/µm
ILP_2DPHDFPHT	diode perimeter leakage current pn 2 @ Vrev=3.6V, T=125°C	-	270	-	fA/µm
MJA_2DPHDFP	area grading coefficient pn 2	-	0.48	-	-
MJP_2DPHDFP	sidewall grading coefficient pn 2	-	0.15	-	-
ORP_2DPHDFP300	optical responsivity anode 2 @ Vrev=2V, T=27°C, λ=300nm	-	-	0.003	A/W
ORP_2DPHDFP405	optical responsivity anode 2 @ Vrev=2V, T=27°C, λ=405nm	-	0.01	-	A/W
ORP_2DPHDFP650	optical responsivity anode 2 @ Vrev=2V, T=27°C, λ=650nm	-	0.3	-	A/W
ORP_2DPHDFP850	optical responsivity anode 2 @ Vrev=2V, T=27°C, λ=850nm	-	0.24	-	A/W
PBA_2DPHDFP	diffusion potential area pn 2	-	0.57	-	V
PBP_2DPHDFP	diffusion potential perimeter pn 2	-	0.36	-	V

Note: Optical responsivity measurement bias conditions: Vpoly = Vanode1=0V, Vcathode= 2V, Vanode2= 0V, Vguard= 0.9V

3.40 CATDOP module

3.40.1 Device independent parameters

Structural and geometrical parameters

Name	Description	Typ	Unit
XJ_NCATDOP	CATDOP junction depth	200	nm

Sheet and contact resistance parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSS_OC	CATDOP sheet resistance @ W=5µm	925	1000	1075	1150	1225	Ω/□

3.40.2 Device parameters

dphoc

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 125°C	-12	-10	0	0.5	V

Note: The photodiode must not be used in forward operation for normal operation mode.
Vpoly & Vcathode synch. sweep, Vguard=0.9V, Vanode=0V
Vpoly = Vcathode is mandatory

Process parameters

Cathode: CATDOP, Anode: p-epi Substrate

Name	Description	Typ	Unit
CJA_DPHC	area junction capacitance	0.11	fF/µm²
CJP_DPHC	perimeter junction capacitance	0.17	fF/µm
ILA_DPHC	diode area leakage current @ Vrev=3.6V, T=27°C	0.7	aA/µm²
ILA_DPHCHT	diode area leakage current @ Vrev=3.6V, T=125°C	1.5	fA/µm²
ILP_DPHC	diode perimeter leakage current @ Vrev=3.6V, T=27°C	0.28	fA/µm
ILP_DPHCHT	diode perimeter leakage current @ Vrev=3.6V, T=125°C	210	fA/µm
MJA_DPHC	area grading coefficient	0.4	-
MJP_DPHC	sidewall grading coefficient	0.15	-
ORP_DPHC300	optical responsivity @ Vrev=2V, T=27°C, λ=300nm	0.11	A/W
ORP_DPHC405	optical responsivity @ Vrev=2V, T=27°C, λ=405nm	0.23	A/W
ORP_DPHC650	optical responsivity @ Vrev=2V, T=27°C, λ=650nm	0.39	A/W
ORP_DPHC850	optical responsivity @ Vrev=2V, T=27°C, λ=850nm	0.26	A/W
PBA_DPHC	diffusion potential area	0.38	V
PBP_DPHC	diffusion potential perimeter	0.36	V

Note: Optical responsivity measurement bias conditions: Vpoly = Vcathode = 2V, Vguard= 0.9V

dphoc0

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 125°C	-12	-10	0	0.5	V

Note: The photodiode must not be used in forward operation for normal operation mode.
Vpoly & Vcathode synch. sweep, Vguard=0.9V, Vanode=0V
Vpoly = Vcathode is mandatory

Process parameters

Cathode: CATDOP, Anode: p-epi Substrate

Name	Description	Low	Typ	High	Unit
CJA_DPHC0	area junction capacitance	-	0.12	-	fF/µm²
CJP_DPHC0	perimeter junction capacitance	-	0.17	-	fF/µm
ILA_DPHC0	diode area leakage current @ Vrev=3.6V, T=27°C	-	0.4	-	aA/µm²
ILA_DPHC0HT	diode area leakage current @ Vrev=3.6V, T=125°C	-	1.6	-	fA/µm²
ILP_DPHC0	diode perimeter leakage current @ Vrev=3.6V, T=27°C	-	0.41	-	fA/µm²
ILP_DPHC0HT	diode perimeter leakage current @ Vrev=3.6V, T=125°C	-	275	-	fA/µm
MJA_DPHC0	area grading coefficient	-	0.32	-	-
MJP_DPHC0	sidewall grading coefficient	-	0.15	-	-
ORP_DPHC0300	optical responsivity @ Vrev=2V, T=27°C, λ=300nm	-	-	0.003	A/W
ORP_DPHC0405	optical responsivity @ Vrev=2V, T=27°C, λ=405nm	-	-	0.003	A/W
ORP_DPHC0650	optical responsivity @ Vrev=2V, T=27°C, λ=650nm	-	-	0.003	A/W
ORP_DPHC0850	optical responsivity @ Vrev=2V, T=27°C, λ=850nm	-	-	0.003	A/W
PBA_DPHC0	diffusion potential area	-	0.38	-	V
PBP_DPHC0	diffusion potential perimeter	-	0.36	-	V

Note: Optical responsivity measurement bias conditions: Vpoly = Vcathode = 2V, Vguard= 0.9V

dphocfp

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 125°C	-12	-10	0	0.5	V

Note: The photodiode must not be used in forward operation for normal operation mode.
Vpoly & Vcathode synch. sweep, Vguard=0.9V, Vanode=0V
Vpoly = Vcathode is mandatory

Process parameters

Cathode: CATDOP, Anode: p-epi Substrate

Name	Description	Low	Typ	High	Unit
CJA_DPHCFP	area junction capacitance	-	0.1	-	fF/µm²
CJP_DPHCFP	perimeter junction capacitance	-	0.15	-	fF/µm
ILA_DPHCFP	diode area leakage current @ Vrev=3.6V, T=27°C	-	0.4	-	aA/µm²
ILA_DPHCFPHT	diode area leakage current @ Vrev=3.6V, T=125°C	-	11	-	fA/µm²
ILP_DPHCFP	diode perimeter leakage current @ Vrev=3.6V, T=27°C	-	0.44	-	fA/µm
ILP_DPHCFPHT	diode perimeter leakage current @ Vrev=3.6V, T=125°C	-	250	-	fA/µm
MJA_DPHCFP	area grading coefficient	-	0.44	-	-
MJP_DPHCFP	sidewall grading coefficient	-	0.18	-	-
ORP_DPHCFP300	optical responsivity @ Vrev=2V, T=27°C, λ=300nm	-	-	0.003	A/W
ORP_DPHCFP405	optical responsivity @ Vrev=2V, T=27°C, λ=405nm	-	0.02	-	A/W
ORP_DPHCFP650	optical responsivity @ Vrev=2V, T=27°C, λ=650nm	-	0.34	-	A/W

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Name	Description	Low	Typ	High	Unit
ORP_DPHCFP850	optical responsivity @ Vrev=2V, T=27°C, λ=850nm	-	0.25	-	A/W
PBA_DPHCFP	diffusion potential area	-	0.45	-	V
PBP_DPHCFP	diffusion potential perimeter	-	0.36	-	V

Note: Optical responsivity measurement bias conditions: Vpoly = Vcathode = 2V, Vguard= 0.9V

3.41 UVWINDOW module

UVWINDOW is only allowed with module ANODOP or CATDOP and there are no additional parameters here for these modules.

3.42 AVLA module

3.42.1 Device independent parameters

Structural and geometrical parameters

Name	Description	Typ	Unit
XJ_AML	AML junction depth	350	nm

3.42.2 Device parameters

dapda

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode[1]	-40°C to 175°C	-	-23	0	0.5	V
Plight[2]	-40°C to 175°C	-	-	0.1	-	W/cm²
Plight[3]	-40°C to 175°C	-	-	-	0.01	W

Note 1 Voltage range valid for current values below 1mA.

Note 2 Max light power (0.1 W/cm² or 3.2 µW) is the operating condition, where the gain drops 10 % due to the high photo current for a maximum W and L device with homogeneous light distribution. Lower light power (0.32 µW) is required, in case the light hits as a small (10 µm) spot in the centre of the device.

Note 3 Abs. max light power is the operating point where the device gets damaged permanently. The stated value is at the maximum response wavelength of 710 nm. Higher light power is possible at lower response wavelengths. This limit is independent of the light distribution within the device.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVJ_DAVLA	breakdown voltage @ Irev=10nA/µm², T=27°C	18.9	19.25	19.6	19.95	20.3	V
BVJ_DAVLAHT	breakdown voltage @ Irev=10nA/µm², T=85°C	-	-	20.4	-	-	V
BVJ_DAVLALT	breakdown voltage @ Irev=10nA/µm², T=-40°C	-	-	18.2	-	-	V
CJA_DAPDA	area junction capacitance @ Vrev=0V, T=27°C	-	-	0.45	-	-	fF/µm²
CJA_DAPDA1	area junction capacitance, Vrev=1% below BV @ T=27°C	-	-	0.18	-	-	fF/µm²
CJP_DAPDA	perimeter junction capacitance @ Vrev=0V, T=27°C	-	-	1.12	-	-	fF/µm
CJP_DAPDA1	perimeter junction capacitance, Vrev=1% below BV @ T=27°C	-	-	0.61	-	-	fF/µm
ILA_DAPDA	diode area leakage current, Vrev=1% below BV @ T=27°C	-	-	0.17	-	-	fA/µm²
ILA_DAPDAHT	diode area leakage current, Vrev=1% below BV @ T=85°C	-	-	17.8	-	-	fA/µm²
ILP_DAPDA	diode perimeter leakage current, Vrev=1% below BV @ T=27°C	-	-	2.36	-	-	fA/µm
ILP_DAPDAHT	diode perimeter leakage current, Vrev=1% below BV @ T=85°C	-	-	1.01	-	-	pA/µm
MJA_DAPDA	area grading coefficient	-	-	0.28	-	-	-
MJP_DAPDA	sidewall grading coefficient	-	-	0.17	-	-	-

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Name	Description	LSL	Low	Typ	High	USL	Unit
ORP_DAPDA405	optical responsivity, Vrev=1% below BV @ T=27°C, λ=405nm	-	-	9	-	-	A/W
ORP_DAPDA525	optical responsivity, Vrev=1% below BV @ T=27°C, λ=525nm	-	-	33	-	-	A/W
ORP_DAPDA625	optical responsivity, Vrev=1% below BV @ T=27°C, λ=625nm	-	-	43	-	-	A/W
ORP_DAPDA850	optical responsivity, Vrev=1% below BV @ T=27°C, λ=850nm	-	-	32	-	-	A/W
PBA_DAPDA	area junction potential	-	-	0.77	-	-	V
PBP_DAPDA	sidewall junction potential	-	-	0.55	-	-	V

Note: Area leakage current, perimeter leakage current and optical responsivity measurement bias conditions: Vguard=0.9 V.

dapda0

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode[1	-40°C to 175°C	-	-23	0	0.5	V

Note 1 Voltage range valid for current values below 1mA.

Note: This device is optically blind, it does not respond to light therefore no maximum light power is defined.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVJ_DAVLA	breakdown voltage @ Irev=10nA/µm², T=27°C	18.9	19.25	19.6	19.95	20.3	V
BVJ_DAVLAHT	breakdown voltage @ Irev=10nA/µm², T=85°C	-	-	20.4	-	-	V
BVJ_DAVLALT	breakdown voltage @ Irev=10nA/µm², T=-40°C	-	-	18.2	-	-	V
CJA_DAPDA0	area junction capacitance @ Vrev=0V, T=27°C	-	-	0.45	-	-	fF/µm²
CJA_DAPDA01	area junction capacitance, Vrev=1% below BV @ T=27°C	-	-	0.18	-	-	fF/µm²
CJP_DAPDA0	perimeter junction capacitance @ Vrev=0V, T=27°C	-	-	1.12	-	-	fF/µm
CJP_DAPDA01	perimeter junction capacitance, Vrev=1% below BV @ T=27°C	-	-	0.61	-	-	fF/µm
ILA_DAPDA0	diode area leakage current, Vrev=1% below BV @ T=27°C	-	-	0.11	-	-	fA/µm²
ILA_DAPDA0HT	diode area leakage current, Vrev=1% below BV @ T=85°C	-	-	17.8	-	-	fA/µm²
ILP_DAPDA0	diode perimeter leakage current, Vrev=1% below BV @ T=27°C	-	-	1.83	-	-	fA/µm
ILP_DAPDA0HT	diode perimeter leakage current, Vrev=1% below BV @ T=85°C	-	-	1.01	-	-	pA/µm
MJA_DAPDA0	area grading coefficient	-	-	0.28	-	-	-
MJP_DAPDA0	sidewall grading coefficient	-	-	0.17	-	-	-
ORP_DAPDA0405	optical responsivity, Vrev=1% below BV @ T=27°C, λ=405nm	-	-	0	-	-	A/W

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Name	Description	LSL	Low	Typ	High	USL	Unit
ORP_DAPDA0525	optical responsivity, Vrev=1% below BV @ T=27°C, λ=525nm	-	-	0	-	-	A/W
ORP_DAPDA0625	optical responsivity, Vrev=1% below BV @ T=27°C, λ=625nm	-	-	0	-	-	A/W
ORP_DAPDA0850	optical responsivity, Vrev=1% below BV @ T=27°C, λ=850nm	-	-	0	-	-	A/W
PBA_DAPDA0	area junction potential	-	-	0.77	-	-	V
PBP_DAPDA0	sidewall junction potential	-	-	0.55	-	-	V

Note: Area leakage current, perimeter leakage current and optical responsivity measurement bias conditions: Vguard=0.9 V.

dspada

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-33	-30	0	0.5	V
Plight(1	-40°C to 175°C	-	-	50	-	μW/cm²
Plight(2	-40°C to 175°C	-	-	-	0.01	W

Note 1 Max light power is the operating condition, where the count rate drops 10 % compared to an ideal quenched device. It is defined for the highest PDP at 405 nm wavelength and 15 ns quenching time, using the X-FAB quenching circuit, with an excess voltage of 2 V (2 V over breakdown voltage).

Note 2 Abs. max light power is the operating point where the device gets damaged permanently. The stated value is at the maximum response wavelength of 710 nm. Higher light power is possible at lower response wavelengths. This limit is independent of the light distribution within the device.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
APP_DSPADA	after pulsing probability @ Vexcess=2V, T=27°C	-	-	3	-	-	%
BVJ_DAVLA	breakdown voltage @ Irev=10nA/μm², T=27°C	18.9	19.25	19.6	19.95	20.3	V
BVJ_DAVLAHT	breakdown voltage @ Irev=10nA/μm², T=85°C	-	-	20.4	-	-	V
BVJ_DAVLALT	breakdown voltage @ Irev=10nA/μm², T=-40°C	-	-	18.2	-	-	V
CJ0_DSPADA	junction capacitance per cell @ Vrev=0V, T=27°C	-	-	60	-	-	fF
CJX_DSPADA	junction capacitance per cell @ Vexcess=2V, T=27°C	-	-	31	-	-	fF
DCR_DSPADA	dark count rate @ Vexcess=2V, T=27°C	-	-	-	100	-	count/(s*μm²)
DCR_DSPADAHT	dark count rate @ Vexcess=2V, T=85°C	-	-	-	1000	-	count/(s*μm²)
MJ0_DSPADA	grading coefficient	-	-	0.19	-	-	-
PB0_DSPADA	junction potential	-	-	0.67	-	-	V
PDP_DSPADA405	photon detection probability @ Vexcess=2V, λ=405nm	-	-	25	-	-	%
PDP_DSPADA525	photon detection probability @ Vexcess=2V, λ=525nm	-	-	19	-	-	%

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Name	Description	LSL	Low	Typ	High	USL	Unit
PDP_DSPADA625	photon detection probability @ Vexcess=2V, λ=625nm	-	-	9	-	-	%
PDP_DSPADA850	photon detection probability @ Vexcess=2V, λ=850nm	-	-	2	-	-	%

Note: Dark count rate, photon detection probability and after pulsing probability are based on the usage of the X-FAB active quenching circuit with an excess bias of 2 V (2 V over breakdown voltage) and 15 ns dead time.

dspada0

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-33	-30	0	0.5	V

Note: This device is optically blind, it does not respond to light therefore no maximum light power is defined.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
APP_DSPADA0	after pulsing probability @ Vexcess=2V, T=27°C	-	-	3	-	-	%
BVJ_DAVLA	breakdown voltage @ Irev=10nA/ µm², T=27°C	18.9	19.25	19.6	19.95	20.3	V
BVJ_DAVLAHT	breakdown voltage @ Irev=10nA/ µm², T=85°C	-	-	20.4	-	-	V
BVJ_DAVLALT	breakdown voltage @ Irev=10nA/ µm², T=-40°C	-	-	18.2	-	-	V
CJ0_DSPADA0	junction capacitance per cell @ Vrev=0V, T=27°C	-	-	60	-	-	fF
CJX_DSPADA0	junction capacitance per cell @ Vexcess=2V, T=27°C	-	-	31	-	-	fF
DCR_DSPADA0	dark count rate @ Vexcess=2V, T=27°C	-	-	-	100	-	count/ (s*µm²)
DCR_DSPADA0HT	dark count rate @ Vexcess=2V, T=85°C	-	-	-	1000	-	count/ (s*µm²)
MJ0_DSPADA0	grading coefficient	-	-	0.19	-	-	-
PB0_DSPADA0	junction potential	-	-	0.67	-	-	V
PDP_DSPADA0405	photon detection probability @ Vexcess=2V, λ=405nm	-	-	0	-	-	%
PDP_DSPADA0525	photon detection probability @ Vexcess=2V, λ=525nm	-	-	0	-	-	%
PDP_DSPADA0625	photon detection probability @ Vexcess=2V, λ=625nm	-	-	0	-	-	%
PDP_DSPADA0850	photon detection probability @ Vexcess=2V, λ=850nm	-	-	0	-	-	%

Note: Dark count rate, photon detection probability and after pulsing probability are based on the usage of the X-FAB active quenching circuit with an excess bias of 2 V (2 V over breakdown voltage) and 15 ns dead time.

3.43 BIPESD module

3.43.1 Device independent parameters

Structural and geometrical parameters

Name	Description	Typ	Unit
XJ_HPWDNW	HVPWELL in DNWELL junction depth	1.3	µm
XJ_NHPW	N+ source/ drain junction depth in HVPWELL	0.2	µm
XJ_PDWHN	PDF in HNW junction depth	0.9	µm
XJ_PWHN	P+ source/ drain junction depth in HNW	0.2	µm
XJ_WHN	HNW junction depth	4.5	µm

Parasitic field parameters

Name	Description	Low	Typ	High	Unit
VTFPM1WHN	p-channel threshold voltage metal 1 on field over HNW @ VD=-12V, Id=-1µA	-10	-	-	V
VTFPM2WHN	p-channel threshold voltage metal 2 on field over HNW @ VD=-12V, Id=-1µA	-25	-	-	V
VTFPP1WHN	p-channel threshold voltage poly 1 on field over HNW @ VD=-12V, Id=-1µA	-2	-	-	V
VTFPP1WHNH	p-channel threshold voltage poly 1 on field over HNW / HVNWELL @ VD=-12V, Id=-1µA	-20	-	-	V
VTFPWM2HNH	p-channel threshold voltage metal 1 on field over HNW / HVNWELL @ VD=-12V, Id=-1µA	-60	-	-	V

Note: Negative values are considered as absolute values for their limits.

Sheet and contact resistance parameters

Name	Description	Typ	Unit
RSSWHN	HNW in PSUB sheet resistance (STI terminated) @ W=6µm	3	kΩ/□

3.43.2 Device parameters

qpvhscr

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VCE	-40°C to 175°C	-50	-45	32	35	V
VEB	-40°C to 175°C	-50	-45	1.5	-	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BCBOPVH	collector- base breakdown voltage (emitter open) @ Ib=1µA	-	50	-	-	-	V
BCEOPVH	collector- emitter breakdown voltage (base open) @ Ic=1µA	51	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEBOPVH	emitter- base breakdown voltage (collector open) @ Ie=-1µA	-	50	-	-	-	V

⇒

Name	Description	LSL	Low	Typ	High	USL	Unit
BECOPVH	emitter- collector breakdown voltage (base open) @ Ie=-1µA	-35.5	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
HF_PVH1U	current gain @ Ie=1µA, L=16µm	22	26.5	31	35.5	40	-
TC_PVHVBE	base-emitter voltage temperature coefficient	-	-	-2.2	-	-	mV/K
VBEPVH	base-emitter voltage @ Ie=1µA, LE=16µm	560	567	574	581	588	mV

Matching parameters

Name	Description	Typ	Unit
SIBPHV161	standard deviation IB mismatch @ Ic=100nA, LE=16µm	0.42	%
SIBPHV162	standard deviation IB mismatch @ Ic=10µA, LE=16µm	0.22	%
SIBPHV251	standard deviation IB mismatch @ Ic=100nA, LE=25µm	0.38	%
SIBPHV252	standard deviation IB mismatch @ Ic=10µA, LE=25µm	0.19	%
SIBPHV401	standard deviation IB mismatch @ Ic=100nA, LE=40µm	0.29	%
SIBPHV402	standard deviation IB mismatch @ Ic=10µA, LE=40µm	0.15	%
SICPVH161	standard deviation IC mismatch @ Ic=100nA, LE=16µm	0.16	%
SICPVH162	standard deviation IC mismatch @ Ic=10µA, LE=16µm	0.12	%
SICPVH251	standard deviation IC mismatch @ Ic=100nA, LE=25µm	0.12	%
SICPVH252	standard deviation IC mismatch @ Ic=10µA, LE=25µm	0.1	%
SICPVH401	standard deviation IC mismatch @ Ic=100nA, LE=40µm	0.12	%
SICPVH402	standard deviation IC mismatch @ Ic=10µA, LE=40µm	0.1	%
SVBPVH161	standard deviation VBE mismatch @ Ic=100nA, LE=16µm	0.17	mV
SVBPVH162	standard deviation VBE mismatch @ Ic=10µA, LE=16µm	0.08	mV
SVBPVH251	standard deviation VBE mismatch @ Ic=100nA, LE=25µm	0.15	mV
SVBPVH252	standard deviation VBE mismatch @ Ic=10µA, LE=25µm	0.08	mV
SVBPVH401	standard deviation VBE mismatch @ Ic=100nA, LE=40µm	0.14	mV
SVBPVH402	standard deviation VBE mismatch @ Ic=10µA, LE=40µm	0.08	mV

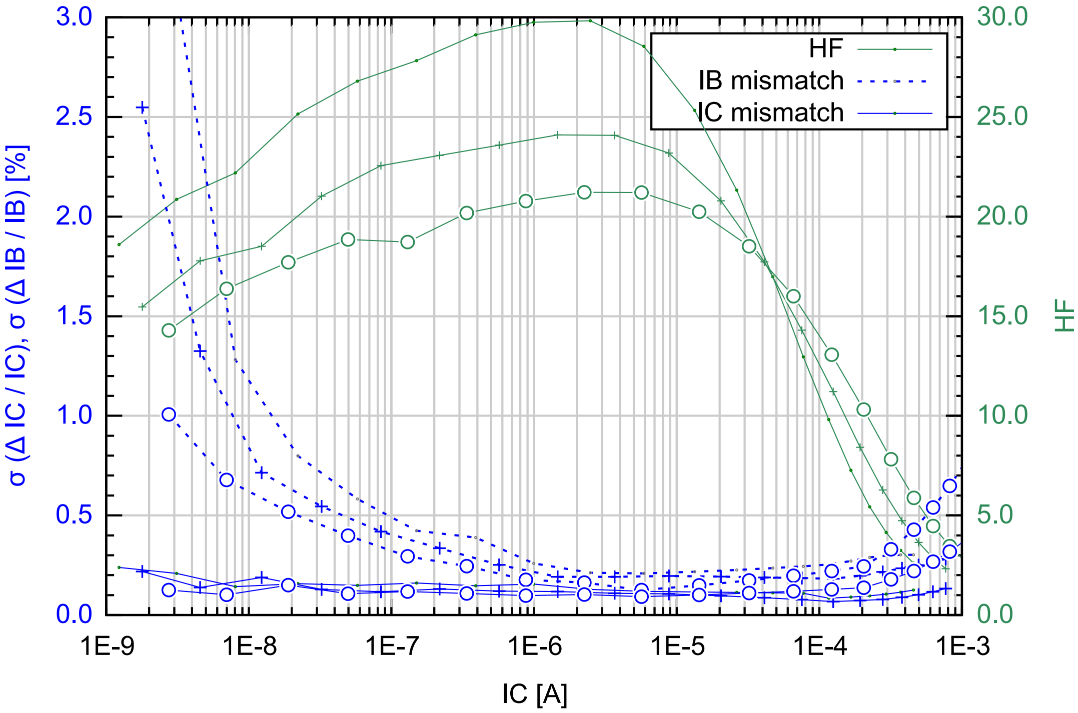

Figure 3.88 Device qpvhscr: IC matching and IB matching vs. IC (typical values) ----- LE=16µm, --+-- LE=25µm, --o-- LE=40µm

3.44 ESDPNP module

3.44.1 Device parameters

qpvhbscr

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VCE	-40°C to 175°C	-50	-45	25	27	V
VEB	-40°C to 175°C	-27	-25	1.5	-	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BCBOPVHB	collector- base breakdown voltage (emitter open) @ Ib=1µA	-	51	-	-	-	V
BCEOPVHB	collector- emitter breakdown voltage (base open) @ Ic=1µA	51	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEBOPVHB	emitter- base breakdown voltage (collector open) @ Ie=-1µA	-	28	-	-	-	V
BECOPVHB	emitter- collector breakdown voltage (base open) @ Ie=-1µA	-28	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
HF_PVHB1U	current gain @ Ie=1µA, LE=12µm	7.5	10.5	13.5	16.5	19.5	-
TC_PVHBVBE	base-emitter voltage temperature coefficient	-	-	-2.2	-	-	mV/K
VBEPVHB	base-emitter voltage @ Ie=1µA, LE=12µm	550	560	570	580	590	mV

3.45 FLATPV module

For the FLATPV module, a planar passivation layer is offered as an alternative to the standard passivation, which is non-planar. The passivation thickness above the top metal layer is unchanged, refer to parameter THV. This alternative passivation scheme may be suitable for post-processing or packaging solutions requiring planar passivation. Primitive devices are not defined for the FLATPV module.

3.45.1 Device independent parameters

Structural and geometrical parameters

Name	Description	Low	Typ	High	Unit
THV_FLAT	passivation thickness with FLATPV module	1470	1750	2030	nm

3.46 SFLATPV module

For the SFLATPV module, a smooth and planar passivation layer is offered as an alternative to the standard passivation, which is non-planar. The passivation thickness above the top metal layer is unchanged, refer to parameter THV. This alternative passivation scheme is preferable for optical applications, with post processing steps, that need to rely on optical grade (polished) interface quality. Primitive devices are not defined for the SFLATPV module.

3.46.1 Device independent parameters

Structural and geometrical parameters

Name	Description	Low	Typ	High	Unit
THV_SFLAT	passivation thickness with SFLATPV module	1470	1750	2030	nm

3.47 PIMIDE module

For the PIMIDE module, an additional resilient barrier layer on top of the passivation is applied. This overcoat of polyimide gives an improved passivation protection and stress relief of the chip.
Primitive devices are not defined for the PIMIDE module.

3.47.1 Device independent parameters

Structural and geometrical parameters

Name	Description	Low	Typ	High	Unit
THV_PMD	Polyimide thickness	3000	4000	5000	nm

3.48 PHOTODIO module

The parameters of the photodiode dphoa and dphob are valid for the recommended layout with guard ring. Please refer to the design rule specification.

3.48.1 Device parameters

dphoa

The parameters of the photodiode dphoa and dphob are valid for the recommended layout with guard ring. Please refer to the design rule specification.

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 125°C	-12	-10	0	0.5	V

Process parameters

Cathode: N+/DNWELL cathode diffusion, Anode: p-Epi substrate.

Name	Description	Typ	Unit
CJA_DPHA	area junction capacitance @ Vrev=2V	0.04	fF/µm²
CJP_DPHA	sidewall junction capacitance @ Vrev=2V	0.35	fF/µm
ILA_DPHA	diode area leakage current @ Vrev=3.6V, T=27°C	0.1	aA/µm²
ILA_DPHAHT	diode area leakage current @ Vrev=3.6V, T=125°C	0.26	fA/µm²
ILP_DPHA	diode perimeter leakage current @ Vrev=3.6V, T=27°C	0.12	fA/µm
ILP_DPHAHT	diode perimeter leakage current @ Vrev=3.6V, T=125°C	260	fA/µm
MJA_DPHA	area grading coefficient	0.57	-
MJP_DPHA	sidewall grading coefficient	0.35	-
ORP_DPHA400	optical responsivity @ Vrev=2.5V, T=27°C, λ=400nm	0.2	A/W
ORP_DPHA500	optical responsivity @ Vrev=2.5V, T=27°C, λ=500nm	0.29	A/W
ORP_DPHA650	optical responsivity @ Vrev=2.5V, T=27°C, λ=650nm	0.37	A/W
ORP_DPHA850	optical responsivity @ Vrev=2.5V, T=27°C, λ=850nm	0.26	A/W
PBA_DPHA	diffusion potential area	0.78	V
PBP_DPHA	diffusion potential perimeter	0.63	V

dphob

The parameters of the photodiode dphoa and dphob are valid for the recommended layout with guard ring. Please refer to the design rule specification.

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 125°C	-12	-10	0	0.5	V

Process parameters

Cathode: shorted P+/PWELL1 and N+/DNWELL cathode diffusion, Anode: p-Epi substrate.

Name	Description	Typ	Unit
CJA_DPHB	area junction capacitance	0.04	fF/µm²
CJP_DPHB	sidewall junction capacitance	0.36	fF/µm

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Name	Description	Typ	Unit
ILA_DPHB	diode area leakage current @ Vrev=3.6V, T=27°C	1.9	aA/µm²
ILA_DPHBHT	diode area leakage current @ Vrev=3.6V, T=125°C	175	fA/µm²
ILP_DPHB	diode perimeter leakage current @ Vrev=3.6V, T=27°C	0.13	fA/µm
ILP_DPHBHT	diode perimeter leakage current @ Vrev=3.6V, T=125°C	180	fA/µm
MJA_DPHB	area grading coefficient	0.52	-
MJP_DPHB	sidewall grading coefficient	0.35	-
ORP_DPHB500	optical responsivity @ Vrev=2.5V, T=27°C, λ=500nm	0.02	A/W
ORP_DPHB650	optical responsivity @ Vrev=2.5V, T=27°C, λ=650nm	0.19	A/W
ORP_DPHB850	optical responsivity @ Vrev=2.5V, T=27°C, λ=850nm	0.2	A/W
PBA_DPHB	diffusion potential area	0.72	V
PBP_DPHB	diffusion potential perimeter	0.61	V

3.49 HALL module

3.49.1 Device independent parameters

Structural and geometrical parameters

Name	Description	Typ	Unit
XJ_HNW	HVNWELL junction depth	1.8	µm
XJ_HPWDNW	HVPWELL in DNWELL junction depth	1.3	µm
XJ_NHPW	N+ source/ drain junction depth in HVPWELL	0.2	µm
XJ_PHNW	P+ source/ drain junction depth in HVNWELL	0.2	µm

Sheet and contact resistance parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSSHNW	HVNWELL sheet resistance (STI terminated) @ W=20µm	0.79	0.84	0.89	0.94	0.99	kΩ/☐

3.49.2 Device parameters

hall1

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 125°C	-0.5	0	1.98	2.3	V

Process parameters

The HALL module delivers a ready-to-use Hall primitive device which is available on request.

Name	Description	LSL	Low	Typ	High	USL	Unit
OTB_HALL1	static offset @ Vlow=0V, Vhigh=1V, VSUB=0V	-	-10	0	10	-	mV
RTB_HALL1	vertical resistance @ Vbias=1V	9.25	9.87	10.5	11.13	11.75	kΩ
SEN_HALL1	sensitivity @ Isupply=100µA	-	280	320	360	-	V/(A*T)
TC1_HALL1	temperature coefficient of resistance 1	-	-	4.1	-	-	1e-03/K
TC2_HALL1	temperature coefficient of resistance 2	-	-	17	-	-	1e-06/K²
TS1_HALL1	temperature coefficient of sensitivity 1	-	-	-0.84	-	-	1e-03/K
TS2_HALL1	temperature coefficient of sensitivity 2	-	-	6.2	-	-	1e-06/K²

3.50 Measurement principles

ABT **Pelgrom coefficient for MOSFET gain factor mismatch**

The gain factor (BETA) of identically designed MOSFET transistor pairs is calculated from the maximum IDS slope (transconductance) divided by the applied drain voltage. The standard deviation of the relative gain factor mismatch for selected device geometries is plotted versus the inverse square root of the device area. The slope of a linear regression through the origin of coordinates delivers the pelgrom coefficient.

AC_ **Pelgrom coefficient for capacitance mismatch**

A floating gate measurement technique with a source follower at the (floating) middle node of a capacitive voltage divider is used for the determination of the relative capacitance mismatch of identically designed capacitor pairs. By applying two input voltages (typical values Vlow= 0.5V, Vhigh= 3.5V) and measuring the corresponding output voltages at the source of the p- channel transistor a slope S1 can be determined. After exchanging the nodes of the voltage divider a second slope S2 can be measured. The resulting capacitor mismatch is defined by:

$$\frac{\Delta C}{C} = 2 \cdot \frac{S1 - S2}{S1 + S2} = \frac{C1 - C2}{C1 + C2}$$

The standard deviation of the relative capacitance mismatch for selected device geometries is plotted versus the inverse square root of the device area. The slope of a linear regression through the origin of coordinates delivers the pelgrom coefficient.

AID **Pelgrom coefficient for MOSFET drain current mismatch**

The relative drain current mismatch of identically designed MOSFET transistor pairs is calculated from drain current measurements. The measurements IDS vs VGS-VTO are performed in the saturation region and at dedicated values for VGS-VTO. The standard deviation of the relative drain current mismatch for selected device geometries is plotted versus the inverse square root of the device area. The slope of a linear regression through the origin of coordinates delivers the pelgrom coefficient.

APP **After pulsing probability**

The after pulsing probability is the probability of retriggering of avalanches by trapped charge carriers. It is measured at the specified reverse bias of Vexcess above the breakdown voltage.

AR_ **Pelgrom coefficient for resistance mismatch**

The relative resistance mismatch of identically designed resistor pairs is calculated from resistance measurements with constant current density for all devices of one type with regard to the maximum allowed terminal voltage and current density. The standard deviation of the relative resistor mismatch for selected device geometries is plotted versus the inverse square root of the device area. The slope of a linear regression through the origin of coordinates delivers the pelgrom coefficient.

AVT **Pelgrom coefficient for MOSFET threshold voltage mismatch**

The linearly extrapolated threshold voltage of identically designed MOSFET transistor pairs is determined by linear regression around the IDS/VGS-point of maximum IDS slope. The intercept with the x- axis minus half the drain voltage is taken as VTO. The standard deviation of the absolute threshold voltage mismatch for selected device geometries is plotted versus the inverse square root of the device area. The slope of a linear regression through the origin of coordinates delivers the pelgrom coefficient.

BA_ **Active breakdown voltage**

The specified base current Ib is applied. The collector-emitter voltage VCE is swept to find the minimum slope of the collector current IC as a function of VCE (minimum slope SLOPEmin at VCEmin). Starting at VCEmin, a linear IC/VCE curve is calculated with the collector current slope SLOPEmin. Then VCE is swept until the collector current reaches 125% of the corresponding calculated IC value at the active breakdown voltage.

BCB **Collector-base breakdown voltage**

Base is connected to 0V and emitter is open. The specified current is forced into collector and the collector voltage BCB is measured.

BCE **Collector-emitter breakdown voltage**

The collector-emitter voltage is swept until the collector current reaches a defined value at the breakdown voltage BCE. The measurement is either performed with the base open (BCEO) or shorted (BCES) All other terminals are floating.

BDO **Oxide breakdown**

The voltage of the capacitor is swept until a defined current is reached at the breakdown voltage BV, or until the voltage limit is reached

BDS **Drain-source breakdown voltage**

Source and substrate are connected to ground, specified gate voltage is applied, for VG=0V gate is also connected to ground. The drain voltage is swept until the current reaches the specified drain current at the breakdown voltage BDS or until the voltage limit is reached.
For specified high voltage p-channel transistors an alternate method may be used. Please refer to device specific measurement notes.

Note for BDSONNEDI, BDSONNEDIA, BDSONNHHV, BDSONNHHVD, BDSONNHV, BDSONNHVD, BDSONNMC, BDSONNMMA, BDSONNMMC, BDSONNMMD

Source and bulk are connected to ground. A static gate voltage VGS is applied at the gate. The output characteristic is measured by applying 100ns current pulses at the drain. At certain drain voltage the parasitic bipolar triggers, leading to device damage. This drain voltage defines the on-state breakdown voltage at this particular gate bias. For further information regarding the detailed ESD characteristic of the device please refer to the "XH018 TLP I-V Characteristics" document available on my X-FAB.

BEB **Emitter-base breakdown voltage**

The emitter-base voltage is swept until the emitter current reaches the defined value at the breakdown voltage BEB. The measurement is either performed with the collector open (BEBO) or shorted (BEBS). All other terminals are floating.

BEC **Emitter-collector breakdown voltage**

Collector is connected to 0V and base is open. The specified current is forced into the emitter and the emitter voltage BEC is measured.

BEX **Temperature exponent of mobility**

The gain factor KP is measured as a function of the temperature T. The temperature exponent of mobility BEX is calculated from the slope of the linear regression:

$$VTO(T) = VTO(T0) + TCV \cdot (T - T0)$$

$$ln\left[KP(T)\right] = ln\left[KP(T0)\right] + BEX \cdot \left[ln(T) - ln(T0)\right]$$

BPR **Punch-through voltage (reverse)**

The measurement conditions for the reverse punch-through are different for different device types.
NDMOS: Substrate is connected to GND. Drain is floating. All other terminals are connected together and their voltage is swept negative until the current limit Ip is reached at the reverse punch though voltage.
PDMOS: Substrate is connect to GND. Bulk, source and gate are floating. The Drain voltage is swept negative until the current limit Ip is reached at the reverse punch though voltage.
HVPMOS: Substrate, source and gate are connected to GND. Bulk is floating. The Drain voltage is swept negative until the current limit Ip is reached at reverse punch though voltage.

BVJ **Diode junction breakdown voltage**

The diode reverse voltage is swept until the diode reverse current reaches the specified current at the breakdown voltage BV, or until the voltage limit is reached. The BV values are valid for T0 = 27°C. The well to substrate breakdown is dominated by the diffusion to substrate breakdown if the well enclosure of the diffusion is not sufficient.

BVP **Punch-through voltage**

The P-substrate is connected to ground. All other terminals are connected together and the voltage is swept until the current limit Ip is reached at the punch-through voltage BVP. In some cases, the P-substrate may be swept with all other terminals grounded.

BV_ **Diode breakdown voltage**

The diode reverse voltage is swept until the diode reverse current reaches the specified current at the breakdown voltage BV.

CAA **Area capacitance**

The capacitance is measured at specified voltage and calculated per area.

CAP **Perimeter capacitance**

The fringing capacitance per length (one edge) of a single minimum width interconnect line is calculated using EDA field solver tools. Adjacent structures reduce this value.

CA_ **Capacitance**

The capacitance is measured at specified bias voltage.

Note for CA_SF3A_B, CA_SF3_B, CA_SF4A_B, CA_SF4_B, CA_SF5A_B, CA_SF5_B, CA_SFP2_B, CA_SFP3_B, CA_SFT4A_B, CA_SFT4_B, CA_SFT5A_B, CA_SFT5_B, CA_SFT6A_B, CA_SFT6_B

The capacitance for an array of capacitors is measured and the capacitance is quoted for a single cell.

CC_ **Coupling Capacitance**

The coupling capacitance per length of adjacent metal or poly lines with minimum separation is calculated using EDA field solver tools. Note, that in the case of adjacent lines the coupling capacitance dominates the fringing capacitance of the line.

CGA **Oxide area capacitance**

The capacitance per area of a large area capacitor is measured at specified bias voltage and calculated per area.

CGO **Gate overlap capacitance**

Gate to Source/Drain overlap capacitances are derived from C-V measurements of long perimeter structures (W/L >>1) and may differ from MOS model values. The model is adjusted to match measured switching performance.

CJ0 **Junction capacitance at zero reverse voltage**

The junction capacitance C of a diode is measured as a function of the reverse bias voltage V. The junction capacitance parameters are then extracted from:

$$C = \frac{CJ0}{(1 + \frac{V}{PB0})^{MJ0}}$$

Parameter	Description
V	diode reverse voltage
CJ0	junction capacitance at zero reverse voltage
MJ0	grading coefficient
PB0	junction potential

CJA **Area Junction capacitance**

The junction capacitances C of diodes with different area to perimeter ratios are measured as a function of the reverse bias voltage V. The junction capacitance parameters are then extracted from:

$$C = \frac{W \cdot L \cdot CJA}{(1 + \frac{V}{PBA})^{MJA}} + \frac{2 \cdot (W + L) \cdot CJP}{(1 + \frac{V}{PBP})^{MJP}}$$

Parameter	Description
W	diode width
L	diode length
V	diode reverse voltage
PBA	area junction potential
PBP	sidewall junction potential
CJA	area capacitance
CJP	sidewall capacitance
MJA	area grading coefficient
MJP	sidewall grading coefficient

Note for CJA_DAPDA01, CJA_DAPDA1

The capacitance C of diodes with different area to perimeter ratios are measured at specific bias voltage, not as a function of bias voltage. The junction capacitance parameters are then extracted from:

$$C = W \cdot L \cdot CJA + 2 \cdot (W + L) \cdot CJP$$

CJP **Perimeter junction capacitance**

The junction capacitances C of diodes with different area to perimeter ratios are measured as a function of the reverse bias voltage V. The junction capacitance parameters are then extracted from:

$$C = \frac{W \cdot L \cdot CJA}{(1 + \frac{V}{PBA})^{MJA}} + \frac{2 \cdot (W + L) \cdot CJP}{(1 + \frac{V}{PBP})^{MJP}}$$

Parameter	Description
W	diode width
L	diode length
V	diode reverse voltage
PBA	area junction potential
PBP	sidewall junction potential
CJA	area capacitance
CJP	sidewall capacitance
MJA	area grading coefficient
MJP	sidewall grading coefficient

Note for CJP_DAPDA01, CJP_DAPDA1

The capacitance C of diodes with different area to perimeter ratios are measured at specific bias voltage, not as a function of bias voltage. The junction capacitance parameters are then extracted from:

$$C = W \cdot L \cdot CJA + 2 \cdot (W + L) \cdot CJP$$

CJX **Extrapolated junction capacitance**

The extrapolated junction capacitance is extracted from the capacitance model at the specified reverse bias of Vexcess above the breakdown voltage.

CNV **Varactor capacitance at negative voltage**

The specified terminal voltage is applied and the corresponding capacitance value C is measured at the specified frequency.

CPA **Parasitic area capacitance**

The dielectric, polysilicon and metal thicknesses are measured. The thickness values are then used by EDA field solver tools to calculate the capacitance of a large area capacitor.

CPP **Parasitic perimeter capacitance**

The fringing capacitance per length (one edge) of a single minimum width interconnect line is calculated using EDA field solver tools. Adjacent structures reduce this value.

CPV **Varactor capacitance at positive voltage**

The specified terminal voltage is applied and the corresponding capacitance value C is measured at the specified frequency.

DCR **Dark count rate**

The dark count rate is the number of induced avalanches by e.g thermal carriers. It is measured at the specified reverse bias of Vexcess above the breakdown voltage.

DLT **transistor delta length**

The delta length is used for the calculation of effective length, according to the measurement principle for effective transistor channel length (refer to the note for LEF)

DWR **resistor delta width**

The delta width is used in the calculation of the resistor mismatch pelgrom coefficient. It is determined according to the measurement principle for effective width (refer to the note for WER)

DWT **transistor delta width**

The delta width is used for the calculation of effective width, according to the measurement principle for effective transistor channel width (refer to the note for WEF)

EPS **Epsilon**

The dielectric constant ϵ for a material is taken from published values. For dielectrics made from a stack of composite materials, the value is estimated based on the values of ϵ for the individual materials and their relative thickness in the stack.

EVF **Early voltage forward**

The emitter (and substrate, if applicable) are connected to 0V. The specified current IB is forced in to the base. The collector voltage VC is swept and the current IC is measured, in order to find the minimum slope of the collector current as a function of the collector voltage. A tangent is taken from this slope. The early voltage is measured as the abscissa at the x-axis intercept of this tangent.

FC_ **corner frequency**

The corner frequency is the frequency at which the flicker noise density equals the thermal noise density. The operating point is taken at the specified drain voltage while the gate is forced to achieve the specified drain current. Source and body are connected to ground.

GAM **Gamma**

The threshold voltages VTX as a function of substrate bias voltage are extracted as described in the corresponding measurement note for VTX. The body factor GAMMA is then extracted from the slope of VT as a function of $\sqrt{(}2 \cdot PHI - VBS)$ by linear regression:

$$VTX = VT + GAMMA \cdot \left(\sqrt{2 \cdot PHI - VBS} - \sqrt{2 \cdot PHI}\right)$$

The effective bulk doping concentration NSUB is calculated from GAMMA and COX (refer to measurement note regarding Oxide capacitance / Oxide thickness):

$$GAMMA = \frac{\sqrt{2 \cdot \epsilon_0 \cdot \epsilon_{Si} \cdot q \cdot NSUB}}{COX}$$

The Fermi potential PHI is a function of the doping concentration NSUB and the intrinsic carrier concentration NI

$$PHI = \frac{kT}{q} \cdot \ln \frac{NSUB}{NI}$$

PHI is recalculated using the extracted value of NSUB. This updated value of PHI is then used again in the extraction of GAMMA and NSUB in an iterative procedure.

GA_ **Body factor**

The threshold voltages VTX as a function of substrate bias voltage are extracted as described in the corresponding measurement note for VTX. The body factor GAMMA is then extracted from the slope of VT as a function of $\sqrt{2 \cdot PHI - VBS}$ by linear regression:

$$VTX = VT + GAMMA \cdot \left(\sqrt{2 \cdot PHI - VBS} - \sqrt{2 \cdot PHI}\right)$$

The effective bulk doping concentration NSUB is calculated from GAMMA and COX (refer to measurement note regarding Oxide capacitance / Oxide thickness):

$$GAMMA = \frac{\sqrt{2 \cdot \epsilon_0 \cdot \epsilon_{Si} \cdot q \cdot NSUB}}{COX}$$

The Fermi potential PHI is a function of the doping concentration NSUB and the intrinsic carrier concentration NI

$$PHI = \frac{kT}{q} \cdot \ln \frac{NSUB}{NI}$$

PHI is recalculated using the extracted value of NSUB. This updated value of PHI is then used again in the extraction of GAMMA and NSUB in an iterative procedure.

HFH **Forward gain; high current**

Base and collector are connected to 0V. The specified emitter current is forced. This is normally at a point above the current used to achieve the maximum gain. Base and collector current are measured. The gain HF is calculated as IC/IB.

HFM **Maximum forward current gain**

The base current IB and the collector current IC are measured as a function of the base-emitter voltage VBE (Gummel plot). The current gain values BETA = IC/IB are calculated. The maximum current gain of this function is defined as HFM.

Note for HFMPA, HFMPA3, HFMPB, HFMPB3, HFMPC, HFMPC3

Special measurement conditions for PNP bipolar transistors: Base and collector are connected to 0V. The specified current Ie is forced into the emitter. The current Ib is measured at the base. The current gain values BETA = -Ie/Ib - 1 .

HF_ **Forward current gain**

Base and collector are connected to 0V. The specific emitter current is forced. Base and collector current are measured. The gain HF is calculated as IC/IB.

ID0 **Saturation current**

The gate is set to 0V and drain are forced to the specified voltage. Source and bulk are connected to ground. The transistor saturation current IDS is measured at the drain. ID0 is specified per drawn transistor width.

IDF **Forward current**

The forward current is measured at the specified forward voltage

IDS **Saturation current**

The gate and drain are forced to the specified voltages. Source and bulk are connected to ground. The transistor saturation current IDS is measured at the drain. IDS is specified per drawn transistor width.

IEB **Current**

Base and collector are connected to ground. The emitter is set to the specified voltage and the current IEB is measured.

ILA **Diode Area Leakage Current**

The specified reverse voltage is applied at the specified temperature. The diode leakage current IS is measured for diodes with different area to perimeter ratios. The leakage current per drawn area ILA and the leakage current per drawn perimeter ILP are then calculated from

$$IS = ILA \cdot W \cdot L + ILP(2 \cdot W + 2 \cdot L)$$

The values may not be applicable to junction diodes as part of other devices (e.g. MOS).

ILP **Diode Perimeter Leakage Current**

The specified reverse voltage is applied at the specified temperature. The diode leakage current IS is measured for diodes with different area to perimeter ratios. The leakage current per drawn area ILA and the leakage current per drawn perimeter ILP are then calculated from

$$IS = ILA \cdot W \cdot L + ILP(2 \cdot W + 2 \cdot L)$$

The values may not be applicable to junction diodes as part of other devices (e.g. MOS).

IL_ **Leakage current**

The specified voltage VL is applied to high terminal(s), 0V is applied to low terminal(s). The leakage current between high and low terminal(s) is measured.

IOF **Off current**

A given voltage is applied to drain, all other transistor terminals are on ground. The drain leakage current is measured as IOF. IOF is normally specified per drawn transistor width

ISB **Bulk current**

A specified drain voltage is applied to the drain, the gate voltage is swept from Vlow to Vhigh within the allowed operating range in order to find the maximum bulk current ISB. ISB is specified per drawn transistor width.

KP_ **Gain factor (beta)**

The gain factor is measured along with the threshold voltage. The maximum slope referred in VTX measuring principle is the transconductance. This figure is divided by the applied drain voltage to calculate the gain factor.

LEF **Effective transistor channel length**

The effective gain factor KP' = KP · Weff / Leff is measured for a L - array of wide transistors according to threshold voltage measurement (refer to notes for VTX and KP_). The length reduction DL = L - Leff is calculated from the x-intercept of the linear regression:

$$\frac{1}{KP'} = \frac{1}{KP \cdot Weff} \cdot (L - DL)$$

MJ0 **Grading coefficient**

The junction capacitance C of a diode is measured as a function of the reverse bias voltage V. The junction capacitance parameters are then extracted from:

$$C = \frac{CJ0}{(1 + \frac{V}{PB0})^{MJ0}}$$

Parameter	Description
V	diode reverse voltage
CJ0	junction capacitance at zero reverse voltage
MJ0	grading coefficient
PB0	junction potential

MJA **Area grading coefficient**

The junction capacitances C of diodes with different area to perimeter ratios are measured as a function of the reverse bias voltage V. The junction capacitance parameters are then extracted from:

$$C = \frac{W \cdot L \cdot CJA}{(1 + \frac{V}{PBA})^{MJA}} + \frac{2 \cdot (W + L) \cdot CJP}{(1 + \frac{V}{PBP})^{MJP}}$$

Parameter	Description
W	diode width
L	diode length
V	diode reverse voltage
PBA	area junction potential
PBP	sidewall junction potential
CJA	area capacitance
CJP	sidewall capacitance
MJA	area grading coefficient
MJP	sidewall grading coefficient

MJP **Sidewall grading coefficient**

The junction capacitances C of diodes with different area to perimeter ratios are measured as a function of the reverse bias voltage V. The junction capacitance parameters are then extracted from:

$$C = \frac{W \cdot L \cdot CJA}{(1 + \frac{V}{PBA})^{MJA}} + \frac{2 \cdot (W + L) \cdot CJP}{(1 + \frac{V}{PBP})^{MJP}}$$

Parameter	Description
W	diode width
L	diode length
V	diode reverse voltage
PBA	area junction potential
PBP	sidewall junction potential
CJA	area capacitance
CJP	sidewall capacitance
MJA	area grading coefficient
MJP	sidewall grading coefficient

NOI **input referred noise**

The input gate referred 1/f noise spectral density at the specified frequency is quoted, normalised to a specified active gate area. The operating point is taken at the specified drain voltage while the gate voltage is forced to achieve the specified drain current. Source and body are connected to ground.

ORP **Optical Responsivity**

The specified reverse voltage is applied to the device. A light point having the defined wavelength is positioned in the centre of the optical active area. The light power P_{light} and the resulting photo current I_{photo} of the photodiode are measured. The optical responsivity is calculated as: $ORP = I_{photo}/P_{light}$

OTB **Hall sensor offset voltage**

The static sensor offset is defined as the voltage difference between the left and right terminals when forcing sub = 0V, bottom = 0V and the specified top voltage

PB0 **Junction potential**

The junction capacitance C of a diode is measured as a function of the reverse bias voltage V. The junction capacitance parameters are then extracted from:

$$C = \frac{CJ0}{(1 + \frac{V}{PB0})^{MJ0}}$$

Parameter	Description
V	diode reverse voltage
CJ0	junction capacitance at zero reverse voltage
MJ0	grading coefficient
PB0	junction potential

PBA **Area junction potential**

The junction capacitances C of diodes with different area to perimeter ratios are measured as a function of the reverse bias voltage V. The junction capacitance parameters are then extracted from:

$$C = \frac{W \cdot L \cdot CJA}{(1 + \frac{V}{PBA})^{MJA}} + \frac{2 \cdot (W + L) \cdot CJP}{(1 + \frac{V}{PBP})^{MJP}}$$

Parameter	Description
W	diode width
L	diode length
V	diode reverse voltage
PBA	area junction potential
PBP	sidewall junction potential
CJA	area capacitance
CJP	sidewall capacitance
MJA	area grading coefficient
MJP	sidewall grading coefficient

PBP **Perimeter junction potential**

The junction capacitances C of diodes with different area to perimeter ratios are measured as a function of the reverse bias voltage V. The junction capacitance parameters are then extracted from:

$$C = \frac{W \cdot L \cdot CJA}{(1 + \frac{V}{PBA})^{MJA}} + \frac{2 \cdot (W + L) \cdot CJP}{(1 + \frac{V}{PBP})^{MJP}}$$

Parameter	Description
W	diode width
L	diode length
V	diode reverse voltage
PBA	area junction potential
PBP	sidewall junction potential
CJA	area capacitance
CJP	sidewall capacitance
MJA	area grading coefficient
MJP	sidewall grading coefficient

PDP **Photon detection probability**

Photon detection probability is the probability that a photon triggers an avalanche at a specified wavelength. It is measured at the specified reverse bias of Vexcess above the breakdown voltage.

QF_ **Quality factor**
The quality factor is extracted from S-parameter measurements at the specified frequency. Refer to the corresponding model file for the used equivalent circuit.

RCT **Contact resistance**
The contact resistance is calculated from the resistance of a contact string divided by the number of contacts. For non-metal layers, except those which are silicided, the resistance between contacts is considered.

ROA **On resistance**
The area specific on resistance ROA is calculated as RO_, RON or ROC multiplied by the minimum pitch for the device.

RO_ **On resistance**
A drain current is measured at the specified gate and drain voltages. The source and substrate are grounded. RO_ is calculated by the drain voltage divided by the drain current and multiplied by the transistor width.

RP_ **Programmed fuse resistance**
A specified voltage is applied to the device. The fuse current is measured and the fuse resistance is calculated. The programming of poly fuse is performed according to the specified fusing conditions.

RSE **Edge resistance**
Connection from the silicided end region to the resistor body has a finite value. This is referred to as the SB edge resistance because it follows the line of the SB edge between the silicided and unsilicided resistor regions. The edge resistance varies inversely with resistor width. It arises from the contact resistance of the silicide to the doped silicon of the resistor body.

RSR **Sheet resistance**
A voltage VRES is applied to one terminal. The second terminal is connected to ground. In case of diffusion or well resistor measurements substrate or well is also connected to ground. The current IRES is measured at the first terminal. The measurements are performed for at least two widths W of long resistors (Leff ~ L). The sheet resistance per square R is calculated from the slope and the width reduction DW = W - Weff is calculated from the x-intercept of the linear regression:

$$\frac{IRES}{VRES} = \frac{1}{R \cdot L} \cdot (W - DW)$$

For metal sheet resistance, four terminal measurement structures are used.

RSS **Sheet resistance**
A voltage VRES is applied to one terminal. The second terminal is connected to ground. In case of diffusion or well resistor measurements substrate or well is also connected to ground. The current IRES is measured at the first terminal. RSS is calculated from number of drawn resistor squares.

RSW **Start wafer resistivity**
The resistivity of the start wafer material is taken from the wafer vendor specification

RTB **Hall sensor resistance**
The Hall sensor resistance is measured at the specified bias voltage.

RU_ **Unprogrammed fuse resistance**
A specified current is forced into the device. The fuse voltage is measured and the fuse resistance is calculated.

RVI **Via resistance**
The via resistance is calculated from the resistance of a long via string divided by the number of vias.

SC_ **standard deviation for capacitance mismatch**
The standard deviation of the capacitance mismatch is calculated using common statistical theory by assuming a normal distribution of the relative capacitance mismatch values of identically designed capacitor pairs.

SEN **Sensor sensitivity**
The Hall sensor sensitivity in units of [V / (A * T)] is determined at T = 27°C and at the specified sensor supply current

SIB **Standard deviation for bipolar transistor base current mismatch**

The standard deviation of the bipolar transistor base current mismatch is calculated using common statistical theory by assuming a normal distribution of the relative base current mismatch values of identically designed bipolar transistor pairs.

SIC **Standard deviation for bipolar transistor collector current mismatch**

The standard deviation of the bipolar transistor collector current mismatch is calculated using common statistical theory by assuming a normal distribution of the relative collector current mismatch values of identically designed bipolar transistor pairs.

STS **Sub-threshold slope**

The gate voltage is swept with the drain held at given drain voltage and the source and substrate grounded. STS is the maximum slope of the log10(Id/w) versus Vg plot.

SVB **Standard deviation for bipolar transistor base emitter voltage mismatch**

The standard deviation of the bipolar base emitter voltage mismatch is calculated using common statistical theory by assuming a normal distribution of the absolute base emitter voltage mismatch values of identically designed bipolar transistor pairs.

TC1 **Linear temperature coefficient**

Variable x is measured as a function of the temperature T. The temperature dependence is modelled using the following formula:

$$x = x_0(T_{nom})\left[1 + TC1(T - T_{nom}) + TC2(T - T_{nom})^2\right]$$

xo(Tnom) is the room temperature value for x
TC1 and TC2 are the polynomial temperature coefficients

TC2 **Quadratic temperature coefficient**

Variable x is measured as a function of the temperature T. The temperature dependence is modelled using the following formula:

$$x = x_0(T_{nom})\left[1 + TC1(T - T_{nom}) + TC2(T - T_{nom})^2\right]$$

xo(Tnom) is the room temperature value for x
TC1 and TC2 are the polynomial temperature coefficients

TCC **Capacitor temperature coefficient**

The capacitance is measured as a function of temperature T. The temperature coefficient of the capacitance TCC is calculated from the slope of the following linear regression:

$$\frac{C(T)}{C(To)} = 1 + TCC \cdot (T - To)$$

C(To) is the room temperature capacitance value

TC_ **Temperature coefficient**

Variable x is measured as a function of the temperature T. The temperature coefficient TC of the variable x is calculated from the slope of the linear regression:

$$x(T) = x_0(T_{nom}) + TC(T - T_{nom})$$

xo(Tnom) is the room temperature value for x
TC is the linear temperature coefficient

THD **Dielectric thickness**

Thickness may be measured either on large area test structures within the wafer fabrication process, or may be determined electrically from capacitance measurements. The parameter values describe thicknesses of fully prepared wafers. For some parameters, the monitoring of these thicknesses is performed by separate monitoring of all separate layers which generate the final layer. For electrical measurements, the capacitance CAA of a large area capacitor is measured. The dielectric thickness THD is then calculated from:

$$THD = \frac{\epsilon 0 \cdot \epsilon r}{CAA}$$

THG **Gate oxide thickness**

The capacitance per area COX of a large area capacitor is measured. The oxide thickness TOX is calculated from:
(with $\epsilon ox = 3.9$)

$$TOX = \frac{\epsilon 0 \cdot \epsilon ox}{COX}$$

THV **Passivation Thickness**

Thickness is measured on large area test structures within the wafer fabrication process. The parameter values describe thicknesses of fully prepared wafers. For some parameters, the monitoring of these thicknesses is performed by separate monitoring of all separate layers which generate the final layer.

TH_ **Thickness**

Measurements may performed either within the wafer fabrication process, or from cross-sections after fabrication. The parameter values describe the thickness of fully prepared wafers. For some parameters, the values come from the wafer supplier specification.

TS1 **Linear Temperature coefficient of sensitivity**

The sensor sensitivity SEN is measured as a function of the temperature T. The linear and quadratic temperature coefficients of the sensitivity TS1 and TS2 are calculated using a quadratic regression:

$$\frac{SEN(T)}{SEN(T0)} = 1 + TS1 \cdot (T - T0) + TS2 \cdot (T - T0)^2$$

TS1 is the linear and TS2 is the quadratic temperature coefficient.

TS2 **Quadratic Temperature coefficient of sensitivity**

The sensor sensitivity SEN is measured as a function of the temperature T. The linear and quadratic temperature coefficients of the sensitivity TS1 and TS2 are calculated using a quadratic regression:

$$\frac{SEN(T)}{SEN(T0)} = 1 + TS1 \cdot (T - T0) + TS2 \cdot (T - T0)^2$$

TS1 is the linear and TS2 is the quadratic temperature coefficient.

TUR **Tuning range**

The tuning range is the difference between the capacitance values at the specified voltages, expressed as a percentage.

U0_ **Effective mobility**

The mobility U0_ is calculated from gain KP_ and gate oxide capacitance CGA:

$$U0 = \frac{KP}{CGA}$$

VBE **Base-emitter voltage**

The base, collector (and substrate, if applicable) are connected to 0V. The specified emitter current is forced into the emitter and the base-emitter voltage VBE is measured. For devices which have a gate connection, the specified voltage is applied to the gate. In some cases, an alternate method may be used; refer to device specific measurement notes.

Note for VBENVA, VBENVB, VBENVC

Special measrement conditions for NPN bipolar transistor: Collector is connected to the specified voltage and Emitter is connected to 0V. The specified current IB is forced into the Base.

VC1 **Linear voltage coefficient for capacitor**

The capacitance C is measured as a function of the voltage V. The voltage dependence of a capacitor (V in volts, $V_{nom} = 0V$) is modeled using the following formula:

$$C = C0(1 + VC1(V - V_{nom}) + VC2(V - V_{nom})^2)$$

C0 is the capacitance at $V = V_{nom}$ VC1 and VC2 are polynomial modeling coefficients.

VC2 **Quadratic voltage coefficient for capacitor**

The capacitance C is measured as a function of the voltage V. The voltage dependence of a capacitor (V in volts, $V_{nom} = 0V$) is modeled using the following formula:

$$C = C0(1 + VC1(V - V_{nom}) + VC2(V - V_{nom})^2)$$

C0 is the capacitance at $V = V_{nom}$ VC1 and VC2 are polynomial modeling coefficients.

VCB **Bulk voltage coeffcient for resistor**

The substrate or bulk voltage coefficient of a poly resistor is measured by applying bias voltage on to the bulk substrate, noted as node voltage v(3). The resistor terminal voltages are noted as v(1) and v(2) respectively. The slope for the voltage coefficient VCB of the sheet resistance is then calculated by linear regression method using a definition equation for the resistance:

$$R = R_0 \left[1 + VCB \frac{V_{(1,3)} + V_{2,3)}}{2} \right]$$

VDF **Forward voltage**

A specified current is forced through the diode and the forward voltage is measured.

VR_ **Reverse voltage**

For the reverse voltage, a specified current of is forced and the reverse voltage measured (this is not the diode breakdown).

VT1 **Snap-back trigger voltage**

Source and bulk are connected to ground. A static gate voltage VGS is applied at the gate. The output characteristic is measured by applying 100ns current pulses at the drain. At certain drain voltage the parasitic bipolar triggers, leading to device damage. This drain voltage defines the snap-back trigger voltage (or on-state breakdown voltage) VT1 at this particular gate bias.

VTF **Field threshold voltage**

Drain is set to specified voltage. Source and bulk are connected to ground. The voltage at gate is swept until the current reaches a specified current density at the threshold voltage VTF.

VTI **Turn-on voltage**

The constant-current turn on voltage with zero substrate bias is measured as follows: The drain voltage is forced to VD, source and bulk are connected to ground. The gate voltage is swept until the drain current reaches Id at the threshold voltage VTI.

Note for VTINE3IL, VTINE3IS, VTINE3ISS, VTINE3L, VTINE3LNAL, VTINE3LNAS, VTINE3LNASS, VTINE3S, VTINE3SS, VTINEDI, VTINEDIA, VTINEIL, VTINEIS, VTINEISS, VTINEL, VTINELIL, VTINELIS, VTINELISS, VTINELL, VTINELNAIL, VTINELNAIS, VTINELNAISS, VTINELNAL, VTINELNAS, VTINELNASS, VTINELS, VTINELSS, VTINES, VTINESS, VTINESVTIL, VTINESVTIS, VTINESVTL, VTINESVTS, VTINHHVL, VTINHVL, VTINMMAL, VTINMMCL, VTIPE3IL, VTIPE3IS, VTIPE3ISS, VTIPE3L, VTIPE3LNAL, VTIPE3LNAS, VTIPE3LNASS, VTIPE3LNIL, VTIPE3LNIS, VTIPE3LNISS, VTIPE3LNL, VTIPE3LNS, VTIPE3LNSS, VTIPE3S, VTIPE3SS, VTIPED, VTIPED2, VTIPEIL, VTIPEIS, VTIPEISS, VTIPEL, VTIPELIL, VTIPELIS, VTIPELISS, VTIPELL, VTIPELS, VTIPELSS, VTIPES, VTIPESS, VTIPESVTIL, VTIPESVTIS, VTIPESVTISS, VTIPESVTL, VTIPESVTS, VTIPESVTSS, VTIPHHVL, VTIPHVL, VTIPMMAL, VTIPMMCL

The specific drain current Id is 0.1µA multiplied by (W/L).

VTX **Extrapolated threshold voltage**

The linearly extrapolated threshold voltage with zero substrate bias is measured as follows: The drain voltage is forced to VD, all other terminals are connected to ground if not otherwise specified. The gate voltage is swept to find the maximum slope of the drain current as a function of the gate voltage. The voltage sweep is positive for n-channel devices and negative for p-channel devices. The intercept with the x-axis minus half the drain voltage VD/2 is taken as VT, the threshold voltage.

$$Id = beta \cdot Vd \cdot (Vg - Vt - \frac{Vd}{2})$$

WEF **Effective transistor channel width**

The effective gain factor KP'=KP · Weff/Leff is measured for a W – array of long transistors according to threshold voltage measurement (refer to notes for VTX and KP_). The width reduction DW = W – Weff is calculated from the x-intercept of the linear regression:

$$KP' = \frac{KP}{Leff} \cdot (W - DW)$$

WER **Effective width**

A voltage VRES is applied to one terminal. The second terminal is connected to ground. In case of diffusion or well resistor measurements substrate or well is also connected to ground. The current IRES is measured at first terminal. The measurements are performed for at least two widths W of long resistors (Leff ~ L). The width reduction DW = W - Weff is calculated from the x-intercept of the linear regression:

$$\frac{IRES}{VRES} = \frac{1}{R \cdot Leff} \cdot (W - DW)$$

For metal sheet resistance, four terminal Van Der Pauw measurement structures are used.

XJ_ **Junction depth**

The junction depth is extracted from SIMS measurements. The measurements are performed on fully prepared wafers.

XT_ **Trench depth**

The trench depth is measured by SEM cross-sections.

4. Process related guidelines

4.1 Matching Introduction

General matching information

This section presents fundamental parameters for description of matching behavior of MOS and bipolar transistors, resistors and capacitors. All matching parameters are information parameters and represent typical values only.
The matching parameters describe the short distance matching: the matching of two identically designed elements located close to each other (maximum distance about 120µm).
The stochastic matching between two parameters P1 and P2 measured at two identically designed elements is defined as the standard deviation of the normal distribution for:

1) absolute differences for threshold voltages, base-emitter voltage

$$\Delta P = (P_1 - P_2) \qquad\qquad [mV]$$

2) relative differences for transistor currents, resistors, capacities

$$\frac{\Delta P}{P} = 200 \cdot \frac{P_1 - P_2}{P_1 + P_2} \qquad\qquad [\%]$$

We assume that ΔP_i values are distributed normally with a variance σ^2 (squared standard deviation). The estimator μ of the distribution mean is close to zero except in the case of strong process parameter gradients or layout related asymmetries.

Matching measurements are performed for MOS transistors, bipolar transistors, resistors and capacitors at a temperature of 27°C. The following model describes the dependence of parameter matching on two identically designed devices with area (W · L):

$$\sigma^2(P_1 - P_2) = \frac{A_p^2}{W \cdot L}$$

where Ap is the process-dependent matching parameter describing the area dependence.

Note: For the calculation of the transistor matching parameters Ap the effective channel lengths Leff and the effective channel widths Weff were used; for resistors the effective width Weff and the drawn length L were used.

Note: The parameter differences are essential for matching characterization, not the absolute values of a parameter. Therefore sequential measurements with the same meters and multiple measurements (5 times for VTO and gain, 10 times for R and ΔC) of each parameter for both elements were performed to obtain maximum accuracy.

Note: For the simulation of device matching a special set of statistical models may be offered (search for the term "GSA Spice Model Checklist" at my.xfab.com). The model parameters used for these statistical models may differ from their corresponding matching parameters because of special simulator requirements.

Note: Two devices with higher distance to each other will exhibit greater mismatch of parameters (long distance mismatch). It is also advisable to avoid the use of minimum length or width for improved matching.

Note: Please also refer to the document Design Guidelines for Improved Device Matching, available on "my X-FAB."

MOS Transistor Matching Parameters

MOS matching is characterized using Pelgrom coefficients (see M. J. Pelgrom et al, IEEE JSSC, vol SC-24 pp.1433-1439, October 1989) where the standard deviation of mismatch between adjacent MOSFETs is plotted versus the square root of the area (W * L). A line fit to the data passes through the origin with a slope which maybe characterized as the Pelgrom coefficient. For the calculation of the matching parameters the effective width (Weff) and length (Leff) of the transistors is used:

⇒

$$W_{eff} = W - \Delta W$$
$$L_{eff} = L - \Delta L$$

The threshold voltage matching and the linear region gain matching are described by:

$$\sigma(VTO) = \frac{AVTO}{\sqrt{W_{eff} \cdot L_{eff}}} \qquad \sigma\left(\frac{\Delta BETA}{BETA}\right) = \frac{ABETA}{\sqrt{W_{eff} \cdot L_{eff}}}$$

The drain current matching is described by:

$$\sigma\left(\frac{\Delta ID}{ID}\right) = \frac{AIDx}{\sqrt{W_{eff} \cdot L_{eff}}} \qquad with \quad x \quad for(VG - VTO)$$

The drain current mismatch strongly depends on the effective gate voltage: $(VG - VTO)$.

Bipolar Transistor Matching Parameters
The matching of base-emitter voltage VBE, collector current IC and base current IB is described.

Resistor Matching Parameters
The resistor matching is calculated using the effective width (Weff) of the resistors:

$$\sigma\left(\frac{\Delta R}{R}\right) = \frac{AR}{\sqrt{W_{eff} \cdot L}} \qquad with \quad W_{eff} = W - \Delta W$$

Note: Metal resistors are not recommended for matching applications.

Capacitor Matching Parameters

The capacitor matching is described by:

$$\sigma\left(\frac{\Delta C}{C}\right) = \frac{AC}{\sqrt{W \cdot L}}$$

4.2 Simulation Models

This section presents a summary of circuit simulation models for the available devices (see "Primitive Devices" list).
All model files, Application Notes, Checklists et cetera are available on https://my.xfab.com or within the actual model library.

For detailed information on supported circuit simulators, model classification, noise, matching, statistical variation and model-specific parameters such as junction temperature, please refer to the GSA SPICE Model Checklist and the related Device Characteristics Documentation (formerly known as Model Guides).

General guidelines how to setup the different simulation environments and on the simulation types itself can be found in Application Note SPICE Models and Simulations.

X-FAB simulation models are intended to be used with the analog circuit simulators Spectre, HSPICE, T-Spice and ELDO. They can also be used in other spice compatible simulation programs if the required compact models are supported.

The simulation models are valid in the junction temperature range -55°C ≤ Tj ≤ +185°C.

Parameter Extraction

High precision mixed analog and digital circuit simulation requires good parameter extraction strategies and accurate models. In general, the quality of a parameter extraction procedure depends on the selection of measured data (1), on the parameter extraction program (2) and on the simulation model (3).

1. The Input Data

We use measured current-voltage and conductance-voltage characteristics of a matrix of element geometries under all operating conditions. The geometries and the operating points are carefully selected in order to fulfill the requirements of typical mixed analog-digital design applications.

2. The Parameter Extraction Program

This program contains tools for extracting and optimizing the SPICE model parameters. The non-linear least-square-fit routine can optimize multiple devices with respect to multiple bias conditions in order to reduce the error between the simulated data and the measured data.

3. The Simulation Model MOS Transistor Model

Different types of MOS models are available for design:

1. LV NMOS & LV PMOS: 4-terminal subcircuits
2. LV NMOS variants: 6-terminal subcircuits | includes parasitic diodes
3. LV PMOS variants: 5-terminal subcircuits | includes parasitic diodes
4. HV NMOS: 4-terminal subcircuits | parasitic diodes or BJTs are modeled
5. HV PMOS: 4-terminal subcircuits | parasitic diodes are modeled
6. HV PMOS: 5-terminal subcircuits | parasitic BJTs are modeled

We supply models which represent the following process corners:

- **tm** = typical mean = model parameters have been extracted from typical wafers
- **wp** = worst case power = fast NMOS & fast PMOS
- **ws** = worst case speed = slow NMOS & slow PMOS
- **wo** = worst case one = fast NMOS & slow PMOS
- **wz** = worst case zero = slow NMOS & fast PMOS
- **mc_g** / **mc_u** = statistical models

Please note that parameters do not vary independently:
The circuit simulation parameters are extracted from the complete set of model equations in order to give the best fit of the entire characteristic for all operating points. The process control parameters are extracted from simplified model equations.
Hence, circuit simulation parameters may differ from their corresponding process control transistor parameters.

⇒

Bipolar Transistor Model

Two types of bipolar models are available for design:

1. vertical PNP: 3-terminal subcircuits
2. vertical NPN: 4-terminal subcircuits | includes parasitic PNP

We supply models which represent the following process corners:

- **tm** = typical mean = typical mean process condition
- **wp** = worst case power = high speed & high beta
- **ws** = worst case speed = low speed & low beta
- **mc_g** / **mc_u** = statistical models

The circuit simulation parameters are extracted from the complete set of model equations in order to give the best fit of the entire characteristic for all operating points. The process control parameters are extracted from simplified model equations.
Hence, the circuit simulation parameters BF and VAF may differ from their corresponding process control transistor parameters HF and EVF.

Resistor Model

Three types of resistor models are available for design:

1. polysilicon resistors: 3-terminal subcircuit with capacitors to the third node or 2-terminal subcircuit with capacitors to the global node 0
2. diffusion & well resistors: 3-terminal subcircuits with junction diodes to the 3rd node
3. metal resistors: 2-terminal subcircuits.

We supply models which represent the following process corners:

- **tm** = typical mean = typical mean process condition
- **wp** = worst case power = low resistance
- **ws** = worst case speed = high resistance
- **mc_g** / **mc_u** = statistical models

Capacitor Model

Two types of capacitor models are available for design:

1. sandwitch, MIM & fringe capacitor: 2-terminal subcircuit, parasitic metal capacitors are not part of the model. The ohmic resistances of the capacitor are not modelled.
2. POD capacitor: 3-terminal subcircuits with parasitic junction diode. The ohmic resistances of the capacitor are not modelled.
3. MOS varactor: 3-terminal & 4-terminal subcircuits with parasitic junction diodes. The ohmic resistances of the capacitor are modelled.

We supply models which represent the following process corners:

- **tm** = typical mean = typical mean process condition
- **wp** = worst case power = low capacitance
- **ws** = worst case speed = high capacitance
- **mc_g** / **mc_u** = statistical models

If voltage coefficients VC1 and VC2 of capacitors were measured to be less than 10e-6/V and 10e-7/V2 respectively, VC1 and VC2 are set to 0 in the device models.

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Diode Model

Four types of diode models are available for design:

1. junction diodes: 2-terminal subcircuits | operation in reverse direction is modeled
2. protection: 2-terminal subcircuits | breakdown region & operation in reverse direction is modeled
3. Schottky diodes: 3-terminal subcircuits | operation in forward & reverse direction is modeled
4. Polysilicon diode: 2-terminal subcircuit | operation in forward & reverse direction is modeled
5. photodiodes: subcircuits | optical behaviour modeled with Verilog-A

We supply models which represent the following process corners:

- **tm** = typical mean = typical mean process condition
- **wp** = worst case power = low capacitance
- **ws** = worst case speed = high capacitance
- **mc_g** / **mc_u** = statistical models

Common Notes on Corner Models and Corner Simulation Parameters

The typical mean parameters have been extracted from typical wafers.
Additionally worst case tolerances of the main parameters are given.
The default spread from typical mean parameters is +/- 3sigma, additionally +/-4sigma, +/-5sigma or +/-6sigma variation can be chosen.

Common Notes on Statistical Models

Statistical models are provided to support Monte Carlo simulation of process variation and device mismatch. These models are available for a subset of primitive devices.
For statistical models two model cases are defined:

- **mc_g** = gaussian distribution of process parameters, gaussian distribution of matching parameters
- **mc_u** = uniform distribution of process parameters, gaussian distribution of matching parameters