



X-FAB Semiconductor Foundries Haarbergstraße 67 D-99097 Erfurt Germany phone (++49) 361-427-6663 fax (++49) 361-427-6631

Application Note The SUBCUT option (splitting the substrate for LVS)

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General

In analog or mixed signal designs, there is sometimes a requirement to connect sections of the substrate to different wiring networks on the chip or to different PADs and package pins. Even though the substrate is common to the whole die, this 'split' is often used for noise reduction.

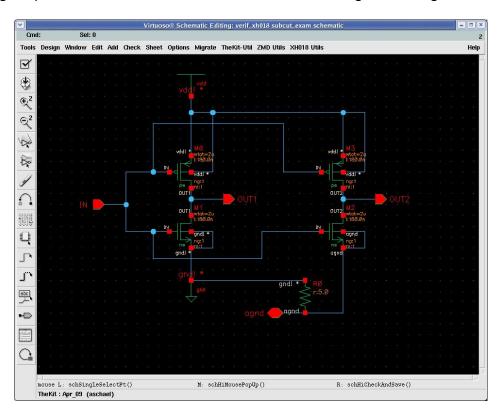
- The SUBCUT option is an LVS aid to check different low resistance (metal wiring) connections to the substrate. It can be used for:
 - Separate ground connections to PADS which have different net names
 - Separate ground connections for digital and analog blocks (GND and AGND) on the die.
- The SUBCUT option is supported in X-FAB technologies when it is described in the layer definitions section of the Design Rule Specification for that technology.
- Layout application:
 - It is necessary to place the layer SUBCUT (GDS 191) around the chosen block (area). The SUBCUT will 'split' the substrate area by a minimum design rule grid spacing
 - o Two Design Rules are included in DRC RunSets:
 - Q1SU "Check right using of the layer SUBCUT"
 - B1SU "DIFF or *WELL crossing SUBCUT edge is not allowed"
- Schematic application:
 - Place the device "s_res" between the 'split' ground nets
- LVS application:
 - The extraction will split the substrate (bulk) and will create a pseudo connection between the different ground nodes by using the "s_res" resistor
 - LVS will check these separated substrates and the use of the "s_res" device
- Simulation application:
 - Any current flow between the separated ground nets, resulting from different ground potentials, will be simulated by using the "s_res" resistance (resistance = 5 Ohm).
- Please note:
 - There is no real substrate isolation! Ground nets are connected through substrate on every die!
 - Do not use different ground potentials -> these will be not be checked in LVS!
 - s_res, even though coded as 5 Ohms, does not have a real substrate resistance!



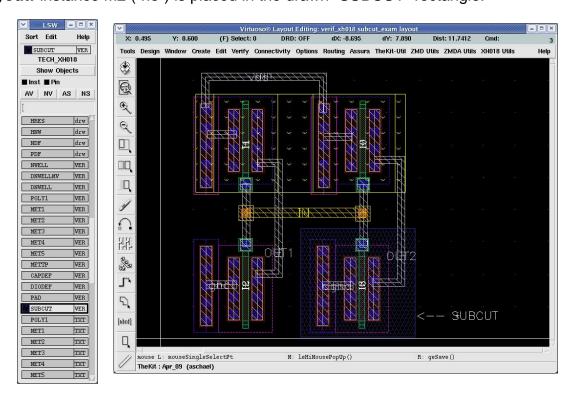
Example of SUBCUT use

The SUBCUT methodology can be applied in all supported design tools, including Cadence, Mentor, Synopsys and Tanner: this example uses Cadence.

Schematic: instance M1 has a bulk connection to *gnd!* and instance M2 is connected to *agnd*; please note instance M0 -> "s_res" between *gnd!* and *agnd*.

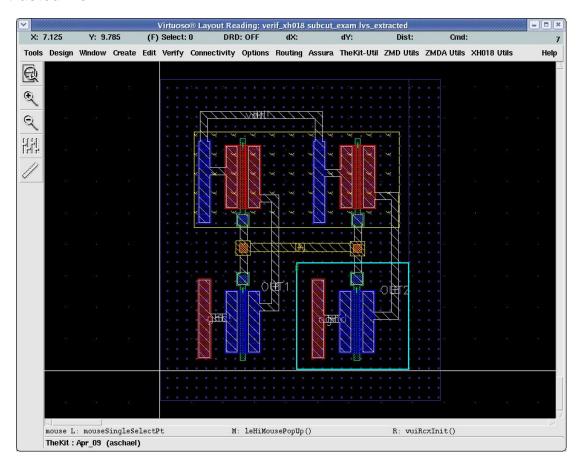


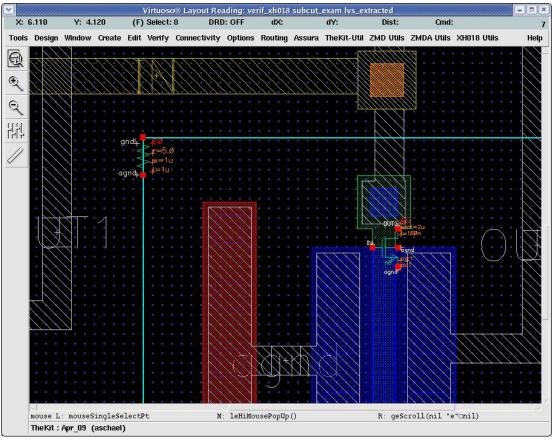
Layout: instance M2 ("ne") is placed in the drawn "SUBCUT" rectangle.





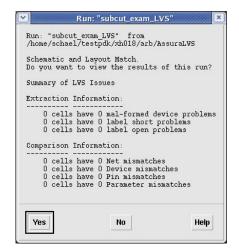
Extracted view:





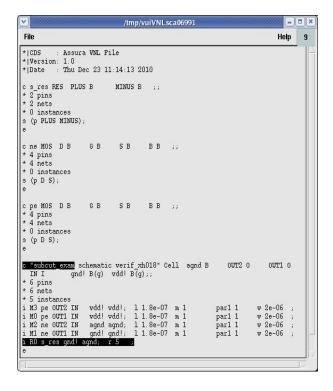


Assura LVS:



LVS schematic netlist

LVS layout netlist



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