Department of Electrical & Computer Engineering The University of Texas at Dallas

Application Specific Integrated Circuit Design

CE 6306

Final Report

Design of the Mini Stereo Digital Audio Processor (MSDAP)

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A Mini Stereo Digital Audio Processor (MSDAP)

Introduction

The Development of Digital Signal Processing chips and high-exactness oversampling Analog to Digital and Digital to Analog converters has led to the popularity of Digital Audio Signal processing. Low power and low-cost chips are always advantageous for any chips. Thus, aiming an improved performance and considering the cost-power ratios, DSP chips are developed.

The basic function for the MSDAP chip is that our mind is a programmable Finite Impulse Response (FIR) digital filter. Using this principle, 2 DSP chips each for the left and right ears were implemented using two-channel FIR digital filtering.

Comparing this MSDAP chip with general DSP chips, the cost and power dissipation of MSDAP was reduced by a factor of 5 to 10 times. In order to use MSDAP in portable systems, the power dissipation will fall on the level of 100mW.

Algorithm Description

MSDAP uses FIR digital filtering which involves linear convolution:

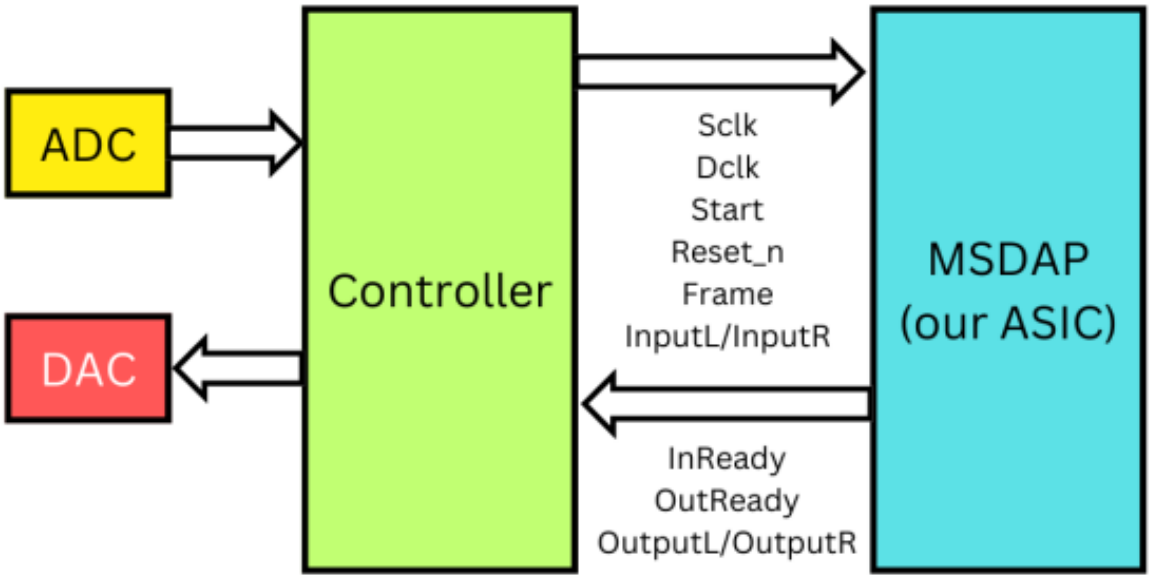
$$y(n) = \sum_{k=0}^{N} h(k) \times x(n-k)$$

where x(n) and y(n) are input and output audio sequences, and h(k) are filter coefficients with the filter order N. Thus, this equation involves N additions and N+1 multiplication.

Example of convolution

038	18C	00F	096	16A	130	110	013	14F	1F1	0FA	08E	1FC	1B0	13E	0CF
R1(0B)											R2(0F)				
0EE	021	1AF	04C	0A5	076	0EB	13E	0A8	055	17A	078	0B4	03D	0B7	1DD
R2(0F)										R3(0E)					
169	16C	1F3	0E1	0B2	14E	1D3	0F8	14D	1FF	170	**003**	04A	1B0	17E	115
R3(0E)								R4(0D)							
132	1F9	15D	024	104	1A3	1BC	007	01A	1E4	0C3	095	0AF	1F7	08C	1C6
R4(0D)					R5(08)								R6(0D)		
19C	0FC	00C	0FB	134	1E9	1AA	176	01C	075	0CC	14A	1B1	142	1B6	1B8
R6(0D)										R7(0D)					
1BB	09F	1FC	027	134	0D1	00F	189	130	199	04B	017	081	0E1	09D	10C
R7(0D)							R8(06)						R9(05)		
1F3	02B	1D3	09C	1D8	01D	0A6	02D	179	0AE	122	076	012	094	090	141
R9(05)		R10(06)						R11(04)			R12(06)				
13D	104	062	0C1	093	068	132	183	0B6	0DD	0BD	1FE	0DD	07C	0E6	105
R12(06)		R13(09)									R14(0B)				
1A2	0F1	00A	049	0AD	095	011	0E0	17C	1E3	1C2	0A7	1F8	12C	123	0C1
R14(0B)						R15(14)									
050	176	057	**103**	155	13F	1FD	1E7	159	047	018	13D	1E6	053	192	
R15(14)										R16(05)					

System Diagram



Input Pins

Sclk (Input)

System clock is running at a frequency of 26.88MHz. It gives the timing reference for the internal and control signals, as well as the output samples. Outputs InReady and OutReady are updated on the rising edge of Sclk.

Dclk (Input)

Data clock is running at a frequency of 768kHz. It gives the timing reference for the input samples.

Start (Input)

When Start is set low, the chip begins to initialize. Start may be asynchronous with Sclk or Dclk.

Reset_n (Input)

When Reset_n is set high, the chip begins to reset. Reset_n may be asynchronous with Sclk or Dclk.

in_dataL (Input)

in_dataL carries the left channel coefficients and audio samples in serial form. Bit 0 is the sign bit and is transmitted first. Bit 15 is the LSB and is transmitted last. in_dataL is read on the falling edge of Dclk.

in_dataR (Input)

in_dataR carries the right channel coefficients and audio samples in serial form. Bit 0 is the sign bit and is transmitted first. Bit 15 is the LSB and is transmitted last. in_dataR is read on the falling edge of Dclk.

Frame (Input)

Frame aligns the serial coefficients, input and output samples. Frame is set high for one Dclk cycle when the first bit of the input samples or coefficients is received, and then it is set low.

Output Pins

InReady (Output)

InReady is set high when the chip is ready to receive coefficients or input samples else it is set low. InReady is updated on the rising edge of Sclk.

OutReady (Output)

OutReady is set high when the chip is transmitting output samples else it is set low. OutReady is aligned with the rising edge of Frame.

out_dataL (Output)

out_dataL carries the left channel serial output samples. Bit 0 is the sign bit and is transmitted first. Bit 39 is the LSB and is transmitted last. out_dataL is updated on the rising edge of Sclk. The output frame starts with the rising edge of Frame and lasts for 40 Sclk cycles.

out_dataR (Output)

out_dataR carries the right channel serial output samples. Bit 0 is the sign bit and is transmitted first. Bit 39 is the LSB and is transmitted last. out_dataR is updated on the rising edge of Sclk. The output frame starts with the rising edge of Frame and lasts for 40 Sclk cycles.

Signal formats

The input signals sent to the chip are each of 16 bits and the output signals from the chip are 40 bits each.

Rj data samples

Both the left and right channel of rj has 16 bits. For each Dclk cycle, entire 16 bits of each channel is read.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSB															LSB

Coefficient data samples

Both the left and right channel of coefficient has 16 bits. For each Dclk cycle, entire 16 bits of each channel is read. 8^{th} bit is the sign bit where 0 means addition and 1 means subtraction. Rest of the bits from 7^{th} to 0^{th} bit becomes the k value in x(n-k).

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSB							Sign bit								LSB

Input data samples

Both the left and right channel of input has 16 bits. For each Dclk cycle, entire 16 bits of each channel is read. MSB is the sign bit.

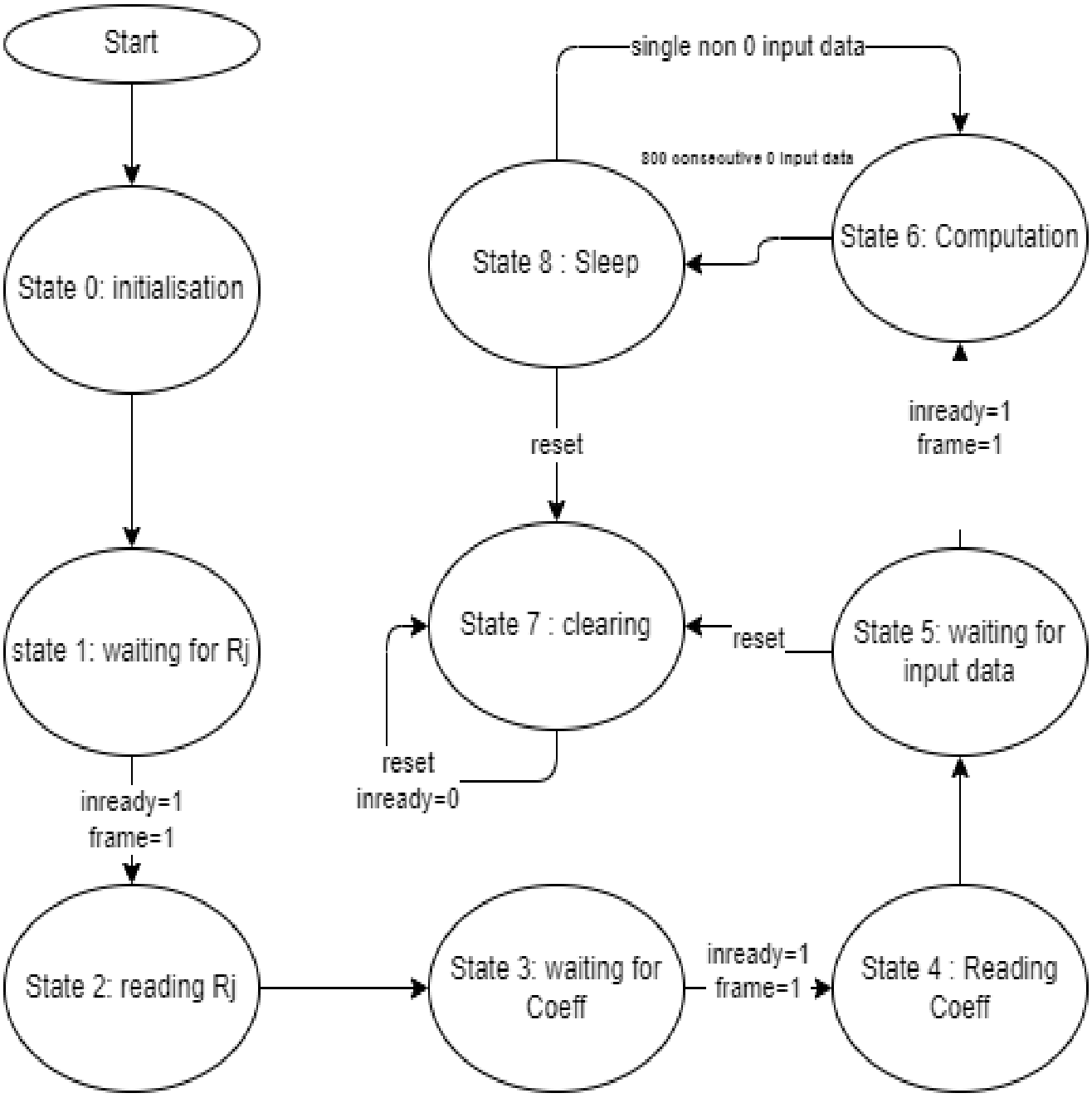
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSB Sign bit															LSB

Output data samples

The output is written bit by bit for every Sclk cycle as a 40-bit value from MSB to LSB. MSB is the sign bit.

39	38	37	36	…….	3	2	1	0
MSB Sign bit								LSB

Flow diagram



Finite State Machine:

Our Specifications: Parallel Input data, Serial Output data, Start is low, Reset is High and Frame is High.

State 0 (Initialization): When Start is low, the chip begins the initialization process, including clearing all the memories and registers. When the initialization process is completed, the chip enters State 1.

State 1 (Waiting to receive Rj): In this state, InReady is set high. If Frame is detected to be high, the chip enters State 2.

State 2 (Reading Rj): In this state, the chip reads the Rj values and InReady remains high. Once all Rj values have been loaded, the MSDAP enters State 3.

State 3 (Waiting to receive coefficients): In this state, InReady is set high. If Frame signal is detected to be high, the MSDAP enters State 4.

State 4 (Reading coefficients): In this state, the chip reads the coefficients. InReady remains high. Once all the coefficients have been loaded, the MSDAP enters State 5.

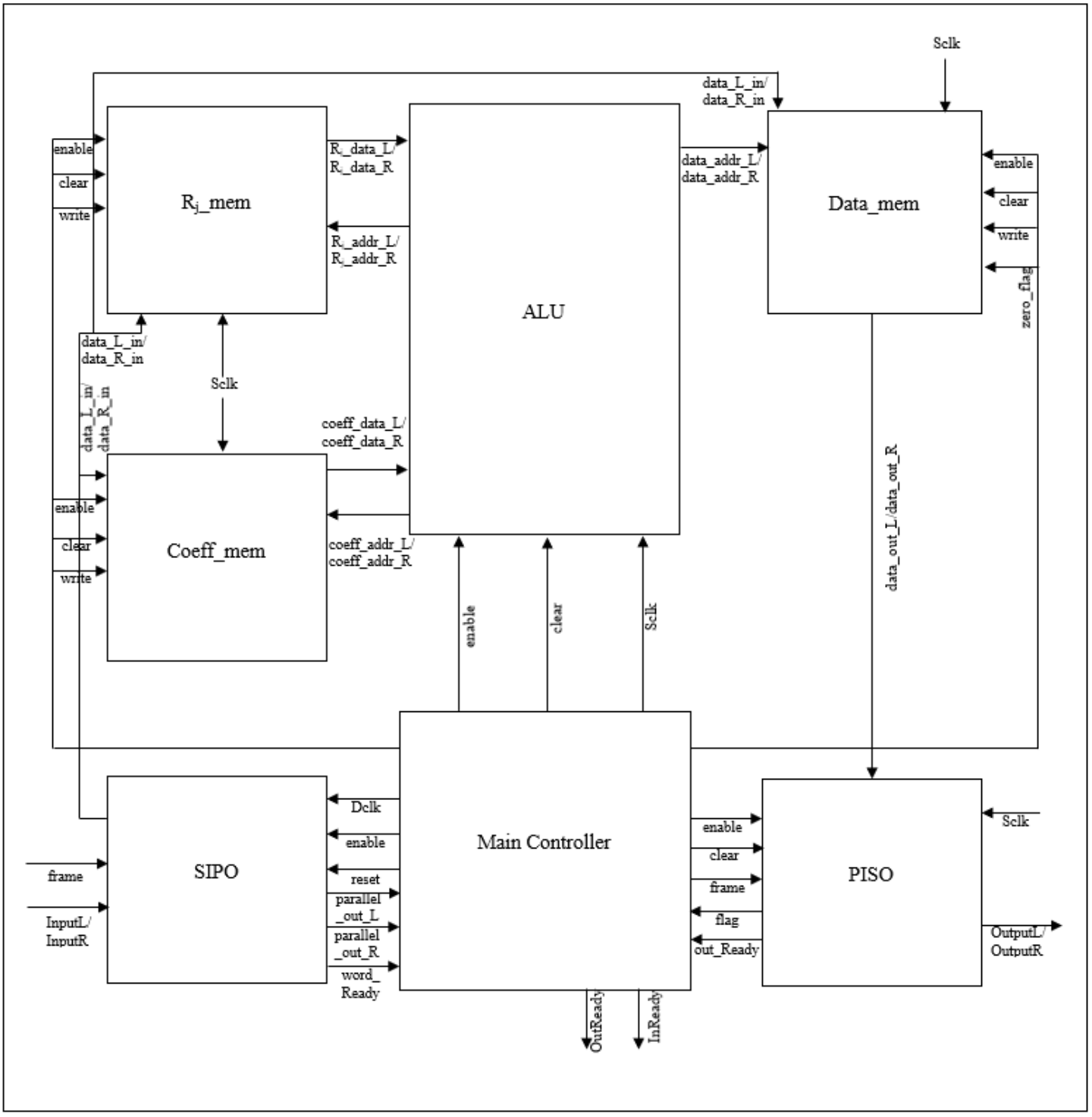
State 5 (Waiting to receive data): In this state, InReady is set high. If Frame is detected to be high, the chip enters State 6, or if Reset_n is detected to be high, the chip enters State 7.

State 6 (Working): In this state, the chip continually reads input samples, does the convolution computation, and sends out the computed output data; InReady remains high. If Reset_n is detected high, the chip enters State 7 or if the chip detects 800 consecutive inputs samples as zero, it enters State 8.

State 7 (Clearing): In this state, InReady is set low. All input and output samples in memories or registers except for Rj and coefficients are cleared to zero. If Reset_n is detected to be high again during this process, the chip will come back to the beginning of this process. The chip will go back to State 5 when completing the task of reset.

State 8 (Sleeping): In this state, the chip goes into sleeping mode while setting InReady high. If any non-zero input sample on either left or right channel is detected, the chip enters State 6. If Reset_n is detected high, the chip enters State 7.

MSDAP Architecture:



MSDAP has the following modules with their descriptions in the trailing MSDAP Specifications section:

1. Rj memory
2. Coefficient memory
3. Data memory
4. ALU
5. PISO
6. Controller
7. Top Module

MSDAP Specifications:

From the Architecture, we have the following the Modules: R_j Memory, Co-Efficient Memory, Serial to Parallel (S2P) Converter, Arithmetic Logic Unit (ALU) Controller, Main Controller, Data Memory, Sign Extender, Accumulator, Shifter and Parallel to Serial (S2P) Converter.

1. R_j Memory:

R_j Memory is used to store the Input R_j Values [Left and Right Channel], the memory is 16-Bit Wide and has 16 Locations. Triggered on rising edge of Sclk and we can direct the output depending on the request.

Signal	I/O	Description
data_L_in/data_R_in	Input	Input Data from S2P (Serial to Parallel) which is stored in the Memory.
Sclk	Input	System Clock. Used as Timing Reference to store values the values during the falling edge of the Clock.
enable	Input	When High – we can store the R_j values.
clear	Input	When High – Used to clear the Memory.
R_j_addr_L/R_j_addr_R	Input	4 Bit, addresses from R_j values are Read and ALU sends this.
write	Input	16 Bit, addresses for R_j values are written.
R_j_data_L/R_j_data_R	Output	16 Bit, Output id directed as per the request.

2. Co-Efficient (Coefficient) Memory [Coeff_mem]:

Co-Efficient Memory is used to store the Input Co-Efficient Values [Left and Right Channel], the memory is 16-Bit Wide and has 512 Locations. Triggered on rising edge of Sclk and we can direct the output depending on the request.

Signal	I/O	Description
data_L_in/data_R_in	Input	Input Data from S2P (Serial to Parallel) which is stored in the Memory.
Sclk	Input	System Clock. Used as Timing Reference to store values the values during the falling edge of the Clock.
enable	Input	When High – we can store the Co-Efficient values.
clear	Input	When High – Used to clear the Memory.
coeff_addr_L/coeff_addr_R	Input	9 Bit, addresses from Co-Efficient values are Read and ALU sends this.
write	Input	16 Bit, addresses for Co-Efficient values are written.
coeff_data_L/coeff_data_R	Output	16 Bit, Output id directed as per the request.

3. Serial to Parallel (S2P) Converter [SIPO]:

S2P is used to receive the Input data Serially [Left and Right Channel, called separately (one bit at a time)]. S2P receives input from both InputL and InputR and sends them to the Main Controller once all the bits are received. Triggered on the falling edge of Dclk. In_Ready, is used to indicate when the entire input is received and sent to Main Controller.

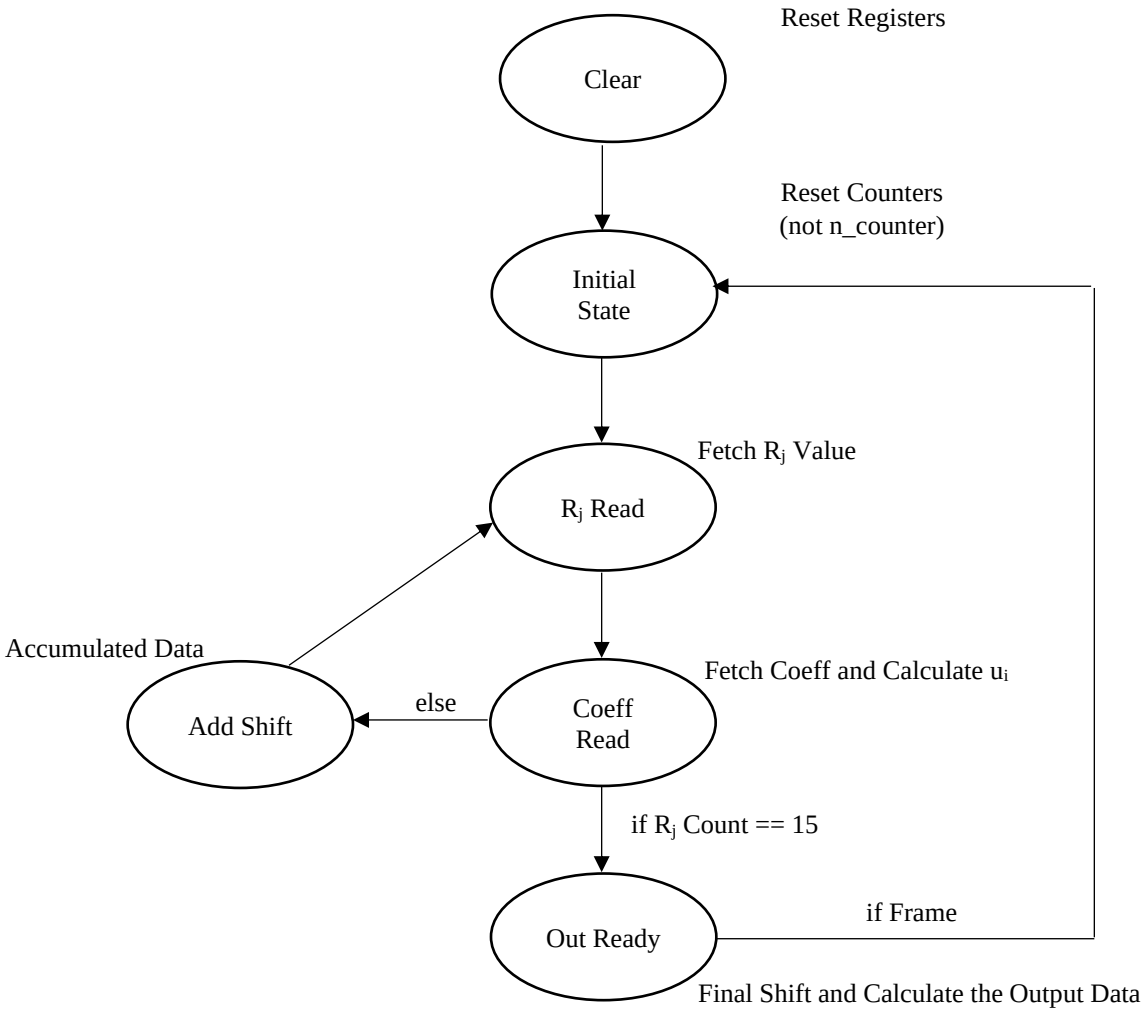
Signal	I/O	Description
InputL	Input	Left Channel – Serial Input (One Bit at a Time).
InputR	Input	Right Channel – Serial Input (One Bit at a Time).
Dclk	Input	Data Clock. Used as Timing Reference to receive the data serially during the falling edge of the Clock.
enable	Input	Indicates when it is ready to receive the data.
frame	Input	Used to enable word_Ready so it can start sending the data.
clear	Input	When High – Used to clear the Memory
parallel_out_L	Output	S2P Output Converter sent to Main Controller when all the bits in the Left Channel are received.
Parallel_out_R	Output	S2P Output Converter sent to Main Controller when all the bits in the Left Channel are received.
word_Ready	Output	Indicates when the whole data is received.

4. Arithmetic Logic Unit (ALU) [ALU]:

ALU is the Main Control Block used for the communications between the blocks in the MSDAP and responsible for sending the necessary signals to activate the functional blocks. The ALU has Finite State Machine (FSM), which is used to compute the output. We have implemented the Shifter, Accumulator and Sign Extension inside the ALU

Signal	I/O	Description
Sclk	Input	System Clock. Used as Timing Reference to perform the computations.
enable	Input	From Main Controller, used to enable the ALU.
memCount_flag	Input	Flag, used to set in accordance with the Main Controller.
coeff_L/coeff_R	Input	16 Bit, Co-Efficient values of Left and Right Channel.
R_j_L/R_j_R	Input	16 Bit, R_j values of Left and Right Channel.
coeff_value_L/coeff_value_R	Output	9 Bit, Addresses of Co-Efficient Data yet to be fetched from the Memory.
R_j_value_L/R_j_value_R	Output	4 Bit, Addresses of R_j Data yet to be fetched from the Memory.
data_mem_L/data_mem_R	Output	16 Bit, Contains Addresses and sent to Data Memory to get the Respective Data.
alu_out_ready	Output	Flag, used to send the values to Initial State when enabled.
PISO_enable	Output	Flag, used to send the values to PISO when enabled.

FSM for ALU:


Reset Registers
Clear
Reset Counters
(not n_counter)
Initial
State
Fetch R_j Value
R_j Read
Accumulated Data
Fetch Coeff and Calculate u_i
else
Add Shift
Coeff
Read
if R_j Count == 15
if Frame
Out Ready
Final Shift and Calculate the Output Data

5. Main Controller:

The Main Controller acts as Building Block where the all the operations is described with a Finite State Machine and responsible for communications between the Modules.

Signal	I/O	Description
Sclk	Input	System Clock. Timing reference for Control, Internal Signals and Output Samples. All operations using Sclk as reference will take place at the Rising Edge of the Clock. Generally, operates at frequency of 200 MHz.
Dclk	Input	Data Clock. Timing reference for Control, Internal Signals and Output Samples. All operations using Sclk as reference will take place at the Rising Edge of the Clock. Generally, operates at frequency of 768 kHz.
reset_n	Input	Used to reset the chip when it is Low and clears the chip till the chip received the Low input signal. It starts receiving Inputs once it is in High State.
start	Input	Used to initialize the Chip and clear the chip till the chip received the High input signal.
frame	Input	Used to align the co-efficients, input and output samples. The frame is set to high when the first bit of the above is received for one Dclk cycle.
InReady	Output	When the Chip is ready to receive the $R_{j,}$ Co-efficients and Input Data it is set to High or else set to Low when it is not Ready. Works on the Rising Edge of Sclk.
OutReady	Output	When the Chip sending the Outputs it is set to High or else set to Low when it is not sending the output. Works on the Rising Edge of frame.

6. Data Memory [Data_mem]:

Data Memory is used to store the Input Data Values [Left and Right Channel], the memory is 16-Bits and has 512 Locations. Data Memory replaces the memory from the 0^{th} position and a flag is set to check 800 consecutive zeros (Sleep State). The output is sent to the modules as required and works on the rising Edge of Sclk.

Signal	I/O	Description
Sclk	Input	System Clock. Used as Timing Reference to store values the values during the falling edge of the Clock.
enable	Input	The Data Memory stores the valye when it is High.
clear	Input	Used to clear the Data Memory when it is High.
write	Input	16-Bit, has the addresses to which the input can stored.
data_L_in/data_R_in	Input	It is the Output from the S2P and will be stored in the Data Memory.
zero_flag	Output	Flag is Set when 800 consecutive Zeors are detected.
data_out_L/data_out_R	Output	16-Bit, the sends to modules as required.

7. Parallel to Serial (P2S) Converter [PISO]:

P2S is used to send the Output data Serially [Left and Right Channel, called separately (one bit at a time)]. P2S receives input from both OutputL and OutputR and sends them to the Main Controller once all the bits are received. Triggered on the falling edge of Sclk. When the Frame is High, the output is written during the rising edge of Sclk. Enable is used to indicate when it is ready to send the Output.

Signal	I/O	Description
data_Out_L/data_Out_R	Input	40-Bit, Input from Data Memory.
Sclk	Input	System Clock. Used as Timing Reference to store values the values during the falling edge of the Clock.
enable	Input	Indicates when it is ready to write the output data.
clear	Input	Used to clear the variables.
frame	Input	Used to enable out_Ready so it can start sending the data.
data_out_L	Output	40-Bit, Output sent to Main Controller Left Channel on the falling edge of Sclk.
data_out_R	Output	40-Bit, Output sent to Main Controller Right Channel on the falling edge of Sclk.
flag	Output	Used to notify the output when it is completely written.
out_ready	Output	Used to indicate the Main Controller that the output is computed and can use data_out_L and data_out_R to write the Output data.

Verification of Design:

Timing Report:

```
Path 1: MET (16201 ps) Setup Check with Pin op_module/outputL_reg[20]/CLK->D
          View: PVT_0P63V_100C.setup_view
         Group: Sclk
    Startpoint: (R) msdap_main/enable_reg/CLK
         Clock: (R) Sclk
      Endpoint: (R) op_module/outputL_reg[20]/D
         Clock: (F) Sclk

                    Capture       Launch
       Clock Edge:+   16667            0
      Src Latency:+       0            0
      Net Latency:+       0 (I)        0 (I)
          Arrival:=   16667            0

            Setup:-       9
      Uncertainty:-     100
    Required Time:=   16558
     Launch Clock:-       0
        Data Path:-     357
            Slack:=   16201

#-------------------------------------------------------------------------------------------------------------------------
#        Timing Point         Flags    Arc    Edge          Cell             Fanout Load Trans Delay Arrival Instance
#                                                                              (fF)  (ps)  (ps)   (ps)  Location
#-------------------------------------------------------------------------------------------------------------------------
  msdap_main/enable_reg/CLK   -       -       R     (arrival)                  458    -     0     -       0    (-,-)
  msdap_main/enable_reg/QN    -       CLK->QN F     ASYNC_DFFHx1_ASAP7_75t_SL    4  2.8    39    54      54    (-,-)
  op_module/g345/Y            -       B->Y    R     NAND2xp5_ASAP7_75t_SL        1  0.8    25    17      72    (-,-)
  op_module/g342/Y            -       A->Y    R     OR2x2_ASAP7_75t_SL           79 52.8   268   134     205    (-,-)
  op_module/g341/Y            -       A->Y    F     INVx3_ASAP7_75t_SL           78 50.9   187   110     316    (-,-)
  op_module/g338/Y            -       A1->Y   R     AOI22xp5_ASAP7_75t_L         1  0.9    72    41      356    (-,-)
  op_module/outputL_reg[20]/D -       -       R     DFFLQNx1_ASAP7_75t_SL        1    -     -     0       357    (-,-)
#-------------------------------------------------------------------------------------------------------------------------
```

```
Path 2: MET (16201 ps) Setup Check with Pin op_module/outputL_reg[19]/CLK->D
          View: PVT_0P63V_100C.setup_view
         Group: Sclk
    Startpoint: (R) msdap_main/enable_reg/CLK
         Clock: (R) Sclk
      Endpoint: (R) op_module/outputL_reg[19]/D
         Clock: (F) Sclk

                    Capture       Launch
       Clock Edge:+   16667            0
      Src Latency:+       0            0
      Net Latency:+       0 (I)        0 (I)
          Arrival:=   16667            0

            Setup:-       9
      Uncertainty:-     100
    Required Time:=   16558
     Launch Clock:-       0
        Data Path:-     357
            Slack:=   16201

#-------------------------------------------------------------------------------------------------------------------------
#        Timing Point         Flags    Arc    Edge          Cell             Fanout Load Trans Delay Arrival Instance
#                                                                              (fF)  (ps)  (ps)   (ps)  Location
#-------------------------------------------------------------------------------------------------------------------------
  msdap_main/enable_reg/CLK   -       -       R     (arrival)                  458    -     0     -       0    (-,-)
  msdap_main/enable_reg/QN    -       CLK->QN F     ASYNC_DFFHx1_ASAP7_75t_SL    4  2.8    39    54      54    (-,-)
  op_module/g345/Y            -       B->Y    R     NAND2xp5_ASAP7_75t_SL        1  0.8    25    17      72    (-,-)
  op_module/g342/Y            -       A->Y    R     OR2x2_ASAP7_75t_SL           79 52.8   268   134     205    (-,-)
  op_module/g341/Y            -       A->Y    F     INVx3_ASAP7_75t_SL           78 50.9   187   110     316    (-,-)
  op_module/g337/Y            -       A1->Y   R     AOI22xp5_ASAP7_75t_L         1  0.9    72    41      356    (-,-)
  op_module/outputL_reg[19]/D -       -       R     DFFLQNx1_ASAP7_75t_SL        1    -     -     0       357    (-,-)
#-------------------------------------------------------------------------------------------------------------------------
```

```
Path 3: MET (16201 ps) Setup Check with Pin op_module/outputR_reg[38]/CLK->D
          View: PVT_0P63V_100C.setup_view
         Group: Sclk
    Startpoint: (R) msdap_main/enable_reg/CLK
         Clock: (R) Sclk
      Endpoint: (R) op_module/outputR_reg[38]/D
         Clock: (F) Sclk

                   Capture       Launch
       Clock Edge:+   16667            0
      Src Latency:+       0            0
      Net Latency:+       0 (I)        0 (I)
          Arrival:=   16667            0

            Setup:-       9
      Uncertainty:-     100
    Required Time:=   16558
     Launch Clock:-       0
        Data Path:-     357
            Slack:=   16201

#-------------------------------------------------------------------------------------------------------------------------
#        Timing Point         Flags    Arc    Edge          Cell            Fanout Load Trans Delay Arrival Instance
#                                                                             (fF)  (ps)  (ps)   (ps)  Location
#-------------------------------------------------------------------------------------------------------------------------
  msdap_main/enable_reg/CLK   -       -      R     (arrival)                458    -     0     -       0    (-,-)
  msdap_main/enable_reg/QN    -       CLK->QN F     ASYNC_DFFHx1_ASAP7_75t_SL  4  2.8    39    54      54    (-,-)
  op_module/g345/Y            -       B->Y   R     NAND2xp5_ASAP7_75t_SL      1  0.8    25    17      72    (-,-)
  op_module/g342/Y            -       A->Y   R     OR2x2_ASAP7_75t_SL         79 52.8   268   134     205    (-,-)
  op_module/g341/Y            -       A->Y   F     INVx3_ASAP7_75t_SL         78 50.9   187   110     316    (-,-)
  op_module/g335/Y            -       A1->Y  R     AOI22xp5_ASAP7_75t_L       1  0.9    72    41      356    (-,-)
  op_module/outputR_reg[38]/D -       -      R     DFFLQNx1_ASAP7_75t_SL      1    -     -     0       357    (-,-)
#-------------------------------------------------------------------------------------------------------------------------
```

Power Report:

```
Instance: /msdap
Power Unit: W
PDB Frames: /stim#0/frame#0
  ------------------------------------------------------------------------
    Category         Leakage     Internal    Switching        Total    Row%
  ------------------------------------------------------------------------
      memory     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
    register     6.70194e-05  1.79844e-05  1.39808e-06  8.64019e-05  45.16%
       latch     9.04795e-06  4.50513e-07  1.24447e-07  9.62291e-06   5.03%
       logic     8.19774e-05  3.93389e-06  4.41753e-06  9.03288e-05  47.21%
        bbox     0.00000e+00  0.00000e+00  1.02019e-07  1.02019e-07   0.05%
       clock     3.55308e-08  5.32884e-09  4.84627e-06  4.88713e-06   2.55%
         pad     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
          pm     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
  ------------------------------------------------------------------------
    Subtotal     1.58080e-04  2.23741e-05  1.08883e-05  1.91343e-04 100.00%
  Percentage          82.62%       11.69%        5.69%      100.00% 100.00%
  ------------------------------------------------------------------------
```

Setup Report:

```
============================================================
  Generated by:           Genus(TM) Synthesis Solution 19.14-s108_1
  Generated on:           May 04 2024  05:05:30 pm
  Module:                 msdap
  Operating conditions:   PVT_0P63V_100C
  Interconnect mode:      global
  Area mode:              physical library
============================================================

   Instance          Module       Cell Count  Cell Area  Net Area   Total Area
-------------------------------------------------------------------------------
msdap                                 2466  24926.855  2010.621    26937.476
  hR           hcoeff_memory_569        10   5864.519     3.479     5867.997
    CO_MEM_1   CO_MEM_566               10   5864.519     3.479     5867.997
  hL           hcoeff_memory            10   5864.519     3.479     5867.997
    CO_MEM_1   CO_MEM                   10   5864.519     3.479     5867.997
  xR           x_memory_571              6   3725.153     2.724     3727.877
    DATA_MEM_1 DATA_MEM_567              6   3725.153     2.724     3727.877
  xL           x_memory                  6   3725.153     2.724     3727.877
    DATA_MEM_1 DATA_MEM                  6   3725.153     2.724     3727.877
  alu          alu_controller          862   1776.660   697.571     2474.231
  msdap_main   main_controller         388    889.730   281.325     1171.055
  add_R        adder_1                 354    744.396   221.257      965.653
  add_L        adder                   354    744.396   221.257      965.653
  op_module    final_output            164    491.288    79.060      570.347
  s2p_module   s2p                     148    377.214    87.960      465.174
  shift_R      shifter_1                80    192.689    29.184      221.873
  shift_L      shifter                  80    192.689    29.184      221.873
  rjR          rj_memory_570             2    169.224     0.742      169.965
    R_MEM_1    R_MEM_568                 2    169.224     0.742      169.965
  rjL          rj_memory                 2    169.224     0.742      169.965
    R_MEM_1    R_MEM                     2    169.224     0.742      169.965
```

Innovus Reports:

Area Report:

Hinst Name	Module Name	Inst Count	Total Area
msdap		3562	26532.288
add_L	adder	508	944.317
add_R	adder_1	504	944.084
alu	alu_controller	1189	2238.088
hL	hcoeff_memory	14	5892.512
hL/CO_MEM_1	CO_MEM	14	5892.512
hR	hcoeff_memory_569	15	5893.679
hR/CO_MEM_1	CO_MEM_566	15	5893.679
msdap_main	main_controller	577	1151.470
op_module	final_output	332	727.600
rjL	rj_memory	3	173.656
rjL/R_MEM_1	R_MEM	3	173.656
rjR	rj_memory_570	3	176.455
rjR/R_MEM_1	R_MEM_568	3	176.455
s2p_module	s2p	210	438.800
shift_L	shifter	80	193.856
shift_R	shifter_1	80	193.622
xL	x_memory	6	3736.118
xL/DATA_MEM_1	DATA_MEM	6	3736.118
xR	x_memory_571	6	3737.984
xR/DATA_MEM_1	DATA_MEM_567	6	3737.984

Power Report:

```
*------------------------------------------------------------------------------
*       Innovus 19.11-s128_1 (64bit) 08/20/2019 20:54 (Linux 2.6.32-431.11.2.el6.x86_64)
*
*
*       Date & Time:    2024-May-04 18:06:05 (2024-May-04 23:06:05 GMT)
*
*------------------------------------------------------------------------------
*
*       Design: msdap
*
*       Liberty Libraries used:
*               PVT_0P63V_100C.setup_view: /proj/cad/library/asap7/asap7sc7p5t_27/LIB/NLDM/asap7sc7p5t_SIMPLE_RVT_SS_nldm_201020.lib
*               PVT_0P63V_100C.setup_view: /proj/cad/library/asap7/asap7sc7p5t_27/LIB/NLDM/asap7sc7p5t_SIMPLE_LVT_SS_nldm_201020.lib
*               PVT_0P63V_100C.setup_view: /proj/cad/library/asap7/asap7sc7p5t_27/LIB/NLDM/asap7sc7p5t_SIMPLE_SLVT_SS_nldm_201020.lib
*               PVT_0P63V_100C.setup_view: /proj/cad/library/asap7/asap7sc7p5t_27/LIB/NLDM/asap7sc7p5t_SIMPLE_SRAM_SS_nldm_201020.lib
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*               PVT_0P63V_100C.setup_view: /home/eng/t/txg150930/workspace/ASIC/Memory/lib/SRAM1RW128x12_lib/SRAM1RW128x12_PVT_0P63V_100C.lib
*               PVT_0P63V_100C.setup_view: /home/eng/t/txg150930/workspace/ASIC/Memory/lib/SRAM1RW256x8_lib/SRAM1RW256x8_PVT_0P63V_100C.lib
*               PVT_0P63V_100C.setup_view: /home/eng/t/txg150930/workspace/ASIC/Memory/lib/SRAM2RW16x8_lib/SRAM2RW16x8_PVT_0P63V_100C.lib
```
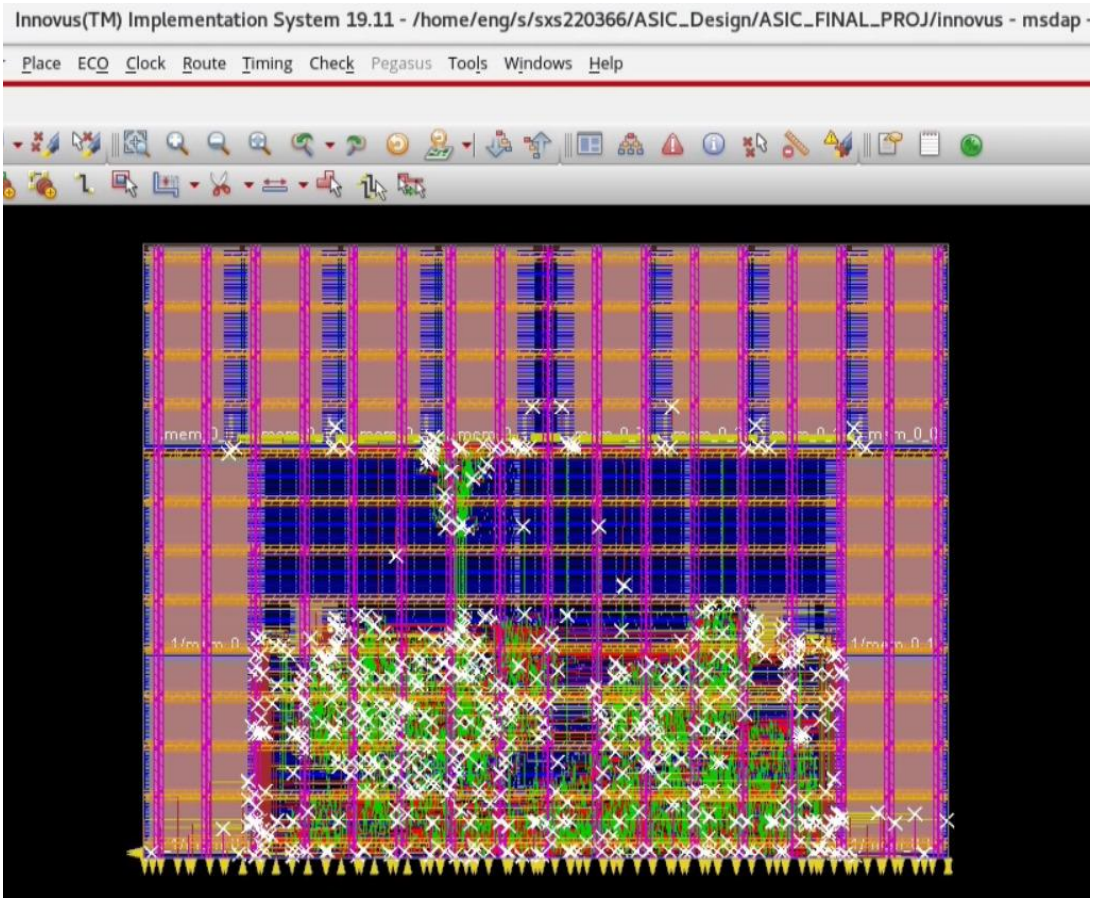
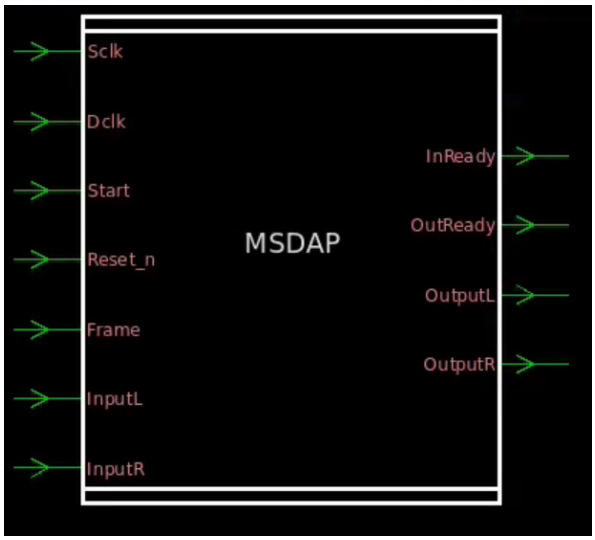

```
*       Power Domain used:
*              Rail:        VDD      Voltage:       0.63
*
*       Power View : PVT_0P63V_100C.setup_view
*
*       User-Defined Activity : N.A.
*
*       Activity File: N.A.
*
*       Hierarchical Global Activity: N.A.
*
*       Global Activity: N.A.
*
*       Sequential Element Activity: 0.200000
*
*       Primary Input Activity: 0.200000
*
*       Default icg ratio: N.A.
*
*       Global Comb ClockGate Ratio: N.A.
*
*       Power Units = 1mW
*
*       Time Units = 1e-12 secs
*
*       report_power -outfile reports/power.rpt
*
--------------------------------------------------------------------------------


Total Power
--------------------------------------------------------------------------------
Total Internal Power:        0.03824016            16.3431%
Total Switching Power:       0.01422068             6.0776%
Total Leakage Power:         0.18152312            77.5793%
Total Power:                 0.23398395
--------------------------------------------------------------------------------


Group                           Internal   Switching     Leakage       Total  Percentage
                                Power      Power         Power         Power  (%)
--------------------------------------------------------------------------------
Sequential                       0.02013    0.001029     0.07419     0.09535       40.75
Macro                                  0   0.0001961           0   0.0001961     0.08381
IO                                     0           0           0           0           0
Combinational                   0.007122    0.006684     0.08922       0.103       44.03
Clock (Combinational)            0.01099    0.006311     0.01811     0.03541       15.13
Clock (Sequential)                     0           0           0           0           0
--------------------------------------------------------------------------------
Total                            0.03824     0.01422      0.1815       0.234         100
--------------------------------------------------------------------------------


Rail                  Voltage   Internal   Switching     Leakage       Total  Percentage
                                Power      Power         Power         Power  (%)
--------------------------------------------------------------------------------
VDD                      0.63    0.03824     0.01422      0.1815       0.234         100


Clock                           Internal   Switching     Leakage       Total  Percentage
                                Power      Power         Power         Power  (%)
--------------------------------------------------------------------------------
Dclk                            6.843e-07   6.465e-06   1.187e-06   8.336e-06    0.003563
Sclk                             0.01099    0.006305     0.01811      0.0354       15.13
--------------------------------------------------------------------------------
Total (excluding duplicates)     0.01099    0.006311     0.01811     0.03541       15.13
--------------------------------------------------------------------------------
 Clock: Dclk
 Clock Period: 0.033333 usec
 Clock Toggle Rate:     1.5361 Mhz
 Clock Static Probability:  0.5000

 Clock: Sclk
 Clock Period: 0.033333 usec
 Clock Toggle Rate:    60.0001 Mhz
 Clock Static Probability:  0.5000



 --------------------------------------------------------------------------------
 *       Power Distribution Summary:
 *               Highest Average Power:       CTS_ccl_a_buf_00062 (BUFx24_ASAP7_75t_SL):         0.001986
 *               Highest Leakage Power:       CTS_ccl_a_buf_00068 (BUFx24_ASAP7_75t_SL):        0.0008622
 *          Total Cap:      8.20301e-12 F
 *          Total instances in design:  3562
 *          Total instances in design with no power:     8
 *          Total instances in design with no activity:     0
 *          Total Fillers and Decap:     0
 --------------------------------------------------------------------------------
```

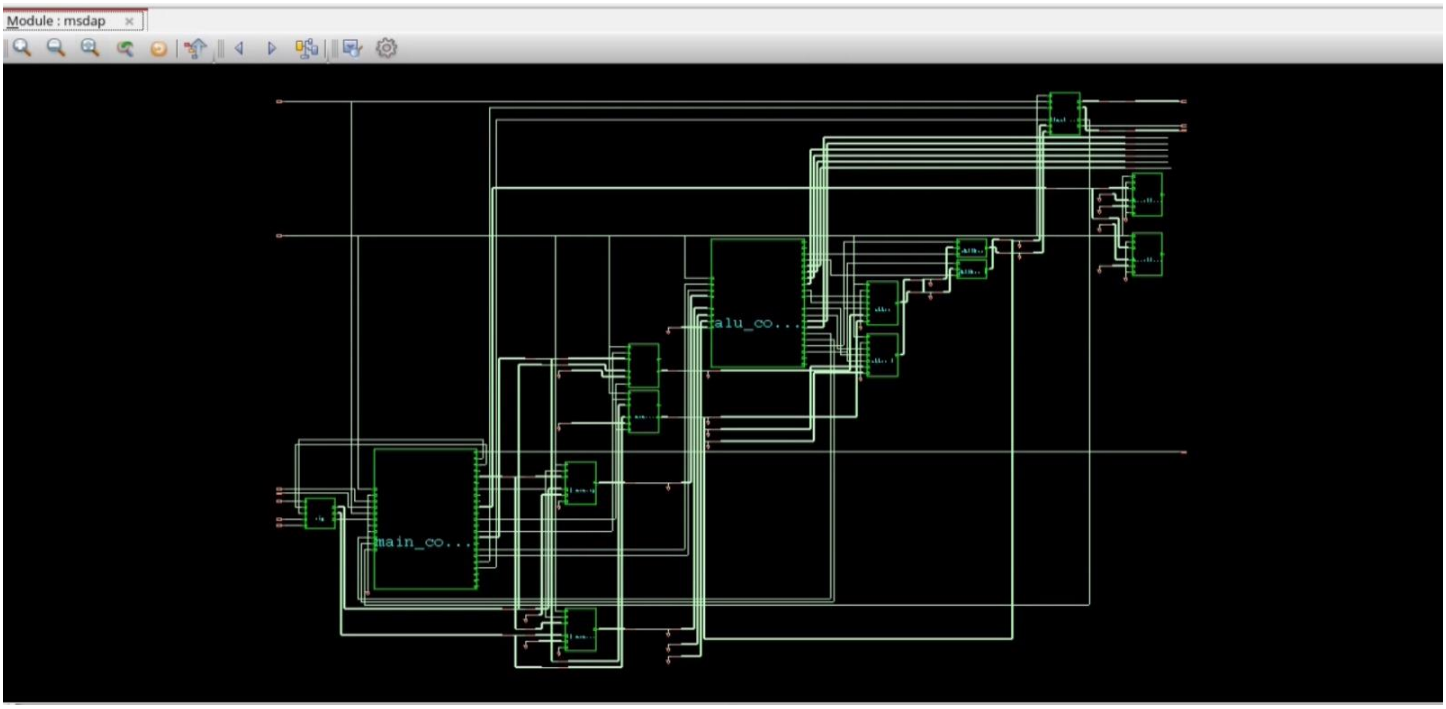
Innovus Layout:



Schematics:

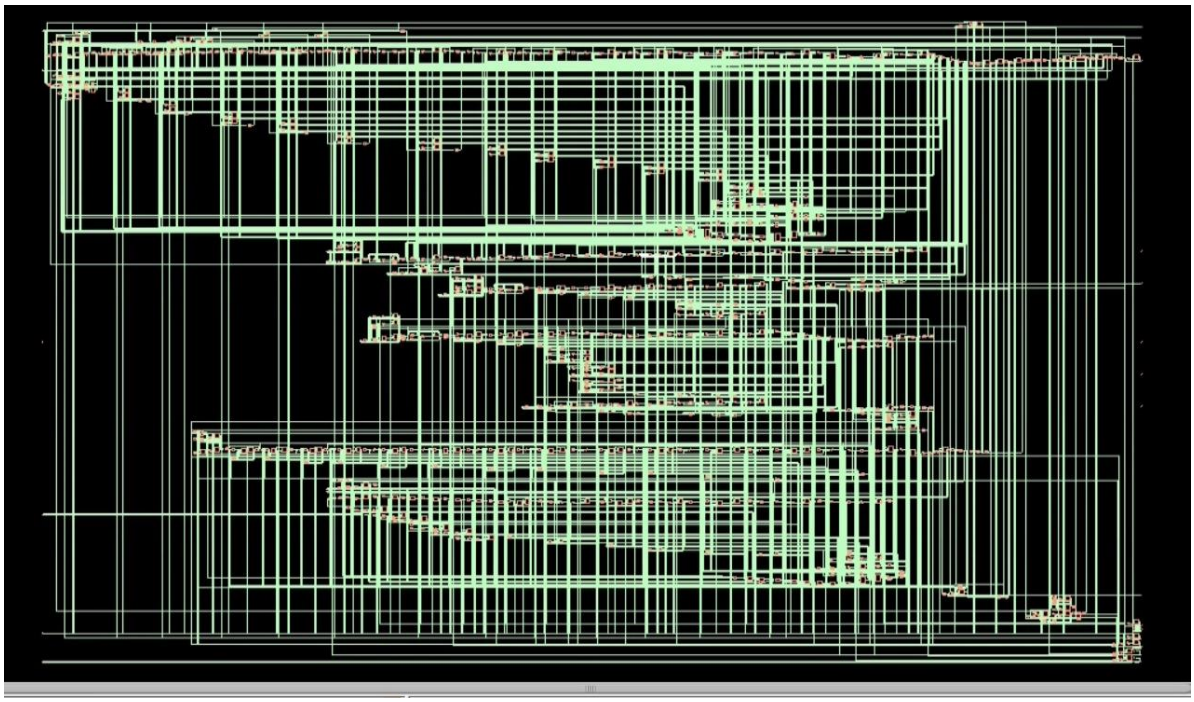
MSDAP:



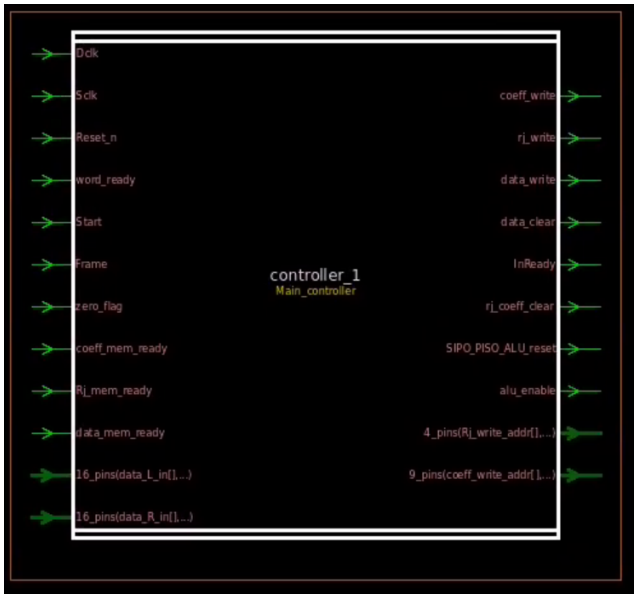


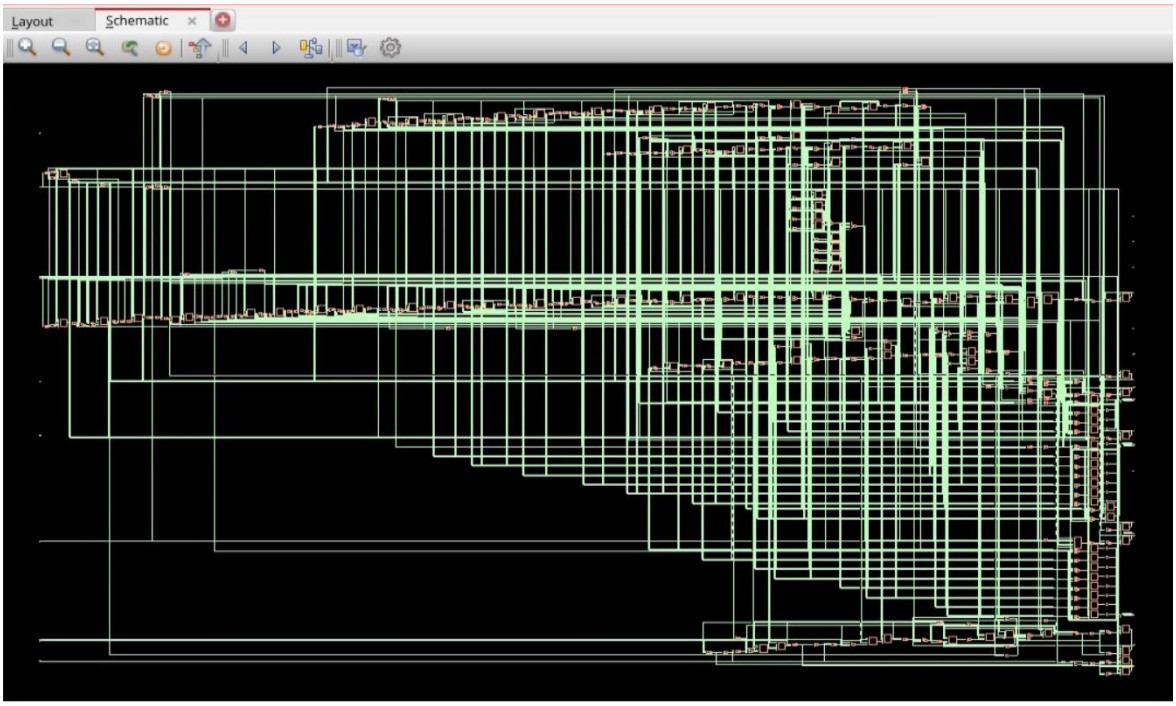
PISO:

ALU Schematic:

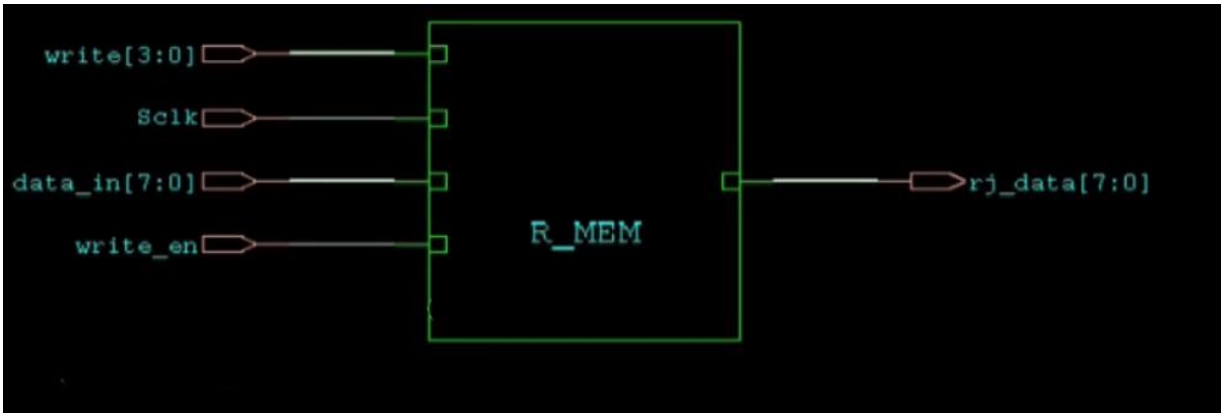


Main Controller:

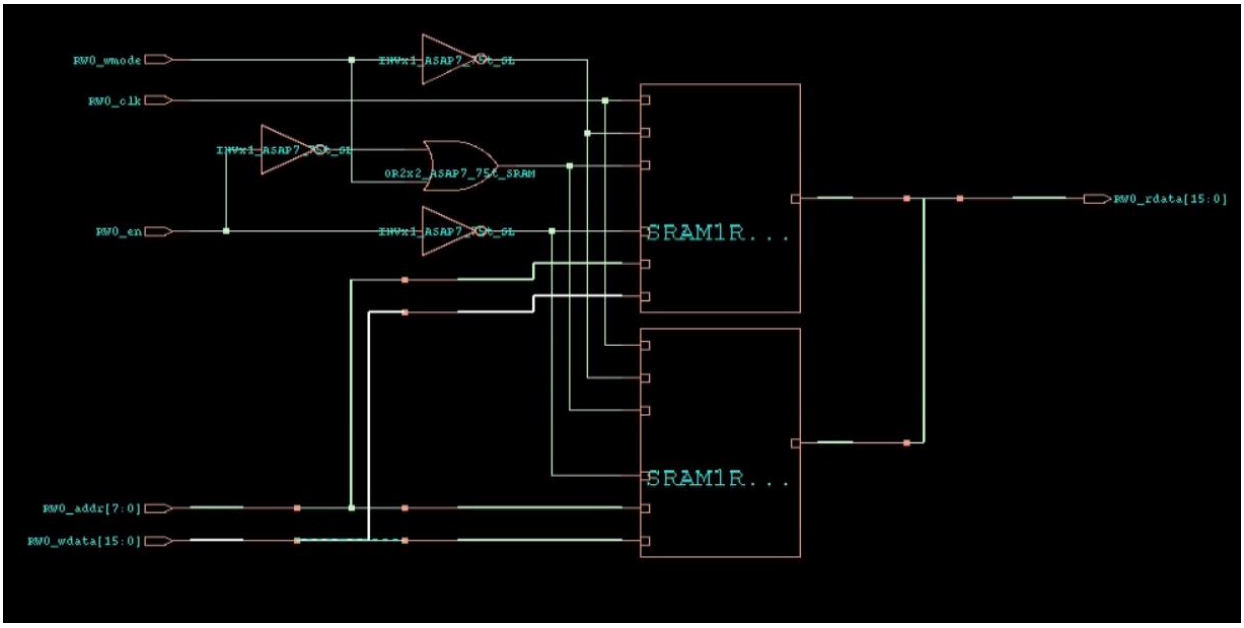




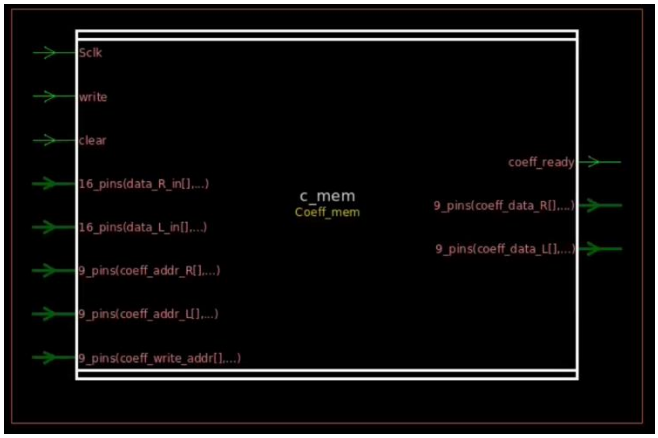
R_j Memory:



Data Memory Schematic:



Co-Efficient Memory:

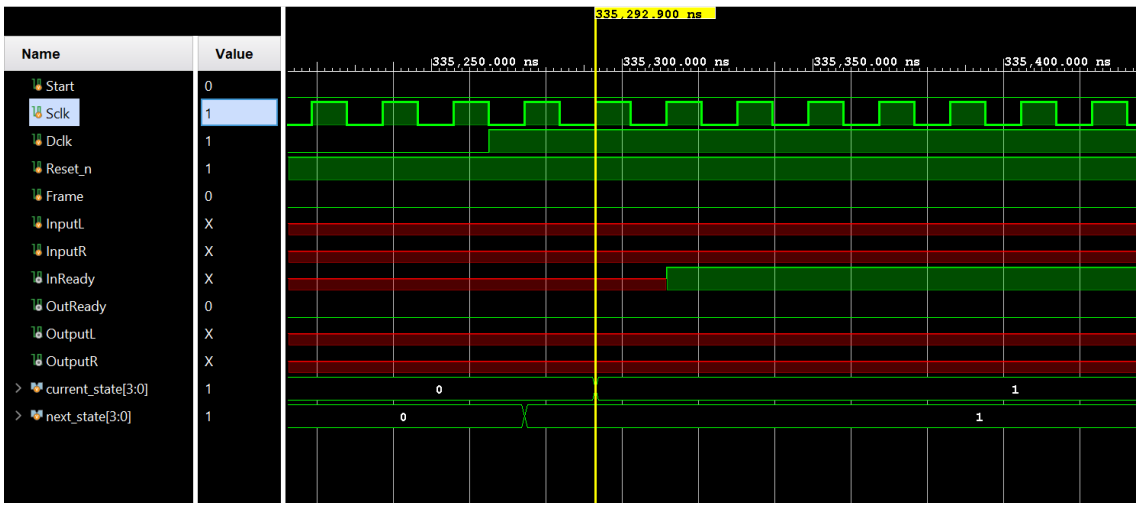


SIPO:

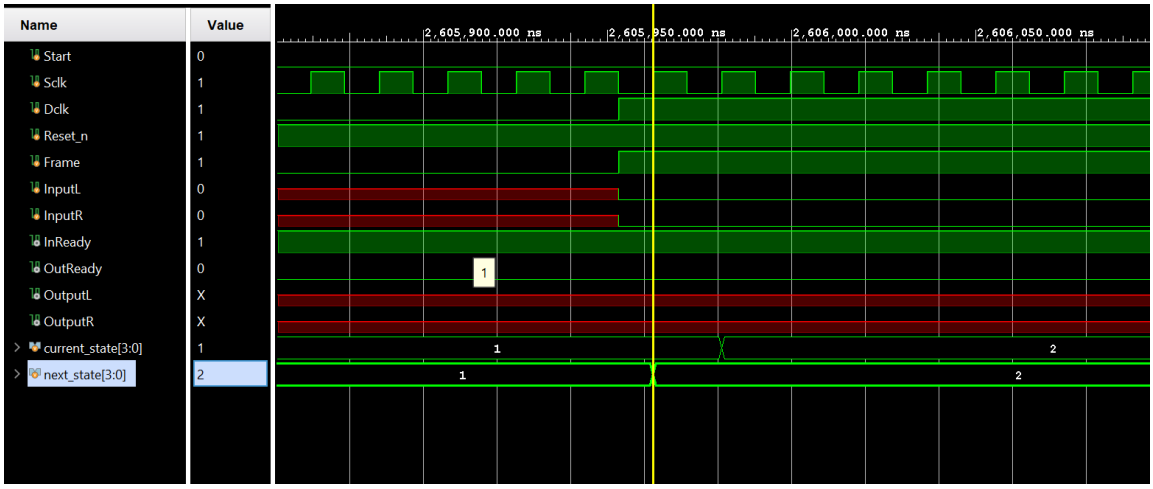
Waveform and explanation

State 0 to 1:

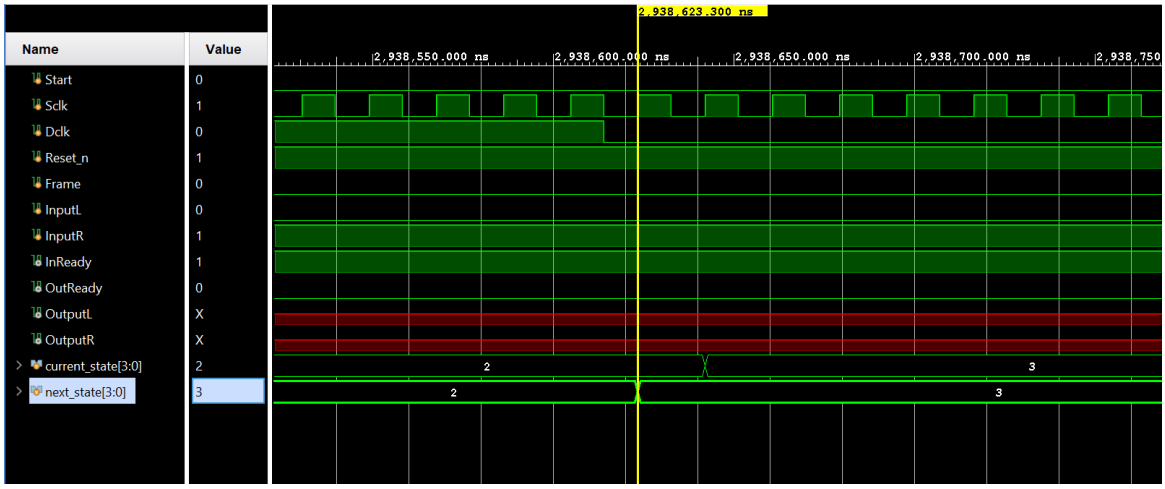
When Start is low, we enter State 1 where we wait to receive Rj.



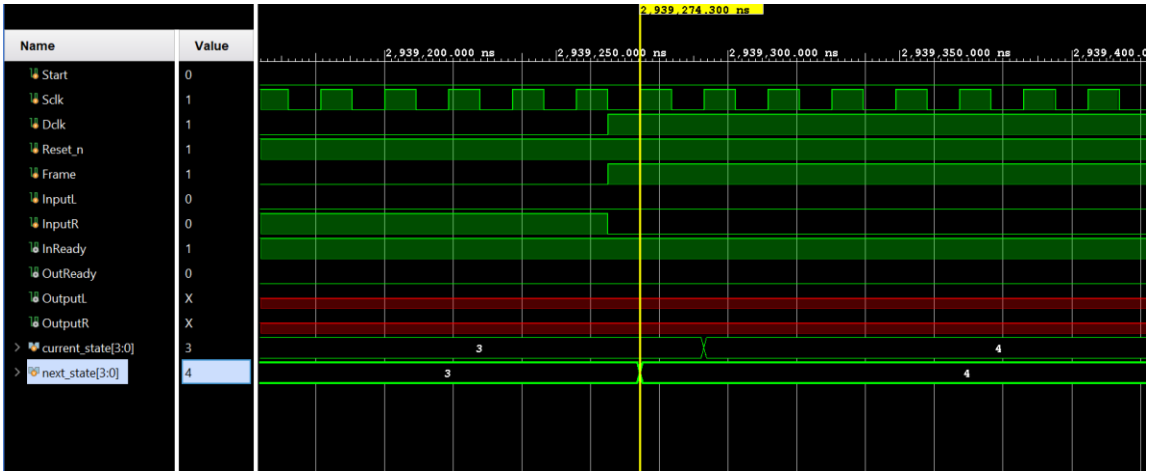
State 1 to 2:
When Frame is high, we enter State 2 where we read the Rj values.



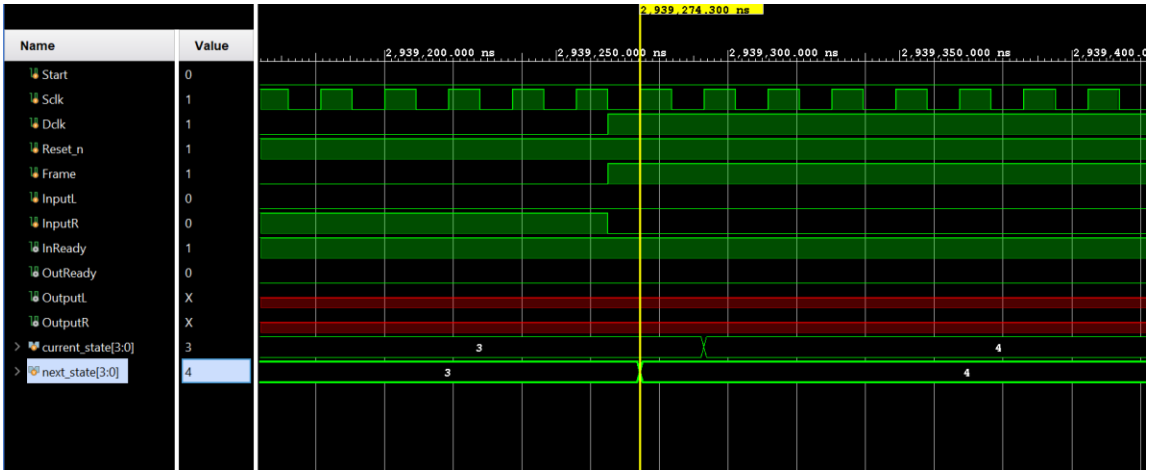
State 2 to 3:
We are done reading Rj values and waiting to receive the coefficient value.



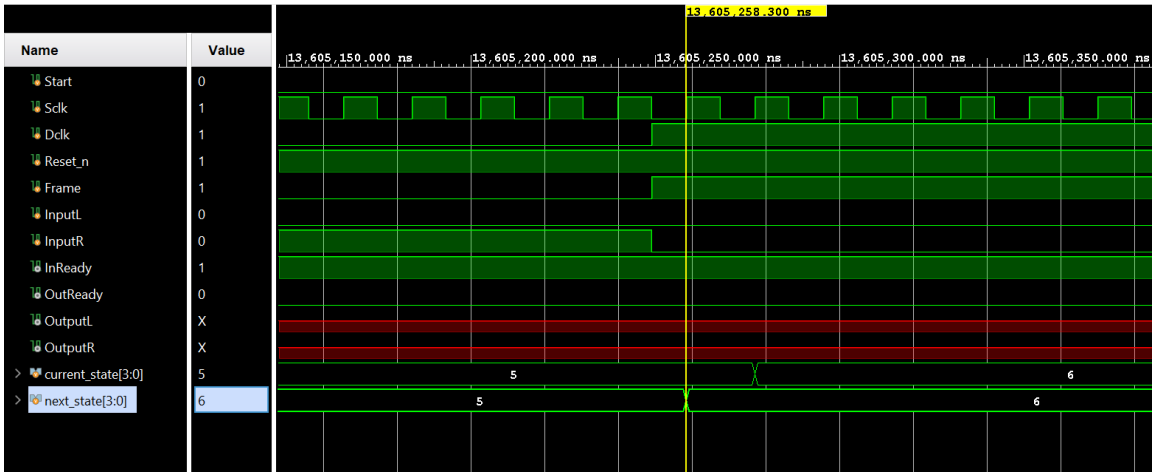
State 3 to 4:
When Frame is high, we enter state 4 and we start reading the coefficients.



State 4 to 5:
We are done reading coefficients values and waiting to receive input.

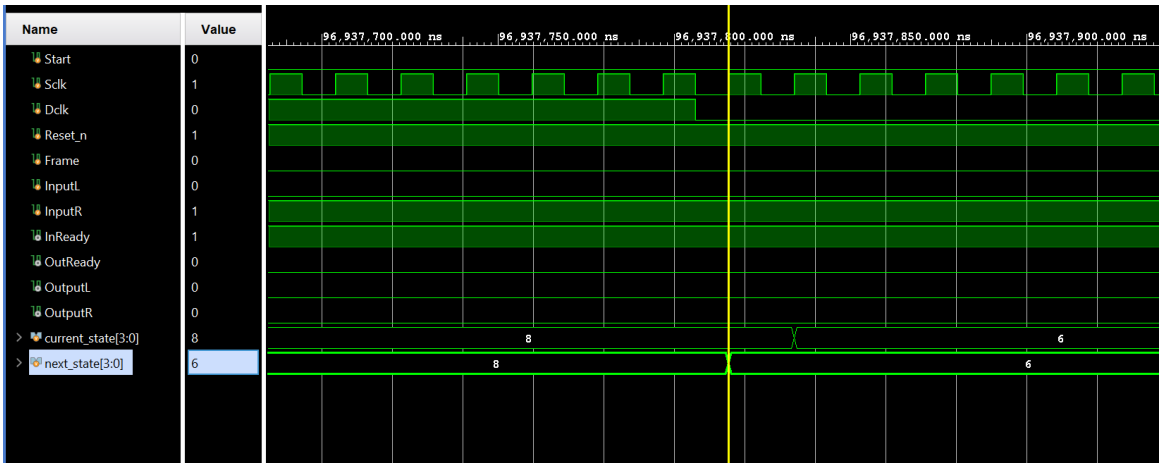


State 5 to 6:
When frame is high, we enter state 6 where we read input samples and perform convolution to obtain a 40-bit output.

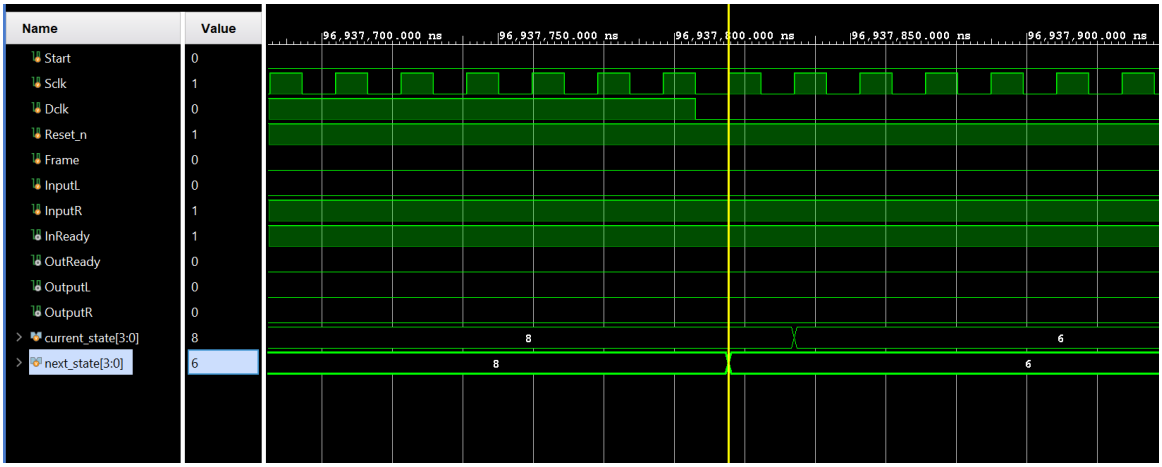


State 6 to 7:
When Reset = 1 in state 6, we enter state 7 from 6 where everything is cleared.

State 6 to 8:
When there are 800 consecutive input samples that are all zeros in both the channels, then we go from State 6 to State 8. State 8 is the Sleeping mode to save energy.

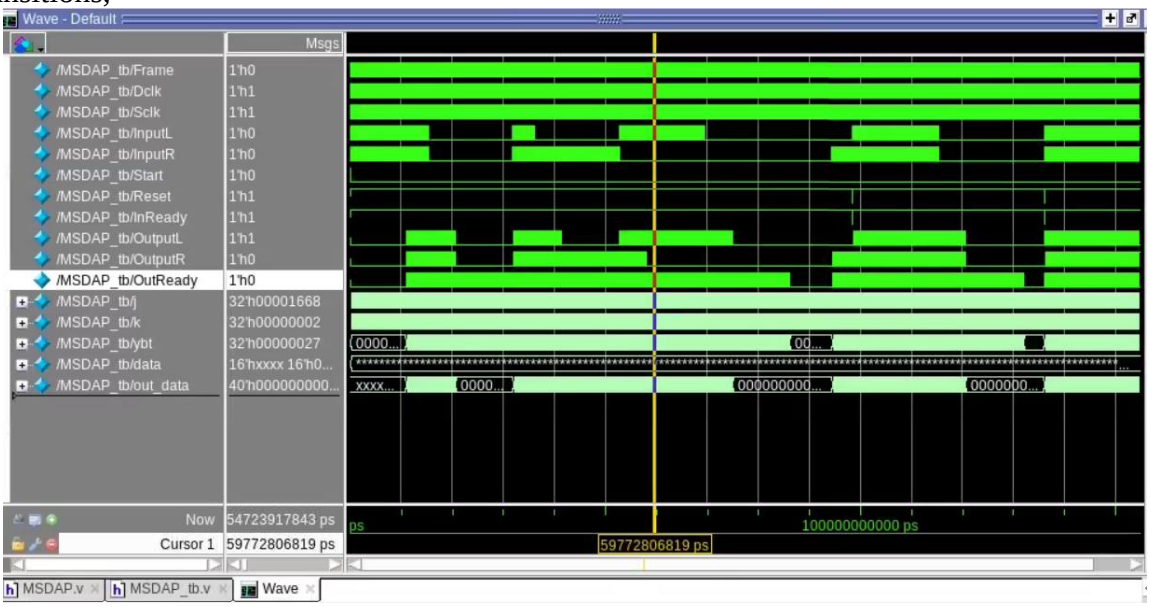


State 7 to 5:
After completion of the task needed for Reset=1 i.e after everything gets cleared, fsm goes to State 5 where it waits to receive the input data.



State 8 to 6:
When there is one non-zero input sample in any one of the input channels, fsm goes from State 8 to 6.

Overall Transitions,



Special Topic On Verification

ASIC design, also known as Application-Specific Integrated Circuit Design, is the process of creating unique integrated circuits for particular applications. Unlike General-Purpose microprocessors, which can handle a variety of functions or processes, ASICs are created to carry out a single mission.

ASIC Design follows the following Steps,

1. Specification
2. Design
3. Verification
4. Layout
5. Fabrication
6. Testing

Specification

First step in ASIC Design, where we define the specifications of the Chip, which it involves determining the parameters like functionality, performance, power consumption and other required parameters that needs to be considered while designing.

Design

This phase involves detailed design of ASIC, which includes Logic Gates, Interconnects, and other components. The Design is generally done in Hardware Description Language (HDL) like VHDL, Verilog and SystemVerilog.

Verification

Once we have the Design, we need to verify whether it meets the required Specifications.

Layout

Once the Verification is done, we can start with the Layout Design, where we create a Physical Layout, which includes the placement of transistors, wiring, and other components.

Fabrication

Once we have the Layout, we manufacture the Chip using the Semiconductor Fabrication Process.

Testing

Once we have the chip fabricated, it is tested to ensure that it functions as intended, which involves the chip under various conditions to ensure that it meets the required specifications.

MSDAP is an example of ASIC Design, where MSDAP has Memory Units, ALU Controller, and S2P/P2S Converters.

To develop a System-Level Behavior Model based on specification, which generally used in Digital Audio Signals, we need to follow the below steps,

1. Define the System Specification:

The first step is defining the system specifications for MSDAP, which includes the functional requirements, interfaces, and performance, which includes defining the input and output interfaces, the sampling rate, the bit resolution, and the processing requirements.

2. Identify the Processor Components:

Once we have the Specs, we need to identify the components which may include identifying the Digital Signal Processing blocks, Memory Blocks, and the other required blocks for processor to function.

3. Develop the Component-Level Behavior Models:

This step will capture the functionalities of each component and how it interacts with the other components.

4. Integrate the Component-Level Behavior Models:

Next Step is to integrate the Component-Level to create a System-Level which involves identifying the interfaces between the components and how they interact with each other.

5. Verify and Validate the System-Level Behavior Models:

This step involves testing the model against the specifications to ensure it meets the functional requirements and performance.

In the case of the Mini Stereo Digital Audio Processor, the system-level behavior model is used to simulate the behavior of the processor at the system level. The model can be used to verify that the processor meets the functional requirements and performance specifications and can be used to develop software that interfaces with the processor.

The system level behavior model for the MSDAP is a high-level abstraction of the processor's functionality, and it is independent from the detailed implementation which means that it can be used to test the processor's behavior without the need for a physical prototype or detailed design information.

We can follow few steps mentioned below:

1. Define Test Scenarios:

The first step is to define the test scenarios that will be used to evaluate the behavior model. The test scenarios will cover all aspects of the processor's functionality, including input/output processing, signal processing, and memory access.

2. Create Input Stimuli:

The next step is to create input stimuli to simulate the audio signals where the MSDAP will process which involves generating audio signals of various types and lengths that cover a wide range of frequencies, amplitudes, and dynamic ranges.

3. Simulate the Behavior Model:

Once we have the input stimuli, the behavior model can be simulated using software tools. The simulation should be run using the input stimuli to generate the corresponding output signals.

4. Analyze the Output Signals:

The output signals generated by the behavior model should be analyzed to verify that they meet the functional requirements and performance specifications of MSDAP. This includes analyzing the signal quality, frequency response, dynamic range, and other characteristics.

5. Iterate and Refine:

If we identify any issues during the analysis, the behavior model can be refined, and the simulation can be re-run to verify that the changes have addressed the issues. The iterative process continues until the behavior model meets all the functional requirements and performance specifications MSDAP.