Saumya Shah

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Education

The University of Texas at Dallas **Dallas, Texas** **January 2023 – December 2024**

- Master of Science in Electrical Engineering **GPA: 3.78/4.00**
- **Relevant Coursework**: VLSI Design, ASIC Design, Physical Design Automation, STA, Functional Verification, Testing & Testable Design, Computer Architecture

Nirma University **Ahmedabad, India** **July 2018 – June 2022**

- Bachelor of Engineering in Electronics and Communication Engineering.

Technical Skills

- **Languages:** Verilog, SystemVerilog, C, Python, Perl, TCL
- **EDA Tools:** Cadence (Virtuoso, Innovus), Synopsys (Design Compiler, PrimeTime, TetraMAX, HSPICE, WaveView), Mentor Calibre, ModelSim, Gem5, AMD Vivado/Vitis
- **Concepts:** Physical Verification (DRC, LVS, ERC, Antenna), STA, Timing ECOs, Place & Route, Clock Tree Synthesis, IR/EM/Noise Analysis, Design for Test (BIST, Scan, ATPG), ASIC Design Flow
- **Protocols:** I2C, SPI, UART
- **Certifications:** Basic Static Timing Analysis (Cadence)

Work Experience

Embedded Engineer **Winwinlabs** **April 2025 – Present**

- Designed and optimized real-time data acquisition and communication framework on ESP32-S3, applying **timing analysis, resource optimization, and verification methodologies** to ensure reliability across deployments.
- Automated firmware updates, configuration management, and debugging processes, demonstrating **scripting and flow automation skills** relevant to EDA workflows.
- Delivered a scalable system architecture balancing performance, power efficiency, and latency, reflecting concepts parallel to **PPA trade-offs in chip implementation**.

Projects

Sobel Edge-Detection for Reconfigurable Computing **September 2024 – December 2024**

- Implemented Sobel filter accelerator with HLS, optimized using synthesis directives.
- Integrated with ARM HPS for hardware/software co-design, reducing latency by 14%.
- Verified cycle-accurate timing and resource utilization with **QoR reports**.

Design and Fault Analysis of Digital Circuits using TetraMAX **January 2024 – April 2024**

- Designed combinational and sequential circuits using Structural Verilog and synthesized using Synopsys Design Compiler.
- Synthesized the design in Synopsys Design Compiler - Design Vision and observed the circuit area, power, and timing reports.
- Enhanced test and fault coverage by 10-12% through Scan Insertion utilizing Design Compiler by generating test vectors using Automatic Test Pattern Generation (ATPG) using Tetramax.

Mini Stereo Digital Audio Processor using ASAP 7nm **January 2024 – April 2024**

- Designed RTL architecture with custom two-channel FIR filter and memory controller.
- Synthesized using Synopsys Design Compiler on ASAP 7nm; verified functionality in ModelSim.
- Automated **floorplan, PnR, STA, and power optimization** via TCL scripting; achieved timing closure and clean signoff.

Analysis of Branch Predictors and Cache Associativity **September 2023 – December 2023**

- Conducted a comprehensive analysis of diverse cache design strategies, assessing the influence on x86 CPU performance. Subsequently, derived an optimal configuration yielding the lowest Cycle Per Instruction (CPI) while maintaining cost efficiency.
- Evaluated the impact of changing variables on branch predictors through experimentation using advanced features from GEM5.
- Generated python scripts to improve the benchmarks' execution speed by 30%.

Design and implementation of FPU with GF65 Technology **September 2023 – December 2023**

- Built custom cell library (NAND, NOR, XOR, AOI, OAI, DFF) in GF65 process.
- Implemented RTL in Verilog and performed synthesis in Synopsys Design Vision.
- Completed **PnR using Cadence Innovus**, optimizing layout for congestion and timing.

RISC Processor Design **January 2023 – March 2023**

- Synthesis and simulation of an 8-bit RISC Harvard Architecture Processor reduced to 32 instructions with user input opcodes.
- Instantiated modules to perform data hazard stall and branch detection logic to avoid writing erroneous data into the memory.
- Developed intricate pipelining techniques within the project scope to enhance instruction execution efficiency of the microcontroller.
- Deployed and verified the design on Nexys3 FPGA.