Chapter

7 Semiconductor Materials Procession

Crystal Growing

Silicon and Germanium are two of the most widely used semiconductor materials. Out of these two, Si has wide spread use because of various favourable factors associated with the material.

- It is most abundant element after oxygen in the earth. About 27.6 % of the earth's crest is made up of silicon.
- The raw material from which pure silicon is extracted is found every where in nature. So it is very cheap.
- There are effective and economical crystallization methods for silicon.
- It is easy for doping by impurities.
- Silicon oxide is used as an excellent insulator, building layer in the MOS devices.
- Silicon has efficient response to solar radiation and light.
- Silicon has relatively high dielectric strength and therefore suitable for power devices.
- It is non toxic. So no special care is needed when using Si for industrial and commercial applications.
- The energy gap of silicon is moderate leading to small leakage current.

There are basically two methods of obtaining pure silicon crystal.

Float Zone Method of Crystal Growth

The Float Zone method is based on the zone melting process as shown in figure. The production takes place under vacuum or in an inert gas medium. The process starts with a high purity polycrystalline rod of raw material and monocrystalline (single crystal) seed crystal that are held face to face in a vertical position and are rotated with a radio frequency (R.F.) heating coil. Both are partially melted.

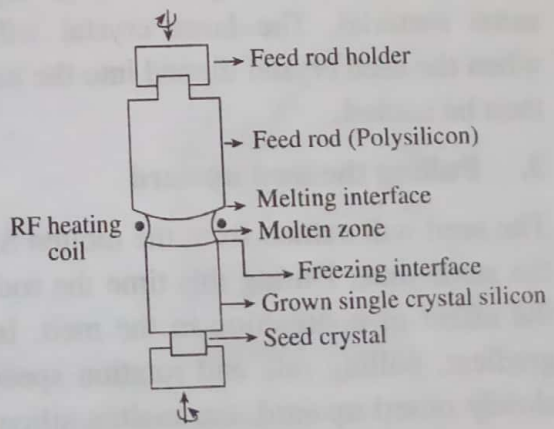


Figure : Floating zone method of crystal growing

As the molten zone is moved along the polycrystalline rod the molten silicon solidifies into a single crystal and simultaneously, the material is purified. Most impurities are more soluble in

melt than in the crystal. A seed crystal is used at one end in order to start growth. The impurities can be removed as they prefer to go to the liquid phase. The diameter of Float Zone wafer (wafer: a round thin piece) are generally not greater than 150 mm due to the surface tension limitation during growth.

The basic feature of this growth technique is that the molten part of the sample is supported by the solid part. After the heating coils move over the whole polysilicon rod, it converts to a single crystal silicon ingot.

Czochralski Crystal Growth

The Czochralsky process is a method of crystal growth used to obtain single crystal of semi conductors. A Silicon wafer is a thin piece of semi conductor material which is used in fabrication process in integrated circuits. The following is the summary of steps in Czochralski process of Silicon wafer manufacturing.

1. Preparation of high purity of molten silicon

In this process high purity of silicon is encouraged to be used as molten form single crystal Silicon. SiO_2 can be used to prepare high purity molten Silicon. Then the substance will be heated to its melting point into a crucible (pot) made of quartz. The supersaturated molten silicon will become the source of silicon wafer.

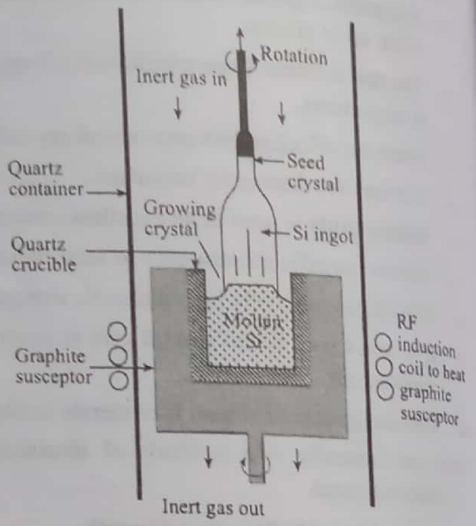


Figure: Single crystal growth by Czochralski method

2. Dipping the seed crystal

A small piece of single crystal material known as seed crystal will be dipped into the saturated molten silicon solution. Seed crystal is equipment used to grow a large crystal of same material. The large crystal will grow when the seed crystal dipped into the melt will then be cooled.

3. Pulling the seed upward

The seed will extract from the molten Silicon pool and rod will be pulled upward and rotated at the same time. During this time the rod and crucible rotated in opposite direction to minimize the effect of contraction in the melt. In manufacturing single crystal silicon, the temperature gradient, pulling rate and rotation speed influences the size of crystal. As the seed crystal is slowly raised upward, the molten silicon will solidifies as same as the seed. This is why this process is called growing which is producing a new crystal of silicon from molten silicon. The large cylindrical crystal silicon is called ingot which can be grown 300mm to 400 mm in diameter.

Diffusion System

Diffusion

Diffusion is a process by which controlled amount of impurities is introduced into the semiconductor to control the majority carrier type and the sheet resistivity of layers formed in the wafer.

The semiconductor is subjected to a high temperature (900 - 1200°C) to an ambient (surrounding on all sides) containing the dopant impurities. These impurity atoms move inside the semiconductor because a concentration gradient exists. The concentration of impurity is high there and there are no impurities to begin with inside the bulk crystal. So concentration of impurity is low into the bulk. Therefore there exists concentration gradient. The movement of impurity is going to be occurred by the existence of point defects i.e. vacancies and interstitial spaces. There are so many vacancies in Silicon. Silicon is a diamond crystal structure where only about 34% space of lattice is occupied by the lattice atoms and 66% of space is free interstitial spaces. So impurity atoms can move in between the regular array of atoms or interstitial spaces. The diffusion in silicon talks place through different mechanism.

Substitutional diffusion takes place by replacing the Si atoms of parent crystal by impurity atoms. At high temperature many atoms in the semiconductor move out of their lattice site leaving vacancies into which impurity atoms can move. The impurities such as P, As, Sb follow this type of diffusion.

In interstitial diffusion, the impurity does not replace the silicon atoms but instead moves into the interstitial voids in the lattice. This type of diffusion occurs for impurity having larger size. Because of large size they do not usually substitute in the silicon lattice. The impurities of group - I and group - VII elements such as Li, Na, He, Ar follow this type of diffusion.

In interstitialcy diffusion mechanism, the impurity atom can move through both vacancies and interstitial spaces. That is, it follows both substitutional and interstitial diffusion.

The impurities such as Cu, Ni, and Gold follow this type of diffusion.

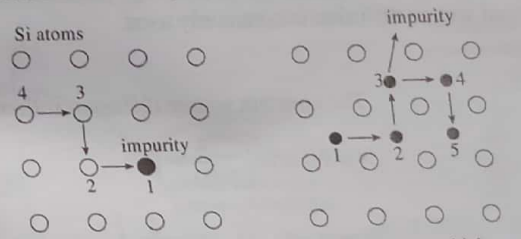


Fig (1): Substitutional diffusion mechanism

Fig (2): Interstitial diffusion mechanism

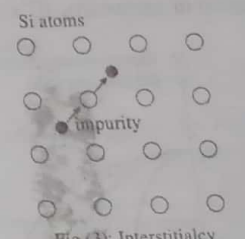


Fig (3): Interstitialcy diffusion mechanism

The diffusion is governed by Fick's first law which states that the rate of transfer of particle per unit area per unit time (F) is proportional to concentration gradient of the particle.

$$\text{i.e. } F = -D\frac{\partial N}{\partial x} \qquad \ldots(1)$$

The negative sign appears because particle flow occurs in the decreasing direction of concentration gradient. Here D is the diffusion coefficient and N is the number of particles per unit volume.

The continuity equation for particle flux is $\frac{\partial N}{\partial t} = -\frac{\partial F}{\partial x}$ ... (2)

Substituting 'F' from equation (1) in equation (2)

$$\frac{\partial N}{\partial t} = -\frac{\partial}{\partial x}\left(-D\frac{\partial N}{\partial x}\right)$$

$$\frac{\partial N}{\partial t} = D\frac{\partial^2 N}{\partial x^2} \qquad ...(3)$$

Equation (3) is called Fick's second law of diffusion

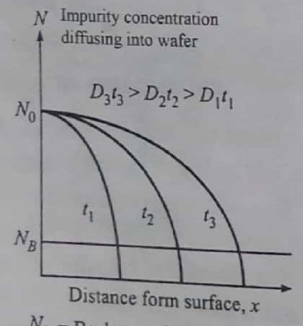
Diffusion Profiles

Depending on boundary equation the Fick's law has two types of solutions. These solutions provide two types of impurity distribution namely constant source diffusion following complementary error function (erfc) and limited source diffusion following Gaussian distribution function.

1. Constant Source Diffusion

In this diffusion, the impurity concentration at the semiconductor surface is maintained at constant level through out the diffusion cycle. As time progresses, the diffusion front proceeds further and further into the wafer with the surface concentration remaining constant. The number of impurity atoms per unit area in Si is called dose (Q)

There is an upper limit to the concentration of any impurity that can be accommodated at the semiconductor at same temperature. This maximum concentration which determines the surface concentration in constant source diffusion is called *solid solubility of the impurity*. In the fabrication of monolithic IC's, constant source diffusion is commonly used.



N_B = Background concentration

The constant source diffusion follows:

$$N = N_o \text{ erfc}\left(\frac{x}{2\sqrt{D_3t_3}}\right),$$

Where $\text{erfc}(z) = 1 - \frac{2}{\sqrt{\pi}}\int_0^z \exp(-x^2)dx$

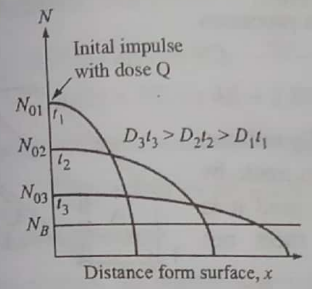
Figure (1): A constant source diffusion results in complementary error function (erfc) impurity distribution. The surface concentration N_0 remains constant, and the diffusion moves deeper into the Si wafer as the Dt product increases.

2. Limited Source Diffusion

Here a predetermined amount of impurity is introduced into the crystal unlike constant source diffusion. The diffusion takes places in two steps.

i. *Predeposition step:* In this step a fixed number of impurity atoms are deposited on the Silicon wafer during short time.

ii. *Drive - in step:* Here the impurity source is turned off and the amounts of impurities already deposited during the first step are allowed to diffuse into silicon wafer.



The limited source diffusion follows,

Gaussian distribution, $N = N_{01} \exp -\left(\frac{x}{2\sqrt{D_1t_1}}\right)^2$

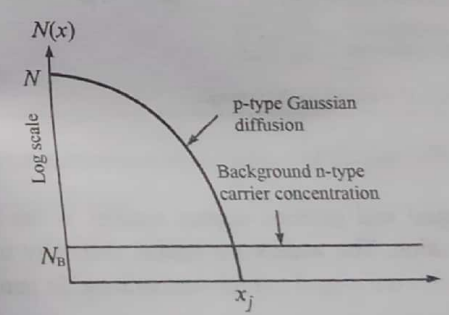
N_{01} = Surface concentration

Figure (2): A Gaussian distribution results from a limited source diffusion. As the Dt product increases, the diffusion front moves more deeply into the wafer and the surface concentration decreases. The area (impurity dose) under each of three curves is the same.

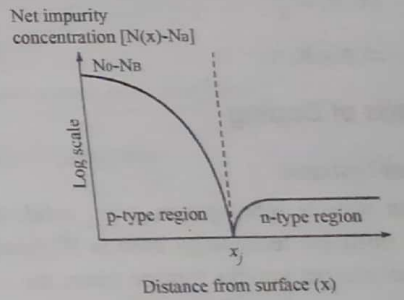
The erfc and Gaussiun function are similar in shape as shown in figure (1) and figure (2). The essential difference between the two types of diffusion is that the surface concentration is held constant for error function diffusion. Where as in Gaussian type it decays with time owing (due to be paid) to a fixed available concentration Q.

Diffusion: pn Junction Formation

Junction Formation by Vertical Diffusion



(1)



(2)

Figure : (1) Formation of pn junction by p-type diffusion into n-type wafer, (2) Net impurity concentration in the wafer

In vertical diffusion, the diffusing species move in a direction normal to the wafer surface. When the acceptors are diffused in n-type wafer, a pn Junction is formed. The diffusion profile is as shown in figure. X_j is the depth where diffused dopant concentration equals wafer dopant concentration (of opposite type)

Lateral Diffusion

It is the diffusion of dopant atoms in the direction parallel to the surface of the wafer. In most semiconductor device manufacturing, it is undesired as it causes lateral distortion of the device geometry. Lateral diffusion is an important effect in coupling device, process design, and for driving the development of self aligned polysilicon gate Mos processes.

Sheet Resistance

It is the measure of resistance of thin films that are nominally uniform in thickness. It is commonly used to characterize the wafers made by semiconductor doping. When the term sheet resistance is used it is implied that the current is along the plane of the sheet not perpendicular to it.

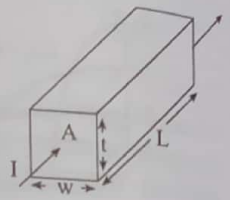


Figure: Resistance block of material having uniform resistivity

In a regular three dimensional conductor, the resistance can be written as,

$$R = \frac{\rho L}{A} = \frac{\rho L}{w.t.} = \frac{\rho}{t} \cdot \frac{L}{w} = \frac{R_s L}{w}$$

$$R = \frac{R_s L}{W}$$

Where R_s is the sheet resistance. If the film thickness is known, the bulk resistivity (ρ) can be calculated by multiplying the sheet resistance by the film thickness.

$$\text{i.e. } R_s = \frac{\rho}{t}$$

$$\Rightarrow \rho = R_s . t.$$

Methods of Doping

Diffusion Systems:

The open furnace tube system using solid, liquid and gaseous dopant sources is the most common diffusion technology used in IC fabrication. The wafers are loaded vertically into a quartz boat and put into the furnace where the wafers are heated to high temperature. In general, diffusion systems are similar to oxidation furnace.

1. **Solid Source:** In this system the dopant source is in solid form as shown in figure (1). The carrier gases N_2 or O_2 picks up the vapour from the dopant source and transport it to the furnace tube, where the dopant atoms are deposited on the surface of wafer.

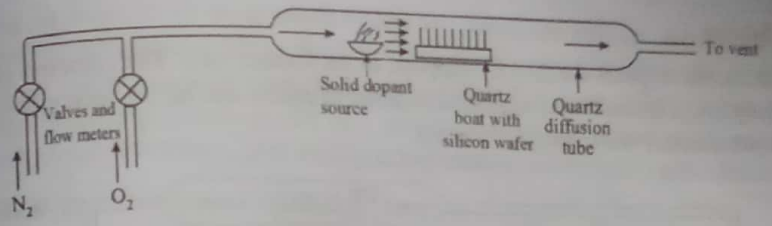


Figure (1): Open furnace tube diffusion system: Solid impurity source

The common solid source of Boron is Trimethyl Borate (TMB)

$$2\,(CH_3O)_3\,B + 9O_2 \xrightarrow{900^0\,C} B_2O_3 + 6CO_2 + 9\,(H_2O)$$

$$2\,B_2O_3 + 3Si \leftrightarrow 4B + 3\,SiO_2$$

The common solid source of Phosphorous is Phosphorous Pentaoxide.

$$2P_2O_5 + 5\,Si \leftrightarrow 4P + 5\,Si\,O_2$$

2. **Liquid Source**

In this system the dopant source is in liquid form as shown in figure (2). The carrier gas passes through a bubbler where it picks up the vapour of the liquid source. The carrier gas carries the vapour into the furnace tube where it reacts with the surface of the silicon wafer.

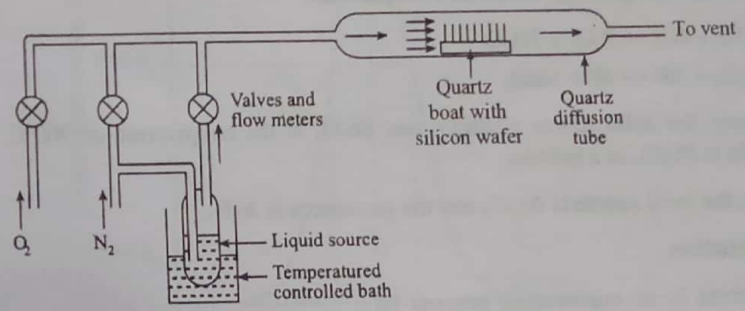


Figure (2): Open furnace tube diffusion system: Liquid impurity source

The most common liquid source of Boron is Boron Tribromide.

The reaction is

$$4\,BBr_3 + 3O_2 \rightarrow 2B_2\,O_3 + 6\,Br_2$$

$$2\,B_2O_3 + 3Si \leftrightarrow 4B + 3\,SiO_2$$

The common liquid source of 'P' is Phosphorous Oxychloride.

$$4\,P\,O\,Cl_3 + 3\,O_2 \rightarrow 2P_2O_5 + 6Cl_2$$

$$2\,P_2O_5 + 5Si \leftrightarrow 4P + 5SiO_2$$

3. Gas Source

In gas sources, the dopants are directly supplied to the furnace tube. The common gas sources are extremely toxic, an additional system is required to ensure that all the source gas is remove from the system before wafer entry or removal.

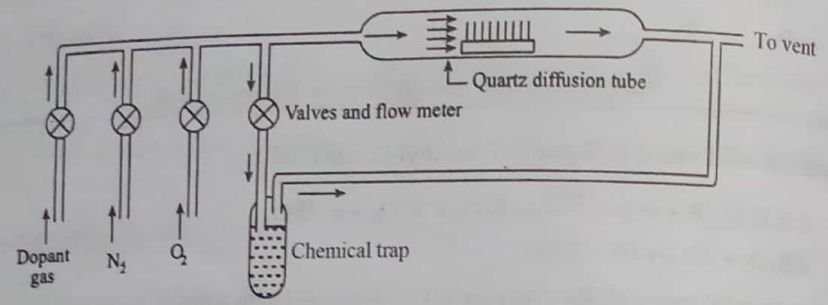


Figure (3): Open furnace tube diffusion system: Gas impurity source

The primary gaseous source of Boron is Diborane. The reaction is,

$$B_2H_6 + 3O_2 \rightarrow B_2O_3 + 3H_2O$$

$$2B_2O_3 + 3Si \leftrightarrow 4B + 3SiO_2$$

Phosphene is used as gaseous source for Phsophorous.

$$2PH_3 + 4O_2 \rightarrow P_2O_5 + 3H_2O$$

$$2P_2O_5 + 5Si \leftrightarrow 4P + 5SiO_2$$

For Antimony, the solid source is Sb_2O_3 and Sb_2O_4 at the temperature of 900°C. The liquid source for Sb is Sb_3Cl_5 in a bubbler.

For Arsenic, the solid source is As_2O_3 and the gas source is AsH_3.

Ion Implantation

Ion implantation is an engineering process by which ions of a material are accelerated in an electric field and impacted into a solid. This process is used to change the physical, chemical or electrical properties of solid. Ion implantation is used in semiconductor device fabrication and in metal finishing as well as in various applications of material science research.

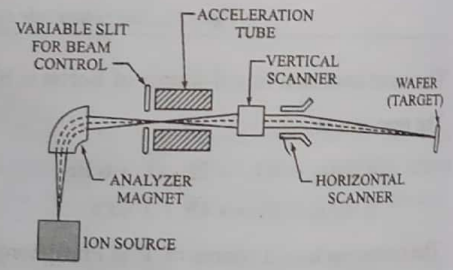


Figure 1: Ion implanter

An ion implantation equipment consists of an ion source where plasma of desired impurity are produced, an accelerator (the accelerating voltage may be from 20 kV to as much as 250 kV) where the ions are accelerated to a high energy and a target chamber where the ions impinge on a target which is the material to be implanted. An analyzer magnet bends the ion beam through a right angle to select the desired impurity ion. Scanning system consist of a vertical scanner and a horizontal scanner which provides necessary deflection to give a uniform implantation and to build up the desired dose.

The centrifugal force is balanced by magnetic force.

$$Bqv = \frac{mv^2}{r}$$

$$B = \frac{mv}{qr}$$

$$r = \frac{mv}{Bq} \qquad ...(1)$$

This means the impurities having different mass have different radius. This allows us to pass desired impurity species by providing slit on the path of beam.

And, the electrostatic energy provides necessary kinetic energy.

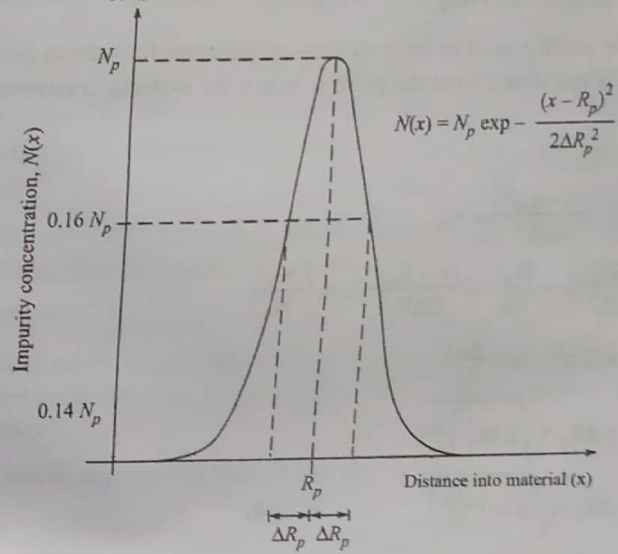


Figure 2: Gaussian distribution resulting from ion implantation

$$qV = \frac{1}{2}mv^2$$

$$v = \sqrt{\frac{2qV}{m}}$$

$$B = \frac{mv}{qr} = \frac{m}{qr}\sqrt{\frac{2qV}{m}} = \sqrt{\frac{2qV}{m} \times \frac{m^2}{q^2r^2}}$$

$$B = \sqrt{\frac{2mV}{qr^2}} \qquad ...(2)$$

So the magnitude of magnetic field can be adjusted for a required ion of mass 'm'.

The target chamber is maintained at relativity low temperature during the implantation which prevents undesired spreading of impurities by diffusion. It is very important in VLSI (very large scale integration) fabrication. A wide range of impurities can be implanted by Ion implantation process as compared to that of diffusion. There is precise control of dose and depth profile.

Ion implantation usually follows a Gaussian distribution as given by

$$N(x) = N_p \exp\left[-\frac{(x - R_p)^2}{2\Delta R_p^2}\right] \qquad ...(3)$$

Where, N(x) is the impurity concentration

N_p is the peak concentration

R_p is the projected range and ΔR_p is the standard deviation called *straggle* (straggle: to spread out from others in a disorganized way)

The ion implantation is often used to form shallow pn junctions for various device applications. The *junction depth* is calculated from the point at which the impurity concentration equals bulk concentration.

i.e. $N(x_j) = N_B$

or, $N_p \exp\left[-\frac{(x_j - R_p)^2}{2\Delta R_p^2}\right] = N_B$

$$\exp\left[\frac{(x_j - R_p)^2}{2\Delta R_p^2}\right] = \frac{N_p}{N_B} \Rightarrow \frac{(x_j - R_p)^2}{2\Delta R_p^2} = ln\left(\frac{N_p}{N_B}\right)$$

$$(x_j - R_p)^2 = 2\,\Delta R_p^2\, ln\left(\frac{N_p}{N_B}\right)$$

$$x_j - R_p = \pm \Delta R_p \sqrt{2\, ln\left(\frac{N_p}{N_B}\right)}$$

$$x_j = R_p \pm \Delta R_p \sqrt{2\, ln\left(\frac{N_p}{N_B}\right)} \qquad ...(4)$$

Lattice Damage and Annealing in Ion Implantation

The incident ions during implantation produce many defects in the target crystal on impact such as vacancies and interstitials. This is called *damaging* the implanted region in the crystal.

Vacancies are crystal lattice points unoccupied by an atom. In this case the incident ion transfer sufficient amount of energy to the target atom such that the target atom leaves crystal site. This target atom then itself becomes a projectile in the solid and can successive collision events. Interstitials results when the incident ion come to rest in solid but finds no vacant space in the lattice to reside. These point defects can migrate and cluster with each other resulting in dislocation loops and other defects.

This damage recovery is done by heating the wafer to a temperature ~ 900°C for approximately 30 minutes and then cooling slowly. This process is called *annealing*. At this temperature, the Si atoms can move back into lattice site and impurity atoms can enter substitutional sites. The larger amount of crystallographic damage can be enough to completely amorphize the surface of the target that is it can become an amorphous solid. With heavier impurity lower dose will be required to create an amorphous layer. An amorphous is a solid that lacks the long range order that is characteristic of metal.

In some cases, the complete amorphization of a target is preferable to a highly defective crystal and regrown by annealing.

Chemical Vapour Deposition

Chemical vapour deposition (CVD) is a technique for depositing thin films of materials on wafer or other substrates. In this process, the substrate is placed inside a reactor where a thermal decomposition and chemical reaction takes place between the source gases. The product of that reaction is a solid which condenses on the surface of wafer.

Polysilicon, Silicon dioxide, Silicon nitride and Phosphorous pento-oxide etc are deposited using CVD technique. CVD can be performed at pressures for which the mean free path for gas molecule is quite small.

⇒ For Silicon the chemical vapour deposition process is the synthesis of polycrystalline Silicon from Silane ($Si H_4$), using the reaction.

$$Si H_4 \rightarrow Si + 2H_2$$

The medium would either be pure Silane gas or Silane with 70-80% Nitrogen. Pure silicon can be deposited at the rate between 10 and 20 nm per minute, perfect for many circuit board components.

⇒ Silicon dioxide can be deposited by using Silane and Oxygen.

$$SiH_4 + O_2 \rightarrow SiO_2 + 2H_2$$

⇒ Silicon nitride is often used as insulator and chemical barrier in manufacturing integrated circuits.

$$3\,Si H_4 + 3NH_3 \rightarrow Si_3 N_4 + 12H_2$$

⇒ Phsophorous pentaoxide can be deposited by using Phosphine and Oxygen gas as

$$4\,PH_3 + 5O_2 \rightarrow 2P_2O_5 + 6H_2$$

Epitaxial Growth

Epitaxy refers to the deposition of a crystalline over layer on a crystalline substrate. The overlayer is called an epitaxial film or epitaxial layer. If the over layer either forms a random orientation with respect to the substrate or does not form an ordered over layer, it is termed as non epitaxial growth. The term epitaxy comes from Greek roots 'epi' meaning 'above' and taxis meaning 'an ordered manner'.

1. The vapour phase epitaxy (VPE) is a modification of chemical vapour deposition is commonly used to deposit Silicon.

   $SiCl_4$ (gas) + $2H_2$ (gas) $\leftrightarrow$ Si (solid) + 4HCl (gas)

   This reaction takes place at approximately 1200 to 1250°C and is reversible.

   The Silicon VPE may also use pyrolytic (Pyrolytic: Chemical change because of heat) decomposition of silane.

   $SiH_4 \xrightarrow{650^\circ C} Si + 2H_2$

   This reaction is not reversible and takes place at lower temperature.

2. In liquid phase epitaxy (LPE), the substrate is dissolved into the melt of the material to be deposited. This happens at temperature well below the melting point of the substrate material. The substrate acts as a seed for material crystallizing directly from the melt.
3. Solid phase epitaxy (SPE) is usually done by first depositing a film of amorphous material on a crystalline substrate. The substrate is then heated to crystallize the film.
4. In molecular beam epitaxy (MBE), a source material is heated to produce an evaporated beam of particles. These particles travel through a very high vaccum to the substrate where they condense. Substrate temperature during this process ranges from 400 - 900°C.

Photolithography

It is the process which involves photographic transfer of a pattern to the surface of wafer to make diffusion window by etching. In this process a geometrical pattern is transferred from a mask to the surface of Silicon wafer. Lithography literally means "Writing on stone". Photolithography involves following steps.

Step 1: *Coat Si with oxide then with photo resist.*

At first the Silicon single crystal is oxidized in an oxidation furnace to form a thin layer of SiO_2, which is excellent barrier against diffusion. Again coat the wafer with a radiation sensitive polymer film called the photo resist. Spin the silicon wafer very fast so that coating is uniform (figure 1)

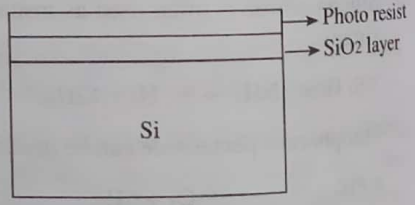


Figure (1)

Step 2: *Expose to radiation and develop the pattern.*

Allow the UV radiation to fall on photo resist through mask. A mask is a glass plate with transparent and opaque regions made on it. Only those regions of the mask which are transparent allow the radiation to fall on the semiconductor. Only those portions which are exposed to radiation, their properties are going to change. The photo resists from the exposed regions are removed. Now the mask pattern is transferred to top of wafer. (Figure 2)

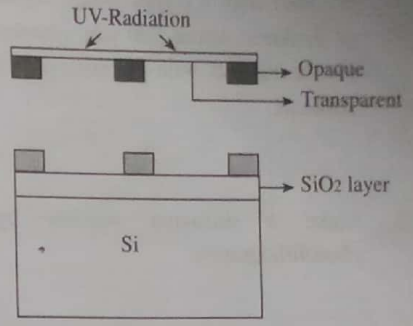


Figure (2)

Step 3: Now the substance is kept in diluted etching solution, the SiO_2 from the Si regions corresponding to transparency of mask is removed. (Figure 3)

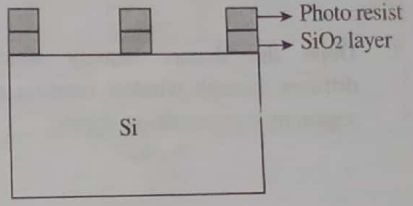


Figure (3)

Step 4: All the photo resist is removed by keeping it on photo resist remover solution. (Figure 4)

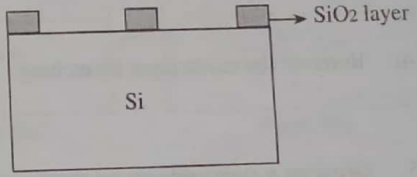


Figure (4)

Compare the pattern on mask with pattern of SiO_2 on the top of Si wafer, the opaque regions on the mask have corresponding pattern of SiO_2 on Si wafer. The regions corresponding to transparency of mask have no oxide. These are the regions where the dopant will be incorporated. This process in which UV light is used to produce the diffusion window pattern is called *Photolithography*.

The pattern on the mask and wafer are identical. Those pattern obtained on wafer are said to be due to positive photo resist. A positive resist is one which gets soften when exposed to radiation. If the photo resist is hard, the complement pattern is obtained with semiconductor regions etched with UV radiation. It is called a negative photo resist.

(Note: SiO_2 is an excellent insulating material. It has good masking properties. The region which is not to be doped is masked with SiO_2. It does not allow dopant to pass through it.)

Monolithic IC Fabrication: Planer Process

In the planner process, the fabrication of IC is done plane by plane at one surface of the wafer so that the deepest region tends to be fabricated first. We will consider fabrication of a npn bipolar junction transistor. The fabrication follows following steps.

1. We start with a p-type single crystal of thickness about 200 μm, oriented {1, 1, 1} and with a resistivity of 10Ω-cm.

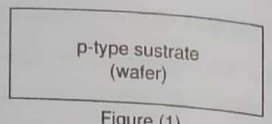


Figure (1)

2. Make a diffusion window by photolithography.

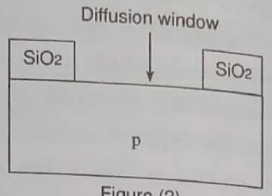


Figure (2)

3. Dope the donors heavily which diffuses through window creating n-region by compensation doping.

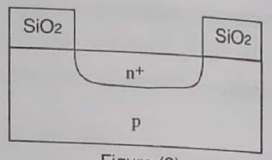


Figure (3)

4. Remove the oxide layer by etching.

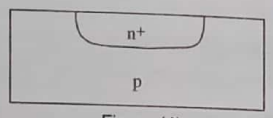


Figure (4)

5. Grow an n-type epilayer on the top of wafer by epitaxy [epitaxy - arranged upon]. The epitaxial layer is very much thinner to the original layer of bulk. This grown epitaxial layer is going to be collector of npn transistor.

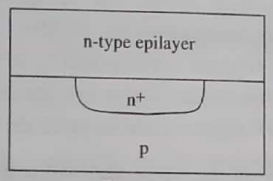


Figure (5)

6. Grow an oxide layer over the whole surface and then etch windows at the corners for isolation diffusion (after photolithography)

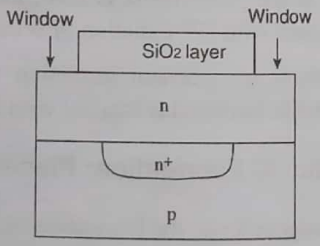


Figure (6)

7. Diffuse acceptor dopants heavily through the windows in oxide.

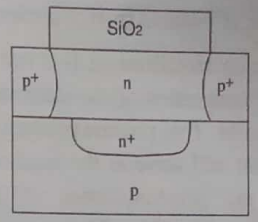


Figure (7)

8. For Integrated circuits, the extended form of figure (7) will be as shown in figure (8). Here the two transistors are isolated called *pn Junction isolation*.

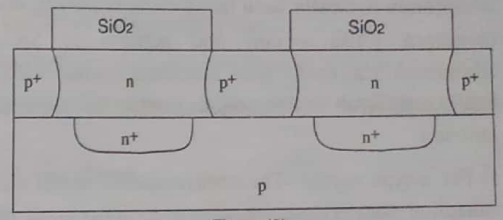


Figure (8)

9. Again focusing on the single npn transistor (fig 9a).
Now doping acceptors over n-region to form p-region for base diffusion [after photolithography] (figure 9b)

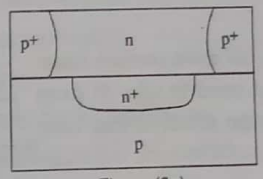


Figure (9a)

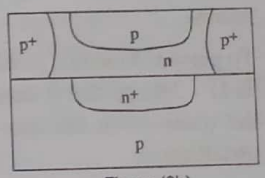


Figure (9b)

10. Again dop donors to form emitter. (After photolithography)

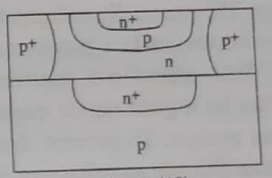


Figure (10)

11. Metalization involves deposition of metal (mostly aluminum) elements over base, collector and emitter region (After photolithography) for electrical connection. Remove all oxide layer and unwanted metal deposition by etching. Thus fabricated 'npn' transistor can be used after electrically tested.

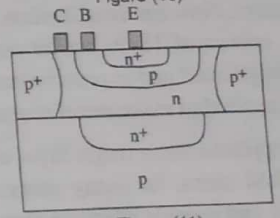


Figure (11)

Note: Doping can be done either by diffusion or by Ion Implantation method.

Metallization: (Contacts In IC Fabrication)

In IC fabrication metallization is a last step. Metal contact is the connection of the integrated circuit to the outside world. This process produces a thin film metal layer that will serve as the required conductor pattern for the interconnection of the various components on the chip. Most commonly used metals for metallization are aluminium and copper.

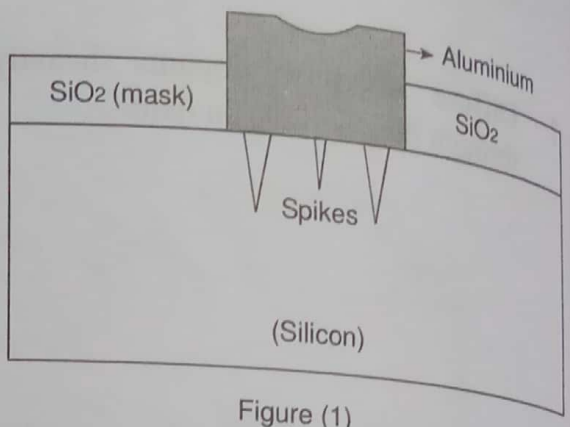


Figure (1)

Aluminium is mostly used being cheaper having low resistance ($3\mu\Omega$ - cm) and adheres to SiO_2. Aluminium can easily form an ohmic contact with p-type region and heavily doped n^+ region. But it is difficult to form ohmic contact to moderately doped n-region rather it forms Schottky junction.

a) For p-type region: The semiconductor reacts with metallization at only 200-250°C. It is the annealing temperature for silicon to form good ohmic contact. However at this temperature Aluminium dissolves silicon and make spike in p-region which can cause short circuits. This problem became more severe as the device dimension is smaller and the contact window is narrow.

To prevent from this problem, A*l* must contain some Si (1 - 2%) so that it does not need to take Si from the wafer. With this cure p-type material can have metallization.

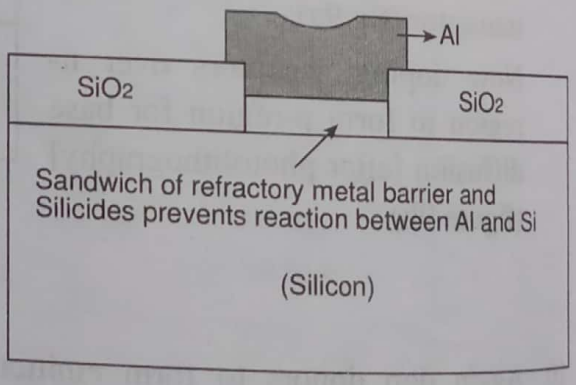


Figure (2)

b) For n^+ - region: If we put Si mixed A*l* in a heavily doped n^+ region. The excess Si will precipitate. The A*l* (trivalent - Acceptor) make a p-type material with precipitate Si. This makes p-n junction with n^+ region. It will not be a good ohmic contact or be a non linear ohmic contact. To prevent from this, first deposit Pt or Pd Silicides. Aluminum is still eating Si from Silicide so refractory barrier of Titanium (Ti) or Tungsten (W) is coated on the top of Silicides. Now for metallization, put Al on top of this barrier. The final contact consist of a sandwich consist of Ti, W barrier over the Silicide through which Al diffuses. Obviously this is more complicated and expensive process but it results in better reliability of contact. This process is also applied to make metal contact in n-region.

In most of the applications, a single layer of metal does not provide sufficient capability to fully interconnect VLSI chips. So many processes use several levels of metallization in order to ensure wirability and provide adequate power distribution.

Note: Silicide - Binary compound of Si.