Saurabh Dash

Curriculum Vitae

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Research Interests

Neuromorphic Algorithms, Deep Learning Algorithms and Accelerators, Brain-Machine Interfaces

Education

2019-Present	**PhD**, *Electrical & Computer Engineering*, Georgia Institute of Technology, *GPA - 4/4*.
2014-2019	**Dual Degree (B.S. + M.S.)**, *Electronics & Electrical Communications Engineering	Minor in Computer Science & Engineering*, Indian Institute of Technology, Kharagpur, *GPA - 9.17/10*.
2012–2014	**Higher Secondary Education**, FIITJEE, Hyderabad, *Aggregate - 96.9%*.
Upto 2012	**Secondary Education**, Delhi Public School, Secunderabad, *GPA - 10/10*.

Publications

Co-Author	*Low Power Implantable Spike Sorting Scheme based on Neuromorphic Classifier with Supervised Training Engine.* IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2017
Co-Author	*Low Cost Autonomous Navigation and Control of a Mechanically Balanced Bicycle.* Transportation Electrification Conference (ITEC), 2015 IEEE International

Internships

May 2018 - July 2018	**Summer Intern**, Texas Instruments, India Developed digital signal processing algorithms for tracking and correction of sampling clock jitter in high speed ADCs. *Received a Pre-Placement offer to join the firm as a Digital Engineer.*
May 2017 - July 2017	**Visiting Student Researcher**, Nanyang Technological University, Singapore Advisor: Dr.Arindam Basu Explored a novel hardware amenable re-wiring training rule to train binary and multi-bit synapses for neuromorphic classifiers to power the next generation of implantable Brain-Computer Interfaces.

Research Experience

July 2017 - April 2019	**Low Power On-Chip Learner for a Neuromorphic Classifier** Undergraduate and Masters' Dissertation Advisors: Dr.Indrajit Chakrabarti, IIT Kharagpur and Dr.Arindam Basu, NTU Singapore Implementing network rewiring rule based sub-threshold analog circuits that can be incorporated on the same chip to train a neuromorphic classifier. *Nominated by the panel for the best B.Tech Thesis award.*
February 2015 - April 2019	**Kharagpur RoboSoccer Students' Group**	Embedded Electronics Team Head Advisors: Dr.Jayanta Mukhopadhyay, Dr.Sudeshna Sarkar, Dr.A.K Deb Developed and fabricated embedded systems based on AVR and ARM microcontrollers and FPGA based architectures. Designed and implemented a proprietary brushless DC motor Controller for the robots. Devised Fuzzy and PID controllers for precision speed control of brushless DC Motors.
August 2017 - November 2017	**Neuronal Encoding/Decoding and Synaptic Plasticity in Visual Cortex** Advisor: Prof.Sharba Bandyopadhyay	Academic Project Used STA and PSTH to estimate parameters from stimulus input and response spikes. Applied Information theory based distance metrics like Van Rossum and Victor-Purpura to quantify discrimination between stimuli. Modelled the spiking behaviour of subplate and L4 neurons, with thalamic inputs from both eyes. Used STDP and Hebbian plasticity to simulate learning and ocular dominance in early stages of development.

March 2016 - April 2016	**Analog Transmitter-Receiver for Energy Efficient, High Speed Data Communication** Advisor: Dr.Mrigank Sharad Explored various topologies like cascade, feedback and inductive peaking for a transmitter-receiver circuit for High Speed, Energy Efficient Communication.
May 2016 - July 2016	**VLSI Summer School, IIT Kharagpur** Advisor: Dr.Mrigank Sharad RTL Design for hamming Distance based pattern matching using Synopsys Design and IC Compiler. Design of low noise amplifier for biomedical frontend, involving capacitive feedback, active common-mode feedback using Cadence Virtuoso along with noise and stability analysis. Analysis and design of various RFIC components like VCO, PLL, Mixer and Power Amplifier.
October 2016 - November 2016	**Recolorization of Greyscale Images using Convolutional Neural Networks** Academic Project Developed a novel Convolutional Neural Network architecture inspired by VGG-16 for recolorization of greyscale images on TensorFlow.
December 2014 - March 2016	**i-Bike: Autonomous Bicycle with Dual Modes of Navigation** Developed a mathematical model of the bicycle control system. Designed and optimised the embedded architecture based on AVR and ARM microcontrollers for improved battery life. Explored various algorithms for path planning and sensors for obstacle detection and avoidance.

Achievements

Scholarships	○ Georgia Tech ECE Fellowship ○ Kishore Vaigyanik Protsahan Yojna (Young Scientist Award), 2013
Awards	○ Received the **Order of Merit** at IIT KGP for distinguished performance in the field of Technology ○ Member of the **Gold** winning Product Exhibition team at the 5th inter IIT Tech Meet ○ Member of the **Bronze** winning Human Computer Interface team at the 5th inter IIT Tech Meet ○ Member of the **Bronze** winning team in FIRA MiroSot 2015 held at Daejeon, South Korea ○ **Contingent Head** of the first Indian Team to qualify for RoboCup 2017 held at Nagoya, Japan ○ Member of the **Gold** winning team in KPIT Sparkle 2015 - an inter collegiate innovation challenge ○ Member of the **Gold** winning team in intra collegiate Hardware Modelling 2015 ○ Won **Bronze** in IEEE Hardware hackathon for a smart walking aid for the visually challenged
Scholastic Achievements	○ Ranked among the top 0.1% students in IIT-Joint Entrance Examination among 485,000 students ○ Ranked in top 0.1% in Royal Australian Chemical Quiz in 2011 and 2012

Relevant Courses

- ○ Computational Neuroscience
- ○ Digital VLSI Circuits
- ○ Digital Signal Processing
- ○ Architectural Design of ICs
- ○ Machine Learning
- ○ Artificial Intelligence
- ○ Computer Architecture
- ○ Design of Algorithms
- ○ Information Theory
- ○ Analog VLSI Circuits
- ○ VLSI Engineering
- ○ Semiconductor Devices

Technical Competencies

Environments	Xilinx ISE, Cadence Virtuoso, Synopsys Design and IC Compiler, Proteus, Eagle, TensorFlow, Linux Kernel, Git
Languages	MATLAB, C, AVR-C, C++, C#, python, Shell

Interests and Activities

- ○ Mentored a group of 20 students for a 7 day IEEE certified workshop leading to the design of an autonomous target finding turret
- ○ Director, IIT KGP Model United Nations 2015 and Member of the IIT Kharagpur Debating Society
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