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Work done till now:

1. learned Roth's 5 valued algebra and D algorithm to finding test vector generation for combinational circuits.
2. Implemented Fanin and Fanout list for representing the circuit.
3. Contributed to path finding step from given node to one of the outputs.

Work to be done:

1. contribute to implement back tracing in combinational circuit after applying propagation step(which is the toughest step in our project).
2. Comparing output of D algorithm with Output of SAT solver which is inbuilt in pyEDA
3. Optimizing D-Algorithm and apply PODEM if possible.