

**Subho S. Banerjee, Saurabh Jha,  
Zbigniew Kalbarczyk, Ravishankar K. Iyer**

# BayesPerf: Minimizing Performance Monitoring Errors Using Bayesian Statistics

ASPLOS 2021

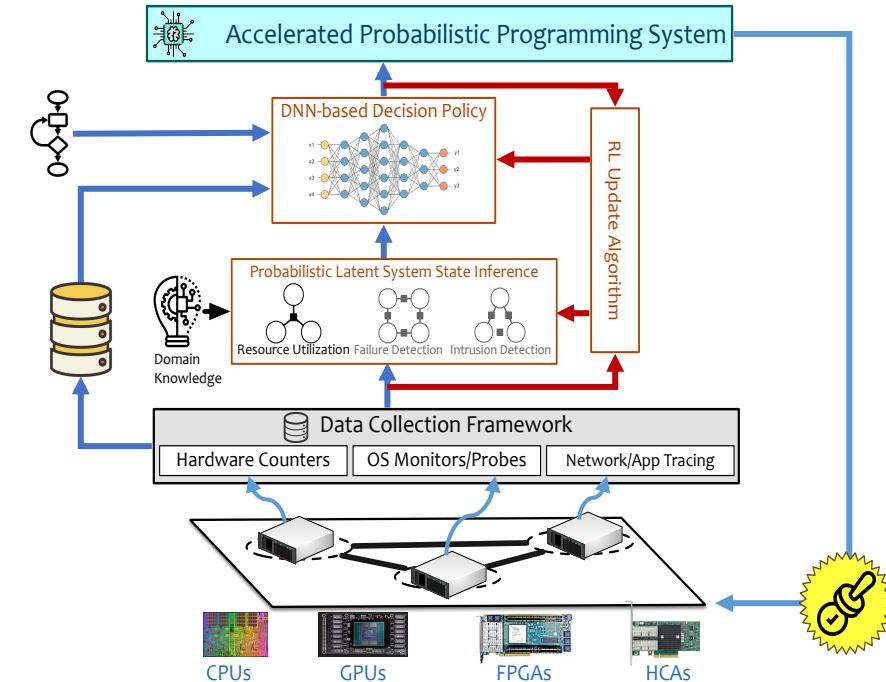


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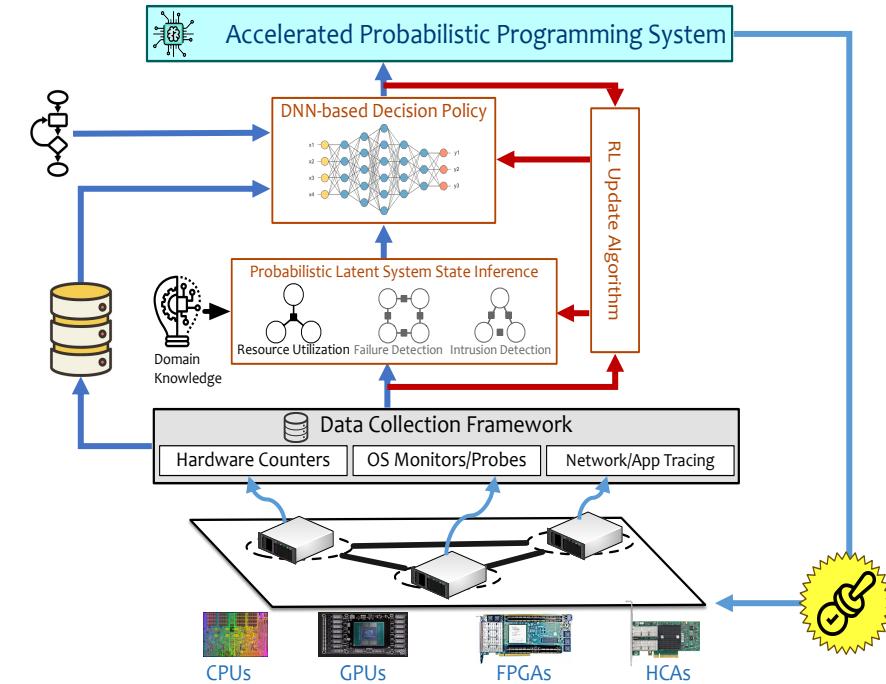
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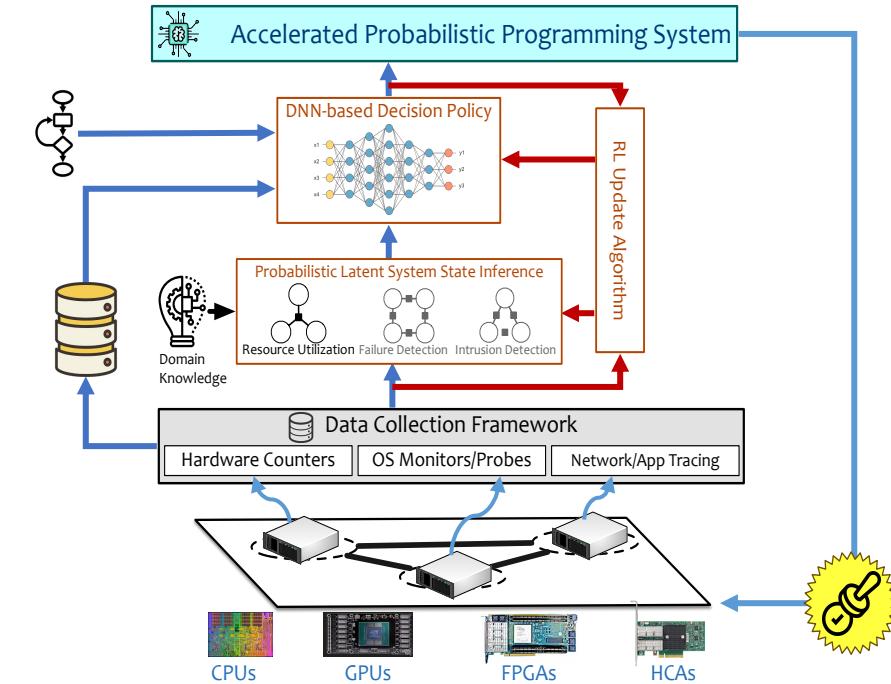
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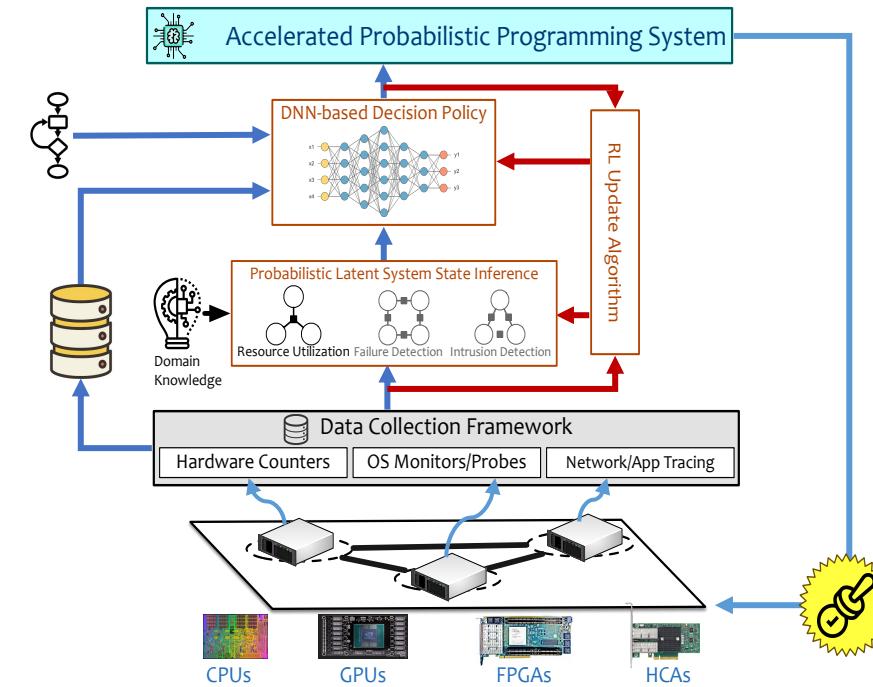


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**BayesPerf: A system to quantify and minimize errors HPCs**

- Bayesian generative model of HPC error process
- System implementation for Linux on x86 and ppc64 CPUs



# Hardware Performance Counter Primer

Counters used in **Polling Mode**

```
ReadCounter(&start);  
  
/* Sum two arrays */  
for(i = 0; i < len; i++)  
    z[i] = x[i] + y[i];  
  
ReadCounter(&end);
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Counted Events = End - Start

- Time
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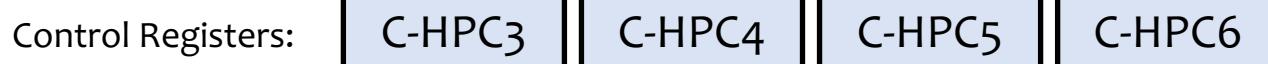
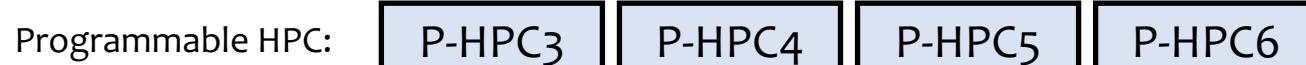
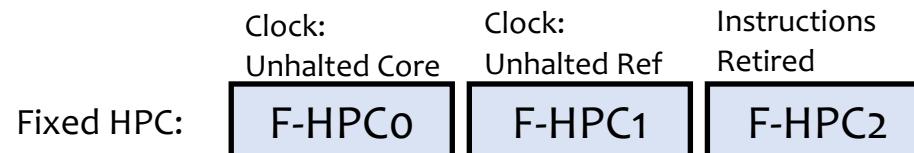
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Fixed HPC:	F-HPC0	F-HPC1	F-HPC2
Programmable HPC:	P-HPC3	P-HPC4	P-HPC5
Control Registers:	C-HPC3	C-HPC4	C-HPC5

} Read counters on x86 processors  
rdmsr, rdpmc, rdtsc, rdtscp

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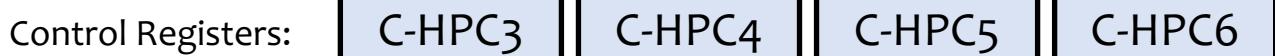
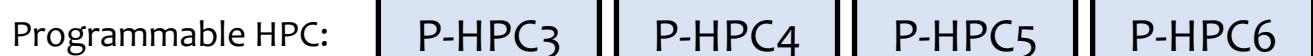
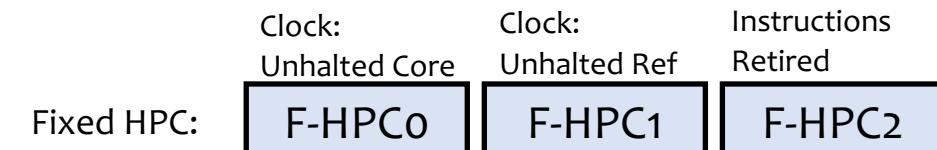
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Counters used in **Sampling Mode**

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ReadCounter1(&start1);
ReadCounter2(&start2);
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/* Sum two arrays */
for(i = 0; i < len; i++) {
    z[i] = x[i] + y[i];
    if (i%2) SwapCounters()
}
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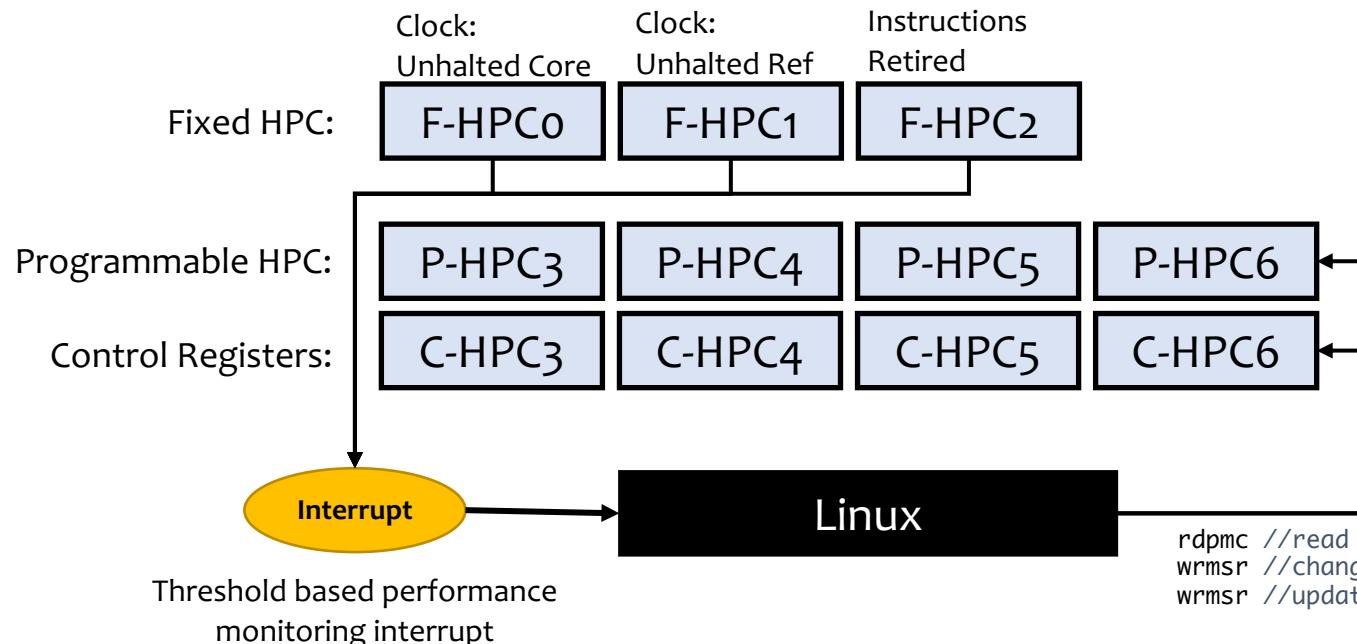
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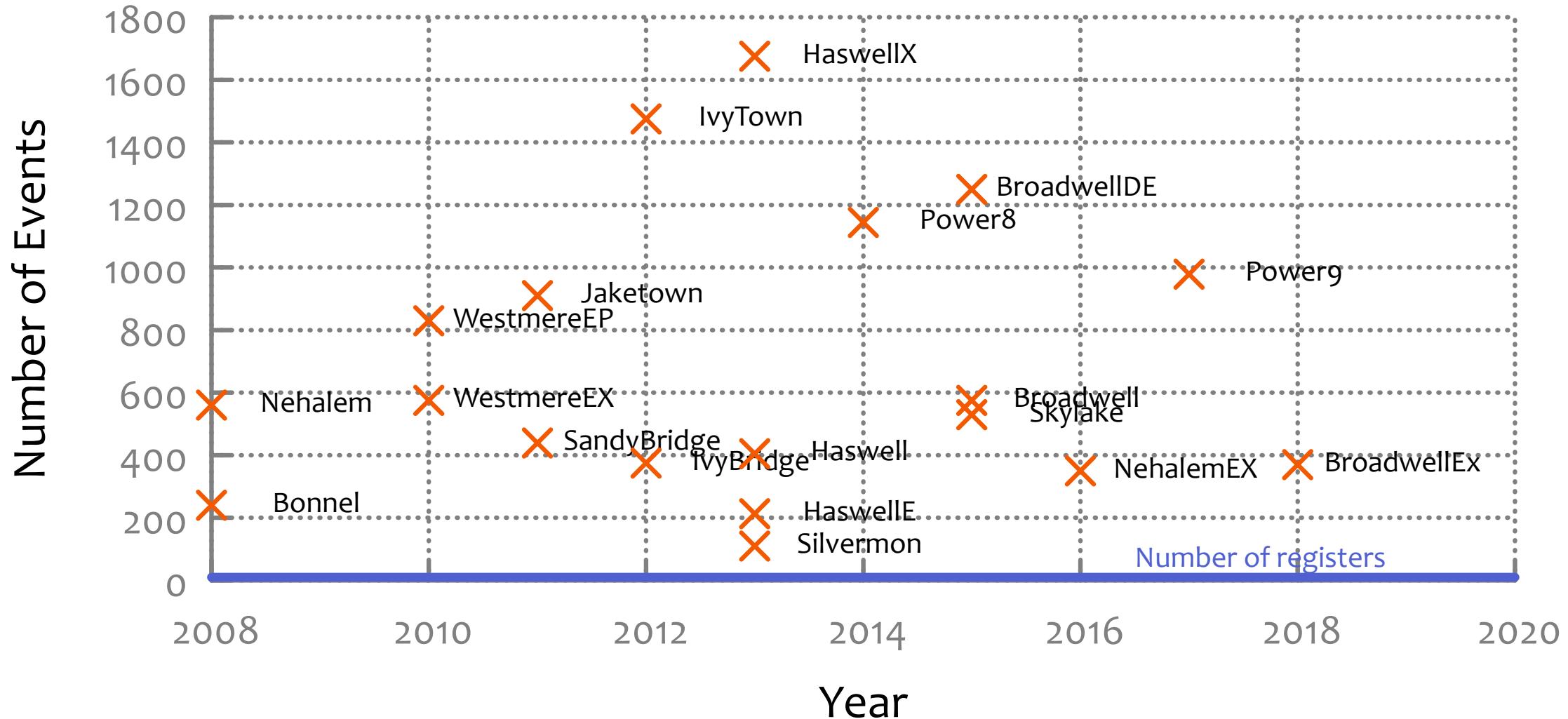
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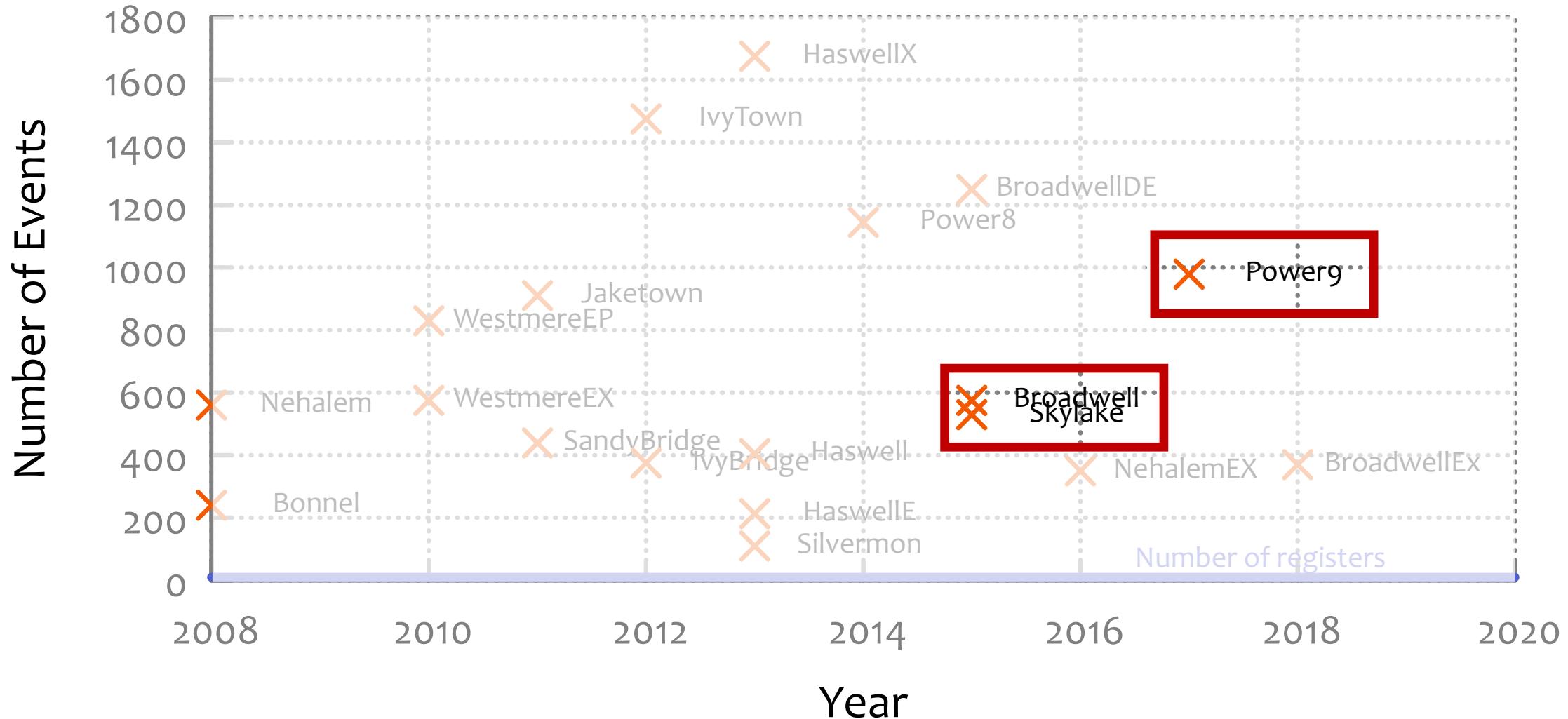
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rdpmc //read old event  
wrmsr //change counter  
wrmsr //update old event

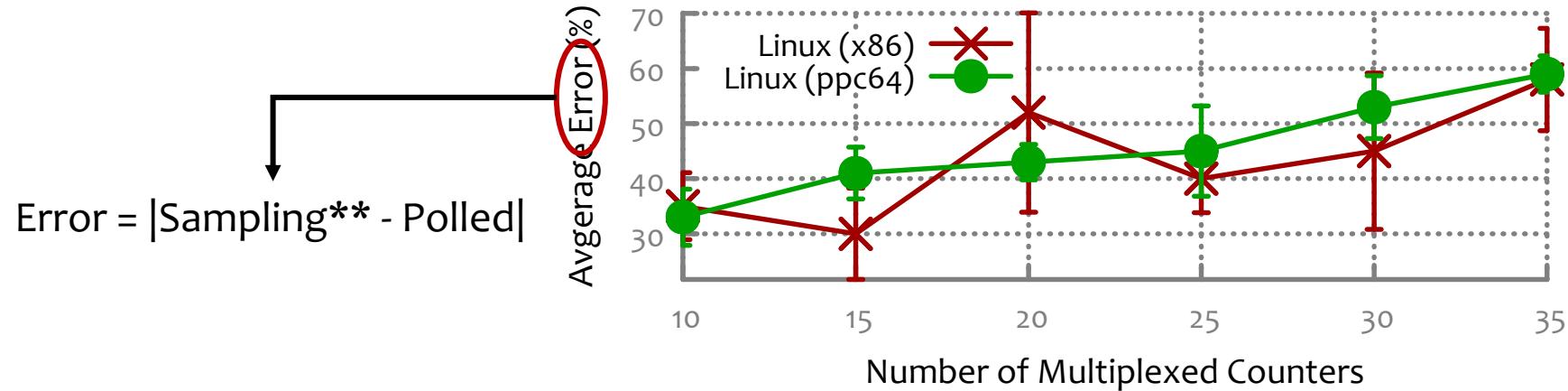
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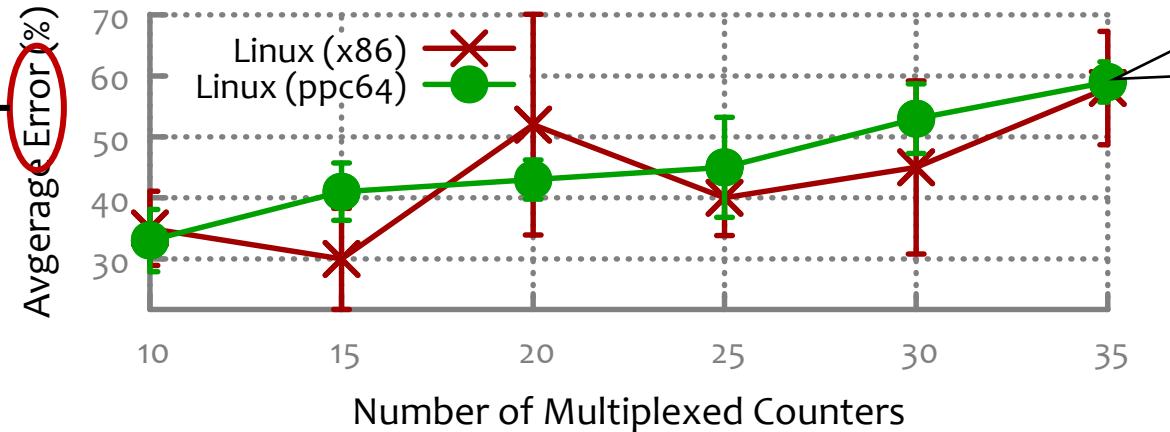


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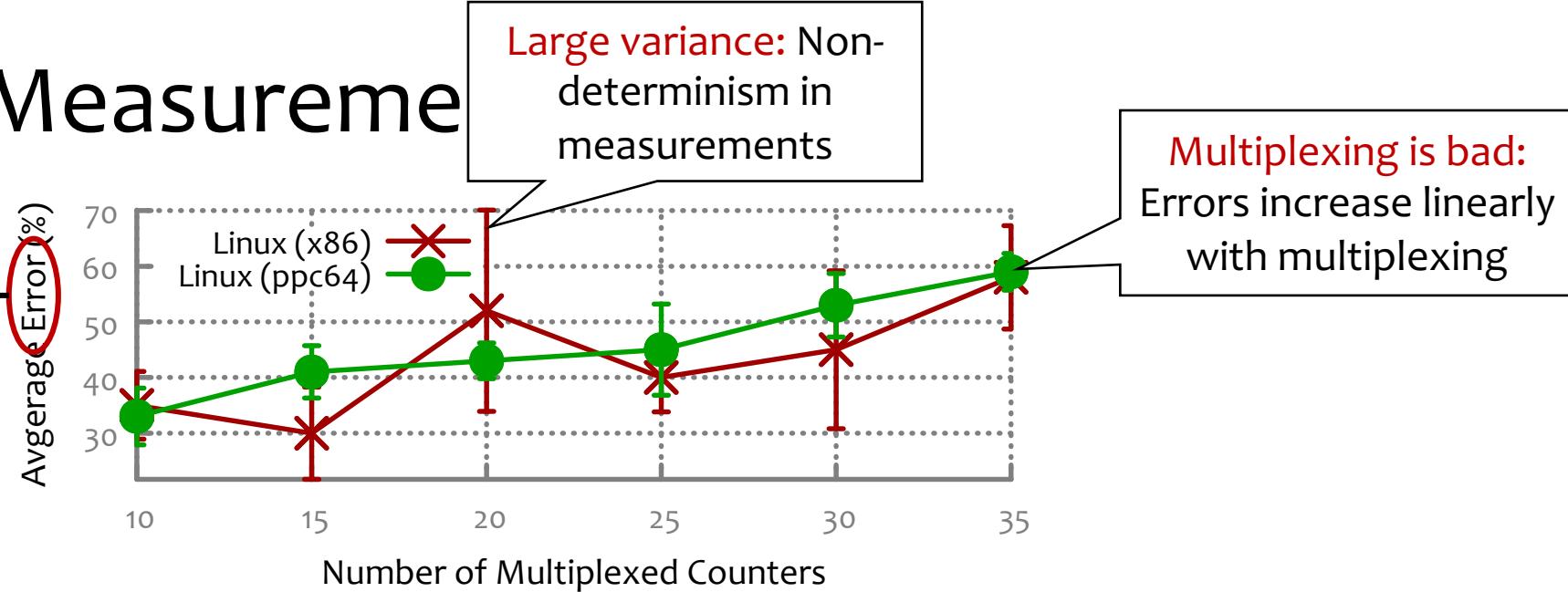
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Errors increase linearly  
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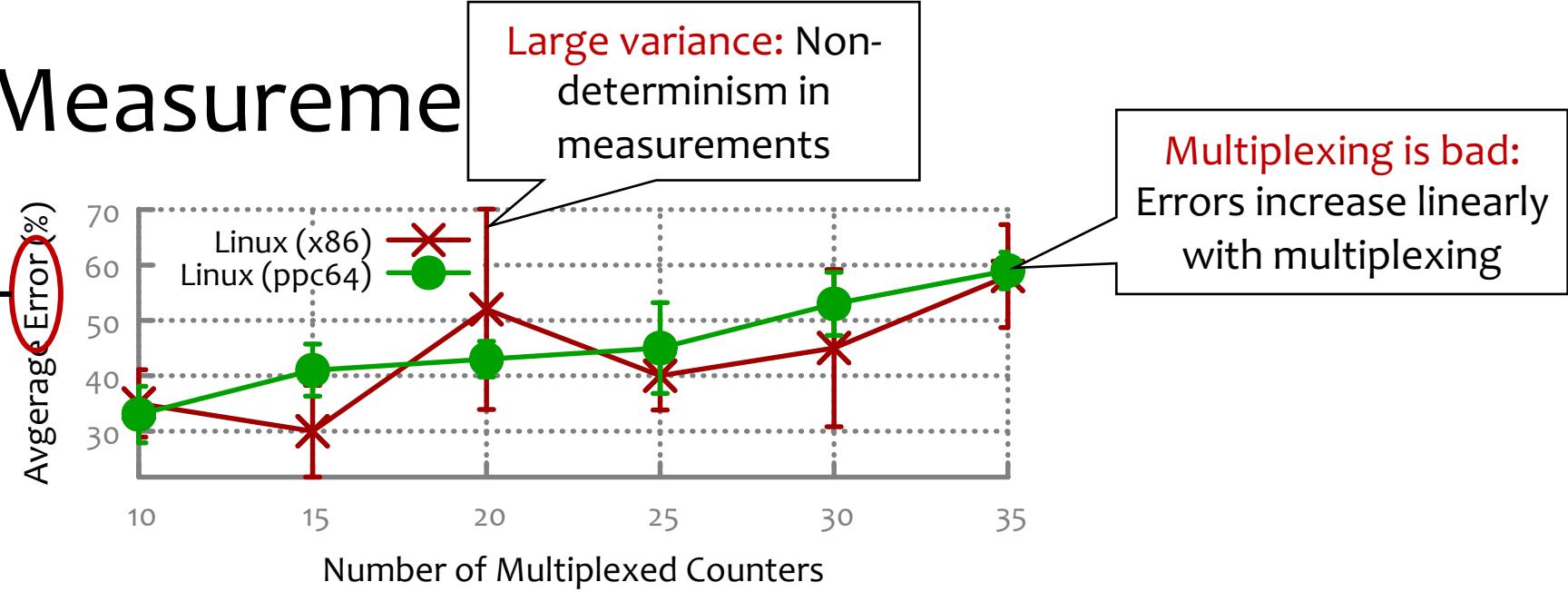


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  - Order in which interrupts are served
  - Dropped measurements: Backpressure in ring-buffers between kernel and userspace
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**Large variance:** Non-determinism in measurements

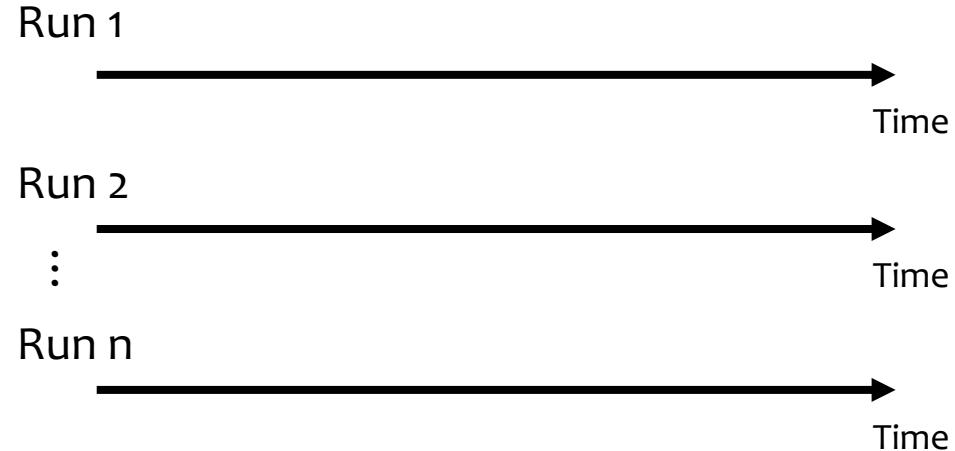
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- (Instruction Pointer) Skid
  - Instruction level parallelism: Counters change between time interrupt enters processor pipeline and the interrupt handler is triggered
- CPU Design/Implementation Bug

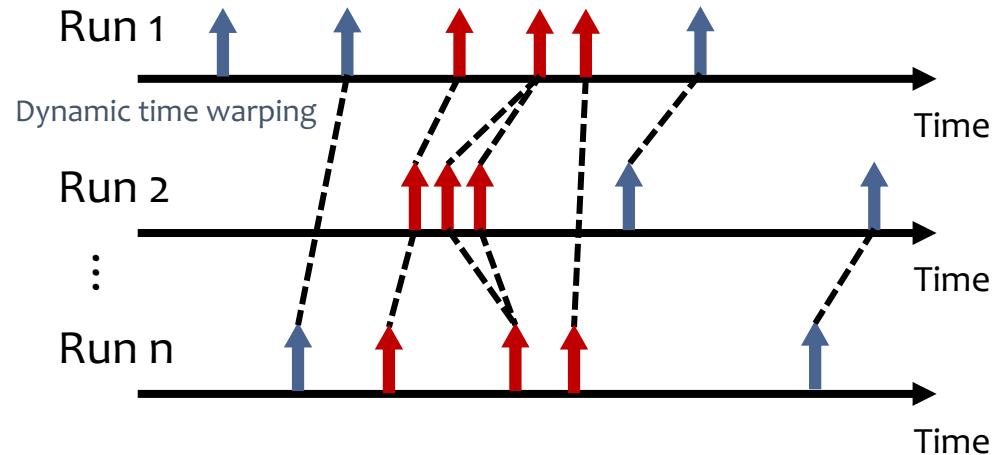
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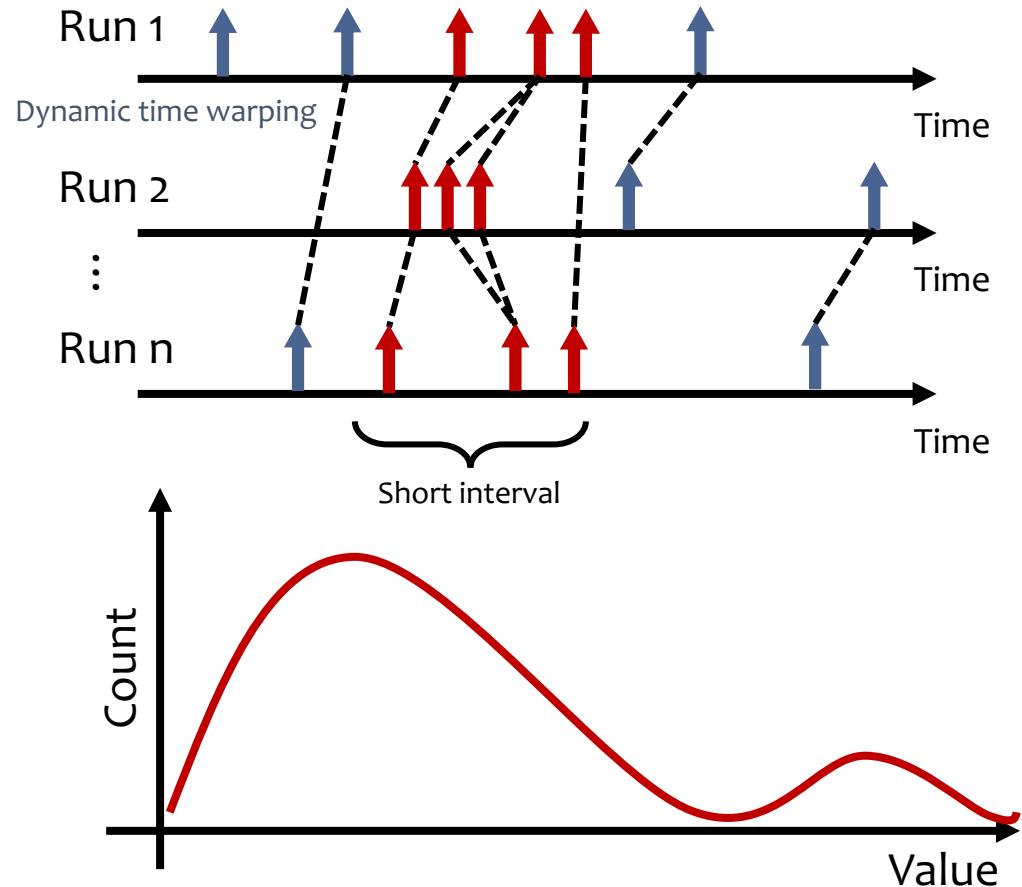
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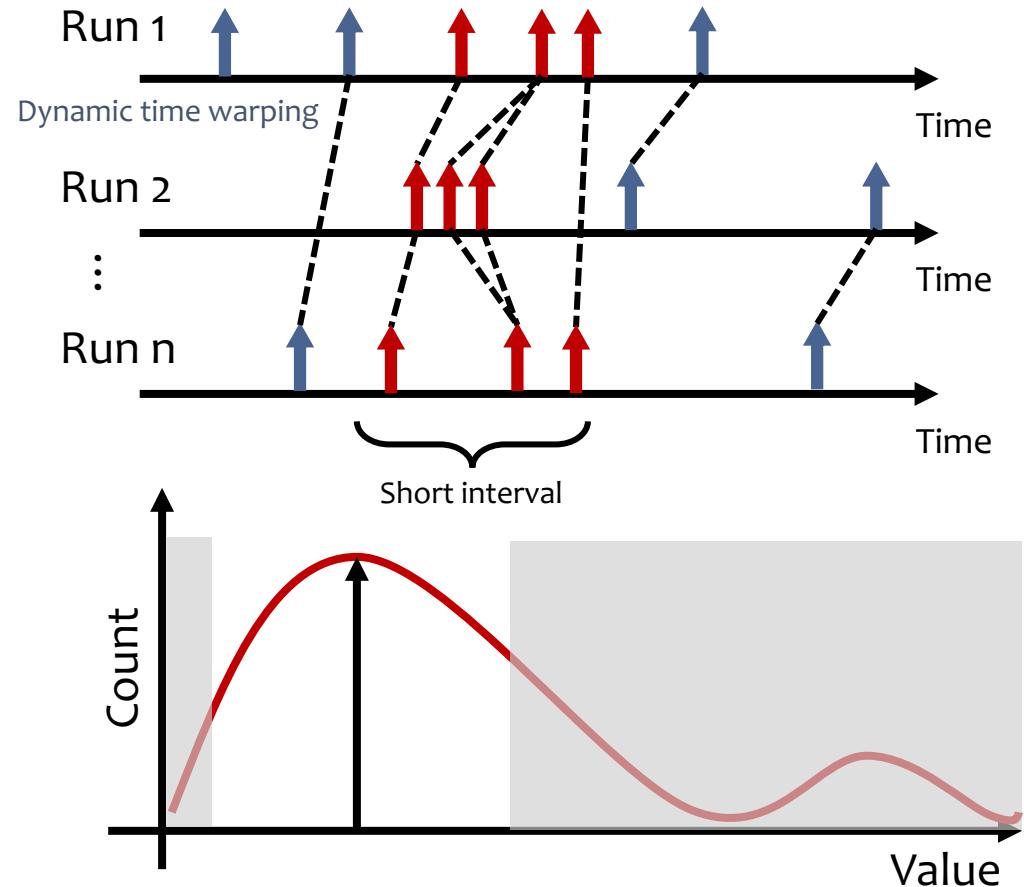
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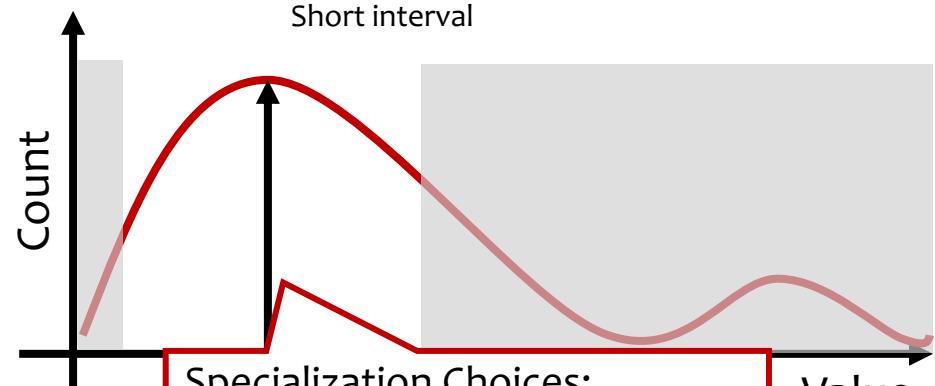
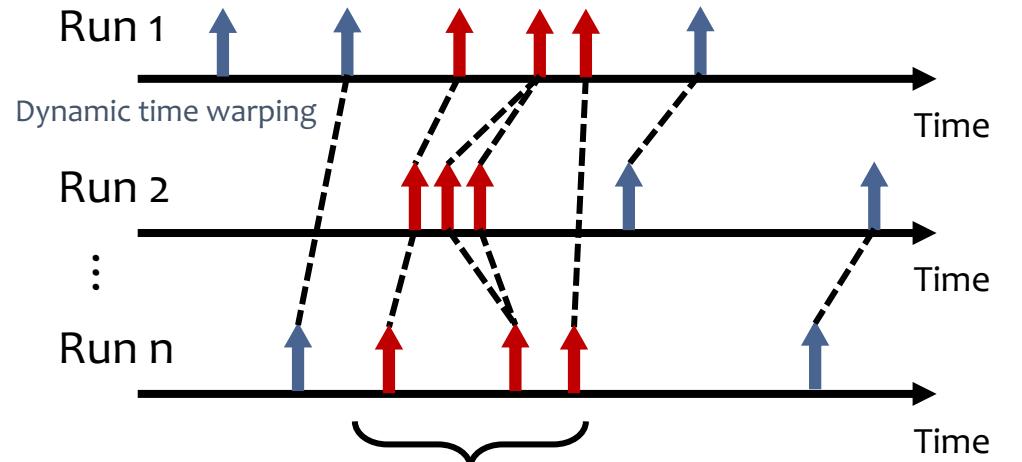
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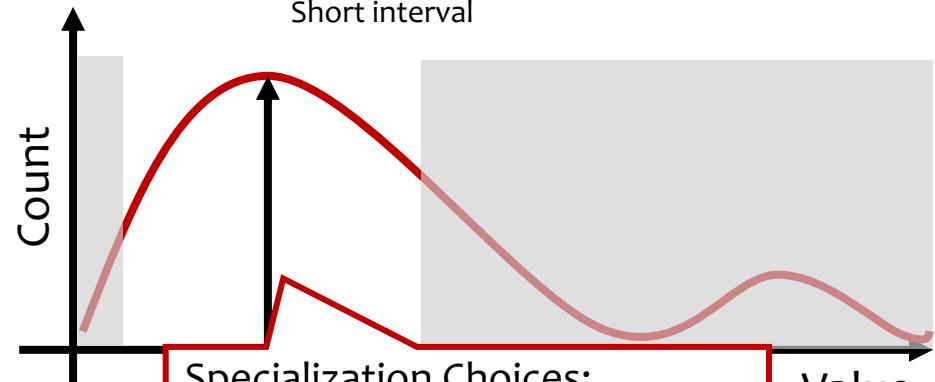
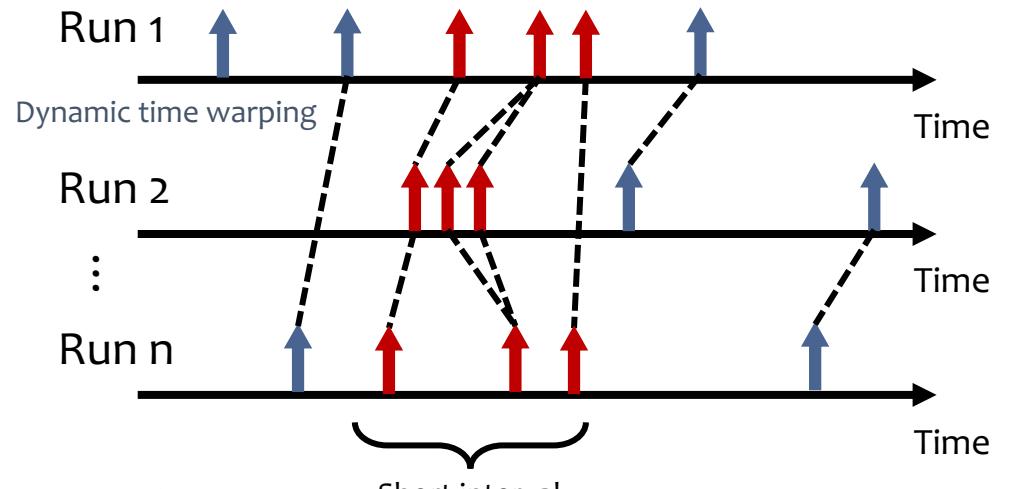


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  - Shape of curve
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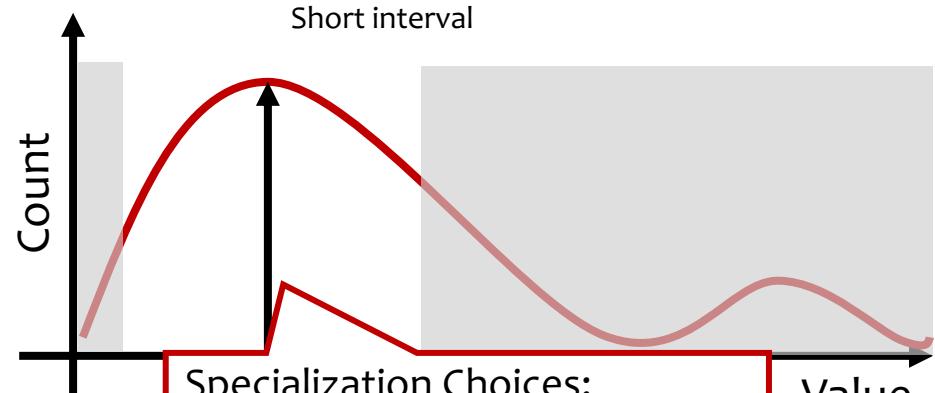
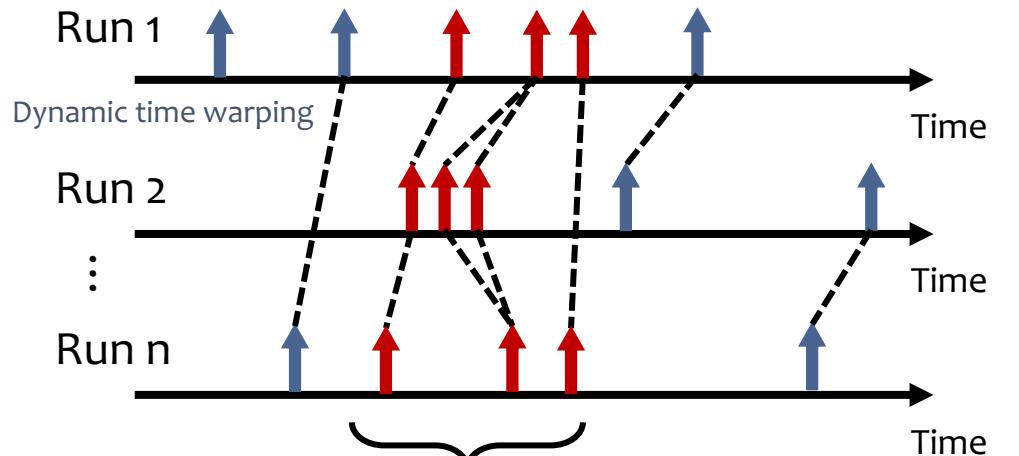
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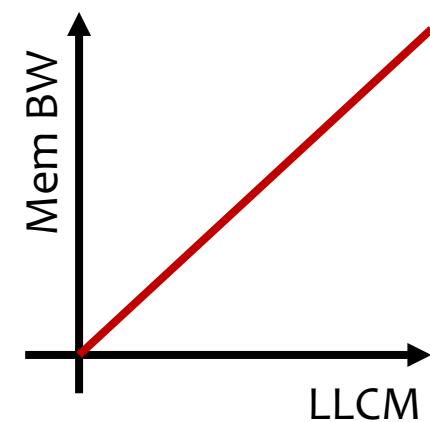
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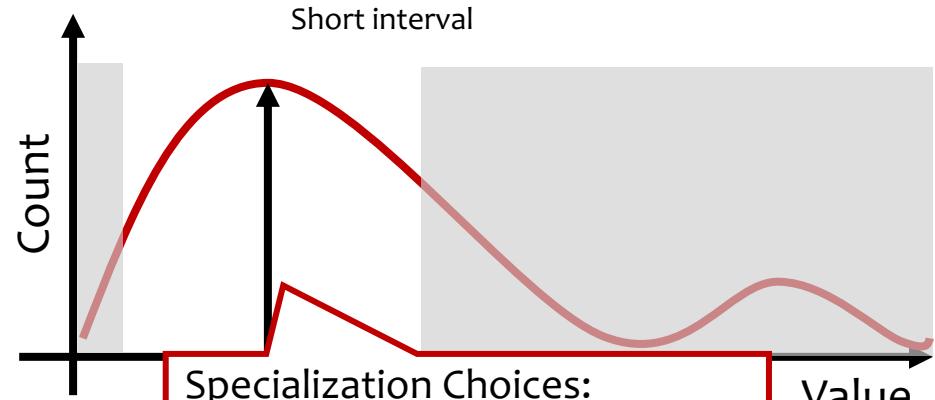
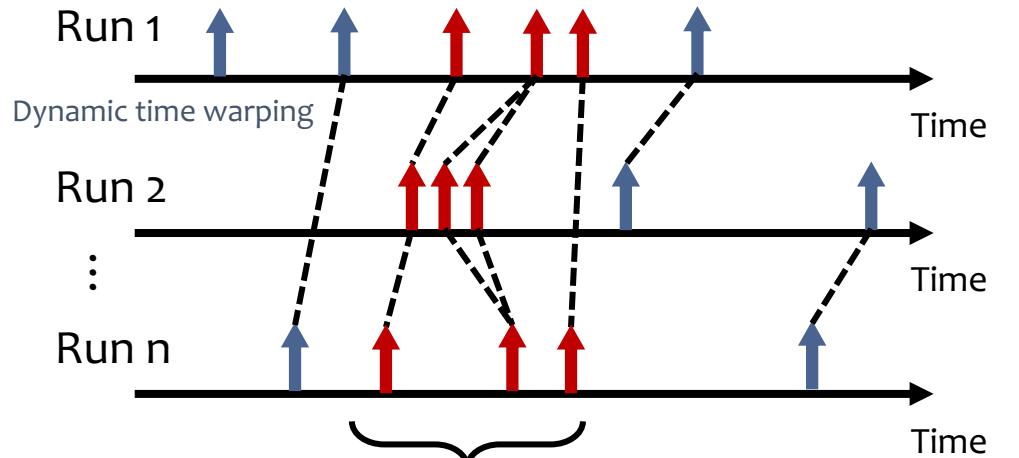
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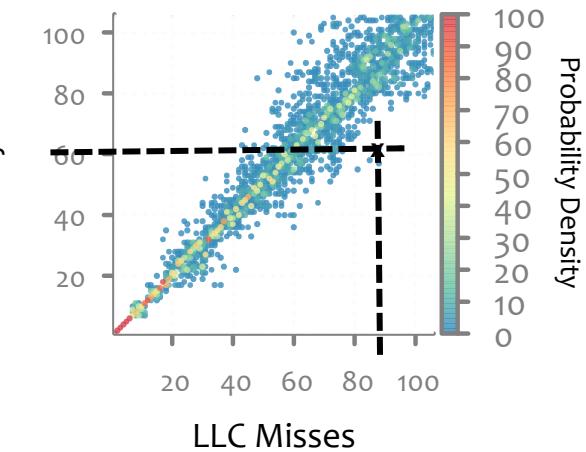
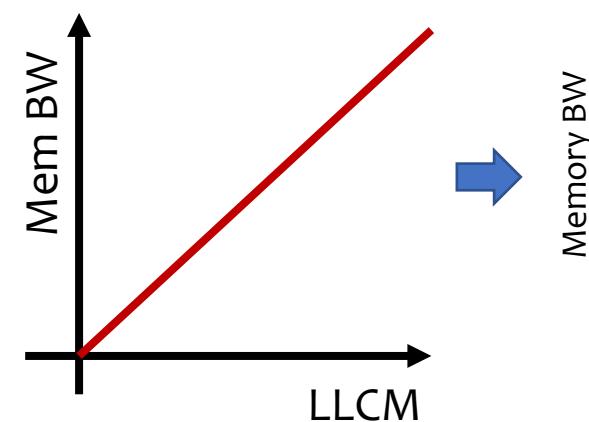
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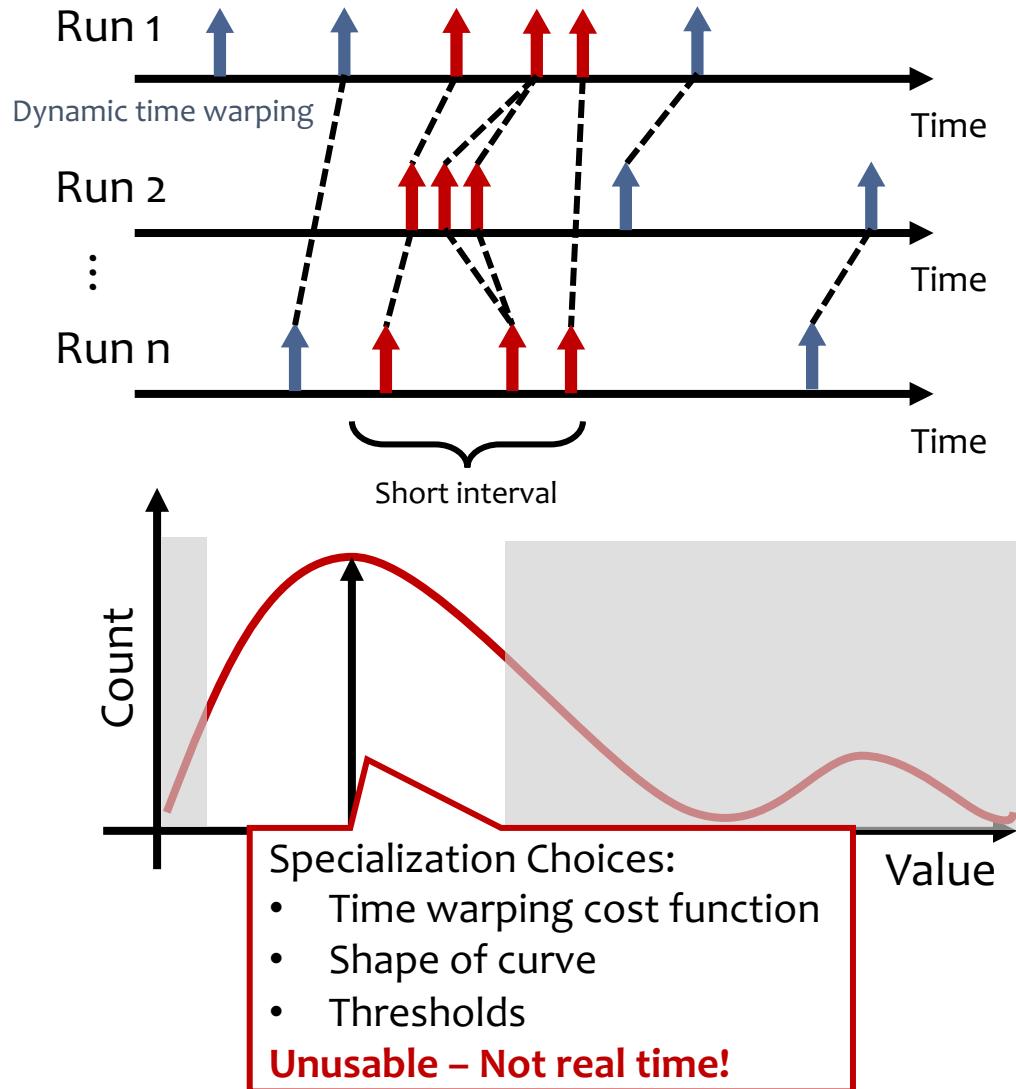
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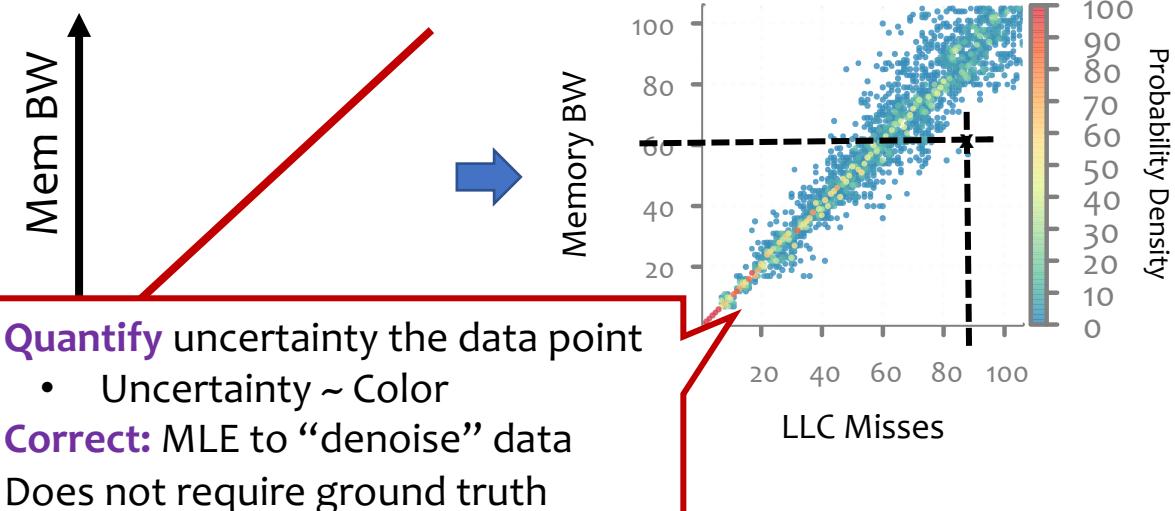


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Noisy values of HPCs  
Measured

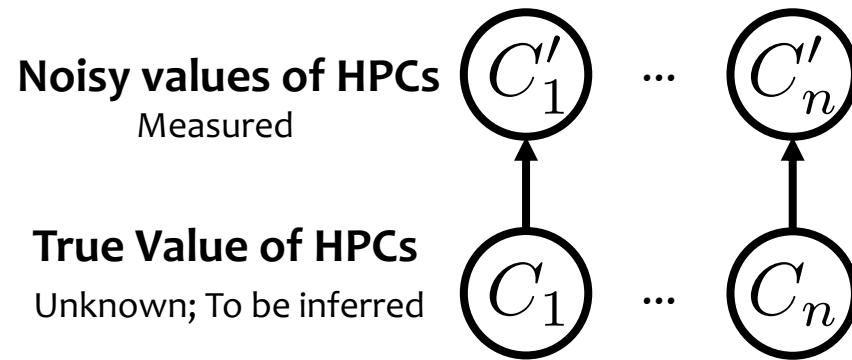


The diagram shows a sequence of noisy measured values. It consists of two rows of circles. The top row contains three circles with the labels  $C'_1$ ,  $\dots$ , and  $C'_n$  respectively. The bottom row contains three corresponding circles, each slightly offset to the right of its counterpart in the top row.

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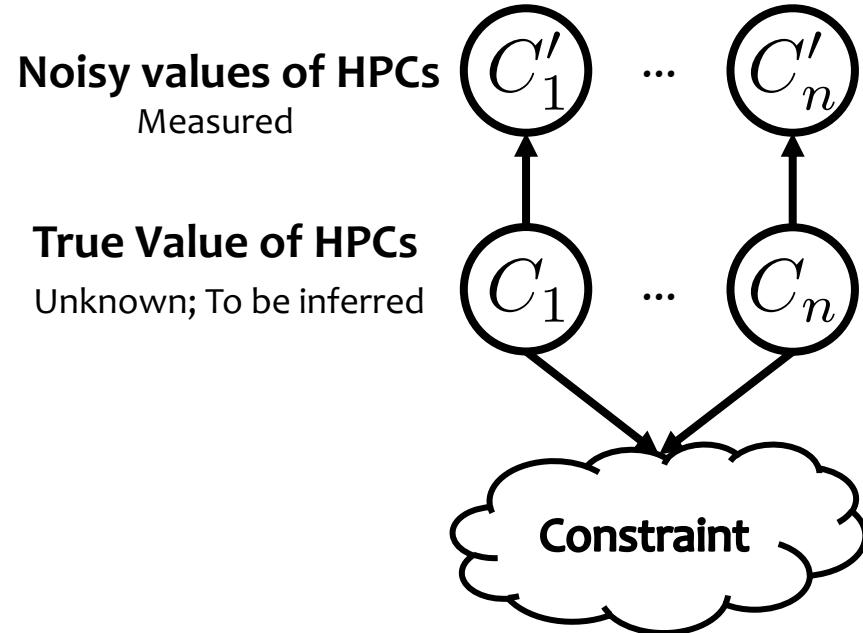
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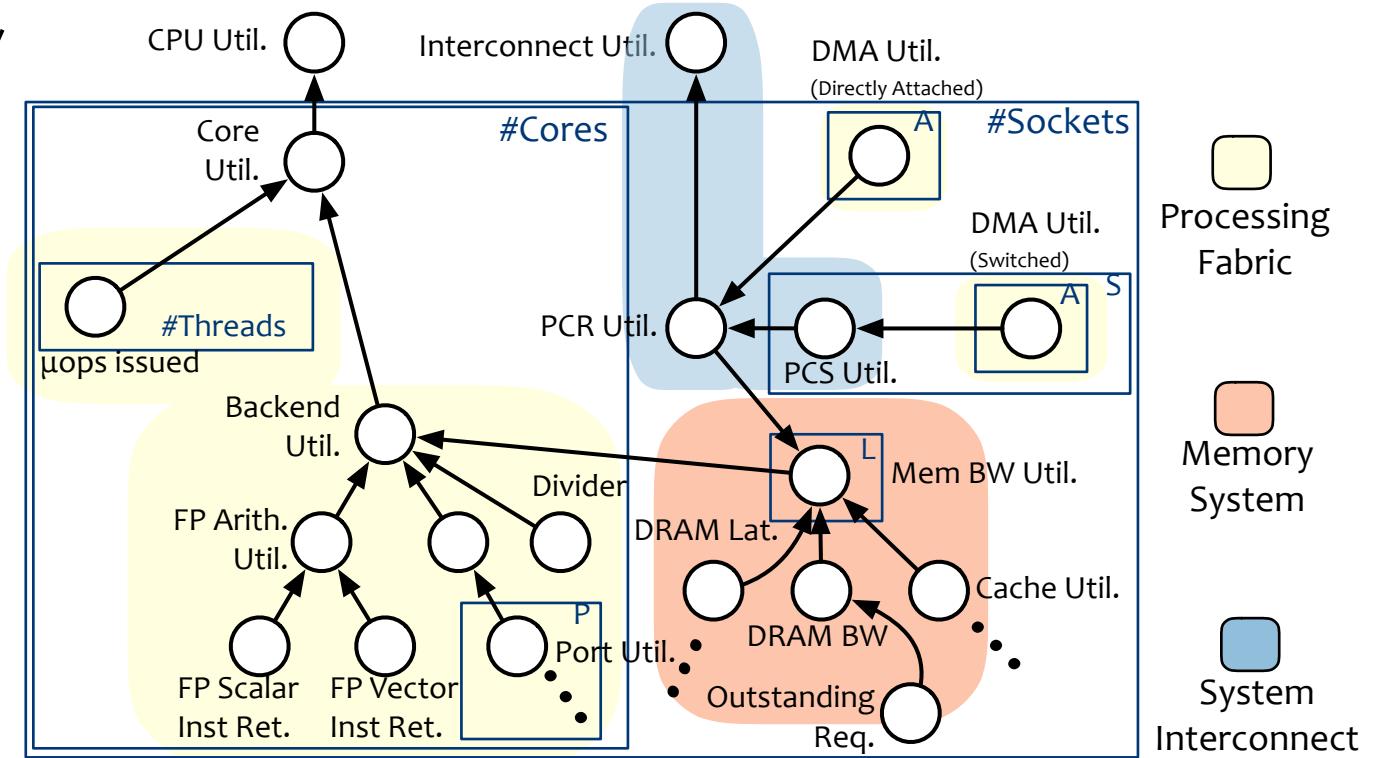
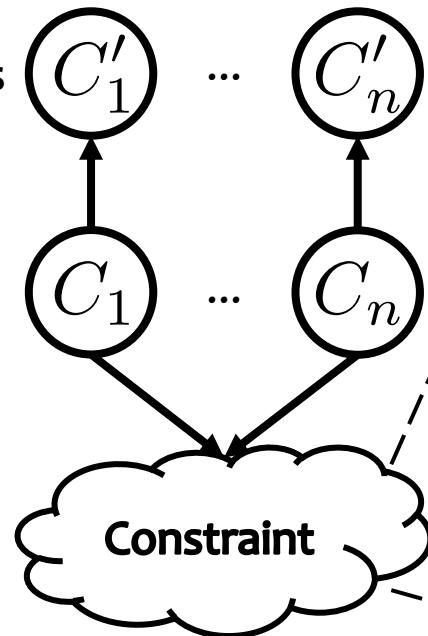
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**Noisy values of HPCs**  
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**True Value of HPCs**  
Unknown; To be inferred



Processing Fabric

Memory System

System Interconnect

- Scalable, general & works for real processors
  - x86 (Intel), ppc64 (IBM)
  - Based on Intel's “Top-Down Microarchitectural Analysis” in VTune
- Parse BN automatically from per μ-arch listing in Linux Source Tree
  - Contributed by vendors to Linux

# Dynamic BayesPerf: Scheduling Counters

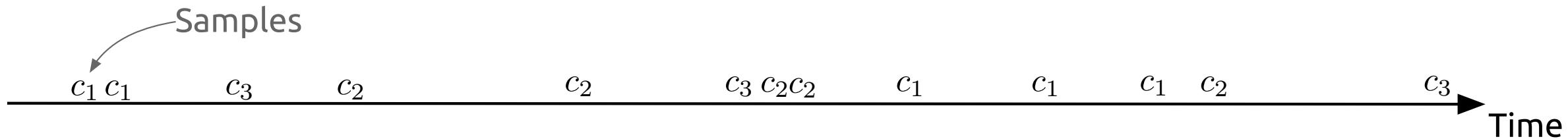
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Hypothetical example: Measure events  $\{e_a, e_b, e_c, e_d, e_e, e_f\}$  on counters  $\{c_1, c_2, c_3\}$

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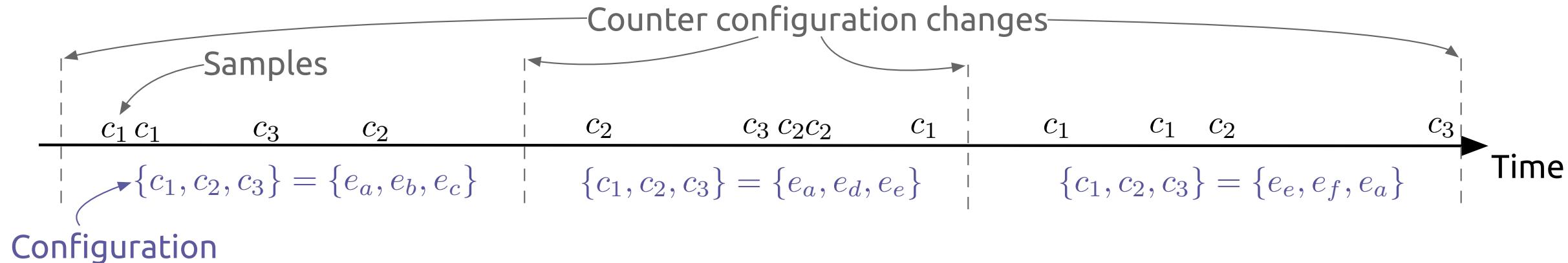
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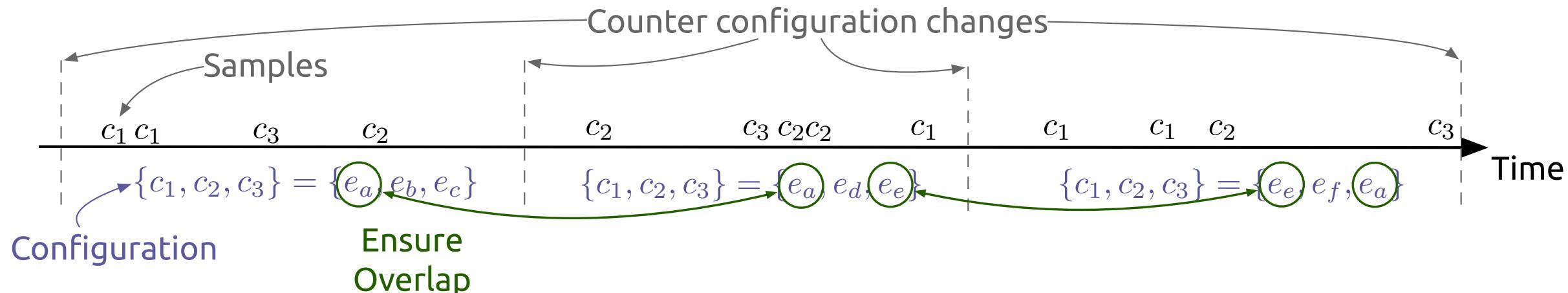
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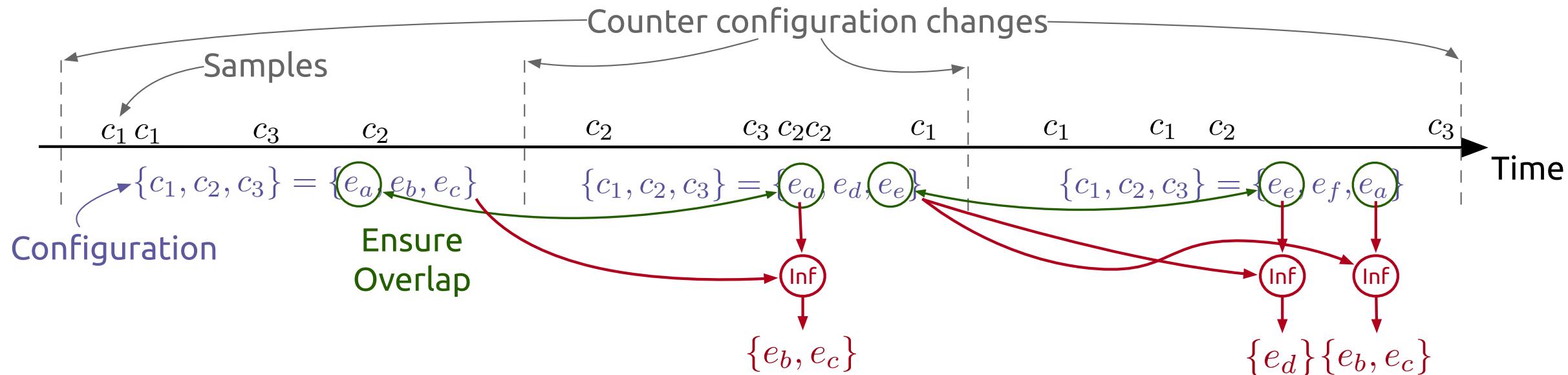
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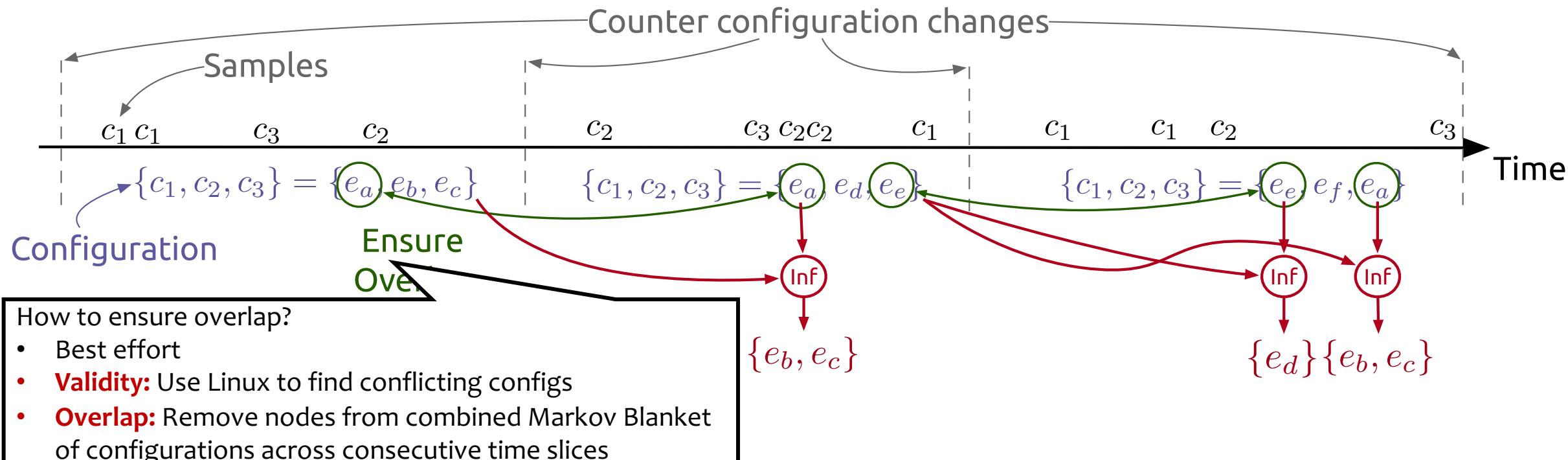


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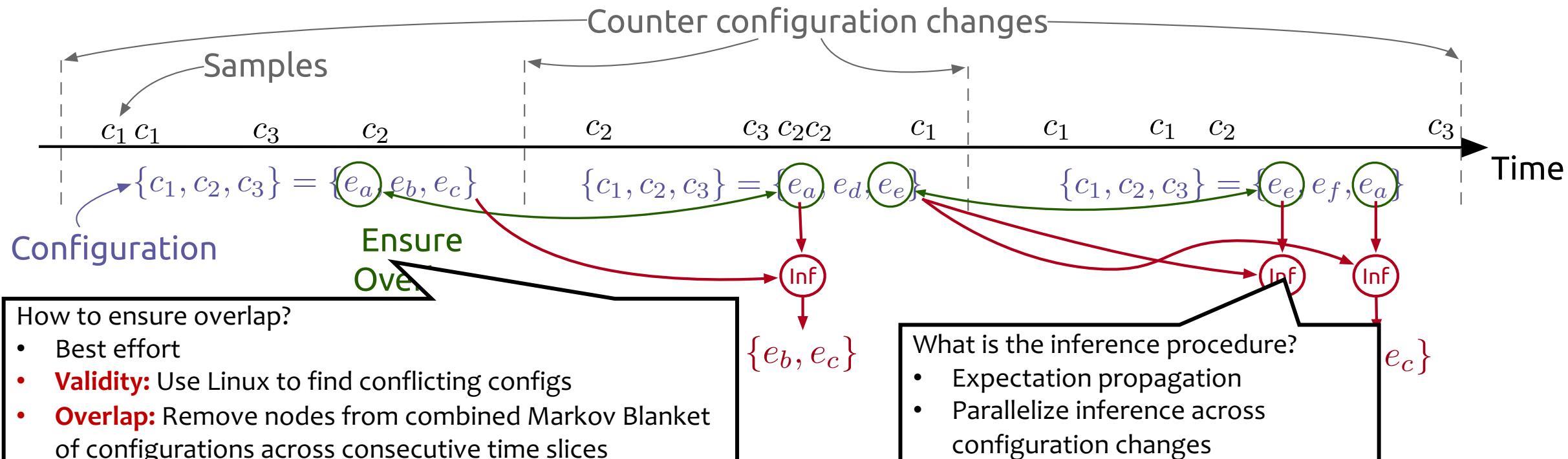


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- In general: BayesPerf can be trained with representative workload set
  - Train BayesPerf model using backpropagation – [ICML 2020]
  - What if error model is not Student-t? – DNNs

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**Inductive-bias-driven Reinforcement Learning for Efficient Schedules in Heterogeneous Clusters**

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Subho S. Banerjee<sup>1</sup> Saurabh Jha<sup>1</sup> Zbigniew T. Kalbarczyk<sup>1</sup> Ravishankar K. Iyer<sup>1</sup>

**Abstract**

The problem of scheduling of workloads onto heterogeneous processors (e.g., CPUs, GPUs, FPGAs) is of fundamental importance in modern data centers. Current system schedulers rely on application/system-specific heuristics that have to be built on a case-by-case basis. Recent work has demonstrated ML techniques for automating the heuristic search by using black-box approaches which require significant training data and time, which make them challenging to use in practice. This paper presents Symphony, a scheduling framework that addresses the challenge in two ways: (i) a domain-driven Bayesian reinforcement learning (RL) model for scheduling, which inherently models the resource dependencies identified from the system architecture; and (ii) a sampling-based technique to compute the gradients of a Bayesian model without performing full probabilistic inference. Together, these techniques reduce both the amount of training data and the time required to produce scheduling policies that significantly outperform black-box approaches by up to 2.2x.

**1. Introduction**

The problem of scheduling of workloads on heterogeneous processing fabrics (i.e., accelerated datacenters including GPUs, FPGAs, and ASICs, e.g., Asanović (2014); Shaw & Brooks (2015)), is at its core an intractable NP-hard problem (Mastrolilli & Svensson, 2008, 2009). System schedulers generally rely on application- and system-specific heuristics with extensive domain-expert-driven tuning of scheduling policies (e.g., Isard et al. (2009); Giceva et al. (2014); Lyerly et al. (2018); Mars et al. (2011); Mars & Tang (2013); Oosterhout et al. (2013); Xu et al. (2018); Yang et al. (2013); Zhang et al. (2014); Zhuravlev et al. (2010); Za-

<sup>1</sup>University of Illinois at Urbana-Champaign, USA. Correspondence to: Subho S. Banerjee [ssbaner2@illinois.edu](mailto:ssbaner2@illinois.edu).

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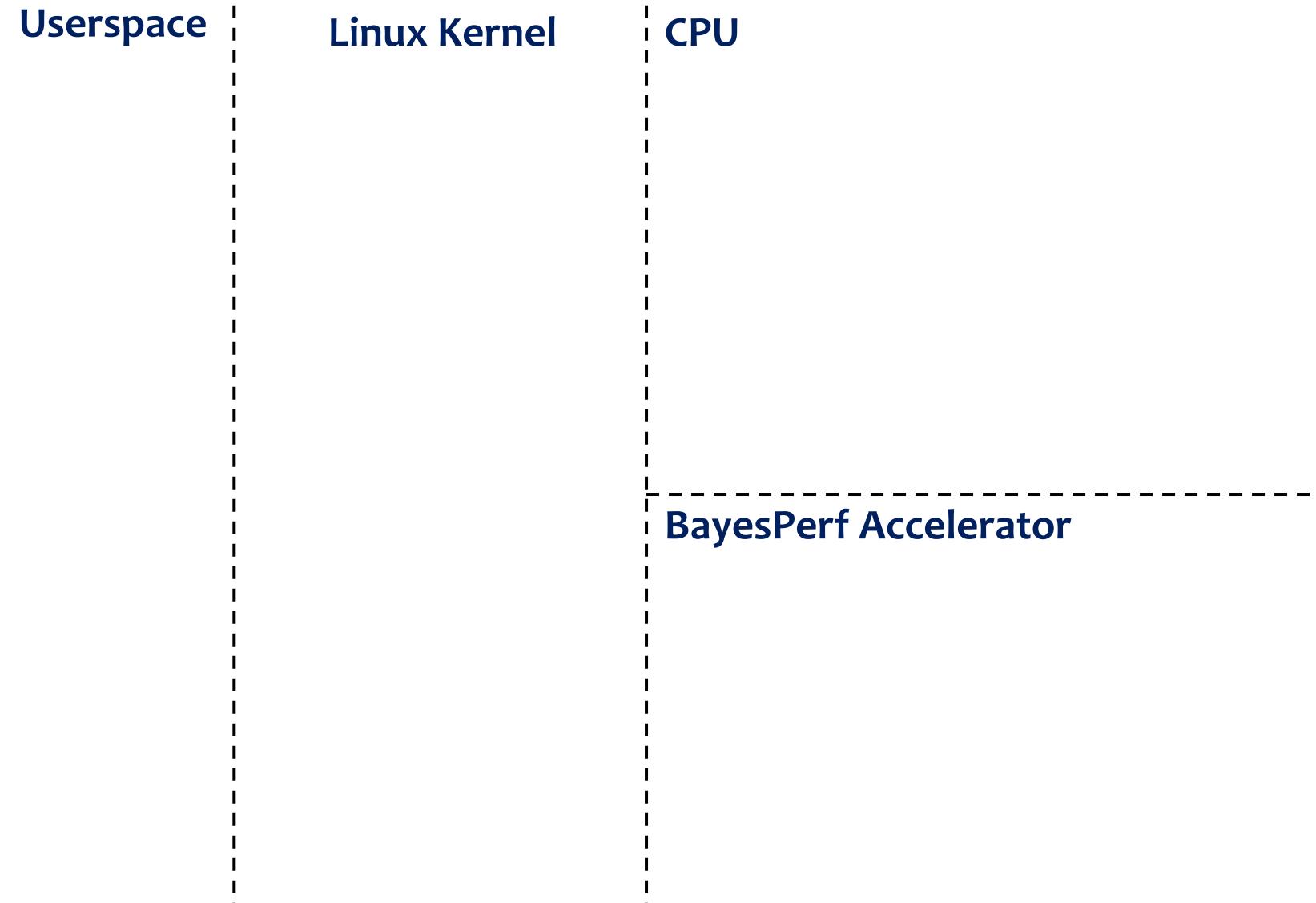
haria et al. (2010)). Such heuristics are difficult to generate, as variations across applications and system configurations mean that significant amounts of time and money must be spent in painstaking heuristic searches. Recent work has demonstrated machine learning (ML) techniques (Delimitrou & Kozyrakis, 2013; 2014; Mao et al., 2016; 2018) for automating heuristic searches by using black-box approaches which require significant training data and time, making them challenging to use in practice.

This paper presents Symphony, a scheduling framework that addresses the challenge in two ways: (i) we use a domain-guided Bayesian model-based partially observable Markov decision process (POMDP) (Astrom, 1965; Kaelbling et al., 1998) to decrease the amount of training data (i.e., sampled trajectories); and (ii) a sampling-based technique that allows one to compute the gradients of a Bayesian model without performing full probabilistic inference. We thus, significantly reduce the costs of (i) running a large heterogeneous computing system that uses an efficient scheduling policy; and (ii) training the policy itself.

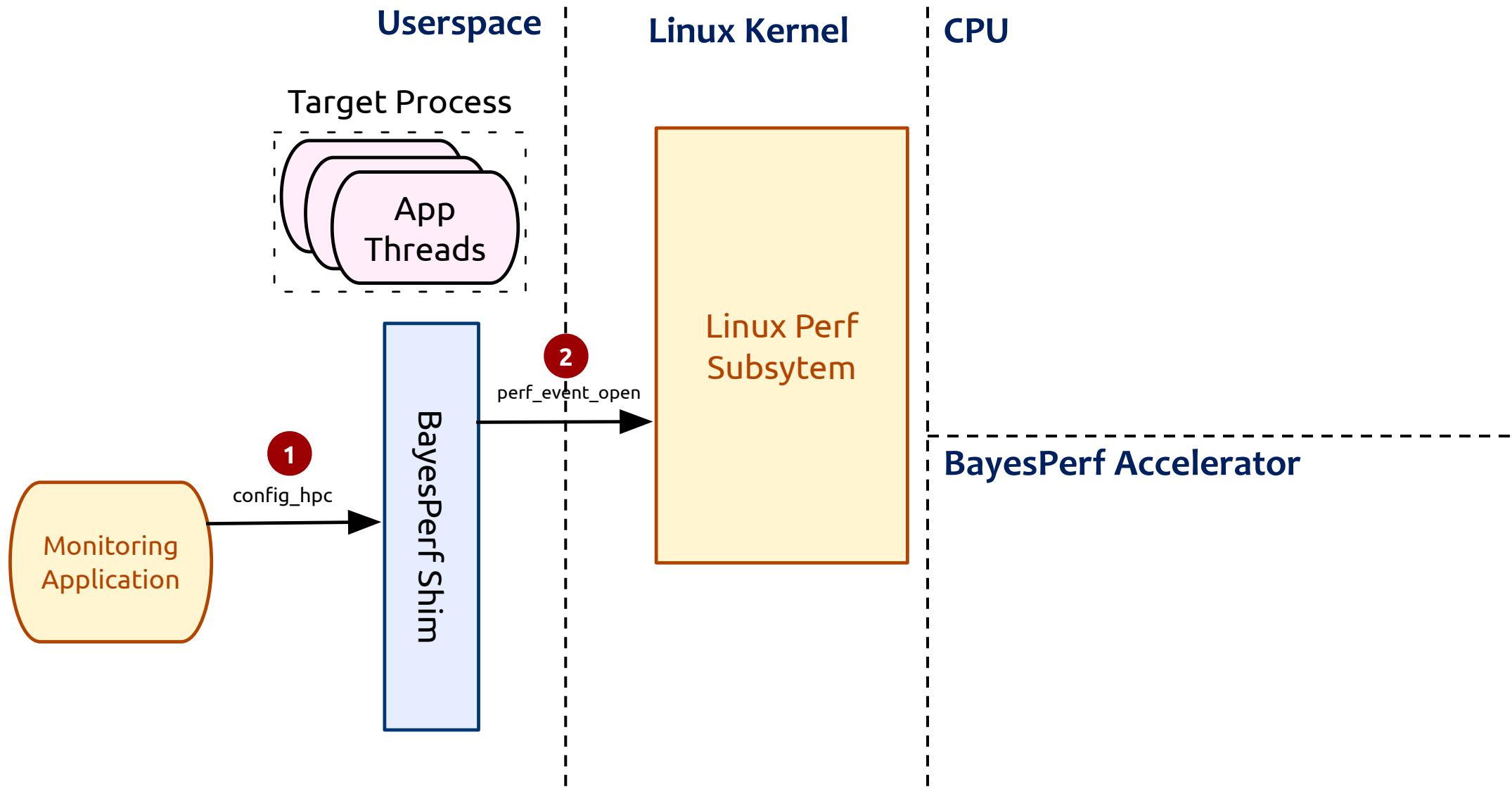
**Reducing Training Data.** State-of-the-art methods for choosing an optimal action in POMDPs rely on training of neural networks (NNs) (Mnih et al., 2016; Dharwal et al., 2017). As these approaches are model-free, training of the NN requires large quantities of data and time to compute meaningful policies. In contrast, we provide an inductive bias for the reinforcement learning (RL) agent by encoding domain knowledge as a Bayesian model that can infer the latent state from observations, while at the same time leveraging the scalability of deep learning methods through end-to-end gradient descent. In the case of scheduling, our inductive bias is a set of statistical relationships between measurements from microarchitectural monitors (Dreyer & Alpert, 1997). To the best of our knowledge, this is the first paper to exploit those relationships and measurements to infer resource utilization in the system (i.e., latent state) to build RL-based scheduling policies.

**Reducing Training Time.** The addition of the inductive bias, while making the training process less data-hungry (i.e., requiring fewer workload executions to train the model), comes at the cost of additional training time: the cost of performing full-Bayesian inference at every training step (Dagum & Luby, 1993; Russell et al., 1995; Binder

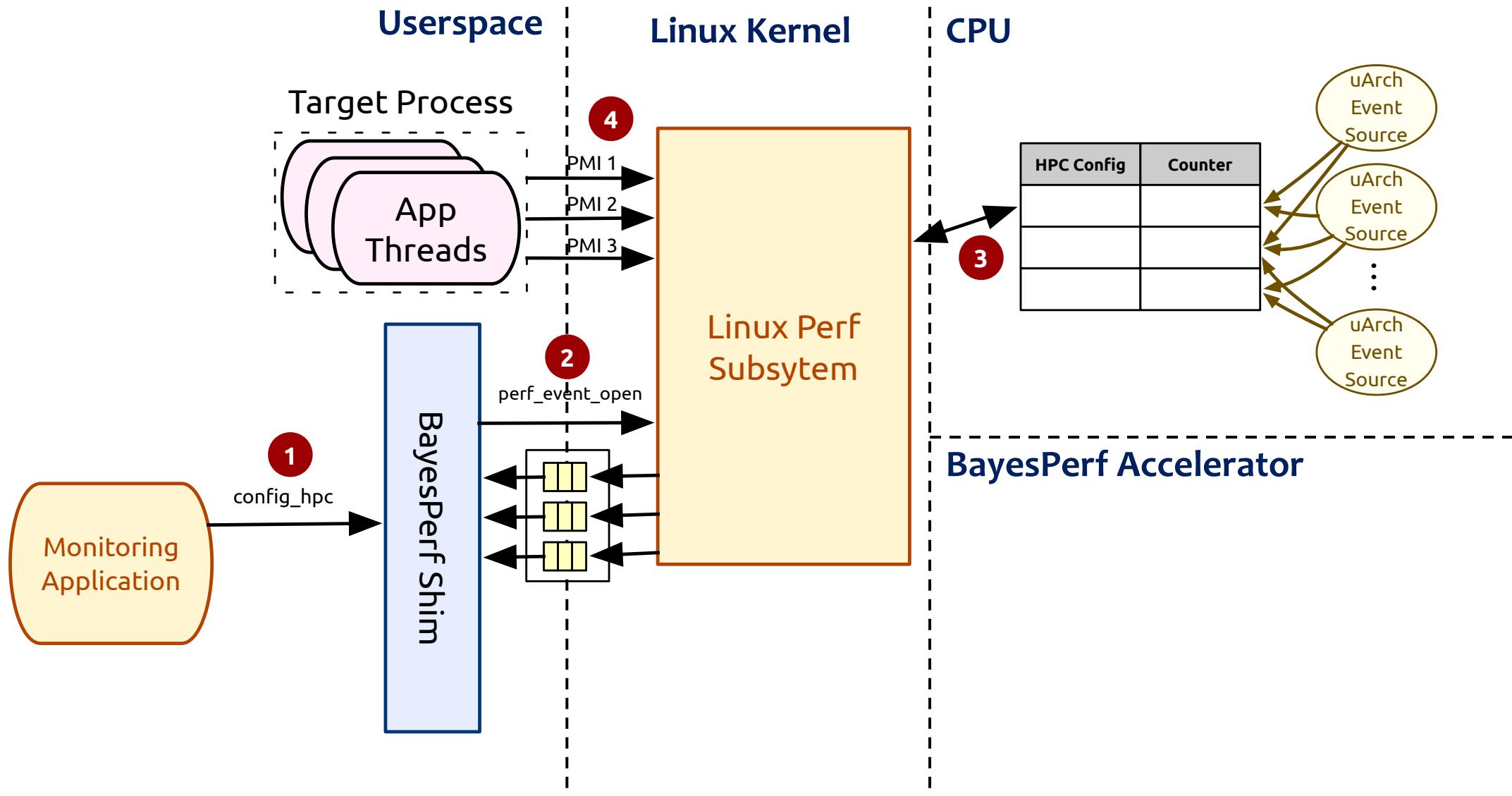
# The BayesPerf System



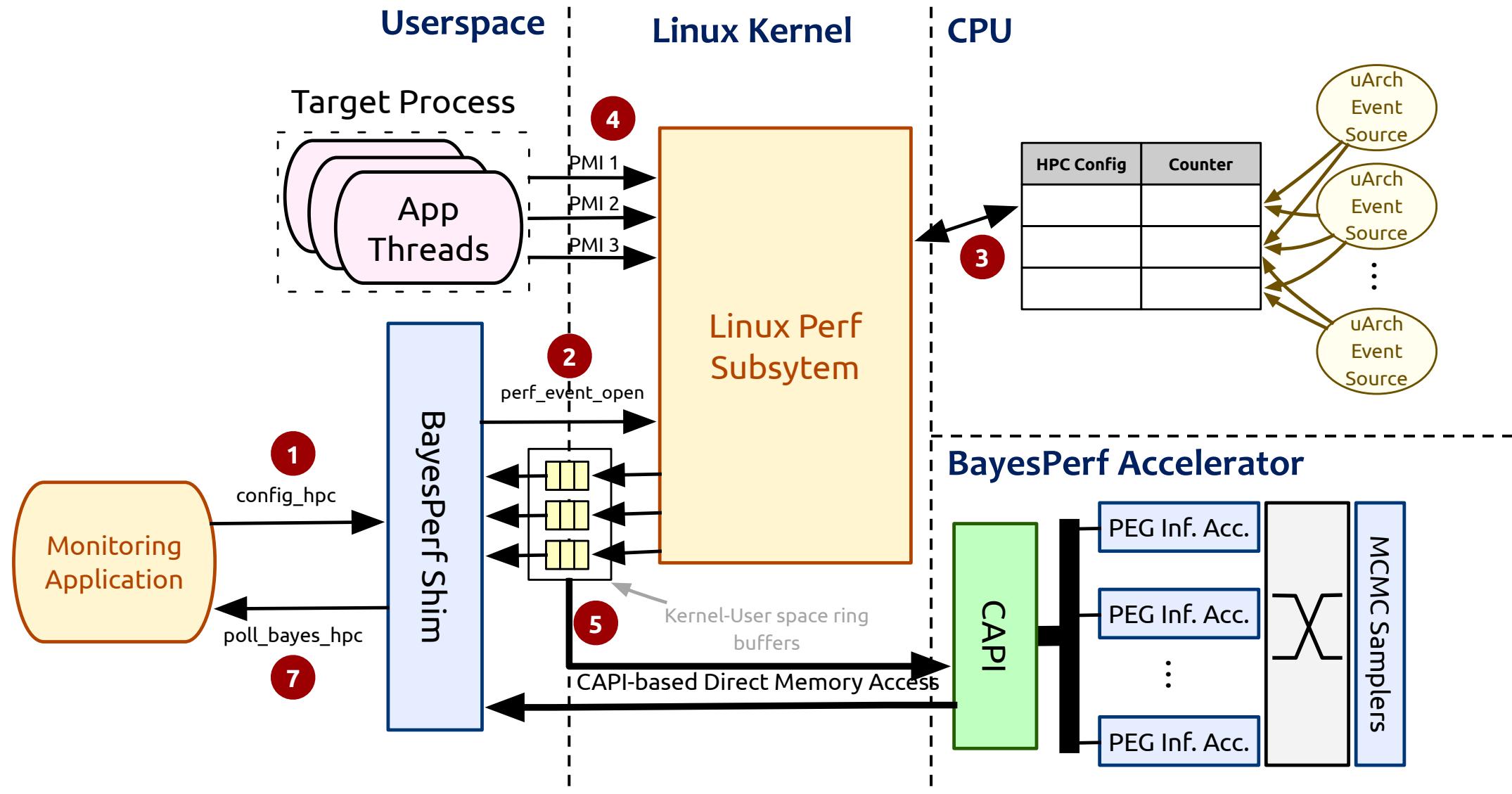
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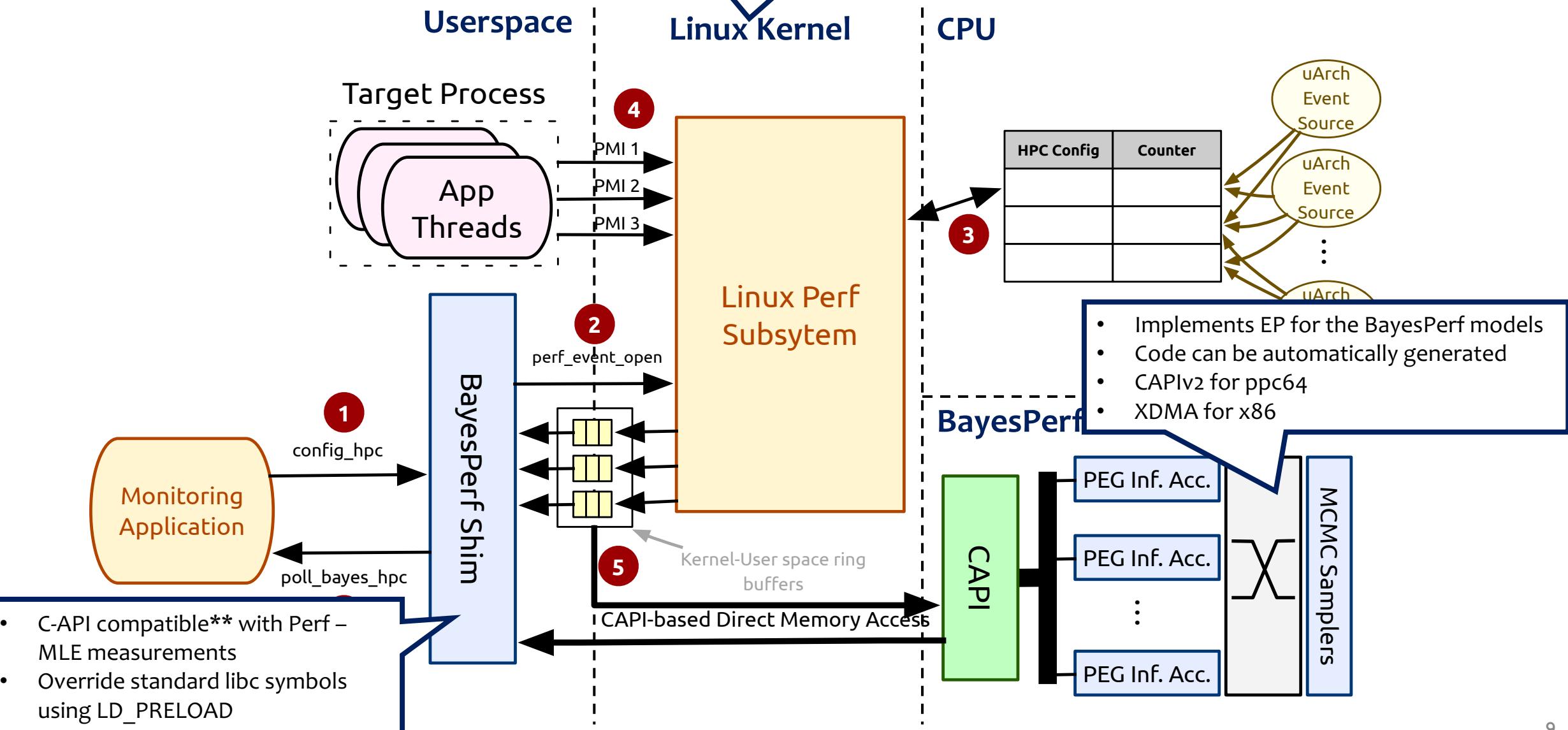


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- No modifications to perf\_event or Linux



# The BayesPerf Accelerator

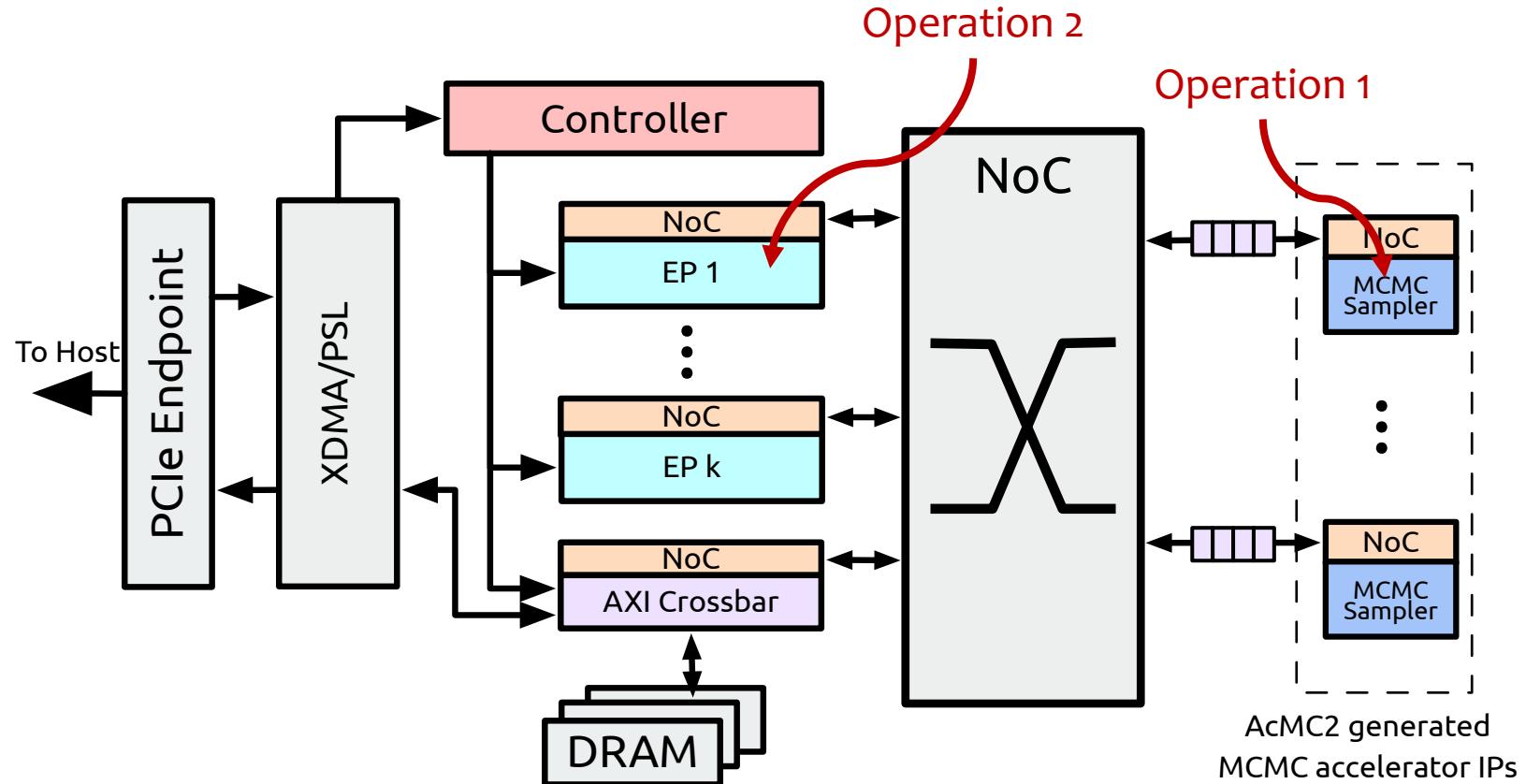
**Accelerates a Bayesian inference algorithm called Expectation Propagation**

- Core operation 1: MCMC Sampling (**85+%** of runtime)
- Core operation 2: Vector Dot Product + Update
  - Keep data in flight between Op1 and Op2

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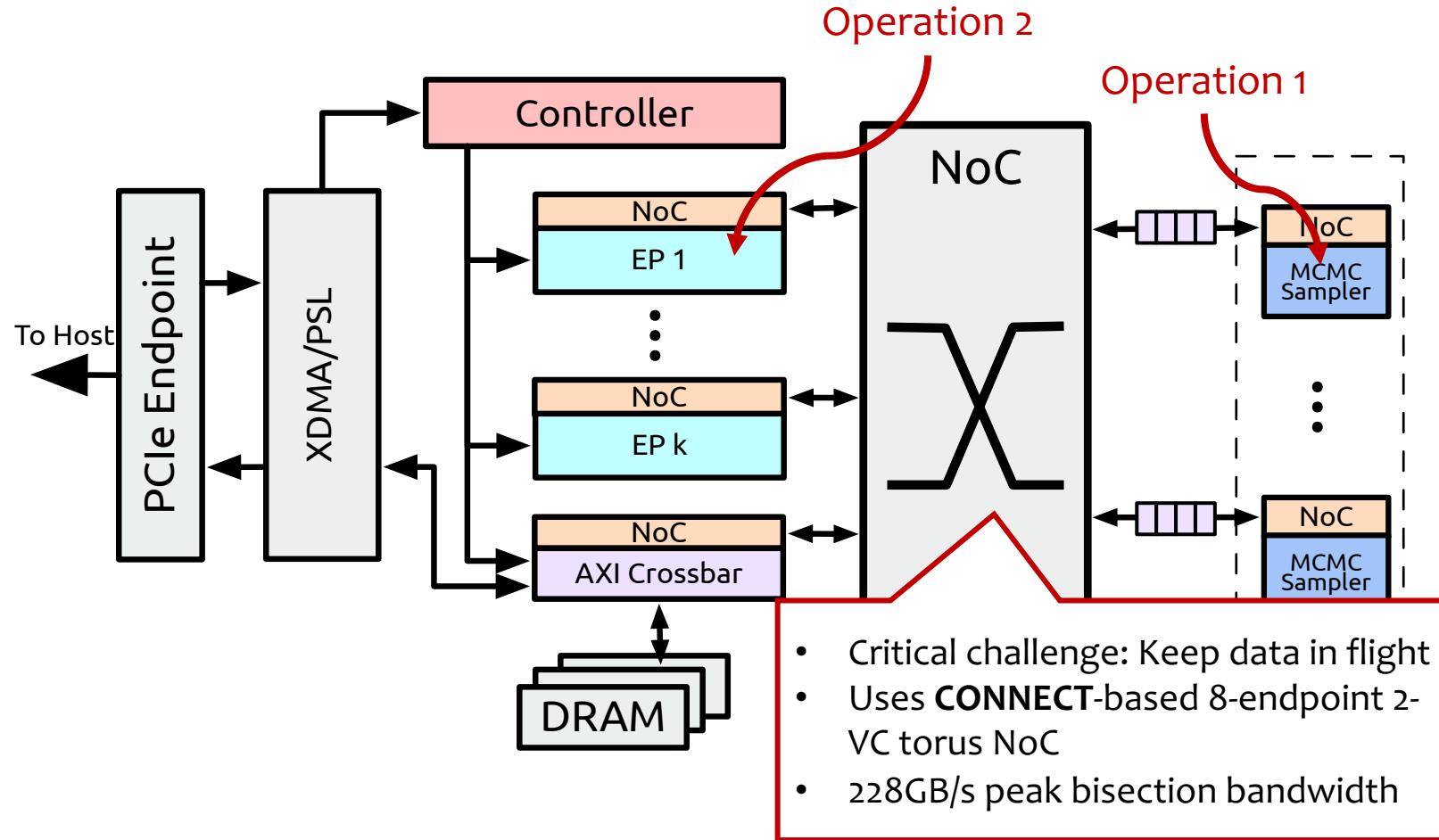
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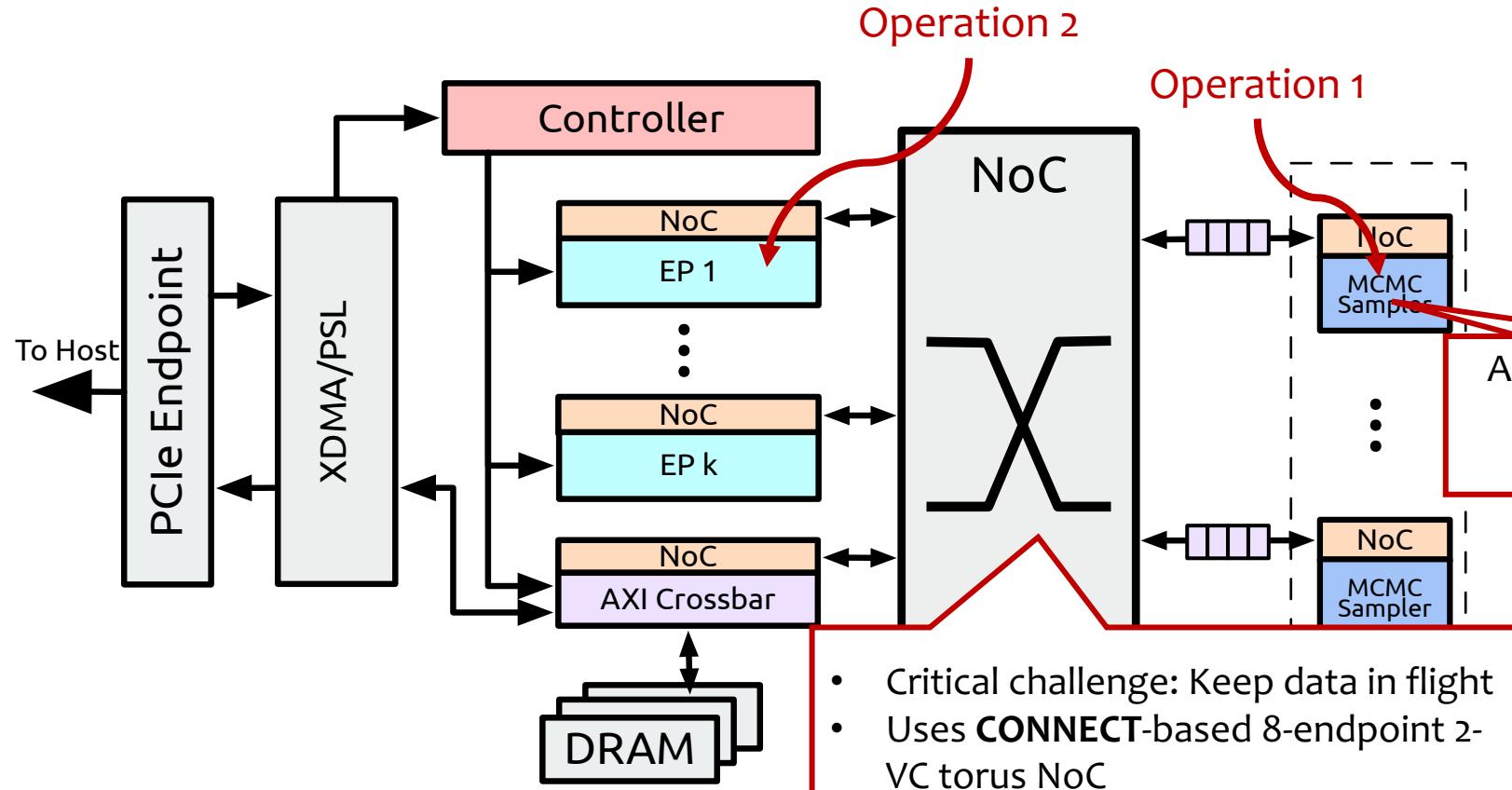
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Session: Accelerators  
ASPLOS'19, April 13–17, 2019, Providence, RI, USA

**AcMC<sup>2</sup>: Accelerated Markov Chain Monte Carlo for Probabilistic Models**

Subho S. Banerjee  
University of Illinois at Urbana-Champaign  
sbanerjee@illinois.edu

Zbigniew T. Kalbarczyk  
University of Illinois at Urbana-Champaign  
kalbarcz@illinois.edu

Ravishankar K. Iyer  
University of Illinois at Urbana-Champaign  
rkiyer@illinois.edu

**Abstract**  
Probabilistic models (PMs) are ubiquitously used across a variety of machine learning applications. They have been shown to successfully integrate structural prior information about data and effectively quantify uncertainty to enable the development of more powerful, interpretable, and efficient learning algorithms. This paper presents AcMC<sup>2</sup>, a compiler that transforms PMs into optimized hardware accelerators (for use in FPGAs or ASICs) that utilize Markov chain Monte Carlo (MCMC) sampling to infer posterior distributions. Existing compilers for probabilistic models either do not support MCMC sampling or do not generate efficient hardware. AcMC<sup>2</sup> generates MCMC samplers that are highly parallelized, yet can be easily integrated into existing hardware architectures.

**AcMC<sup>2</sup> [ASPLOS 2019] generated MCMC samplers**

Parallel architectures → Hardware accelerators; Software and its engineering → Compilers; Domain specific languages.

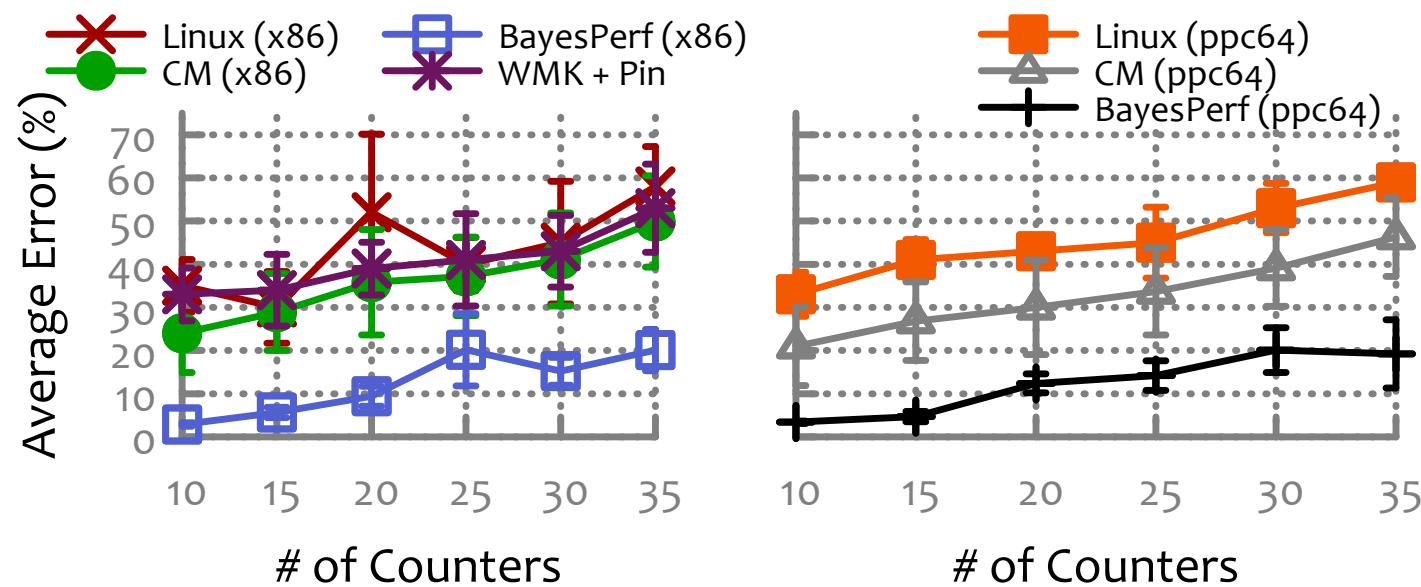
**Keywords**: Accelerated Markov Chain Monte Carlo, Probabilistic Graphical Models, Probabilistic Programming

**ACM Reference Format:**  
Subho S. Banerjee, Zbigniew T. Kalbarczyk, and Ravishankar K. Iyer. 2019. AcMC<sup>2</sup>: Accelerated Markov Chain Monte Carlo for Probabilistic Models. In *ASPLOS '19: Architecture and Programming Languages and Operating Systems (ASPLOS '19), April 13–17, 2019, Providence, RI, USA*. ACM, New York, NY, USA, 14 pages. <https://doi.org/10.1145/3297858.3304019>

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# Evaluation: Error Correction Performance of BayesPerf

On average BayesPerf reduces error by **as much 43.6% less error** when scaling to 35 counters  
[KMeans app from the HiBench benchmark suite]

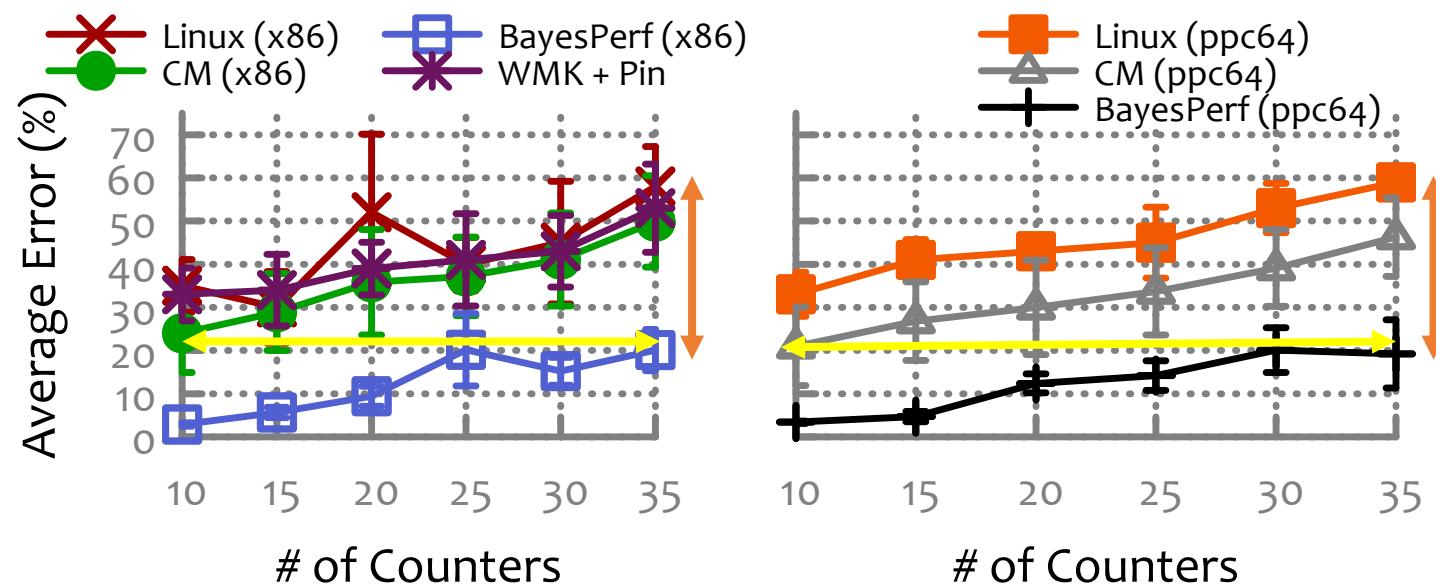


## Baselines for comparison

- Linux (\*) – Vanilla perf\_event
- CM (\*) – Counter Miner [MICRO 2018]
  - Gumbel Extreme Value Detector + Logistic Regression
- WMK+Pin – [IISWC 2008]
  - Rule-based correction

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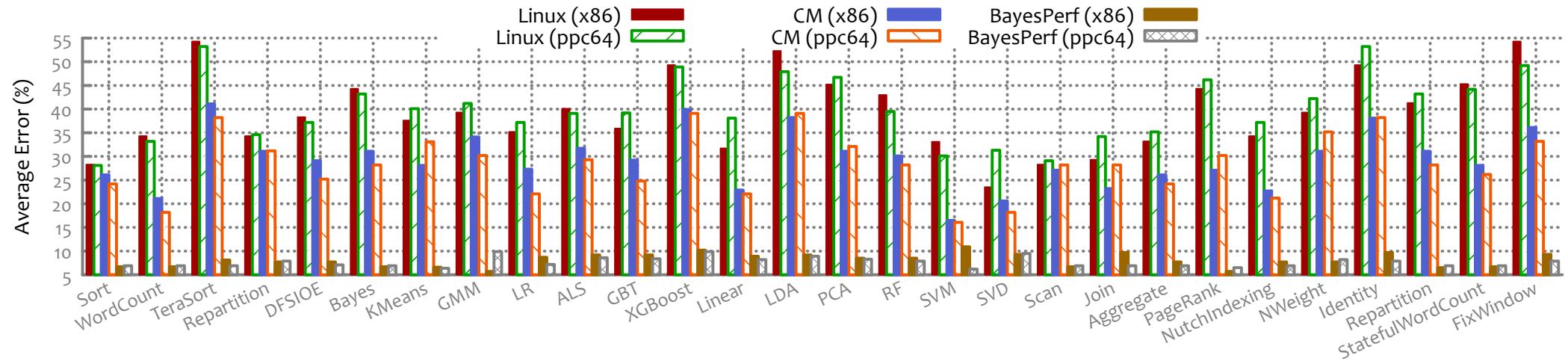


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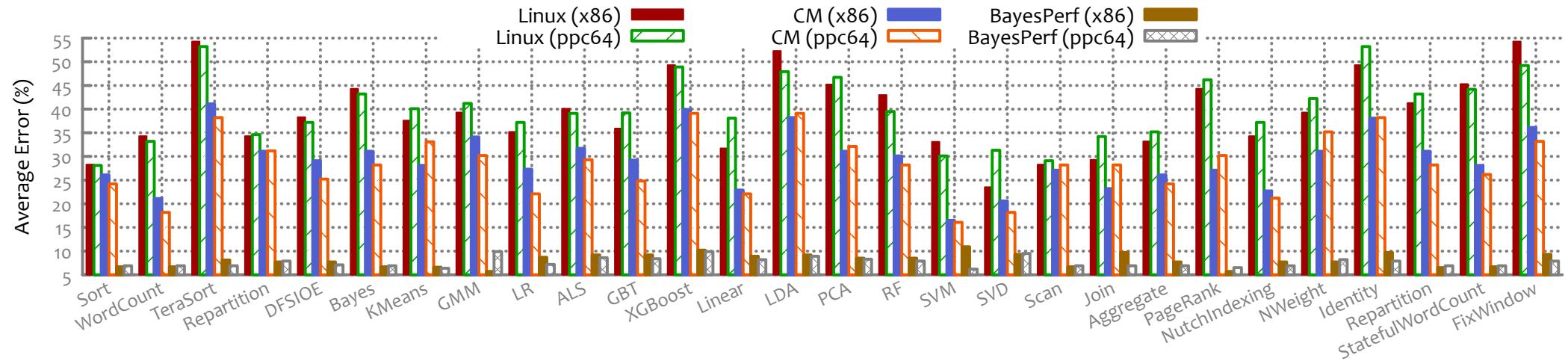
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BayesPerf running the entire HiBench suite for 25 HPCs



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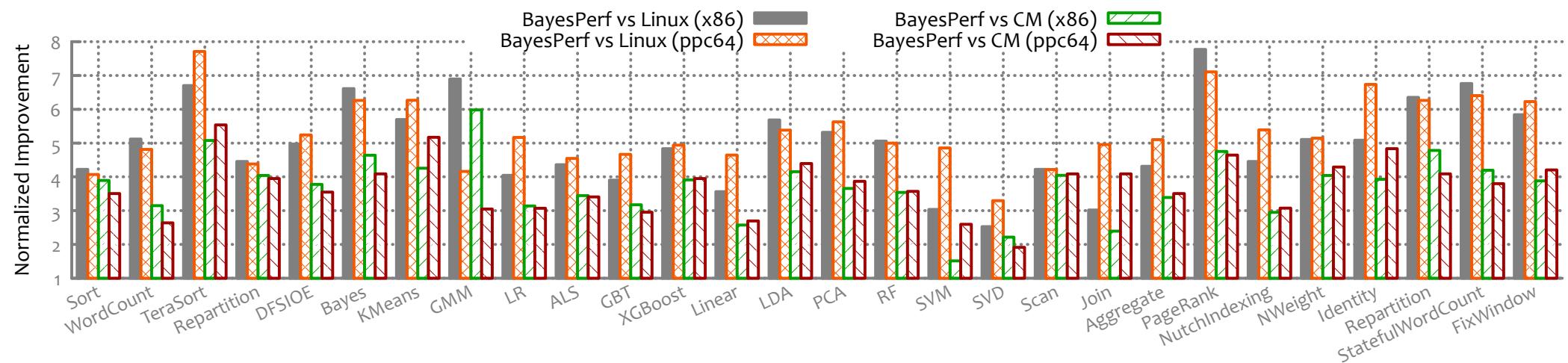


Average Improvement: **BP vs Linux = 4.9x, 5.3x**

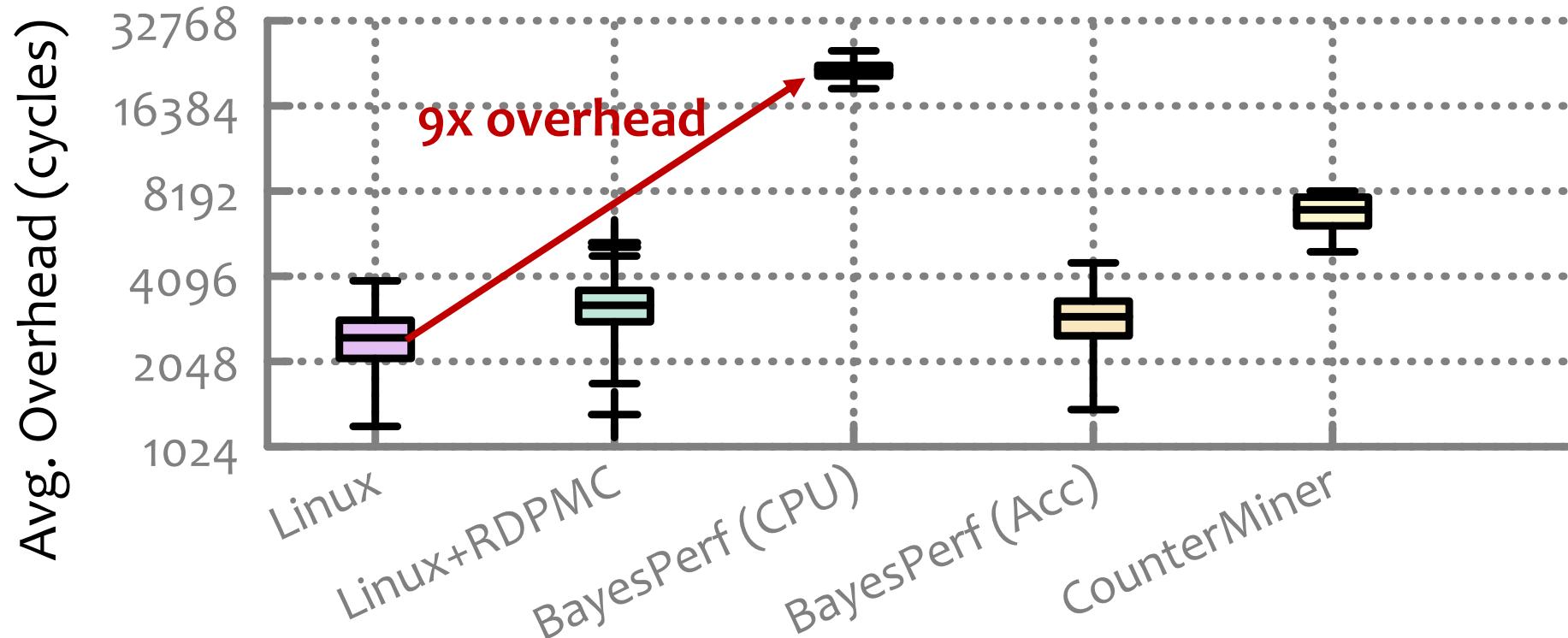
Best Improvement: **BP vs Linux = 7.8x, 7.6x**

**BP vs CM = 3.6x, 3.7x**

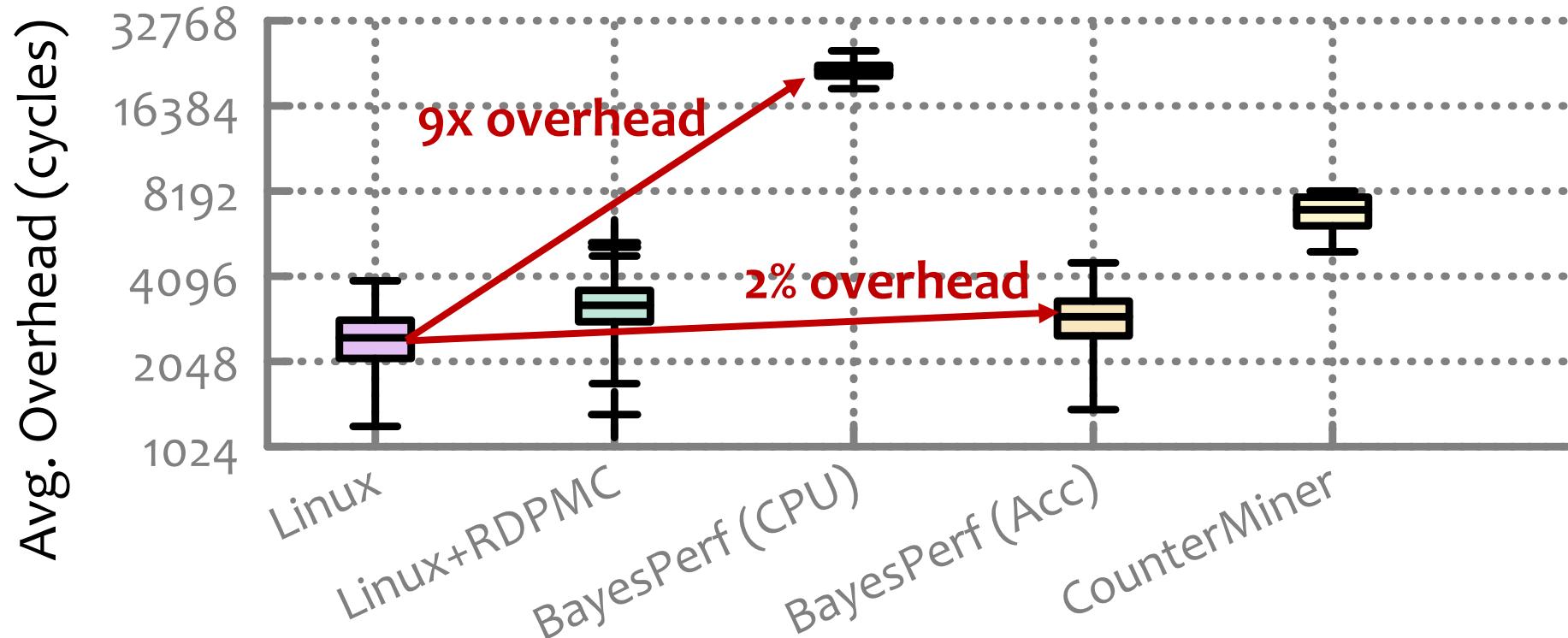
**BP vs CM = 6x, 5.4x**



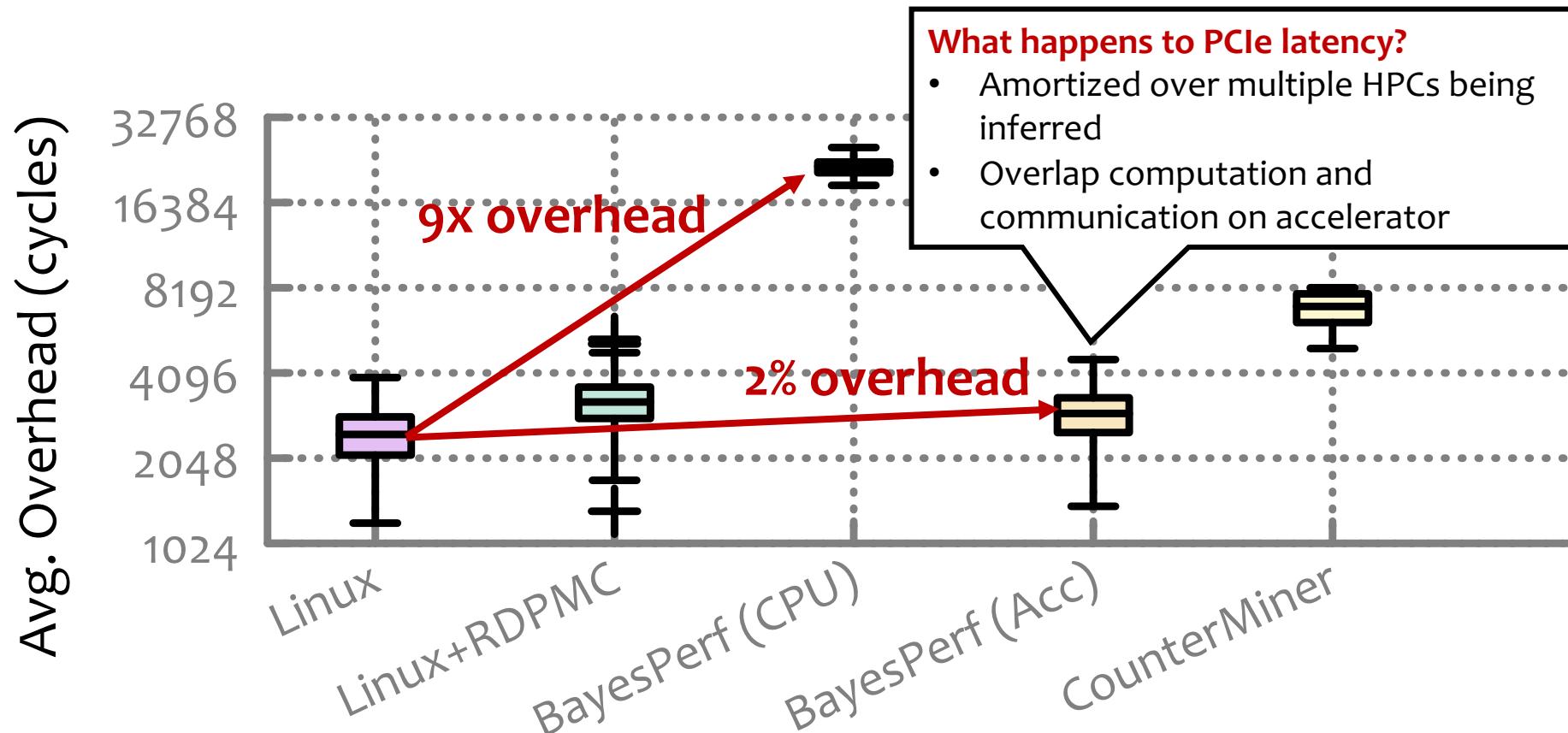
# Evaluation: Overheads



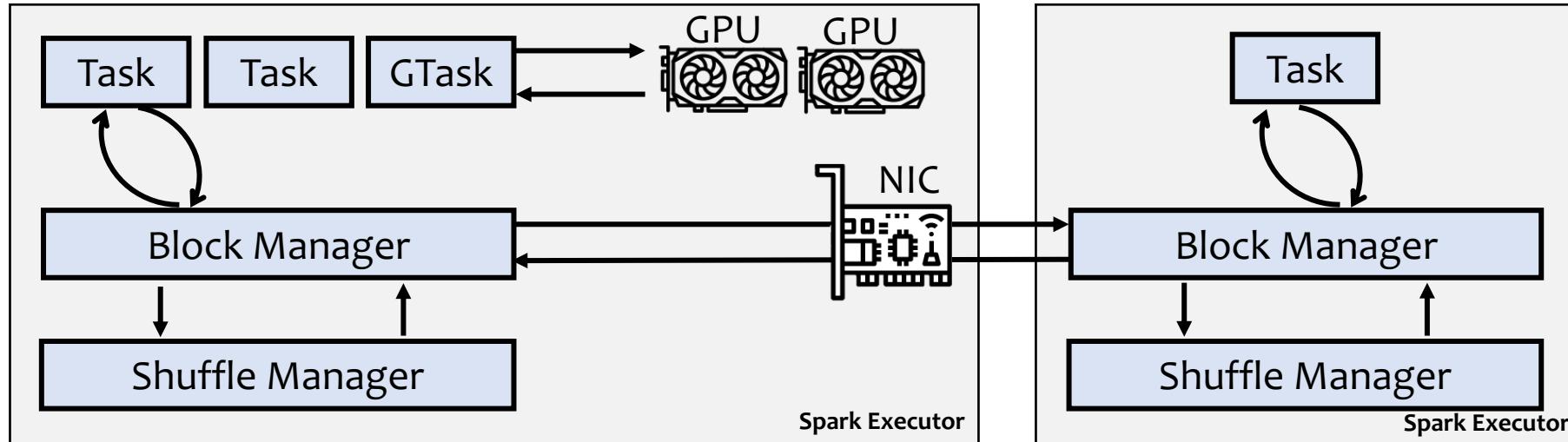
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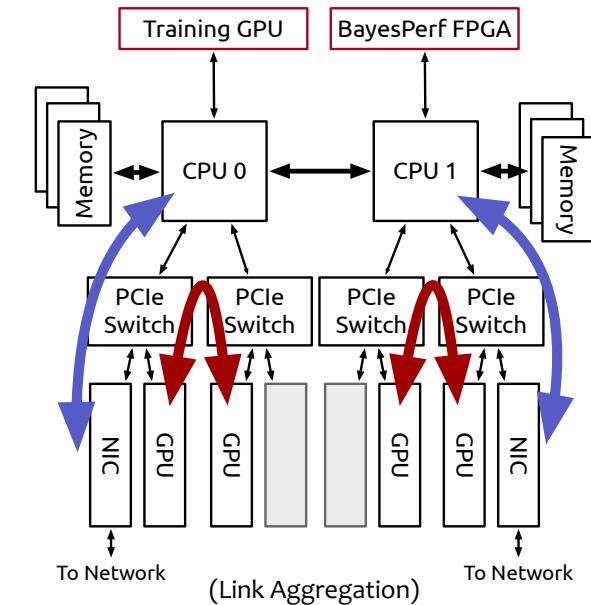
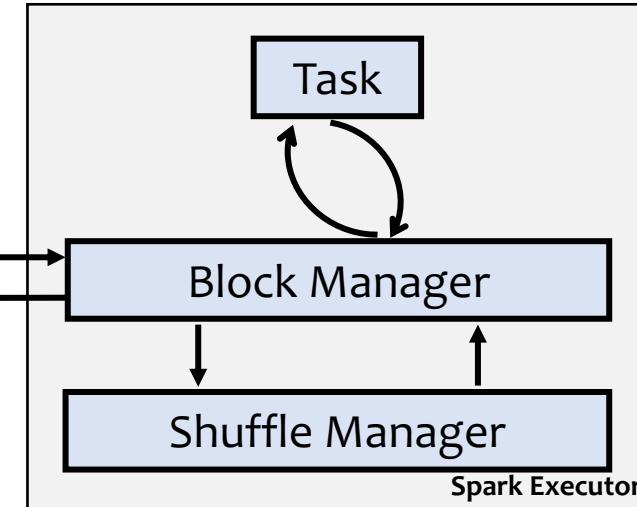
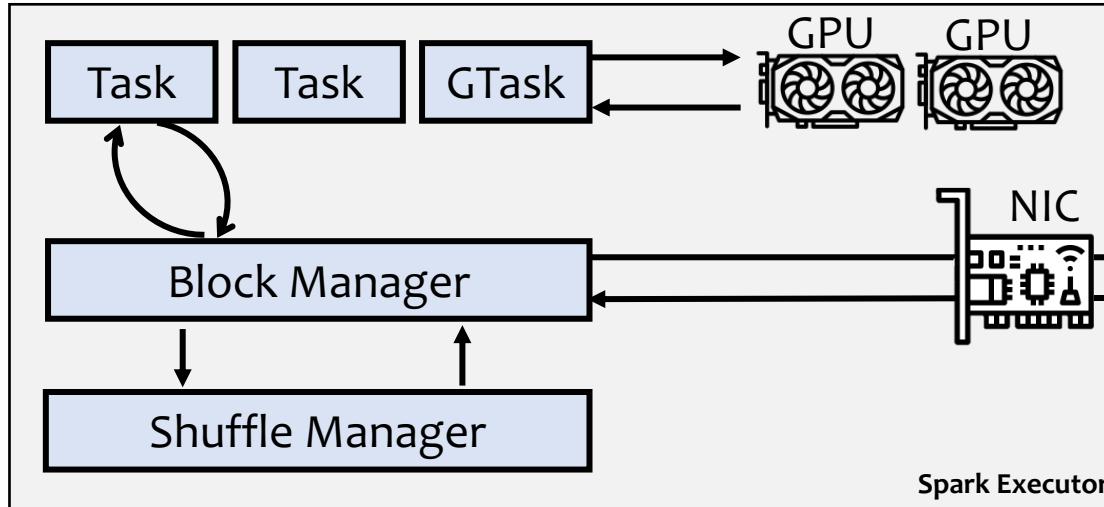
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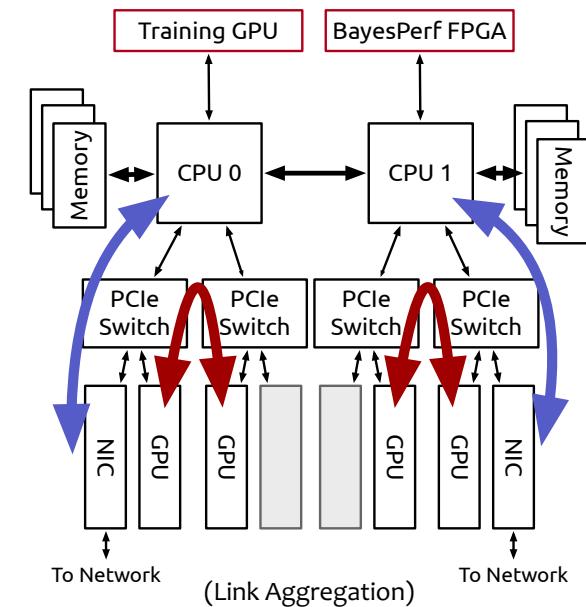
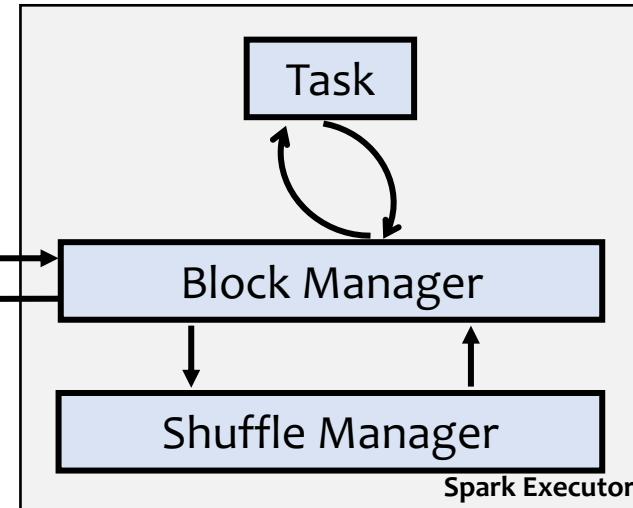
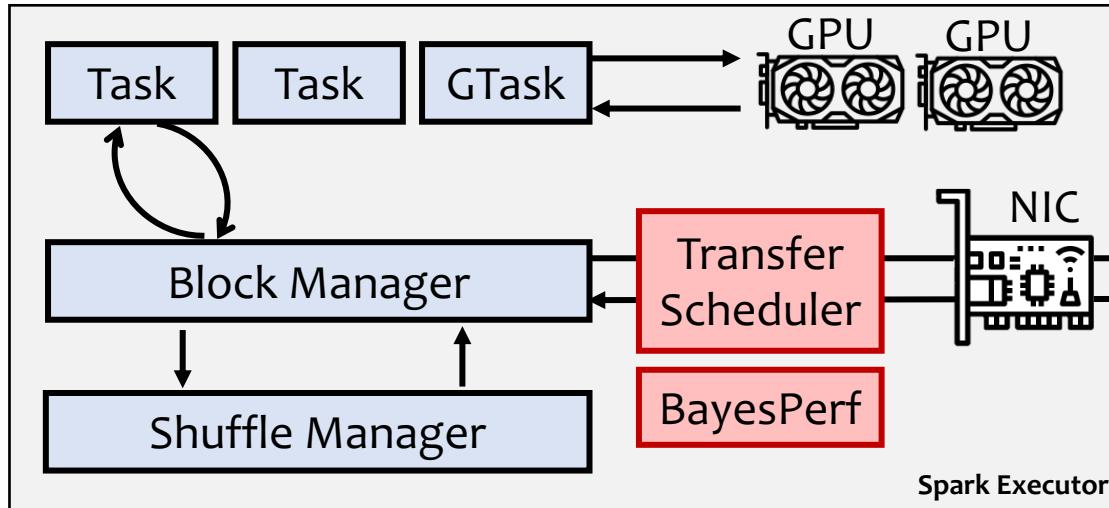
# Learned Controller Case Study: Scheduling PCIe Transfers



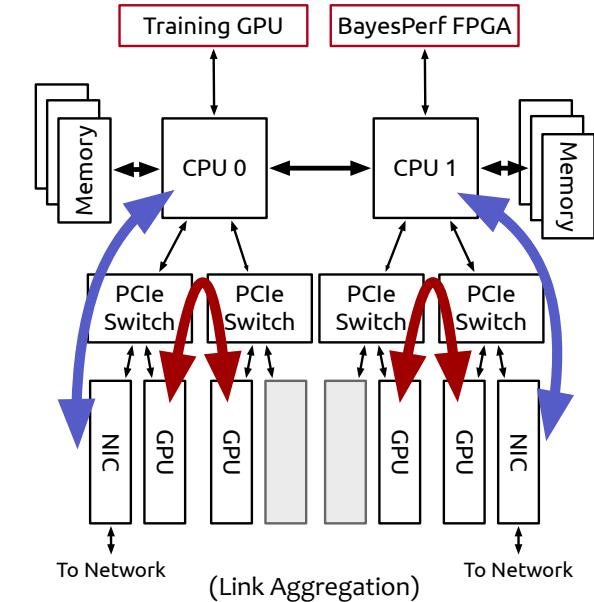
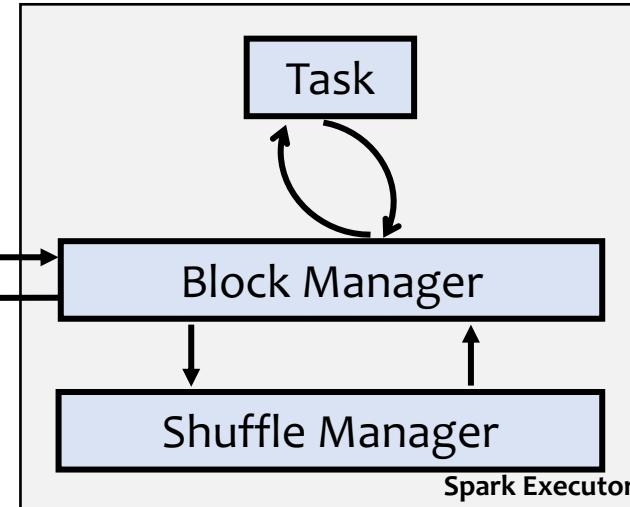
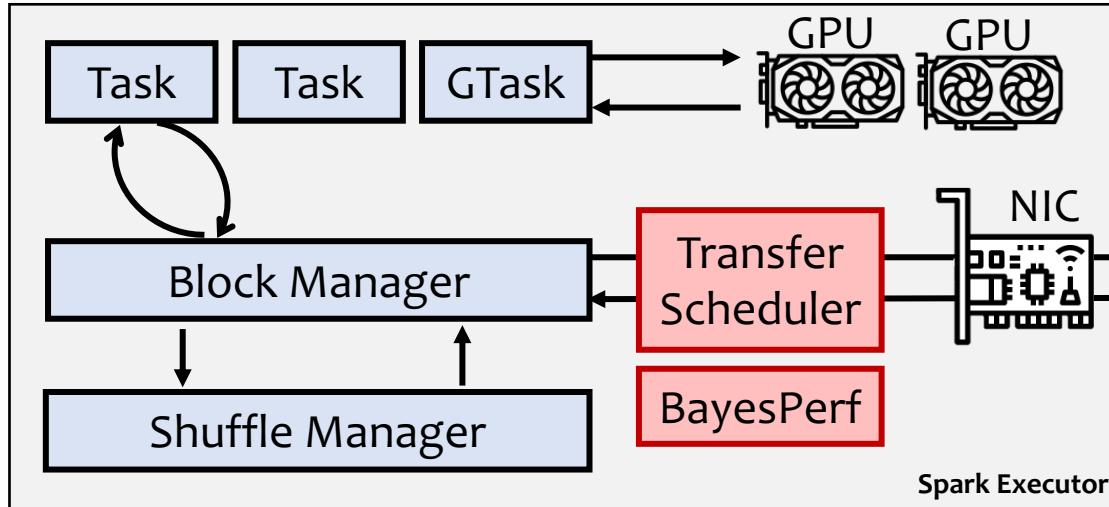
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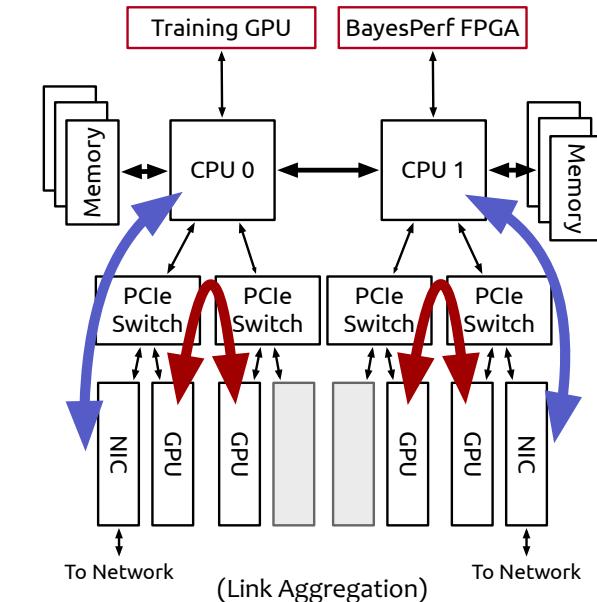
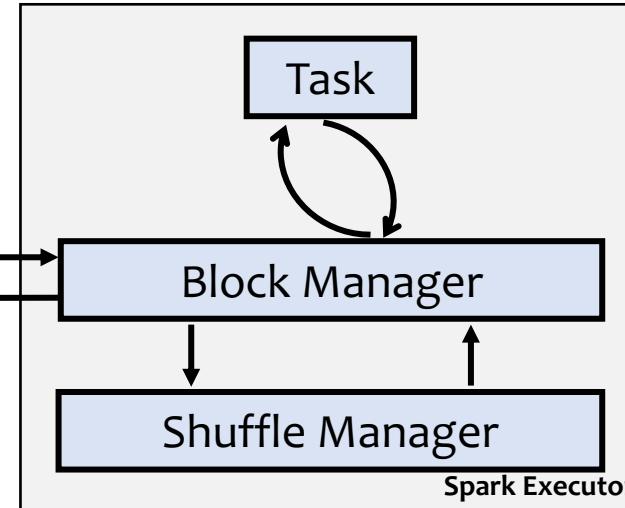
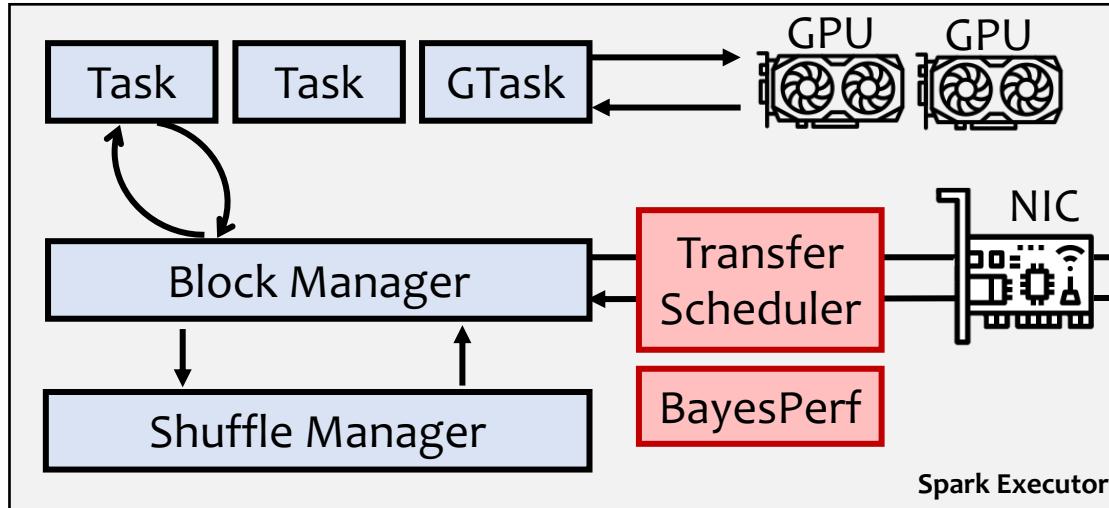


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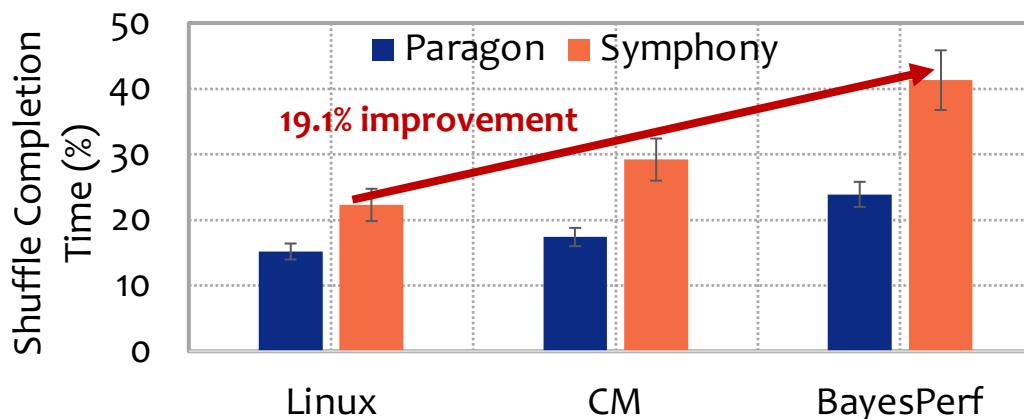
- The Transfer Scheduler is trained using: RL [Symphony - ICML2020], CF [Paragon - ASPLOS 2013]

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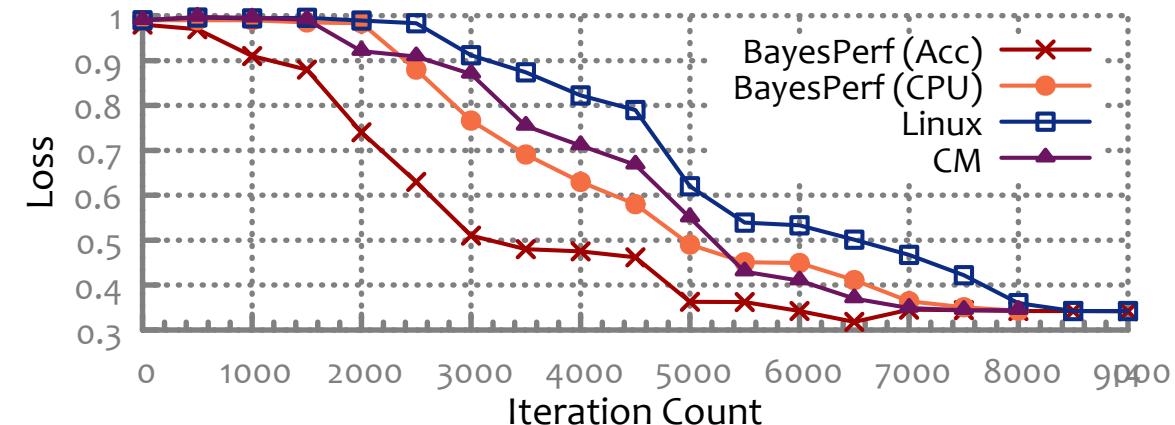


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Up to **19% improvement** in overall shuffle completion time



**37% reduction** in time to convergence for the RL model



# Conclusion

BayesPerf: A system for **real-time quantification** and **minimization** of HPC measurement errors

Can reduce errors by **as much as 8x** with **<2% latency overhead**

- Net effect of BayesPerf
  - Increases the number of HPC registers
  - Decreases the sampling frequency

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  - Composability with other ML models

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- We think this idea can be used quantifying and correcting errors other ML applications