Verilog Lab 1

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Course: DIGITAL ELECTRONICS AND VLSI DESIGN LAB (AV232)

Question No. 1 A room has two switch and one Fan. The switches are denoted by “A” and “B” and the Fan is denoted by “F”. The condition is given that the Fan will be running (ON) when any one of the switch is ON. As a designer you have to make a circuit which will do the operation. Write the Boolean Expression for the Circuit. Write the Verilog Module for the circuit. [The circuit input as Switches “A”, “B”. The output of the Circuit is “F”.]

Sol:

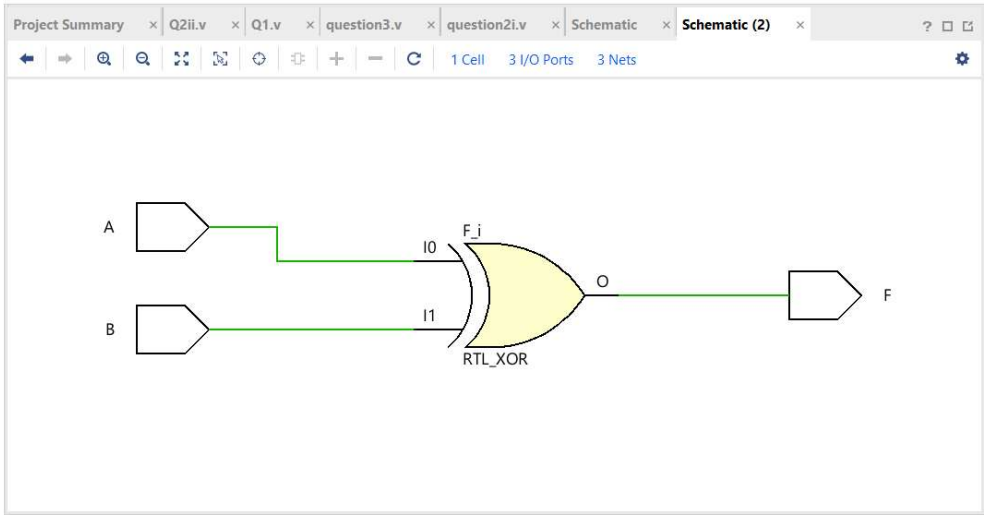
The **boolean expression** should be:

F = A xor B

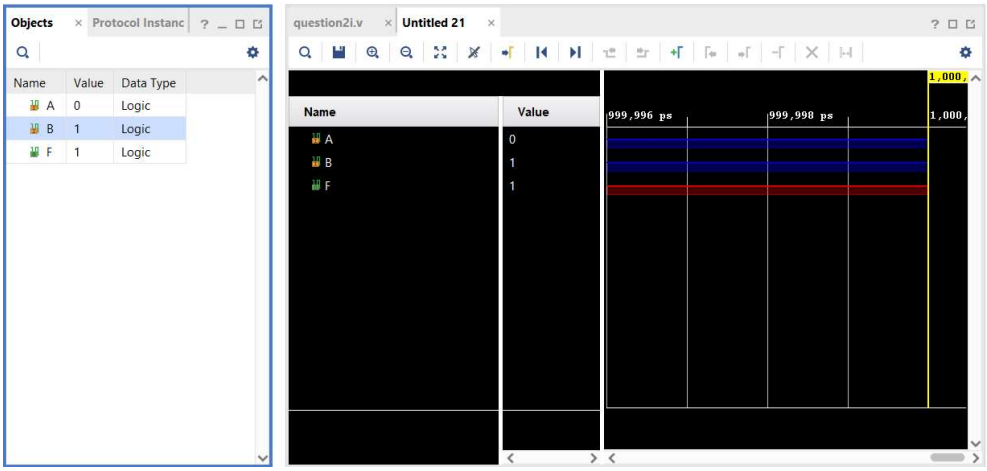
Code:

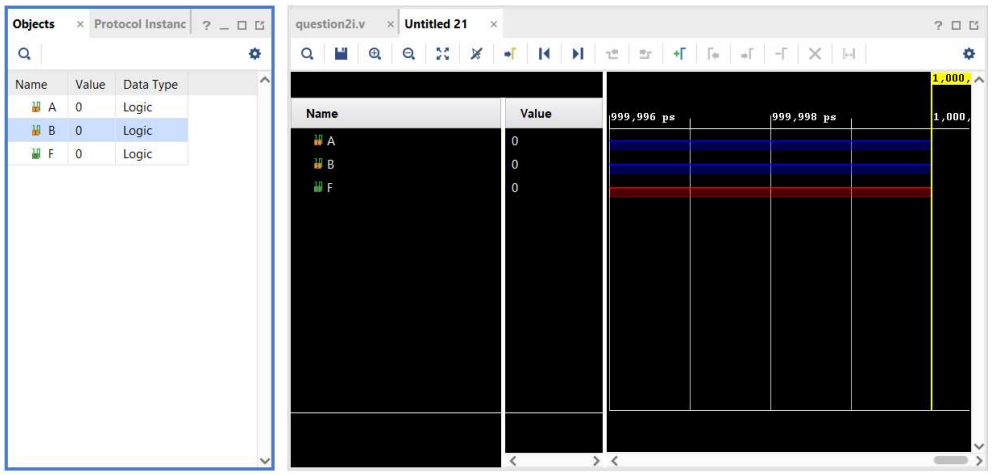
```
module fan(
   input A,
   input B,
   output F
   );
  assign F = A^B;
endmodule
```

Schematic:



Simulation:





Question No. 2

- Write the Verilog module for Half Adder Circuit.

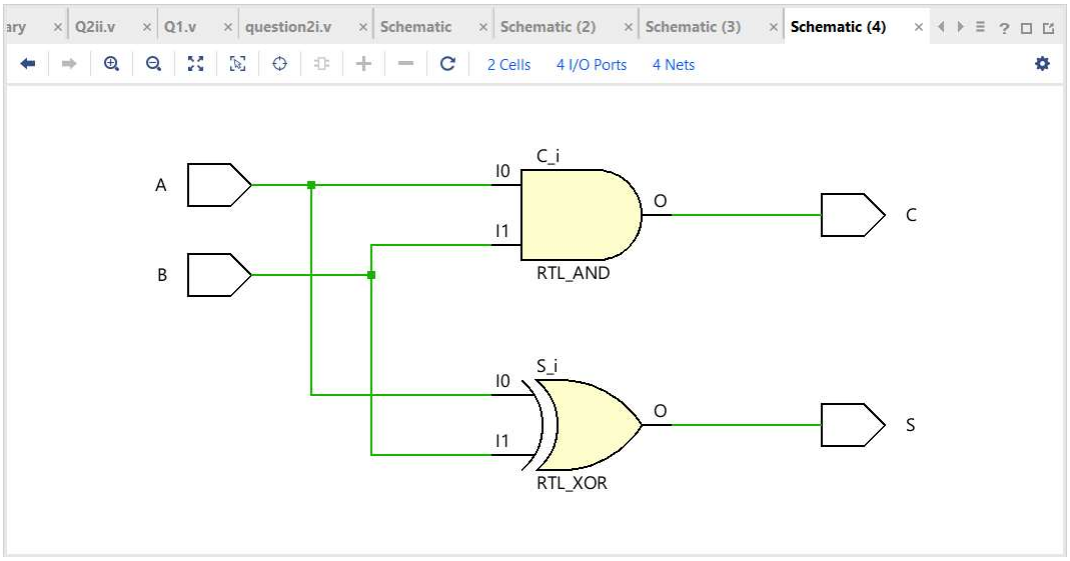
Sol: **Boolean expression:**

Sum, S = A xor B
Carry, C = A and B

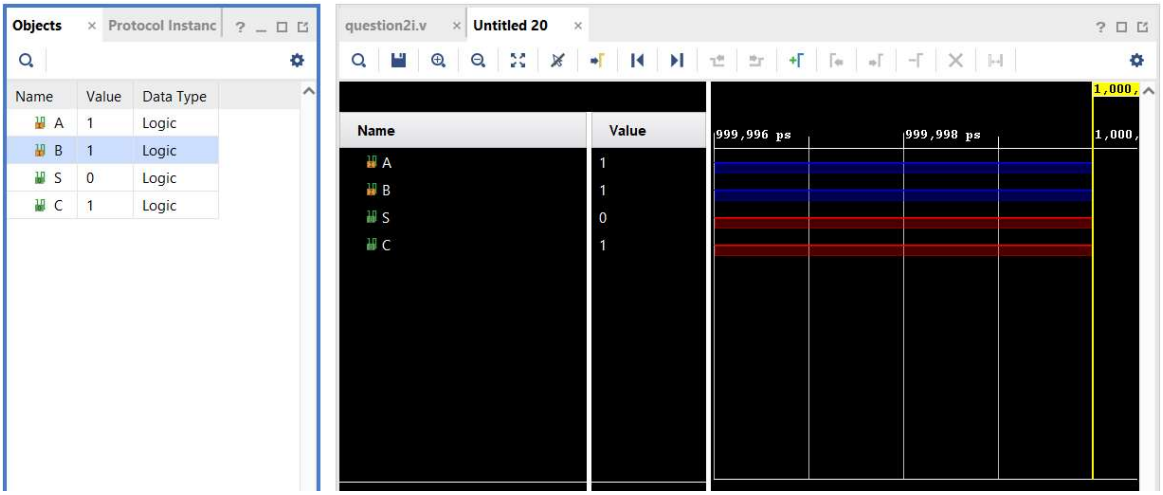
Code:

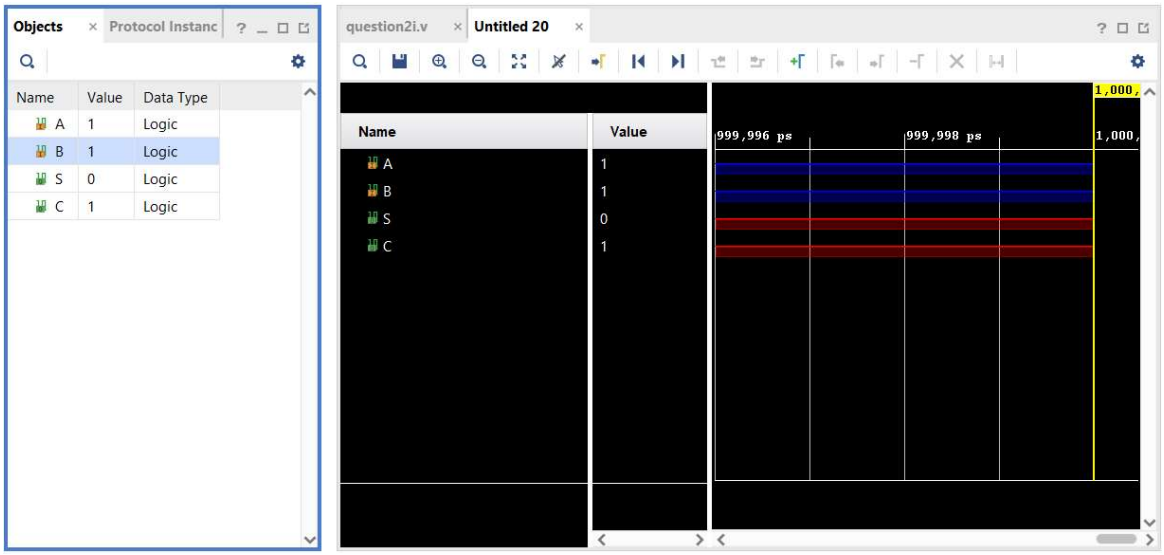
```
module halfAdder(A,B,C,S);
input A, B;
output S, C;
assign S = A^B;
assign C = A&B;
Endmodule
```

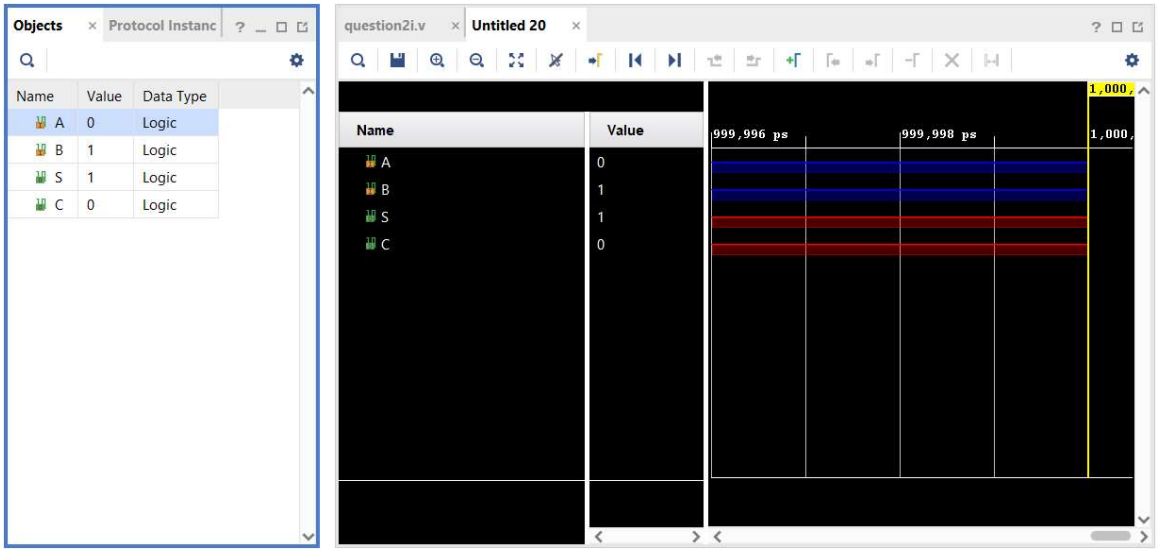
Schematic:



Simulation:







- Write the Verilog module for Full Adder Circuit

Sol: **Boolean expression:**

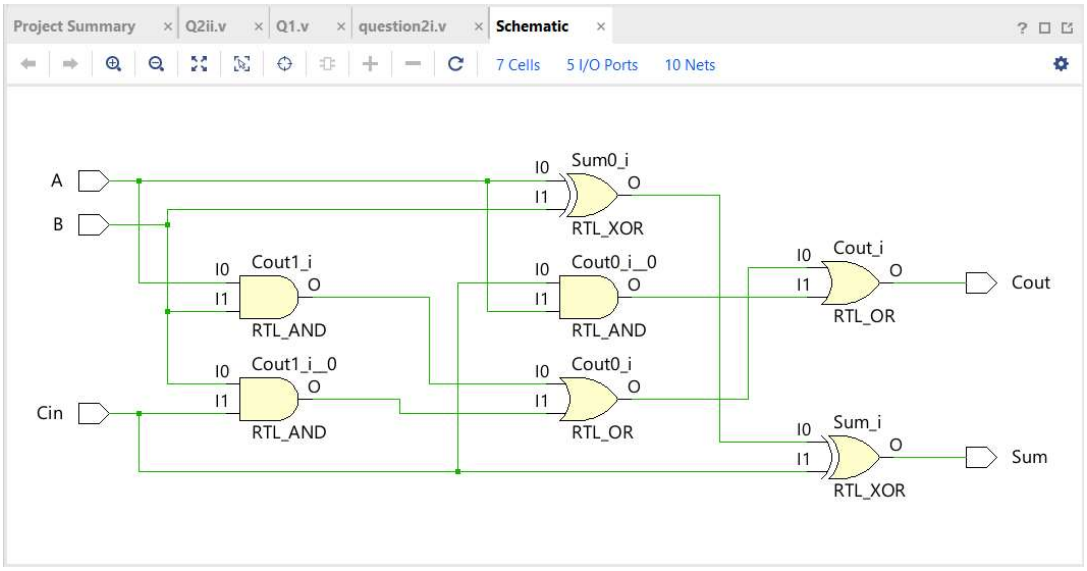
Sum, S = A xor B xor Cin

Carry, Cout = (A and B) or (B and Cin) or (Cin and A)

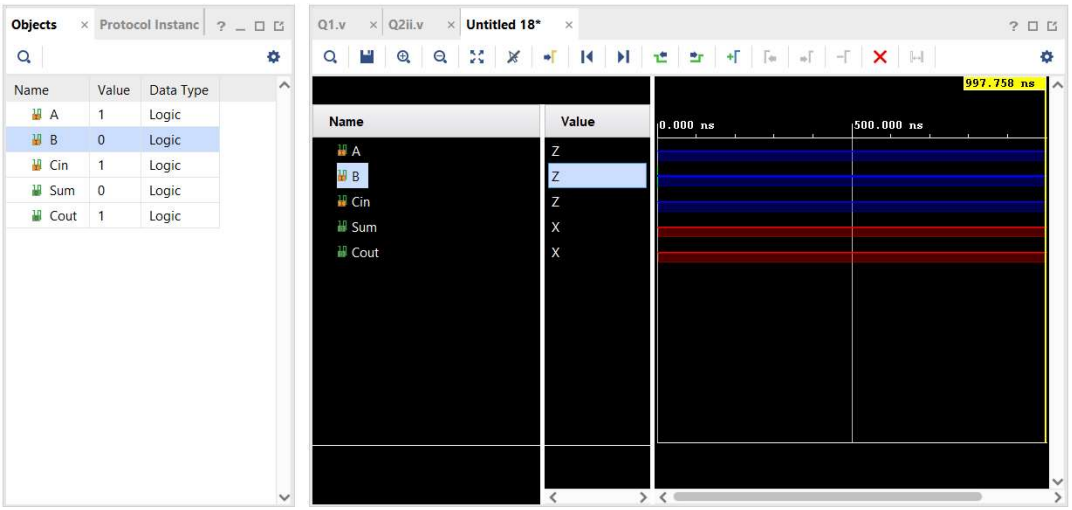
Code:

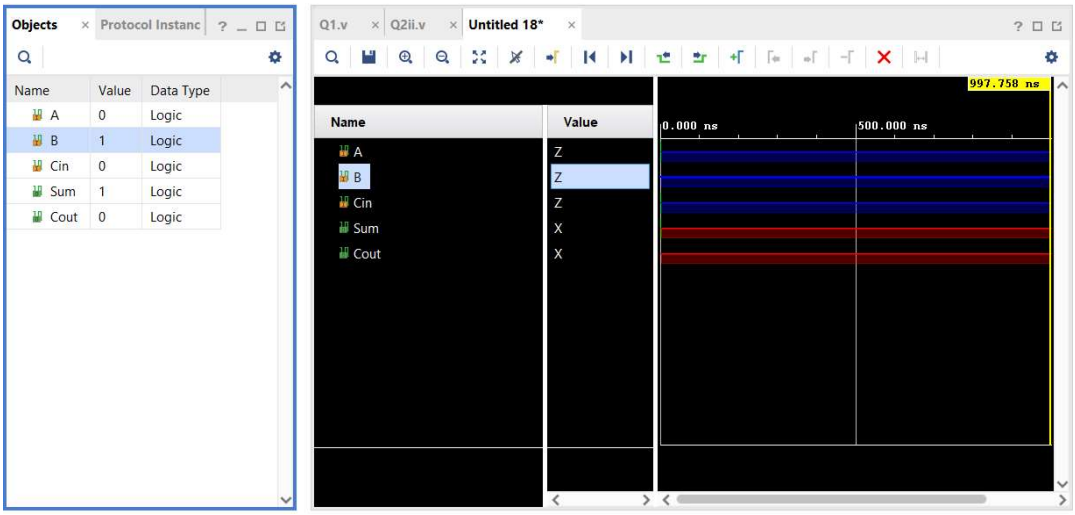
```
module fullAdder(A,B,Cin,Cout,Sum);
input A,B,Cin;
output Sum,Cout;
assign Sum = (A^B^Cin);
assign Cout = (A&B)|(B&Cin)|(Cin&A);
endmodule
```

Schematic:



Simulation:





Question No. 3 Write a Verilog module for 2:1 Multiplexor

Sol: **Boolean expression:**

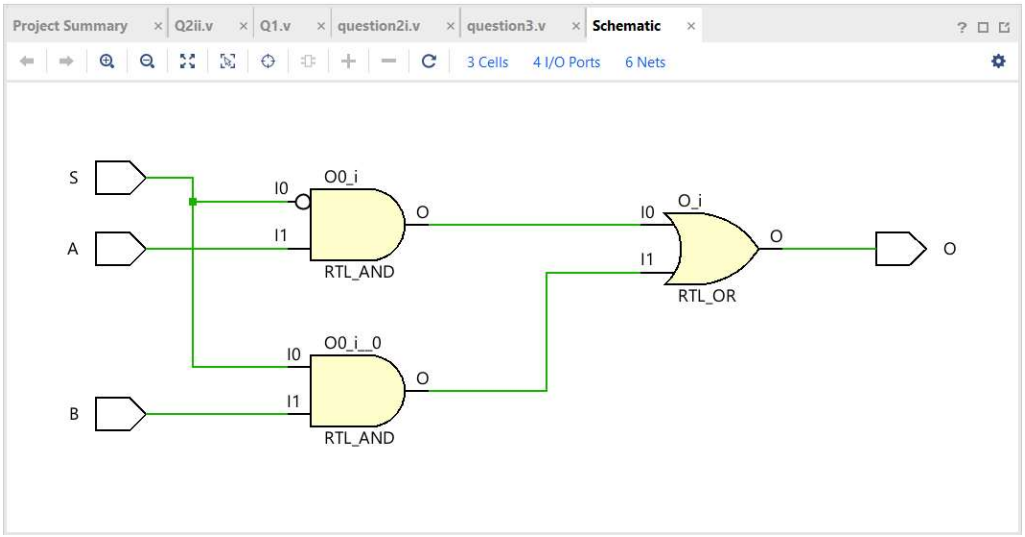
Output, O = ((not S) and A) or (S and B)

Code:

```
module mux(
   input A,
   input B,
   input S,
   output O
   );
assign O = (~S&A)|(S&B);
```

endmodule

Schematic:



Simulation: