LAB 4 Pre-Labwork

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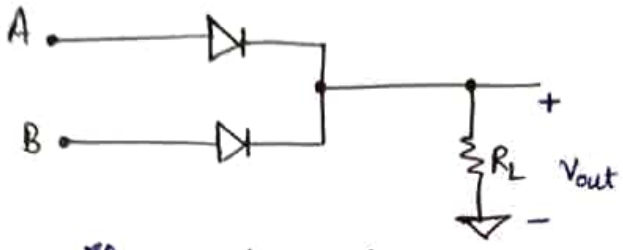
SC22B146

Realization of Logic Gates using Diodes and Transistor and study the performance metric

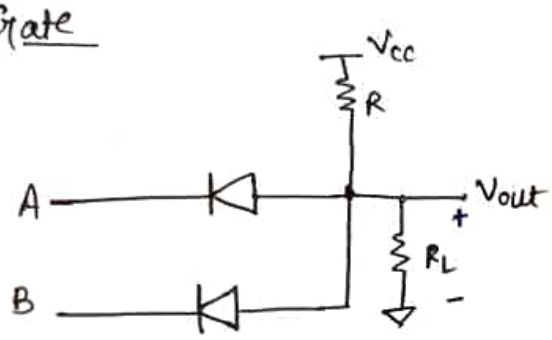
① Realizing two input AND, OR, NAND, NOR, NOT, using Diode and Transistor Logic (TTL).

OR Gate



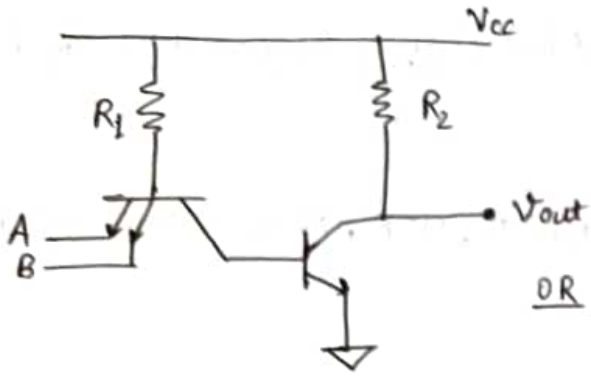
A	B	V_{out}
0	0	0
0	1	1
1	0	1
1	1	1

AND Gate

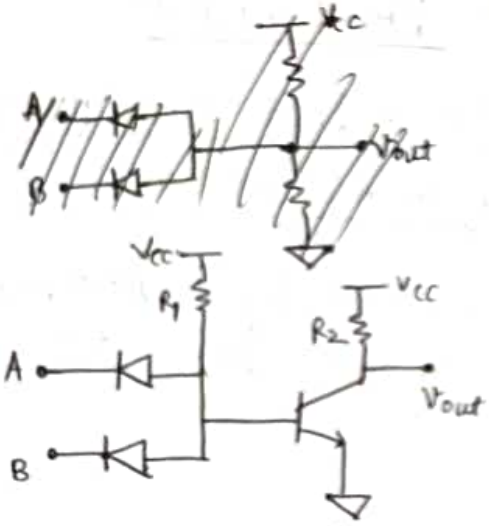


A	B	V_{out}
0	0	0
0	1	0
1	0	0
1	1	1

TTL NAND Gate:

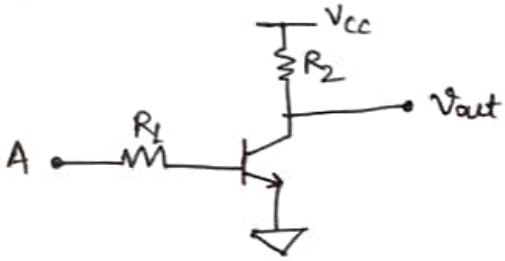


OR



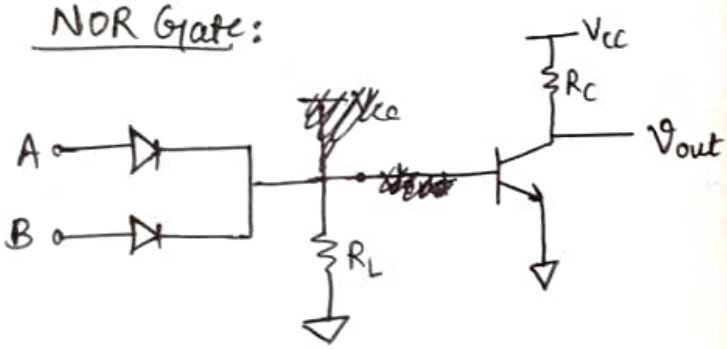
A	B	Vout
0	0	1
0	1	1
1	0	1
1	1	0

NOT Gate:



A	Vout
0	1
1	0

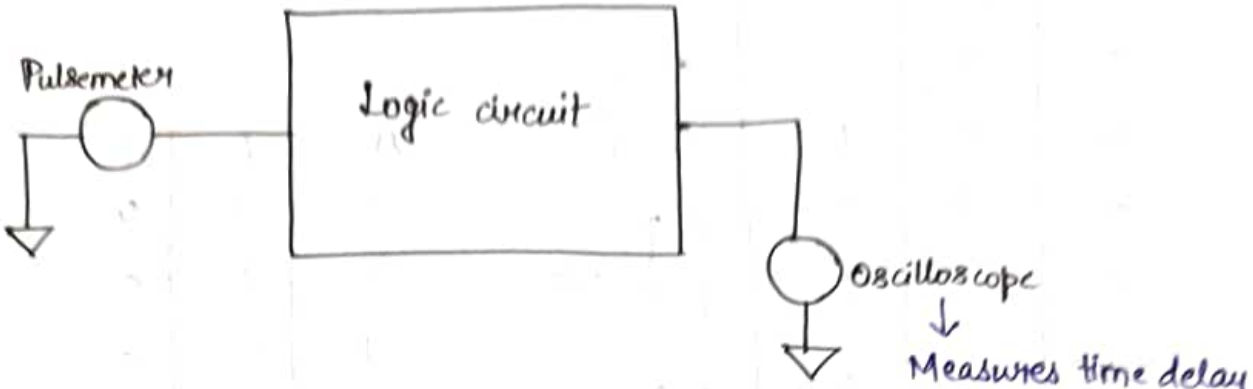
NOR Gate:

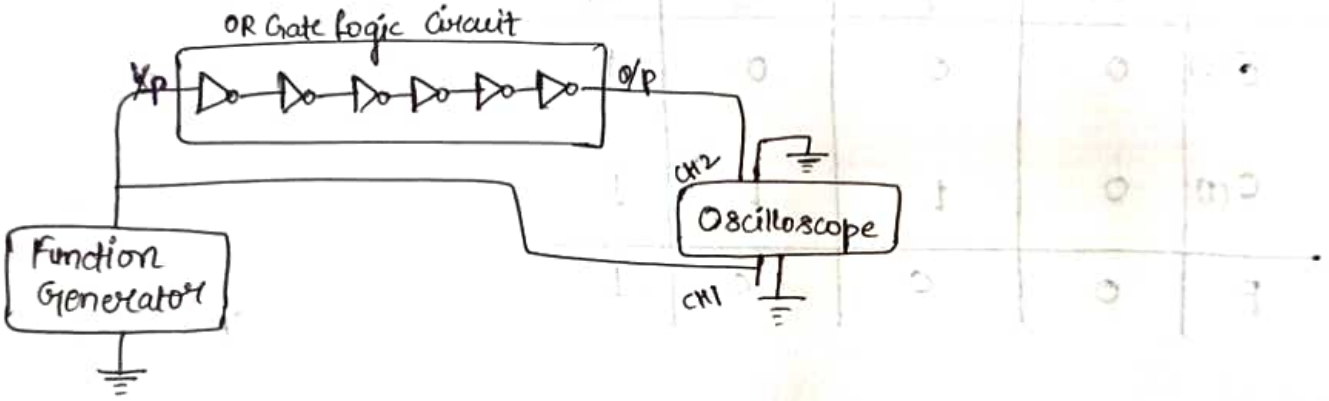


A	B	Vout
0	0	1
0	1	0
1	0	0
1	1	0

Verified
Ans

② Measuring the propagation delay of a logic using logic circuit.





Propagation delay of one OR Gate = $\frac{\text{P.D. for entire IC}}{\text{No. of OR Gates in an IC}}$

$= \frac{24\ ns}{6}$

$= 4\ ns$

③ 3 input majority logic function using 4 to 1 Mux.

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

⇒

A	B	F
0	0	0
0	1	C
1	0	C
1	1	1

	$\bar{A}\bar{B}$ I_0	$\bar{A}B$ I_1	$A\bar{B}$ I_2	AB I_3
$\bar{C}$ (0)	0	0	0	1
C (1)	0	1	1	1
F	0	C	C	1