Assignment-2: Sequential Assignment

AV212 - Digital Electronics and VLSI Design

Submitted by:

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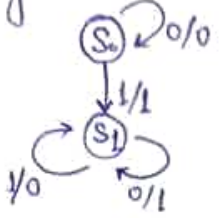
Q.① Design a sequential circuit using JK Flip flop for generating 2's complement of serial data.

Sol^n: State diagram:



State table:

PS	NS		O/P	
	x=0	x=1	x=0	x=1
S_0	S_0	S_1	0	1
S_1	S_1	S_1	1	0

State Assignment:

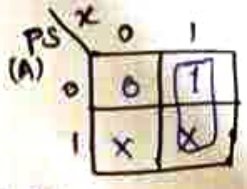
$S_0 \rightarrow 0$

$S_1 \rightarrow 1$

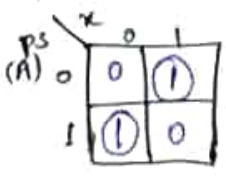
PS (A)	x	NS	O/P	J	K
0	0	0	0	0	X
0	1	1	1	1	X
1	0	1	1	X	0
1	1	1	0	X	0

K-Map:

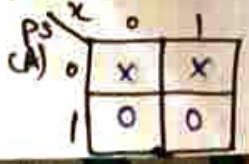
For J:



For O/p:



For K:

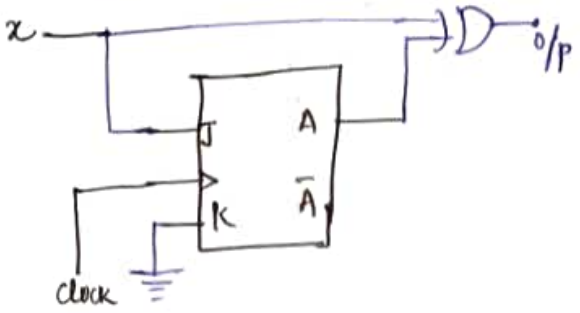


$J = x$

$K = 0$

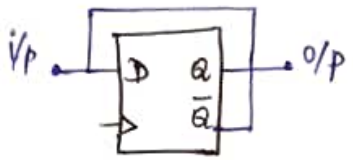
$O/p = A \oplus x$

Circuit:



(2) Design a binary counter that will convert a 64 KHz pulse signal into a 2 KHz square wave. Use D flip flop.

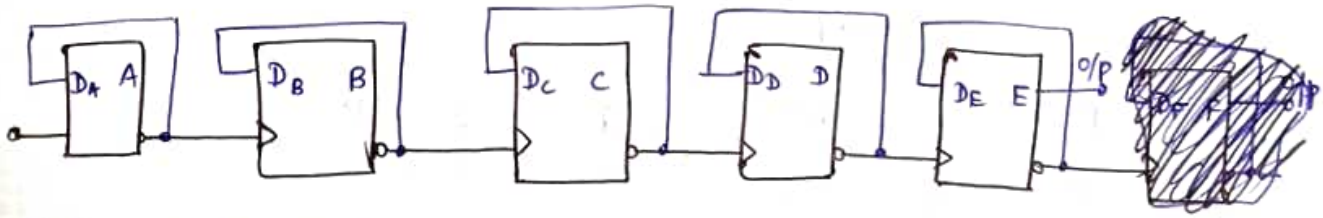
Soln: By using positive edge-triggered D FF:



Pulse signal is converted into square wave (but with same frequency).

By frequency division ratio = $\frac{f_{in}}{f_{out}} = \frac{64\text{ KHz}}{2\text{ KHz}} = 32$.

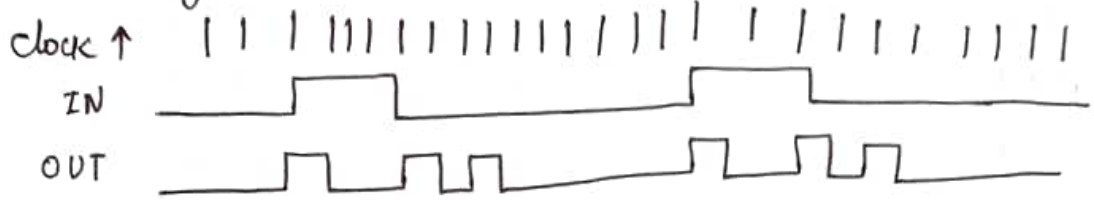
So, we need 5 flip flops to achieve 2 KHz.



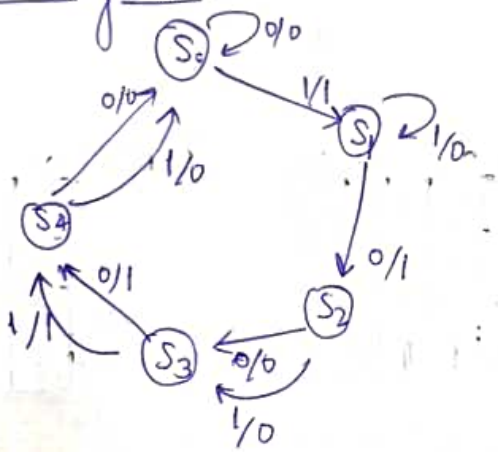
Using 5 bit ripple counter,

output frequency = 2 KHz.

③ Design a sequential circuit that generates one pulse when an input goes from low to high and when the input goes from high to low, the circuit generates two pulses as shown below. The input signal needs to be synchronized with the clock. Use T flip flop for the design. In between the double pulse if any transition occurs in the input, neglect it.



Soln: State diagram:



State table:

PS	NS		op	
	x=0	x=1	x=0	x=1
S_0	S_0	S_1	0	1
S_1	S_2	S_1	1	0
S_2	S_3	S_3	0	0
S_3	S_4	S_4	1	1
S_4	S_0	S_0	0	0

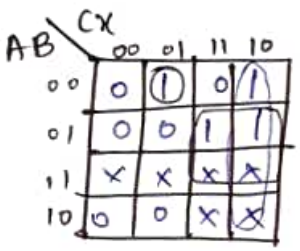
State Assignment:

$S_0 \rightarrow 000$
$S_1 \rightarrow 001$
$S_2 \rightarrow 010$
$S_3 \rightarrow 011$
$S_4 \rightarrow 100$

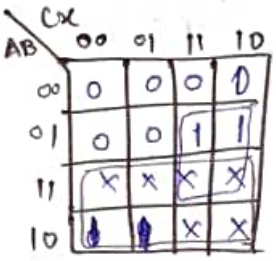
PS (ABC)	x	NS (ABC)	O/P	T_A	T_B	T_C
000	0	000	0	0	0	0
000	1	001	1	0	0	1
001	0	010	1	0	1	1
001	1	001	0	0	0	0
010	0	011	0	0	0	1
010	1	011	0	0	0	1
011	0	100	1	1	1	1
011	1	100	1	1	1	1
100	0	000	0	1	0	0
100	1	000	0	1	0	0

K-Map:

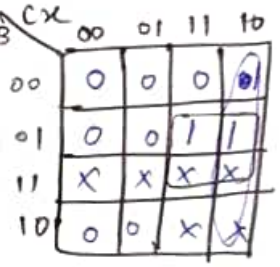
O/P:



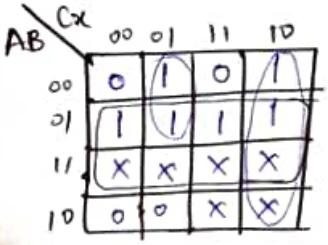
T_A:



T_B:



T_C:

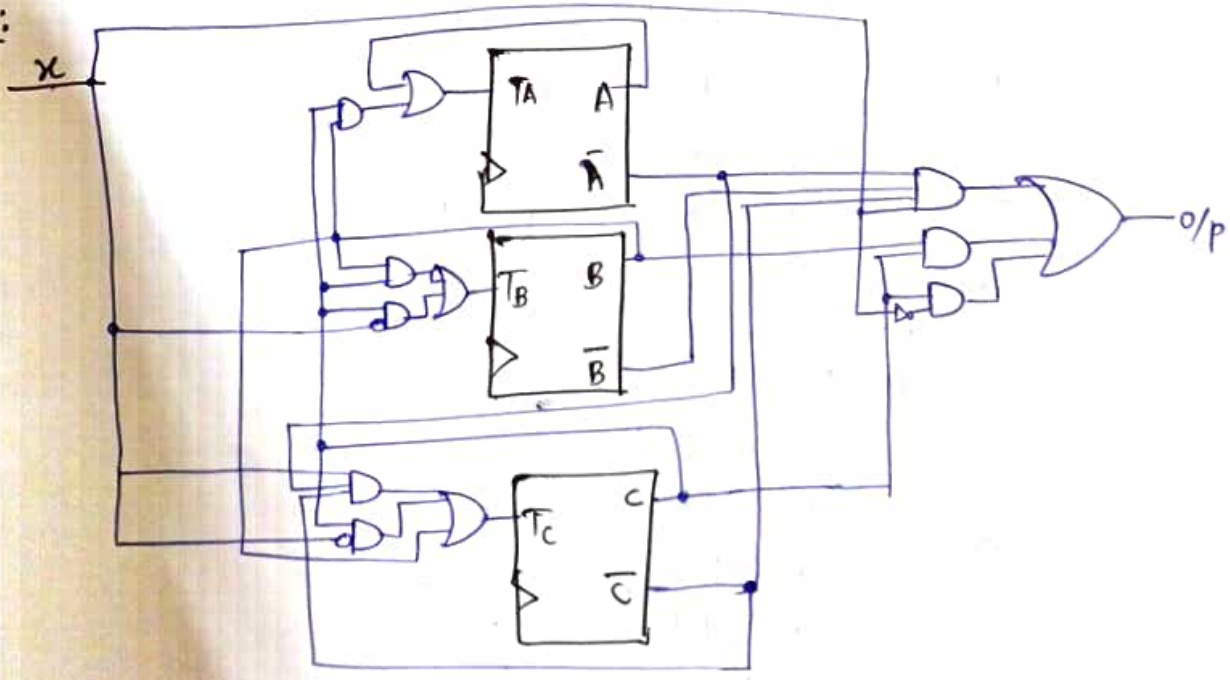


$O/P = \bar{A}\bar{B}\bar{C}x + BC + C\bar{x}$

$T_B = BC + C\bar{x}$, $T_C = C\bar{x} + B + \bar{A}\bar{C}x$

$T_A = A + BC$

Circuit:



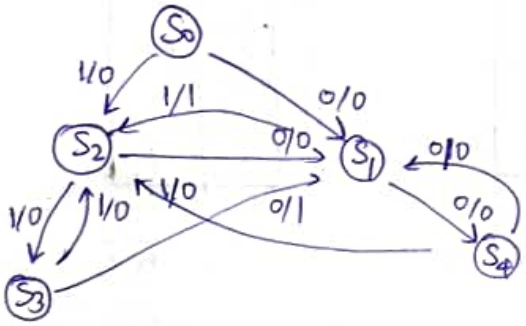
④ A finite-state machine has one input (w) and one output (z). The input 'w' is a serial input synchronised to a clock. The state machine is a part of a communication system that is using the following rules for transmission of data through the input w: If a 1 occur in the input system, then there should be an odd numbers of 1's; if a 0 occurs, then there should be an even no.s of 0's. If it is not so, then it has to report an error signal showing in the output, i.e, z=1.

w = 1110001001110000

z = 0000001000010000

Design the circuit using T flip flop.

Soln:



Assignment:

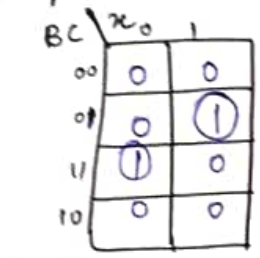
	A B C
S_0 →	0 0 0
S_1 →	0 0 1
S_2 →	0 1 0
S_3 →	0 1 1
S_4 →	1 0 0

PS	NS		O/P	
A B C	x=0	x=1	x=0	x=1
S_0	S_1	S_2	0	0
S_1	S_4	S_2	0	1
S_2	S_3	S_3	0	0
S_3	S_1	S_2	1	0
S_4	S_1	S_2	∅	∅

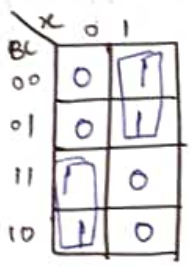
PS A B C	x	NS A B C	o/p	T_B	T_C
000	0	001	0	0	1
000	1	110	0	1	0
01	0	00	0	0	1
01	1	10	1	1	1
10	0	01	0	1	1
10	1	11	0	0	1
11	0	01	1	1	0
11	1	10	0	0	1

K-Map:

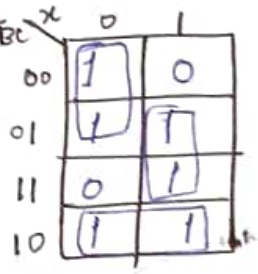
o/p:



T_B:

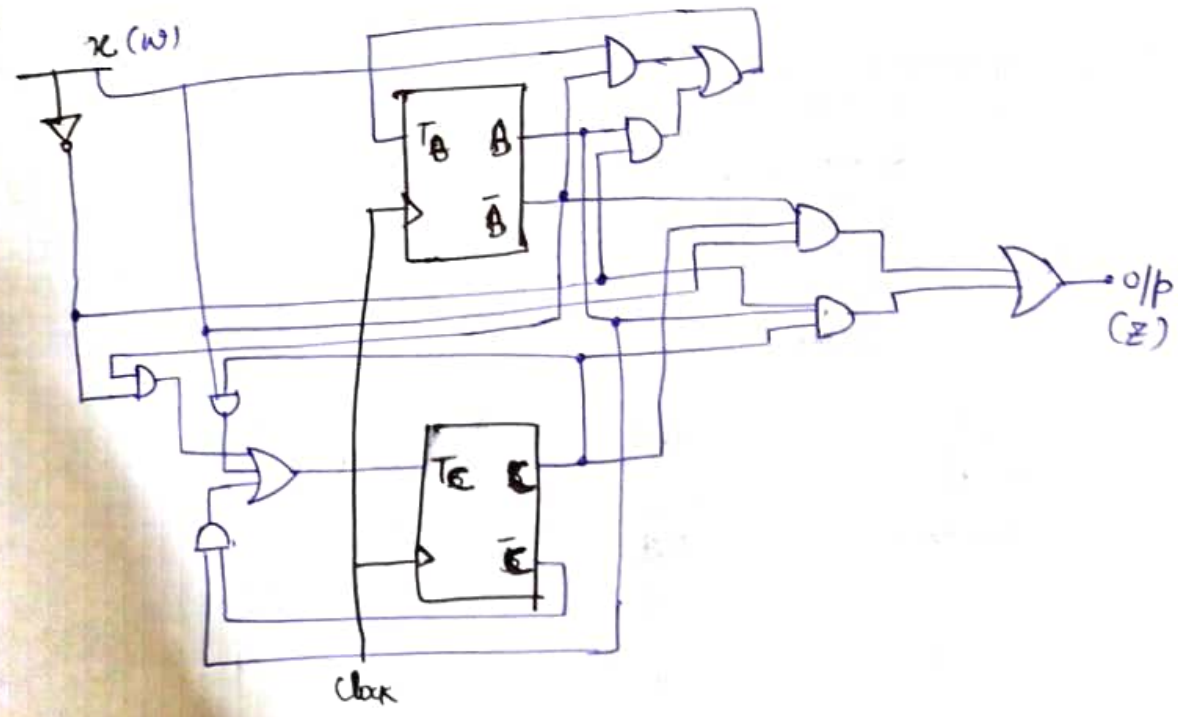


T_C:

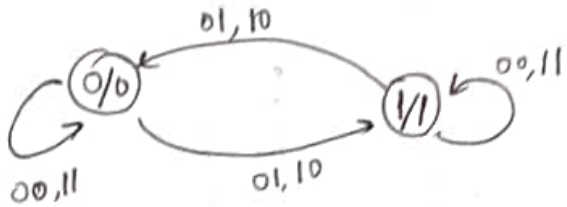


$o/p = \bar{B}Cx + BC\bar{x}$ $\quad T_B = \bar{B}x + B\bar{x}$ $\quad T_C = \bar{B}\bar{x} + Cx + B\bar{C}$

Circuit:



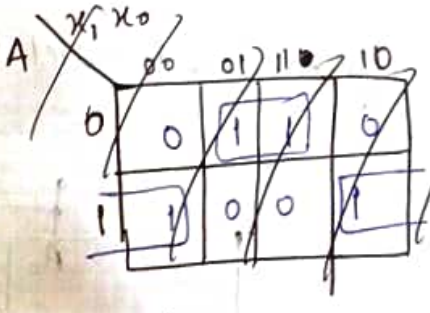
⑤ Design a sequential circuits with D flip-flops to implement the following state diagram:



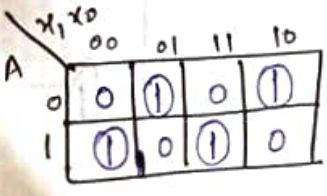
Soln: State Table:

PS (A)	Input x_1	Input x_0	NS (D_A)	O/P
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	0	1
1	1	1	1	

K-Map for D_A:



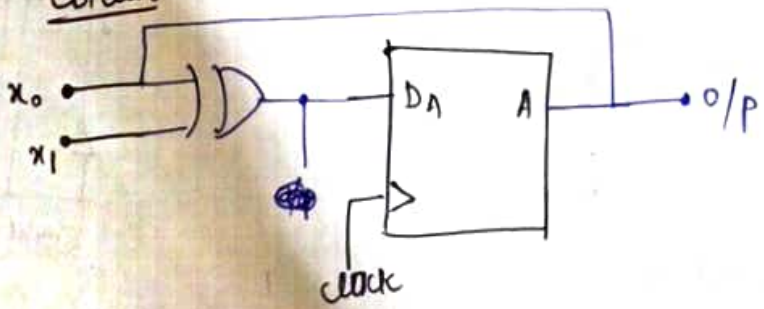
$D_A = O/P = \bar{A}$ (=NS)



$D_A = O/P = A \oplus x_1 \oplus x_0$ (=NS)

$O/P = A$

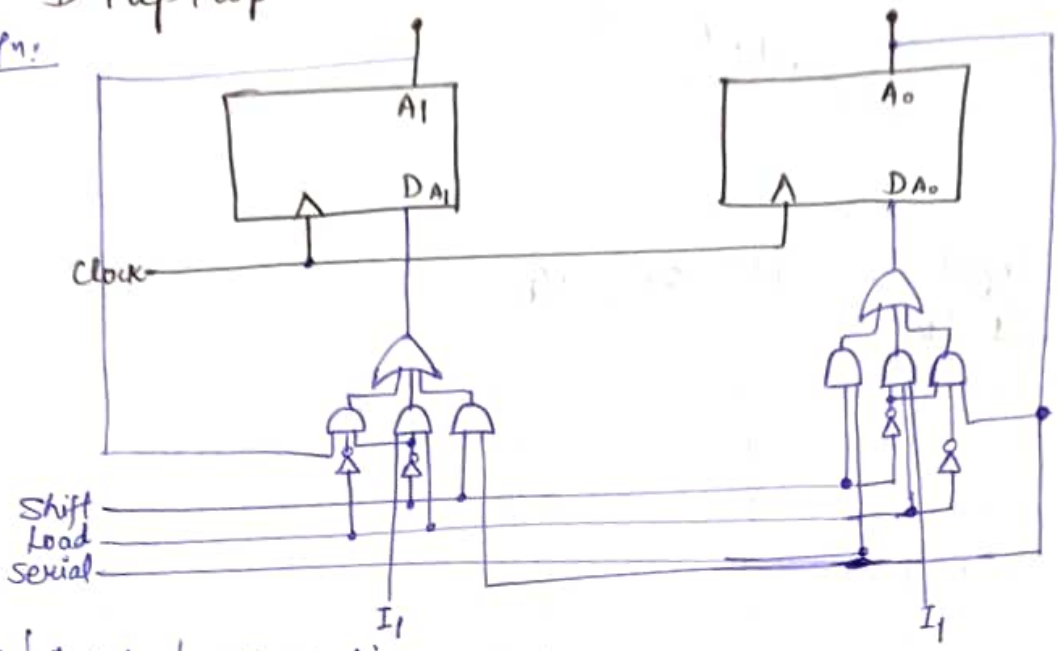
Circuit:



⑥ You only have D-Flip Flops with asynchronous preset and reset.

(i) Design 2-bit shift register with asynchronous parallel load using D Flip Flops.

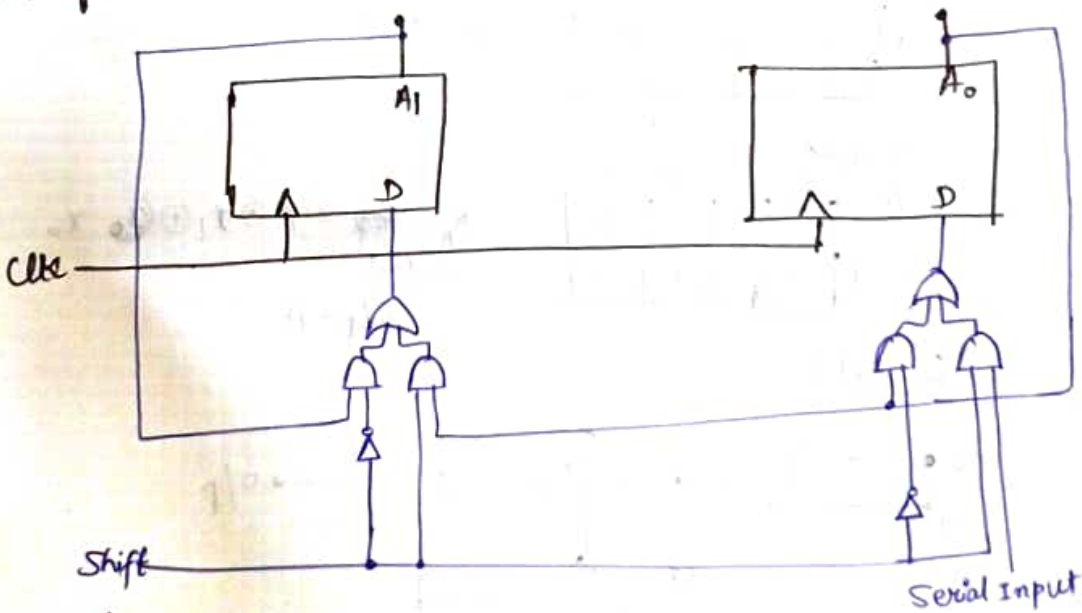
Soln:



Shift	Load	Operation
0	0	No change
0	1	Parallel load
1	x	shift from A_0 to A_1

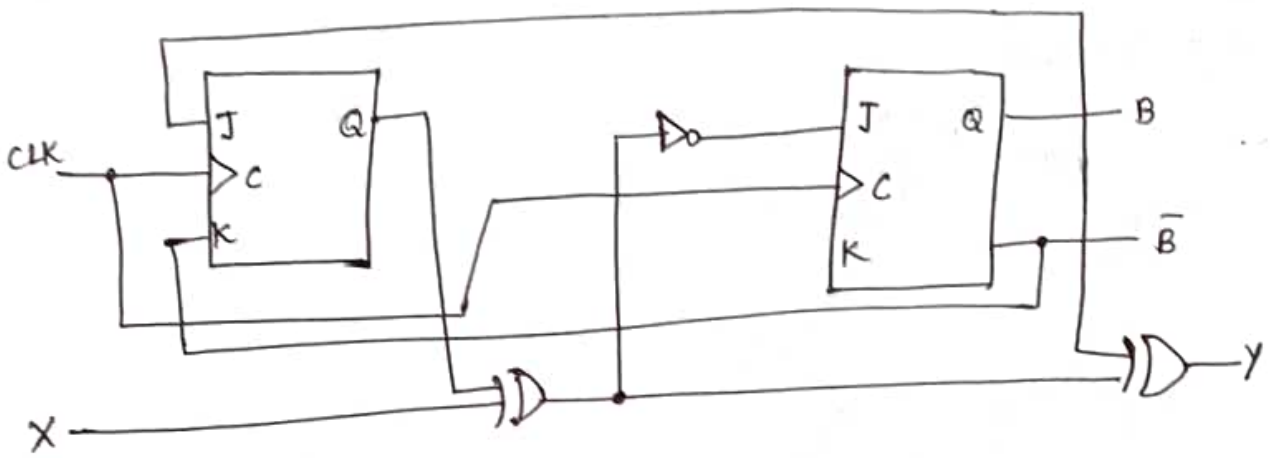
(ii) Design 2-bit shift register with asynchronous parallel load using D Flip Flops.

Soln:



Shift	Operation
0	No change
1	shift from A_0 to A_1

(7) A sequential circuit shown below has two JK Flip-Flops, one input X, and one output Y. Derive the state table and state diagram of the circuit.

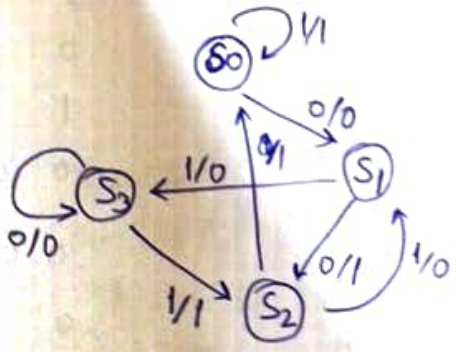


Soln: Assign the states as

$S_0 = 00$, $S_1 = 01$, $S_2 = 10$, $S_3 = 11$

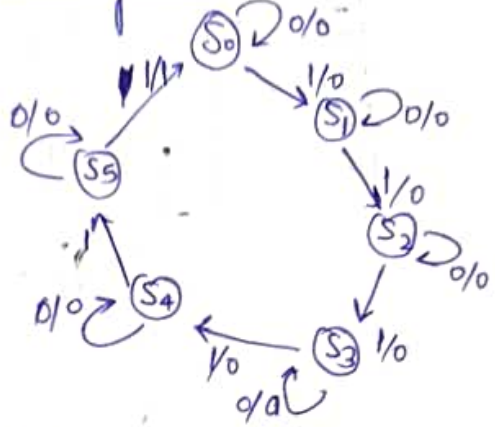
PS (AB)	X	NS (AB)	O/P	J_A	K_A	J_B	K_B
00	0	01	0	0	X	1	X
00	1	00	1	0	X	0	X
01	0	10	1	1	X	X	1
01	1	11	0	1	X	X	0
10	0	00	1	X	1	0	X
10	1	01	0	X	1	1	X
11	0	11	0	X	0	X	0
11	1	10	1	X	0	X	1

State diagram:



⑧ Design MOD 6 counter using T flip flop? If the clock frequency of the counter is 10 MHz, find the output frequencies generated by the flipflops.

Soln: State diagram:



Assignment:
$S_0 \rightarrow 000$
$S_1 \rightarrow 001$
$S_2 \rightarrow 010$
$S_3 \rightarrow 011$
$S_4 \rightarrow 100$
$S_5 \rightarrow 101$

State table:

PS (A B C)	x	NS (A B C)	O/P	T_A	T_B	T_C
0 0 0	0	0 0 0	0	0	0	0
0 0 0	1	0 0 1	0	0	0	1
0 0 1	0	0 0 1	0	0	0	0
0 0 1	1	0 1 0	0	0	1	1
0 1 0	0	0 1 0	0	0	0	0
0 1 0	1	0 1 1	0	0	0	1
0 1 1	0	0 1 1	0	0	0	0
0 1 1	1	1 0 0	0	1	1	1
1 0 0	0	1 0 0	0	0	0	0
1 0 0	1	1 0 1	0	0	0	1
1 0 1	0	1 0 1	0	0	0	0
1 0 1	1	0 0 0	1	1	0	1

K-Map:

o/p:

AB \ Cx	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	x	x	x	x
10	0	0	1	0

T_A:

AB \ Cx	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	x	x	x	x
10	0	0	1	0

T_B:

AB \ Cx	00	01	11	10
00	0	0	1	0
01	0	0	1	0
11	x	x	x	x
10	0	0	0	0

T_C:

AB \ Cx	00	01	11	10
00	0	1	1	0
01	0	1	1	0
11	x	x	x	x
10	0	1	1	0

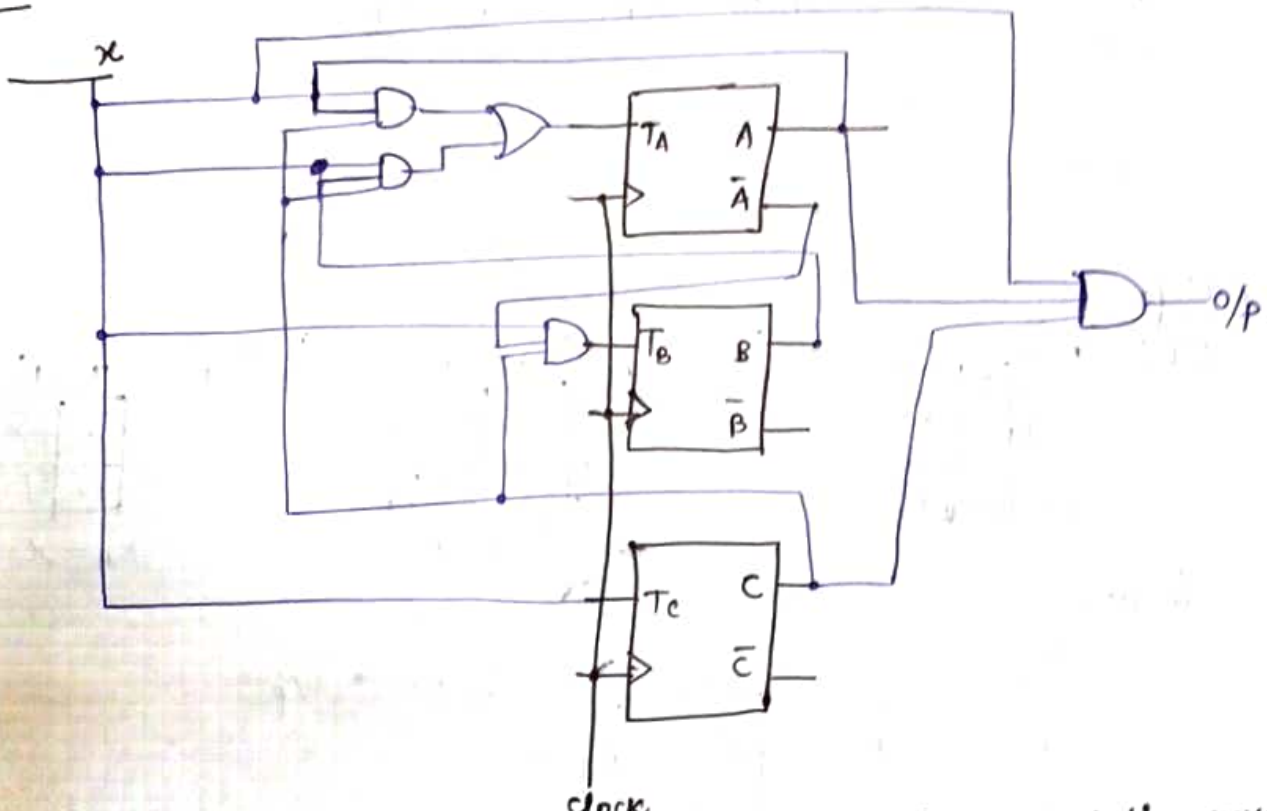
$o/p = A\bar{C}x$

$T_A = B\bar{C}x + A\bar{C}x$

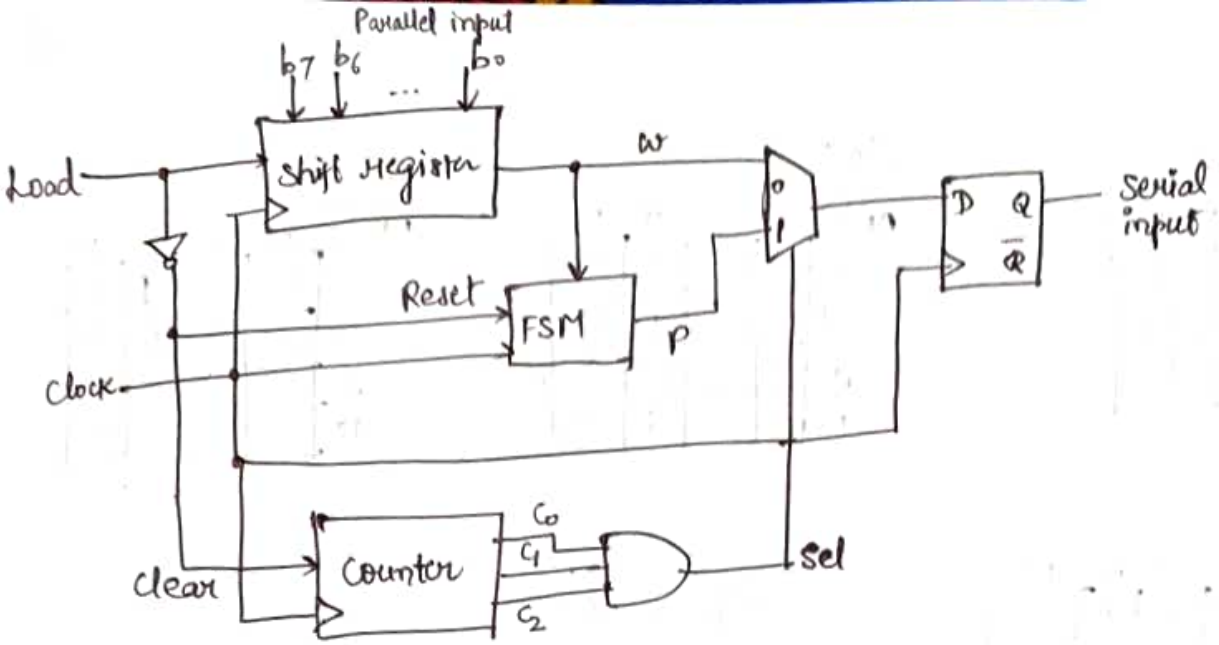
$T_B = \bar{A}\bar{C}x$

$T_C = x$

Circuit:



⑨ Consider the Block diagram. The shift register is used to convert the parallel data to serial data. The ~~sto~~ bit b7 is set 0 when the parallel input is given. Before transmitting the signal b0 to b7, a parity bit (odd) is added in the bit position b7. A FSM need to be designed to generate the parity bit and argument with the serial o/p w. A 3 bit counter is used to count from 0 to 7 and when it reaches 7, the sel line becomes high to transmit the generated parity bit. Design the FSM using JK Flip flop.



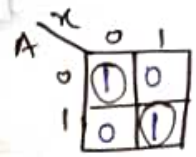
Soln: State diagram:

Assignment: $S_0 \rightarrow 0$
$S_1 \rightarrow 1$

PS(A)	x	NS(A)	o/p	J_A	K_A
(S_0) 0	0	0	1	0	X
(S_0) 0	1	1	0	1	X
(S_1) 1	0	1	0	X	0
(S_1) 1	1	0	1	X	1

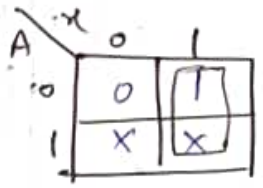
K-Map:

o/p:



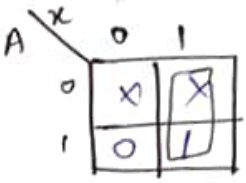
$o/p = \overline{A \oplus x}$

J_A:



$J_A = x$

K_A:



$K_A = x$

Circuit: