Indian Institute of Space Science and Technology

AV221 Digital Electronics and VLSI Design

II year ECE (Avionics)

Quiz II 31-3-2023

Answer all questions.

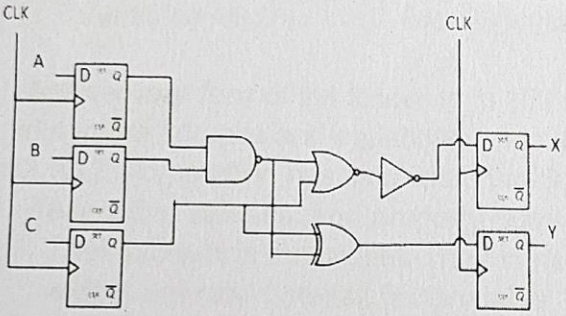
Duration : 1 hour

Marks: 20

1. We have a new type of Flip Flop with inputs A and B. if A=0 then Q'=B; if A=1, Q'=B'; Show the state diagram for this Flip Flop. Write an equation for Q* in terms. Draw the logic diagram [4]
2. (a) Design a Mealy system using T flip flop whose output (Z) is 1 for every third input (not necessarily consecutive). Draw the logic diagram. For example [5]

   X = 0 1 1 1 1 1 1 1 0 1 1 0

   Z = 0 0 0 1 0 0 1 0 0 0 1 0
3. Draw the logic diagram of a 4-bit Johnson counter and 4-bit ring counter. What is the difference between the two? If the clock frequency of the counter is 160Khz what is the output frequency obtained in the counters. [3]
4. Obtain the Maximum clock frequency for reliable operation of the circuit given below [1]
   b. What is the amount of clock skew the circuit can bear if it needs to operate at 5 Ghz. [2]
   c. How much clock skew the circuit can tolerate before it experiences a hold time violation? [2]



Gate	Tpd(ps)	Tcd(ps)
2-input NAND	20	15
2-input NOR	30	20
NOT	15	10
2-input XOR	60	40
Flip Flop Clock to Q delay	35	20
Flipflop setup time	30	
FlipFlop Hold time	10	

5. Draw the logic diagram of a 1-bit register using D flip-flops and 4 × 1 multiplexer with mode selection input s1 and s0. The register operates according to the following function table: [3]

S0	S1	Register Operation
0	0	No change
0	1	Complement the output
1	0	Register output 0
1	1	Load Parallel data