12-08-2025

Book:

- Design of Analog CMOS IC (Razavi)
- Analysis and Design of Analog IC

Course:

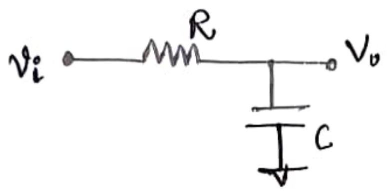
Mid-Term — 25%

Internal Assessment — 35% [cadence]

Final-exam — 40% (Formula sheet allowed)

14-08-2025

RC Circuit



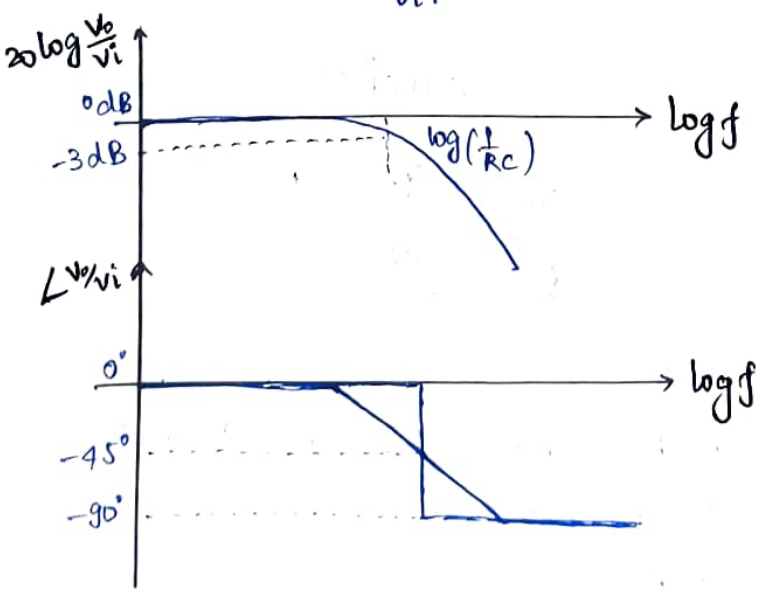
$$\frac{V_o}{V_i}(s) = \frac{1/sC}{R + \frac{1}{sC}} = \frac{1}{1+sRC}$$

Bode plot:

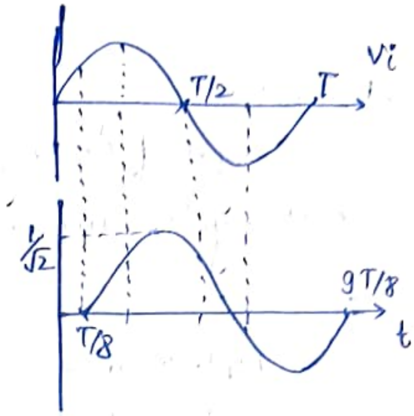
$$\left|\frac{V_o}{V_i}\right| = \left|\frac{1}{\sqrt{1+(\omega RC)^2}}\right| , \quad \omega_p = -\frac{1}{RC}$$

$\omega \to 0, \ |V_o/V_i| = 1$

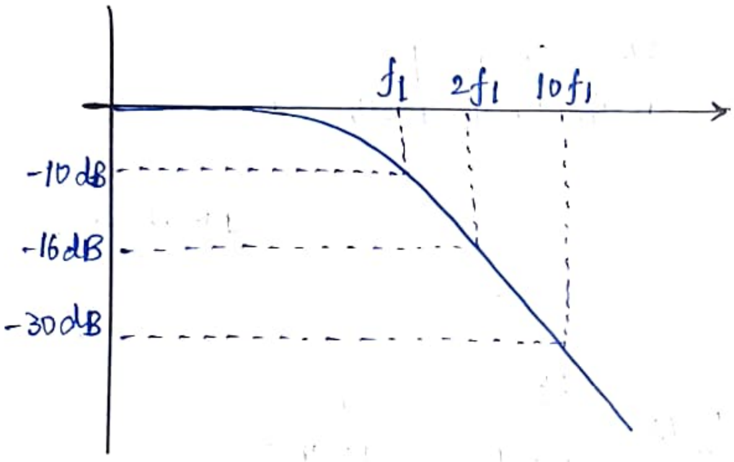
$\omega \to \infty, \ \left|\frac{V_o}{V_i}\right| \to 0, \ \angle V_o/V_i = -90^\circ$



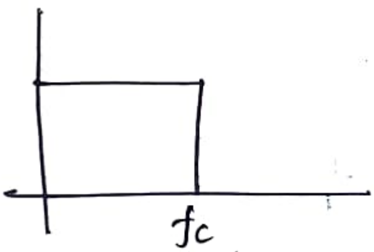
Phase of TF: W.R.T. V_{in}, how much V_{out} is being delayed.



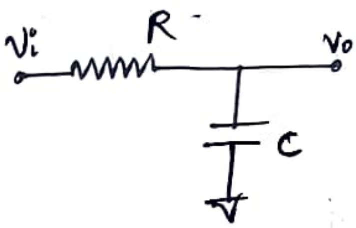
octave: twice the frequency.
decade: ten-times the frequency.



→ -20 dB/decade
→ -6 dB/octave.

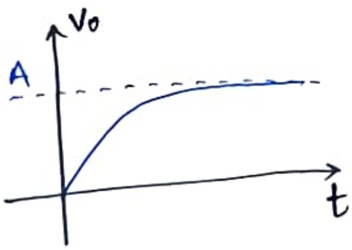


→ Ideal Lowpass frequency
(Brick-Wall Response)



$$\left|\frac{V_o}{V_i}\right| = \frac{1}{1+SRC}$$

$$V_o = \frac{A}{S(1+SRC)}$$



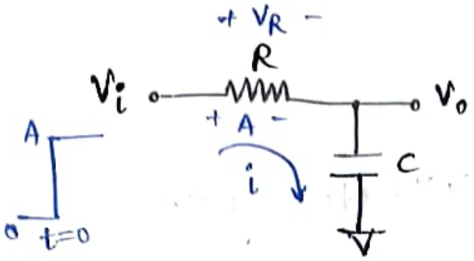
$$V_o = A(1-e^{-t/RC})$$

$$i_c = C\frac{dV_c(t)}{dt}$$

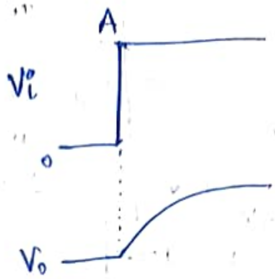
↳ capacitor can have non-zero current, but zero potential at an instant.

$$V_c(t) = \frac{1}{C}\int i\,dt$$

19-08-2025



$$f_p = \frac{1}{2\pi RC}$$



$V_o(t=0^-) = 0$

$V_o(t=0^+) = A$

$i(t=0^+) = A/R$

As $V_o \uparrow$, $V_R \downarrow$, $i \downarrow$

$$\boxed{V_o(t) = A\,(1 - e^{-t/RC})}$$

$t>0$, $A = (i)R + V_o(t)$

$$i(t) = C\frac{dV_o}{dt}$$

$$A = RC\frac{dV_o}{dt} + V_o(t)$$

$$\Rightarrow A - V_o(t) = RC\frac{dV_o}{dt}$$

$$\Rightarrow \frac{dt}{RC} = \frac{dV_o}{A - V_o(t)}$$

Integrating both sides,

$$\left[\begin{array}{l} u = A - V_o(t) \\ du = -dV_o(t) \end{array}\right]$$

$$\frac{t}{RC} = -\ln(A - V_o(t)) + K$$

At $t=0$, $V_o(t) = 0 \Rightarrow K = \ln(A)$

$$\Rightarrow \frac{t}{RC} = -\ln\left(\frac{A - V_o(t)}{A}\right)$$

$$\Rightarrow e^{-t/RC} = \frac{A - V_o(t)}{A} = 1 - \frac{V_o(t)}{A}$$

$$\Rightarrow V_o(t) = \cancel{1 A e^{-t/RC}}\ A(1 - e^{-t/RC})$$

For $V_o(t=0) = V_1$,

$$K = \ln(A - V_1)$$

$$\Rightarrow \frac{t}{RC} = -\ln\left(\frac{A - V_o(t)}{A - V_1}\right)$$

$$\Rightarrow A - V_o(t) = (A - V_1)\,e^{-t/RC}$$

$$\Rightarrow \boxed{V_o(t) = A - (A - V_1)\,e^{-t/RC}} = V_f - (V_f - V_{init})\,e^{-t/RC}$$

Time constant, $\tau = RC$

$\tau \uparrow \Rightarrow$ Slower settling

Systems: I | II [1st order system]

(3dB freq.) $f_0 = 10\,MHz$ | $f = 1\,MHz$

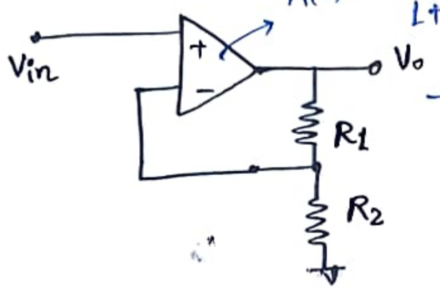
$\Downarrow$ | $\Downarrow$

(Large B/W) $f_0 \uparrow \Rightarrow \tau \downarrow$ | Slow settle

$\Downarrow$

Fast settle

$$A(S) = \frac{A_0}{1 + S/\omega_p} \quad \text{(Non-ideal/Actual)}$$



→ Non-inverting amplifier | $V_{in} = V_0 \frac{R_2}{R_1 + R_2}$

Gain : $G = 1 + \frac{R_1}{R_2}$

Neg. F/B gain: $G(S) = \frac{A(S)}{1 + \beta A(S)}$

where $\beta = \frac{R_2}{R_1 + R_2}$

$$H(S) = \frac{1}{1 + SRC} = \frac{1}{1 + S/\omega_p}$$

$[\omega_p = 1/RC]$

Non-ideal/Actual Opamp : $G(S) = \dfrac{\dfrac{A_0}{1 + S/\omega_p}}{1 + \beta \dfrac{A_0}{1 + S/\omega_p}}$

$$= \frac{A_0}{1 + S/\omega_p + \beta A_0}$$

pole : $\omega_{p_1} = \omega_p (1 + A_0 \beta)$

$$G(S) = \frac{\dfrac{A_0}{1 + \beta A_0}}{1 + \dfrac{S}{\omega_p (1 + \beta A_0)}} = \frac{\dfrac{A_0}{1 + \beta A_0}}{1 + S/\omega_{p_1}} \approx \frac{1 + R_1/R_2}{1 + S/\omega_{p_1}}$$

[Divide by $(1 + \beta A_0)$]

$\downarrow$

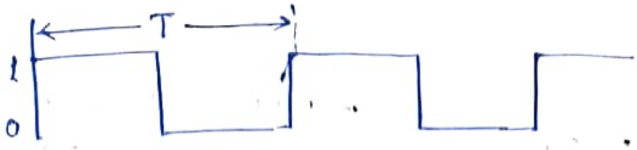
1st order system (Behaves like RC n/w)

Vin :

Vo :

(step response)

V_{in} :



[Discharges as $Ae^{-t/\tau}$]

→ RC or non-inverting amp. responses

V_o:

(i) $T/2 = 5\tau$

↳ $f_s < f_{BW}$

(ii) $T/2 = 50\tau$

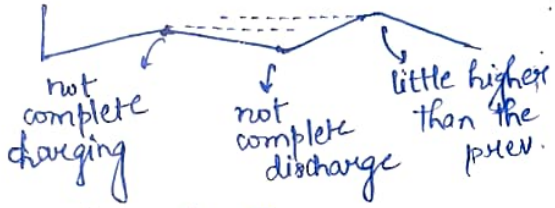
↳ $f_s \ll f_{BW}$

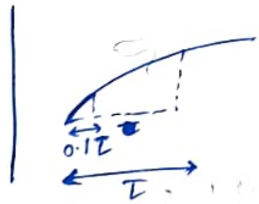
(almost square wave)

(iii) $T/2 = 0.1\tau$

↳ $f_s > f_{BW}$

signal





$\left[\tau = 1/\omega_{p1}\right]$

$\boxed{21\text{-}08\text{-}2025}$

T: Sq. wave :

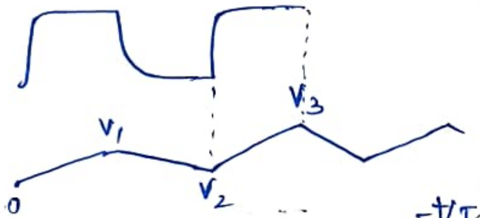
→ dc avg. = 0
($0 \to +A \Rightarrow$ dc avg. $= A/2$)

$f_{BW} \to$ amplifier

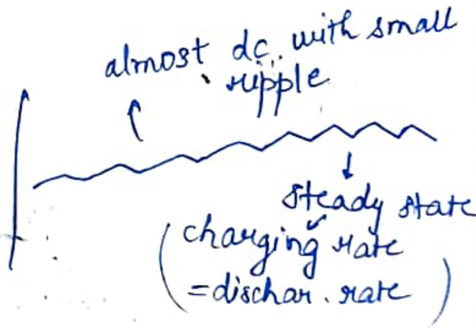
$\tau_{amp.} = \frac{1}{\omega_{BW}}$

$\tau_{amp} \ll T/2$:
($f_{BW} \gg f_{sq.}$)

$\tau_{amp} > T/2$:
($f_{BW} < f_{sq.}$)



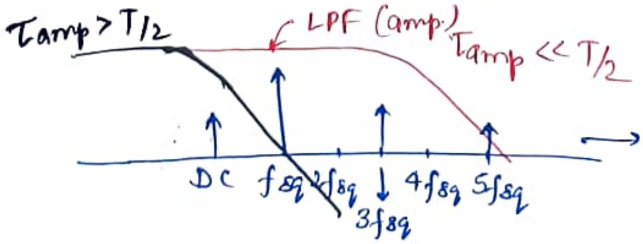
$V_1 e^{-t/\tau}$



$V_{ini} = V_2$

$V_{final} = V_{DD}$

$V_{out} = V_{DD} - (V_{DD} - V_2)\, e^{-t/\tau}$



→ squarewave components.

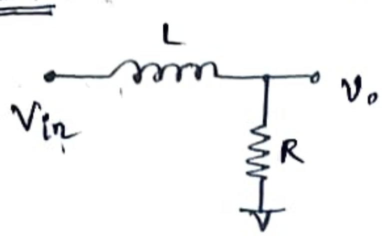
$\tau_{amp} \sim T/2$

$5\tau_{amp} = T/2$

$\Rightarrow \tau_{amp} = T/10$

$\Rightarrow 2\pi f_{BW} = 10 f_{sq}.$

LR LPF:



→ shorted dc
↳ current cannot change instantaneously.

$Z_L = j\omega L$

$|Z_L| = |\omega L|$

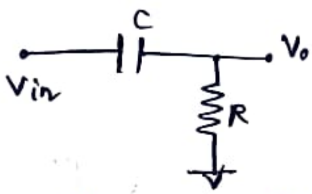
$$\frac{V_o}{V_{in}}(s) = \frac{R}{R+sL}$$

$$\omega_p = R/L$$

$$\tau = L/R$$

HPF:

RC:

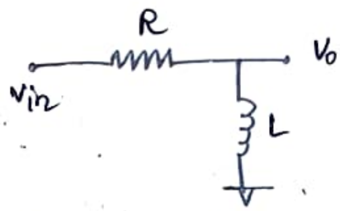


$$\frac{V_o}{V_{in}}(s) = \frac{R}{R+1/sC} = \frac{sRC}{1+sRC}$$

$$\omega_p = \frac{1}{RC}$$

$$\omega_z = 0$$

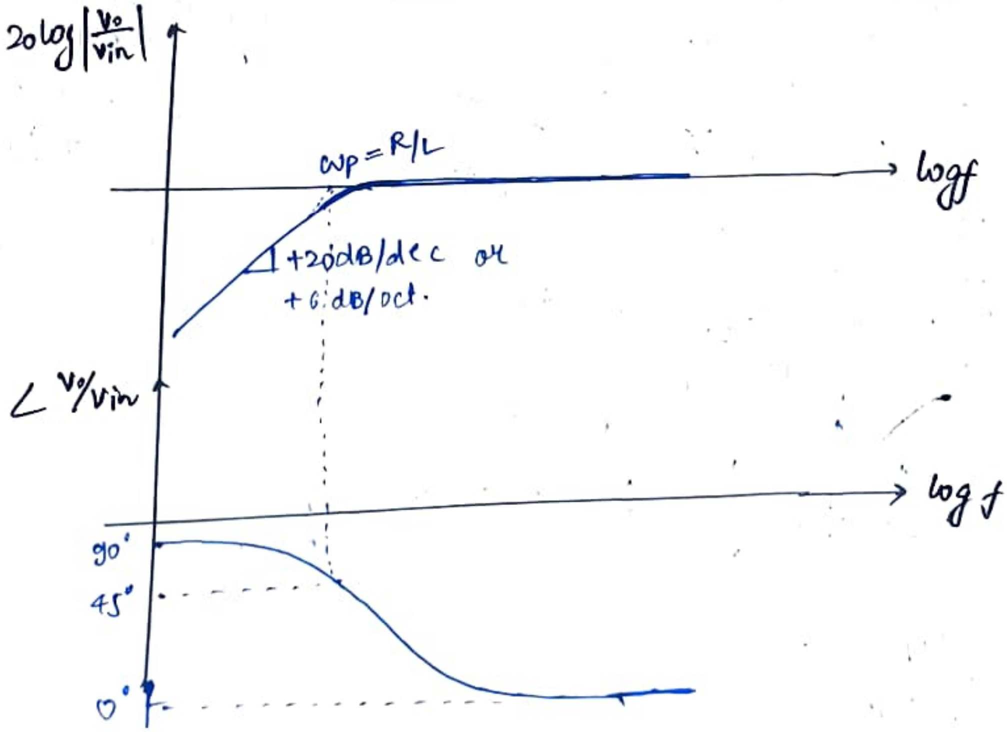
RL:



$$\frac{V_o}{V_{in}}(s) = \frac{sL}{R+sL}$$

$$\omega_p = R/L$$

$$\omega_z = 0$$

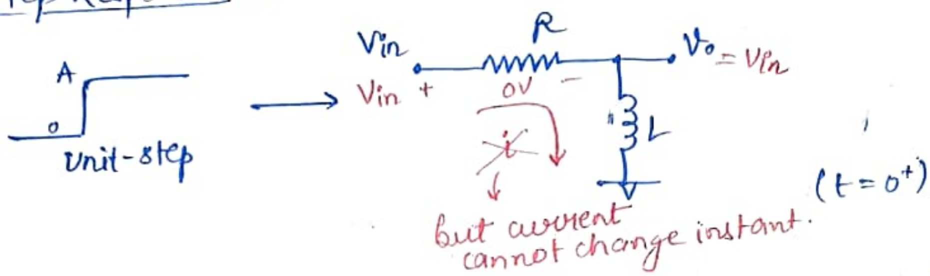


$\underline{RL}$: $\frac{V_o}{V_{in}}(s) = \frac{sL}{R+sL}$

$$\left|\frac{V_o}{V_{in}}\right| = \left|\frac{j\omega L}{R+j\omega L}\right| = \frac{\omega L}{\sqrt{R^2+\omega^2L^2}} \rightarrow \text{20dB/dec at zero}(\omega_z).$$

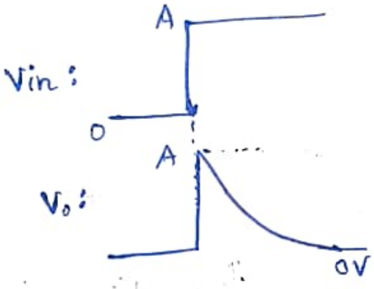
$$\angle(V_o/V_{in}) = 90^\circ - \tan^{-1}\left(\frac{\omega L}{R}\right).$$

Step Response (RL HP):

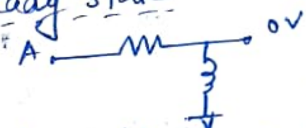


At $t=0^+$: $v_o = v_{in}$ (no current flow)
$t>0$: current starts to increase
↳ voltage across R ↑

$\left[v_L(t) = L\frac{di}{dt}\right]$



At steady state:



$i(t) = A/R \rightarrow$ constant current flows

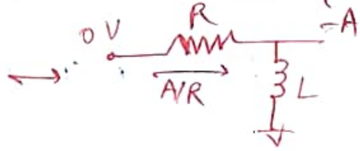
$$V_{in} = iR + L\frac{di}{dt}$$

Square-wave Response (RL HP):

$T = T_{sq}$; $f_{sq} = 1/T_{sq}$

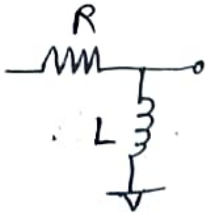
(i) $\tau \ll T_{sq}/2$:

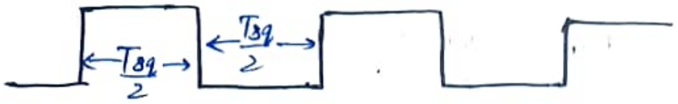
Has to be (−A) for the current to flow in the same dirn instant.



~~(ii) $\tau \gg T_{sq}/2$:~~

~~(iii) $\tau = T_{sq}/2$:~~

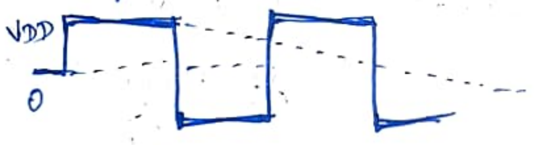




(i) $\tau \ll \frac{T_{sq}}{2}$:

(ii) $5\tau = T_{sq}/2$:

(iii) $\tau \gg T_{sq}/2$:



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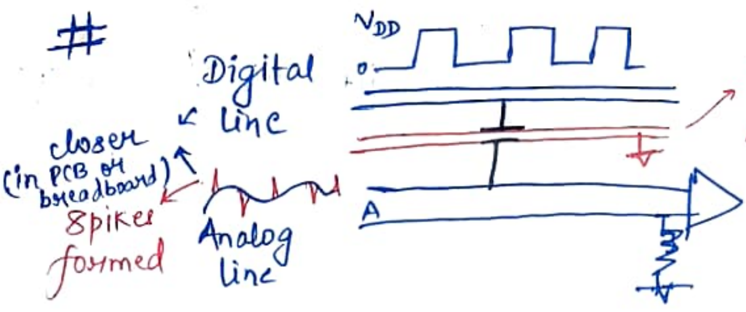
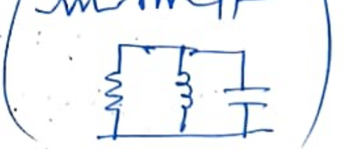


To mitigate
⇓
Add a guard line in b/w. (grounded)

Second-Order System

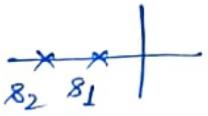
$$H(s) = \frac{N_r}{s^2 + 2\xi\omega_n s + \omega_n^2}$$

→ Any system with two poles close to each other.



Poles (s_1, s_2) conditions:

(i) s_1, s_2 both real and negative $(s_1 \neq s_2)$



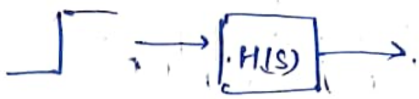
$A_1 e^{s_1 t} + A_2 e^{s_2 t}$

(Overdamped system)

(ii) s_1, s_2 are complex conjugates (LHS)

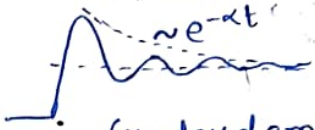
$s_1 = -\alpha + j\omega$

$s_2 = -\alpha - j\omega$



$A_1 e^{(-\alpha t + j\omega t)} + A_2 e^{(-\alpha t - j\omega t)}$

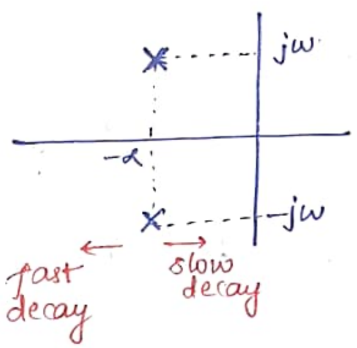
$= (A_1 + A_2) e^{-\alpha t} \cdot (\cdot)$



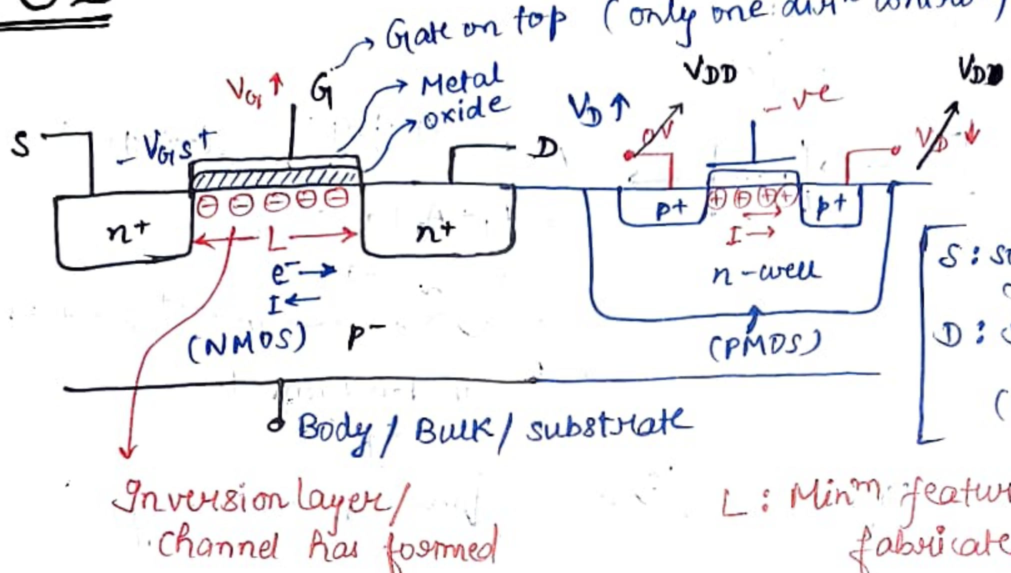
$[A e^{-\alpha t} \sin \omega t + B e^{-\alpha t} \cos \omega t]$

(underdamped system)

High α: (Faster decay)



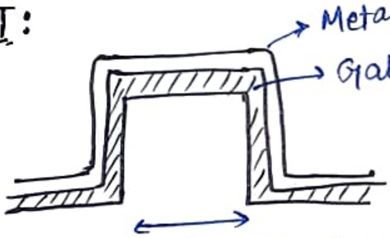
MOS



S : sources charge carriers
D : Drains charge carriers
(in any case)

L : Minᵐ feature length fabricated
↳ can go higher but not lower
↳ Any arbitrary value possible.

FINFET:



L ↳ only multiples of fin-length possible

NMOS : $V_{GS} \geq V_{THN}$ (To turn ON)

PMOS : $V_{SG} \geq |V_{THP}|$ (To turn ON)

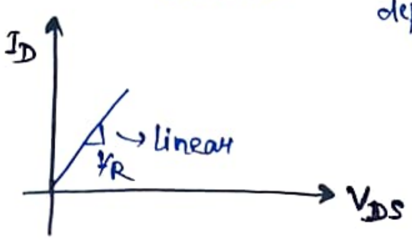
[OR $V_G < V_{DD} - V_{THP}$ → Keeping all voltages positive]

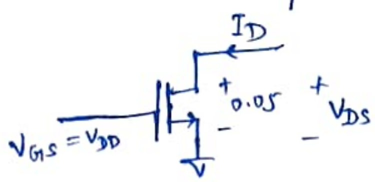
$V_{SD} > 0$ (For current flow)

Deep Triode / Linear:

$$I_D = \underbrace{\mu_n C_{ox} (V_{GS} - V_{TH})}_{\text{constant}} \underbrace{V_{DS}}_{\text{linear dependence}}$$ (For small V_{DS})

MOSFET → better switch than BJTs



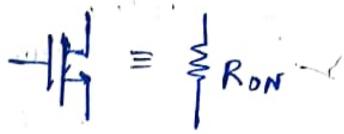


$$\left.\frac{\partial I_D}{\partial V_{DS}}\right|_{V_{GS}} = \mu_n C_{ox} \left(\frac{W}{L}\right) (V_{GS} - V_{TH}) = g_{ds}$$

↳ transconductance

On-resistance (when used as switch):

$$R_{ON} = \frac{1}{g_{ds}} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_{TH})}$$



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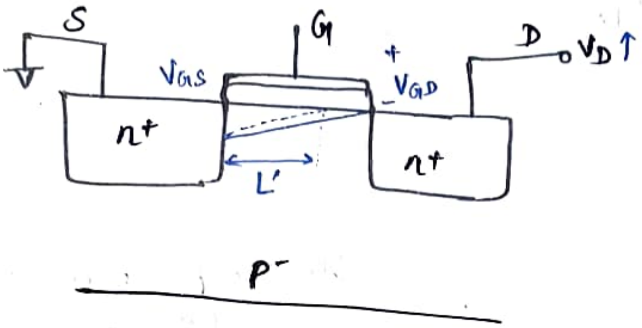


$$I_D = \mu_n C_{ox}\left(\frac{W}{L}\right)\left[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

For $V_{DS} \ll 1$,

$$I_D = \mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_{TH})V_{DS}$$

If we keep increasing V_D, at one time, the channel ceases to exist and V_{DS} loose control over the channel [Pinch-off]

↳ But current continues to flow due to energy bonds.

$V_{GD} \leq V_{TH}$

$V_{GS} - V_{DS} \leq V_{TH}$

$\Rightarrow V_{DS} \geq V_{GS} - V_{TH}$

Overdrive voltage: $V_{OV} = V_{GS} - V_{TH}$

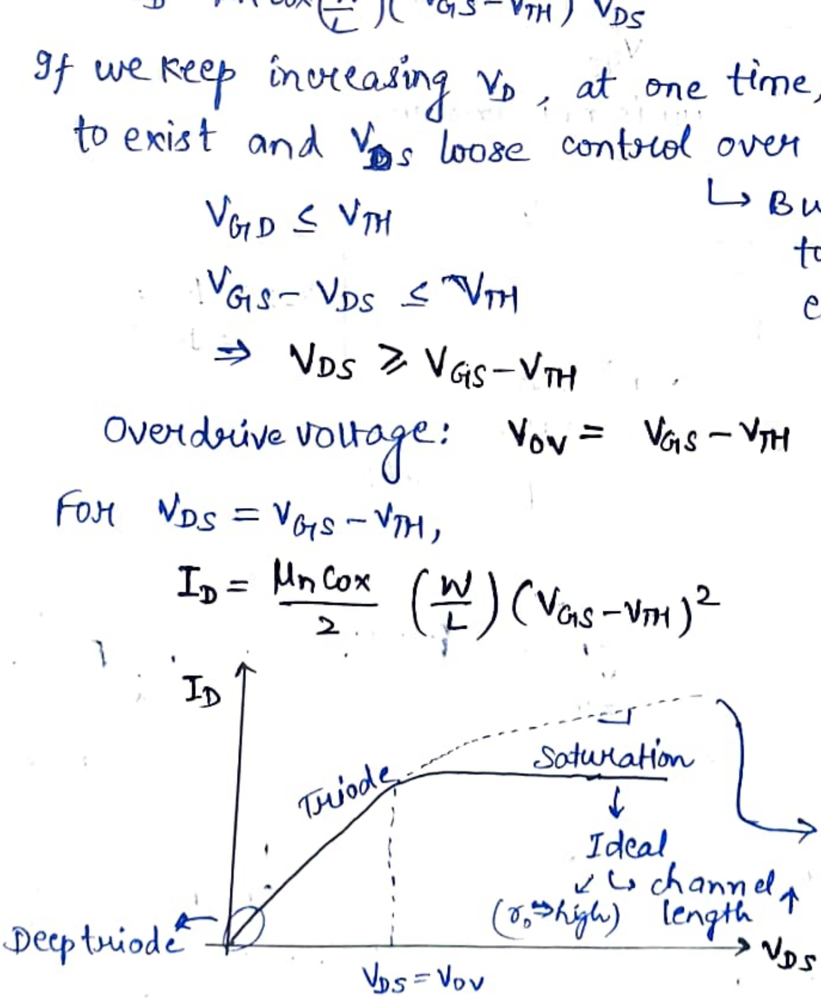
For $V_{DS} = V_{GS} - V_{TH}$,

$$I_D = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)(V_{GS} - V_{TH})^2$$

Proportionalities still work eg., $I_D \propto \left(\frac{W}{L}\right)$

↑

⇒ These equations do not work for newer technology.



→ Actual: Current is not constant but varies with V_{DS} (with a different slope) as channel length starts decreasing

↳ channel length ↓

(r_o : low)

Eg. Channel length modulation :

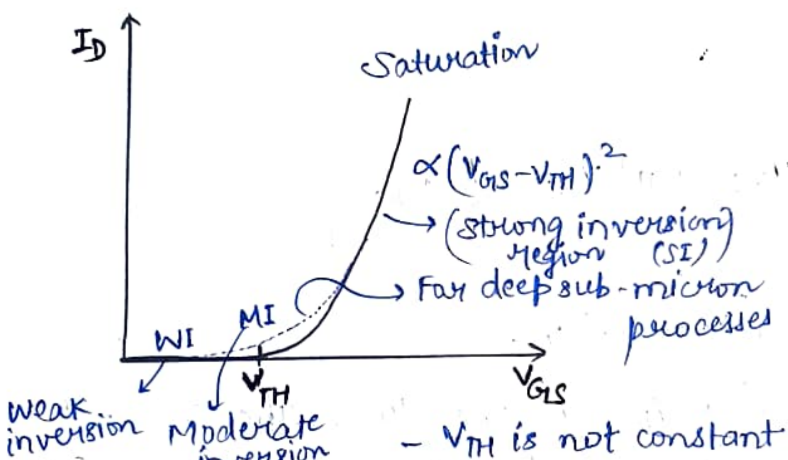
1 µm	350 nm	180 nm	60 nm	28 nm
r_o :	>	>	>	>

28 nm ↓ worst case

$$I_D = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)(V_{GS}-V_{TH})^2(1+\lambda V_{DS})$$

$$\left.\frac{\partial I_D}{\partial V_{DS}}\right|_{V_{GS}} \approx \lambda I_D = g_{ds}$$

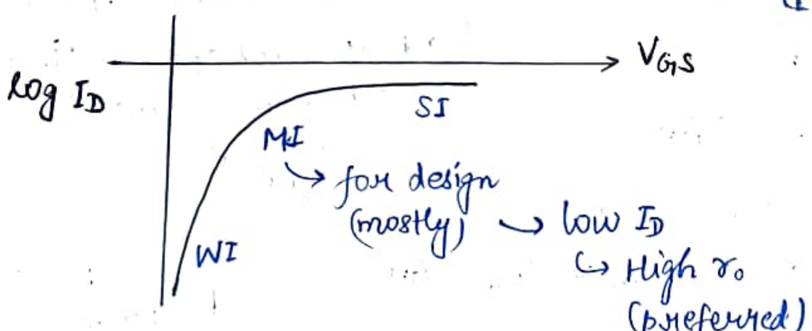
$$r_o = \frac{1}{g_{ds}} \approx \frac{1}{\lambda I_D}$$



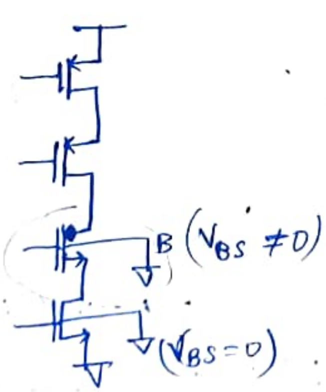
Deep sub-micron processes
↳ below ~180 nm

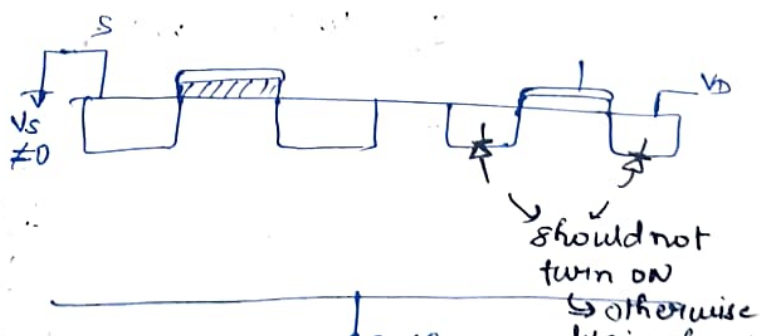
Lookup Table based design
↳ No formula

- V_{TH} is not constant



$V_{DD} = 1.2\,V$ (65 nm)
$= 1.0\,V$ (40 nm, 28 nm, ...)





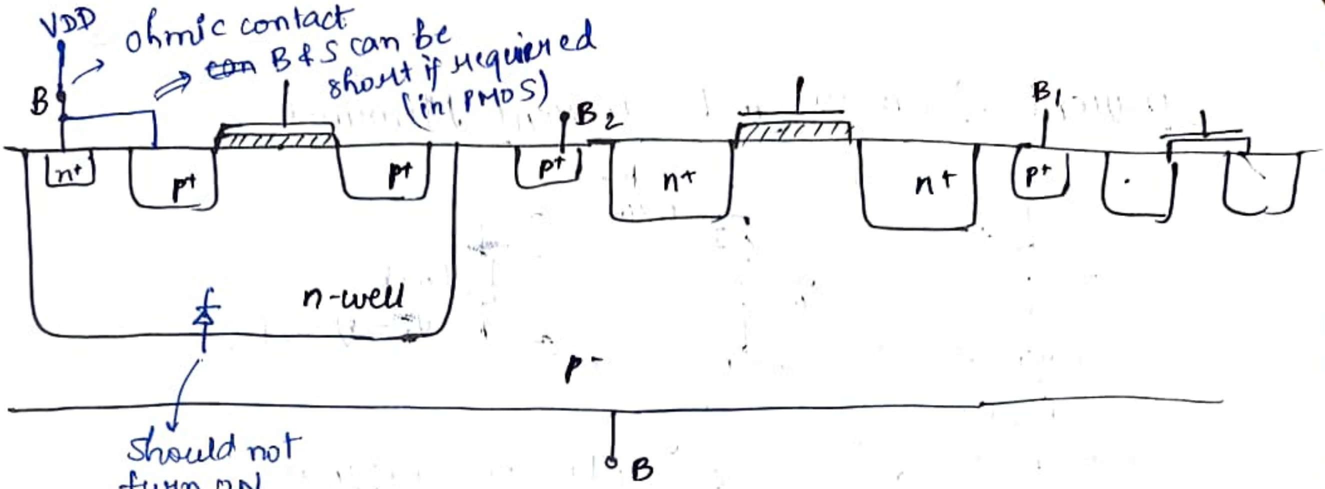
↳ Fabricated on the same substrate → share the same V_B.

should not turn ON
↳ otherwise drain shorts the body
↳ Device damage

B (Back gate)

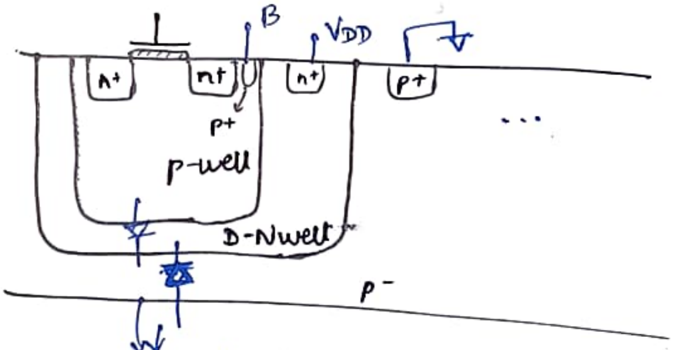
↓ connect to the lowest voltage (GND)

b/c affects V_{TH}



Should not turn ON
↳ connect B to the highest voltage (VDD)

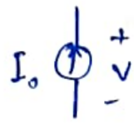
Deep N-well / Triple N-well / Tube-well :



Should not turn ON

28-08-2025

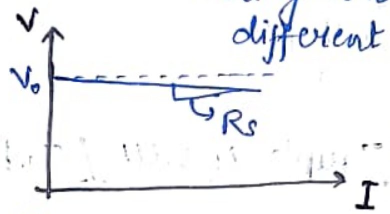
Current Sources and Current Mirrors



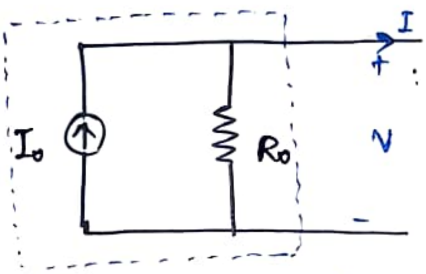
Current source
↓
constant current irrespective of V
↓
Non-ideality: Shunt resistance

$V_t = V_o - IR_S$

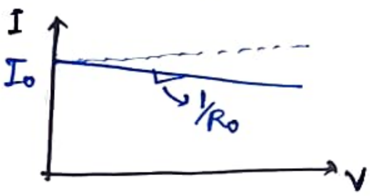
Voltage source
↓
Non-ideality: Internal resistance
↓
voltage drops with different current



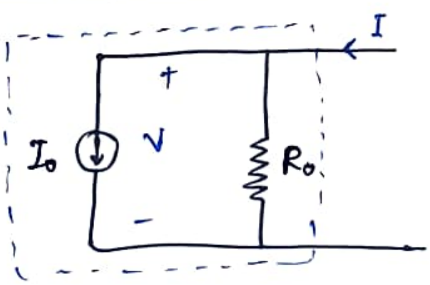
Ideally, $R_S \to 0$



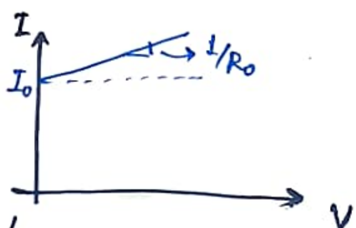
$$I = I_o - \frac{V}{R_o}$$



Current Sink:

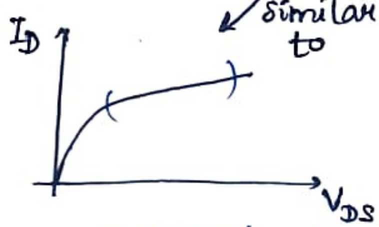


$I = I_o + V/R_o$

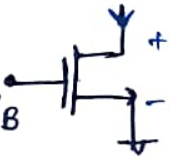


Ideally, $R_o \to \infty$

similar to



(Bias voltage) V_B



$V_{DS} > V_{DS_{sat}}$

≡

Current source to ground

$r_o = \frac{1}{\lambda I_D}$

Saturation:

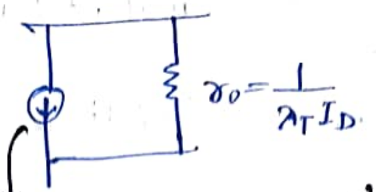
$V_{DS} \geq V_{GS} - V_{TH}$

↳ May not work (may be in sat. without satisfying this or vice versa)

Use simulators ⇑

Current source to VDD

$\equiv$



$\frac{\mu_n C_{ox}}{2} \left(\frac{W}{L}\right) (V_{GS} - V_{TH})^2$

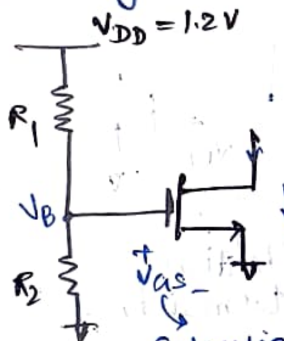
$R_S = r_o = \frac{1}{\lambda I_D}$

Ideally, $r_o \uparrow$.

$L \uparrow \Rightarrow \lambda \downarrow, \; r_o \uparrow$

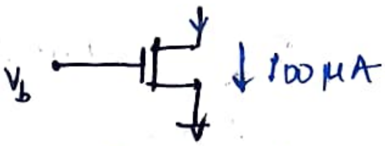
L_{min} : Technology nodes
L_{max} : Typically large
} foundary limit

Bias voltage:



V_{GS} → Get using approp. R_1, R_2.

→ Providing fixed voltage is not ideal
- ↳ temp. variation
- ↳ process variation



For fixed V_{GS},

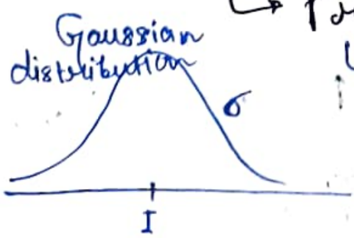
$T \uparrow \Rightarrow I_D \downarrow$ (Opposite to BJT)

↳ Heating due to internal circuitary : wires being thin & wide
(Localised Heating)

↳ Process Variation

↳ Large no. of identical devices fabricated have little different ~~to~~ responses.

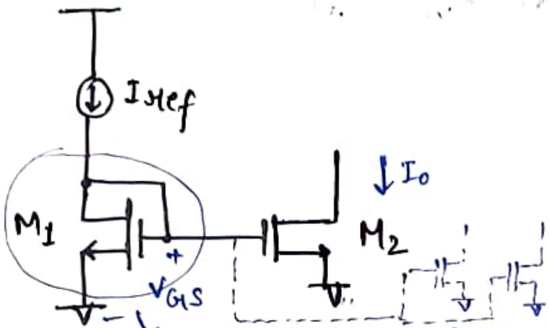
↳ Same with resistors.



Circuit to provide V_{GS}: Current Mirror

— track T

— track process variation.

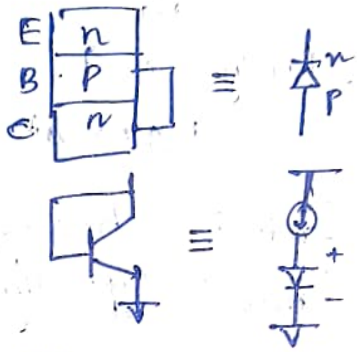


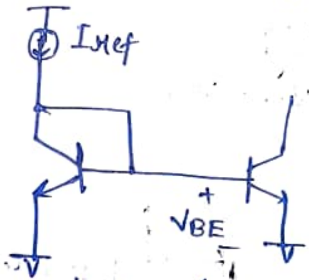
Diode-connected transistor (not an actual diode in MOS)

(any no. of transistors)

$M_1 = M_2$

$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2$

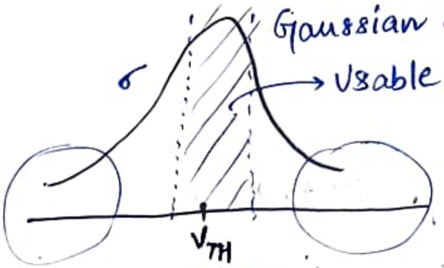




identical transistors

29-08-2025

Process Variation (Chip-to-chip variation)



Gaussian distribution

→ Usable

$V_{TH} \rightarrow \mu$

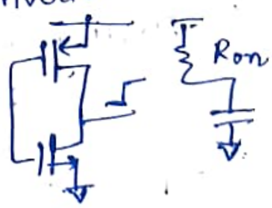
$\left.\begin{array}{l}\pm 3\sigma \\ \pm 6\sigma\end{array}\right\}$ Levels

Run simulations around process corner.

$\mu - 6\sigma$	μ	$\mu + 6\sigma$
(Fast corner)	(T) (Typical corner)	(Slow corner)

(NMOS)

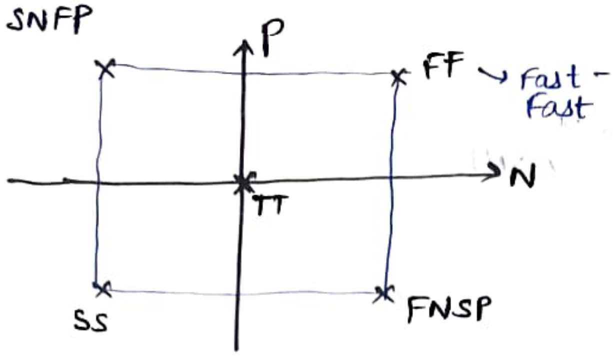
Inverter



RC-charging

$$R_{on}\uparrow = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{SG} - (V_{THP}\uparrow))}$$

↳ slow switching (as $V_{THP}\uparrow \rightarrow R_{ON}\uparrow$)



Corner Simulations :

First run simulations at TT

↓

Then at FF, SS

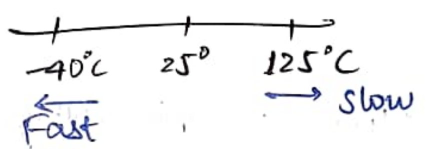
↓

Then can also be done at SNFP, FNSP.

- If they work at all, most of them (> 99.9 %) are good.

→ In Current mirror, V_{GS} adjust a/c to the corners they are running.

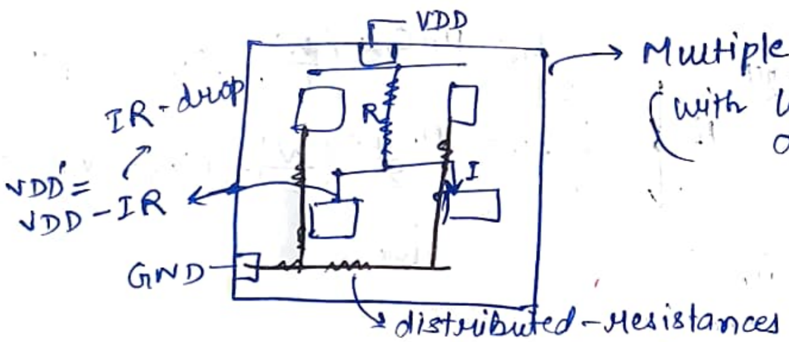
Temperature Variation :



SS (125°C) → slowest of all

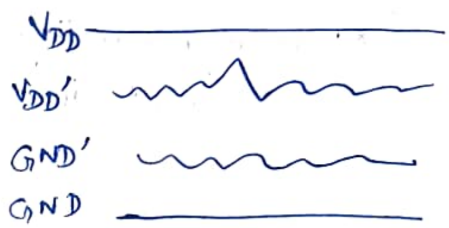
FF (-40°C) → Fastest of all

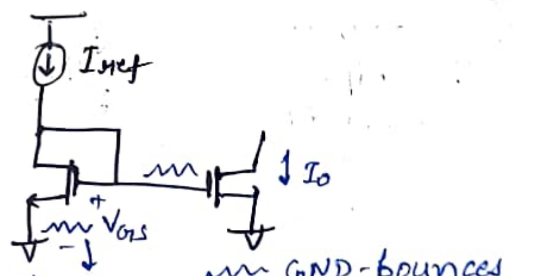
Voltage Variation :



→ Multiple stacks (with lower-tech. node, stack width also decreases ⇒ Resistance ↑)

→ Power-lines should be thick.





V_{GS} bounces accordingly ⇒ V_{GS} : constant

PVT variation : Process - Voltage - Temp Variations

↳ Design should work for atleast ± 10% power variation.

$$\underset{\substack{P \\ \text{(3-corners)}}}{3} \times \underset{\substack{V \\ (\text{V-typical}, \pm 10\%)}}{3} \times \underset{T}{3} \longrightarrow \text{Run 27 simulations}$$

(Atleast run $\underset{P}{3} \times \underset{T}{3} = 9$ simulations; V can be tolerated)

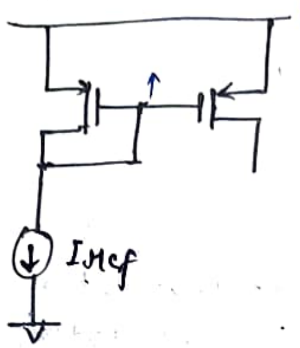
AGND —— DGND

POWER GND

DGND ⇝ doesn't affect AGND

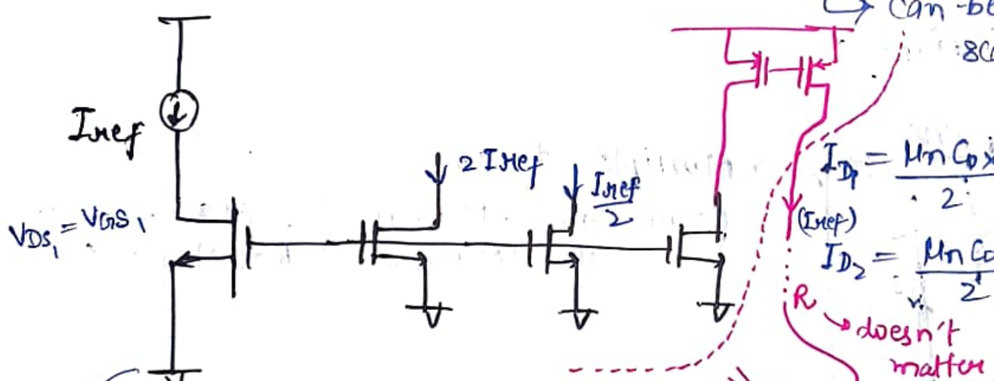
- 0 kΩ DC
- → inductor
- ↳ Ferrite-gate

PMOS-Current Mirror :



1.0V → 1.1V (±10%)

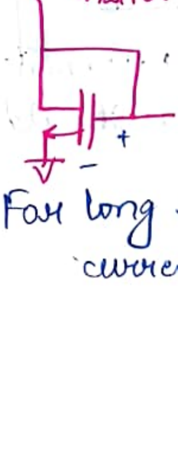
Current Mirror: Copies voltage
↳ can be used to get scaled current.



$$\left(\frac{W}{L}\right)_1 = \frac{10\,\mu m}{180\,nm} \quad \frac{20\,\mu m}{180\,nm} \quad \frac{5\,\mu m}{180\,nm}$$

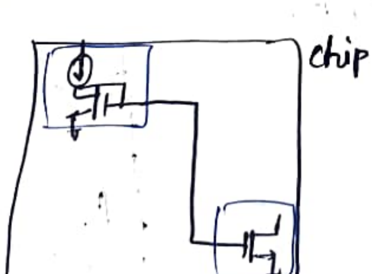
$$I_{D_1} = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_1 (V_{GS}-V_{TH})^2$$

$$I_{D_2} = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_2 (V_{GS}-V_{TH})^2$$



↳ For long routing, use current line.

Used across the chip.
↳ should be used in vicinity



$$\frac{I_{D2}}{I_{D1}} = \frac{\cancel{\frac{\mu_n C_{ox}}{2}}\cancel{\left(\frac{W}{L}\right)_2}\cancel{(V_{GS}-V_{TH})^2}(1+\lambda V_{DS2})}{\cancel{\frac{\mu_n C_{ox}}{2}}\cancel{\left(\frac{W}{L}\right)_1}\cancel{(V_{GS}-V_{TH})^2}(1+\lambda V_{DS_1})}$$

[Assume $\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2$, for now]

↳ ① **Systematic error:** If two transistors ~~of~~ have mismatched V_{DS}, then due to channel-length-modulation, they may have different I_D.

↳ If λ is very small, $I_{D_2} \approx I_{D_1}$. (r_o ↑),

↳ Solution: Increase r_o by increasing L. ⟹

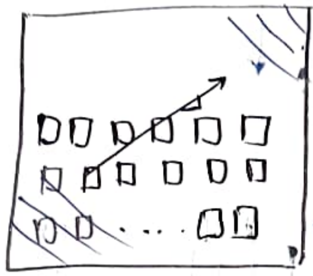
$r_o \approx \frac{1}{\lambda I_D}$

② Gradient error:

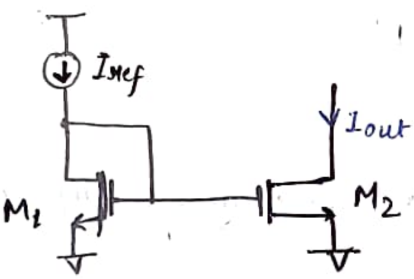
→ Even within the same die (chip), there can be gradients of variations.

↳ Not process variation.

↳ Within the same chip, two transistors may not have same V_{th}.



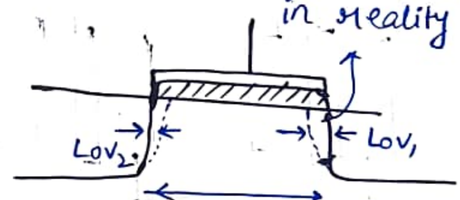
2-09-2025



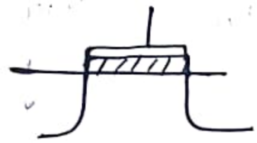
$\left(\frac{W}{L}\right)_2 = 2\left(\frac{W}{L}\right)_1$

$W_2 = W_1$, $L_2 = \frac{1}{2} L_1$ } Mathematically correct but does not work in reality

∴ Keep L constant.



$L' = L_{drawn} - L_{ov_1} - L_{ov_2}$



$L_2' = L_{2drawn} - L_{ov_1} - L_{ov_2}$

↳ does not scale properly

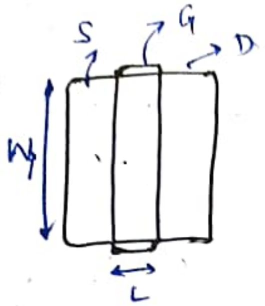
↳ No current doubling in reality

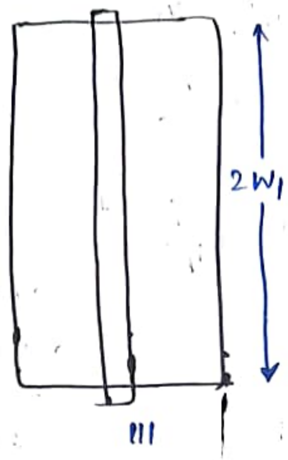
⟹ Keep L constant.

→ To increase L, for getting current mirroring, Keep $\left(\frac{W}{L}\right)$ constant

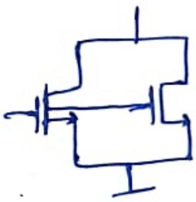
⟹ Increase W, L proportionally

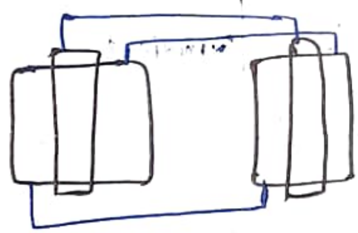
⟹ V_{GS} → little changes





→ Top view (while layouting)

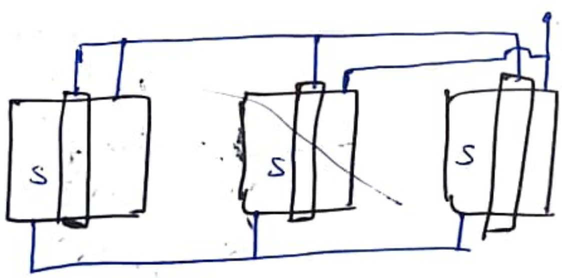




→ Use unit cells instead
↳ Any kind of scaling can be done
↳ No issues in this (inaccuracies)

$\left.\begin{matrix} W_2 = W_1 \\ L_2 = L_1 \end{matrix}\right\} M$

→



→ Best way for layouting

A B (2 transistors)

$V_{THA} < V_{THB_1} < V_{THB_2}$ [Gradient error]

↓

$\boxed{B}$ $\boxed{A}$ $\boxed{B}$ → Assuming linear gradient, avg. V_{TH} of A = avg. V_{TH} of B

↳ Common Centroid Layout
↳ All transistors have the same centroid.
↳ Linear gradient cancels out.

→ ↓ I_{ref} ↓ ½ I_{ref}

Either make W of 2nd half, but with inaccuracies, or

2 : 1.

→ For 2 transistors (2:2)

A A   B B

[B] [A] [A] [B]

OR [A] [B] [B] [A]

→ 4 : 4

[B] [A] [A] [B]
[A] [B] [B] [A]

→ 2D → Same centroid in both the axes.

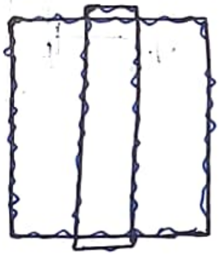
→ 1 : 8

[B] [B] [B]
[B] [A] [B]
[B] [B] [B]

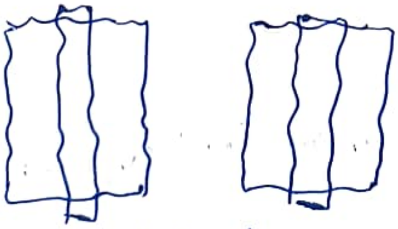
<u>Solution for gradient error</u>: Common Centroid Layout.

③ <u>Random Mismatch</u>:

These errors apply not just to current mirror, but everywhere where there is symmetry required.

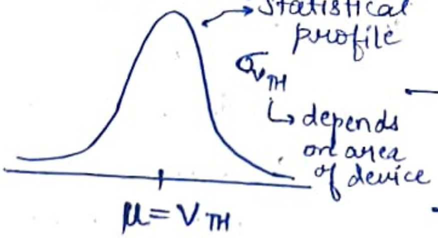


→ Jagged when ~~manufact~~ fabricated, not straight lines.



1 : 1

→ Mismatch even when no other inaccuracies
↳ cannot be predicated; can only get statistical values out of it.



→ Different from process-variation (wafer-to-wafer)
↳ interwafer variation; very high
→ Intra-wafer variation.

$$\sigma_{V_{TH}} = \frac{A_{V_{TH}}}{\sqrt{WL}}$$

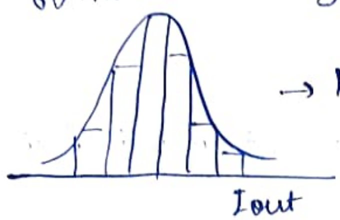
$A_{V_{TH}}$ → Pelgrom's coefficient

→ Larger random variations.

→ No real Solution
↳ Can only shift to where we want. [Increase the area]

$\frac{0.5\,\mu m}{60\,nm} \longrightarrow \frac{2\,\mu m}{360\,nm}$

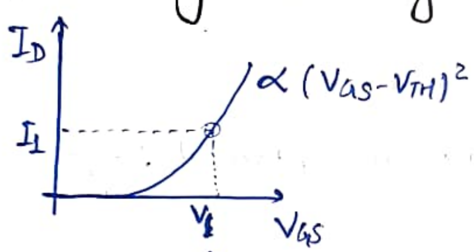
Monte Carlo ~~variation~~ analysis



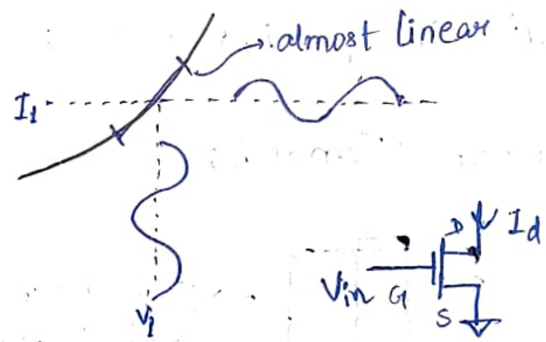
→ Histogram

04-09-2025

Small Signal Analysis



→ Non-linear → complex



apply small ac signal

$V_{in} = V_1 + V_{ac}\sin\omega t$

$|V_{ac}| \ll V_1$

$$I_d = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)(V_1 + V_{ac}\sin\omega t - V_{TH})^2$$

↓ approx.

$$I_d = I_1 + \frac{\partial I_d}{\partial V_{GS}} \cdot V_{ac}\sin\omega t \quad , \quad I_1 = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)(V_1 - V_{TH})^2,$$

$$\left.\frac{\partial I_d}{\partial V_{GS}}\right|_{V_{GS}=V_1} = \mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS}-V_{TH}) = g_m$$ → transconductance

⇓

↳ Dimensionality of conductance
↳ Trans or transferred-cond. b/c current is applied b/w D & S, and voltage b/w G and S.

$$\boxed{\begin{aligned} g_m &= \mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS}-V_{TH}) \\ &= \frac{2 I_D}{V_{GS}-V_{TH}} \\ &= \sqrt{2 I_D \mu_n C_{ox}\left(\frac{W}{L}\right)} \end{aligned}}$$

$V_{in} = V_1 + v_{ac} \sin \omega t$

$I_d = I_1 + g_m v_{ac} \sin \omega t \rightarrow$ 'g_m' works only for small signal

$I_1 = g_m V_1 \longrightarrow \times$

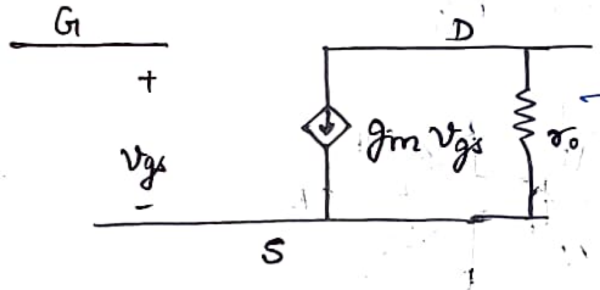
Eg: $0.5 + 1mV \sin \omega t$

$g_m = 2mS$

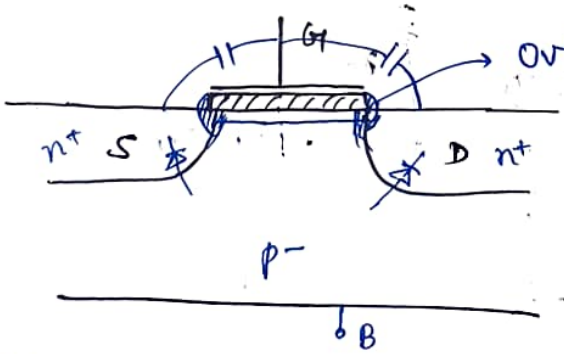
$0.5V \rightarrow 700\,\mu A$

$I_d = 0.7mA + 2\mu A \sin \omega t$

Small signal ~~Model~~ Equivalent Circuit of MOSFET:



→ captures only the incremental /ac current (actually, $I_1 + g_m v_{ac}$)



→ overlapping

Capacitance b/w gate and channel:

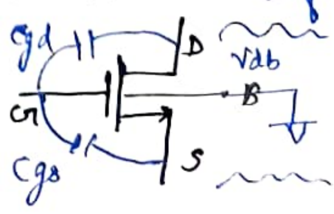
Channel capacitance $= C_{ox} WL$

↳ can be assumed to be half b/w G & S and other half b/w G & D.

$C_{gs} = \frac{1}{2} WL C_{ox}$

$C_{gd} = \frac{1}{2} WL C_{ox}$

} Linear



Capacitance due to overlapping : $C_{ov} \rightarrow$ even when channel is not formed (OFF)

$\therefore \quad C_{gs} = \frac{1}{2} WL\, C_{ox} + C_{ov}$

$C_{gd} = \frac{1}{2} WL\, C_{ox} + C_{ov}$

Junction capacitance:

1. C_{sb}, C_{db} } diode

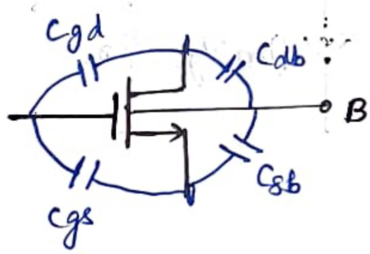
↳ Non-linear, voltage-dependent

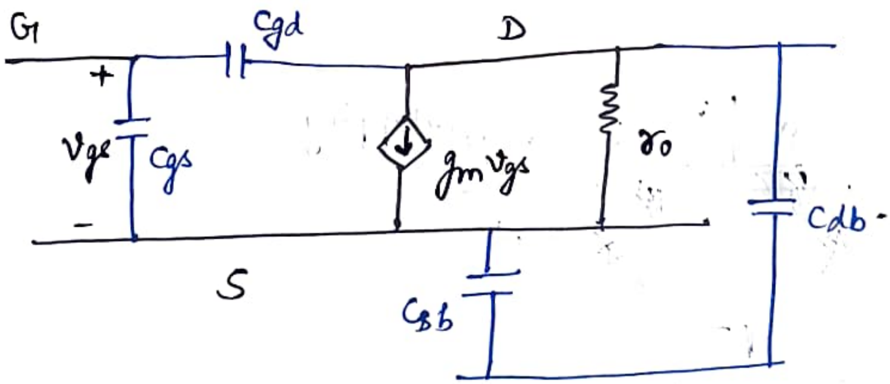
Saturation:

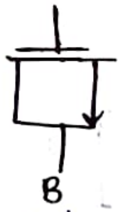
$C_{gs} = \frac{2}{3} WL\, C_{ox} + C_{ov}$ → found empirically

$C_{gd} = C_{ov}$

$C_{sb}, C_{db} \rightarrow$ as before

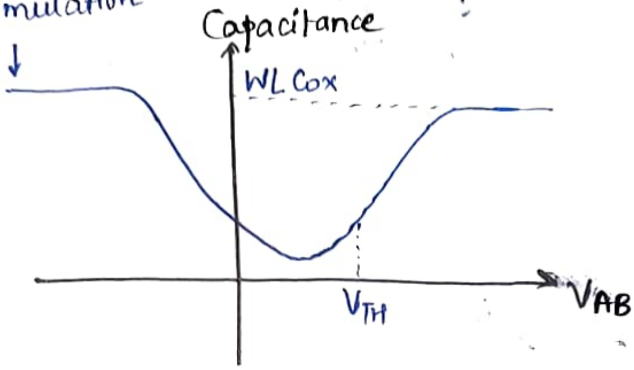




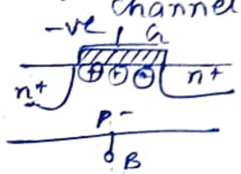


→ MOS capacitor with shorted D and S ; $V_{DS} = 0$ → linear

accumulation
↓



→ With ⊖ve V_{AB}, channel region attracts opposite charges (⊕) and forms a channel.



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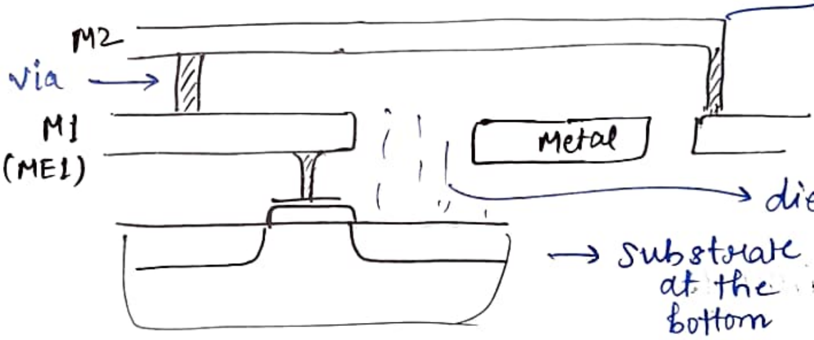
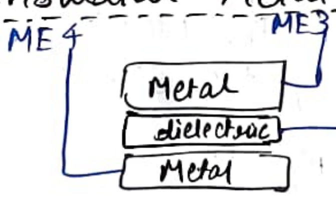


→ Metal layers

→ dielectric everywhere in b/w
↳ with different ε_r

→ substrate at the bottom

Metal-Insulator-Metal (MIM) capacitor:



→ Stack connected to existing metal layers

→ special dielectric

⇒ Height ↓, capacitance ↓

↳ 1 fF − 2 fF/μm²

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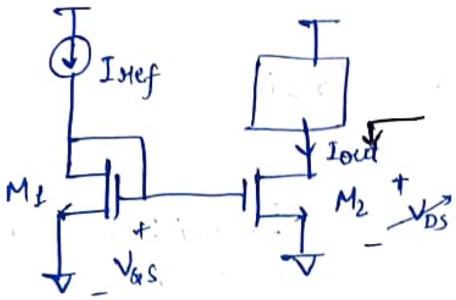
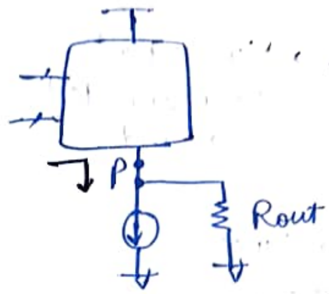
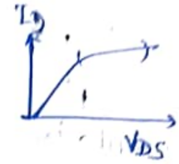


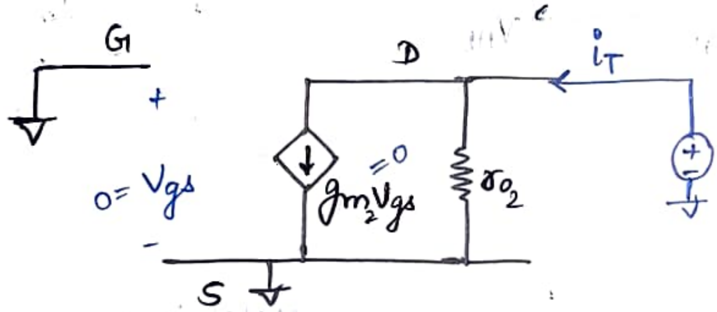
≡





$$\frac{\partial I_D}{\partial V_{DS}} = g_{ds} = \frac{1}{r_o}$$

$$I_{out} = I_o + \frac{V_P}{R_{out}\uparrow}$$

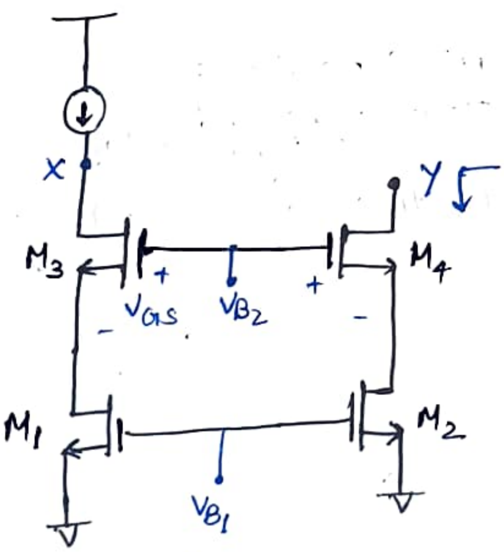


V_T (Test voltage)
↳ To calculate the impedance

$$i_T = \frac{V_T}{r_{o2}}$$

$$R_{out} = r_{o_2}$$

Cascode current Mirrors



Cascoding: Putting one on top of the other.

Top transistor : Cascoded transistor

$M_1 = M_2$, $M_3 = M_4$ } same length, same width

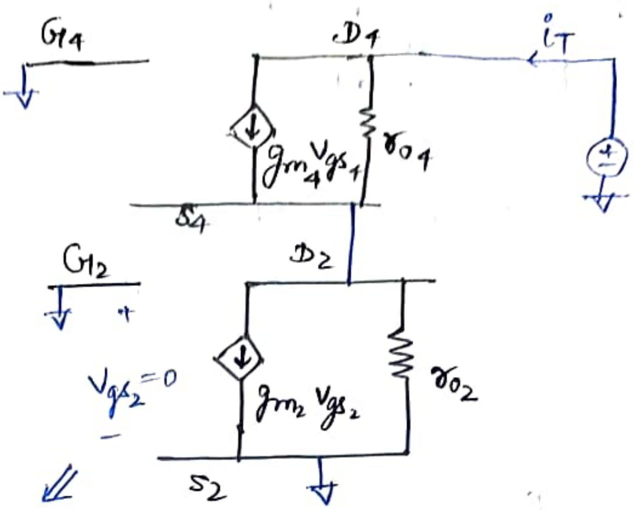
1 : 1

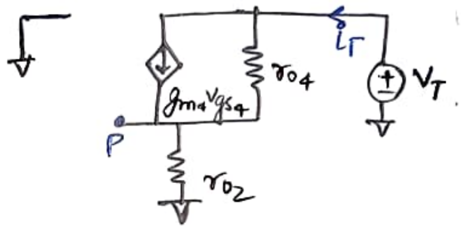
V_X may not be equal to V_Y.

$$V_{DS_1} = V_{B_2} - V_{GS_3}$$

$$V_{DS_2} = V_{B_2} - V_{GS_4}$$

Small-signal model:





$$i_T = g_{m4} v_{gs4} + \frac{(V_T - V_P)}{r_{o4}}$$

$$v_{gs4} = 0 - V_P = -V_P$$

$$V_P = i_T r_{o2}$$

$$\Rightarrow i_T = g_{m4} (-\cancel{V_P}^{\,i_T r_{o2}}) + \frac{V_T - i_T r_{o2}}{r_{o4}}$$

$$\Rightarrow \quad 1 = -g_{m4} r_{o2} + \frac{V_T/i_T - r_{o2}}{r_{o4}}$$

$$\Rightarrow \frac{V_T}{i_T} = r_{o4} + g_{m4} r_{o2} r_{o4} + r_{o2} = R_{out}$$

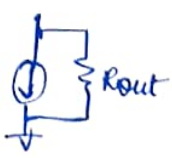
Eg. $g_m = 0.5\ mS$

$r_{o2} = r_{o4} = 10\ k\Omega$

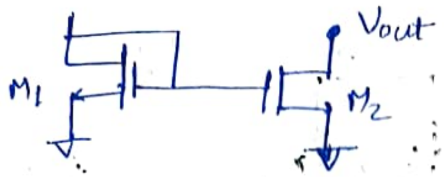
$\Rightarrow R_{out} = 20 + 50 = 70\ k\Omega \rightarrow$ o/p impandance

$10\ K \longrightarrow 70 \Rightarrow$ Larger ↑ ⇒ Better

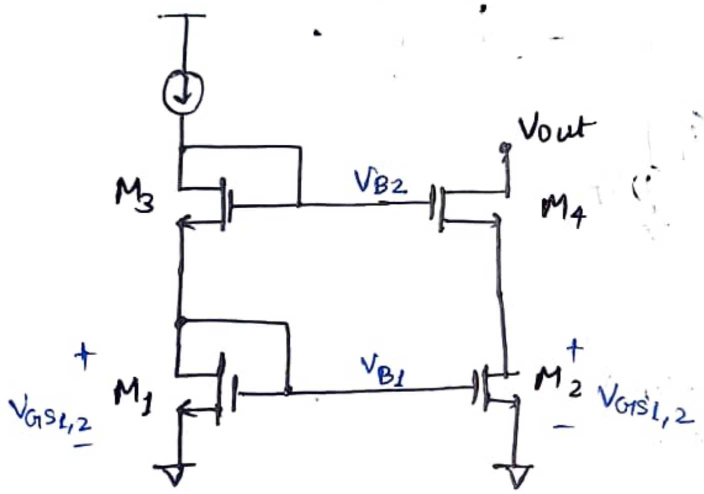
↳ stabalize the current.



#



$$V_{out,min} = V_{dsat_2} = V_{GS_2} - V_{TH_2} = V_{OV_2}$$



$$V_{out,min} = V_{dsat_4} + V_{GS_{1,2}} = V_{OV_{1,2}} + V_{TH} + V_{OV_4}$$

$$V_{DS_1} = V_{B2} - V_{GS_3}$$

$$V_{DS_2} = V_{B2} - V_{GS_4}$$

$$V_{GS_3} = V_{GS_4}$$

$$\Rightarrow V_{DS_1} = V_{DS_2} = V_{GS,2}$$

Eg.

Cascode

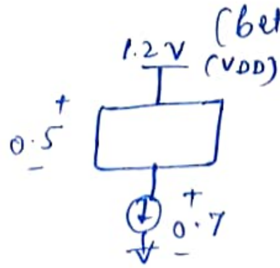
$V_{TH} = 0.4\ V$
$V_{OV} = 0.15\ V$

$V_{out,min} = V_{OV} + (V_{OV} + V_{TH})$
$= 0.7\ V$

↳ Bad idea to bias at low voltages (better for 3.3 V, 5 V, ...)

Simple

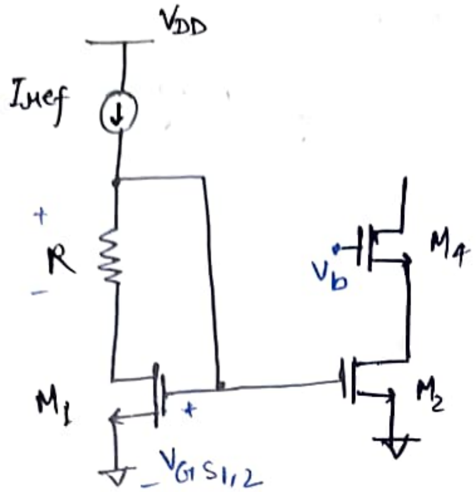
$V_{out,min} = 0.15\ V$



Disadvantage: Voltage head load.

Solution :

11-09-2025



$V_{DS1} = V_{GS1,2} - I_{ref}.R$

$V_{DS2} = V_b - V_{GS4}$

$\Rightarrow V_b = V_{DS1} + V_{GS4}$

$V_{out,min} = V_{GS1,2} + V_{dsat4}$

$= V_{TH} + V_{OV1,2} + V_{OV4} = 0.7\,V$

$\therefore V_{DS1} = V_{GS1,2} - V_{TH}$ [If $I_{ref}.R = V_{TH}$]

$= V_{OV1,2} = V_{DS2}$

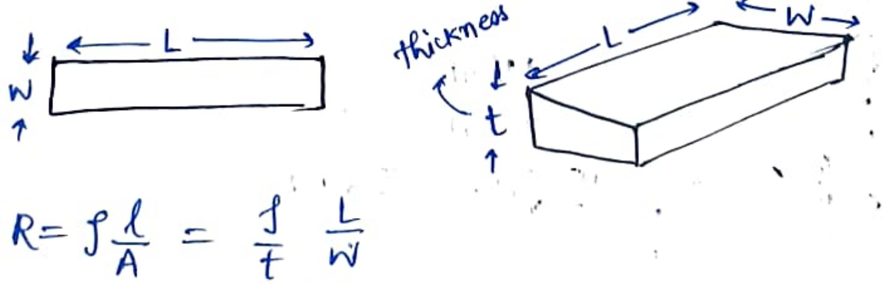
[For $V_{TH} = 0.4V$
$V_{OV} = 0.15\,V$]

$\therefore V_{out\,min} = V_{d\,sat4} + V_{DS2}$

$= V_{OV4} + V_{OV2}$

$= 0.3V$

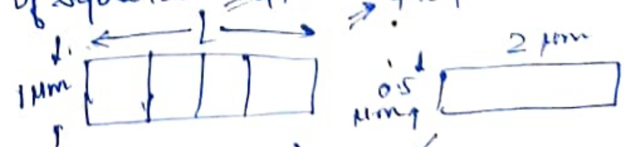
Resistance using CMOS Process :



$R = \rho\frac{l}{A} = \frac{\rho}{t}\frac{L}{W}$

$= R_s.\left(\frac{L}{W}\right)$ → No. of squares

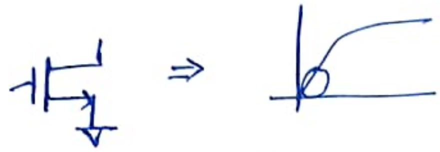
Sheet resistance



same resistance
(count no. of squares)

Types: Sheet resistance varies.

1. Diffusion (100 Ω – few kΩ)
2. Polycrystalline / Poly (Few Ω – 10k Ω)
3. High Resistance using special material in foundry.
4. Metal



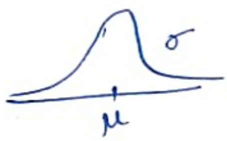
↳ In linear region
↳ voltage-dependent resistance when voltage changes.

→ Process variations in resistances, capacitances.

→ Random Mismatch in rectangles:

$$\sigma_{\Delta R/R} = \frac{A_{\Delta R/R}}{\sqrt{WL}}$$

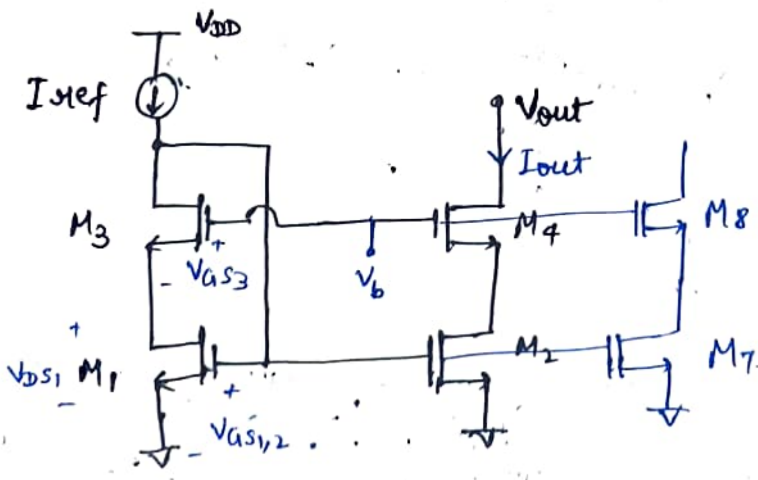
→ Increase the area to mitigate ⇒ $\sigma \downarrow$



↳ Larger random mismatch

→ Limited value resistances and capacitances can be made.

Solution:



$V_{DS_1} = V_{GS\,1,2} - V_{DS3}$

or, $V_{DS_1} = V_b - V_{GS3}$ [More ~~useful~~ useful ⇒ To do calc: in terms of V_{GS} instead of V_{DS}]

$V_{DS_2} = V_b - V_{GS_4}$

$I_{ref} = I_{out}$ and $M_3 = M_4$ } ⇒ $V_{GS_3} = V_{GS_4}$

⇒ $V_{DS_1} = V_{DS_2}$

Eg. Req. $V_{DS\,1,2} = 0.2\,V$

$V_b = 0.2 + V_{GS,\,3,4}$ [choose V_b]

$V_b = V_{DS\,1,2} + V_{GS\,3,4}$

$V_{out,min} = V_{dsat\,4} + V_{DS_2}$

Min^m V_b: $V_{b,min} = V_{GS4} + V_{OV1,2}$

Max^m V_b:

$V_{DS_3} \geq V_{GS_3} - V_{TH}$

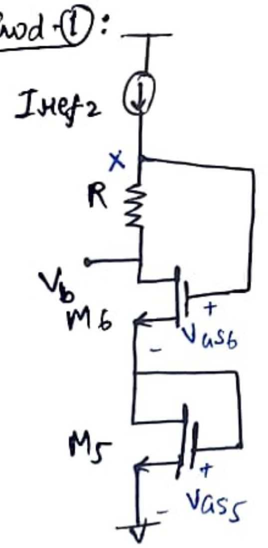
$\Rightarrow V_{GS_1} - (V_b - V_{GS_3}) \geq V_{GS_3} - V_{TH}$

$\Rightarrow V_{GS_1} - V_b + \cancel{V_{GS_3}} \geq \cancel{V_{GS_3}} - V_{TH}$

$\Rightarrow V_b \leq V_{GS_1} + V_{TH}$

V_b Generation:

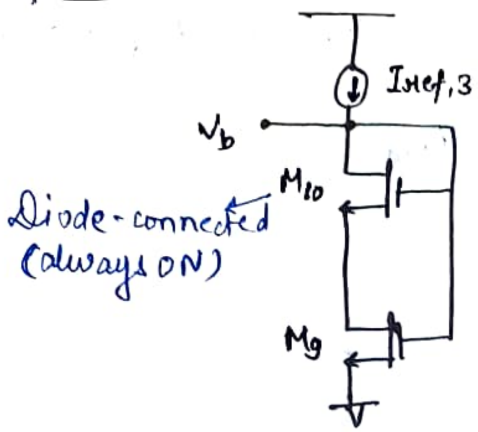
Method (1):



$V_X = V_{GS5} + V_{GS6}$

$V_b = V_{GS5} + V_{GS6} - I_{ref2} \cdot R$

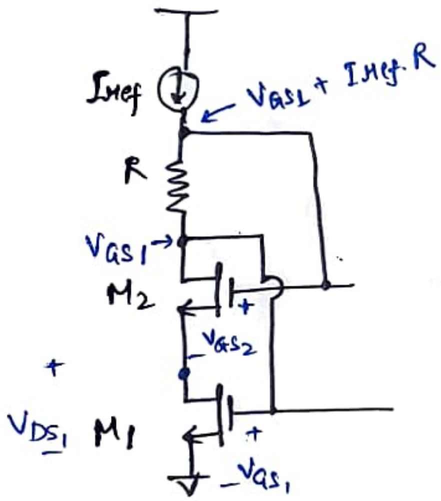
Method-2 :



$V_b = V_{GS_{3,4}} + V_{DS_{1,2}}$

↓ from M_{10}

Eg.

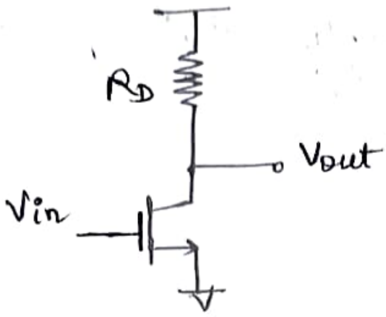


$V_{DS_1} = V_{GS_1} + I_{ref}\cdot R - V_{GS_2}$

12-09-2025

Single Stage Amplifiers

Common Source



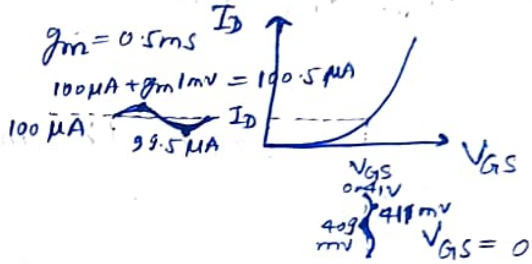
$V_{GS} \to DC$
$v_{gs} \to ac$
$V_{gs} \to DC + ac$

$$V_{in} = V_{GS} + v_{ac,in}$$

$$I_d = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} + v_{ac} - V_{TH})^2$$

$$i_d^+ = I_D + g_m v_{ac} \quad [|v_{ac}| \ll V_{GS} : \text{Small-signal approx.}]$$

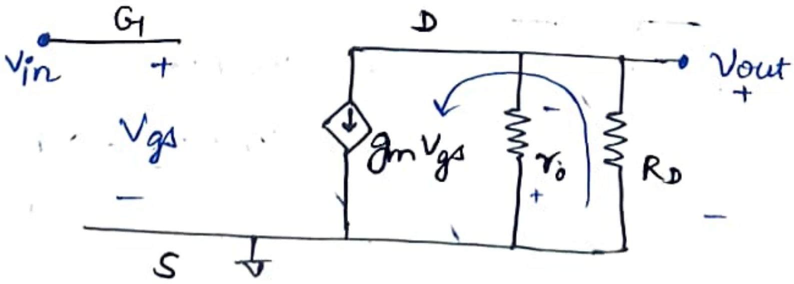
$$V_{out} = V_{DD} - I_d R_D$$
$$= V_{DD} - (I_D R_D + g_m v_{ac} R_D)$$
$$= \underbrace{V_{DD} - I_D R_D}_{DC} \underbrace{- g_m v_{ac} R_D}_{ac}$$



$V_{GS} = 0.41V$
$V_{ac} = 1mV \sin\omega t$

$$A_v = \frac{-g_m v_{ac} R_D}{v_{ac}} = -g_m R_D$$

Small-signal model:



$$V_{out} = -g_m V_{gs}(r_o \parallel R_D)$$
$$V_{in} = V_{gs}$$
$$V_{out} = -g_m V_{in}(R_D \parallel r_o)$$
$$A_v = \frac{V_{out}}{V_{in}} = -g_m(R_D \parallel r_o)$$

- In discrete transistors, r_o is very high ($\sim 10\,k\Omega$), so

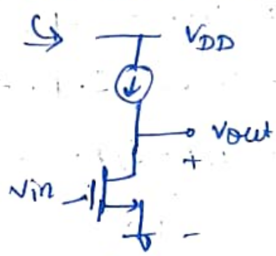
$$A_v \approx -g_m R_D$$

- For CMOS transistors, r_o is comparable to R_D.
- In linear region, r_o is much low, which brings down the gain (even <1), so for amplification, operate the transistors in saturation region.

$$V_{gs} \xrightarrow[g_m]{} i_d \longrightarrow V_{out}$$

changing current
↳ non-linear

Max. theoretical gain $= g_m r_o$: intrinsic gain
(when $R_D \to \infty$)



	350 nm	180nm	65nm	28nm
$g_m r_o$:	>		>	>

→ Limited per stage gain in lower technology.

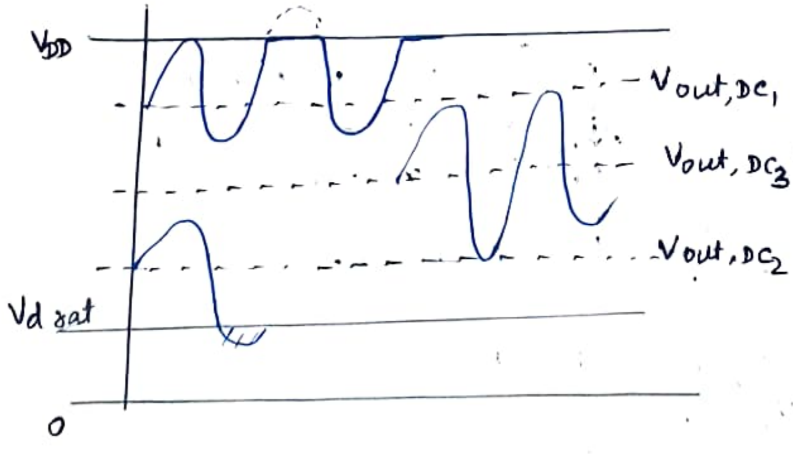
741 opamp
↳ bipolar device

DC Biasing:

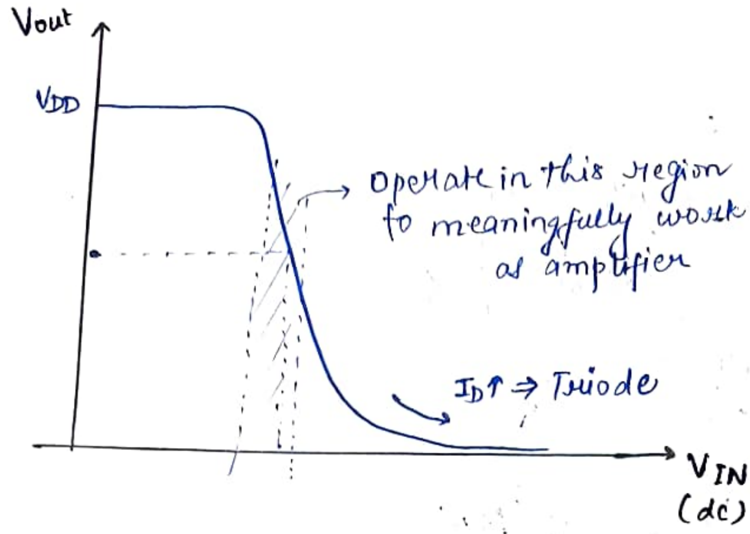
$$\downarrow V_{out,DC} = V_{DD} - I_D R_D \uparrow$$

↓

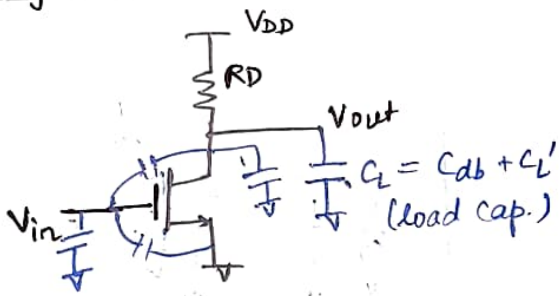
Below, $V_{out} = V_{dsat}$, the transistor will go into triode region.



→ Best option
↓
More headroom



Capacitances:

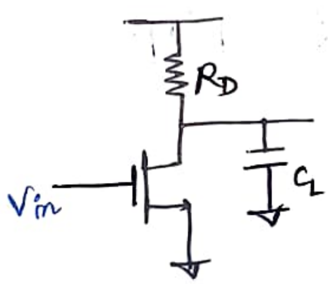


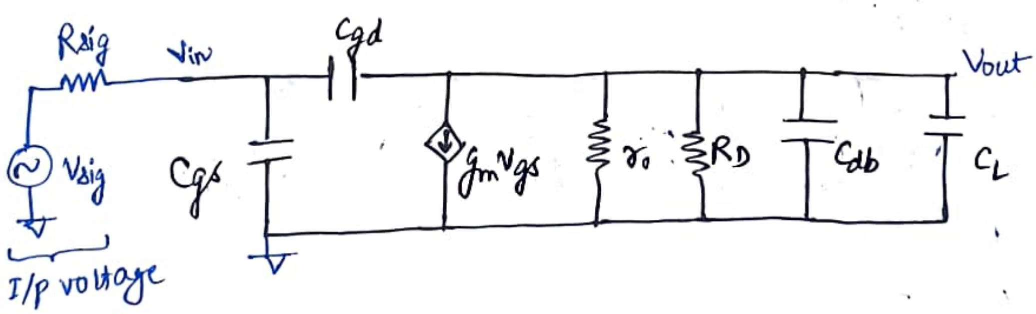
$C_{gs} = \frac{2}{3} WLC_{ox} + C_{ov}$

$C_{gd} = C_{ov}$

$C_{gd} << C_{gs}$

16-09-2025

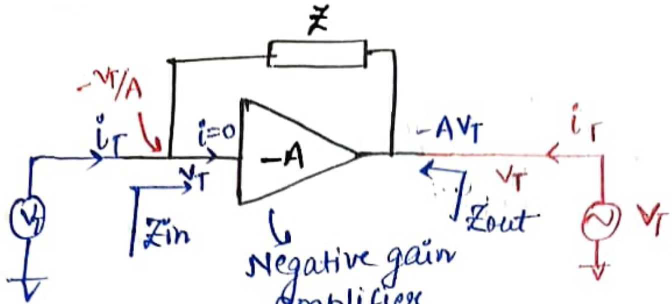




$C_{gs} = \frac{2}{3} WL C_{ox} + C_{ov}$

$C_{gd} = C_{ov}$

Miller's Theorem:



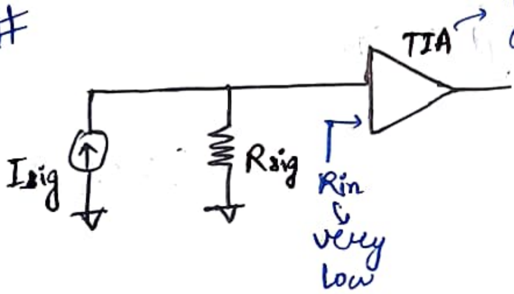
↳ Negative gain amplifier
↳ phase inversion

Input-side:

$$i_T = \frac{V_T - (-AV_T)}{Z} = \frac{V_T(1+A)}{Z}$$

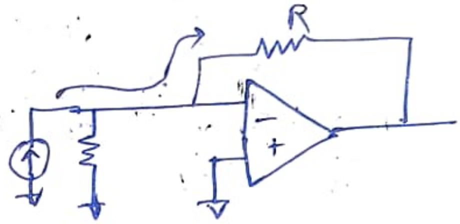
$$Z_{in} = \frac{V_T}{i_T} = \frac{Z}{A+1}$$

#



Transimpedance amplifier

R_{in} ↳ very low



Opamp-based TIA

↳ Low i/p imp.

Output side:

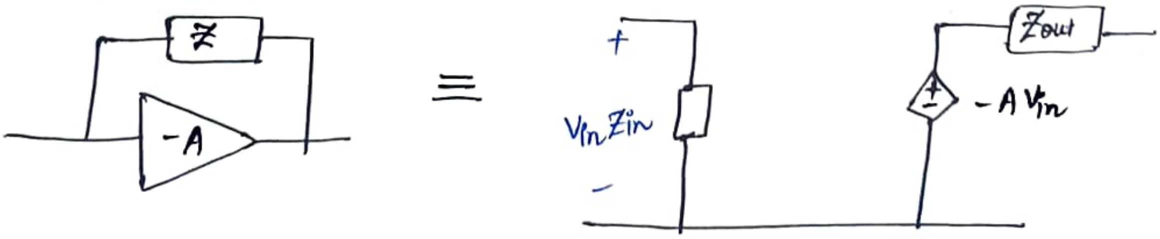
$$i_T = \frac{V_T - \left(\frac{-V_T}{A}\right)}{Z} = \frac{V_T\left(1+\frac{1}{A}\right)}{Z}$$

$$Z_{out} = \frac{V_T}{i_T} = \frac{Z}{(1+1/A)} = Z\frac{A}{1+A} \approx Z$$

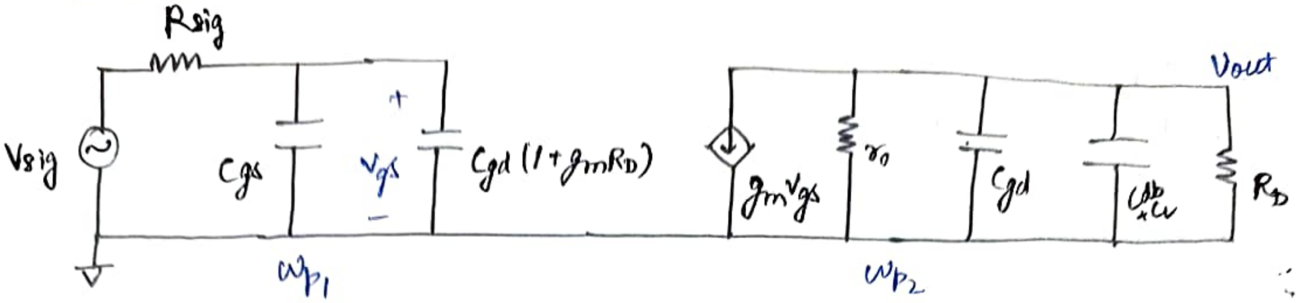
$Z_{in} = \frac{Z}{1+A}$ | R: $Z_{in} = \frac{R}{1+A}$ | L: $Z_{in} = \frac{sL}{1+A}$ | C: $Z_{in} = \frac{1}{sC(1+A)}$

$$Z_{out} = Z\left(\frac{A}{1+A}\right) \approx Z$$

Miller's theorem:



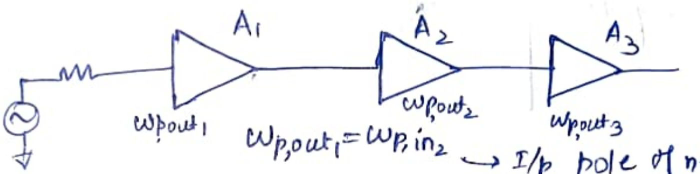
Redraw the circuit:



$$\omega_{p_1} = \frac{1}{R_{sig}\left(C_{gs} + C_{gd}(1+g_m R_D)\right)}$$

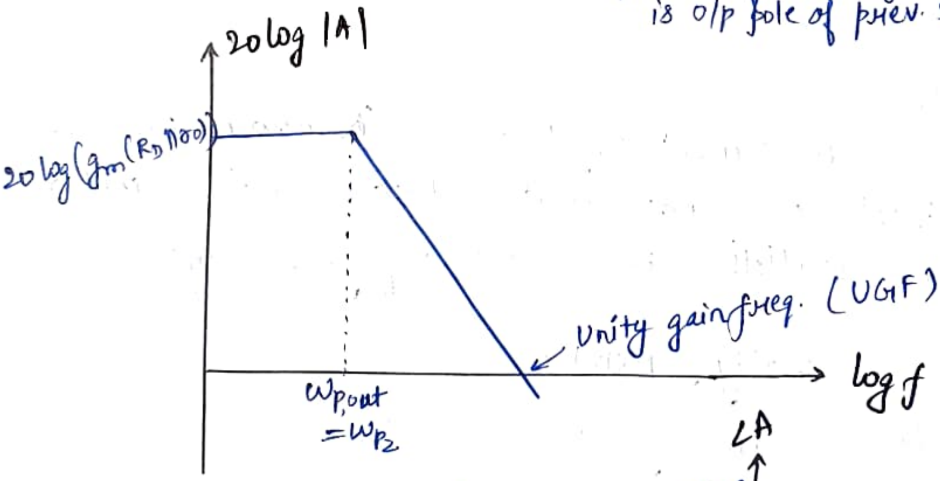
✓ $$\omega_{p_2} = \frac{1}{(R_D \parallel r_o)\,(C_{gd} + C_{db} + C_L)}$$

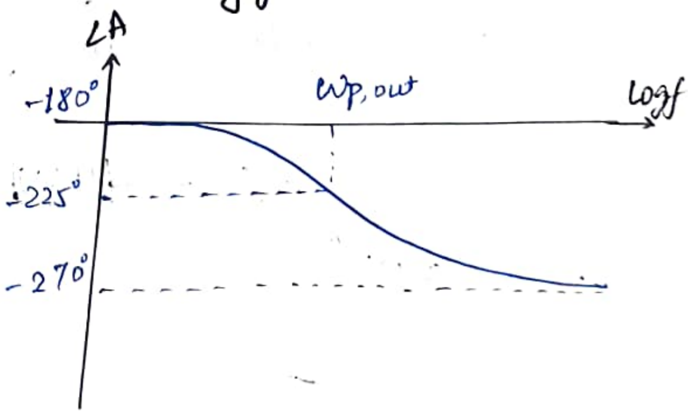
\#



[Cascaded]

$\omega_{p,out_1} = \omega_{p,in_2} \rightarrow$ I/p pole of next stage is o/p pole of prev. stage





$$A(s) = \frac{-g_m (R_D \parallel r_o)}{(1 + s/\omega_p)},$$

$$\omega_p = \frac{1}{(R_D \parallel r_o)\, C_L'},$$

$$C_L' = C_{gd} + C_{db} + C_L$$

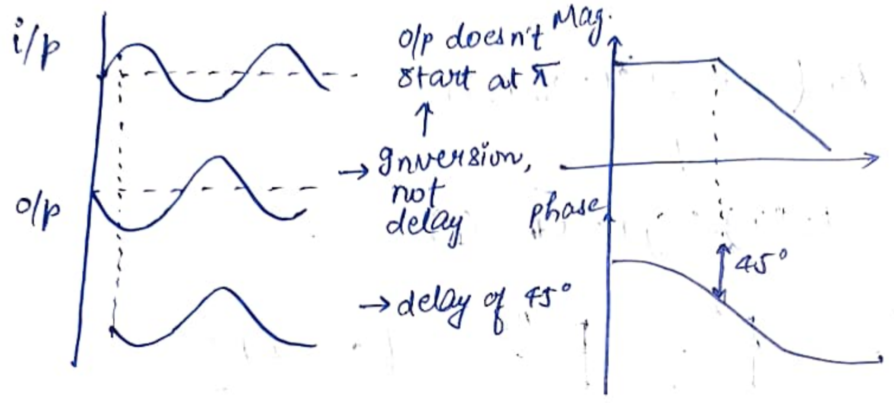
ω_{UGF} : $$\left| \frac{g_m (R_D \parallel r_o)}{\sqrt{1 + \left(\frac{\omega_{UGF}}{\omega_p}\right)^2}} \right| = 1 \Rightarrow \omega_{UGF} \approx g_m (R_D \parallel r_o) \cdot \omega_p$$

$$\uparrow \qquad \approx \frac{g_m \uparrow}{C_L'}$$

↳ Doesn't depend on o/p imp. (R_D; r_o)

17-09-2025

- DC Biasing.
- Voltage swing limits
+ Gain
- Bandwidth
- Noise.



Noise

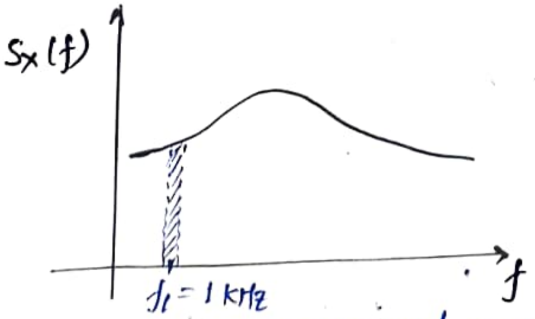
Thermal Noise

↳ Due to random movement of electrons (Random process)
↳ Not deterministic; cannot write deterministic equation.
↳ Can only give statistical measure: mean, variance, SD.
                                        ‖ 0 (M)   (σ^2)

Power Spectral Density (PSD):

↳ Fourier Transform of autocorrelation of the random variable.

$$S_x(f) \longrightarrow \boxed{H(f)} \longrightarrow S_y(f) = S_x(f)\,|H(f)|^2$$



↳ PSD: integrated power in 1 Hz BW.

Noise in Resistor:

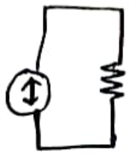
Voltage Noise:

$\overline{V_n^2}(f) = 4KTR$

↳ PSD

Noise Current:

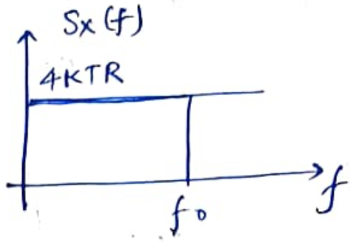
$\equiv \overline{i_n^2}(f) = \dfrac{4KT}{R} \left(= \dfrac{\overline{V_n^2}}{R^2}\right)$



$\sigma^2 \equiv$ Mean-squared value $(\overline{V_n^2})$

Total noise power in BW

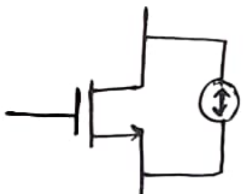
$= \int_0^{f_0} 4KTR \, df$



↳ "white noise"

→ In ideal capacitor or ideal inductor, there is no noise due to absence of parasitic resistances, but actual capacitors and ~~ide~~ actual inductors have noise.

Noise in Transistors: (Thermal Noise)



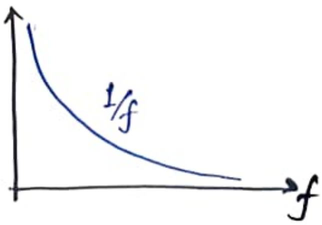
$\overline{i_{nd}^2} = 4KT\gamma g_m$, $\gamma = 2/3$, for long channel devices

$= 1$, for short channel devices

↳ drain noise current PSD (b/w D & S)

↳ white noise.

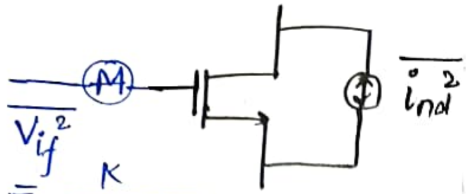
Flicker Noise: Due to dangling bonds



↳ "Pink noise"

↳ Not considered in RF, as it is below thermal noise.

↳ Affects when working with low frequency.



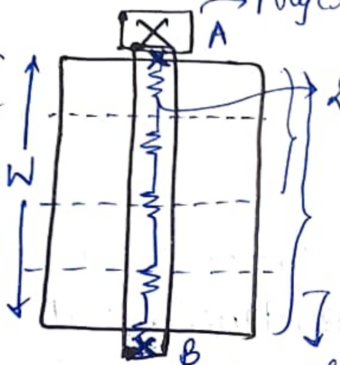
$\overline{V_{if}^2} = \frac{K}{WLC_{ox}f}$

Reduce flicker noise ⇒ Increase area
Also Reduces random mismatch
(but larger capacitances)

Layout view :

→ Polycrystalline

This chunk sees a small R_g ←

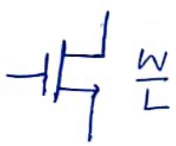


Distributed resistances in gate materials
R_G
⇓
Noise:

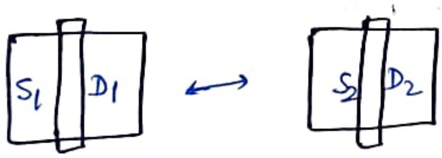
$$\overline{V_{ng}^2} = \frac{4KTR_G}{3}$$

→ empirically

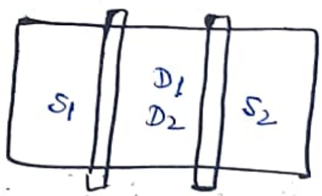
This part sees the complete R_g



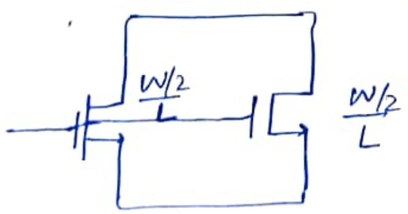
⇓ chop into 2 and put in parallel (same area)



→ Merge one region (Overlap D or S)

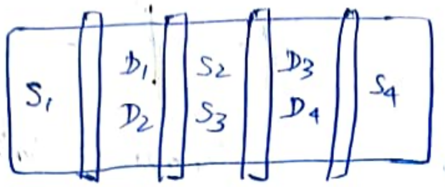


↓
Device with fingers
↓
no. of fingers (nf) = 2
↓
Reduces area and capacitances.



$$\begin{cases} R_G' = R_G/4 \quad (2 \text{ in parallel}) \\ \overline{V_{ng_2}^2} = 4KT\frac{R_G}{12} \end{cases}$$

Splitting in 4,

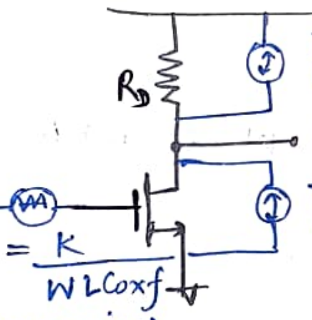


$\hookrightarrow n_f = 4$

$R_G' = \frac{R_G}{16}$ (Four $\frac{R_G}{4}$ in parallel)

$\overline{V_{ng_4}^2} = \frac{4KTR_G}{48}$

$\boxed{19\text{-}09\text{-}2025}$



$\overline{i_{nR_D}^2} = \frac{4KT}{R_D}$

$\overline{i_{nd}^2} = 4KT\gamma g_m$

$\overline{V_{nf}^2} = \frac{K}{WLC_{ox}f}$

(flicker noise)

source/ip

V_s

$\overline{V_n^2}$

noise

(10) A_1

$\overline{V_{nA_1}^2}$ (10nV/$\sqrt{Hz}$)

$\left\{ \text{Amplifier: amplifies the noise \& add its own noise} \right\}$

$\hookrightarrow$ AV_s (voltage signal o/p)

$A_1^2\overline{V_n^2} + \overline{V_{nA_1}^2}$ (noise power o/p) $\hookrightarrow$ PSD

$\downarrow$

Represent in

$\sqrt{W/Hz}$

or $\sqrt{V^2/Hz}$ or $V/\sqrt{Hz}$

$$SNR = \frac{A^2 V_s^2}{A_1^2\overline{V_n^2} + \overline{V_n^2}A_1}$$

5   8nV/$\sqrt{Hz}$

$$SNR = \frac{A_2^2 V_s^2}{A_2^2 V_n^2 + \overline{V_{nA_2}^2}}$$

Input Referred Noise:

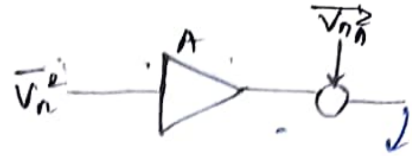
$\overline{V_{n,inA}^2}$

(Input-referred)

Ideal noiseless amplifier

$(\overline{V_n^2} + \overline{V_{n,inA}^2})A^2$

=



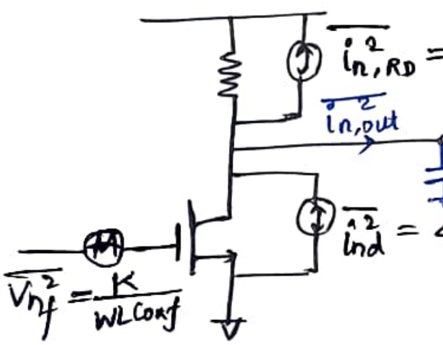
$\overline{V_{n,out}^2} = \overline{V_n^2}A^2 + \overline{V_{n,A}^2}$

$$\overline{V_{n,inA}^2} = \frac{\overline{V_{n,A}^2}}{A^2}$$

Ways to find Input-referred noise:

① $\overline{V_{n,out}^2} \longrightarrow \div A^2$

② $\overline{I_{n,out}^2} \longrightarrow \div g_m^2$



∞ (blocks DC) [Actually ckt does not have S.C.]

all ac-shorted

$$\overline{I_{n,out}^2} = \frac{4KT}{R_D} + 4KT\gamma g_m + \frac{K}{WLC_{ox}f}\cdot g_m^2$$

O/p S.C. noise current PSD

I/p-referred voltage noise density: (PSD)

$$\overline{V_{n,in}^2} = \frac{\overline{I_{n,out}^2}}{g_m^2}$$

$$= \frac{4KT}{R_D g_m^2} + \frac{4KT\gamma}{g_m} + \frac{K}{WLC_{ox}f}$$

$i_{out} = g_m V_{gs}$

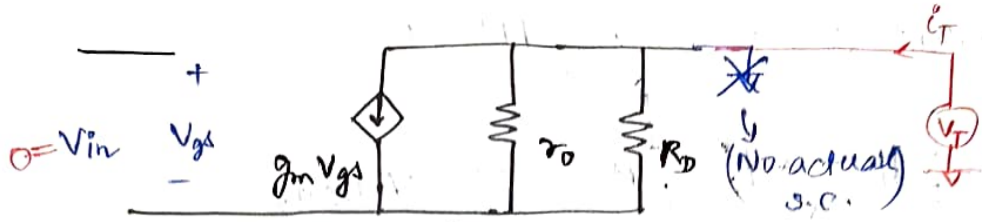
$\frac{i_{out}}{V_{in}} = g_m \rightsquigarrow \frac{\text{output short circuit current}}{\text{applied voltage}}$

$g_m \uparrow \Rightarrow$ Noise $\downarrow$ (current $\uparrow$)

Noise-power tradeoff:

$g_m \uparrow$ (by increasing current) $\Rightarrow$ Noise $\downarrow$

$\Rightarrow$ Power $\uparrow$



$i_{out,sc} = g_m V_{gs}$

$V_{out} = i_{out,sc} \times R_{out}$

$= g_m V_{in} (r_o \parallel R_D)$

$R_{out} = r_o \parallel R_D$

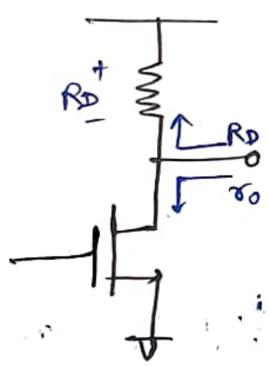
$\overline{V_{n,out}^2} = \overline{I_{n,out}^2} \times R_{out}^2$

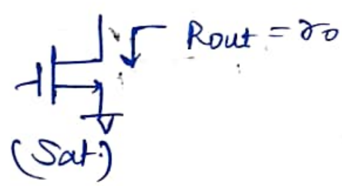
$\overline{V_{n,in}^2} = \dfrac{\overline{I_{n,out}^2} \times \cancel{R_{out}^2}}{g_m^2 \cancel{R_{out}^2}}$

$A = g_m (r_o \parallel R_D)$

$= g_m R_{out}$

→ $\boxed{\text{Gain} = G_M \times R_{out}}$: For any ~~circuit~~ amplifier (Lemma)





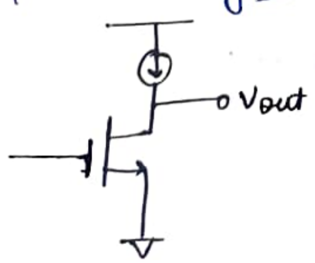
$R_{out} = r_o \parallel R_D$

$= R_{up} \parallel R_{down}$

Limitations of Common Source :

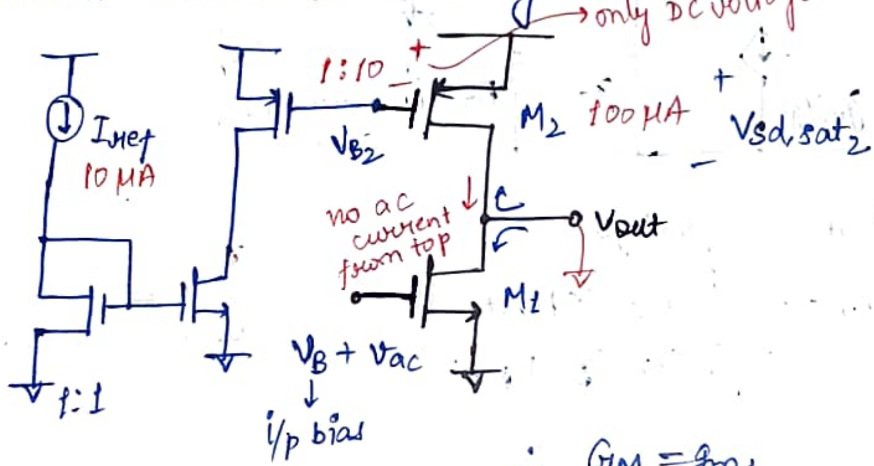
$g_m (r_o \parallel R_D) \approx g_m R_D \Rightarrow$ ~~Increase~~ Gain depends on $R_D \uparrow$ $\Downarrow$ voltage drop $\uparrow$

Replace R_D by current source :



$g_m r_o$: intrinsic gain of the amplifier (max^m gain)

Implement current source using a PMOS :



$\therefore \; G_M = g_{m1}$ (overall)

$R_{out} = r_{o1} \,||\, r_{o2}$

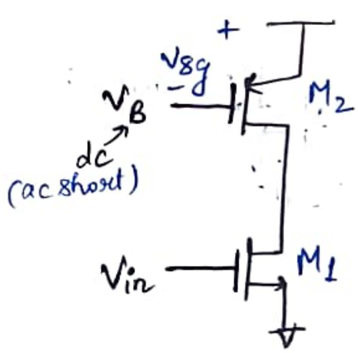
$Gain = g_{m1}(r_{o1} \,||\, r_{o2})$

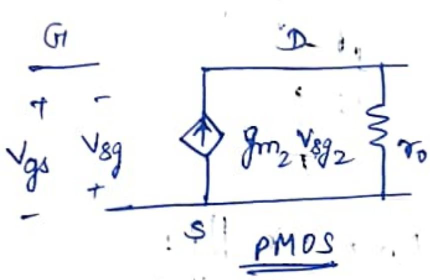
23-09-2025

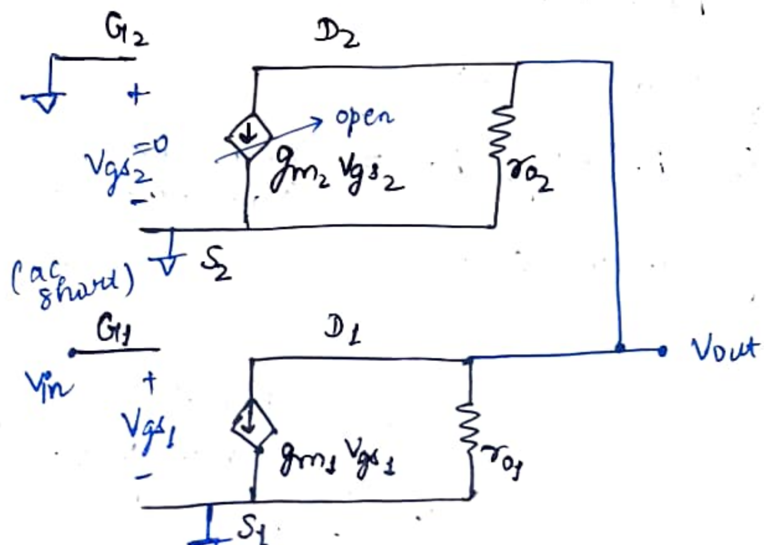
CS amplifier with current source load

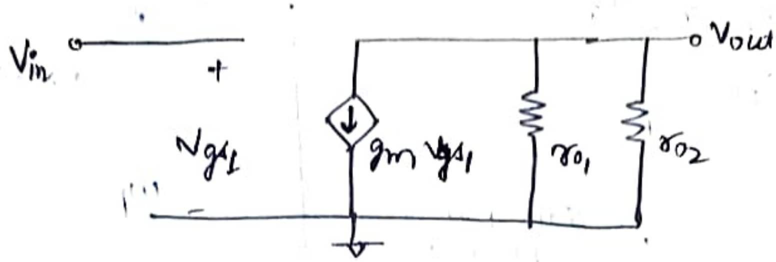
$G_m = g_{m1}$

$A_v = g_{m1}(r_{o1} \,||\, r_{o2})$



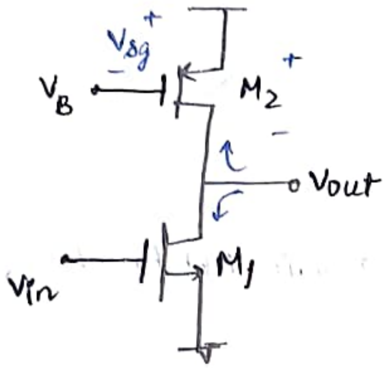






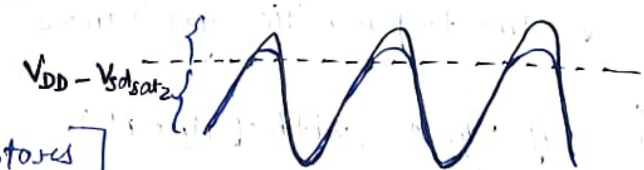
$V_{out} = -g_m V_{gs_1} (r_{o_1} \parallel r_{o_2})$

$R_{out} = r_{o_1} \parallel r_{o_2}$

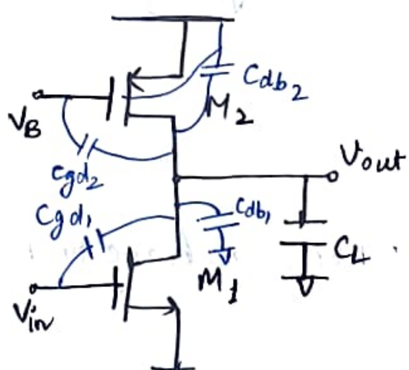


$V_{out,max} = V_{DD} - V_{sd\,sat_2}$

$V_{out,min} = V_{d\,sat_1}$



[Preserve all the transistors in saturation]

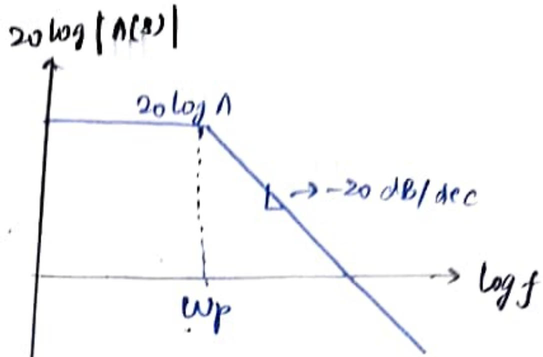


Capacitance at Vout:

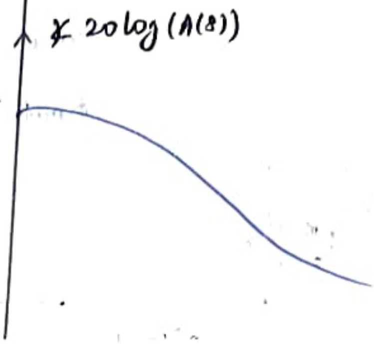
$$C_L' = \underbrace{C_L}_{\substack{\text{load cap.} \\ \text{(or i/p cap. of next stage)}}} + \underbrace{C_{db_1} + C_{gd_1} + C_{db_2} + C_{gd_2}}_{\substack{\text{parasitic cap} \\ \text{(part of device)}}}$$

$$BW = f_p = \frac{1}{2\pi R_{out} C_L'}$$

$$A(s) = \frac{-g_{m1}(r_{o1} \parallel r_{o2})}{\left(1 + \frac{s}{\omega_p}\right)}$$



$$f_{UGF} = \frac{g_{m1}}{2\pi C_L'} \quad \left(= \text{Gain-BW product} = A_V \cdot BW \right)$$



To increase gain:

① $r_o \uparrow$ by $L \uparrow$ (channel length).

I remains same.

BW ↓ (as $C_L' \uparrow$, $R_{out} \uparrow$)

UGF remains same for 1^{st} order;

little ↓ due to parasitic capacitances → Gain-BW trade-off.

② $g_m \uparrow$ by $W_{1,2} \uparrow$ (width of M_1 & M_2).

⇓

$I \uparrow$

$R_{out} = r_{o1} \parallel r_{o2}$

$\downarrow r_o \approx \frac{1}{\lambda I_D \uparrow}$ [$r_o \downarrow$ by the same factor as $g_m \uparrow$]

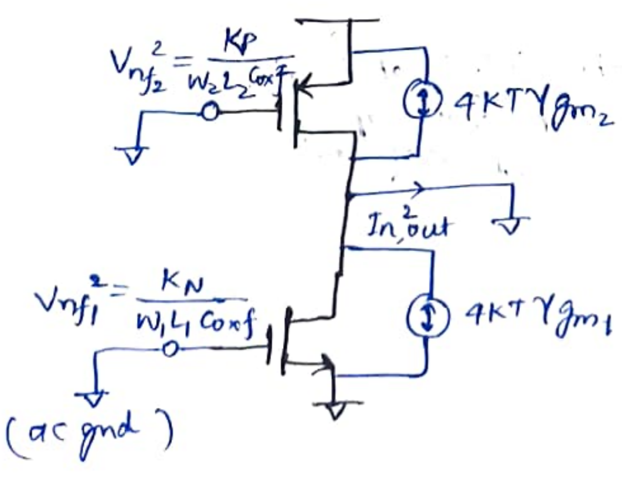
Gain remains same.

3-dB BW ↑

UGF ↑

↳ Power-BW tradeoff: To ↑ BW, we have to burn more current.

Noises:



Coeff. for NMOS, PMOS (K_P, K_N): flicker noise coeff

↳ different for PMOS, NMOS

↳ $K_P < K_N$

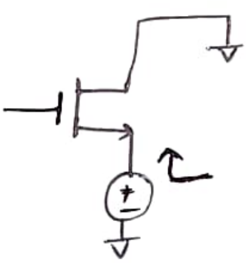
$$\overline{I_{n,out}^2} = 4KT\gamma g_{m_1} + 4KT\gamma g_{m_2} + \frac{K_N}{W_1 L_1 C_{ox} f} g_{m_1}^2 + \frac{K_P}{W_2 L_2 C_{ox} f} \cdot g_{m_2}^2$$

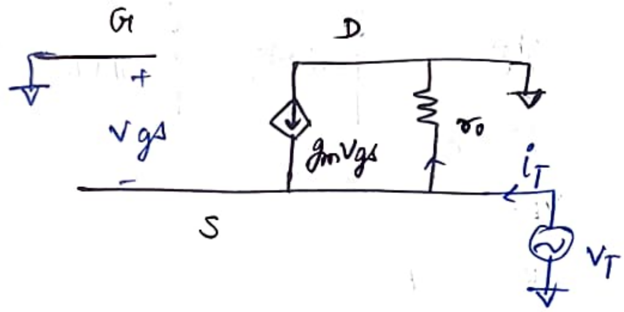
↳ Total o/p short-circuit noise current PSD

$$\overline{V_{n,in}^2} = \frac{\overline{I_{n,out}^2}}{g_{m_1}^2}$$

↳ i/p referred voltage noise PSD

↳ Noise-Power tradeoff : Noise ↓ ⇒ g_m ↑ ⇒ Current ↑





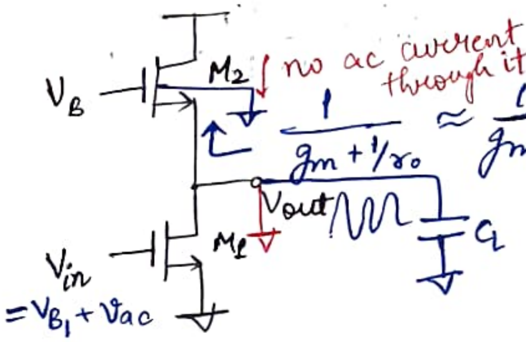
$$i_T = -g_m V_{gs} + \frac{V_T}{r_o}$$

$$V_{gs} = -V_T$$

$$i_T = g_m V_T + \frac{V_T}{r_o}$$

$$\frac{V_T}{i_T} = \frac{1}{g_m + 1/r_o} \approx \frac{1}{g_m}, \quad \frac{1}{r_o} \ll g_m$$

25-09-2025



$$\frac{1}{g_m + 1/r_o} \approx \frac{1}{g_m + g_{mb}}$$

$v_{bs} \xrightarrow{\text{results in}} i_d$

$g_{mb} \rightarrow g_m$ writ. body terminal

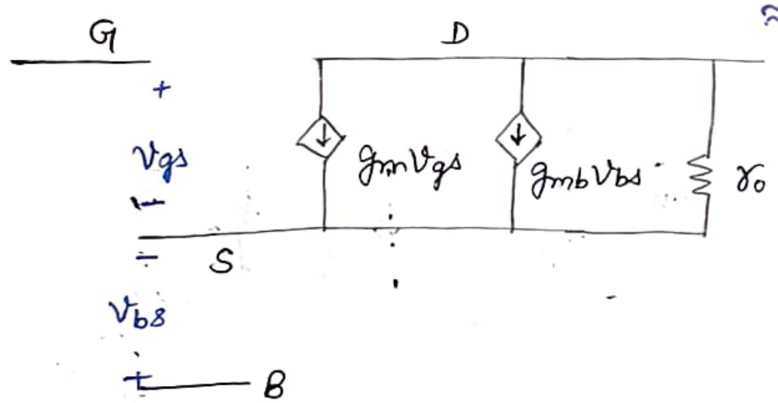
$v_{gs} \xrightarrow{g_m} i_d$ (small signal current)

[Connect bulk to GND or use triple-well]

$G_m = g_{m_1}$

$$R_{out} = \frac{1}{(g_{m_2} + 1/r_{o2})} \,||\, r_{o1} \rightarrow \frac{1}{g_{m_2} + g_{mb} + \frac{1}{r_{o2}}}$$

$$\approx \frac{1}{g_{m_2} + g_{mb_2}}$$



$g_{mb} = \chi g_m$

$$A_v = g_{m_1}\left[\frac{1}{g_{m_2} + g_{mb_2} + r_{o2}} \,||\, r_{o1}\right]$$

$$\approx \frac{g_{m_1}}{g_{m_2} + g_{mb_2}} \quad \text{[Lower gain]}$$

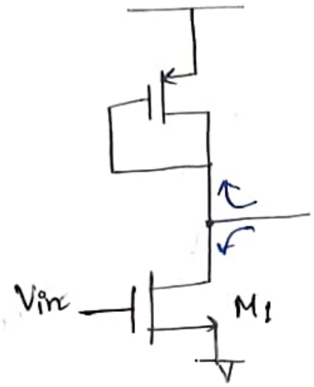
Total load capacitances,

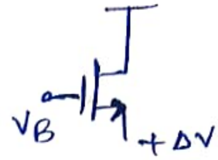
$$C_L' = C_L + C_{db_1} + C_{gb_1} + C_{sb_2} + C_{gs_2}$$

$$BW = \frac{1}{2\pi R_{out} C_L'} \approx \frac{g_{m_2} + g_{mb_2}}{2\pi C_L'} \rightarrow \text{very high BW}$$

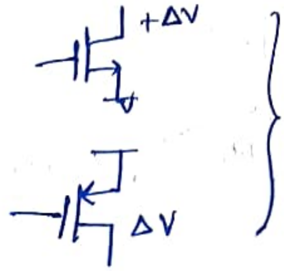
↳ Useful topology when we need very high BW (~GHz) but are okay with lower gain (lower single digit).

Diode connected load:

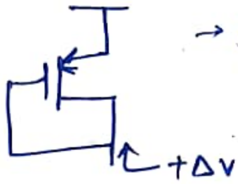




: Low impedance nodes"



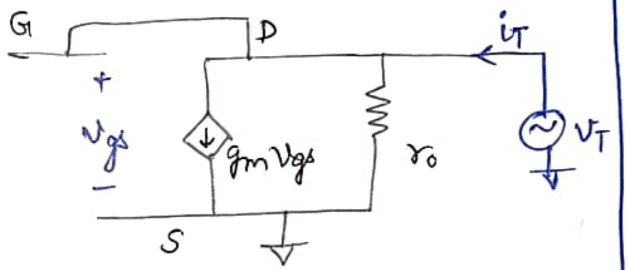
: High impedance nodes



→ Diode-connected transistor

$$\Delta I = g_m \Delta V$$

$$\frac{\Delta V}{\Delta I} = \frac{1}{g_m}$$



$$i_T = g_m v_{gs} + \frac{v_T}{r_o}$$

$$v_{gs} = v_T$$

$$i_T = g_m v_T + v_T / r_o$$

$$\Rightarrow \frac{v_T}{i_T} = \frac{1}{g_m + 1/r_o} \approx \frac{1}{g_m}$$

[Body effect is neglected in this topology.]

$G_m = g_{m1}$ [All current coming from M_1]

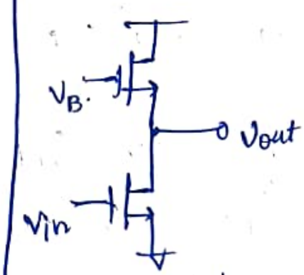
$$R_{out} = \left(\frac{1}{g_{m2} + 1/r_{o2}}\right) \parallel r_{o1}$$

$$\approx \frac{1}{g_{m2}}$$

$$A_v = \frac{-g_{m1}}{g_{m2}}$$

$$BW = \frac{1}{2\pi R_{out} C_L'} \approx \frac{g_{m2}}{2\pi C_L'}$$

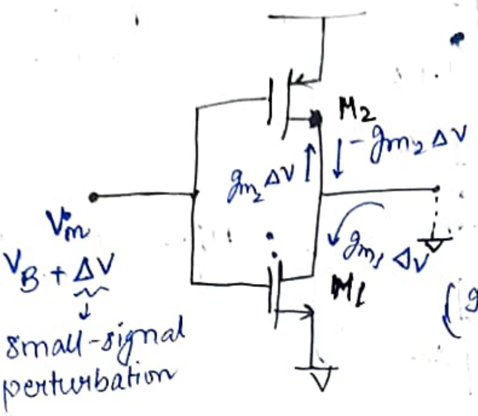
$$V_{out,max} = V_{DD} - V_{SG_2}$$

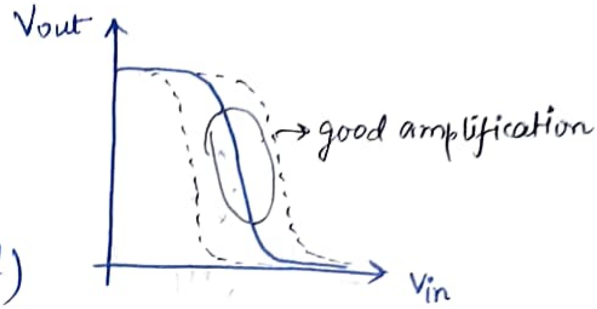


$$V_{out,max} = V_B - V_{GS_2}$$

30-09-2025

Common Source with Active Load (Inverter)





$$G_m = g_{m_1} + g_{m_2}$$

$$R_{out} = r_{o_1} \parallel r_{o_2}$$

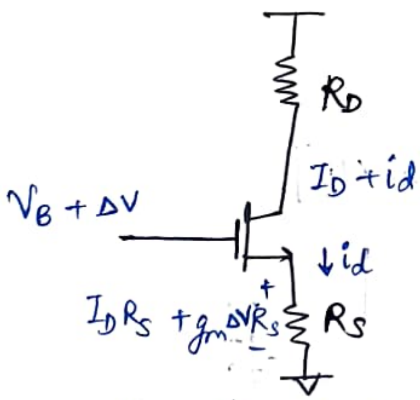
$$\text{Gain} = (g_{m_1} + g_{m_2})(r_{o_1} \parallel r_{o_2})$$

"Current Reuse" → Higher gain $(g_{m_1} + g_{m_2})$

But hard to ~~configure~~ precisely bias.

Common Source with Source Degeneration

degenerating the transconductance



$$V_{gs} = \Delta V - i_d R_s$$

$$i_d = g_m V_{gs}$$

$$\frac{i_d}{g_m} = \Delta V - i_d R_s$$

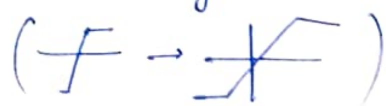
$$i_d\left(\frac{1}{g_m} + R_s\right) = \Delta V$$

$$G_m = \frac{i_d}{\Delta V} = \frac{g_m}{1 + g_m R_s} < g_m$$

→ Negative feedback

↳ The loop is trying to get back (reversing) what we did.

↳ Enhances linearity (g_m non-linearity), but lower gain.



$$R_{out} = R_D \parallel (\underbrace{R_S + r_{o1} + g_{m1} r_{o1} R_S}_{\text{result from cascoding}})$$

$\approx R_D$ ↳ very high

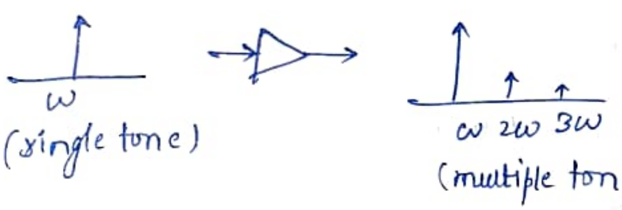
$$\text{Gain} = \frac{g_m R_D}{1 + g_m R_S}$$

$$g_{m,\,actual} = g_m + g_m' V_{gs} + g_m'' V_{gs}^2$$

$$i_d = g_m V_{gs} + g_m' V_{gs}^2 + g_m'' V_{gs}^3 + \dots$$

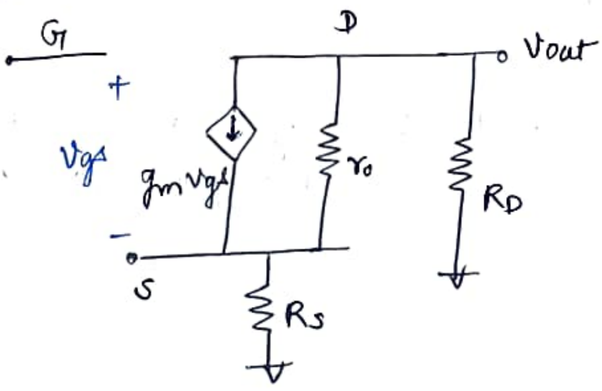
For $V_{gs} = A\cos\omega t$,

$$i_d = \underbrace{g_m A\cos\omega t}_{\text{desired}} + \underbrace{g_m' A^2 \cos^2\omega t}_{2\omega,\ dc} + \underbrace{g_m'' A^3 \cos^3\omega t}_{3\omega,\ \omega} + \dots$$

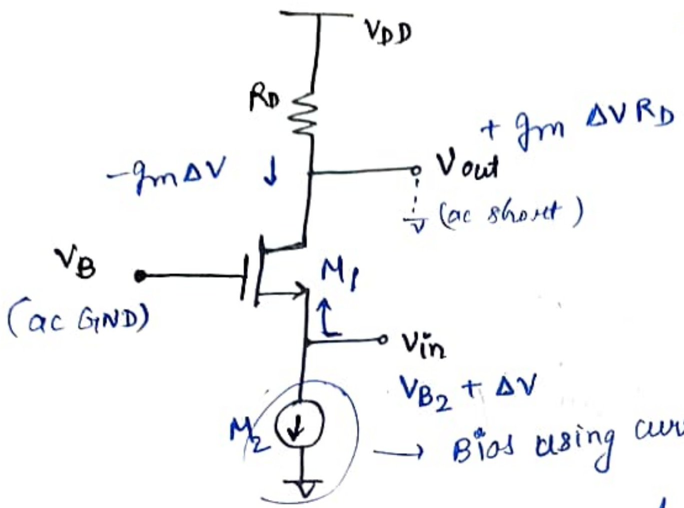


: Harmonic Distortion ↓ THD

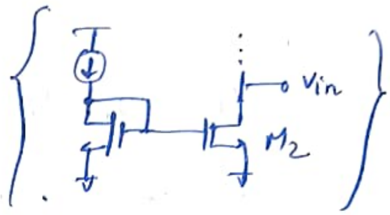
Small-signal equivalent circuit :



Common Gate



→ Bias using current mirror



→ Used as input stage to match the i/p impedance (which is very low) (eg., 50 Ω, 75 Ω).
↳ Frontend circuit.

$$R_{in} = \frac{1}{g_m} \quad \text{OR} \quad \frac{1}{g_m + g_{mb}}$$

(if B is shorted to S) (if B is grounded)

↳ very low

Effective transconductance,

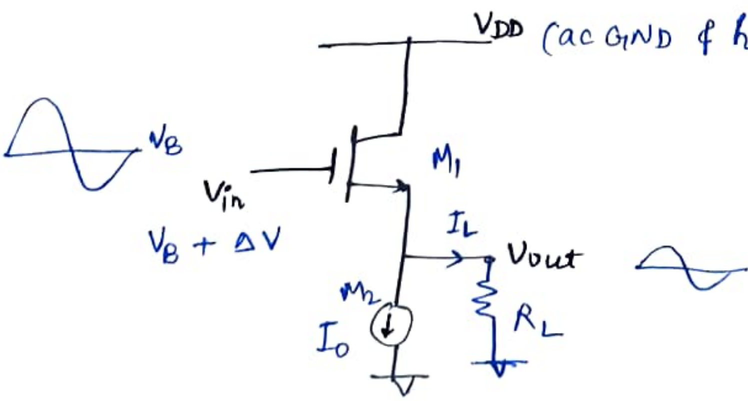
$$G_M = g_{m_1}$$

$$\text{Gain} = g_m R_{out}$$
$$= g_m R_D$$

- Providing extra voltage to Vin ⇒ V_{gs} ↓ ⇒ current ↓
  ⇒ output voltage ↑

- No ~~the~~ inversion.

Common Drain



VDD (ac GND & higher voltage than S)

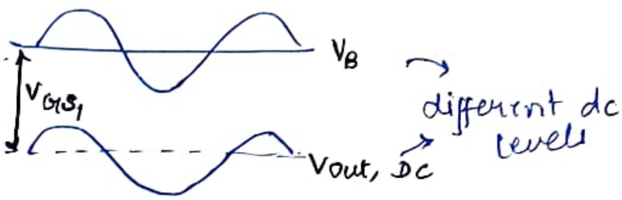
→ Acts as level shifter (dc level shifting)

$$I_d = \frac{K_n}{2}(V_B + \Delta V - V_{TH})^2$$

$$I_d - I_o = I_L$$

$$V_{out} = I_L R_2$$

$$I_D = I_o + I_L$$

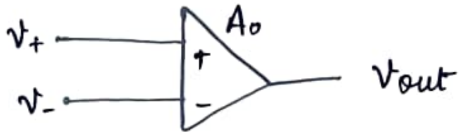


$$V_{out} = V_{in} - V_{gs_1}$$

- Gain little ~~low~~ lower than 1.
- Output stage (acs as buffer) to drive the resistive load.

16-10-2025

Opamp Design



$$V_{out} = A_0 (v_+ - v_-)$$

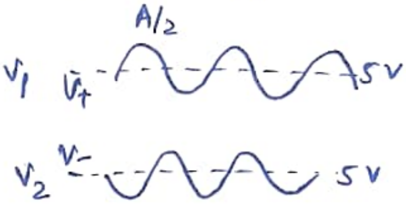
Differential Signals :

$V_{in} = A \sin \omega t$

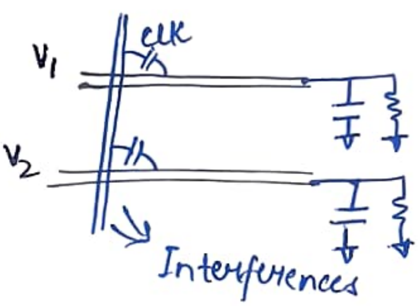
Single-ended signal:

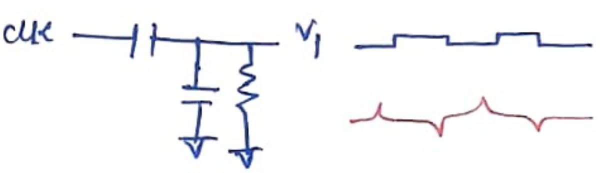
$V_{ind} = A \sin \omega t$

Differential signal:

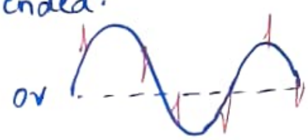


$$V_+ - V_- = \left(5 + \frac{A}{2} \sin \omega t\right) - \left(5 - \frac{A}{2} \sin \omega t\right)$$
$$= A \sin \omega t$$

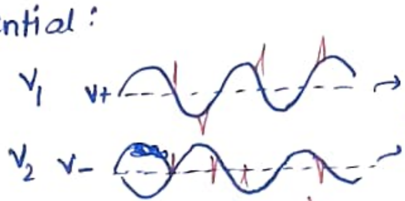




Single-ended:



Differential :



→ Both getting interfered by same clk

Both the interferences cancel

$V_d = V_1 - V_2$

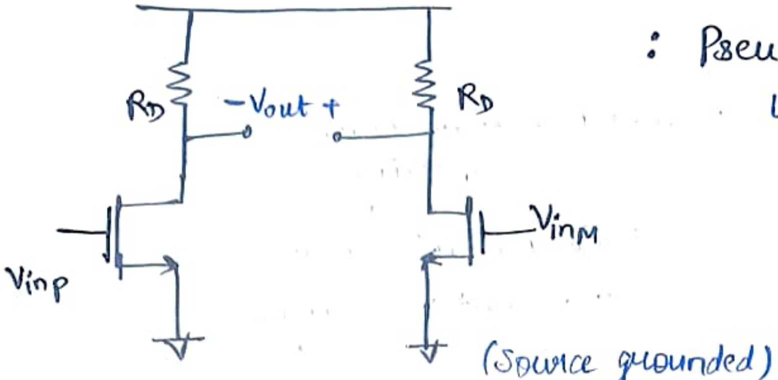
$V_{CM} = \dfrac{V_1 + V_2}{2}$ (common mode)

$\Rightarrow V_1 = V_{CM} + \dfrac{V_d}{2}$

$V_2 = V_{CM} - \dfrac{V_d}{2}$

: Pseudo-differential circuit

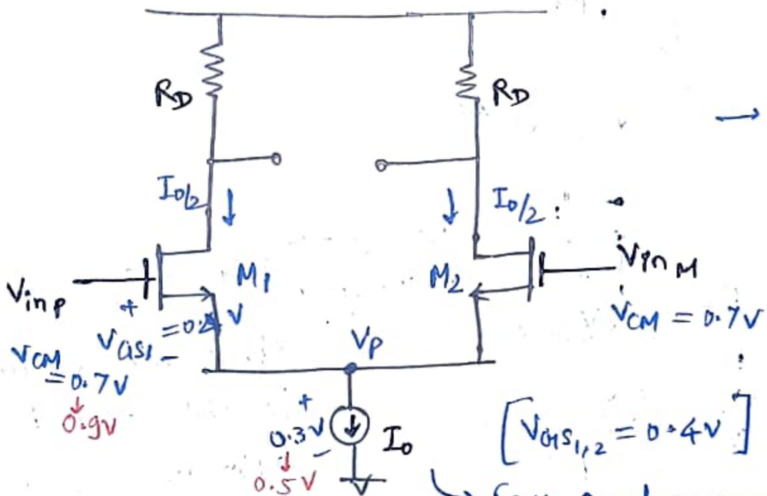
↳ Not resiliant to common mode



$V_{inp} = V_{CM} + V_d/2$

$V_{inM} = V_{CM} - V_d/2$

⇓



→ symmetry required

$[V_{GS_{1,2}} = 0.4V]$

↳ For good current source, current should not change with change in V_{CM}. [Ideal]

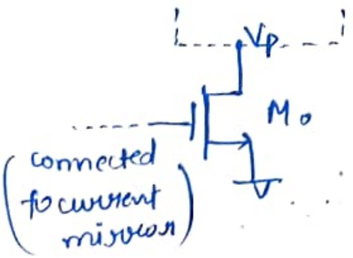
Absence of V_d:

For $I_o/2$,

$$V_{GS_1} = V_{GS_2} = \sqrt{\frac{2\, I_o/2}{\mu_n C_{ox}\left(\frac{W}{L}\right)}} + V_{TH}$$

$$V_p = V_{inp} - V_{GS_1} = V_{inM} - V_{GS_2}$$

$$= V_{CM} - V_{GS_{1,2}}$$

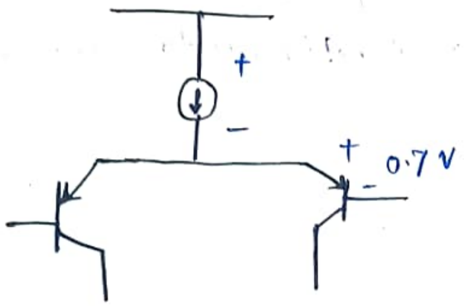


For M_o to be in saturation (to act as current source),

$$V_{in,CM\,min} = \underset{0.4}{V_{GS_{1,2}}} + \underset{0.2}{V_{dsat\,o}}$$

$$= 0.6\,V$$

With p-n-p transistor (used in 741 datasheet):

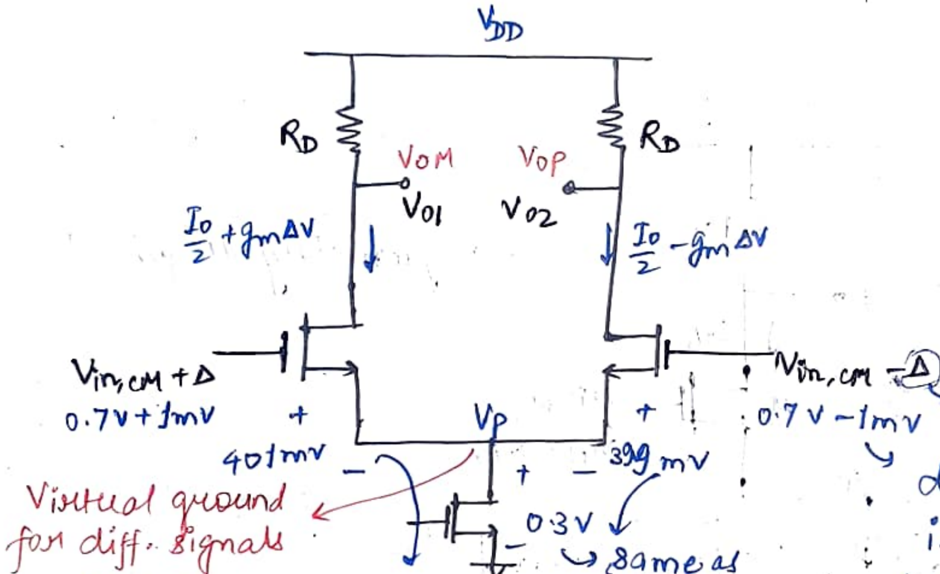


$V_{in,CM}$ → has max value $= V_{CC} -$ (something)

↳ also has min-value

[DC-voltage range]

With differential signals:



↳ small signal

difference (small signal) is absorbed by V_{gs}.

↳ No longer same current on both sides

KVL:

$$V_{in,CM} + \Delta V - V_{gs_1} - V_P = 0$$

$$V_{in,CM} - \Delta V - V_{gs_2} - V_P = 0$$

$$\Rightarrow \boxed{V_{gs_1} - V_{gs_2} = 2\Delta V}$$

$$V_{o1} = V_{DD} - I_d R_D = V_{DD} - \left(\frac{I_o}{2} + g_m \Delta V\right) R_D$$

$$V_{o2} = V_{DD} - \left(\frac{I_o}{2} - g_m \Delta V\right) R_D$$

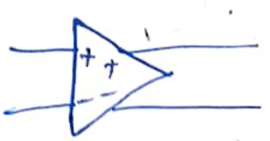
$$\Rightarrow V_{o1} = V_{DD} - \frac{I_o}{2} R_D - g_m \Delta V R_D \rightarrow V_{OM}$$

$$V_{o2} = V_{DD} - \frac{I_o}{2} R_D + g_m \Delta V R_D \rightarrow V_{OP}$$

in-phase

$$V_{o,CM} = \frac{V_{o1} + V_{o2}}{2} = V_{DD} - \frac{I_o}{2} R_D$$

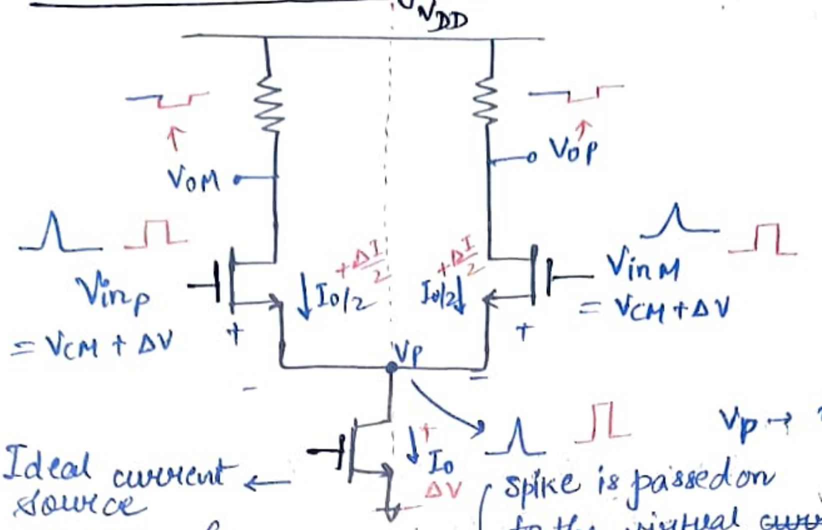
$$\rightarrow A_d = \frac{\text{diff o/p}}{\text{diff i/p}} = \frac{2 g_m \Delta V R_D}{2\Delta V} = g_m R_D.$$



Fully-differential-opamp

Common-mode signals:

21-10-2025



→ Equal change in both sides

→ Rejects common-mode signals

Ideal current source ←
↳ No V_{gs} change

(spike is passed on to the virtual ~~current~~ ground point) → as V_{gs} remains the same.

V_P → no longer virtual ground

$$\left.\begin{aligned} V_{inP} &= V_{gs1} + V_P \\ V_{inM} &= V_{gs2} + V_P \end{aligned}\right\} \quad V_{gs1} = V_{gs2}$$

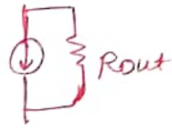
$\uparrow\Delta V$, $+\Delta V$

$$V_{OP} = V_{OM}$$

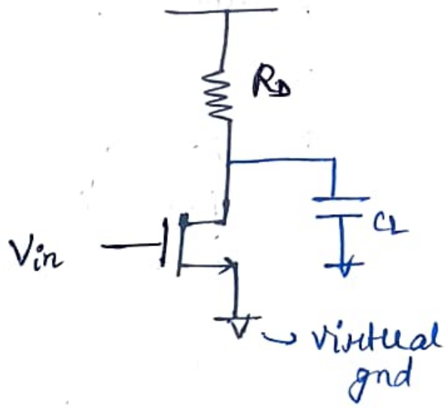
$$V_{out} = V_{OP} - V_{OM}$$

$$\Delta I = \frac{\Delta V}{R_{out}}$$

$$I_0 \longrightarrow I_0 + \Delta I$$



Differential-Mode Half Circuit



$$R_{out} = r_o \,||\, R_D$$

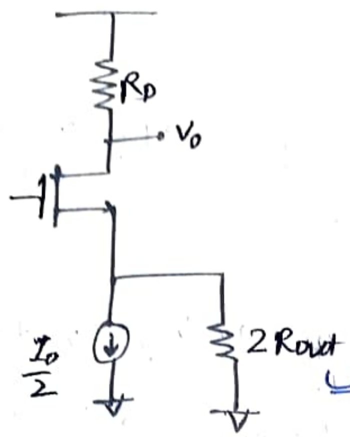
$$A_{dm} = -g_{m1,2}\,(R_D \,||\, r_o)$$

$$BW = \frac{1}{2\pi R_{out} C_L'}$$

Full-diff. noise : $\overline{V_{n,in}^2}$ = $2\times$ Noise in single-side

[Noise at V_{OM} & V_{OP} are uncorrelated]

Common-mode half circuit :



↳ on-joining, we should get-back R_{out}

$$A_{CM} = \frac{-g_{m1,2}(R_D \| r_o)}{1 + 2g_m R_{out}}$$

: Common-source with source degeneration configuration

Higher R_{out} ⇒ Better current source ⇒ Less ΔI

$V_{inP} = V_{CM} + V_d/2 = V_1$

$V_{inM} = V_{CM} - V_d/2 = V_2$

$\overset{\to V_{inP}}{V_1}, \overset{\to V_{inM}}{V_2}$

$V_d = V_1 - V_2$

$V_{CM} = \frac{V_1 + V_2}{2}$

$V_{OM} = A_{dm}\left(\frac{V_d}{2}\right) + A_{CM} V_{CM}$

$V_{OP} = A_{dm}\left(-\frac{V_d}{2}\right) + A_{CM} V_{CM}$

$V_o = V_{OP} - V_{OM}$

$= -A_{dm} V_d$

In mixed signals / SOC, differential signals is used exclusively to maintain signal integrity

Eg. $V_1 = 0.8 - 0.01 \sin\omega_1 t + 0.1 \sin\omega_2 t = V_{CM} + V_d/2$

$V_2 = 0.8 + 0.01 \sin\omega_1 t + 0.1 \sin\omega_2 t = V_{CM} - V_d/2$

$V_{CM} = 0.8 + 0.1 \sin\omega_2 t$

$V_d = -0.02 \sin\omega_1 t$

$V_{OM} = A_{CM}(0.1 \sin\omega_2 t) + A_{dm}(-0.01 \sin\omega_1 t)$

$V_{OP} = A_{CM}(0.1 \sin\omega_2 t) + A_{dm}(+0.01 \sin\omega_1 t)$

$V_o = A_{dm}(0.02 \sin\omega_1 t)$

[Let $A_{dm} = 50$
$A_{CM} = 0.1$]

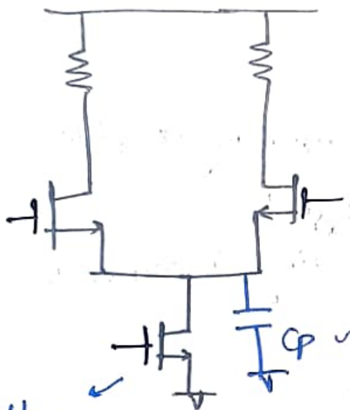
$$\rightarrow \text{CMRR} = \frac{A_{dm}}{A_{cm}}$$ [Ideally, $\rightarrow \infty$]

↪ valid only when considering individual signals

$$= \frac{g_{m1,2}(r_o \| R_D)}{\dfrac{g_{m1,2}(r_o \| R_D)}{1 + 2g_{m1,2} R_{out}}}$$

$$= 1 + 2g_{m1,2} R_{out}$$

↪ Frequency-dependent



↓ Random-noise with same $\left(\frac{W}{L}\right)$ ratio

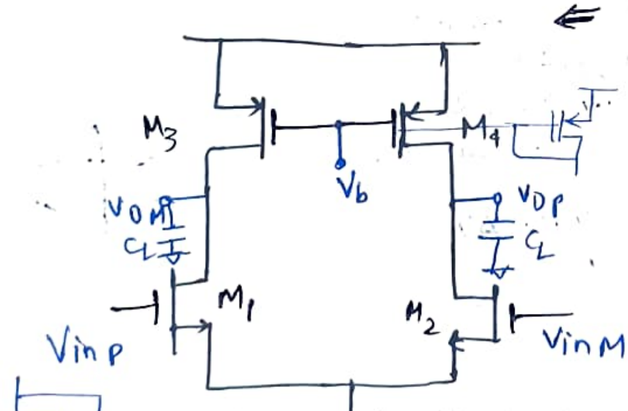
⇒ Increase area

C_p ⇝ critical in large BW

↪ Degrades CMRR at higher f.

$R_{out} \rightarrow Z_{out} = r_o \| \frac{1}{sC_p}$

23-10-2025

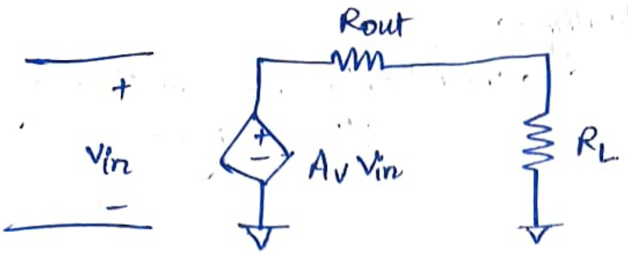


⇐ Operational Transconductance Amplifier (OTA)

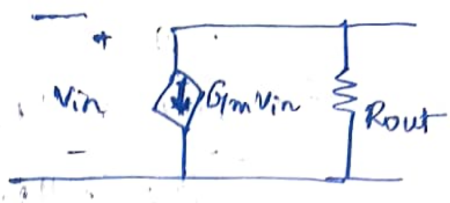
(or loosely, opamp)

$A_{dm} = g_{m1}(r_{o1} \| r_{o3})$

$R_{out} = r_{o2} \| r_{o4}$



OTA



Opamp

$$BW = \frac{1}{2\pi R_{out} C_L}$$

$$UGB = \frac{g_m}{2\pi C_L}$$

Rout of OTA $(= r_{o2} \| r_{o4})$
↓
parallel
↓
usually high

Rout of opamp
↓
ideally zero

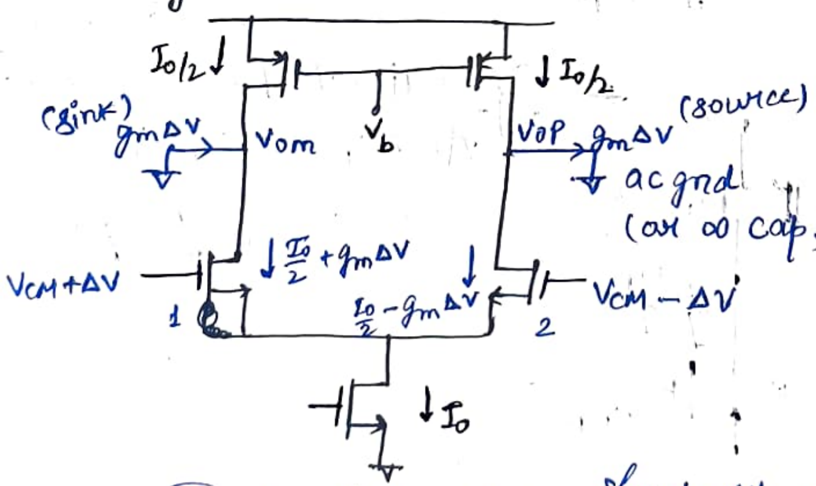
$$V_{CM,in,min} = V_{GS_{1,2}} + V_{dsat_0}$$

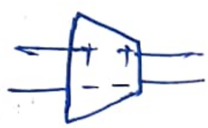
Random mismatch in transistor on left and right side

⇒ Input-referred offset.

⇒ ~~Use~~ do (M_1, M_2) layouting in common-centroid
&
(M_3, M_4)
&
(M_0, its current mirror)

Working:



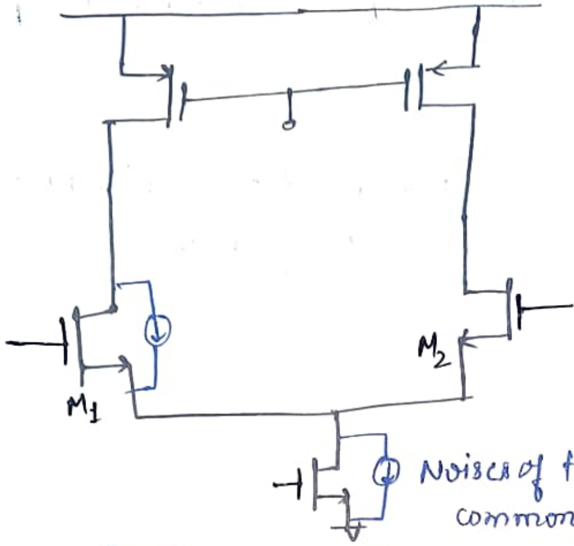


$$\text{Transconductance} = \frac{\text{Short-ckt o/p current}}{\text{i/p voltage}}$$

$$\Rightarrow G_m = \frac{2 g_{m_{1,2}} \Delta V}{2 \Delta V}$$

$$= g_{m_{1,2}}$$

Noise Model:



→ Noise from all transistors (flicker + thermal)

→ Noise pdf from M_1 & M_2 are the same (same g_m) but their instantaneous values are not the same.

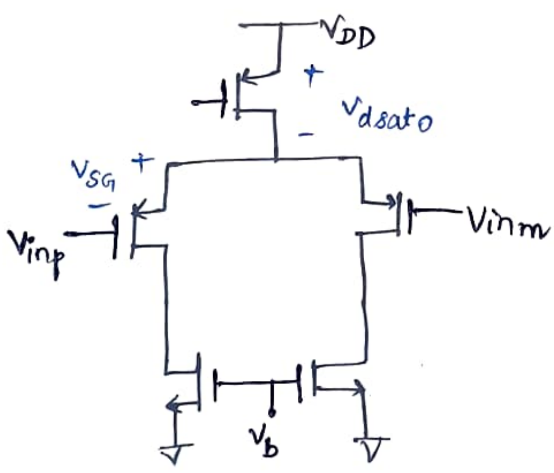
Noises of tail tr (both flicker & thermal) become common-mode on both-side & get cancelled

$$\overline{I_{n,out}^2} = 2\times\left(4KT\gamma g_{m1} + 4KT\gamma g_{m3} + \frac{K_N}{W_1L_1C_{ox}f}\, g_{m1}^2 + \frac{K_P}{W_3L_3C_{ox}f}\cdot g_m^3\right)$$

$$\overline{V_{n,in}^2} = \frac{\overline{I_{n,out}^2}}{g_{m1,2}^2}$$

[Symmetrical on both-side (even though noise values are not same; random) ↳ variances get added]

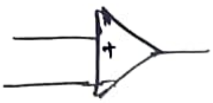
PMOS input, NMOS output:



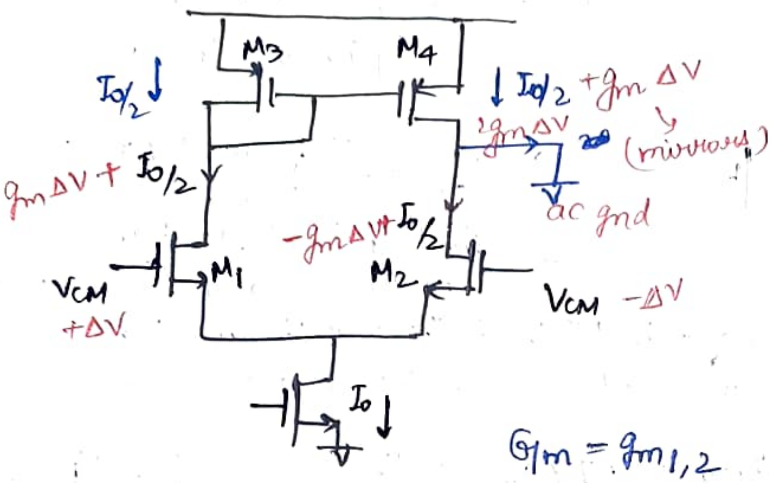
→ Make common source as virtual ground, biased with a current source.

$$V_{in,CM,max} = V_{DD} - |V_{dsato}| - V_{SG\,1,2}$$

Single-ended output opamp:

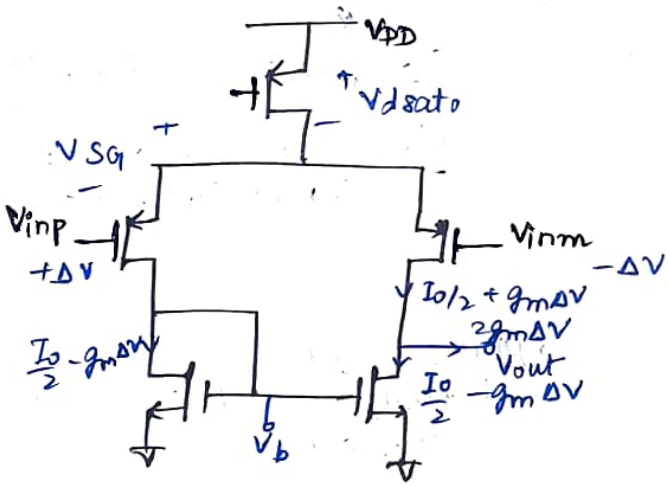


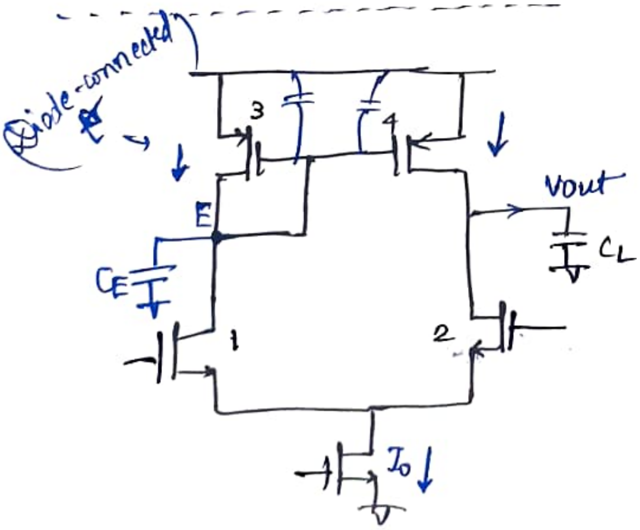
→ Differential i/p single-ended o/p



→ No need to bias PMOS'
↳ self biased

$G_m = g_{m1,2}$





$G_m = g_{m1,2}$

$R_{out} = r_{o2} \| r_{o4}$

$A_v = g_{m1,2}(r_{o2} \| r_{o4})$

BW

$C_L' = C_L + C_{gs2} + C_{gd4} + C_{db4} + C_{db2}$

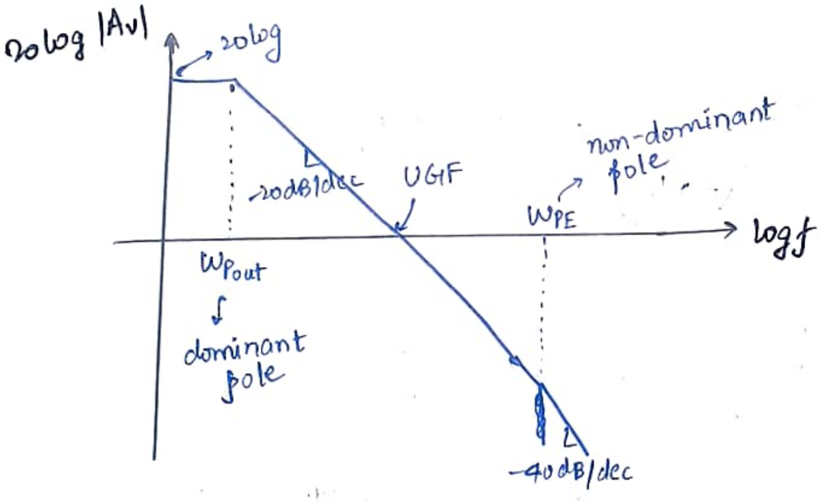
$$\omega_{p\,out} = \frac{1}{R_{out} \cdot C_L'} = \frac{1}{(r_{o2} \| r_{o4})\, C_L'}$$

$C_E = C_{gd1} + C_{db1} + C_{gs3} + C_{gs4} + C_{db3} + C_{gd4}$

$$\omega_{pE} = \frac{g_{m3}}{C_E} \quad \because \left[\frac{1}{g_{m3}} \| r_{o1} \approx \frac{1}{g_{m3}}\right]$$

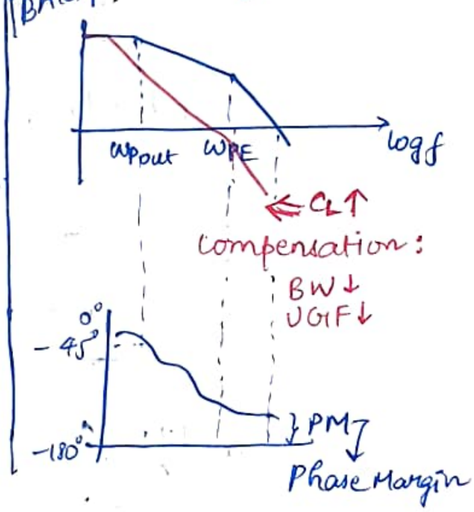
2-poles: one with lower mag. → Dominating sets the BW (dominates the behaviour)

$\omega_{p\,out} \ll \omega_{pE}$

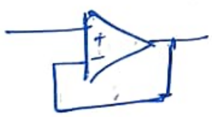


24-10-2025

Suppose, two poles are nearby.



#



$\frac{A}{1+A}$ → Unity-gain F/B ↳ Unstable

$$G(s) = \frac{A(s)}{1+\beta A(s)} \quad ; \quad PM = 5^\circ$$

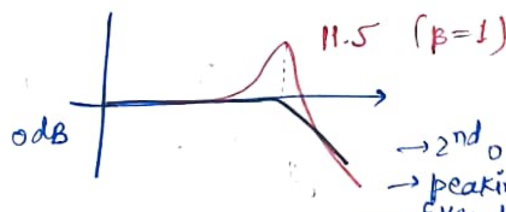
At UGF of $A(s)$,

$\beta A(s) = 1 \angle -175^\circ$

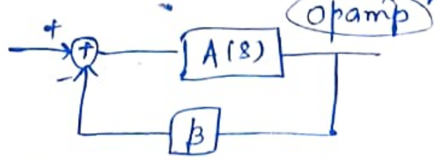
$$\frac{Y(s)}{X(s)} = G(s) = \frac{\frac{1}{\beta} e^{-j175}}{1 + \beta e^{-j175}}$$

$$= \frac{1}{\beta} \; \frac{e^{-j175}}{1 + e^{-j175^\circ}}$$

$$|G(s)|_{s \equiv UGF} \approx \frac{11.5}{\beta}$$



→ 2nd order
→ peaking in freq. domain



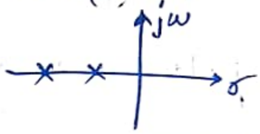
$$\frac{Y}{X} = \frac{A(s)}{1+\beta(s)} \approx \frac{1}{\beta}$$

$$A(s) = \frac{A_0}{(1+s/\omega_{P1})(1+s/\omega_{P2})}$$

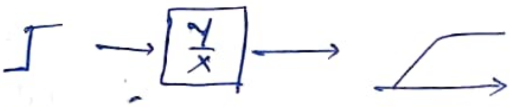
$$\frac{Y}{X}(s) = \frac{A(s)}{1+\beta A(s)} = \frac{A_0\,\omega_{P1}\omega_{P2}}{s^2 + (\omega_{P1}+\omega_{P2})s + (1+A_0\beta)\,\omega_{P1}\omega_{P2}}$$

↳ 2nd order : Overdamped
[Stable]   Underdamped
Marginally-damped (mathematical)
↳ difficult to achieve

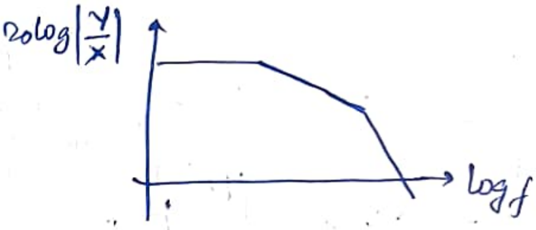
<u>Overdamped system</u> :



→ Pole location : real & negative

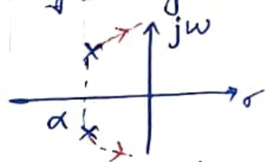


→ No overshoot in time domain

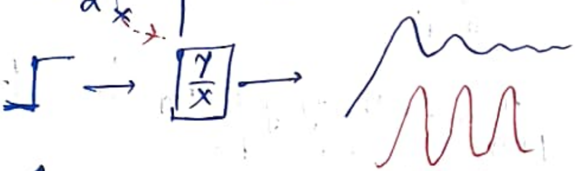


→ No peaking

<u>Underdamped system</u> :



→ complex conjugate

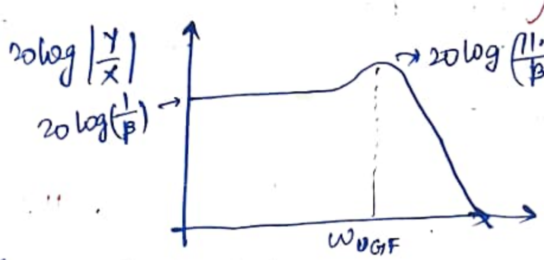


→ Overshoot

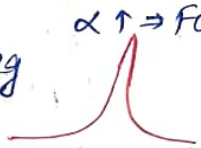
$\omega_P = \alpha \pm j\omega_0$

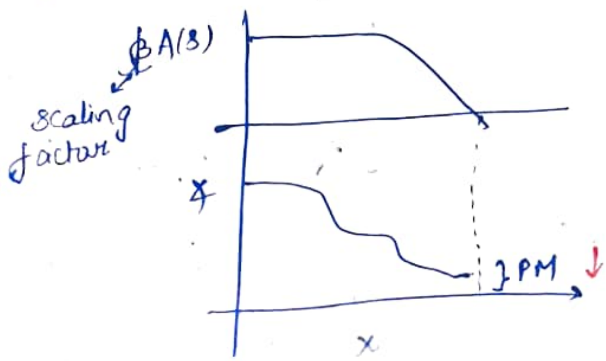
$e^{\alpha t \pm j\omega}$

$\alpha \uparrow \Rightarrow$ Faster decay



→ Peaking





PM ↓ ⇒ Poles move towards jω-axis

PM = 0 ⇒ Poles on jω-axis
↳ Purely oscillatory
(Infinite T.F.)

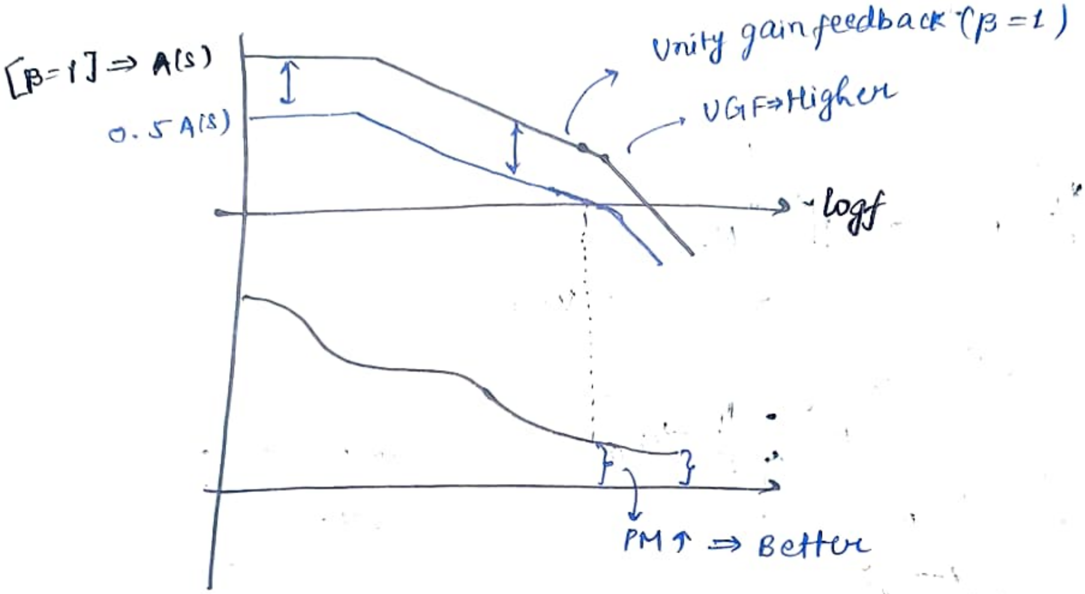
Eg. PM = 45°

$\left|\frac{Y}{X}\right| \approx \frac{1.3}{\beta}$ → 13% peaking

Eg. PM = 60°

$\left|\frac{Y}{X}\right| \approx \frac{1}{\beta}$ → No peaking

Eg. PM = 90° → overdamped



Slew Rate:

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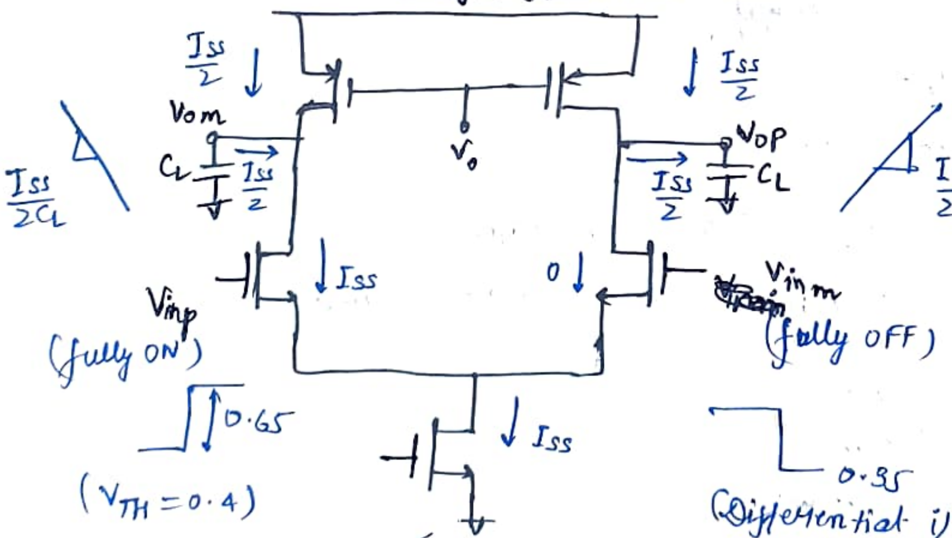
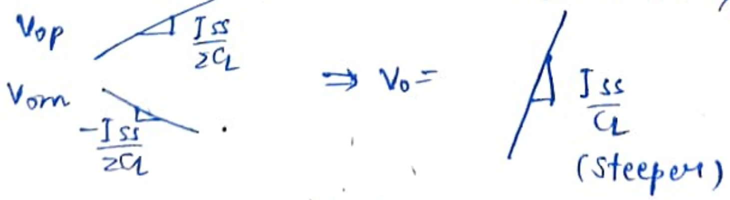
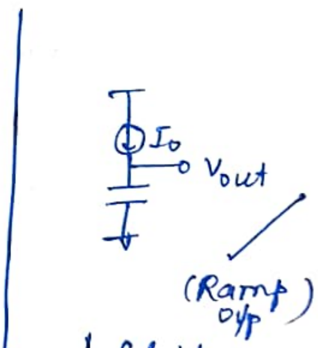
Fully differential Case:



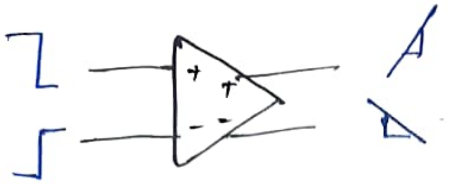




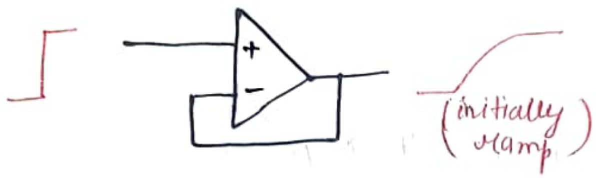
$\frac{1}{C}\int i\,dt = \frac{I_0}{C}t$ → slope

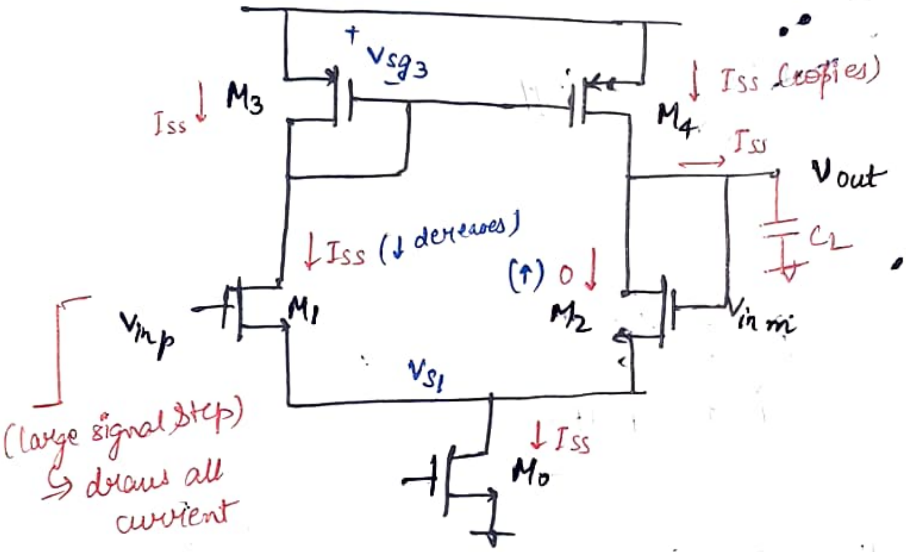
Slew rate $= \frac{I_{SS}}{C_L}$ ↑ ⇒ Power ↑

(Effect of slow rate ↓)



Single-ended case:





$V_{out} = \frac{I_{ss}}{C_L} t$

$S.R. = \frac{I_{ss}}{C_L}$

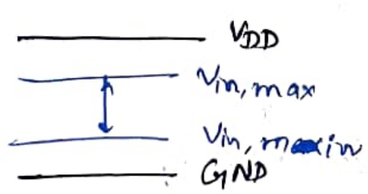
$V_{in,min} = V_{out,min} = V_{GS_2} + V_{d\,sat\,0}$

Saturation of M_1:

$V_{DS} \geq V_{GS} - V_{TH}$

$\Rightarrow V_{DD} - V_{SG_3} - \cancel{V_{S_1}} \geq V_{in} - \cancel{V_{S_1}} - V_{THN}$

$\Rightarrow V_{DD} - V_{SG_3} + V_{THN} \geq V_{in}$ → Max. limit



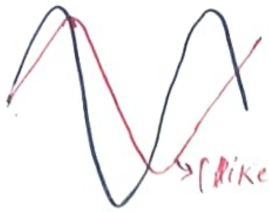
$V_{in} = A \sin \omega t$

$\frac{dV_{in}}{dt} = A\omega \cos \omega t$

$\left| \frac{dV_{in}}{dt} \right|_{max} = A\omega$ (max slope)

: For SR > Aω

If S.R > Aω ⇒ opamp will be able to track the i/p.



: For SR < Aω.

Gain = $g_m (r_{o2} \| r_{o4})$ → for diff / single-ended.

↳ For a single stage : Not sufficient gain

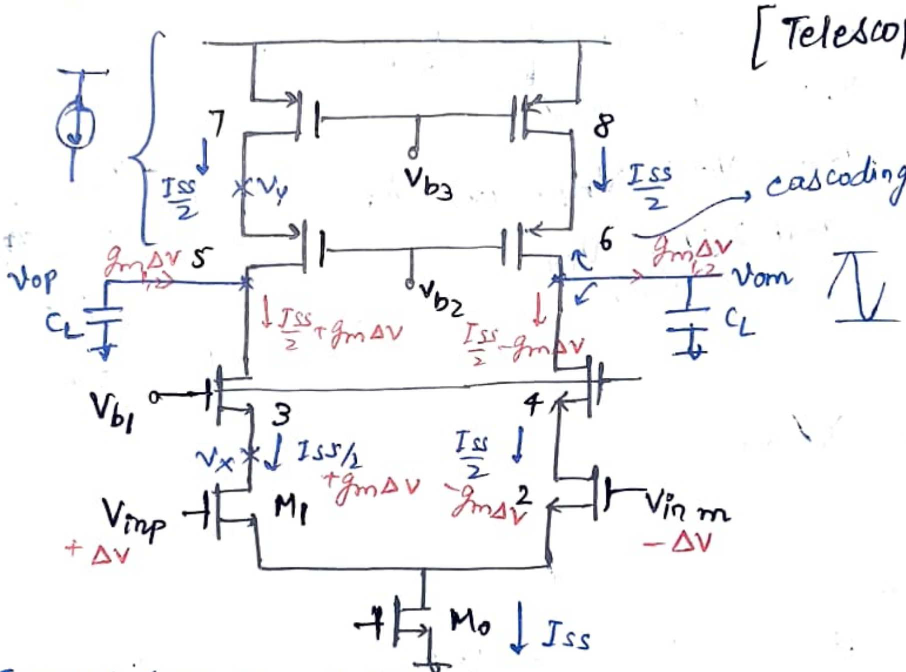
↳ ↑ ⇒ Large o/p impedance

⇓

Cascoding:

Fully differential case:

[Telescoping Cascodes]



Overall transconductance,

$G_M = g_{m1,2}$ (only equal to the i/p pair)

Output impedance,

$R_{out} = R_{up} \| R_{down}$

$= (r_{o6} + r_{o8} + g_{m6} r_{o6} r_{o8}) \| (r_{o4} + r_{o2} + g_{m4} r_{o2} r_{o4})$

$A_v = g_{m1,2} \cdot R_{out}$

$V_{in,min\,(CM)} = V_{GS1,2} + V_{dsat_0}$

31-10-2025

To find $V_{in,cm,max}$:

Saturation condition for $M_{1,2}$:

$$V_{DS1} \geq V_{GS1} - V_{TH}$$

$$\Rightarrow V_{b1} - V_{GS3,4} - \cancel{V_P} \geq V_{in,cm} - \cancel{V_P} - V_{TH}$$

$$\Rightarrow \underbrace{V_{in,cm}}_{V_{in,CM,max}} \leq \uparrow V_{b1} - V_{GS3,4} + V_{TH}$$

↳ larger i/p common mode range

Output swing limits:

$V_{out,min}$:

Saturation condition for $M_{3,4}$:

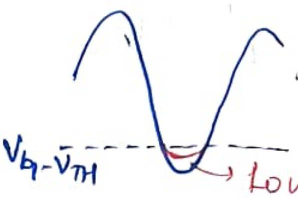
$$V_{DS,3} \geq V_{GS,3} - V_{TH}$$

$$\Rightarrow V_{out} - \cancel{V_X} \geq V_{b1} - \cancel{V_X} - V_{TH}$$

$$\Rightarrow V_{out} \geq \downarrow V_{b1} - V_{TH}$$

↳ Large swing (o/p)

T? 5,6 → first to go out of sat.
⇓
Then 7,8
⇓
others helped by gate bias.



→ Low gain here (Gain collapse)
↳ voltage-dependent gain

$V_{out,max}$:

Saturation condition for M_5:

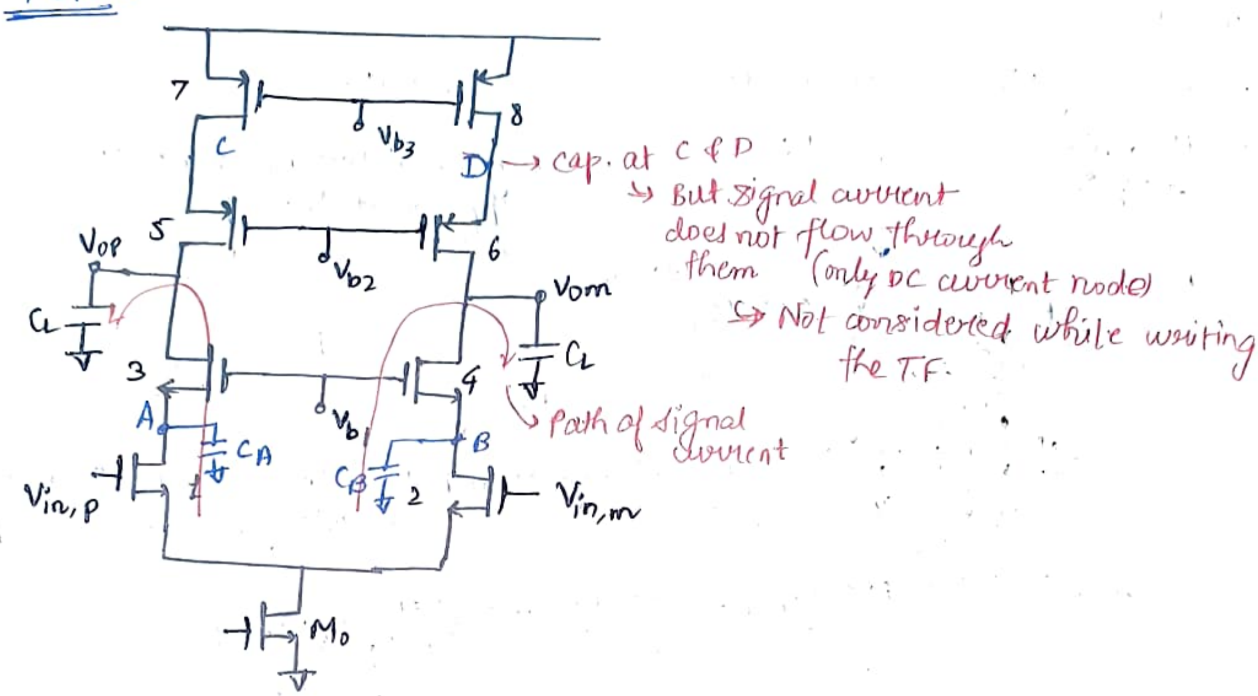
$$V_{SD5} \geq V_{SG5} - |V_{THP}|$$

$$\Rightarrow V_y - V_{out} \geq V_y - V_{b2} - |V_{THP}|$$

$$\Rightarrow V_{out} \leq \uparrow V_{b2} + |V_{THP}|$$

- Large gain limited by I/p common mode range and o/p swing limits.

Poles:



$$\omega_{p,out} = \frac{1}{R_{out} C_L'} \quad \longrightarrow \text{Dominant pole}$$

$C_L' = C_L + \text{parasitics}$

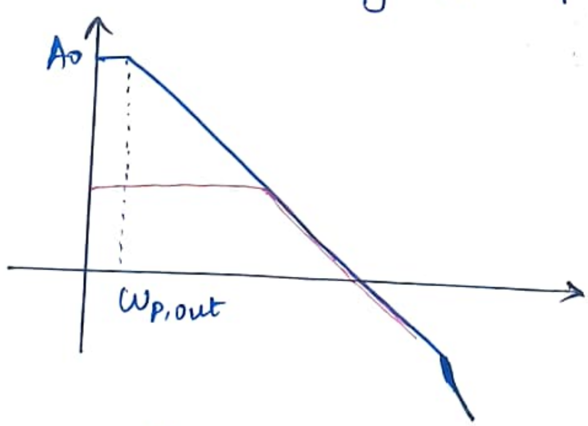
$C_A = C_{gs3} + C_{db1} + C_{gd1} + C_{sb3}$

$C_A = C_B$

$$\omega_{pA} = \frac{g_{m3}}{C_A} \quad \longrightarrow \text{Non-dominant pole}$$

$\omega_{p,out} \ll \omega_{pA}$

- Behaves like single-pole opamp.



$R_{out} \uparrow\uparrow \Rightarrow \omega_{p,out} \downarrow\downarrow$ (BW)

- Same g_m & C_L

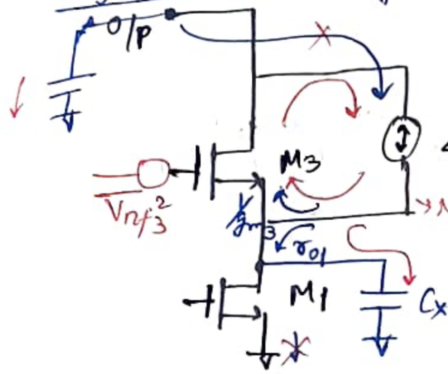
$$\omega_{UGF} = \frac{g_m}{C_L'}$$

→ Same ω_{UGF}

→ low gain for high 3-dB BW

Noises:

- Noise of M_0 is common-mode ⇒ Cancels out.
- M_3 noise: (Same for M_5)



- Only consider noises which appear at the o/p.

Noise from o/p sees low imp. of $1/g_{m3}$

↳ Noise, mostly go into M_3 and does not get a ground path.

↳ Noise current flows within this loop itself.

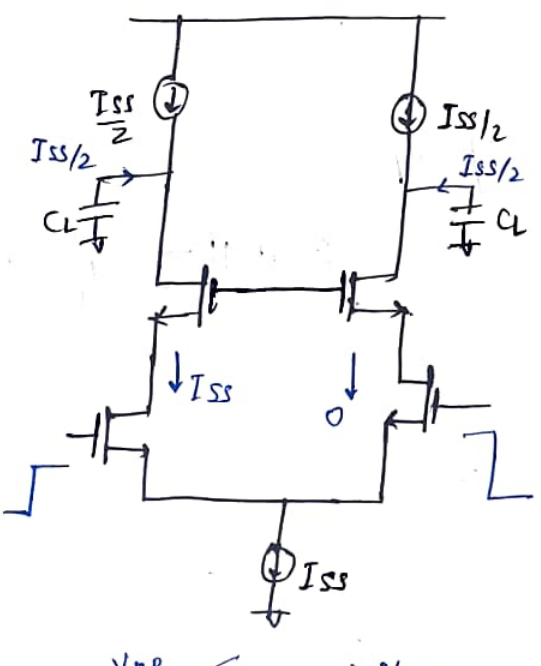
C_x ⇒ [If C_x is high ⇒ Imp ↓ ⇒ Noise finds GND path ⇒ Noise flows through o/p.]

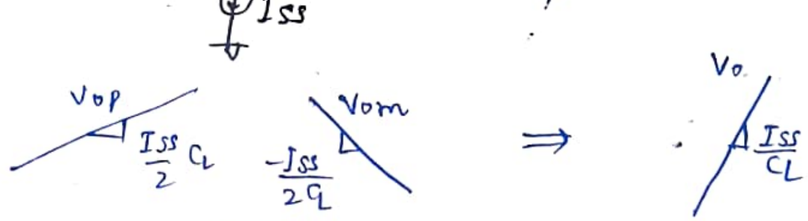
$$\overline{I_{n,out}^2} = 2\times\left(4KT\gamma g_{m1} + 4KT\gamma g_{m7} + \frac{K_N}{W_1 L_1 C_{ox} f}\cdot g_{m1}^2 + \frac{K_P}{W_7 L_7 C_{ox} f}\cdot g_{m7}^2\right)$$

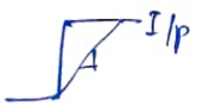
$$\overline{V_{n,in}^2} = \frac{\overline{I_{n,out}^2}}{g_{m1,2}^2}$$

- Noise of cascode transistors does not go into o/p.

Slew Rate:

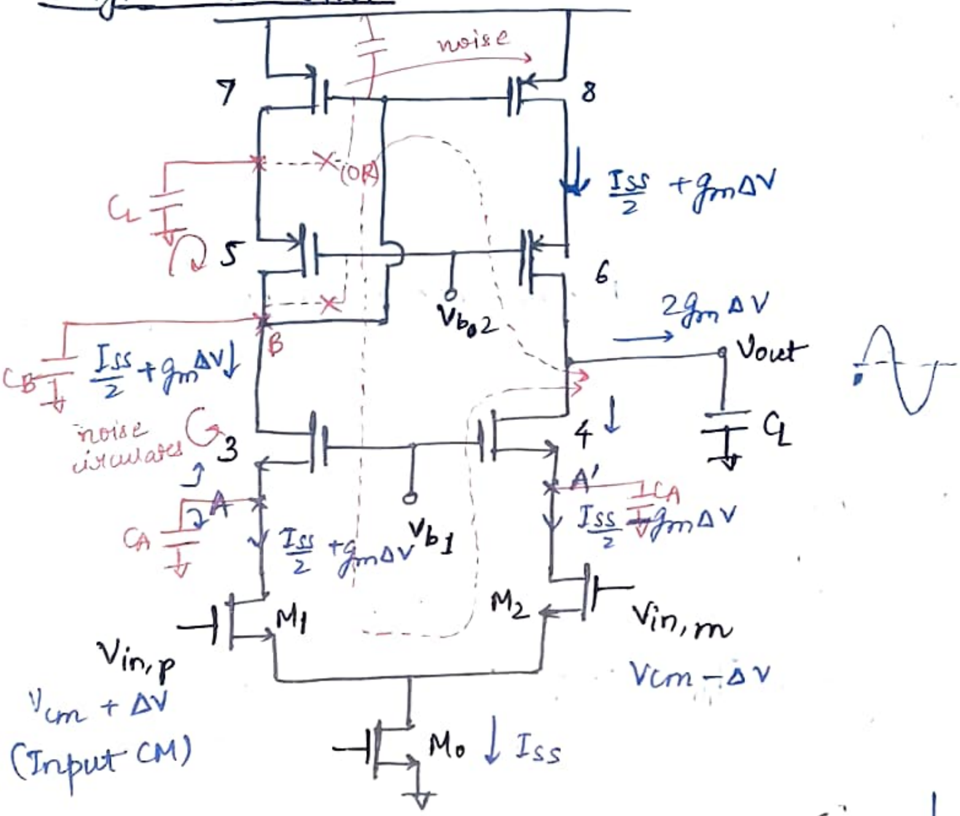






⇒ For higher slope ⇒ Tail current ↑

Single-ended Mode:



capacitive load

→ OTA and opamp are used interchangeably

$$G_M = \frac{2 g_m \Delta V}{2 \Delta V} = g_{m1,2}$$

$$R_{out} = (r_{o6} + r_{o8} + g_{m6} r_{o6} r_{o8}) \,||\, (r_{o2}' + r_{o4} + g_{m4} r_{o2} r_{o4})$$

↳ very large.

$$BW = \frac{1}{2\pi R_{out} C_L'}$$

$$C_L' = C_L + \text{parasities}$$

$$\omega_{PA} = \frac{g_{m3}}{C_A} \qquad [1/g_{m3} \rightarrow \text{dominant}]$$

$$C_A = C_{gd1}' + C_{db1} + C_{gs3} + C_{sb3}$$

$$C_B = C_{db3} + C_{gd3} + C_{gd5} + C_{db5} + C_{gs7} + C_{gs8}$$

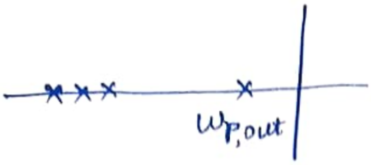
$$\omega_{PB} = \frac{g_{m7}}{C_B}$$

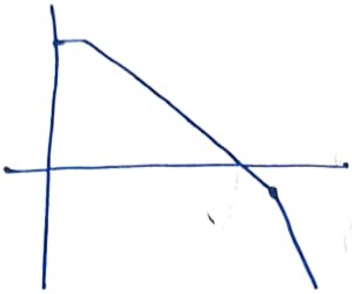
[Signal touches all the transistors here]

$$\omega_{PC} = \frac{g_{m5}}{C_C}$$

$$\underset{\text{dominant pole}}{\omega_{P,out}} = \frac{1}{R_{out} C_L'} \ll \underbrace{\omega_{PA}, \omega_{PB}, \omega_{PC}}_{\text{Non-dominant poles}}$$

[Total 4 poles]



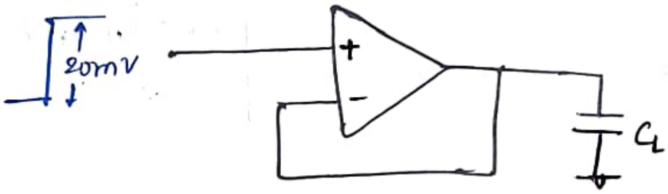


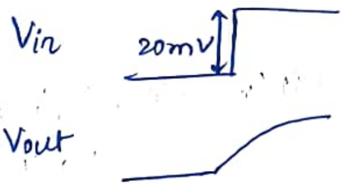
[Behaves like single pole system]

$$UGF = GBW = \frac{g_{m_{1,2}}}{2\pi C_L'}$$

Noises: Same as fully-differential case.

Slew Rate:





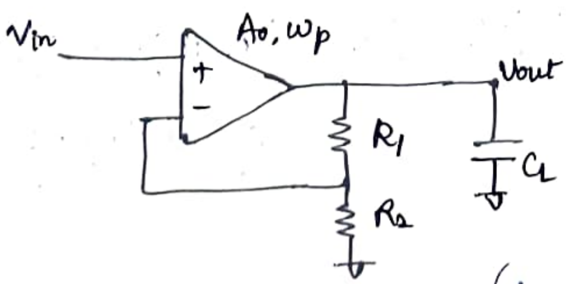
capacitor charges

Opamp: $\frac{A_0}{1+\frac{s}{\omega_p}} \xrightarrow{\text{UG Feedback}} \frac{A_0/1+s/\omega_p}{1+\frac{A_0}{1+\frac{s}{\omega_p}}}$; $\tau_{UGF} = \frac{1}{\omega_{UGF}}$

$$= \frac{\frac{A_0}{1+A_0}}{1+s/\omega_{UGF}}$$

$BW = \omega_{UGF} \simeq A_0\omega_p$ (GBW) (for 1st order)

Eg.



(non-inv. amplifier)

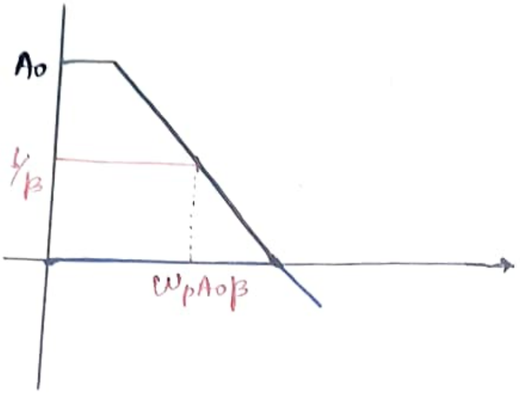
$$\beta = \frac{R_2}{R_1+R_2}$$

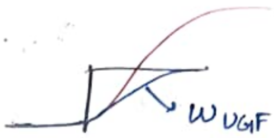
$$H(s) = \frac{V_{out}}{V_{in}}(s) = \frac{(1+R_1/R_2)}{1+\frac{s}{\omega_{p1}}}$$

$\omega_{p1} = \omega_p(1 + A_0\beta)$; $\tau_1 = \frac{1}{\omega_{p1}}$

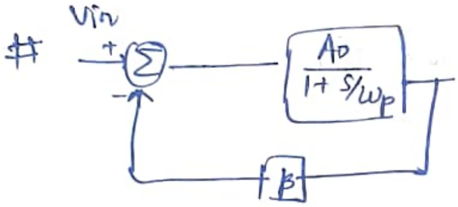
GBW product will be the same.

$\Rightarrow A_0\omega_p = \left(1 + \frac{R_1}{R_2}\right).\omega_{p1} \Rightarrow \omega_{p1}$ approx. same.



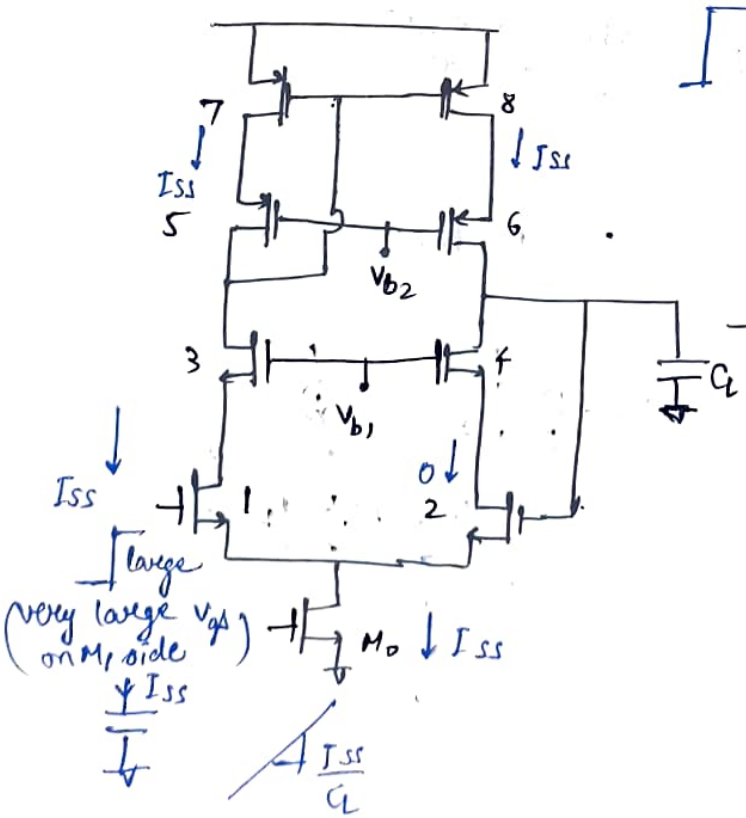


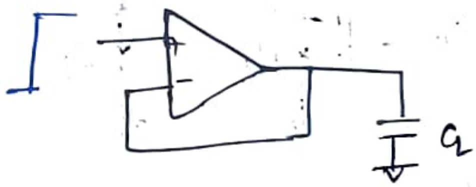
BW ↑ ⇒ Faster

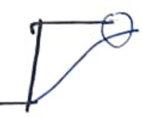


$$H(s) = \frac{\frac{A_0}{1+s/\omega_p}}{1 + \beta\frac{A_0}{1+s/\omega_p}} = \frac{A_0}{1 + s/\omega_p + \beta A_0} = \frac{\frac{A_0}{1+A_0\beta}}{1 + \frac{s}{\omega_p(1+A_0\beta)}}$$

<u>Unity-Gain Feedback</u> :





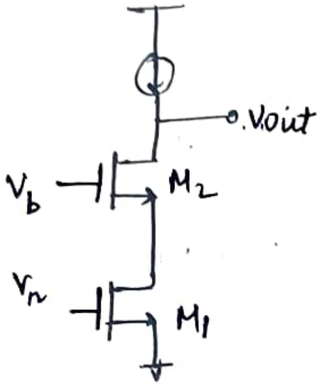


06-11-2025

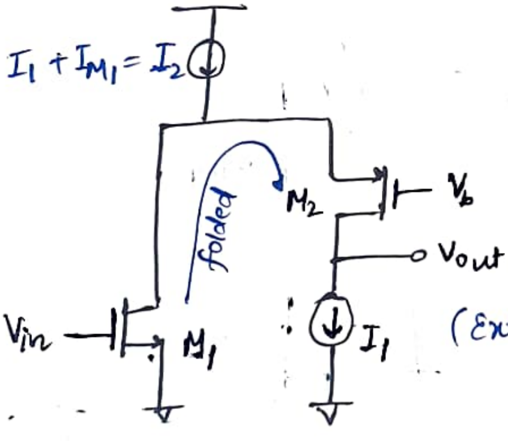
Folded Cascode

If input transistor is NMOS, change the cascoding transistor to PMOS, and vice-versa.

(Telescoping)

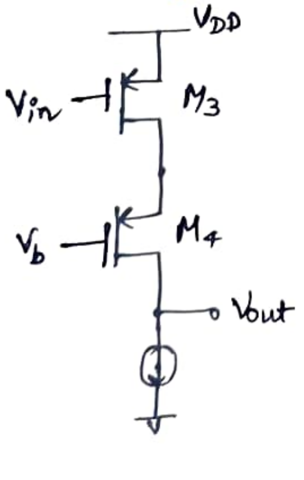


Only the type of transistor changes, other things like connections (of D, G, S) remain the same.

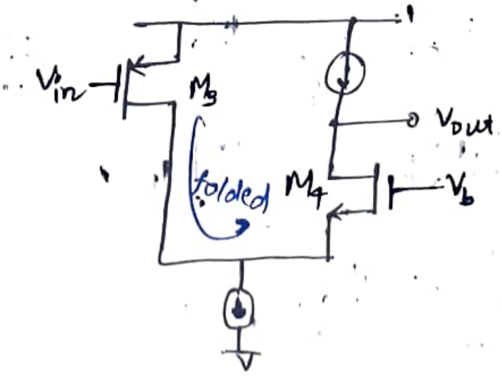


For PMOS:

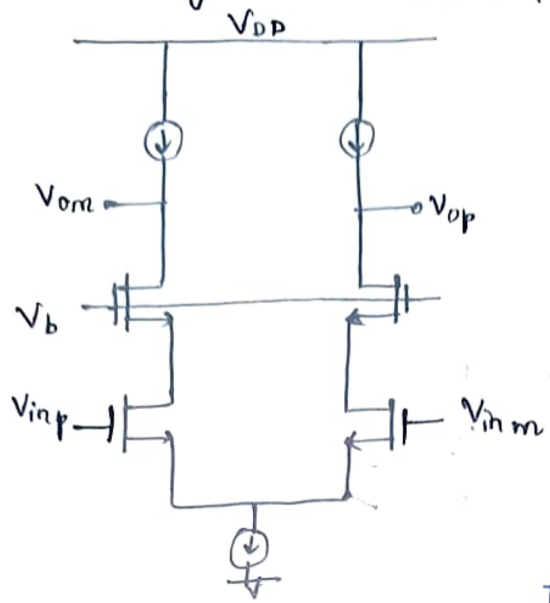
Telescoping

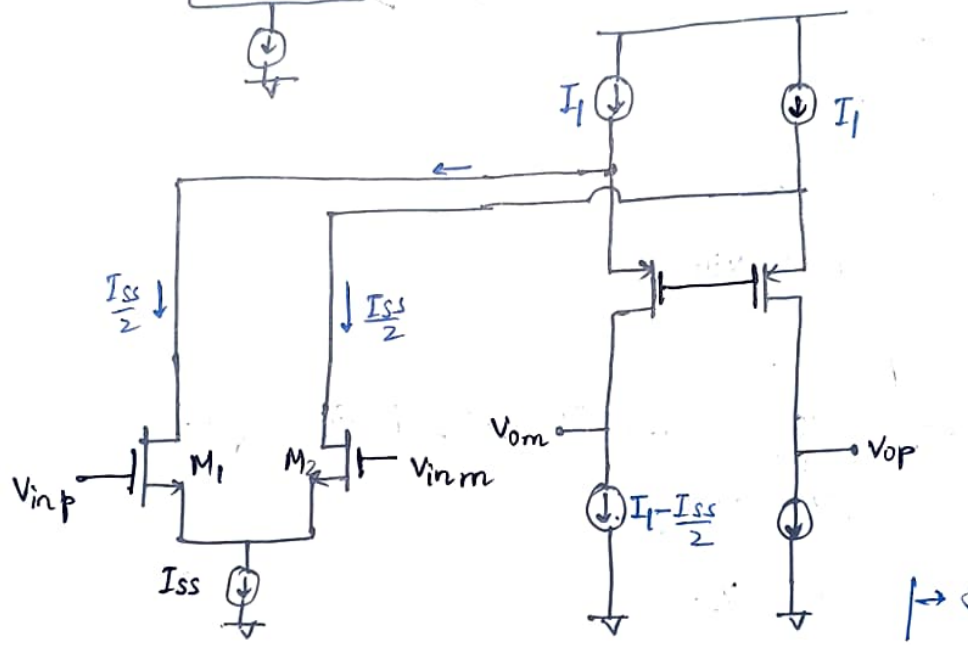


Folded:



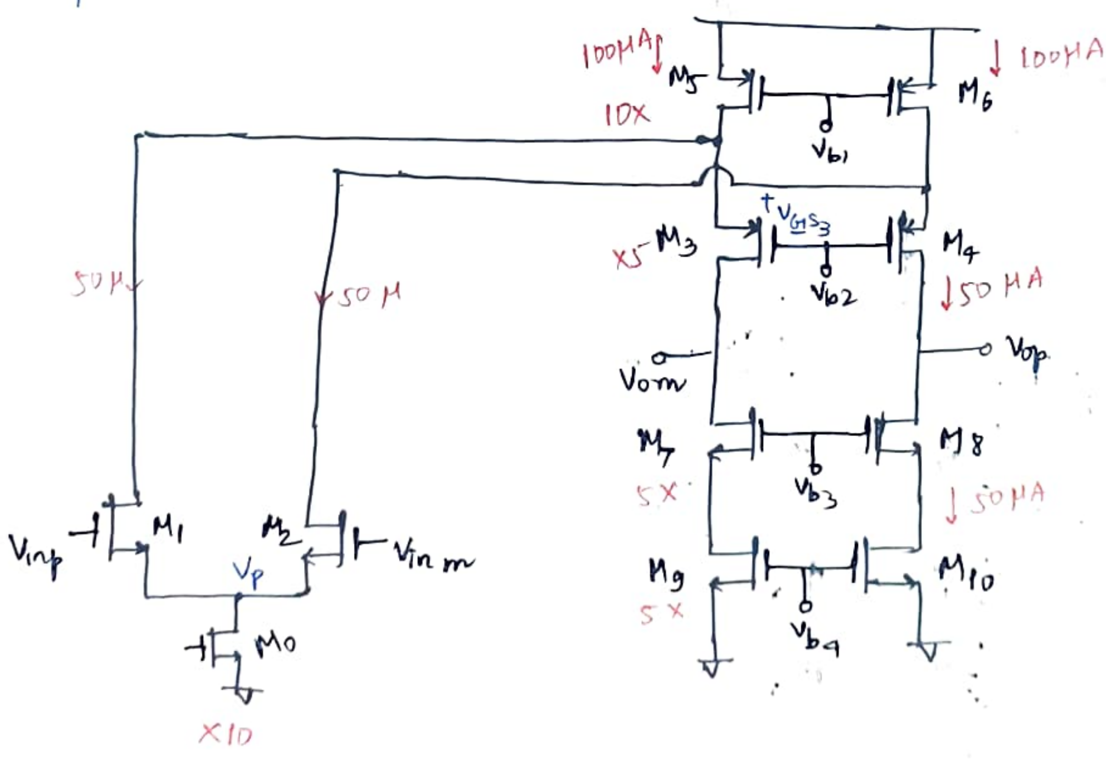
Convert singled ended cascode to folded cascode:





→ Solving input CM range

Replace current sources with MOS:



Input common Mode Range:

$$V_{in,CM,min} = V_{GS_{1,2}} + V_{dsat_0}$$

$V_{in,CM,max}$:

$$V_{DS1,2} \geq V_{GS_{1,2}} - V_{TH}$$

$$\Rightarrow V_{b_2} + V_{SG3,4} - V_P \geq V_{in,CM} - \cancel{V_P} - V_{TH}$$

$$\Rightarrow V_{inCM} \leq \underset{\uparrow}{V_b} + V_{SG3,4} + V_{TH} \quad > V_{DD}$$

Eg. $V_{DD} = 1.8\,V$

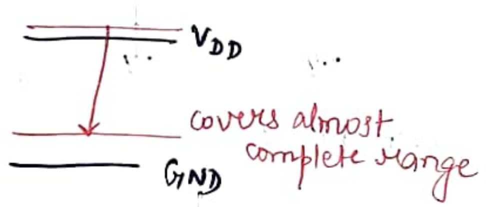
$V_{SG} = 0.6\,V$

$V_{TH} = 0.4\,V$

$V_b = 1\,V$

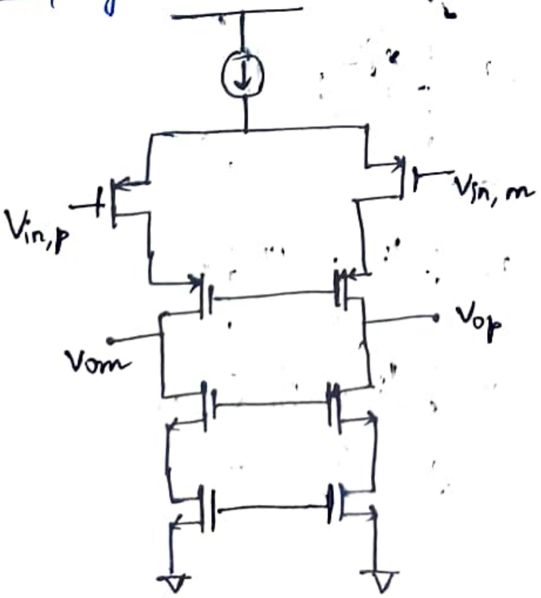
$V_{in,CM} \leq 2\,V \quad > V_{DD}$

- Large I/p CM range.
- If higher i/p is provided ($\geq V_{DD}$), lifetime of the device decrease (dies quickly).

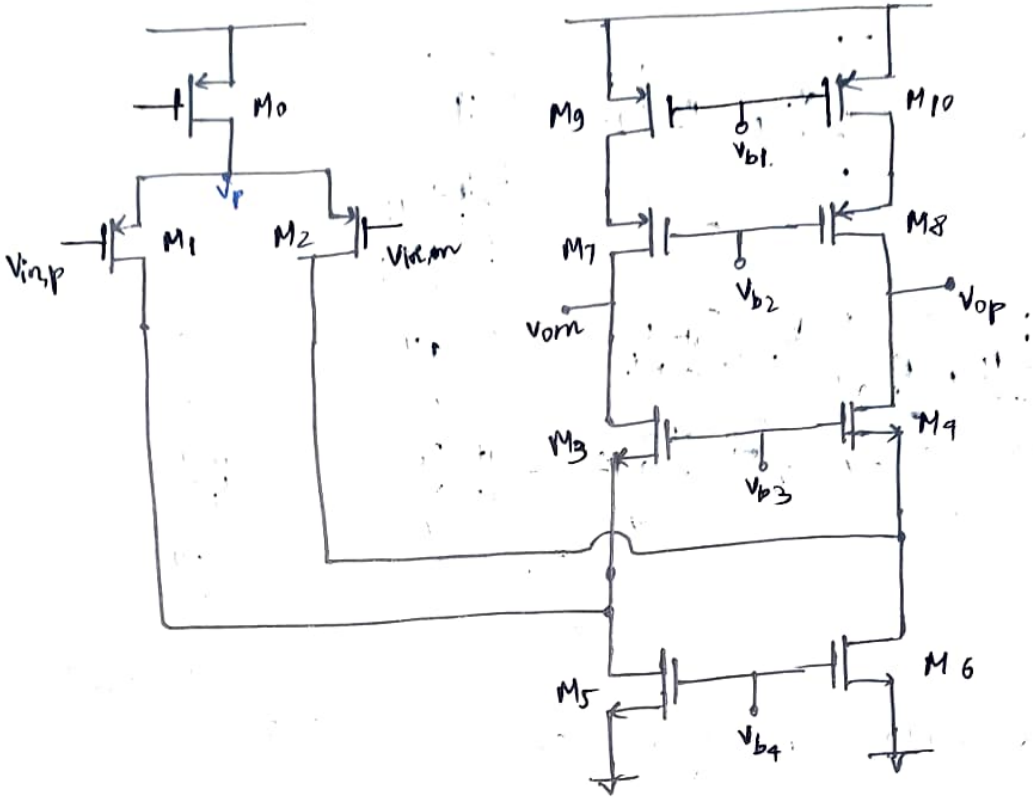


For PMOS:

Telescoping:



Folded :



$V_{in,CM,max} = V_{DD} - V_{d\,sat} - V_{SG1,2}$

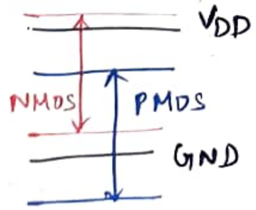
Saturation condition for $M_{1,2}$:

$$V_{SD1,2} \geq V_{SG1,2} - |V_{THP}|$$

$$\Rightarrow V_P - (V_{b3} - V_{GS3,4}) \geq V_P - V_{in,CM} - |V_{THP}|$$

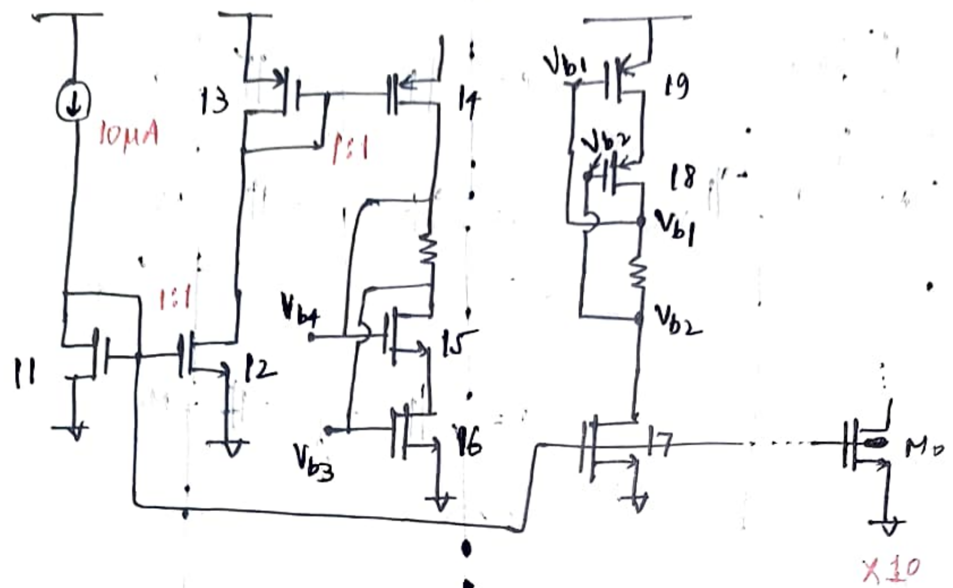
$$\Rightarrow V_{b3} - V_{GS3,4} \leq V_{in,CM} + |V_{THP}|$$

$$\Rightarrow V_{in,CM} \geq \underbrace{V_{b3} - V_{GS3,4} - |V_{THP}|}_{<0}$$



[Rail-to-Rail Inputs]

Generate bias voltages ($V_{b1}, V_{b2}, V_{b3}, V_{b4}$) using current mirror:



07-11-2025

Refer to N-MOS input folded cascode circuit:

$$G_m = \frac{2 g_{m_{1,2}} \Delta V}{2 \Delta V} = g_{m_{1,2}}$$

Effective ~~[illegible]~~ transconductance gain

$$R_{out} = \left(r_{o6} + (r_{o6} \| r_{o2}) + g_{m6}(r_{o6} \| r_{o2}) r_{o4}\right) \| \left(r_{o8} + r_{o10} + g_{m8} r_{o8} r_{o10}\right)$$

→ r_{o10} helps to increase the output impedance.

$$A_v = g_{m_{1,2}} \cdot R_{out}$$

- Due to $r_{o4} \| r_{o2}$, there will be a little difference in R_{out} in comparison to telescoping cascode.
- Demerit of this configuration is high power consumption.

$$Power = V_{DD} \times (I_{SS} \times 2 I_1)$$

Frequency Response:

$$\omega_{p,out} = \frac{1}{R_{out} C_L'}, \quad C_L' = C_L + \text{parasities}$$

$$\omega_{PA} = \frac{g_{m4}}{C_A} \quad \left(\because \frac{1}{g_{m4}} \| r_{o2} \| r_{o4} \propto \frac{1}{g_{m4}}\right)$$

$$\omega_{p\,out} \ll \omega_{PA}$$

$$UGF = \frac{g_{m1,2}}{2\pi C_L'}$$

$UGF = GBW$ (1st order)

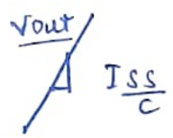
Noise

$$\overline{I_{n,out}^2} = 2 \times \left[4KT\gamma\,(g_{m1} + g_{m3} + g_{m9})\right] + 2\left[\frac{K_N}{W_1 L_1 C_{ox} f} g_{m1}^2 + \frac{K_P}{W_3 L_3 f C_{ox}} g_{m3}^2 + \frac{K_N}{W_9 L_9 C_{ox} f} g_{m9}^2\right]$$

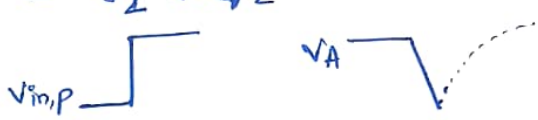
$$\overline{V_{n,in}} = \frac{\overline{I_{n,out}^2}}{g_{m1,2}}$$

Slew Rate:

① $I_1 > I_{SS}/2$

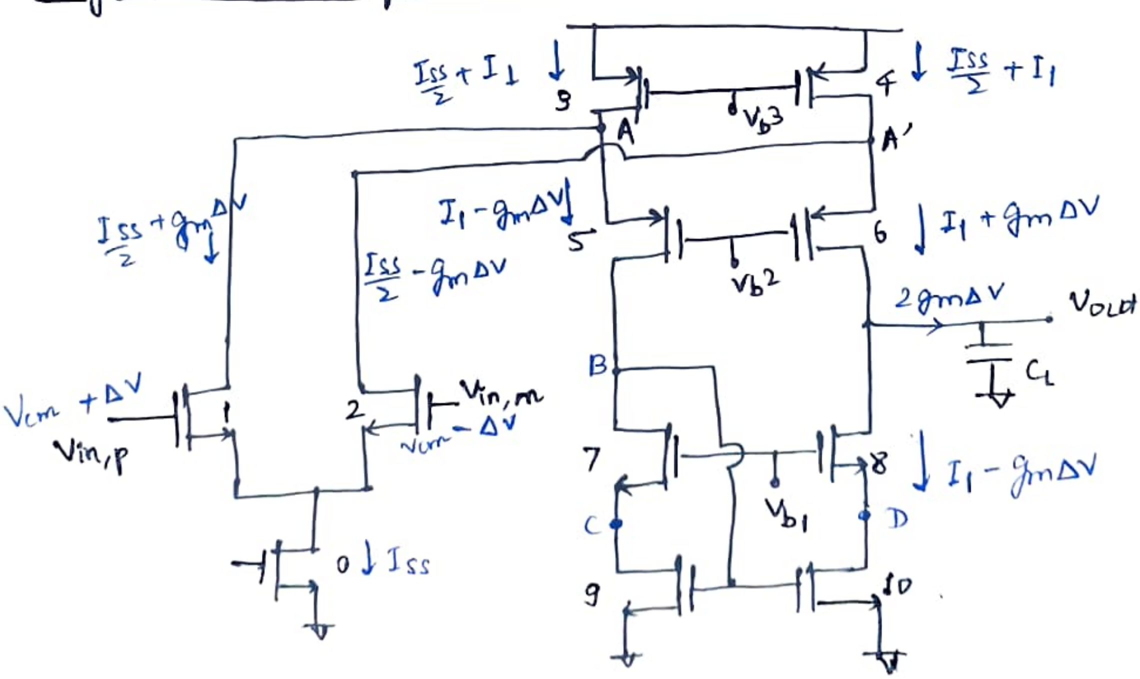


② $I_1 < I_{SS}/2$



- very bad slew rate (triode region)
- Make sure $I_1 > I_{SS}/2$.

Single-Ended Output OTA:



$G_m = g_{m1,2}$

$R_{out} = \left[(r_{o6} + r_{o2} \| r_{o4}) + g_{m6} r_{o6} (r_{o2} \| r_{o4}) \right] \| (r_{o8} + r_{o10} + g_{m8} r_{o8} r_{o10})$

$A_v = g_{m1,2} \cdot R_{out}$

$\omega_{p,out} = \dfrac{1}{R_{out} \cdot C_L'}$ (Dominant pole)

- More no. of non-dominant poles:

$\omega_{pA} = \dfrac{g_{m5}}{C_A} = \dfrac{1}{(r_{o1} \| r_{o3} \| 1/g_{m5}) C_A}$

$\omega_{pB} = \dfrac{g_{m9}}{C_B}$

$\omega_{pC} = \dfrac{g_{m7}}{C_C}$

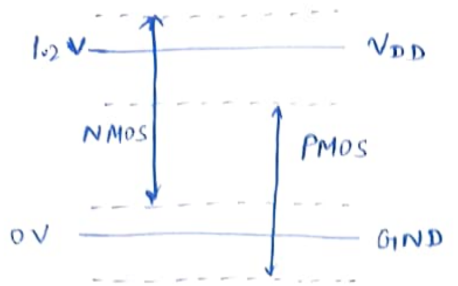
$\omega_{pD} = \dfrac{g_{m8}}{C_D}$

Slew Rate :

- Similar to fully differential

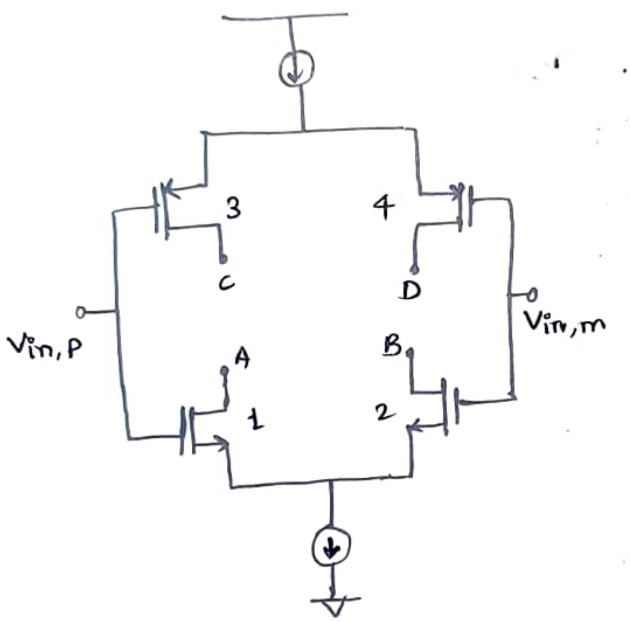
$I_1 \gg I_{SS}/2$

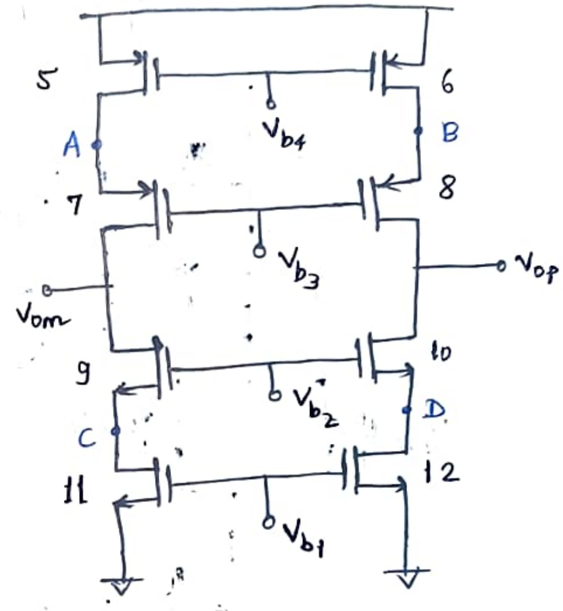
11-11-2025



- How to ensure $V_{in,cm}$ of GND to VDD?

Rail-to-Rail Input OTA (Input is Rail-to-Rail)





$V_{in,cm} \to 0 \Rightarrow$ PMOS is active, NMOS is OFF ($G_M = g_{mp}$)

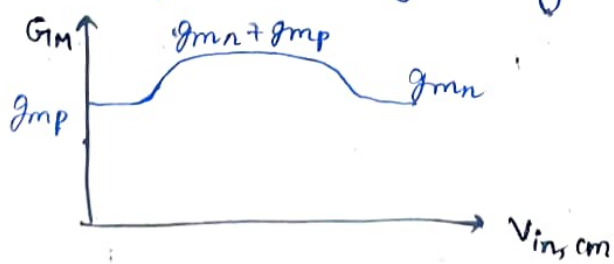
$V_{in,cm} \to V_{DD} \Rightarrow$ PMOS is off, NMOS is active. ($G_M = g_{mn}$)

$V_{in,cm} \sim \frac{V_{DD}}{2} \Rightarrow$ PMOS & NMOS are active

$$G_M = \underline{g_{mn} + g_{mp}}$$

↳ voltage-dependent transconductance.

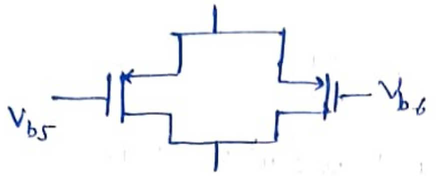
→ when operated using a negative feedback, it is linear.



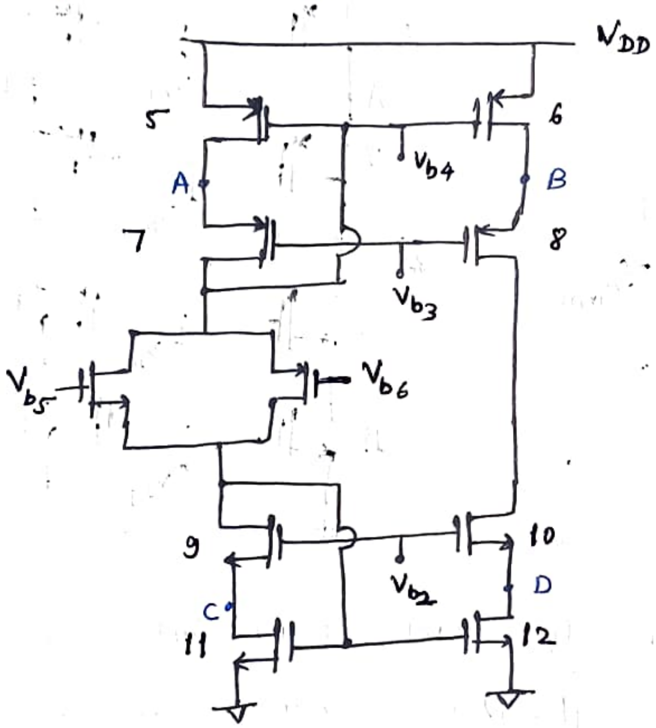
$$V_{out,max} = V_{DD} - (V_{b_3} - V_{SG_8}) - V_{sd\,sat_8}$$

$$V_{out,min} = V_{dsat_{10}} + V_{b_2} - V_{GS_{10}}$$

FVS: Floating voltage source
(To isolate both nodes at V_{cm})

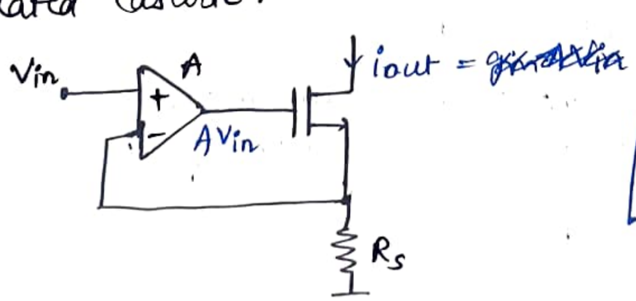


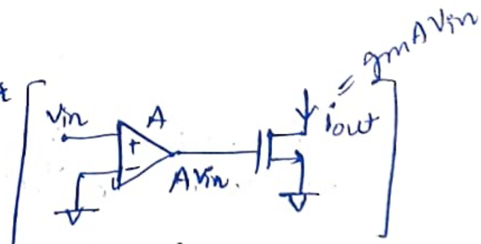
For single-ended output, put a FVS.



For very high gain (100, 120 dB):

Regulated Cascode:





$G_m = A g_m$
(Boosted transconductance)

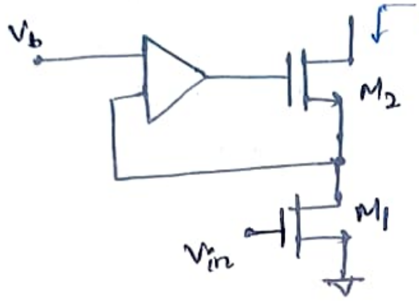
$$i_{out} = g_m\left[A(V_{in} - i_{out}R_s) - i_{out}R_s\right]$$

$$G_m = \frac{i_{out}}{V_{in}} = \frac{A g_m}{1 + A g_m R_s + g_m R_s} = \frac{A g_m}{1 + R_s(1 + g_m A)}$$

$R_{out} = r_o + R_S + (1+A)\, g_m r_o R_S$

$\simeq r_o + R_S + A g_m r_o R_S$ [very ~~out~~ high output resistance)

Cascoded :

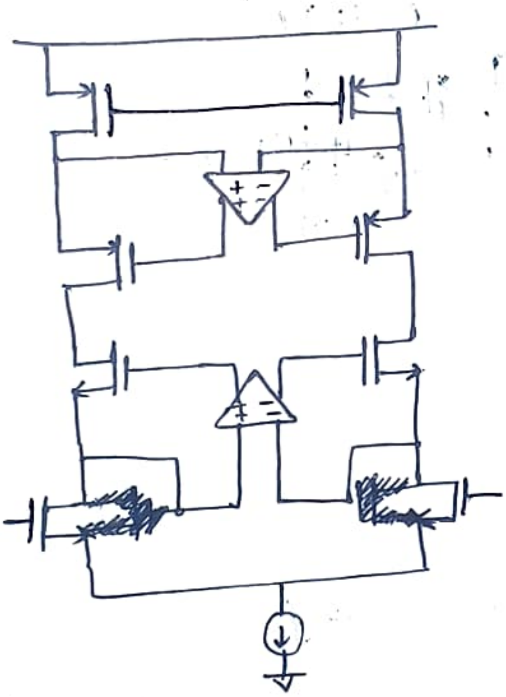


$R_{out} = r_{o1} + r_{o2} + (1+A)\, g_{m_2} r_{o1} r_{o2}$

↳ Regulated Cascode / Gain-boosted OTA

↳ Bandwidth ↓

3-MOS cascaded ↳ Large Space



How to implement the amplifier (opamp)?

→ Use NMOS CS topology mitigation

$V_{DS_1} = V_{GS_3}$

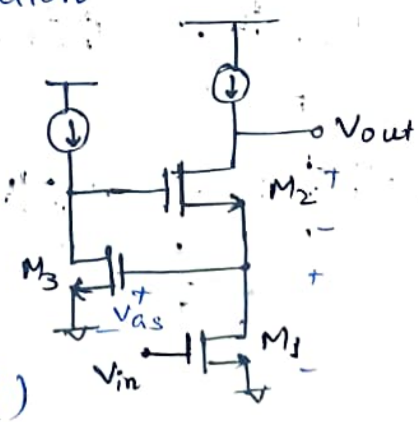
↳ For M_3 to work, V_{DS_1} should be large enough.

Due to this,

$V_{DS\,min} \neq V_{dsat}$

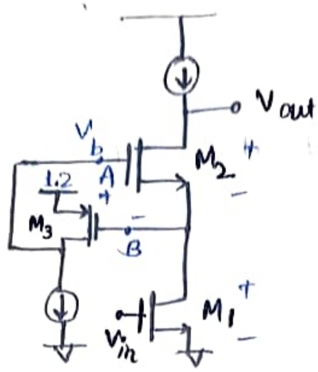
⇒ $V_{D\,min} = V_{TH_3}$ (for M_3 to work)

⇒ $V_{out,\,min}$ ↑



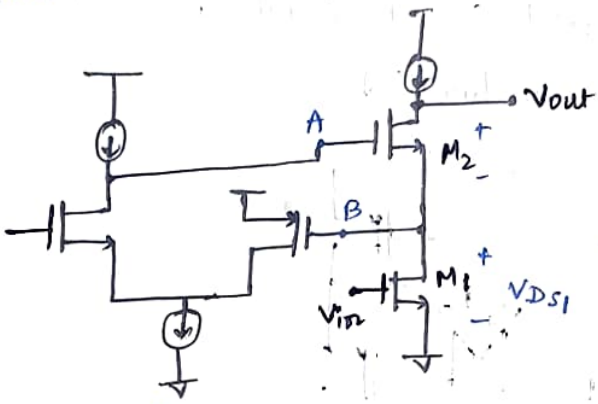
Mitigation:

→ Use PMOS :

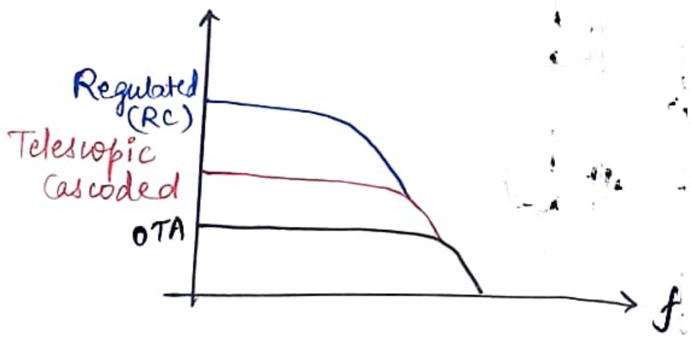


→ But M_3 can have very high V_{GS} and less V_{DS} (b/c V_b has to be low)
∴ → M_3 may go to triode region
∴ → Not a good design

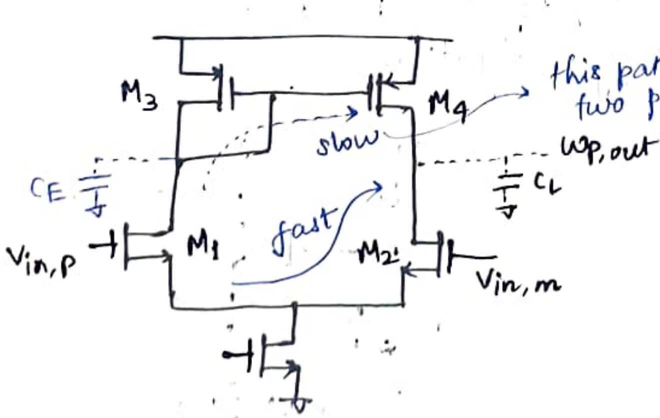
→ Use folded :



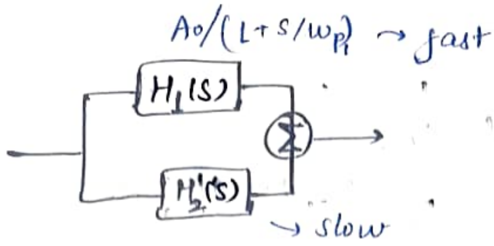
→ Bandwidth will decrease.



13-11-2025



this path experiences two poles



$$A_0 \left[\frac{1}{(1+ s/\omega_{p1})(1+ s/\omega_{p2})} \right]$$

- Presence of a transmission zero.

$$H(s) = H_1(s) + H_2(s)$$

$$= \frac{A_0}{1+ s/\omega_{p1}} + \frac{A_0}{(1+ s/\omega_{p1})(1+ s/\omega_{p2})}$$

$$= \frac{A_0}{1+ s/\omega_{p1}} \left[1 + \frac{1}{1+ s/\omega_{p2}} \right]$$

$$= \frac{A_0}{(1+ s/\omega_{p1})} \cdot \frac{(2+ s/\omega_{p2})}{(1+ s/\omega_{p2})}$$

$$s_z = -2\omega_{p2}$$

$$\omega_{p1} << \omega_{p2}$$

- But zero is located @ $2\omega_{p2}$.
- Anyway, if there are two paths for a signal, there will be a zero.

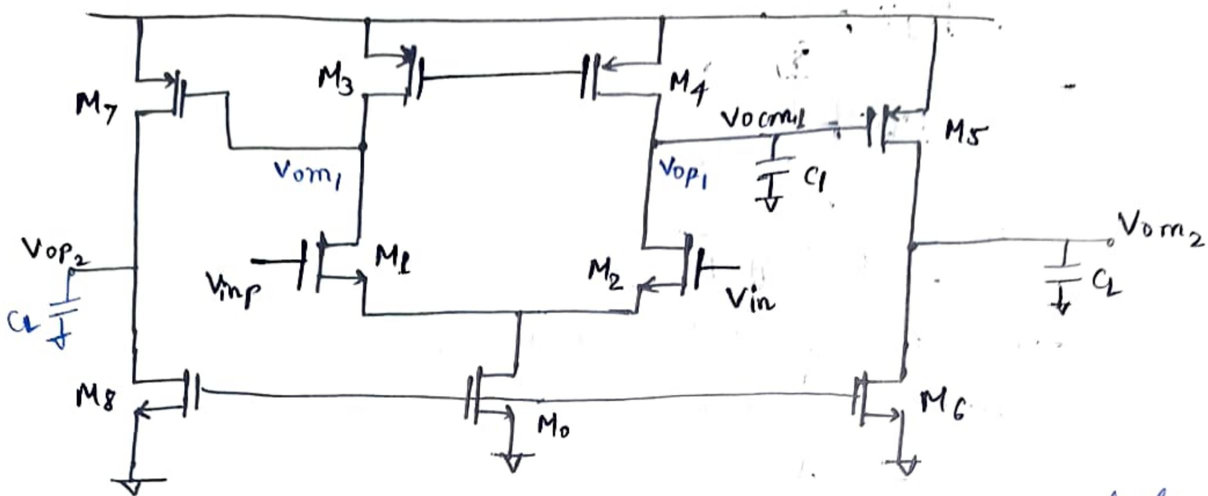
2-Stage OTA

(any topology; high gain) (CS; high swing)

→ High gain
→ very good output swing.

$$A_v = A_{v1} \cdot A_{v2}$$

- Regulated-topology has very low B/W with high gain.



→ If CS is NMOS, high voltage is required.

$$A_v = g_{m1}(r_{o2} \parallel r_{o4}) \cdot g_{m5}(r_{o6} \parallel r_{o5})$$

$$V_{out,max} = V_{DD} - V_{sd\,sat\,5,7}$$

$$V_{out,min} = V_{d\,sat\,6,8}$$

$$\omega_{p1} = \frac{1}{R_{out1} C_1} = \frac{1}{(r_{o2} \parallel r_{o4}) C_1}$$

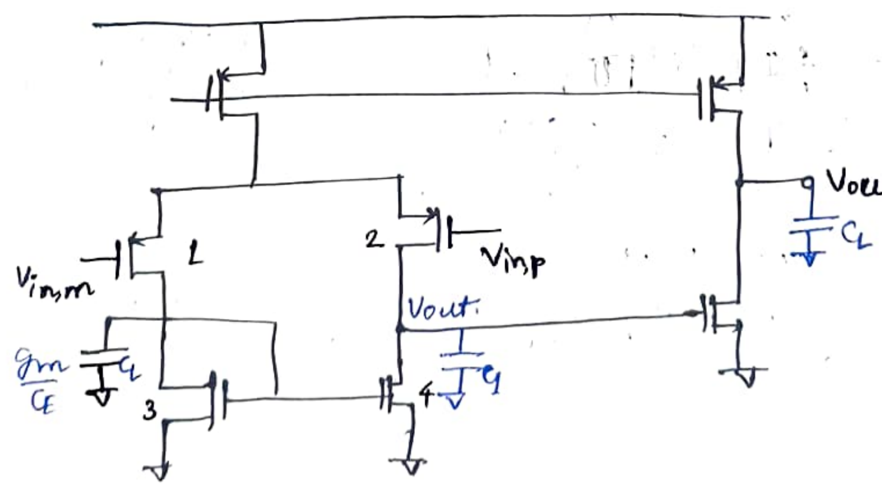
$$\omega_{p2} = \frac{1}{R_{out2} C_2} = \frac{1}{(r_{o5} \parallel r_{o6}) C_L}$$

→ R_{out1} can be > R_{out2}

→ Both pole are nearby (within UGF).

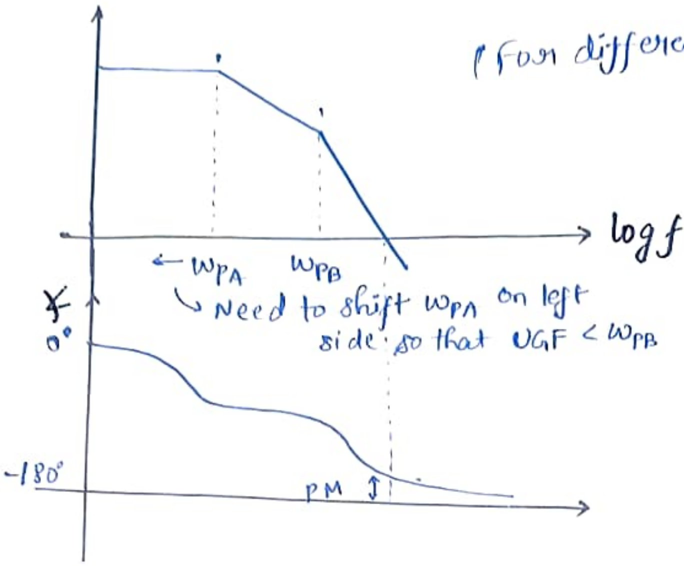
→ Advantage: High gain; high i/p common mode swing.

Single-ended:



$\omega_p = \frac{g_m}{C_E}$

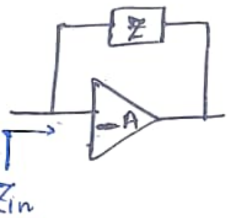
(For differential)



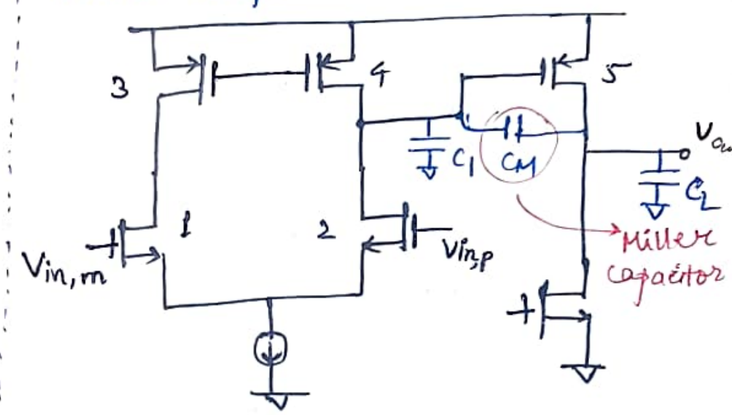
→ Poor phase margin
↳ Needs to be improved

Miller Effect

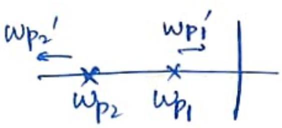
$$Z_{in} = \frac{Z}{1+A}$$
$$= \frac{1}{sC(1+A)}$$
$$= \frac{1}{sC'}, \quad C' = C(1+A)$$



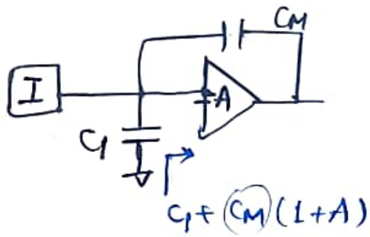
Miller Compensation:



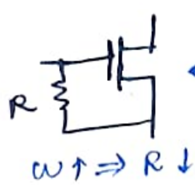
$$\omega_{p1} = \frac{1}{R_{out,1} C_1}$$
$$\downarrow$$
$$\omega_{p1}' = \frac{1}{R_{out}\left[C_1 + (1 + g_{m5}(r_{o5} \| r_{o6}))\right] C_M}$$

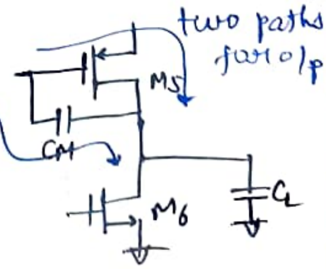


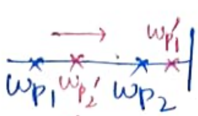
(Pole splitting)

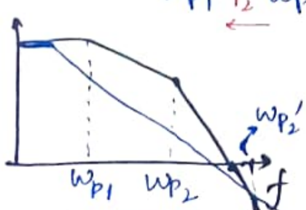


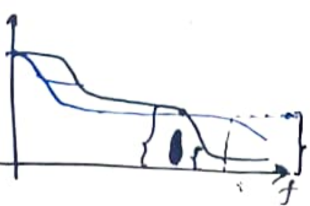
- At high frequency, $\frac{1}{j\omega C_M} \downarrow$ ($C_M \rightarrow$ impedance)$\downarrow$,
  $M_5 \rightarrow$ like diode-connected.
  $$\omega_{p2} = \frac{1}{R_{out2}(C_L + C_M)}, \quad R_{out} = (r_{o6} \| r_{o5})$$
  @ high freq., $R_{out5} = 1/g_{m5} \downarrow$ ($\omega_{p2} \uparrow$) → Bootstroping
- to give extremely large capacitive load,





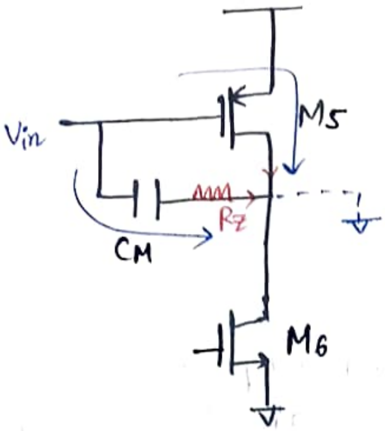






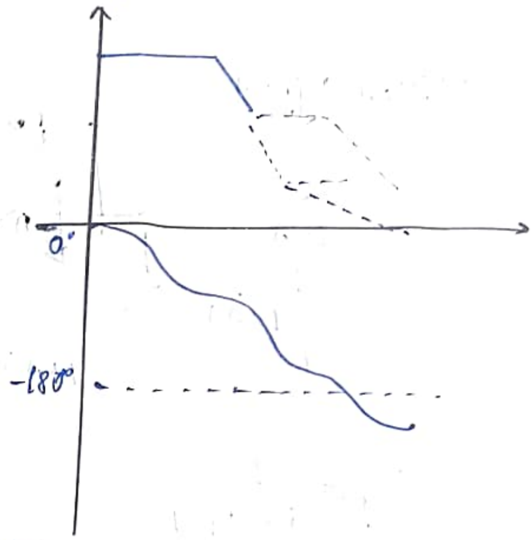
Good phase margin

14-11-2025



$s(C_M + C_{gd5}) \cdot V_{in} = g_m V_{in}$ (Condn for a zero)

$$\Rightarrow \omega_Z = \frac{g_{m5}}{C_M + C_{gd5}}$$



$\left(1 - s/\omega_Z\right)$

$-\tan^{-1}\left(\frac{\omega}{\omega_Z}\right)$

RHP zero $\rightarrow$ -ve phase shift

$\Rightarrow$ worsen the problem $\Rightarrow$ Unstable.

$\Rightarrow$ solve by adding a resistor (R_Z) [LHP]

$$g_m V_{in} = \frac{V_{in}}{R_Z + \frac{1}{sC_M}}$$ [Current from two paths]

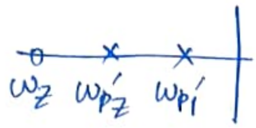
$$\Rightarrow \frac{1}{sC_M} + R_Z = \frac{1}{g_m}$$

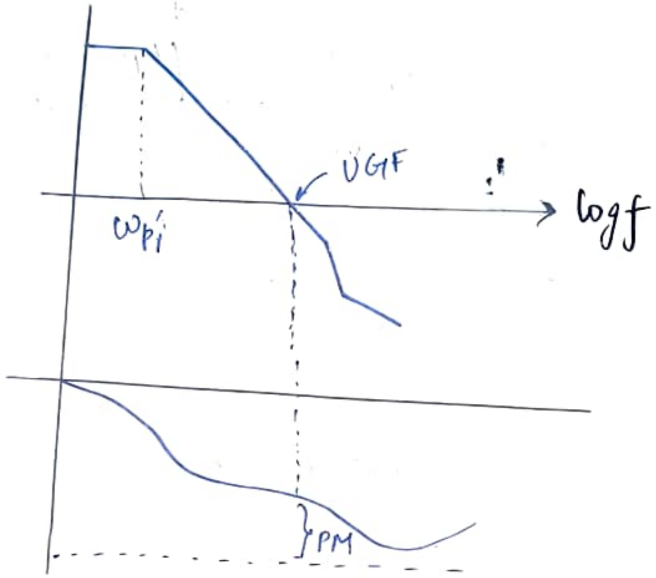
$$\Rightarrow \frac{1}{sC_M} = \frac{1}{g_m} - R_Z$$

$$\Rightarrow \omega_Z = \frac{1}{C_M\left(\frac{1}{g_m} - R_Z\right)}$$

Case 1: (1) $1/g_{m5} = R_Z$ [Zero at infinite freq.]

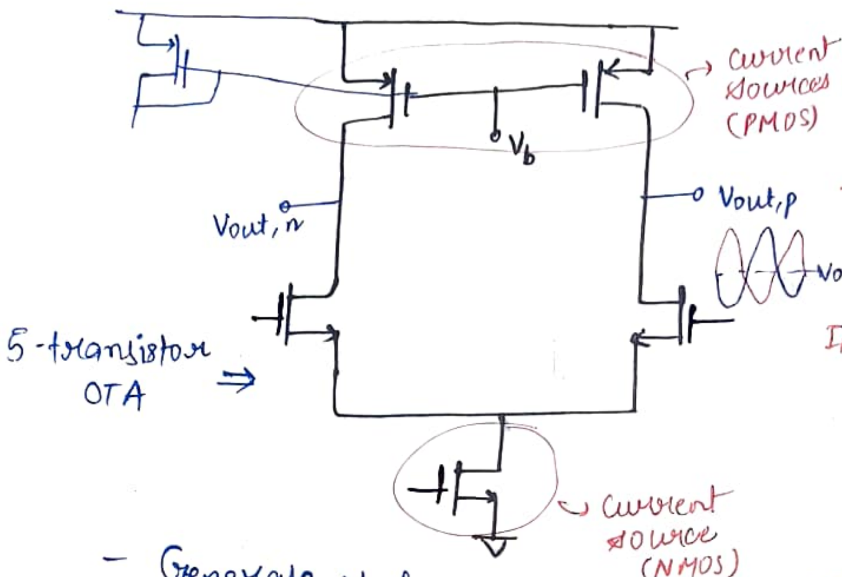
Case 2: (2) $R_Z > 1/g_m$ [Zero becomes -ve]

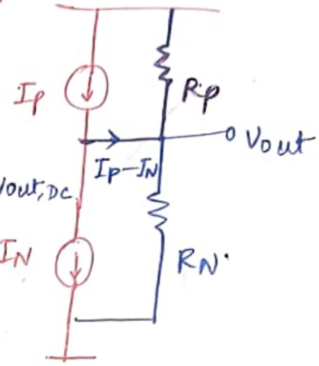




- High gain, o/p swing.
- Reasonable BW, UGF

Common Mode Feedback (CMFB)





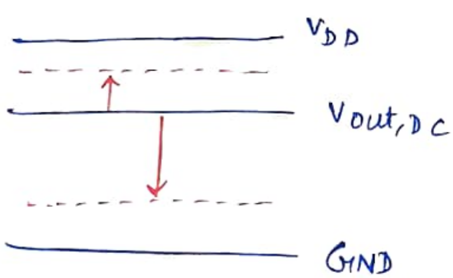
- Generate V_b by current mirror ⇒ May not be accurate
- Process variation of PMOS and NMOS may not be the same.
- Sum of current from 2 PMOS current sources should be same as current from NMOS source.
  ↳ May not be the case.

  In reality, sources are not ideal.

$I_P = I_N$ → ideal

$I_P > I_N$ → V_{out} ↑

$I_P < I_N$ → V_{out} ↓

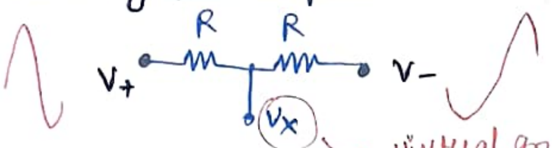


Correction Mechanism:

1. Sensing $V_{out,CM}$
2. Correcting either PMOS or NMOS source (let the other be on its own)

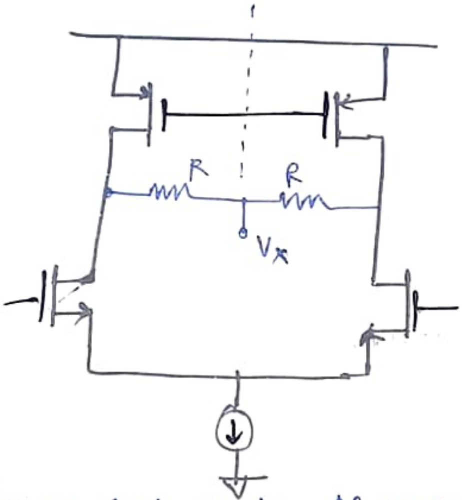
- Every fully differential circuit will have CMFB. (simulations may not have)

Sensing CM output:

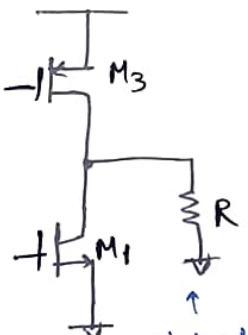


→ virtual gnd for diff. signals

$V_x = \frac{V_+}{2} + \frac{V_-}{2}$ (avg. of V_+ & V_-)



Differential-Mode Half Circuit: To see the effect on gain



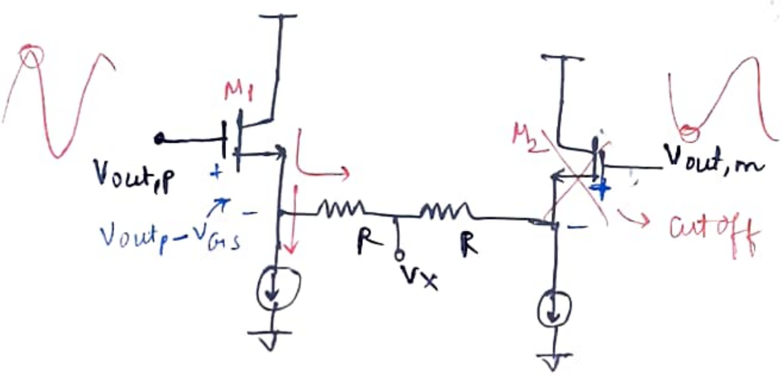
↑ virtual gnd

$\text{Gain} = g_{m1}(r_{o1} \| r_{o3} \| R)$

$R \gg r_{o1} \| r_{o3}$ ✓ [Little more area / real-estate required]

For telescope / FC ✗ → very bad choice

↳ either area will increase too much or low gain.



→ Resistors are not interfering o/p node

⇒ Gain will not change.

→ Voltage drop ($V_{out_p} - V_{GS}$) on both-side ⇒ No effect

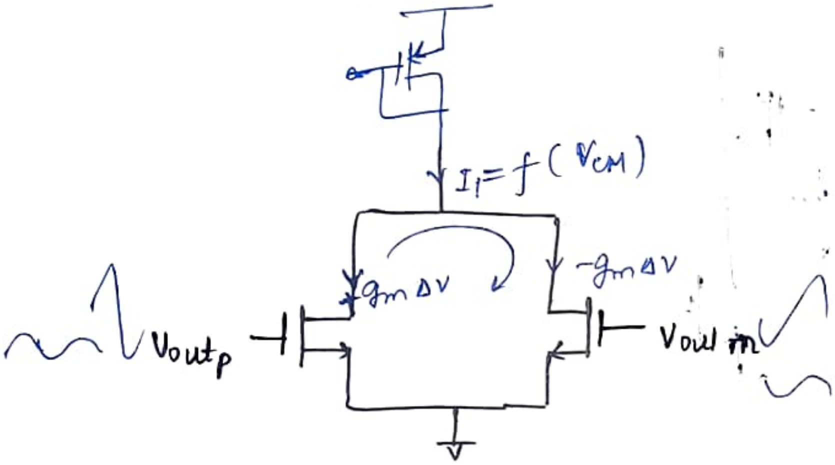
Limitation: cannot handle large o/p signal.

For large voltages, M_2 will go into cutoff when voltage is min.

↳ M_1 has to supply both currents

↳ common-mode voltage may not be accurate.

Short the drain Nodes:



Same problem: cannot handle large o/p signal.

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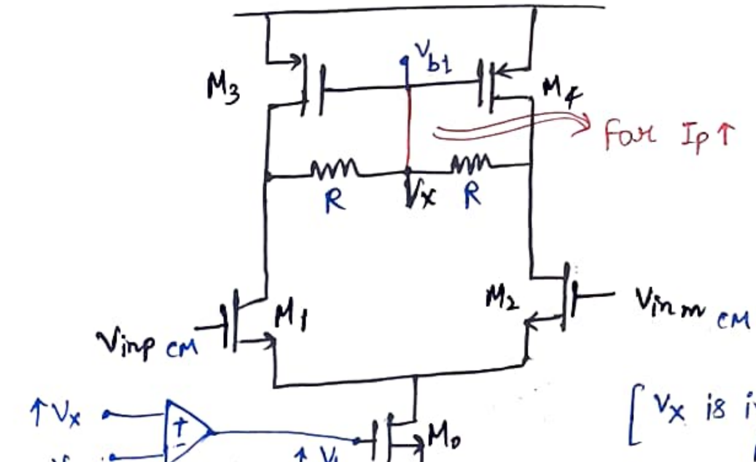


[V_x is in phase with V_{b0} (↑), so it has to be +ve terminal of opamp]

(Required o/p CM voltage) ⇓ For I_N ↑

$I_P > V_N \Rightarrow V_{out,CM}$ ↑ (V_x ↑)

↓

Solutions

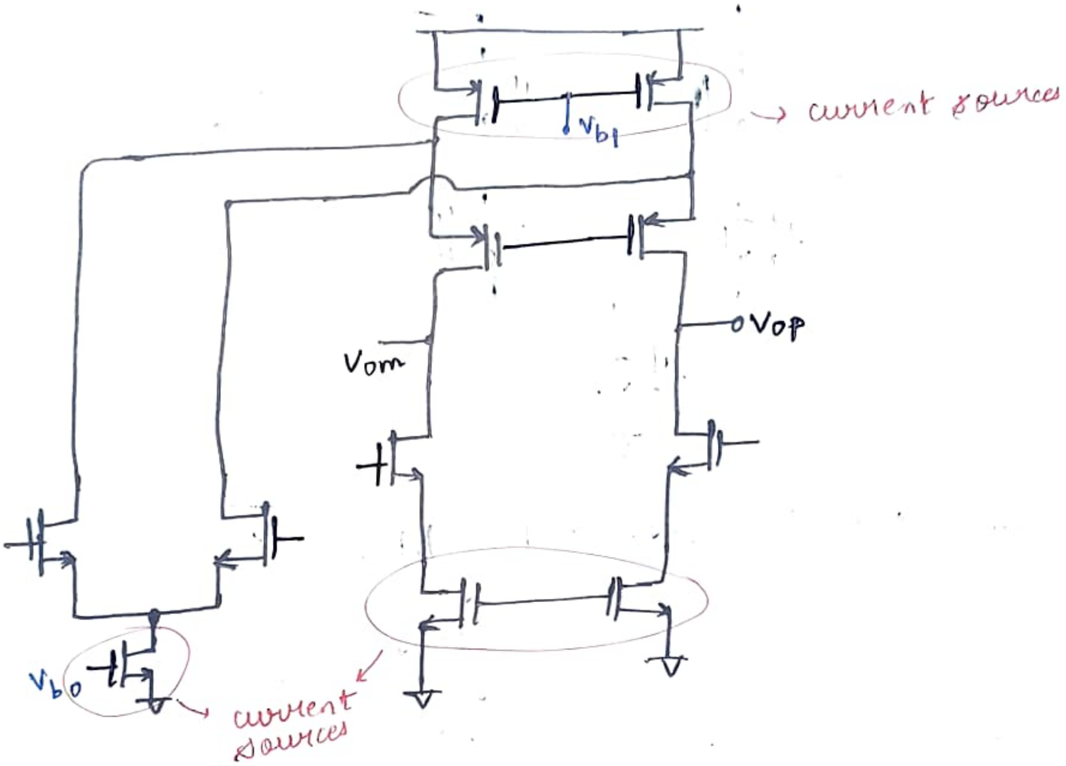
I_P ↑ (PMOS gate ↑) Controlling PMOS current

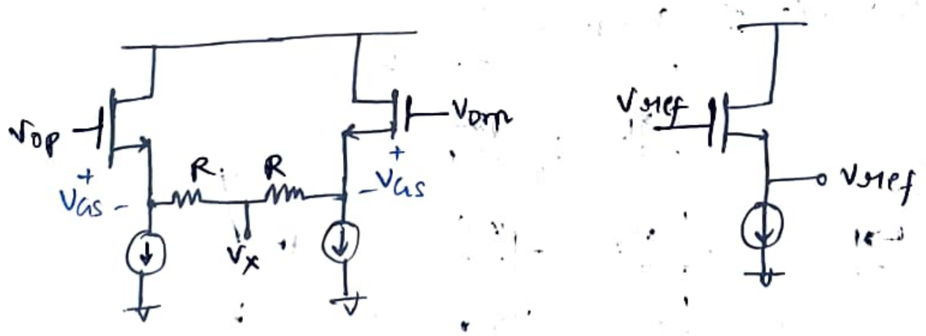
I_N ↑ ⇓ V_b ↑

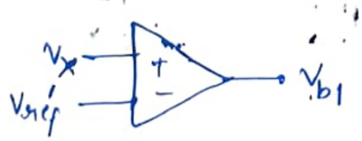
Another advantage:

V_x reacts to CM ac signals @ i/p ; reducing the CM signals within the BW of CMFB loop.

(Again V_x will be +ve terminal)





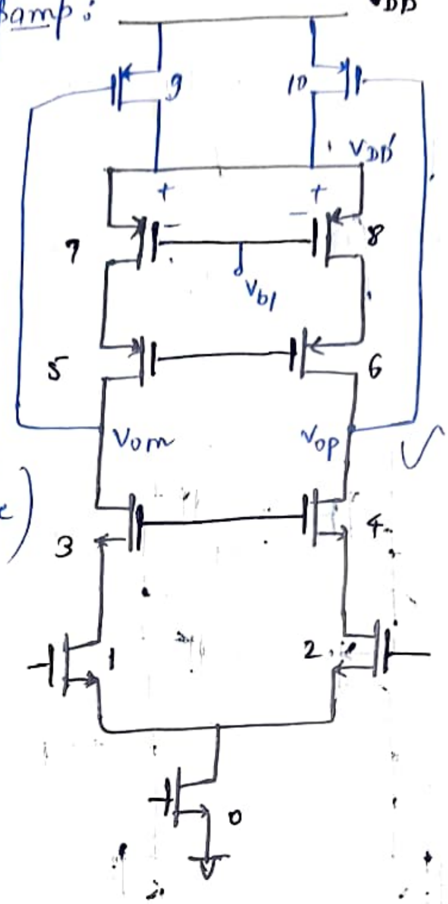


[Same terminals for V_{b0}]

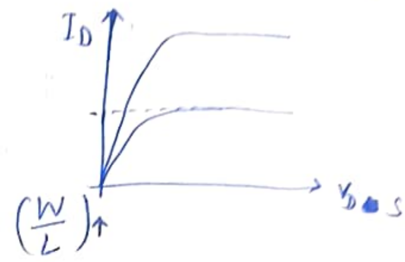
$V_x \uparrow$ $(I_P > I_N)$

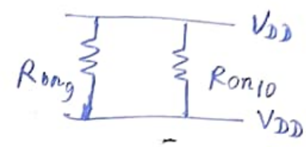
Soln: $I_P \downarrow \longrightarrow V_{b1} \uparrow$

Without additional opamp:



[Transistors 9 and 10 are kept in triode]



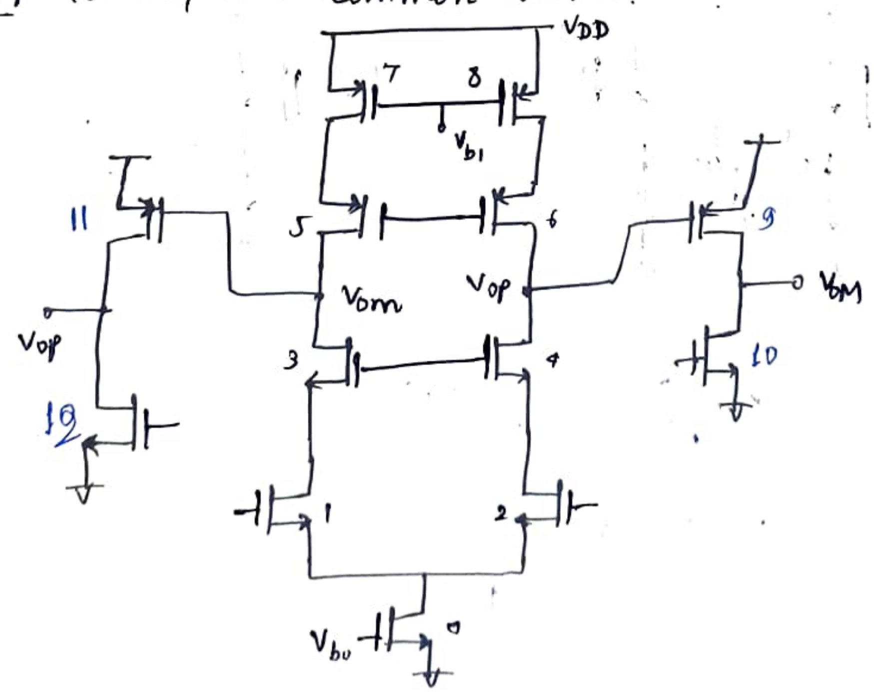


(works only if o/p swings are limited)

$$V_{O,CM}\uparrow \rightarrow V_{SG9,10}\downarrow \rightarrow (R_{on9} \| R_{on10})\uparrow$$
$$\downarrow$$
$$V_{DD'}\downarrow$$
$$\downarrow$$
$$I_P\downarrow$$

Limitation: Limited o/p swing.

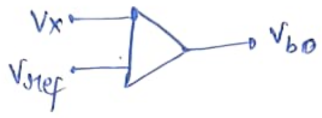
Two stages: Telescopic + Common Source.

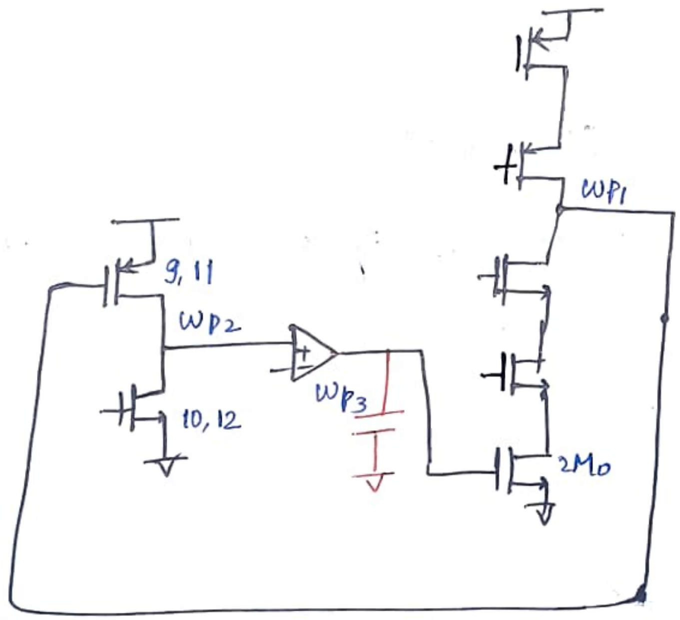


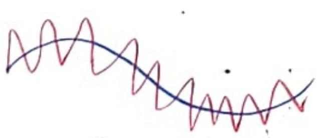
CMFB:

① CMFB for 1st stage + CMFB for 2nd stage. [Preferred]

② CMFB → same o/p CM @ 2nd stage o/p
and correct 1st stage bias.







DC instability : ↔ Diff.-wise good
→ CM-wise bad.

↳ Soln: Use large capacitor

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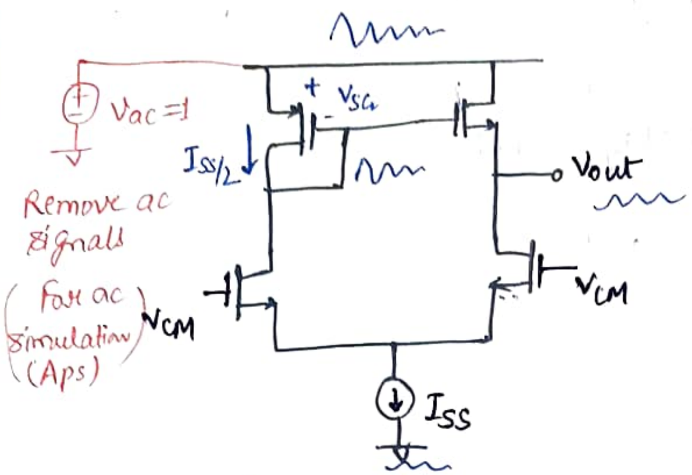
PSRR



[Noise from power supply appears on the output side]

$A_{ps} \approx 1$

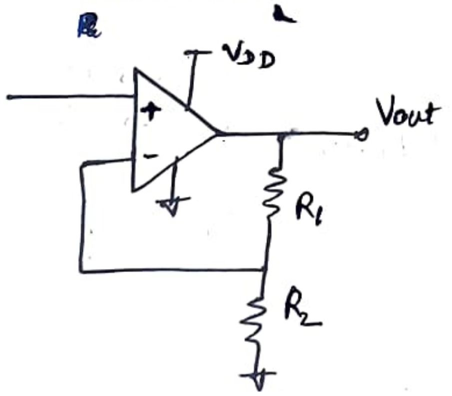
$$PSRR^+ = \frac{A_{dm}}{A_{ps}}$$ (from VDD)

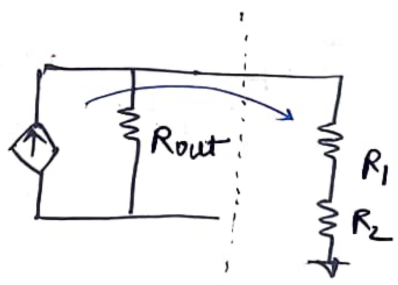
– Mainly for single-ended i/p ; very high ~~PSRR~~ for fully differential signals.

OTA : $R_{out} \rightarrow$ very high

Ideal opamp :

$R_{out} \sim 0$



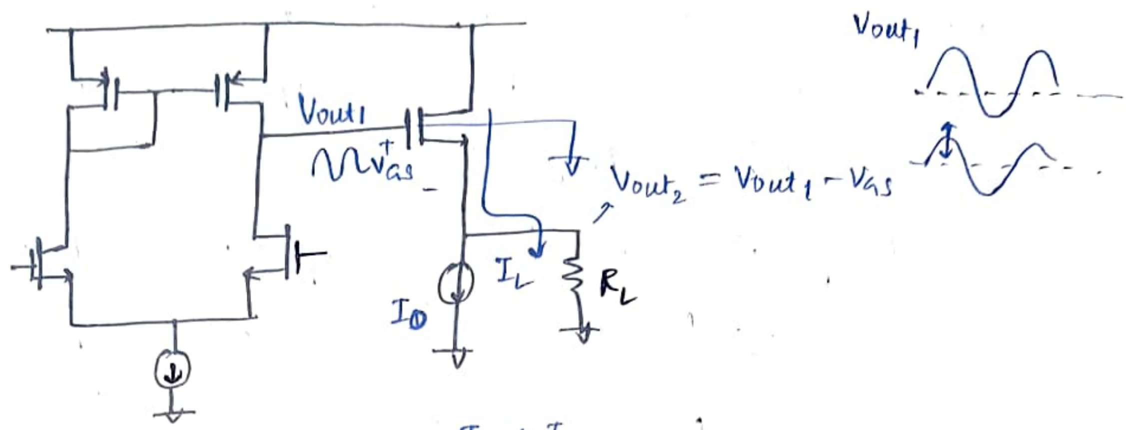


$\Rightarrow$ cannot support resistive load; capacitive load is fine.

↳ Connect an o/p stage.

Output stages:

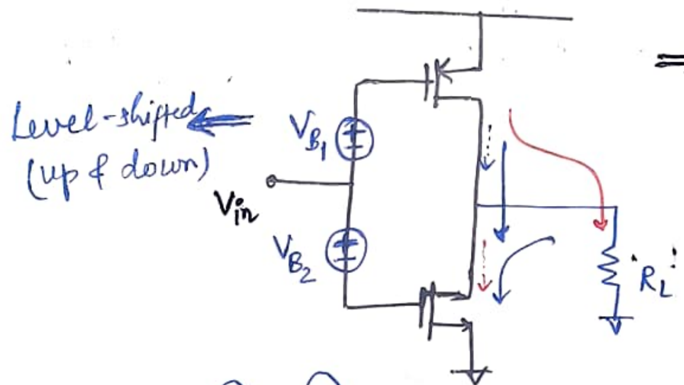
① Common Drain (CD) : Class A driver amplifier



$I_L \leq I_D$

$V_{out_2 max} = V_{out_1} - V_{GS}$

② Class AB output stages [Push-pull amplifier]

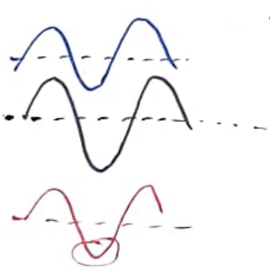


⇒ Inverter (in saturation)

← has to be operated exactly here

↳ Level-shift

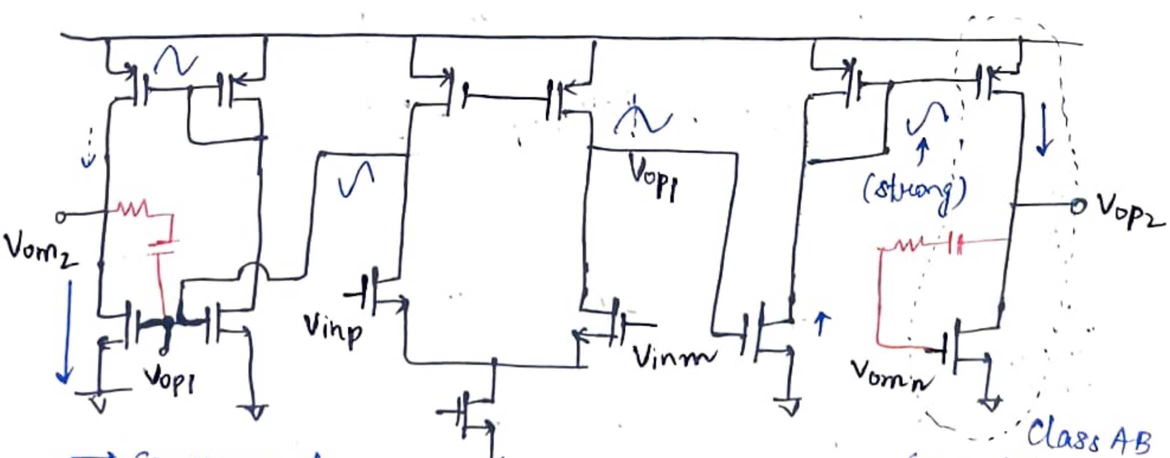
Both has to be ON ⇒ ↑ power



Higher voltage ⇒ NMOS already ON; PMOS near cutoff (NMOS consume more current)

Lower voltage ⇒ PMOS consumes more current

One scheme:



→ Consumes less current
↳ direct current to o/p

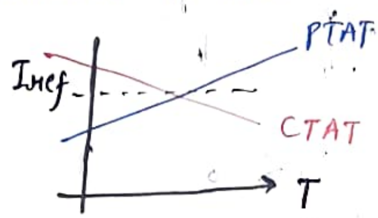
Class AB (CS with active load stage)

Reference Generation :

↳ Voltage generation (eg., for ADC, DAC) / current generation

1. ↳ Has to be constant across temp., process variation, power supply variation

2. Proportional to Absolute Temperature (PTAT)

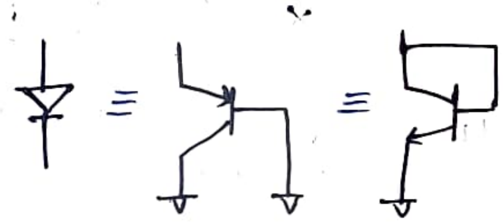


→ With temp., gain may change
↳ adjust ref. accordingly

3. Complementary to Absolute Temperature (CTAT)
→ decrease with temp. (to get non-linearity, etc.)

→ ZTC → Zero Temperature Coefficient current.

→ $\alpha_1 I_{ZTC} + \alpha_2 I_{PTAT}$ → to get current of any slope



Diode : Highly sensitive to temp. (used as temp. sensor)

$$I_D = I_S \exp\left(\frac{V_D}{V_T}\right),$$

where $V_T = \frac{KT}{q}$

$$T\uparrow \Rightarrow V_T \downarrow \text{ but } I_S \Uparrow \Rightarrow I_D \uparrow$$

$$I_S = bT^{4+m} \exp\left(\frac{-E_g}{KT}\right)$$

$$\frac{\partial V_{BE}}{\partial T} \approx -1.5 \text{ mV/K}$$

↳ temp.-dependent voltage with constant slope.
↳ negative temp.-coefficient.

No device with ZTC

↳ Use two with opposite coefficients.

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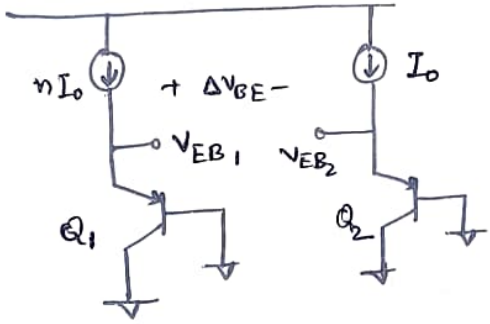
$V_{BE} \longrightarrow$ CTAT $(\sim -1.5\ mV/K)$



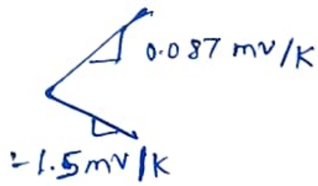
$$I_c = I_s \exp\left(\frac{V_{EB}}{V_T}\right)$$

$$V_{EB_1} = V_T \ln\left(\frac{nI_0}{I_s}\right)$$

$$V_{EB_2} = V_T \ln\left(\frac{I_0}{I_s}\right)$$

$$\Delta V_{EB} = V_T \ln(n) = \frac{KT}{q}\ln(n) \longrightarrow \text{PTAT}$$

$$\left[\frac{K}{q} \sim 0.087\ mV/K\right]$$



$$V_{ref} = \alpha_1 V_{BE} + \alpha_2 (\Delta V_{BE})$$

$$= \underbrace{\alpha_1 V_{BE}}_{-1.5mV/K} + \alpha_2 \frac{KT}{q}\ln(n)$$

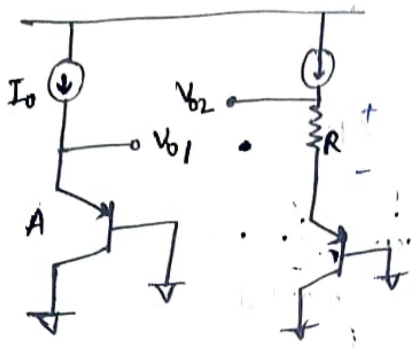
V_{ref}
$\doteq 0.8 + 17.2\ V_T$
$\approx 1.25\ V$
(Bandgap)

$\alpha_1 = 1$

$\alpha_2 \ln(n) = 17.2$

$\alpha_2 \ln(n) \times 0.087\ mV/K = +1.5\ mV/K$

How to add ?



$V_{01} = V_{EB_1}$

$V_{02} = V_{EB_2} + IR$

If $V_{01} = V_{02}$

$\Rightarrow V_{EB_1} = V_{EB_2} + IR$

$\Rightarrow IR = V_{EB_1} - V_{EB_2}$

$\Rightarrow IR = \Delta V_{BE}$

$\therefore V_{02} = V_{EB_2} + \Delta V_{BE}$

$\alpha_2 \ln(n) = 17.2$ $[\alpha_1 = 1, \alpha_2 = 1]$

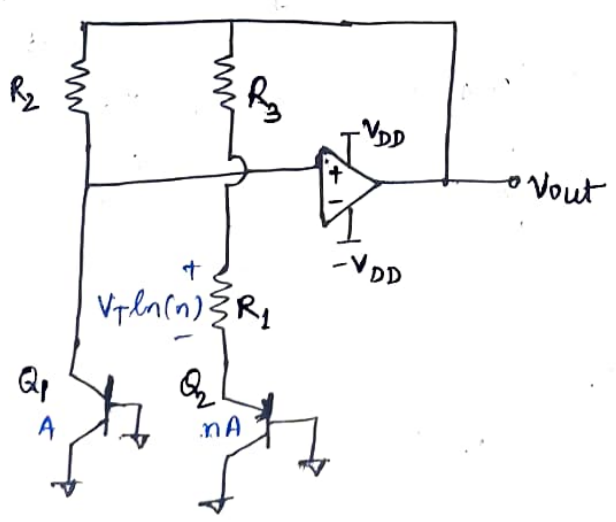
$\alpha_2 = 1 \Rightarrow \ln(n) = 17.2$

$\Rightarrow n = e^{17.2}$ → very large

↳ Practically not implementable

Conditions: ① $V_{01} = V_{02}$

② 'n' should become implementable.



$$V_{out} = V_{EB_2} + \frac{V_T \ln(n)}{R_1}(R_3 + R_1)$$

$$= \underbrace{V_{EB_2}}_{NTC} + \underbrace{V_T \left[\ln(n)\left(1 + \frac{R_3}{R_1}\right)\right]}_{PTC}$$

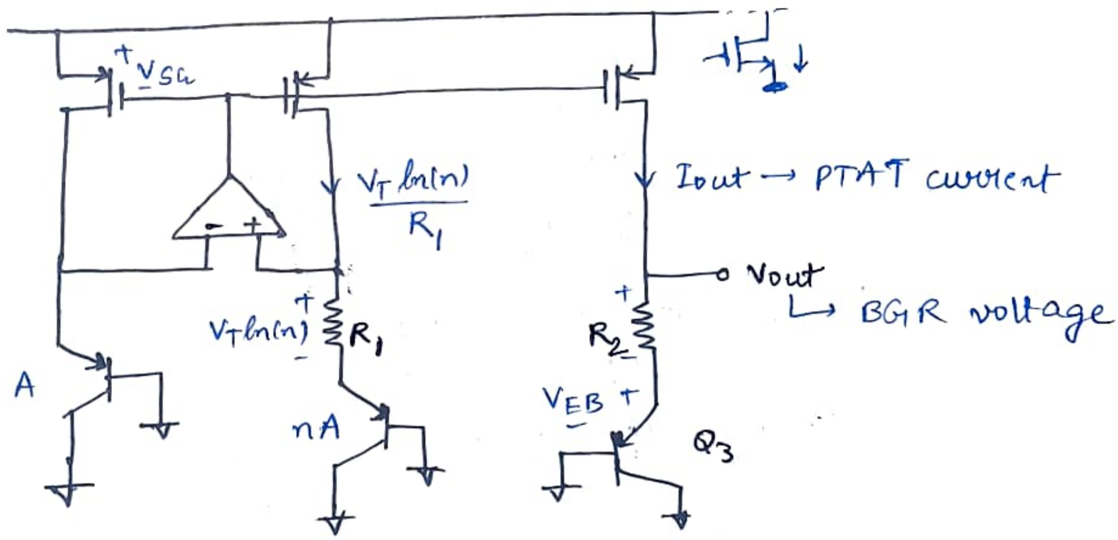
So, to make $V_{out} \longrightarrow ZTC$

$$\left(1 + \frac{R_3}{R_1}\right)\ln(n) = 17.2$$

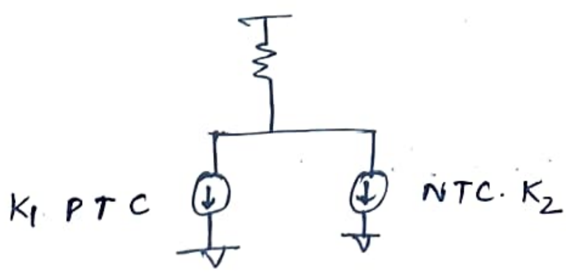
Let $n = 31$, then $\frac{R_3}{R_1} = 4$.

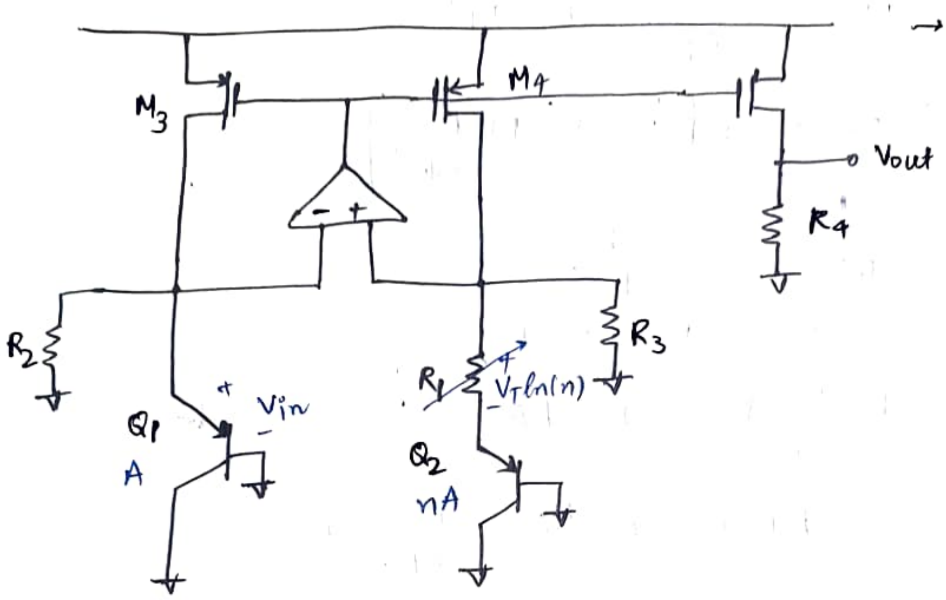
$$V_{ref} = \frac{E_g}{q} + (4+m)V_T$$ — Band gap references (BGR)

PTAT source :



Also, we may add PTC and NTC current.





→ Banber circuit

$$I_{d_3} = I_{c_1} + \frac{V_{EB_1}}{R_2}$$

$$I_{d_4} = I_{c_2} + \frac{V_{EB_1}}{R_3}$$

$$I_{d_3} = I_{d_4}$$

If $R_2 = R_3 \Rightarrow I_{c_1} = I_{c_2}$

$$\Rightarrow V_{EB_1} = V_{EB_2} + I_{c_2} R_1$$

$$\Rightarrow I_{c_2} R_1 = V_T \ln(n)$$

$$\therefore I_{d_4} = \frac{V_T \ln(n)}{R_1} + \frac{V_{EB_1}}{R_3}$$

$$V_{out} = R_4 \left(\frac{V_T \ln(n)}{R_1} + \frac{V_{EB_1}}{R_3} \right)$$

$$= \frac{R_4}{R_3} \left(\frac{R_3}{R_1} V_T \ln(n) + V_{EB_1} \right)$$

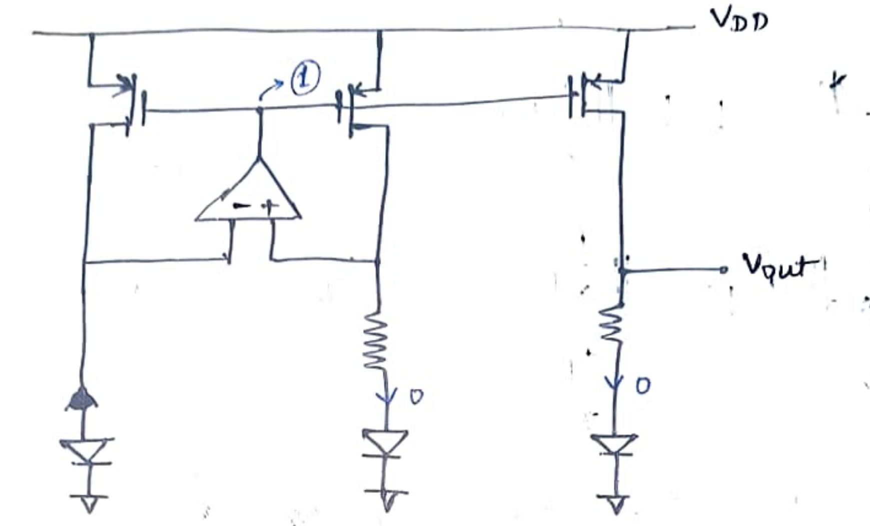
can control voltage (R_4) here — $\frac{R_4}{R_3}$

$V_T \ln(n)$ ↓ PTC

V_{EB_1} ↓ NTC

$$\frac{R_4}{R_3} \ln(n) V_T = 17.2 \, V_T$$

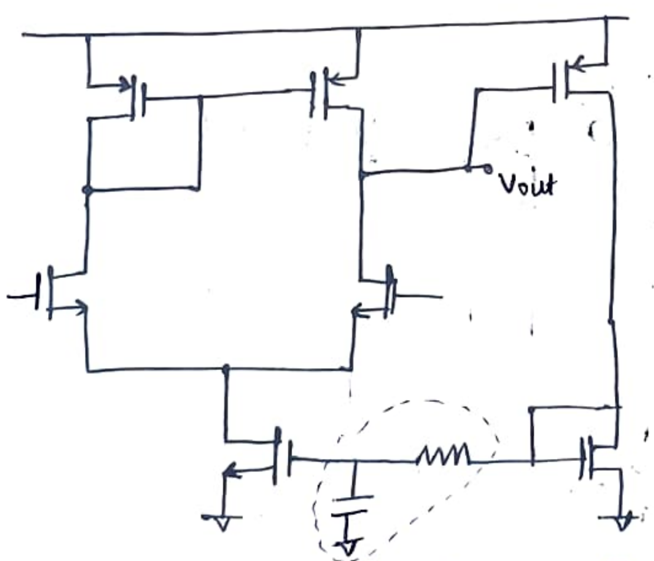
Startup Problem :



If node ① reaches V_{DD}, it will stop the complete circuit and even opamp won't be able to correct the loop.

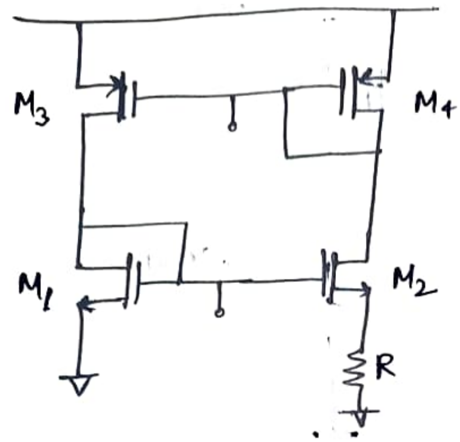
↳ Put a switch at ① to pull down it to gnd for a moment then opamp will take care of it.

Self-Biased 5-OTA



↳ Prevents the circuit from oscillation (to slow down)

Constant gm-biasing :



$V_{GS_1} = V_{GS_2} + I_D R$

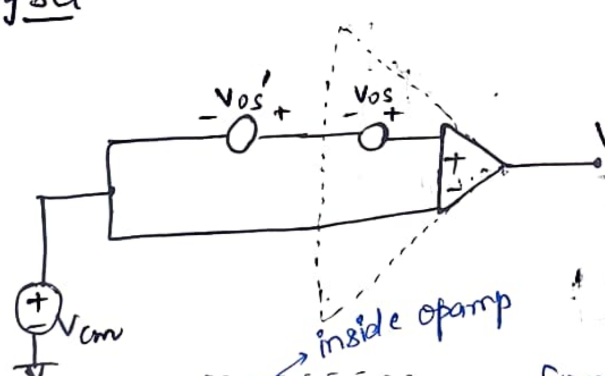
$\left(\frac{W}{L}\right)_2 = K\left(\frac{W}{L}\right)_N$

$$I_D = \frac{\mu_n C_{ox}}{2} K\left(\frac{W}{L}\right)_N \left(V_G - I_D R - V_{th}\right)^2$$

$$= \frac{2}{\mu_n C_{ox}\left(\frac{W}{L}\right)_N} \frac{1}{R^2}\left(1 - \frac{1}{\sqrt{K}}\right)^2$$

$\therefore \; g_m = \frac{2}{R}\left(1 - \frac{1}{\sqrt{K}}\right) \rightarrow g_m$ controlled by R.

Offset

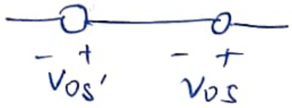


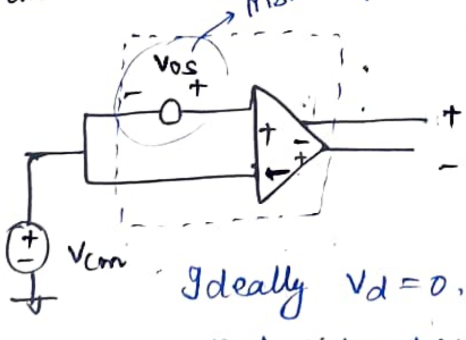
$V_{out} = A V_{os}$

$V_{os}' = -V_{os}$

↳ At this, $V_{out} = 0$

Compensate



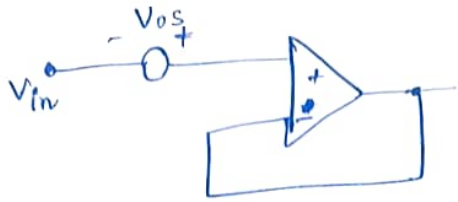


$+ \; V_d \neq 0 \; -$
$= A V_{os}$

Ideally $V_d = 0$, if V_{cm} is applied to both.

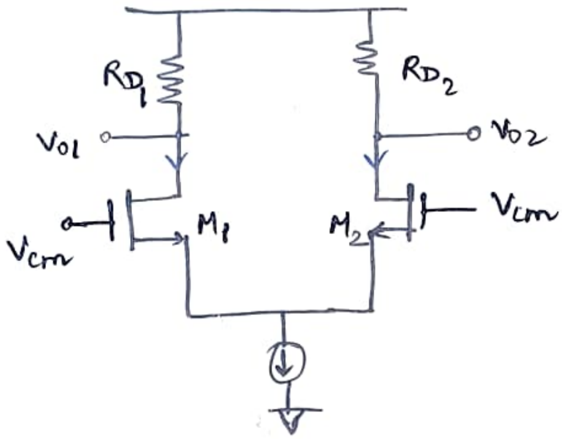
But $V_d = A V_{os}$

— Offset is usually b/c of random mismatch during fabrication.



$$V_{out} = \frac{A}{1+A} V_{in}$$

$$V_{out}' = \frac{A}{1+A} (V_{in} + V_{os})$$



If $g_{m1} \neq g_{m2}$

$R_{D1} \neq R_{D2}$

$\Rightarrow I_{D1} \neq I_{D2}$,

$V_{o1} \neq V_{o2}$

↳ Offset

To make $V_d = 0$

$\Rightarrow V_{o1} = V_{o2}$

$\Rightarrow V_{DD} - I_{D1} R_{D1} = V_{DD} - I_{D1} R_{D2}$

$\Rightarrow I_{D1} R_{D1} = I_{D2} R_{D2}$

↳ Apply differential signals

$$\sigma_{V_{th}} = \frac{A}{\sqrt{WL}}$$

Offset Variation: