

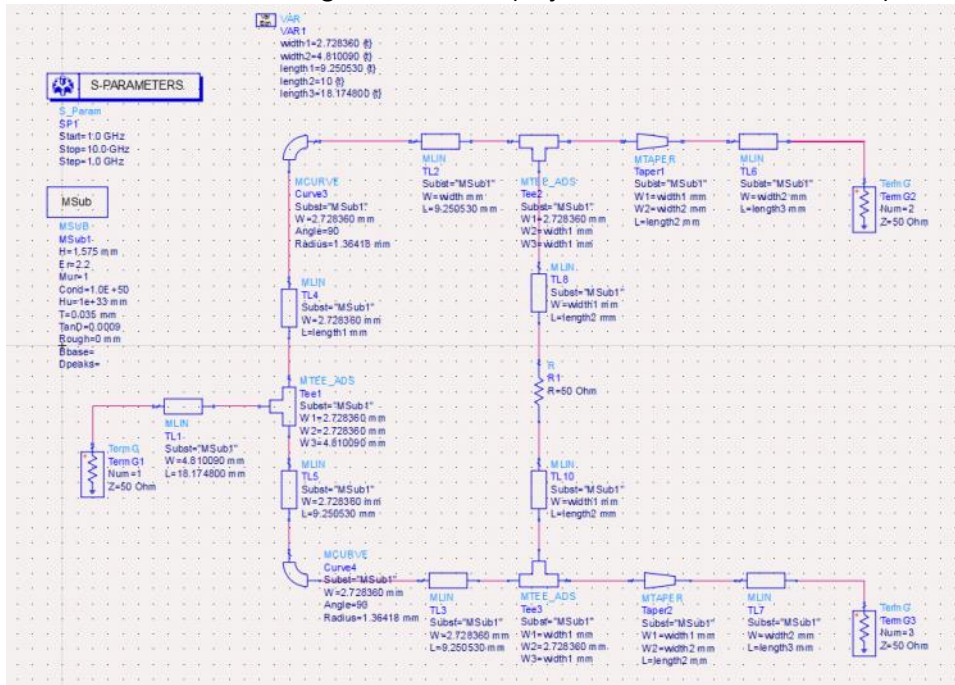
# RF and Microwave (ADS) Lab 3 Report

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(SC22B146)

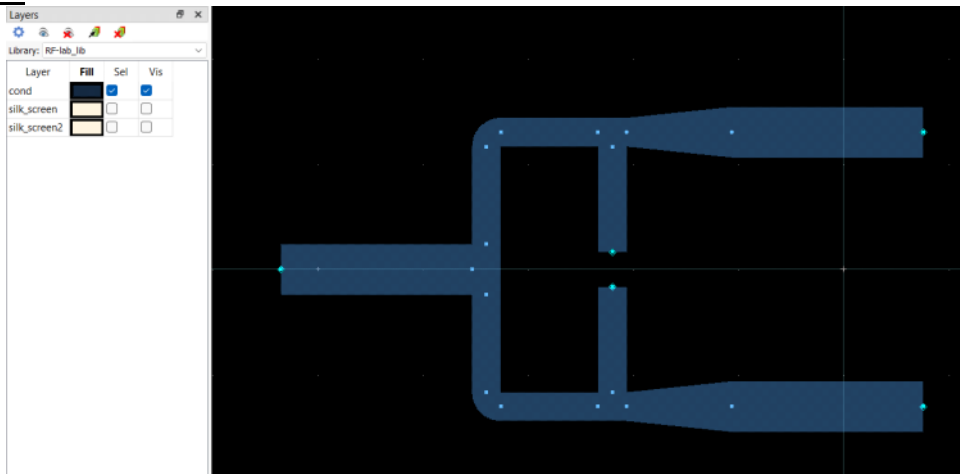
## 1. Design a 1:2 Wilkinson Equal Power Divider using Microstrip line. (The operating frequency is also 5 GHz).

### Schematic:

Design the power divider with the help of MLIN, MCURVE and MTEE components, with their lengths and widths calculated using **LineCalc** tool. (Adjacent dimensions are same)

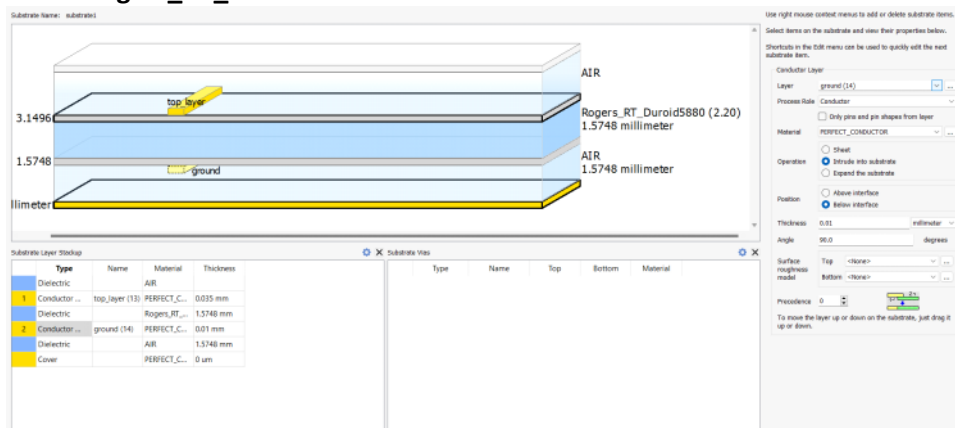


### Layout:

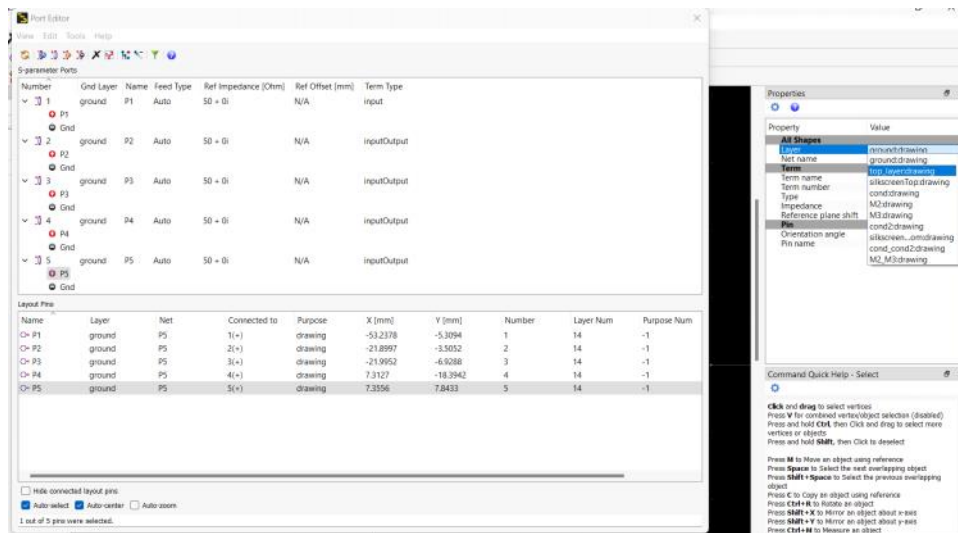


### Substrate Editor:

Select **Rogers\_RT\_Duroid5880** material with thickness 1.5748 mm for the substrate.



### Port Editor:

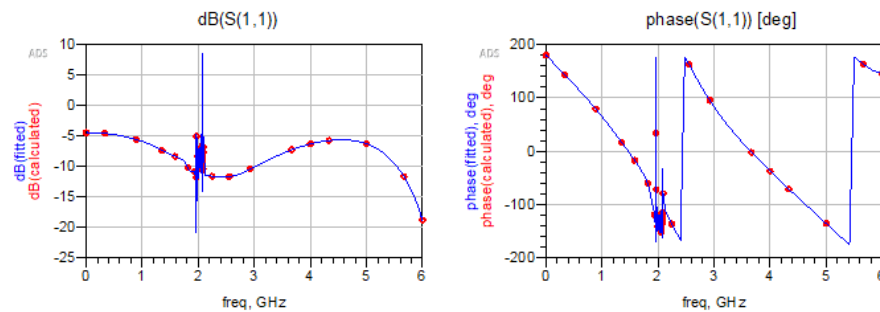


## Simulation:

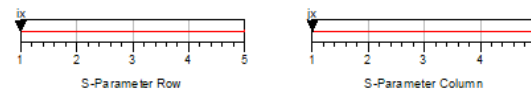
Set frequency 0 to 6 GHz and Mesh density (Cells/Wavelength) = 40.

## Mag/Phase of S(1,1)

Adaptively Fitted Points Discrete Frequency Points

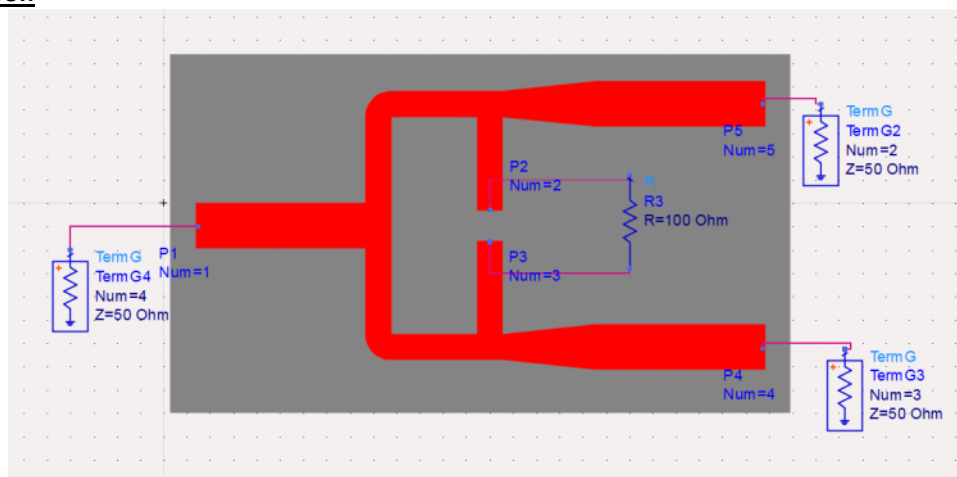


Select markers and use arrow keys to plot S(i,j,x)

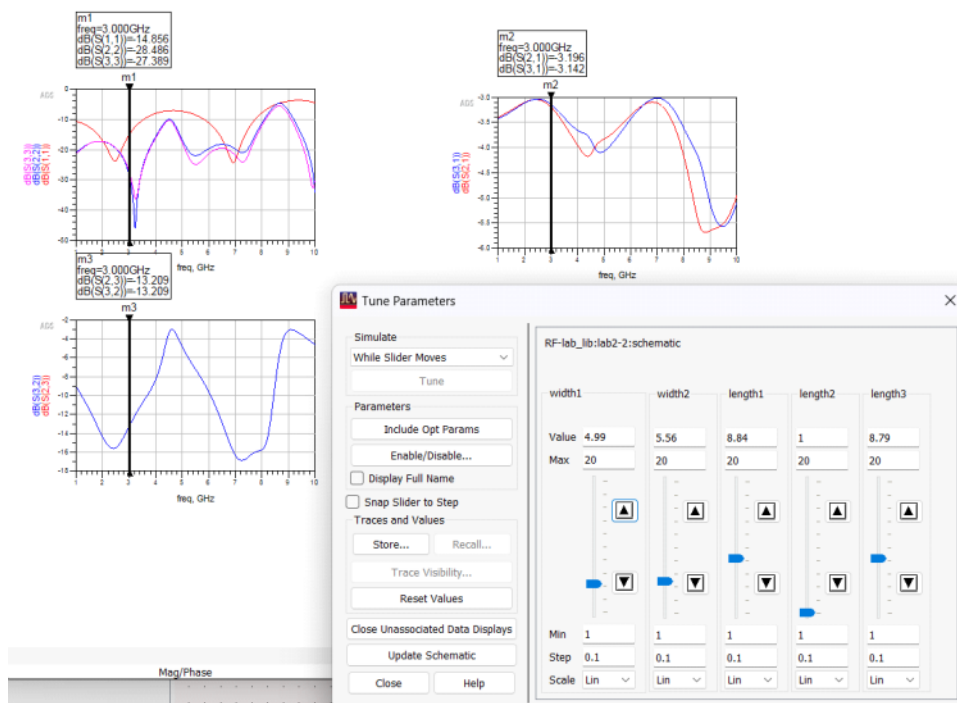


Dataset: lab2\_2\_MomUW\_a - Nov 12, 2024

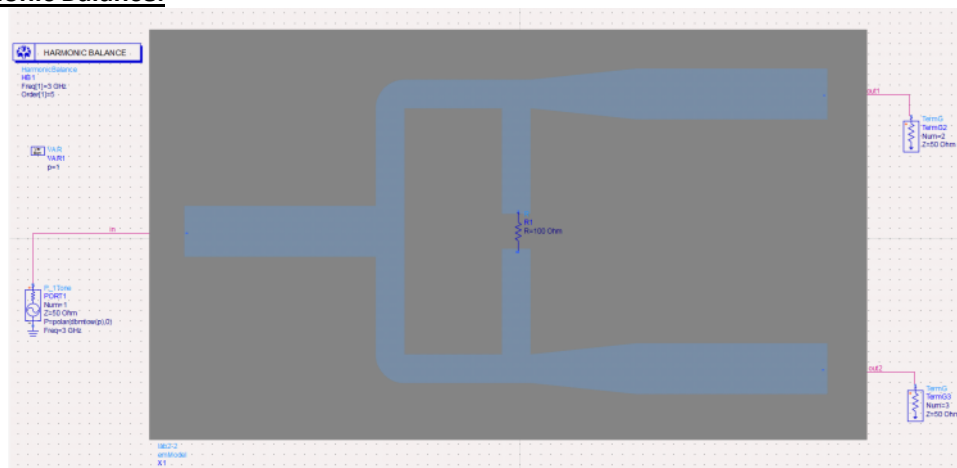
## Symbol:



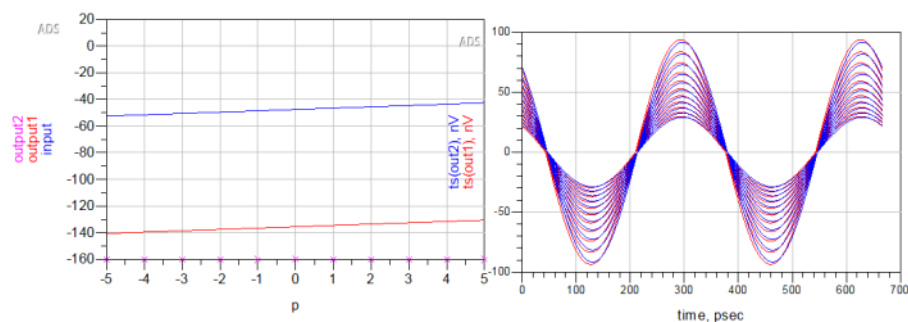
## Tuning:



### Harmonic Balance:



```
Eqn input=dBm(in[:,1])
Eqn output1=dBm(out1[:,1])
Eqn output2=dBm(out2[:,2])
```



### Results:

S11 = -14.856 dB, S22 = -28.486 dB, S33 = -27.389 dB

S21 = -3.196 dB, S31 = -3.142 dB

Ideally S21 and S31 should be -3 dB. Non-ideality is due to loss at the curve, effective length of the quarter wavelength is more than what is required at 3 GHz and due to the length of output port.