VLSI Signal Processing

AVM867

Assignment I

1. A N -bit signed fixed point integer is in the range $-2^{(N-1)} \leq x \leq 2^{-(N-1)}-1$
   i. What is the most negative number than can b be represented if N=12?
   ii. What is the most positive number that can be represented if N=12?

2. Obtain the dynamic range of fixed point integer format for N=24? Represent it in dB also.

3. A N-bit signed fractional fixed point number is used to represent a number x.

(i) What is the dynamic range of the number x if N=24 bit

(ii) What is the precision for a signed fractional fixed point format of N=24 bit?

(iii) If the number of bits is doubled what is the dynamic range and precision – Comment on it

(iv) If the precision is increased by a factor of 8 how much bit need to increased from N bit

3. Determine the IEEE single precision foating point representation of the following numbers:

2, 1000, 23/4, $(23/4) \times 2^{100}$, $(23/4) \times 2^{-100}$

4. How will you represent the following numbers in a. signed magnitude b. one's complement b. two's complement

+0.4375 , -0.4375

5. Perform the following arithmetic using 4 bit two's complement format

0.25-0.625

6. Find the Q.7 representation of the following numbers -0.72

7. Find the Q.15 format and Q8.7 format for the number 0x ABCD

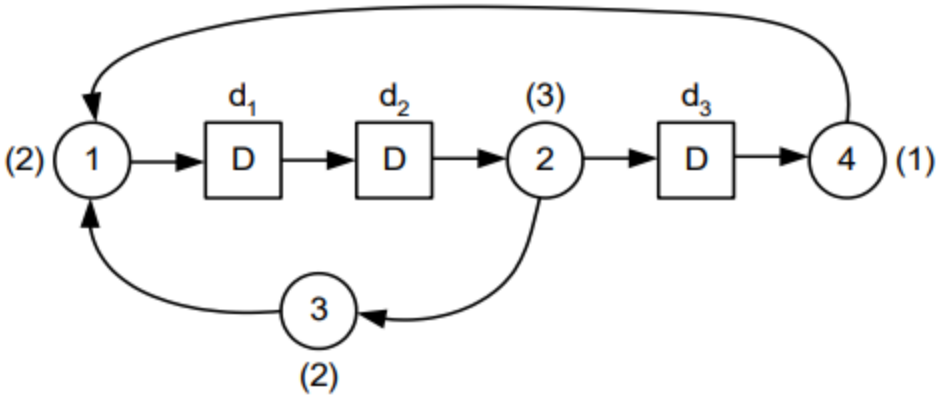
8. Perform binary multiplication of the following numbers in Q.3 format -.5 x 0.875. If the results are stored in Q.6 format. What is the quantization error

9. Find the smallest and largest positive number that can be represented in the IEEE Extended double precision floating point format?

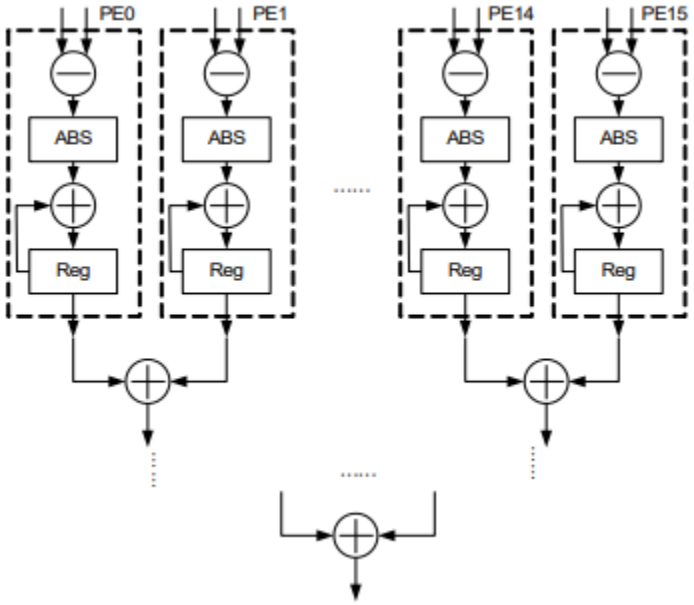
10 Compare a 32 bit fixed point number and floating point number in terms of accuracy, precision and dynamic range?

11. Represent the decimal number 0.7524 56 as Q4 number. What is the error while representing in the given format. What is the most positive, most negative.

12. Compute the iteration using LPM for the following DFG



13. Consider the core of a systolic array motion estimation architecture shown in the following figure. Assume the computation time of subtractor, absolutor, and adder are 5ns, 7ns, and 6ns, respectively. (a) Where is the critical path? What is the maximum working frequency of this circuit? (b) If we want to double the working frequency, please design the associated architecture.



14. Consider a 2D moving average filter for an image, which can be shown as the following equation:

$$y(i,j)=\sum_{m=-1}^{1}\sum_{n=-1}^{1}x(i+m,j+n),$$
$$i,i+m\in[0,W]$$
$$j,j+n\in[0,H]$$

where x(i,j) is the input image, y(i,j) is the filtered image, and W and H are the width and height of the image, respectively draw the dependence Graph.