AV322 – VLSI Technology

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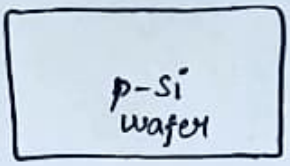
SC22B146

CMOS Fabrication Assignment
Using Twin well Technology

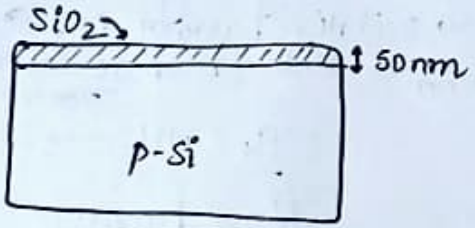
Twin-well Technology: Allows both n-channel MOS (NMOS) and p-channel MOS (PMOS) devices to be fabricated on the same substrate by using both n-well and p-well regions.

Fabrication:

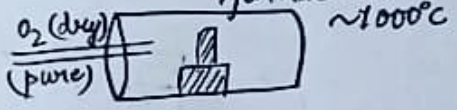
Step-①: Substrate preparation: Take p-type Si wafer.



Step-②: Form SiO_2 layer by dry oxidation



Equipment:



$Si + O_2 \uparrow \xrightarrow{1000^\circ C} SiO_2$ (solid)

[20-30 minutes]

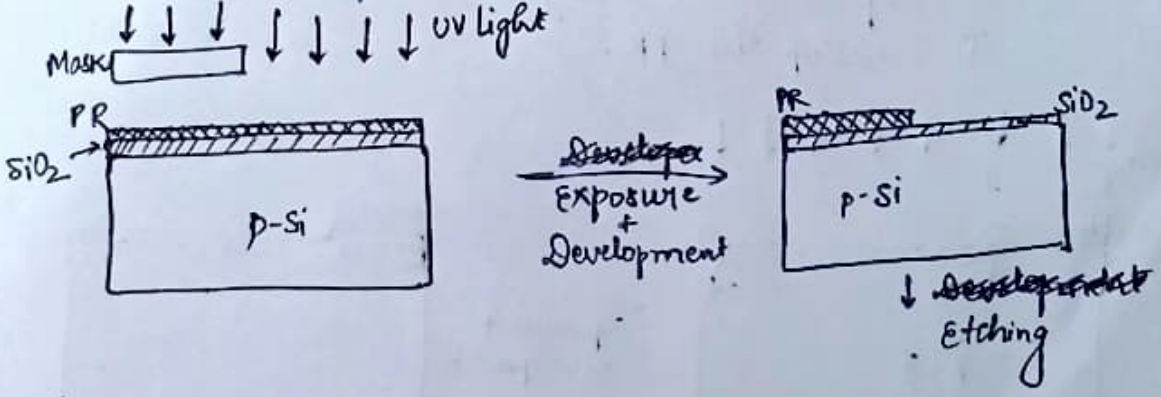
Step-③: Patterning SiO_2 layer

③.① **Photolithography:** ① Apply positive photoresist on SiO_2 and do spin-coating.

② Align the photomask.

③ Expose the photoresist to UV light through the mask.

④ Dissolve exposed PR in developer.



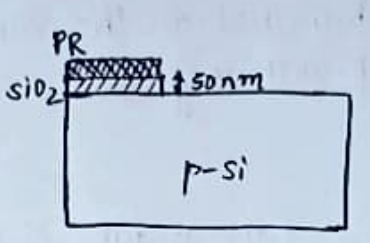
(3.2) Etching: Wet eching using HF → selective etching of SiO_2.

$$CF_4 \xrightarrow[\text{plasma}]{<300^\circ C} CF_3 + F^*$$

$$F^* + H_2 \longrightarrow HF$$

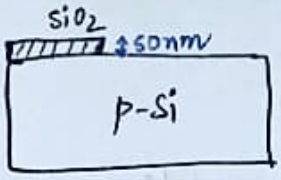
$$HF + SiO_2 \longrightarrow SiF_6^{2-}\uparrow + H_2\uparrow$$

Result:



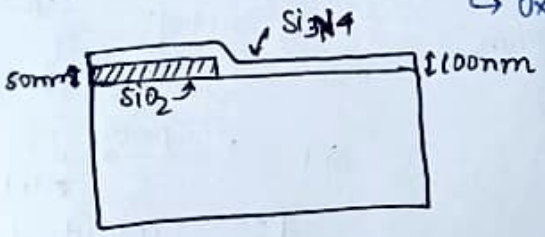
(3.3) Stripping: Remove PR using $H_2SO_4 + H_2O_2$ solution.

Result:



Step ④: Deposit Si_3N_4 layer over SiO_2 using dry oxidation (Hard Mask).

↳ Oxidation barrier to selectively grow oxide elsewhere later



$$SiH_4 + NH_3 \xrightarrow{(700\text{-}800^\circ C)} Si_3N_4 + H_2$$

[Low-Pressure Chemical Vapour Deposition]

Step ⑤: Patterning Si_3N_4 for n-well region.

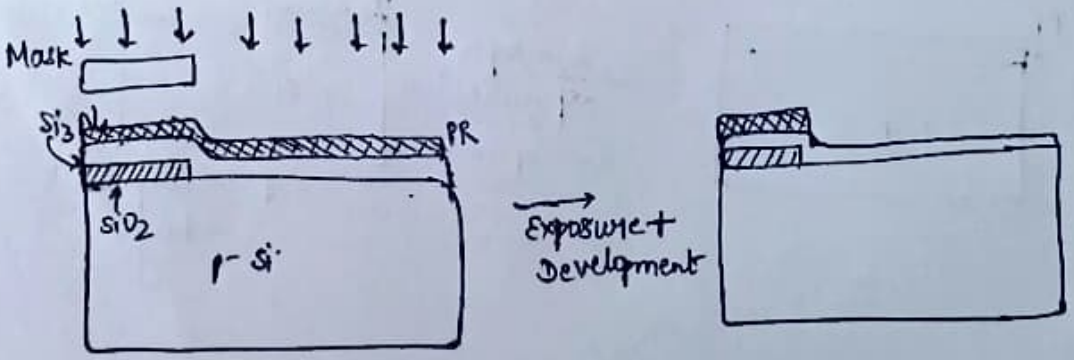
↳ Open windows to implant n-well.

① Photolithography: ⓐ Apply +ve photoresist.

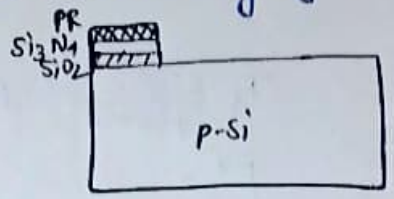
ⓑ Align the photomask.

ⓒ Expose it to UV light.

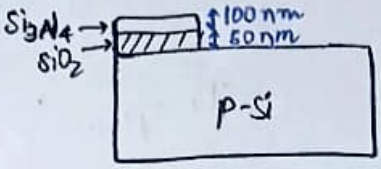
ⓓ Develop the PR.



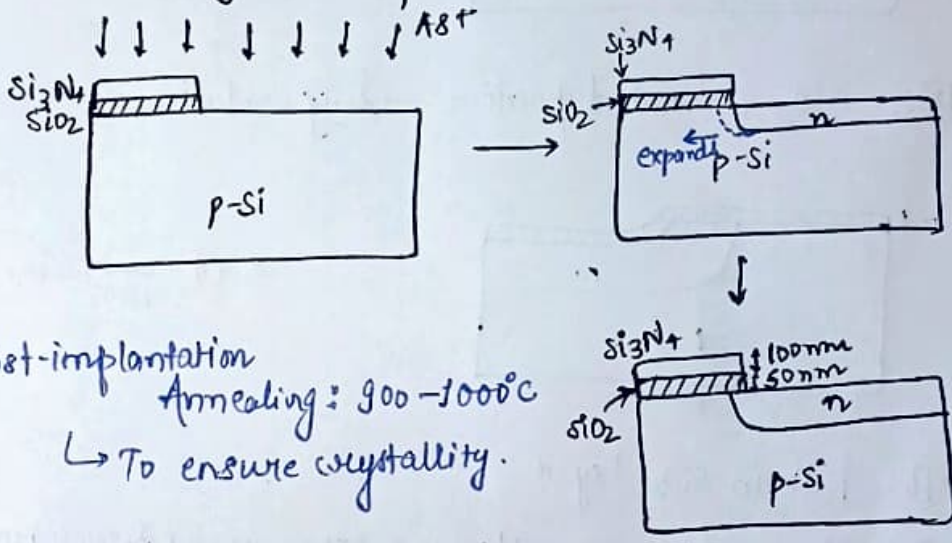
(ii) Etching: Use wet-etching by H_3PO_4 to etch Si_3N_4 selectively.



(iii) Stripping using $H_2SO_4 + H_2O_2$ solution.

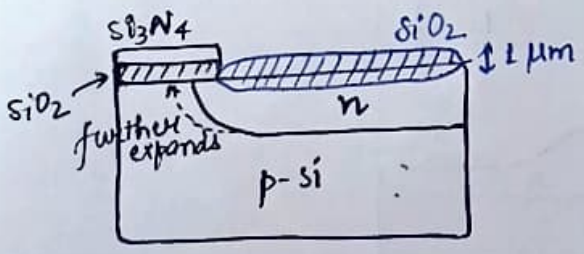


Step-6: Form N-well by Ion implantation.



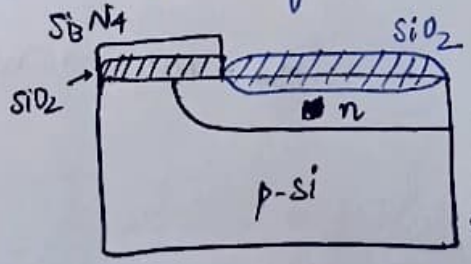
Post-implantation Annealing: 900 – 1000°C
↳ To ensure crystallity.

Step-7: Grow thick oxide by wet-oxidation.

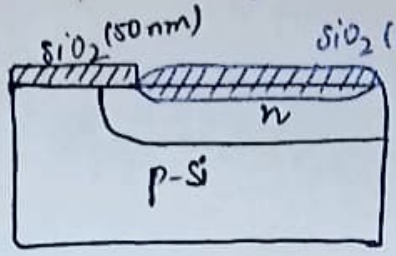


$$Si + H_2O \xrightarrow[1000^\circ C]{wet} SiO_2\ (solid) + H_2\uparrow$$

N-well expands further due to high temperature.



Step-⑧: Si_3N_4 etching → using CF^* recipe

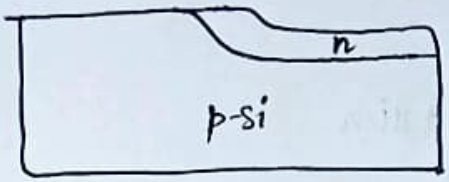


$$CF_4 \xrightarrow[\text{plasma}]{\leq 300^\circ C} CF_3 + F^*$$

$$F^* + Si_3N_4 \longrightarrow N_2\uparrow + SiF_6^{2-}\uparrow$$

Step-⑨: SiO_2 etching (wet)

Result:

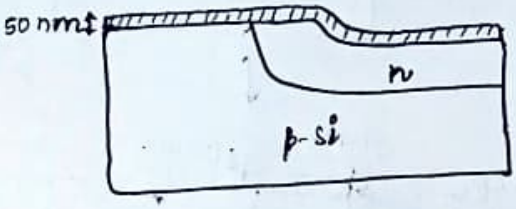


$$CF_4 \xrightarrow[\text{plasma}]{<300^\circ C} CF_3 + F^*$$

$$H_2 + F^* \longrightarrow HF$$

$$HF + SiO_2 \longrightarrow SiF_6^{2-}\uparrow + H_2\uparrow$$

Step-⑩: - SiO_2 (50 nm) deposition → Dry Oxidation



$$Si + O_2 \xrightarrow[1000^\circ C]{} SiO_2$$

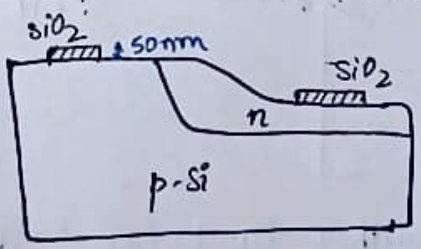
Step-⑪: Pattern SiO_2 layer

Photolithography: PR → Mask → Exposure → Development

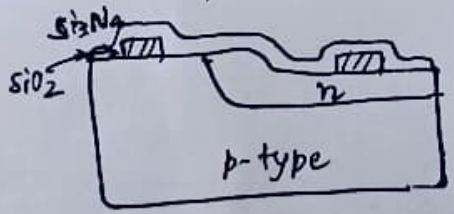
↓ Etching

↓ Stripping

Result:



Step-⑫: Si_3N_4 deposition



$$SiH_4 + NH_3 \longrightarrow Si_3N_4 + H_2$$

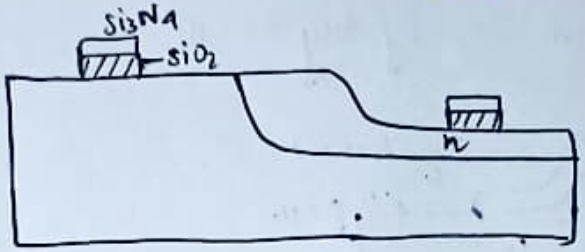
Step-(13): Pattern Si_3N_4 layer

Photolithography : PR → Mask → Exposure → Development
↓ Etching
↓ stripping

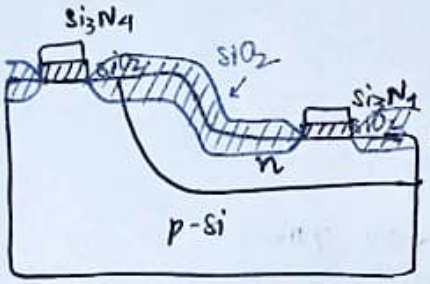
Mask

Mask

Result :



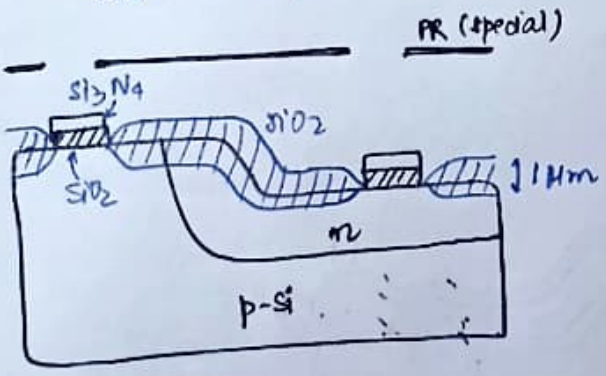
Step-(14): Grow oxide all over by wet oxidation



$$Si + H_2O \xrightarrow[1000^\circ C]{wet} SiO_2 + H_2\uparrow$$

Step-(15): $Si_3N_4 + SiO_2$ etching

Using special photoresist to remove SiO_2 using CF_4 recipe, and F^* recipe to remove Si_3N_4.



Recipe for SiO_2 :

$$CF_4 \xrightarrow[plasma]{<300^\circ C} CF_3 + F^*$$

$$F^* + H_2 \longrightarrow HF$$

$$HF + SiO_2 \longrightarrow SiF_6^{2-}\uparrow + H_2\uparrow$$

Recipe for Si_3N_4 :

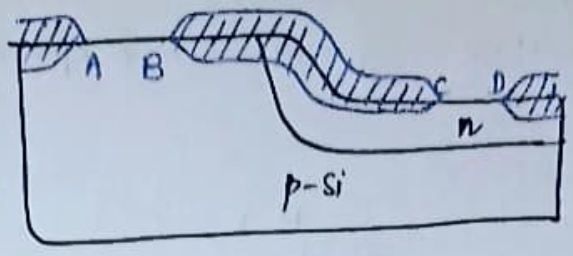
$$CF_4 \xrightarrow[plasma]{<300^\circ C} F^* + CF_3$$

$$F^* + Si_3N_4 \longrightarrow SiF_6^{2-}\uparrow + H_2\uparrow$$

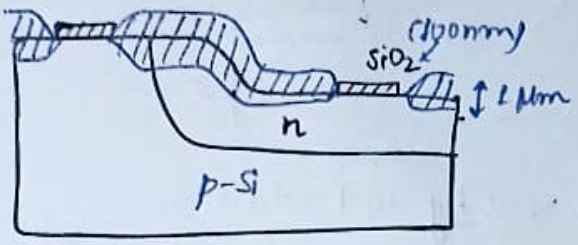
Ashing : $C_xH_y + O_2 \xrightarrow{Ash} CO_2 + H_2$

↳ To save one-sid MOS using photoresist.
↳ No developer or mask required.
↳ Remove PR using acetone.

Result:

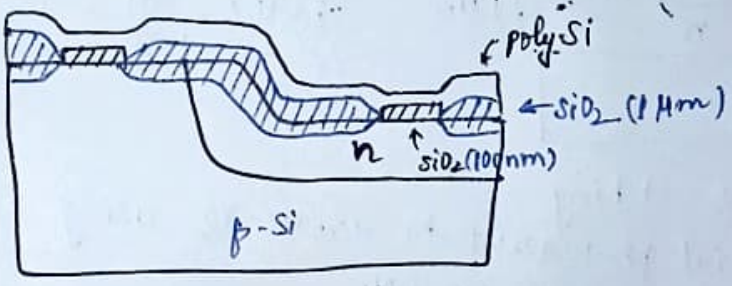


Step-⑯ : Deposit 100nm SiO_2 by dry oxidation



$$Si + O_2 \xrightarrow[1000^\circ C]{dry} SiO_2$$

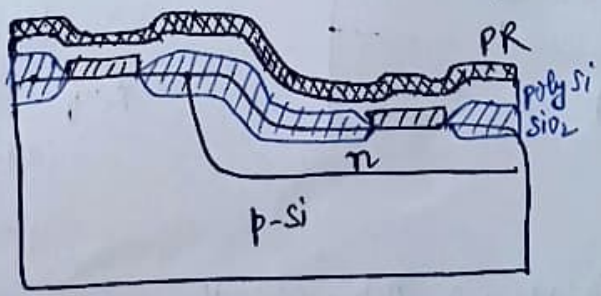
Step-⑰ : Deposit polysilicon



Step-⑱ : Pattern poly Si.

① Photolithography

ⓐ Apply positive PR

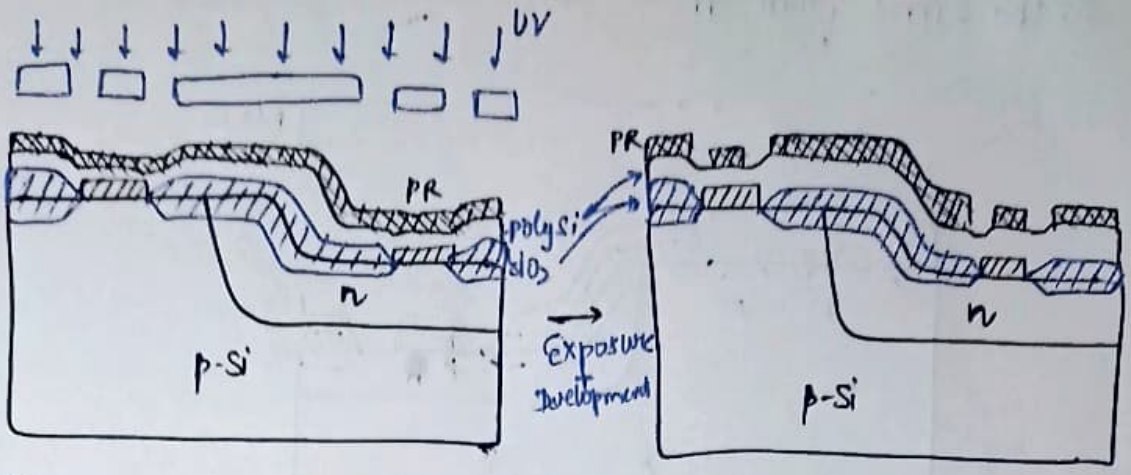


ⓑ Align the photomask

ⓒ Expose it to uv light.

ⓓ Development.

Result:



(ii) Etching

poly Si: $CF_4 \xrightarrow[\text{plasma}]{<300^\circ C} CF_3 + F^*$

$F^* + Si \longrightarrow SiF_6^{2-} \uparrow$

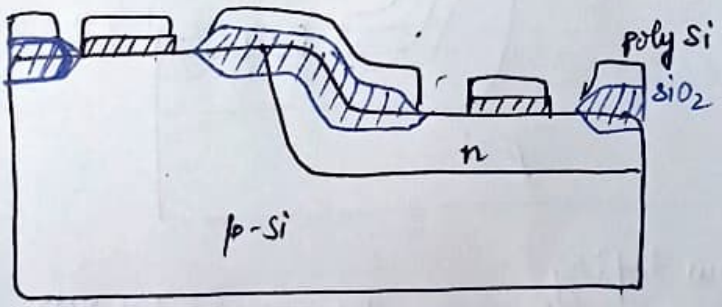
SiO_2: $CF_4 \xrightarrow[\text{plasma}]{<300^\circ C} CF_3 + F^*$

$F^* + H_2 \longrightarrow HF$

$HF + SiO_2 \longrightarrow SiF_6^{2-} \uparrow + H_2 \uparrow$

(iii) Stripping: Use $H_2O_2 + H_2SO_4$ solution to remove the PR.

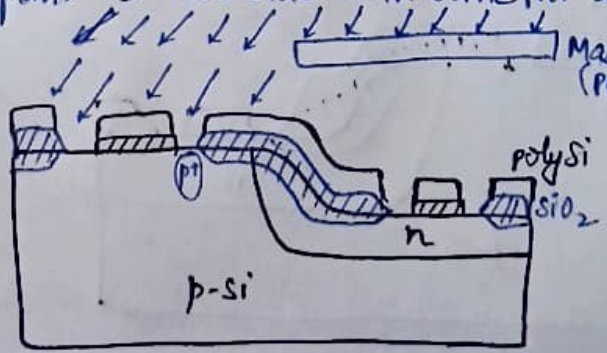
Result:



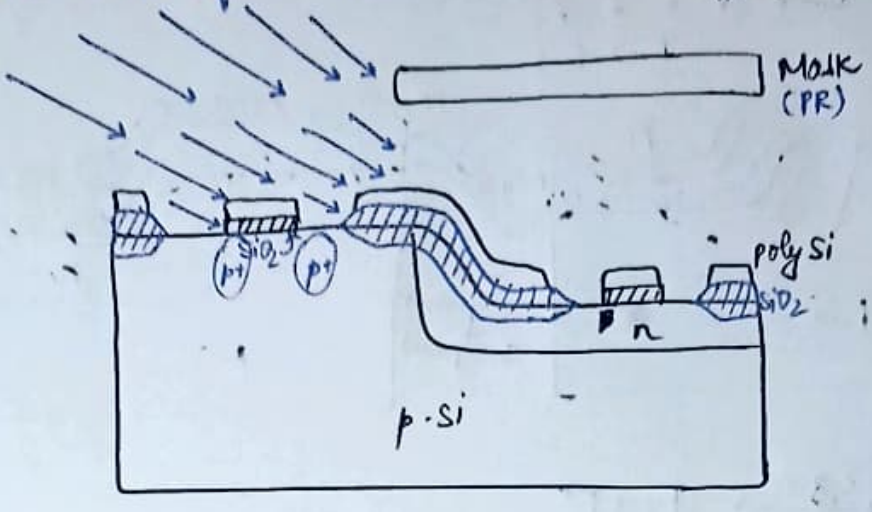
Step-(19): Halo / Tilted Implantation → Using Boron (NMOS side)

↳ Use spin-coat, PR to protect PMOS side. Then expose and develop.

↳ Implant B NMOS side with some tilt angle.



Do the same from opposite direction.....

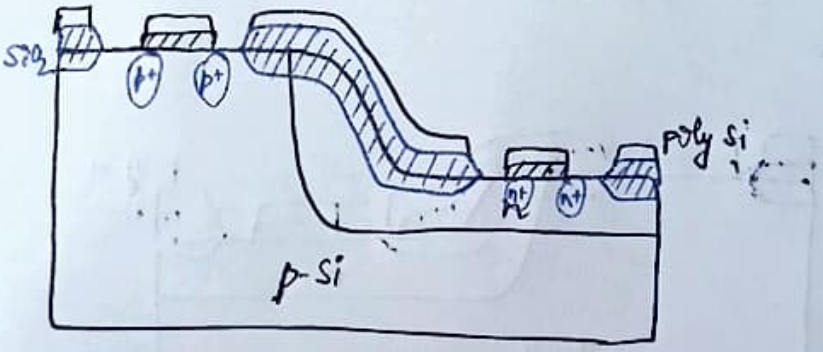


Remove the PR using O_2 plasma ashing.

$$C_xH_y + O_2 \xrightarrow{ash} CO_2 + H_2$$

step-(20): Repeat halo-implantation PMOS side with As.

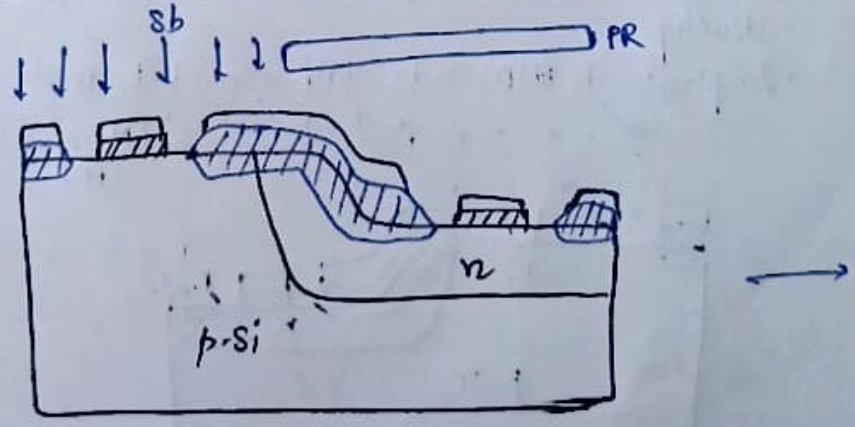
Result:



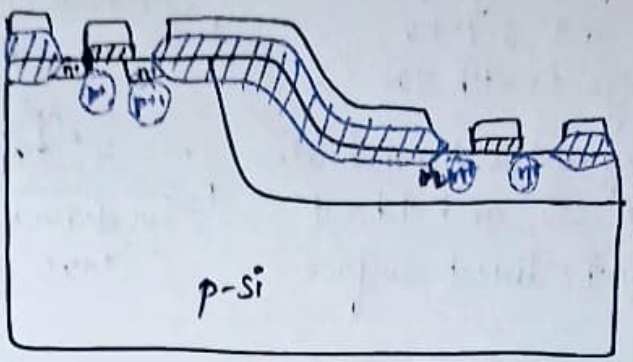
step-(21): Shallow doping

↳ Use very low diffusivity dopants (Sb for NMOS, Ni for PMOS) for very thin film implantation.

↳ Mask the other side PR.



→

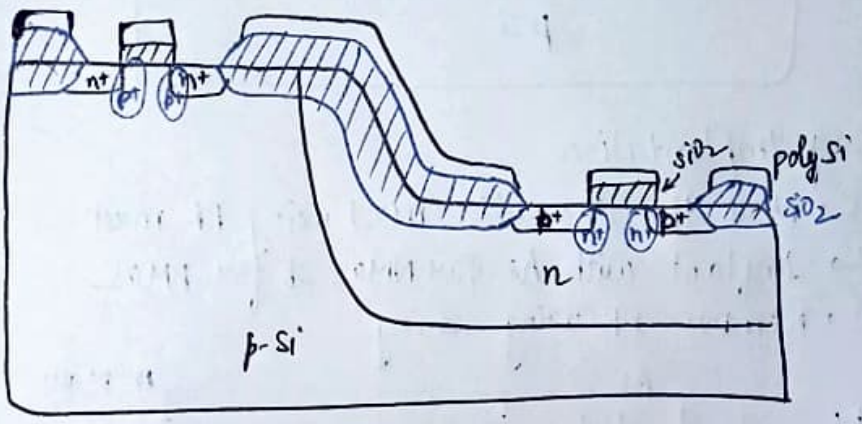


→ Annealing will further make n+ bulgy, so make it thin for now.

Remove the PR mask by ashing.

Repeat the process for PMOS side.

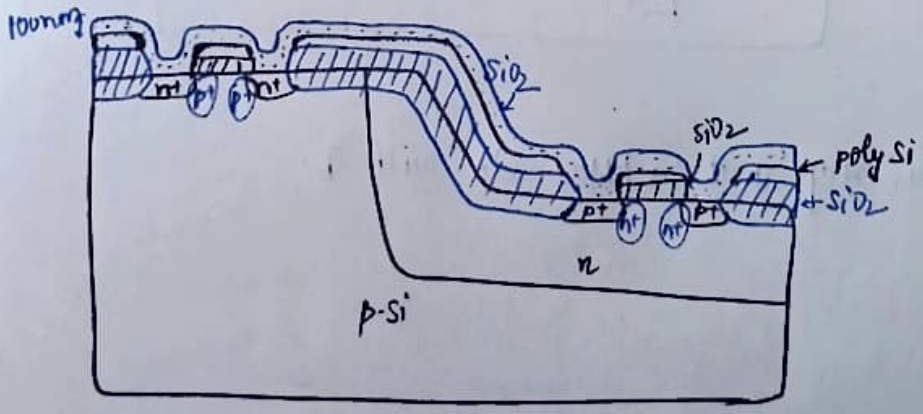
Result:



step-㉒: SiO_2 deposition

$$SiH_4 + O_2 \xrightarrow[\text{plasma}]{200^\circ C} SiO_2 + H_2$$

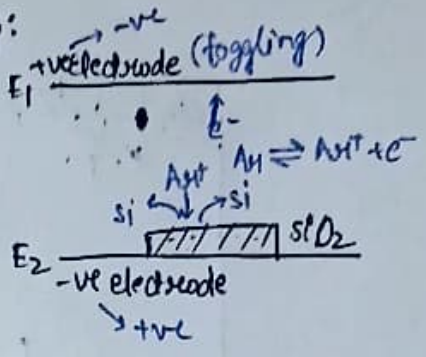
(100nm)



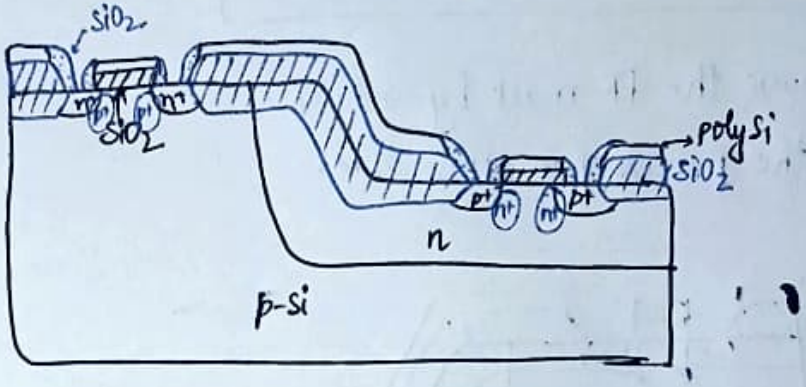
Step (23): Anisotropic Argon Etching

↳ Using 13.56 MHz frequency of changing polarity and 5–10 KV of operating voltage to etch SiO_2 using Ar^+ (heavy nucleus; less mobile), which bombards SiO_2 and etches it.

Setup:



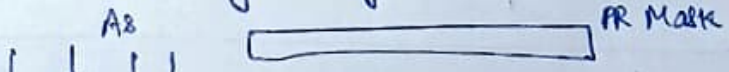
Result: ↳ Etches only the direct surface.

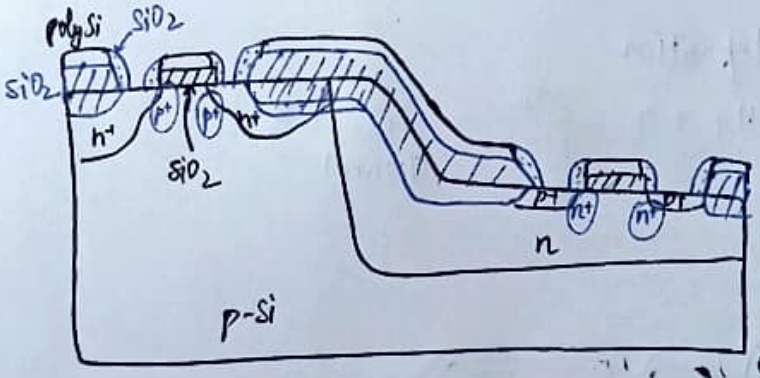


Step-(24): Deep Implantation

↳ Mask the other side (PMOS) using PR mask.
↳ Implant with As for NMOS, Sb for PMOS.
↳ Remove PR using ashing.

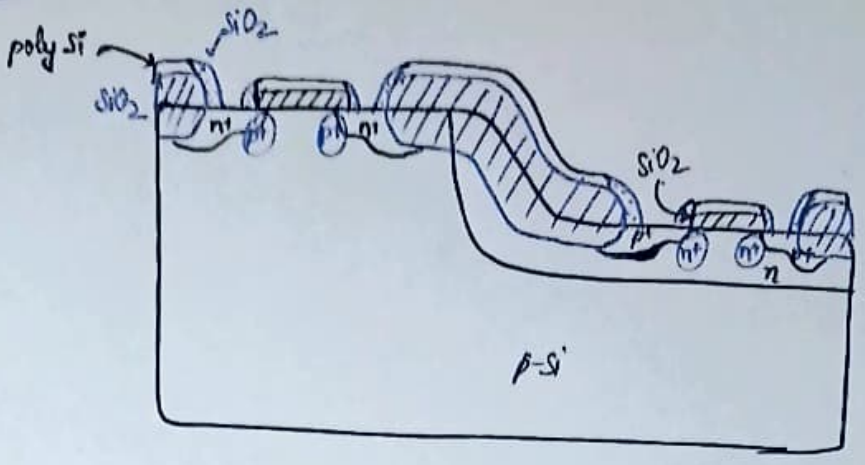
Result:





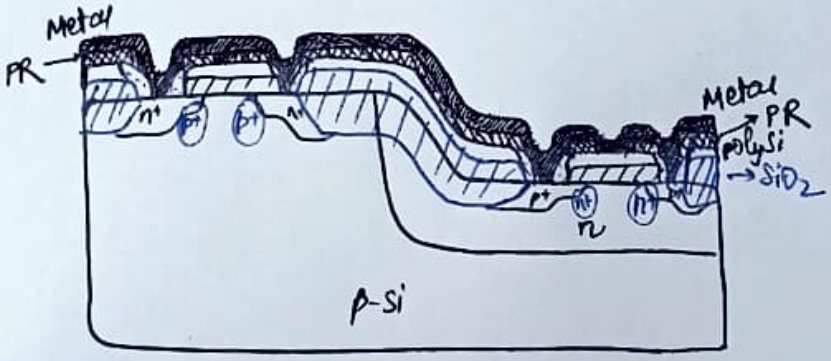
Now, repeat it on PMOS side with Sb.

Result:



Step-(29): Metal Deposition and Liftoff

(i) Spincoat PR everywhere.
(ii) Align photomask
(iii) Expose + Develop to get PR pattern.
(iv) Deposit metal everywhere.
(v) Use ~~acto~~ acetone to remove PR and liftoff the metal on top of it. Metal remains in the region where there was no PR.



Final structure :