

# LAB 3 Pre-Labwork

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SC22B146

## Design of Adders

- ① Logic Circuit to add two 4-bit BCD numbers and with proper correction circuit to get correct BCD output (Addition using carry look ahead adder).

### Implementation:

- 4-bit carry look ahead binary adder for initial addition
- logic circuit to detect sum greater than 9 or a carry.
- one more 4-bit adder to add  $(0110)_2$  or  $6_{10}$  if the sum  $\geq 9$  or carry is 1.

Eg 6 0 1 1 0

+8 1 0 0 0

14 1 1 1 0

+ 0 1 1 0

← Invalid BCD

← Add 6 for correction.

0 0 0 1 0 1 1 0

← BCD for 14

Truth Table:  
(Detecting if sum > 9)

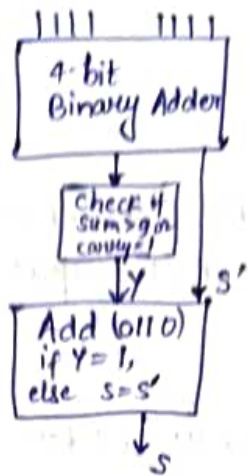
	$S_3$	$S_2$	$S_1$	$S_0$	Output (Y)
0 →	0	0	0	0	0
1 →	0	0	0	1	0
2 →	0	0	1	0	0
3 →	0	0	1	1	0
4 →	0	1	0	0	0
5 →	0	1	0	1	0
6 →	0	1	1	0	0
7 →	0	1	1	1	0
8 →	1	0	0	0	0
9 →	1	0	0	1	0
10 →	1	0	1	0	1
11 →	1	0	1	1	1
12 →	1	1	0	0	1
13 →	1	1	0	1	1
14 →	1	1	1	0	1
15 →	1	1	1	1	1

K-Map:

$S_3 S_2$	$S_1 S_0$	00	01	11	10
00	0	0	0	0	0
01	0	0	0	0	0
11	1	1	1	1	1
10	0	0	1	1	1

Output,  $Y = S_3 S_2 + S_3 S_1$

Sketch:



Circuit diagram:

for  $A = A_3 A_2 A_1 A_0 \text{ Cin}$

$B = B_3 B_2 B_1 B_0$

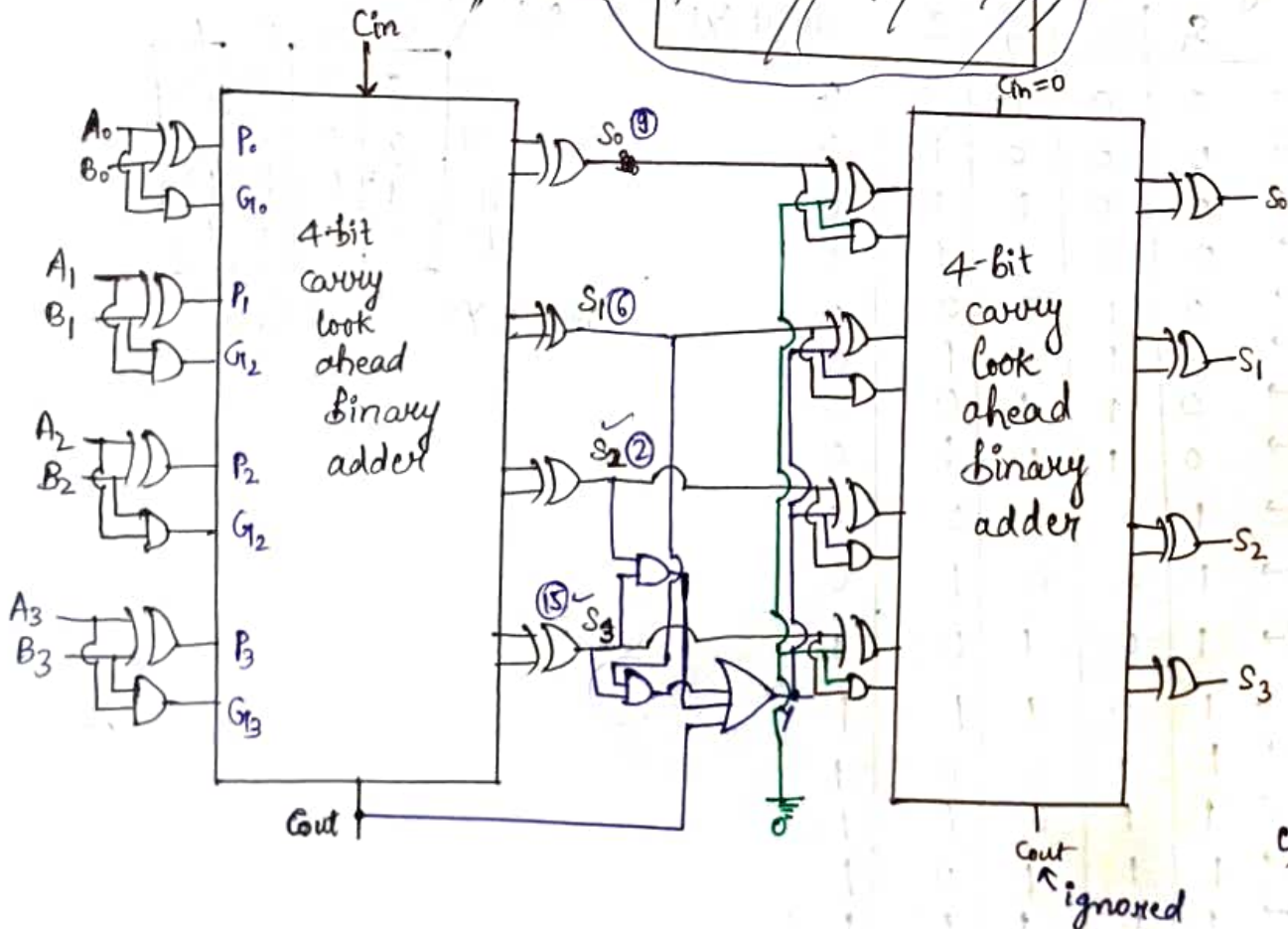
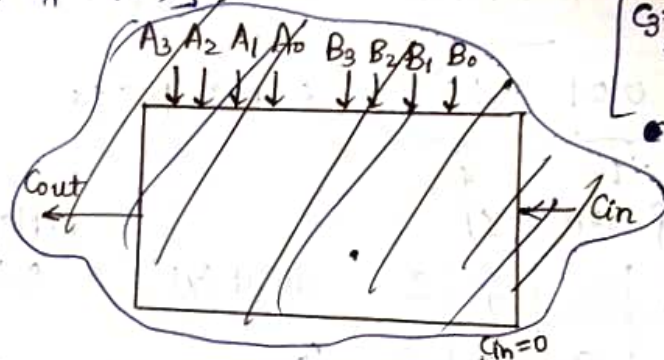
$\text{Sum} = \text{Carry } S_3 S_2 S_1 S_0$

$+ 0110 \leftarrow \text{if Sum} > 9 \text{ or } \text{Carry} = 1$

$S_i = P_i \oplus C_i$   
 $C_{i+1} = G_i + P_i C_i \quad (P_i = A_i \oplus B_i, G_i = A_i B_i)$

$C_1 = G_0 + P_0 C_0$   
 $C_2 = G_1 + P_1 C_1$   
 $= G_1 + P_1 G_0 + P_1 P_0 C_0$

$C_3 = G_2 + P_2 C_2$   
 $= G_2 + P_2 G_1 + P_2 P_1 G_0$   
 $+ P_2 P_1 P_0 G_0$



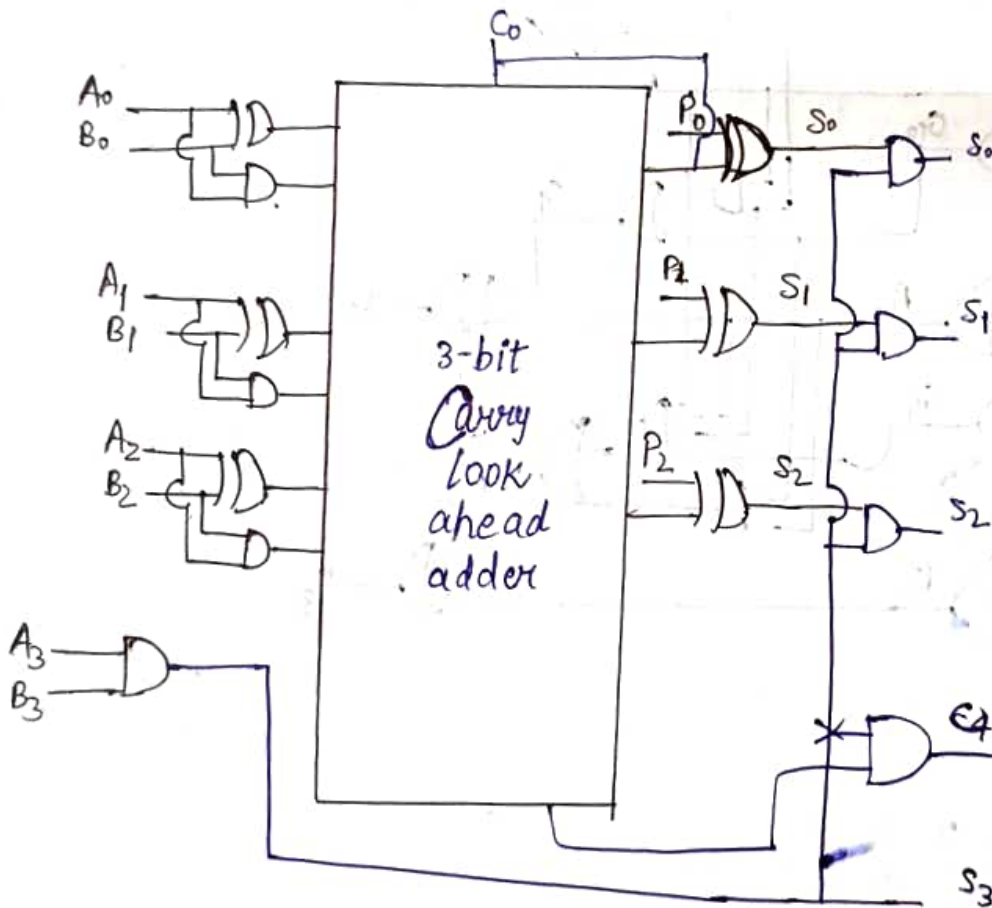
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② 3 bit signed binary adder circuit (4 bits, 1 bit for sign) to add two negative numbers; control logic to predict whether the number is negative or not and based on that do the addition.

Soln:

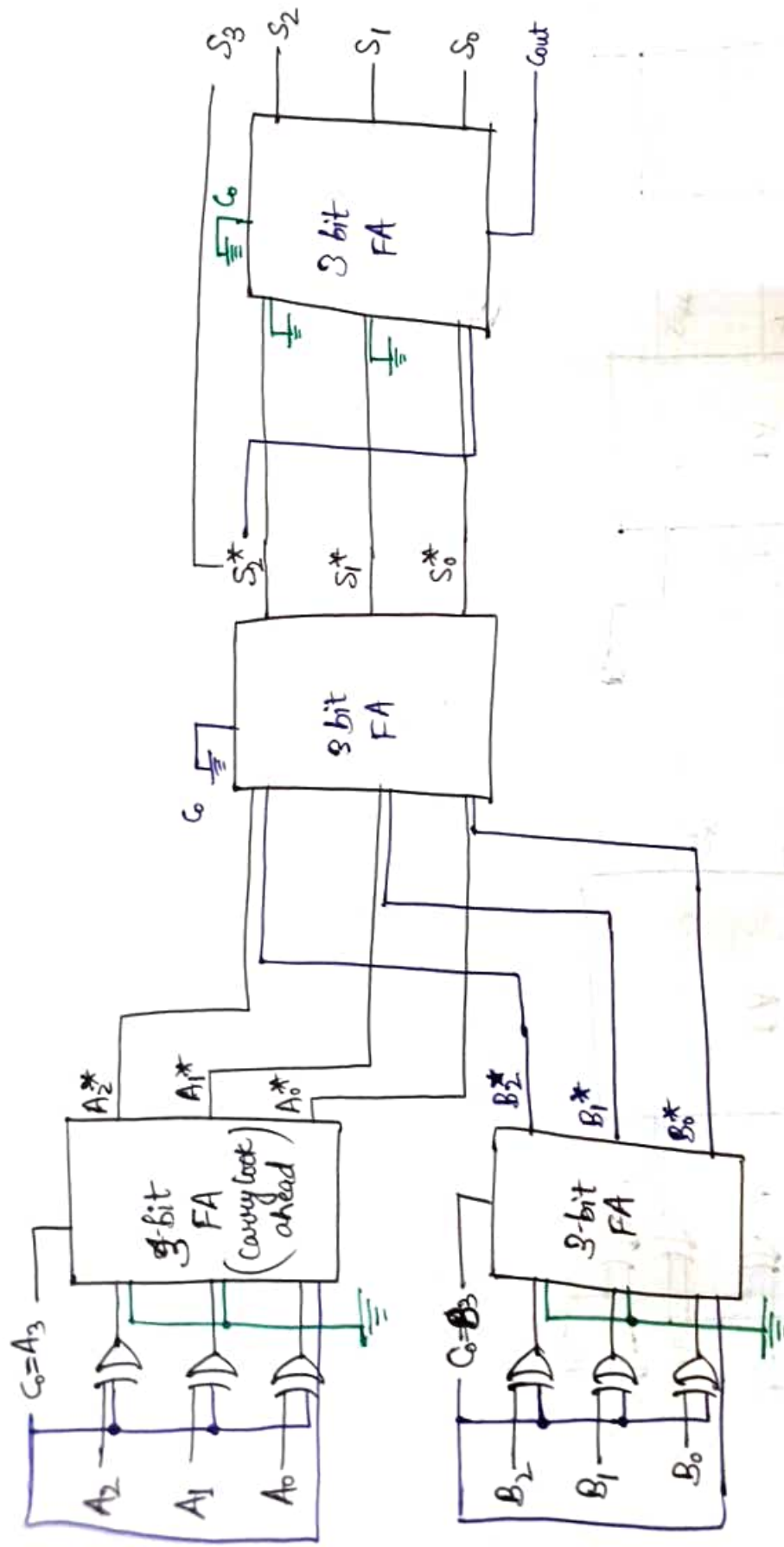
$$\begin{array}{r}
 A = \begin{array}{|c|c|c|c|} \hline A_3 & A_2 & A_1 & A_0 \\ \hline \end{array} \\
 B = \begin{array}{|c|c|c|c|} \hline B_3 & B_2 & B_1 & B_0 \\ \hline \end{array} \\
 \hline
 \begin{array}{|c|c|c|c|} \hline S_3 & S_2 & S_1 & S_0 \\ \hline \end{array} \\
 \text{sign} \\
 S_3 = A_3 B_3
 \end{array}$$

*Sign Magnitude Addition*



*Good*

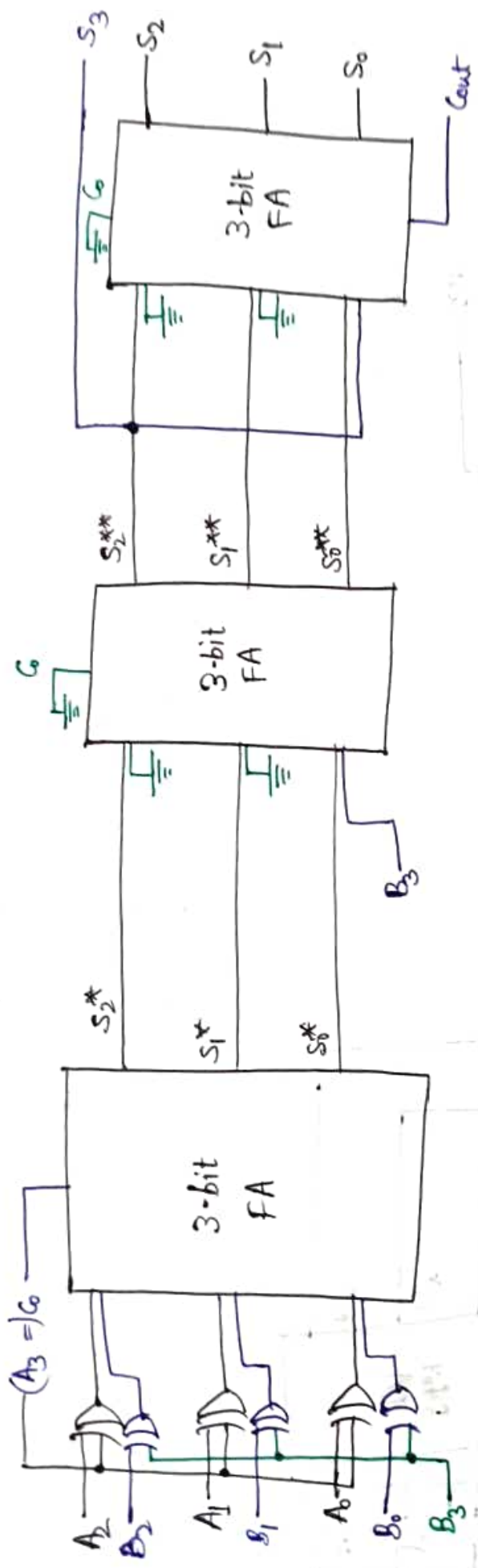
# Alternative Implementation





Alternative Exp

Yet another implementation (using 3 FAs only):



## Carry look ahead adder:

$$\begin{array}{l|l} S_i = P_i \oplus C_i & P_i = A_i \oplus B_i \\ G_{i+1} = G_i + P_i C_i & G_i = A_i B_i \end{array}$$

$$C_0 = C_0$$

$$C_1 = G_0 + P_0 C_0$$

$$G_2 = G_1 + P_1 C_1$$

$$= G_1 + P_1 G_0 + P_1 P_0 C_0$$

$$S_0 = P_0 \oplus C_0$$

$$S_1 = P_1 \oplus C_1$$

$$S_2 = P_2 \oplus C_2$$

