Lab 5 Record: Study of FLIP Flops

Submitted by:

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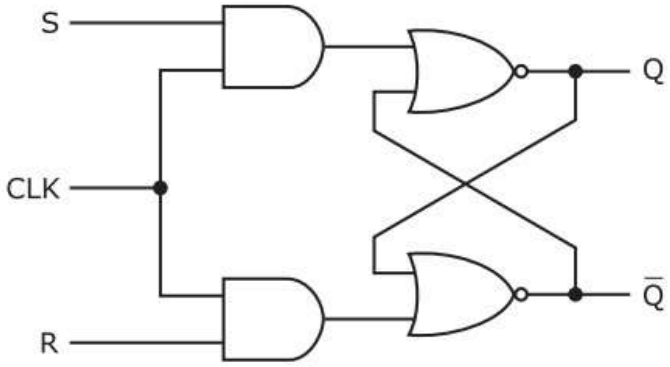
SC22B146

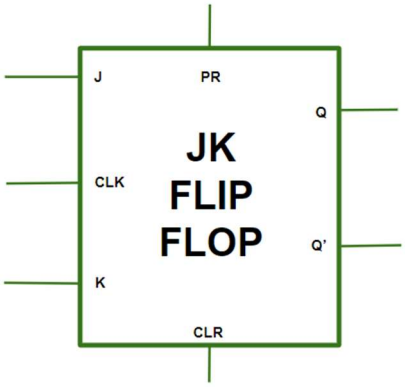
Course: DIGITAL ELECTRONICS AND VLSI DESIGN LAB (AV232)

Aim: To study flip flops

Materials required: AND Gates, OR Gates, NOT Gates, Connecting wires

SR Fip Flop:

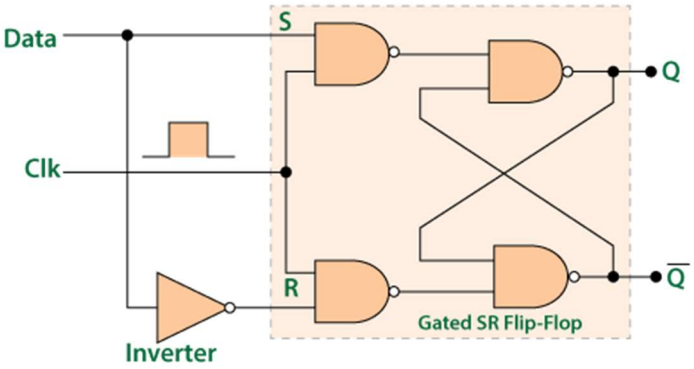


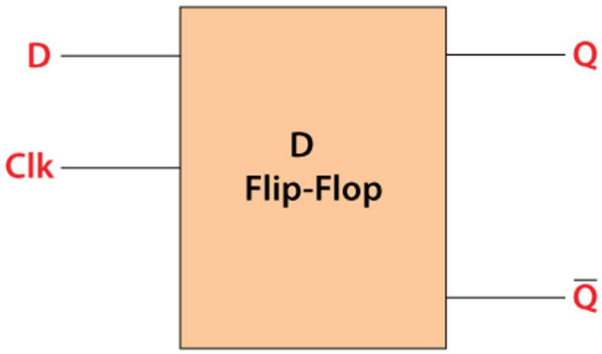


Truth Table:

S	R	Q	Q’
0	0	0	1
0	1	0	1
1	0	1	0
1	1	Indetermined State	

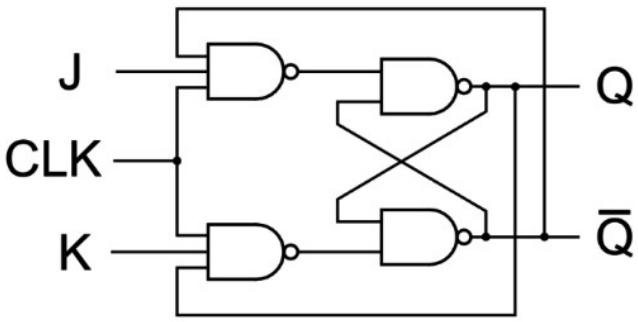
D Flip Flop:

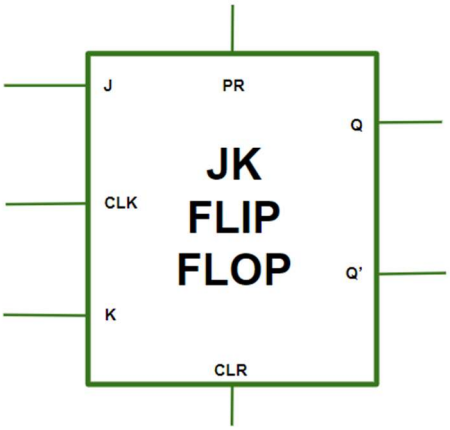




E	D	Q(n+1)
0	X	Q(n)
1	0	0
1	1	1

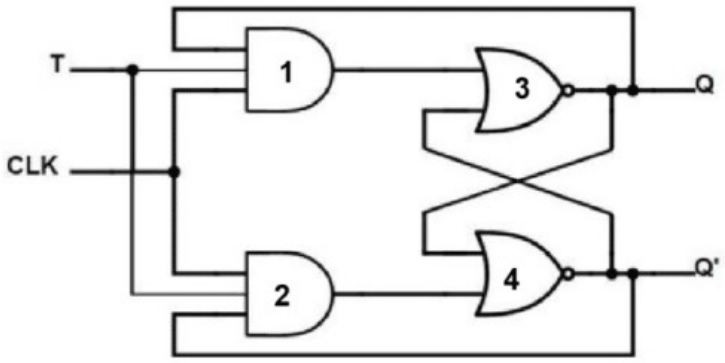
JK Flip Flop:

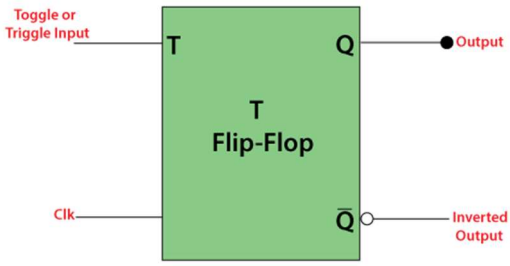




J	K	Q(t)	Q(t+1)	Q'(t+1)
0	0	0	0	1
0	0	1	1	0
0	1	0	0	1
0	1	1	0	1
1	0	0	1	0
1	0	1	1	0
1	1	0	1	0
1	1	1	0	1

Toggle Flip Flop:





T	Q(t)	Q(t+1)	Q’(t+1)
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1