वैद्युतकशास्त्रम्

ELECTRONICS

16-03-2023

SEMICONDUCTOR

- Diode (Switch)
  - Rectifiers
  - Clipers
  - Clampers

Transistor
- Types
- characteristics
- Analysis
  - AC
  - DC

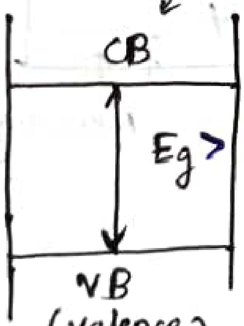
Diode: [p | n]

- 1930 : first diode
- 1947 : first transistor (germenium)
- 1956 : transistor with silicon
- 1970 : transistor with galium arsenite
  - basis for very large scale integration (VLSI)

Material Classification based on Energy Band

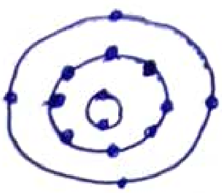
Insulator

(conductor band)

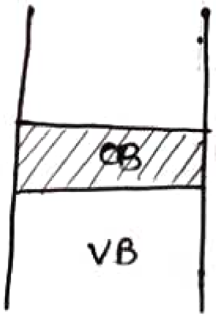


(valence band)

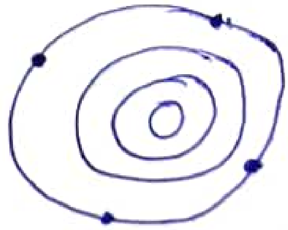
Si: 2+8+4 = 14 e^-



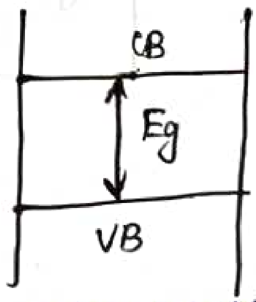
Conductor



Ge: 32 e^-



Semiconductor



Ge : 0.67 eV
Si : 1.1 eV
GA : 1.43 eV

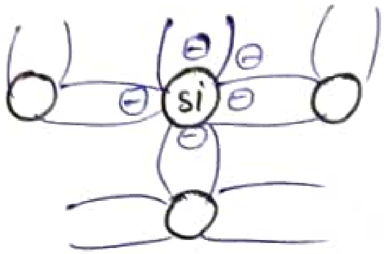
Gallium → 31 e^-
- trivalent

Arsenic → 33 e^-
- pentavalent

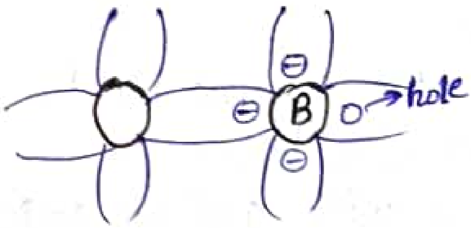
Intrinsic SC: Pure

Extrinsic SC: Impure
↳ by doping

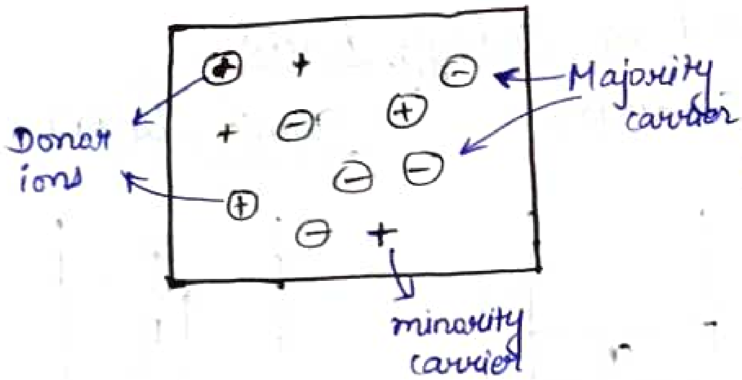
↳ n-type: Adding pentavalent impurity to a Si which is pure.



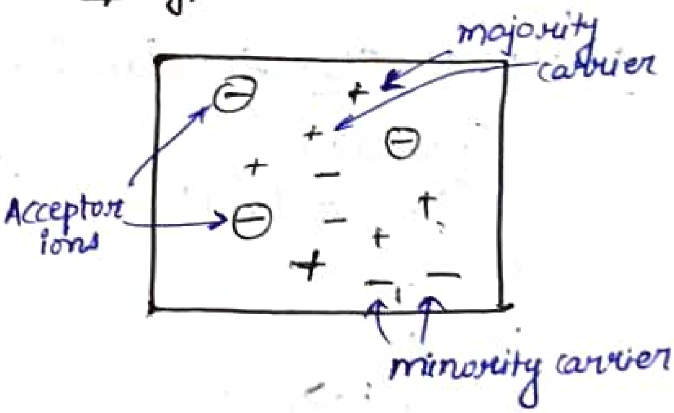
↳ p-type: Adding trivalent impurity

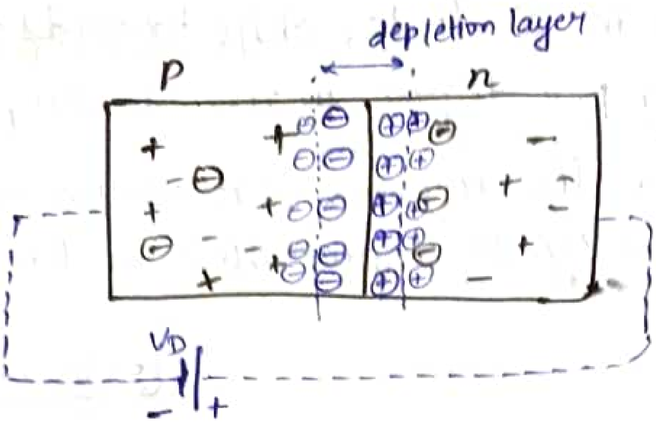


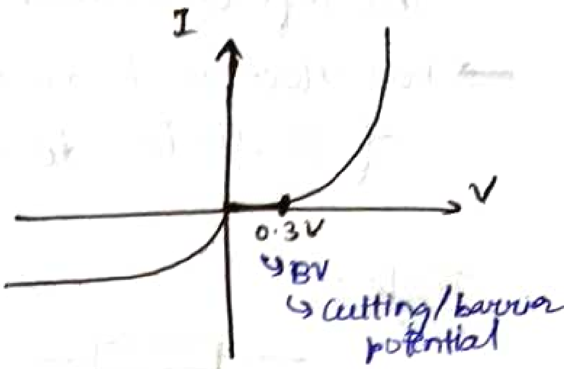
n-type:



p-type:







Conditions:

- No Bias: $V_D \to 0$
- Forward Bias: $V_D > 0V$
- Reverse Bias: $V_D < 0V$

$$I_D = I_s \left(e^{\frac{V_D}{\eta V_T}} - 1\right)$$, where

I_s : saturation current
V_D : Applied voltage
η : Ideality factor (1 or 2)
V_T : Thermal voltage

(If V_D is $\ominus$ve, $I_D \sim I_s$
If $V_D = 0$, $I_D = 0$)

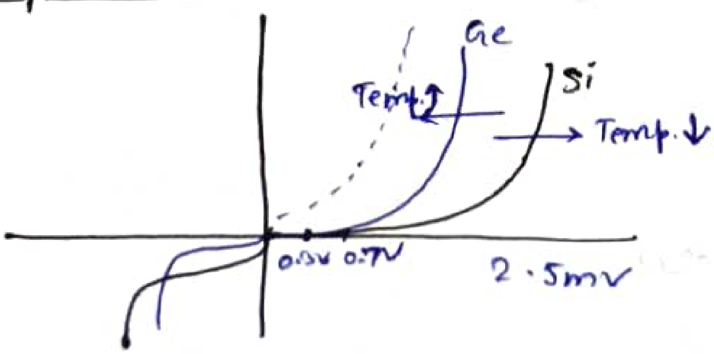
Thermal voltage, $V_T = \frac{kT}{q}$, where

k : Boltzmann's constant $= 1.38 \times 10^{-23}$ J/K
T : Absolute temp. in K (273 + °C)
q : e^- charge $\to 1.6 \times 10^{-19}$ C

Eg. Find the thermal voltage at the temp. of 27°C.

Soln: $V_T = \frac{1.38 \times 10^{-23} \times 300}{1.60 \times 10^{-19}} = \frac{414}{160} \times 10^{-2} = 25.8$ mV

Temperature Variation:

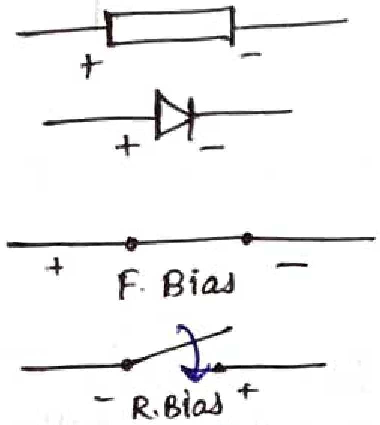


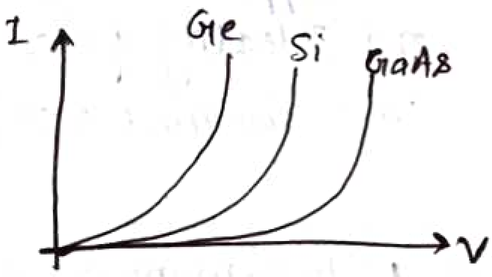
→ For forward biased region in Si diode, shift towards to the left @ 2.5mV for every per degree increase in temp.

→ For reverse biased region, the reverse saturation current of Si diode double for every 10 degree rise in temp.

23-03-2023

Diode:



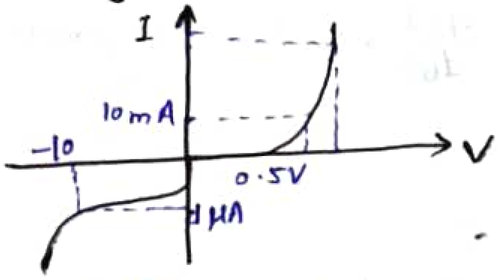


Practical diode

Ideal diode

Resistance

- → Static resistance
- → Dyamic resistance



$$r_1 = \frac{0.5}{10\times10^{-3}} = 50\Omega$$

$$r_2 = \frac{10}{1\times10^{-6}} = 10\times10^{6}\Omega$$

$$r_D = \frac{\Delta V_D}{\Delta I_D}$$

$$I_D = I_S \left(e^{\frac{V_D}{\eta V_T}} - 1\right)$$

$$\Rightarrow I_D \simeq I_S e^{\frac{V_D}{\eta V_T}}$$

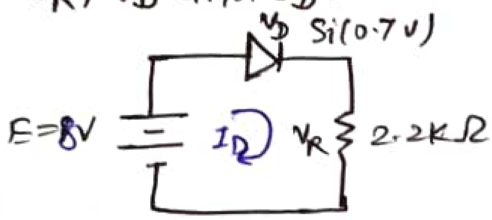
$$\frac{dI_D}{dV_D} = \frac{\left(I_S e^{V_D/\eta V_T}\right) I_D}{\eta V_T} = \frac{I_D}{\eta V_T}$$

$$\therefore r_D = \frac{dV_D}{dI_D} = \frac{\eta V_T}{I_D}$$

Let $\eta = 1$, $V_T = 26\,mV$ (at room temp.)

$$\Rightarrow \boxed{r_D = \frac{20\,mV}{I_D}}$$

Q) Find V_R, V_D and I_D.



Soln: $V_R = I_D R$

$E - V_D - V_R = 0$

$\Rightarrow \cancel{E}^{\,8} - 0.7 - 2.2 \times 10^3 I_D = 0$

$$\Rightarrow I_D = \frac{8 - 0.7}{2.2 \times 10^3}$$

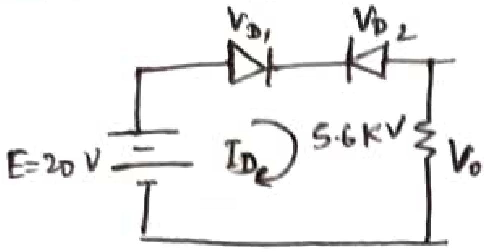
$= 3.32\,mA$

$V_R = 3.32 \times 10^{-3} \times 2.2 \times 10^3$

$= 7.3\,V$

Q Find I_D, V_{D2}, V_o.

| Software: LTSPICE



Soln:

$V_o = I_D \times 5.6 \times 10^3$

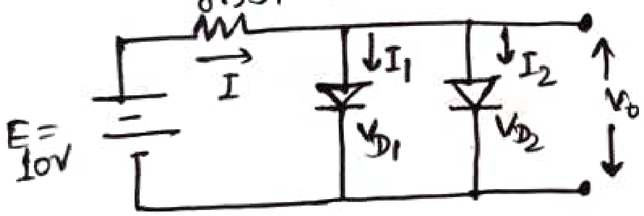
$V_{D2} = 20V$ | $I_o = 0$

$V_o = 0$ | $V_{D_1} = 0$

$I_D = 0$ | $V_R = 0$

$E - \cancel{V_{D_1}}^{0} - V_{D_2} - \cancel{V_R}^{0} = 0$

Q



Consider Si- diode.

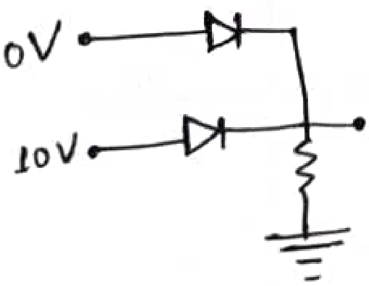
Determine V_o, I, I_1, I_2.

Soln: $V_o = 0.7V$ (For Si)

$$I = \frac{\cancel{E}^{10} - \cancel{V_o}^{0.7}}{0.33 \times 10^3} = 28.18mA$$

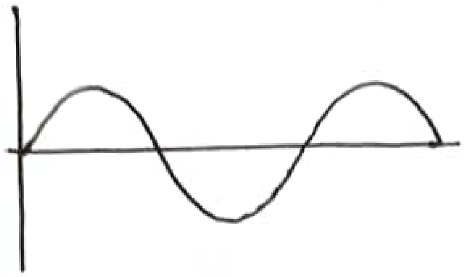
$$I_1 = I_2 = \frac{I}{2} = 14.09$$

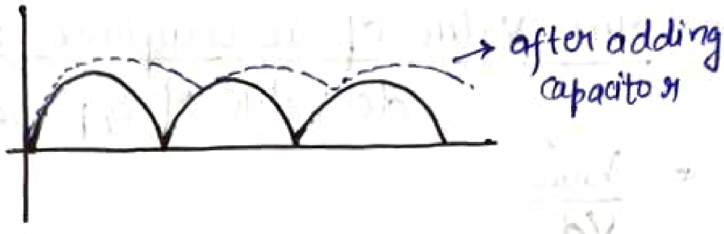
OR GATE



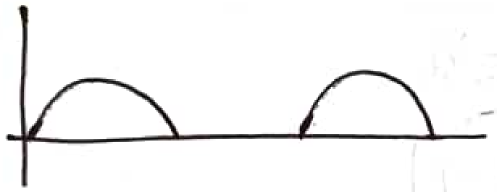
Output = 9.3V

RECTIFIER





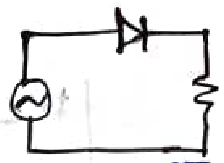
(Full wave Rectifier)



(Half wave Rectifier)

AC — Rectifier — Filter — Voltage Regulator — DC o/p

Half wave Rectifier (HWR)



$$V_{dc} = \frac{1}{2\pi} \int_0^{2\pi} V_m \sin \omega t \, d\omega t$$

$$= \frac{1}{2\pi} \left[\int_0^{\pi} V_m \sin \omega t \, dt + \int_{\pi}^{2\pi} \cancel{V_m}^{0} \sin \omega t \, dt \right]$$

$$= \frac{1}{2\pi} \left[-V_m \cos \omega t \right]_0^{\pi}$$

$$\therefore \boxed{V_{dc} = \frac{V_m}{\pi} = 0.318 \, V_m}$$

$V_{RMS} \rightarrow$ Root mean square

$$V_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{\pi} V_m^2 \sin^2 \omega t \, d\omega t}$$

$$\Rightarrow \boxed{V_{rms} = \frac{V_m}{2}}$$

Ripple factor, γ = $\frac{\text{rms value of ac component of o/p waveform}}{\text{dc value of o/p waveform}}$

(gamma)

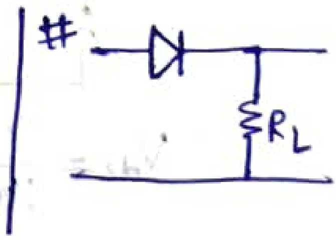
$$= \frac{V'_{rms}}{V_{dc}}$$

$$V'_{rms} = \sqrt{V_{rms}^2 - V_{dc}^2}$$

$$\gamma = \frac{\sqrt{V_{dc}^2\left(\frac{V_{rms}^2}{V_{dc}^2} - 1\right)}}{V_{dc}}$$

$$= \frac{\sqrt{V_{rms}^2 - V_{dc}^2}}{V_{dc}} = \sqrt{\left(\frac{V_m/2}{V_m/\pi}\right)^2 - 1} = \sqrt{\frac{\pi^2}{4} - 1}$$

$$\Rightarrow \gamma = 1.21$$



$\rightarrow$ Efficiency = $\frac{\text{o/p dc power}}{\text{i/p ac power}}$

$$= \frac{V_{dc}^2/R_L}{V_{rms}^2/R_L}$$

$$= \left(\frac{V_m/\pi}{V_m/2}\right)^2 = \frac{4}{\pi^2} = 0.40$$

$= 40.6\ \%$

$\rightarrow$ Form factor = $\frac{\text{rms value}}{\text{Average value}}$

$$= \frac{\pi}{2} = 1.57$$

$\rightarrow$ Peak factor = $\frac{\text{peak value}}{\text{rms value}}$

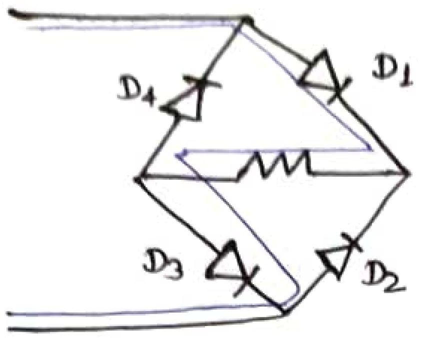
$$= \frac{V_m}{V_m/2}$$

$$= 2$$

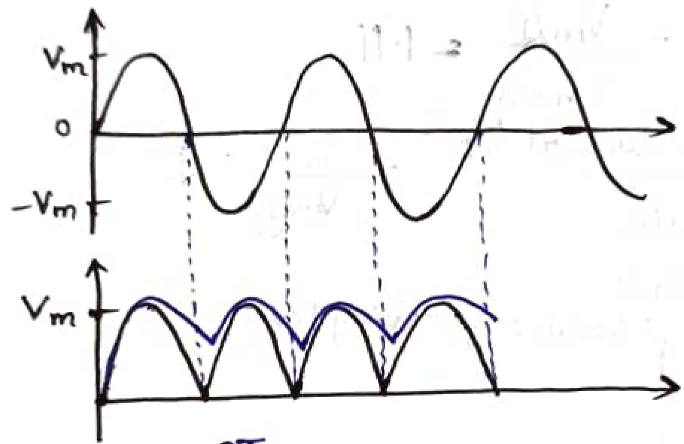
27-03-23

Full Wave Rectifier

* Bridge Rectifier
* Centre Tapped Transformer



+ve cycle:
$D_1 = D_3$
-ve cycle:
$D_2 = D_4$



$$V_{dc} = \frac{1}{2\pi}\int_0^{2\pi} V_m \sin\omega t \, d\omega t$$

$$= \frac{1}{2}\int_0^{\pi} V_m \sin\omega t \, d\omega t + \int_{\pi}^{2\pi} -V_m \sin\omega t \, d\omega t$$

$$\Rightarrow \boxed{V_{dc} = \frac{2V_m}{\pi}}$$

$$V_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} V_m^2 \underbrace{\sin^2\omega t}_{\left(\frac{1-\cos 2\omega t}{2}\right)} \, d\omega t}$$

$$= \frac{1}{\pi}\int_0^{\pi} V_m^2 \left(\frac{1-\cos 2\omega t}{2}\right) d\omega t$$

$$\Rightarrow \boxed{V_{rms} = \frac{V_m}{\sqrt{2}}}$$

→ Ripple factor, $\gamma = \frac{V'_{rms}}{V_{dc}} = 0.482$

$$V'_{rms} = \sqrt{V_{rms}^2 - V_{dc}^2}$$

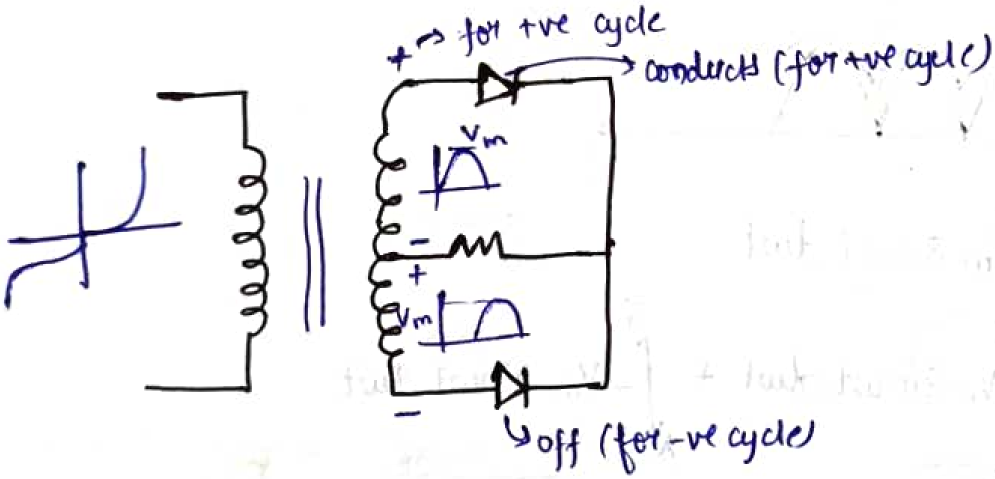
→ $\eta = \frac{\text{dc power}}{\text{ac power}}$

$$= \frac{V_{dc}^2/R_L}{V_{rms}^2/R_L} = \frac{(2V_m/\pi)^2}{(V_m/\sqrt{2})^2}$$

$$= 81.2\%$$

→ form factor $= \frac{V_{rms}}{V_{dc}} = \frac{V_m/\sqrt{2}}{2V_m/\pi} = 1.11$

→ peak factor $= \frac{\text{peak value at o/p}}{\text{rms value}} = \frac{V_m}{V_m/\sqrt{2}} = \sqrt{2}$

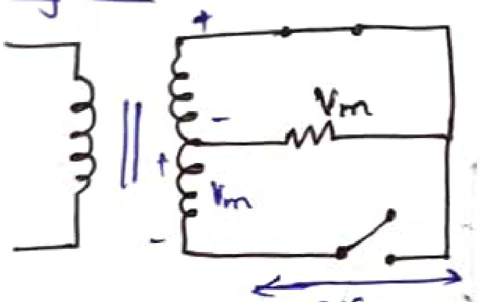


PIV (Peak Inverse Voltage):

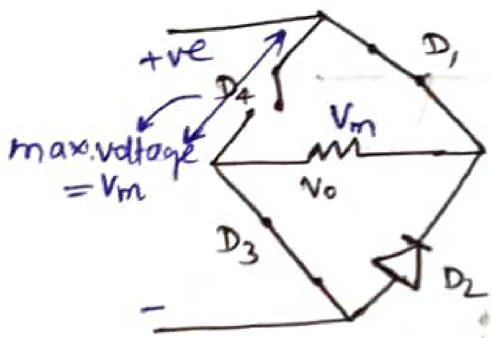
↳ The max. reverse bias voltage a diode can tolerate before breakdown.

Bridge transformer: PIV $\geq V_m$.
centre tapped transformer: PIV $\geq 2V_m$

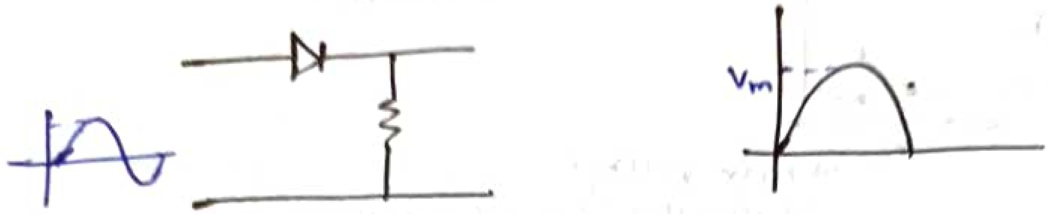
In +ve cycle:



2Vm → max. voltage
↳ after this, breakdown will happen.

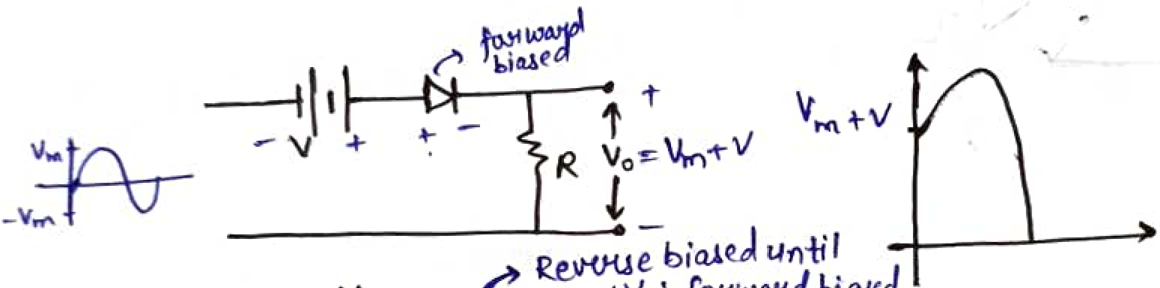


CLIPPERS

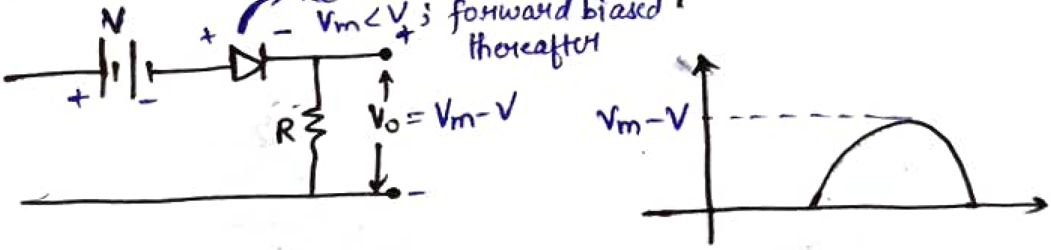


Vm

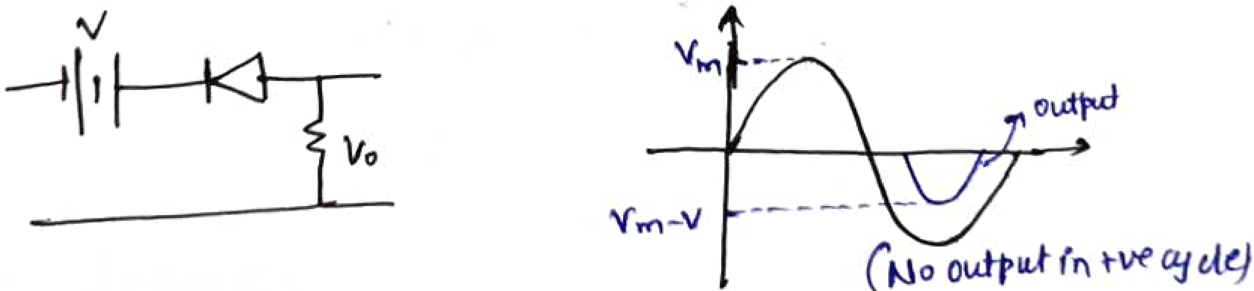
-Vm



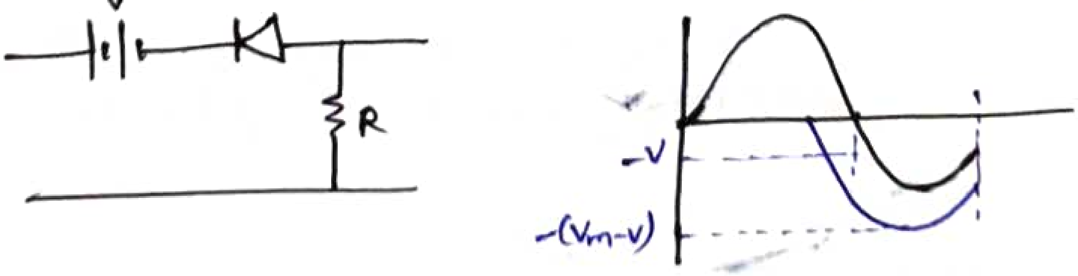
forward biased
- V +
+ -
R
+
Vo = Vm+V
-
Vm
-Vm
Vm + V



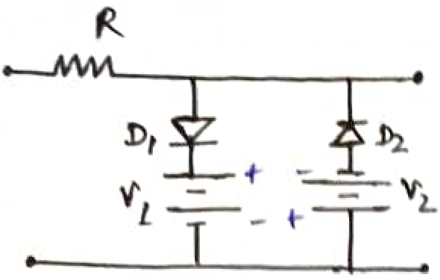
Reverse biased until Vm < V ; forward biased thereafter
V
+ -
+ -
R
+
Vo = Vm-V
-
Vm-V



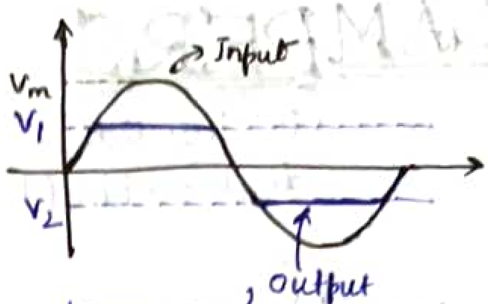
V
Vo
Vm
output
Vm-V
(No output in +ve cycle)

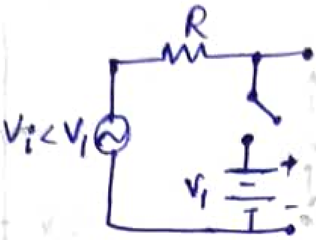


V
R
-V
-(Vm-v)

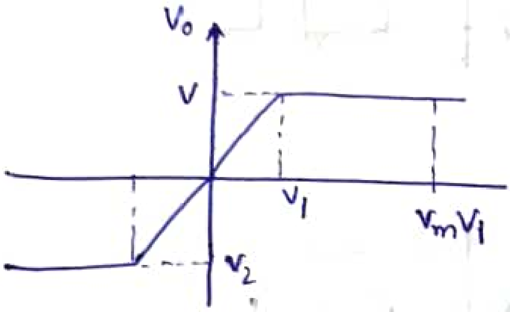
→ 

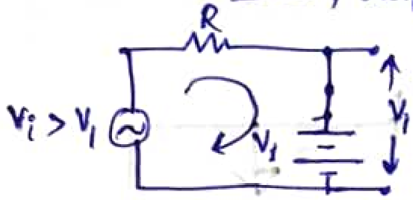
(Ideal diodes: $V_1 > V_2$)

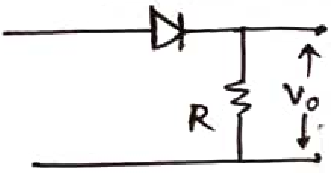


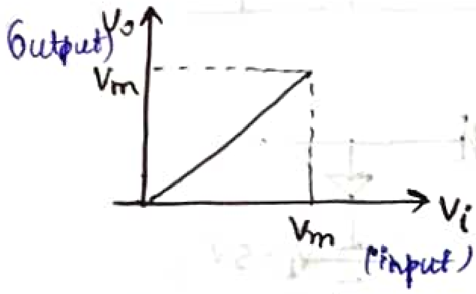


In +ve cycle,
upto V_1, Input follows the output.
above V_1, output voltage $= V_1$
$= \text{constant}$

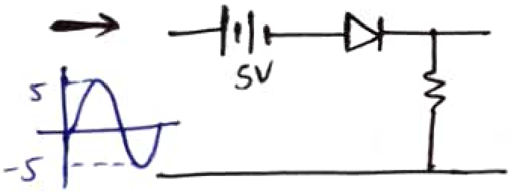


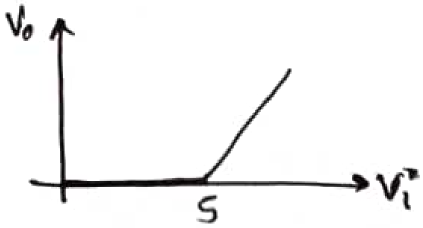


→ 



Transfer curve → Relation b/w V_o and V_i

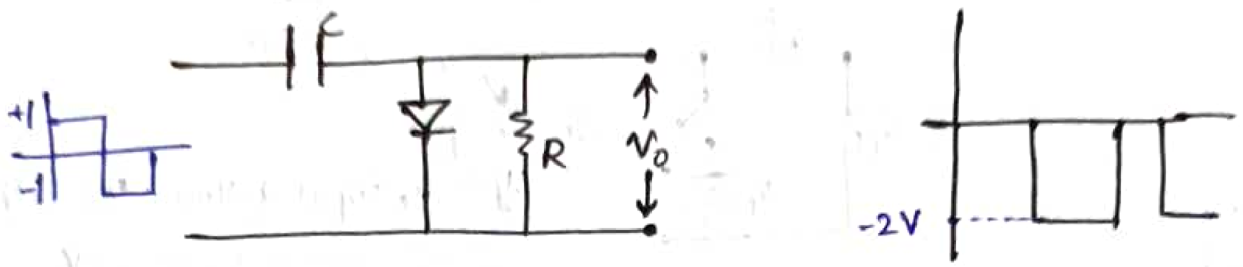
→ 

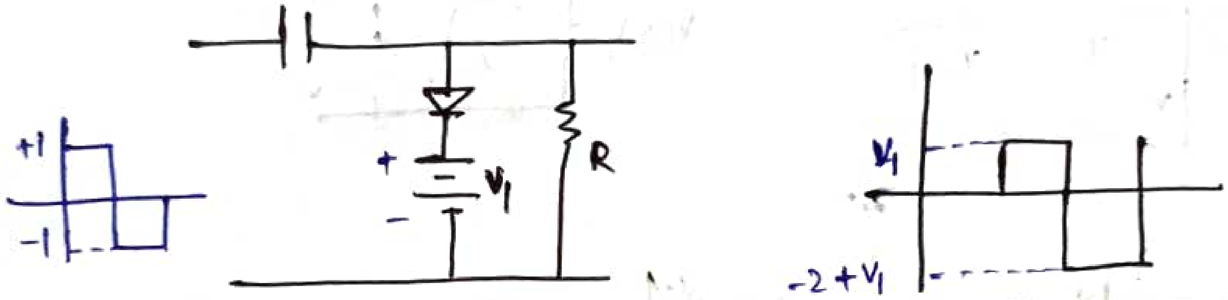


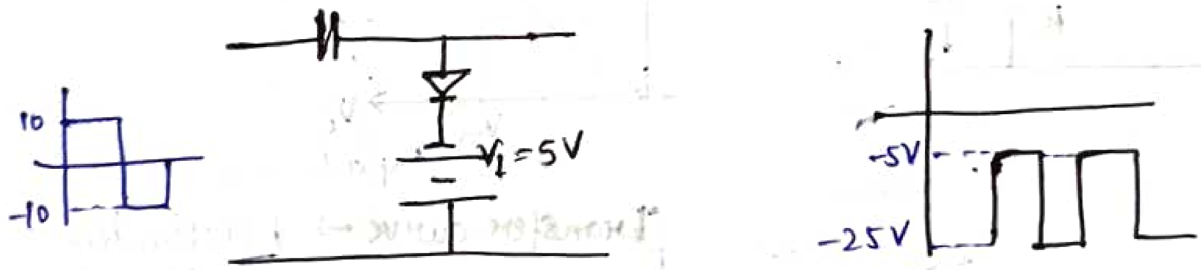
CLAMPERS

(DC Insertor)

(diode → ideal)

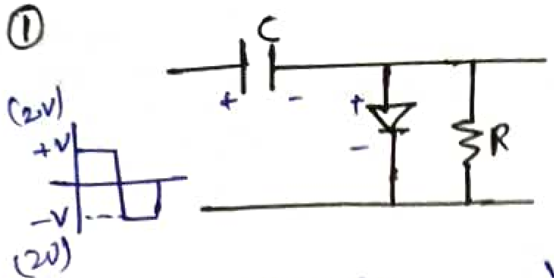




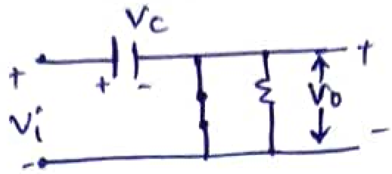


30-03-23

①

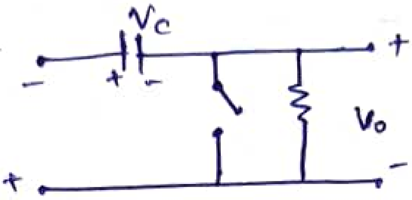


+ve cycle:



$V_i = V_c$

-ve cycle:

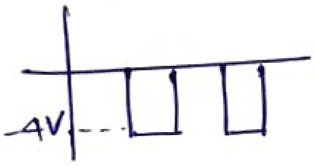


$+V_i - V_c - V_o = 0$

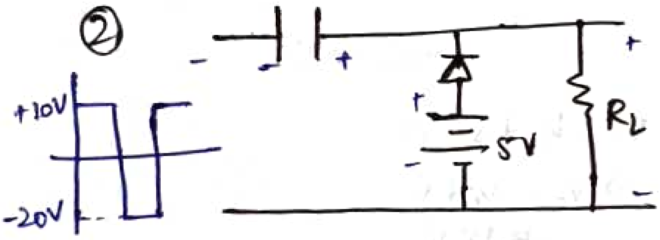
$\Rightarrow V_o = -V_i - V_c$

$= -2V - 2V$

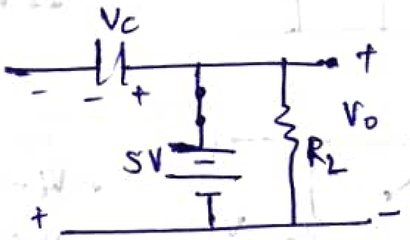
$= -4V$



②



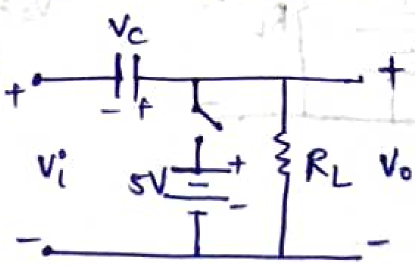
-ve cycle:



$-20V + V_c - 5 = 0$

$\Rightarrow V_c = 25V$

+ve cycle:

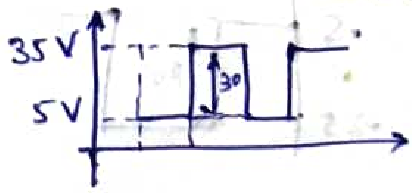


$V_i + V_c - V_o = 0$

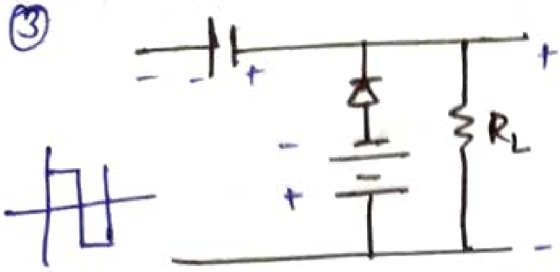
$\Rightarrow V_o = V_i + V_c$

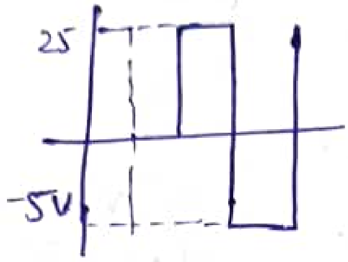
$= 10 + 25$

$= 35V$

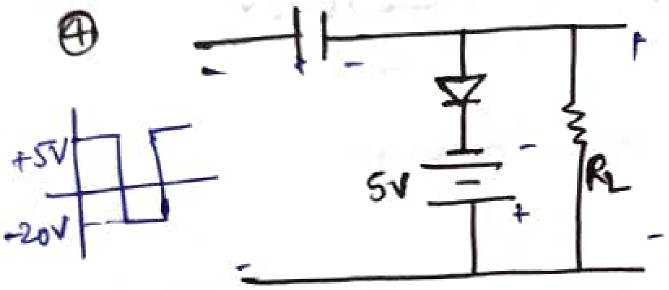


③

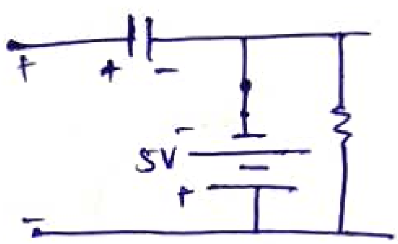




④



+ve cycle:

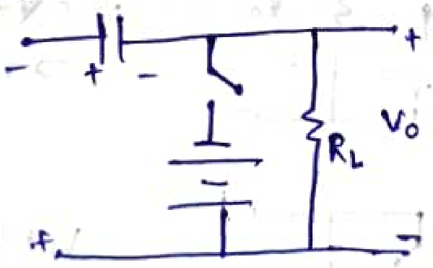


$V_i - V_L + 5 = 0$

$\Rightarrow V_c = V_i + 5$

$= 15V$

-ve cycle:

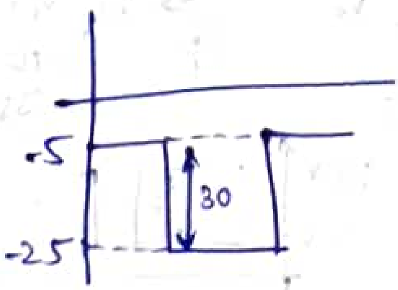


$-V_i - V_c - V_o = 0$

$V_o = -V_i - V_c$

$= -20-15$

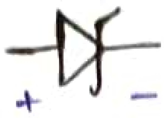
$= -35$

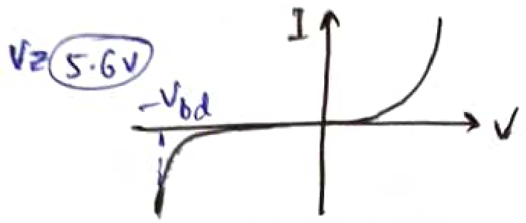


ZENER DIODES

(Reverse Bias Diode)

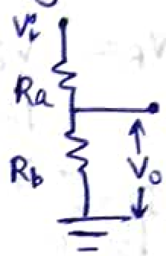
- → Application in reverse bias
- → Characteristic is similar to p-n diodes in forward bias.





PIV } Peak Inverse/Reverse
PRV } Voltage

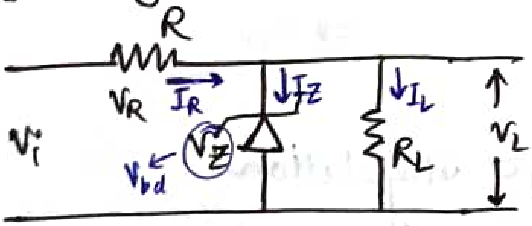
\# Voltage divider rule:



* Zener Breakdown

* Avalanche Breakdown — ionization

Voltage Regulation



$$V_L = \frac{V_i \times R_L}{R + R_L}$$

↳ when input $V_i < V_Z$, diode is an open circuit (switch).
when input $V_i \geq V_Z$, diode is closed circuit (switch).

$$I_R = I_Z + I_L$$

$$I_L = I_R - I_Z$$

$$I_L = \frac{V_L}{R_L}$$

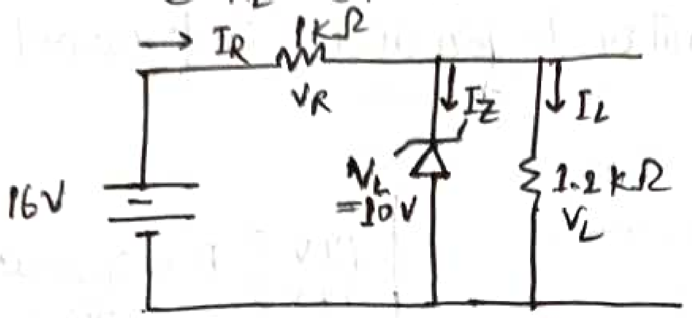
$$P_Z = I_Z \cdot V_Z$$

$$I_R = \frac{V_R}{R} = \frac{V_i - V_L}{R}$$

Q For the given circuit, calculate: V_L, V_R, I_Z & P_Z,

for (a) $R_L = 1.2\,k\Omega$

(b) $R_L = 3\,k\Omega$



Soln: (a) $V_L = \dfrac{16V \times 1.2\,k\Omega}{(1k + 1.2k)\,\Omega} = 8.73\,V$

$V_R = V_i - V_L$
$= 16 - 8.73$
$= 7.27\,V$

$I_Z = 0$
$P_Z = 0$

(b) $V_L = \dfrac{16 \times 3\,k\Omega}{3k + 1k} = 12\,V$

$V_R = V_i - V_L$
$= 16 - \cancel{12} \, 10$ ⤳ voltage regulation
$= 6V$

$I_L = \dfrac{V_L}{R_L} = 3.33\,mA$

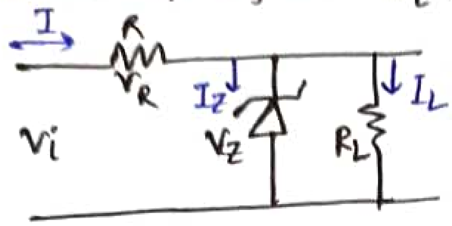
$I_R = \dfrac{V_R}{R} = \dfrac{6V}{1k}$

$I_Z = I_R - I_L = 2.67\,mA$

$P_Z = I_Z V_Z$

3-04-2023

Q)
① Fixed V_i & fixed R_L.
② Fixed V_i & variable R_L.
③ Variable V_i & fixed R_L.



Soln:

$$V_L = \frac{V_i R_L}{R+R_L}$$

R_{Lmin} & R_{Lmax}

$$V_L(R+R_L) = V_i R_L$$

$$R_L(V_L - V_i) = V_L R$$

$$R_{Lmin} = \frac{V_L R}{V_i - V_L}.$$

$$\boxed{R_{Lmin} = \frac{V_Z R}{V_i - V_Z}}$$

$$I = I_Z + I_L$$

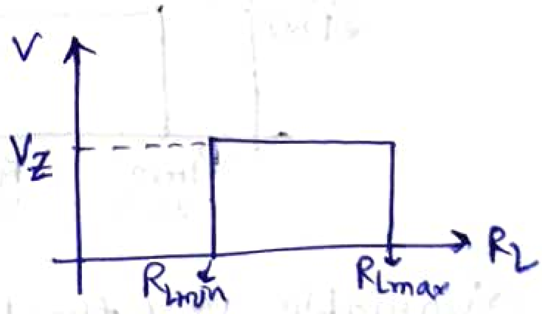
$$V_R = V_i - V_Z$$

$$I_R = \frac{V_R}{R}$$

$$I_Z = I_R - I_L$$

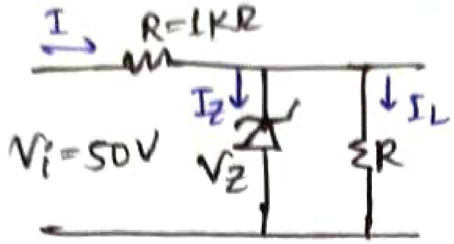
$$I_{Lmin} = I_R - I_Z$$

$$R_{Lmax} = \frac{V_Z}{I_{Lmin}}$$



Q Calculate the min^m & max^m resistance values and currents of the load resulting in $V_L = 10V$ or $V_Z = 10V$.

Take $V_i = 50V$, $R = 1k\Omega$, $I_Z = 32mA$.



Soln: $R_{Lmin} = \dfrac{V_L R}{V_i - V_L} = \dfrac{10 \times 1000}{50-10} = 250\Omega$

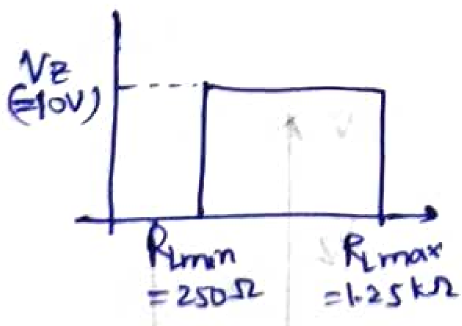
$V_R = V_i = V_Z = 40V$

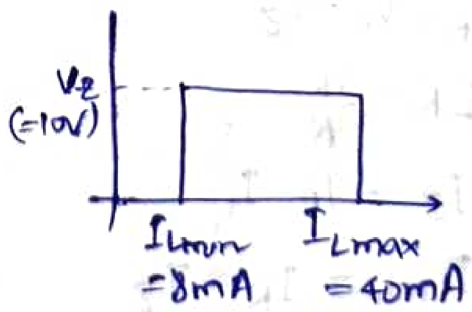
$I_R = \dfrac{V_R}{R} = 0.04A$

$I_{Lmin} = I_R - I_Z = 0.04 - 0.032 = 0.008 = 8mA$

$R_{Lmax} = \dfrac{V_Z}{I_{Lmin}} = \dfrac{10}{8\times10^{-3}} = 1.25\,k\Omega$

$I_{Lmax} = \dfrac{V_Z}{R_{Lmin}} = \dfrac{10}{250} = 40mA$





→ **Variable V_i & fixed R_L:**

$$V_L = \frac{V_i R_L}{R + R_L}$$

$$V_{i,min} = \frac{V_Z (R_L + R)}{R_L}$$

The max^m value of V_i is limited by V_{ZM}.

$$I_{ZM} = I_R - I_L$$

$$I_{R\,max} = I_{ZM} + I_L$$

$$I_L = \frac{V_L}{R_L}$$

$$I = I_Z + I_L$$

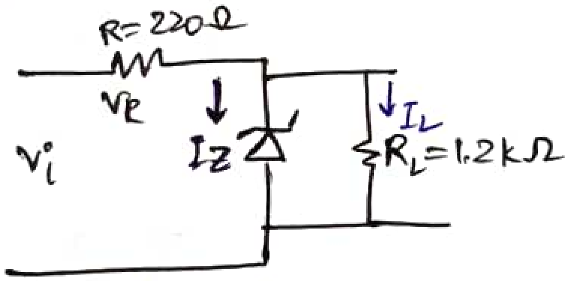
$$V_R = V_i - V_Z$$

$$V_{i,max} = V_{R,max} + V_Z$$

$$= I_{R,max} + V_Z.$$

Q) Calculate the range of input values for the voltage regulation.

$V_Z = 20V$, $I_{ZM} = 60mA$.



Soln: $V_{i,min} = \frac{V_Z(R_L+R)}{R_L} = \frac{20(1.2K+220)}{1.2K}$

$$= 23.6V$$

$$I_L = \frac{V_L}{R_L} = \frac{20}{1.2k\Omega} = 16.67\,mA$$

$$I_{R,max} = I_{ZM} + I_L$$

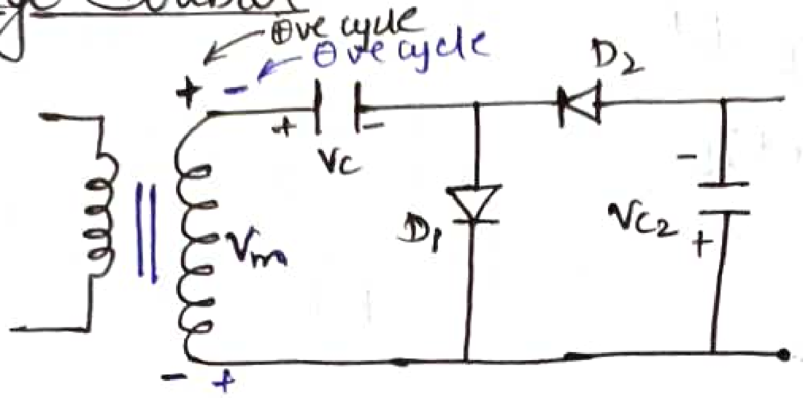
$$= 60\,m + 16.67\,m = 76.67\,mA$$

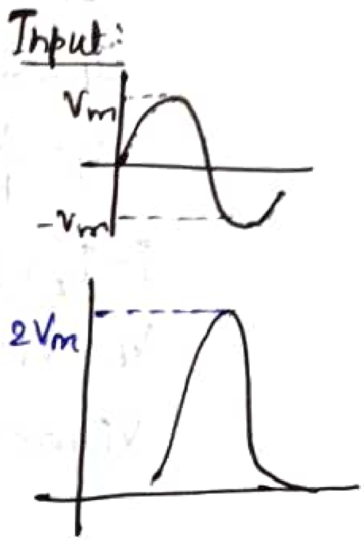
$$V_{i,max} = V_{R\,max} + V_Z$$

$$= (76.76\,m)(220) + 20$$

$$= 36.8V$$

Voltage Doubler





+ve cycle:

$$+V_m - V_c = 0$$

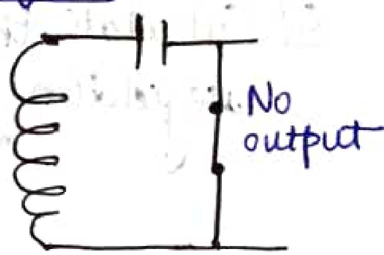
$$\Rightarrow V_c = +V_m$$

-ve cycle:

$$-V_m - V_c + V_{c_2} = 0$$

$$\Rightarrow V_{c_2} = 2V_m$$

+ve cycle:



6-04-2023

Bipolar Junction Transistor

(BJT)

↳ Current conduction is due to major and minor carries.

↳ Type → npn
→ pnp

↳ Applications → Amplifier
→ Switch

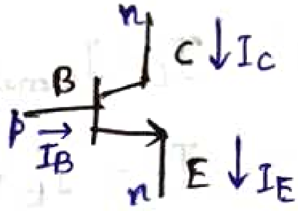
↳ 3 terminals
→ Base : lightly doped
→ Emitter : highly doped
→ Collector : moderately doped

n	p	n
E	B	C

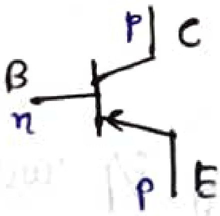
p	n	p
E	B	C

Symbol:

npn:



pnp:

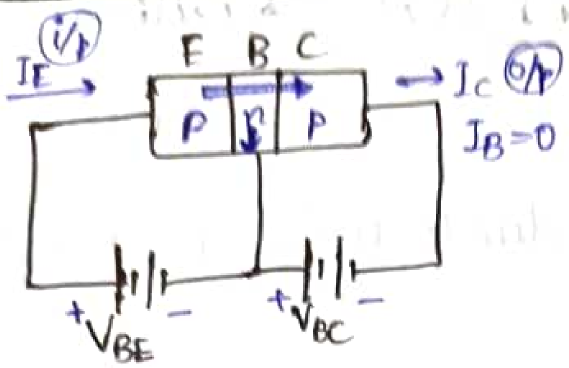


$$\boxed{I_E = I_B + I_C}$$

Characteristics:

* Common Base (CB)
* Common Emitter (CE)
* Common Collector (CC)

Common Base Characteristics/Configuration



Regions of operation:

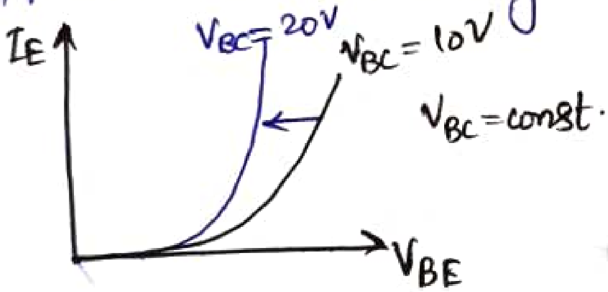
① **Active:** i/p is F.Bias & o/p is R.Bias

② **Cutoff:** i/p & o/p are R.Bias.

③ **Saturation:** i/p & o/p are F.Bias.

Input (i/p) chts.:

i/p current & i/p voltage keeping o/p voltage constant.



$I_C = I_{C_{majority}} + I_{C_{minority}}$

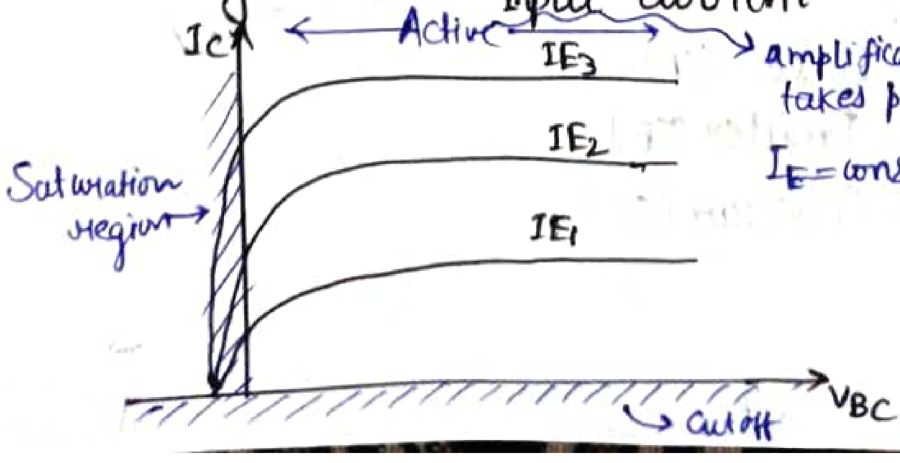
$I_E = I_B + I_C$

o/p chts.:

o/p current & o/p voltage keeping i/p current constant.

CB

current gain, $\alpha_{dc} = \frac{\text{output current}}{\text{Input current}} = \frac{I_C}{I_E} \rightarrow 0.908$ to $0.99 \approx 1$



→ amplification takes place

I_E = const.

Current gain:

α, β, γ

↓ CB ↓ CE ↓ CC

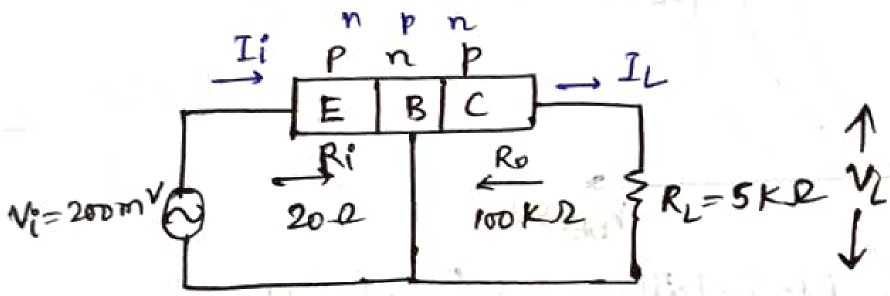
$$\alpha_{ac} = \frac{\Delta I_C}{\Delta I_E}$$

→

I_{CB_0} → b/w C & B when E is open

$$I_c = \underbrace{\alpha I_{E,}}_{\text{maj. carrier} \downarrow \text{mA}} + \underbrace{I_{CB_0}}_{\text{min. carrier} \downarrow \mu A}$$ (including minority carriers)

"$I_c \cong \alpha I_E$"



R_i, R_o → i/p & o/p resistance of transistor

It is understood that the transistor is Biased in the active region with dc voltage

$$I_i = \frac{V_i}{R_i} = \frac{200mV}{20\Omega} = 10mA$$

$I_i \approx I_L$ [CB, $\alpha \approx 1$]

$V_L = I_L \cdot R_L = 50V$

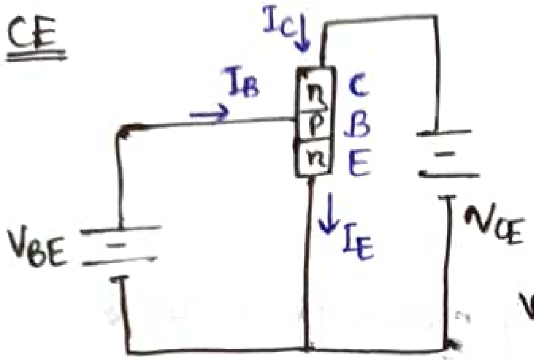
$$A_v = \frac{V_L}{V_i} = \frac{50}{200mV} = 250$$

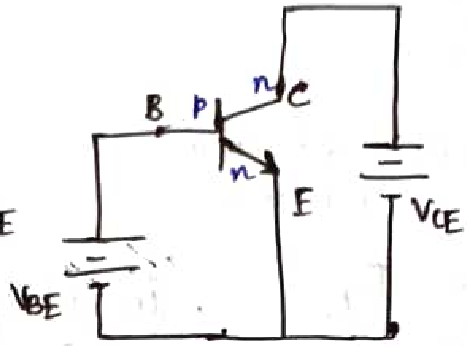
A_v → Voltage gain

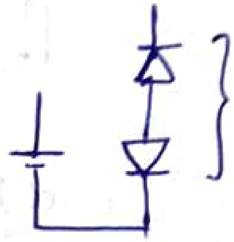
CB

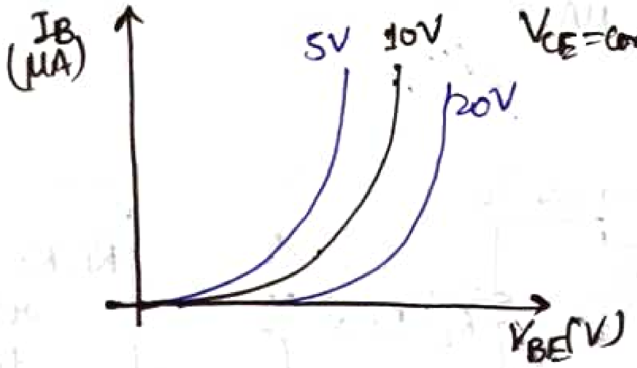
$$\alpha = \frac{I_C}{I_E}$$

CE

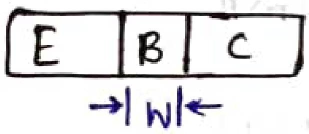








→ Base Width Modulation → "Early effect".



$$W_{eff} = W - W_B$$

$$I_E = I_C + I_B \quad -①$$

$$I_C = \alpha I_E + I_{CBo}$$

$$\Rightarrow I_C = \alpha(I_C + I_B) + I_{CBo}$$

$$\Rightarrow I_C(1-\alpha) = \alpha I_B + I_{CBo}$$

$$\Rightarrow I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBo}$$

If $I_B = 0$, $I_C = \frac{1}{1-\alpha} I_{CBo}$

$\alpha : 0.96 - 0.98$

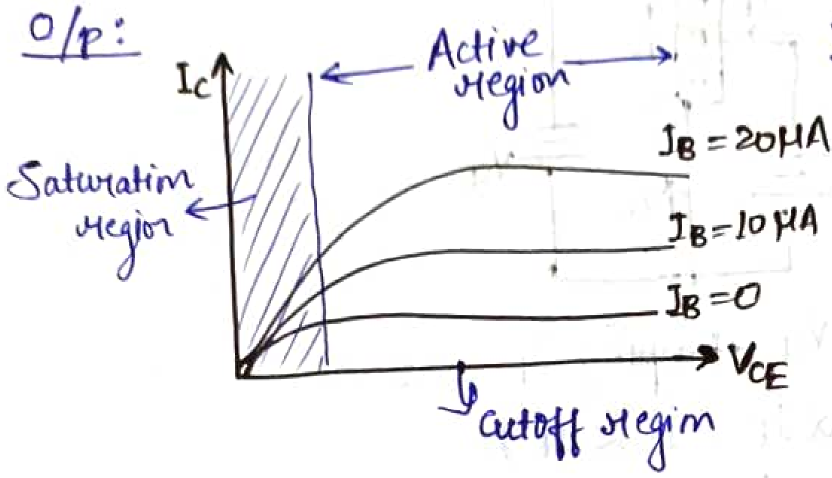
Let $I_{CBo} = 1\ \mu A$

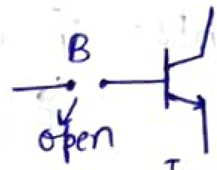
$\therefore I_C = 25\ \mu A,\ 50\ \mu A$
(for $\alpha = 0.96$) (for $\alpha = 0.98$)

$\rightarrow \beta = \frac{\Delta I_C}{\Delta I_B}$

$\beta : 50 \sim 400$

O/p:





$I_{CE_0} \rightarrow$ minority current in CE

$\frac{I_{CB_0}}{1-\alpha} = I_{CE_0}$

Relation b/w α and β:

$\alpha = \frac{I_C}{I_E}$

$\beta = \frac{I_C}{I_B}$

$I_E = I_C + I_B$

$\Rightarrow \frac{I_C}{\alpha} = I_C + \frac{I_C}{\beta}$

$\Rightarrow \frac{1}{\alpha} = 1 + \frac{1}{\beta} \Rightarrow \frac{1}{\beta} = \frac{1}{\alpha} - 1 = \frac{1-\alpha}{\alpha} \Rightarrow \boxed{\beta = \frac{\alpha}{1-\alpha}}$

$\Rightarrow \frac{1}{\alpha} = \frac{\beta + 1}{\beta}$

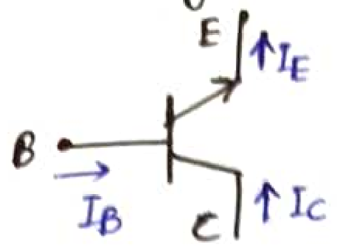
$\Rightarrow \boxed{\alpha = \frac{\beta}{\beta + 1}}$

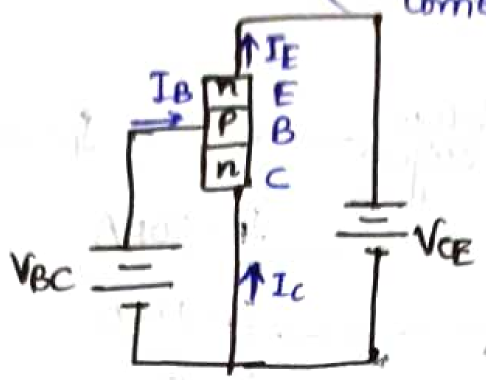
CB: $I_C = \alpha I_E + I_{CB_0}$

CE: $I_C = \underbrace{\beta I_B}_{\text{maj.}} + \underbrace{(1+\beta) I_{CB_0}}_{\underbrace{I_{CE_0}}_{\text{min.}}} \Rightarrow \beta \gg 1$

CC configuration ⇝ called as Emitter follower

(# whatever is given in input, comes out at output)





O/p chts: I_E vs. V_{CE}, keeping I_B constant.

$I_c = \alpha I_E \ (I_c \approx I_E)$

voltage gain → 1

↳ Applications:

- → Buffer
- ↳ Impedence matching

$$\gamma = \frac{I_E}{I_B}$$

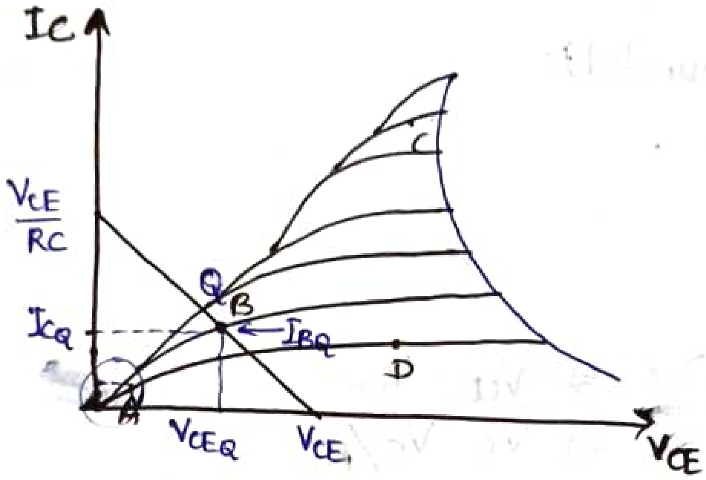
(17-04-2023)

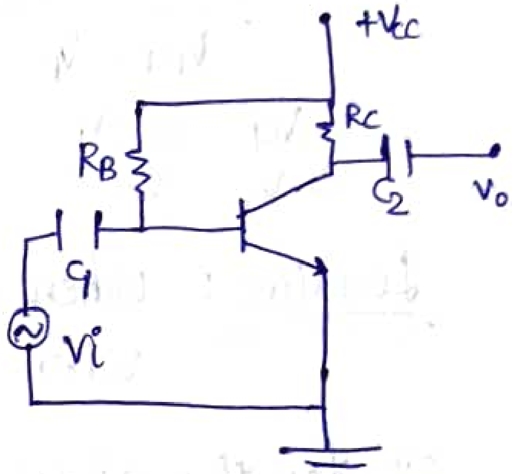
DC Biasing

Bias → helps to fix the operating point (Q point).

Application of BJT
- → Switch
- → amplifier

CE - chts.





Fixed Bias

* Fixed Bias
* Self Bias / Emitter Bias
* Voltage Divider Bias

→ Biasing:

$V_{BE} \approx 0.7V$

$I_C = \beta I_B$

$I_E = I_B + I_C$

$= I_B + \beta I_B$

$= (1+\beta) I_B$

$\beta >> 1$

$\therefore I_E = \beta I_B \approx I_C$

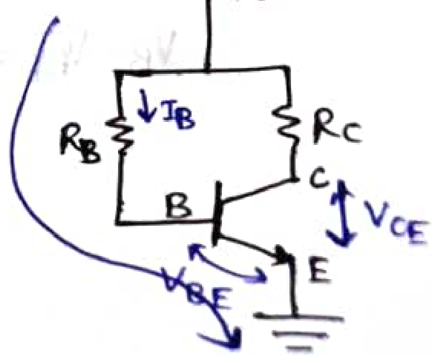
→ DC Biasing

↳ Steps: ① Remove ac supply.

② Open circuit capacitors.

$V_{CC} - I_B R_B - V_{BE} = 0$

$\Rightarrow I_{BQ} = \dfrac{V_{CC} - V_{BE}}{R_B}$



O/p chts. :

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$\Rightarrow I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

$$V_{BE} = V_B - V_E$$

As $V_E = 0$ ($\because$ grounded)

$$\therefore V_{BE} = V_B$$

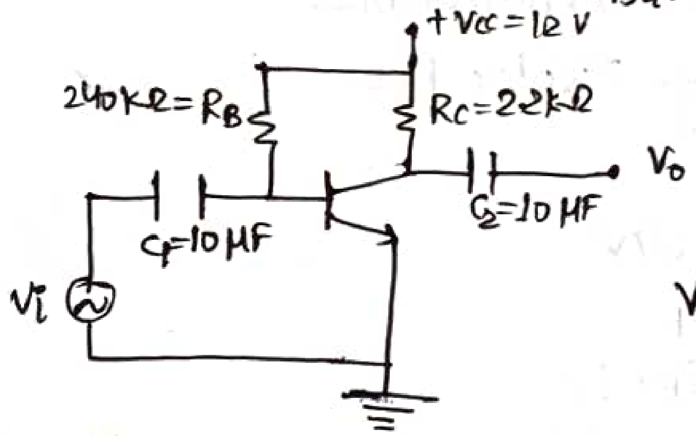
$$V_{CE} = V_C - V_E$$

$$\Rightarrow V_{CE} = V_C$$

Loadline: when $I_C = 0 \Rightarrow V_{CE} = V_{CC}$

when $V_{CE} = 0 \Rightarrow V_C = V_{CC}/R_C$

Q) For the given circuit, determine I_{BQ}, I_{CQ}, V_{CEQ}, V_B, V_C & V_{BC}



$V_{BE} = 0.7\,V$
$\beta = 50$

Soln:

$$I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12 - 0.7}{240k} = 47.08\,\mu A$$

$$I_{CQ} = \beta I_{BQ} = 50 \times 47.08\,\mu$$
$$= 2.35\,mA$$

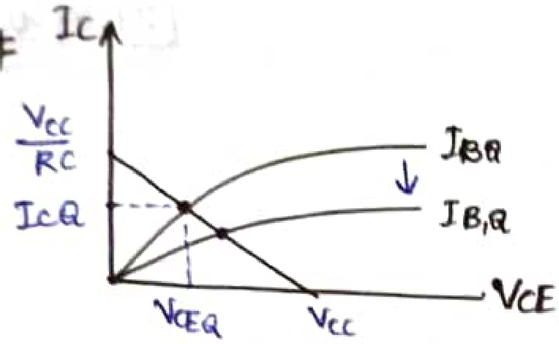
$$V_{CEQ} = V_{CC} - I_C R_C = 6.83\,V$$

$$V_B = V_{BE} = 0.7\,V$$

$$V_C = V_{CE} = 6.83\,V$$

$$V_{BC} = 0.7 - 6.83\,V$$
$$\approx -6.1\,V$$

#



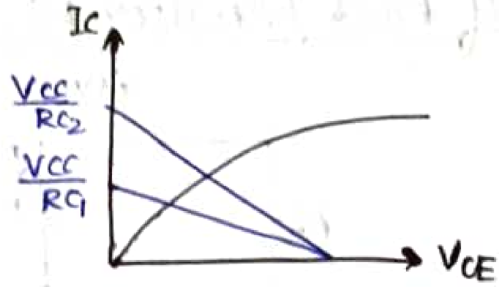
→ Variation with R_B,

$$I_{BQ} = \frac{V_{CC} - V_{CE}}{R_{B_1}}$$

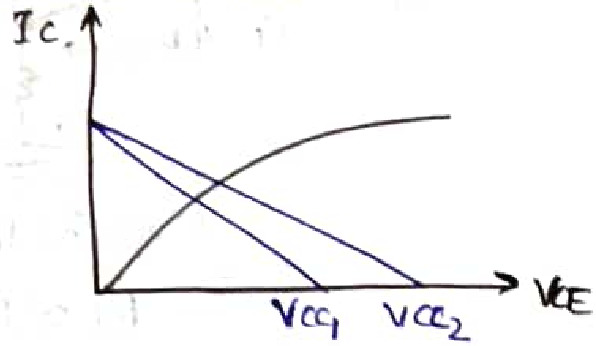
$$R_{B_1} > R_{B_2}$$

→ Variation with R_C,

$$R_{C_1} > R_{C_2}$$

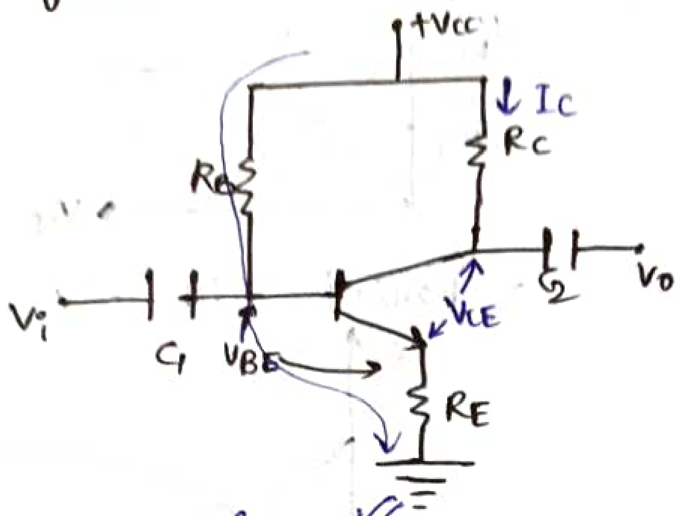


→ Variation with V_{CC}:



27-04-2023

Self Bias / Emitter Bias



increased the stability

$$R_i \approx (1+\beta) R_E$$

i/p chrt:

$$V_{cc} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$\Rightarrow I_E = (\beta+1) I_B$$

$$\Rightarrow \boxed{I_{BQ} = \frac{V_{cc} - V_{BE}}{R_B + (\beta+1) R_E}}$$

→ acts like feedback

o/p chrt.:

$$V_{cc} - I_C R_C - V_{CE} - I_C R_E$$

$$I_C \approx I_C$$

$$V_{CE} = V_{cc} - I_C (R_C + R_E)$$

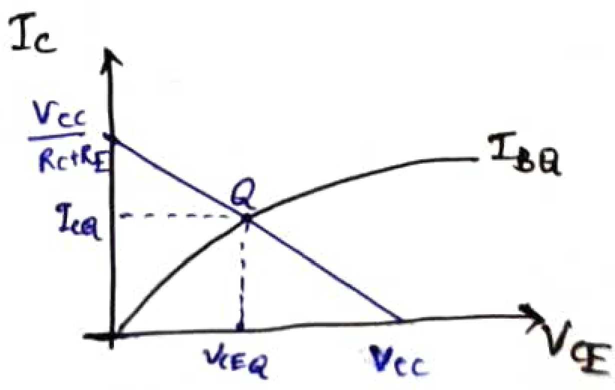
$$V_E = I_E R_E$$

$$V_{cc} = V_C - V_E$$

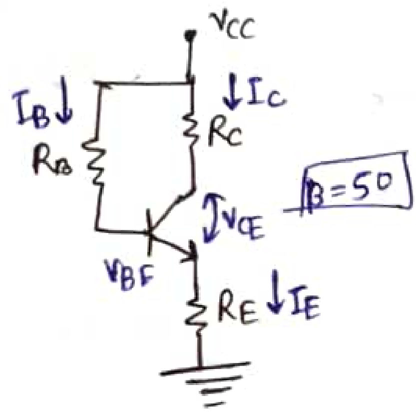
$$V_C = V_{CC} - I_C R_E$$

$I_C = 0$, $V_{CE} = V_{CC}$

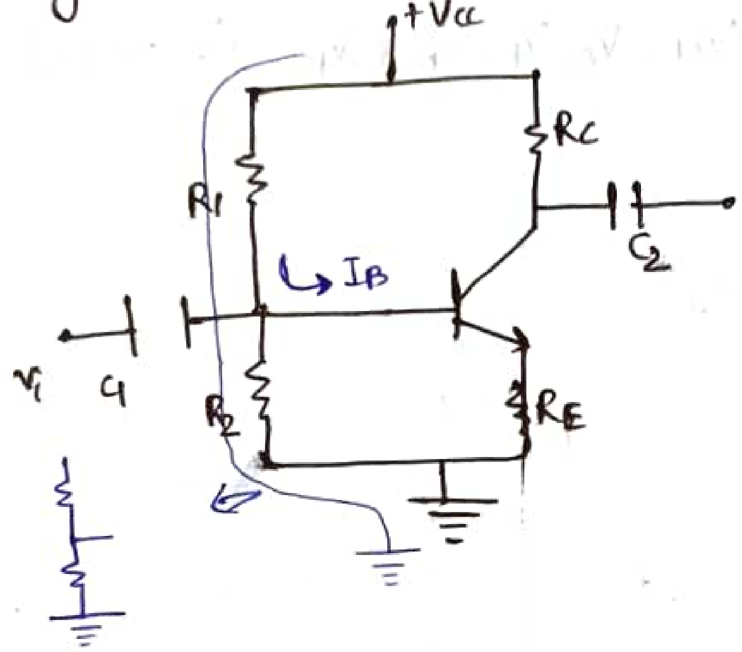
$V_{CE} = 0 \rightarrow I_C = \frac{V_{CC}}{R_C + R_E}$



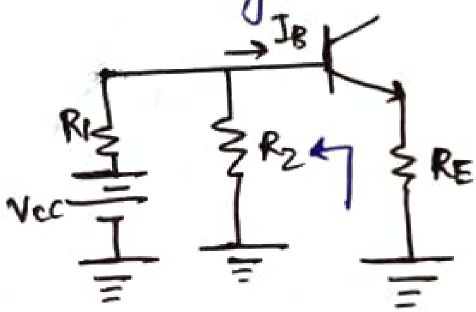
Q For the emitter base network, $R_B = 430\,k\Omega$, $R_C = 2\,k\Omega$; $\beta = 50$. $R_E = 1\,k\Omega$. Determine $I_B, I_C, V_{CE}, V_C, V_E, V_B$ & V_{BC}. ($V_{CC} = 20V$)



Voltage Divider Bias



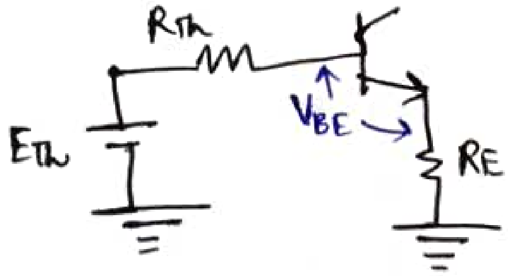
Exact Analysis:



$$R_{Th} = R_1 \,||\, R_2$$

$$R_{Th} = \frac{R_1 \cdot R_2}{R_1 + R_2}$$

$$E_{Th} = \frac{V_{cc} R_2}{R_1 + R_2}$$



$$E_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$$

Using $I_E = (\beta + 1) I_B$,

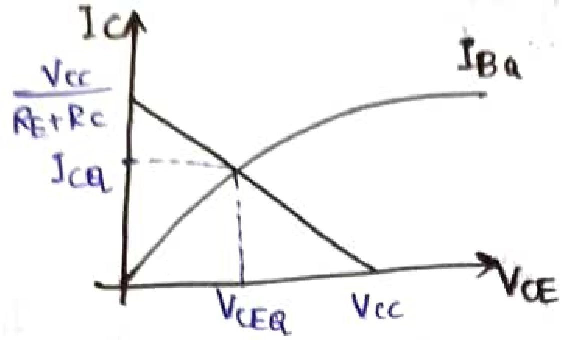
$$E_{Th} - I_B R_{Th} - V_{BE} - (\beta+1) I_B R_E = 0$$

$$\Rightarrow I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta+1) R_E}$$

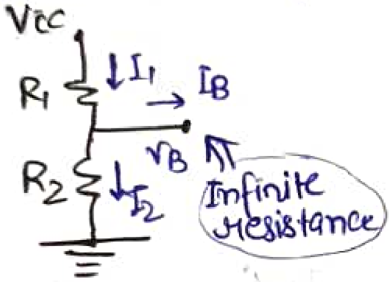
O/p :

$$V_{CC} - R_C I_C - V_{CE} - I_E R_E = 0$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E) \qquad (\because I_E \approx I_C)$$



Approximate: $\beta R_E \gg 10 R_2$



$$V_B = \frac{V_{CC} \cdot R_2}{R_1 + R_2}$$

$$I_C \approx I_E$$

$$V_E = I_E R_E$$

$$V_{BE} = V_B - V_E$$

$$V_E = V_B - V_{BE}$$

Q) Determine the operating point, dc bias voltage V_{CEQ} & I_{CQ} for $\beta = 100$. ($V_{CC} = 22V$, $R_1 = 39K\Omega$, $R_2 = 3.9K$, $R_E = 1.5K$, $R_C = 10K\Omega$)

Soln: $E_{Th} = \frac{V_{CC} R_2}{R_1 + R_2} = \frac{22(3.9)}{42.9} = 2V$

$(\because V_{BE} = 0.7V)$

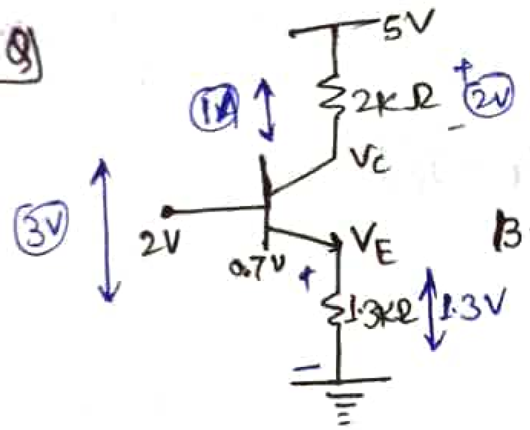
$$R_{Th} = \frac{R_1 R_2}{R_1 + R_2} = 3.54 K\Omega$$

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta+1) R_E} = \frac{2 - 0.7}{(3.54 + 101 * 1.5) \times 1000} = 8.38 \mu\Omega = I_{BQ}$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$
$$= 22 - (10K + 15K)(100)\, 8.38\,\mu$$
$$= 12.36 V$$
$$(\because I_C = I_{CQ} = \beta I_B)$$

27-04-2023

Q



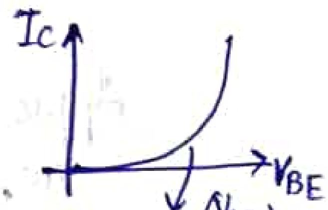
$V_{BE} = 0.7\,V$

$\beta \to$ very large

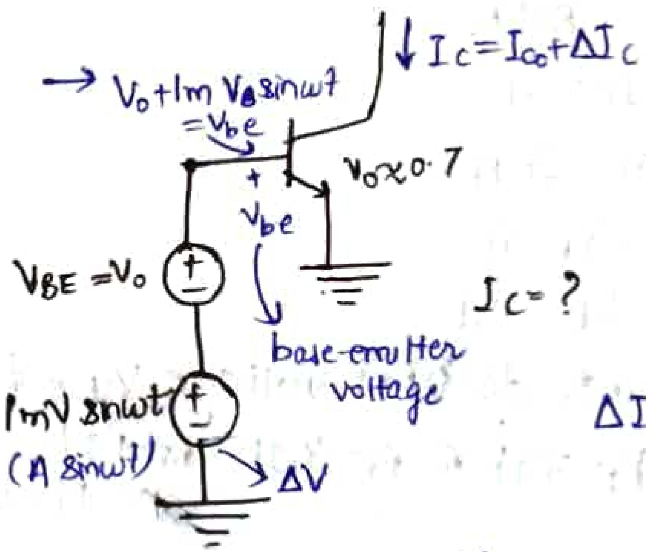
$V_C = ?\,;\ V_E = ?,\ I_C = ?$

Soln: $V_E = 2 - 0.7 = 1.3\,V$

$I_E = (1+\beta)\,I_B$

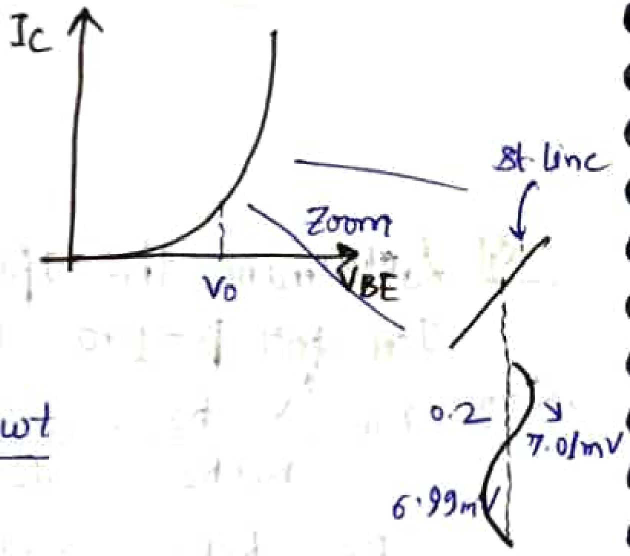


$I_S\, e^{\left(\frac{V_{BE}}{nV_T}\right)}$



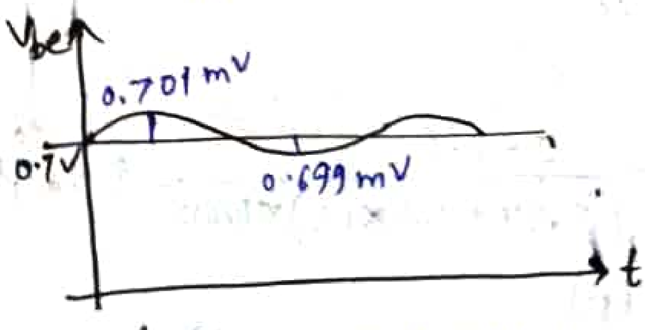
$I_C = ?$

$\Delta I_C = g_m \Delta V$



Small signal operation

$$I_C = I_S\, e^{\frac{V_{BE}}{nV_T}} = I_S\, e^{\frac{V_0 + 1m\,V \sin\omega t}{nV_T}}$$



$A \ll V_0 \rightsquigarrow$ small signal approx./operation

$$I_c = I_s e^{\left(\frac{V_0 + A\sin\omega t}{nV_T}\right)}$$

$$= \underbrace{I_s e^{\frac{V_0}{nV_T}}}_{\text{DC current flowing}} e^{\frac{A\sin\omega t}{nV_T}} = I_{co}\, e^{\underbrace{\frac{A\sin\omega t}{nV_T}}_{\text{small (arguments)}}} \approx I_{co}\left(1 + A\frac{\sin\omega t}{nV_T}\right)$$

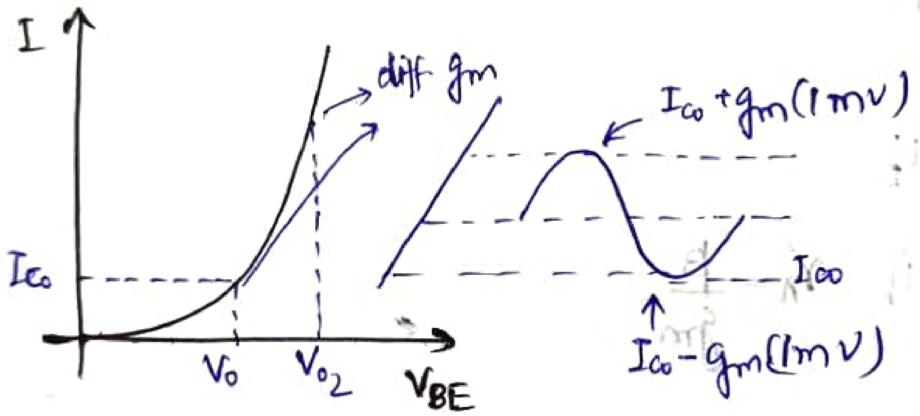
$$= I_{co} + \frac{I_{co}}{nV_t} A\sin\omega t$$

$G = \frac{I}{V}$ → conductance

$$= I_{co} + KA\sin\omega t, \quad K: \text{transconductance} \rightarrow g_m$$

$$= I_{co} + g_m A\sin\omega t$$

$V_0 = 0 \Rightarrow I_{co} = 0$



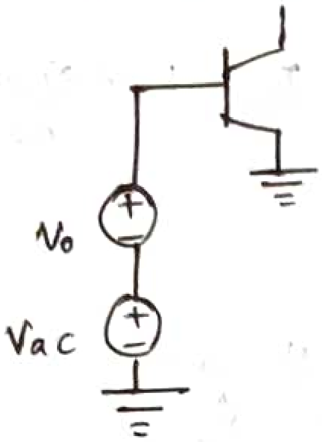
$$I_C = I_{co} + \Delta I_C$$

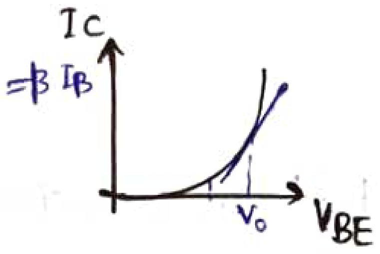
$$\Delta I_C = g_m \Delta V$$

$$g_m = \frac{I_{co}}{nV_T}$$

$$\frac{\Delta I_C}{\Delta V} = \frac{\partial I_C}{\partial V_{BE}} = \frac{1}{nV_T} I_s e^{\frac{V_{BE}}{nV_T}} = \frac{I_C}{nV_T} = g_m$$

$\rightarrow \quad V_B = V_0 + V_{ac}$





$|V_{ac}| \ll V_0$

$i_c = g_m v_{ac}$

$\Delta I_C = g_m \Delta V_{BE}$

$i_b = \frac{g_m V_{ac}}{\beta}$

$V_{ac} = \frac{\beta}{g_m} \cdot i_b$

$= r_\pi i_b, \quad r_\pi = \frac{\beta}{g_m}$

$V_{be} = r_\pi i_b$

$V_{be} = V_0 + V_{ac}$

$I_c = I_0 + i_{ac}$

Eg. $V_{BE} = 0.71\ V$

$I_C = ?$

$= g_m V_{BE} \rightarrow X$

$V_{be} = 0.71 + 0.01 \sin\omega t$

$I_c = 1mA = I_S e^{\left(\frac{V_{BE}}{nV_T}\right)}$

$g_m = \frac{I_C}{nV_T} = \frac{1mA}{25mV} = 40mS$

$\boxed{1-05-2023}$

Convention

DC $\rightarrow$ capital with ~~small~~ capital subscript (eg, I_B)

Small signal $\rightarrow$ small (ac) letter (with small subscript)
small perturbation around dc
(e.g., i_b)

Composite signal $\rightarrow$ capital with small subscript
(eg., I_b)
$\hookrightarrow$ total = DC + AC

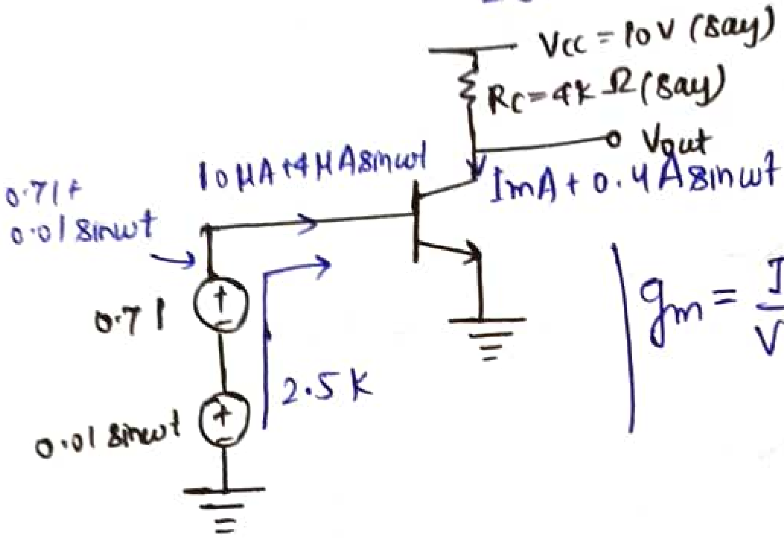
$$I_c = 1mA + \overbrace{g_m \times 0.01 \sin\omega t}^{\Delta I_c / I_c}$$

$$= 1mA + 0.04m \sin\omega t \ A$$

$$I_b = I_B + i_b$$

$$= 0.001mA + \frac{1}{r_\pi} V_{ac}$$

$$= 10\mu A + \frac{0.01}{2.5k} \sin\omega t$$



$$g_m = \frac{I_c}{V_T} = \frac{1mA}{25mV} = 0.04 \times 0.01 = 0.0004$$

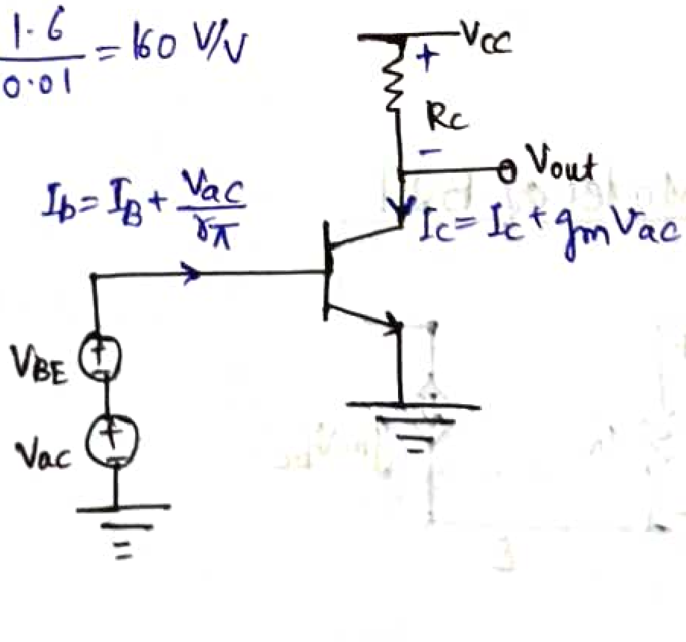
$$V_{out} = V_{cc} - I_c R_c$$

$$= 10V - (1mA + 0.4mA \sin\omega t)\, 4k\Omega$$

$$= 6V - 1.6 \sin\omega t$$

$V_c = V_{CE} = V_{out}$

$$V_{gain} = \frac{1.6}{0.01} = 160 \ V/V$$

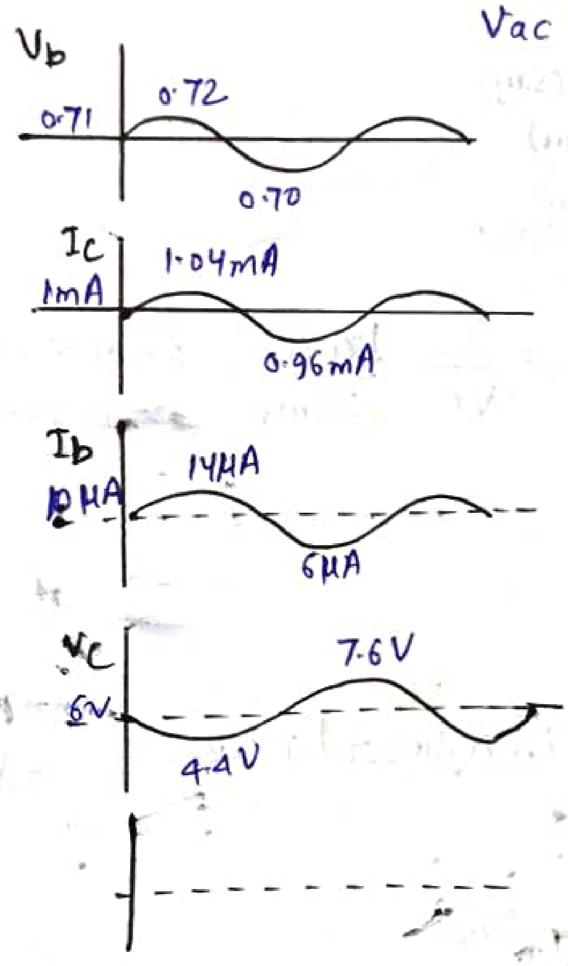


→ Common Emitter Amplifier

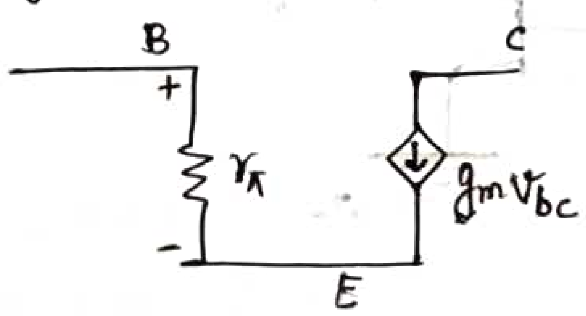
$$V_{out} = V_{cc} - I_C R_C$$
$$= V_{cc} - I_C R_C - g_m V_{ac} R_C$$

$$\text{Voltage gain} = \frac{\text{Small signal @ } V_{out}}{\text{Small signal @ i/p}}$$

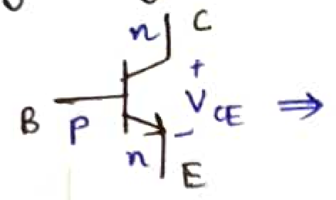
$$= \frac{-g_m V_{ac} R_C}{V_{ac}} = -g_m R_C$$



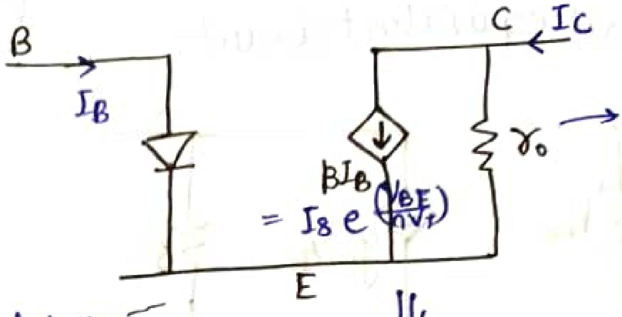
Small signal Model of BJT



Large Signal Model



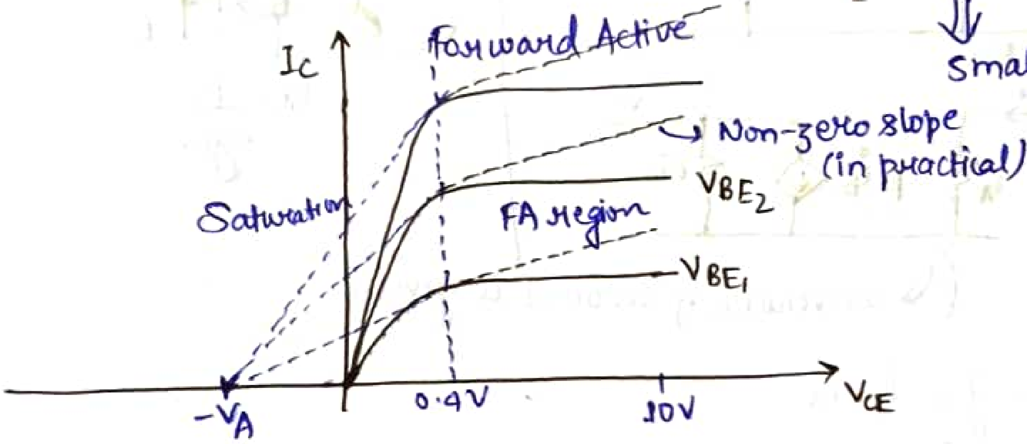
$\Rightarrow$



$r_o \rightarrow \left(\dfrac{\partial I_C}{\partial V_{CE}} \Big|_{V_{BE}} \right)^{-1} \approx \dfrac{|-V_A|}{I_C}$

$\Downarrow$

Small signal Model



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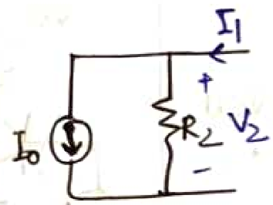

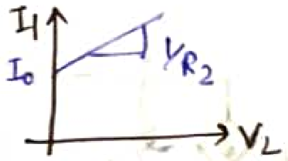

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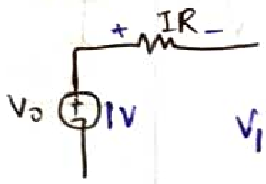


$V_1 = V_0 - IR$

V_A : Early voltage

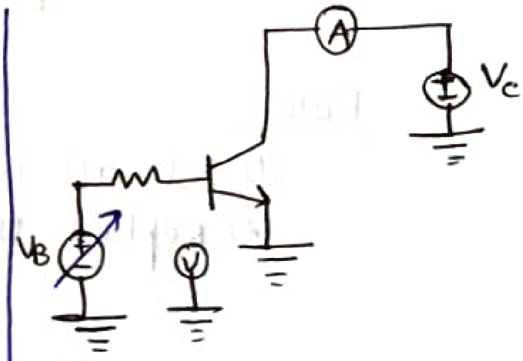
↳ gives a measure of the slope

→ slope ↓ ⇒ $|V_A|$ ↑

$$\frac{\partial I_C}{\partial V_{CE}} \Big| \approx \frac{I_C}{|-V_A| + V_{CE}} \approx \frac{I_C}{V_A}$$

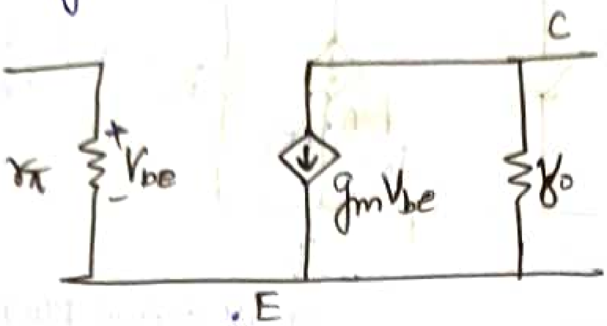
$$r_o = \left(\frac{\partial I_C}{\partial V_{CE}} \Big|_{V_{BE}} \right)^{-1} \approx \frac{|-V_A|}{I_C}$$

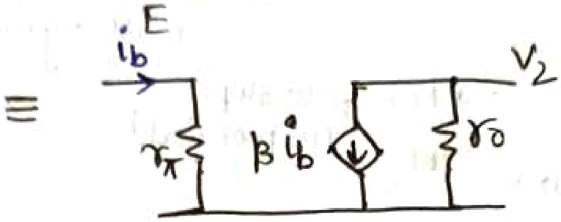
r_o ↓ output resistance

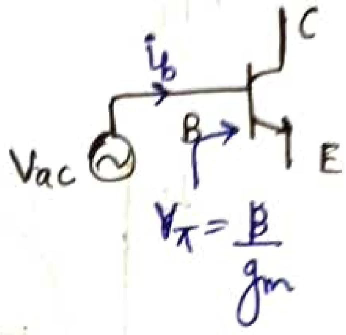


Small Signal Model $\rightsquigarrow$ doesn't work for dc

Small signal equivalent circuit:



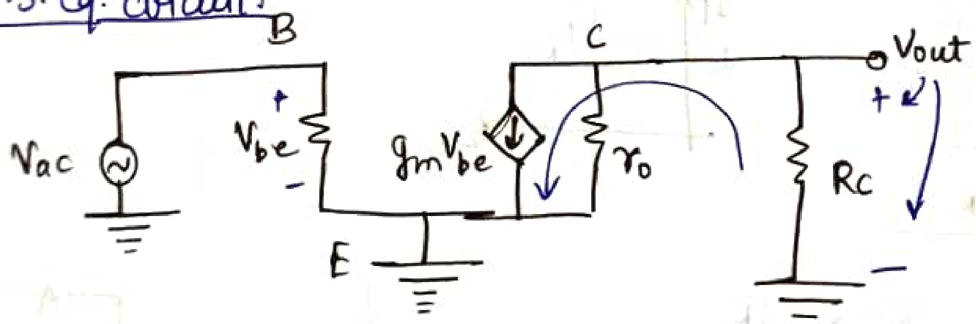


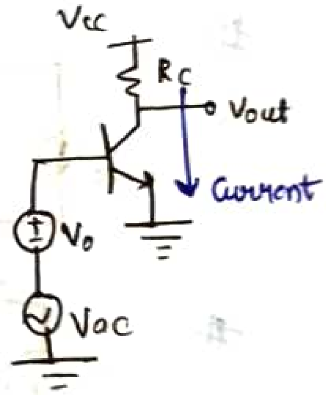


(↳ convenient, if current is given)

$$g_m \cdot V_{be} = g_m \cdot i_b \cdot r_\pi$$
$$= \beta i_b$$

S.S. eq. circuit:

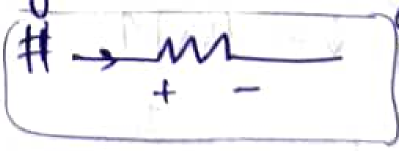




Rules:

1. Set all DC sources = 0
2. Replace transistor with S.S. model

DC voltage sources → AC grounds



Voltage gain $= \frac{V_{out}}{V_{in}}$

$$V_{out} = -g_m V_{be} (r_o \parallel R_C)$$

$$V_{be} = V_{ac} = V_{in}$$

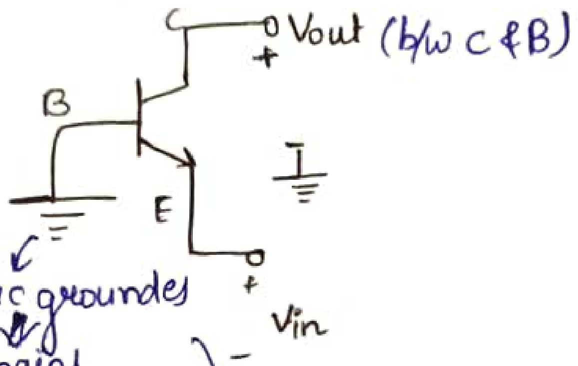
$$\therefore V_{out} = -g_m V_{in} (r_o \parallel R_C)$$

$$\text{Gain} = \frac{V_{out}}{V_{in}} = -g_m (r_o \parallel R_C) = -g_m R_C$$

$r_0 \sim 40-80\,k\Omega$

$R_C \sim 5\,k\Omega$

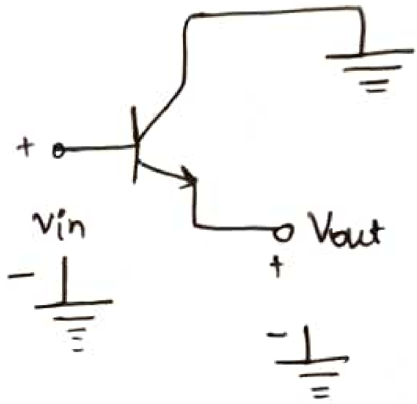
Common Base



ac groundes

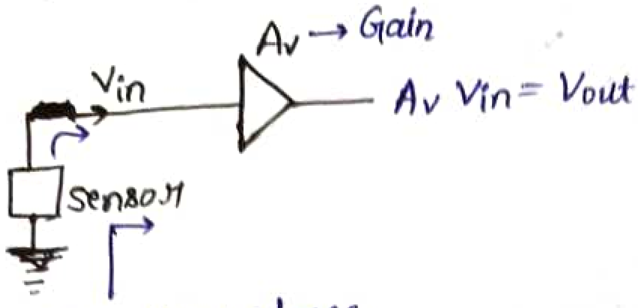
remains unresponsive to ac signal

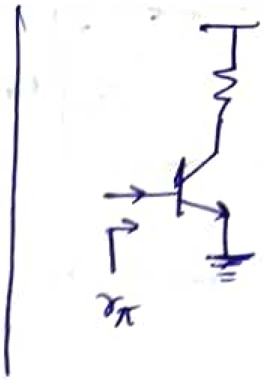
Common Collector



15-05-2023

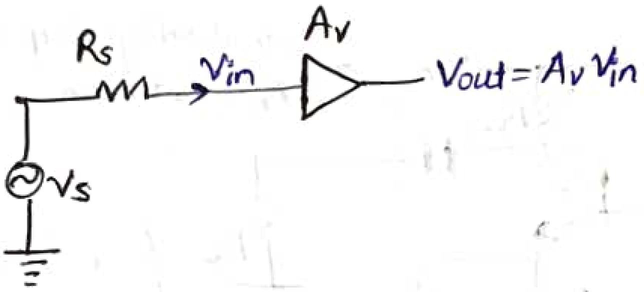
Voltage Amplifier

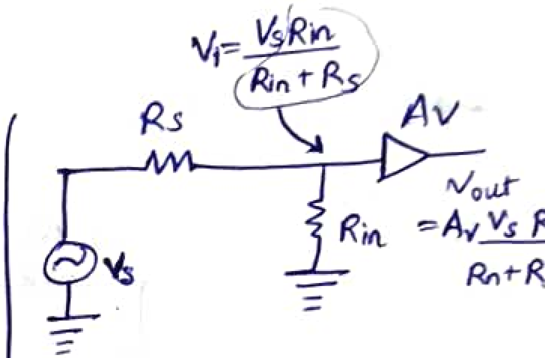


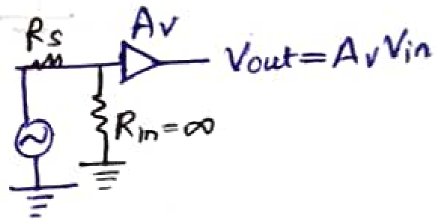


Input impedence
(R_{in})

↓
Reduced to



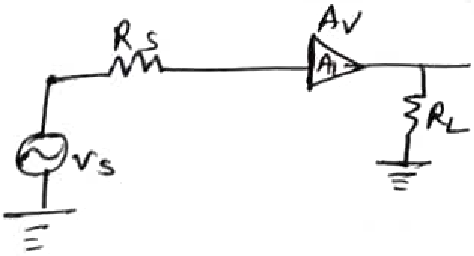


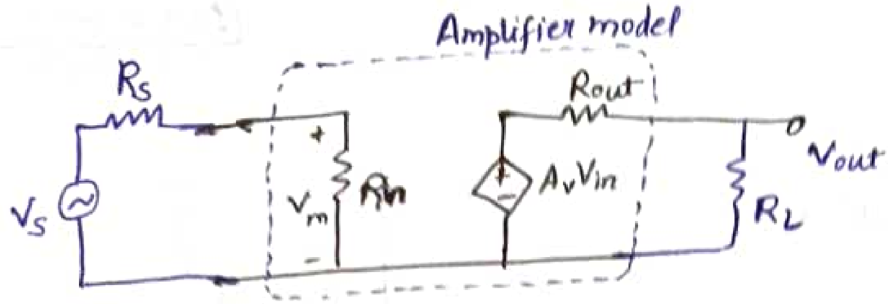


Ideally $R_{in} \rightarrow \infty$

$$r_\pi = R_{in} = \frac{\beta}{g_m}$$

Characteristics (we look for):
- Gain
- Input Impedence

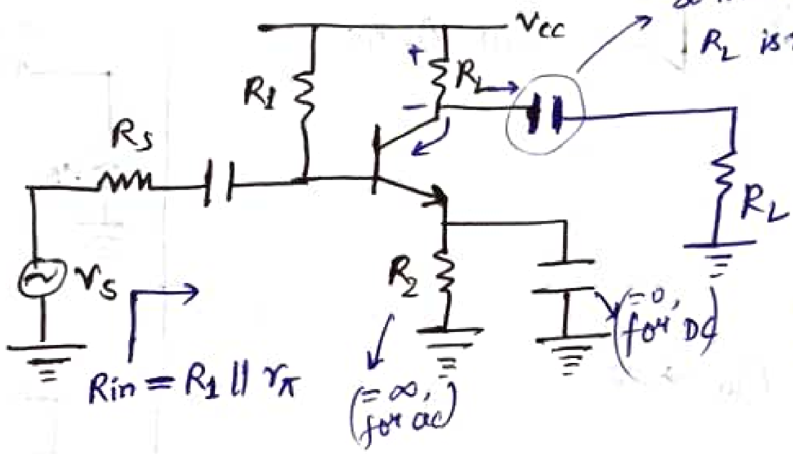




$$V_{out} = V_s \cdot \frac{R_{in}}{R_{in}+R_s} \cdot A_V \cdot \frac{R_L}{R_L+R_{out}}$$

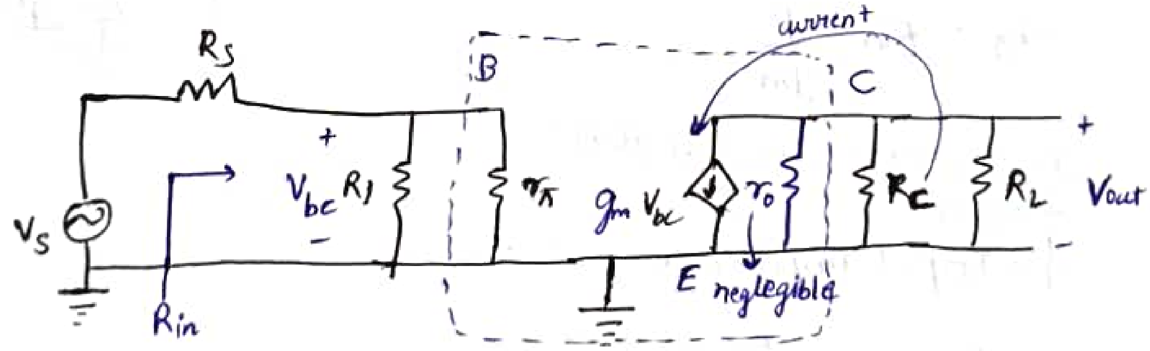
$$G_V = \frac{V_{out}}{V_s}$$

→



so that voltage drop across R_L is not much

① set all DC = 0
② All cap ⇒ short



~~Vout~~

$$G_V = \frac{V_{out}}{V_s}$$

$$R_{in} = R_1 \parallel r_\pi$$

$$V_{be} = V_s \frac{R_1 \parallel r_\pi}{R_s + R_1 \parallel r_\pi}$$

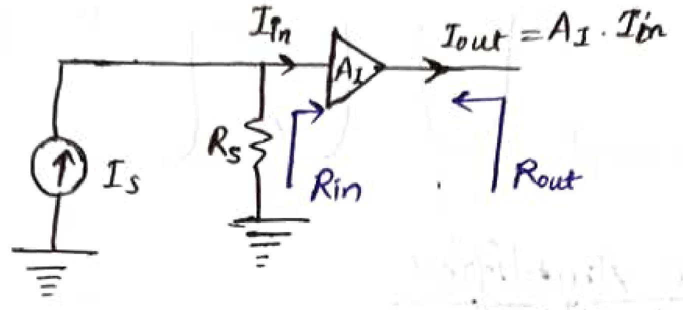
$$V_{out} = -V_s \cdot \frac{R_1 \parallel r_\pi}{R_1 \parallel r_\pi + R_s} \cdot g_m \overbrace{\left(R_c \parallel R_L \parallel r_o\right)}^{\simeq (R_c \parallel R_L)}$$

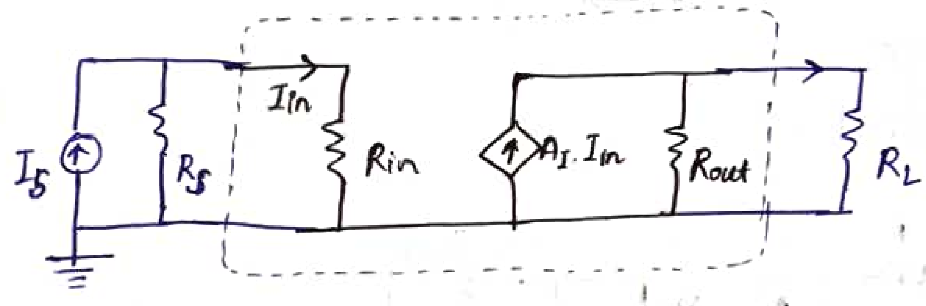
$(r_o >> R_c \parallel R_L)$

$$G_V = -\frac{R_1 \parallel r_\pi}{R_1 \parallel r_\pi + R_S} \cdot g_m (R_C \parallel R_L)$$

Datasheet of BC547 transistor

Current Amplifiers → Current In Current Out





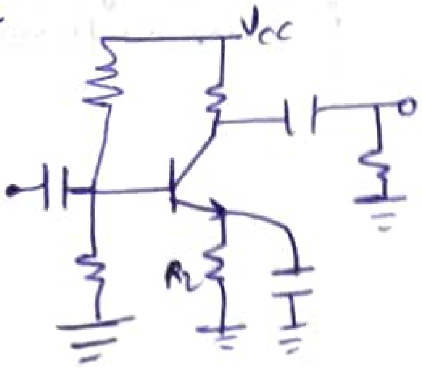
Ideal $R_{in} = 0$

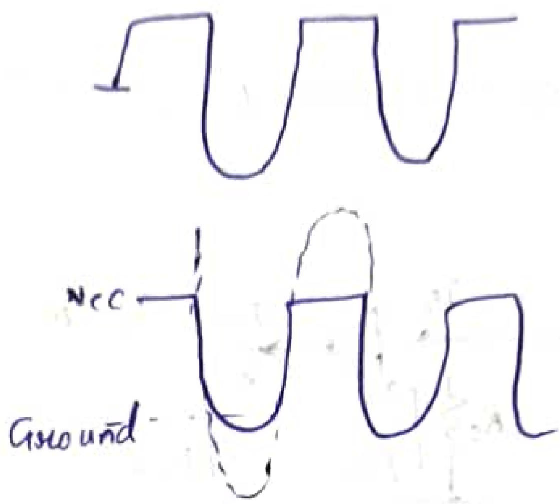
Ideal $R_{out} \to \infty$.

$$I_{out} = I_S \cdot \frac{R_S}{R_S + R_{in}} \cdot A_I \cdot \frac{R_{out}}{R_{out} + R_S}$$

18-05-23

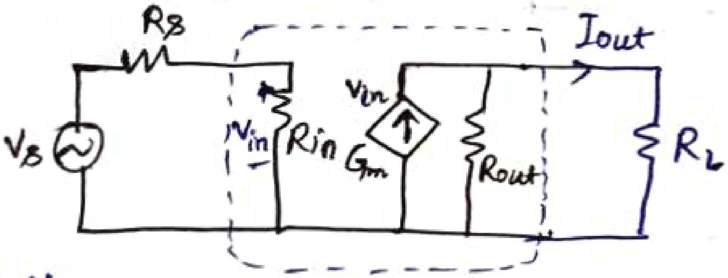
#





Transconductance Amplifier

I/p : voltage
O/p : current



Ideally,

$R_{in} = \infty$

$R_{out} = \infty$

$$G_m' = \frac{I_{out}}{V_s} = \frac{R_{in}}{R_{in}+R_s} \cdot G_m \cdot \frac{R_{out}}{R_{out}+R_L}$$

effective/overall transconductance (of the system)

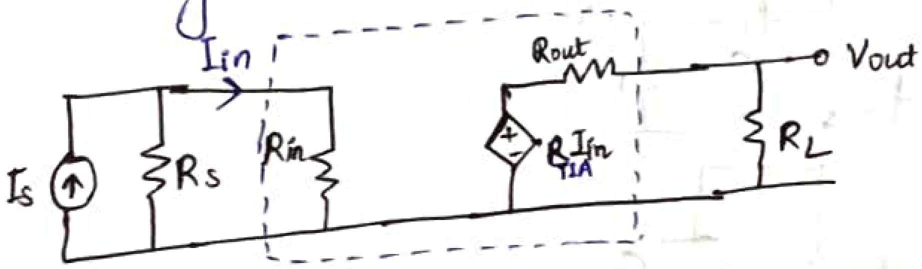
$$I_{out} = G_m V_{in} \frac{R_{out}}{R_{out}+R_L}$$

$$V_{in} = V_s \cdot \frac{R_{in}}{R_{in}+R_s}$$

Transimpedence (TIA) / Transresistance Amplifier

Input : current

Output : voltage



Ideally,

$R_{in} = 0$

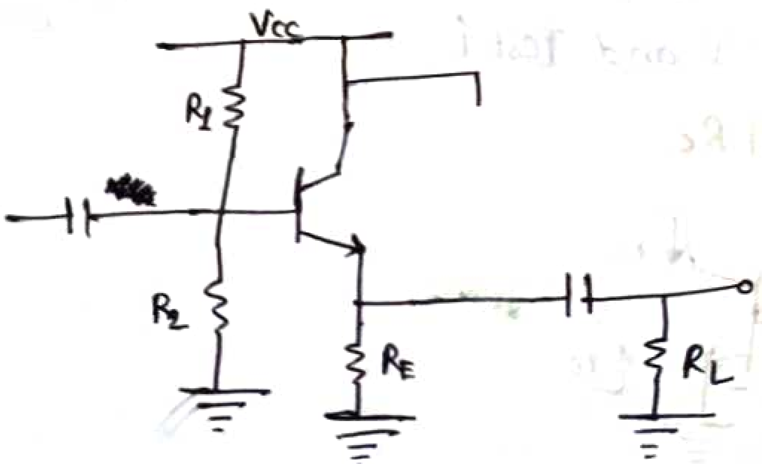
$R_{out} = 0$

$$\underbrace{R_T}_{\text{overall transimpedence}} = \frac{V_{out}}{I_s} = \frac{R_s}{R_s + R_{in}} \cdot R_{TIA} \cdot \frac{R_L}{R_L + R_{out}}$$

$$I_{in} = \frac{R_s}{R_s + R_{in}} \cdot I_s$$

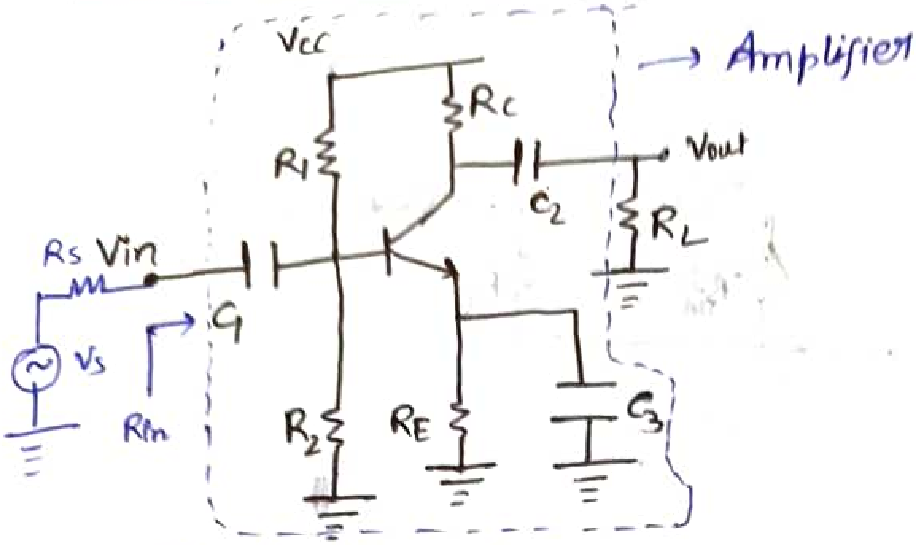
$$V_{out} = R_{TIA} \cdot I_{in} \cdot \frac{R_L}{R_L + R_{out}}$$

Common Collector Amplifier



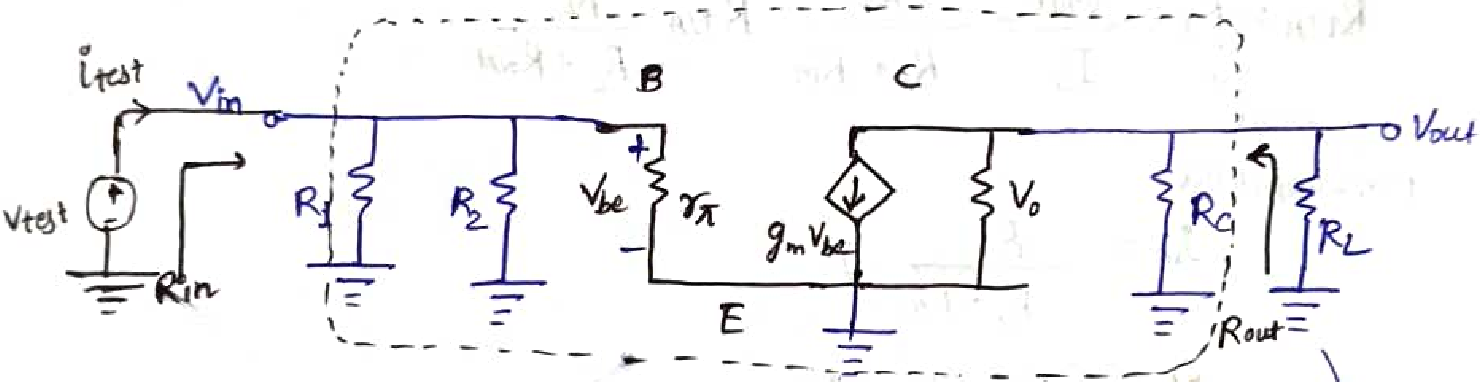
22-05-2023

Common Emitter Amplifier

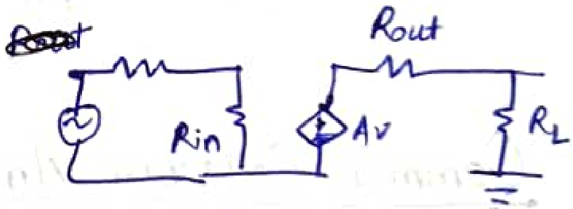


① set all DC=0

② All capacitors short circuit



$$R_{in} = R_1 \parallel R_2 \parallel r_\pi = \frac{V_{test}}{i_{test}}$$



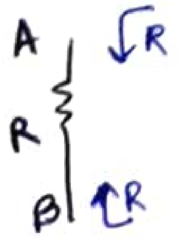
$$A_V = g_m (r_o \parallel R_L)$$

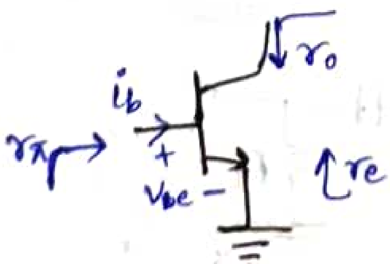
For calculating Rout,

① set $V_{in} = 0$

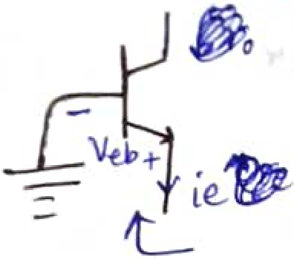
② Test V and test i.

$$R_{out} = r_o \parallel R_C$$





$$R_{in} = \frac{V_{be}}{i_b} = r_\pi = \frac{\beta}{g_m}$$



$$R_{in,E} = \frac{V_{eb}}{-i_e} = \frac{V_{be}}{i_e}$$

$$R_{in,E} = \frac{V_{be}}{i_e} = \frac{V_{be}}{(\beta+1)i_b} = \frac{r_\pi}{\beta+1} = \frac{\beta}{g_m(\beta+1)} = \frac{\alpha}{g_m} = r_e$$

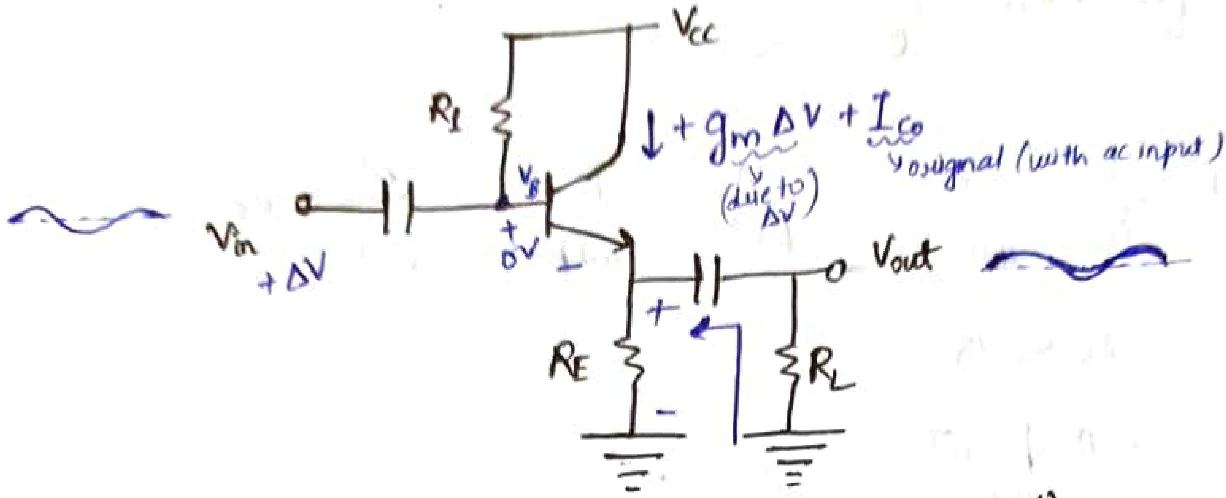
$$r_e \ll r_\pi$$

$I_c = 1mA$, $\beta = 100$

$r_\pi = 2.5\,k\Omega$

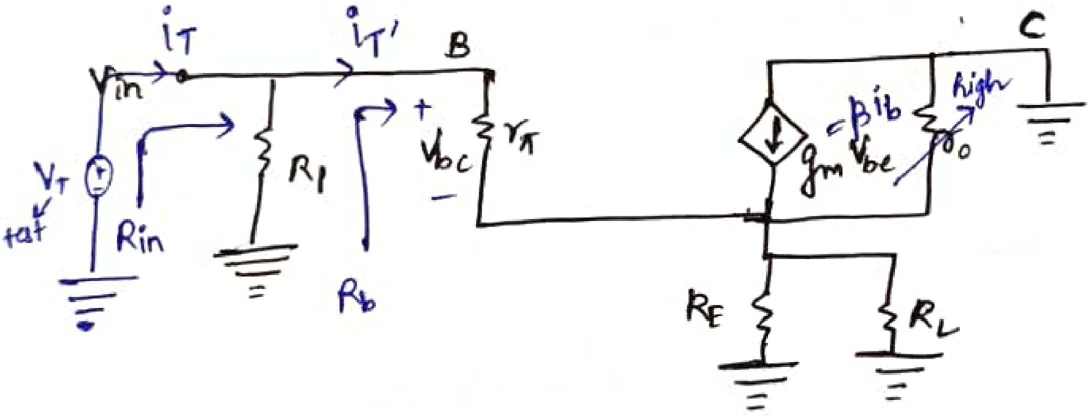
$r_e = 24.7\,\Omega$

Common Collector Amplifier → Emitter follower



$$V_E = \underbrace{(I_{co} + I_{Bo})R_E}_{\text{(original) DC}} + \underbrace{\left(g_m \Delta V + \frac{\Delta V}{r_\pi}\right) R_E}_{AC}$$

$$\frac{V_{out}}{V_{in}} \approx \frac{g_m R_E}{1 + g_m R_E} \approx 1.$$



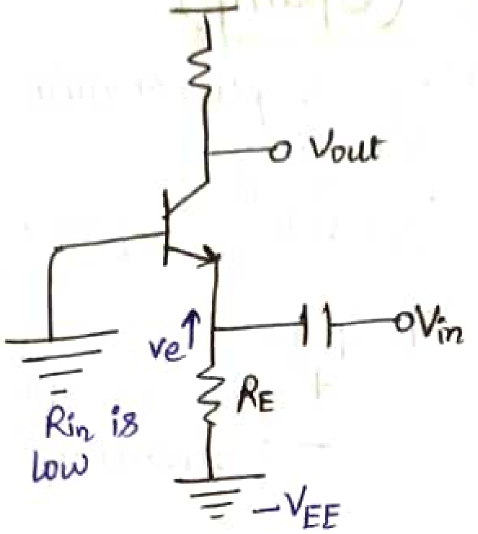
$$R_{in} = R_1 \parallel R_b$$

$$R_b = \frac{V_T}{i_T} = \frac{i_b r_\pi + (\beta+1) i_b (R_E \parallel R_L)}{i_b}$$

$$= r_\pi + \underbrace{(\beta+1)}_{V_{in} \text{ magnified by}} (R_E \parallel R_L)$$

25-05-23

CB



r_e

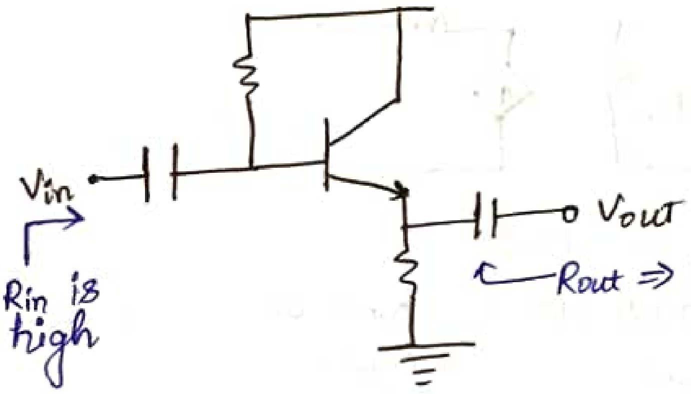
$\frac{V_{be}}{i_b}$

$-\frac{V_{eb}}{i_e}$

$$= \frac{V_{be}}{r_e} = \frac{V_{be}}{(\beta+1)i_b} = \frac{r_\pi}{\beta+1}$$

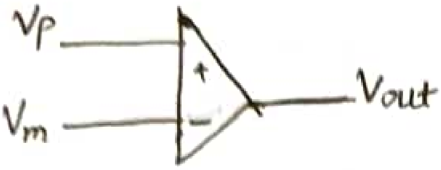
$$= \frac{\beta}{g_m(\beta+1)} = \frac{\alpha}{g_m}$$

CC



Rout $\Rightarrow r_e = \frac{\alpha}{g_m}$

OPERATIONAL AMPLIFIER (Opamp)



└ Voltage amplifier with very high gain
(i/p: voltage, o/p: voltage)

Opamps:
gain: ~10^5–10^6
LM 741
OP07

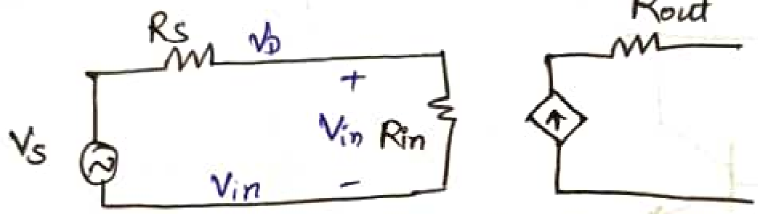
$V_{out} = A(V_p - V_m)$, A: gain (opamp gain)

$A \to \infty$

+ : Non-inverting terminal
− : Inverting terminal

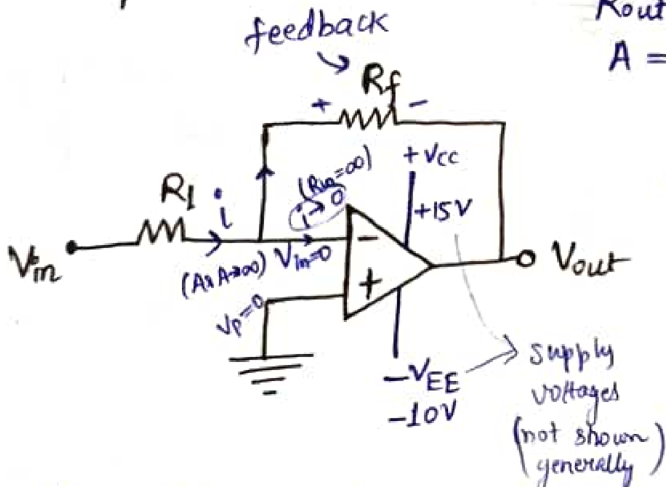
$R_{in} = \infty$

$R_{out} = 0$.



For $V_s = V_{in}$, $R_{in} \to \infty$

→ Ideal Opamp behaviour : $R_{in} = \infty$
$R_{out} = 0$
$A = \infty$



→ Inverting Amplifier

$V_{out} = A(V_p - V_m)$

$\Rightarrow \frac{V_{out}}{A} = V_p - V_m$

If $A \to \infty$ $V_p - V_m = 0$

$\Rightarrow \boxed{V_p = V_m}$ → (Acts as if there is short circuit b/w ⊕ & ⊖ terminals) (not really)

"Virtual short"

"virtual ground"

| Generally, $A \sim 10^5$

$$i = \frac{V_{in}}{R_1}$$

$$iR_F = V_{in} \cdot \frac{R_F}{R_1}$$

$$V_{out} = -iR_F = -V_{in} \cdot \frac{R_F}{R_1}$$

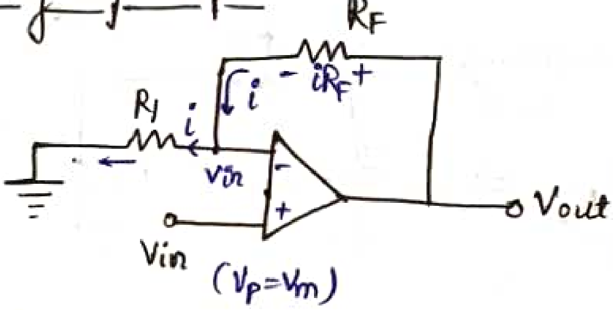
$$A_I = \frac{V_{out}}{V_{in}} = -\frac{R_F}{R_1}$$ ⇝ Gain of the circuit

→ Putting opamp in a circuit, gain reduces (can be manipulated)

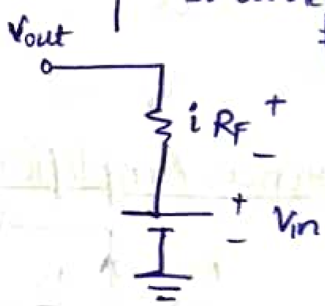
circuit gain (not opamp gain anymore)

Non-Inverting Opamp

(2-06-23)



current cannot come from opamp, so current comes from o/p.



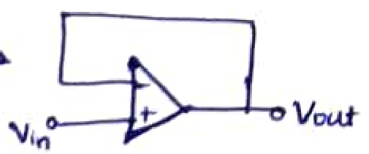
$$V_{out} = A(V_p - V_m)$$

$$i = \frac{V_{in}}{R_1}$$

$$V_{out} = iR_F + V_{in}$$

$$= \frac{V_{in}}{R_1} R_F + V_{in}$$

$$\Rightarrow \frac{V_{out}}{V_{in}} = 1 + \frac{R_F}{R_1}$$

→ 

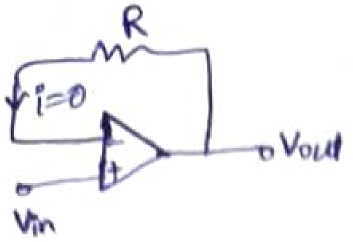
$\Rightarrow V_{out} = V_{in}$

Mathematical Proof: $V_{out} = A(V_p - V_m)$

$$= A(V_{in} - V_{out})$$

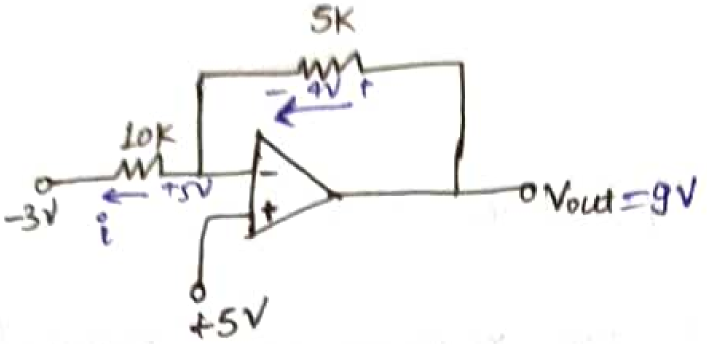
$$\Rightarrow V_{out}(1 + A) = AV_{in}$$

$$\Rightarrow \frac{V_{out}}{V_{in}} = \frac{A}{1+A} \Rightarrow \text{As } A \to \infty,\ \frac{V_{out}}{V_{in}} = 1.$$

→ 

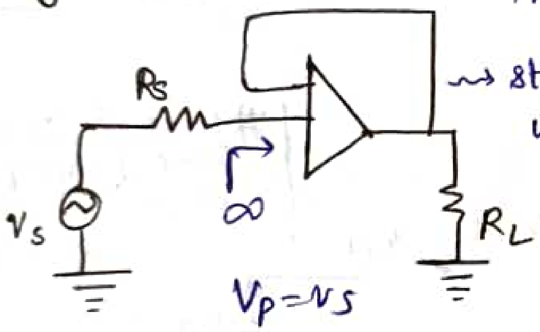
$\Rightarrow V_{out} = V_{in}$

Eg.



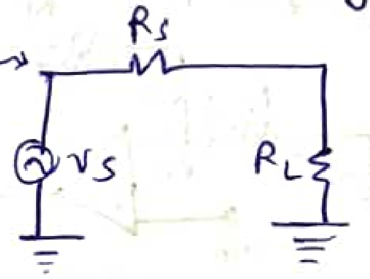
$$i = \frac{5-(-3)}{10K} = 0.8\,mA$$

→ Unity Gain Buffer: Bufferble when i/p & o/p cannot be directly connected b/c of voltage drop.



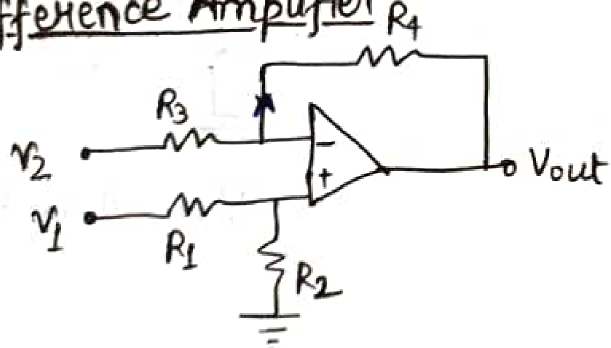
⇝ straight wire ⇝

⇒



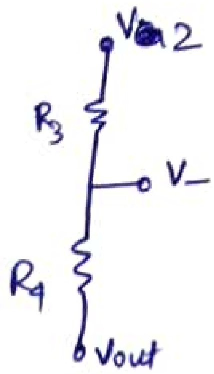
$$\frac{R_L}{R_S+R_L} \cdot V_S$$

Eg. Difference Amplifier



$$V_+ = V_1 \cdot \frac{R_2}{R_1+R_2} = V_{in}$$

$$V_{out} = K(V_1 - V_2)$$



$$i = \frac{V_2 - V_{out}}{R_3+R_4}$$

$$V_- = V_2 - iR_3$$

$$= V_2 - \frac{V_2 - V_{out}}{R_3+R_4} \cdot R_3 = \frac{V_2 R_4 + R_3 V_{out}}{R_3+R_4}$$

$$\Rightarrow V_1 \cdot \frac{R_2}{R_1+R_2} = \frac{V_2 R_4 + V_{out} R_3}{R_3 + R_4}$$

$$\Rightarrow V_{out} = \frac{R_3+R_4}{R_3}\left(\frac{V_1 R_2}{R_1+R_2} - \frac{R_4 V_2}{R_3+R_4}\right)$$

If $\frac{R_1}{R_2} = \frac{R_3}{R_4}$ (Assumption)

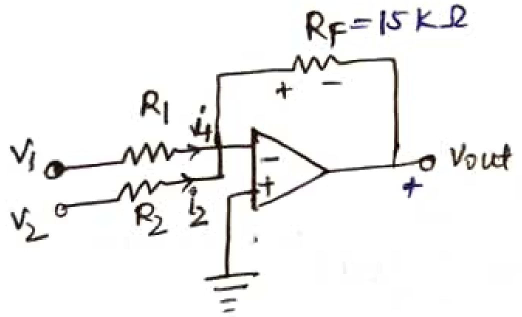
$$\Rightarrow V_{out} = K(V_1 - V_2)$$

Summing Amplifier

In electronics, adding current is far easier than adding voltage.

Adding current $\Downarrow$ in parallel

Adding voltage $\Downarrow$ in series



$i_1 = \frac{V_1}{R_1}$

$i_2 = \frac{V_2}{R_2}$

$i = i_1 + i_2$

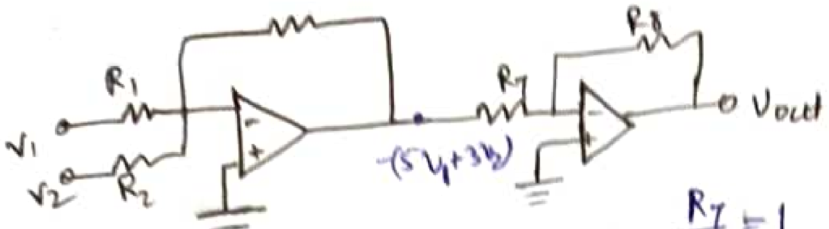
$$V_{out} = -iR_F$$
$$= -\left(V_1 \cdot \frac{R_F}{R_1} + V_2 \frac{R_F}{R_2}\right)$$

$R_1 = 3k \quad R_2 = 5k$

$V_{out} = -(5V_1 + 3V_2)$ $\rightsquigarrow$ inverting summation

For getting non-inverting summation:

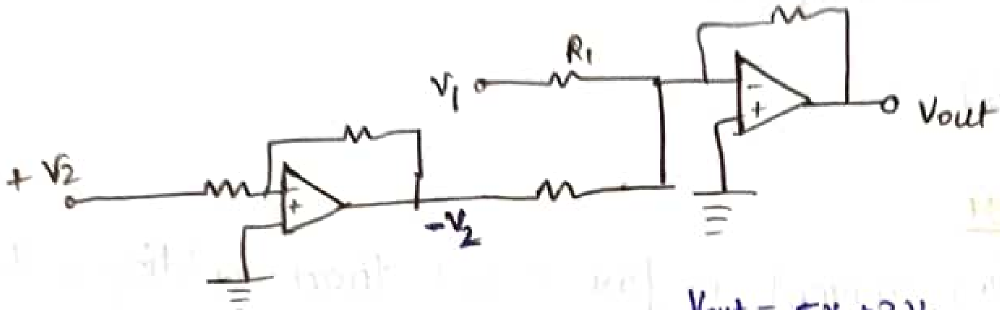
- One way: Take $V_1 = -V_1$, $V_2 = -V_2$.
- Other way: Add one inverting opamp.
- Third way: Add an opamp to V_2.



$5V_1 - 3V_2$

$\frac{R_7}{R_8} = 1$

$V_{out} = 5V_1 + 3V_2$

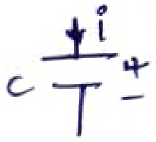


$V_{out} = 5V_1 + 3V_2$

Integrators

R, D, C, L, opamp, V, I

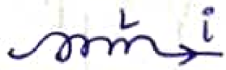
$i = C\frac{dv}{dt}$

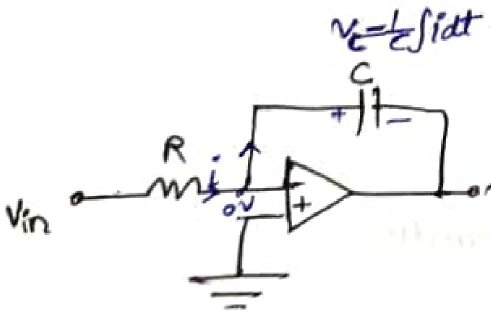


$\Rightarrow V = \frac{1}{C}\int i\,dt$

$V = L\frac{di}{dt}$

$\Rightarrow i = \frac{1}{L}\int v\,dt$





$V_{out} = -V_c$

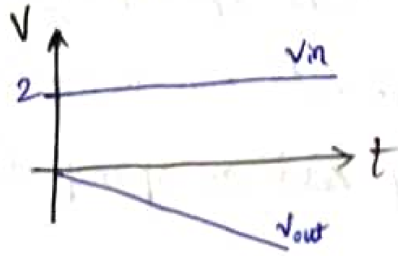
$= -\frac{1}{C}\int i\,dt = -\frac{1}{C}\int \frac{V_{in}}{R}dt$

$= -\frac{1}{RC}\int V_{in}\,dt$

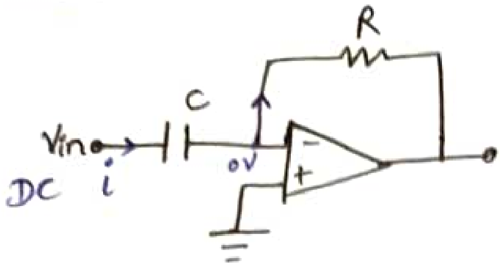
$i = C\frac{dv}{dt}$
constant | time-varying

$V_{in} = 2V$ (say)

$\therefore V_{out} = -\frac{1}{RC}\cdot 2 \cdot t$



Differentiator



$V_{out} = -RC\dfrac{dV_{in}}{dt}$

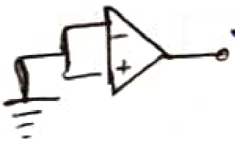
$i = C\dfrac{dV_{in}}{dt}$

Ideal Opamp

① Gain $= \infty$

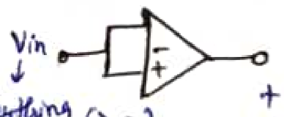
② Input impedence, $R_{in} = \infty$

③ Input offset voltage

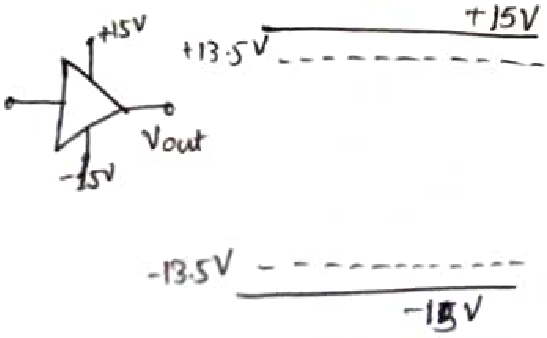


$\rightarrow A \times (V_p - V_m) = 0$

$(\because V_p = V_m)$

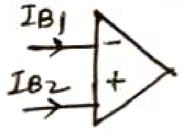


④ Voltage & current limitation
↳ output



Practical Opamp

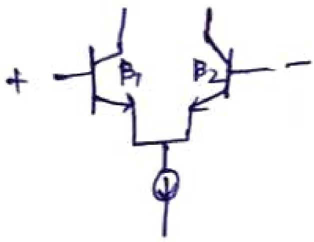
① Gain = very high.

② 

$I_{B_1}, I_{B_2} \neq 0$ ⇝ very low

↓

Input bias current

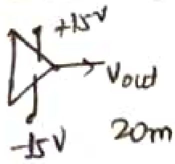


I_{B_1}, I_{B_2} ⇝ random
($I_{B_1} \geq I_{B_2}$ or $I_{B_1} \leq I_{B_2}$).

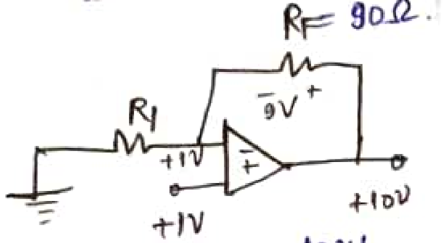
- $I_{B_1} \neq I_{B_2}$
- $\Delta I_B = |I_{B_1} - I_{B_2}|$
  ↳ Input bias offset current
- $I_B = \dfrac{I_{B_1} + I_{B_2}}{2}$
  ↳ Input bias current
- $I_{B_1}, I_{B_2} \rightarrow$ have input bias current drift w/ temp (temp. dependent).

↳ I/p bias offset current temp.
↳ I/p bias offset current drif.

Current limitation :



20mA



$I = 0.1A$

10 V/V

$$\frac{R_F}{R_1} = 9 = \frac{9k}{1k} = \frac{900}{100} = \frac{90}{10} = \frac{9}{1}.$$

(say)

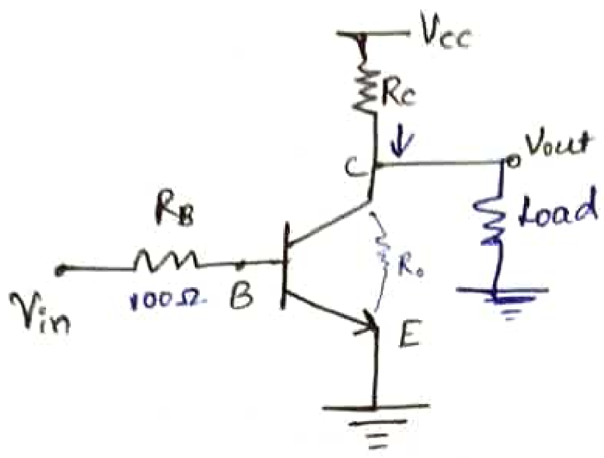
$9K = 1mA$

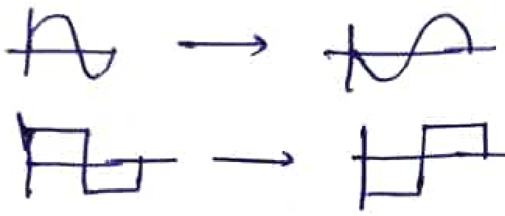
$90\Omega = 0.1\,A$

DIGITAL ELECTRONICS

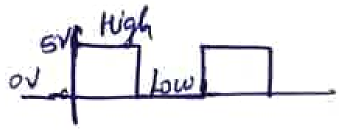
08-06-2023

CE Transistor

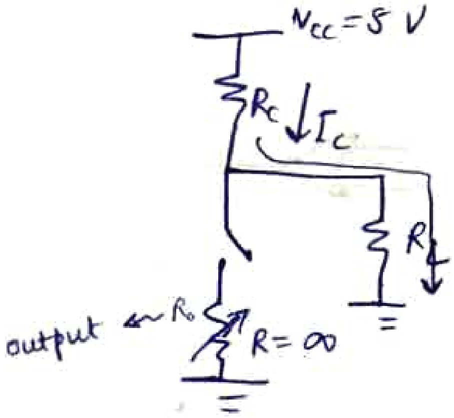




→ Inverting (NOT GATE)



For $V_{in} = 0V$ ⇝ Equivalent transistor model: open ~~short~~-circuit.

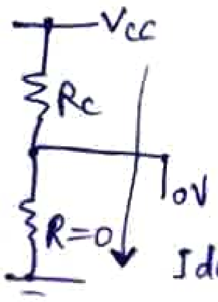


Switch regions:

cut off, saturation

↓ off, ↓ on

For V_{in} → high: Model : short-circuit.



Ideally $V = 0$

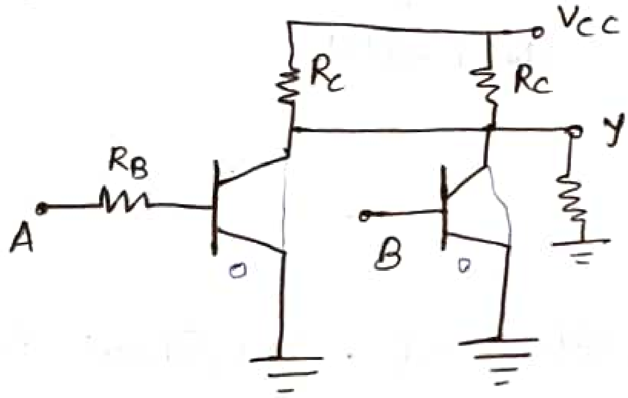
Practically, $V \neq 0$ ⇝ very low ≈ 0.01 V

NOT GATE:

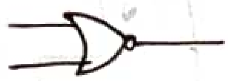
Truth Table:

Input	Output
0	1
1	0

NOR GATE:



A	B	y
0	0	1
0	1	0
1	0	0
1	1	0



12-06-2023

Logic Gates

NOT $y=\overline{A}$

AND $y=A\cdot B$

OR $y=A+B$

NAND $Y=\overline{A\cdot B}$

NOR $y=\overline{A+B}$

EXOR $A\oplus B=\overline{A}B+A\overline{B}$

EXNOR $A\odot B=AB+\overline{A}\,\overline{B}$

Boolean Algebra

$B=\{A,B\}$ $\{+,\circ\}$

$\downarrow$ Boolean element

$\downarrow$ Operators

$\{0,1\}$

$\downarrow$ Boolean values

Truth Table:

A	Y
0	1
1	0

→ Inverted

	A	B	Y
$\overline{A}\,\overline{B}$	0	0	0
$\overline{A}B$	0	1	0
$A\overline{B}$	1	0	0
AB	1	1	1

$n=2$,

2^n ⇝ total no. of combination

Eg. MSB LSB (Least Significant Bit)

0 0

2^1 2^0

$0\times 2^1 + 0\times 2^0 = 0$

0 1

2^1 2^0 $\rightarrow x = 0\times 2^1 + 1\times 2^0$

$x = 1$

1 0

2^1 2^0 $\rightarrow 1\times 2^1 + 0\times 2^0$

$= 2$

1 1

2^1 2^0 $\rightarrow 2+1 = 3$

Eg. 3 to binary

$$\begin{array}{r|l} 2 & 3 \\ \hline 2 & 2 - 1 \\ \hline & 1 \end{array} \rightarrow 1\ 1$$

→ Boolean algebra satisfies Closure $(0+1=1)$ property.

A	B	Y_{AND} $(A\cdot B)$	Y_{OR} $(A+B)$	Y_{NAND} $(\overline{A\cdot B})$	Y_{NOR} $(\overline{A+B})$	Y_{EXOR} $(\bar{A}B + A\bar{B})$	Y_{EXNOR} $(AB + \bar{A}\bar{B})$
0	0	0	0	1	1	0	1
0	1	0	1	0	0	1	0
1	0	0	1	0	0	1	0
1	1	1	1	0	0	0	1

Symbols

NOT:

AND:

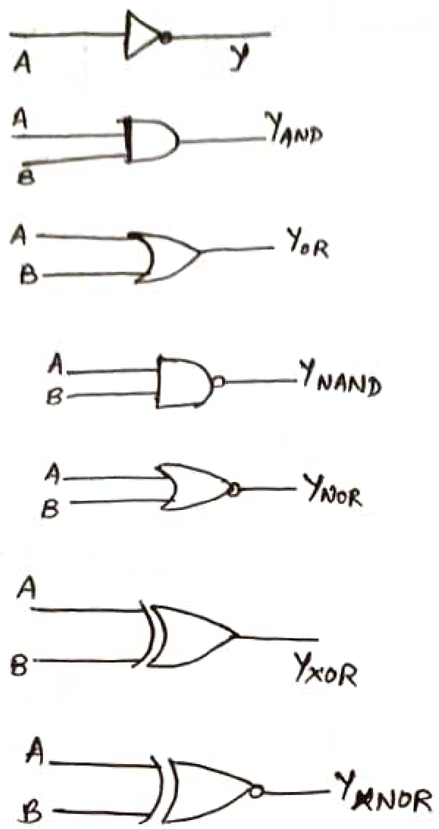
OR:

NAND:

NOR:

XOR:

XNOR:



$$\begin{array}{r|l} 2 & 7 \\ \hline 2 & 3-1 \\ \hline & 1-1 \end{array} \quad 111$$

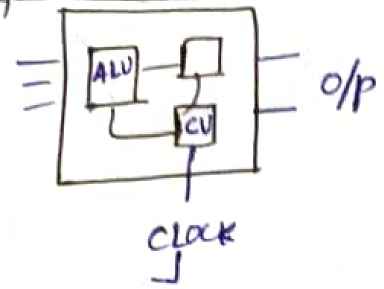
$$\begin{array}{r|l} 2 & 6 \\ \hline 2 & 3-0 \\ \hline & 1-1 \end{array} \quad 110$$

3-inputs NAND

	A	B	C	Y_{AND} $(A.B.C)$	Y_{NAND} $(\overline{A \cdot B.C})$	Y_{OR} $(A+B+C)$	Y_{NOR} $(\overline{A+B+C})$
0	0	0	0	0	1	0	1
1	0	0	1	0	1	1	0
2	0	1	0	0	1	1	0
3	0	1	1	0	1	1	0
4	1	0	0	0	1	1	0
5	1	0	1	0	1	1	0
6	1	1	0	0	1	1	0
7	1	1	1	1	0	1	0

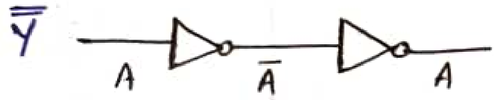
→ NAND & NOR Gates → Universal Gates
↳ can be derived any gates from these two.

Computer Architecture:



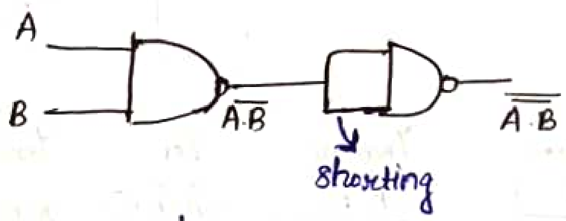
- In memory = on chip
  fast

AND from NAND:



$Y = A\,B$

$Y = \bar{\bar{Y}} = \overline{\overline{AB}}$



↳ 2 NANDs required

15-06-2023

BOOLEAN ALGEBRA

$\{0, 1\}$

$\{+, \cdot\}$

Axioms:

$+ \qquad \cdot \qquad -$

$X + 0 = X \qquad X \cdot 1 = X$

$X + 1 = 1 \qquad X \cdot 0 = 0$

$\boxed{X + \overline{X} = 1} \qquad X \cdot \overline{X} = 0$

$X + X = X \qquad X \cdot X = X$

$\overline{\overline{X}} = X$

Duality of $+ \rightarrow \cdot$
Duality of $0 \rightarrow 1$

$X + Y = Y + X, \quad XY = YX$ ... Commutative property

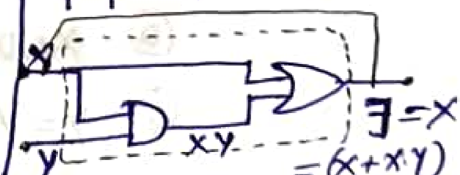
$X + (Y + Z) = (X + Y) + Z$ ... Associative property

$X + (Y \cdot Z) = (X + Y) \cdot (X + Z)$ ... Distributive property

$X \cdot (Y + Z) = X \cdot Y + X \cdot Z$

$F = X + X \cdot Y = X$

X	Y	$(X \cdot Y)$	$F = (X + X \cdot Y) = X$
0	0	0	0
0	1	0	0
1	0	0	1
1	1	1	1



De Morgan's laws:

(I) $\overline{X + Y} = \overline{X} \cdot \overline{Y}$

(II) $\overline{X \cdot Y} = \overline{X} + \overline{Y}$

For 3-inputs:

$\overline{X + Y + Z} = \overline{X} \cdot \overline{Y} \cdot \overline{Z}$

$\overline{X \cdot Y \cdot Z} = \overline{X} + \overline{Y} + \overline{Z}$

Consensus theorem

Q) $\boxed{xy + x'z + yz = xy + x'z}$. Prove this, and write its duality.

Soln: $xy + \bar{x}z + yz$

$= xy + \bar{x}z + yz(x+\bar{x})$

$= xy + \bar{x}z + yzx + yz\bar{x}$

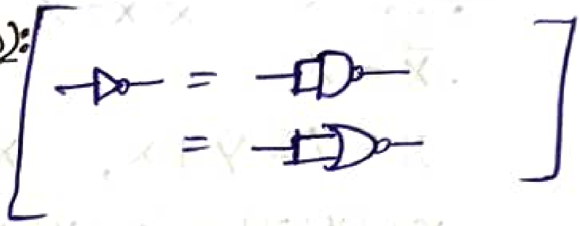
$= x[y + yz] + \bar{x}[z + yz]$

$= xy + \bar{x}z$

Duality: $(x+y).(\bar{x}+z).(y+z) = (x+y).(\bar{x}+z)$

NAND Implementation

→ EXOR implementation (using NAND):

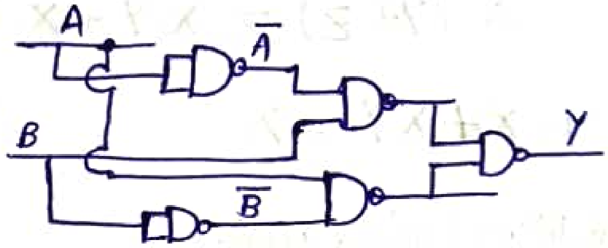


$Y = A\bar{B} + \bar{A}B$

$\bar{\bar{Y}} = \overline{\overline{\underbrace{A\bar{B}}_{X} + \underbrace{\bar{A}B}_{Y}}}$

$\Rightarrow Y = \underbrace{\overline{\overline{A\bar{B}} \cdot \overline{\bar{A}B}}}_{NAND}$

$[\overline{X+Y} = \bar{X}\cdot\bar{Y}$ ... De Morgan's law$]$



→ NAND Implementation of:

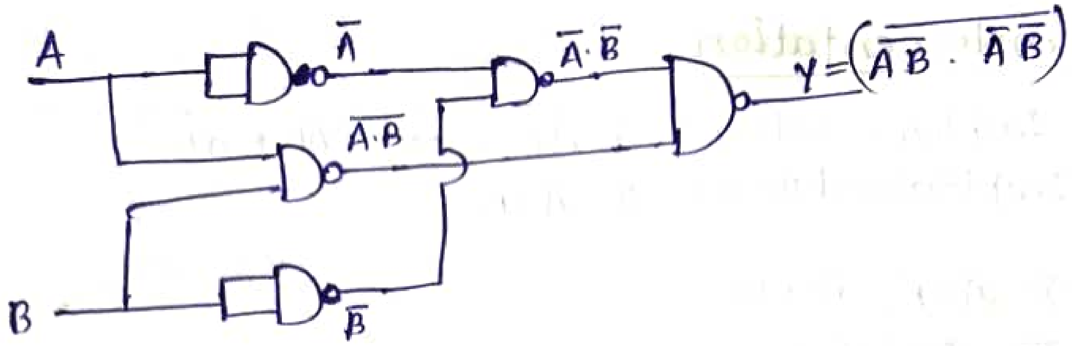
(a) XNOR: $A \odot B = (A+\bar{B}).(\bar{A}+B)$ or $(A\cdot B + \bar{A}\cdot\bar{B})$

(b) $Y = A\bar{B}C + \bar{A}B\bar{C} + ABC$

(a) $Y = A\cdot B + \bar{A}\cdot\bar{B}$

$Y = \bar{\bar{Y}} = \overline{\overline{A\cdot B + \bar{A}\cdot\bar{B}}}$

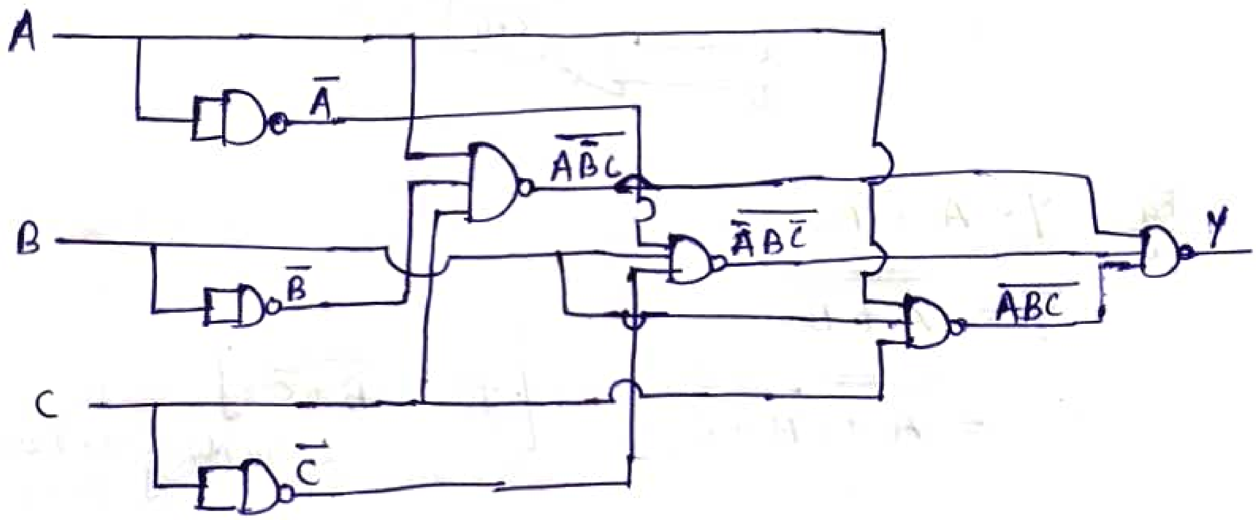
$= \overline{\overline{(A\cdot B)}.\overline{(\bar{A}.\bar{B})}}$



(B) $Y = A\bar{B}C + \bar{A}B\bar{C} + ABC$

$Y = \bar{\bar{Y}} = \overline{\overline{A\bar{B}C + \bar{A}B\bar{C} + ABC}}$

$= \overline{(\overline{A\bar{B}C}).(\overline{\bar{A}B\bar{C}}).(\overline{ABC})}$



NOR Implementation

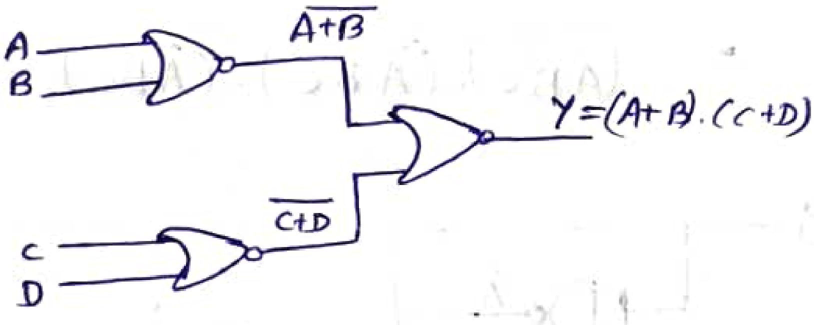
NAND Implementation : $Y = \overline{AB}$ Eg → $Y = (\bar{A}B + A\bar{B})$

NOR Implementation : $Y = \overline{A+B}$

Eg $Y = (A+B).(C+D)$

$$Y = \overline{\overline{Y}} = \overline{\overline{(A+B).(C+D)}}$$

$$= \overline{\overline{(A+B)} + \overline{(C+D)}}$$

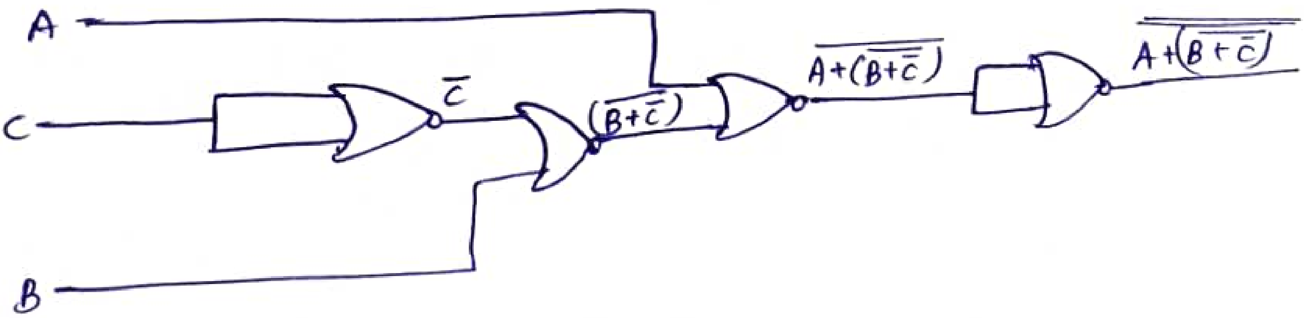


Eg $Y = A + \bar{B}C$

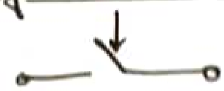
$$\overline{\overline{Y}} = \overline{\overline{A + \bar{B}C}}$$

$$= \overline{\overline{A + \overline{(B+\bar{C})}}} \quad [\because \bar{B}C = \overline{B+\bar{C}}]$$

↳ De Morgan's Law

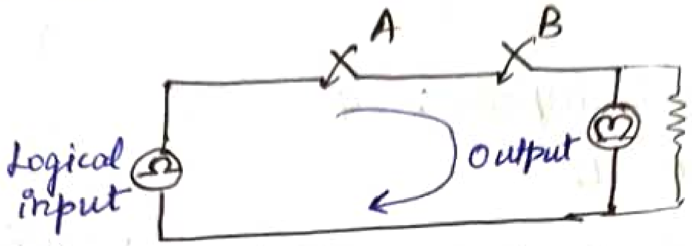


Types of Connections:



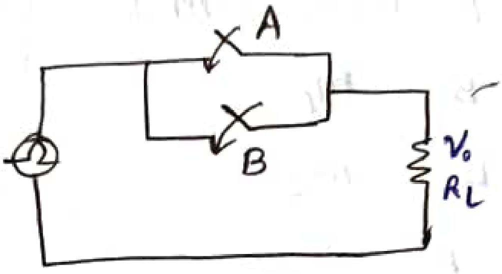
① Series $\xrightarrow{\text{Analogous to}}$ AND $(A \cdot B)$

② Parallel $\longrightarrow$ OR $(A+B)$

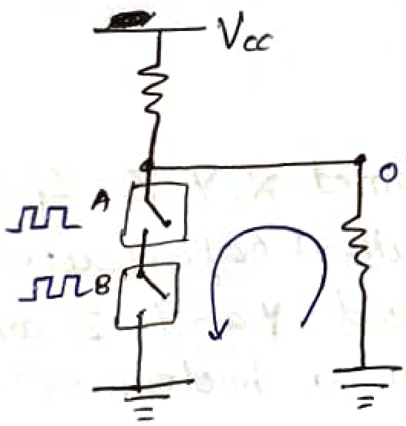


Analogy:

$\rightarrow$ Series – AND

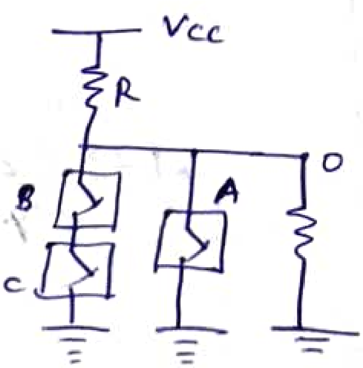


$\rightarrow$ Parallel – OR



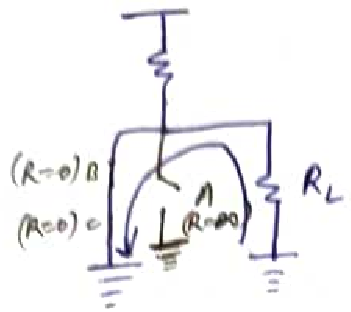
A	B	O/P
0	0	1
0	1	1
1	0	1
1	1	0

Eg. Implement $Y=\overline{A+BC}$ using switches.



A	B	C	BC	A+BC	$\overline{A+BC}$
0	0	0	0	0	1
0	0	1	0	0	1
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	1	0
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	1	1	0

Equivalent circuit for input (0 1 1):



→ Possible combination for 2 inputs : 4

Decimal eqⁿ	Digital	A	B	
0	0 0	A′	B′	Minterms (m_0)
1	0 1	A′	B	m_1
2	1 0	A	B′	m_2
3	1 1	A	B	m_3

$F = A'B + AB'$
$m_1 \quad m_2$

$F = A'B' + A'B + AB' + AB$

Eg. 3 doors are there in a room, named X, Y, Z. If X is open, Y and Z are in any combinations (open/closed), output is equal to 1. If X is closed, Y and Z are in any state, output is zero. Obtain a boolean eqⁿ.

Soln:

X	Y	Z	Output
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

Open = 0
Closed = 1

$F = \underbrace{X'Y'Z'}_{m_0} + X'Y'Z + X'YZ' + X'YZ$

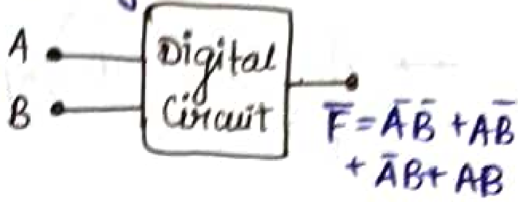
→ If minterm is $x'y'z'$, its maxterm is its duality
$M_0 = x + y + z$.

→ Any boolean expression /digital logic can be implemented using
Sum of product, $F = A'B' + A'B + AB' + AB$ (Min term)
and, Product of sum, $F = (A+B)(A+B')(A'+B)(A'+B')$ (Max term)
i.e., using AND and OR gates, or NAND and NOR
(which are easier to fabricate).

22-06-2019

→ For any circuit with two inputs, the output F will be
$F = \bar{A}\bar{B} + A\bar{B} + \bar{A}B + AB$. (~~OR~~ AND followed by OR)

Any circuit's output can be expressed in terms of 'min-terms' as "sum of products" (SOP).



Eg., XOR ⇒ $F = \bar{A}B + \bar{B}A$

Here, $\bar{A}B$ & $\bar{B}A$ min-terms are involved in the output.

~~For the~~

Minterms (Product)			Maxterms	
A	B			
$\bar{A}\cdot\bar{B}$	m_0		$\bar{A}+\bar{B}$	M_0
$A\cdot\bar{B}$	m_1		$\bar{A}+B$	M_1
$\bar{A}\cdot B$	m_2		$A+\bar{B}$	M_2
$A\cdot B$	m_3		$\bar{A}+\bar{B}$	M_3

$m_j = \overline{M_j}$

Maxterms:

Again consider $XOR = A\bar{B} + \bar{A}B$

$$\overline{XOR} = \overline{A\bar{B} + \bar{A}B} = (\overline{A\bar{B}}).(\overline{\bar{A}B})$$
$$= (\bar{A}+B).(A+\bar{B})$$

Here, OR and AND are required along with NOT (OR followed by AND). "Product of sums" (POS)

We obtain complement of the output that we obtained in case of min-terms.

Adder : logical sum

(A) Half Adder

↳ 2 bits

	A	B	SUM	CARRY
$\bar{A}\bar{B}$	0	0	0	0
$\bar{A}B$	0	1	1	0
$A\bar{B}$	1	0	1	0
AB	1	1	0	1

SUM, CARRY hold only one bit.

$\rightarrow 1+1=2$ (Decimal) $\Rightarrow 10$ (Binary): 1 = carry, 0 = sum

For SUM = 1

SUM: $A \oplus B = A\bar{B} + \bar{A}B = A \oplus B$ ← XOR gate (from minterms)

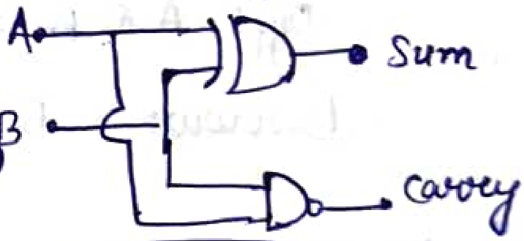
$\overline{SUM}$: $= (A+\bar{B})(\bar{A}+B)$ ~~(from maxterms)~~

For SUM = 0

$\overline{SUM} = \bar{A}\bar{B} + AB$

$SUM = (A+B) \cdot (\bar{A}+\bar{B})$ (from maxterms)

XOR gate



$CARRY = A \cdot B \Rightarrow \overline{CARRY} = \bar{A}+\bar{B} = \overline{AB}$ (from minterms)

$\overline{CARRY} = \bar{A}\bar{B} + \bar{A}B + A\bar{B}$ (from maxterms)

$\Rightarrow CARRY = (A+B) \cdot (A+\bar{B}) \cdot (\bar{A}+B)$

minterm	maxterm
$\bar{A}\bar{B}$ $\longrightarrow$	$A+B$

(B) Full Adder

↳ 3-bit adder

↳ 2 bits at a term + 1-bit of carry from previous addition

A	B	C ← previous carry	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

~~Sum = $\bar{A}\bar{B}C + \bar{A}BC$~~

$SUM = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC = A \oplus B \oplus C$

XNOR: $\bar{B}\bar{C} + BC = \overline{B\oplus C}$

$\overline{SUM} = \bar{A}\bar{B}\bar{C} + \bar{A}BC + A\bar{B}C + AB\bar{C} \Rightarrow$ Sum $= \bar{A}(B\oplus C) + A(\overline{B\oplus C})$

$\Rightarrow \boxed{Sum = A\oplus(B\oplus C) \text{ or } (A\oplus B)\oplus C}$ → XOR gates

$CARRY = \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$

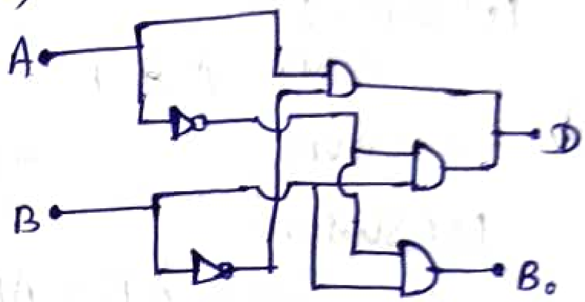
$\overline{CARRY} = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C}$

$\Rightarrow \boxed{carry = C(A\oplus B) + AB}$

Subtractor

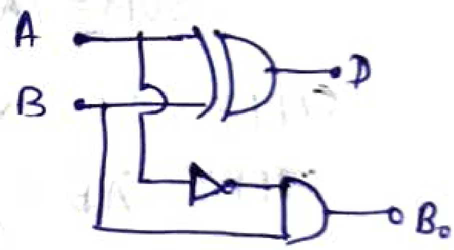
(A) Half Subtractor

A	B	D (Diff)	Borrowout (B_o)
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0



Diff: $A \oplus B = \bar{A}B + A\bar{B} = D$ (min-terms)

Borrow: $B_o = \bar{A}B$ (min-terms)



(B) Full subtractor : 3bit (A-B-C)

↳ 2 bits with one borrow

A	B	C (borrow)	D	B_o
0	0	0	0	0
0	0	1	1	1
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

$D = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$

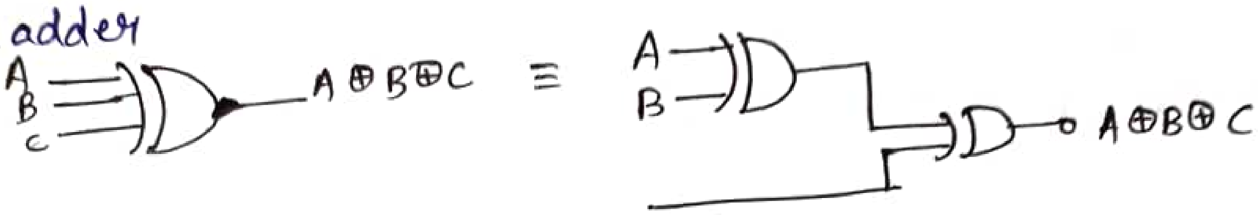
$D = \bar{B}(\bar{A}C + A\bar{C}) + B(\bar{A}\bar{C} + AC)$

$= \bar{B}(\bar{A}C + A\bar{C}) + B(\overline{\bar{A}C + C\bar{A}})$

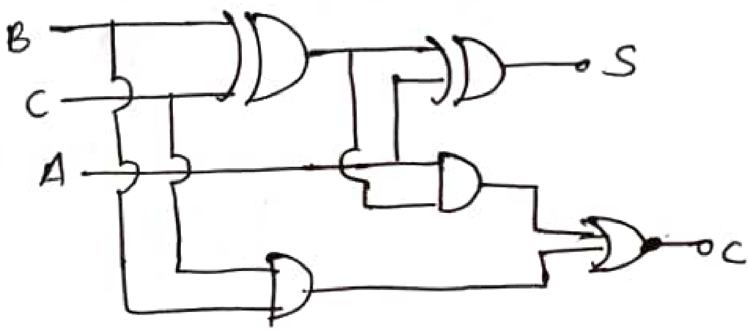
$\Rightarrow \boxed{D = A \oplus B \oplus C}$

$B_0 = \bar{A}\bar{B}C + \bar{A}BC + ABC$

→ Full adder



→ Full adder with carry



2 half adder + 1 OR gate
↓
S & C of full adder

Binary Representation of Negative Numbers

(A) Signed Representation

Negative number is represented as 1.

Most significant Bit is used to represent sign, if it is signed number.

8-bit is std. representation

Eg., +9 in 8 bits is 0 0 0 0 1 0 0 1

-9 in 8 bits is $\underbrace{1}_{\text{sign}}\ \underbrace{0\,0\,0\,1\,0\,0\,1}_{\text{Magnitude (7-bits)}}$

↓

Not followed nowadays.

(B) Complement Representation

(a) 1's complement representation (Diminished Radix):

Eg., +9 : 0 0 0 0 1 0 0 1

Take complement of each bit,

-9 : 1 1 1 1 0 1 1 0

As it is 1 ⇒ ⊖ve

(b) 2's complement Radix :

→ First take the complement.

→ Then, add 1.

→ Start moving from LSB towards MSB. Keep the bits same until first 1 is encountered.

→ Thereafter take the complement of bits.

Eg., 9 : 0 0 0 0 1 0 0 1

-9 : 1 1 1 1 0 1 1 0 → taken compliment

+1 → added 1

1 1 1 1 0 1 1 1

$\underbrace{1\,1\,1\,1\,0\,1\,1}_{\text{Taken compliment}}\ \underbrace{1}_{\text{kept same}}$

→ Computer uses 2's complement rather than 1's complement as it gives unique values for each data.

Subtraction using Addition

Using signed representation, subtraction can be done through addition.

6 :	00000110		6 :	00000110
+13 :	00001101		−13 :	11110011
+19 :	00010011		−7 :	11111001
				↓
				00000111
				−7

−6 :	11111010
−13 :	11110011
−19 :	1 | 11101101 → 00010011 = 19

$\underbrace{1}_{\text{carry}}$ $\underbrace{1}_{\text{MSB}}$

∴ −19

Binary Codes

→ Binary Coded Decimal (BCD): 4 bit

→ ASCII → American Standard Code for Information Interchange

- → 128 symbols → 7 bits
- → special characters
- → Small/capital letters
- → Alpha-num

→ BCD: Represent decimal numbers.

4 bits — Weighted Code (8 4 2 1)

Total 16 combinations.

10 codes we use

Remaining 6: unknown/don't care. ('X' - symbol)

→ For representing 2-digit decimal no.: 8 bits are required

Eg. 25

0010 0101

⇒ 00100101

Similarly, it can be extended to any digits.

Gray code: Decoding logics → 1 bit change

0	0	0	—	0
0	0	1	—	1
0	1	1	—	2
0	1	0	—	3
1	1	0	—	4

In successive members, only single bit changes.

Binary → Gray : Preserve MSB
→ Do EXOR with successive pairs.

Eg., 3 = 0 1 1 EXOR
Gray : 0 1 0

4 = 1 0 0
same EXOR
1 1 0