High-Throughput Bit-Packing Architecture for CCSDS-123 Hyperspectral Image Compression

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Abstract

This project focuses on the practical implementation of the CCSDS-123 compression standard on a Zynq FPGA for real-time hyperspectral image compression. The design leverages a sophisticated multi-stage pipelined architecture to achieve continuous, high-throughput processing with minimal latency. Hyperspectral imaging (HSI) generates massive data volumes, requiring efficient on-board compression before transmission. The CCSDS-123 standard provides a lossless compression algorithm widely adopted in space applications, where its entropy encoder produces variable-length codewords that must be packed into fixed-size transmission units. This project presents a high-throughput, memory-optimized bit-packing architecture designed for real-time CCSDS-123 implementations.

The proposed system integrates seamlessly into the CCSDS-123 pipeline, accepting variable-length Golomb-coded words (1–48 bits) and packing them into configurable B-byte output words. A dual-register shifting technique (current/next register) eliminates stalls by dynamically splitting codewords across registers when they exceed remaining space. Control logic tracks write positions via a pointer-based state machine, ensuring continuous throughput. Designed for FPGA/ASIC implementation, the module supports on-the-fly processing at 147 MSamples/s (2.35 Gb/s) with minimal buffering, aligning with the CCSDS-123 standard's low-latency requirements.

The bit packing module collects variable-length encoded words from the entropy encoder and packs them into fixed-size output words (configurable size B bytes). This is necessary because the entropy encoder produces variable-length codewords that need to be efficiently packed for transmission or storage.

Benchmarked on a Xilinx Zynq-7020 FPGA, the design achieves 98% utilization efficiency with 8B output words, outperforming prior FIFO-based approaches in throughput and resource usage. This architecture is scalable for space-grade ASICs and adaptable to other variable-length coding standards.