20-01-2025

VLSI Technology

Course Outcomes:

- How semiconductor devices are fabricated in large scale.
- Issue in fabricating large no. of devices on a single chip
- Processes involved in the fabrication

VLSI ⇝ Very Large scale Integration

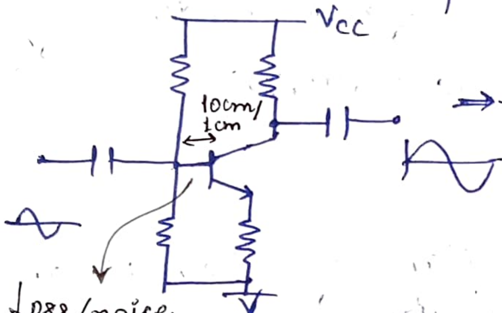
→ chip
→ dice or substrate → base at which we construct devices

Area = constant → Pack as many device (transistors) as possible.

+ diodes + capacitors + inductors + resistors → functional components

Scaling Laws: When we reduce the size of the device.

(Transistor + Resistor + Capacitor):



→ Amplifier → On breadboard
↳ Reconfigurable

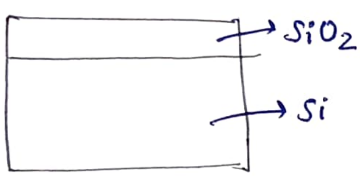
On IC
↳ Trying to achieve reconfigurability.

Crystal → Periodic/uniform arrangement throughout the structure.

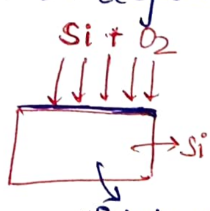
Single crystal Si → Lattice constant = 5.4 Å

Deposition : depositing of one material over other (substrate).

Etching : Removing material

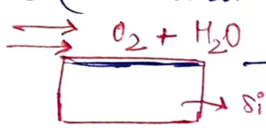


① Grow or deposit SiO_2

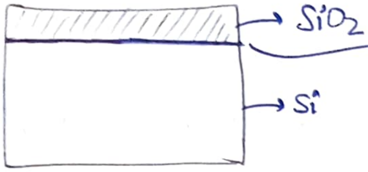


- Precisely control thickness. ← by controlling amount of Si & O_2 → control P, V, T of O_2 → [PV = nRT]
- Control morphology (atom arrangement).

② Mix O_2 (and water) vapour, and oxidise the substrate.



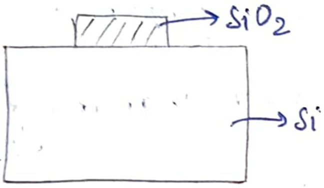
→ Thin and poor quality of SiO_2.



→ Interface
↳ Dangling bonds (highly unstable)
Si : $1s^2 2s^2 2p^6 \underbrace{3s^2 3p^2}$
↳ captures e^-s and diminishes current.

→ While depositing, ensure that it does not damages the substrate and interface is perfect (minimizing dangling bonds).

↓ Etching → Removing unwanted materials.



↳ Maximize etching of SiO_2, minimize etching of Si.

- ★ Selective etching
- Dry etching → Use of gas ~~…~~ or mixture of gas.
- Wet etching → Use of (acids + alkalis).

Planarization : IC Making
↳ Make the devices on the plane of substrate and interconnect them (electrical interconnection).
↳ deposit metals (that can drive voltages).

21-01-2025

Semiconductor Revolution

Point-contact transistor
≡ Vacuum Triode ⇝ Germanium

Transistor : BJT vs MOSFET

1^{st} IC : 3 BJTs + 2 diodes + few resistors

↓

Increase functionalities

↓

Increase no. of transistors

↓

Speed ↑ (Area = constant)

↳ Reduce size of transistor

↳ Scaling

Moore's law of scaling: Device downsizing

Semiconductor:

↳ Change conductivity using doping

↳ In realtime: By

① Electric field
② Photons
③ Temperature
④ Pressure

↳ Conductivity decided by the amount of free electrons.

IC: Collection of devices such that when put collectively, can perform some operation.

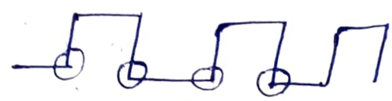
→ Si vs GaAs

Si ↓ cheap

GaAs ↓ fast ↓ Carriers are more mobile

Mobility, $\mu \propto \frac{1}{m^*}$

Data representation: 0 and 1



↳ Current should be detected.

→ High purity silicon crystal ⇝ perfect atomic arrangement, with only si-atoms.

↳ Impurities:

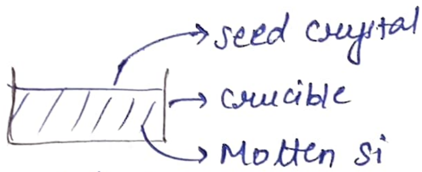
$$\underset{\text{(silica)}}{SiO_2} \rightleftharpoons Si + O_2$$

Czochralski Process:

↳ High purity polycrystalline si in crucible.
↳ Heated to m.p. of Si (1412°C).
↳ Crucible rotates for uniform temp.
↳ A "seed" crystal is placed into the melt and then pulled out.
↳ Molten si crystallizes in the appropriate orientation and forms an ignot.

↓ slice

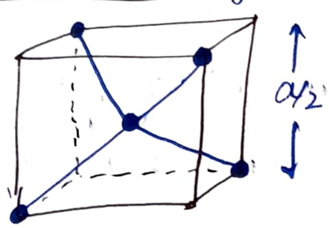
Silicon wafer or slice or substrate



Si can attend all solid crystal structure:

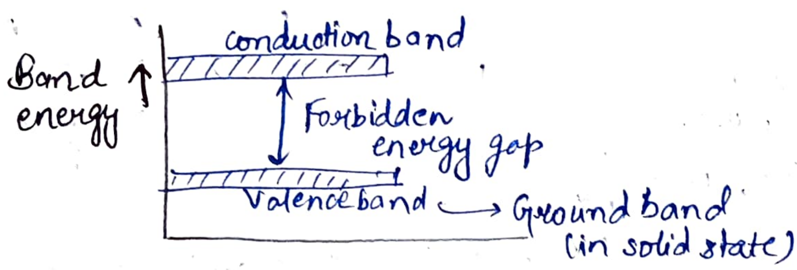
- Amorphous 
- Polycrystalline ⇝ e^- behaviour different in different lattice  grain boundaries } for forming solar cells
  - current fluctuates. (due to dangling bonds at grain boundaries)
- Single-crystalline ⇝ for VLSI 
  - ↳ for IC

Diamond Lattice (for Si)



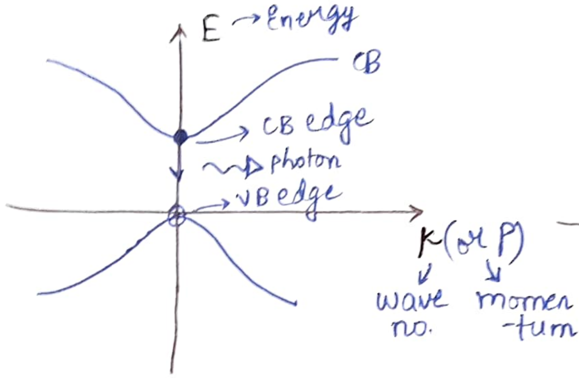
a: lattice constant ~5.4 Å

2 Si atoms coming together ⇝ forms closely-spaced ~~bands~~ levels or bands

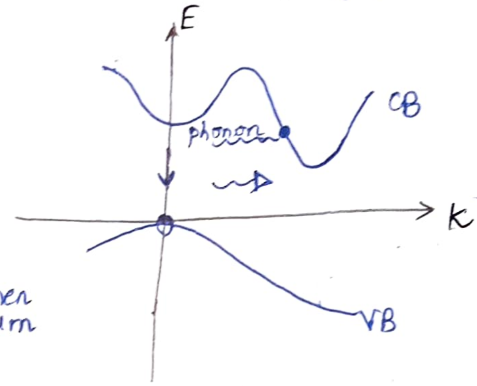


For Si at room temp., band gap = 1.1eV.

Direct Bandgap



Indirect Bandgap



: Band Structure

→ Difficult to recombine

$P = \hbar k$
$= \frac{h}{2\pi} \cdot k$

↳ e^- collide with lattice to loose momentum (producing phonon)

e^- and hole recombine: Energy & momentum conservation

Effective Mass

m_0 $(= 9.1 \times 10^{-31}$ kg$)$: mass of e^- with no force.

Total force (F) = Internal forces + External force = $m_0 a$

Internal forces ↓ (repulsive + attractive) ↳ Unknown

External force (voltage applied) ↳ Known

or

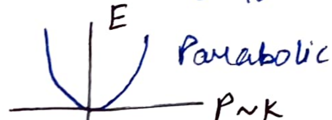
$F = m^* a$ (ignoring internal forces)
↳ effective mass
(m_e^*, m_h^*)

EHP: Electrons and holes are generated in pair by light or heat.

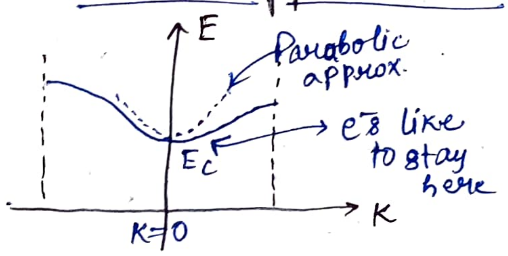
E-K Diagram:

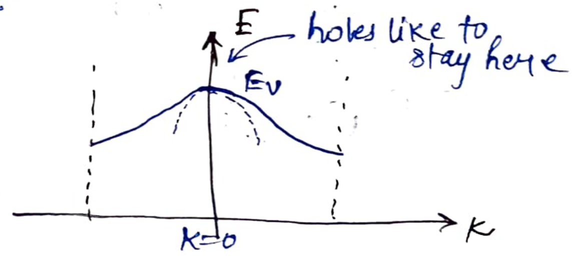
$$E = \frac{\hbar^2 k^2}{2m_0}$$

$$E = \frac{1}{2} m_0 v^2 = \frac{m_0^2 v^2}{2m_0} = \frac{p^2}{2m_0}$$



Parabolic Approximation:





27-01-2025

Free electron: Min^{m} energy $= 0$ (at rest)

Bound electron: Non-zero energy
↳ Zero-point energy

$$E = \frac{\hbar^2 k^2}{2m_0}$$

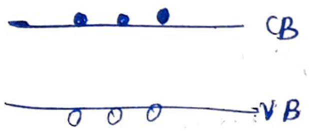
$$E = \frac{\hbar^2 k^2}{2m^*} \quad \text{(bound } e^-\text{)}$$

$$\frac{d^2E}{dk^2} = \text{constant.}$$

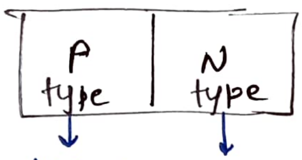
Pure semiconductor (intrinsic):

↳ No. of e^-s in CB = No. of holes in VB

$\boxed{n_0 = p_0}$ (Thermal equilibrium)
↳ constant temperature
↳ No electric field

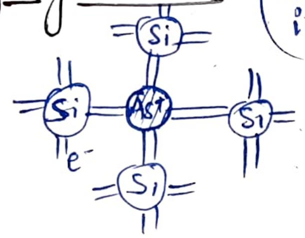


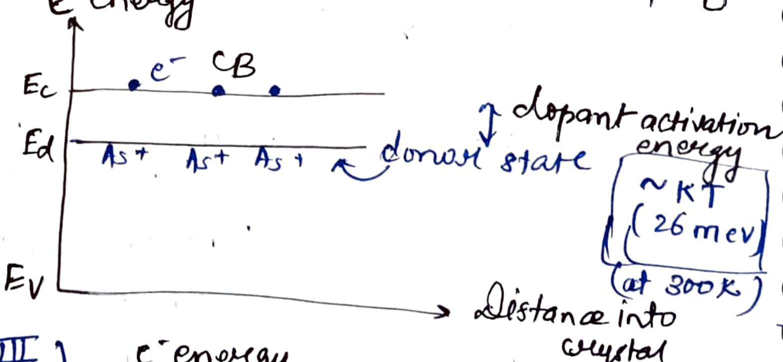
(EHP)



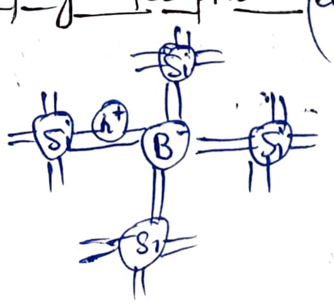
$p_0 > n_0$ $\quad$ $n_0 > p_0$ ⟶ To change conductivity: Doping

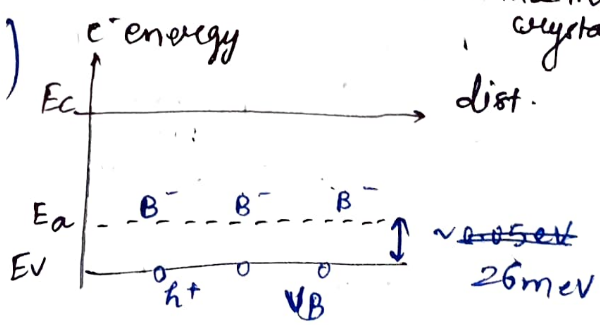
Doping: Donars (column V impurity)





Doping: Acceptors (Column III impurity)





[Freeze-out : No e^-s ⇔ At 0 K] ← ↑ → [10^{16} e^-s : Partial ionization]

→ 10^{18} Arsenic atoms /cm3 ⇒ 10^{18} e^-s [$n_0 = 10^{18}/cm^3$]

↓ dopant density

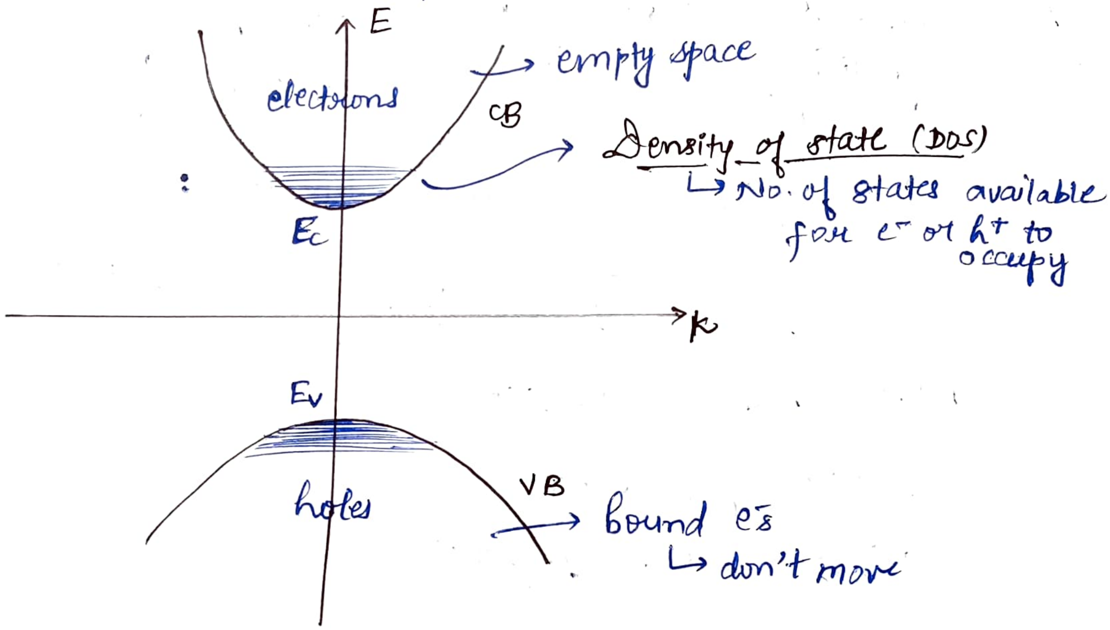
↳ [Complete ionization (at 250–350 K)]

Room Temperature Activation : Energy available at the room temperature should be sufficient to take the e^-s from donor state to CB.

↳ Only possible for column III or V atoms.

Dopant stability : Dopant atoms should not move ; ~~not the~~ only the e^-s donated by them should move.

↳ Only for col. III or V atoms.



DOS : $g(E) = \frac{4\pi (2m)^{3/2}}{h^3} \sqrt{E}$ (for 3D Semiconductor materials)

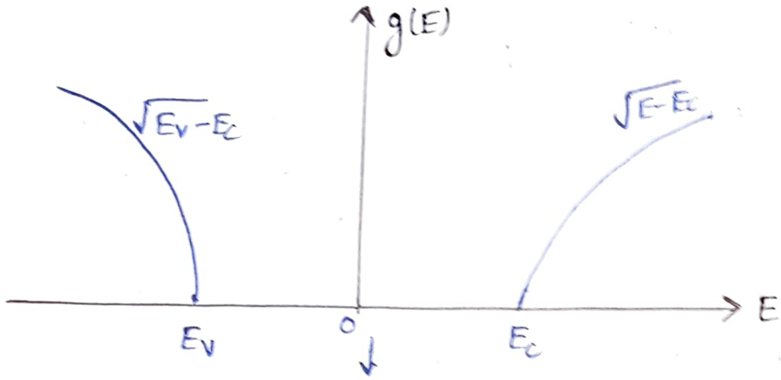
→ Based on DoF (degree of freedom) and doc (degree of confinement), Semiconductor materials can be :

→ 3D
→ 2D
→ 1D
→ 0D

$g_{CB}(E) = \frac{4\pi (2m_e^*)^{3/2}}{h^3} \sqrt{E - E_c}$, $E \geq E_c$

$g_{VB}(E) = \frac{4\pi (2m_h^*)^{3/2}}{h^3} \sqrt{E_v - E}$, $E \leq E_v$

Between E_c & E_v ⇓ Forbidden state



$\frac{E_c + E_v}{2}$ = midgap

03-02-2025

No. of electrons in C.B.,

$n(E)$ = DOS × probability function.

Probability density function (in CB), $f(E) = \frac{n(E)}{DOS}$ = $\frac{\text{actual no. of electrons}}{\text{max. no. of electrons}}$

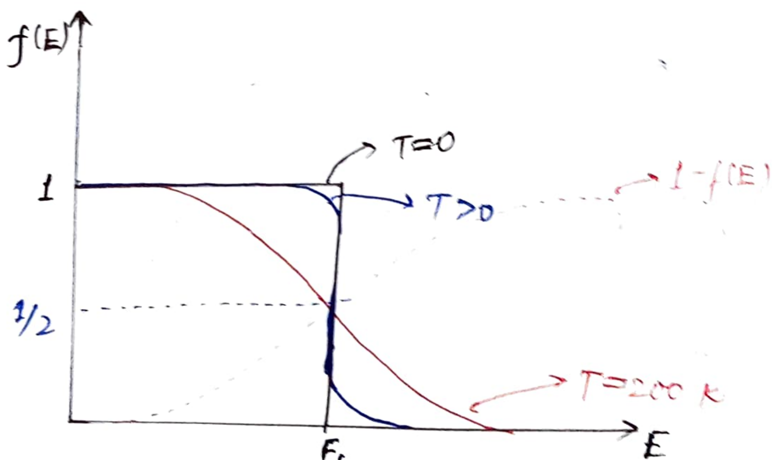
↳ Fermi-Dirac distribution function:

$$\boxed{f(E) = \frac{1}{1 + e^{(E-E_f)/KT}}} , \quad 0 \leq f(E) \leq 1$$

P.D.F. (in VB) $= 1 - f(E)$

$n(E) = g_{CB}(E) \times f(E)$

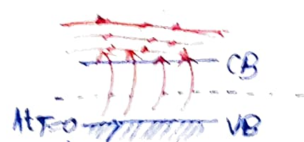
$p(E) = g_{VB}(E) \times (1 - f(E))$



At $T=0$, for $E < E_f$, $f(E) = 1$

for $E > E_f$, $f(E) = 0$

↳ All states upto E_f will be filled with electrons.



$$n_0 = \int_{E_c}^{\infty} n(E)\, dE = \int_{E_c}^{\infty} \frac{4\pi (2m_e^*)^{3/2}}{h^3} \sqrt{E-E_c} \cdot \frac{1}{1+e^{(E-E_f)/KT}} dE$$

$$p_0 = \int_{-\infty}^{E_V} p(E)\, dE = \int_{-\infty}^{E_V} \frac{4\pi (2m_h^*)^{3/2}}{h^3} \sqrt{E_V - E} \cdot \left(1 - \frac{1}{1+e^{\left(\frac{E-E_f}{KT}\right)}}\right) dE$$

If $E - E_f \gg 3KT$ [Boltzmann's approximation], then

$$f(E) = \frac{1}{1+e^{(E-E_f)/KT}} \approx e^{-\frac{(E-E_f)}{KT}}$$

$$\Rightarrow n_0 = \frac{4\pi(2m_e^*)^{3/2}}{h^3} \int_{E_c}^{\infty} \sqrt{E-E_c} \cdot e^{-\frac{(E-E_c+E_c-E_f)}{KT}} \cdot dE$$

Let $\frac{E-E_c}{KT} = u \Rightarrow du = \frac{dE}{KT}$

When $E = E_c \Rightarrow u = 0$

$E \to \infty \Rightarrow u \to \infty$

$$= (\cdot) \int_0^{\infty} \sqrt{u}\sqrt{KT} \cdot e^{-\left(\frac{E-E_c}{KT}\right)} e^{-\left(\frac{E_c-E_f}{KT}\right)} du \cdot KT$$

$$= (\cdot) \int_0^{\infty} \sqrt{u}\sqrt{KT} \cdot e^{-u} \left(e^{-\frac{(E_c-E_f)}{KT}}\right) du \cdot KT$$

$$= (\cdot) \int_0^{\infty} \sqrt{u}\, (KT)^{3/2} e^{-u} du$$

$$= (\cdot) \int_0^{\infty} e^{-u} u^{1/2} du = \frac{\sqrt{\pi}}{2} \quad \text{[Gamma function]}$$

$$= \frac{4\pi (2m_e^*)^{3/2}}{h^3} (KT)^{3/2} \cdot e^{-\frac{(E_c-E_f)}{KT}}$$

$$n_0 = 2\left(\frac{2m_e^* \pi KT}{h^2}\right)^{3/2} \exp\left(-\frac{(E_c-E_f)}{KT}\right), \quad p_0 = 2\left(\frac{2m_h^* \pi KT}{h^2}\right)^{3/2} \exp\left(\frac{-(E_c-E_f)}{KT}\right)$$

$$= \int_{E_c}^{\infty} DOS_{CB} \cdot f(E) \qquad = \int_{-\infty}^{E_V} DOS_{VB} \times [1-f(E)]$$

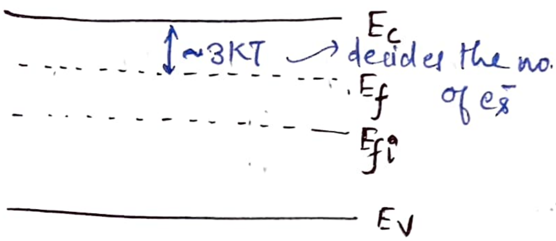
04-02-2025

$E_c - E_v$ = Band gap

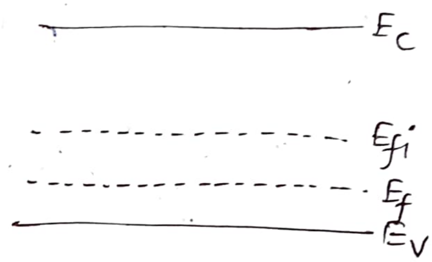
$\frac{E_c + E_v}{2}$ = Mid band

Law of Mass Action : $n_0 p_0 = n_i^2$

n-type



p-type

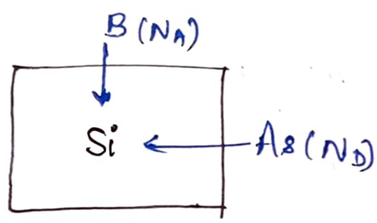


→ Degenerate Semiconductors

As ↑ ⇒ $E_c - E_v$ ↓

~3KT

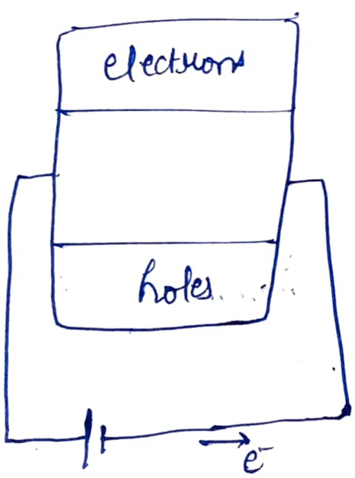
Compensated Semiconductor : Both donors & acceptors



$N_A > N_D$: p-compensated

$N_D > N_A$: n-compensated

$N_A = N_A$: completely compensated → intrinsic



Carrier transport

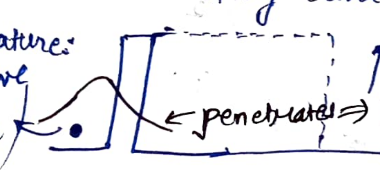
↳ By electric field : Drift current

↳ By difference in carrier concentration : Diffusion current

↳ Tunneling :

  ↳ in : tunnel diode, schottky diode.

Dual nature: wave + particle



Scattering: Electrons collide with electrons, nucleus or semiconductor lattice and change their direction.

07-02-2025

Drift → Electric field → Parameter: Mobility (μ)
Diffusion → Concentration gradient → Diffusion coefficient / Diffusivity (D)
Tunneling → Significant for small devices

{ GaAs → High μ for carriers → high speed
{ Si →

$$\boxed{\frac{D}{\mu} = \frac{KT}{q}}$$: Einstein's relationship

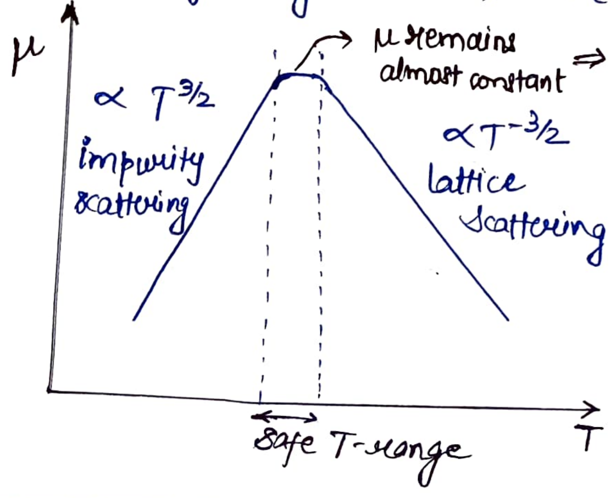
Collisions: Either with a charged carrier
or
with a lattice atom → Lattice scattering → Depends on temperature
(Lattice atoms vibrating)
or
with an impurity atom ⇒ ionized (ionized impurities)
↳ Ionized impurity scattering

[n-type V: Si — As^+]
[p-type III: Si — B^-]

Larger scattering
⇓
More resistance

$KT = 26\ meV$ at $T = 300K$

→ a-Si (amorphous Si)
poly-Si (polycrystalline Si)
X-Si (single crystalline Si) ⇝ least collision.

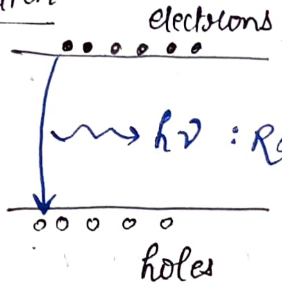


⇒ preferable

→ Applicable for holes as well

$$\boxed{\frac{1}{\mu} = \frac{1}{\mu_L} + \frac{1}{\mu_I} + \frac{1}{\mu_{other}}}$$

Recombination



$h\nu$: Radiative recombination

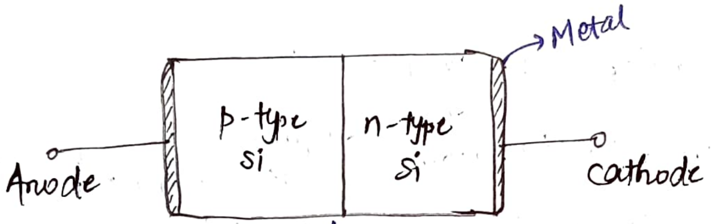
For different $k \rightarrow$ non-radiative recombination

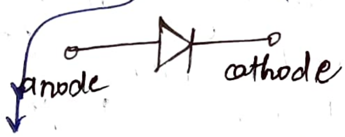
Surface recombination: At the surface of the device, due to the dangling bonds capturing the electrons going out.

SiO_2 (passivation layer) : Suppress the dangling bonds

10-02-2025

PN Junction





Graded junction

Metallurgical interface

⇓

Step junction or abrupt junction

↳ by epitaxial technique

$\xrightarrow{\text{Join}}$ SiO_2 ~~becomes~~ acts as barrier

⇓

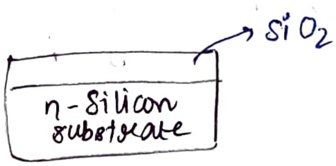
Does not act as p-n junction

SiO_2 → natural SiO_2 layer

↓

insulator

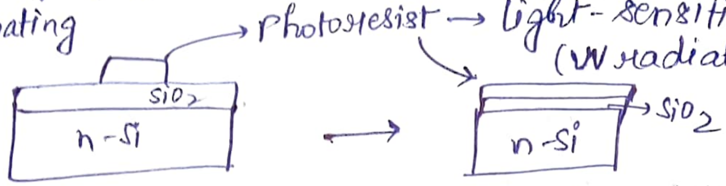
Fabrication :

1. Clean the substrate (by default, Si is n-type).
2. 

Deposit a thin layer of SiO_2 by oxidation.

③ Photolithography

① Spin-coating

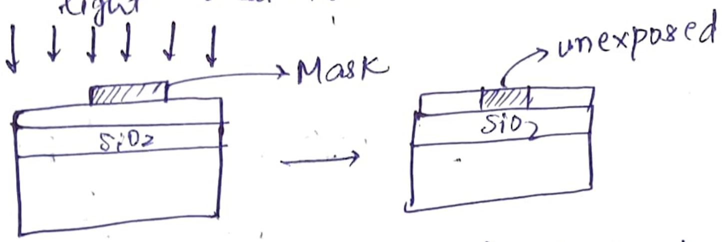


Put droplets of photoresist and spin it at high speed.

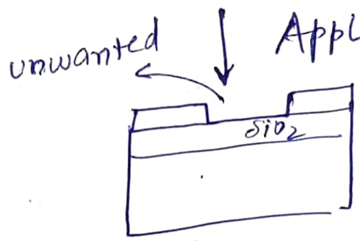
positive ↓ after exposing to UV, it gets weakened.

negative ↓ after exposure, it gets hardened.

② Exposure



③ Developing



Apply developer ↓ eats the ⊖ve photoresist

11-02-2025

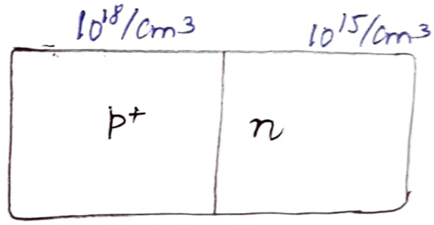
PN JUNCTION DIODE

Intrinsic carrier concⁿ of Si, $n_i = 10^{10}/cm^3$.

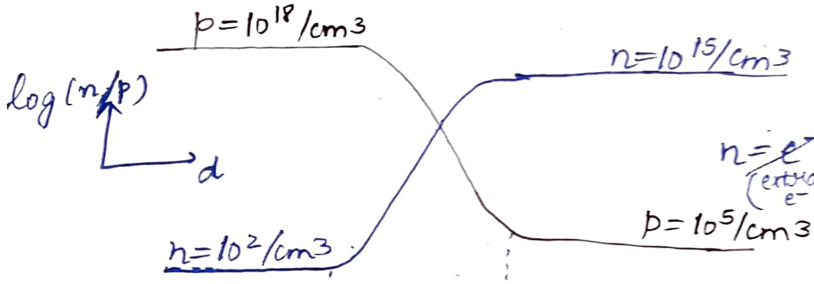
Lightly doped : $10^{15}/cm^3 = n_e$

Highly doped, $p^+ = 10^{18}/cm^3$.

SCL in India
↓
180nm technology



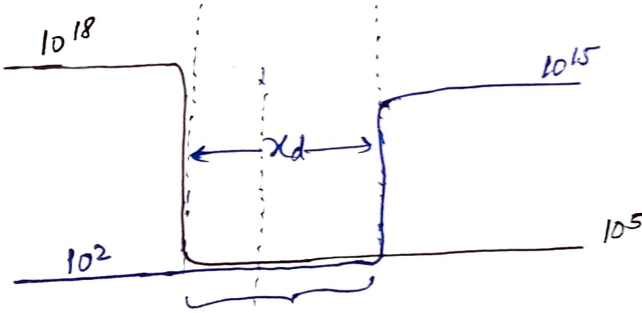
Either p^+n or n^+p fabrication pratically.



$p \cdot n = n_i^2$

$n = e^- + N_D^+$ (extra e^-)

(log scale)



(normal scale)

↳ Depletion region

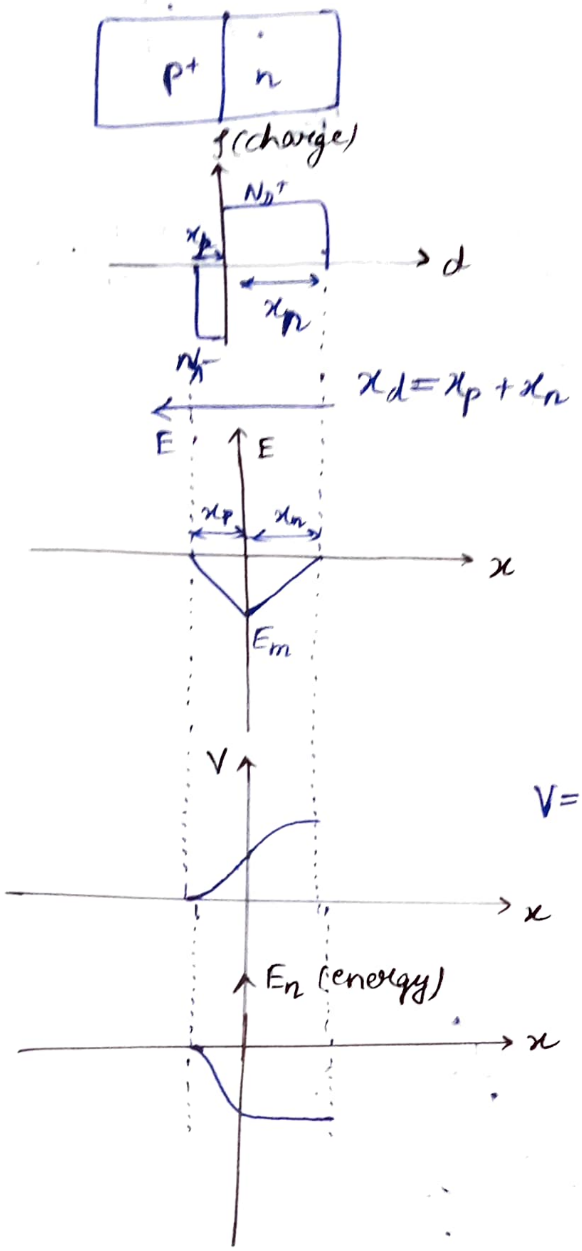
↳ Less no. of mobile carriers (but not zero), but can be assumed zero, analitically.

↳ $J = q \underset{\downarrow}{n} \underset{\uparrow}{v}$

→ p-side charge = n-side charge

$q \cdot p(x_p \cdot A) = q \cdot n(x_n \cdot A)$

$\Rightarrow \underset{\uparrow}{p} \cdot \underset{\downarrow}{x_p} = \underset{\downarrow}{n} \cdot \underset{\uparrow}{x_n}$ ⇒ p-side depletion region is small.



$$\frac{dE}{dx} = \frac{qN_D^+}{\epsilon}$$

Si : $\epsilon = 11.8 \approx 12$

SiO_2 : $\epsilon = 4$

$\frac{dE}{dx} = \frac{\rho}{\epsilon}$: Gauss Law (ρ → total charge)

$$V = -\int E\,dx$$

$$E_n = -qV$$

14-02-2025

→ $p\mu E - D\frac{dp}{dx} = J_p$

In depletion region, no charge so no current, i.e., equilibrium :

$$p\mu E - D\frac{dp}{dx} = 0$$

$$\Rightarrow pE - V_T\frac{dp}{dx} = 0$$

$$\Rightarrow E = \left(\frac{V_T}{p}\right)\frac{dp}{dx}$$

$$\Rightarrow V = -\int E\,dx$$

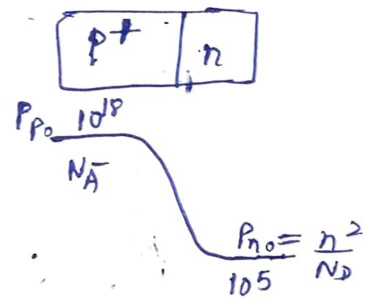
$\frac{D}{\mu} = \frac{KT}{q} = V_T$: Einstein's eq^n

V_T → thermal voltage

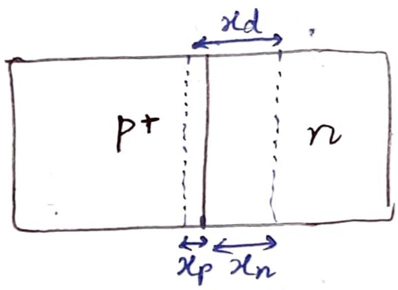
$D = V_T\,\mu$

$$\Rightarrow V = -V_T \int_{P_{p_0}}^{P_{n_0}} \frac{dP}{P}$$

$$= + V_T \ln \frac{P_{p_0}}{P_{n_0}} = V_T \ln \frac{N_A N_D}{n_i^2}$$



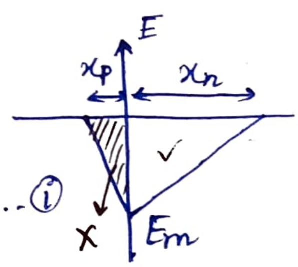
$$\therefore \boxed{V_{bi} = V_T \ln \frac{N_A N_D}{n_i^2}}$$: Built-in potential



$$x_d = x_n + x_p$$

$E_m = ?$

$x_d = ?$



$[x_n >> x_p]$

$$V_{bi} = \frac{1}{2} E_m x_d$$

$$= \frac{1}{2} E_m (x_n + x_p) \quad \ldots (i)$$

$$N_A x_p = N_D x_n$$

$$\Rightarrow x_p = \frac{N_D}{N_A} x_n \quad \ldots (ii)$$

(ii) → (i),

$$V_{bi} = \frac{1}{2} E_m \left(x_n + \frac{N_D}{N_A} x_n \right) \quad \ldots (iii)$$

Assumption,

$$\boxed{\frac{E_m}{x_n} = \frac{q N_D}{\epsilon}}$$ $[x_n >> x_p]$

$$\Rightarrow E_m = \frac{q N_D x_n}{\epsilon} \quad \ldots (iv) \quad \Rightarrow x_n = \frac{E_m \epsilon}{q N_D}$$

$$V_{bi} = \frac{1}{2} E_m x_d$$

$$\Rightarrow x_d = \frac{2 V_{bi}}{E_m} = \frac{2 V_{bi} \epsilon}{q N_D x_n}$$

$$\Rightarrow V_{bi} = \frac{1}{2} E_m \left(1 + \frac{N_D}{N_A}\right)\left(\frac{E_m \cdot \epsilon}{q N_D}\right) = \frac{E_m^2}{2}\left(\frac{N_A + N_D}{N_A N_D}\right)\frac{\epsilon}{q}$$

$$\Rightarrow E_m = \sqrt{\frac{2 V_{bi} N_A N_D q}{(N_A + N_D)\epsilon}}$$

$$\text{As } x_d = \frac{2V_{bi}}{E_m} = \frac{2V_{bi}}{\sqrt{2V_{bi}}}\sqrt{\frac{N_A+N_D}{N_A N_D} \cdot \frac{\epsilon}{q}}$$

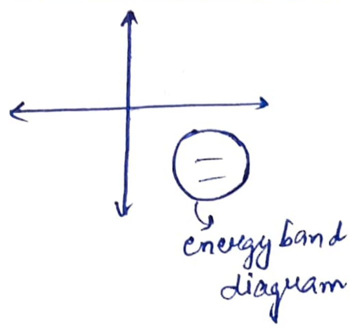
$$= \sqrt{\frac{2V_{bi}\epsilon}{q}\left(\frac{N_A+N_D}{N_A N_D}\right)}$$

$$\therefore \; x_d = \sqrt{\frac{2V_{bi}\epsilon}{q}\left(\frac{1}{N_A}+\frac{1}{N_D}\right)}.$$

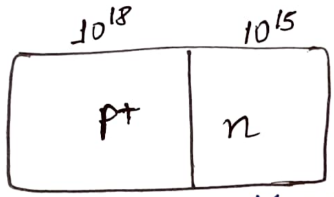
H/W:

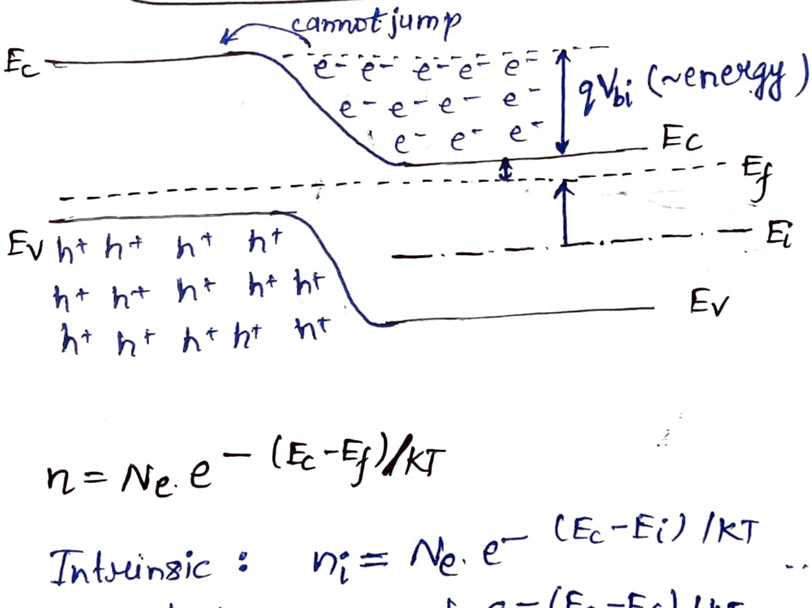
Energy $(E) = -qV$

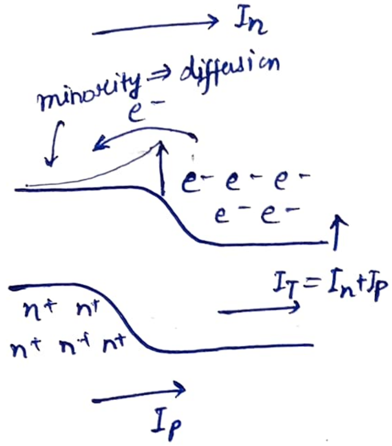
~~do~~ Coulomb's law
↓
potential
↓
work
↓
energy



Equilibrium:







$$n = N_e \cdot e^{-(E_c - E_f)/KT}$$

Intrinsic : $n_i = N_e \cdot e^{-(E_c - E_i)/KT}$ ...ⓐ

Doped : $n_e = N_e \, e^{-(E_c - E_f)/KT}$ ...ⓑ

$$ⓑ/ⓐ \Rightarrow \frac{n_e}{n_i} = \frac{N_e \, e^{-(\cancel{E_c} - E_f)/KT}}{N_e \cdot e^{-(\cancel{E_c} - E_i)/KT}}$$

$$\Rightarrow n_e = n_i \, e^{-(E_i - E_f)/KT},$$

$$p = n_i \, e^{-(E_f - E_i)/KT}$$

Thumb rule :

If $n = 10^{18}$

$E_f - E_i = 8 \times 0.06$
↓
8 level higher than n_i
(90% correct)

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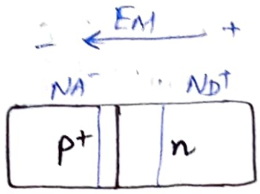
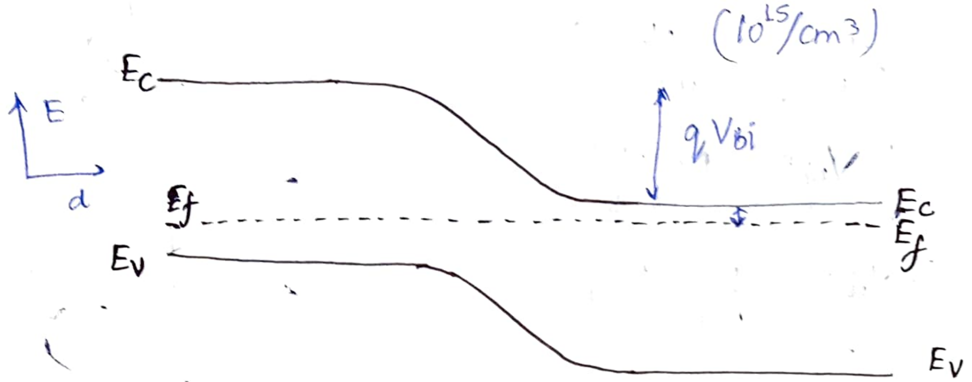
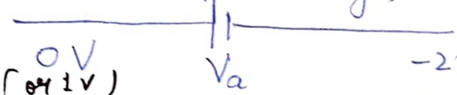




(applied voltage)



0 V (or 1 V)

$E = -qV$

$= 0\ eV$

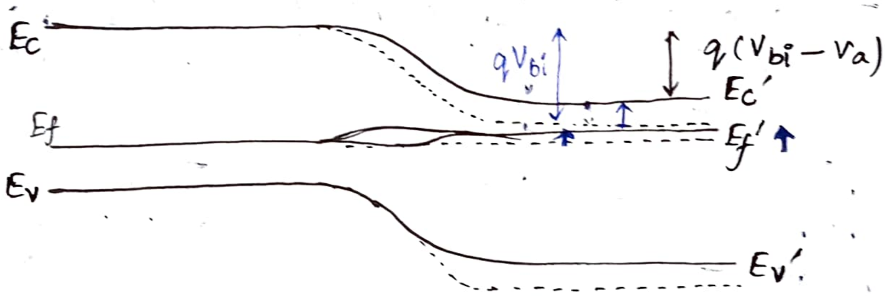
(No change this side)

−2 V (or −1 V)

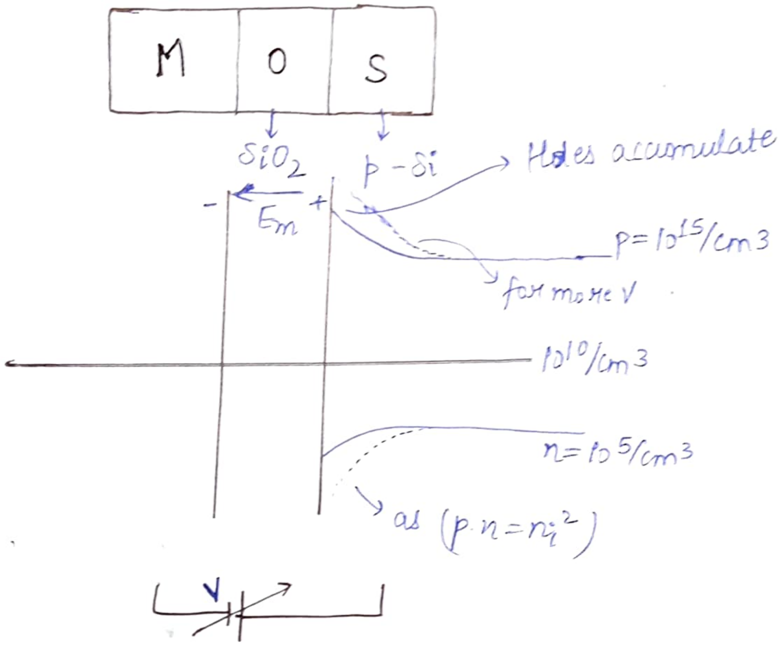
$E = -q(-2V)$

$= 2eV$

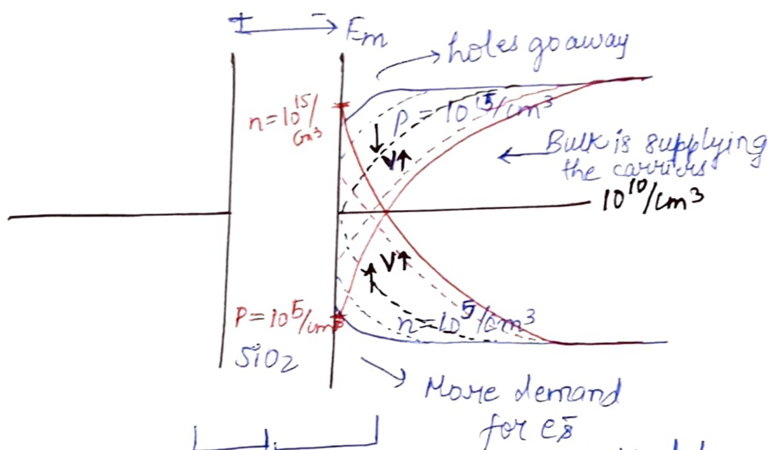
(Energy levels shift up)



MOS (Metal Oxide Semiconductor)



Holes accumulate here ⇒ Accumulation region



More demand for e^-s

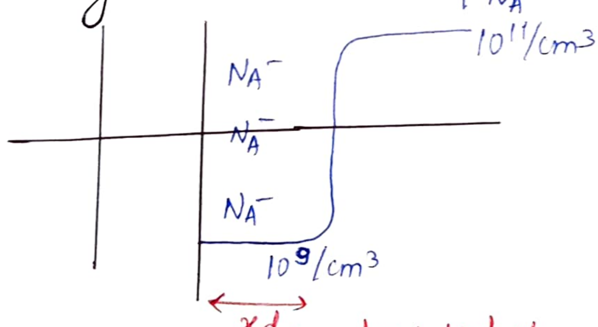
↳ fulfilled by minority carriers & N_A^-

As V ↑, at threshold voltage, the carrier ~~concentration &~~ polarity inverts (with same concn).

⇓

Inversion

In log-scale:



x_d → depleted of mobile carriers ⇒ Depletion Region

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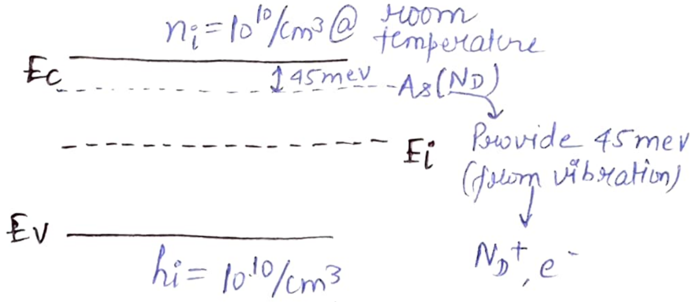
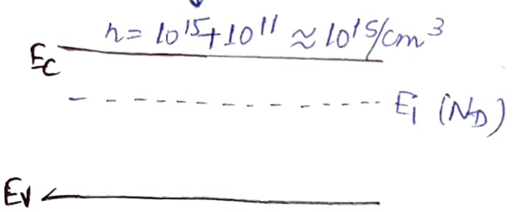
Band Model:



No. of Si available $= 5\times10^{22}/cm^3$

$N_D = 10^{15}/cm^3$ (As)



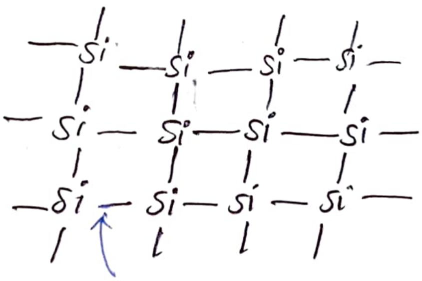
$N_D = 10^{15}/cm^3$

$N_D^+ = 10^{15}/cm^3$

n = no. of $e^- = 10^{15}\ cm^3$

$\therefore\ n = N_D^+$ (good approximation)

Bond Model:

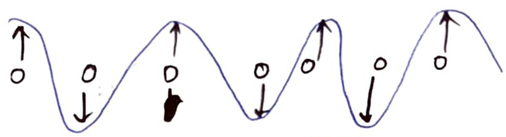


1.1 eV required to break the bond (band gap)

Energy at room temp. $= 26$ meV

$\Downarrow$

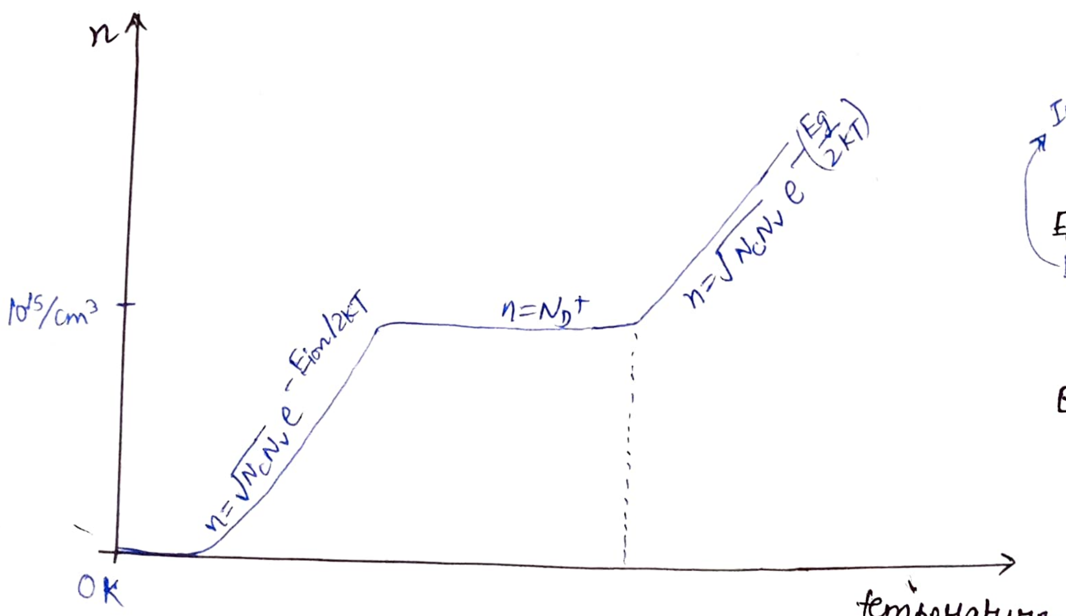
Generates vibration

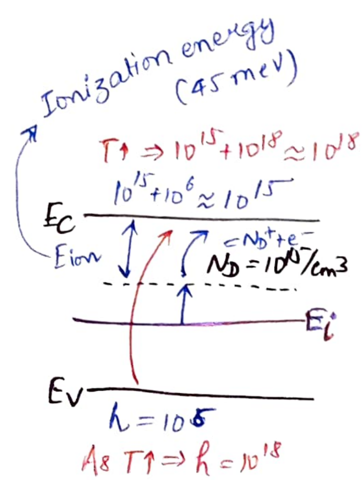


↳ wave : $E = h\nu$

$\Downarrow$

constructive interference $\Rightarrow$ Generates 1.1 eV

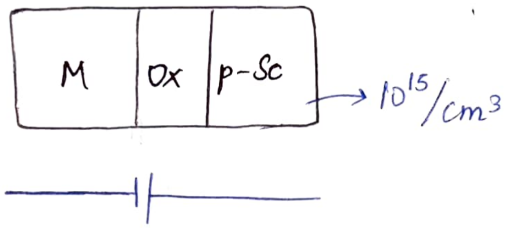


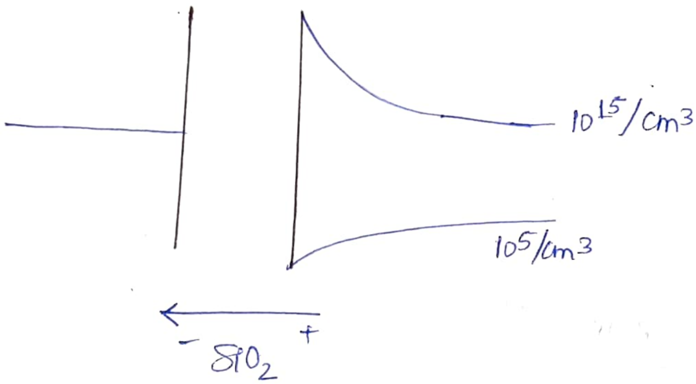


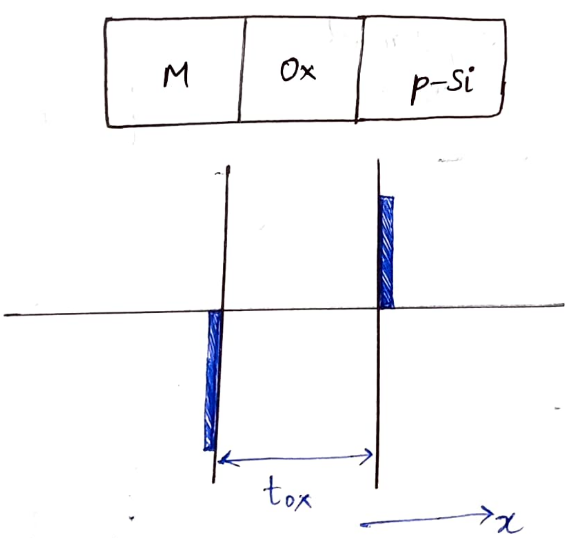
$n = 2\left(\frac{2\pi m KT}{h^2}\right)^{3/2} \cdot e^{-\left(\frac{E_c - E_f}{KT}\right)}$

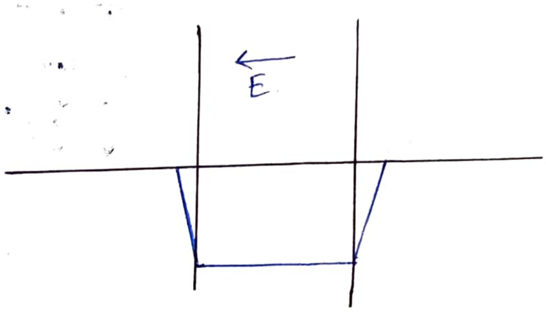
21-02-2025

MOS Electrostatic Model









$$\frac{dE}{dx} = \frac{\rho}{\epsilon}$$

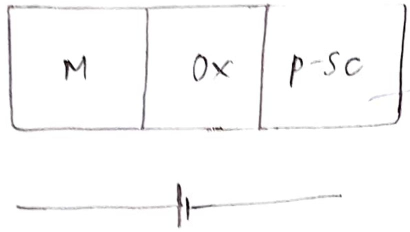
$$E = \int \frac{\rho\, dx}{\epsilon}$$

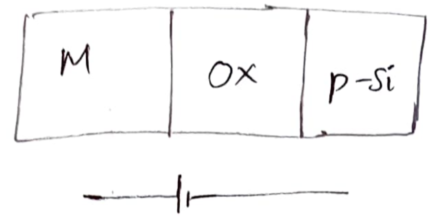
$$V = \frac{-Q_0 t_{ox}}{\epsilon}$$, Q_0 = total charge

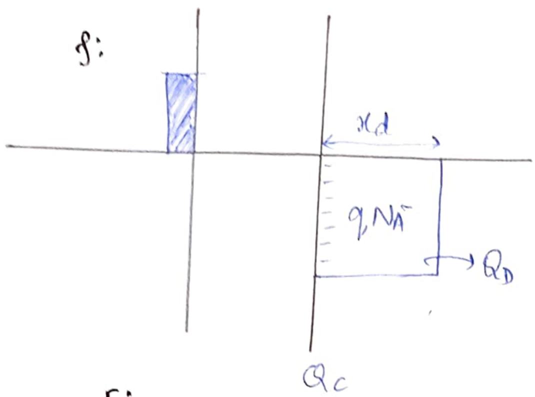
$$\Rightarrow V = -Q_0 / C_{ox}$$

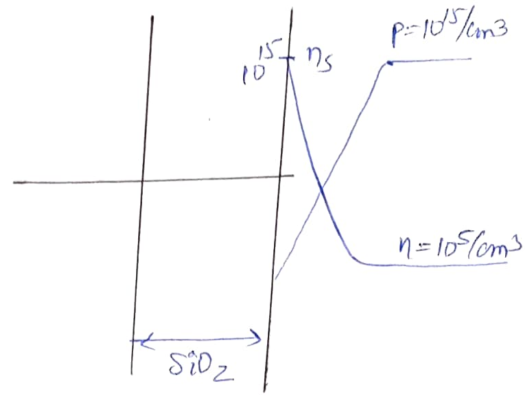
where $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$

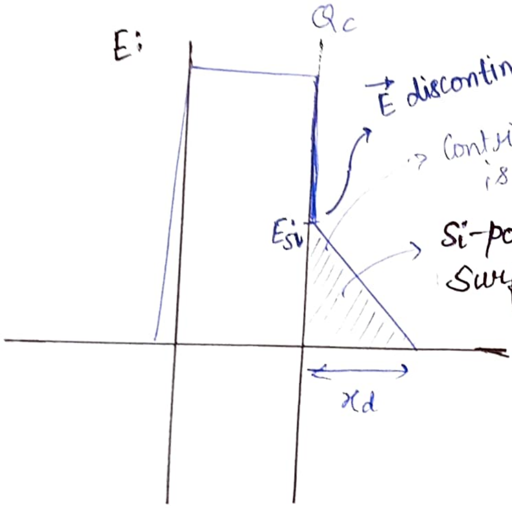
Accumulation charge $\therefore$ $\boxed{Q_0 = -C_{ox} V}$











$\vec{E}$ discontinuous

→ Contribution of ⊖ve charge is mostly due to N_A^- (not inverted charge) [80 (N_A^-) + 20 (e^-)]

Si-potential

Surface potential

$$\left[\frac{E_{si}}{x_d} = \frac{qN_A^-}{\epsilon_{si}}\right]$$

$\epsilon_{ox} E_{ox} = \epsilon_{si} E_{si}$ [electric displacement ↳ continuous]

$$E_{ox} = \frac{\epsilon_{si}}{\epsilon_{ox}} E_{si}$$

$$\approx \frac{12}{4} E_{si} = 3E_{si}$$

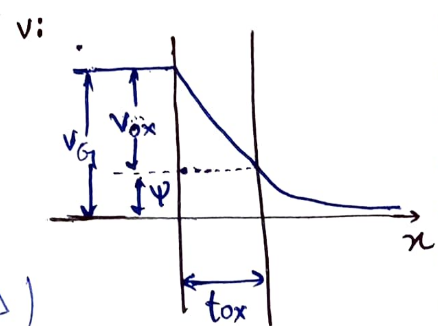
Method-1: Boltzmann

$$V_{si} = V_T \ln \frac{n_s}{n}$$

$$= V_T \ln \frac{P_0^2}{n_i^2} \qquad (\because n = n_i^2/p_0)$$

$$= 2V_T \ln \frac{N_A^-}{n_i} \qquad \text{(Surface-potential at threshold)}$$

$$V_{si} = \frac{1}{2} E_{si} x_d \qquad \text{(Area of the } \Delta\text{)}$$



Calculate threshold voltage.

$$Q_D = qN_A^- x_d = +Q_M$$

$$\Rightarrow \cancel{x_d = \left(\frac{Q_D}{qN_A}\right)} \quad Q_D = qN_A^- \sqrt{\frac{2\epsilon_{si} V_{si}}{qN_A}}$$

$$= \sqrt{2\epsilon_{si}\, qN_A^- V_{si}}$$

$$\cancel{\Rightarrow V_{si} = \frac{1}{2} E_{si} \cdot \left(\frac{Q_D}{qN_A}\right)}$$

$$V_{si} = \frac{1}{2} E_{si} x_d$$

$$= \frac{1}{2}\left(\frac{qN_A^- x_d}{\epsilon_{si}}\right) x_d$$

$$\Rightarrow x_d = \sqrt{\frac{2\epsilon_{si} V_{si}}{qN_A^-}}$$

$$\Rightarrow E_{si} = \frac{2V_{si} \cdot qN_A^-}{Q_D} \quad \left[\because x_d = \frac{Q_D}{qN_A^-} \; ; \; V_{si} = \frac{1}{2} E_{si} \frac{Q_D}{qN_A^-} \right]$$

$$\therefore V_G = V_{ox} + V_{si}$$
$$= E_{ox} t_{ox} + V_{si}$$
$$\approx 3E_{si} \cdot t_{ox} + V_{si}$$
$$= \frac{\epsilon_{si}}{\epsilon_{ox}} \left(\frac{2V_{si} \cdot qN_A^-}{Q_D} \right) t_{ox} + V_{si} = \frac{\epsilon_{si}}{\cancel{\epsilon_{ox}}} \left(\frac{2V_{si} qN_A^-}{\sqrt{2\epsilon_{si} qN_A^- V_{si}}} \right) \left(\frac{\cancel{\epsilon_{ox}}}{C_{ox}} \right) + V_{si}$$

$$\Rightarrow \boxed{V_G = \frac{\sqrt{2q\epsilon_{si} N_A V_{si}}}{C_{ox}} + V_{si}}, \quad C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

→ threshold voltage

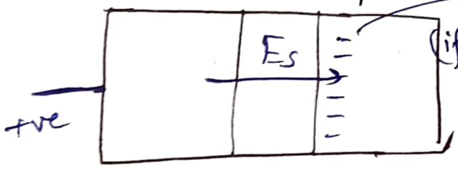
24-02-2025

$$V_{si} = 2V_T \ln \frac{N_A}{n_i}$$
$$\epsilon_r(si) = 11.8$$
$$N_A = 10^{15}/cm^3 \; (p\text{-}si)$$

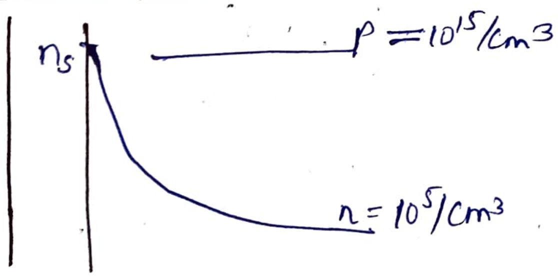
$$V_G = \frac{\sqrt{2q\epsilon N_A V_{si}}}{C_{ox}} + V_{si}$$
(0.5V) (at threshold)

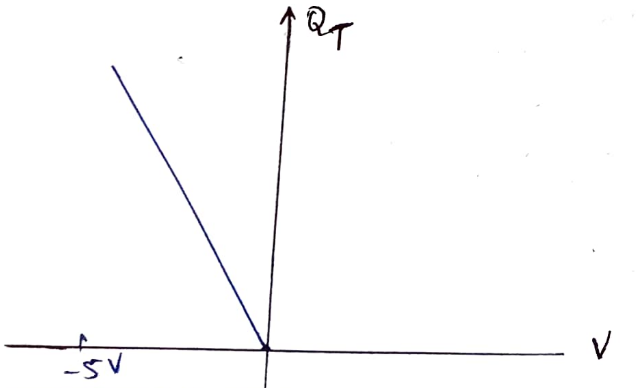
$$V_{th} = \frac{\sqrt{2q\epsilon N_A \psi}}{C_{ox}} + V_{si} \; (\text{or } \psi)$$
(1V)

or V_{si} or ϕ_t : surface / si-potential → $2V_T \ln \frac{N_A}{n_i}$



→ $e^\ominus$ → $\ominus$ve charge ⇒ NMOS
(if) holes → $\oplus$ve ⇒ PMOS





$$V_G = \frac{\sqrt{2q\epsilon N_A V_{si}}}{C_{ox}} + V_{si} \quad \cdots (1)$$

$$V_G = V_{ox} + V_{si}$$

$$= E_{ox} t_{ox} + V_{si}$$

$$= \frac{-Q_T}{\epsilon_{ox}} \cdot t_{ox} + V_{si}$$

$$= \frac{-Q_T}{C_{ox}} + V_{si} \quad \cdots (2)$$

$$= -\frac{(Q_D + \cancel{Q_i}^{\approx 0})}{C_{ox}} + V_{si} \quad \cdots (3)$$

As $Q_D = -\sqrt{2q\epsilon N_A V_{si}}$

$$\Rightarrow V_{si} = \frac{Q_D^2}{2q\epsilon N_A}$$

$$\therefore \boxed{V_G = \frac{-Q_D}{C_{ox}} + \frac{Q_D^2}{2q\epsilon N_A}}$$

Gauss law:

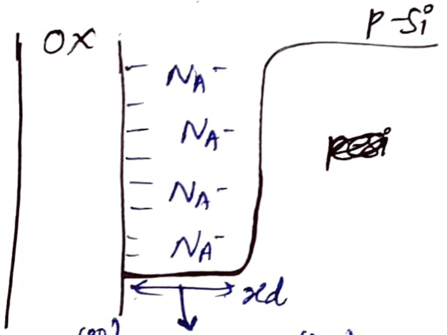
$$\epsilon_{ox} \cdot E_{ox} = E_{si} \cdot \epsilon_{si}$$

$$E_{ox} = \frac{E_{si}}{\epsilon_{ox}} \cdot \epsilon_{si}$$

$$= \frac{-Q_T}{\epsilon_{si} \cdot \epsilon_{ox}} \cdot \epsilon_{si}$$

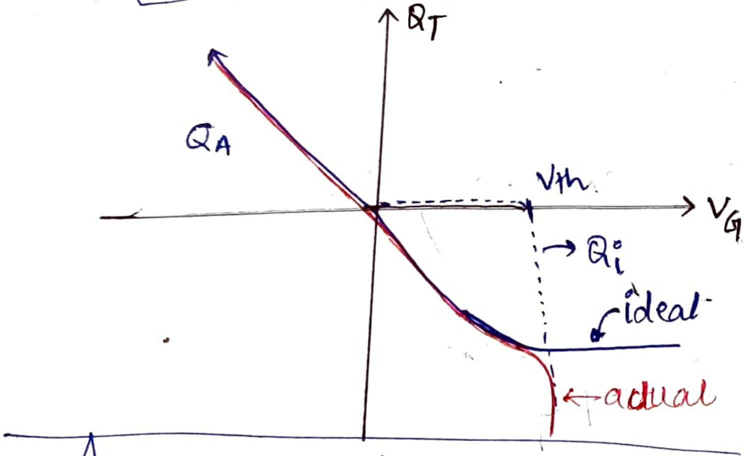
Q_T → total ($N_A^- + e^-$); N_A^- → depletion charge; e^- → inverted charge

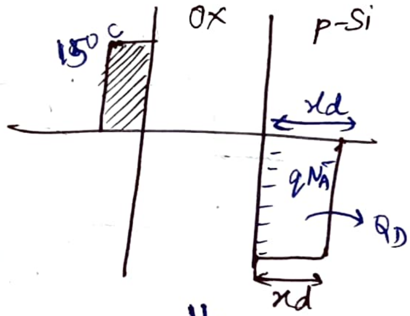
$$= \frac{-Q_T}{\epsilon_{ox}} \quad [\because Q_T = \epsilon_{si} \cdot E_{si}]$$



(80) $Q_{N_A^-} \gg Q_i$ (20)

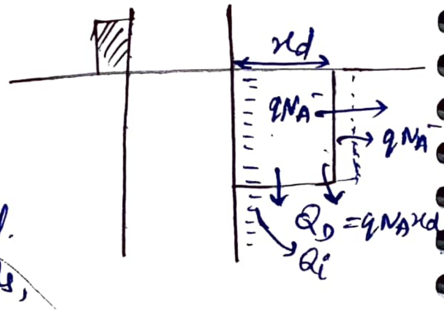
$\underbrace{Q_{N_A^-}}_{\text{depletion charge}(=Q_D)}$; Q_i → inverted charge





⇓

$V_G' > V_{th}$:



As V_G increases from V_{th},
x_d has to expand (surface potential ↑)
but $\psi = 2V_T \ln \frac{N_A}{n_i}$ (related by log).
For ψ to increase significantly,
V_G has to be increased by large amound.
so, as a result, inversion charge expands,
and $\boxed{x_d \approx \text{constant}}$

$$V_{th} = \frac{\sqrt{2q \epsilon N_A V_{si}}}{C_{ox}} + V_{si}$$

$$= -\frac{Q_D}{C_{ox}} + \psi$$

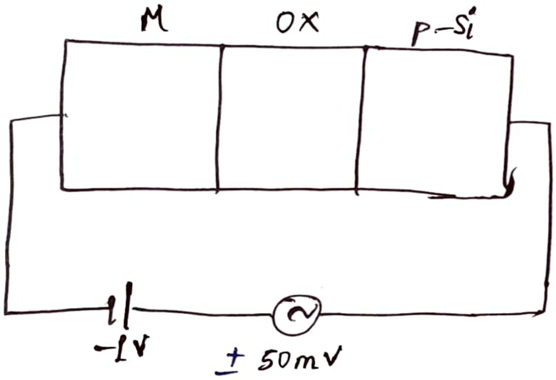
$$V_G' = -\left(\frac{Q_D + Q_i}{C_{ox}}\right) + \psi$$

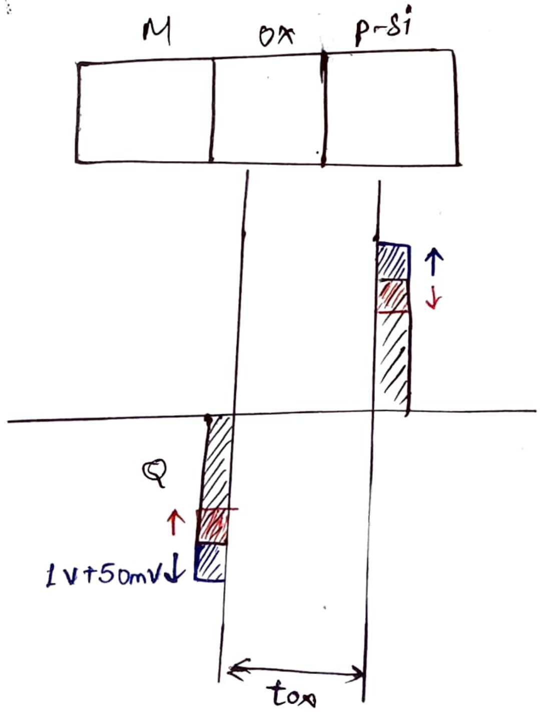
$$= \left(-\frac{Q_D}{C_{ox}} + \psi\right) + \left(\frac{-Q_i}{C_{ox}}\right)$$

$$= V_{th} + \left(\frac{-Q_i}{C_{ox}}\right)$$

$$\therefore \boxed{Q_i = -(V_G' - V_{th})\, C_{ox}}$$

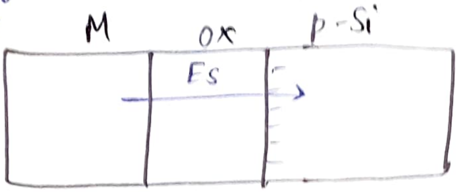
25-02-2025

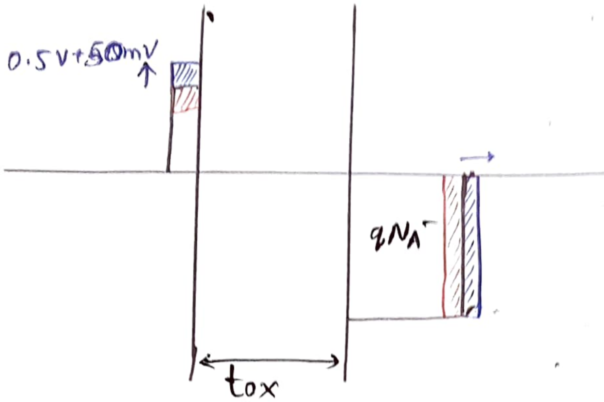




$$C = \frac{\epsilon}{t_{ox}} / \text{Area}$$

Depletion mode:

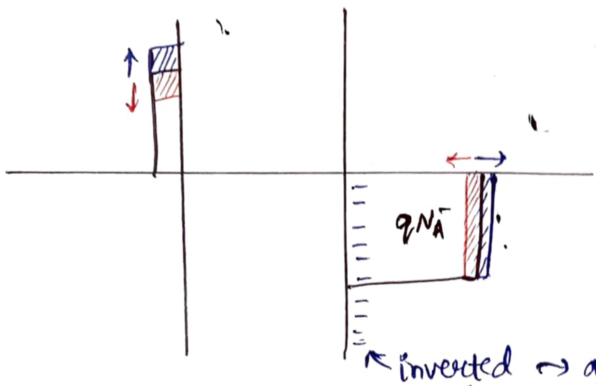




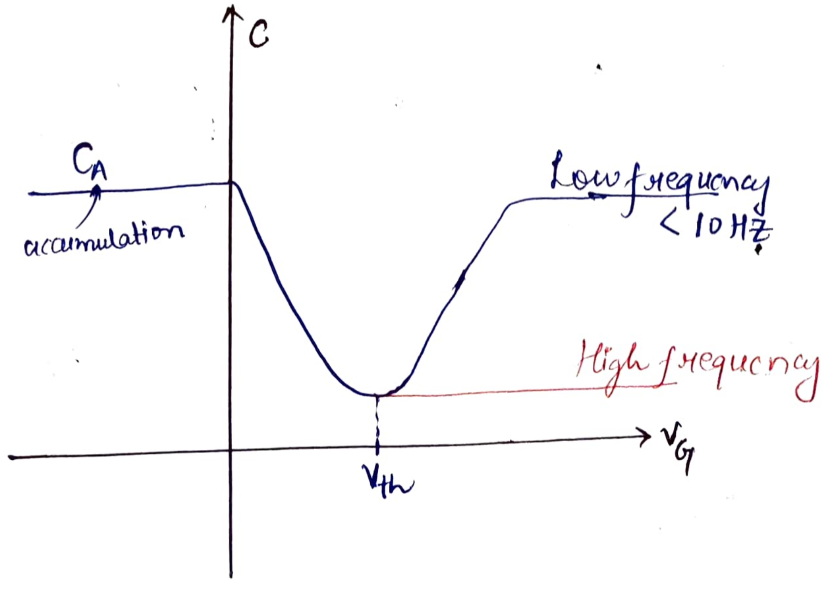
C_{ox}, C_D

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \quad ; \quad C_D = \frac{\epsilon_{Si}}{x_d}$$

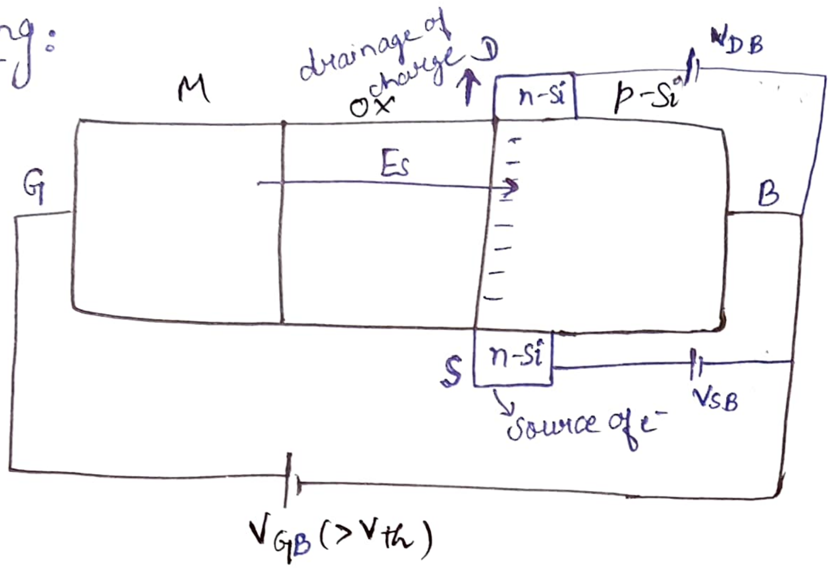
Say, $V_{th} = 1V$, $V_G = 1.5V$

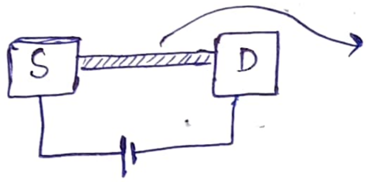


inverted charge → at low freq. get enough time



Biasing:



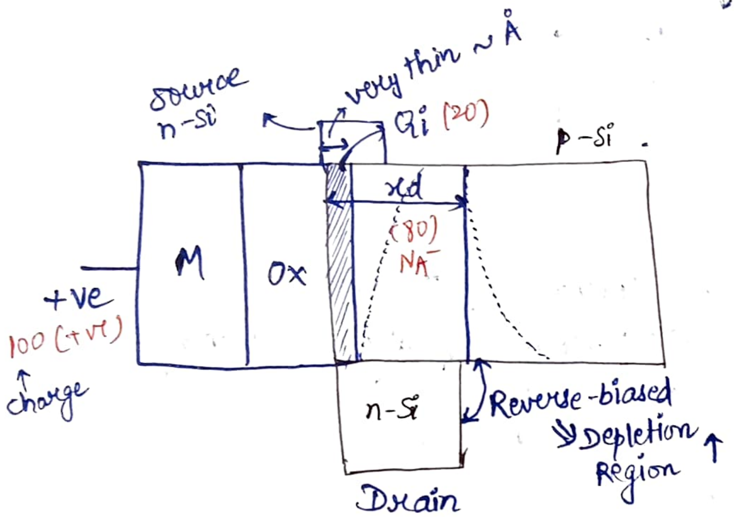


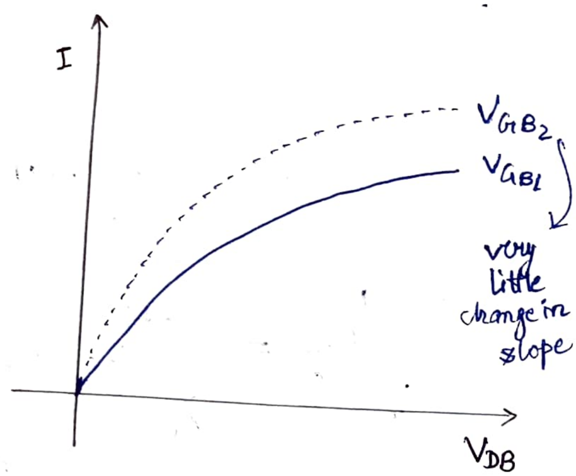
$R = \rho \frac{l}{A}$: controlled by V_G

$J = q n \mu E$ (in inverted zone)

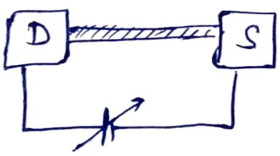
[E: $\frac{V \text{ b/w D \& S}}{\text{dist.}}$]

$\boxed{28\text{-}02\text{-}2025}$



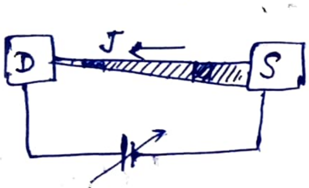


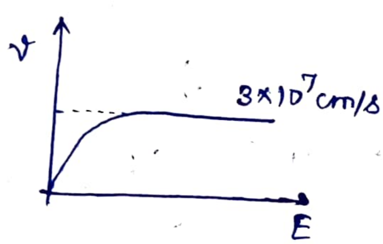
100 (+ve) ≈ Q_i (20) + Q_D (80)



$\uparrow R = \rho \frac{l}{A\downarrow}$

$\Downarrow$ $V\uparrow$



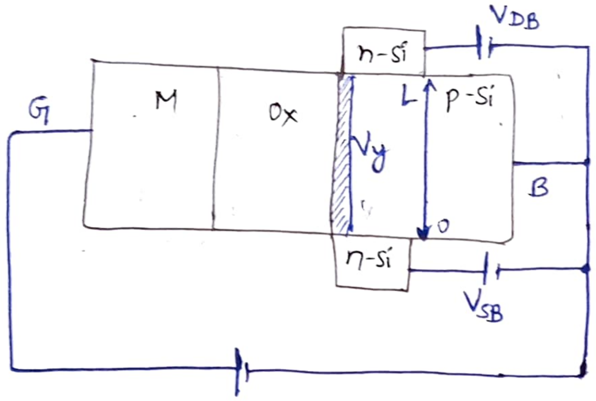


$J = q n v$
$\quad\;\downarrow\;\uparrow$

$$V_{th} = \psi + \sqrt{\frac{2q\epsilon N_A \psi}{C_{ox}}}$$

$$= \psi + \gamma\sqrt{\psi}$$

$$V_{th} = \psi + V_y + \gamma\sqrt{\psi + V_y}\,, \quad V_y = V_D - V_s$$



$$I = AJ$$
$$= (w t_i)\, q n_i \mu E,$$ w: thickness of transistor
t_i: thickness of inverted charge
E: $\frac{V \text{ b/w D \& S}}{\text{distance}}$

$$= \underbrace{(q n_i t_i)}_{Q_i}\, w\mu \frac{dV_y}{dy}$$

$$\Rightarrow \int_0^L I\,dy = \int_{V_{SB}}^{V_{DB}} C_{ox}(V_{GB} - V_{th})\, w\mu\, dV_y$$

$$\Rightarrow I = \frac{w\mu C_{ox}}{L} \int_{V_{SB}}^{V_{DB}} (V_{GB} - V_{th})\, dV_y$$

$$= \frac{w\mu C_{ox}}{L} \int_{V_{SB}}^{V_{DB}} \left(V_{GB} - \psi - V_y - \gamma\sqrt{\psi + V_y}\right) dV_y$$

$$\left[\text{let } \psi + V_y = t^2 \Rightarrow dV_y = 2t\,dt\right]$$

$$= \frac{\mu W C_{ox}}{L} \int_{V_{SB}}^{V_{DB}} 2(V_{GB} - t^2 - \gamma t)\, t\, dt$$

$$= \frac{\mu W C_{ox}}{L} \left[2V_{GB}\frac{t^2}{2} - 2\frac{t^4}{4} - 2\gamma\frac{t^3}{3} \right]_{V_{SB}}^{V_{DB}}$$

$$= \frac{\mu W C_{ox}}{L} \left[V_{GB}(\psi + V_y) - \frac{1}{2}(\psi + V_y)^2 - \frac{2}{3}\gamma(\psi + V_y)^{3/2} \right]_{V_{SB}}^{V_{DB}}$$

$$= \frac{\mu W C_{ox}}{L} \left[\left\{ V_{GB}(\cancel{\psi} + V_{DB}) - \frac{1}{2}\overbrace{(\psi + V_{DB})^2}^{\cancel{\psi^2} + 2\psi V_{DB} + V_{DB}^2} - \frac{2}{3}\gamma(\psi + V_{DB})^{3/2} \right\} - \left\{ (V_{GB})(\cancel{\psi} + V_{SB}) - \frac{1}{2}\underbrace{(\psi + V_{SB})^2}_{\cancel{\psi^2} + 2\psi V_{SB} + V_{SB}^2} - \frac{2}{3}\gamma(\psi + V_{SB})^{3/2} \right\} \right]$$

$$= \frac{\mu W C_{ox}}{L} \left[\left(V_{GB}\cdot V_{DB} - V_{DB}^2 - \psi V_{DB} \right) - \frac{2}{3}\gamma(\psi + V_{DB})^{3/2} - \left(V_{GB} \times V_{SB} - V_{SB}^2 - \psi V_{SB} \right) + \frac{2}{3}\gamma(\psi + V_{SB})^{3/2} \right]$$

$$= \frac{\mu W C_{ox}}{L} \left[(V_{GB} - \psi)(V_{DB} - V_{SB}) - \frac{V_{DB}^2 - V_{SB}^2}{2} - \frac{2\gamma}{3}\left\{ (\psi + V_{DB})^{3/2} - (\psi - V_{SB})^{3/2} \right\} \right]$$

Generally, S and B are short.

$$\therefore\ I = \frac{\mu W C_{ox}}{L} \left[(V_{GS} - \psi) V_{DS} - \frac{V_{DS}^2}{2} - \frac{2\gamma}{3}\left\{ (\psi + V_{DS})^{3/2} - \psi^{3/2} \right\} \right]$$

$$\left[\begin{aligned} (V_{DS} + \psi)^{3/2} &= \psi^{3/2}\left(1 + \frac{V_{DS}}{\psi}\right)^{3/2} \\ &= \psi^{3/2}\left(1 + \frac{3}{2}\frac{V_{DS}}{\psi}\right), \quad \psi \gg V_{DS} \\ &= \psi^{3/2} + \frac{3}{2} V_{DS}\sqrt{\psi} \end{aligned} \right]$$

$$\Rightarrow\ I = \frac{\mu W C_{ox}}{L} \left[(V_{GS} - \psi) V_{DS} - \frac{V_{DS}^2}{2} - \gamma V_{DS}\sqrt{\psi} \right]$$

$$= \frac{\mu W C_{ox}}{L} \left[(V_{GS} - \psi - \gamma\sqrt{\psi}) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$$\therefore\ \boxed{I = \frac{\mu W C_{ox}}{L} \left[(V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right]}$$

18-03-2025

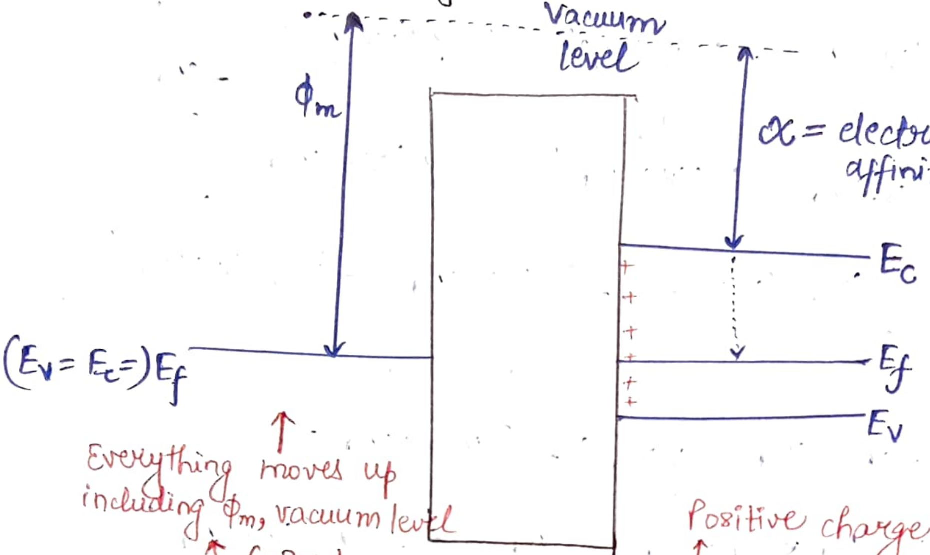
MOSFET – Band Diagram

M	Ox	p-Si

p-Si → $(10^{15}/cm^3)$

$$V_{th} = \frac{\sqrt{2q\epsilon N_A \psi}}{C_{ox}} + \psi$$

Perfect Band Diagram:



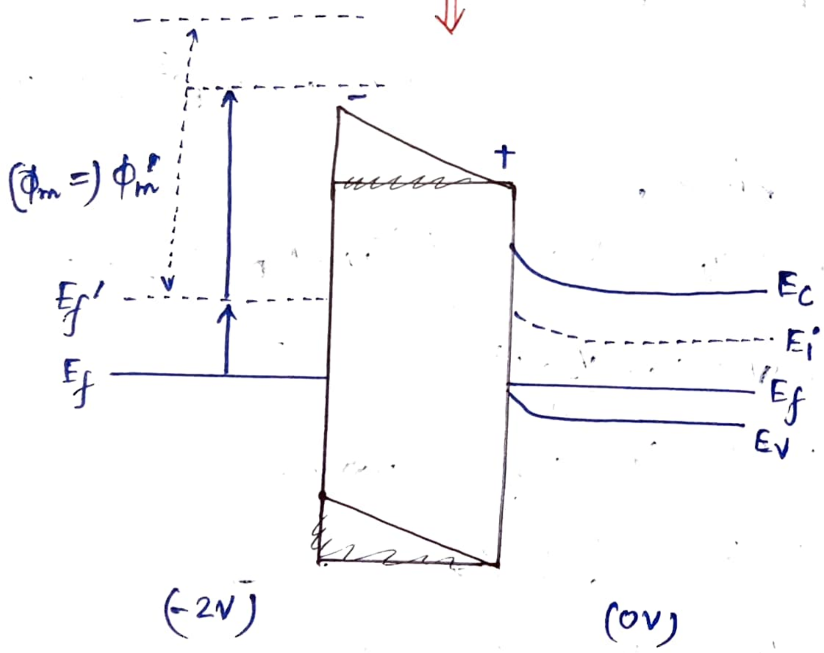
ϕ_m: work function of metal
↳ constant

ϕ_{si} / E_f: variable (on Temp.)
↳ Not a good choice

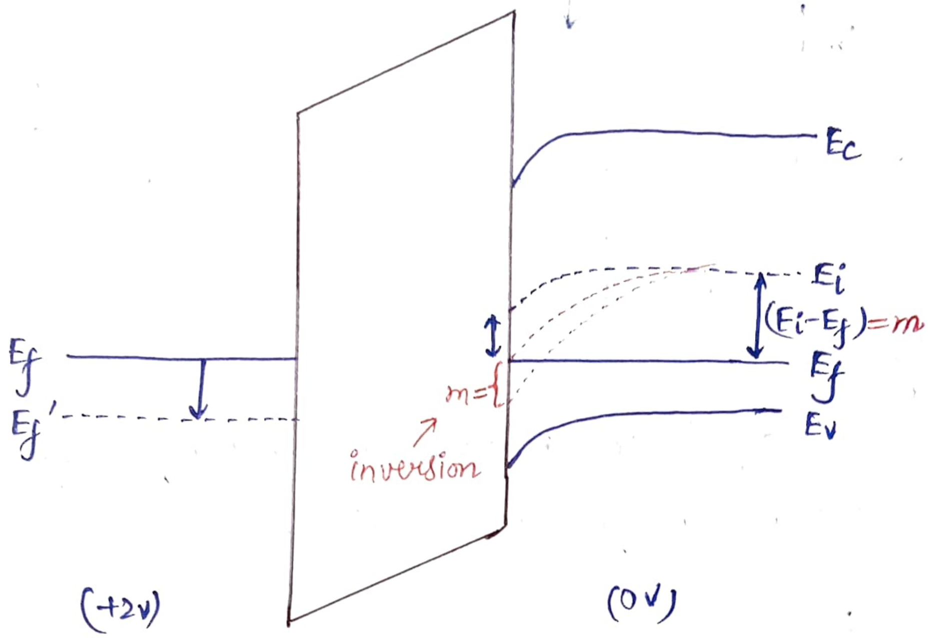
Everything moves up including ϕ_m, vacuum level
(−2V)

Positive charge accumulation (Moves down)
(0V)
↳ fermi level moves towards valence band

⇓



In depletion region :



$(E_i - E_f) > 0$: Positive charge (holes) majority carriers

$$p = p_i e^{(E_i - E_f)/KT}$$

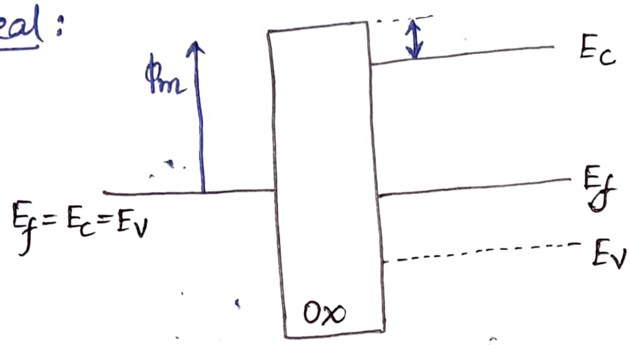
$$\Rightarrow p = 10^{15} = n_i e^{(E_i - E_f)/KT} \quad : \text{Depletion}$$

$$n = 10^{15} = n_i e^{(E_i - E_f)/KT} \quad : \text{Inversion}$$

$$\Psi = \underbrace{2V_T}_{\text{b/c of } m} \ln \frac{N_A}{n_i}$$

Non-Idea MOS

Ideal:

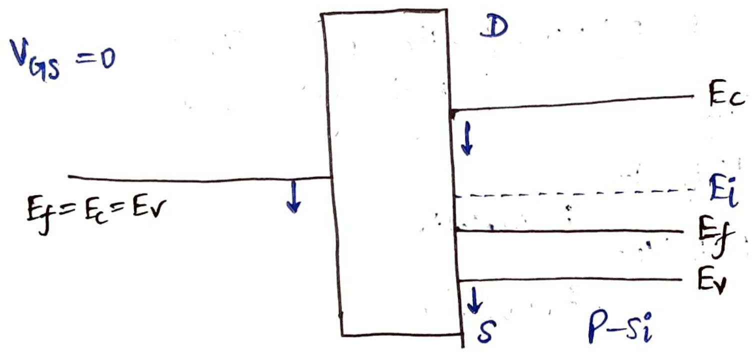


Si and SiO_2 combination
↳ good and smooth

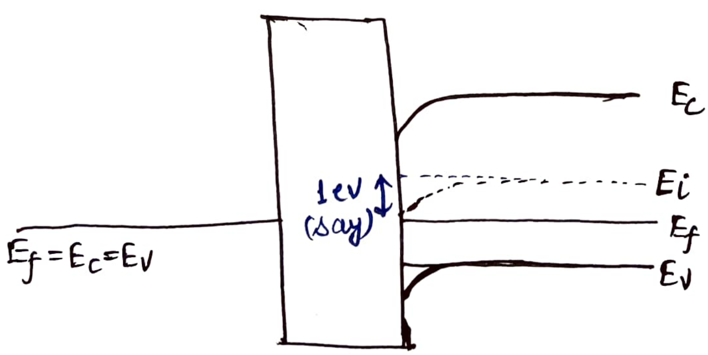
Ideality:

1. Fermi-level of Si and metals are already aligned.
2. There are no charges inside oxide.

Non-ideal:

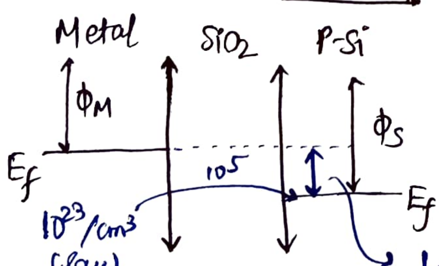


↓



[Partially inverted; without any voltage]

↳ V_{th} decreases.



$$|\phi_M - \phi_S| = 4eV - 3eV = 1eV$$

$$10^{23} - 10^5 \approx 10^{23}/cm^3$$

$$V_{th} = \psi + \frac{\sqrt{2q\epsilon N_A \psi}}{C_{ox}}$$

$\downarrow \; (\phi_m - \phi_s) - Q_F/C_{ox}$

$$V_{th} = \psi \pm V_{FB} + \frac{\sqrt{2q\epsilon N_A \psi}}{C_{ox}}$$

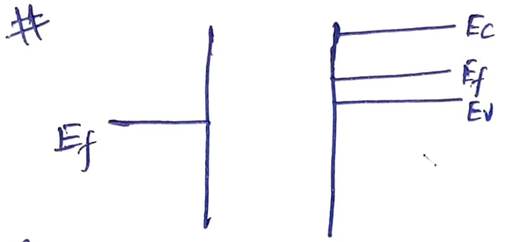
$\downarrow$

1eV [Flat Band]

$\downarrow$

$(\phi_M - \phi_S)$

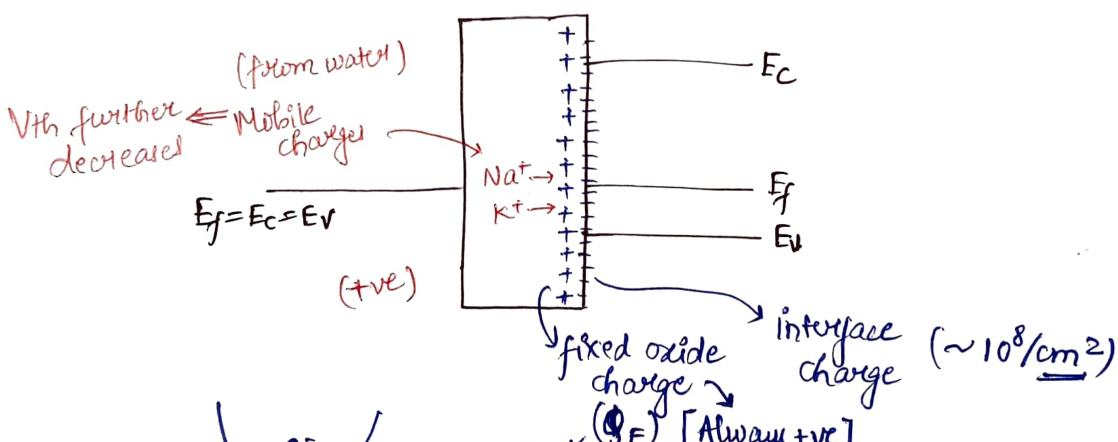
#



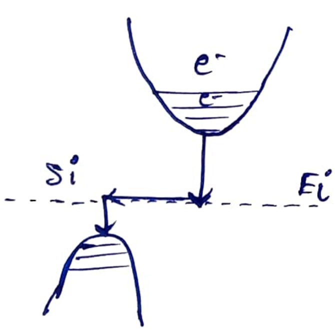
$\Rightarrow$ V_{th} increases.

<u>Charges:</u>

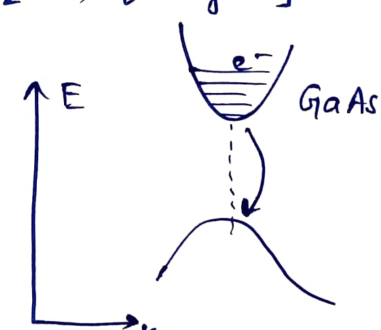
1. Fixed Oxide charge
2. Interface charge
3. Mobile charge



$\left(\frac{-Q_F}{C_{ox}}\right)$



Indirect Bandgap



Direct Bandgap.

$(\phi_M - \phi_s)$ → energy scale + $\left(\frac{-Q_F}{C_{ox}}\right)$ → voltage scale

$$V_{th} = \psi \pm V_{FB} + \frac{\sqrt{2q\epsilon N_A \psi}}{C_{ox}}$$

→ decreases for PMOS
→ increases for NMOS

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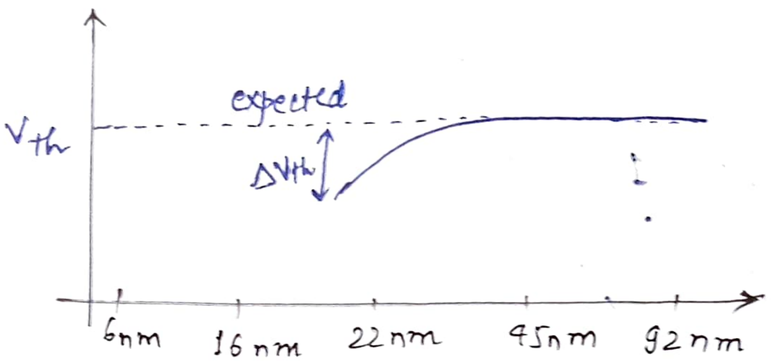
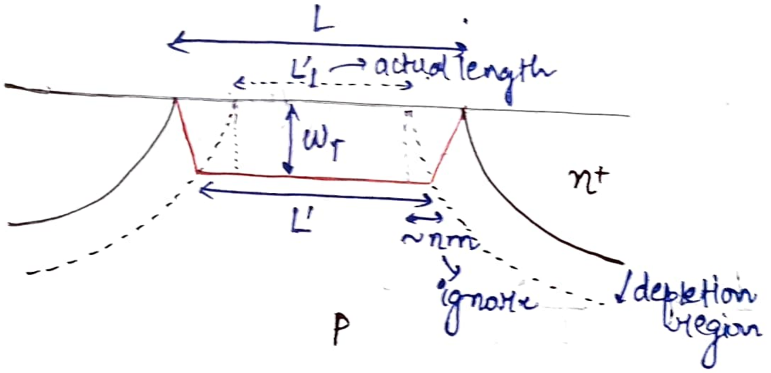


→ Charge Sharing Model (Yau's)

180 nm $\xrightarrow[0.7]{}$ 132 nm / 126 nm $\xrightarrow[0.7]{}$

ΔV_{th} = Threshold voltage swing
= 0 (expected)



Assumption-①:
Actual length $= L' \ (\approx L_1')$

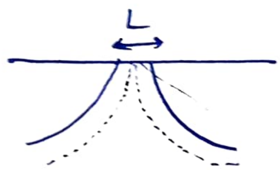
Assumption-②:
Depletion region charge is confined in the area of the trapezium.

$$V_{th} = \Psi + \frac{-Q_T}{C_{ox}}$$

$$Q_T = \frac{-q\left(\frac{L+L'}{2}\right) W_T \, Z \, N_A}{ZL}$$, Z: depth (into the paper)

$$\underset{\text{(long channel)}}{Q_T} = -q N_A W_T \left(\frac{L+L'}{2L}\right)$$

$$= -q N_A W_T \qquad (\because L \approx L')$$



V_{th} (long channel)
↓
$L \approx L'$

$$\underset{\text{(short channel)}}{Q_T} = -q N_A W_T \left(\frac{L+L'}{2L}\right)$$

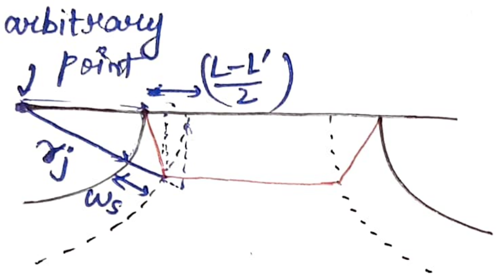
$$\Delta V_{th} = V_{th}(\text{long}) - V_{th}(\text{short})$$

$$= \cancel{\psi} + \frac{-Q_T(\text{long})}{C_{ox}} - \cancel{\psi} - \frac{-Q_T(\text{short})}{C_{ox}}$$

$$= +\frac{qN_A W_T}{C_{ox}} - \frac{qN_A W_T}{C_{ox}}\left(\frac{1}{2} + \frac{L'}{2L}\right)$$

$$= \frac{qN_A W_T}{2C_{ox}} - \frac{qN_A W_T}{2C_{ox}}\left(\frac{L'}{L}\right)$$

$$= \frac{qN_A W_T}{C_{ox}}\left(\frac{L-L'}{2L}\right)$$



r_j : junction depth

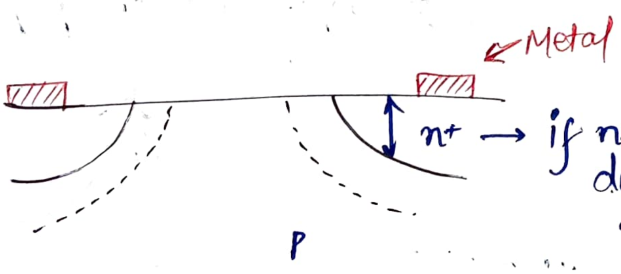
$W_S \approx x_d$

$$(r_j + W_S)^2 = W_T^2 + \left(r_j + \frac{L-L'}{2}\right)^2 \quad \text{[Pythagorus theorem]}$$

$$\Downarrow$$

$$\therefore \Delta V_{th} = -\frac{qN_A W_T}{C_{ox}\uparrow} \frac{r_j\downarrow}{L}\left[\sqrt{1 + \frac{2W_T}{r_j}} - 1\right]$$

$$\uparrow C_{ox} = \frac{\epsilon}{t_{ox}\downarrow}$$



n^+ → if n^+ is too thin, depositing a metal on source or drain can short it with p. → Source-Drain Engineering

↳ $W_T \downarrow$ ✗

$N_A \downarrow$ but for scaling $N_A \uparrow$.

$r_j \downarrow$

$\Rightarrow L\uparrow$ but $L\downarrow$ (scaling)

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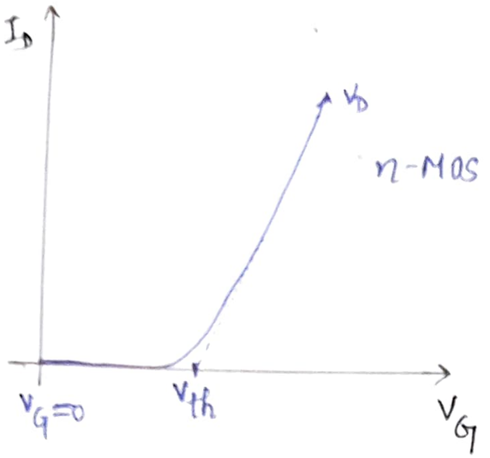
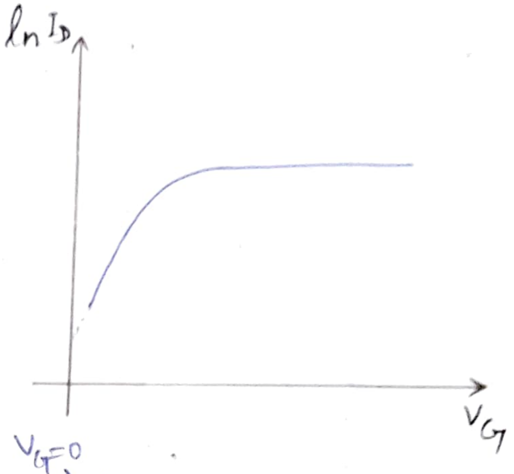
Sub-Threshold slope

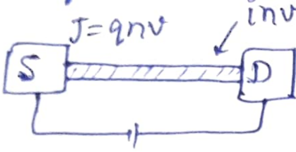




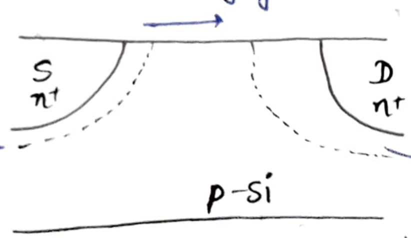
$I_D \neq 0$
↳ current is draining

$$J = qnv$$
$$= qn\mu E$$
$$\Rightarrow I_D = A\,(qn\mu E)$$

inverted charge



density gradient ⇒ e^- flows



⇒ D→S voltage applied

reverse-biased
↳ large depletion region
↳ more depleted of charge carriers

less depletion
↓
more charge carriers

$$\downarrow J = qD_n \frac{dn}{dx\uparrow}\ ,$$

for long channel, ~~to~~ channel length is small
⇓
J can be neglected
(not for short channel)

$$J = qD\,\frac{n(S) - n(D)}{L}\ ,$$

$$n(S) = n_{p_0} \exp\left(\frac{q\psi}{KT}\right)$$

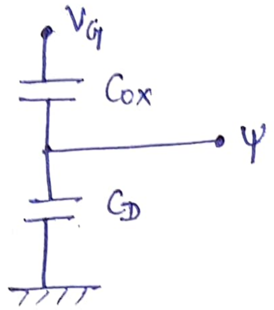
$$n(D) = n_{p_0} \exp\left(\frac{q(\psi - V_{DS})}{KT}\right)$$

[Boltzmann approximation]

$$\Rightarrow J = qD\frac{n_{p_0}}{L}\left(\exp\left(\frac{q\psi}{KT}\right) - \exp\left(\frac{q(\psi - V_{DS})}{KT}\right)\right)$$

$$= qD\frac{n_{p_0}}{L}\exp\left(\frac{q\psi}{KT}\right)\underbrace{\left[1 - \exp\left(-\frac{qV_{DS}}{KT}\right)\right]}_{\text{constant }(k)}$$

$$= qD\frac{n_{p_0}}{L}\exp\left(\frac{q\psi}{KT}\right).k \quad , \quad \psi: \text{variable}$$



$$\psi = \frac{C_{ox}}{C_{ox}+C_D}.V_G \quad \text{[capacitance divider]}$$

$$= \frac{V_G}{1+\frac{C_D}{C_{ox}}} = \frac{V_G}{m}$$

$$\Rightarrow I_D = qD\frac{n_{p_0}}{L}\exp\left(\frac{q\psi}{KT}\right).kA$$

$$\Rightarrow I_D = qD\frac{n_{p_0}}{L}\exp\left(\frac{qV_G}{mKT}\right).kA$$

$$\Rightarrow \cancel{\log}\ \ln I_D = \ln\left(\left(qD\frac{n_{p_0}}{L}\right)kA\right) + \frac{qV_G}{mKT}$$

$$\frac{d\ln I_D}{dV_G} = \frac{q}{mKT} = \frac{1}{mV_T}$$

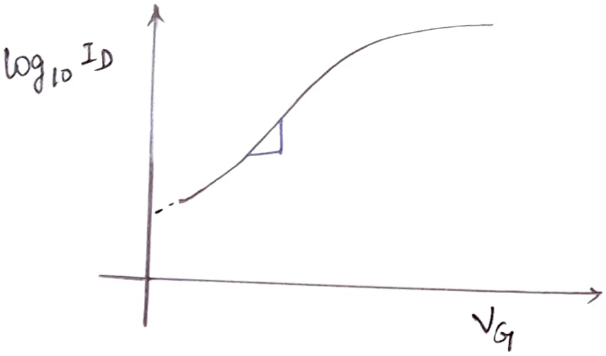
$$\frac{d\log_{10} I_D}{dV_G} = \frac{1}{2.3\,mV_T}$$

$$S = 2.3\,mV_T$$

$$= 60\left(1+\frac{C_D}{C_{ox}}\right)\text{ mV/decade}$$

$$= 60 \text{ mV/decade, for } \frac{C_D}{C_{ox}} \approx 0.$$

$$> 60 \text{ mV/decade}$$



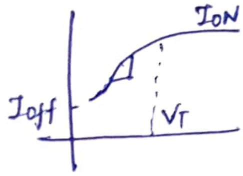
<u>eg.</u> $S = 100$ mV/decade

$I_{ON} = 1mA$

$V_T = 0.6V = 600mV$

$$I_{off} = \frac{1mA}{10^6} = 10^{-9} A.$$

$$\frac{I_{ON}}{I_{off}} = 10^{(V_T/S)} = 10^9.$$



$$\frac{1}{S} = \frac{\log_{10} I_{ON} - \log_{10} I_{off}}{V_T}$$

$$\Rightarrow \frac{V_T}{S} = \log_{10}\left(\frac{I_{ON}}{I_{off}}\right)$$

$$\Rightarrow I_{off} = \frac{I_{ON}}{10^{V_T/S}}$$

18-03-2025

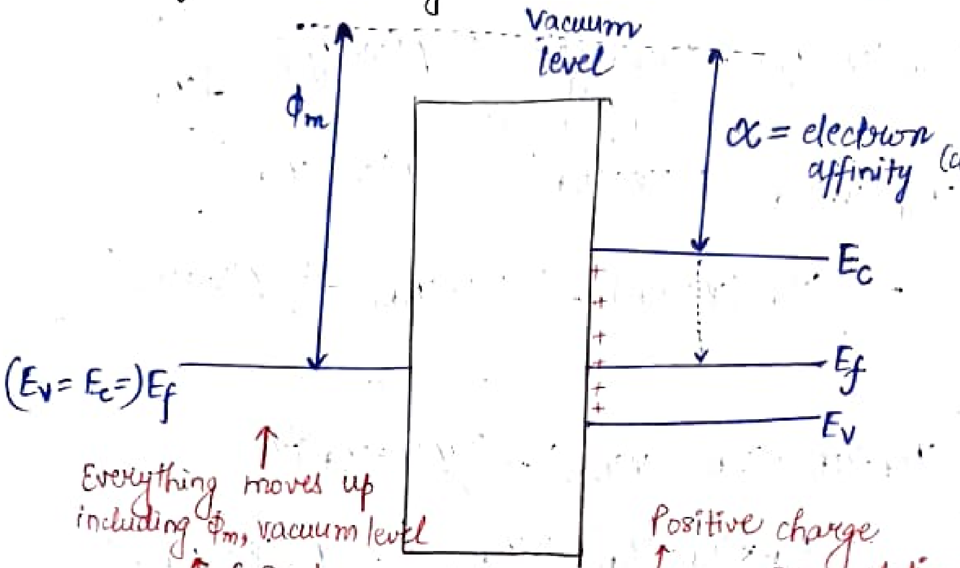
MOSFET – Band Diagram

M	Ox	p-Si

p-Si → ($10^{15}/cm^3$)

$$V_{th} = \frac{\sqrt{2q\epsilon N_A \psi}}{C_{ox}} + \psi$$

Perfect Band Diagram:



ϕ_m: work function of metal → constant

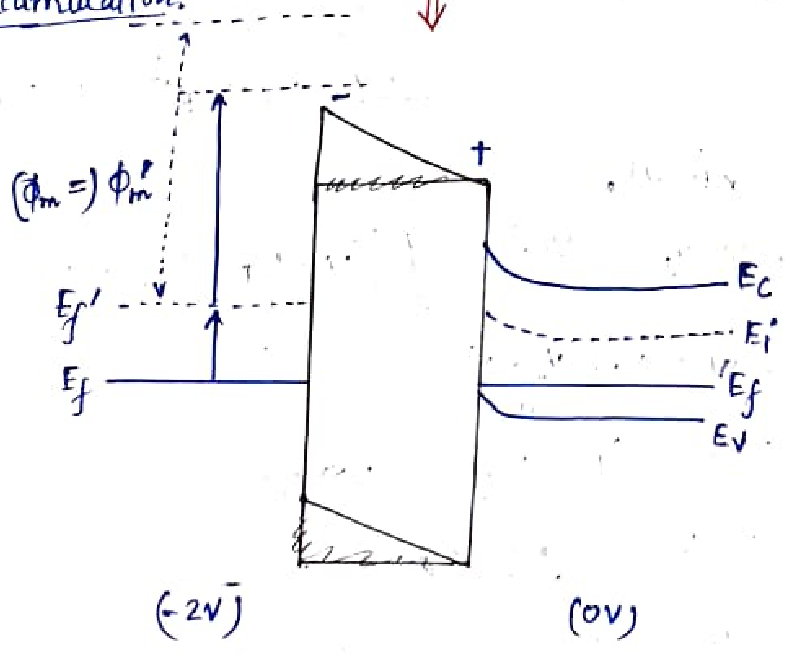
ϕ_{si} / E_f : variable (on Temp.) → Not a good choice

Everything moves up including ϕ_m, vacuum level (−2V)

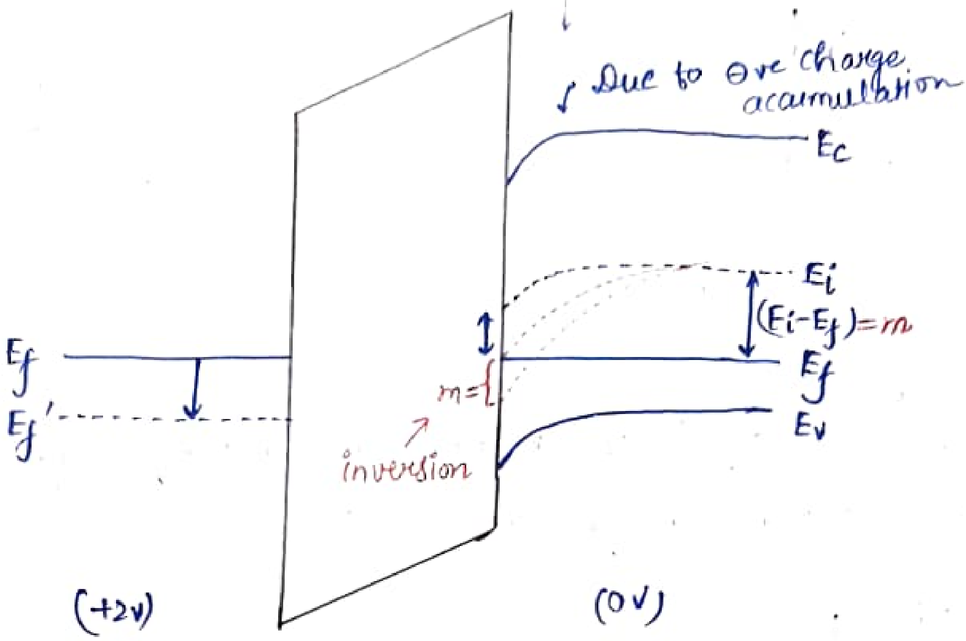
Positive charge accumulation (Moves down) (0V)

→ fermi level moves towards valence band

Accumulation:



In depletion region :



$(E_i - E_f) > 0$: Positive charge (holes) majority carriers

$p = p_i e^{(E_i - E_f)/kT}$

$\Rightarrow p = 10^{15} = n_i e^{(E_i - E_f)/kT}$: Depletion

$n = 10^{15} = n_i e^{(E_i - E_f)/kT}$: Inversion

$$\Psi = \underbrace{2V_T}_{\text{b/c of } m} \ln \frac{N_A}{n_i}$$

If $E_i - E_f > 0$, then majority carrier is ⊕ve.

If $E_i - E_f$ starts to decrease, then majority carrier shifts from ⊕ve to ⊖ve charge.

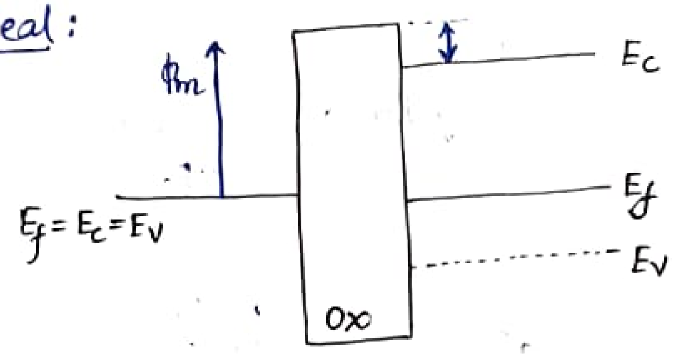
$p = 10^{15}/cm^3$ (depletion).

$n = 10^{15}/cm^3$ (inversion)

If we keep increasing voltage, at the interface, $n \uparrow$ and hence, inversion layer is formed.

Non-Idea MOS

Ideal:

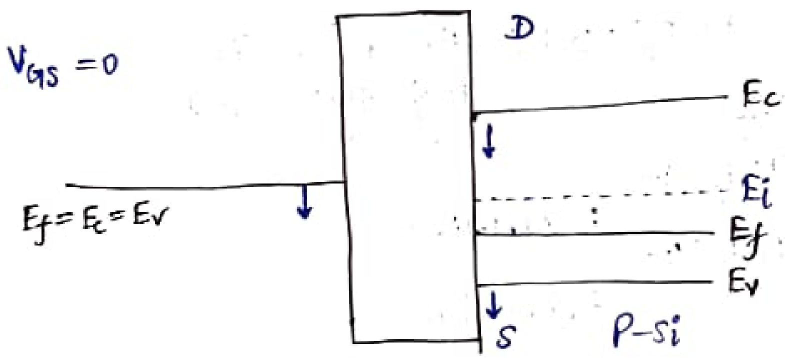


Si and SiO_2 combination
↳ good and smooth

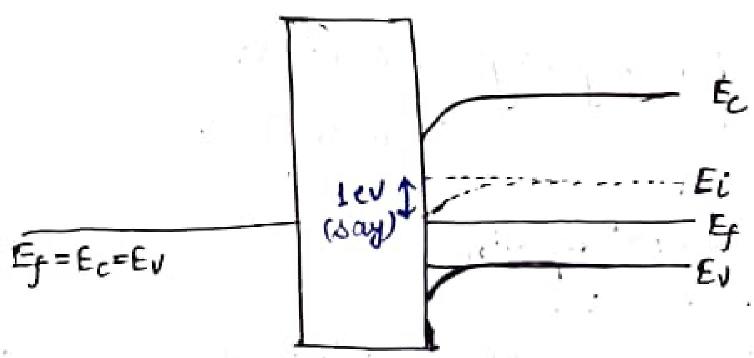
Ideality:

1. Fermi-level of Si and metals are already aligned.
2. There are no charges inside oxide.

Non-ideal:

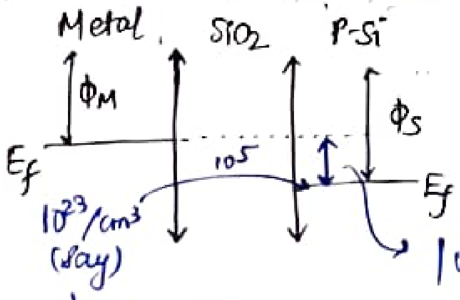


↓



[Partially inverted; without any voltage]

↳ V_{th} decreases.



$10^{23} - 10^5 \approx 10^{23}/cm^3$

$|\phi_M - \phi_S| = 4eV - 3eV$
$= 1eV$

$$V_{th} = \psi + \frac{\sqrt{2q\epsilon N_A \psi}}{C_{ox}}$$

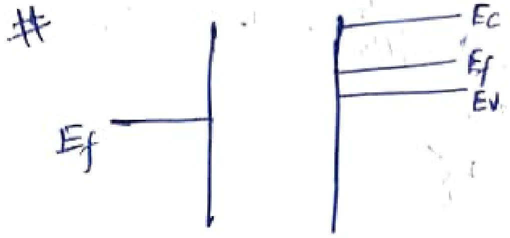
$$\downarrow \quad (\phi_m - \phi_s) - Q_F/C_{ox}$$

$$V_{th} = \psi \pm V_{FB} + \frac{\sqrt{2q\epsilon N_A \psi}}{C_{ox}}$$

1eV [Flat Band]

$(\phi_M - \phi_S)$

#



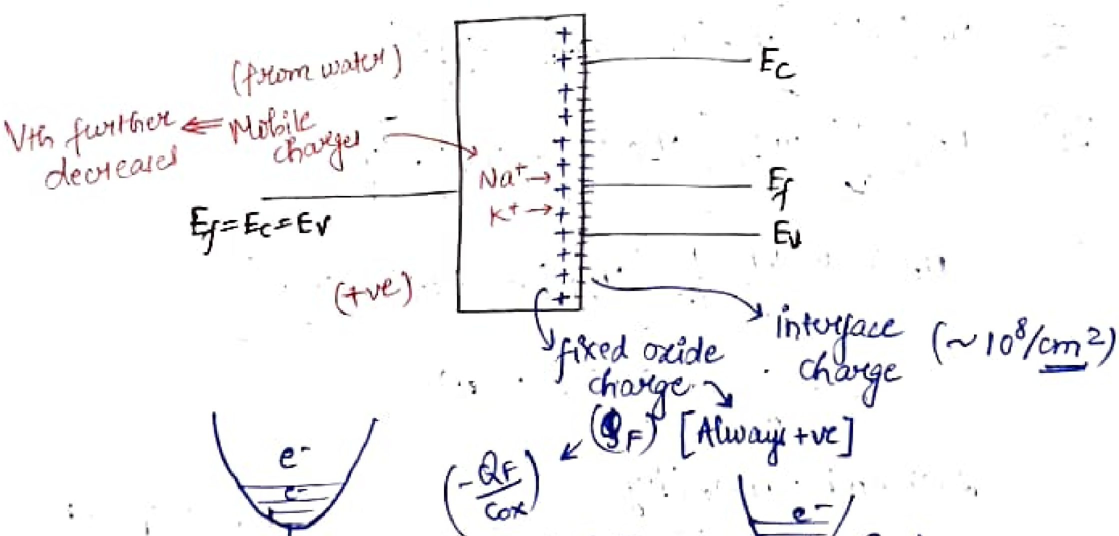
$\Rightarrow$ V_{th} increases.

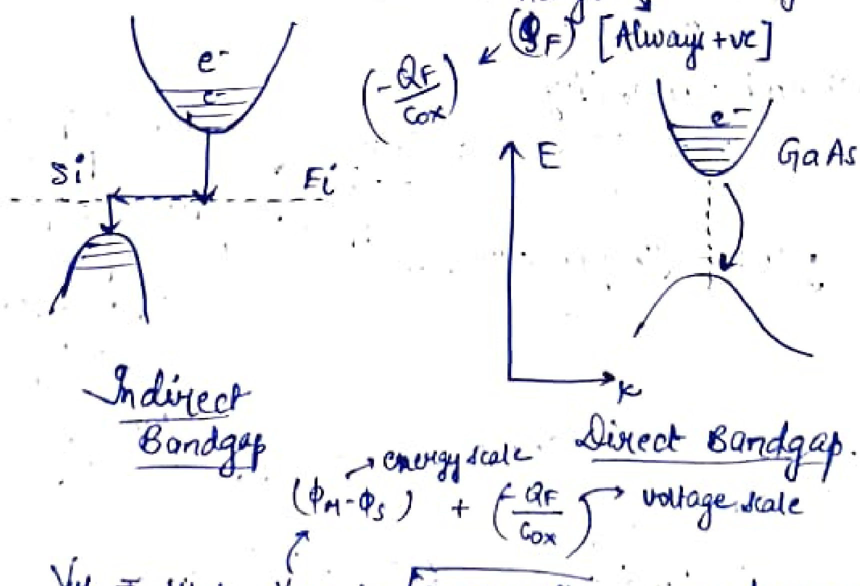
<u>Charges:</u>

① Fixed Oxide Charge

② Interface charge

③ Mobile Charge





<u>Indirect Bandgap</u>

<u>Direct Bandgap</u>

$$(\phi_M - \phi_S) + \left(\frac{-Q_F}{C_{ox}}\right)$$

$(\phi_M - \phi_S)$ → energy scale; $\left(\frac{-Q_F}{C_{ox}}\right)$ → voltage scale

$$V_{th} = \psi \pm V_{FB} + \frac{\sqrt{2q\epsilon N_A \psi}}{C_{ox}}$$

→ decreases for PMOS

→ increases for NMOS

24-03-2025

Scaling

↳ Dennard's rule of CMOS scaling.

[we'll only discuss constant electric field CMOS scaling.]

CSMOS scaling ⇒ constant electric field

Rules:

① All the dimensions are scaled by factor K.

$L \Rightarrow L/K$

$W \Rightarrow W/K$

$t_{ox} \Rightarrow t_{ox}/K$

$x_d = \sqrt{\dfrac{2\epsilon V_{bi}}{qN_A}}$, $N_D \Rightarrow N_D/K$

$\Downarrow$

x_d/K

② All the voltages should be scaled by K.

$V_{DS} \Rightarrow V_{DS}/K$.

Constant electric field,

$$\underset{\text{previous generation}}{E_P} = V_P/L_P = \frac{V_P/K}{L_P/K} = E.$$

Now,

$$I_D = \mu_n \frac{C_{ox} W}{L}\left[V_{DS}(V_{GS}-V_{th}) - \frac{V_{DS}^2}{2}\right]$$

$$I_D' = \mu_n \frac{C_{ox} K^2}{L/\cancel{K}} \cdot W/\cancel{K}\left[\frac{V_{DS}}{K}\left(\frac{V_{GS}}{K}-\frac{V_{th}}{K}\right) - \frac{V_{DS}^2}{2K^2}\right]$$

$$= \mu_n C_{ox} K^2 \cdot \frac{W}{L} \cdot \frac{1}{K^2}\left[V_{DS}(V_{GS}-V_{th}) - \frac{V_{DS}^2}{2}\right]$$

$$C_{ox} = \frac{C}{A} \Rightarrow \frac{C}{A}K^2 = C_{ox} \cdot K^2$$

Determine mobility,

$$\tau = \frac{CV}{I} \Rightarrow K^2 C \cdot \frac{V/K}{I/K^2} \downarrow \text{ (speed ↑)}$$

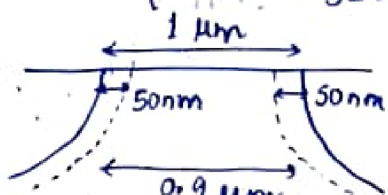
$$\downarrow V_{th} = \frac{\sqrt{2qN_D\epsilon\psi}}{C_{ox}} + \psi$$

BJT: speed ↑, power consumption ↑

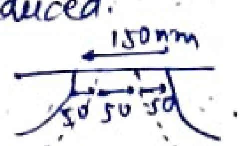
MOSFET: speed ↓, power consumption ↓

↳ Find perfect configuration: BICMOS device

→ V_{th} will decrease as channel length is reduced.



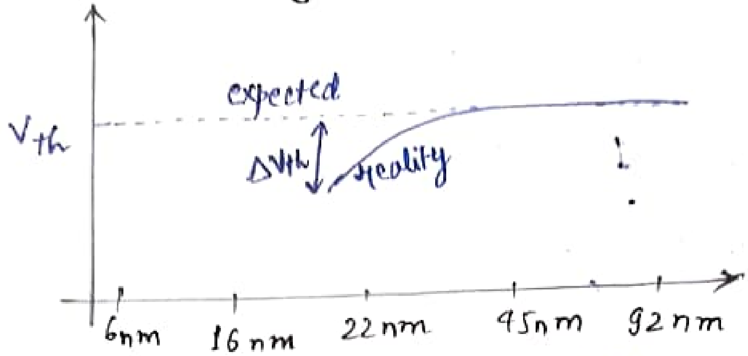
⇐



(short channel effect)

25-03-2025

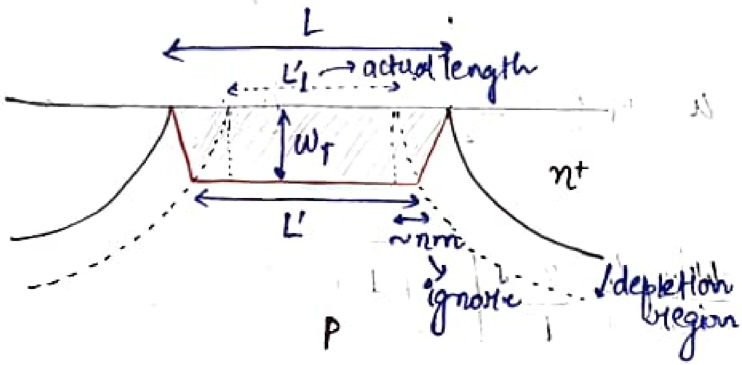
Threshold voltage swings :



→ Charge Sharing Model (Yau's)

$$180\,nm \xrightarrow[0.7]{} \begin{matrix} 132\,nm \rightarrow \text{(actually)} \\ 126\,nm \end{matrix} \xrightarrow[0.7]{}$$ [Normally K factor is 0.7]

ΔV_{th} = Threshold voltage swing
= 0 (expected)



Assumption - ① :
Actual length = L' (≈ L'₁)

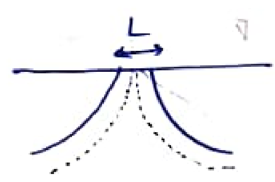
Assumption - ② :
Depletion region charge is confined in the area of the trapezium.

$$V_{th} = \Psi + \frac{-Q_T}{C_{ox}}$$

$$Q_T = \frac{-q\left(\frac{L+L'}{2}\right) W_T \cdot Z \; N_A}{ZL}$$, Z : depth (into the paper)

$$\underset{\text{(long channel)}}{Q_T} = -q N_A W_T \left(\frac{L+L'}{2L}\right)$$

$$= -q N_A W_T \qquad (\because L \approx L')$$



V_{th} (long channel)
↓
$L \approx L'$

$$\underset{\text{(Short channel)}}{Q_T} = -q N_A W_T \left(\frac{L+L'}{2L}\right)$$

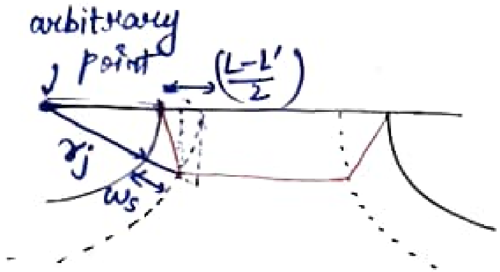
$$\Delta V_{th} = V_{th}(\text{long}) - V_{th}(\text{short})$$

$$= \psi + \frac{-Q_T(\text{long})}{C_{ox}} - \cancel{\psi} - \frac{-Q_T(\text{short})}{C_{ox}}$$

$$= +q\frac{N_A w_T}{C_{ox}} - q\frac{N_A w_T}{C_{ox}}\left(\frac{1}{2} + \frac{L'}{2L}\right)$$

$$= q\frac{N_A w_T}{2C_{ox}} - q\frac{N_A w_T}{2C_{ox}}\left(\frac{L'}{L}\right)$$

$$= q\frac{N_A w_T}{C_{ox}}\left(\frac{L-L'}{2L}\right)$$



r_j : junction depth

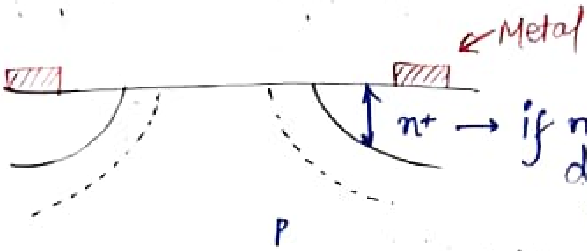
$w_s \approx x_d$

$$(r_j + w_s)^2 = w_T^2 + \left(r_j + \frac{L-L'}{2}\right)^2 \quad \text{[Pythagoras theorem]}$$

$$\Downarrow$$

$$\therefore \Delta V_{th} = -\frac{qN_A w_T}{C_{ox}\uparrow}\,\frac{r_j\downarrow}{L}\left[\sqrt{1 + \frac{2w_T}{r_j}} - 1\right]$$

$$\uparrow C_{ox} = \frac{\epsilon}{t_{ox}\downarrow}$$



→ if n^+ is too thin, depositing a metal on source or drain can short it with p. → Source-Drain Engineering

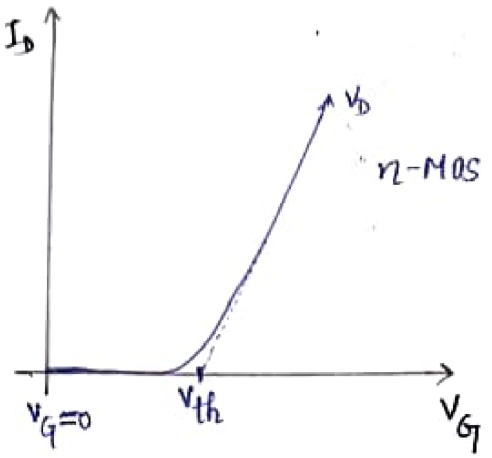
↳ $w_T \downarrow$ ✗

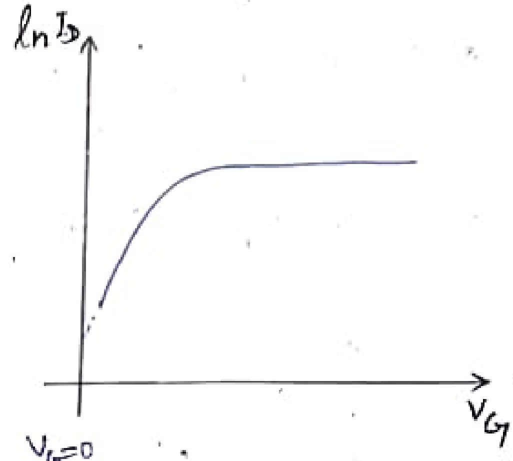
$N_A \downarrow$ but for scaling $N_A \uparrow$.

$r_j \downarrow$

$\Rightarrow L\uparrow$ but $L\downarrow$ (scaling)

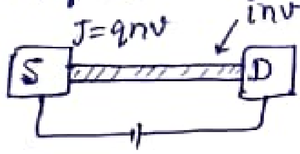
Sub-Threshold slope



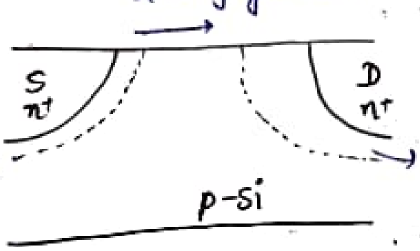


$V_G=0 \rightarrow I_D \neq 0$
↳ current is draining

$J = qnv$
$= qn\mu E$
$\Rightarrow I_D = A(qn\mu E)$



density gradient ⇒ e^- flows



⇒ D→S voltage applied

reverse-biased
↳ large depletion region
↳ more depleted of charge carriers

Less depletion
↓
more charge carriers

$\downarrow J = qD_n \frac{dn}{dx\uparrow}$, for long channel, ~~to~~ channel length is small
⇓
J can be neglected
(not for short channel)

$J = qD \frac{n(S) - n(D)}{L}$,

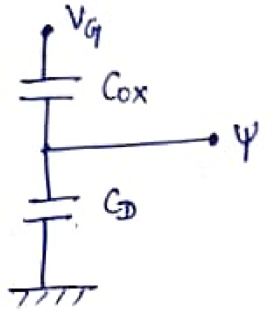
$n(S) = n_{p_0} \exp\left(\frac{q\psi}{KT}\right)$

$n(D) = n_{p_0} \exp\left(\frac{q(\psi - V_{DS})}{KT}\right)$ [Boltzmann approximation]

$$\Rightarrow J = qD\frac{n_{p_0}}{L}\left(\exp\left(\frac{q\psi}{KT}\right) - \exp\left(\frac{q(\psi - V_{DS})}{KT}\right)\right)$$

$$= qD\frac{n_{p_0}}{L}\exp\left(\frac{q\psi}{KT}\right)\underbrace{\left[1 - \exp\left(-\frac{qV_{DS}}{KT}\right)\right]}_{\text{constant } (k)}$$

$$= qD\frac{n_{p_0}}{L}\exp\left(\frac{q\psi}{KT}\right).k \quad , \quad \psi: \text{variable}$$



$$\psi = \frac{C_{ox}}{C_{ox}+C_D}\cdot V_G \quad [\text{capacitance divider}]$$

$$= \frac{V_G}{1+\frac{C_D}{C_{ox}}} = \frac{V_G}{m}$$

$$\Rightarrow I_D = qD\frac{n_{p_0}}{L}\exp\left(\frac{q\psi}{KT}\right).kA$$

$$\Rightarrow I_D = qD\frac{n_{p_0}}{L}\exp\left(\frac{qV_G}{mKT}\right).kA$$

$$\Rightarrow \cancel{\log}\ \ln I_D = \ln\left(\left(qD\frac{n_{p_0}}{L}\right)kA\right) + \frac{qV_G}{mKT}$$

$$\frac{d\ln I_D}{dV_G} = \frac{q}{mKT} = \frac{1}{mV_T}$$

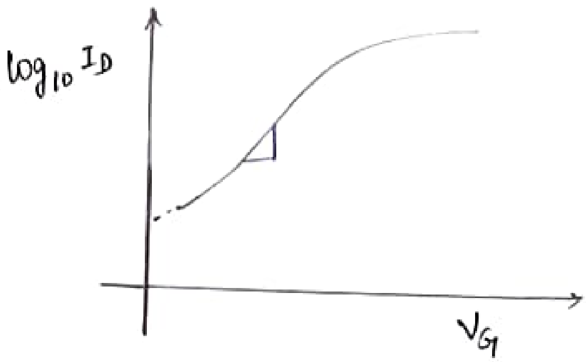
$$\frac{d\log_{10} I_D}{dV_G} = \frac{1}{2.3\,mV_T}$$

$$S = 2.3\,mV_T$$

$$= 60\left(1+\frac{C_D}{C_{ox}}\right) \text{ mV/decade}$$

$$= 60 \text{ mV/decade}, \text{ for } \frac{C_D}{C_{ox}} \approx 0.$$

$$> 60 \text{ mV/decade}$$



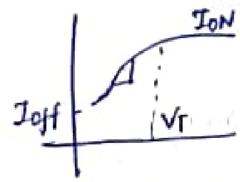
eg. $S = 100\ mV/decade$

$I_{ON} = 1mA$

$V_T = 0.6V = 600\,mV$

$$I_{off} = \frac{1mA}{10^6} = 10^{-9}A.$$

$$\frac{I_{ON}}{I_{off}} = 10^{(V_T/S)} = 10^9.$$



$$\frac{1}{S} = \frac{\log_{10} I_{ON} - \log_{10} I_{off}}{V_T}$$

$$\Rightarrow \frac{V_T}{S} = \log_{10}\left(\frac{I_{ON}}{I_{off}}\right)$$

$$\Rightarrow I_{off} = \frac{I_{ON}}{10^{V_T/S}}$$

04-04-2025

FABRICATION

1. Oxidation
2. Ion Implantation
3. Photo lithography [self study]
4. Etching
5. Metal Deposit [self study]

Oxidation

(1) $Si + O_2\uparrow \xrightarrow{1000^\circ c} SiO_2$ (solid) → Requires activation energy

↳ Temp. ↓ ⇒ Pressure ↑

↳ Looking for low temperature.

diameter		thickness
4′ - Si (4-inch Si wafer)	⟶	≈400 μm
6′ - Si	⟶	≈ 600 μm
8′ - Si	⟶	≈ 800 μm
12′ - Si	⟶	≈1200 μm

Dry oxd^n: To form thin gate oxide layer.

↳ slower, produces denser oxide.

(high quality SiO_2)

O_2 from air

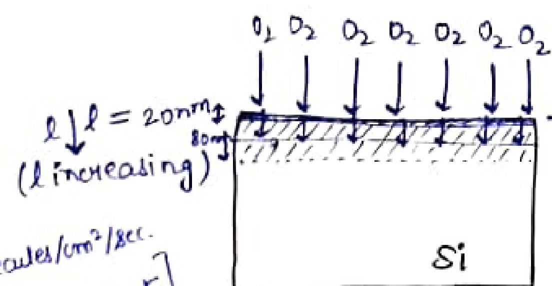
↓

79 % N_2 + 20 % O_2 → carbon contaminants

↳ Pass pure O_2 from gas cylinders.

↳ Dry oxidation process

↳ Not more than 100 nm SiO_2



[Dry oxd^n]

→ First, the top layer converts to SiO_2

→ very slow reaction process (5 - 6 hrs.)

(at 1000°c)

molecules/cm²/sec.

↑

[flux of oxidant (O_2)]

O_2 has diffusivity (density gradient) inside SiO_2

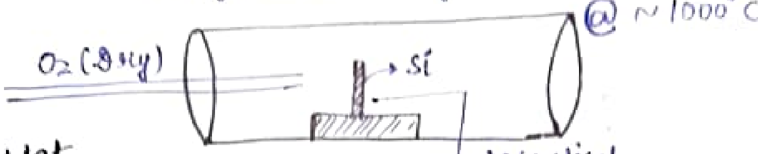
$T_{ox, final} \downarrow$ ~~t_{ox}~~ $\propto D \dfrac{C_{O_2}(out) - C_{O_2}(in)}{l \uparrow}$, C_{O_2} : conc^n of O_2

l : SiO_2 layer thickness

↳ l increases ⇒ tox decreases

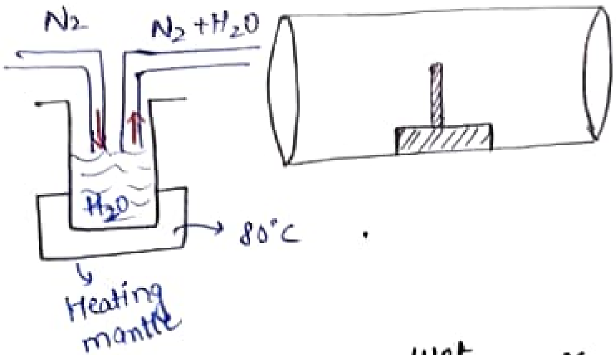
↳ till ~100 nm.

Dry oxidation furnace

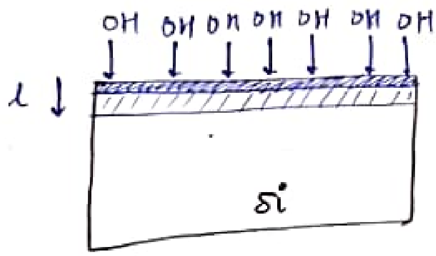


↳ Vertical
↳ To react with O_2

② ~~Dry~~ Wet Oxidation



$$Si + H_2O\uparrow \xrightarrow[1000°c]{wet} \underset{(solid)}{SiO_2} + H_2\uparrow$$

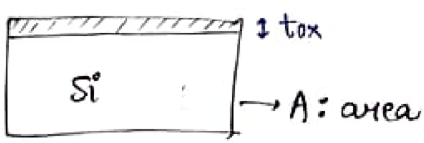


→ Faster growth (field oxide), but lower quality
↳ For isolation

→ 1000 nm

$$\downarrow T_{ox,final} \propto D \frac{C_{OH}(out) - C_{OH}(in)}{l \uparrow}$$

$$H_2O \longrightarrow OH + \underset{\text{(nascent oxygen)}}{O^*\uparrow} \quad + \underset{\text{(H comes out)}}{H}$$



$$\underset{\substack{28 \\ \text{(consumed)}}}{Si} + \underset{32}{O_2} \longrightarrow \underset{\substack{60 \\ \text{(produced)}}}{SiO_2} \quad : \text{mass}$$

$m = D \times V$

For Si,

$28 = 2.3 \times \cancel{tox}\, A\, \underbrace{t_{si}}_{\text{consumed Si thickness}}$

For SiO_2,

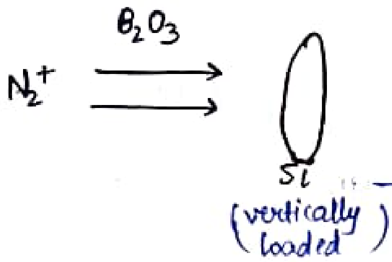
$$60 = 2.3 \times A\, t_{SiO_2} \Rightarrow \frac{t_{SiO_2}}{t_{Si}} \approx 2$$

→ If 1000 nm SiO_2 is produced, 500 nm Si is consumed.
If 50 nm SiO_2 is produced, 25 nm Si is consumed.

07-04-2025

Diffusion → ₹ 5-10 L
OR
Ion implantation → ₹ 10-100 Cr

} Doping

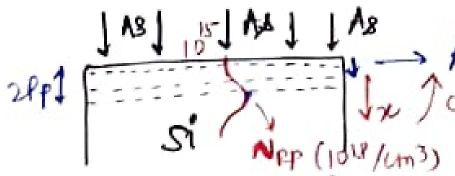


→ Si-B_2 complex (500°C) → B goes as dopant into Si
[B_2O_3 conc^n is low so that boro-silicate does not form]
↓
should ~~not~~ react
↓
to be controlled

Dilution approx:

Si : $10^{22}/cm^3$

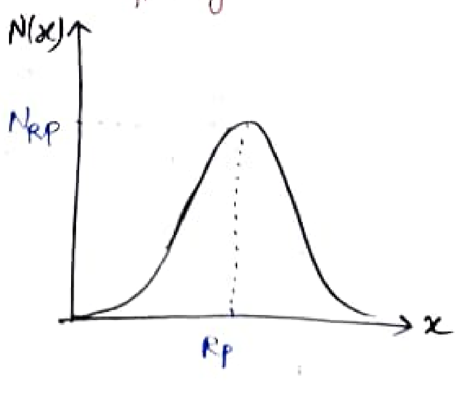
B : $10^{16}/cm^3$



→ As hits Si → Si turns amorphous

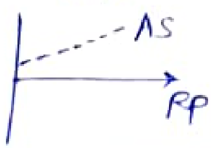
↓x ↑ conc. gradient ⇒ As atoms starts diffusing ⇒ $10^{18}/cm^3$ ↓

$$N(x) = \overset{10^{18}/cm^3}{N_{RP}} \exp\left[\left(\frac{x - R_p}{\sqrt{2}\,\Delta R_p}\right)^2\right] \rightarrow \text{Gaussian}$$



R_p : projected range
ΔR_p : std. deviation

↓ As



Si : ~~amp~~ amorphous → e⁻s can't flow

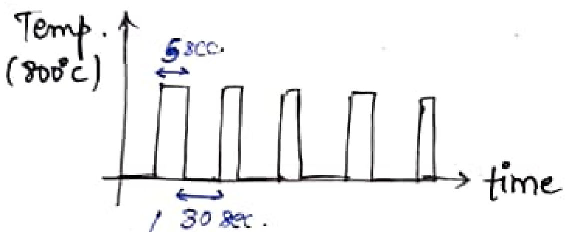
↓ Heat (called Annealing, at 800-900°C)

Crystalline

RTA (Rapid Thermal Annealing) :

↳ we don't want diffusion

Time for crystallity < Time for diffusion
[3 sec. (say)] [10 sec.]

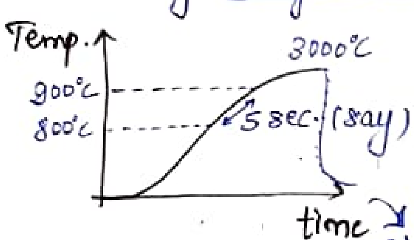


crystallises ↳ don't give chance for diffusion.

↳ Done using Halogen Bulb (multiple)

↳ work in complementary manner

↳ very complicated process



Needs time to turn off

↳ Self bombard Si with Si itself to make it ~~amp~~ amorphous, then dope As.

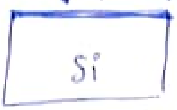
Lift-off = photolithography metal patterning

08-04-2025

Gas Phase Etching

↳ Good for automation

Gas + Si ⟶ Product ↑
(SiO_2, Si_3N_4)



→ if reac^n forms solid layer ⇒ Reac^n stops ⇒ should form gas by-product

Fluorine process : CF_4

✗ SF_4 → decomposes fast → avoided

$$CF_4 \xrightarrow[800°C]{} CF_3 + F^*$$

(nascent fluorine)

$$F^* + Si \longrightarrow SiF_6^{2-} \uparrow$$

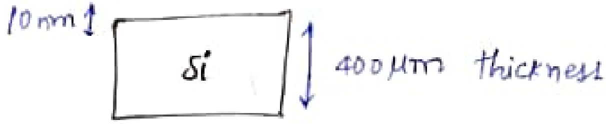
→ very optimised

[Etching rate : constant]

↳ 1nm/sec. (say)

↓

Run the reac^n for 10 sec. (for 10nm etch)



To reduce temp.,

$$CF_4 \xrightarrow[plasma]{<300°C} CF_3 + F^*$$

$$F^* + Si \xrightarrow[plasma]{} SiF_6^{2-} \uparrow$$

↳ ionization/ very high energy state

↳ To provide activation energy (by temp / plasma / light excitation)

$Ar \longrightarrow Ar^+ + e^-$

↳ emits light (blue)

To etch SiO_2, use HF (hydrofluoric acid).

↳ very dangerous

[very less material is available to be used]

$$CF_4 \xrightarrow[plasma]{<300°C} CF_3 + F^*$$

$$H_2 + F^* \longrightarrow HF$$

$$HF + SiO_2 \longrightarrow SiF_6^{2-} \uparrow + H_2$$

→ Etch SiO_2 and not Si [selective etching]

$CF_4 \xrightarrow{plasma} F^* + CF_3$

$F^* + Si_3N_4 \longrightarrow N_2 + SiF_6^{2-} \uparrow$

etches both Si and Si_3N_4

Si_3N_4 etching rate : 0.5 nm/min
Si etching rate = 1 nm/min
(with same F^* recipe)

Deposition :

poly-Si

① $SiH_4 \xrightarrow{plasma} \underset{(polySi)}{Si} + H_2$

② $SiH_4 + N_2O \longrightarrow SiO_2 + N_2$

③ $SiH_4 + O_2 \longrightarrow SiO_2$

④ $SiH_4 + NH_3 \longrightarrow Si_3N_4 + H_2$

SM SZE Book

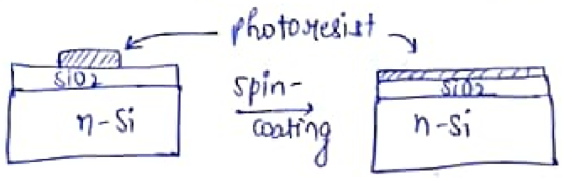
Photolithography

↳ Patterning technique that uses UV light to transfer a geometric pattern from a photomask to a photoresist-coated wafer.
↳ Define regions for etching, doping or deposition.

Steps:

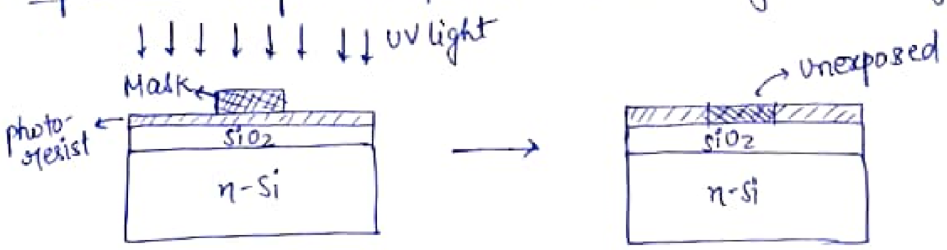
① Spin-coating: Apply few drops of photoresist (liquid polymer) on the wafer and spin the wafer at high speed.
  ↳ Creates a uniform thin layer of photoresist (~1–2 μm).

② Soft-Bake: Bake wafer at ~90–100°c to evaporate the solvent.

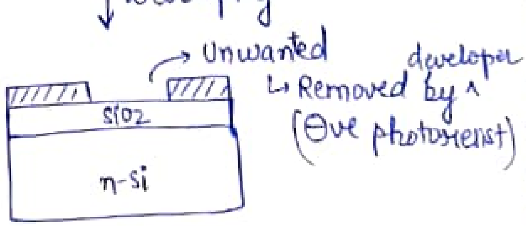


③ Align a photomask ~~with~~ over the wafer.

④ Exposure: Expose the photoresist to UV light through the mask.



Positive photoresist:
  ↳ Exposed regions become soluble.
  ↳ Exposed regions are removed by the developer.



Negative photoresist:
  ↳ Exposed regions become insoluble.
  ↳ Unexposed regions are removed by the developer.

⑤ Development: Wafer is immersed in developer solution.
  ↳ Developer removes soluble regions of the photoresist.

⑥ Hard-Bake: Bake at ~120°–150°c to strengthens the pattern.

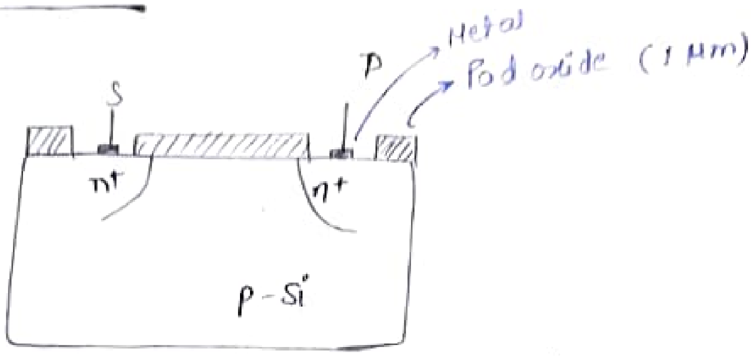
⑦ Etching or Ion implantation → with pattern resist as mask, etch or implant ions into exposed areas. (PR protects selected areas).

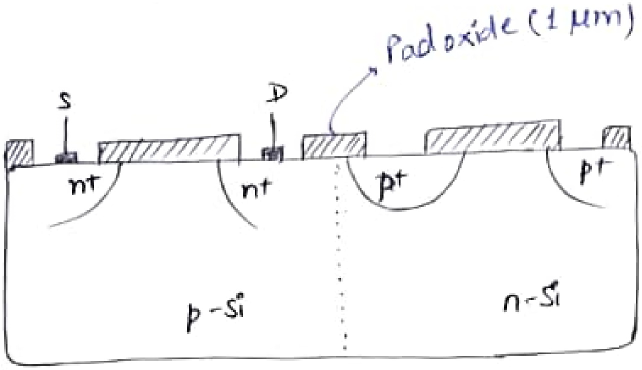
⑧ Photoresist stripping (or strip removal) → Remove photoresist.

21-04-2025

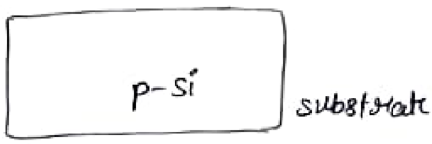
CMOS Fabrication

Structure:

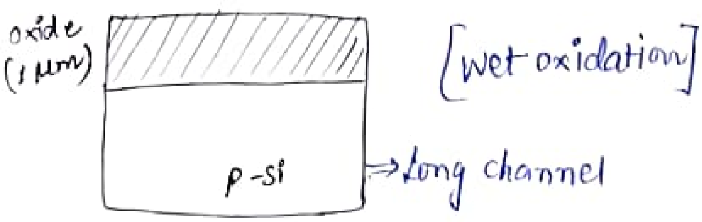




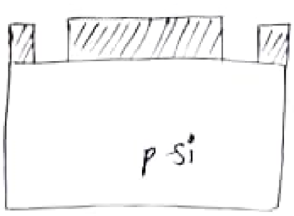
Fabrication:



↓

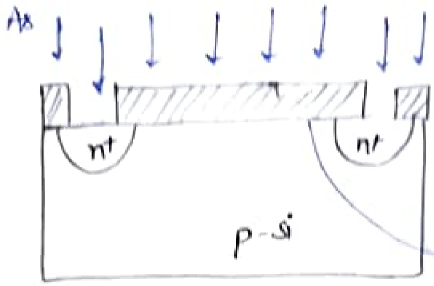


↓



↓

↓



Ion Implantation of As

high energy ions disturbs SiO_2

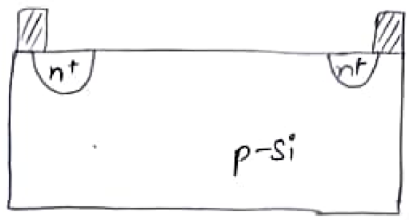
↳ poor quality SiO_2

Take out this SiO_2

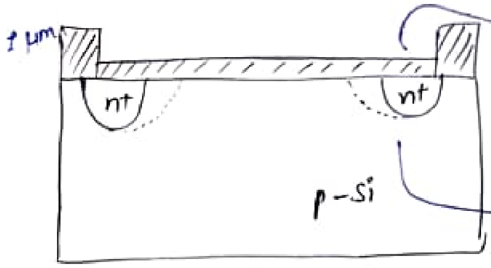
↓

Rapid Thermal Annealing

↓



↓



Realize gate oxide (Thickness ≃ technology) by dry oxidation

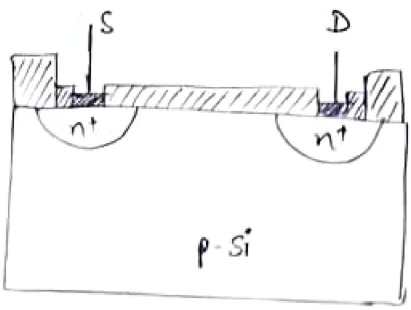
↳ High quality oxide

Expands

↳ due to high temp. of dry oxdn

↳ To be calculated beforehand

↓



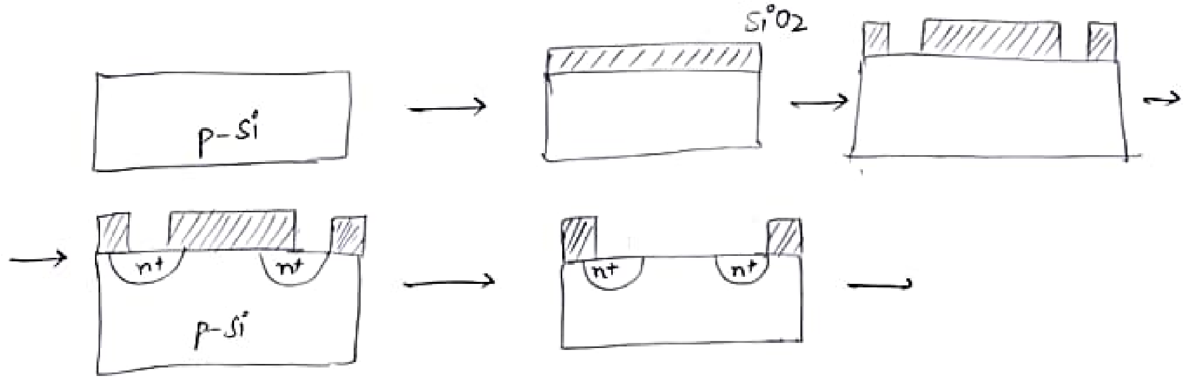
⇒ Metallization

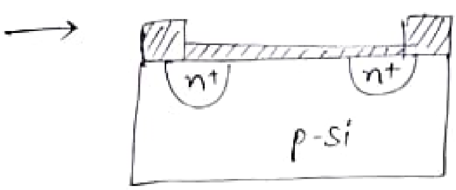
Steps: [write with recipes]

1. Wet oxidation.
2. Photolithography followed by patterning ~~[illegible]~~ and etching of 1 μm SiO_2.
3. Ion implantation of As.
4. Etching of SiO_2 (1 μm) except pad oxide.
5. Dry oxidation.
6. Photolithography with patterning and etching of gate SiO_2.
7. Lift-off for metallization (Al).
8. Wire-bonding for S and D.

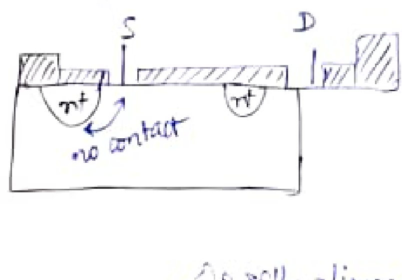
<u>Modification-1:</u>

Self Alignment





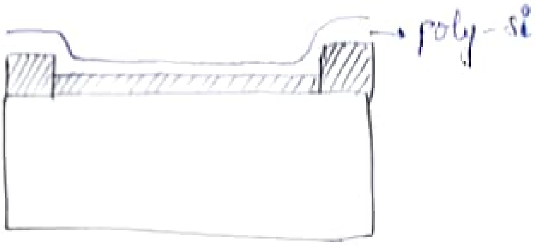
50 nm channel → gate oxide thickness = 10 nm



→ Error in masking [Misalignment] (under 500 nm tech.)

↳ Happens in the whole batch of transistors

Go to self-alignment



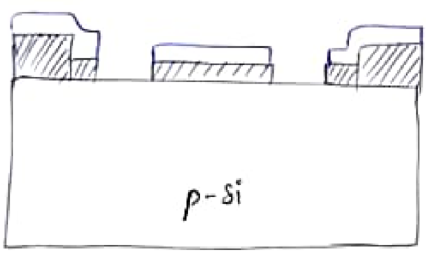
$$SiH_4 \xrightarrow[\text{plasma}]{200^\circ C} Si + H_2$$

OR

$$SiH_4 \xrightarrow[O_2 \text{ free}]{800^\circ C} Si + H_2$$

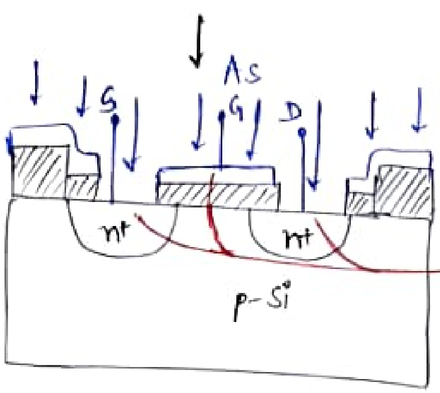
$\Rightarrow$ The chamber should be O_2 free.
↳ Otherwise si and gate SiO_2 will react with O_2.

↓

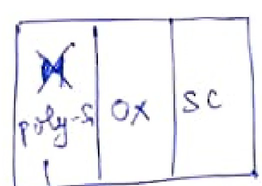


→ First do the opening before implantation

↓



→ Metallization with poly
↳ due to high doping



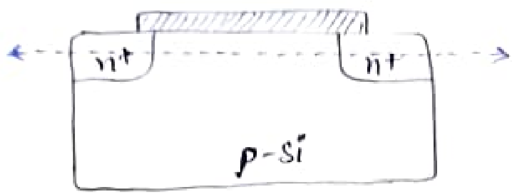
heavily-doped to be metal-like

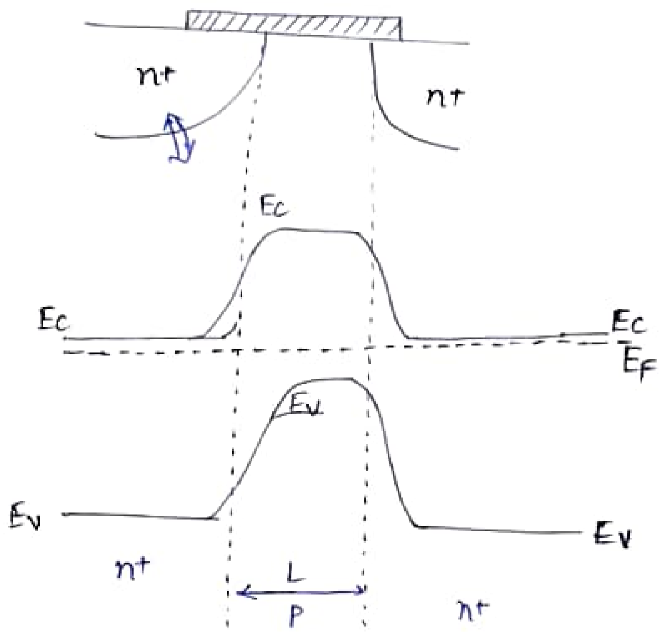
↳ Even if there is misalignment, there won't be any problem, as ion-implantation is happening after the opening

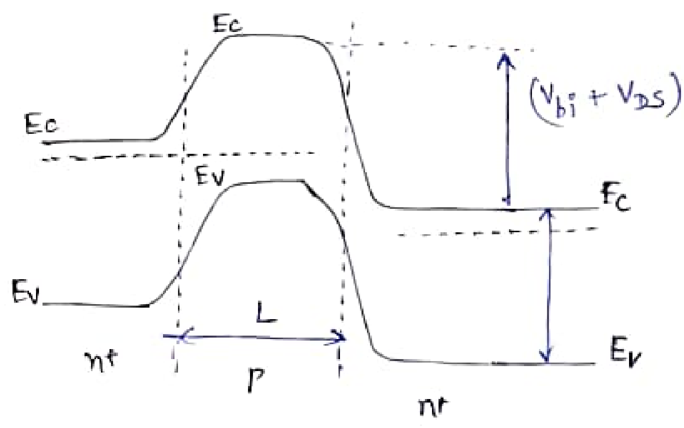
↳ Preferred over the one without self-alignment.

22-04-2025

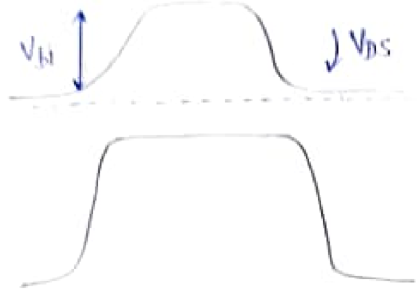
Drain Induced Barrier Lowering (DIBL)

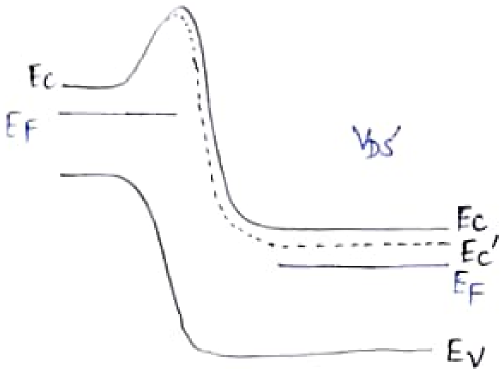






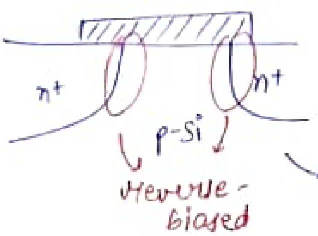
→ Long channel





$$\frac{|V_{th_2} - V_{th_1}|}{|V_{DS_2} - V_{DS_1}|} = \frac{mV}{V}$$

$\Rightarrow$ DIBL



→ Increase doping density

⇒ Mobility ↓

$\Delta V_{th} \downarrow \propto x_j \downarrow$

(threshold voltage swing)

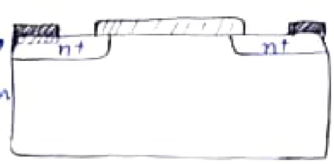
→ Decrease ~~channel length~~ n+ thickness

(Metal Spiking)

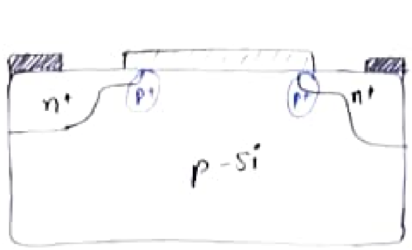
Metal deposition

↓

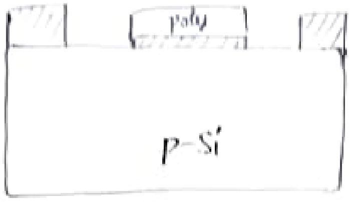
penetrates into n+ and connects with p-Si



↓ Solution

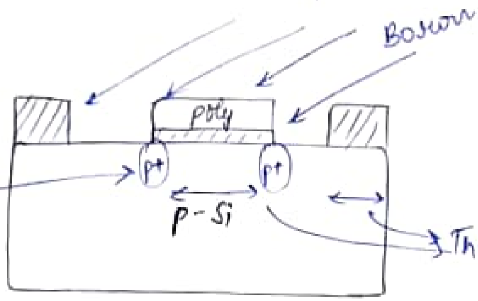


Fabrication :



↓

Halo - Implantation
or
Tilted - implantation

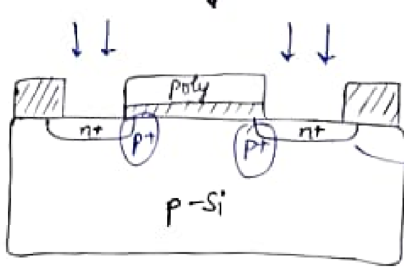


Tilt to other side to get this

These thicknesses are well calculated

↓

Shallow doping or Shallow implantation



Annealing will further make it bulgy, so take (make) it thin for now.

For NMOS - S_b → antimony (heavy) → less deposition
PMOS - N_i

} diffusion

E_1 ——— +ve electrode → -ve

e^- ↑

$Ar \rightleftharpoons Ar^+ + e^-$

collide e^-

heavy nucleus ⇓ less mobile ← Ar^+

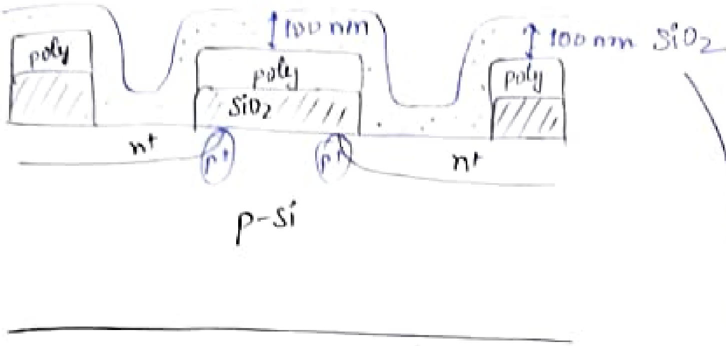
Si Si

E_2 ——— -ve electrode → +ve

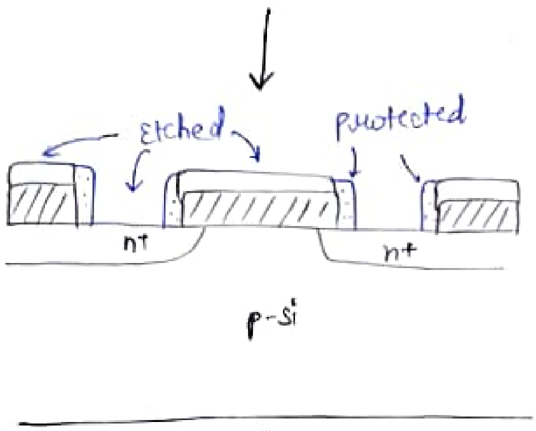
Place a $Si / SiO_2 / Si_3N_4$ material
↳ Gets bombared with Ar^+
↳ Gets etched

Then ~~so~~ toggle the electrodes

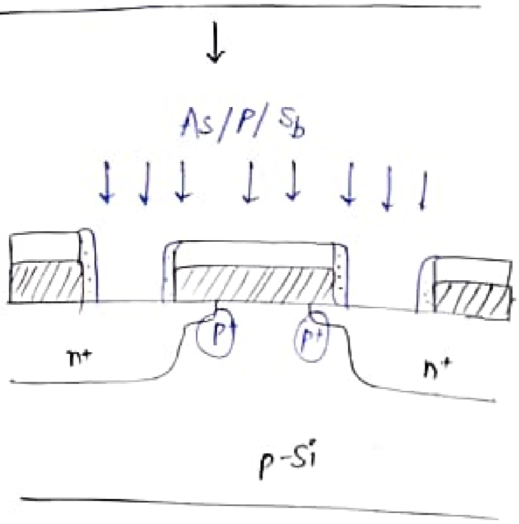
(13.56 MHz)
↳ freq. of changing polarity



$$SiH_4 + O_2 \xrightarrow[\text{plasma}]{200^\circ C} SiO_2 + H_2$$
(100nm)



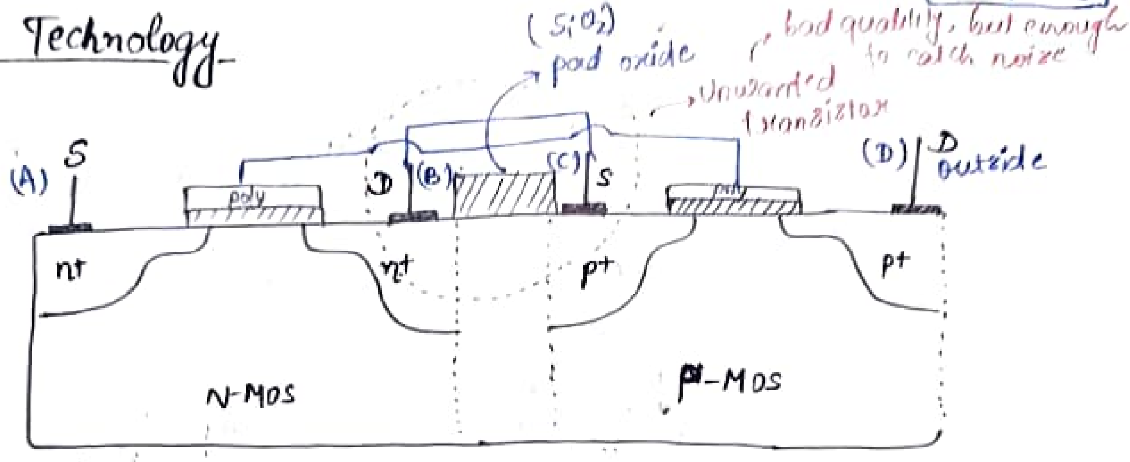
→ Anisotropic Argon Etching
↳ etches only the direct surface
↳ Uses Ar^+



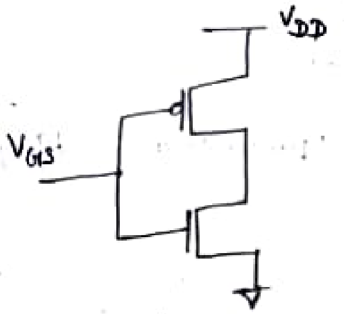
→ Deep Implantation

25-04-2025

Twin well Technology



CMOS:

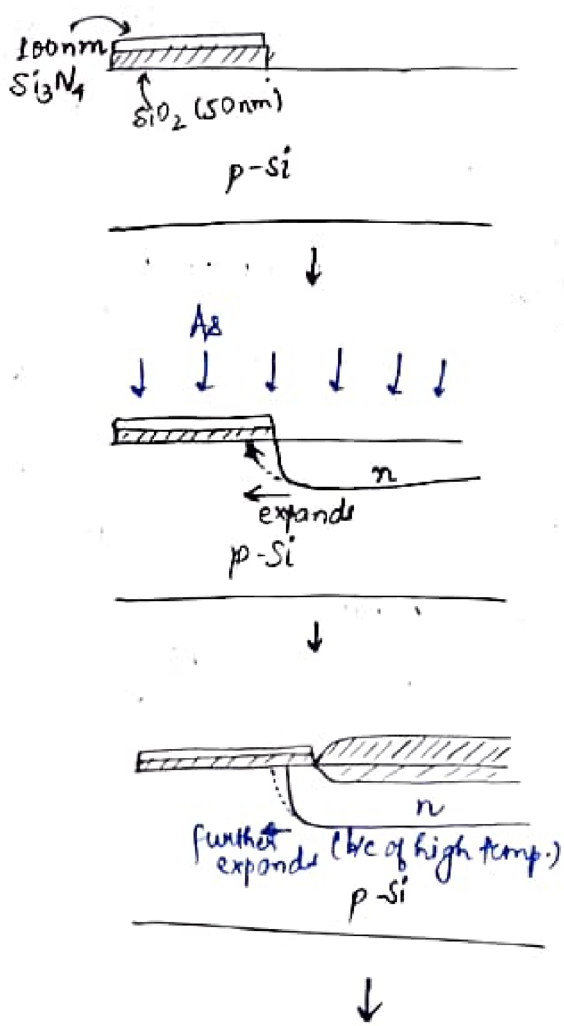


$\uparrow V_{th} \propto \frac{1}{C_{ox}\downarrow}$ ⇒ pad oxide thickness ↑

⇓

can't catch unwanted signal

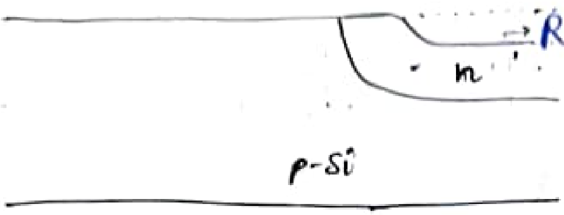
fabrication



→ Deposit and etch Si_3N_4

→ Si-wet oxidation of 1 µm (high temp.)

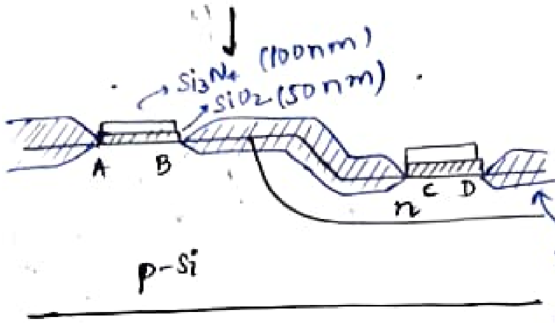
↓



→ Remove / Etch Si_3N_4 first using CF_4 recipe

↓

Then etch SiO_2



→ Deposit SiO_2 & Si_3N_4

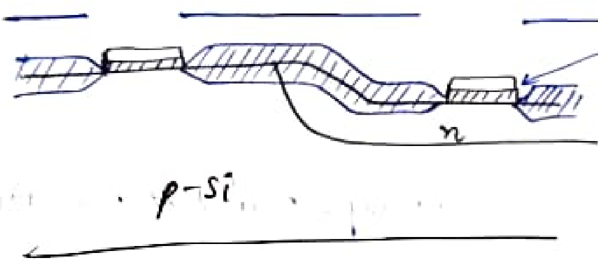
↓ Then

Full wet-oxidation

1μm SiO_2

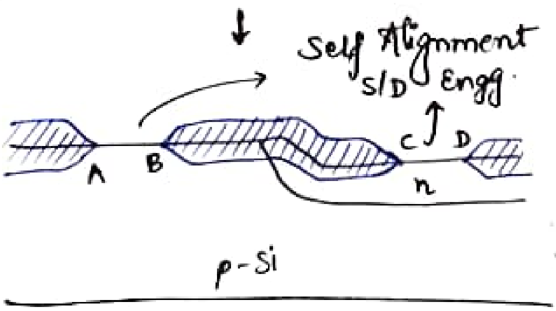
[1μm − 50 nm ≈ 1μm]

OR for better quality:

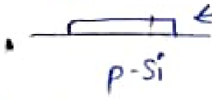


special photoresist to etch SiO_2

→ Extra cost of photolithography and etching



→ such problems won't occur if there was a single stack of Si_3N_4

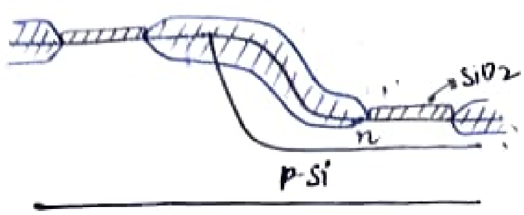


(no SiO_2 stack)

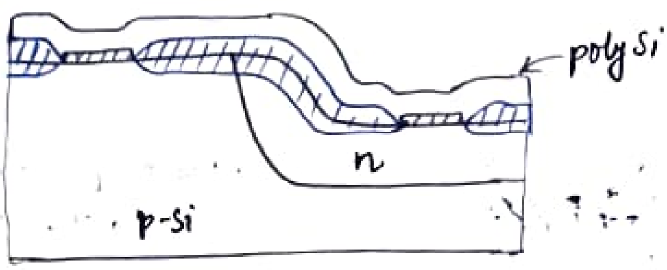
Save one-side MOS using photoresist (no developer or mask)

$C_xH_y + O_2 \xrightarrow{Ash} CO_2 + H_2$ [Ashing]

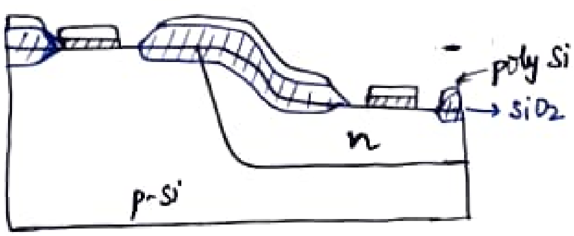
Remove photoresist using acetone or ashing.



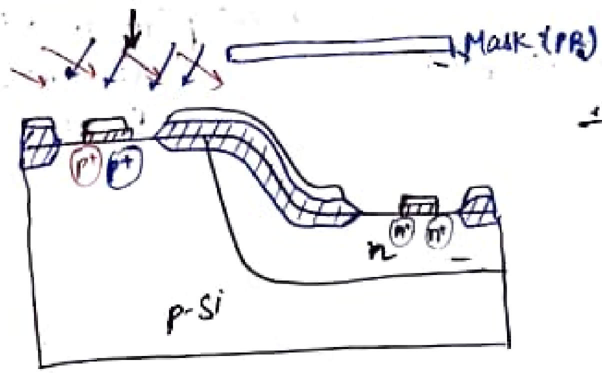
→ Deposit 100nm SiO_2 by dryoxidation



→ Deposit polysilicon



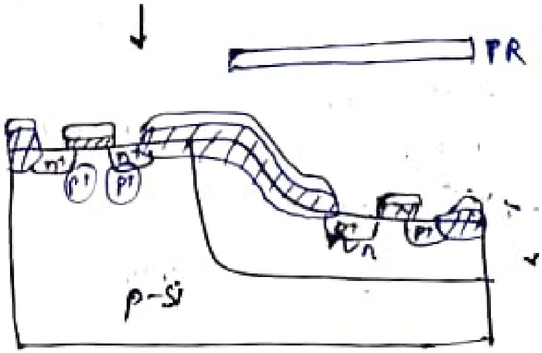
→ Pattern polySi



→ Halo/Tilted implantation

B (on NMOS side)

As (on PMOS side)



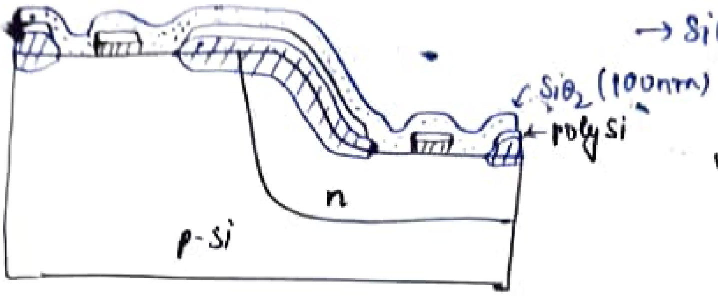
→ shallow doping

Sb (NMOS)

Ni (PMOS)

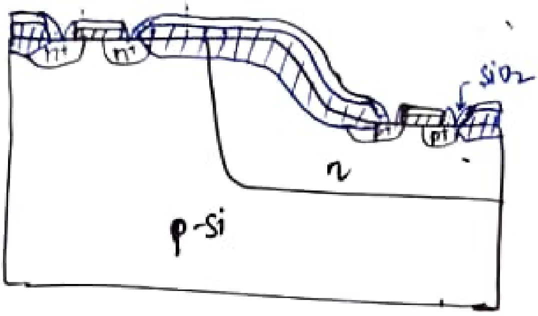
very low diffusivity

↓



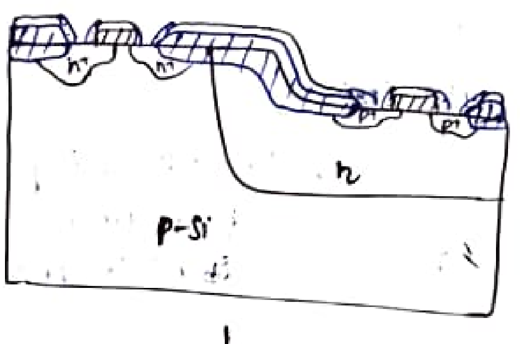
→ SiO_2 deposition

↓



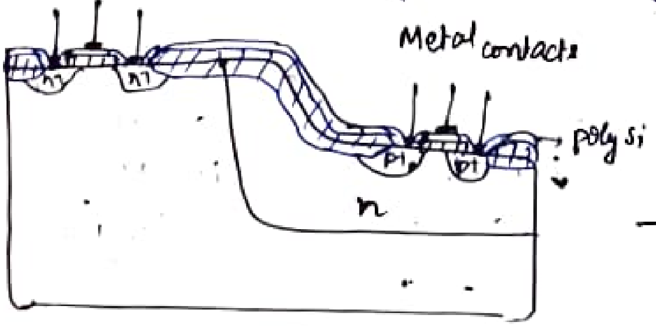
→ Anisotropic Argon Etching
↳ etch SiO_2 on the direct surface

↓



→ Deep Implantation
As. (NMOS)
Sb (PMOS)

↓



→ Metal deposition and liftoff

→ CMOS