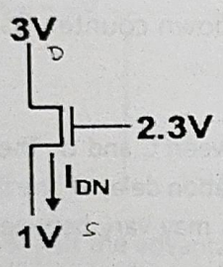
INDIAN INSTITUTE OF SPACE SCIENCE AND TECHNOLOGY
THIRUVANTHAPURAM 695 022
End Semester Examination – May 2023
AV221 – Digital Electronics and VLSI
Fourth Semester

Time: 3 Hours Date: 10/5/2023 Max. Marks: 50

ANSWER ALL QUESTIONS

1. a. There are three major courses X, Y and Z, and two minor courses A and B in a department. A student can graduate if he or she passes:
   (i) All the major courses from X to Z
   OR
   (ii) Two major courses and both minor courses
   Write a Boolean equation to represent the graduation condition. Implement using Decoder. [2.5]

2. a. Draw the CMOS schematic for the Boolean equation F=BC+A+D. [2]
   b. Draw the Equivalent RC model of the CMOS circuit. What conditions of inputs of (A,B,C,D) give worst case rise and fall delay of the logic circuit and obtain the worst case rise and fall delay.[2]
   c. If λ=600nm then what is the feature dimension of the transistor [1]
   d. For the given transistor below Figure 1. What is the value of VGS, VDS and what is the region of operation of the transistor? [1]
   e. Draw the cross-sectional view of a CMOS inverter chip and mark all the regions. [2]
   f. Define Overdrive voltage, device transconductance, process transconductance of NMOS. [2]



V_T=1V

Figure 1

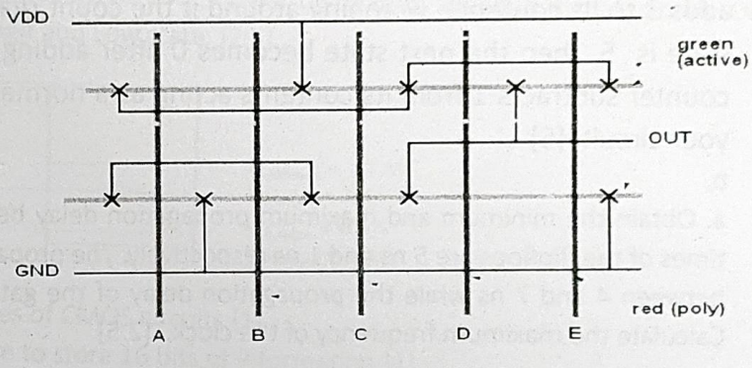


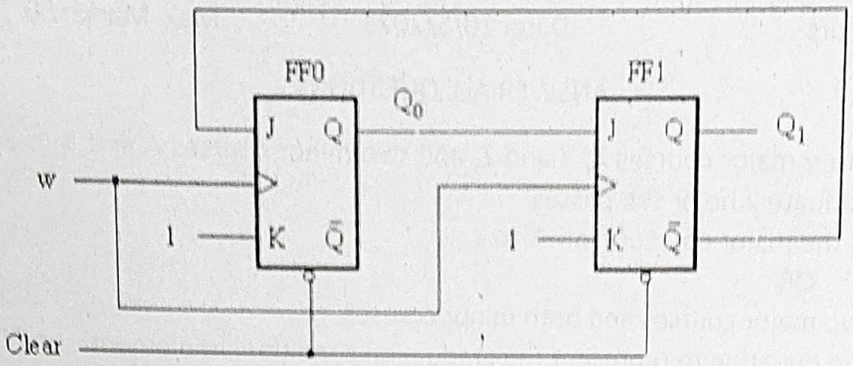
Figure 2

3. Consider the stick diagram shown in Figure 2. Draw the electrically equivalent transistor-level schematic. What logic equation does the circuit implement? Find the area of the CMOS layout.[2.5].

4. A logic system has three inputs A, B and C and two outputs Y1 and Y2. The output functions Y1 and Y2 are expressed by Y_1= A'BC+BC+A'C'+AB'C+ABC and Y_2= A'B+AC'+ABC. Determine the minimized output logic functions using the Quine–McCluskey tabular method. And implement the same using NAND gates. [5]

5. Design a priority encoder with four active high inputs A,B,C, D and three active high outputs X and Y indicating the number of the highest priority device requesting service, and P indicating the active request. (Input A is the highest priority and D the lowest). Implement the same using suitable multiplexer and logic gates.[2.5]

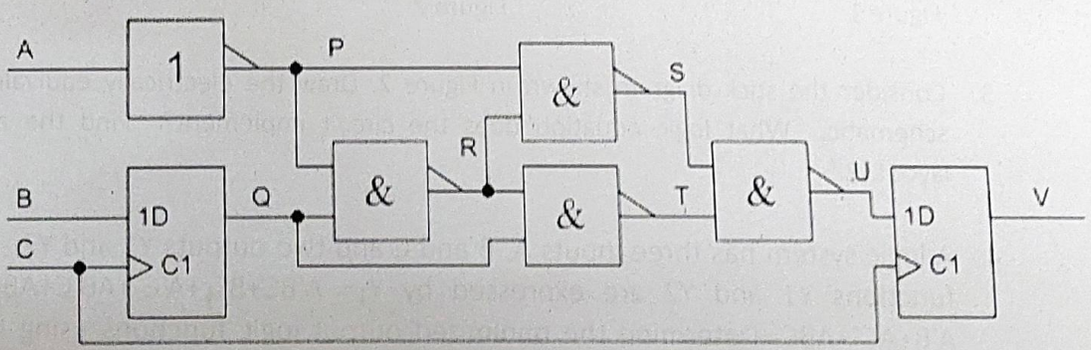
6. Determine the functional behavior of the circuit. Assume that input w is driven by a square wave signal. State diagram and logic equation [2.5]



7. Design a synchronous sequential circuit with one input (x) and one output (z) line that recognizes the input string x=1111. It should recognize overlapping sequence also. For example if x = 1101111111010 then z = 0000001111000.
   a. Draw the Moore model state diagram.[2]
   b. Generate next-state and output tables[1]
   c. Obtain the equations and logic diagram using D Flip Flop [2]

8. Design a three-bit counter like circuit controlled by the input w. If w=1, then the counter adds 3 to its contents, wrapping around if the count reaches 8/9/10. Thus, if the present state is 5, then the next state becomes 0 after adding 3, respectively. If w=0, then the counter subtracts 1 from its contents acting as a normal down counter. Use T flips flop in your circuit. [5]
   b.

9. a. Obtain the minimum and maximum propagation delay between C and U. The setup and hold times of the flipflops are 5 ns and 1 ns respectively. The propagation delay of the flipflops may vary between 4 and 7 ns while the propagation delay of the gates may vary between 2 and 6 ns. b. Calculate the maximum frequency of the clock. [2.5]



b. For the positive edge triggered D flip flop shown below the clock input is logic low(0) from t=0ns to t=10ns, make a transition from logic low to logic high(1) at t=10ns, and stays high until t=20ns. However, for the input at D to be propagated to Q correctly at this clock transition the flip flop designer specifies that the input has to be available before t=9ns and has to remain unchanged until t=12ns. Find the setup time and hold time. [1]

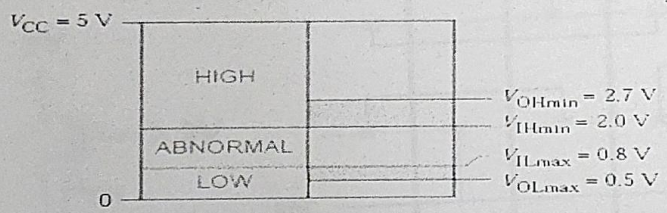
c. What is race around condition. Give an example. How it is avoided? [1.5]

10. Show the block diagram and logic diagram for the function given in the truth table. The available components to design the logic diagram are one, two and three input NAND gates. Say what is this component/function [2.5]

Input				Output		
E1	E2	A	B	O1	O2	O3
0	X	X	X	1	1	1
X	0	x	x	1	1	1
1	1	0	1	1	1	1
1	1	0	1	0	1	1
1	1	1	0	1	0	1
1	1	1	1	1	1	0

10. A 10bit ripple counter has a 256KHz clock signal applies
    (a) What is the mod number of this counter [0.5]
    (b) What will be the frequency at the MSB output [0.5]
    (c)What will be the duty cycle of the MSB signal [0.5]
    (d) Assume the counter starts at zero. What will be the count in hexadecimal after 1000 input pulses [1]

11. a. In what output state does a CMOS circuit sink current from a load [0.5]
    b. Define Noise margin, Fan in, Fan out, Power dissipation Speed in digital circuit. Obtain the DC Noise margin for the High and Low state. [2.5]



    c. List out the advantages of CMOS circuits [1]
    d. Draw a ROM structure to store 16 bits of information.[1]