Digital Electronics and VLSI Design August 2023

III Semester B.Tech (ECE)

Assignment -I

Due Date of Submission 30th August 2023

1. Parity is a common error detection mechanism used in data transmission. If a word contains an even number of 1's, the parity bit is 1. If the word has an odd number of 1's, the parity bit is 0. Derive the minimized function for a parity bit generator, where every word contains 6 bits. Use a 6 variable Karnaugh map for the minimization.
2. A. Draw a block diagram of a 16-bit ripple-carry adder. How much time does the ripple-carry adder take to complete one addition? If every XOR gate has a propagation delay of 10 ps, and every AND or OR gate has a propagation delay of 4 ps.
   B. Construct a b bit carry look ahead adder and find the propagation delay for the adder to complete one addition.
3. Design a combinational circuit that generates the 9's complement of a BCD digit. (learn to do 9's complement and approach the problem).
4. Give the Boolean expression for the following problem definition. (i) The company store well should be unlocked only when Mr.Bell is in the office or Mr.Dell in the ofice and only when the company is open for business and only when the security guard is present. Design and error detected (giving alarm sound) for the above problem if the alarm is unlocked for invalid conditions.
5. Consider the design of a light for the staircase of a house. The light should be controlled from both the bottom and the top of the staircase. The rule to be followed is that switching either switch should change the state of the light, i.e, if the light was on it goes off, if it was off it goes on, when either switch is switched. Develop a truth table for this function.
6. Simplify the following using Tabulation method and Karnaugh method
   $F(A,B,C,D,E)=\Sigma$ (0, 1,5,8,11,12,14,16,20,21,25,27,28,30,31) with don't care terms 2,7,13,22,23
7. Simplify the function using POS
   $F(A,B,C,D)=\prod(1,3,5,7,13,15)$
8. Using Boolean Properties reduce the following expressions
   (i) X(y+w'z)+wxz
   (ii) F=x'y'z'+x'y'z+x'yz+xy'z+xyz
9. Deduce the following function F3=F1+F2 as a product of maxterms where F1=
   $F1(A,B,C,D)=\prod(1,3,5,11,15)$
   $F2(A,B,C,D)=\prod(1,3,5,7,8,9,11)$
10. Draw a block diagram of a 16-bit ripple-carry adder. How much time does the ripple-carry adder take to complete one addition? Every XOR gate has a propagation delay of 12 ps, and every AND or OR gate has a propagation delay of 6 ps.

Draw the block diagram of 8 bit carry ahead adder and obtain how much time does the adder take to complete one addition if the delay of the gates are same as mentioned above.

11. Two decimal numbers, both between 0 and 99, need to be added to each other. Design a logic circuit that performs a BCD addition of these two numbers. Use block diagrams for adders and other components that you need, use any combinational logic gates that you require. (Refer Morris mano text book for reference)