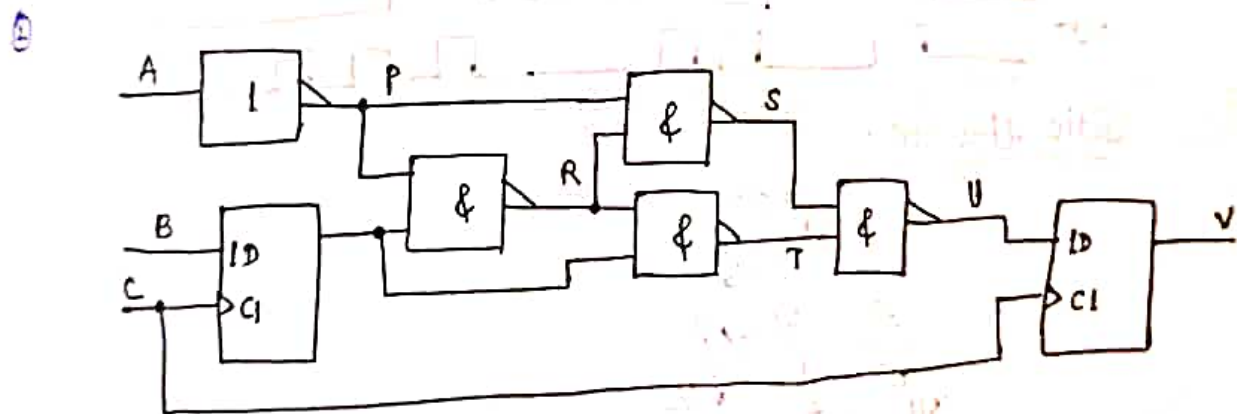
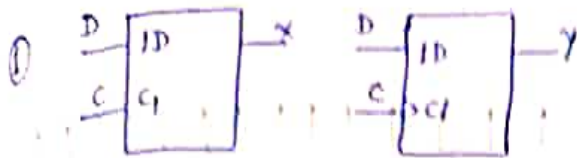


Assignment - 3

AV212- Digital Electronics and VLSI Design

Saurabh Kumar
SC22B146



Given: $t_{SU,FF} = 6ns$; $t_{H,FF} = 2ns$

$5ns < t_{P,FF} < 8ns$

$3ns < t_{P,gate} < 7ns$

$$C \rightarrow U: (t_{clock})_{min} = t_{SU,FF} + (\max t_{P,D}) + (\max t_{P,Q}) + (\max t_{P,Q}) + (\max t_{P,Q})$$

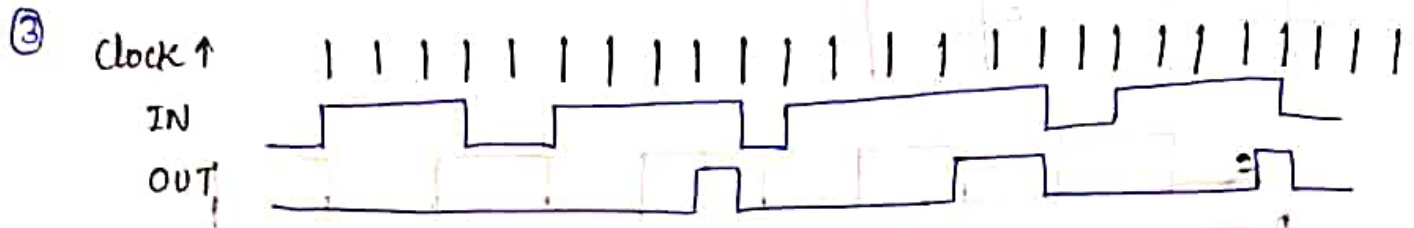
$$= 6 + 8 + 7 + 7$$

$$= 28ns$$

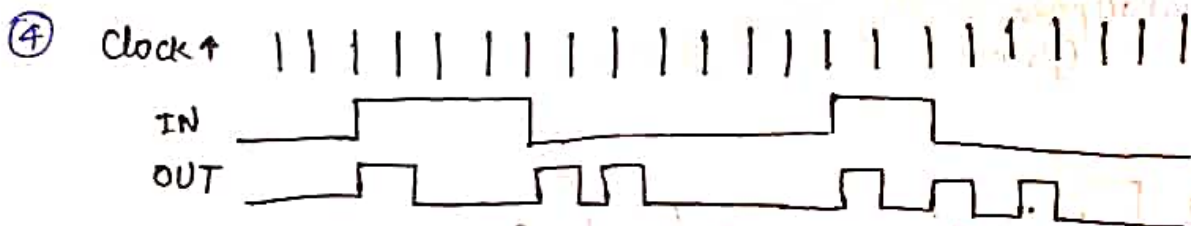
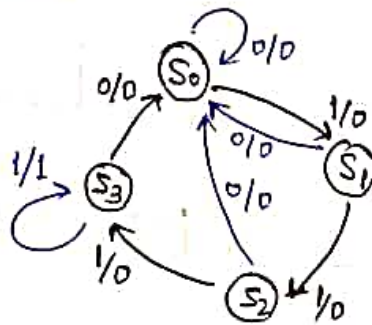
By another path of $C \rightarrow Q \rightarrow Q \rightarrow U: (t_{clock})_{min} = 28ns$ (same)

\therefore Min^m clock period = 28ns.

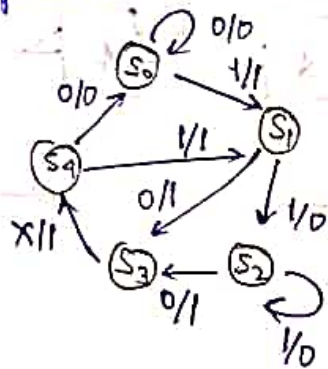
\therefore Maximum frequency of clock = $\frac{1}{(t_{\text{clock}})_{\text{min}}} = \frac{1}{28 \text{ ns}} = 35.7 \text{ MHz}$



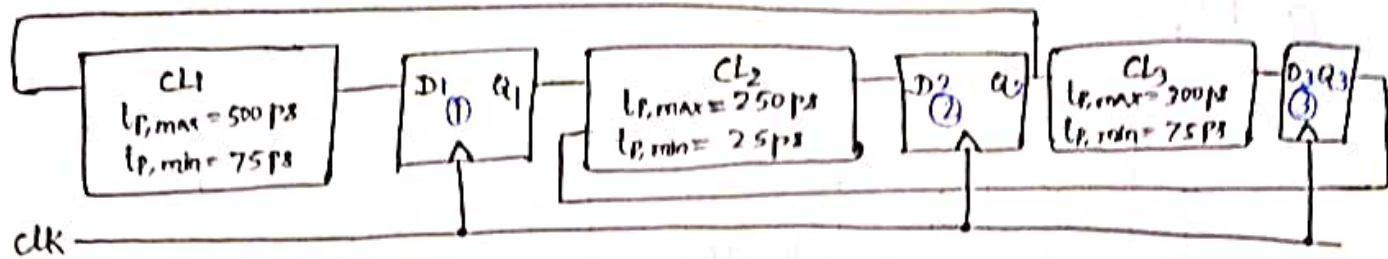
State diagram:



State diagram:



⑤



$$\begin{aligned} \text{Path } Q_2 \rightarrow Q_1 : t_{PQ2} (t_{\text{clock}})_{\min} &= \max t_{PC2} + \max t_{PC1} \\ &= 250 + 500 \text{ ps} \\ &= 750 \text{ ps} \end{aligned}$$

$$\begin{aligned} \text{Path } Q_3 \text{ to } Q_2 : (t_{\text{clock}})_{\min} &= \max t_{PC3} + \max t_{PC2} \\ &= 300 + 250 \text{ ps} \\ &= 550 \text{ ps} \end{aligned}$$

$$\begin{aligned} \text{Path } Q_2 \text{ to } Q_3 : (t_{\text{clock}})_{\min} &= \max t_{PC2} + \max t_{PC3} \\ &= 250 + 300 \text{ ps} \\ &= 550 \text{ ps} \end{aligned}$$

$$\begin{aligned} \text{Path } Q_3 \text{ to } Q_1 : (t_{\text{clock}})_{\min} &= \max t_{PC2} + \max t_{PC1} \\ &= 250 + 500 \\ &= 750 \text{ ps} \end{aligned}$$

$$\begin{aligned} \text{Path } Q_1 \text{ to } Q_2 : (t_{\text{clock}})_{\min} &= \max t_{PC2} \\ &= 250 \text{ ps} \end{aligned}$$

$$\begin{aligned} \text{Path } Q_1 \text{ to } Q_3 : (t_{\text{clock}})_{\min} &= \max t_{PC2} + \max t_{PC3} \\ &= 250 + 300 \\ &= 550 \text{ ps} \end{aligned}$$

$$\therefore t_{\text{clock}} \geq 750 \text{ ps}.$$

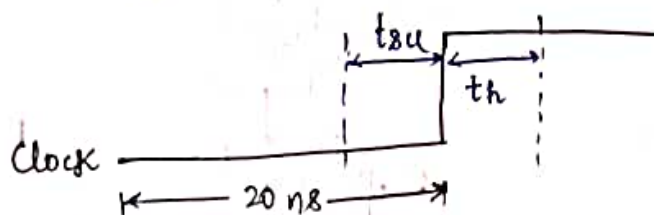
$$\Rightarrow (t_{\text{clock}})_{\min} = 750 \text{ ps}.$$

⑥

$$t_{\text{SU FF}} = 5 \text{ ns}$$

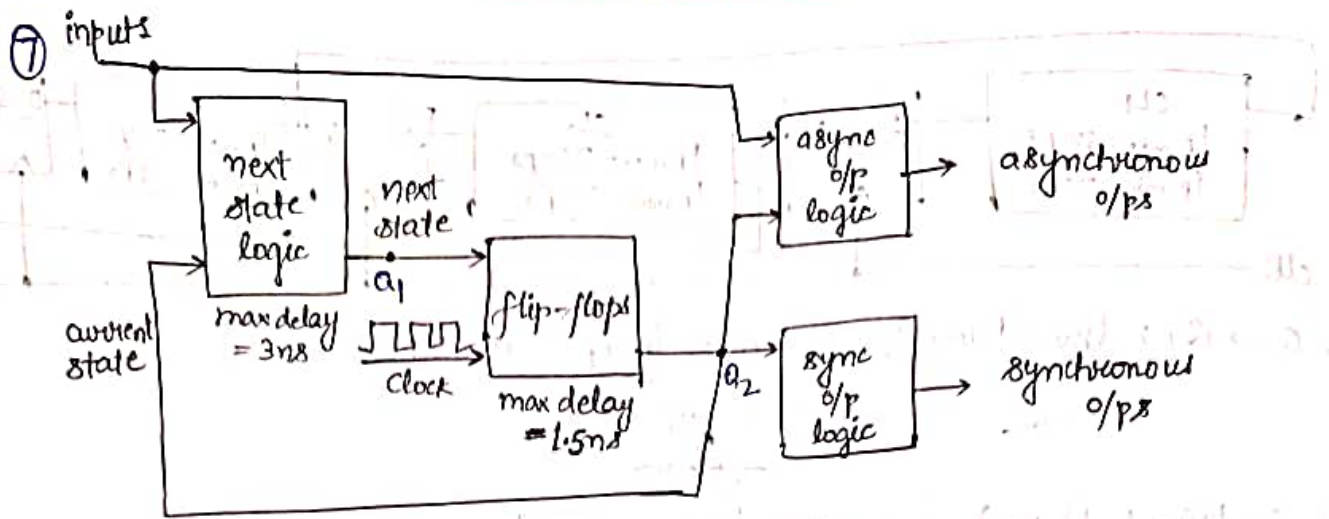
$$t_{\text{H FF}} = 3 \text{ ns}$$

$$\text{clock cycle} : 20 \text{ ns}$$



The ~~need~~ ^{input} needs to be stable ~~for~~ at least t_{su} amount of time before the clock edge.

$$\therefore \text{latest time D can change} = 20 - t_{\text{su}} = 20 - 5 = 15 \text{ ns}.$$



$$\begin{aligned}
 t_{su} &= 1.5ns \\
 \max t_{sk} &= 0.5ns \\
 t_{PFF} &= 1.5ns \\
 t_{PNS} &= 3ns
 \end{aligned}$$

Path $Q_2 \rightarrow Q_1$: $(t_{clock})_{min} = t_{sk} + t_{PFF}$

$$\begin{aligned}
 &= 0.5 + 1.5 \\
 &= 2ns
 \end{aligned}$$

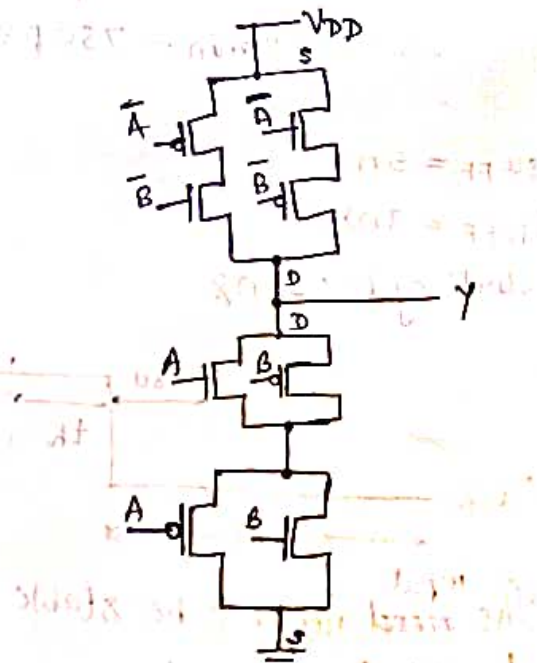
Path $Q_2 \rightarrow Q_2$: $(t_{clock})_{min} = t_{PNS} + t_{suFF} = 3 + 1.5$

$$= 4.5ns$$

$\therefore (t_{clock})_{smallest} = 4.5ns$

⑧ @ XOR gate:

$$\begin{aligned}
 Y &= A\bar{B} + \bar{A}B \\
 \bar{Y} &= \overline{A\bar{B} + \bar{A}B} \\
 &= \overline{A\bar{B}} \cdot \overline{\bar{A}B} \\
 &= (\bar{A} + B)(A + \bar{B})
 \end{aligned}$$



⑥ Full adder circuit:

$$S = A \oplus B \oplus C = A\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}\bar{B}C + ABC$$

$$C = AB + BC + AC$$

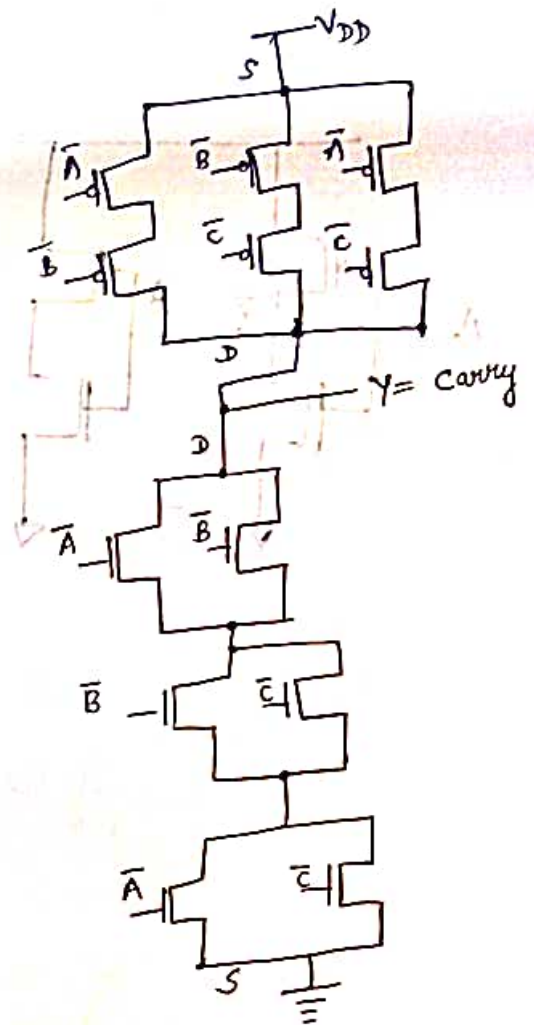
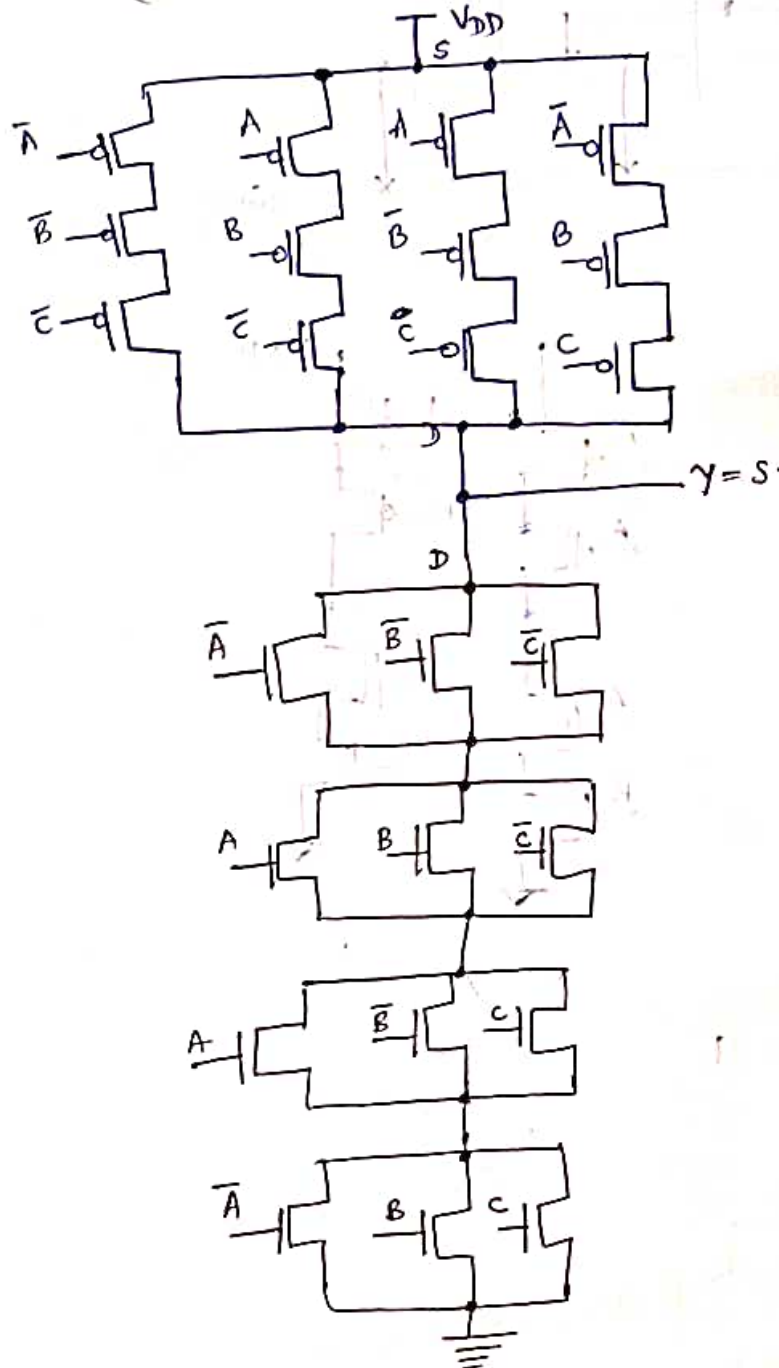
$$C = AB + C(A \oplus B)$$

$$\bar{S} = (\bar{A}\bar{B}\bar{C})(\bar{A}B\bar{C})(\bar{A}\bar{B}C)(ABC)$$

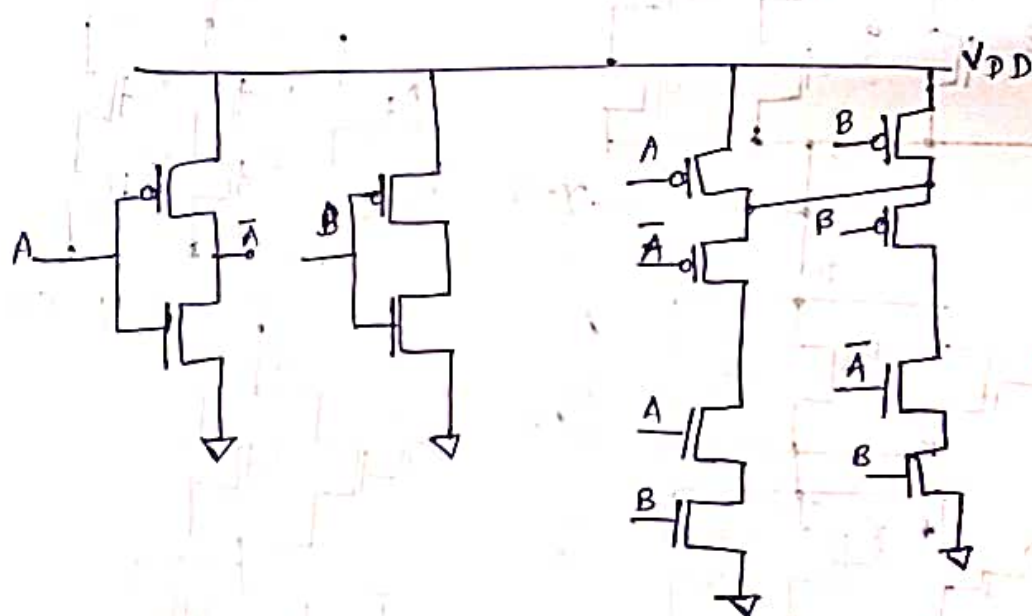
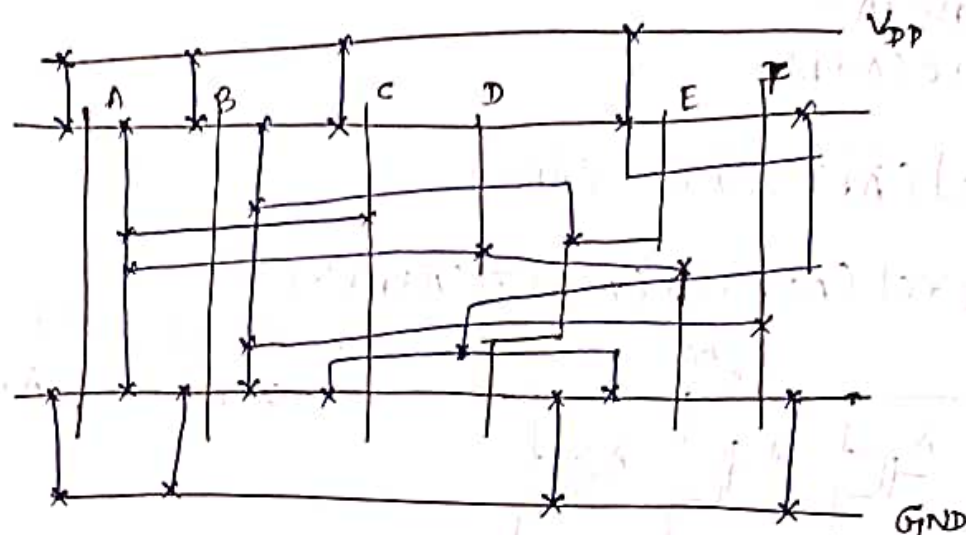
$$= (\bar{A} + B + C)(A + \bar{B} + C)(A + B + \bar{C})(\bar{A} + \bar{B} + \bar{C})$$

$$\bar{C} = (\bar{A}\bar{B})(\bar{B}\bar{C})(\bar{A}\bar{C})$$

$$= (\bar{A} + \bar{B})(\bar{B} + \bar{C})(\bar{A} + \bar{C})$$



⑨ Stick diagram:

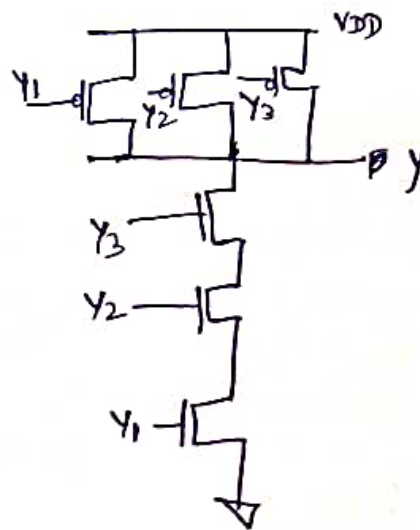
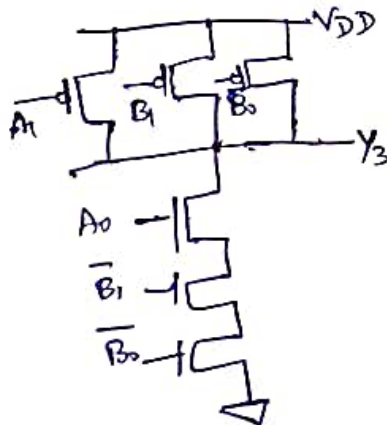
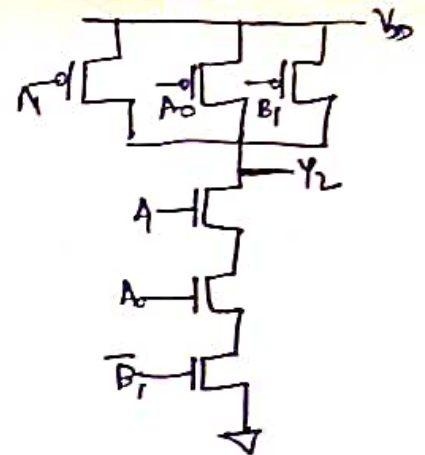
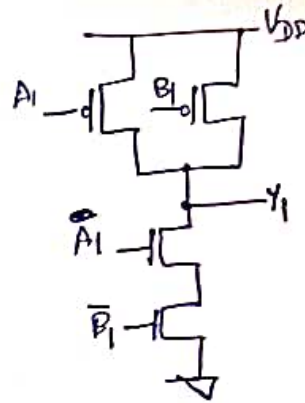
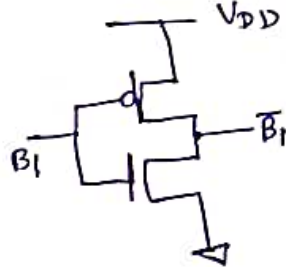
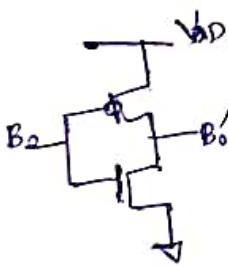
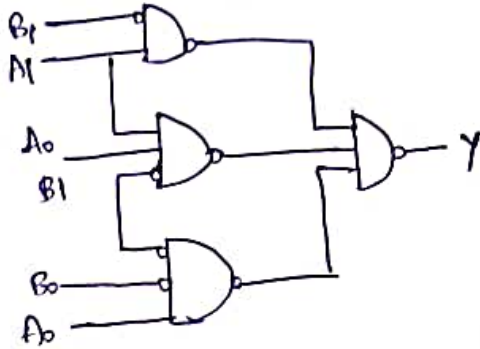


⑩ $A = A_1 A_0$
 $B = B_1 B_0$

$$Y(A > B) = A_1 \bar{B}_1 + (A_1 B_1 + \bar{A}_1 \bar{B}_1) (A_0 \bar{B}_0)$$

$$\bar{Y} = (\bar{A}_1 \bar{B}_1) \left[(\bar{A}_1 B_1 + \bar{A}_1 \bar{B}_1) + (\bar{A}_0 \bar{B}_0) \right]$$

$$Y = \bar{\bar{Y}} = \overline{\bar{A}_1 \bar{B}_1 \cdot \bar{A}_1 A_0 \bar{B}_1' \cdot A_0 \bar{B}_1 \bar{B}_0}$$



$$\begin{aligned} \text{Area} &= (1992) / (64) \lambda^2 \\ &= 288 (64) \lambda^2 \\ &= 14592 \lambda^2 \end{aligned}$$