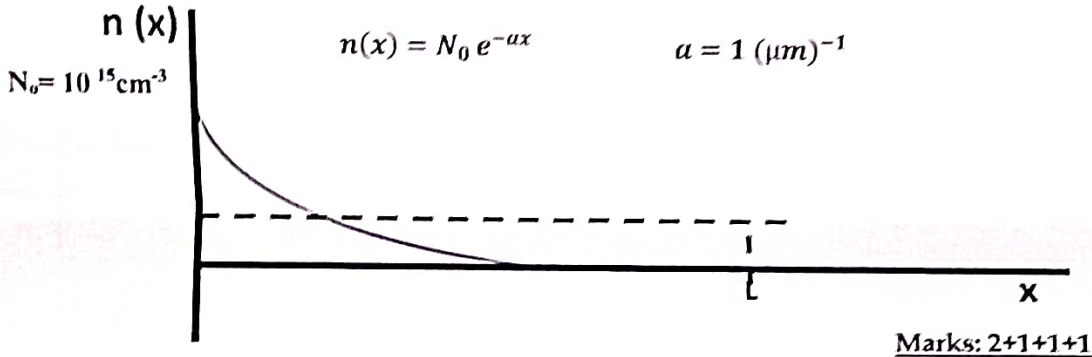
INDIAN INSTITUTE OF SPACE SCIENCE AND TECHNOLOGY

VLSI Technology (AV 323)
Quiz 1: Total Marks 15
Date: 20-02-2024
You are allowed to make assumptions with proper justification.

1. An n-silicon wafer is non-uniformly doped with an exponential profile, as shown in the figure below.
   a) Under thermal equilibrium, derive an expression for built in electric field at any point x, along the region where there is doping variation.
   b) What is the magnitude of electric field?
   c) Sketch the electric filed profile from 0 to L
   d) Draw the band diagram from 0 to L.



Marks: 2+1+1+1

2. A silicon P-N junction is doped by Boron ($10^{18}/cm^3$) and Arsenic ($10^{15}/cm^3$). Draw the band-diagram (approximate as per scale) by calculating the necessary parameters.

   [Hint: Identify and calculate the position of Fermi level with respect to E_c and E_v. Find out the value of Build in potential and Depletion region and show it on the diagram. Also show how vacuum level varies from P to N region.] Marks: 5

3. A MOS capacitor having the gate oxide thickness t_{ox} = 100nm and the substrate BORON doping density $N_A=10^{15}/cm^3$ is biased in the depletion mode with a gate voltage, Vg. If the surface potentrial is 0.2V for this bias condition, determine the following (a) peak electric field in Si substrate, and electric field in the oxide (b) the gate voltage Vg (c) thermal equilibrium hole concentrations p_p. Here $\varepsilon_0 = 8.854 \times 10^{-14}$ F/cm and Dielectric constant for Si is 12 and oxide is 4.

Marks: 2.5+1 +1.5

END

INDIAN INSTITUTE OF SPACE SCIENCE AND TECHNOLOGY

VLSI Technology (AV 323)
Quiz II
Date: 03-04-2024

You are allowed to make assumptions with proper justification. No step jumps are allowed.

1. Kindly consider a Nano transistor with a subthreshold slope:
   a. Derive the expression of the best possible subthreshold slope, that can be achieved at room temperature. [Derive the expressions without any step jumps. A detailed explanations of each step are expected]

   b. A transistor has a subthreshold slope of 100 mV/decade and threshold voltage (Vt) is 0.3 V at room temperature. If the on current is 1mA/μm, then what is the off-state current? Suppose that the transistors are cooled down to 100°K. Then what is the subthreshold slope?

   c. At low temperature, Vt also increases slightly due to bandgap widening, and the on current also increases [since the improvement in mobility more than compensates for increased Vt]. Suppose the new Vt ´at 100°K is 0.32V and on-current is 1.5mA/μm. Then what would be the off-state current?

Marks: 3+3+2

2. In a High K Gate Dielectric Technology, the gate insulator consists of a hybrid stack of an Ultrathin SiO2 layer and a High-K insulator on Top. If the SiO2 thickness is 1nm, and the High K insulator on top of the SiO2 has a thickness of 5nm with relative permittivity 20.
   a. Then what is the EOT (Effective Oxide Thickness) of this gate insulator stack?
   b. What is the per-unit gate capacitance density?

Marks: 3+4

END

INDIAN INSTITUTE OF SPACE SCIENCE AND TECHNOLOGY
VLSI Technology (AV 323)
End Sem Exam: Total Mark 50
Date: 06-05-2024
You are allowed to make assumptions with proper justification. No step jumps are allowed.

1. Derive the expression of the Threshold voltage of N-MOS considering the Flat band condition while a 100mV appears on top of the surface potential. At this condition derive the expression for inversion charge in detail. Draw the detailed band diagram of the above-mentioned condition with metal work function 4.1eV. The electron affinity of Si is 4.05eV and substrate doping is $10^{15}/cm^3$.

[**Instructions:** Neat and clean band diagram (try to draw as per the scale). Mention all the values in the Diagram. Draw two diagrams, one in the equilibrium condition and the other one in the non-equilibrium case where 100mV appears on the surface potential. Consider the flat band condition for both cases. You need to calculate flat band voltage with the assumption that the total fixed charge is zero.]

Marks: 4+3+5

2. Derive the expression for threshold voltage swings for N-MOS. Discuss in detail with neat and clean pictures/schematic.

Marks: 5

3. What is DIBL and Threshold voltage swings in nanoscale CMOS? How was this resolved (both DIBL and Threshold voltage swings and short channel effect)? Give a detailed process flow of CMOS. Give a detailed process flow with recipes. Draw the cross-sectional schematic in one column and provide the process description in the other column. Show it for CMOS. The justification should be there against every process steps.

[**Hints:** Source & Drain Engineering with different doping levels and profiles. Similarly, Channel engineering with Halo implantation along with Isolation Technology]

Marks: 2+15

4. A Ge P-N Junction has a cross-sectional area of A =0.01 cm2. The hole density in the P-Region is $2.5 \times 10^{17}/cm^3$. The electron density in the N-region is $2.5 \times 10^{14}/cm^3$. The lifetime of the hole in the N region is 100μ sec. The intrinsic electron density in Ge is $2.5 \times 10^{13}/cm^3$. Assume the diffusion constant of holes to be 44 cm^2/sec. Calculate the value of hole current injected from the P region into the N region when a forward voltage of 100mv is applied across the diode.

Marks: 8

5. For 30 nm length, N channel MOS transistor, the Threshold voltage of the transistor as measured at drain voltage of 0.1 V and 1.1 V are 200mV and 100mV.
   a. What is the DIBL for the transistor?
   b. Sketch the band diagram (the scale may be relative) along the source to drain direction if gate voltage =100mV, Drain voltage =1V and Source voltage =0V.

(Assume the substrate doping is $10^{17}/cm^3$, if you need to use this information for any purpose.)

Marks: 3+5

END