

Specifications of 8085 Microprocessor Trainer Kit (ESA 85-2)

- Power supply for ESA 85-2 kit is 5V, 3.0A
- CPU: 8085 operated at 3.072MHz
- Memory :
 - 16K Bytes EPROM by a 27128 at the socket U4.(0000h-3FFFh)
 - 32K Bytes of static RAM by a 62256 at the socket U6. (8000h-FFFFh)

HOW TO USE ESA 85-2 TRAINER KIT

Entering the Program and Data

1. Press 'RESET' key, it will show 'ESA 85'.
2. Press 'EXAM MEM' key followed by the Starting address to where the program has to write (Eg:8000) and press 'NEXT' key
3. Enter the byte (Opcode of each instruction) and press 'NEXT' key till all instruction complete.

Execution of Program

1. Press 'RESET' key.
2. Press 'GO' key followed by the starting address of the program and press 'EXEC' key.

Verification of Program

1. You can see the contents of each registers by, pressing 'EXAM REG' key followed by name of Register and by Pressing 'NEXT' key.
2. You can see/modify the contents of memory location by, pressing 'EXAM MEM' key followed by typing the address.

Example Program:

- An Assembly Language Program(ALP) in 8085 to add two immediate eight bit numbers without carry (Eg: 37H and 55H) and store the sum in the memory location 8500.

Algorithm:

- Start the program by loading first data/number (1 byte) into Accumulator.
- Move second data/number (1 byte) to register B
- Add the two register contents
- Store the value of sum from accumulator to the memory location 8500.
- Return control to the monitor

Address	Opcode	Mnemonics	Operands	Comments
8000	3E	MVI	A,37	Move the immediate data 37 to the accumulator
8001	37			
8002	06	MVI	B,55	Move the immediate data 55 to the register B
8003	55			
8004	80	ADD	B	Add the value of register B to A
8005	32	STA	8500	Store the sum value from accumulator to memory location 8500
8006	00			
8007	85			
8008	DF	RST 3		Return control to the monitor

Lab Exercise:

1. a. Write an ALP in 8085 to add two 8-bit numbers which are stored in the memory locations 8500 and 8501. Store the sum in the memory locations 8502. (Discard carry)
b. Complement the result (Accumulator Register) obtained in Program (a) and store the result in 8503.
2. a. Write an ALP in 8085 to multiply two 8-bit numbers
b. Write an ALP in 8085 for the division of two 8-bit numbers. Store Quotient and remainder.

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INTRODUCTION TO 8085

Features of 8085 Microprocessor

- It is an 8 bit microprocessor (each character is represented by 8 bits or a byte).
- It is manufactured with N-MOS technology implemented with 6200 transistors.
- It has 16-bit address lines and hence can point up to $2^{16} = 65536$ bytes (64KB) memory locations.
- The first 8 lines of address bus and 8 lines of data bus are multiplexed AD0-AD7.
- It generates 8 bit I/O address, hence it can access $2^8 = 256$ input/output ports.
- It has five hardware interrupts: TRAP, RST 5.5, RST 6.5, RST 7.5, INTR
- A 16 bit program counter (PC).
- A 16 bit stack pointer (SP).
- It provides 1 accumulator, 1 flag register & six 8-bit general purpose register arranged in pairs: BC, DE, HL
- It consists of 74 instruction sets.
- It requires a signal +5V power supply and operates at 3MHz clock frequency.
- It is enclosed with 40 pins DIP (Dual in line package).

Instructions useful for today's Lab Session:

Instruction	Operands	Description
MOV Copy from source to destination	Rd, Rs M, Rs Rd, M	This instruction copies the contents of the source M, Rs register into the destination register of Rd, M ; the contents of the source register are not altered. If one of the operands is a memory location, its location is specified by the contents of the HL registers. Example: MOV B, C or MOV B, M
MVI Move immediate 8-bit	Rd, data M, data	The 8-bit data is stored in the destination register or memory. If the operand is a memory location, its location is specified by the contents of the HL registers. Example: MVI B, 57 or MVI M, 57
LDA Load accumulator	16-bit address	The contents of a memory location, specified by a 16-bit address in the operand, are copied to the accumulator. The contents of the source are not altered. Example: LDA 8200
STA Store accumulator direct	16-bit address	The contents of the accumulator are copied into the memory location specified by the operand. This is a 3-byte instruction, the second byte specifies the low-order address and the third byte specifies the high-order address. Example: STA 8500
ADD Add register or memory to accumulator	R M	The contents of the operand (register or memory) are added to the contents of the accumulator and the result is stored in the accumulator. If the operand is a memory location, its location is specified by the contents of the HL registers. All flags are modified to reflect the result of the addition. Example: ADD B or ADD M
SUB Subtract register or memory from accumulator	R M	The contents of the operand (register or memory) are subtracted from the contents of the accumulator, and the result is stored in the accumulator. If the operand is a memory location, its location is specified by the contents of the HL registers. All flags are modified to reflect the result of the subtraction. Example: SUB B or SUB M
RST 3	none	The RST instruction is equivalent to a 1-byte call instruction. RST 3 instruction returns control to monitor.

DATA TRANSFER GROUP

ARITHMETIC AND LOGICAL CIRCUITS

BRANCH CONTROL

VIA AND ASSEMBLER

Batch-2

Appendix I—The 8085 Instruction Set

ACI data(8b)

Description: Add Immediate 8-bit data to the accumulator with carry.

Bytes/M-Cycles/T-States: 2/2/7

Hex Code: CE

Flags: All flags are affected based upon the result of the addition.

ADC R

Description: Add register to accumulator with carry.
Bytes/M-Cycles/T-States: 1/1/4

Register

Hex Codes: 8F

A

88

B

89

C

8A

D

8B

E

8C

H

8D

L

Flags: All flags are affected based upon the result of the addition.

ADC M

Description: Add contents of memory location pointed to by HL to register pair to the accumulator with carry.
Bytes/M-Cycles/T-States: 1/2/7

Hex Codes: 8E

A5
L

A4
H

A3
E

A2
D

A1
C

A0
B

Flags: All flags are affected based upon the result of the addition.

ANA R

Description: The contents of the accumulator and the register are logically ANDed and the result is put in the accumulator.
Bytes/M-Cycles/T-States: 1/1/4

Register

Hex Codes: A7

A

A0

B

A1

C

A2

D

A3

E

A4

H

A5

L

Flags: S, Z, and P are modified based upon the result of the operation.
CY is reset, and AC is set.

ANA M

Description: The contents of the accumulator and the contents of the memory location pointed to by HL are logically ANDed, and the result is put in the accumulator.
Bytes/M-Cycles/T-States: 1/2/7

Hex Codes: A6

Flags: S, Z, and P are modified based upon the result of the operation.
CY is reset, and AC is set.

ANI data(8b)

Description: The contents of the accumulator and the 8-bit data are ANDed and the result is put in the accumulator.
Bytes/M-Cycles/T-States: 2/2/7

Hex Codes: E6

85

L

Flags: All flags are affected based upon the result of the addition.
CY is reset, and AC is set.

CALL address[16b]

Description: The program sequence is transferred to the address specified by the 16-bit address. Before the program is transferred, the address of the instruction following the CALL instruction is pushed onto the stack.

Bytes/M-Cycles/T-States: 3/5/18

Hex Codes: CD

Flags: No flags are affected.

CC address[16b]

Description: The program sequence is transferred to the address specified by the 16-bit address if the CY flag is set. If CY = 0, no transfer takes place. If the transfer takes place, the address of the instruction following the CC instruction is pushed onto the stack.

Bytes/M-Cycles/T-States:

3/2/9 if transfer is not taken

3/5/18 if transfer is taken

Hex Codes: DC

Flags: No flags are affected.

CNC address[16b]

Description: The program sequence is transferred to the address specified by the 16-bit address if the CY flag is not set. If CY = 1, no transfer takes place. If the transfer takes place, the address of the instruction following the CNC instruction is pushed onto the stack.

Bytes/M-Cycles/T-States:

3/2/9 if transfer is not taken

3/5/18 if the transfer is taken

Hex Codes: D4

Flags: No flags are affected.

CP address[16b]

Description: The program sequence is transferred to the address specified by the 16-bit address if parity is odd, or if the P flag = 0. If P = 1, no transfer takes place. If the transfer takes place, the address of the instruction following the CPO instruction is pushed onto the stack.

Bytes/M-Cycles/T-States:

3/2/9 if transfer is not taken

3/5/18 if the transfer is taken

Hex Codes: EC

Flags: No flags are affected.

CP address[16b]

Description: The program sequence is transferred to the address specified by the 16-bit address if parity is even, or if the P flag = 1. If P = 0, no transfer takes place. If the transfer takes place, the address of the instruction following the CPO instruction is pushed onto the stack.

Bytes/M-Cycles/T-States:

3/2/9 if transfer is not taken

3/5/18 if the transfer is taken

Hex Codes: FC

Flags: No flags are affected.

CZ address[16b]

Description: The program sequence is transferred to the address specified by the 16-bit address if zero, or if the Z flag = 1. If Z = 0, no transfer takes place. If the transfer takes place, the address of the instruction following the CZ instruction is pushed onto the stack.

Bytes/M-Cycles/T-States:

3/2/9 if transfer is not taken

3/5/18 if the transfer is taken

Hex Codes: CC

Flags: No flags are affected.

CNZ address[16b]

Description: The program sequence is transferred to the address specified by the 16-bit address if not zero, or if the Z flag = 0. If Z = 1, no transfer takes place. If the transfer takes place, the address of the instruction following the CNZ instruction is pushed onto the stack.

Bytes/M-Cycles/T-States:

3/2/9 if transfer is not taken

3/5/18 if the transfer is taken

Hex Codes: C4

Flags: No flags are affected.

CMA

Description: The contents of the accumulator are complemented.

Bytes/M-Cycles/T-States: 1/1/4

Hex Codes: 2F

Flags: No flags are affected.

CPE address[16b]

Description: The program sequence is transferred to the address specified by the 16-bit address if parity is even, or if the P flag = 1. If P = 0, no transfer takes place. If the transfer takes place, the address of the instruction following the CPE instruction is pushed onto the stack.

Bytes/M-Cycles/T-States:

3/2/9 if transfer is not taken

3/5/18 if the transfer is taken

Hex Codes: E4

Flags: No flags are affected.

Hex Code: 35

Flags: S, AC, Z, and P are affected by the results of the operation. The CY flag is not affected.

DCX R_P

Description: The contents of the register pair are decremented by 1. The result is stored in the register pair. The register pair is treated as a 16-bit number.

Bytes/M-Cycles/T-States: 1/1/6**Register Pair**

Hex Codes: OB	BC
1B	DE
2B	HL
3B	SP

Flags: No flags are affected.**DI**

Description: The interrupt Enable flip-flop is reset, and all of the interrupts except the TI&LP interrupt are disabled.

Bytes/M-Cycles/T-States: 1/1/4**Hex Codes:** F3**Flags:** No flags are affected.**EI**

Description: The interrupt Enable flip-flop is set and all interrupts are enabled.

Bytes/M-Cycles/T-States: 1/1/4**Hex Codes:** FB**Flags:** No flags are affected.**INR R_M**

Description: The contents of the memory location pointed to by HL are incremented by one and the result is put in the memory location, as a 16-bit number.

Bytes/M-Cycles/T-States: 1/3/10**Hex Codes:** 34

Flags: S, Z, P, and AC are affected by the results of the operation. CY is not modified.

INR M

Description: The contents of the memory location pointed to by HL are incremented by one and the result is put in the memory location, as a 16-bit number.

Bytes/M-Cycles/T-States: 1/3/10**Hex Codes:** 34

Flags: S, Z, P, and AC are affected by the results of the operation. CY is not modified.

HLT

Description: The MPU finishes executing the current instruction and halts any further execution. The MPU enters the Halt Acknowledge machine cycle, and Wait states are inserted in every clock period. It requires an interrupt or a reset to get the MPU out of the Halt state.

Bytes/M-Cycles/T-States: One / two or more / five or more**Hex Codes:** 76**Flags:** No flags are affected.**IN port address[8b]**

Description: The contents of the input port designated are read and loaded into the accumulator.

Bytes/M-Cycles/T-States: 2/3/10**Hex Codes:** DB**Flags:** No flags are affected.**JMP address[6b]**

Description: The program execution is transferred to the memory address specified.

Bytes/M-Cycles/T-States: 3/3/10**Hex Codes:** C3**Flags:** No flags are affected.**JC address[6b]**

Description: Program execution is transferred to the memory address specified if the carry flag is set, or CY = 1. If CY = 0, no transfer takes place.

Bytes/M-Cycles/T-States:	3/2/7	if condition is not true	JZ address[16b]	Description: Program execution is transferred to the memory address specified if zero, or $Z = 1$. If $Z = 0$, no transfer takes place.
Hex Codes:	1A		Bytes/M-Cycles/T-States:	3/2/7
Flags:	No flags are affected.		if condition is not true	Description: Program execution is transferred to the memory address specified if not zero, or $Z = 0$. If $Z = 1$, no transfer takes place.
JNC address[16b]			Bytes/M-Cycles/T-States:	3/3/10
Description: Program execution is transferred to the memory address specified if the carry flag is not set, or $CY = 0$. If $CY = 1$, no transfer takes place.			if condition is true	Description: Program execution is transferred to the memory address specified if the carry flag is set, or $CY = 1$. If $CY = 0$, no transfer takes place.
Hex Codes:	C4		Hex Codes:	CA
Flags:	No flags are affected.		Flags:	No flags are affected.
JNZ address[16b]			JNZ address[16b]	
Description: Program execution is transferred to the memory address specified if positive, or $S = 0$. If $S = 1$, no transfer takes place.			Description: Program execution is transferred to the memory address specified if not positive, or $S = 1$. If $S = 0$, no transfer takes place.	
Bytes/M-Cycles/T-States:	3/2/7	if condition is not true	Bytes/M-Cycles/T-States:	3/3/10
Flags:	No flags are affected.		if condition is true	Description: Program execution is transferred to the memory address specified if negative, or $S = 1$. If $S = 0$, no transfer takes place.
JM address[16b]			Bytes/M-Cycles/T-States:	3/2/7
Description: Program execution is transferred to the memory address specified if minus, or $S = 1$. If $S = 0$, no transfer takes place.			if condition is not true	Description: Program execution is transferred to the memory address specified if positive, or $S = 0$. If $S = 1$, no transfer takes place.
Bytes/M-Cycles/T-States:	3/2/7	if condition is not true	Bytes/M-Cycles/T-States:	3/3/10
Flags:	No flags are affected.		if condition is true	Description: Program execution is transferred to the memory address specified if plus, or $S = 0$. If $S = 1$, no transfer takes place.
JM address[16b]			Bytes/M-Cycles/T-States:	3/2/7
Description: Program execution is transferred to the memory address specified if parity is even, or $P = 1$. If $P = 0$, no transfer takes place.			if condition is not true	Description: Program execution is transferred to the memory address specified if parity is odd, or $P = 0$. If $P = 1$, no transfer takes place.
Bytes/M-Cycles/T-States:	3/2/7	if condition is not true	Bytes/M-Cycles/T-States:	3/3/10
Flags:	No flags are affected.		if condition is true	Description: Program execution is transferred to the memory address specified if parity is odd, or $P = 1$. If $P = 0$, no transfer takes place.
JPE address[16b]			Bytes/M-Cycles/T-States:	3/4/13
Description: Program execution is transferred to the memory address specified if parity is even, or $P = 1$. If $P = 0$, no transfer takes place.			Register Pairs	Hex Codes: 3A
Bytes/M-Cycles/T-States:	3/2/7	if condition is not true		Flags: No flags are affected.
Flags:	No flags are affected.			Hex Codes: 0A 1A BC DE
JPO address[16b]				Flags: No flags are affected.
Description: Program execution is transferred to the memory address specified if parity is odd, or $P = 0$. If $P = 1$, no transfer takes place.				Description: The contents of the memory location pointed to by the register pair are loaded into the accumulator.
Bytes/M-Cycles/T-States:	3/2/7	if condition is not true		Bytes/M-Cycles/T-States: 3/2/7
Flags:	No flags are affected.			Description: The contents of the memory location specified are loaded into register L and the contents of the next memory location are loaded into register H.
LHLD address[16b]				Bytes/M-Cycles/T-States: 3/5/16
Description: The contents of the memory location specified are loaded into register L and the contents of the next memory location are loaded into register H.				Hex Codes: 2A
Bytes/M-Cycles/T-States:	3/2/7	if condition is not true		Flags: No flags are affected.
Flags:	E2			LXI R_p, data[16b]
Bytes/M-Cycles/T-States:	3/3/10	if condition is true		Description: The 16-bit data is loaded into the register pair.
Flags:	No flags are affected.			Bytes/M-Cycles/T-States: 3/3/10

Register Pair
 Hex Codes: 01 BC
 11 DE
 21 HL
 31 SP

Flags: No flags are affected.

MOV R_d, R_s

Description: The contents of the source register R_s are transferred into the destination register R_d.

Bytes/M-Cycles/T-States: 1/1/4
 Hex Codes: Source Register

	A	B	C	D	E	H	L
Destination Register	A	7F	79	7A	7B	7C	7D
	B	47	40	41	42	43	44
	C	41	48	49	4A	4B	4C
	D	57	50	51	52	53	54
	E	5F	58	59	5A	5B	5C
	H	67	60	61	62	63	64
	L	6F	68	69	6A	6B	6C
							6D

Flags: No flags are affected.

MOV M_s, R_s

Description: The contents of the source register R_s are transferred to the memory location pointed to by HL.

Bytes/M-Cycles/T-States: 1/2/7
 Hex Codes: Source Register

77	A
70	B
71	C
72	D
73	E
74	H
75	L

Flags: No flags are affected.

MOV R_d, M

Description: The contents of the memory location pointed to by HL are transferred to the destination register.

Bytes/M-Cycles/T-States: 1/2/7
 Hex Codes: Destination Register

7E	A
46	B
4E	C

Flags: No flags are affected.

56 D
 5E E
 66 H
 6E L

Flags: No flags are affected.

MVI R, data[8b]

Description: The 8 bits of data are stored in the register.

Bytes/M-Cycles/T-States: 2/2/7
 Register

Hex Codes: 3E A
 06 B
 0E C
 16 D
 1E E
 26 H
 2E L

Flags: No flags are affected.

MVI M, data[8b]

Description: The 8 bits of data are stored in the memory location pointed to by HL.

Bytes/M-Cycles/T-States: 2/3/10
 Hex Codes: 3E

Flags: No flags are affected.

NOP

Description: No operation is performed. The instruction is fetched and decoded, but no operation is executed.

Bytes/M-Cycles/T-States: 1/1/4
 Hex Codes: 00

Flags: No flags are affected.

ORA R

Description: The contents of the accumulator are logically OR'd with the contents of the register. The result is stored in the accumulator.

Bytes/M-Cycles/T-States: 1/1/4
 Register

Hex Codes: B7 A
 B0 B
 B1 C
 B2 D
 B3 E
 B4 H
 B5 L

Flags: Z, S, and P are affected based upon the operation. AC and CY are reset.

Appendix I ■ The 8085 Instruction Set

ORI M

Description: The contents of the accumulator are logically OR'd with the contents of the memory location pointed to by HL.

Bytes/M-Cycles/T-States: 1/2/7

Hex Codes: B6

Flags: Z, S, and P are affected based upon the operation. AC and CY are reset.

ORI data[8b]

Description: The contents of the accumulator are logically OR'd with the 8 bits of data. The result is stored in the accumulator.

Bytes/M-Cycles/T-States: 2/2/7

Hex Codes: F6

Flags: Z, S, and P are affected based upon the operation. AC and CY are reset.

OUT port address[8b]

Description: The contents of the accumulator are copied out to the output port specified.

Bytes/M-Cycles/T-States: 2/3/10

Hex Codes: D3

Flags: No flags are affected.

PCHL

Description: The contents of registers H and L are copied into the program counter. H is the high-order bits and L is the low-order bits.

Bytes/M-Cycles/T-States: 1/1/6

Hex Codes: E9

Flags: No flags are affected.

POP Rp

Description: The contents of the memory location [stack] pointed to by the stack pointer are copied to the low-order register of the register pair. [C, E, L, and flags.] The stack pointer is then incremented and the contents of that memory location being pointed to are copied to the high-order register of the register pair.

Bytes/M-Cycles/T-States: 1/3/10

Register:

Hex Codes: C1 BC

D1 DE

E1 HL

F1 PSW

Flags: No flags are affected.

PUSH Rp

Description: The contents of the register pair are copied into the stack. The high-order register [B, D, H, A] is put on the stack first, then the contents of the low-order register [C, E, L, flags] are put onto the stack.

Bytes/M-Cycles/T-States: 1/3/10

BYT

Bytes/M-Cycles/T-States: 1/3/12

Register Pair:

Hex Codes: C5 R

D5 D

E5 H

F5 PSW

Flags: No flags are affected.

RAL

Description: The contents of the accumulator are rotated left by one position through the carry flag.

Bytes/M-Cycles/T-States: 1/1/4

Hex Codes: 17

Flags: CY is modified according to bit D7. S, Z, P, and AC are not affected.

RAR

Description: The contents of the accumulator are rotated right by one position through the carry flag.

Bytes/M-Cycles/T-States: 1/1/4

Hex Codes: 1F

Flags: CY is modified according to bit D0. S, Z, P, and AC are not affected.

RLC

Description: The contents of the accumulator are rotated left one position. Bit D7 is placed in both D0 and CY.

Bytes/M-Cycles/T-States: 1/1/4

Hex Codes: 07

Flags: CY is modified according to bit D7. S, Z, P, and AC are not affected.

RRC

Description: The contents of the accumulator are rotated right by one bit. Bit D0 is placed in both D7 and CY at the same time.

Bytes/M-Cycles/T-States: 1/1/4

Hex Codes: 0F

Flags: CY is modified according to bit D0. S, Z, P, and AC are not affected.

RET

Description: The program sequence is transferred from the subroutine to the calling program. The two bytes from the top of the stack are copied into the Program Counter and this is the address that program execution begins.

Bytes/M-Cycles/T-States: 1/3/10

Hex Codes: C9
Flags: No flags are affected.

RC

Description: The program sequence is transferred from the subroutine to the calling program if the carry flag is set, or CY = 1. If CY = 0, no transfer takes place.

Bytes/M-Cycles/T-States: 1/1/6 if condition is not true
1/3/12 if condition is true

Hex Codes: D8
Flags: No flags are affected.

RNC

Description: The program sequence is transferred from the subroutine to the calling program if the carry flag is not set, or CY = 0. If CY = 1, no transfer takes place.

Bytes/M-Cycles/T-States: 1/1/6 if condition is not true
1/3/12 if condition is true

Hex Codes: D9
Flags: No flags are affected.

RP

Description: the program sequence is transferred from the subroutine to the calling program if positive, or S = 0. If S = 1, no transfer takes place.

Bytes/M-Cycles/T-States: 1/1/6 if condition is not true
1/3/12 if condition is true

Hex Codes: F0
Flags: No flags are affected.

RM

Description: The program sequence is transferred from the subroutine to the calling program if minus, or S = 1. If S = 0, no transfer takes place.

Bytes/M-Cycles/T-States: 1/1/6 if condition is not true
1/3/12 if condition is true

Hex Codes: F0
Flags: No flags are affected.

RPE

Description: The program sequence is transferred from the subroutine to the calling program if the parity is even, or P = 1. If P = 0, no transfer takes place.

Bytes/M-Cycles/T-States: 1/1/6 if condition is not true
1/3/12 if condition is true

Hex Codes: E9
Flags: No flags are affected.

RPO

Description: The program sequence is transferred from the subroutine to the calling program if the parity is odd, or P = 0. If P = 1, no transfer takes place.

Bytes/M-Cycles/T-States: 1/1/6 if condition is not true
1/3/12 if condition is true

Hex Codes: E0
Flags: No flags are affected.

RZ

Description: The program sequence is transferred from the subroutine to the calling program if zero, or Z = 1. If Z = 0, no transfer takes place.

Bytes/M-Cycles/T-States: 1/1/6 if condition is not true
1/3/12 if condition is true

Hex Codes: C8
Flags: No flags are affected.

RNZ

Description: The program sequence is transferred from the subroutine to the calling program if not zero, or Z = 0. If Z = 1, no transfer takes place.

Bytes/M-Cycles/T-States: 1/1/6 if condition is not true
1/3/12 if condition is true

Hex Codes: C0
Flags: No flags are affected.

RIM

Description: This instruction is used to both read in the status of interrupts 7.5, 6.5, and 5.5, as well as to read in the serial input data bit. An 8-bit word is read in and stored in the accumulator. The layout of that word is shown in Figure A1-1.

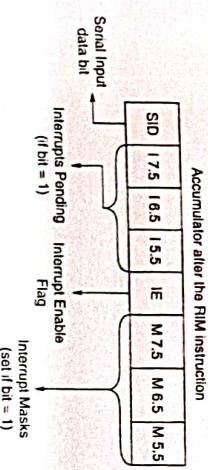


Figure A1-1 ■ The RIM instruction layout in the accumulator

Bytes/M-Cycles/T-States: 1/1/4

Hex Codes: 20

Flags: No flags are affected.

RST n (where n = 0 – 7)

Description: This instruction operates like a call instruction that goes to one of eight predetermined memory locations on page 0. Each instruction [RST 0-RST 7] goes to a specific address listed next.

Instruction Restart Address

RST 0	0000
RST 1	0008
RST 2	0010
RST 3	0018
RST 4	0020
RST 5	0028
RST 6	0030
RST 7	0038

Bytes/M-Cycles/T-States: 1/3/12

Hex Codes: C7 RST 0
CF RST 1
D7 RST 2
DF RST 3
E7 RST 4
EF RST 5
F7 RST 6
FF RST 7

Flags: No flags are accepted.

SBB R

Description: The contents of the register and the borrow flag are subtracted from the contents of the accumulator and the results are stored in the accumulator.

Bytes/M-Cycles/T-States: 1/1/4

Register
Hex Codes: 9F A
98 B
99 C
9A D
9B E
9C H
9D L

Flags: All flags are affected based upon the results of the operation.

SBB M

Description: The contents of the memory location pointed to by HL and the borrow flag are subtracted from the contents of the accumulator. The results are then stored in the accumulator.

Bytes/M-Cycles/T-States: 1/2/7

Hex Codes: 9E
Flags: All flags are affected based upon the results of the operation.

SBI data(8b)

Description: The 8 bits of data and the borrow flag are subtracted from the accumulator and the results are stored in the accumulator.

Bytes/M-Cycles/T-States: 2/2/7

Hex Codes: DE
Flags: All flags are affected based upon the results of the operation.

SHLD address(16b)

Description: The contents of register L are stored at the memory location specified and the contents of register H are stored at the next memory location by incrementing the operand by 1.

Bytes/M-Cycles/T-States: 3/5/16

Hex Codes: 22
Flags: No flags are affected.

SIM

Description: This is an instruction that is used to set the interrupt masks as well as set the serial output data bit. The accumulator is laid out as shown in Figure A1-2.

Accumulator Set Up for the SIM instruction

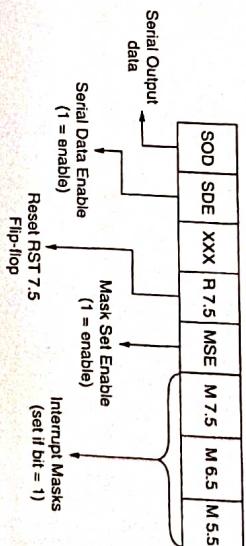


Figure A1-2 ■ The SIM instruction accumulator layout

Bytes/M-Cycles/T-States: 1/1/4

Hex Codes: 30
Flags: No flags are affected.

SPHL

Description: The contents of registers H and L are loaded into the Stack Pointer. H has the high-order portion of the address, while L has the low-order portion.

Bytes/M-Cycles/T-States: 1/1/6

Hex Codes: F9
Flags: No flags are affected.