Indian Institute of Space Science and Technology

Dept of Avionics

M.Tech VLSI and Microsystems

Quiz I February 2024

AVM867- VLSI Signal Processing

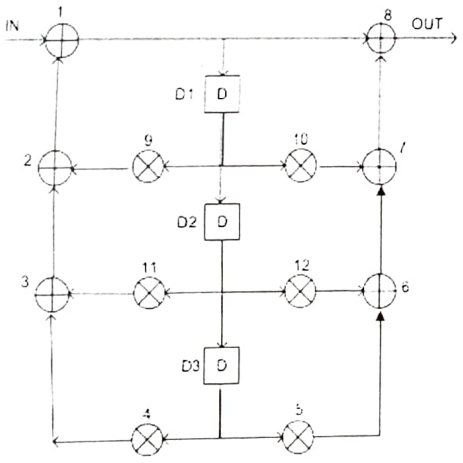
Time: 1 hour Marks: 25

Answer all Questions.

1. . Implement the following equation, where x[n] and y[n] are in Q1.7 and Q2.6 formats, respectively, and z[n] is an unsigned number in Q0.8 format. Design block level architecture for computing and what is the output Q format required: [4]

$$w[n] = x[n]y[n] + y[n]z[n] + x[n] + y[n] + z[n]$$

2. If the number representation used is n-bit signed fractional fixed-point format
   (i) What is the precision of the representation? [1]
   (ii) What is the accuracy of the representation? [1]
   (iii) What is the dynamic range of the representation? [1]
   (iv) Suppose you double the number of bits to represent a number so that it is now 2n. By what factor precision improve [1]
   (v) Why would one use fractional representation instead of integer representation of numbers [1]
3. Obtain the critical path and Iteration bound using LPM method for the following DFG [6]



4. Consider a direct form implementation of the FIR filter
   Y[n]=ax[n]+bx[n-2]+cx[n-3]
   Assume the time required for 1 multiply add operation is T.

Draw a block filter architecture for a block size of three. Pipeline this block filter such that the clock period is about T. What is the system Sample rate. [5]

5. For the following inequality obtain the retimed value using Bellman Ford algorithm [5]

$r_1 - r_2 \leq 1$

$r_3 - r_1 \leq 3$

$r_4 - r_1 \leq 2$

$r_4 - r_3 \leq -1$

$r_3 - r_2 \leq 1$

$r_2 - r_1 \leq 2$

$r_3 - r_4 \leq -6$

$r_4 - r_5 \leq -2$

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Quiz II March 2023
AVM867- VLSI Signal Processing

Time: 1 hour Marks: 20

Answer all Questions

1. For the given DFG given figure 1 [5]

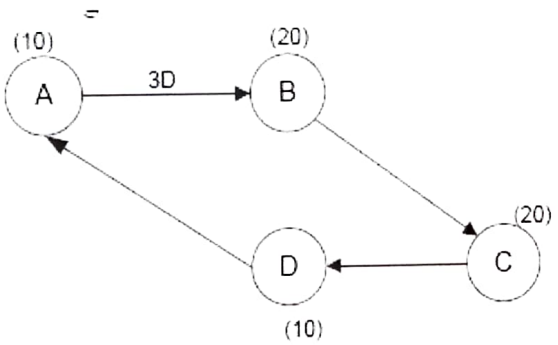


Figure 1

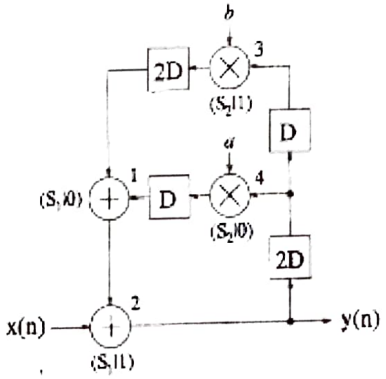
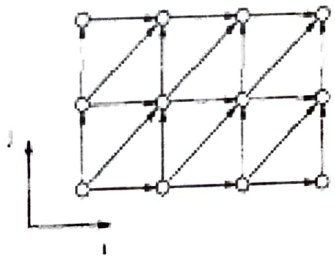


Figure 2

   a. Unfold the DFG with unfolding factor J=2
2. Obtain the folder architecture for the retimed IIR filter figure 2 [6]

3. For a given DFG shown below [5]



   a. What are the two conditions to be satisfied for the scheduling and the projection vector for making systolic array.
   b. Check whether the conditions are satisfied.

$$S = \begin{bmatrix} 1 & 0 \end{bmatrix}^T \quad d = \begin{bmatrix} 1 & 0 \end{bmatrix}^T \Rightarrow p = \begin{bmatrix} 0 \\ 1 \end{bmatrix}$$

If the condition is permissible obtain the systolic architecture

4. Define Algorithmic strength reduction with one example. [4]

Indian Institute of Space Science and Technology
Thiruvananthapuram
End Semester Examination May 2024
AVM867 VLSI Signal Processing

Marks: 50

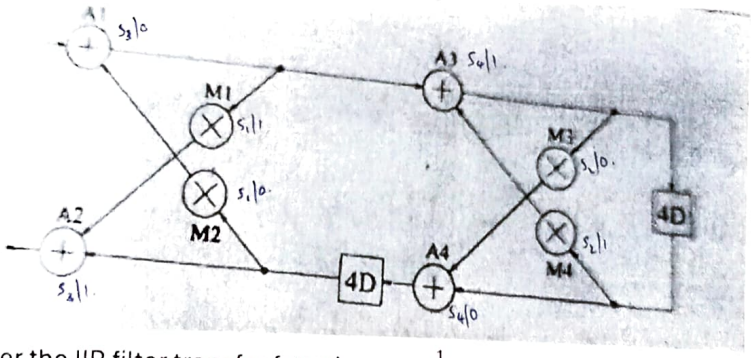
Time: 3 Hours

Answer all the questions

1. Consider the 6th order FIR filter y[n]=ax[n]+bx[n-4] +cx[n-6]. Draw DFG of the filter so that the clock period is limited by one multiply and add time unit. [5]
2. Assume the folding factor N=2 and each multiplier are pipelined by 2 stages and each adder is pipelined by 1 stage. Each operator is clocked with clock period of one unit time. The multiplication operation requires 2 unit time and addition operation requires 1ut. Fold the given DFG assuming the folding sets.

   $S_{M1}=\{M_2,M_1\}$
   $S_{M2}=\{M_3.M_4\}$
   $S_{M3}=\{A_1,A_2\}$
   $S_{M4}=\{A_4,A_3\}$

   i. Perform retiming for folding so that the folding sets result in non-negative edge delays in the folded architecture [3]
   ii. Fold the retimed DFG. [4]
   iii. Minimize the number of registers and redesign the folded architecture. [3]



3. Consider the IIR filter transfer function $\frac{1}{1-\frac{4z^{-1}}{3}+\frac{5z^{-2}}{12}}$ Obtain an equivalent 4 level pipelined transfer function using clustered look ahead decomposition approach? Draw the pole zero plot of the new system. Mention the advantages in terms of hardware aspects. [5]
4. a. Represent the coefficients a_1=0.00011011100 and a_2= 0.01001111110 (which is in 2's complement) in CSD representation. [2]

b. If y(n)=a1y(n-1)+a2y(n-2) +x(n) . Using the CSD representation obtain the multiplication and draw the DFG of the same. What is the advantage of this representation. [4]

5. Consider the inner product between two vectors A and Y using DA concept of Length N=4 and K=4. Introduce Offset Binary Coding for ROM decomposition and obtain the reduction factor in ROM size. Show the content of the ROM using tabulation. [6]

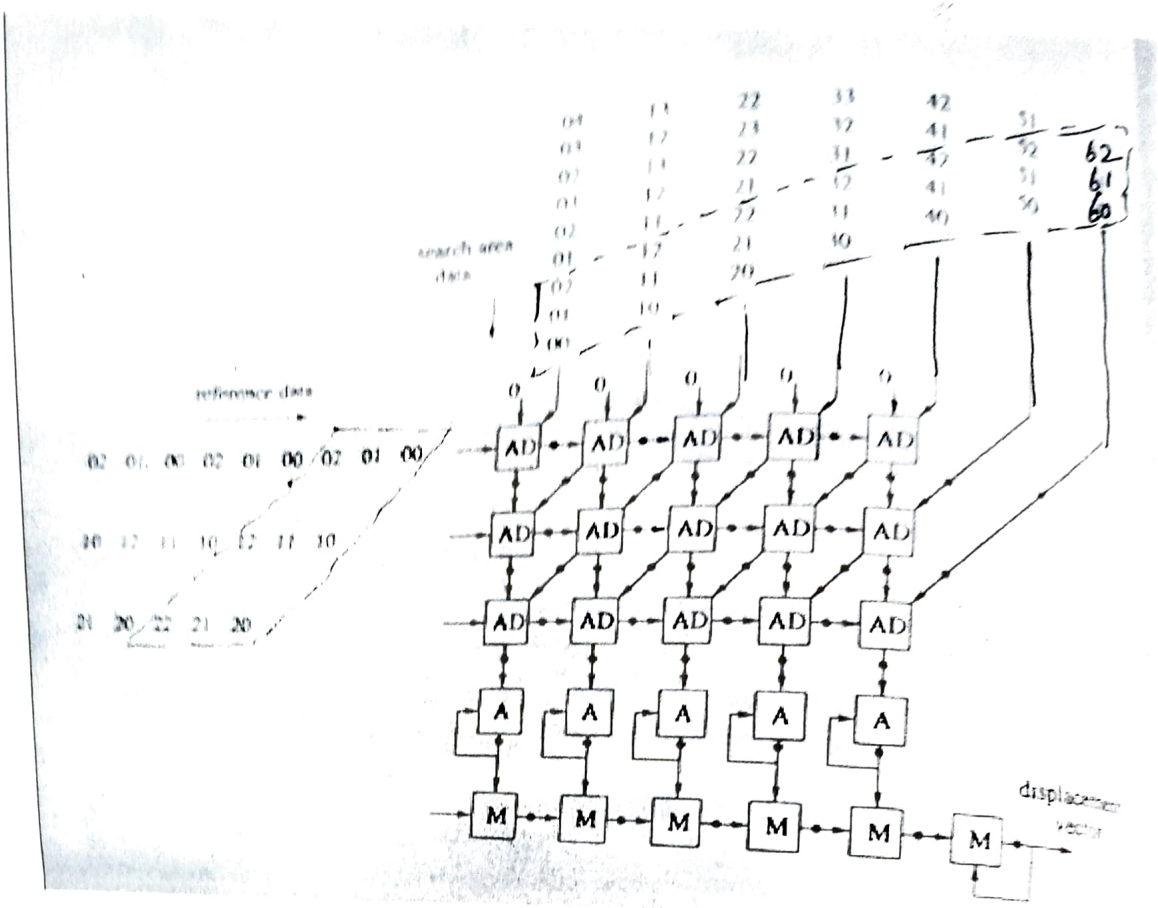
6.. Obtain an efficient 8 -point DCT architecture using algorithm strength reduction.[8]

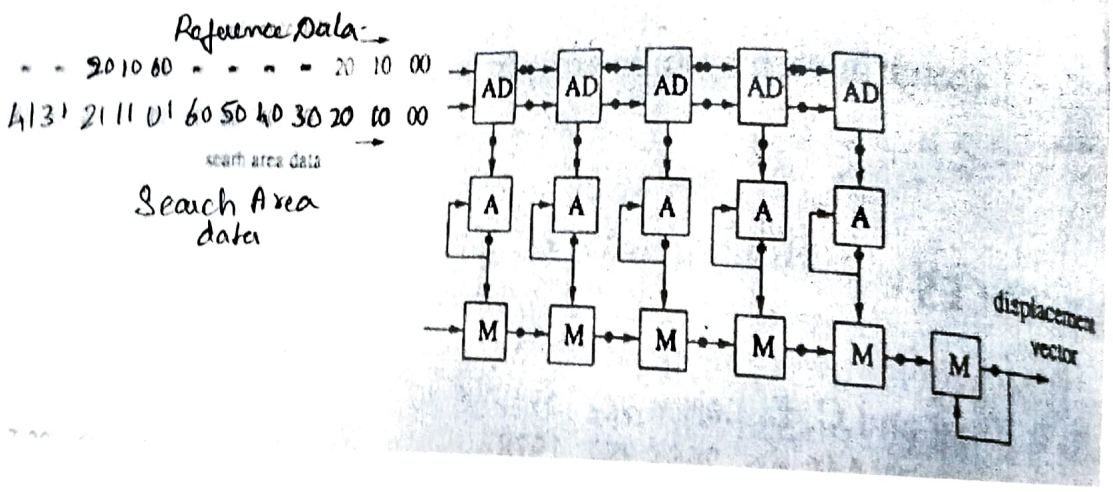
7. Consider the motion estimation computation

$$s(m,n) = \sum_{i-0}^{N-1} \sum_{j=0}^{N-1} |x(i,j) - y(i+m, j+n)| \quad 0 \leq m \quad n \leq 2p \quad v = (m,n) given\ u \quad u = min_{(m,n)} s(m,n)$$

Using the 2D and 1D systolic architecture shown for N=3; P=2; dots represent delay elements. AD computes the absolute difference; A computes addition and M compares s(m,n) and selects the displacement vector. The indexes are data s(I,j) and y(i+m, j+n)

a. Obtain the operation of the systolic architecture [5]
b. How many clock cycles are needed for calculation of one motion vector in each systolic array [5]


search area data
reference data
AD
A
M
displacement vector


Reference Data
search area data
Search Area data
AD
A
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displacement vector