Computer Organization Lab
Project RISC V Simulator

Team 11 – Ultron

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GitHub Repository Link – https://github.com/saurabhkr4/Ultron1.0.git

Phase I:

Highlights of the Project in **Previous** Phase:-

- 13 Instructions executed –
  1)ADD
  2)SUB
  3)MUL
  4)ADDI
  5)SUBI
  6)MULI
  7)LW
  8)SW
  9)BEQ
  10) BNE
  11) BGE
  12) BLT
  13) JAL

- 3 Programs in . asm format are attached in repo-
  1) BubbleSort.asm
  2)sumofTenNaturalNumbers.asm
  3)LoadStorecheck.asm

- User Friendly Interface made using Tkinter which enables show output in Binary, HexaDecimal and Decimal systems
- The Outputs of the registers are visible in the GUI, while the memory Elements are visible in Terminal

- Simulator code written in an easy to interpret language- Python!

Phase II:

Highlights of the Project in this Phase:-

- It diagrammatically shows the pipeline flow of the code in the terminal.
- User can see the output of pipeline diagram in both – Forwarding and Non-Forwarding mode (in terminal).
- It gives the count of Clock Cycles in Forwarding and Non-Forwarding mode.
- It Tells the gives the count of Stalls in Forwarding and Non-Forwarding mode.
- It prints the memory elements after execution of the Program.
- 5 Programs in . asm format are attached in repo-
  - BubbleSort.asm
  - sumofTenNaturalNumbers.asm
  - LoadStorecheck.asm
  - SpecialStall.asm
  - addreg.asm

Possible Further Improvements:

- We couldn’t completely add the pipelining in Tkinter GUI, hence in a proper presentable manner, we have implemented it in Terminal only. This can be improved
- Single Line Implementation can be added

The Backend part was done by Pranav.

The Frontend part and linking of Frontend with Backend was done by Saurabh.

Thanks!

Team Ultron.