Saurabh Shrikant Labde

Computer Architecture · Digital Design · Verification · System Software

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Education

North Carolina State University *Raleigh, NC*

M.S. in Electrical and Computer Engineering *Aug. 2017 - Expected May. 2019*

- **Relevant Courses:** Microprocessor Architecture, Architecture of Parallel Computers , Data Parallel Processor Architecture, ASIC and FPGA Design(Verilog), ASIC Verification(System Verilog), Advanced Verification with UVM, Operating Systems, Compiler Design

University Of Mumbai *Mumbai, India*

B.S. in Electronics and Telecommunications Engineering *Aug. 2013 - May.2017*

- **Relevant Courses:** Digital Electronics, VLSI Design, Neural Networks , Analog Electronics, Microprocessors and Microcontrollers

Skills

Languages	C, C++, Verilog, System Verilog, Python, Ruby, Perl, Assembly (x86, MIPS, ARM), Shell , CUDA, Java
Tools	ModelSim, QuestaSim, Veloce Emulator, Synopsys Design Vision, MATLAB, Xilinx ISE, Git, Make Utility, GDB, Valgrind, LLDB
Platforms	Linux, Unix(MAC OS), Windows, XINU-OS, GPGPU-sim, SNIPER-sim, GEM5-sim
Design	Logic Design, RTL Design, Synthesis, Clock Domain Crossing, Static Timing Analysis,FSM, Low Power Design
Verification	UVM Framework, Functional Verification , Assertions, Coverage, Constrained Random testing, Test Bench Design, Emulation
CPU/GPU	Multilevel Cache, Branch Prediction, Superscalar processors, Vector processors, GPGPU, SIMD, VLIW, Cache Coherence

Work Experience

ARPERS Research Group - NC State University *Raleigh, NC*

Research Student *Jun. 2017 - Aug. 2018*

- Performed a detailed study and analysis of Sniper Multicore simulator and created a tutorial on it for the ARPERS team.
- Ported a set of persistent memory microbenchmarks to work with SNIPER multicore simulator using simulator hooks.
- Created Python scripts to automate the compilation and generation of CPI and power visualizations.

Projects

Verification *(Tools: ModelSim, QuestaSim, Veloce Emulator. Languages: System Verilog , Python Scripting)*

UVM based Block Level Verification IP for AMBA-APB bus Protocol *May. 2018*

- Designed and Implemented a hierarchical and re-usable verification environment for APB protocol using UVM class libraries
- The package includes APB bridge master and APB slave agents, drivers , monitors, environment, sequences and sequencers.

Emulation Compatible Chip Level Verification Environment for LC3 Microcontroller using UVM Framework *Dec. 2018*

- Constructed a hierarchical, re-usable and emulation compatible chip-level verification environment for LC3 Micro-controller using UVM class libraries which includes environments, subenvs, agents, drivers, monitors and BFM's, predictors and scoreboards.
- Designed a detailed test plan and achieved 100% coverage through constrained random testing, assertions and directed test cases.
- Automated the process using python scripts and detected the maximum number of bugs in a class of 120 students.

RTL Design *(Tools: ModelSim, Synopsys Design Vision. Languages: Verilog)*

Hardware accelerator for convolutional neural network using ASIC *Nov. 2017*

- Designed and Implemented a Hardware for two stage convolutional neural network arithmetic. The Design performs the convolution of two 16 bit integers and outputs a 8 bit vector for object classification .
- Design was verified for functional correctness using ModelSim and synthesized using Synopsys Design Vision to be optimized for area and performance .

Architectural Simulators *(Languages: C , C++. Platforms: GPGPU-Sim.)*