

Saurabh Shrikant Labde

COMPUTER ARCHITECTURE · DIGITAL DESIGN · VERIFICATION · SYSTEM SOFTWARE

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Education

North Carolina State University

Raleigh, NC

M.S. IN ELECTRICAL AND COMPUTER ENGINEERING

Aug. 2017 - Expected May. 2019

- **Relevant Courses:** Microprocessor Architecture, Architecture of Parallel Computers, Data Parallel Processor Architecture, ASIC and FPGA Design(Verilog), ASIC Verification(System Verilog), Advanced Verification with UVM, Operating Systems, Compiler Design

University Of Mumbai

Mumbai, India

B.S. IN ELECTRONICS AND TELECOMMUNICATIONS ENGINEERING

Aug. 2013 - May.2017

- **Relevant Courses:** Digital Electronics, VLSI Design, Neural Networks, Analog Electronics, Microprocessors and Microcontrollers

Skills

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|---------------------|--|
| Languages | C, C++, Verilog, System Verilog, Python, Ruby, Perl, Assembly, Shell, CUDA, Java |
| Tools | ModelSim, QuestaSim, Veloce Emulator, Synopsys Design Vision, MATLAB, Xilinx ISE, Git, Make Utility, GDB, Valgrind, LLDB |
| Platforms | Linux, Unix(MAC OS), Windows, XINU-OS, GPGPU-sim, SNIPER-sim, GEM5-sim |
| Design | Logic Design, RTL Design, Synthesis, Clock Domain Crossing, Static Timing Analysis,FSM, Low Power Design |
| Verification | UVM Framework, Functional Verification, Assertions, Coverage, Constrained Random testing, Test Bench Design |
| CPU/GPU | Multilevel Cache, Branch Prediction, Superscalar processors, Vector processors, GPGPU, SIMD, VLIW, Cache Coherence |

Work Experience

ARPERS Research Group - NC State University

Raleigh, NC

RESEARCH STUDENT

Jun. 2017 - Aug. 2018

- Performed a detailed study of Sniper Multicore simulator and created a tutorial on it for the ARPERS team.
- Ported a set of persistent memory microbenchmarks to work with SNIPER multicore simulator with simulator hooks.
- Automated the compilation and generation of CPI and power visualizations with python scripts

Projects

Verification (Tools: ModelSim, QuestaSim, Veloce Emulator. Languages: System Verilog, Python Scripting)

Functional Verification of AMBA APB Protocol using UVM Framework

May. 2018

- Designed and Implemented a hierarchical and re-usable verification environment for APB protocol using UVM class libraries
- Drafted a test plan for verification and achieved a coverage of 100% through constrained random tests and directed testing.

Verification Environment for Pipelined LC3 Microcontroller using UVM Framework

Dec. 2018

- Designed and Implemented a hierarchical, re-usable and emulation compatible chip-level verification environment for Pipelined LC3 Micro-controller using UVM class libraries
- Developed Interface and Environment Packages for all the 5 stages of LC3 pipeline including agents, drivers, BFM's, monitors, environment, subenvironment, predictors and scoreboards
- Designed a detailed test plan and achieved 100% coverage through constrained random testing, assertions and directed test cases.
- Automated the process using python scripts and detected the maximum number of bugs in a class of 120 students.

RTL Design (Tools: ModelSim, Synopsys Design Vision. Languages: Verilog)

Hardware accelerator for convolutional neural network using ASIC

Nov. 2017

- Designed and Implemented a Hardware for two stage convolutional neural network arithmetic. The Design performs the convolution of two 16 bit integers and outputs a 8 bit vector for object classification.
- Design was verified for functional correctness using ModelSim and synthesized using Synopsys Design Vision to be optimized for area and performance.

Architectural Simulators (Languages: C, C++. Platforms: GPGPU-Sim.)