

Saurabh Shrikant Labde

COMPUTER ARCHITECTURE · DIGITAL DESIGN · VERIFICATION · SYSTEM SOFTWARE

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Education

North Carolina State University

Raleigh, NC

M.S. IN ELECTRICAL AND COMPUTER ENGINEERING

Aug. 2017 - Expected May. 2019

- **Relevant Courses:** Microprocessor Architecture, Architecture of Parallel Computers, Advanced Architecture with Data Parallel Processors, ASIC Design with Verilog, ASIC Verification with System Verilog, Advanced Verification with UVM, Operating Systems, Compiler Design

University Of Mumbai

Mumbai, India

B.S. IN ELECTRONICS AND TELECOMMUNICATIONS ENGINEERING

Aug. 2013 - May.2017

- **Relevant Courses:** Digital Electronics, VLSI System Design, Neural Networks, Analog Electronics, Microprocessors and Microcontroller

Skills

Languages	C, C++, Verilog, System Verilog, Python, Ruby, Perl, Assembly, Shell, Java, Ruby on Rails, SQL, CUDA
Tools	ModelSim, QuestaSim, Veloce Emulator, Synopsys Design Vision, MATLAB, Xilinx ISE, Git, Make Utility, GDB, Valgrind, LLDB
Platforms	Linux/Unix, Windows, XINU-OS, GPGPU-sim, SNIPER-sim, GEM5-sim
Design	Logic Design, RTL Design, Synthesis, Clock Domain Crossing, Static Timing Analysis, FSM, Low Power Design
Verification	UVM Framework, Functional Verification, Assertions, Coverage, Constrained Random testing, Test Bench Design
CPU/GPU	Multilevel Cache, Branch Prediction, Superscalar processors, vector processors, SIMD, VLIW, Cache Coherence

Work Experience

ARPERS Research Group - NC State University

Raleigh, NC

RESEARCH STUDENT

Jun. 2017 - Aug. 2018

- Ported the Whisper data structures micro benchmark suite to work with SNIPER multicore simulator.
- Co created and debugged wrapper classes for all the benchmarks.
- Analysied the varying performance of the benchmarks through visualizations generated with scripts.

Projects

Verification Projects (Tools: ModelSim, QuestaSim, Veloce Emulator. Languages: System Verilog)

Functional Verification of AMBA APB Protocol using UVM Framework (SV, Questasim)

May. 2018

- Designed and Implemented a hierarchical and re-usable verification environment for APB protocol using UVM class libraries
- Drafted a test plan for verification and achieved a coverage of 100% through constrained random tests and directed testing.

Verification Environment for Pipelined LC3 Microcontroller using UVM Framework (SV, Questasim, Veloce Emulator)

Dec. 2018

- Designed and Implemented a hierarchical, re-usable and emulation compatible chip-level verification environment for Pipelined LC3 Microcontroller using UVM class libraries
- Developed Interface and Environment Packages for all the 5 stages of LC3 pipeline including agents, drivers, BFM's, monitors, environment, subenvironment, predictors and scoreboards
- Designed a detailed test plan and achieved 100% coverage through constrained random testing, assertions and directed test cases.
- Automated the process using python scripts and detected the maximum number of bugs in a class of 120 students.

Hardware accelerator for convolutional neural network using ASIC (Verilog, MODELSIM, Synopsys Design Vision)

Nov. 2017

- Designed and Implemented a Hardware for two stage convolutional neural network arithmetic. The Design performs the convolution of two 16 bit integers and outputs a 8 bit vector for object classification.
- Design was verified for functional correctness using ModelSim and synthesized using Synopsys Design Vision to be optimized for area and performance.