Saurabh Shrikant Labde

Computer Architecture · Digital Design · Verification · System Software

2510 Avent Ferry Road, Apt 205 , Raleigh , NC - 27606

(+1) 984-218-6364 | sslabde@ncsu.edu | www.saurabhlabde.com | saurabhlabde29 | saurabhlabde

Education

North Carolina State University *Raleigh, NC*

M.S. in Electrical and Computer Engineering *Aug. 2017 - Present*

- **Relevant Courses:** Microprocessor Architecture, Architecture of Parallel Computers , Advanced Architecture with Data Parallel Processors, ASIC Design with Verilog, ASIC Verification with System Verilog, Advanced Verification with UVM, Operating Systems Design, Compiler Design and Optimization

University Of Mumbai *Mumbai, India*

B.S. in Electronics and Telecommunications Engineering *Aug. 2013 - May.2017*

- **Relevant Courses:** Digital Electronics, VLSI System Design, Artificial Neural Networks , Analog Electronics, Microprocessors and Microcontroller

Skills

Languages	C, C++, Verilog, System Verilog, Python, Ruby, Perl, Assembly, Shell , Java, Ruby on Rails, SQL, CUDA
Tools	ModelSim, QuestaSim, Synopsys Design Vision,MATLAB, Xilinx ISE, Git, Make Utility, GDB, Valgrind, LLDB
OS and Packages	Linux/Unix, Windows, XINU-OS, GPGPU-sim, SNIPER-sim, GEM5-sim
Design	Logic Design, RTL Design, Synthesis, Clock Domain Crossing, Static Timing Analysis,FSM, Low Power Design
Verification	UVM Framework, Functional Verification , Assertions, Coverage, Constrained Random testing, Test Bench Design
CPU/GPU Architecture	Multilevel Cache, Branch Prediction,Superscalar processors, vector processors, SIMD, VLIW, Cache Coherence