REPORT-PROGRAM 3

MSI:

Varying cache size and keeping block size constant at 64B:

32KB:

		32KB			
	Cache 0	**Cache 1**	**Cache 2**	**Cache 3**	**Average**
Number of read transactions the cache has received	112661	110830	114938	113428	112964.3
Number of read misses the cache has suffered	6361	6391	6382	6404	6384.5
Number of write transactions the cache has received	11942	11710	12383	12108	12035.75
Number of write misses the cache has suffered.	39	41	42	39	40.25
The total miss rate of the cache	0.051363	0.052489	0.050455	0.051324	0.051407
Number of dirty cache blocks written back to the main memory	647	635	655	646	645.75
Number of BusRds that have been issued.	6361	6391	6382	6404	6384.5
Number of BusRdXs that have been issued	716	700	725	714	713.75
Number of BusUpgrs that have been issued	0	0	0	0	0

64KB:

		64KB			
	Cache 0	**Cache 1**	**Cache 2**	**Cache 3**	**Average**
Number of read transactions the cache has received	112661	110830	114938	113428	112964.3
Number of read misses the cache has suffered	6044	6063	6044	6070	6057.25
Number of write transactions the cache has received	11942	11710	12383	12108	12035.75
Number of write misses the cache has suffered.	39	41	42	39	40.25
The total miss rate of the cache	0.048819	0.049812	0.0478	0.048663	0.047877
Number of dirty cache blocks written back to the main memory	573	555	587	570	571.25
Number of BusRds that have been issued.	6044	6063	6044	6070	6055.25
Number of BusRdXs that have been issued	716	700	725	714	713.75
Number of BusUpgrs that have been issued	0	0	0	0	0

128KB:

		128kB			
	Cache 0	**Cache 1**	**Cache 2**	**Cache 3**	**Average**
Number of read transactions the cache has received	112661	110830	114938	113428	112964.3
Number of read misses the cache has suffered	5842	5865	5837	5879	5855.75
Number of write transactions the cache has received	11942	11710	12383	12108	12035.75
Number of write misses the cache has suffered.	39	41	42	39	40.25
The total miss rate of the cache	0.047198	0.048197	0.046175	0.047142	0.047118
Number of dirty cache blocks written back to the main memory	420	434	446	414	428.5
Number of BusRds that have been issued.	5842	5865	5837	5879	5855.75
Number of BusRdXs that have been issued	716	700	725	714	713.75
Number of BusUpgrs that have been issued	0	0	0	0	0

256KB:

		256kB			
	Cache 0	**Cache 1**	**Cache 2**	**Cache 3**	**Average**
Number of read transactions the cache has received	112661	110830	114938	113428	112964.3
Number of read misses the cache has suffered	5775	5865	5771	5813	5806
Number of write transactions the cache has received	11942	11710	12383	12108	12035.75
Number of write misses the cache has suffered.	39	41	42	39	40.25
The total miss rate of the cache	0.04666	0.047707	0.045656	0.046616	0.04666
Number of dirty cache blocks written back to the main memory	254	235	278	234	250.25
Number of BusRds that have been issued.	5775	5805	5771	5813	5791
Number of BusRdXs that have been issued	716	700	725	714	713.75
Number of BusUpgrs that have been issued	0	0	0	0	0

512KB:

		512kB			
	Cache 0	**Cache 1**	**Cache 2**	**Cache 3**	**Average**
Number of read transactions the cache has received	112661	110830	114938	113428	112964.3
Number of read misses the cache has suffered	5757	5792	5756	5796	5775.25
Number of write transactions the cache has received	11942	11710	12383	12108	12035.75
Number of write misses the cache has suffered.	39	41	42	39	40.25
The total miss rate of the cache	0.046516	0.047601	0.045538	0.046481	0.046534
Number of dirty cache blocks written back to the main memory	190	170	205	171	184
Number of BusRds that have been issued.	5757	5792	5756	5796	5775.25
Number of BusRdXs that have been issued	716	700	725	714	713.75
Number of BusUpgrs that have been issued	0	0	0	0	0

Varying Block size and keeping cache size constant at 1MB:

64B:

		64B			
	Cache 0	**Cache 1**	**Cache 2**	**Cache 3**	**Average**
Number of read transactions the cache has received	112661	110830	114938	113428	112964.3
Number of read misses the cache has suffered	5752	5781	5752	5790	5768.75
Number of write transactions the cache has received	11942	11710	12383	12108	12035.75
Number of write misses the cache has suffered.	39	41	42	39	40.25
The total miss rate of the cache	0.046476	0.047511	0.045507	0.046433	0.046482
Number of dirty cache blocks written back to the main memory	170	155	186	157	167
Number of BusRds that have been issued.	5752	5781	5752	5790	5768.75
Number of BusRdXs that have been issued	716	700	725	714	713.75
Number of BusUpgrs that have been issued	0	0	0	0	0

128B:

		128B			
	Cache 0	**Cache 1**	**Cache 2**	**Cache 3**	**Average**
Number of read transactions the cache has received	112661	110830	114938	113428	112964.3
Number of read misses the cache has suffered	5340	5386	5341	5384	5362.75
Number of write transactions the cache has received	11942	11710	12383	12108	12035.75
Number of write misses the cache has suffered.	39	40	42	39	40
The total miss rate of the cache	0.043169	0.044279	0.042279	0.043199	0.043232
Number of dirty cache blocks written back to the main memory	275	250	283	269	269.25
Number of BusRds that have been issued.	5340	5386	5341	5384	5362.75
Number of BusRdXs that have been issued	729	711	745	733	729.5
Number of BusUpgrs that have been issued	0	0	0	0	0

256B:

		256B			
	Cache 0	**Cache 1**	**Cache 2**	**Cache 3**	**Average**
Number of read transactions the cache has received	112661	110830	114938	113428	112964.3
Number of read misses the cache has suffered	5023	5070	5004	5084	5045.25
Number of write transactions the cache has received	11942	11710	12383	12108	12035.75
Number of write misses the cache has suffered.	39	40	42	39	40
The total miss rate of the cache	0.040625	0.041701	0.039632	0.04809	0.042512
Number of dirty cache blocks written back to the main memory	363	342	383	332	355
Number of BusRds that have been issued.	5023	5070	5004	5084	5045.25
Number of BusRdXs that have been issued	751	735	780	743	752.25
Number of BusUpgrs that have been issued	0	0	0	0	0

MOSI:

Varying cache size and keeping block size constant at 64B:

32KB:

		32KB			
	Cache 0	**Cache 1**	**Cache 2**	**Cache 3**	**Average**
Number of read transactions the cache has received	112661	110830	114938	113428	112964.3
Number of read misses the cache has suffered	6361	6391	6382	6404	6384.5
Number of write transactions the cache has received	11942	11710	12383	12108	12035.75
Number of write misses the cache has suffered.	39	41	42	39	40.25
The total miss rate of the cache	0.051363	0.052489	0.050455	0.051324	0.051478
Number of dirty cache blocks written back to the main memory	550	548	549	561	552
Number of BusRds that have been issued.	6361	6391	6382	6404	6384.5
Number of BusRdXs that have been issued	39	41	42	39	40.25
Number of BusUpgrs that have been issued	677	659	683	675	673.5

64KB:

		64kB			
	Cache 0	**Cache 1**	**Cache 2**	**Cache 3**	**Average**
Number of read transactions the cache has received	112661	110830	114938	113428	112964.3
Number of read misses the cache has suffered	6044	6063	6044	6070	6055.25
Number of write transactions the cache has received	11942	11710	12383	12108	12035.75
Number of write misses the cache has suffered.	39	41	42	39	40.25
The total miss rate of the cache	0.048819	0.049812	0.0478	0.048663	0.048773
Number of dirty cache blocks written back to the main memory	471	466	475	485	474.25
Number of BusRds that have been issued.	6044	6063	6044	6070	6055.25
Number of BusRdXs that have been issued	39	41	42	39	40.25
Number of BusUpgrs that have been issued	677	659	683	675	673.5

128KB:

		128kB			
	Cache 0	**Cache 1**	**Cache 2**	**Cache 3**	**Average**
Number of read transactions the cache has received	112661	110830	114938	113428	112964.3
Number of read misses the cache has suffered	5842	5865	5837	5879	5855.75
Number of write transactions the cache has received	11942	11710	12383	12108	12035.75
Number of write misses the cache has suffered.	39	41	42	39	40.25
The total miss rate of the cache	0.047198	0.048197	0.046175	0.047142	0.047178
Number of dirty cache blocks written back to the main memory	315	343	331	326	328.75
Number of BusRds that have been issued.	5842	5865	5837	5879	5855.75
Number of BusRdXs that have been issued	39	41	42	39	40.25
Number of BusUpgrs that have been issued	677	659	683	675	673.5

256KB:

		256kB			
	Cache 0	**Cache 1**	**Cache 2**	**Cache 3**	**Average**
Number of read transactions the cache has received	112661	110830	114938	113428	112964.3
Number of read misses the cache has suffered	5775	5865	5771	5813	5806
Number of write transactions the cache has received	11942	11710	12383	12108	12035.75
Number of write misses the cache has suffered.	39	41	42	39	40.25
The total miss rate of the cache	0.046666	0.047707	0.045656	0.046616	0.046659
Number of dirty cache blocks written back to the main memory	141	143	158	146	147
Number of BusRds that have been issued.	5775	5805	5771	5813	5791
Number of BusRdXs that have been issued	39	41	42	39	40.25
Number of BusUpgrs that have been issued	677	659	683	675	673.5

512KB:

		512kB			
	Cache 0	**Cache 1**	**Cache 2**	**Cache 3**	**Average**
Number of read transactions the cache has received	112661	110830	114938	113428	112964.3
Number of read misses the cache has suffered	5757	5792	5756	5796	5775.25
Number of write transactions the cache has received	11942	11710	12383	12108	12035.75
Number of write misses the cache has suffered.	39	41	42	39	40.25
The total miss rate of the cache	0.046516	0.047601	0.045538	0.046481	0.046534
Number of dirty cache blocks written back to the main memory	74	78	84	83	79.75
Number of BusRds that have been issued.	5757	5792	5756	5796	5775.25
Number of BusRdXs that have been issued	39	41	42	39	40.25
Number of BusUpgrs that have been issued	677	659	683	675	673.5

Varying Block size and keeping cache size constant at 1MB:

64B:

		64B			
	Cache 0	**Cache 1**	**Cache 2**	**Cache 3**	**Average**
Number of read transactions the cache has received	112661	110830	114938	113428	112964.3
Number of read misses the cache has suffered	5752	5781	5752	5790	5768.75
Number of write transactions the cache has received	11942	11710	12383	12108	12035.75
Number of write misses the cache has suffered.	39	41	42	39	40.25
The total miss rate of the cache	0.046476	0.047511	0.045507	0.046433	0.046482
Number of dirty cache blocks written back to the main memory	54	62	65	68	62.25
Number of BusRds that have been issued.	5752	5781	5752	5790	5768.75
Number of BusRdXs that have been issued	39	41	42	39	40.25
Number of BusUpgrs that have been issued	677	659	683	675	673.5

128B:

		128B			
	Cache 0	**Cache 1**	**Cache 2**	**Cache 3**	**Average**
Number of read transactions the cache has received	112661	110830	114938	113428	112964.3
Number of read misses the cache has suffered	5340	5386	5341	5384	5362.75
Number of write transactions the cache has received	11942	11710	12383	12108	12035.75
Number of write misses the cache has suffered.	39	40	42	39	40
The total miss rate of the cache	0.043169	0.044279	0.042279	0.043199	0.043232
Number of dirty cache blocks written back to the main memory	111	121	117	134	120.75
Number of BusRds that have been issued.	5340	5386	5341	5384	5362.75
Number of BusRdXs that have been issued	39	40	42	39	40
Number of BusUpgrs that have been issued	690	671	703	694	689.5

256B:

		256B			
	Cache 0	**Cache 1**	**Cache 2**	**Cache 3**	**Average**
Number of read transactions the cache has received	112661	110830	114938	113428	112964.3
Number of read misses the cache has suffered	5023	5070	5004	5084	5045.25
Number of write transactions the cache has received	11942	11710	12383	12108	12035.75
Number of write misses the cache has suffered.	39	40	42	39	40
The total miss rate of the cache	0.040625	0.041701	0.039632	0.040809	0.040692
Number of dirty cache blocks written back to the main memory	152	164	152	162	157.5
Number of BusRds that have been issued.	5023	5070	5004	5084	5045.25
Number of BusRdXs that have been issued	39	40	42	39	40
Number of BusUpgrs that have been issued	712	695	738	704	712.25

MOESI:

Varying cache size and keeping block size constant at 64B:

32KB:

		32kB			
	Cache 0	**Cache 1**	**Cache 2**	**Cache 3**	**Average**
Number of read transactions the cache has received	112661	110830	114938	113428	112964.25
Number of read misses the cache has suffered	6361	6391	6382	6404	6384.5
Number of write transactions the cache has received	11942	11710	12383	12108	12035.75
Number of write misses the cache has suffered.	39	41	42	39	40.25
The total miss rate of the cache	0.051363	0.052489	0.050455	0.051324	0.05140775
Number of dirty cache blocks written back to the main memory	550	548	549	561	552
Number of BusRds that have been issued.	6361	6391	6382	6404	6384.5
Number of BusRdXs that have been issued	39	41	42	39	40.25
Number of BusUpgrs that have been issued	674	650	674	662	665

64KB:

		64kB			
	Cache 0	**Cache 1**	**Cache 2**	**Cache 3**	**Average**
Number of read transactions the cache has received	112661	110830	114938	113428	112964.25
Number of read misses the cache has suffered	6044	6063	6044	6070	6055.25
Number of write transactions the cache has received	11942	11710	12383	12108	12035.75
Number of write misses the cache has suffered.	39	41	42	39	40.25
The total miss rate of the cache	0.048819	0.049812	0.0478	0.048663	0.0487735
Number of dirty cache blocks written back to the main memory	471	466	475	485	474.25
Number of BusRds that have been issued.	6044	6063	6044	6070	6055.25
Number of BusRdXs that have been issued	39	41	42	39	40.25
Number of BusUpgrs that have been issued	674	650	674	662	665

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Number of write transactions the cache has received	11942	11710	12383	12108	12035.75
Number of write misses the cache has suffered.	39	41	42	39	40.25
The total miss rate of the cache	0.04666	0.047707	0.045656	0.046616	0.04666
Number of dirty cache blocks written back to the main memory	141	143	158	146	147
Number of BusRds that have been issued.	5775	5805	5771	5813	5791
Number of BusRdXs that have been issued	39	41	42	39	40.25
Number of BusUpgrs that have been issued	674	650	674	662	665

512KB:

		512kB			
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Number of read misses the cache has suffered	5757	5792	5756	5796	5775.25
Number of write transactions the cache has received	11942	11710	12383	12108	12035.75
Number of write misses the cache has suffered.	39	41	42	39	40.25
The total miss rate of the cache	0.046516	0.047601	0.045538	0.046481	0.046534
Number of dirty cache blocks written back to the main memory	74	78	84	83	79.75
Number of BusRds that have been issued.	5757	5792	5756	5796	5775.25
Number of BusRdXs that have been issued	39	41	42	39	40.25
Number of BusUpgrs that have been issued	674	650	674	662	665

Varying Block size and keeping cache size constant at 1MB:

64B:

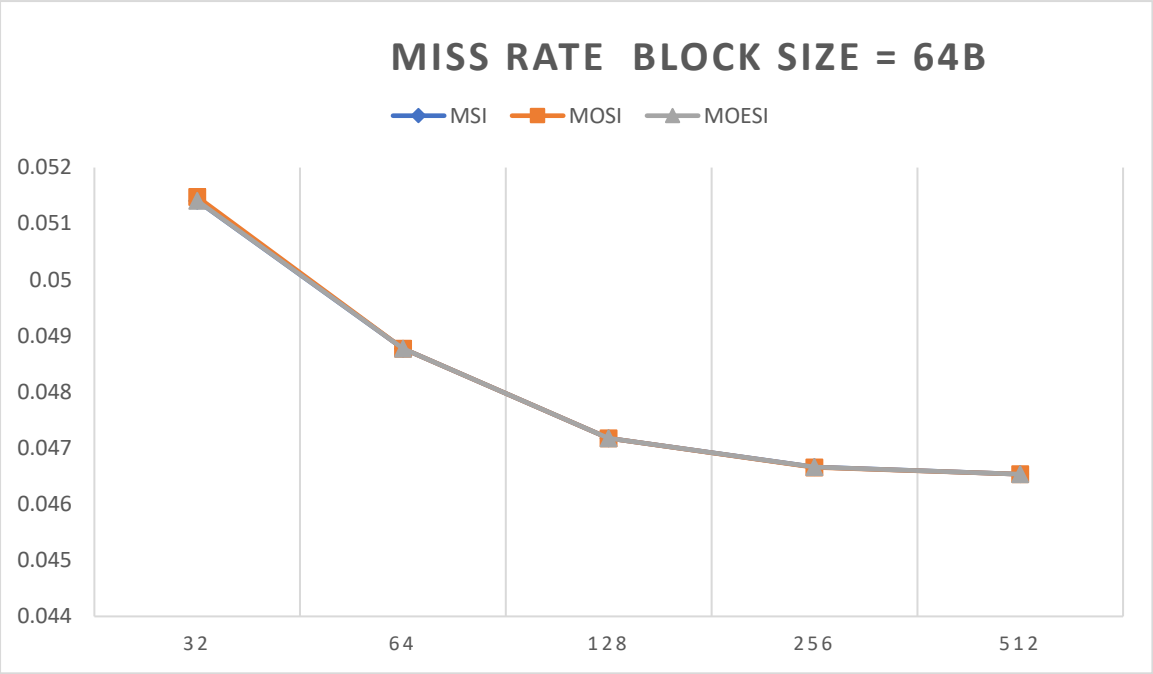
		64B			
	Cache 0	**Cache 1**	**Cache 2**	**Cache 3**	**Average**
Number of read transactions the cache has received	112661	110830	114938	113428	112964.25
Number of read misses the cache has suffered	5752	5781	5752	5790	5768.25
Number of write transactions the cache has received	11942	11710	12383	12108	12035.75
Number of write misses the cache has suffered.	39	41	42	39	40.25
The total miss rate of the cache	0.046476	0.047511	0.045507	0.046433	0.0648175
Number of dirty cache blocks written back to the main memory	54	62	65	68	62.25
Number of BusRds that have been issued.	5752	5781	5752	5790	5768.75
Number of BusRdXs that have been issued	39	41	42	39	40.25
Number of BusUpgrs that have been issued	674	650	674	662	665

128B:

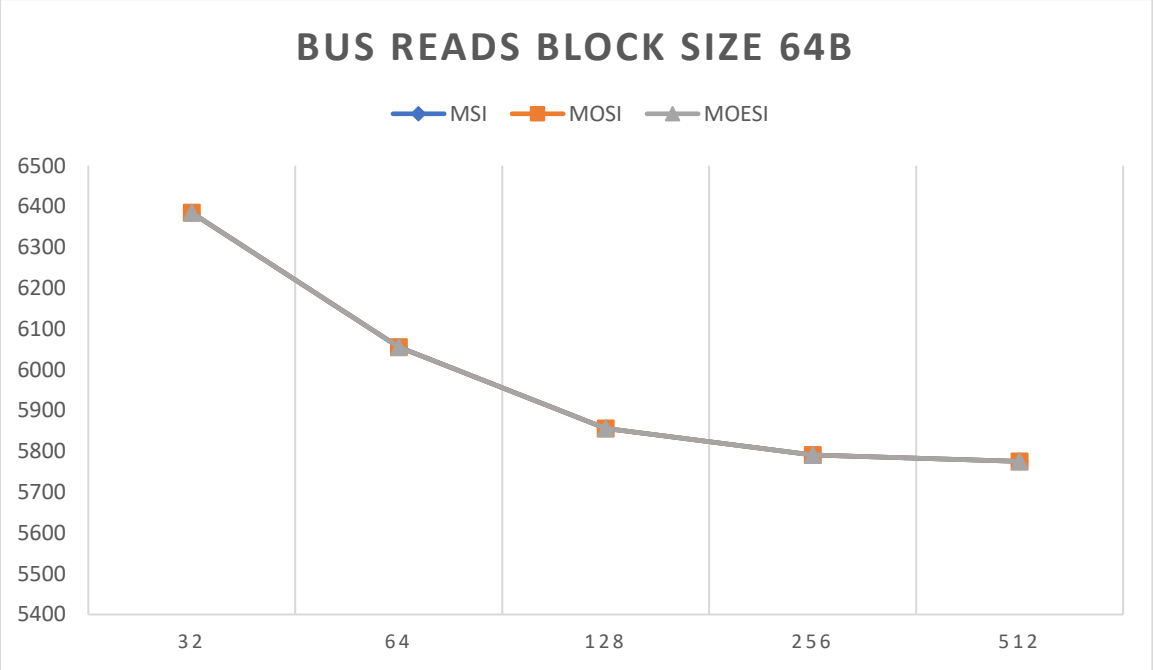
		128B			
	Cache 0	**Cache 1**	**Cache 2**	**Cache 3**	**Average**
Number of read transactions the cache has received	112661	110830	114938	113428	112964.25
Number of read misses the cache has suffered	5340	5386	5341	5384	5362.75
Number of write transactions the cache has received	11942	11710	12383	12108	12035.75
Number of write misses the cache has suffered.	39	40	42	39	40
The total miss rate of the cache	0.043169	0.044279	0.042279	0.043191	0.0432295
Number of dirty cache blocks written back to the main memory	111	121	117	134	120.75
Number of BusRds that have been issued.	5340	5386	5341	5384	5362.75
Number of BusRdXs that have been issued	39	40	42	39	40
Number of BusUpgrs that have been issued	688	663	695	682	682

256B:

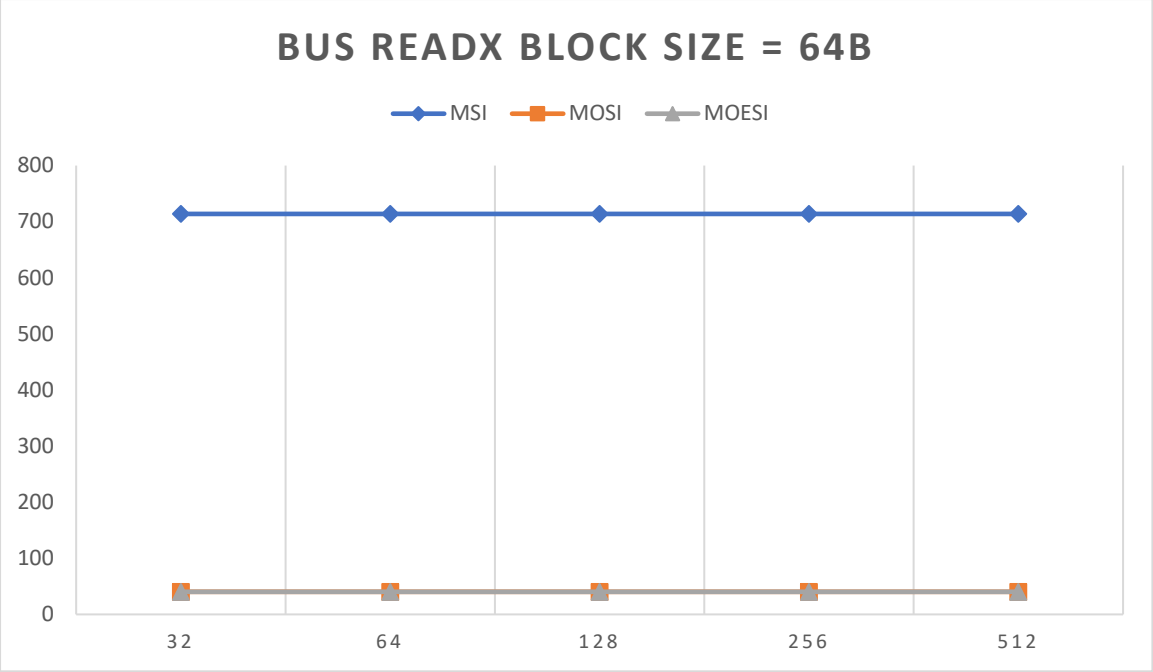
		256B			
	Cache 0	**Cache 1**	**Cache 2**	**Cache 3**	**Average**
Number of read transactions the cache has received	112661	110830	114938	113428	112964.3
Number of read misses the cache has suffered	5023	5070	5004	5084	5045.25
Number of write transactions the cache has received	11942	11710	12383	12108	12035.75
Number of write misses the cache has suffered.	39	40	42	39	40
The total miss rate of the cache	0.040625	0.041701	0.039632	0.040809	0.040692
Number of dirty cache blocks written back to the main memory	152	164	152	162	157.5
Number of BusRds that have been issued.	5023	5070	5004	5084	504.25
Number of BusRdXs that have been issued	39	40	42	39	40
Number of BusUpgrs that have been issued	710	687	731	692	705



As the cache size increases, the capacity to store new data increases therefore we see a decrease in the miss rate.



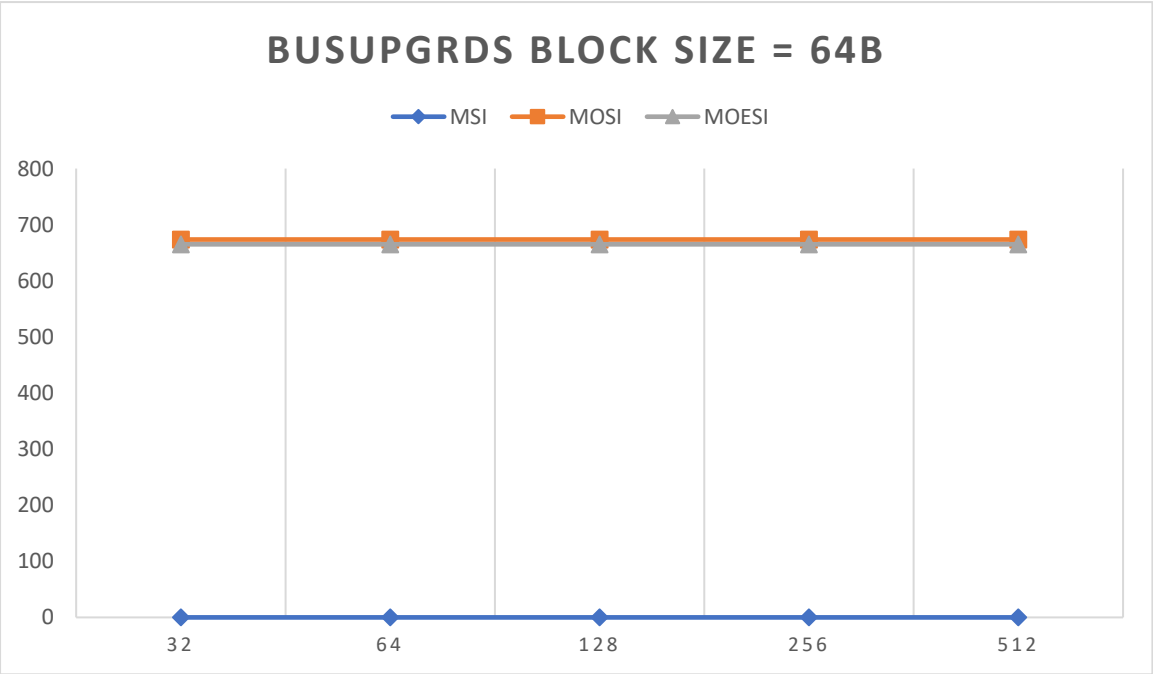
From the previous we graph we conclude that the increase in cache size decreases the miss rate and we also know from the results we know that the number of Bus reads are equal to the number of read misses. Thus, as cache size increases number of bus reads decreases.



In MSI, in case of read followed by write operations, two Bus transactions occur, a BusRd and a BusRdX (to invalidate other copies). This happens regardless of whether the block is in only one cache or shared by other caches. The BusRdXs in the case where the block is not shared by other caches are unnecessary.

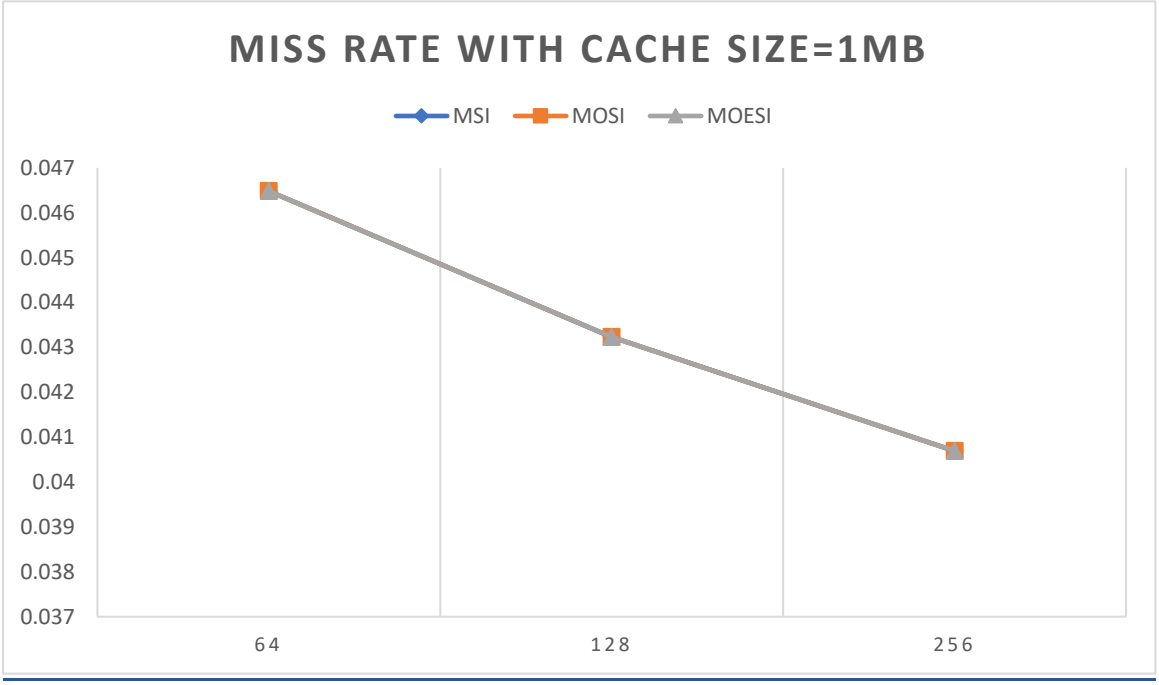
This problem is eliminated in case of MOSI and MOESI protocols and thus we see a decrease in the number of BusRdXs.

Also, number of BusRdXs issued depends on the number of write requests and has no dependency on the cache size. Thus, as cache size increases the BusRdX remains constant.

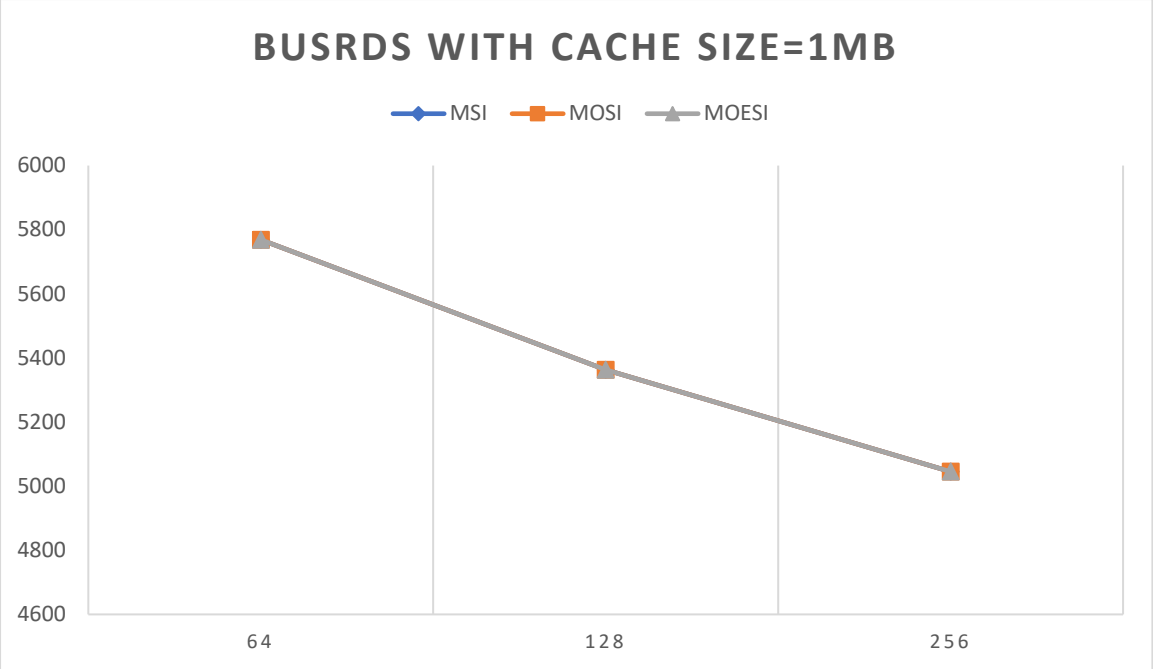


In case of a BusRdX, the memory controller has no way to distinguish between the case where the requesting cache block has a copy and only needs to upgrade or does not have a copy and needs it from memory. If the cache block only needs to upgrade, then the memory transaction is unnecessary and thus MOSI and MOESI protocols use BusUpgr request for this case.

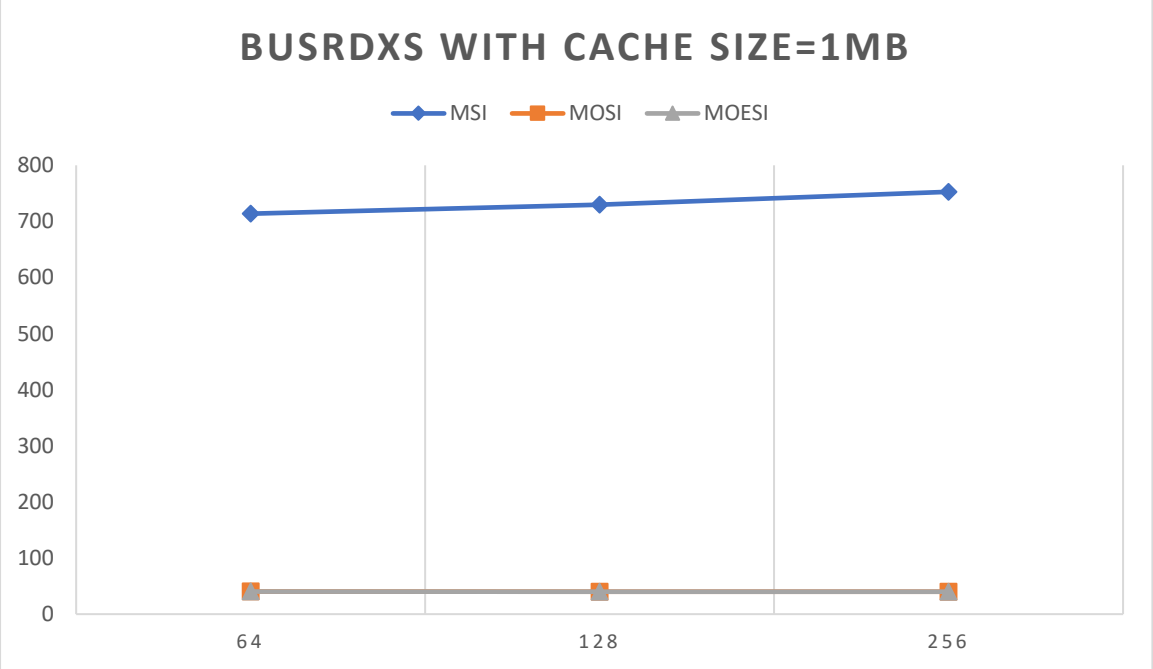
Also, number of BusUpgrs issued depends on the number of write requests and has no dependency on the cache size. Thus, as cache size increases the BusUpgr remains constant.



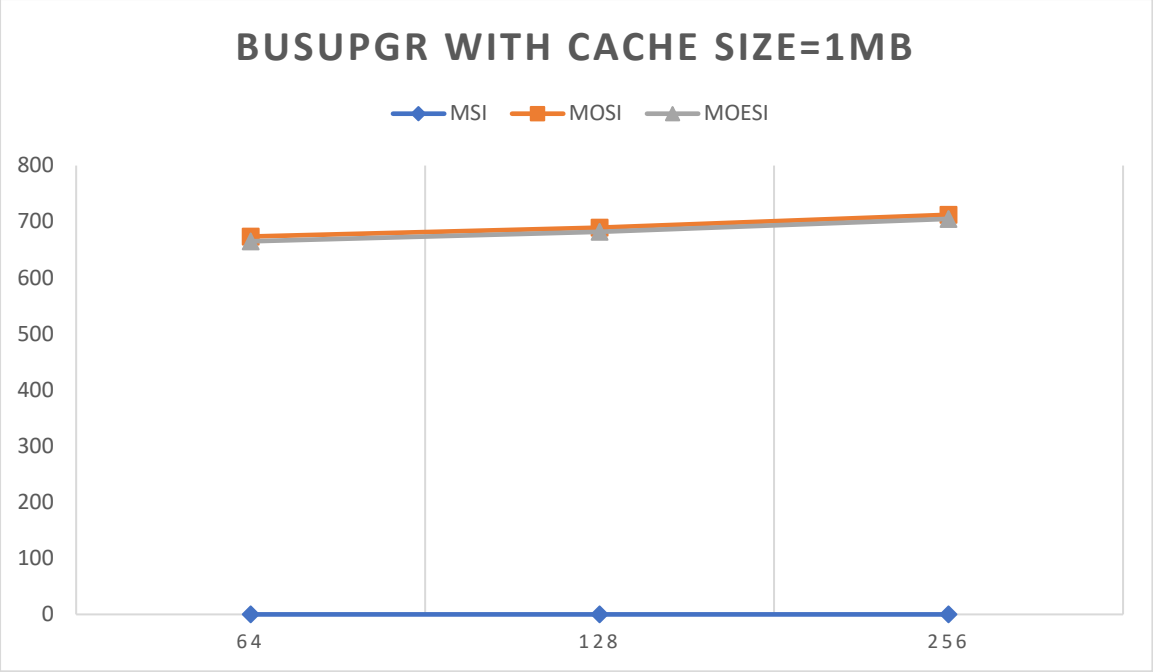
Caches operate in the unit of blocks, thus, in case of miss an entire block is fetched from the memory. Thus, if we increase the block size due to spatial locality the number of misses will reduce. Thus, miss rate decreases with increasing block size.



From the previous graph we concluded that the miss rate thereby the number of misses reduces by increasing the block size. We know that the number of BusRds is equal to the number of read misses. Thus, increasing the cache block size will decrease the number of BusRds.



From the discussion for BusRdX in case of constant block size we concluded that MOSI and MOESI avoids unnecessary BusRdXs. The same happens in case of varying block size, only difference is that the BusRdXs increase with increase in Block size since they are dependent on the number of write hits which will increase with increase in block size.



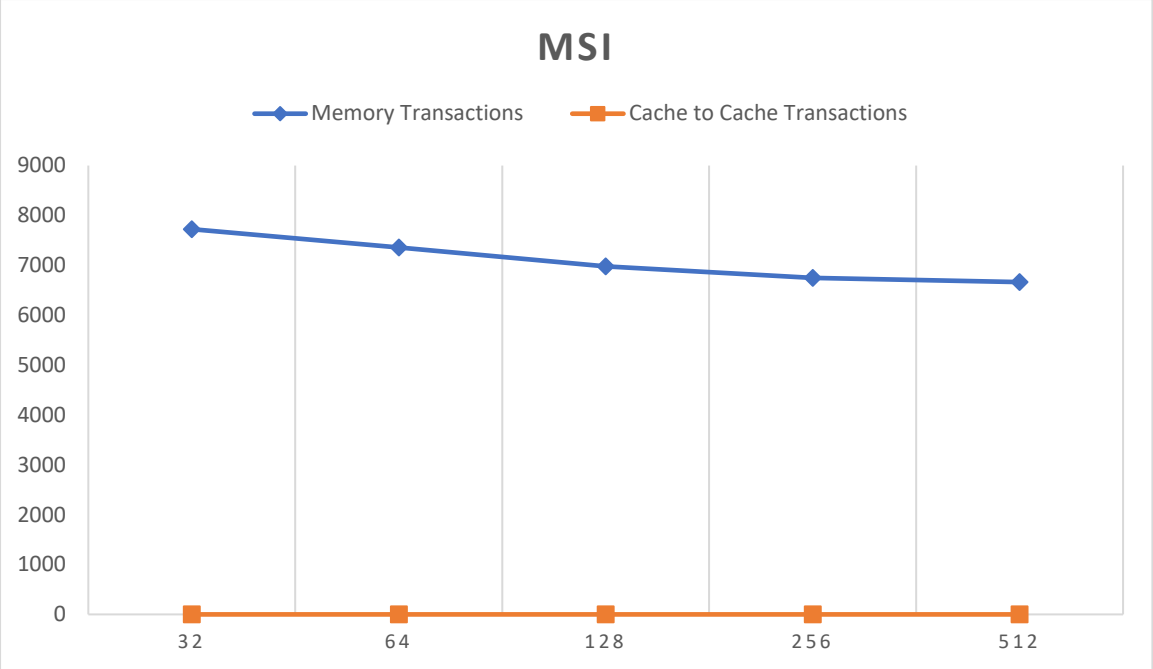
As the block size increases the number of write hits will increase and since the BusUpgr requests are directly proportional to the number of write hits, we see an increase in the number of BusUpgr with increasing block size. Also, for MOESI when a block is in E state there is no bus transaction in case of a write hit and thus number of MOESI BusUpgr is less than that of MOSI.

BLOCK SIZE: 64B

PROTOCOL: MSI

Cache 0:

L1 Cache Size (Kilo Bytes)	Memory Transactions	Cache to Cache Transactions
32	**7724**	**0**
64	**7356**	**0**
128	**6978**	**0**
256	**6745**	**0**
512	**6663**	**0**

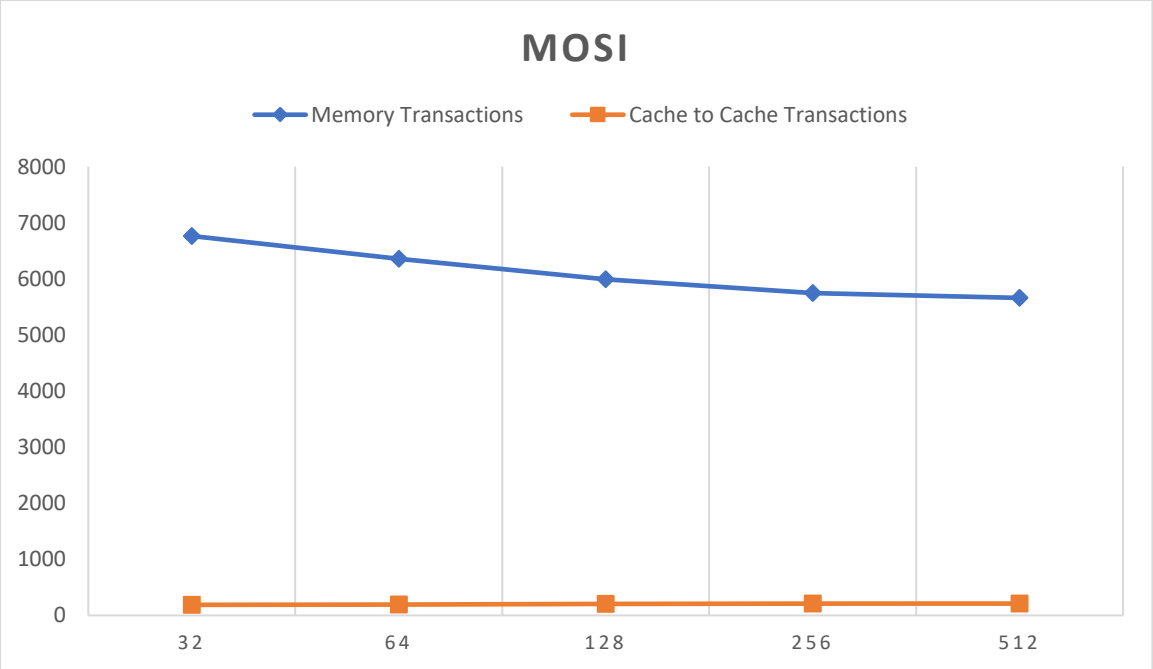


The MSI protocol does not support cache to cache transactions. Also, as the cache size increases the number of misses reduces thereby reducing the number of memory transactions.

PROTOCOL: MOSI

Cache 0:

L1 Cache Size (Kilo Bytes)	Memory Transactions	Cache to Cache Transactions
32	**6762**	**188**
64	**6358**	**196**
128	**5992**	**204**
256	**5745**	**210**
512	**5659**	**211**

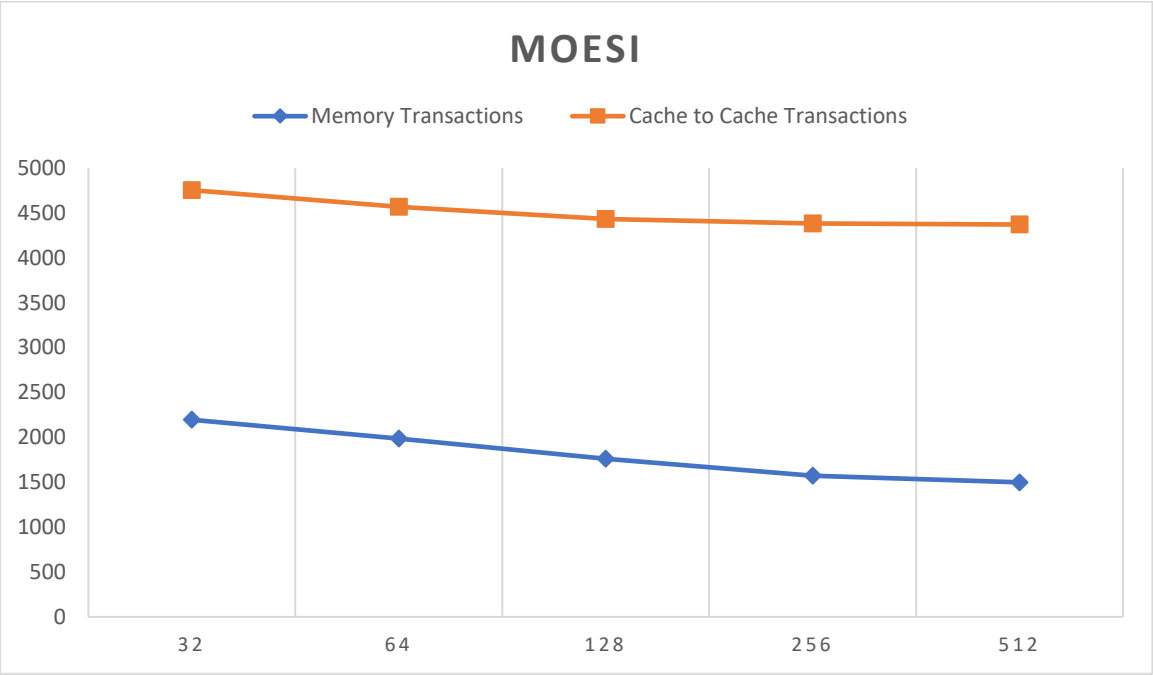


Cache to cache transactions for MOSI protocols occur when there is BusRd and the block is in owned or modified state. As cache size increases, the number of misses reduces thereby reducing total number of transactions.

PROTOCOL: MOESI

Cache 0:

L1 Cache Size (Kilo Bytes)	Memory Transactions	Cache to Cache Transactions
32	**2196**	**4754**
64	**1985**	**4569**
128	**1763**	**4433**
256	**1571**	**4384**
512	**1499**	**4371**



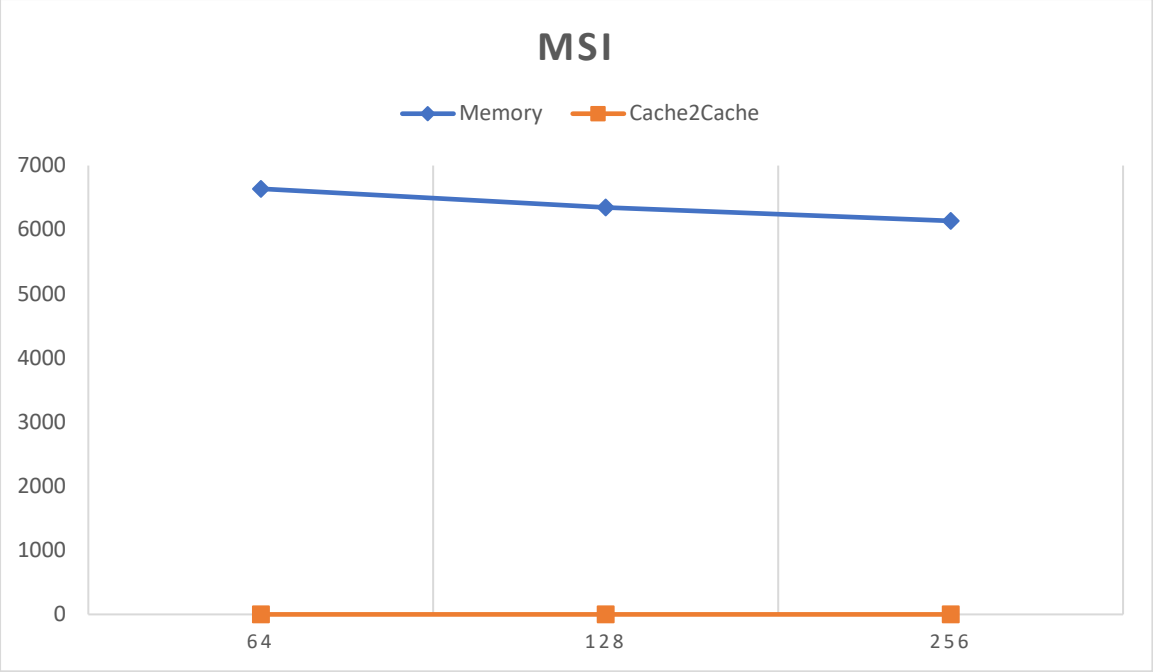
Cache to cache transactions for MOESI protocols occur when there is BusRd and the block is in exclusive or owned or modified state. As cache size increases, the number of misses reduces thereby reducing total number of transactions.

CACHE SIZE: 1MB

PROTOCOL: MSI

Cache 0:

Block Size(Bytes)	Memory Transactions	Cache to Cache Transactions
64	**6638**	**0**
128	**6344**	**0**
256	**6137**	**0**

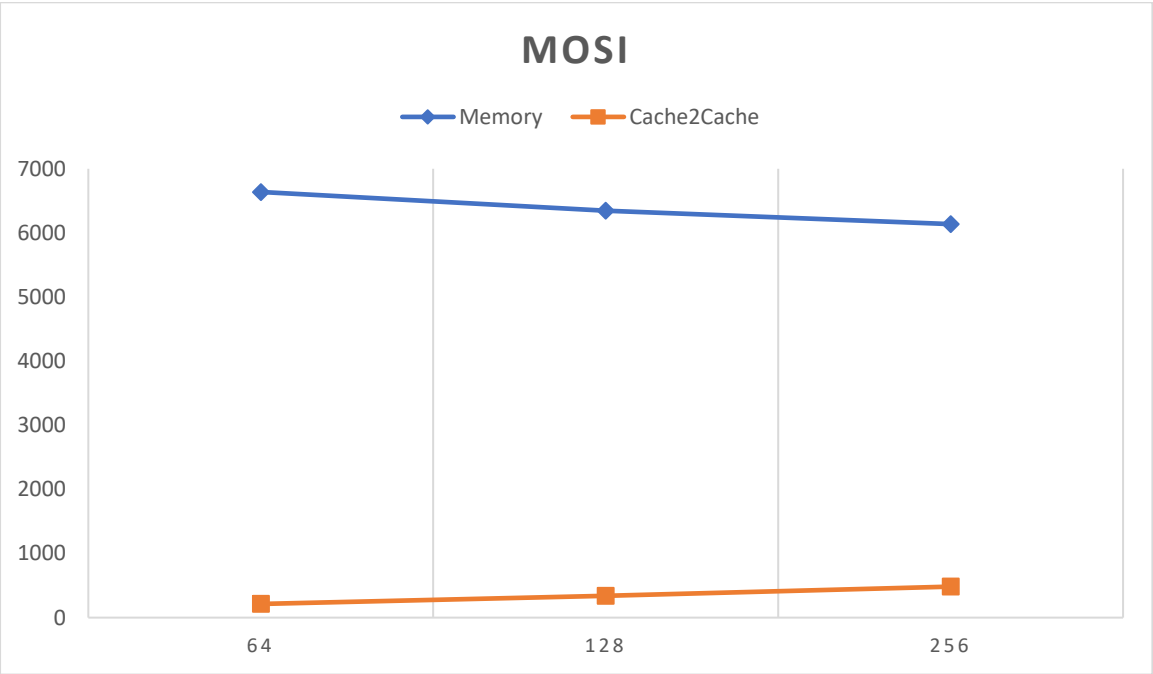


The MSI protocol does not support cache to cache transactions. Also, as the block size increases the number of misses reduces thereby reducing the number of memory transactions.

PROTOCOL: MOSI

Cache 0:

Block Size(Bytes)	Memory Transactions	Cache to Cache Transactions
64	**5632**	**213**
128	**5152**	**338**
256	**4731**	**483**

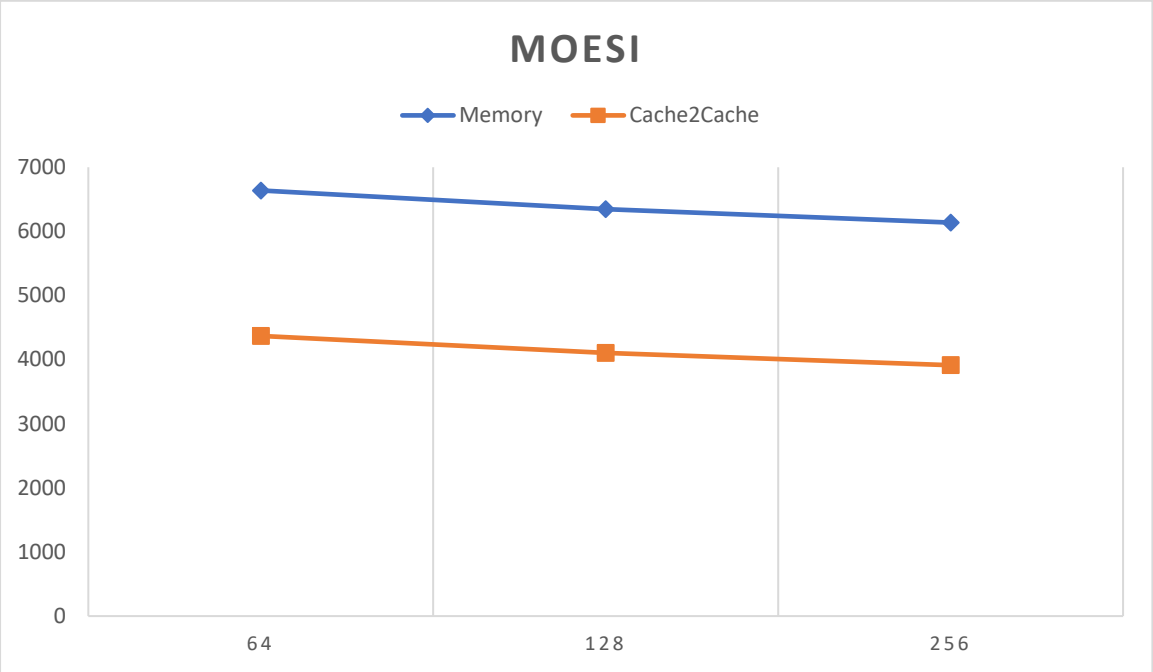


Cache to cache transactions for MOSI protocols occur when there is BusRd and the block is in owned or modified state. As block size increases, the number of misses reduces thereby reducing total number of transactions.

PROTOCOL: MOESI

Cache 0:

Block Size(Bytes)	Memory Transactions	Cache to Cache Transactions
64	**1476**	**4369**
128	**1386**	**4104**
256	**1301**	**3913**



Cache to cache transactions for MOESI protocols occur when there is BusRd and the block is in exclusive or owned or modified state. As block size increases, the number of misses reduces thereby reducing total number of transactions.