Compiled SW Kernels Library

- Conv2D
- MaxPool
- SoftMax
- ReLU/LeakyReLU

Objective Function(s):
<Energy,Throughput,Latency,...>

DNN Description

Layer	Input	WTS
Conv	416x416x3	3x3x16
MaxPool	416x416x16	x
Conv	208x208x16	3x3x64
...	...	...

Mapping Framework

1. Tiling Parameters
2. Schedule
3. Data Resolution

Architecture Specification

cores=MxN
L2: on-chip buffer=256KB
L1:core DM=16KB,PM=16KB
BusWidth=64 bits
MACs per core per cycle=256

Use Cases

Optimizing memory accesses of CNN to improve energy efficiency on CNN Accelerators
Optimizing throughput and energy efficiency of LSTM/RNN
Data Resolution for mapping SOM on DRRA/FPGA
Mapping Homography CNN on CGRA/DRRA