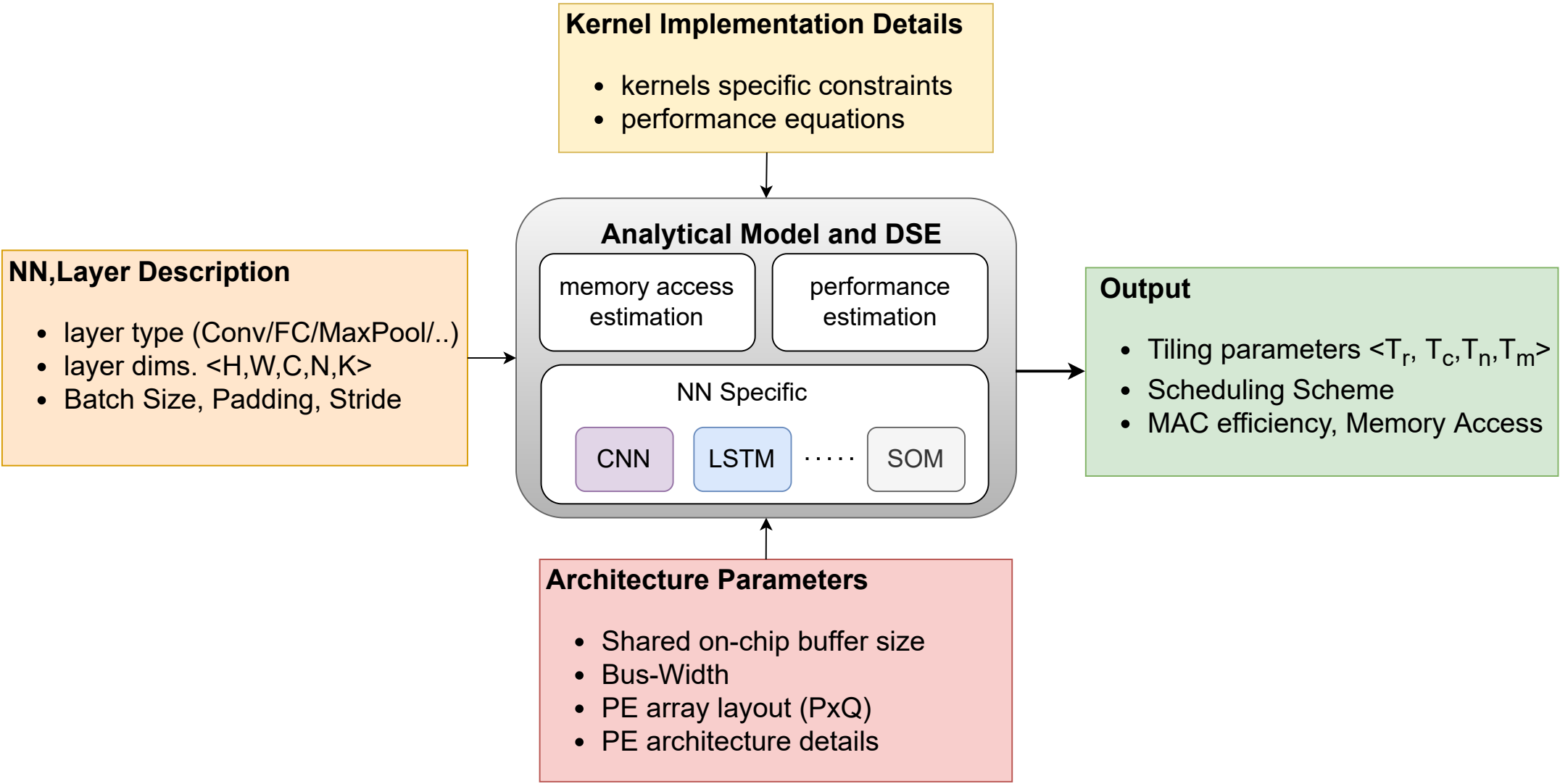
Kernel Implementation Details
kernels specific constraints
performance equations
NN,Layer Description
layer type (Conv/FC/MaxPool/..)
layer dims. <H,W,C,N,K>
Batch Size, Padding, Stride
Analytical Model and DSE
memory access estimation
performance estimation
NN Specific
CNN
LSTM
SOM
Output
Tiling parameters <Tr, Tc,Tn,Tm>
Scheduling Scheme
MAC efficiency, Memory Access
Architecture Parameters
Shared on-chip buffer size
Bus-Width
PE array layout (PxQ)
PE architecture details