Designed and implemented the function simulator in C++ for 32bit RISCV ISA instructions. Function simulator takes instruction encoding in .mc file as input. All the instructions in the input .mc file is executed as per the functional behavior of the instructions.

Along with execution of instruction stages, simulators also provide messages about what it is doing in each stage, Implements an additional instruction which exits the simulator, writes the data memory in .mc file before exiting.

Complete Project is divided in 4 different phases:-
Phase 1: Conversion of Assembly code to Machine code

Phase 2: Code for a 5 stage instruction execution.Each instruction must go through the following stages:

- Fetch
- Decode
- Execute
- Memory
- Writeback

Phase 3: Code for the pipeline version of Phase 2.

Phase 4: Appending a cache like memory module to Phase 3.

We tested the software using assembly programs of:

- Fibonacci Program
- Sum of the array of N elements. Initialize an array in the first loop with each element equal to its index. In the second loop find the sum of this array, and store the result at Arr[N].
- Factorial Program
- Bubble Sort Program

Link to the code:- https://github.com/saurav8683/RISC_V-Simulator