Indian Institute of Technology

Dept. of Electrical Engineering

EE-705: VLSI Design lab.

Assignment 7

Description of design:

Design a router using *synthesizable Verilog* to be used with network-on-chip (NoC) that is organized in an array of 4x4. A router consists of 4 routing ports (*N, S, E, W*) and a local port for the connected core. Keeping it a low cost router, it should use dimension order routing (DOR) so that it does not require to store routing table. Data is transferred as flit. It uses virtual channels (2 virtual channel per input) to prevent deadlock condition.

Flit Format:
The flit format is presented in Table 1 and 2. The 32-bit packet consists of a header flit followed by payload flits. Two additional 2-bit heads are type and (Identity ID) bits. The flit type can be as header (Header flit), message body, and the end of message body or the last flit of the message (Tail flit)

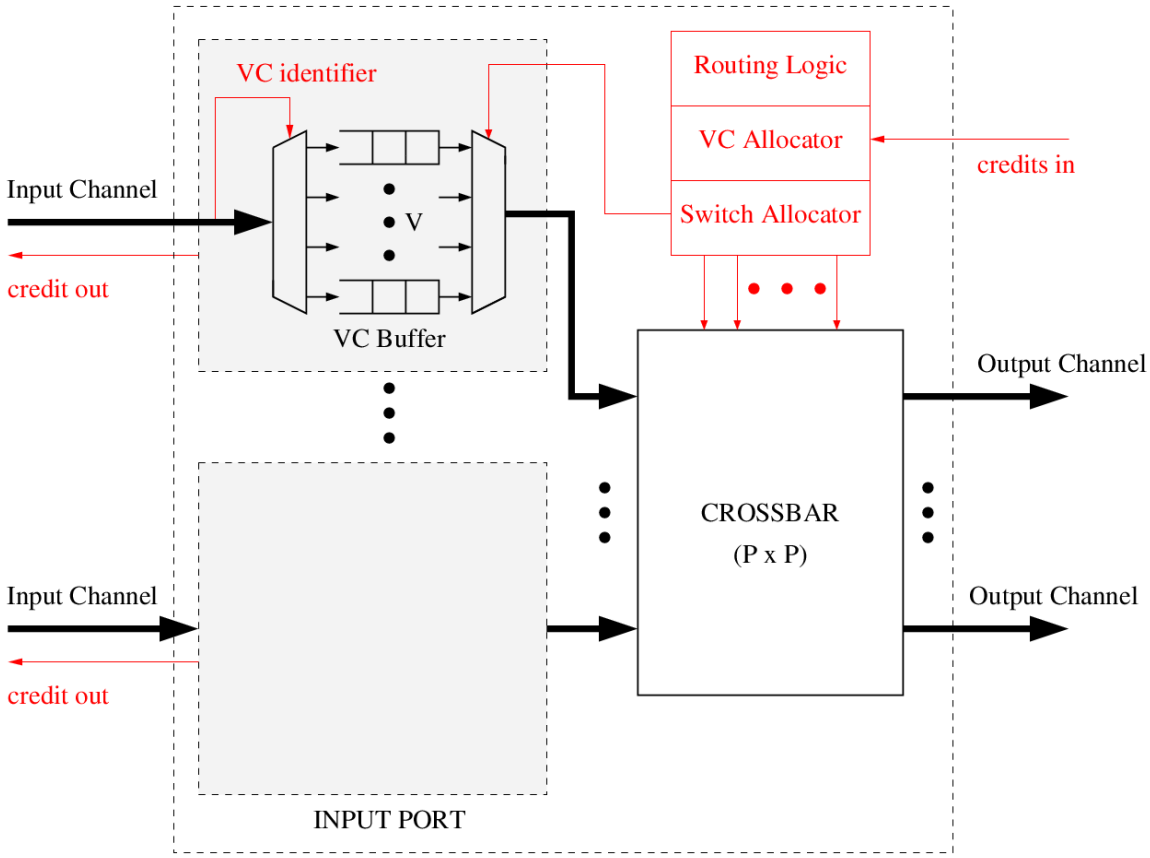
Table 1: Flit format

Type header (2 bits)	ID (2 bits)	Source X (2 bits)	Source Y (2 bits)	Dest. X (2 bits)	Dest. Y (2 bits)	Payload (20 bits)
Type header	ID	Payload (28 bits)				
. . . . .						
Type header	ID	Payload (28 bits)				

Table 2: Flit types

Type of flits	Binary (Decode) code
No flit	00 (0)
Header Flit	01 (1)
Message/Data body	10 (2)
Tail flit	11 (3)

ROUTER ARCHITECTURE



In order to control the flow every router sends a credit (availability of one flit space or not). Based on the credit it transfers the flit to the neighbour.