Indian Institute of Technology

Dept. of Electrical Engineering

EE-705: VLSI Design lab.

Assignment-6

Description of design:

We want to design a data compression circuit using run length encoding. It replaces continuously repeated occurrences of a byte by a repeat count and the byte value.

The circuit receives a fresh byte at every positive transition of an externally supplied clock. We shall use the ESC character (code = 1BH) to signal the use of a repeat count. Therefore, if the ESC character itself appears in the input stream, it has to be handled in a special way. The output is byte wide and every data byte being output is signaled by a rising transition on a *DataValid* line.

- If any character 'c' repeats n times in the input stream with n > 2, we output the three byte sequence ESC n c.
- If n ESC characters arrive contiguously in the input stream, we output the 3 byte sequence ESC n ESC, where n can be from 1 to 255.
- Otherwise, we just output the received characters without any change.
- if the repeat count is more than 255, we handle the first 255 characters as above and treat the 256th occurrence on wards as if a new character has been received.

Write a *synthesizable behavioural description* of the above circuit in **Verilog**.

The external system provides a 'fast clock' and a 'data clock' which is at ¼ the frequency of fast clock. Fresh data is input/output at rising edge of 'data clock'. Since the output data rate may be less or more than the data rate over short periods, provision must be made for buffering the data and providing a 'data valid'(*DataValid* line.) output which becomes 1 in a clock signal in which valid data is being output.

A single entity-architecture pair or module is to be described, in synthesizable behavioural style. No component instantiation is permitted. Standard Logic arithmetic libraries can be used and integer type signals are considered synthesizable. A clear block diagram must accompany the description in your report.