Assignment 2:

Submission Deadline: **January 31, 2016 (Sunday**) 11:55 pm

Description of design:

Design a greatest common divisor (GCD) which can compute the GCD of two 8 bit signed numbers (1 sign bit is included). Use two's complement format to represent negative numbers. Partition the design into control (state machine) and datapath (functional units, storage, and steering logic) part. Use VHDL for the describing and simulation of the design. Description of datapath and controller must be clearly shown. Also, write a test bench to verify your design.

The entity is described here

entity GCD **is**

port (reset, clk, start: in std_logic;

X, Y: in std_logic_vector (7 downto 0);

Z: out std_logic_vector (7 downto 0));

end GCD;

The machine will proceed computation on getting start input.