For the second part of the lab, we had to modify the already existing SRAM_BIST file that is associated with the exercise 2 file.

Through ModelSim, we were able to spectate the wave simulation which enabled us to read the first half of 256k locations in decreasing order from 1FFF to 0 on the SRAM. The other half of the 256k locations are in increasing order, from 2000 to 3FFF.

The multiple number cycles that were implemented in our code made it easier to have the code run successfully. Our first read cycle that was utilized began once the BIST_address decrementation ended (for the first address). For this cycle, we made sure that each one of the 256k SRAM locations had no other value. After the first cycle, the second one incremented by 1 from 131071 until 3FFF. After these cycles were completed, state delay3 starts. After state delay 3 ends, the fourth delay starts right after. The fourth delay state would check the final values for the data that was expected. Finally, the BIST_STATE would return the system to an idle state.