Introduction to Quartus/DE10-Lite Platform

Signature and Grading Sheet

Group #:_____ Name(s):_____ .

Grading

- Section 5.4(b): VHDL code design (20 points):_____.
  Attach VHDL code file.
- Section 5.4(c): Synthesized .vho file (10 points):_____.
  Attach .vho file
- Section 5.4(d): simulation timing waveform (20 points): _____.
  Attach the snapshot of simulation waveform (in a .jpeg file)
- Section 5.4(e): simulation timing waveform (20 points): _____.
  Attach the snapshot of simulation waveform (in a .jpeg file)
- VHDL code and .vho file format and comments (15 points):_____.
- Zip and internal file naming conventions (15 points):_____.
  Follow the instruction in the cover sheet.

Total points: .

Experiment

Introduction to Quartus/DE10-Lite Platform

1 Purpose

To learn the Intel/Altera Quartus Platform and DE10 lite prototyping broad

2 Reading

- Chapters 1 and 2 of *FPGA Prototyping by VHDL Examples 2nd edition.*

3 Software

- You can obtain Quartus Pro Lite edition (18.1 Release) free of charge software and install them in your own machine. The link is:
  http://fpgasoftware.intel.com/?edition=lite
  Make sure that Lite edition and 18.1 release are selected in the pulldown menu.
- (Optional) You may need to set up the USB-Blaster driver afterward and the procedure can be found in "Getting Started with DE Series Boards." The link is ftp://ftp.intel.com/Pub/fpgaup/pub/Intel_Material/17.0/Tutorials/Getting_Started_with_DE-series_boards.pdf

4 VHDL code format guideline

- The VHDL code (.vhd file):
  - Include the following header

```
-- ======================================
-- file_name:  my_file.vhd.
-- author: first_name last_name (CSU id)
-- ======================================
```

  - Follow the format (indents, white space etc.) in the example codes
  - Include adequate comments
- The post-synthesis code (.vho file):
  - Include the following header

```
-- ======================================
-- file_name:  my_file.vhd.
-- author: first_name last_name (CSU id)
-- ======================================
```

  - No need to comment or format
- Points will be deducted for not following the format guideline.

5 Design Procedure

5.1 Introduction to Quartus

Follow *Quartus Synthesis Tutorial* and get familiar with Quartus.
(Optional) Sections 4.4 and 4.5.

5.2 RT-level simulation

Follow Sections 1 – 4 of *ModelSim/Quartus Simulation Tutorial* and get familiar with the ModelSim RT-level simulation.

5.3 Post-synthesis simulation

Follow Section 5 of *ModelSim/Quartus Simulation Tutorial* and get familiar with the ModelSim post-synthesis simulation.

5.4 3-bit comparator

(a) Expand the 2-bit comparator into a 3-bit comparator. The entity declaration is

```
entity eq3 is
   port(
     a, b : in  std_logic_vector(2 downto 0);
     aeqb : out std_logic );
end eq3;
```

(b) Derive the VHDL using a 1-bit comparator. Relational operator is not allowed in this lab. The code should follow the format guideline in Section 4.

(c) Perform compiling (synthesis/placement and routing) and obtain the .vho file. Follow the format guideline in Section 4 to add a header to the file.

(d) Perform RT-level simulation with testbench eq3_tb.vhd. Use Windows "snip tool" to capture a snapshot of the simulation result, similar to that in Step 10 of Section 4.4.

(e) Perform Post-synthesis simulation with testbench eq3_tb.vhd. Use Windows "snip tool" to capture a snapshot of the simulation result, similar to that in Section 5.6. Since the waveform is the same as the RT-level simulation, the snapshot should include the expanded uut on the left panel. No point will be given if the uut unit is not expanded in the snapshot.