Approximate Nearest One Detector Design for an Improved Logarithmic Multiplier

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Logarithmic Multipliers

Logarithmic Multipliers

- Base-2 logarithmic multipliers use the shifting and additive properties of binary addition to compute the approximate product of two n-bit numbers
- Challenge is designing a multiplier that is both **accurate** and **hardware efficient**
- **Objective**: Approximating certain components (Nearest One Detector) to achieve better hardware performance

Mitchell Multipliers (MITCHELL) [1]

- Each number N can be written as the sum of the **leading power of two** and a difference factor x
- Uses an approximation for the base-2 representation of N using the sum of the exponent and the factor x

$$N = 2^k(1+x),\ 0 \le x < 1 \quad (1)$$

$$log_2 N \approx k + x \quad (2)$$

Improved Logarithmic Multipliers (ILM) [2], [3]

- Mitchell multipliers will always underestimate the final product
- To allow for double-sided error distribution, introduce over and underestimation depending on the number
- Each number N can be written as the sum of the **nearest power of two** and a difference factor depending on if the number is overestimated or underestimated
- Uses an approximation for the base-2 representation of N using the sum of the exponent and the factor

$$N = \begin{cases} 2^k(1+x),\ 0 \le x < 1 \\ 2^{k+1}(1-y),\ 0 < y \le 1 \end{cases} \quad (3)$$

$$log_2 N \approx \begin{cases} k+x,\ for\ N = 2^k(1+x) \\ k+1-y,\ for\ N = 2^{k+1}(1-y) \end{cases} \quad (4)$$

ILM Architecture

Improved Logarithmic Multiplier Architecture

$$A = 2^{k_1} + q_1 \qquad B = 2^{k_2} + q_2$$

$$A \times B \approx 2^{k_1+k_2} + 2^{k_1}q_2 + 2^{k_2}q_1 + q_1 q_2 \quad (5)$$

- Converts product into exponents of base 2 that can be calculated using binary arithmetic
- Last term is disregarded as approximation error
- Uses Nearest One Detector (NOD) to determine exponent values for arithmetic operations

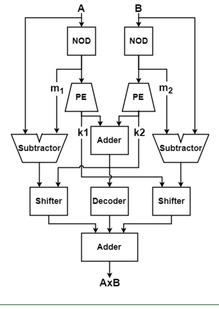


Figure 1. Improved Logarithmic Multiplier Design from [2]

8-bit Unsigned Nearest One Detector Designs

Exact Nearest One Detector (ENOD)

- Evaluates the nearest one and clears the rest of the bits to zero

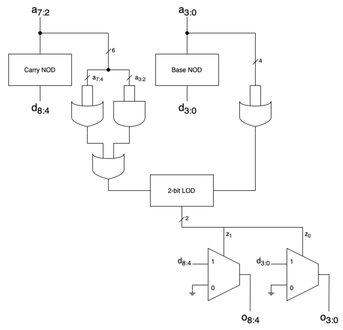


Figure 2. Exact Nearest One Detector

Approximate Nearest One Detector (ANOD)

- Uses only the Carry NOD slice and approximates the bottom four bits using a multiplexer
- Retains the NOD for values greater than 2^4

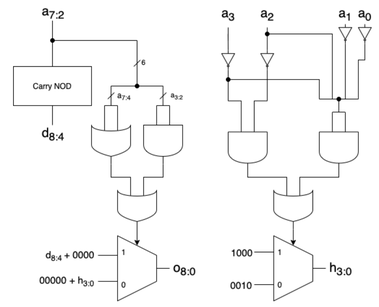
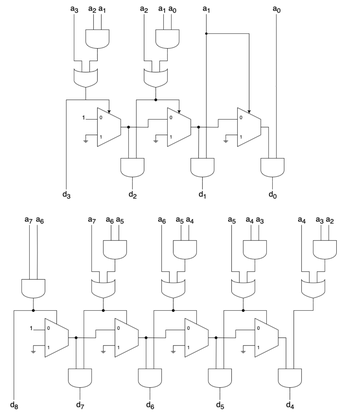


Figure 3. Approximate Nearest One Detector



Figures 4 & 5. Base NOD Slice (top) and Carry NOD Slice (bottom)

Results

Error Metrics

- Each logarithmic multiplier design was simulated using MATLAB for 2^8 test cases (0-255) each input
- ILM-ENOD uses the exact NOD, ILM-ANOD uses an approximate NOD with the ILM architecture
- Error Metrics used: absolute error, mean relative error distance, and normalized mean error distance

Table 1. Error Metrics for Logarithmic Multipliers

	AE	MRED	NRED
Mitchell	606.398	0.0376	0.0093
ILM-ENOD	**0.246**	**0.0284**	**0.0070**
ILM-ANOD	0.250	0.0310	0.0070

Hardware Metrics

- Each design was implemented on using Verilog HDL on 45 nm process technology and synthesized with Synopsys Design Compiler
- 1 V supply voltage and 250 MHz clock

Table 2. Hardware Metrics for Logarithmic Multipliers

	Area (μm^2)	Power (μW)	Delay (nS)	PDP (fJ)
Mitchell	**600.5**	**26.2**	**3.71**	**97.20**
ILM-ENOD	1252.5	28.4	3.84	109.1
ILM-ANOD	1166.2	29.2	3.86	112.7

Table 3. Hardware Metrics for Nearest One Detectors

	Area (μm^2)	Power (μW)	Delay (ns)	PDP (fJ)
ILM-ENOD	230.9	**1.31**	**0.43**	**0.563**
ILM-ANOD	**191.5**	1.32	0.53	0.700

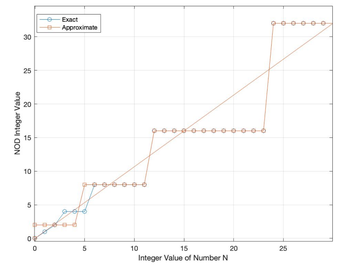
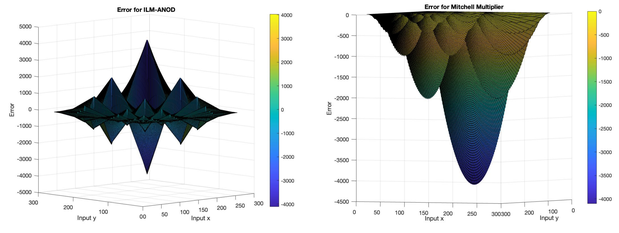
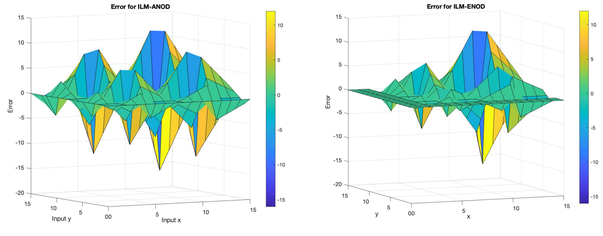


Figure 6. Exact vs. Approximate Nearest One Detector Values (Range 0-32)



Figures 7 & 8. Error Comparison for Improved Logarithmic Model and Mitchell Multiplier (Range 0-255)



Figures 9 & 10. Error Comparison for Improved Logarithmic Multipliers Implementing Approximate NOD and Exact NOD (Range 0-15)

Error-Hardware Results

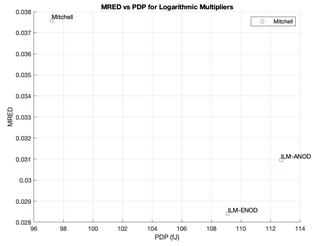


Figure 11. Mean Relative Error vs. Power Delay Product of Logarithmic Multipliers

Table 4. PDP x MRED for Logarithmic Multipliers

	PDP (fJ)	MRED	PDP x MRED
Mitchell	**97.20**	0.0376	3.653
ILM-ENOD	109.1	**0.0284**	**3.097**
ILM-ANOD	112.7	0.0310	3.489

Conclusion

- Exact and Approximate ILM were **27.9% and 19.2% more accurate** than the Mitchell multiplier
- Both ILM's performed slightly worse than the Mitchell in PDP metrics, **requires around twice as much area**
  - Due to more computationally extensive signed operations within the ILM model
- Approximate ILM had the worst PDP performance, however had **7.14% less area** than the exact counterpart
- ENOD performed 21.7% better than ANOD in power and delay, **ANOD had 18.7% less area**
- Both ILM's had a lower PDPxMRED than MITCHELL, with the **ILM-ENOD performing 11.9% better than ILM-ANOD**
- **ILM-ENOD is the best model in terms of error-hardware efficiency, however ILM-ANOD uses less area and works as a similar performing alternative**

References

[1] J. N. Mitchell, "Computer Multiplication and Division Using Binary Logarithms," in IRE Transactions on Electronic Computers, vol. EC-11, no. 4, pp. 512-517, Aug. 1962, doi: 10.1109/TEC.1962.5219391.
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[3] M. S. Ansari, B. F. Cockburn and J. Han, "An Improved Logarithmic Multiplier for Energy-Efficient Neural Computing," in IEEE Transactions on Computers, vol. 70, no. 4, pp. 614-625, 1 April 2021, doi: 10.1109/TC.2020.2992113.
[4] S. Gandhi, M. S. Ansari, B. F. Cockburn and J. Han, "Approximate Leading One Detector Design for a Hardware-Efficient Mitchell Multiplier," 2019 IEEE Canadian Conference of Electrical and Computer Engineering (CCECE), Edmonton, AB, Canada, 2019, pp. 1-4, doi: 10.1109/CCECE.2019.8861800.
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[6] T. Zhang, Z. Niu and J. Han, "A Brief Review of Logarithmic Multiplier Designs," 2022 IEEE 23rd Latin American Test Symposium (LATS), Montevideo, Uruguay, 2022, pp. 1-4, doi: 10.1109/LATS57337.2022.9936921.

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