1. Description

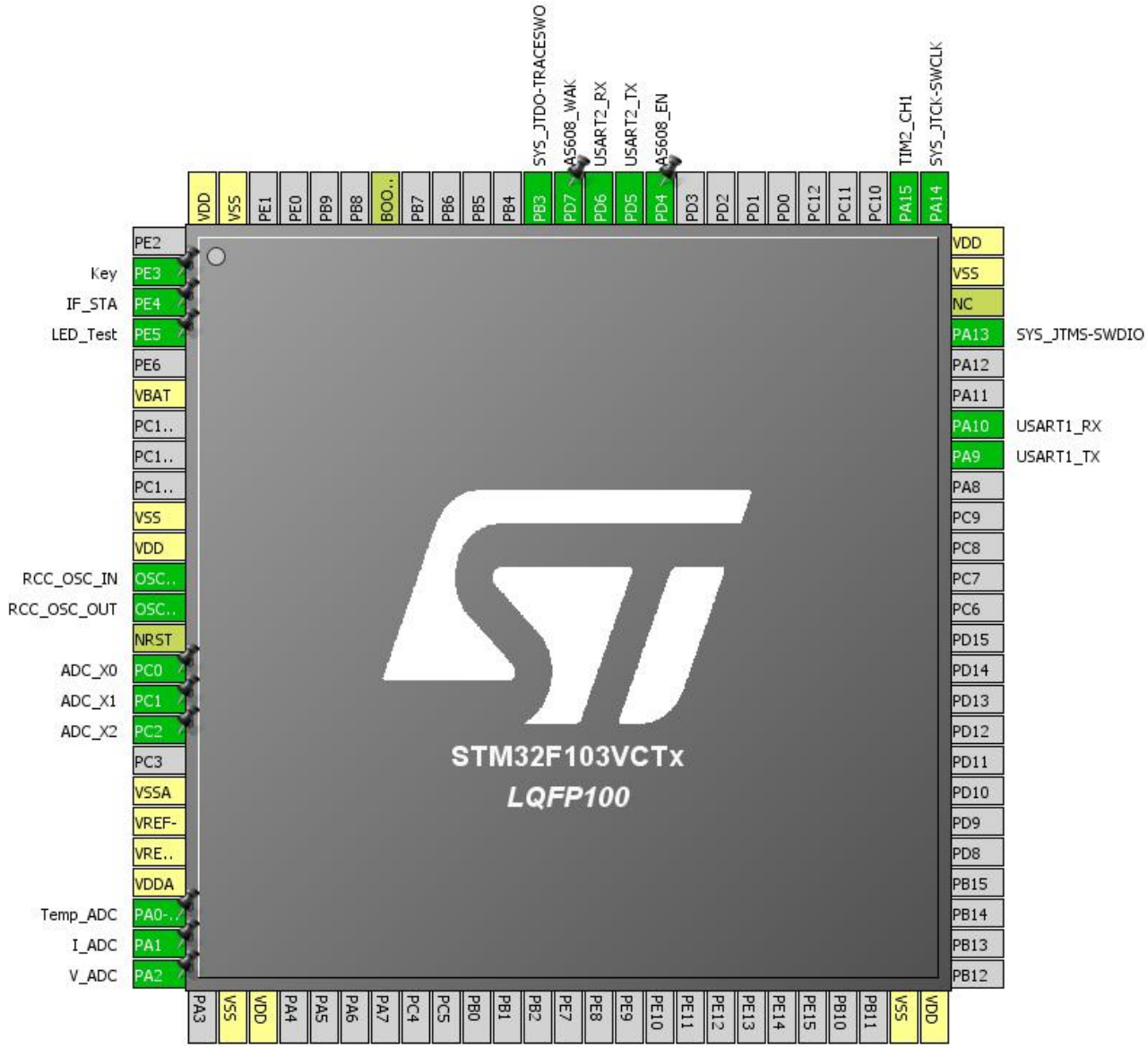
1.1. Project

Project Name	CPS-Slaver
Board Name	CPS-Slaver
Generated with:	STM32CubeMX 4.18.0
Date	03/14/2017

1.2. MCU

MCU Series	STM32F1
MCU Line	STM32F103
MCU name	STM32F103VCTx
MCU Package	LQFP100
MCU Pin number	100

2. Pinout Configuration



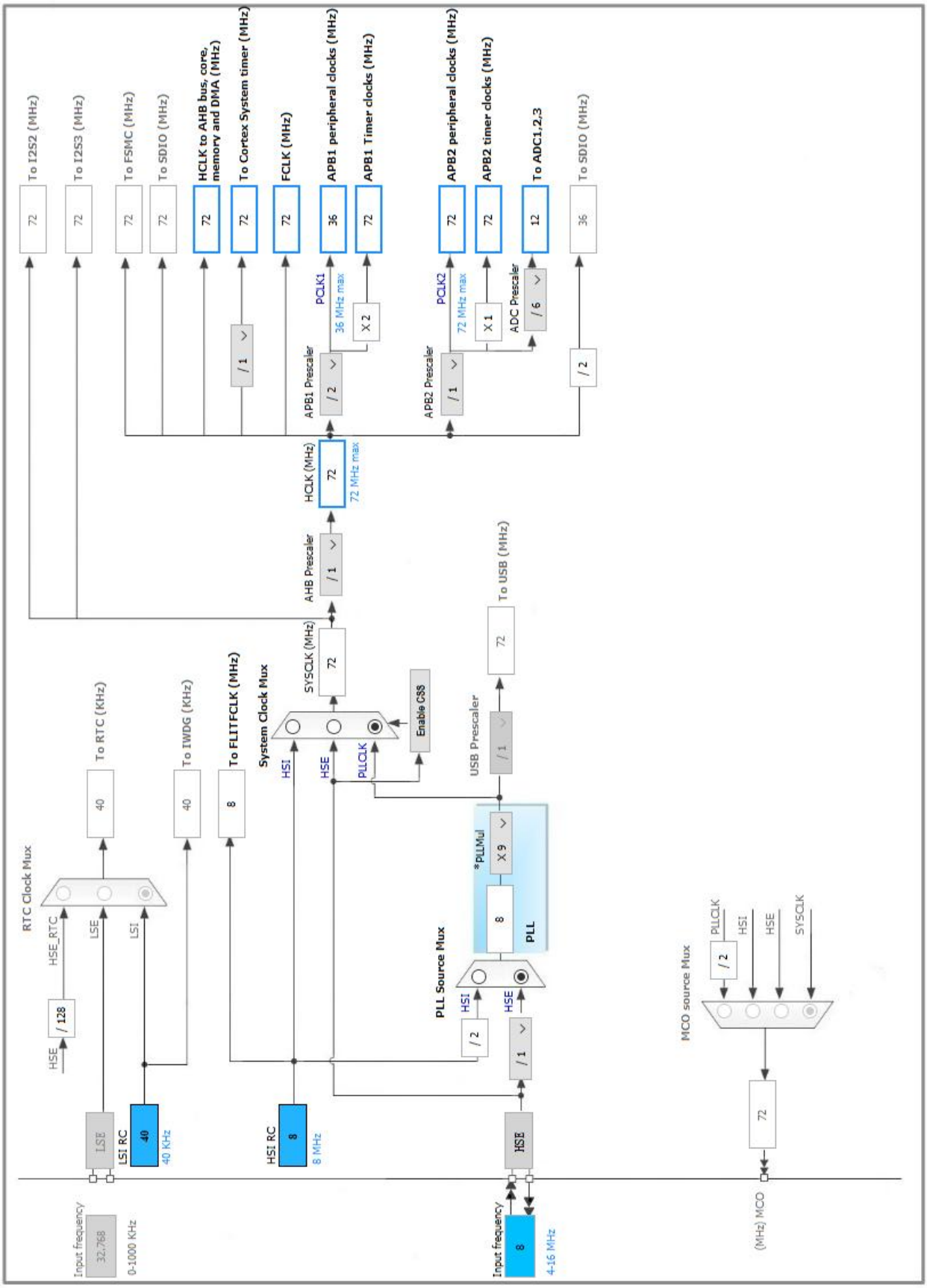
3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
2	PE3 *	I/O	GPIO_Input	Key
3	PE4 *	I/O	GPIO_Input	IF_STA
4	PE5 *	I/O	GPIO_Output	LED_Test
6	VBAT	Power		
10	VSS	Power		
11	VDD	Power		
12	OSC_IN	I/O	RCC_OSC_IN	
13	OSC_OUT	I/O	RCC_OSC_OUT	
14	NRST	Reset		
15	PC0 *	I/O	GPIO_Output	ADC_X0
16	PC1 *	I/O	GPIO_Output	ADC_X1
17	PC2 *	I/O	GPIO_Output	ADC_X2
19	VSSA	Power		
20	VREF-	Power		
21	VREF+	Power		
22	VDDA	Power		
23	PA0-WKUP	I/O	ADC1_IN0	Temp_ADC
24	PA1	I/O	ADC2_IN1	I_ADC
25	PA2	I/O	ADC3_IN2	V_ADC
27	VSS	Power		
28	VDD	Power		
49	VSS	Power		
50	VDD	Power		
68	PA9	I/O	USART1_TX	
69	PA10	I/O	USART1_RX	
72	PA13	I/O	SYS_JTMS-SWDIO	
73	NC	NC		
74	VSS	Power		
75	VDD	Power		
76	PA14	I/O	SYS_JTCK-SWCLK	
77	PA15	I/O	TIM2_CH1	
85	PD4 *	I/O	GPIO_Output	AS608_EN
86	PD5	I/O	USART2_TX	
87	PD6	I/O	USART2_RX	
88	PD7 *	I/O	GPIO_Output	AS608_WAK
89	PB3	I/O	SYS_JTDO-TRACESWO	

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
94	BOOT0	Boot		
99	VSS	Power		
100	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

mode: IN0

5.1.1. Parameter Settings:

ADCs_Common_Settings:	
Mode	Independent mode
ADC_Settings:	
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
ADC_Regular_ConversionMode:	
Enable Regular Conversions	Enable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
Rank	1
Channel	Channel 0
Sampling Time	**71.5 Cycles ***
ADC_Injected_ConversionMode:	
Number Of Conversions	0
WatchDog:	
Enable Analog WatchDog Mode	false

5.2. ADC2

mode: IN1

5.2.1. Parameter Settings:

ADCs_Common_Settings:	
Mode	Independent mode
ADC_Settings:	
Data Alignment	Right alignment
Scan Conversion Mode	Disabled

Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
Rank	1
Channel	Channel 1
Sampling Time	**71.5 Cycles ***

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.3. ADC3

mode: IN2

5.3.1. Parameter Settings:

ADC_Settings:

Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
Rank	1
Channel	Channel 2
Sampling Time	**71.5 Cycles ***

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.4. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

5.4.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

5.5. SYS

Debug: Trace Asynchronous Sw

Timebase Source: TIM7

5.6. TIM2

Slave Mode: Reset Mode

Trigger Source: ITR0

Clock Source : Internal Clock

Channel1: PWM Generation CH1

5.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**17 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**999 ***
Internal Clock Division (CKD)	No Division
Slave Mode Controller	Reset Mode

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	**100 ***
Fast Mode	Disable
CH Polarity	High

5.7. TIM6

mode: Activated

5.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**71 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**9 ***

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

5.8. USART1

Mode: Asynchronous

5.8.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

5.9. USART2

Mode: Asynchronous

5.9.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

5.10. FREERTOS

mode: Enabled

5.10.1. Config parameters:

Versions:

CMSIS-RTOS version	1.02
FreeRTOS version	8.2.3

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	7
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Disabled
USE_COUNTING_SEMAPHORES	Disabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
TOTAL_HEAP_SIZE	**13072 ***
Memory Management scheme	heap_4
USE_ALTERNATIVE_API	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Disabled
USE_TICKLESS_IDLE	Disabled

USE_TASK_NOTIFICATIONS	Enabled

Hook function related definitions:

USE_IDLE_HOOK	**Enabled ***
USE_TICK_HOOK	**Enabled ***
USE_MALLOC_FAILED_HOOK	**Enabled ***
CHECK_FOR_STACK_OVERFLOW	**Option1 ***

Run time and task stats gathering related definitions:

USE_TRACE_FACILITY	Enabled
GENERATE_RUN_TIME_STATS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Disabled
TIMER_TASK_PRIORITY	2
TIMER_QUEUE_LENGTH	10
TIMER_TASK_STACK_DEPTH	256

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

5.10.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Disabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Disabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Disabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Disabled
xEventGroupSetBitFromISR	Disabled

xTimerPendFunctionCall	Disabled

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0-WKUP	ADC1_IN0	Analog mode	n/a	n/a	Temp_ADC
ADC2	PA1	ADC2_IN1	Analog mode	n/a	n/a	I_ADC
ADC3	PA2	ADC3_IN2	Analog mode	n/a	n/a	V_ADC
RCC	OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
	PB3	SYS_JTDO-TRACESWO	n/a	n/a	n/a	
TIM2	PA15	TIM2_CH1	Alternate Function Push Pull	n/a	Low	
USART1	PA9	USART1_TX	Alternate Function Push Pull	n/a	**High ***	
	PA10	USART1_RX	Input mode	No pull-up and no pull-down	**n/a**	
USART2	PD5	USART2_TX	Alternate Function Push Pull	n/a	**High ***	
	PD6	USART2_RX	Input mode	No pull-up and no pull-down	**n/a**	
GPIO	PE3	GPIO_Input	Input mode	**Pull-up ***	n/a	Key
	PE4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	IF_STA
	PE5	GPIO_Output	Output Push Pull	n/a	Low	LED_Test
	PC0	GPIO_Output	Output Push Pull	n/a	Low	ADC_X0
	PC1	GPIO_Output	Output Push Pull	n/a	Low	ADC_X1
	PC2	GPIO_Output	Output Push Pull	n/a	Low	ADC_X2
	PD4	GPIO_Output	Output Push Pull	n/a	Low	AS608_EN
	PD7	GPIO_Output	Output Push Pull	n/a	Low	AS608_WAK

6.2. DMA configuration

DMA request	Stream	Direction	Priority
USART1_TX	DMA1_Channel4	Memory To Peripheral	Low
USART2_RX	DMA1_Channel6	Peripheral To Memory	Low

USART1_TX: DMA1_Channel4 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART2_RX: DMA1_Channel6 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
DMA1 channel4 global interrupt	true	5	0
DMA1 channel6 global interrupt	true	5	0
USART1 global interrupt	true	5	0
TIM6 global interrupt	true	0	0
TIM7 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 global interrupts	unused		
TIM2 global interrupt	unused		
USART2 global interrupt	unused		
ADC3 global interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F1
Line	STM32F103
MCU	STM32F103VCTx
Datasheet	14611_Rev12

7.2. Parameter Selection

Temperature	25
Vdd	3.3

8. Software Project

8.1. Project Settings

Name	Value
Project Name	CPS-Slaver
Project Folder	C:\Users\Saven\Desktop\CPS\CPS-Slaver
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_F1 V1.4.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Add necessary library files as reference in the toolchain project configuration file
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	Yes