# An FPGA Run-Time System for Dynamical On-Demand Reconfiguration

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## Abstract

*The handling of an increasing number of automotive comfort functionalities has become a significant problem for the most automobile manufacturers since communication, power consumption, available space and cost become important issues for a growing number of engine control units. Our contribution presents a first approach for a flexible versatile FPGA-based run-time system supporting a resource saving function multiplex.*

**Keywords:** ECUs, FPGA, PRTR, run-time system

## 1. Introduction

During the last 30 years the deployment of electronics and control driven hardware in the automotive domain has significantly increased. Today many automobile manufacturers complain about the handling of the increasing number of control units and the growing costs of development, production and maintenance (e.g. storage of spare parts etc.). As the number of control units and services desired by customers increases, electrical power dissipation will grow to keep all devices working. Until the year 2010 annual growth rate of electronic automotive control devices will be more than 10% and the prorated cost of electronics assembled in production will increase by 40% in total [18].

The sector of control devices was dominated by microcontrollers and ASICs so that every function was implemented by a dedicated control unit. Today upper class automobiles contain up to 100 control units and even in inactive mode their total power consumption may discharge the battery which can result in a disabled automobile. Additionally the devices become sooner obsolete and the product life cycle decreased from 5 years down to 2 years [18].

Reconfigurable logic has been used for development and rapid prototyping purposes whereas their deployment in the final product has been avoided because of their higher component costs compared to off-the-shelf standard ASICs. Nevertheless some automobile manufacturers have discovered the advantages of reconfigurable devices since their high flexibility and adaptivity will increase the products life cycle and reduce costs and risks for development and maintenance later on.

Companies like Xilinx [24] and Altera [1] have reacted on that and extended their product palette for low power and low cost FPGAs which can be used as flexible ASIC replacements. Despite of this step towards reconfigurable hardware their possibilities and potentials are not exploited in the automotive domain. Although low-cost FPGAs can also be reconfigured at run-time they don't currently support partial run-time reconfiguration like state-of-the-art FPGAs (e.g. Xilinx Virtex II series [24]). These features might make such new FPGAs attractive for embedded systems because they enable for hardware-based task switching and there exist different academic approaches wherein they try to exploit these novel features [3][4][6][7][16][19]. Virtex FPGAs may look oversized but it would be conceivable to do a trade-off on cost, size and power consumption to apply them in dynamic embedded automotive systems.

Hardware-based task switching enables for a dynamic function multiplex at run-time where hardware mapped function-blocks can be placed at run-time on different (on-chip / off-chip) execution locations [13][14]. Run-time task management is not a trivial job so that many approaches adopted solutions from operating system theory [10][12][15][20]. Some researchers implemented complex operating systems by adapting LINUX-based system kernels to their needs so that their systems can do a migration of software-based tasks to hardware and vice versa [21][22]. Additionally they had to solve the HW/HW – HW/SW inter-task communications issue, so they added complex resource demanding network-on-chip (NoC) structures like packet-based 2D-torus rings containing routers and reconfigurable processing blocks [21]. The approaches described above result in complex hardware/software systems from which we believe that they are less suitable for compact automotive and other embedded target applications. This paper presents an approach for a MicroBlaze soft-core processor based run-





0-7695-2132-0/04/$17.00 (C) 2004 IEEE

time system on Xilinx Virtex II FPGAs targeting embedded automotive cabin functions (e.g. seat control, window lift) supporting resource saving hardware function-multiplex. In the following we give a short description on the basic hardware architecture supporting run-time reconfiguration, bitstream decompression & placement and on-chip/peripheral communication. Later we will describe the structure of our proposed run-time system and some first implementation results concerning its resource consumption. The paper closes with our conclusions and a preview on our future work to be done.

## 2. Target Hardware Architecture

The target hardware architecture which is used for the first implementation of a run-time system software, combined with a partially dynamically reconfigurable structure, is mapped on a Xilinx XC2V3000 FPGA. As shown in figure 1 the function modules are separated in slots and are connected to a bus structure. Function (A) is located in the first slot whereas other functions can be positioned in further three slots on the right side (not shown in figure 1). The physical separation between the single functions was realized by a bus macro, which connects the signal lines between the functional blocks and the arbitration/ run-time-system module. More details about the bus-macro approach can be found in [9].

The configuration data consists of a selected subset of compressed automotive control functions which are stored in external Flash-memory. A module which connects the Flash-memory via a decompressor unit to the FPGA's internal reconfiguration interface ICAP [3][4][24] (internal configuration access port) controls the dynamic and partial reconfiguration. On demand partial reconfiguration data is transferred via the ICAP interface into the FPGA's reconfiguration memory. Using a low latency pipelined LZSS- decompressor saves valuable memory resources and reduces costs [8][2][25]. After a successful partial reconfiguration dedicated signal lines give feedback to the run-time system which makes the new function available to the environment. See also figure 2 which shows a global view of the complete system; including ICAP- module, LZSS- decompressor unit, Microblaze running the run-time system software, internal on-chip module bus and function slots.

The run-time system itself is implemented as software on a Xilinx MicroBlaze soft-core processor [24]. Designed with Xilinx Embedded Development Kit (EDK) the run-time system is connected via the on-chip peripheral bus to peripheral functions like the decompressor module and the arbiter. This core handles the incoming and outgoing messages of the complete system. Messages from peripheral devices will be decoded, processed and sent to the bus arbiter which controls the on-chip-bus-lines connecting the currently available functions (see figure 1). Messages from the function-modules will be received by the arbiter and redirected to the external devices. The implemented structure is also capable of saving states and all necessary parameters if a function-module has to be substituted by another. This context-save mechanism is administrated by the run-time system but the data is transmitted via the bus lines and controlled by the arbiter. Further details on our target hardware architecture will be presented in a different publication which is in preparation.

The next section describes the basic functions of the run-time system, the approach for a function request management and the decision strategy of module substitution.

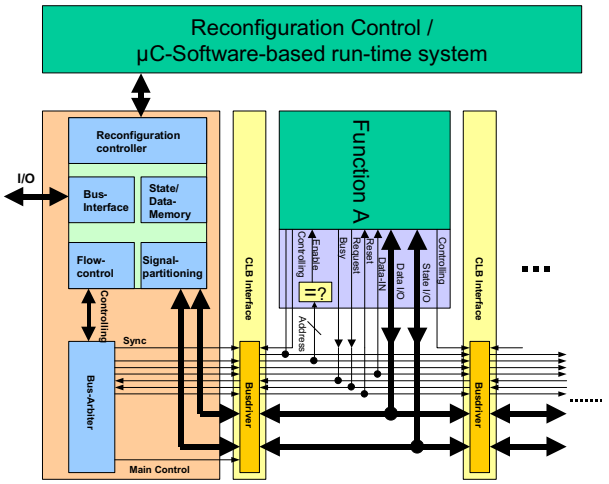


**Figure 1. Run-time system with FPGA partial run-time reconfiguration support and soft-processor**

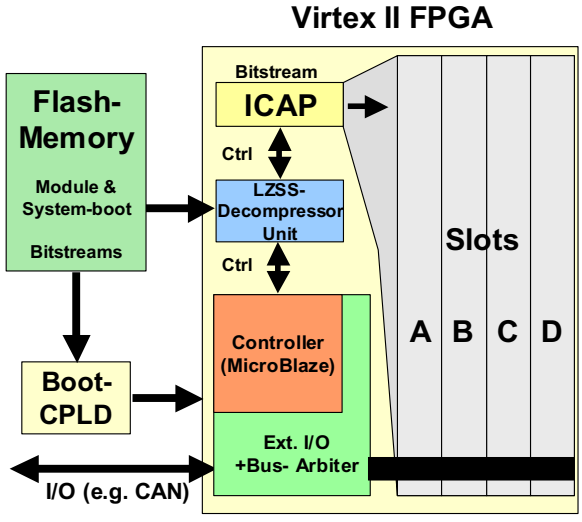


**Figure 2. Connection to external memory**





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## 3. Run-Time System

### 3.1. Requirements for the Run-Time System

The run-time system handles messages with time constraints like user requests for services or sensor monitoring messages of engine movements. Thus the run-time system has to be able to fulfill real-time constraints.

The system should also be reusable for different scenarios and other fields of application like domestic area (e.g. windows, lights, heating). To take into account the different sizes of function-modules and FPGA types the run-time system must be scalable for a changing number of function-modules and FPGA-slots (FPGA sizes).

### 3.2. Basic Tasks of the Run-Time System

It is the run-time system's basic job to handle the communication of the function-modules with the corresponding sensors and actuator components by translating and forwarding the messages. It is relevant to preserve the order of incoming and outgoing messages for every function-module. Furthermore the run-time system manages and controls the reconfiguration process of the function-modules and in this context it performs a resource management on the FPGA as well. The run-time system also stores the state information of the available function-modules which are currently inactive and not physically available on FPGA.

### 3.3. Basic Structure

The run-time system consists of four major parts:

- Reconfiguration process: It saves the state information of the depending function-module, reconfigures the FPGA's module slots and reloads the state information of the new module.
- Management of the incoming messages: It receives the incoming messages, translates them into an internal message representation and forwards them to the function-modules.
- Management of the outgoing messages: It receives the messages from the modules, translates them into external messages and transmits them to the external environment.
- Message-buffer management unit: It stores and forwards messages which could not be delivered to their destination function-module units after these have been deactivated and removed by reconfiguration.

As shown in figure 4 these parts are executed in a pseudo parallel way by defined task switches between the software parts to guarantee a fast message handling. Additionally there exists an interrupt handling, which receives and buffers all incoming external messages for the run-time system, so that it may handle them later when ready.

3.3.1. **Administrative Data Structures.** The administration of FPGA-slots and handling of incoming messages will be done by using tabular data structures.

The message-module tables are needed for assigning the messages to the corresponding function-modules and for translating them into internal bus-messages. There exist two tables where the first one keeps informations about individual dedicated messages for modules and the second one keeps handling informations on common/public messages which can involve different function-modules who need input from the same external source(s).

The function-module table stores the state information of the inactive function-modules, the start- and end-addresses of the function's bitstream Flash-memory location and further module-specific informations, like the previously sent message. The slot table is a further data structure, which stores information about the currently allocated slots and its history which can be evaluated for slot selection/reconfiguration purposes.

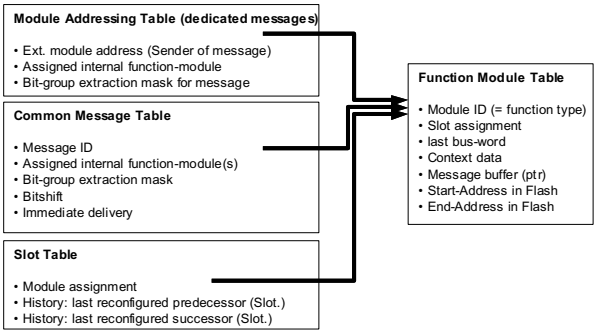


**Figure 3. Structure of administrative tables**

Beside these tables there exist several buffers for the communication's management between the run-time system's main parts and for buffering messages and demands of modules. Additional buffers are needed for the interrupt service routines, which store incoming messages for the run-time system arriving from the external Controller Area Network (CAN) -bus. To do an efficient buffer management the buffers are implemented as concatenated dynamic lists of message elements which can be moved/ removed logically to/from a list of concatenated free elements without much effort.

The following subsections describe the run-time system's basic structures in detail.




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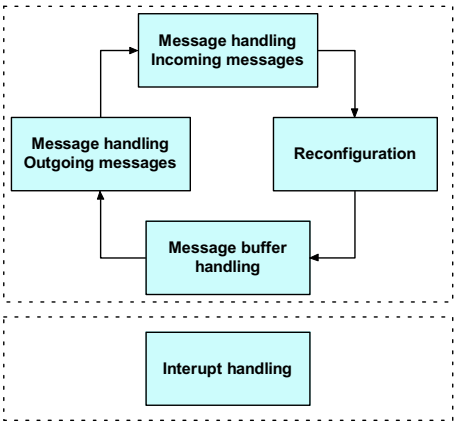


**Figure 4. Major parts of the RTS**

3.3.2. **Message Handling / Management Unit.** This unit handles incoming messages from the external CAN-bus and forwards them to the internal on-chip module bus.

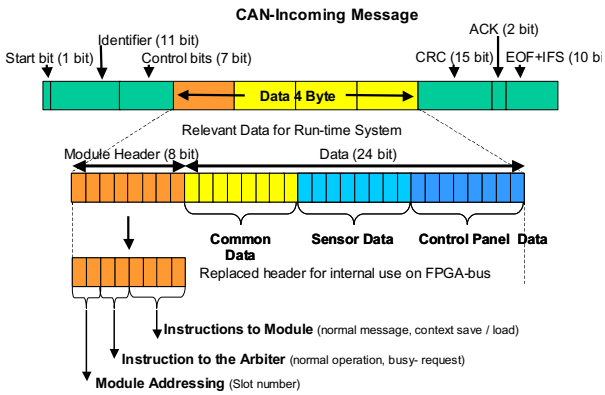


**Figure 5. CAN- Message structure and internal data representation**

As shown in figure 5 the incoming CAN-bus message contains 4 bytes of data which represent the relevant informations on module destination and module data input patterns. After its receipt, the data block is extracted and depending on its first identifier byte (module header) it will be decided how to treat the subsequent three message bytes.

Incoming messages are differed in individual messages designated for only one function-module and in common (broadcast) messages, which are relevant for multiple function-modules. The run-time system identifies the incoming message as individual or common. Depending on its type the header byte is modified, so that it can be used as message header on the internal on-chip FPGA bus. Individual messages are directly forwarded to the corresponding module after having been furnished with the internal function-module slot address if the function-module is active and physically available in the designated FPGA-slot (shown in figure 7). If the function-module is not active in the FPGA, the message is buffered into a module specific message-buffer and, if it is the first buffered message for this module, the reconfiguration unit will be requested for reconfiguration of the desired function-module. If there are already messages in the buffer, then reconfiguration was already requested when the first message was added to the buffer.

Common messages have to be looked up in the message-module table (see figure 3). The message has to be split up and translated in several messages for every module (see figure 7). Then these messages will be handled like individual messages.

The request for reconfiguration is sent to the reconfiguration task by writing it into the module-reconfiguration- request- buffer. After the reconfiguration request has been forwarded the management unit is ready to handle the next message from CAN. In some cases not every message has to be forwarded directly to the function even when the function is inactive and not physically available on FPGA. One case may be that the message is only essential for active function-modules because it does not cause any reaction besides deactivating a module, a reaction of an inactive function module is not expected.

So the message can be postponed and it suffices to ensure, that the function-module will receive the information about the change of essential conditions by changing its last internal bus message, which is stored in the function-module table (figure 3). The information will arrive at its destination function-module after its next reconfiguration. In this way needless reconfigurations and traffic on the FPGA-bus can be avoided. Messages which have to be directly forwarded are treated like individual messages.

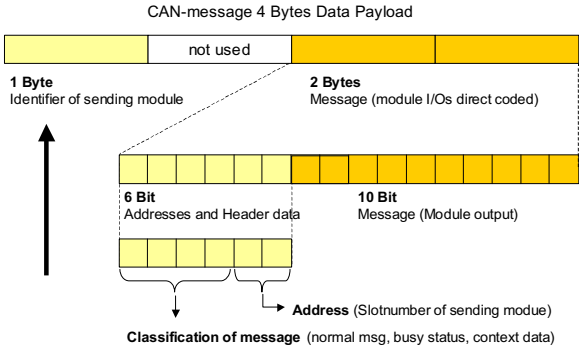


**Figure 6. Outgoing CAN messages- data payload scheme.**

If a function- module changes its local output these informations have to be forwarded to the external recipients (e.g. actuator components, other control units). An output of 10 signal bits is assumed (to give a reason





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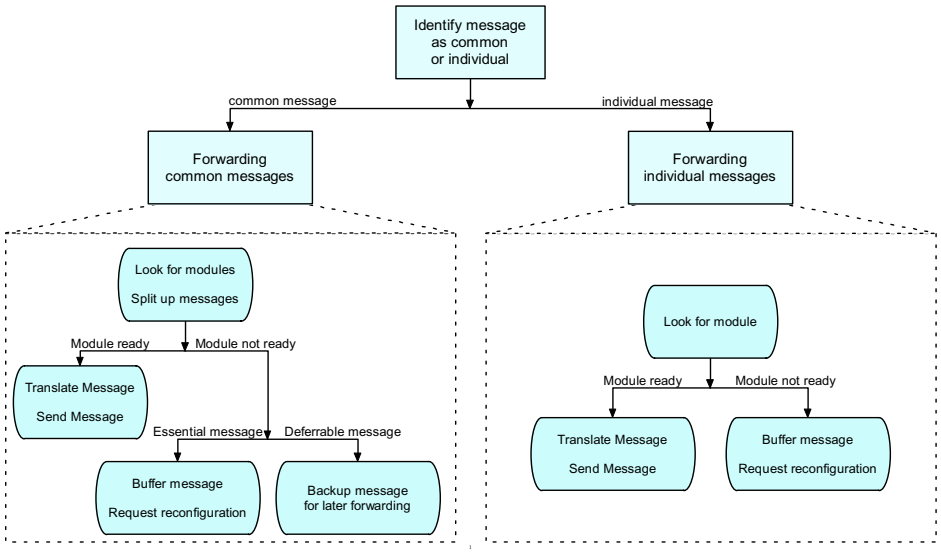


**Figure 7. Handling of common / individual messages**

the implemented modules like window lift, seat control etc. don't need more than 10 logic signal output lines each). Depending on its module ID which is stored in the slot allocation table the run-time system can decide from the transmitted slot number which recipients have to receive the module's output bit vector.

So an identifier byte is generated and added to the output vector (see figure 6) which is send as 4 byte data payload to the CAN- interface for transmission to the external CAN-bus.

3.3.3. **Reconfiguration Unit.** The reconfiguration unit controls the reload process of requested functions into the FPGA. As shown in figure 8 the reconfiguration is executed in four steps. Between these steps the run-time system is waiting for input from other modules like bus arbiter or ICAP-module or it may perform extended tasks which may be defined at a later stage of development.

If there is a request for a function-module, the reconfiguration unit looks for a free slot on the FPGA. If there is none available, it sends a message to the bus arbiter for verifying, which module is currently in inactive state and can be replaced. The run-time system chooses one of the inactive modules to replace it. The module's entry is removed from the slot table, so that no further messages will be forwarded while reconfiguration.

It should be mentioned that the run-time system's module replacement/ scheduling mechanism is event driven, depending on incoming messages from external peripheral devices. It is not possible to remove a function module from its slot until it has not left its busy state. Otherwise such a hard context switch could cause serious malfunctions, especially if momentarily moving actuator components are controlled which could cause injuries otherwise (e.g. blocking car window). So for further future extensions it would be conceivable to implement an advanced priority controlled mechanism for the preemptive task/context-switch.

It is evident that critical functions which always have to be active are not candidates fur such a function multiplex system. Additionally one should check the functions for their importance and degree of utilization, so that less critical functions can be selected for implementation on the described system.

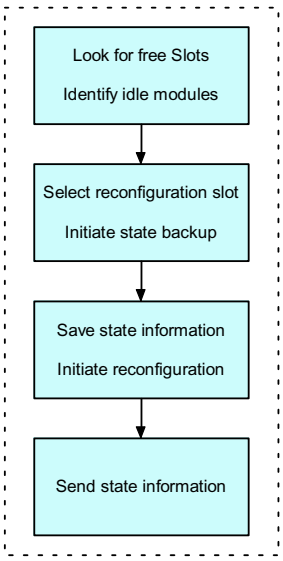


**Figure 8. Reconfiguration unit control steps**

In contrast to other approaches [5] [11] [17] where the function's state information is laboriously extracted by filtering the function's bitstream for relevant information which was previously read back from FPGA by using the Java JBits API [5], in our approach the function-module is





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prompted for sending the actual state information to the run-time system, which then stores the state information for re-initialization at a later point of time. So here a read back of the module's whole bitstream is not necessary.

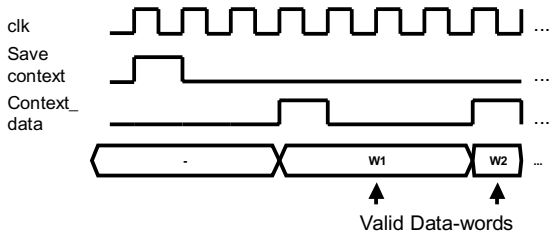


**Figure 9. Module context data save**

Figure 9 gives an example how the function module context data is saved. Dedicated bus-signals enable the module for storing its context which consists of a fixed number of 20 times 10 bit context words. Each new word is transmitted at the rising edge of the signal *context_data*, as shown in figure 9. Figure 10 shows how context data is restored on the reloaded module.

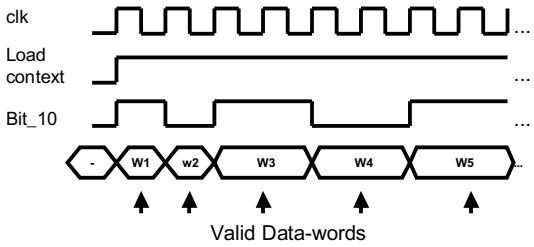


**Figure 10. Module context data restore**

After the receipt of the old function's state information the reconfiguration unit sends the start-address and end-address to the Virtex-ICAP module, which loads the new reconfiguration bitstream into the FPGA. The ICAP module reports a done signal when the reconfiguration succeeded. Before context data is restored, the last valid module's input pattern must be send from the module-administration table via the on-chip bus to the local module input. The loaded module won't start at this moment until it has received its context data, so that context and input correlate and accidental state transitions inside the module are prevented. For synchronization purposes the bus signal *Bit_10* must alternate its state (see also figure 10). After finish of transmission the function-module can continue working from the point before it was removed last time and is ready to accept new messages.

The reconfiguration process is completed by enlisting the information on the new reconfigured module into the slot table.

3.3.4. **Message Buffer Management Unit.** The main task of the message buffer management unit is to forward the stored messages to the reconfigured function-modules, which arrived while the recipient module was not physically available.

This unit looks for messages in all function-module message buffers for being sent to active function modules each cycle. The first buffered message in each function-module's buffer is forwarded to its destination, so it is assured that every module is served with its messages and there is enough time for the modules for changing their internal states until the next message arrives/will be served (see figure 11).

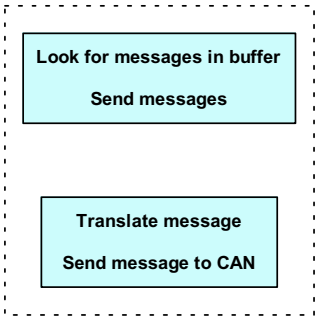


**Figure 11. Message buffer management and message translation tasks**

3.3.5. **Management of Outgoing Messages**. The management unit which handles the outgoing messages receives the message from the hardware bus arbiter. The run-time system translates them to the CAN-protocol, furnishes them with the sender's address and transmits them to the CAN-bus. Due to the short execution time of this unit several messages can be broadcasted each step (see figure 11).

3.3.6. **Optimization of the Message Handling.** If there is an opportunity for taking influence on the definition of the external messages at design time, it will be possible to design messages in a way to minimize the translation effort between internal and external messages.

Additionally it is possible to reduce the reconfiguration overhead by intercepting irrelevant messages which don't influence the function's internal states.

## 4. Results

The first results presented here must be regarded as preliminary since the implementation and integration process of all hardware/software components is currently at its final stage but not completed (see figure 12). So detailed results on performance and its real-time-capabilities are not available at this moment. Although the run-time system and the target hardware architecture are scalable we conceive a first system implementation which offers 8 control-function modules where 4 of them can be made available for parallel execution on FPGA. From




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previous tests we have found an average compression rate of about 60%. We assume a global partial uncompressed bitstream size of 118 kB for every function-module, since this can be seen as an upper limit for all functions. Each function-module can be placed on 4 different locations, so that a total amount of 118kB*0.6*4*8=2266kB Flash-memory will be needed. Depending on the FPGA's type we need additionally 832 kB (XC2V2000) or 1282 kB (XC2V3000) of Flash-memory for the basic FPGA-boot-configuration. The run-time system's binary code which is a part of the MicroBlaze boot-configuration bitstream takes about 6.3 kB whereas tables and variables will consume about 1.8 kB of RAM-memory.

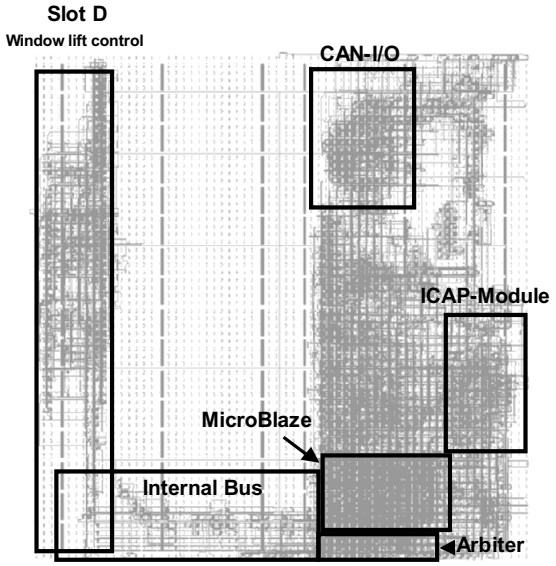


**Figure 12. Implementation on Virtex XC2V2000 FPGA**

**Table 1. Used FPGA Resources**

| | | |
|---|---|---|
| IOBs | 114 | (15 %) |
| Multiplexors | 3 | (3 %) |
| RAM | 16 | (16 %) |
| Slices | 1754 | (12 %) |
| Software Code Size | 1100 lines C-Code<br>eq. 6,3 kB Hex-Code | |
| Mircoblaze Clock | 66 MHz | |
| Internal FPGA Bus Clock | 66 MHz | |

## 5. Conclusions and Future Work

We have presented a first approach for a flexible FPGA-based run-time system for dynamical on- demand reconfiguration which is targeted for less critical automotive control applications supporting resource saving run-time function multiplex. We will have to evaluate the system's behavior on real-time constraints and its performance. Our preliminary results are promising and we intend to improve the system's set of features. For example we conceive a run-time bitstream address conversion so that we have to store only one bitstream image of every function which can be moved at run-time to different FPGA-slots by doing a recalculation of the function's placement address offsets. This improvement will save Flash-memory which can be used for other purposes. Additionally we conceive a linking mechanism to other FPGA-RTS-units so that several FPGA-units offer a set of common services which decreases the failure probability by increasing redundancy.

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